AM62D Sitara® Processors

Technical Reference Manual

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Preface

Read This First

About This Manual

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Related Documentation

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1

Introduction

This chapter introduces the features, subsystems, and architecture of the AM62D Sitara Processor Platform high-performance System-on-Chip (SoC).

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1.1 Overview

1.2 Module Allocation and Instances within Device Domains

Module Full Name	Module Abbreviation	Device Domain		
		MCU	MAIN	WKUP
Quad-Core Arm Cortex A53 Subsystem	A53SS	-	1	-
Single-Core Arm Cortex-R5F Subsystem	R5FSS	1	-	1
Deep Learning Accelerator	C7x MMA	-	1	
Interprocessor Communication - Mailbox	Mailbox	-	1	-
Interprocessor Communication - Spinlock	Spinlock	-	1	-
Dual Data Rate Random Access Memory (32-Bit) Subsystem	DDRSS	-	1	-
Data Movement Subsystem	DMSS	-	1	-
Peripheral DMA	PDMA	-	3	-
General Purpose Input/Output	GPIO	1	2	-
Inter-Integrated Circuit	I2C	1	4	1
Multi-channel Serial Peripheral Interface	MCSPI	2	3	-
Universal Asynchronous Receiver/Transmitter	UART	1	7	1
3 Port Gigabit Ethernet Switch	CPSW	-	1	-
Universal Serial Bus Subsystem	USB	-	2	-
Enhanced Pulse Width Modulation Module	EPWM	-	3	-
Enhanced Quadrature Encoder Pulse Module	EQEP	-	3	-
Enhanced Capture Module	ECAP	-	3	-
Controller Area Network Interface	MCAN	2	1	-
Flash Memory Subsystem	FSS	-	1	-
Octal Serial Peripheral Interface	OSPI	-	1	-
General Purpose Memory Controller	GPMC	-	1	-
Error Location Module	ELM	-	1	-
Multi-Media Card/Secure Digital Interface	MMCSD	-	3	-
Global Time Counter	GTC	-	-	1
Real Time Interrupt/Windowed WatchDog Timer	RTI/WWDT	1	5	1
Dual-Mode Timer	TIMER	4	8	2
Dual Clock Comparator	DCC	2	7	-
Error Signaling Module	ESM	-	1	1
Memory Cyclic Redundancy Check Controller	MCRC	1	1	-
Multi-channel Audio Serial Port	MCASP	-	3	-

1.3 Functional Block Diagram

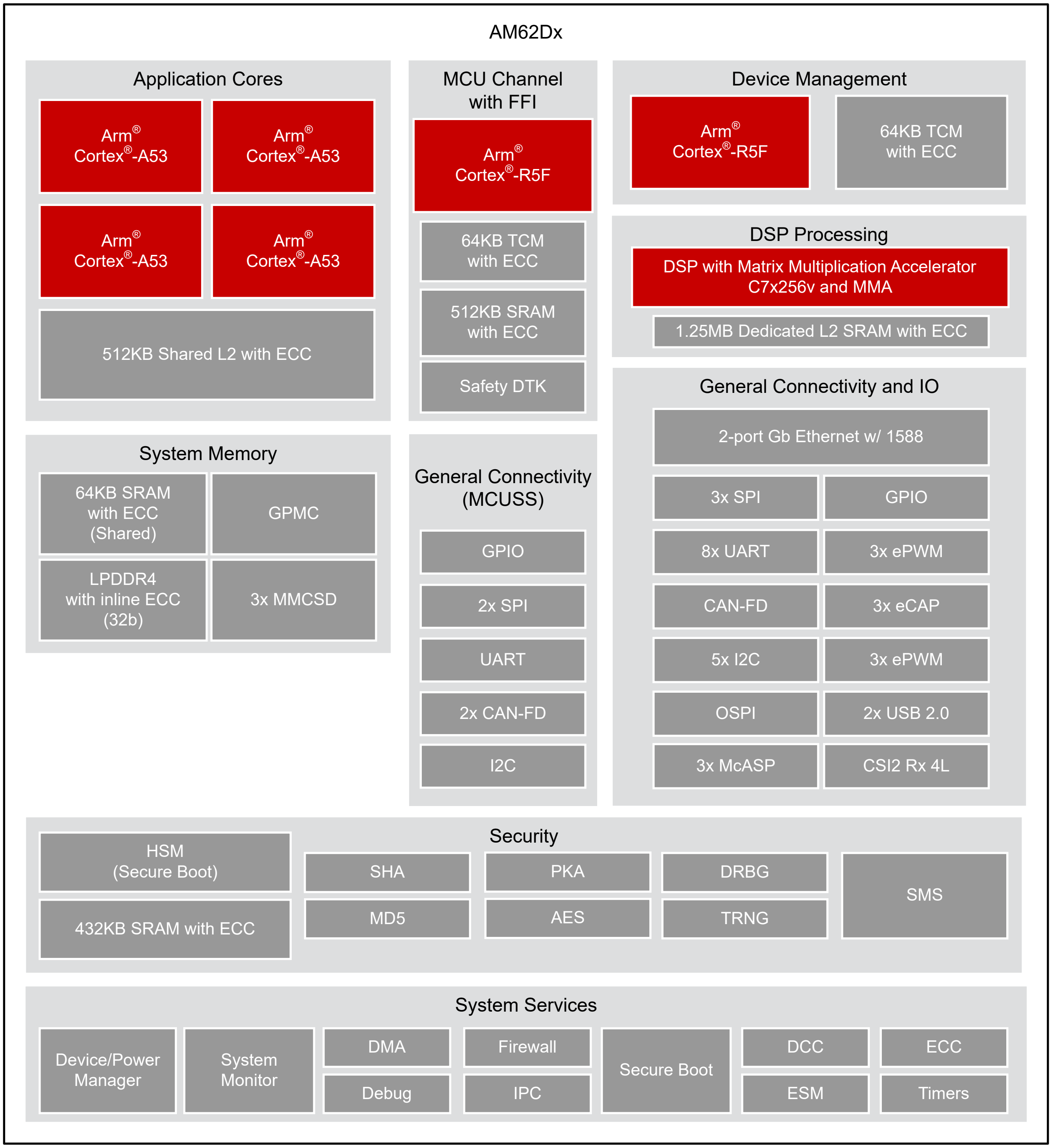

Figure 1-1. Device Block Diagram

1.4 Device MAIN Domain

This section describes the modules integrated in the device MAIN domain.

1.4.1 Arm® Cortex®-A53 Subsystem (A53SS)

The integrated 64-bit Arm® Cortex®-A53 subsystem (A53SS) supports the following main features:

- Up to a quad-core Arm Cortex-A53 MPCore processor with L1 memory system and a single shared L2 cache.
- Full Arm®v8-A architecture compliancy
- Advanced Single Instruction Multiple Data (SIMD) and floating point extension (Arm® Neon™)
- Floating-Point Unit (FPU) VFPv4
- Armv8 Cryptography Extensions
- Arm General Interrupt Controller (GICv3) architecture
- In-order pipeline with symmetric dual-issue of most instructions
- 32KB program and 32KB data Level 1 (L1) Cache
- 512KB shared Level 2 (L2) Cache
- Support for up to four timers within each Cortex-A53 core
- Arm® CoreSight™ Debug and Trace Architecture
- ECC protection for L1 data cache and L2 Cache
- Parity protection for L1 Instruction Cache
- 128-bit wide, synchronous or asynchronous VBUSM initiator interface
- Dedicated RTI windowed watchdog timer per core
- Support for Big-Endian (BE) and Little-Endian (LE) at core level
- Interface with Arm GIC-500 Interrupt Controller (SoC level, not part of A53SS)
- Advanced power management for low power optimization

1.4.2 Deep Learning Accelerator (C7x256v)

- Single Core C7x/MMA subsystem
  - C7x ISA and RISC-V G ISA extensions
    - Vector DSP, 40 GFLOPS
    - 256-bit vector width
    - Deep-learning Matrix Multiply Accelerator (MMA), up to 2 TOPS
  - L1 memory architecture
    - 32KB I-cache
    - 64KB D-cache
  - L2 memory architecture
    - Repurposing of its L2/EL2 embedded memory for use by SOC resources when C7x/MMA/DRU are disabled
    - 1.25MB L2 with ECC protection on L2 SRAM
    - Unified Memory Controller (UMC) facilitates L2 SRAM accesses from CPU and SOC (DMAs) as well as EMIF accesses from CPU.
    - DRU (DMA engine) integrated that facilitates data transfer between L2, VPAC and EMIF.
      - Data compression support
      - Event bus interface integrates with SOC DMSS
      - Tightly coupled with C7x/MMA (DRU is not available for use when the C7x/MMA is disabled)
  - Interrupts
    - Local event controller (CLEC) integrated within CorePac for routing and handling of DRU interrupts, CPU generated IPC events to SOC, interrupts coming from SOC
  - Security
    - Support for C7x Authenticated Boot. Security is in-context during boot to facilitate the authentication and loading of the C7x image.
    - The C7x L2 SRAM (UMC) should not be used for storing security content as there is no protection of UMC memory from C7x itself. In a threat scenario, the C7x can be activated if in reset to execute malicious code to access data in UMC thereby defeating a protection for security data in UMC.
    - No security should be inferred from DRU as this IP is out of scope for security.
    - TrustZone debug controls (DBGEN, NIDEN, SPIDEN, SPNIDEN) are supported
  - Safety
    - Support for reporting safety errors to SOC via interrupt
  - Debug

    - Independent debug interface supporting access to embedded features
    - Debug features include: Core debug, Advanced Event Triggering, Trace, CTSETs, and an embedded CP Tracer Aggregator with bus probes on internal memory interfaces
  - Power Management
    - support for granular gated clock domains to support low power modes and to support memory interface utilization while IP disabled.
  - Advanced SOC Integration
    - Dedicated PLL for full flexibility in performance and power trade-offs
    - Dedicated windowed watchdog timer per core

1.4.3 Mailbox (MAILBOX)

Integrated in MAIN domain: One Mailbox (MAILBOX) module to facilitate the communication between the various on-chip processor cores of the device by providing a queued mailbox-interrupt mechanism with the following main features:

- 1x clusters
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation

1.4.4 Spinlock (SPINLOCK)

One Spinlock module with (256 hardware semaphores) for synchronizing the processes running on multiple cores in the device.

1.4.5 DDR 32-bit Subsystem (DDR32)

Integrated in MAIN domain: One instance of DDR 32-bit Subsystem (DDR32) (also referred to as DDRSS) is used as an interface to external SDRAM devices which can be utilized for storing program or data. The DDRSS provides the following main features:

- Support of LPDDR4 memory type (up to 3733 Mbps)
- 32-bit memory bus interface with in-line ECC
- Up to 8 GB memory address range
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Dynamic change of refresh reach via SW for extended temperatures
- Prioritized refresh scheduling
- Statistical counters for performance management

1.4.6 Data Movement Subsystem (DMSS)

Integrated in the MAIN domain: One Data Movement Subsystem (DMSS) can be used for efficient transfer of data support between software, firmware, and hardware in all combinations. It consists of the following main modules:

- Packet DMA Controller
- Block Copy DMA Controller
- Ring Accelerator provides hardware acceleration to enable straightforward passing of work between a producer and a consumer and has the following main features:
  - Supports up to 20 independent memory-mapped ring structures
  - Supports various modes for each ring based on usage and compatibility
  - Provides single-word deep shared incoming Transfer Response FIFO
  - Provides bit-wide source VBUSM read/write target interface for accesses from DMA controller entities
- Secure proxy module is a modified version of the proxy module and in addition has the following main features:
  - Provides proxy function to store large data bursts that a host can only access in smaller amounts

  - Supports a configurable number of threads, where each has their own independent proxy function
  - Keeps the large data burst coherent until the complete data has been accessed
  - Allows for interleaved access between multiple hosts or tasks using multiple proxy threads
  - Supports a configurable target resource. The target has a configurable number of channels, size of each channel and base address
  - Supports a programmable fixed queue for each proxy thread
  - Supports multiple producers all writing to the same queue
  - Supports programmable thresholds for when to generate events
  - Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
  - Optionally supports dynamic clock gating
- Interrupt Aggregator modules provide a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. Main features are as follows:
  - 64-bit VBUSP target using 64-bit registers
  - Provide a set of TI Interrupt Architecture compliant interrupt status and mask registers which are used to pass specific event status to one or more host blocks.
  - Provides an optional set of Unmapped event (UNMAP) which can take an 'unmapped' event from the ingress ETL and generate a Global event on the egress Event Transport Lane (ETL) interface.
  - Provides an optional set of Global Event Input (GEVI) counters which can count events delivered via an ingress Event Transport Lane (ETL)
  - Provides an optional set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL
  - Provides an optional set of Global Event Input (GEVI) 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on two egress ETL interfaces

1.4.7 General Purpose Input/Output Interface (GPIO)

Integrated in MAIN domain: General Purpose Input/Output (GPIO) module that provide dedicated general-purpose pins that can be configured as either inputs or outputs. The GPIO module main features include:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.4.8 Inter-Integrated Circuit Interface (I2C)

Integrated in MAIN domain: Four instances of the multi-controller Inter-Integrated Circuit (I2C) interface module, each with the following main features:

- 1x Instances with open-drain voltage buffers in compliance with the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- 8-bit-wide data access
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with fixed size of 32 bytes.
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous wake-up mechanisms
- Low power consumption

1.4.9 Serial Peripheral Interface (SPI)

Integrated in MAIN domain: Three instances of the Serial Peripheral Interface (SPI) module with the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receiver mode

- Support for various controller multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

1.4.10 Universal Asynchronous Receiver/Transmitter (UART)

Instances of the configurable Universal Asynchronous Receiver/Transmitter (UART) interface module have the following main features:

- 16C750-compatible interface
- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Baud-rate from 300 bits/s up to 3.6864 Mbits/s with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.4.11 3-port Gigabit Ethernet Switch (CPSW3G)

Integrated in MAIN domain: One instance of the 3-port Gigabit Ethernet Switch (CPSW3G) subsystem provides Ethernet packet communication for the device. The CPSW3G subsystem provides the following main features:

- Two external Ethernet ports with selectable RGMII and RMII interfaces and one internal Communications Port Programming Interface (CPPI) port.
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Support of eight priority level Quality Of Service (QOS) - 802.1p
- Support for Audio/Video Bridging (P802.1Qav/D6.0 and 802.1Qaz)
- Ethernet port reset isolation
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
- Differentiated Services Code Point (DSCP) Priority Mapping (IPv4 and IPv6)
- IPV4/IPV6 UDP/TCP checksum offload
- Priority Based Flow Control (801.1QBB) and Flow Control (802.3x) Support
- Wire rate switching (802.1d)
- Store and Forward Switching
- Non-Blocking switch fabric
- Support of Time Sensitive Network - IEEE P902.3br/D2.0 Interspersing Express Traffic and IEEE 802.1Qbv/D2.2 Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE) with 512 ALE table entries
- EtherStats and 802.3 Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Maximum frame size of 2020 bytes
- Management Data Input/Output (MDIO) module for PHY Management
- Host port CPPI Streaming Packet Interface
- Emulation support

1.4.12 Universal Serial Bus (USB) Subsystem 2.0

Instantiated in MAIN domain: Two instances of the Universal Serial Bus (USB) subsystem with integrated USB2.0 PHY module has the following main features:

- Dual-Role Device (DRD) capability
- Support of Peripheral (aka Device) mode at High Speed (HS at 480 Mbps) and Full Speed (FS at 12 Mbps)
- Support of Host mode at High Speed (HS at 480 Mbps), Full Speed (FS at 12 Mbps), and Low Speed (LS at 1.5 Mbps)
- Support of Host Negotiation Protocol (HNP)

- Support of USB3 low power protocol states (U1, U2, and U3)
- USB instance contains a single xHCI compliant with xHCI 1.0 specification with internal DMA controller
- Embedded USB 2.0 PHY

1.4.13 Enhanced Pulse-Width Modulation Module (EPWM)

Integrated in MAIN domain: Three Enhanced Pulse-Width Modulation (EPWM) modules, each with the following main features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs that can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

1.4.14 Enhanced Quadrature Encoder Pulse Module (EQEP)

Integrated in MAIN domain: Three 32-bit Enhanced Quadrature Encoder Pulse (EQEP) modules for position, speed, and frequency measurements support, each with the following main features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low speed measurement
- Unit time base for speed/frequency measurement
- Watchdog timer for detecting stalls

1.4.15 Enhanced Capture Module (ECAP)

Integrated in MAIN domain: Three Enhanced Capture (ECAP) modules provide accurate timing for different events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output). Each ECAP module supports the following main features:

- 32-bit time base counter
- 4 x 32 bits event time-stamp capture registers
- 4 stage sequencer (Mod4 counter), synchronized to external events
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- Interrupt capabilities on any of the four capture events
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or delta mode time-stamp capture)

1.4.16 Controller Area Network (MCAN)

Integrated in the domain: One Controller Area Network interfaces (MCAN) supporting both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications and having the following main features:

- Conforms with CAN Protocol version 2.0 part A, B and ISO 11898-1:2015
- Full CAN FD (up to 64 data bytes) support
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs, up to 64 elements each
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit event FIFO, up to 32 elements

- Up to 128 filter elements
- Maskable interrupts, two interrupt lines
- Timestamp Counter

1.4.17 Flash Subsystem (FSS) with Octal Serial Peripheral Interface (OSPI)

Integrated in MAIN domain: One instance of the Flash Subsystem (FSS) module provides access to external flash devices via Octal Serial Peripheral Interface (OSPI) along with encryption/decryption and in-line ECC protection. FSS supports the following main features:

- Provides one OSPI flash interfaces
- OSPI interface supports:
  - Execute in place (XIP) operation
  - 32-byte Block Copy (BC) operation
  - ECC
- OSPI supports up to 4 devices
- OSPI supports single, dual, quad, or octal SPI devices
- The OSPI interface has independent power management for low power operations

1.4.18 General Purpose Memory Controller (GPMC)

One instance of the General-Purpose Memory Controller (GPMC) module. The GPMC is dedicated to interfacing with external memory devices and has the following main features:

- Support of 8- or 16-bit-wide data path to external memory devices
- Supports up to 4 independent chip-select regions of programmable size and programmable base addresses on 16MB, 32MB, 64MB, or 128MB boundary in a total address space of 1GB
- Support of the following wide range of external memories/devices:
  - Asynchronous or synchronous 8-bit wide memory or device (non-burst device)
  - Asynchronous or synchronous 16-bit wide memory or device
  - 16-bit non-multiplexed NOR flash device
  - 16-bit address and data multiplexed NOR flash device
  - 8-bit and 16-bit NAND flash device
  - 16-bit pseudo-SRAM (pSRAM) device
- Supports various interface protocols when communicating with external memory or external devices:
  - Asynchronous read/write access
  - Asynchronous read page access (4, 8, and 16 Word16)
  - Synchronous read/write access
  - Synchronous read burst access without wrap capability (4, 8, and 16 Word16)
  - Synchronous read burst access with wrap capability (4, 8, and 16 Word16)
- Supports up to 16-bit on-the-fly error code detection using the Bose-Chaudhuri-Hocquenghem (BCH) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)

1.4.19 Error Location Module (ELM)

One instance of the Error Location Module (ELM). The ELM module works in conjunction with the GPMC and has the following main features:

- ECC calculations (up to 16-bit) for NAND support and ability to work in both page-based and continuous modes
  - 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
  - Eight simultaneous processing contexts
  - Page-based and continuous modes
  - Interrupt generation on error-location process completion

1.4.20 Multi-Media Card/Secure Digital Interface (MMCSD)

Integrated in MAIN domain: Three Multi-Media Card/Secure Digital (MMCSD) controller modules with the following main features:

- One controller with 8-bit wide data bus
- Two with 4-bit wide data bus
- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 3.3/1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 3.3/1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 3.3/1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, SDR104, DDR50

1.4.21 Windowed Watchdog Timer/Real Time Interrupt

- Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Fast enabling/disabling of events

1.4.22 TIMER

- Dual mode Timer (TIMER) module with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2^n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code

1.4.23 Dual Clock Comparator

- Dual Clock Comparator (DCC) modules, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement

1.4.24 Error Signaling Module (ESM)

Error Signaling Module (ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:

- Selectable low and high priority interrupt error pin prioritization of each error event
- Up to 1024 level or pulse error event inputs
- Error signal routed out of device through MCU_ESM error signal
- Configurable time base for error signal
- Error forcing capability

- Internal redundant flops on safety critical fields

1.5 Device MCU Domain

This section describes the modules integrated in the device MCU domain.

Note

In TI documentation, the MCU Domain may be referred to as "MCU Island", "MCU Channel", or "MCU Subsystem".

The Microcontroller Unit Domain (MCU Domain) is a “chip-in-a-chip” concept and it operates using separate clock sources and resets. This allows the MCU Domain to function continuously regardless of the state of the rest of the device, including periods in which the rest of the device is held in reset or powered down. The MCU island integrates communication peripherals such as SPI, I2C, and UART which are expected to be used for safety critical communication, so if the main SoC goes down, the MCU island can communicate this information to the rest of the system.

1.5.1 Arm Cortex-R5F Processor (R5FSS)

The ARM Core Cortex-R5F processor subsystem (R5FSS) supports the following main features:

- Armv7-R architecture
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 32 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces

Note

CORE0 has 64KB of TCM.

Note

These details describe a superset of the R5FSS memory configuration. For additional details on device memory availability, please refer to the device-specific Datasheet.

1.5.2 MCU General Purpose Input/Output Interface (MCU_GPIO)

Integrated in MCU domain: One General Purpose Input/Output (MCU_GPIO) module provides dedicated general-purpose pins that can be configured as either inputs or outputs. the MCU_GPIO module includes these main features:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.5.3 MCU Inter-Integrated Circuit Interface (MCU_I2C)

Integrated in MCU domain:One multi-controller Inter-Integrated Circuit (MCU_I2C) interface with the following main features:

- Compliancy to the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with programmable size of 8 to 64 bytes for buffered read or write
- 8-bit-wide data access
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous Wakeup mechanisms
- Low power consumption

1.5.4 MCU Multi-channel Serial Peripheral Interface (MCU_SPI)

Integrated in MCU domain: Two Multi-channel Serial Peripheral Interface (MCU_SPI) modules where each have the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in receiver mode
- Support of different controller multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

1.5.5 MCU Universal Asynchronous Receiver/Transmitter (MCU_UART)

Integrated in MCU domain: One configurable Universal Asynchronous Receiver/Transmitter (MCU_UART) interface with the following main features:

- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- 16C750 compatible interface
- Baud rates up to 3.6 Mbps with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.5.6 MCU Windowed Watchdog Timer/Real Time Interrupt

- Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Windowed Watchdog Timer (WWDT) feature
  - Some RTI modules are pre-dedicated to specific processor cores

1.5.7 MCU TIMER

- Timer modules with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code
  - Each odd numbered timer instance may be optionally cascaded with the previous even numbered timer instance to form up to a 64-bit timer

1.5.8 MCU Dual Clock Comparator

- The Dual Clock Comparator (MCU_DCC) module, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement

1.5.9 MCU Memory Cyclic Redundancy Check

- Memory Cyclic Redundancy Check module used to perform CRC to verify the integrity of a memory system. The MCRC module has the following main feature:
  - Four Channels of CRC Compression based Signature Generation
  - 8, 16, 32, or 64-bit Data Size
  - Maximum Length PSA based on 64-bit Polynomial
  - Programmable 20 bit pattern counter per channel
  - Three Operating Modes: Auto, Semi-CPU, Full CPU
  - MCRC or CPU can perform signature verification for each Channel
  - Timeout Interrupt if CRC is not performed within the time limit

1.6 Device WKUP Domain

This section describes the modules integrated in the device WKUP domain.

1.6.1 Arm Cortex-R5F Processor (R5FSS)

The ARM Core Cortex-R5F processor subsystem (R5FSS) supports the following main features:

- Armv7-R architecture
- R5FSS Memory System

  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 32 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts

  - Synchronous clock domain crossing on all core interfaces

Note

CORE0 has 64KB of TCM.

Note

These details describe a superset of the R5FSS memory configuration. For additional details on device memory availability, please refer to the device-specific Datasheet.

1.6.2 Inter-Integrated Circuit Interface (I2C)

Multi-controller Inter-Integrated Circuit (I2C) interface module, with the following main features:

- 1x Instances with open-drain voltage buffers in compliance with the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- 8-bit-wide data access
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with fixed size of 32 bytes.
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous wake-up mechanisms
- Low power consumption

1.6.3 Universal Asynchronous Receiver/Transmitter (UART)

Instances of the configurable Universal Asynchronous Receiver/Transmitter (UART) interface module have the following main features:

- 16C750-compatible interface
- Support of RS-485 external transceiver auto flow control

- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Baud-rate from 300 bits/s up to 3.6864 Mbits/s with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.6.4 MCU Error Signaling Module

- Error Signaling Module (MCU_ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:
  - Up to 1024 level or pulse error event inputs
  - Selectable low and high priority interrupt error pin prioritization of each error event
  - Single Error Pin output to signal severe device failure to outside world
  - Configurable time base for error signal
  - Triple Redundant Pulse Inputs
  - Two Priority Levels
  - Error Forcing capability
  - Internal redundant flops on safety critical fields

1.6.5 Global Time Counter

- Global Time Counter (GTC) module that can be used for time synchronization and debug trace time stamping with the following main features:
  - 64-bit up counter
  - No rollover during the lifetime of the device
  - Compatible with Armv8 system counter requirements
  - Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
  - Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols

1.6.6 MCU Windowed Watchdog Timer/Real Time Interrupt

- Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Windowed Watchdog Timer (WWDT) feature
  - Some RTI modules are pre-dedicated to specific processor cores

1.6.7 MCU TIMER

- Timer modules with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code
  - Each odd numbered timer instance may be optionally cascaded with the previous even numbered timer instance to form up to a 64-bit timer

1.7 Device Identification

The device part number identification data can be read in the WKUP_CTRL_MMR_CFG0_JTAG_USER_ID register. See Table 1-1 for more information.

Table 1-1. Device Part Number Identifier

WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register Field	Value and Description	Comment
[31-13] DEVICE_ID	Base Part Number.	Refer to the Device Comparison table in the device specific datasheet for the combined DEVICE_ID and FEATURES value of a given part number
[12] SAFETY	0 = Non Functional Safety 1 = Functional Safety	
[11] SECURITY	0 = Non-Secure 1 = Secure	
[10-6] SPEED	Device Speed Grade. 16 (0x10) = P speed designator 18 (0x12) = R speed designator 20 (0x14) = V speed designator	Refer to the device-specific Datasheet for the supported speed grades and the definitions for a given device.
[5-3] TEMP	Temperature grade. 4 = -40°C to 105°C 5 = -40°C to 125°C Others = Reserved	Operating junction temperature range.
[2-0] PKG	Package 6 = ANF Others = Reserved	Device Package type.

The manufacturer identity, the boundary scan part number, and the silicon revision of the device can be read in the WKUP_CTRL_MMR_CFG0_JTAGID register. See Table 1-2 and Table 1-3 tables for more information.

Table 1-2. Device JTAG ID

WKUP_CTRL_MMR_CFG0_JTAGID Register Field	Value	Comment
[31-28] VARIANT	See Table 1-3	Silicon Revision (SR) identifier.
[27-12] PARTNO	See Table 1-3	Part number for boundary scan.
[11-1] MFG	0x17	Manufacturer identity (TI).
[0] LSB	0x1	Always reads 1.

Table 1-3. Device JTAG ID Values

Silicon Type	VARIANT	PARTNO	WKUP_CTRL_MMR_CFG0_JTAGID Register Value
AM62Dx SR1.0	0x0	0xBB8D	0x0BB8 D02F

Chapter 2

Memory Map

2.1 AM62D Memory Map

AM62D SoC level memory map is constructed using 36b physical address and follows the guideline to put peripheral at 64KB aligned boundary. No virtual address is supported on the SoC level. However, A53 core can support virtual address internally. If software utilizes the address more than 36b, only the lower 36b is used for SoC level address decoding and the upper address bits will be ignored by the SoC. Not all the 36b memory regions are implemented by AM62D. Any transactions hitting the unimplemented address range will be terminated and routed to null end point to avoid system hang. An interrupt will be asserted and the above transaction will be logged.

All the SoC level peripherals and processors use the common SoC memory except the 32b only processors, such as the R5 core. For those processors and peripherals which natively only supports 32b physical address, the Region based Address Translation (RAT) module is used to remap the 32b address into the common 36b SoC address map.

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2.1.1 Processor Memory Map View

Since AM62D is built on 36b physical address, there are memory regions beyond 4GB address, such as DDR data space and debug configuration space. This is not a problem for the ARM V8 core such as A53, since it supports up to 44b physical address. However, the R5 processors natively support only a 32b physical address space. In order to allow these micro controllers accessing the full 36b physical address space, a region based remapping module is dedicated for each processor.

2.1.1.1 A53 Memory View

All the A53 cores use the common 36b SoC memory map shown in Memory Map Summary for their physical address map. Since A53 natively supports up to 44b physical address, if A53 issues any transaction with non-zero upper 8 physical address bits, those upper 8 address bits are ignored by SoC address decoding logic.

Sitara's SoC memory map is constructed to allow software utilizing bigger MMU page. The majority of the peripherals are put at 64KB aligned boundary. This is to allow A53 software to use 64KB MMU page to manage individual peripherals instead of using 4KB MMU page. There are a few exceptions.

Main domain GPIO is implemented by using two GPIO modules. However, these two GPIO modules are placed together. Software needs to manage two GPIO modules using a single MMU page. Since each GPIO pin is managed by a single bit inside GPIO registers, there is no virtual machine or OS isolation implemented.

The SoC also contains multiple DCC modules that are located at 4KB boundaries instead of 64KB. The A53 software can still use 64KB MMU page to manage these DCC modules. If any of the DCC needs to be allocated for other processors, the region-based firewall can provide the additional isolation needed. The firewall boundary granularity is 4KB, which allows each DDC to be assigned individually.

Firewall, QoS, ISC configurations are not on 64KB boundary. And each individual firewall module, QoS module, and ISC module is placed at 1KB boundaries.

2.1.1.2 MCU R5F Memory View

AM62D has one single R5F core in the wakeup domain. The R5F is a native 32b processor, which the R5F core itself can only generate transactions using 32b address. A dedicated RAT module is integrated for this single core R5F to allow the R5F software to remap the 32b R5F address into the common 36b SoC address.

In addition, the R5F core has its own TCM, which the R5F core can access with its TCM with a single R5F core cycle. Those TCM memories have two sets of address, one set address is used for the R5F core for a single cycle access to those TCM. The second set of address is used by other initiators outside this R5F subsystem to access those TCM. The R5F core shall always use the first set of address to access its TCM. If the R5F core utilizes the second set of address to those TCM, the R5F core will receives an exception, since those transactions will be routed to be terminated by sending them to the null end point.

While the SoC level address for TCM is fixed, the address used by the R5F to access to its own TCM can be remapped by software. By default, AM62D puts the R5F's ATCM at address 0x0 and the BTCM address at 0x4101_0000.

The R5F also has one section of the region dedicated for peripheral access from address 0x0400_0000 to 0x07FF_FFFF. This memory region is treated as normally memory, which can't be cached. The R5F accesses this memory region through a dedicated single-issue interface, and none of the transactions accessing this memory region can be remapped by using RAT module.

The R5F core accesses its own ATCM and BTCM memory directly, and there is no address remapping for those access. All the other access than ATCM, BTCM and address range 0x0400_0000 to 0x07FF_FFFF from the R5F core go through RAT module, which could be remapped into different address to access the rest of the SoC using the common 36b SoC memory map.

Table 2-1. MCU R5F Memory Map

Base Address	Size	Memory Region	Additional Note
0000_0000	32KB	ATCM	The R5F can re-map its ATCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function.
0000_8000	64MB-32KB	RAT_region0	
0400_0000	64M-128K	Non_RAT region	
07FE_0000	4K	RAT_CFG	This is within the non_RAT region
07FF_0000	16K	VIM_CFG	This is within the non_RAT region
0800_0000	912MB+64KB	RAT_region1	
4101_0000	32KB	BTCM	The R5F can re-map its BTCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function.
4101_8000	1GB-16480K	RAT_Region2	
8000_0000	2GB	RAT_Region3	

The common SoC memory map assigns the R5F’s ATCM and BTCM to address 0x7900_0000 and 0x7902_0000. The R5F software can optionally reprogram the its internal ATCM and BTCM address to match the address assigned by the common SoC memory map as well. Regardless where the R5F puts its own ATCM and BTCM, the R5F accesses its own ATCM and BTCM directly without going through RAT.

ATCM is by default disabled at address 0x0. BTCM is by default enabled and the default address for BTCM is 0x4101_0000. The base address of VIM is at 0x07FF_0000 and the base address for RAT configuration is at 0x07FE_0000.

All the R5F transactions can go through RAT for address re-mapping function except the transactions targeted to address range 0x0400_0000 to 0x07FF_FFFF and its own ATCM and BTCM. It is highly recommended only remap the R5F’s address range from 0x8000_0000 to 0xFFFF_FFFF to access the target region located at the common memory map between 0x8000_0000 and 0xF_FFFF_FFFF.

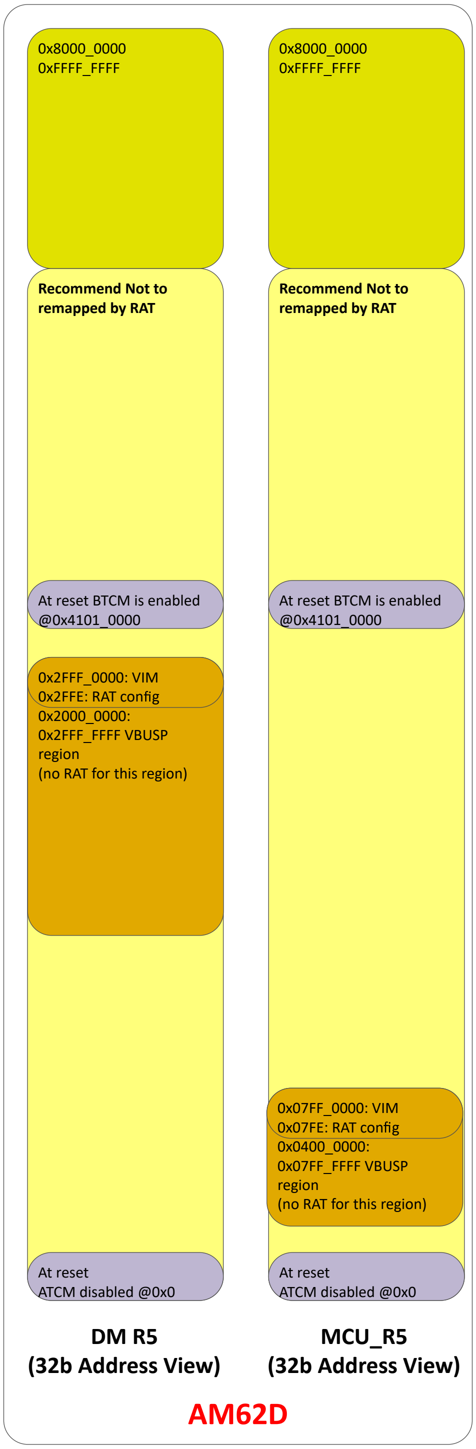

Figure 2-1. MCU and Device Manager R5F Memory Map View

2.1.1.3 Device Manager R5F Memory View

AM62D has one single R5F core in the wakeup domain. The R5F is a native 32b processor, which the R5F core itself can only generate transactions using 32b address. A dedicated RAT module is integrated for this single core R5F to allow the R5F software to remap the 32b R5F address into the common 36b SoC address.

In addition, the R5F core has its own TCM, which the R5F core can access with its TCM with a single R5F core cycle. Those TCM memories have two sets of address, one set address is used for the R5F core for a single cycle access to those TCM. The second set of address is used by other initiators outside this R5F subsystem to access those TCM. The R5F core shall always uses the first set of address to access its TCM. If the R5F core utilizes the second set of address to those TCM, the R5F core will receives an exception, since those transactions will be routed to be terminated by sending them to the null end point.

While the SoC level address for TCM is fixed, the address used by the R5F to access to its own TCM can be remapped by software. By default, AM62D puts the R5F's ATCM at address 0x0 and the BTCM address at 0x4101_0000.

The R5F also has one section of the region dedicated for peripheral access from address 0x2000_0000 to 0x2FFF_FFFF. This memory region is treated as normally memory, which can't be cached. The R5F accesses this memory region through a dedicated single-issue interface, and none of the transactions accessing this memory region can be remapped by using RAT module.

The R5F core accesses its own ATCM and BTCM memory directly, and there is no address remapping for those access. All the other access than ATCM, BTCM and address range 0x2000_0000 to 0x2FFF_FFFF from the R5F core go through RAT module, which could be remapped into different address to access the rest of the SoC using the common 36b SoC memory map.

Table 2-2. Device Manager R5F 32b Address Map View (Default)

Base address	Size	Memory Region	Additional Note
0000_0000	32KB	ATCM	The R5F can re-map its ATCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function.
0000_8000	512M-32K	RAT_region0	
2000_0000	256MB-128K	Non_RAT region	
2FFE_0000	4K	RAT_CFG	This is within the non_RAT region
2FFF_0000	16K	VIM_CFG	This is within the non_RAT region
3000_0000	273M-960K	RAT_region1	
4101_0000	32KB	BTCM	The R5F can re-map its BTCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function.
4101_8000	1GB-16480K	RAT_Region2	
8000_0000	2GB	RAT_Region3	

The common SoC memory map assigns the R5F's ATCM and BTCM to address 0x7800_0000 and 0x7810_0000. The R5F software can optionally reprogram the its internal ATCM and BTCM address to match the address assigned by the common SoC memory map as well. Regardless where the R5F puts its own ATCM and BTCM, the R5F accesses its own ATCM and BTCM directly without going through RAT.

ATCM is by default disabled at address 0x0. BTCM is by default enabled and the default address for BTCM is 0x4101_0000. The base address of VIM is at 0x2FFF_0000 and the base address for RAT configuration is at 0x2FFE_0000.

All the R5F transactions can go through RAT for address re-mapping function except the transactions targeted to address range 0x2000_0000 to 0x2FFF_FFFF and its own ATCM and BTCM. It is highly recommended only remap the R5F's address range from 0x8000_0000 to 0xFFFF_FFFF to access the target region located at the common memory map between 0x8000_0000 and 0xF_FFFF_FFFF.

2.1.2 DDR Memory Region

AM62D includes two DDR data regions: 2GB at 0x8000_0000 and 30GB at 0x8_8000_0000.

2.1.3 MMU Optimization Note

The SoC memory map is constructed to enable using MMU granule sizes of 64KB and above by placing most of the system resources on a 64KB address boundary. This also enables isolation of resources and peripherals from individual software processes through unique MMU entries.

The following is a non-exhaustive list of exceptions to this alignment rule:

- Debug SS
- MAIN GPIO0/GPIO1, MCU GPIO
- DCC
- ISC, QOS, Firewall

Resources and peripherals excluded from the 64KB addressing placement are either meant to have a single owner or are logically the same function (such as GPIO).

2.1.4 Memory Map Summary

Since different type of the processors have different memory map views, this section provides a summary on how each type of processor and initiator access various target end points within the SoC.

2.1.4.1 MAIN Memory Map

Table 2-3. MAIN Memory Map

Region Name	Start Address	End Address	Size
PSRAMECC0_RAM	0x0000000000	0x00000003FF	1KB
PADCFG_CTRL0_CFG0	0x00000F0000	0x00000F7FFF	32KB
CTRL_MMR0_CFG0	0x0000100000	0x000011FFFF	128KB
CBASS_DBG0_ERR	0x0000200000	0x00002003FF	1KB
CBASS_INFRA1_ERR	0x0000210000	0x00002103FF	1KB
CBASS_FW0_ERR	0x0000220000	0x00002203FF	1KB
CBASS_IPCSS0_ERR	0x0000230000	0x00002303FF	1KB
CBASS_MCASP0_ERR	0x0000240000	0x00002403FF	1KB
EFUSE0	0x0000300000	0x00003000FF	256B
COMPUTE_CLUSTER0_PBIST	0x0000330000	0x00003303FF	1KB
C7X256V0_PBIST	0x0000360000	0x00003603FF	1KB
PSCSS0_PSC	0x0000400000	0x0000400FFF	4KB
PLLCTRL0	0x0000410000	0x00004101FF	512B
ESM0_CFG	0x0000420000	0x0000420FFF	4KB
DFTSS0	0x0000500000	0x00005003FF	1KB
DDPA0	0x0000580000	0x00005803FF	1KB
GPIO0	0x0000600000	0x00006000FF	256B
GPIO1	0x0000601000	0x00006010FF	256B
PLL0_CFG	0x0000680000	0x000069FFFF	128KB
PSRAMECC0_ECC_AGGR	0x0000700000	0x00007003FF	1KB
PSCSS0_REGS	0x0000700400	0x00007007FF	1KB
PSRAMECC1_ECC_AGGR	0x0000701000	0x00007013FF	1KB
USB0_DEBUG_TRACE_MMR_TRACE_VBUSP_USB2SS_DEBUG_TRACE	0x0000703000	0x00007031FF	512B
CPSW0_ECC	0x0000704000	0x00007043FF	1KB
MMCSD0_ECC_AGGR_RXMEM	0x0000706000	0x00007063FF	1KB
MMCSD0_ECC_AGGR_TXMEM	0x0000707000	0x00007073FF	1KB
MMCSD1_ECC_AGGR_RXMEM	0x0000708000	0x00007083FF	1KB
MMCSD1_ECC_AGGR_TXMEM	0x0000709000	0x00007093FF	1KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MMCSD2_ECC_AGGR_TXMEM	0x000070A000	0x000070A3FF	1KB
MMCSD2_ECC_AGGR_RXMEM	0x000070B000	0x000070B3FF	1KB
USB1_DEBUG_TRACE_MMR_TRACE_VBUSP_USB2SS_DEBUG_TRACE	0x000070C000	0x000070C1FF	512B
MSRAM_64K0_ECC_AGGR_REGS	0x0000710000	0x00007103FF	1KB
SA3_SS0_ECC_AGGR	0x0000712000	0x00007123FF	1KB
FSS0_OSPI0_ECC_AGGR	0x0000716000	0x00007163FF	1KB
COMPUTE_CLUSTER0_SS_ECC_AGGR	0x0000718000	0x00007183FF	1KB
COMPUTE_CLUSTER0_CORE0_ECC_AGGR	0x0000718400	0x00007187FF	1KB
COMPUTE_CLUSTER0_CORE1_ECC_AGGR	0x0000718800	0x0000718BFF	1KB
COMPUTE_CLUSTER0_CORE2_ECC_AGGR	0x0000718C00	0x0000718FFF	1KB
COMPUTE_CLUSTER0_CORE3_ECC_AGGR	0x0000719000	0x00007193FF	1KB
C7X256V0_ECC_AGGR	0x000071A000	0x000071A3FF	1KB
DCC0	0x0000800000	0x000080003F	64B
DCC1	0x0000804000	0x000080403F	64B
DCC2	0x0000808000	0x000080803F	64B
DCC3	0x000080C000	0x000080C03F	64B
DCC4	0x0000810000	0x000081003F	64B
DCC5	0x0000814000	0x000081403F	64B
DCC6	0x0000818000	0x000081803F	64B
PSRAMECC1_RAM	0x0000900000	0x00009003FF	1KB
MAIN_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0000A00000	0x0000A007FF	2KB
CMP_EVENT_INTROUTER0_INTR_ROUTER_CFG	0x0000A30000	0x0000A307FF	2KB
TIMESYNC_EVENT_ROUTER0_INTR_ROUTER_CFG	0x0000A40000	0x0000A403FF	1KB
WKUP_GTC0_CFG0	0x0000A80000	0x0000A803FF	1KB
WKUP_GTC0_CFG1	0x0000A90000	0x0000A93FFF	16KB
WKUP_GTC0_CFG2	0x0000AA0000	0x0000AA3FFF	16KB
WKUP_GTC0_CFG3	0x0000AB0000	0x0000AB3FFF	16KB
WKUP_VTM0_VTM_CFG1	0x0000B00000	0x0000B003FF	1KB
WKUP_VTM0_VTM_CFG2	0x0000B01000	0x0000B013FF	1KB
WKUP_VTM0_ECCAGGR_CFG	0x0000B02000	0x0000B023FF	1KB
PDMA0	0x0000C00000	0x0000C003FF	1KB
PDMA1	0x0000C01000	0x0000C013FF	1KB
GICSS0_GIC_TRANSLATER	0x0001000000	0x00013FFFFF	4MB
GICSS0_GIC	0x0001800000	0x00018FFFFF	1MB
TIMER0_CFG	0x0002400000	0x00024003FF	1KB
TIMER1_CFG	0x0002410000	0x00024103FF	1KB
TIMER2_CFG	0x0002420000	0x00024203FF	1KB
TIMER3_CFG	0x0002430000	0x00024303FF	1KB
TIMER4_CFG	0x0002440000	0x00024403FF	1KB
TIMER5_CFG	0x0002450000	0x00024503FF	1KB
TIMER6_CFG	0x0002460000	0x00024603FF	1KB
TIMER7_CFG	0x0002470000	0x00024703FF	1KB
UART0	0x0002800000	0x00028001FF	512B
UART1	0x0002810000	0x00028101FF	512B
UART2	0x0002820000	0x00028201FF	512B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
UART3	0x0002830000	0x00028301FF	512B
UART4	0x0002840000	0x00028401FF	512B
UART5	0x0002850000	0x00028501FF	512B
UART6	0x0002860000	0x00028601FF	512B
MCASP0_CFG	0x0002B00000	0x0002B01FFF	8KB
MCASP0_DMA	0x0002B08000	0x0002B083FF	1KB
MCASP1_CFG	0x0002B10000	0x0002B11FFF	8KB
MCASP1_DMA	0x0002B18000	0x0002B183FF	1KB
MCASP2_CFG	0x0002B20000	0x0002B21FFF	8KB
MCASP2_DMA	0x0002B28000	0x0002B283FF	1KB
WKUP_PSC0_PSC	0x0004000000	0x0004000FFF	4KB
MCU_PLLCTRL0	0x0004020000	0x00040201FF	512B
WKUP_ECC_AGGR2_ECC_AGGR	0x0004030000	0x00040303FF	1KB
WKUP_PLL0_CFG	0x0004040000	0x0004040FFF	4KB
MCU_PADCFG_CTRL0_CFG0	0x0004080000	0x0004087FFF	32KB
WKUP_ESM0_CFG	0x0004100000	0x0004100FFF	4KB
MCU_GPIO0	0x0004201000	0x00042010FF	256B
WKUP_MCU_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0004210000	0x00042101FF	512B
MCU_TIMEOUT0_CFG	0x0004301000	0x00043013FF	1KB
MCU_R5FSS0_EVNT_BUS_VBUSP_MMRS	0x0004400000	0x00044000FF	256B
MCU_CTRL_MMR0_CFG0	0x0004500000	0x000451FFFF	128KB
WKUP_CBASS_SAFE1_ERR	0x0004600000	0x00046003FF	1KB
MCU_MCAN0_ECC_AGGR	0x0004701000	0x00047013FF	1KB
MCU_MCAN1_ECC_AGGR	0x0004702000	0x00047023FF	1KB
MCU_ECC_AGGR0_ECC_AGGR	0x0004703000	0x00047033FF	1KB
MCU_ECC_AGGR1_ECC_AGGR	0x0004704000	0x00047043FF	1KB
MCU_MSRAM_256K0_ECC_AGGR_REGS	0x0004705000	0x00047053FF	1KB
MCU_MSRAM_256K1_ECC_AGGR_REGS	0x0004706000	0x00047063FF	1KB
MCU_R5FSS0_CORE0_ECC_AGGR	0x0004707000	0x00047073FF	1KB
MCU_CBASS0_ERR	0x0004720000	0x00047203FF	1KB
MCU_TIMER0_CFG	0x0004800000	0x00048003FF	1KB
MCU_TIMER1_CFG	0x0004810000	0x00048103FF	1KB
MCU_TIMER2_CFG	0x0004820000	0x00048203FF	1KB
MCU_TIMER3_CFG	0x0004830000	0x00048303FF	1KB
MCU_RTI0_CFG	0x0004880000	0x00048800FF	256B
MCU_I2C0_CFG	0x0004900000	0x00049000FF	256B
MCU_UART0	0x0004A00000	0x0004A001FF	512B
MCU_MCSPI0_CFG	0x0004B00000	0x0004B003FF	1KB
MCU_MCSPI1_CFG	0x0004B10000	0x0004B103FF	1KB
MCU_DCC0	0x0004C00000	0x0004C0003F	64B
MCU_DCC1	0x0004C10000	0x0004C1003F	64B
MCU_MCRC64_0_REGS	0x0004D00000	0x0004D00FFF	4KB
MCU_MCAN0_MSGMEM_RAM	0x0004E00000	0x0004E07FFF	32KB
MCU_MCAN0_CFG	0x0004E08000	0x0004E081FF	512B
MCU_MCAN0_SS	0x0004E09000	0x0004E090FF	256B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MCU_MCAN1_MSGMEM_RAM	0x0004E10000	0x0004E17FFF	32KB
MCU_MCAN1_CFG	0x0004E18000	0x0004E181FF	512B
MCU_MCAN1_SS	0x0004E19000	0x0004E190FF	256B
MCU_PBIST0	0x0004F00000	0x0004F003FF	1KB
CPSW0_NUSS	0x0008000000	0x00081FFFFF	2MB
RTI0_CFG	0x000E000000	0x000E0000FF	256B
RTI1_CFG	0x000E010000	0x000E0100FF	256B
RTI2_CFG	0x000E020000	0x000E0200FF	256B
RTI3_CFG	0x000E030000	0x000E0300FF	256B
RTI4_CFG	0x000E040000	0x000E0400FF	256B
DDR32SS0_REGS_SS_CFG_SSCFG	0x000F300000	0x000F3001FF	512B
DDR32SS0_CTLPHY_WRAP_CTL_CFG_CTLCFG	0x000F308000	0x000F30FFFF	32KB
USB0_MMR_MMRVBP_USB2SS_CFG	0x000F900000	0x000F9007FF	2KB
USB0_PHY2	0x000F908000	0x000F9083FF	1KB
USB1_MMR_MMRVBP_USB2SS_CFG	0x000F910000	0x000F9107FF	2KB
USB1_PHY2	0x000F918000	0x000F9183FF	1KB
USB0_ECC_AGGR	0x000F980000	0x000F9803FF	1KB
USB1_ECC_AGGR	0x000F990000	0x000F9903FF	1KB
MMCSD1_CTL_CFG	0x000FA00000	0x000FA00FFF	4KB
MMCSD1_SS_CFG	0x000FA08000	0x000FA083FF	1KB
MMCSD0_CTL_CFG	0x000FA10000	0x000FA10FFF	4KB
MMCSD0_SS_CFG	0x000FA18000	0x000FA183FF	1KB
MMCSD2_CTL_CFG	0x000FA20000	0x000FA20FFF	4KB
MMCSD2_SS_CFG	0x000FA28000	0x000FA283FF	1KB
FSS0_CFG	0x000FC00000	0x000FC000FF	256B
FSS0_FSAS_CFG	0x000FC10000	0x000FC100FF	256B
FSS0_OTFA_CFG	0x000FC20000	0x000FC20FFF	4KB
FSS0_OSPI0_CTRL	0x000FC40000	0x000FC400FF	256B
FSS0_OSPI0_SS_CFG	0x000FC44000	0x000FC441FF	512B
I2C0_CFG	0x0020000000	0x00200000FF	256B
I2C1_CFG	0x0020010000	0x00200100FF	256B
I2C2_CFG	0x0020020000	0x00200200FF	256B
I2C3_CFG	0x0020030000	0x00200300FF	256B
MCSPI0_CFG	0x0020100000	0x00201003FF	1KB
MCSPI1_CFG	0x0020110000	0x00201103FF	1KB
MCSPI2_CFG	0x0020120000	0x00201203FF	1KB
CBASS_MISC_PERI0_ERR	0x00201F0000	0x00201F03FF	1KB
MCAN0_SS	0x0020700000	0x00207000FF	256B
MCAN0_CFG	0x0020701000	0x00207011FF	512B
MCAN0_MSGMEM_RAM	0x0020708000	0x002070FFFF	32KB
EPWM0_EPWM	0x0023000000	0x00230000FF	256B
EPWM1_EPWM	0x0023010000	0x00230100FF	256B
EPWM2_EPWM	0x0023020000	0x00230200FF	256B
ECAP0_CTL_STS	0x0023100000	0x00231000FF	256B
ECAP1_CTL_STS	0x0023110000	0x00231100FF	256B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
ECAP2_CTL_STS	0x0023120000	0x00231200FF	256B
EQEP0_REG	0x0023200000	0x00232000FF	256B
EQEP1_REG	0x0023210000	0x00232100FF	256B
EQEP2_REG	0x0023220000	0x00232200FF	256B
MCAN0_ECC_AGGR	0x0024018000	0x00240183FF	1KB
ELM0	0x0025010000	0x0025010FFF	4KB
MAILBOX0_REGS0	0x0029000000	0x00290001FF	512B
MAILBOX0_REGS1	0x0029010000	0x00290101FF	512B
MAILBOX0_REGS2	0x0029020000	0x00290201FF	512B
MAILBOX0_REGS3	0x0029030000	0x00290301FF	512B
SPINLOCK0	0x002A000000	0x002A007FFF	32KB
WKUP_RTI0_CFG	0x002B000000	0x002B0000FF	256B
WKUP_TIMER0_CFG	0x002B100000	0x002B1003FF	1KB
WKUP_TIMER1_CFG	0x002B110000	0x002B1103FF	1KB
WKUP_RTCSS0_RTC	0x002B1F0000	0x002B1F007F	128B
WKUP_I2C0_CFG	0x002B200000	0x002B2000FF	256B
WKUP_UART0	0x002B300000	0x002B3001FF	512B
WKUP_CBASS0_ERR	0x002B400000	0x002B4003FF	1KB
WKUP_PBIST0	0x002B500000	0x002B5003FF	1KB
WKUP_PBIST1	0x002B510000	0x002B5103FF	1KB
WKUP_ECC_AGGR0_ECC_AGGR	0x002B600000	0x002B6003FF	1KB
WKUP_ECC_AGGR1_ECC_AGGR	0x002B601000	0x002B6013FF	1KB
WKUP_PSRAMECC_8K0_REGS	0x002B608000	0x002B6083FF	1KB
DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX	0x0030110000	0x0030110FFF	4KB
DPHY_RX0_MMR_SLV_K3_DPHY_WRAP	0x0030111000	0x00301110FF	256B
C7X256V0	0x0030240000	0x003024FFFF	64KB
MCRC64_0_REGS	0x0030300000	0x0030300FFF	4KB
A53_WS_BW_LIMITER1_REGS	0x0030402000	0x0030402FFF	4KB
A53_RS_BW_LIMITER0_REGS	0x0030403000	0x0030403FFF	4KB
JPGENC_RS_BW_LIMITER4_REGS	0x0030404000	0x0030404FFF	4KB
JPGENC_WS_BW_LIMITER5_REGS	0x0030405000	0x0030405FFF	4KB
C7XV_RSWS_BS_LIMITER6_REGS	0x0030406000	0x0030406FFF	4KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_CAP	0x0031000000	0x003100001F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_OPER	0x0031000020	0x003100005F	64B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_PORT	0x0031000420	0x003100043F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_RUNTIME	0x0031000440	0x003100045F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_INTR	0x0031000460	0x003100049F	64B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DB	0x0031000560	0x003100075F	512B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_EXTCAP	0x0031000960	0x003100096F	16B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP2	0x0031000970	0x003100097F	16B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP3	0x0031000980	0x003100099F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_GBL	0x003100C100	0x003100C8FF	2KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEV	0x003100C700	0x003100CEFF	2KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_LINK	0x003100D000	0x003100D07F	128B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG	0x003100D800	0x003100D9FF	512B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG_RAM0	0x0031040000	0x003104FFFF	64KB
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_CAP	0x0031100000	0x003110001F	32B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_OPER	0x0031100020	0x003110005F	64B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_PORT	0x0031100420	0x003110043F	32B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_RUNTIME	0x0031100440	0x003110045F	32B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_INTR	0x0031100460	0x003110049F	64B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DB	0x0031100560	0x003110075F	512B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_EXTCAP	0x0031100960	0x003110096F	16B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP2	0x0031100970	0x003110097F	16B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP3	0x0031100980	0x003110099F	32B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_GBL	0x003110C100	0x003110C8FF	2KB
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEV	0x003110C700	0x003110CEFF	2KB
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_LINK	0x003110D000	0x003110D07F	128B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG	0x003110D800	0x003110D9FF	512B
USB1_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG_RAM0	0x0031140000	0x003114FFFF	64KB
CBASS0_ERR	0x003A000000	0x003A0003FF	1KB
GPMC0_CFG	0x003B000000	0x003B0003FF	1KB
WKUP_R5FSS0_EVNT_BUS_VBUSP_MMRS	0x003C018000	0x003C0180FF	256B
GICSS0_REGS	0x003F004000	0x003F0043FF	1KB
DMASS0_ECCAGGR	0x003F005000	0x003F0053FF	1KB
WKUP_R5FSS0_CORE0_ECC_AGGR	0x003F00D000	0x003F00D3FF	1KB
ECC_AGGR1_ECC_AGGR	0x003F00E000	0x003F00E3FF	1KB
ECC_AGGR0_ECC_AGGR	0x003F00F000	0x003F00F3FF	1KB
CBASS_CENTRAL2_ERR	0x003F012000	0x003F0123FF	1KB
PBIST0	0x003F110000	0x003F1103FF	1KB
SA3_SS0_REGS	0x0040900000	0x0040900FFF	4KB
SA3_SS0_MMRA	0x0040901000	0x00409011FF	512B
SA3_SS0_EIP_76	0x0040910000	0x004091007F	128B
SA3_SS0_EIP_29T2	0x0040920000	0x004092FFFF	64KB
DEBUGSS0_SYS	0x0041000000	0x0041000FFF	4KB
WKUP_ROM0	0x0041800000	0x004183FFFF	256KB
WKUP_PSRAMECC_8K0_RAM	0x0041880000	0x0041887FFF	32KB
STM0_STIMULUS	0x0042000000	0x0042FFFFFF	16MB
WKUP_CTRL_MMR0_CFG0	0x0043000000	0x004301FFFF	128KB
SA3_SS0_SEC_PROXY_SRC_TARGET_DATA	0x0043600000	0x004360FFFF	64KB
SA3_SS0_ECCAGGR_CFG	0x0043702000	0x00437023FF	1KB
MSRAM_64K0_RAM	0x0043C40000	0x0043C4FFFF	64KB
SA3_SS0_PSILCFG_CFG_PROXY	0x0044801000	0x00448011FF	512B
SA3_SS0_PSILSS_CFG_MMRS	0x0044802000	0x0044802FFF	4KB
SA3_SS0_IPCSS_SEC_PROXY_CFG_MMRS	0x0044804000	0x00448040FF	256B
SA3_SS0_IPCSS_RINGACC_CFG_GCFG	0x0044805000	0x00448053FF	1KB
SA3_SS0_INTAGGR_CFG	0x0044808000	0x004480801F	32B
SA3_SS0_INTAGGR_CFG_IMAP	0x0044809000	0x00448093FF	1KB
SA3_SS0_INTAGGR_CFG_MCAST	0x004480A000	0x004480A3FF	1KB
SA3_SS0_INTAGGR_CFG_GCNTCFG	0x004480B000	0x004480B3FF	1KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
SA3_SS0_INTAGGR_CFG_INTR	0x0044810000	0x0044817FFF	32KB
SA3_SS0_INTAGGR_CFG_GCNTRTI	0x0044820000	0x004483FFFF	128KB
SA3_SS0_INTAGGR_CFG_UNMAP	0x0044840000	0x004484FFFF	64KB
SA3_SS0_IPCSS_SEC_PROXY_CFG_SCFG	0x0044860000	0x004487FFFF	128KB
SA3_SS0_IPCSS_SEC_PROXY_CFG_RT	0x0044880000	0x004489FFFF	128KB
SA3_SS0_IPCSS_RINGACC_CFG	0x00448C0000	0x00448FFFFF	256KB
SA3_SS0_PKTDMA_CFG_GCFG	0x0044910000	0x00449100FF	256B
SA3_SS0_PKTDMA_CFG_RFLOW	0x0044911000	0x00449113FF	1KB
SA3_SS0_PKTDMA_CFG_RCHAN	0x0044912000	0x00449123FF	1KB
SA3_SS0_PKTDMA_CFG_TCHAN	0x0044913000	0x00449131FF	512B
SA3_SS0_PKTDMA_CFG_RCHANRT	0x0044914000	0x0044917FFF	16KB
SA3_SS0_PKTDMA_CFG_TCHANRT	0x0044918000	0x0044919FFF	8KB
SA3_SS0_PKTDMA_CFG_RING	0x004491A000	0x004491BFFF	8KB
SA3_SS0_PKTDMA_CFG_RINGRT	0x0044940000	0x004497FFFF	256KB
SA3_SS0_IPCSS_RINGACC_CFG_RT	0x0044C00000	0x0044FFFFFF	4MB
CBASS0_FW	0x0045000000	0x0045003FFF	16KB
WKUP_CBASS0_FW	0x0045008000	0x0045009FFF	8KB
CBASS_CENTRAL2_FW	0x0045010000	0x0045010FFF	4KB
PSCSS0_FW	0x0045020000	0x00450203FF	1KB
CBASS_IPCSS0_FW	0x0045028000	0x00450287FF	2KB
DMASS0_PKTDMA_CRED	0x0045810000	0x0045810FFF	4KB
DMASS0_BCDMA_CRED	0x0045812000	0x00458127FF	2KB
WKUP_CBASS0_ISC	0x0045814000	0x0045814FFF	4KB
MCU_CBASS0_ISC	0x0045818000	0x0045818FFF	4KB
CBASS0_ISC	0x0045820000	0x004582FFFF	64KB
MAIN_SEC_MMR0_CFG2	0x0045900000	0x004591FFFF	128KB
WKUP_WKUP_SEC_MMR0_CFG2	0x0045920000	0x004593FFFF	128KB
MCU_MCU_SEC_MMR0_CFG2	0x0045940000	0x00459403FF	1KB
MAIN_SEC_MMR0_CFG0	0x0045A00000	0x0045A1FFFF	128KB
WKUP_WKUP_SEC_MMR0_CFG0	0x0045A20000	0x0045A3FFFF	128KB
MCU_MCU_SEC_MMR0_CFG0	0x0045A40000	0x0045A403FF	1KB
CBASS_IPCSS0_GLB	0x0045B01000	0x0045B013FF	1KB
MCU_CBASS0_GLB	0x0045B02000	0x0045B023FF	1KB
WKUP_CBASS0_GLB	0x0045B03000	0x0045B033FF	1KB
CBASS_CENTRAL2_GLB	0x0045B04000	0x0045B043FF	1KB
CBASS0_GLB	0x0045B08000	0x0045B083FF	1KB
PSCSS0_GLB	0x0045B09000	0x0045B093FF	1KB
WKUP_CBASS0_QOS	0x0045D14000	0x0045D14FFF	4KB
MCU_CBASS0_QOS	0x0045D18000	0x0045D18FFF	4KB
CBASS0_QOS	0x0045D20000	0x0045D2FFFF	64KB
DMASS0_INTAGGR_INTR	0x0048000000	0x00480FFFFF	1MB
DMASS0_INTAGGR_IMAP	0x0048100000	0x0048103FFF	16KB
DMASS0_INTAGGR_CFG	0x0048110000	0x004811001F	32B
DMASS0_INTAGGR_L2G	0x0048120000	0x00481203FF	1KB
DMASS0_PSILCFG_PROXY	0x0048130000	0x00481301FF	512B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
DMASS0_PSILSS_MMRS	0x0048140000	0x0048140FFF	4KB
DMASS0_INTAGGR_UNMAP	0x0048180000	0x004819FFFF	128KB
DMASS0_INTAGGR_MCAST	0x0048210000	0x0048210FFF	4KB
DMASS0_INTAGGR_GCNTCFG	0x0048220000	0x0048221FFF	8KB
DMASS0_ETLSW_MMRS	0x0048230000	0x0048230FFF	4KB
DMASS0_RINGACC_GCFG	0x0048240000	0x00482403FF	1KB
DMASS0_SEC_PROXY_MMRS	0x0048250000	0x00482500FF	256B
DMASS0_BCDMA_BCHAN	0x0048420000	0x0048421FFF	8KB
DMASS0_PKTDMA_RFLOW	0x0048430000	0x0048430FFF	4KB
DMASS0_PKTDMA_TCHAN	0x00484A0000	0x00484A1FFF	8KB
DMASS0_BCDMA_TCHAN	0x00484A4000	0x00484A5FFF	8KB
DMASS0_PKTDMA_RCHAN	0x00484C0000	0x00484C1FFF	8KB
DMASS0_BCDMA_RCHAN	0x00484C2000	0x00484C3FFF	8KB
DMASS0_PKTDMA_GCFG	0x00485C0000	0x00485C00FF	256B
DMASS0_BCDMA_GCFG	0x00485C0100	0x00485C01FF	256B
DMASS0_PKTDMA_RING	0x00485E0000	0x00485EFFFF	64KB
DMASS0_BCDMA_RING	0x0048600000	0x0048607FFF	32KB
DMASS0_RINGACC_RT	0x0049000000	0x00493FFFFF	4MB
DMASS0_RINGACC_CFG	0x0049800000	0x004983FFFF	256KB
DMASS0_INTAGGR_GCNTRTI	0x004A000000	0x004A0FFFFF	1MB
DMASS0_SEC_PROXY_SCFG	0x004A400000	0x004A47FFFF	512KB
DMASS0_SEC_PROXY_RT	0x004A600000	0x004A67FFFF	512KB
DMASS0_PKTDMA_RCHANRT	0x004A800000	0x004A81FFFF	128KB
DMASS0_BCDMA_RCHANRT	0x004A820000	0x004A83FFFF	128KB
DMASS0_PKTDMA_TCHANRT	0x004AA00000	0x004AA1FFFF	128KB
DMASS0_BCDMA_TCHANRT	0x004AA40000	0x004AA5FFFF	128KB
DMASS0_PKTDMA_RINGRT	0x004B800000	0x004B9FFFFF	2MB
DMASS0_BCDMA_RINGRT	0x004BC00000	0x004BCFFFFF	1MB
DMASS0_BCDMA_BCHANRT	0x004C000000	0x004C01FFFF	128KB
DMASS0_SEC_PROXY_SRC_TARGET_DATA	0x004D000000	0x004D07FFFF	512KB
GPMC0_DATA	0x0050000000	0x0057FFFFFF	128MB
FSS0_DAT_REG1	0x0060000000	0x0067FFFFFF	128MB
MSRAM_64K0_RAM	0x0070000000	0x007000FFFF	64KB
MCU_R5FSS0_CORE0_ICACHE	0x0073000000	0x00737FFFFF	8MB
MCU_R5FSS0_CORE0_DCACHE	0x0073800000	0x0073FFFFFF	8MB
WKUP_R5FSS0_CORE0_ICACHE	0x0074000000	0x00747FFFFF	8MB
WKUP_R5FSS0_CORE0_DCACHE	0x0074800000	0x0074FFFFFF	8MB
WKUP_R5FSS0_CORE0_ATCM(1)	0x0078000000	0x0078007FFF	32KB
WKUP_R5FSS0_CORE0_BTCM(1)	0x0078100000	0x0078107FFF	32KB
MCU_R5FSS0_CORE0_ATCM(1)	0x0079000000	0x0079007FFF	32KB
MCU_R5FSS0_CORE0_BTCM(1)	0x0079020000	0x0079027FFF	32KB
MCU_MSRAM_256K0_RAM	0x0079100000	0x007913FFFF	256KB
MCU_MSRAM_256K1_RAM	0x0079140000	0x007917FFFF	256KB
C7X256V0_UMC	0x007C000000	0x007C01FFFF	128KB
C7X256V0_CLEC	0x007C200000	0x007C2FFFFF	1MB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
C7X256V0_DRU	0x007C400000	0x007C403FFF	16KB
C7X256V0_DRU_SET	0x007C404000	0x007C407FFF	16KB
C7X256V0_DRU_QUEUE	0x007C408000	0x007C40FFFF	32KB
C7X256V0_DRU_CHNRT	0x007C440000	0x007C45FFFF	128KB
C7X256V0_DRU_CHRT	0x007C460000	0x007C47FFFF	128KB
C7X256V0_DRU_CHATOMIC_DEBUG	0x007C480000	0x007C49FFFF	128KB
C7X256V0_DRU_CHCORE	0x007C4A0000	0x007C4BFFFF	128KB
C7X256V0_DRU	0x007C4E0000	0x007C4FFFFF	128KB
C7X256V0_UMC_MEM_MAIN	0x007E000000	0x007E0FFFFF	1MB
C7X256V0_UMC_MEM_AUX	0x007F000000	0x007F03FFFF	256KB
DDR32SS0_SDRAM	0x0080000000	0x00FFFFFFFF	2GB
FSS0_DAT_REG0	0x0400000000	0x04FFFFFFFF	4GB
FSS0_DAT_REG3	0x0500000000	0x05FFFFFFFF	4GB
DEBUGSS_WRAP0_ROM_TABLE_0_0	0x0700000000	0x0700000FFF	4KB
DEBUGSS_WRAP0_RESV0_0	0x0700001000	0x0700001FFF	4KB
DEBUGSS_WRAP0_CFGAP0	0x0700002000	0x07000020FF	256B
DEBUGSS_WRAP0_APBAP0	0x0700002100	0x07000021FF	256B
DEBUGSS_WRAP0_AXIAP0	0x0700002200	0x07000022FF	256B
DEBUGSS_WRAP0_PWRAP0	0x0700002300	0x07000023FF	256B
DEBUGSS_WRAP0_PVIEW0	0x0700002400	0x07000024FF	256B
DEBUGSS_WRAP0_JTAGAP0	0x0700002500	0x07000025FF	256B
DEBUGSS_WRAP0_SECAP0	0x0700002600	0x07000026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG0	0x0700002700	0x07000027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG0	0x0700002800	0x07000028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG0	0x0700002900	0x07000029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG0	0x0700002A00	0x0700002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG0	0x0700002B00	0x0700002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG0	0x0700002C00	0x0700002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG0	0x0700002D00	0x0700002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG0	0x0700002E00	0x0700002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG0	0x0700002F00	0x0700002FFF	256B
DEBUGSS_WRAP0_RESV1_0	0x0700003000	0x0700003FFF	4KB
DEBUGSS_WRAP0_RESV2_0	0x0700004000	0x0702003FFF	32MB
DEBUGSS_WRAP0_ROM_TABLE_1_0	0x0720000000	0x0720000FFF	4KB
DEBUGSS_WRAP0_CSCTI	0x0720001000	0x0720001FFF	4KB
DEBUGSS_WRAP0_DRM0	0x0720002000	0x0720002FFF	4KB
DEBUGSS_WRAP0_RESV3_0	0x0720003000	0x0720003FFF	4KB
DEBUGSS_WRAP0_CSTPIU0	0x0720004000	0x0720004FFF	4KB
DEBUGSS_WRAP0_CTF0	0x0720005000	0x0720005FFF	4KB
DEBUGSS_WRAP0_RESV4_0	0x0720006000	0x0721005FFF	16MB
COMPUTE_CLUSTER0_SS_ROM	0x0730000000	0x073000FFFF	64KB
DEBUGSS_WRAP0_EXT_APB0	0x0730000000	0x073FFFFFFF	256MB
COMPUTE_CLUSTER0_CORE0_DBG	0x0730010000	0x073001FFFF	64KB
COMPUTE_CLUSTER0_CORE0_CTI	0x0730020000	0x073002FFFF	64KB
COMPUTE_CLUSTER0_CORE0_PMU	0x0730030000	0x073003FFFF	64KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
COMPUTE_CLUSTER0_CORE0_ETM	0x0730040000	0x073004FFFF	64KB
COMPUTE_CLUSTER0_CORE1_DBG	0x0730110000	0x073011FFFF	64KB
COMPUTE_CLUSTER0_CORE1_PMU	0x0730120000	0x073012FFFF	64KB
COMPUTE_CLUSTER0_CORE1_ETM	0x0730130000	0x073013FFFF	64KB
COMPUTE_CLUSTER0_CORE1_CTI	0x0730140000	0x073014FFFF	64KB
COMPUTE_CLUSTER0_CORE2_DBG	0x0730210000	0x073021FFFF	64KB
COMPUTE_CLUSTER0_CORE2_PMU	0x0730220000	0x073022FFFF	64KB
COMPUTE_CLUSTER0_CORE2_ETM	0x0730230000	0x073023FFFF	64KB
COMPUTE_CLUSTER0_CORE2_CTI	0x0730240000	0x073024FFFF	64KB
COMPUTE_CLUSTER0_CORE3_DBG	0x0730310000	0x073031FFFF	64KB
COMPUTE_CLUSTER0_CORE3_PMU	0x0730320000	0x073032FFFF	64KB
COMPUTE_CLUSTER0_CORE3_ETM	0x0730330000	0x073033FFFF	64KB
COMPUTE_CLUSTER0_CORE3_CTI	0x0730340000	0x073034FFFF	64KB
C7X256V0_THINMAN	0x0734000000	0x0734001FFF	8KB
C7X256V0_COLOMBO	0x0734001000	0x0734002FFF	8KB
C7X256V0_MATLOCK	0x0734002000	0x0734003FFF	8KB
C7X256V0_CSCTI	0x0734003000	0x0734003FFF	4KB
C7X256V0_CTSET2	0x0734008000	0x0734009FFF	8KB
C7X256V0_CSCTI	0x073400A000	0x073400AFFF	4KB
C7X256V0_CSCTI	0x073400B000	0x073400BFFF	4KB
C7X256V0_DBG_AGR0_MMR	0x0734040000	0x07340400FF	256B
C7X256V0_DBG_AGR0_MEM_CFG	0x0734040100	0x07340401FF	256B
C7X256V0_DBG_AGR0_MEM0	0x0734060000	0x0734060FFF	4KB
C7X256V0_DBG_AGR0_MEM1	0x0734061000	0x0734061FFF	4KB
C7X256V0_DBG_AGR0_MEM2	0x0734062000	0x0734062FFF	4KB
C7X256V0_DBG_AGR0_MEM3	0x0734063000	0x0734063FFF	4KB
C7X256V0_DBG_AGR0_MEM4	0x0734064000	0x0734064FFF	4KB
C7X256V0_DBG_AGR0_MEM5	0x0734065000	0x0734065FFF	4KB
C7X256V0_DBG_AGR0_MEM6	0x0734066000	0x0734066FFF	4KB
C7X256V0_DBG_AGR0_MEM7	0x0734067000	0x0734067FFF	4KB
C7X256V0_DBG_AGR0_MEM8	0x0734068000	0x0734068FFF	4KB
C7X256V0_DBG_AGR0_MEM9	0x0734069000	0x0734069FFF	4KB
C7X256V0_DBG_AGR0_MEM10	0x073406A000	0x073406AFFF	4KB
C7X256V0_DBG_AGR0_MEM11	0x073406B000	0x073406BFFF	4KB
C7X256V0_DBG_AGR0_MEM12	0x073406C000	0x073406CFFF	4KB
C7X256V0_DBG_AGR0_MEM13	0x073406D000	0x073406DFFF	4KB
C7X256V0_DBG_AGR0_MEM14	0x073406E000	0x073406EFFF	4KB
C7X256V0_DBG_AGR0_MEM15	0x073406F000	0x073406FFFF	4KB
C7X256V0_DBG_AGR0_MEM16	0x0734070000	0x0734070FFF	4KB
C7X256V0_DBG_AGR0_MEM17	0x0734071000	0x0734071FFF	4KB
C7X256V0_DBG_AGR0_MEM18	0x0734072000	0x0734072FFF	4KB
C7X256V0_DBG_AGR0_MEM19	0x0734073000	0x0734073FFF	4KB
C7X256V0_DBG_AGR0_MEM20	0x0734074000	0x0734074FFF	4KB
C7X256V0_DBG_AGR0_MEM21	0x0734075000	0x0734075FFF	4KB
C7X256V0_DBG_AGR0_MEM22	0x0734076000	0x0734076FFF	4KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
C7X256V0_DBG_AGR0_MEM23	0x0734077000	0x0734077FFF	4KB
C7X256V0_DBG_AGR0_MEM24	0x0734078000	0x0734078FFF	4KB
C7X256V0_DBG_AGR0_MEM25	0x0734079000	0x0734079FFF	4KB
C7X256V0_DBG_AGR0_MEM26	0x073407A000	0x073407AFFF	4KB
C7X256V0_DBG_AGR0_MEM27	0x073407B000	0x073407BFFF	4KB
C7X256V0_DBG_AGR0_MEM28	0x073407C000	0x073407CFFF	4KB
C7X256V0_DBG_AGR0_MEM29	0x073407D000	0x073407DFFF	4KB
C7X256V0_DBG_AGR0_MEM30	0x073407E000	0x073407EFFF	4KB
C7X256V0_DBG_AGR0_MEM31	0x073407F000	0x073407FFFF	4KB
DEBUGSS0_DEBUG_CELL_ROM_SLV	0x073C020000	0x073C020FFF	4KB
DEBUGSS0_CTSET2_WRAP_CFG_CTSET2_CFG	0x073C022000	0x073C023FFF	8KB
DEBUGSS0_CT_TRACECELL_TETRIS	0x073C024000	0x073C024FFF	4KB
DEBUGSS0_CT_TBR	0x073C025000	0x073C025FFF	4KB
DEBUGSS0_CSCTI	0x073C026000	0x073C026FFF	4KB
DEBUGSS0_CSCTI	0x073C028000	0x073C028FFF	4KB
DEBUGSS0_CSCTI	0x073C029000	0x073C029FFF	4KB
DEBUGSS0_CSCTI	0x073C02A000	0x073C02AFFF	4KB
DEBUGSS0_CSCTI	0x073C02B000	0x073C02BFFF	4KB
DEBUGSS0_CSCTI	0x073C02C000	0x073C02CFFF	4KB
DEBUGSS0_CSCTI	0x073C02D000	0x073C02DFFF	4KB
DEBUGSS0_CSCTI	0x073C02E000	0x073C02EFFF	4KB
DEBUGSS0_CSCTI	0x073C02F000	0x073C02FFFF	4KB
STM0_CSSTM	0x073D200000	0x073D200FFF	4KB
STM0_CTI_CSCTI	0x073D201000	0x073D201FFF	4KB
DBGSUSPENDROUTER0_INTR_ROUTER_CFG	0x073D300000	0x073D3007FF	2KB
CPT2_AGGR0_MMR	0x073E100000	0x073E1000FF	256B
CPT2_AGGR0_STP2ATB_CFG	0x073E100100	0x073E1001FF	256B
CPT2_AGGR0_MEM0	0x073E120000	0x073E120FFF	4KB
CPT2_AGGR0_MEM1	0x073E121000	0x073E121FFF	4KB
CPT2_AGGR0_MEM2	0x073E122000	0x073E122FFF	4KB
CPT2_AGGR0_MEM3	0x073E123000	0x073E123FFF	4KB
CPT2_AGGR0_MEM4	0x073E124000	0x073E124FFF	4KB
CPT2_AGGR0_MEM5	0x073E125000	0x073E125FFF	4KB
CPT2_AGGR0_MEM6	0x073E126000	0x073E126FFF	4KB
CPT2_AGGR0_MEM7	0x073E127000	0x073E127FFF	4KB
CPT2_AGGR0_MEM8	0x073E128000	0x073E128FFF	4KB
CPT2_AGGR0_MEM9	0x073E129000	0x073E129FFF	4KB
CPT2_AGGR0_MEM10	0x073E12A000	0x073E12AFFF	4KB
CPT2_AGGR0_MEM11	0x073E12B000	0x073E12BFFF	4KB
CPT2_AGGR0_MEM12	0x073E12C000	0x073E12CFFF	4KB
CPT2_AGGR0_MEM13	0x073E12D000	0x073E12DFFF	4KB
CPT2_AGGR0_MEM14	0x073E12E000	0x073E12EFFF	4KB
CPT2_AGGR0_MEM15	0x073E12F000	0x073E12FFFF	4KB
CPT2_AGGR0_MEM16	0x073E130000	0x073E130FFF	4KB
CPT2_AGGR0_MEM17	0x073E131000	0x073E131FFF	4KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
CPT2_AGGR0_MEM18	0x073E132000	0x073E132FFF	4KB
CPT2_AGGR0_MEM19	0x073E133000	0x073E133FFF	4KB
CPT2_AGGR0_MEM20	0x073E134000	0x073E134FFF	4KB
CPT2_AGGR0_MEM21	0x073E135000	0x073E135FFF	4KB
CPT2_AGGR0_MEM22	0x073E136000	0x073E136FFF	4KB
CPT2_AGGR0_MEM23	0x073E137000	0x073E137FFF	4KB
CPT2_AGGR0_MEM24	0x073E138000	0x073E138FFF	4KB
CPT2_AGGR0_MEM25	0x073E139000	0x073E139FFF	4KB
CPT2_AGGR0_MEM26	0x073E13A000	0x073E13AFFF	4KB
CPT2_AGGR0_MEM27	0x073E13B000	0x073E13BFFF	4KB
CPT2_AGGR0_MEM28	0x073E13C000	0x073E13CFFF	4KB
CPT2_AGGR0_MEM29	0x073E13D000	0x073E13DFFF	4KB
CPT2_AGGR0_MEM30	0x073E13E000	0x073E13EFFF	4KB
CPT2_AGGR0_MEM31	0x073E13F000	0x073E13FFFF	4KB
CPT2_AGGR1_MMR	0x073E140000	0x073E1400FF	256B
CPT2_AGGR1_STP2ATB_CFG	0x073E140100	0x073E1401FF	256B
CPT2_AGGR1_MEM0	0x073E160000	0x073E160FFF	4KB
CPT2_AGGR1_MEM1	0x073E161000	0x073E161FFF	4KB
CPT2_AGGR1_MEM2	0x073E162000	0x073E162FFF	4KB
CPT2_AGGR1_MEM3	0x073E163000	0x073E163FFF	4KB
CPT2_AGGR1_MEM4	0x073E164000	0x073E164FFF	4KB
CPT2_AGGR1_MEM5	0x073E165000	0x073E165FFF	4KB
CPT2_AGGR1_MEM6	0x073E166000	0x073E166FFF	4KB
CPT2_AGGR1_MEM7	0x073E167000	0x073E167FFF	4KB
CPT2_AGGR1_MEM8	0x073E168000	0x073E168FFF	4KB
CPT2_AGGR1_MEM9	0x073E169000	0x073E169FFF	4KB
CPT2_AGGR1_MEM10	0x073E16A000	0x073E16AFFF	4KB
CPT2_AGGR1_MEM11	0x073E16B000	0x073E16BFFF	4KB
CPT2_AGGR1_MEM12	0x073E16C000	0x073E16CFFF	4KB
CPT2_AGGR1_MEM13	0x073E16D000	0x073E16DFFF	4KB
CPT2_AGGR1_MEM14	0x073E16E000	0x073E16EFFF	4KB
CPT2_AGGR1_MEM15	0x073E16F000	0x073E16FFFF	4KB
CPT2_AGGR1_MEM16	0x073E170000	0x073E170FFF	4KB
CPT2_AGGR1_MEM17	0x073E171000	0x073E171FFF	4KB
CPT2_AGGR1_MEM18	0x073E172000	0x073E172FFF	4KB
CPT2_AGGR1_MEM19	0x073E173000	0x073E173FFF	4KB
CPT2_AGGR1_MEM20	0x073E174000	0x073E174FFF	4KB
CPT2_AGGR1_MEM21	0x073E175000	0x073E175FFF	4KB
CPT2_AGGR1_MEM22	0x073E176000	0x073E176FFF	4KB
CPT2_AGGR1_MEM23	0x073E177000	0x073E177FFF	4KB
CPT2_AGGR1_MEM24	0x073E178000	0x073E178FFF	4KB
CPT2_AGGR1_MEM25	0x073E179000	0x073E179FFF	4KB
CPT2_AGGR1_MEM26	0x073E17A000	0x073E17AFFF	4KB
CPT2_AGGR1_MEM27	0x073E17B000	0x073E17BFFF	4KB
CPT2_AGGR1_MEM28	0x073E17C000	0x073E17CFFF	4KB

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
CPT2_AGGR1_MEM29	0x073E17D000	0x073E17DFFF	4KB
CPT2_AGGR1_MEM30	0x073E17E000	0x073E17EFFF	4KB
CPT2_AGGR1_MEM31	0x073E17F000	0x073E17FFFF	4KB
MCU_CPT2_AGGR0_MMR	0x073E180000	0x073E1800FF	256B
MCU_CPT2_AGGR0_STP2ATB_CFG	0x073E180100	0x073E1801FF	256B
MCU_CPT2_AGGR0_MEM0	0x073E1A0000	0x073E1A0FFF	4KB
MCU_CPT2_AGGR0_MEM1	0x073E1A1000	0x073E1A1FFF	4KB
MCU_CPT2_AGGR0_MEM2	0x073E1A2000	0x073E1A2FFF	4KB
MCU_CPT2_AGGR0_MEM3	0x073E1A3000	0x073E1A3FFF	4KB
MCU_CPT2_AGGR0_MEM4	0x073E1A4000	0x073E1A4FFF	4KB
MCU_CPT2_AGGR0_MEM5	0x073E1A5000	0x073E1A5FFF	4KB
MCU_CPT2_AGGR0_MEM6	0x073E1A6000	0x073E1A6FFF	4KB
MCU_CPT2_AGGR0_MEM7	0x073E1A7000	0x073E1A7FFF	4KB
MCU_CPT2_AGGR0_MEM8	0x073E1A8000	0x073E1A8FFF	4KB
MCU_CPT2_AGGR0_MEM9	0x073E1A9000	0x073E1A9FFF	4KB
MCU_CPT2_AGGR0_MEM10	0x073E1AA000	0x073E1AAFFF	4KB
MCU_CPT2_AGGR0_MEM11	0x073E1AB000	0x073E1ABFFF	4KB
MCU_CPT2_AGGR0_MEM12	0x073E1AC000	0x073E1ACFFF	4KB
MCU_CPT2_AGGR0_MEM13	0x073E1AD000	0x073E1ADFFF	4KB
MCU_CPT2_AGGR0_MEM14	0x073E1AE000	0x073E1AEFFF	4KB
MCU_CPT2_AGGR0_MEM15	0x073E1AF000	0x073E1AFFFF	4KB
MCU_CPT2_AGGR0_MEM16	0x073E1B0000	0x073E1B0FFF	4KB
MCU_CPT2_AGGR0_MEM17	0x073E1B1000	0x073E1B1FFF	4KB
MCU_CPT2_AGGR0_MEM18	0x073E1B2000	0x073E1B2FFF	4KB
MCU_CPT2_AGGR0_MEM19	0x073E1B3000	0x073E1B3FFF	4KB
MCU_CPT2_AGGR0_MEM20	0x073E1B4000	0x073E1B4FFF	4KB
MCU_CPT2_AGGR0_MEM21	0x073E1B5000	0x073E1B5FFF	4KB
MCU_CPT2_AGGR0_MEM22	0x073E1B6000	0x073E1B6FFF	4KB
MCU_CPT2_AGGR0_MEM23	0x073E1B7000	0x073E1B7FFF	4KB
MCU_CPT2_AGGR0_MEM24	0x073E1B8000	0x073E1B8FFF	4KB
MCU_CPT2_AGGR0_MEM25	0x073E1B9000	0x073E1B9FFF	4KB
MCU_CPT2_AGGR0_MEM26	0x073E1BA000	0x073E1BAFFF	4KB
MCU_CPT2_AGGR0_MEM27	0x073E1BB000	0x073E1BBFFF	4KB
MCU_CPT2_AGGR0_MEM28	0x073E1BC000	0x073E1BCFFF	4KB
MCU_CPT2_AGGR0_MEM29	0x073E1BD000	0x073E1BDFFF	4KB
MCU_CPT2_AGGR0_MEM30	0x073E1BE000	0x073E1BEFFF	4KB
MCU_CPT2_AGGR0_MEM31	0x073E1BF000	0x073E1BFFFF	4KB
DEBUGSS_WRAP0_ROM_TABLE_0_1	0x0740000000	0x0740000FFF	4KB
DEBUGSS_WRAP0_RESV0_1	0x0740001000	0x0740001FFF	4KB
DEBUGSS_WRAP0_CFGAP1	0x0740002000	0x07400020FF	256B
DEBUGSS_WRAP0_APBAP1	0x0740002100	0x07400021FF	256B
DEBUGSS_WRAP0_AXIAP1	0x0740002200	0x07400022FF	256B
DEBUGSS_WRAP0_PWRAP1	0x0740002300	0x07400023FF	256B
DEBUGSS_WRAP0_PVIEW1	0x0740002400	0x07400024FF	256B
DEBUGSS_WRAP0_JTAGAP1	0x0740002500	0x07400025FF	256B

Table 2-3. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
DEBUGSS_WRAP0_SECAP1	0x0740002600	0x07400026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG1	0x0740002700	0x07400027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG1	0x0740002800	0x07400028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG1	0x0740002900	0x07400029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG1	0x0740002A00	0x0740002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG1	0x0740002B00	0x0740002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG1	0x0740002C00	0x0740002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG1	0x0740002D00	0x0740002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG1	0x0740002E00	0x0740002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG1	0x0740002F00	0x0740002FFF	256B
DEBUGSS_WRAP0_RESV1_1	0x0740003000	0x0740003FFF	4KB
DEBUGSS_WRAP0_RESV2_1	0x0740004000	0x0742003FFF	32MB
DEBUGSS_WRAP0_ROM_TABLE_1_1	0x0760000000	0x0760000FFF	4KB
DEBUGSS_WRAP0_CSCTI	0x0760001000	0x0760001FFF	4KB
DEBUGSS_WRAP0_DRM1	0x0760002000	0x0760002FFF	4KB
DEBUGSS_WRAP0_RESV3_1	0x0760003000	0x0760003FFF	4KB
DEBUGSS_WRAP0_CSTPIU1	0x0760004000	0x0760004FFF	4KB
DEBUGSS_WRAP0_CTF1	0x0760005000	0x0760005FFF	4KB
DEBUGSS_WRAP0_RESV4_1	0x0760006000	0x0761005FFF	16MB
DEBUGSS_WRAP0_EXT_APB1	0x0770000000	0x077FFFFFFF	256MB
DDR32SS0_SDRAM	0x0880000000	0x08FFFFFFFF	2GB
DDR32SS0_SDRAM	0x0900000000	0x09FFFFFFFF	4GB
DDR32SS0_SDRAM	0x0A00000000	0x0BFFFFFFFF	8GB
DDR32SS0_SDRAM	0x0C00000000	0x0FFFFFFFFF	16GB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.1.4.2 MCU_R5FSS0 Memory Map

Table 2-4. MCU_R5FSS0 Memory Map

Region Name	Start Address	End Address	Size
MCU_R5FSS0_ATCM(1)	0x0000000000	0x0000007FFF	32KB
MCU_R5FSS0_RAT_REGION0	0x0000010000	0x000400FFFF	64MB
MCU_R5FSS0_NON_RAT_REGION0	0x0004000000	0x0007FDFFFF	64MB
MCU_R5FSS0_RAT_CFG	0x0007FE0000	0x0007FE0FFF	4KB
MCU_R5FSS0_VIC_CFG	0x0007FF0000	0x0007FF3FFF	16KB
MCU_R5FSS0_RAT_REGION1	0x0008000000	0x004100FFFF	912MB
MCU_R5FSS0_BTCM(1)	0x0041010000	0x0041017FFF	32KB
MCU_R5FSS0_RAT_REGION2	0x0041018000	0x007FFFFFFF	1008MB
MCU_R5FSS0_RAT_REGION3	0x0080000000	0x00FFFFFFFF	2GB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.1.4.3 WKUP_R5FSS0 Memory Map

Table 2-5. WKUP_R5FSS0 Memory Map

Region Name	Start Address	End Address	Size
WKUP_R5FSS0_ATCM(1)	0x0000000000	0x0000007FFF	32KB
WKUP_R5FSS0_RAT_REGION0	0x0000010000	0x001FFFFFFF	512MB
WKUP_R5FSS0_NON_RAT_SOC_REGION0	0x0020000000	0x002FFDFFFF	256MB
WKUP_R5FSS0_NON_RAT_SOC_REGION0	0x0020000000	0x002FFFFFFF	256MB
WKUP_R5FSS0_RAT_CFG	0x002FFE0000	0x002FFE0FFF	4KB
WKUP_R5FSS0_VIC_CFG	0x002FFF0000	0x002FFF3FFF	16KB
WKUP_R5FSS0_RAT_REGION1	0x0030000000	0x004100FFFF	272MB
WKUP_R5FSS0_RAT_SOC_REGION1	0x0030000000	0x004100FFFF	272MB
WKUP_R5FSS0_BTCM(1)	0x0041010000	0x0041017FFF	32KB
WKUP_R5FSS0_RAT_REGION2	0x0041018000	0x007FFFFFFF	1008MB
WKUP_R5FSS0_RAT_REGION3	0x0080000000	0x00FFFFFFFF	2GB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.1.4.4 DMASS0 Memory Map

Table 2-6. DMASS0 Memory Map

Region Name	Start Address	End Address	Size
DMASS0_RINGACC__SRC__FIFOS	0x0000400000	0x00007FFFFF	4MB

2.1.4.5 SA3_SS0 Memory Map

Table 2-7. SA3_SS0 Memory Map

Region Name	Start Address	End Address	Size
SA3_SS0_RINGACC__SRC__FIFOS	0x0000400000	0x0000405FFF	24KB

Chapter 3

System Interconnect

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3.1 Terminology

- **CBASS**: Crossbar module to provide physical connections among the initiators and targets
- **VBUSP Interface**: Single-issue interface
- **VBUSM Interface**: Multi-issue interface
- **Channel ID:** Channel ID for an interface indicates a logical flow. All transactions with the same channel ID and initiator are consider an orthogonal and independent flow.
- **Order ID**: 4 bit value associated with each transaction. All transactions with the same initiator, target end point, and Order ID are executed in order. Order ID is also to be used to select real-time and non-real time path for the transaction. Order ID 8-15 is reserved for real-time path.
- **ASEL:** Address Selection is an attribute associated with each transaction. ASEL can be either used to select a unique memory map or be used to indicate IO coherent transactions.
- **PrivID**: PrivID is an attribute associated with each transaction. The privID value indicates the security access group. PrivID is either assigned by the ISC block or DMA configuration.
- **Priv:**Priv is a transaction attribute to determine whether the transaction has supervisor privilege. Priv =1 indicates supervisor privilege. Priv=0 indicates user privilege.
- **Secure**: this is a single bit control signal carried with each transaction. If it is set to 1b1, it means this is a secure transaction. If it is set to 1b0, then it is a non-secure transaction.
- **ISC**: Initiator Security Control. ISC can add or overwrite the transaction attributes such as PrivID, Priv and Secure.
- **Region Based Firewall**: Firewall block based on address region. The minimal region granularity is 4KB. User can configure each the protection region and its access privilege.
- **Channelized firewall**: provide protection for a predefined region size, the predefined region size can be as small as 4B.
- **QoS**: Quality of Service allows user to add additional sideband signals to the transaction to fine tune system level performance.

3.2 System Interconnect Overview

The SoC is divided into three domains: WKUP Domain,MCU Domain and MAIN Domain. Inside each domain resides multiple CBASS crossbar IPs to provide connectivity among initiators and targets.

The MAIN Domain contains the following CBASS IPs:

- CBASS0
- CBASS_INFRA1
- CBASS_FW0
- CBASS_DBG0
- CBASS_IPCSS0
- CBASS_CENTRAL2
- CBASS_MCASP0

The MCU Domain contains the following CBASS IP:

- MCU_CBASS0

The WKUP Domain contains the following CBASS IP:

- WKUP_CBASS0

CBASS_FW0 is dedicated to route the firewall, QoS Block and ISC Block configurations. CBASS_DBG0 is dedicated to route all debug configuration related transactions.

Figure 3-1. Device System Interconnect Overview

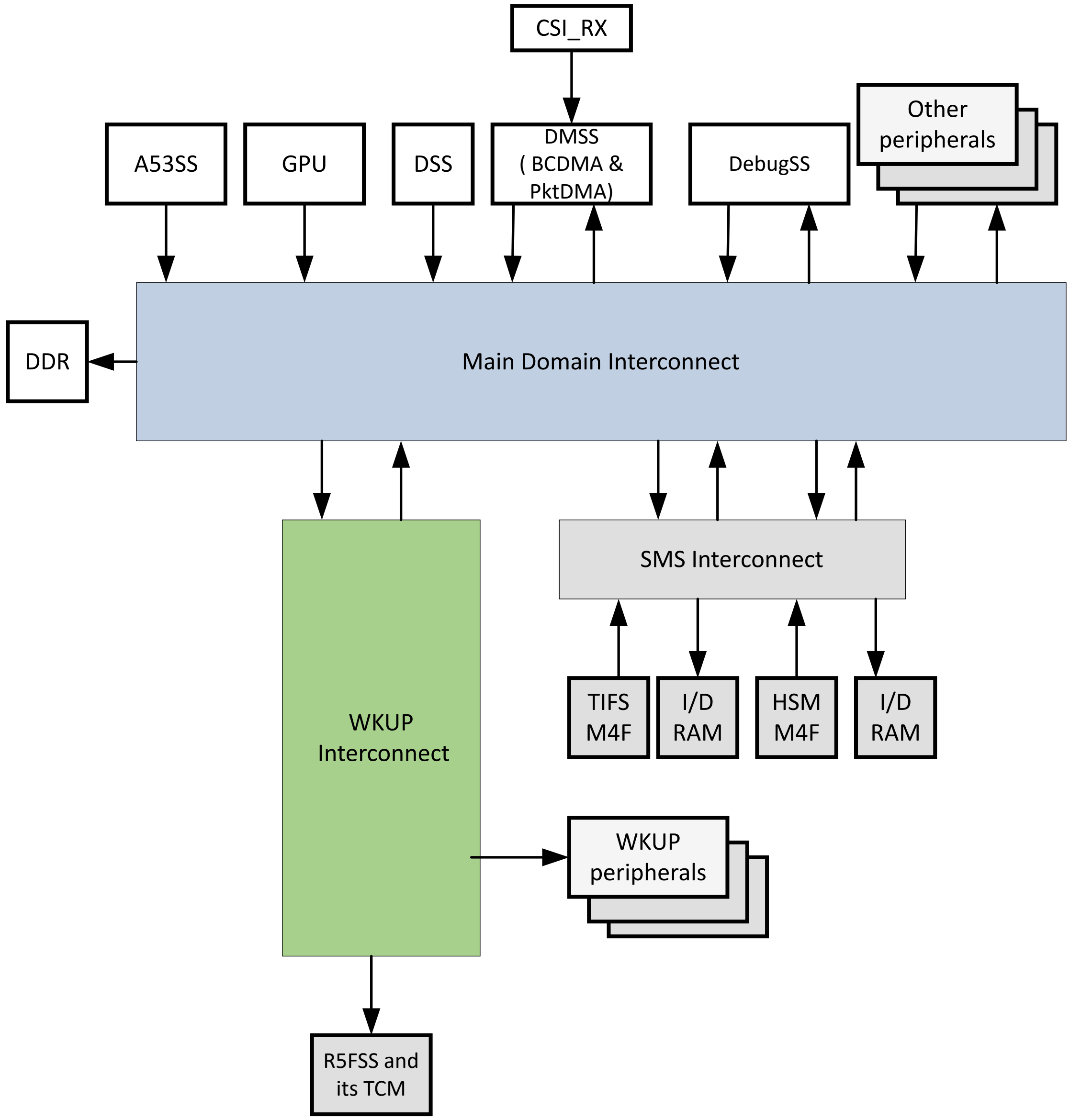

3.3 Initiator/Target Connectivity

All processors and DMA have the physical path to read from and write to any memory mapped end points listed in the SoC memory map.

The configuration of the crypto DMSS is only accessible by TIFS M4F core, and is not included in the SoC level memory map.

3.4 Interrupt Condition for Interconnect

Each CBASS crossbar IP may generate up to two interrupts:

- default_err_intr: the intent of this interrupt is for debug purposes. Any illegal transactions will trigger this interrupt and the illegal transaction information is logged by CBASS IP.
- default_exp: this interrupt is asserted whenever there is a firewall violation. Only the CBASS IP contains firewall module that can generate this interrupt.

The illegal transactions triggering default_err_intr can be caused by multiple reasons:

- The transaction is sent to a memory region not implemented in CBASS
- The target interface or target peripheral is in disabled state

When CBASS detects an illegal transaction, it terminates the transaction gracefully to avoid a system hang. In addition, the CBASS sends return status back to the initiator with error status. If this illegal transaction is a read transaction, the read data is returned with all zeros. If this illegal transaction is a write transaction, this write transaction is terminated and returns a write error back to initiator. The interrupt and illegal transaction logging can be found in the CBASS's err_regs region.

For any transaction blocked by the firewall, the transaction is terminated gracefully and the initiator will receive error status for the blocked transaction. If this blocked transaction is read, the read data is returned with all zeros. If this blocked transaction is a write transaction, this write transaction is terminated and returns a write error back to the initiator. The default_exp interrupt and the blocked transaction information can be found in the glb_regs region.

Table 3-1. CBASS Interrupt

CBASS Name	default_err_intr supported	default_exp Interrupt supported
CBASS0	Yes	Yes
MCU_CBASS0	Yes	No
CBASS_INFRA1	Yes	Yes
CBASS_FW0	Yes	No
CBASS_DBG0	Yes	No
CBASS_IPCSS0	Yes	Yes
CBASS_CENTRAL2	Yes	Yes
CBASS_MCASP0	Yes	No
WKUP_CBASS0	Yes	Yes

3.4.1 Register MMR for default_err_intr

Each CBASS supports default_err_intr containing an err_regs region, which includes the following registers:

Address Offset	Register Mnemonic	Register Name
0x0	PID	Revision Register
0x4	DESTINATION_ID	Destination ID Register
0x24	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
0x28	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
0x2c	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
0x30	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
0x34	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
0x38	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
0x50	ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register
0x54	ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register
0x58	ERR_INTR_ENABLE_SET	Interrupt Enable Set Register
0x5c	ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register
0x60	ERR_EOI	EOI Register

PID (Revision Register) is located at offset 0x0. The following shows the definition of each field of this register.

The Revision Register contains the major and minor revisions for the module.

Bit	Name	Type	Reset	Description
31:30	scheme	r	0x1	PID register scheme
29:28	bu	r	0x2	Business Unit: 10 = Processors
27:16	func	r	0x600	Module ID
15:11	rtl	r	0x6	RTL revision. Will vary depending on release.
10:8	major	r	0x1	Major revision
7:6	custom	r	0x0	Custom
5:0	minor	r	0x2	Minor revision

DESTINATION_ID (Destination ID Register) has offset 0x4.

The Destination ID Register defines the destination ID value for error messages.

Bit	Name	Type	Reset	Description
31:8	reserved	r	0x0	Reserved
7:0	dest_id	rw	0x0	The destination ID.

EXCEPTION_LOGGING_HEADER0 (Exception Logging Header 0 Register), (0x24)

The Exception Logging Header 0 Register contains the first word of the header.

Bit	Name	Type	Reset	Description
31:24	type_f	r	0x0	Type. 7 = CBASS.
23:8	src_id	r	0x0	Source ID. Always 0.
7:0	dest_id	r	0x0	Destination ID.

EXCEPTION_LOGGING_HEADER1 (Exception Logging Header 1 Register) has offset 0x28.

The Exception Logging Header 1 Register contains the second word of the header.

Bit	Name	Type	Reset	Description
31:24	group	r	0x0	Group. Always 0.
23:16	code	r	0x0	Code. 0 = CBASS decode error.
15:0	reserved	r	0x0	Reserved

EXCEPTION_LOGGING_DATA0 (Exception Logging Data 0 Register) has offset 0x2c.

The Exception Logging Data 0 Register contains the first word of the data.

Bit	Name	Type	Reset	Description
31:0	addr_l	r	0x0	Address lower 32 bits.

EXCEPTION_LOGGING_DATA1 (Exception Logging Data 1 Register), (0x30)

The Exception Logging Data 1 Register contains the second word of the data.

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	addr_h	r	0x0	Address upper 16 bits.

EXCEPTION_LOGGING_DATA2 (Exception Logging Data 2 Register has offset 0x34.

The Exception Logging Data 2 Register contains the third word of the data.

Bit	Name	Type	Reset	Description
31:28	reserved	r	0x0	Reserved
27:16	routeid	r	0x0	Route ID.
15:14	reserved	r	0x0	Reserved
13	write	r	0x0	Write.
12	read	r	0x0	Read.
11	debug	r	0x0	Debug.
10	cacheable	r	0x0	Cacheable.
9	priv	r	0x0	Priv.
8	secure	r	0x0	Secure.
7:0	priv_id	r	0x0	Priv ID.

EXCEPTION_LOGGING_DATA3 (Exception Logging Data 3 Register) has offset 0x38.

The Exception Logging Data 3 Register contains the fourth word of the data.

Bit	Name	Type	Reset	Description
31:10	reserved	r	0x0	Reserved

Bit	Name	Type	Reset	Description
9:0	bytecnt	r	0x0	Byte count.

ERR_INTR_RAW_STAT (Global Interrupt Raw Status Register), (0x50)

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr	rw1ts	0x0	Level Interrupt status

ERR_INTR_ENABLED_STAT (Global Interrupt Enabled Status Register), (0x54)

The interrupt status register is gated by the interrupt enable

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	enabled_intr	rw1tc	0x0	Level Enabled Interrupt status

ERR_INTR_ENABLE_SET (Interrupt Enable Set Register), (0x58)

Only when this register is set, null access will cause interrupt to be generated.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr_enable_set	rw1ts	0x0	Interrupt Enable Set Register

ERR_INTR_ENABLE_CLR (Interrupt Enable Clear Register), (0x5c)

Setting this register disables the null interrupt generation

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr_enable_clr	rw1tc	0x0	Interrupt Enable Clear Register

ERR_EOI (EOI Register), (0x60)

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	eoi_wr	rw	0x0	End Of Interrupt Register

3.4.2 Register MMR for default_exp

All of the registers for default_exp_intr are located in the glb_regs region of the CBASS which supports this feature. For each glb_reg region, the following registers are supported.

Table 3-2. glb_regs for default_exp_intr

Address Offset	Register Mnemonic	Register Name
0x0	PID	Revision Register
0x4	DESTINATION_ID	Destination ID Register
0x20	EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register
0x24	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
0x28	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register

Table 3-2. glb_regs for default_exp_intr (continued)

Address Offset	Register Mnemonic	Register Name
0x2c	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
0x30	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
0x34	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
0x38	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
0x40	EXCEPTION_PEND_SET	Exception Logging Pending Set Register
0x44	EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register

The Revision Register contains the major and minor revisions for the module.

Bit	Name	Type	Reset	Description
31:30	scheme	r	0x1	PID register scheme
29:28	bu	r	0x2	Business Unit: 10 = Processors
27:16	func	r	0x600	Module ID
15:11	rtl	r	0x6	RTL revision. Will vary depending on release.
10:8	major	r	0x1	Major revision
7:6	custom	r	0x0	Custom
5:0	minor	r	0x2	Minor revision

The Destination ID Register defines the destination ID value for error messages.

Bit	Name	Type	Reset	Description
31:8	reserved	r	0x0	Reserved
7:0	dest_id	rw	0x0	The destination ID.

The Exception Logging Control Register controls the exception logging.

Bit	Name	Type	Reset	Description
31:2	reserved	r	0x0	Reserved
1	disable_pend	rw	0x0	Disables logging pending when set.
0	disable_f	rw	0x0	Disables logging when set.

The Exception Logging Header 0 Register contains the first word of the header.

Bit	Name	Type	Reset	Description
31:24	type_f	r	0x0	Type.
23:8	src_id	r	0x0	Source ID.
7:0	dest_id	r	0x0	Destination ID.

The Exception Logging Header 1 Register contains the second word of the header.

Bit	Name	Type	Reset	Description
31:24	group	r	0x0	Group.
23:16	code	r	0x0	Code.
15:0	reserved	r	0x0	Reserved

The Exception Logging Data 0 Register contains the first word of the data.

Bit	Name	Type	Reset	Description
31:0	addr_l	r	0x0	Address lower 32 bits.

The Exception Logging Data 1 Register contains the second word of the data.

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	addr_h	r	0x0	Address upper 16 bits.

The Exception Logging Data 2 Register contains the third word of the data.

Bit	Name	Type	Reset	Description
31:28	reserved	r	0x0	Reserved
27:16	routeid	r	0x0	Route ID.
15:14	reserved	r	0x0	Reserved
13	write	r	0x0	Write.
12	read	r	0x0	Read.
11	debug	r	0x0	Debug.
10	cacheable	r	0x0	Cacheable.
9	priv	r	0x0	Priv.
8	secure	r	0x0	Secure.
7:0	priv_id	r	0x0	Priv ID.

The Exception Logging Data 3 Register contains the fourth word of the data.

Bit	Name	Type	Reset	Description
31:10	reserved	r	0x0	Reserved
9:0	bytecnt	r	0x0	Byte count.

The Exception Logging Pending Set Register allows to set the pend signal.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_set	rw1ts	0x0	Write a 1 to set the exception pend signal.

The Exception Logging Pending Clear Register allows to clear the pend signal.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_clr	rw1tc	0x0	Write a 1 to clear the exception pend signal.

3.5 IO Coherency Support

The SoC has limited IO Coherency support through the ACP interface of the MPU Cluster. Sending transactions to the ACP interface allows those transactions, outside of the MPU cluster, to directly go through the shared L2 cache controller. There are two types of cache operations supported through ACP: write allocation and write through. Read through ACP interface has no impact on the cache operation. The main function of the ACP interface is to allow write transactions from the SoC side to push data directly into the MPU's L2 cache. Therefore, the MPU can access this data much faster from the L2 cache rather than fetching it from system memory, while still maintaining the cache coherency.

Not all initiators have the capability to send transactions to ACP interface for IO coherency. This feature is limited to a subset of the initiators such as BCDMA, pktDMA, and some high-speed peripherals such as USB and EMMC. The transactions sent to the ACP interface must have the ASEL value set to either 14 or 15.

- Write transactions with ASEL=14 cause MPU L2 cache allocation: for cache warming feature
- Write transactions with ASEL=15 do not cause MPU A53SS L2 cache allocation
- Read transactions with ASEL=14 and 15 do not cause L2 cache allocation
  - All the transactions to ACP port can be protected by firewall if firewall is inserted by the SoC level interconnect

By default, all transactions have ASEL set to zero. For any transactions from pktDMA and BCDMA, the ASEL can be set as part of the DMA configuration. For all other transactions, the ASEL value can be set through QoS MMR. For more details, see Quality of Service (QoS) Block.

Not all initiators have a connection to the ACP interface. MPU A53SS, DebugSS and Security Manager do not have access to ACP interfaces even with the ASEL value set to 14 or 15.

3.6 Quality of Service (QoS) Block

CBASS arbitrates the transaction based on priority from high to low. If the transactions going to the same end point have the same priority, then the CBASS uses round robin method for these transactions.

In the CBASS with parallel paths, orderID is used to determine how the transactions are forwarded to those parallel paths. The parallel paths are defined as two target interfaces with the exact same memory map assignment.

By default, all the target interfaces have a certain address assigned and CBASS routes the transactions based on this address. However, some of the special target interfaces can be routed through a different mechanism using the ASEL signal, such as MPU A53SS’s ACP interface and PCIe target interfaces.

By default, the majority of the transactions default to the lowest priority level, ASEL value to zero and orderID to zero. The transactions from BCDMA and pktDMA have those attributes as part of the DMA configuration. ASEL value is part of the address information passed to the DMA engine. It is normally specified in descriptors such as host packet descriptor and host buffer descriptor for pktDMA, and Transfer Request (TR) packet descriptor for BCDMA. The priority and orderID information can be configured through each DMA channel’s priority control register.

For the rest of the initiators, the CBASS IP provides QoS block to allow the user to program the transaction’s attributes such as priority level, ASEL coding and orderID.

The QoS block programming is through CBASS’s qos_regs region. Each initiator, except the BCDMA, pktDMA, and debugss, has an MMR to allow the user to set the priority, ASEL, and orderID value. There is another exception on priority setting. The display IP implements dynamic priority schedule based on the FIFO threshold. The QoS block inside CBASS does not have the ability to overwrite the priority value coming from the display IP.

Section 3.6.2 shows the mapping between initiators and QoS block physical addresses.

Each QoS block has one 4B MAP register per channel that allows the user to program ASEL, orderID, and priority. The first MAP register is at offset 0x100 and the MAP register for channel X is located at offset 0x100+400x. See Section 3.6.1 .

For any write to address range 0x4500_0000 to 0x45FF_FFFF, it is recommended to read back the value after the write to make sure the write landed. The registers in this regions are mainly for firewall configuration, ISC/DMA credential configuration, QoS MMR configuration.

On QoS MMR configuration, in order to configure certain transaction to be the highest priority, the priority field needs to be set to zero for that transaction. In order to make sure that priority field is indeed to set to zero, the following sequence should be followed:

1. Read the priority field, if it is non-zero value, follow a write to overwrite priority field to be 0x0.

2. If read back priority field is zero, write to QoS MMR register to set priority field to be 0x7. Read back the same priority field. If the read back value is 0x7, write to QoS MMR register to set priority field to be 0x0. If the read back value is 0x0, it means this register is not implemented and priority setting is not working.

3.6.1 QoS Block MMR

Each QoS block has one 4B MAP register per channel. It defines ASEL, orderID and priority field user can program. The first MAP register is at offset 0x100 and the MAP register for channel X is located at offset 0x100+4*x.

Bit	Name	Type	Reset	Description
31:30	reserved	r	0x0	Reserved
29:28	atype	rw	0x0	atype signal for channel N. 0 = physical. 1 = intermediate. 2 = virtual. 3 = physical with coherence. Keep it as default value. Do not program it to different value.
27:16	virtid	rw	0x0	virtid signal for channel N. Shall be 0x0.
15	reserved	r	0x0	Reserved
14:12	epriority	rw	0x7	epriority signal for channel N. 0x7 is the lowest priority, 0x0 is the highest priority.
11:8	asel	rw	0x0	ASEL signal for channel N. Default to zero. Set to either 0xE or 0xF for IO coherency transactions.
7:4	orderid	rw	0x0	orderid signal for channel N. Default to zero and keep it to 0x0.
3	reserved	r	0x0	Reserved
2:0	qos	rw	0x0	qos signal for channel N. Not used. No impacted if it is programed to different value.

3.6.2 QoS Summary Table

Table 3-3. QoS Summary Table

Initiator	QoS Index	Channel Count	Virtual ID Capable	Order ID Capable	Transaction Priority Capable	Address Type Capable	Asel Capable	QoS Block Physical Address
WKUP_R5FSS0_CPU0_RMST	80	1	N	Y	Y	N	Y	0x45D14000
WKUP_R5FSS0_CPU0_WMST	81	1	N	Y	Y	N	Y	0x45D14400
WKUP_R5FSS0_CPU0_PMST	82	1	N	Y	Y	N	Y	0x45D14800
MCU_R5FSS0_CPU0_RMST	96	1	N	Y	Y	N	Y	0x45D18000
MCU_R5FSS0_CPU0_WMST	97	1	N	Y	Y	N	Y	0x45D18400
MCU_R5FSS0_CPU0_PMST	98	1	N	Y	Y	N	Y	0x45D18800
COMPUTE_CLUSTER0_A53_QUAD_WRAP_CBA_AXI_R	129	1	N	Y	Y	N	Y	0x45D20400
COMPUTE_CLUSTER0_A53_QUAD_WRAP_CBA_AXI_W	130	1	N	Y	Y	N	Y	0x45D20800
DEBUGSS_WRAP0_VBUSMW	134	1	N	Y	Y	N	Y	0x45D21800
DEBUGSS_WRAP0_VBUSMR	135	1	N	Y	Y	N	Y	0x45D21C00
GICSS0_MEM_WR_VBUSM	136	1	N	Y	Y	N	Y	0x45D22000
GICSS0_MEM_RD_VBUSM	137	1	N	Y	Y	N	Y	0x45D22400
MMCSD0_EMMCSDSS_RD	138	1	N	Y	Y	N	Y	0x45D22800
MMCSD0_EMMCSDSS_WR	139	1	N	Y	Y	N	Y	0x45D22C00
MMCSD1_EMMCSDSS_RD	140	1	N	Y	Y	N	Y	0x45D23000
MMCSD1_EMMCSDSS_WR	141	1	N	Y	Y	N	Y	0x45D23400
MMCSD2_EMMCSDSS_WR	142	1	N	Y	Y	N	Y	0x45D23800
MMCSD2_EMMCSDSS_RD	143	1	N	Y	Y	N	Y	0x45D23C00
USB0_MSTW0	144	1	N	Y	Y	N	Y	0x45D24000
USB0_MSTR0	145	1	N	Y	Y	N	Y	0x45D24400
USB1_MSTR0	146	1	N	Y	Y	N	Y	0x45D24800
USB1_MSTW0	147	1	N	Y	Y	N	Y	0x45D24C00
SA3_SS0_CTXCACH_EXT_DMA	149	1	N	Y	Y	N	Y	0x45D25400
C7X256V0_C7XV_SOC	158	2	N	Y	N	N	N	0x45D27800

3.7 Route ID

The route ID is used by the interconnect to route return status and data back to the transaction initiator. Each initiator has one or multiple unique route IDs assigned to it. The route ID has no other usage. There are no software controls for the route ID. The initiator-to-route-ID assignment is shown in Section 3.7.1 .

3.7.1 Route ID Table

Table 3-4. Route ID Table

Module Name	Initiator Interface	Which CBASS it is connected to	Route ID	Physical Address
COMPUTE_CLUSTER0	A53_QUAD_WRAP_CBA_AXI_W	CBASS0	0 - 7	0x45D20800
COMPUTE_CLUSTER0	A53_QUAD_WRAP_CBA_AXI_R	CBASS0	16 - 23	0x45D20400
C7X256V0	C7XV_SOC	CBASS0	32 - 39	0x45D27800
MMCSD0	EMMCSDSS_WR	CBASS0	256	0x45D22C00
MMCSD0	EMMCSDSS_RD	CBASS0	257	0x45D22800
DEBUGSS_WRAP0	VBUSMR	CBASS0	258	0x45D21C00
DEBUGSS_WRAP0	VBUSMW	CBASS0	259	0x45D21800
MMCSD1	EMMCSDSS_WR	CBASS0	269	0x45D23400
MMCSD1	EMMCSDSS_RD	CBASS0	270	0x45D23000
MMCSD2	EMMCSDSS_WR	CBASS0	271	0x45D23800
MMCSD2	EMMCSDSS_RD	CBASS0	272	0x45D23C00
SA3_SS0	CTXCACH_EXT_DMA	CBASS0	277	0x45D25400
GICSS0	MEM_WR_VBUSM	CBASS0	302	0x45D22000
GICSS0	MEM_RD_VBUSM	CBASS0	303	0x45D22400
USB0	MSTR0	CBASS0	304	0x45D24400
USB0	MSTW0	CBASS0	305	0x45D24000
USB1	MSTR0	CBASS0	306	0x45D24800
USB1	MSTW0	CBASS0	307	0x45D24C00
WKUP_R5FSS0	CPU0_RMST	WKUP_CBASS0	4088	0x45D14000
WKUP_R5FSS0	CPU0_WMST	WKUP_CBASS0	4089	0x45D14400
WKUP_R5FSS0	CPU0_PMST	WKUP_CBASS0	4090	0x45D14800
MCU_R5FSS0	CPU0_RMST	MCU_CBASS0	4092	0x45D18000
MCU_R5FSS0	CPU0_WMST	MCU_CBASS0	4093	0x45D18400
MCU_R5FSS0	CPU0_PMST	MCU_CBASS0	4094	0x45D18800

3.8 ISC and Firewall

There are two basic building blocks to achieve security isolation on the SoC level: firewall block and ISC block.

3.8.1 Initiator-Side Security Controls (ISC)

The purpose of the ISC block is to provide a mechanism to either add or overwrite the attributes of the transaction, such as privID, priv, and secure. Each transaction in the system carries those attributes, either driven internally by the IP, or added/modified by the ISC block for that initiator.

All the transactions coming from pktDMA, BCDMA, and DMSS_crypto, the privID, priv, and secure attributes are driven internally by the DMA engine. There is no ISC block to override the values for these transactions. For the transactions from pktDMA, BCDMA, and XLCDMA, the secure, priv, and privID values are determined by the credential register for each DMA flow.

Transactions from all other initiators, attributes can be added or overridden by the ISC block.

The majority of the ISC blocks only contain one region, therefore all the transactions through that ISC block share the same ISC setting. There are a few ISC blocks supporting either multiple channels or multiple regions. The default setting for those ISC blocks with multiple channels, or multiple regions, are the same. However, the transaction attributes can be modified in a finer granularity by utilizing the multiple channel/region mode. If the channel mode is enabled, the starting address and the end address MMRs should be programmed to the starting and end channel number for that ISC region. If the region mode is enabled, the starting and end address MMRs are the address range the transactions are sent to.

Section 3.8.1.1 shows the default setting for privID/priv setting. It is recommended not to change those settings except some specific conditions.

3.8.1.1 ISC and Priv-ID

Table 3-5. ISC and Priv-ID

Default Priv ID	Inititator	ISC Interface	ISC ID	MMR Base Address	Region Count
4	COMPUTE_CLUSTER0	A53_QUAD_WRAP_CBA_AXI_R	129	0x45820400	1
		A53_QUAD_WRAP_CBA_AXI_W	130	0x45820800	1
32	C7X256V0	C7XV_SOC	158	0x45827800	2
96	MCU_R5FSS0	CPU0_RMST	96	0x45818000	4
		CPU0_WMST	97	0x45818400	4
		CPU0_PMST	98	0x45818800	4
128	MMCSD0	EMMCSDSS_RD	138	0x45822800	1
		EMMCSDSS_WR	139	0x45822C00	1
129	MMCSD1	EMMCSDSS_RD	140	0x45823000	1
		EMMCSDSS_WR	141	0x45823400	1
130	MMCSD2	EMMCSDSS_WR	142	0x45823800	1
		EMMCSDSS_RD	143	0x45823C00	1
152	SA3_SS0	CTXCACH_EXT_DMA	149	0x45825400	1
154	GICSS0	MEM_WR_VBUSM	136	0x45822000	1
		MEM_RD_VBUSM	137	0x45822400	1
155	USB0	MSTW0	144	0x45824000	1
		MSTR0	145	0x45824400	1
156	USB1	MSTR0	146	0x45824800	1
		MSTW0	147	0x45824C00	1
177	DEBUGSS_WRAP0	VBUSMW	134	0x45821800	1
		VBUSMR	135	0x45821C00	1
212	WKUP_R5FSS0	CPU0_RMST	80	0x45814000	4
		CPU0_WMST	81	0x45814400	4
		CPU0_PMST	82	0x45814800	4

3.8.1.2 ISC Registers

CBASS ISC Registers are described in Table 3-6.

Each ISC block contains a set of MMRs for each region/channel: Control MMR, start address, and end address. If an ISC block is configured to have x region/channels, this ISC block contains x+1 sets of MMRs.

Table 3-6. ISC Registers

Address Offset	Register Mnemonic	Register Name
(b*0x20), b=0..31	REGION[b]_CONTROL	ISC a Region b Control Register
(b*0x20)+0x10, b=0..31	REGION[b]_START_ADDR_L	ISC a Region b Start Address Low Register
(b*0x20)+0x14, b=0..31	REGION[b]_START_ADDR_H	ISC a Region b Start Address High Register

Table 3-6. ISC Registers (continued)

Address Offset	Register Mnemonic	Register Name
(b*0x20)+0x18, b=0..31	REGION[b]_END_ADDR_L	ISC a Region b End Address Low Register
(b*0x20)+0x1c, b=0..31	REGION[b]_END_ADDR_H	ISC a Region b End Address High Register

Each ISC can be configured in one of two modes: region mode and channel mode.

When the region mode is configured, the start and end address MMRs shall be programmed with an SoC address range.

When ISC is configured as channel mode, the start and end address MMRs shall be programmed using channel number.

Each region and channel can be configured to determine whether to overwrite or add values for priv, privID, and secure attributes. A default value for the control MMR, located at offset x*0x20, is used so that transactions do not map to a valid region.

The following is the SW sequence to modify the default ISC setting for region/channel b:

- If channel mode is needed, set ch_mode field to 0x1. Program the start and end address MMRs to be the channel ID
- If region mode is needed, set ch_mode field to be 0x0. Program the start and the end address MMRs to match the address range.
- Set enable field to be 0xA
- If lock field is set to 0x1, then this control MMR can’t be changed until it is reset to 0x0
- PrivID: if the transaction carries privID attribute, ISC can either direct use the privID attribute from the transaction by setting the pass field to 0x0, or overwrite it using the new value define in this control register by setting the pass field to be 0x1. If the transaction does not have privID attribute, the ISC will add the privID to this transaction, regardless of the value in the pass field.
- Secure attribute: the transaction can either be forced to be non-secure mode by setting nonsec field to be 0x1, or force the transaction to be secure by setting sec field to be 0xA, or just pass through the secure attribute if the original transaction carries secure attribute. For an initiator which does not provide secure attributes, it is default set to non-secure.
- Priv attribute: by default priv attribute is not set. ISC can be used to overwrite priv attribute either to be user mode by setting nopri field to 0xF, or supervisor mode by setting priv field to be 0xF

3.8.2 Transaction Attributes for BCDMA and PktDMA Transactions

Section 3.6 and Section 3.8.1 provide information on how to set up the attributes on the generic transaction. But the BCDMA and pktDMA transactions do not rely on the ISC block and QoS block to set the transaction attributes. Instead, those attributes are determined by the various DMA configuration registers:

Table 3-7. BCDMA and PktDMA Transaction Attributes

	How to configure BCDMA/PktDMA Transactions	Link
ASEL	descriptors: host packet descriptor and host buffer descriptor for pktDMA and Transfer Request (TR) descriptors for BCDMA	See DMASS Transfer Request Descriptor
priority	channel priority control register	See Channel Priority Control Register
orderID	channel priority control register	
secure	flow credential registers	See Flow Credential Register
priv	flow credential registers	
privID	flow credential registers	
atype	channel configuration MMR. Fixed to 2b'00	

3.8.3 Firewall Block

There are two types of firewall: region based firewall and channelized firewall.

The channelized firewall is only implemented to protect the registers which control the power domain and LPSC for security enclave. User can’t modify the channelized firewall setting.

Region based firewalls are inserted at the target end point in the interconnect. Normally a group of the target interfaces share one region-based firewall. Each region-based firewall has its unique configuration of:

- FWID: this is a unique index of firewall block.
- Number of protected regions: this is to indicate how many protected regions users can define and program
- Memory regions behind this firewall: transactions sent to those memory regions will go through this firewall protection

Majority of the memory regions in the SoC are protected by region-based firewalls, except the public boot ROM, debug cell, and STM.

Section 3.8.3.1 shows the firewall summary on SoC.

3.8.3.1 Region Based Firewalls

Table 3-8. Region Based Firewalls

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	DDR32SS0	0	3	8	0x45000000	DDR32SS0	SDRAM	0x80000000	0xFFFFFFFF	No
CBASS0	DDR32SS0	0	3	8	0x45000000	DDR32SS0	SDRAM	0x880000000	0x8FFFFFFFF	No
CBASS0	DDR32SS0	0	3	8	0x45000000	DDR32SS0	SDRAM	0x900000000	0x9FFFFFFFF	No
CBASS0	DDR32SS0	0	3	8	0x45000000	DDR32SS0	SDRAM	0xA00000000	0xBFFFFFFFF	No
CBASS0	DDR32SS0	0	3	8	0x45000000	DDR32SS0	SDRAM	0xC00000000	0xFFFFFFFFF	No
CBASS0	DDR32SS0	1	3	16	0x45000400	DDR32SS0	SDRAM	0x80000000	0xFFFFFFFF	No
CBASS0	DDR32SS0	1	3	16	0x45000400	DDR32SS0	SDRAM	0x880000000	0x8FFFFFFFF	No
CBASS0	DDR32SS0	1	3	16	0x45000400	DDR32SS0	SDRAM	0x900000000	0x9FFFFFFFF	No
CBASS0	DDR32SS0	1	3	16	0x45000400	DDR32SS0	SDRAM	0xA00000000	0xBFFFFFFFF	No
CBASS0	DDR32SS0	1	3	16	0x45000400	DDR32SS0	SDRAM	0xC00000000	0xFFFFFFFFF	No
CBASS0	COMPUTE_CLUSTER0	2	3	8	0x45000800	COMPUTE_CLUSTER0				Yes
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	ROM_TABLE_0_0	0x700000000	0x700000FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV0_0	0x700001000	0x700001FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CFGAP0	0x700002000	0x7000020FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	APBAP0	0x700002100	0x7000021FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	AXIAP0	0x700002200	0x7000022FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	PWRAP0	0x700002300	0x7000023FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	PVIEW0	0x700002400	0x7000024FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	JTAGAP0	0x700002500	0x7000025FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	SECAP0	0x700002600	0x7000026FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX0_CFG0	0x700002700	0x7000027FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX1_CFG0	0x700002800	0x7000028FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX2_CFG0	0x700002900	0x7000029FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX3_CFG0	0x700002A00	0x700002AFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX4_CFG0	0x700002B00	0x700002BFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX5_CFG0	0x700002C00	0x700002CFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX6_CFG0	0x700002D00	0x700002DFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX7_CFG0	0x700002E00	0x700002EFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX8_CFG0	0x700002F00	0x700002FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV1_0	0x700003000	0x700003FFF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV2_0	0x700004000	0x702003FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	ROM_TABLE_1_0	0x720000000	0x720000FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	cscti	0x720001000	0x720001FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	DRM0	0x720002000	0x720002FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV3_0	0x720003000	0x720003FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CSTPIU0	0x720004000	0x720004FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CTF0	0x720005000	0x720005FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV4_0	0x720006000	0x721005FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	EXT_APB0	0x730000000	0x73FFFFFFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	ROM_TABLE_0_1	0x740000000	0x740000FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV0_1	0x740001000	0x740001FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CFGAP1	0x740002000	0x7400020FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	APBAP1	0x740002100	0x7400021FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	AXIAP1	0x740002200	0x7400022FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	PWRAP1	0x740002300	0x7400023FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	PVIEW1	0x740002400	0x7400024FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	JTAGAP1	0x740002500	0x7400025FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	SECAP1	0x740002600	0x7400026FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX0_CFG1	0x740002700	0x7400027FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX1_CFG1	0x740002800	0x7400028FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX2_CFG1	0x740002900	0x7400029FF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX3_CFG1	0x740002A00	0x740002AFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX4_CFG1	0x740002B00	0x740002BFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX5_CFG1	0x740002C00	0x740002CFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX6_CFG1	0x740002D00	0x740002DFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX7_CFG1	0x740002E00	0x740002EFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CORTEX8_CFG1	0x740002F00	0x740002FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV1_1	0x740003000	0x740003FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV2_1	0x740004000	0x742003FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	ROM_TABLE_1_1	0x760000000	0x760000FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	cscti	0x760001000	0x760001FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	DRM1	0x760002000	0x760002FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV3_1	0x760003000	0x760003FFF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CSTPIU1	0x760004000	0x760004FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	CTF1	0x760005000	0x760005FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	RESV4_1	0x760006000	0x761005FFF	No
CBASS0	DEBUGSS_WRAP0	3	3	4	0x45000C00	DEBUGSS_WRAP0	EXT_APB1	0x770000000	0x77FFFFFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	UMC	0x7C000000	0x7C01FFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CLEC	CLEC	0x7C200000	0x7C2FFFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU	0x7C400000	0x7C403FFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_SET	0x7C404000	0x7C407FFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_QUEUE	0x7C408000	0x7C40FFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_CHNRT	0x7C440000	0x7C45FFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_CHRT	0x7C460000	0x7C47FFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_CHATOMIC_DEBUG	0x7C480000	0x7C49FFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	DRU_CHCORE	0x7C4A0000	0x7C4BFFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	dru	0x7C4E0000	0x7C4FFFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	UMC_MEM_MAIN	0x7E000000	0x7E0FFFFF	No
CBASS0	C7X256V0_CORE0	4	3	8	0x45001000	C7X256V0_CORE0	UMC_MEM_AUX	0x7F000000	0x7F03FFFF	No
CBASS0	GPMC0	6	3	8	0x45001800	GPMC0	CFG	0x3B000000	0x3B0003FF	No
CBASS0	GPMC0	6	3	8	0x45001800	GPMC0	DATA	0x50000000	0x57FFFFFF	No
CBASS0	FSS0_FSAS_0	7	3	8	0x45001C00	FSS0_FSAS_0	DAT_REG0	0x400000000	0x4FFFFFFFF	No
CBASS0	FSS0_FSAS_0	7	3	8	0x45001C00	FSS0_FSAS_0	DAT_REG3	0x500000000	0x5FFFFFFFF	No
CBASS0	FSS0_FSAS_0	7	3	8	0x45001C00	FSS0_FSAS_0	DAT_REG1	0x60000000	0x67FFFFFF	No
CBASS0	PDMA0	8	3	16	0x45002000	PDMA0	REGS	0x00C00000	0x00C003FF	No
CBASS0	DMASS0_ECC_AGGR_0	9	3	32	0x45002400	DMASS0_ECC_AGGR_0	ECCAGGR	0x3F005000	0x3F0053FF	No
CBASS0	CBASS_DBG0	10	3	16	0x45002800	CBASS_DBG0	ERR	0x00200000	0x002003FF	No
CBASS0	CBASS_MCASP0	11	3	16	0x45002C00	CBASS_MCASP0	ERR	0x00240000	0x002403FF	No
CBASS0	MCRC64_0	13	3	1	0x45003400	MCRC64_0	REGS	0x30300000	0x30300FFF	No
CBASS0	MCASP0	14	3	8	0x45003800	MCASP0	CFG	0x02B00000	0x02B01FFF	No
CBASS0	MSRAM_64K0	15	3	16	0x45003C00	MSRAM_64K0	RAM	0x43C40000	0x43C4FFFF	No
CBASS0	MSRAM_64K0	15	3	16	0x45003C00	MSRAM_64K0	RAM	0x70000000	0x7000FFFF	No
WKUP_CBASS0	WKUP_R5FSS0_CORE0	32	3	4	0x45008000	WKUP_R5FSS0_CORE0	CORE0_ICACHE	0x74000000	0x747FFFFF	No
WKUP_CBASS0	WKUP_R5FSS0_CORE0	32	3	4	0x45008000	WKUP_R5FSS0_CORE0	CORE0_DCACHE	0x74800000	0x74FFFFFF	No
WKUP_CBASS0	WKUP_R5FSS0_CORE0	32	3	4	0x45008000	WKUP_R5FSS0_CORE0	CORE0_ATCM	0x78000000	0x78007FFF	No
WKUP_CBASS0	WKUP_R5FSS0_CORE0	32	3	4	0x45008000	WKUP_R5FSS0_CORE0	CORE0_BTCM	0x78100000	0x78107FFF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
WKUP_CBASS0	PSRAMECC0	33	3	16	0x45008400	PSRAMECC0	RAM	0x00000000	0x000003FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_GTC0	CFG0	0x00A80000	0x00A803FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_GTC0	CFG1	0x00A90000	0x00A93FFF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_GTC0	CFG2	0x00AA0000	0x00AA3FFF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_GTC0	CFG3	0x00AB0000	0x00AB3FFF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_VTM0	VTM_CFG1	0x00B00000	0x00B003FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_VTM0	VTM_CFG2	0x00B01000	0x00B013FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_VTM0	ECCAGGR_CFG	0x00B02000	0x00B023FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_RTI0	CFG	0x2B000000	0x2B0000FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_RTCSS0	RTC	0x2B1F0000	0x2B1F007F	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_I2C0	CFG	0x2B200000	0x2B2000FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_UART0	MEM	0x2B300000	0x2B3001FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_CBASS0	ERR	0x2B400000	0x2B4003FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_PBIST0	MEM	0x2B500000	0x2B5003FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_PBIST1	MEM	0x2B510000	0x2B5103FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_ECC_AGGR0	REGS	0x2B600000	0x2B6003FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_ECC_AGGR1	REGS	0x2B601000	0x2B6013FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_PSRAMECC_8K0	REGS	0x2B608000	0x2B6083FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_R5FSS0_COMMON0	EVNT_BUS_VBUSP_MMRS	0x3C018000	0x3C0180FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_R5FSS0_COMMON0	CORE0_ECC_AGGR	0x3F00D000	0x3F00D3FF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_PSRAMECC_8K0	RAM	0x41880000	0x41887FFF	No
WKUP_CBASS0	WKUP_GTC0	34	3	16	0x45008800	WKUP_CTRL_MMR0	CFG0	0x43000000	0x4301FFFF	No
WKUP_CBASS0	WKUP_PSC0	35	3	16	0x45008C00	WKUP_PSC0	psc	0x04000000	0x04000FFF	No
WKUP_CBASS0	MCU_TIMEOUT0	36	3	8	0x45009000	MCU_TIMEOUT0	CFG	0x04301000	0x043013FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	CBASS_FW0	ERR	0x00220000	0x002203FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	CBASS_IPCSS0	ERR	0x00230000	0x002303FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SA3_SS0_SA_UL_0	ECC_AGGR	0x00712000	0x007123FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	MAILBOX0_MAILBOX_CLUSTER_0	REGS0	0x29000000	0x290001FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	MAILBOX0_MAILBOX_CLUSTER_1	REGS1	0x29010000	0x290101FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	MAILBOX0_MAILBOX_CLUSTER_2	REGS2	0x29020000	0x290201FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	MAILBOX0_MAILBOX_CLUSTER_3	REGS3	0x29030000	0x290301FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SPINLOCK0	REGS	0x2A000000	0x2A007FFF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	ECC_AGGR1	REGS	0x3F00E000	0x3F00E3FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	ECC_AGGR0	REGS	0x3F00F000	0x3F00F3FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	CBASS_CENTRAL2	ERR	0x3F012000	0x3F0123FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SA3_SS0_SA_UL_0	REGS	0x40900000	0x40900FFF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SA3_SS0_SA_UL_0	MMRA	0x40901000	0x409011FF	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SA3_SS0_SA_UL_0	EIP_76	0x40910000	0x4091007F	No
CBASS_CENTRAL2	CBASS_FW0	66	3	4	0x45010800	SA3_SS0_SA_UL_0	EIP_29T2	0x40920000	0x4092FFFF	No
AM62A_PSC_CHFW_CBASS	PSC0	128	3	5	0x45020000	PSC0	psc	0x00400A6C	0x00400A6F	No
AM62A_PSC_CHFW_CBASS	PSC0	128	3	5	0x45020000	PSC0	psc	0x00400A74	0x00400A77	No
AM62A_PSC_CHFW_CBASS	PSC0	128	3	5	0x45020000	PSC0	psc	0x00400A78	0x00400A7B	No
AM62A_PSC_CHFW_CBASS	PSC0	128	3	5	0x45020000	PSC0	psc	0x00400A7C	0x00400A7F	No
AM62A_PSC_CHFW_CBASS	PSC0	128	3	5	0x45020000	PSC0	psc	0x00400A80	0x00400A83	No
CBASS_IPCSS0	DMASS0_SEC_PROXY_0	160	3	8	0x45028000	DMASS0_SEC_PROXY_0	SEC_PROXY_SRC_TARGET_DATA	0x4D000000	0x4D07FFFF	No
CBASS_IPCSS0	SA3_SS0_SEC_PROXY_0	161	3	8	0x45028400	SA3_SS0_SEC_PROXY_0	SEC_PROXY_SRC_TARGET_DATA	0x43600000	0x4360FFFF	No

3.8.3.2 Region Based Firewall Programming

Each firewall block can be configured to support multiple regions and each region can be configured individually. See Section 3.8.3.1 .

Chapter 4

Module Integration

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4.1 Memory Controllers

4.1.1 DDR32 Subsystem (DDR32SS)

This section contains the integration details for the 32-bit DDR module on this device. For Further information, see the DDR32 Subsystem (DDR32SS) section of the Processors and Accelerators chapter

4.1.1.1 DDR32SS Unsupported Features

The following features are not supported on this family of devices:

- DDR3, DDR3L, DDR3U, and LPDDR4x Devices
- Two independent 16-bit channels for LPDDR4
- DIMMS
- Data bus obfuscation / data encryption
- Fail-safe reset I/O to maintain reset state during SoC power OFF
- Automatic periodic scrubbing of SDRAM for ECC
- Coherence of transactions arriving across the RT and NRT bus interfaces
- Maximum of 17 row bits are supported for LPDDR4. LPDDR4 with 18 row bits are not supported
- LPDDR4 devices with byte mode die configurations
- The ECC engine of the DDR controller
- 1T command timing (only 2T timing is supported)

4.1.1.2 DDR32SS Frequency Change

It is not possible to execute DDR frequency change code from DDR while the DDR frequency change procedure is in progress. Frequency change requires multiple steps and during these steps the DDR contents are not accessible from the SOC. Therefore any code that implements the frequency change procedure needs to execute from memory other than DDR.

4.1.1.3 ddr32ss Integration

Table 4-1. DDR32SS Module Allocations

Instance	MAIN	MCU	WKUP
DDR32SS0	✓		

Table 4-2. Integration Attributes for ddr32ss

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DDR32SS0	PSC0	PD_DDR	LPSC_EMIF_local	60	OFF	YES	LPSC_main_IP

Table 4-3. Clock Integration for ddr32ss

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DDR32SS0	DDRSS_DDR_PLL_CLK	MAIN_PLL12_HSDIV0_CLKOUT		None
DDR32SS0	PLL_CTRL_CLK	MAIN_SYSCLK0		None

Table 4-4. Reset Integration for ddr32ss

Module Instance	Source	Description
DDR32SS0	PSC0	DDR32SS0 reset

Table 4-5. Hardware Requests for ddr32ss

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DDR32SS0	DDR32SS0_ddrss_controller_0	GICSS0_spi_151	GICSS0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_controller_0	WKUP_R5FSS0_CORE0_intr_151	WKUP_R5FSS0_CORE0	DDR32SS0 interrupt request	level

Table 4-5. Hardware Requests for ddr32ss (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DDR32SS0	DDR32SS0_ddrss_controller_0	MCU_R5FSS0_CORE0_cpu0_intr_151	MCU_R5FSS0_CORE0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_controller_0	C7X256V0_CLEC_gic_spi_119	C7X256V0_CLEC	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_dram_ecc_corr_err_lvl_0	ESM0_esm_lvl_event_174	ESM0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_dram_ecc_uncorr_err_lvl_0	ESM0_esm_lvl_event_175	ESM0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_pll_freq_change_req_0	GICSS0_spi_172	GICSS0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_pll_freq_change_req_0	WKUP_R5FSS0_CORE0_intr_181	WKUP_R5FSS0_CORE0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_pll_freq_change_req_0	MCU_R5FSS0_CORE0_cpu0_intr_181	MCU_R5FSS0_CORE0	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_pll_freq_change_req_0	C7X256V0_CLEC_gic_spi_140	C7X256V0_CLEC	DDR32SS0 interrupt request	level
DDR32SS0	DDR32SS0_ddrss_v2a_other_err_lvl_0	ESM0_esm_lvl_event_176	ESM0	DDR32SS0 interrupt request	level

4.2 Processors and Accelerators

4.2.1 Arm Cortex A53 Subsystem (A53SS)

This section contains the integration details for the A53SS module on this device. For further information, see the *Arm Cortex A53 Subsystem (A53SS)* section of the *Processors and Accelerators* chapter.

4.2.1.1 A53SS Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.2.1.2 A53SS Integration

Table 4-6. A53SS Module Allocations

Instance	MAIN	MCU	WKUP
A53SS0_CORE_0	✓		
A53SS0_CORE_1	✓		
A53SS0_CORE_2	✓		
A53SS0_CORE_3	✓		
A53SS0	✓		

Table 4-7. Integration Attributes for A53SS

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
A53SS0_CORE_0	PSC0	PD_A53_0	LPSC_A53_0	46	OFF	YES	LPSC_A53_cluster_0
A53SS0_CORE_1	PSC0	PD_A53_1	LPSC_A53_1	47	OFF	YES	LPSC_A53_cluster_0
A53SS0_CORE_2	PSC0	PD_A53_2	LPSC_A53_2	48	OFF	YES	LPSC_A53_cluster_0
A53SS0_CORE_3	PSC0	PD_A53_3	LPSC_A53_3	49	OFF	YES	LPSC_A53_cluster_0
A53SS0	PSC0	PD_A53_cluster_0	LPSC_A53_cluster_0	43	OFF	YES	LPSC_main_IP

Table 4-8. Clock Integration for A53SS

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
A53SS0_CORE_0	CLK	MAIN_PLL8_HSDIV0_CLKOUT		None
A53SS0_CORE_1	CLK	MAIN_PLL8_HSDIV0_CLKOUT		None
A53SS0_CORE_2	CLK	MAIN_PLL8_HSDIV0_CLKOUT		None
A53SS0_CORE_3	A53_CORE3_ARM_CLK_CLK	MAIN_PLL8_HSDIV0_CLKOUT		None
A53SS0	COREPAC_ARM_CLK	MAIN_PLL8_HSDIV0_CLKOUT		a53ss clock
A53SS0	PLL_CTRL_CLK	MAIN_SYSCLK0		None

Table 4-9. Reset Integration for A53SS

Module Instance	Source	Description
A53SS0_CORE_0	PSC0	A53SS0_CORE_0 reset
A53SS0_CORE_1	PSC0	A53SS0_CORE_1 reset
A53SS0_CORE_2	PSC0	A53SS0_CORE_2 reset

Table 4-9. Reset Integration for A53SS (continued)

Module Instance	Source	Description
A53SS0_CORE_3	PSC0	A53SS0_CORE_3 reset
A53SS0	PSC0	A53SS0 reset

Table 4-10. Hardware Requests for A53SS

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
A53SS0	A53SS0_cnthpirq0_0	GICSS0_ppi0_0_26	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cnthpirq1_0	GICSS0_ppi0_1_26	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cnthpirq2_0	GICSS0_ppi0_2_26	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cnthpirq3_0	GICSS0_ppi0_3_26	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpnsirq0_0	GICSS0_ppi0_0_30	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpnsirq1_0	GICSS0_ppi0_1_30	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpnsirq2_0	GICSS0_ppi0_2_30	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpnsirq3_0	GICSS0_ppi0_3_30	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpsirq0_0	GICSS0_ppi0_0_29	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpsirq1_0	GICSS0_ppi0_1_29	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpsirq2_0	GICSS0_ppi0_2_29	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntpsirq3_0	GICSS0_ppi0_3_29	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntvirq0_0	GICSS0_ppi0_0_27	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntvirq1_0	GICSS0_ppi0_1_27	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntvirq2_0	GICSS0_ppi0_2_27	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_cntvirq3_0	GICSS0_ppi0_3_27	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_commirq0_0	GICSS0_ppi0_0_22	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_commirq1_0	GICSS0_ppi0_1_22	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_commirq2_0	GICSS0_ppi0_2_22	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_commirq3_0	GICSS0_ppi0_3_22	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq0_0	GICSS0_ppi0_0_24	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq0_0	GICSS0_ppi0_1_17	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq0_0	GICSS0_ppi0_2_17	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq0_0	GICSS0_ppi0_3_17	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq1_0	GICSS0_ppi0_0_18	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq1_0	GICSS0_ppi0_1_24	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq1_0	GICSS0_ppi0_2_18	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq1_0	GICSS0_ppi0_3_18	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq2_0	GICSS0_ppi0_0_19	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq2_0	GICSS0_ppi0_1_19	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq2_0	GICSS0_ppi0_2_24	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq2_0	GICSS0_ppi0_3_19	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq3_0	GICSS0_ppi0_0_20	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq3_0	GICSS0_ppi0_1_20	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq3_0	GICSS0_ppi0_2_20	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ctiirq3_0	GICSS0_ppi0_3_24	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr0_corrected_err_level_0	ESM0_esm_lvl_event_24	ESM0	A53SS0 interrupt request	level

Table 4-10. Hardware Requests for A53SS (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
A53SS0	A53SS0_ecc_eccaggr0_uncorrected_err_level_0	ESM0_esm_lvl_event_94	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr1_corrected_err_level_0	ESM0_esm_lvl_event_25	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr1_uncorrected_err_level_0	ESM0_esm_lvl_event_93	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr2_corrected_err_level_0	ESM0_esm_lvl_event_45	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr2_uncorrected_err_level_0	ESM0_esm_lvl_event_46	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr3_corrected_err_level_0	ESM0_esm_lvl_event_47	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr3_uncorrected_err_level_0	ESM0_esm_lvl_event_48	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr_corepac_corrected_err_level_0	ESM0_esm_lvl_event_26	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_ecc_eccaggr_corepac_uncorrected_err_level_0	ESM0_esm_lvl_event_95	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_exterrirq_0	ESM0_esm_lvl_event_144	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_interrirq_0	ESM0_esm_lvl_event_145	ESM0	A53SS0 interrupt request	level
A53SS0	A53SS0_pmuirq0_0	GICSS0_ppi0_0_23	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_pmuirq1_0	GICSS0_ppi0_1_23	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_pmuirq2_0	GICSS0_ppi0_2_23	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_pmuirq3_0	GICSS0_ppi0_3_23	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_vcpumntirq0_0	GICSS0_ppi0_0_25	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_vcpumntirq1_0	GICSS0_ppi0_1_25	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_vcpumntirq2_0	GICSS0_ppi0_2_25	GICSS0	A53SS0 interrupt request	level
A53SS0	A53SS0_vcpumntirq3_0	GICSS0_ppi0_3_25	GICSS0	A53SS0 interrupt request	level

4.2.1.3 a53_rs_bw_limiter Integration

Table 4-11. A53_RS_BW_LIMITER Module Allocations

Instance	MAIN	MCU	WKUP
A53_RS_BW_LIMITER0	✓		

Table 4-12. Clock Integration for a53_rs_bw_limiter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
A53_RS_BW_LIMITER0	CLK_CLK	MAIN_SYSCLK0		None

4.2.1.4 a53_ws_bw_limiter Integration

Table 4-13. A53_WS_BW_LIMITER Module Allocations

Instance	MAIN	MCU	WKUP
A53_WS_BW_LIMITER1	✓		

Table 4-14. Clock Integration for a53_ws_bw_limiter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
A53_WS_BW_LIMITER1	CLK_CLK	MAIN_SYSCLK0		None

4.2.1.5 Event In Glue Logic

Because the C7xv256 CLEC may not be configured or even enabled in all application scenarios, for backward compatibility with other AM6xx devices, the cpu_event_o is combined with the CLEC event back to the A53SS with an OR gate as showin in Figure 4-1.

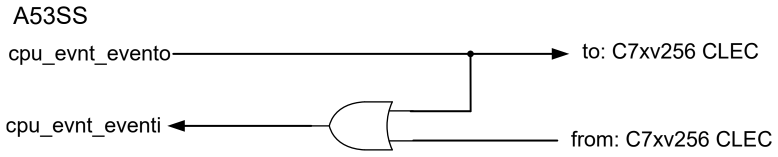

Figure 4-1. A53SS Event Glue Logic

4.2.2 Deep Learning Accelerator (C7X256V)

This section contains the integration details for the Deep Learning Accelerator module on this device.

4.2.2.1 C7X256V Unsupported Features

The following features are not supported on this family of devices:

- C7x native security level (TrustZone equivalent) is not supported and will execute code in non-secure state of C7x.

4.2.2.2 C7x256v Integration

Table 4-15. C7X256V Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0	✓		

4.2.2.3 C7X256V_C7XV_CORE_0 Integration

Table 4-16. C7X256V_C7XV_CORE_0 Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_C7XV_CORE_0	✓		

Table 4-17. Integration Attributes for C7X256V_C7XV_CORE_0

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
C7X256V0_C7XV_CORE_0	PSC0	PD_C7x	LPSC_C7x_core	55	OFF	YES	LPSC_C7x_common

Table 4-18. Clock Integration for C7X256V_C7XV_CORE_0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
C7X256V0_C7XV_CORE_0	C7XV_CLK	MAIN_PLL7_HSDIV0_CLKOUT		None

Table 4-19. Reset Integration for C7X256V_C7XV_CORE_0

Module Instance	Source	Description
C7X256V0_C7XV_CORE_0	PSC0	C7X256V0_C7XV_CORE_0 reset

4.2.2.4 C7X256V_CLEC Integration

Table 4-20. C7X256V_CLEC Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_CLEC	✓		

Table 4-21. Hardware Requests for C7X256V_CLEC

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_arm_0_eventi_out_0	COMPUTE_CLUSTER0_cpu_evnt_eventi_0	COMPUTE_CLUSTER0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event0_194	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event1_194	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event2_194	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	WKUP_R5FSS0_CORE0_intr_116	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	pulse

Table 4-21. Hardware Requests for C7X256V_CLEC (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	MCU_R5FSS0_CORE0_cpu0_intr_116	MCU_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_safety_error_0	ESM0_esm_lvl_event_149	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_0	ESM0_esm_lvl_event_160	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_1	ESM0_esm_lvl_event_161	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_2	ESM0_esm_lvl_event_162	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_3	ESM0_esm_lvl_event_163	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_4	ESM0_esm_lvl_event_164	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_5	ESM0_esm_lvl_event_165	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_6	ESM0_esm_lvl_event_166	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_7	ESM0_esm_lvl_event_167	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_0	GICSS0_spi_280	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_1	GICSS0_spi_281	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_2	GICSS0_spi_282	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_3	GICSS0_spi_283	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_4	GICSS0_spi_284	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_5	GICSS0_spi_285	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_6	GICSS0_spi_286	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_7	GICSS0_spi_287	GICSS0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_8	MCU_R5FSS0_CORE0_cpu0_intr_249	MCU_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_9	MCU_R5FSS0_CORE0_cpu0_intr_250	MCU_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_10	MCU_R5FSS0_CORE0_cpu0_intr_254	MCU_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_11	MCU_R5FSS0_CORE0_cpu0_intr_255	MCU_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_12	WKUP_R5FSS0_CORE0_intr_249	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_13	WKUP_R5FSS0_CORE0_intr_250	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_14	WKUP_R5FSS0_CORE0_intr_254	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_15	WKUP_R5FSS0_CORE0_intr_255	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level

4.2.2.5 C7X256V_CLK Integration

Table 4-22. C7X256V_CLK Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_CLK	✓		

Table 4-23. Clock Integration for C7X256V_CLK

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
C7X256V0_CLK	C7XV_CLK	MAIN_PLL7_HSDIV0_CLKOUT		None
C7X256V0_CLK	PLL_CTRL_CLK	MAIN_SYSCLK0		None

4.2.2.6 C7X256V_CORE0 Integration

Table 4-24. C7X256V_CORE0 Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_CORE0	✓		

Table 4-25. Integration Attributes for C7X256V_CORE0

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
C7X256V0_CORE0	PSC0	PD_C7x	LPSC_C7x_common	57	OFF	YES	LPSC_main_IP

Table 4-26. Clock Integration for C7X256V_CORE0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
C7X256V0_CORE0	DIVH_CLK2_SOC_GCLK	C7X256V0_CLK (INSTANCE)		None
C7X256V0_CORE0	DIVH_CLK4_GCLK	C7X256V0_CLK (INSTANCE)		None
C7X256V0_CORE0	DIVH_CLK4_SOC_GCLK	C7X256V0_CLK (INSTANCE)		None
C7X256V0_CORE0	DIVP_CLK1_GCLK	C7X256V0_CLK (INSTANCE)		None
C7X256V0_CORE0	DIVP_CLK1_SOC_GCLK	C7X256V0_CLK (INSTANCE)		None

Table 4-27. Reset Integration for C7X256V_CORE0

Module Instance	Source	Description
C7X256V0_CORE0	PSC0	C7X256V0_CORE0 reset

4.2.2.7 C7X256V_DEBUG Integration

Table 4-28. C7X256V_DEBUG Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_DEBUG	✓		

4.2.2.8 C7X256V_ECC_AGGR Integration

Table 4-29. C7X256V_ECC_AGGR Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_ECC_AGGR	✓		

4.2.2.9 C7X256V_PBIST Integration

Table 4-30. C7X256V_PBIST Module Allocations

Instance	MAIN	MCU	WKUP
C7X256V0_PBIST	✓		

4.2.2.10 c7xv_rsws_bs_limiter Integration

Table 4-31. C7XV_RSWS_BS_LIMITER Module Allocations

Instance	MAIN	MCU	WKUP
C7XV_RSWS_BS_LIMITER6	✓		

Table 4-32. Clock Integration for c7xv_rsws_bs_limiter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
C7XV_RSWS_BS_LIMITER6	CLK_CLK	MAIN_SYSCLK0		None

4.2.3 Arm Cortex R5F Subsystem (MCU_R5FSS)

This section contains the integration details for the MCU_R5FSS module on this device. For Further information, see the Arm Cortex R5F Subsystem (MCU_R5FSS) section of the Processors and Accelerators chapter

4.2.3.1 MCU_R5FSS Unsupported Features

The following features are not supported on this family of devices:

- Non-Maskable Interrupts (NMI)

4.2.3.2 MCU_R5FSS Integration

Table 4-33. MCU_R5FSS Module Allocations

Instance	MAIN	MCU	WKUP
MCU_R5FSS0		✓	
MCU_R5FSS0_CORE0		✓	
MCU_R5FSS0_COMMON0		✓	

Table 4-34. Integration Attributes for MCU_R5FSS

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCU_R5FSS0_CORE0	WKUP_PSC0	PD_MCUSS	LPSC_mcu_r5	6	OFF	YES	LPSC_MCU_common

Table 4-35. Clock Integration for MCU_R5FSS

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_R5FSS0_CORE0	CPU0_CLK	MCU_PLL0_HSDIV3_CLKOUT		None
MCU_R5FSS0_CORE0	ICLK	MCU_PLL0_HSDIV3_CLKOUT		interface clock

Table 4-36. Reset Integration for MCU_R5FSS

Module Instance	Source	Description
MCU_R5FSS0_CORE0	WKUP_PSC0	MCU_R5FSS0_CORE0 reset

Table 4-37. Hardware Requests for MCU_R5FSS

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_commrx_level_0_0	MCU_R5FSS0_CORE0_cpu0_intr_90	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_commtx_level_0_0	MCU_R5FSS0_CORE0_cpu0_intr_91	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_cti_0	MCU_R5FSS0_CORE0_cpu0_intr_175	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_exp_intr_0	WKUP_ESM0_esm_lvl_event_30	WKUP_ESM0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_exp_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_4	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_pmu_0	MCU_R5FSS0_CORE0_cpu0_intr_94	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_valfiq_0	MCU_R5FSS0_CORE0_cpu0_intr_95	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_cpu0_valirq_0	MCU_R5FSS0_CORE0_cpu0_intr_96	MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0 interrupt request	level
MCU_R5FSS0_COMMON0	MCU_R5FSS0_COMMON0_ecc_de_to_esm_0_0	WKUP_ESM0_esm_lvl_event_28	WKUP_ESM0	MCU_R5FSS0_COMMON0 interrupt request	level

Table 4-37. Hardware Requests for MCU_R5FSS (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_R5FSS0_COMMON0	MCU_R5FSS0_COMMON0_ecc_se_to_esm_0_0	WKUP_ESM0_esm_lvl_event_29	WKUP_ESM0	MCU_R5FSS0_COMMON0 interrupt request	level

4.2.4 Arm Cortex R5F Subsystem (WKUP_R5FSS)

This section contains the integration details for the WKUP_R5FSS module on this device. For Further information, see the Arm Cortex R5F Subsystem (WKUP_R5FSS) section of the Processors and Accelerators chapter

4.2.4.1 WKUP_R5FSS Unsupported Features

The following features are not supported on this family of devices:

- CPU1 is not supported. This family of devices only supports a single core R5F implementaion

4.2.4.2 WKUP_R5FSS Integration

Table 4-38. WKUP_R5FSS Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_R5FSS0			✓
WKUP_R5FSS0_CORE0			✓
WKUP_R5FSS0_COMMON0			✓

Table 4-39. Integration Attributes for WKUP_R5FSS

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_R5FSS0_CORE0	PSC0	GP_Core_CTL	LPSC_main_dm	1	OFF	YES	LPSC_main_alwayson

Table 4-40. Clock Integration for WKUP_R5FSS

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_R5FSS0_CORE0	CLK	MAIN_PLL15_HSDIV2_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL[0:0]=0	None
WKUP_R5FSS0_CORE0	CLK	MCU_PLL0_HSDIV0_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL[0:0]=1	None
WKUP_R5FSS0_CORE0	ICLK	MAIN_PLL15_HSDIV2_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL[0:0]=0	interface clock
WKUP_R5FSS0_CORE0	ICLK	MCU_PLL0_HSDIV0_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL[0:0]=1	interface clock

Table 4-41. Reset Integration for WKUP_R5FSS

Module Instance	Source	Description
WKUP_R5FSS0_CORE0	PSC0	WKUP_R5FSS0_CORE0 reset

Table 4-42. Hardware Requests for WKUP_R5FSS

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_cti_0	WKUP_R5FSS0_CORE0_intr_175	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_ecc_corrected_level_0	ESM0_esm_lvl_event_30	ESM0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_ecc_uncorrected_level_0	ESM0_esm_lvl_event_91	ESM0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_exp_intr_0	ESM0_esm_lvl_event_124	ESM0	WKUP_R5FSS0_CORE0 interrupt request	level

Table 4-42. Hardware Requests for WKUP_R5FSS (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_exp_intr_0	WKUP_R5FSS0_CORE0_intr_4	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_pmu_0	WKUP_R5FSS0_CORE0_intr_58	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_valfiq_0	WKUP_R5FSS0_CORE0_intr_59	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_valirq_0	WKUP_R5FSS0_CORE0_intr_60	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_commrx_level_0_0	WKUP_R5FSS0_CORE0_intr_5	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_COMMON0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_commtx_level_0_0	WKUP_R5FSS0_CORE0_intr_6	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_COMMON0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_ecc_de_to_esm_0_0	ESM0_esm_lvl_event_40	ESM0	WKUP_R5FSS0_COMMON0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_ecc_se_to_esm_0_0	ESM0_esm_lvl_event_42	ESM0	WKUP_R5FSS0_COMMON0 interrupt request	level

4.3 Interprocessor Communication

4.3.1 Mailbox

This section contains the integration details for the Mailbox module on this device. For further information, see the *Mailbox* section of the I*nterprocessor Communication* chapter.

4.3.1.1 Mailbox Unsupported Features

The following features are not supported on this family of devices:

- 'User' protection of mailbox in hardware. If required, must be implemented by software.

4.3.1.2 mailbox Integration

Table 4-43. MAILBOX Module Allocations

Instance	MAIN	MCU	WKUP
MAILBOX0	✓		

4.3.1.3 MAILBOX_MAILBOX_CLUSTER_0 Integration

Table 4-44. MAILBOX_MAILBOX_CLUSTER_0 Module Allocations

Instance	MAIN	MCU	WKUP
MAILBOX0_MAILBOX_CLUSTER_0	✓		

Table 4-45. Integration Attributes for MAILBOX_MAILBOX_CLUSTER_0

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MAILBOX0_MAILBOX_CLUSTER_0	PSC0	GP_Core_CTL	LPSC_SMS_common	27	ON	YES	LPSC_main_alwayson

Table 4-46. Clock Integration for MAILBOX_MAILBOX_CLUSTER_0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MAILBOX0_MAILBOX_CLUSTER_0	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2		None

Table 4-47. Reset Integration for MAILBOX_MAILBOX_CLUSTER_0

Module Instance	Source	Description
MAILBOX0_MAILBOX_CLUSTER_0	PSC0	MAILBOX0_MAILBOX_CLUSTER_0 reset

Table 4-48. Hardware Requests for MAILBOX_MAILBOX_CLUSTER_0

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster0_pend_0	GICSS0_spi_108	GICSS0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster0_pend_0	C7X256V0_CLEC_gic_spi_76	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster0_pend_1	C7X256V0_CLEC_soc_events_in_0	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster0_pend_2	MCU_R5FSS0_CORE0_cpu0_intr_240	MCU_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster0_pend_3	WKUP_R5FSS0_CORE0_intr_240	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level

Table 4-48. Hardware Requests for MAILBOX_MAILBOX_CLUSTER_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster1_pend_0	GICSS0_spi_109	GICSS0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster1_pend_0	C7X256V0_CLEC_gic_spi_77	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster1_pend_1	C7X256V0_CLEC_soc_events_in_1	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster1_pend_2	MCU_R5FSS0_CORE0_cpu0_intr_241	MCU_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster1_pend_3	WKUP_R5FSS0_CORE0_intr_241	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster2_pend_0	GICSS0_spi_140	GICSS0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster2_pend_0	C7X256V0_CLEC_gic_spi_108	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster2_pend_1	C7X256V0_CLEC_soc_events_in_2	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster2_pend_2	MCU_R5FSS0_CORE0_cpu0_intr_242	MCU_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster2_pend_3	WKUP_R5FSS0_CORE0_intr_242	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster3_pend_0	GICSS0_spi_141	GICSS0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster3_pend_0	C7X256V0_CLEC_gic_spi_109	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster3_pend_1	C7X256V0_CLEC_soc_events_in_3	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster3_pend_2	MCU_R5FSS0_CORE0_cpu0_intr_243	MCU_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster3_pend_3	WKUP_R5FSS0_CORE0_intr_243	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level

4.3.1.4 MAILBOX_MAILBOX_CLUSTER_1 Integration

Table 4-49. MAILBOX_MAILBOX_CLUSTER_1 Module Allocations

Instance	MAIN	MCU	WKUP
MAILBOX0_MAILBOX_CLUSTER_1	✓		

4.3.1.5 MAILBOX_MAILBOX_CLUSTER_2 Integration

Table 4-50. MAILBOX_MAILBOX_CLUSTER_2 Module Allocations

Instance	MAIN	MCU	WKUP
MAILBOX0_MAILBOX_CLUSTER_2	✓		

4.3.1.6 MAILBOX_MAILBOX_CLUSTER_3 Integration

Table 4-51. MAILBOX_MAILBOX_CLUSTER_3 Module Allocations

Instance	MAIN	MCU	WKUP
MAILBOX0_MAILBOX_CLUSTER_3	✓		

4.3.2 Spinlock

This section contains the integration details for the Spinlock module on this device. For further information, see the *Spinlock* section of the *Interprocessor Communication* chapter.

4.3.2.1 SPINLOCK Unsupported Features

The following features are not supported on this family of devices:

- ARM architectural Spinlock instructions (LDREX,STREX)
- Any use model other than binary mutex (for example, counting semaphore, lockless programming): Spinlock MMR is a single binary 0,1 implemented by a state machine.
- 64-bit accesses: Spinlock MMRs are aligned on 32-bit boundaries meaning a 64-bit access affects the state of 2 Spinlocks.

4.3.2.2 SPINLOCK Integration

Table 4-52. SPINLOCK Module Allocations

Instance	MAIN	MCU	WKUP
SPINLOCK0	✓		

Table 4-53. Integration Attributes for SPINLOCK

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
SPINLOCK0	PSC0	GP_Core_CTL	LPSC_SMS_common	27	ON	YES	LPSC_main_alwayson

Table 4-54. Clock Integration for SPINLOCK

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
SPINLOCK0	FICLK	MAIN_PLL15_HSDIV0_CLKOUT/2		functional and interface clock

Table 4-55. Reset Integration for SPINLOCK

Module Instance	Source	Description
SPINLOCK0	PSC0	SPINLOCK0 reset

4.4 Device Configuration

4.4.1 Control Module (CTRL_MMR)

This section contains the integration details for the CTRL_MMR module on this device. For further information, see the *Memory Mapped Control Register Modules (CTRL_MMR)* section of the *Device Configuration* chapter.

4.4.1.1 MAIN_CTRL_MMR Integration

Table 4-56. MAIN_CTRL_MMR Module Allocations

Instance	MAIN	MCU	WKUP
CTRL_MMR0	✓		

Table 4-57. Clock Integration for MAIN_CTRL_MMR

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
CTRL_MMR0	VBUSP_CLK	MAIN_SYSCLK0/4		None

Table 4-58. Hardware Requests for MAIN_CTRL_MMR

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CTRL_MMR0	CTRL_MMR0_IPC_SET0_ipc_set_ipcfg_0	C7X256V0_CLEC_soc_events_in_5	C7X256V0_CLEC	CTRL_MMR0 interrupt request	level
CTRL_MMR0	CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_39	MCU_R5FSS0_CORE0	CTRL_MMR0 interrupt request	level
CTRL_MMR0	CTRL_MMR0_access_err_0	GICSS0_spi_129	GICSS0	CTRL_MMR0 interrupt request	level
CTRL_MMR0	CTRL_MMR0_access_err_0	WKUP_R5FSS0_CORE0_intr_128	WKUP_R5FSS0_CORE0	CTRL_MMR0 interrupt request	level
CTRL_MMR0	CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_128	MCU_R5FSS0_CORE0	CTRL_MMR0 interrupt request	level
CTRL_MMR0	CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_97	C7X256V0_CLEC	CTRL_MMR0 interrupt request	level

4.4.1.2 MCU_CTRL_MMR Integration

Table 4-59. MCU_CTRL_MMR Module Allocations

Instance	MAIN	MCU	WKUP
MCU_CTRL_MMR0		✓	

Table 4-60. Clock Integration for MCU_CTRL_MMR

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_CTRL_MMR0	VBUSP_CLK	MCU_SYSCLK0/4		None

Table 4-61. Hardware Requests for MCU_CTRL_MMR

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_CTRL_MMR0	MCU_CTRL_MMR0_IPC_SET0_ipc_set_ipcfg_0	WKUP_R5FSS0_CORE0_intr_0	WKUP_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
MCU_CTRL_MMR0	MCU_CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_39	MCU_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
MCU_CTRL_MMR0	MCU_CTRL_MMR0_access_err_0	GICSS0_spi_129	GICSS0	MCU_CTRL_MMR0 interrupt request	level
MCU_CTRL_MMR0	MCU_CTRL_MMR0_access_err_0	WKUP_R5FSS0_CORE0_intr_128	WKUP_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level

Table 4-61. Hardware Requests for MCU_CTRL_MMR (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_CTRL_MMR0	MCU_CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_128	MCU_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
MCU_CTRL_MMR0	MCU_CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_97	C7X256V0_CLEC	MCU_CTRL_MMR0 interrupt request	level

4.4.1.3 WKUP_CTRL_MMR Integration

Table 4-62. WKUP_CTRL_MMR Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_CTRL_MMR0			✓

Table 4-63. Clock Integration for WKUP_CTRL_MMR

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_CTRL_MMR0	VBUSP_CLK	DM_CLK/4		None

Table 4-64. Hardware Requests for WKUP_CTRL_MMR

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_39	MCU_R5FSS0_CORE0	WKUP_CTRL_MMR0 interrupt request	level
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	GICSS0_spi_129	GICSS0	WKUP_CTRL_MMR0 interrupt request	level
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	WKUP_R5FSS0_CORE0_intr_128	WKUP_R5FSS0_CORE0	WKUP_CTRL_MMR0 interrupt request	level
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	MCU_R5FSS0_CORE0_cpu0_intr_128	MCU_R5FSS0_CORE0	WKUP_CTRL_MMR0 interrupt request	level
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_97	C7X256V0_CLEC	WKUP_CTRL_MMR0 interrupt request	level

4.4.2 Voltage and Thermal Manager (VTM)

This section contains the integration details for the VTM module on this device. For further information, see the *Voltage and Thermal Manager (VTM)* in *Power* section of the *Device Configuration* chapter.

4.4.2.1 VTM Integration

Table 4-65. VTM Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_VTM0			✓

Table 4-66. Integration Attributes for VTM

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_VTM0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-67. Clock Integration for VTM

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_VTM0	FIX_REF2_CLK	CLK_12M_RC		reference clock
WKUP_VTM0	FIX_REF_CLK	CLK_12M_RC		reference clock
WKUP_VTM0	FIX_REF_CLK	HFOSC0 (INSTANCE)		reference clock

Table 4-67. Clock Integration for VTM (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_VTM0	ICLK	DM_CLK/4		interface clock

Table 4-68. Reset Integration for VTM

Module Instance	Source	Description
WKUP_VTM0	PSC0	WKUP_VTM0 reset

Table 4-69. Hardware Requests for VTM

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_VTM0	WKUP_VTM0_corr_level_0	ESM0_esm_lvl_event_139	ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_corr_level_0	WKUP_ESM0_esm_lvl_event_11	WKUP_ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	ESM0_esm_lvl_event_137	ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	WKUP_ESM0_esm_lvl_event_8	WKUP_ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	GICSS0_spi_183	GICSS0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	WKUP_R5FSS0_CORE0_intr_183	WKUP_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_183	MCU_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th1_intr_0	C7X256V0_CLEC_gic_spi_151	C7X256V0_CLEC	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	ESM0_esm_lvl_event_138	ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	WKUP_ESM0_esm_lvl_event_10	WKUP_ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	GICSS0_spi_184	GICSS0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	WKUP_R5FSS0_CORE0_intr_184	WKUP_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_184	MCU_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_gt_th2_intr_0	C7X256V0_CLEC_gic_spi_152	C7X256V0_CLEC	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	ESM0_esm_lvl_event_136	ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	WKUP_ESM0_esm_lvl_event_9	WKUP_ESM0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	GICSS0_spi_185	GICSS0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	WKUP_R5FSS0_CORE0_intr_185	WKUP_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_185	MCU_R5FSS0_CORE0	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_therm_lvl_lt_th0_intr_0	C7X256V0_CLEC_gic_spi_153	C7X256V0_CLEC	WKUP_VTM0 interrupt request	level
WKUP_VTM0	WKUP_VTM0_uncorr_level_0	ESM0_esm_lvl_event_140	ESM0	WKUP_VTM0 interrupt request	level

Table 4-69. Hardware Requests for VTM (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_VTM0	WKUP_VTM0_uncorr_level_0	WKUP_ESM0_esm_lvl_event_12	WKUP_ESM0	WKUP_VTM0 interrupt request	level

4.4.2.2 Voltage and Thermal Manager Locations

There are 3 Voltage and Thermal Monitors located on AM62D.

- Temp Sensor 0: C7x
- Temp Sensor 1: A53
- Temp Sensor 2: DDR

4.4.3 Power Glitch Detect (PGD)

This section contains the integration details for the PGD module on this device. For further information, see the Power Glitch Detect (PGD) section of the Device Configuration chapter.

4.4.3.1 Resets, Interrupts, and Clocks

Table 4-70. PGD Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies

Table 4-71. PGD Resets

Module Instance	Source	Description

Table 4-72. PGD Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
PGD0	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_thresh_hi_flag_ipcfg_0	ESM0_esm_lvl_event_IN_101	ESM0	PGD0 Threshold High flag level Interrupt	level
PGD0	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_thresh_low_flag_ipcfg_0	ESM0_esm_lvl_event_IN_102	ESM0	PGD0 Threshold Low flag level Interrupt	level

Table 4-73. PGD Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description

4.5 Interrupts

4.5.1 Generic Interrupt Controller Subsystem (GICSS)

This section contains the integration details for the GICSS modules on this device. For Further information, see the *Generic Interrupt Controller (GICSS)* section of the *Interrupts* chapter.

4.5.1.1 gicss Integration

Table 4-74. GICSS Module Allocations

Instance	MAIN	MCU	WKUP
GICSS0	✓		

Table 4-75. Integration Attributes for gicss

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
GICSS0	PSC0	GP_Core_CTL	LPSC_GIC	36	ON	YES	LPSC_main_IP

Table 4-76. Clock Integration for gicss

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
GICSS0	FICLK	MAIN_SYSCLK0/2		functional and interface clock

Table 4-77. Reset Integration for gicss

Module Instance	Source	Description
GICSS0	PSC0	GICSS0 reset

Table 4-78. Hardware Requests for gicss

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GICSS0	GICSS0_axim_err_0	ESM0_esm_pls_event0_198	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_axim_err_0	ESM0_esm_pls_event1_198	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_axim_err_0	ESM0_esm_pls_event2_198	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_ecc_aggr_corr_level_0	ESM0_esm_lvl_event_12	ESM0	GICSS0 interrupt request	level
GICSS0	GICSS0_ecc_aggr_uncorr_level_0	ESM0_esm_lvl_event_75	ESM0	GICSS0 interrupt request	level
GICSS0	GICSS0_ecc_fatal_0	ESM0_esm_pls_event0_199	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_ecc_fatal_0	ESM0_esm_pls_event1_199	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_ecc_fatal_0	ESM0_esm_pls_event2_199	ESM0	GICSS0 interrupt request	pulse
GICSS0	GICSS0_gic_pwr0_wake_request_0	WKUP_R5FSS0_CORE0_intr_154	WKUP_R5FSS0_CORE0	GICSS0 interrupt request	level
GICSS0	GICSS0_gic_pwr0_wake_request_1	WKUP_R5FSS0_CORE0_intr_155	WKUP_R5FSS0_CORE0	GICSS0 interrupt request	level
GICSS0	GICSS0_gic_pwr0_wake_request_2	WKUP_R5FSS0_CORE0_intr_156	WKUP_R5FSS0_CORE0	GICSS0 interrupt request	level
GICSS0	GICSS0_gic_pwr0_wake_request_3	WKUP_R5FSS0_CORE0_intr_157	WKUP_R5FSS0_CORE0	GICSS0 interrupt request	level

4.5.2 GPIOMUX_INTROUTER

This section contains the integration details for the GPIOMUX_INTROUTER modules on this device. For Further information, see the GPIOMUX_INTROUTER section of the Interrupts chapter

4.5.2.1 main_gpiomux_introuter Integration

Table 4-79. MAIN_GPIOMUX_INTROUTER Module Allocations

Instance	MAIN	MCU	WKUP
MAIN_GPIOMUX_INTROUTER0	✓		

Table 4-80. Integration Attributes for main_gpiomux_introuter

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MAIN_GPIOMUX_INTROUTER0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-81. Clock Integration for main_gpiomux_introuter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MAIN_GPIOMUX_INTROUTER0	INTR_CLK	MAIN_SYSCLK0/4		None

Table 4-82. Reset Integration for main_gpiomux_introuter

Module Instance	Source	Description
MAIN_GPIOMUX_INTROUTER0	PSC0	MAIN_GPIOMUX_INTROUTER0 reset

Table 4-83. Hardware Requests for main_gpiomux_introuter

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_0	GICSS0_spi_32	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_0	WKUP_R5FSS0_CORE0_intr_32	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_0	C7X256V0_CLEC_gic_spi_0	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_1	GICSS0_spi_33	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_1	WKUP_R5FSS0_CORE0_intr_33	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_1	C7X256V0_CLEC_gic_spi_1	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_2	GICSS0_spi_34	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_2	WKUP_R5FSS0_CORE0_intr_34	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_2	C7X256V0_CLEC_gic_spi_2	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_3	GICSS0_spi_35	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_3	WKUP_R5FSS0_CORE0_intr_35	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_3	C7X256V0_CLEC_gic_spi_3	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_4	GICSS0_spi_36	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse

Table 4-83. Hardware Requests for main_gpiomux_introuter (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_4	WKUP_R5FSS0_CORE0_intr_36	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_4	C7X256V0_CLEC_gic_spi_4	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_5	GICSS0_spi_37	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_5	WKUP_R5FSS0_CORE0_intr_37	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_5	C7X256V0_CLEC_gic_spi_5	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_6	GICSS0_spi_38	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_6	WKUP_R5FSS0_CORE0_intr_38	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_6	C7X256V0_CLEC_gic_spi_6	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_7	GICSS0_spi_39	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_7	WKUP_R5FSS0_CORE0_intr_39	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_7	C7X256V0_CLEC_gic_spi_7	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_8	GICSS0_spi_40	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_8	WKUP_R5FSS0_CORE0_intr_40	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_8	C7X256V0_CLEC_gic_spi_8	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_9	GICSS0_spi_41	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_9	WKUP_R5FSS0_CORE0_intr_41	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_9	C7X256V0_CLEC_gic_spi_9	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_10	GICSS0_spi_42	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_10	WKUP_R5FSS0_CORE0_intr_42	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_10	C7X256V0_CLEC_gic_spi_10	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_11	GICSS0_spi_43	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_11	WKUP_R5FSS0_CORE0_intr_43	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_11	C7X256V0_CLEC_gic_spi_11	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_12	GICSS0_spi_44	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_12	WKUP_R5FSS0_CORE0_intr_44	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_12	C7X256V0_CLEC_gic_spi_12	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse

Table 4-83. Hardware Requests for main_gpiomux_introuter (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_13	GICSS0_spi_45	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_13	WKUP_R5FSS0_CORE0_intr_45	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_13	C7X256V0_CLEC_gic_spi_13	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_14	GICSS0_spi_46	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_14	WKUP_R5FSS0_CORE0_intr_46	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_14	C7X256V0_CLEC_gic_spi_14	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_15	GICSS0_spi_47	GICSS0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_15	WKUP_R5FSS0_CORE0_intr_47	WKUP_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_15	C7X256V0_CLEC_gic_spi_15	C7X256V0_CLEC	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_22	DMASS0_INTAGGR_0_intaggr_levi_pend_24	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_23	DMASS0_INTAGGR_0_intaggr_levi_pend_25	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_24	DMASS0_INTAGGR_0_intaggr_levi_pend_16	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_25	DMASS0_INTAGGR_0_intaggr_levi_pend_17	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_26	DMASS0_INTAGGR_0_intaggr_levi_pend_18	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_27	DMASS0_INTAGGR_0_intaggr_levi_pend_19	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_28	DMASS0_INTAGGR_0_intaggr_levi_pend_20	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_29	DMASS0_INTAGGR_0_intaggr_levi_pend_21	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_30	DMASS0_INTAGGR_0_intaggr_levi_pend_22	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_31	DMASS0_INTAGGR_0_intaggr_levi_pend_23	DMASS0_INTAGGR_0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_34	MCU_R5FSS0_CORE0_cpu0_intr_32	MCU_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_outp_35	MCU_R5FSS0_CORE0_cpu0_intr_33	MCU_R5FSS0_CORE0	MAIN_GPIOMUX_INTROUTER0 interrupt request	pulse

4.5.2.2 mcu_gpiomux_introuter Integration

Table 4-84. MCU_GPIOMUX_INTROUTER Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_MCU_GPIOMUX_INTROUTER0		✓	

Table 4-85. Integration Attributes for mcu_gpiomux_introuter

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_PSC0	GP_core_CTL_MCU	LPSC_mcu_alwayson	0	ON	NO	

Table 4-86. Clock Integration for mcu_gpiomux_introuter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_MCU_GPIOMUX_INTROUTER0	INTR_CLK	MCU_SYSCLK0/4		None

Table 4-87. Reset Integration for mcu_gpiomux_introuter

Module Instance	Source	Description
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_PSC0	WKUP_MCU_GPIOMUX_INTROUTER0 reset

Table 4-88. Hardware Requests for mcu_gpiomux_introuter

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_0	GICSS0_spi_104	GICSS0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_0	WKUP_R5FSS0_CORE0_intr_104	WKUP_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_0	C7X256V0_CLEC_gic_spi_72	C7X256V0_CLEC	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_1	GICSS0_spi_105	GICSS0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_1	WKUP_R5FSS0_CORE0_intr_105	WKUP_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_1	C7X256V0_CLEC_gic_spi_73	C7X256V0_CLEC	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_2	GICSS0_spi_106	GICSS0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_2	WKUP_R5FSS0_CORE0_intr_106	WKUP_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_2	C7X256V0_CLEC_gic_spi_74	C7X256V0_CLEC	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_3	GICSS0_spi_107	GICSS0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse

Table 4-88. Hardware Requests for mcu_gpiomux_introuter (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_3	WKUP_R5FSS0_CORE0_intr_107	WKUP_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_3	C7X256V0_CLEC_gic_spi_75	C7X256V0_CLEC	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_4	MCU_R5FSS0_CORE0_cpu0_intr_104	MCU_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_5	MCU_R5FSS0_CORE0_cpu0_intr_105	MCU_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_6	MCU_R5FSS0_CORE0_cpu0_intr_106	MCU_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_7	MCU_R5FSS0_CORE0_cpu0_intr_107	MCU_R5FSS0_CORE0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_8	WKUP_ESM0_esm_pls_event0_88	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_8	WKUP_ESM0_esm_pls_event1_88	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_8	WKUP_ESM0_esm_pls_event2_88	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_9	WKUP_ESM0_esm_pls_event0_89	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_9	WKUP_ESM0_esm_pls_event1_89	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_9	WKUP_ESM0_esm_pls_event2_89	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_10	WKUP_ESM0_esm_pls_event0_90	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_10	WKUP_ESM0_esm_pls_event1_90	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_10	WKUP_ESM0_esm_pls_event2_90	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_11	WKUP_ESM0_esm_pls_event0_91	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_11	WKUP_ESM0_esm_pls_event1_91	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_outp_11	WKUP_ESM0_esm_pls_event2_91	WKUP_ESM0	WKUP_MCU_GPIOMUX_INTROUTER0 interrupt request	pulse

4.5.3 CMP_EVENT_INTROUTER

This section contains the integration details for the CMP_EVENT_INTROUTER modules on this device. For Further information, see the CMP_EVENT_INTROUTER section of the Interrupts chapter

4.5.3.1 cmp_event_introuter Integration

Table 4-89. CMP_EVENT_INTROUTER Module Allocations

Instance	MAIN	MCU	WKUP
CMP_EVENT_INTROUTER0	✓		

Table 4-90. Integration Attributes for cmp_event_introuter

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
CMP_EVENT_INTROUTER0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-91. Clock Integration for cmp_event_introuter

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
CMP_EVENT_INTROUTER0	INTR_CLK	MAIN_SYSCLK0/4		None

Table 4-92. Reset Integration for cmp_event_introuter

Module Instance	Source	Description
CMP_EVENT_INTROUTER0	PSC0	CMP_EVENT_INTROUTER0 reset

Table 4-93. Hardware Requests for cmp_event_introuter

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_0	GICSS0_spi_48	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_0	C7X256V0_CLEC_gic_spi_16	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_1	GICSS0_spi_49	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_1	C7X256V0_CLEC_gic_spi_17	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_2	GICSS0_spi_50	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_2	C7X256V0_CLEC_gic_spi_18	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_3	GICSS0_spi_51	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_3	C7X256V0_CLEC_gic_spi_19	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_4	GICSS0_spi_52	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_4	C7X256V0_CLEC_gic_spi_20	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_5	GICSS0_spi_53	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_5	C7X256V0_CLEC_gic_spi_21	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_6	GICSS0_spi_54	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse

Table 4-93. Hardware Requests for cmp_event_introuter (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_6	C7X256V0_CLEC_gic_spi_22	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_7	GICSS0_spi_55	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_7	C7X256V0_CLEC_gic_spi_23	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_8	GICSS0_spi_56	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_8	C7X256V0_CLEC_gic_spi_24	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_9	GICSS0_spi_57	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_9	C7X256V0_CLEC_gic_spi_25	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_10	GICSS0_spi_58	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_10	C7X256V0_CLEC_gic_spi_26	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_11	GICSS0_spi_59	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_11	C7X256V0_CLEC_gic_spi_27	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_12	GICSS0_spi_60	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_12	C7X256V0_CLEC_gic_spi_28	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_13	GICSS0_spi_61	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_13	C7X256V0_CLEC_gic_spi_29	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_14	GICSS0_spi_62	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_14	C7X256V0_CLEC_gic_spi_30	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_15	GICSS0_spi_63	GICSS0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_15	C7X256V0_CLEC_gic_spi_31	C7X256V0_CLEC	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_16	WKUP_R5FSS0_CORE0_intr_48	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_17	WKUP_R5FSS0_CORE0_intr_49	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_18	WKUP_R5FSS0_CORE0_intr_50	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_19	WKUP_R5FSS0_CORE0_intr_51	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_20	WKUP_R5FSS0_CORE0_intr_52	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_21	WKUP_R5FSS0_CORE0_intr_53	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_22	WKUP_R5FSS0_CORE0_intr_54	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse

Table 4-93. Hardware Requests for cmp_event_introuter (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_23	WKUP_R5FSS0_CORE0_intr_55	WKUP_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_24	DMASS0_INTAGGR_0_intaggr_levi_pend_0	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_25	DMASS0_INTAGGR_0_intaggr_levi_pend_1	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_26	DMASS0_INTAGGR_0_intaggr_levi_pend_2	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_27	DMASS0_INTAGGR_0_intaggr_levi_pend_3	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_28	DMASS0_INTAGGR_0_intaggr_levi_pend_4	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_29	DMASS0_INTAGGR_0_intaggr_levi_pend_5	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_30	DMASS0_INTAGGR_0_intaggr_levi_pend_6	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_31	DMASS0_INTAGGR_0_intaggr_levi_pend_7	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_32	EPWM0_epwm_syncin_0	EPWM0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_34	MCU_R5FSS0_CORE0_cpu0_intr_58	MCU_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_35	MCU_R5FSS0_CORE0_cpu0_intr_59	MCU_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_36	MCU_R5FSS0_CORE0_cpu0_intr_60	MCU_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_37	MCU_R5FSS0_CORE0_cpu0_intr_61	MCU_R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse

4.6 Data Movement Architecture

4.6.1 Data Movement Subsystem (DMSS)

This section contains the integration details for the DMSS module on this device. For Further information, see the Data Movement Subsystem (DMSS) section of the Data Movement Architecture chapter

4.6.1.1 DMSS Unsupported Features

The following features are not supported on this family of devices:

- Ring Accelerator QM and CREDENTIAL Modes

4.6.1.2 DMASS Integration

Table 4-94. DMASS Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0	✓		

4.6.1.3 DMASS_CBASS_0 Integration

Table 4-95. DMASS_CBASS_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_CBASS_0	✓		

4.6.1.4 DMASS_COMMON_0 Integration

Table 4-96. DMASS_COMMON_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_COMMON_0	✓		

4.6.1.5 DMASS_ECC_AGGR_0 Integration

Table 4-97. DMASS_ECC_AGGR_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_ECC_AGGR_0	✓		

Table 4-98. Clock Integration for DMASS_ECC_AGGR_0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DMASS0_ECC_AGGR_0	FICLK	MAIN_SYSCLK0/4		None

Table 4-99. Hardware Requests for DMASS_ECC_AGGR_0

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ecc_corrected_err_level_0	ESM0_esm_lvl_event_9	ESM0	DMASS0_ECC_AGGR_0 interrupt request	level
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ecc_uncorrected_err_level_0	ESM0_esm_lvl_event_10	ESM0	DMASS0_ECC_AGGR_0 interrupt request	level

4.6.1.6 DMASS_IPCSS_0 Integration

Table 4-100. DMASS_IPCSS_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_IPCSS_0	✓		

4.6.1.7 DMASS_PSILCFG_0 Integration

Table 4-101. DMASS_PSILCFG_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_PSILCFG_0	✓		

4.6.1.8 DMASS_PSILSS_0 Integration

Table 4-102. DMASS_PSILSS_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_PSILSS_0	✓		

4.6.1.9 DMASS_RINGACC_0 Integration

Table 4-103. DMASS_RINGACC_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_RINGACC_0	✓		

4.6.1.10 DMASS_SEC_PROXY_0 Integration

Table 4-104. DMASS_SEC_PROXY_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_SEC_PROXY_0	✓		

4.6.1.11 Global Event Map

The global event map for all DMSS events is shown in Table 4-105.

Table 4-105. Global Event Map

Destination		Offset	PSIL Routed Slots	Actual Slots
DMSS Instance or External	Port			
DMSS	DMSS INTAGGR SEVI	0 (0k)	8192 (8k)	1536
DMSS	DMSS INTAGGR MEVI	8192 (8k)	2048 (2k)	128
DMSS	DMSS INTAGGR GEVI	10240 (10k)	2048 (2k)	256
External	DMSC IA SEVI	18432 (18k)	2048 (2k)	-
DMSS	DMSS INTAGGR LEVI	32768 (32k)	32 (0.03k)	32
External	PDMA_MAIN0 LEVI	41984 (41.000k)	128	-
External	PDMA_MAIN1 LEVI	42112 (41.125k)	128	-
DMSS	DMSS BCDMA Triggers	50176 (49k)	1024 (1k)	164
External	UTC	62464 (61k)	128	-
External	DRU	62976 (61.5k)	64	-

4.6.1.12 PSI-L System Thread Map

Table 4-106. DMSS PSILSS Thread Map

Thread Number	NAV Instance	Endpoint
0x0000	DMSS	PSILCFG CFGSTRM
0x0020	DMSS	PKTDMA CFGSTRM
0x0021	DMSS	BCDMA CFGSTRM
0x1000-0x1fff	DMSS	PKTDMA Threads
0x2000-0x2fff	DMSS	BCDMA Threads
0x3000-0x42ff	DMSS	Reserved

Table 4-106. DMSS PSILSS Thread Map (continued)

Thread Number	NAV Instance	Endpoint
0x4300-0x43ff	DMSS	PDMA_MAIN0
0x4400-0x44ff	DMSS	PDMA_MAIN1
0x4500-0x45ff	DMSS	PDMA_MCASP
0x4600-0x46ff	DMSS	CPSW2
0x4700-0x74ff	DMSS	Reserved
0x7500-0x7506	DMSS	SAUL0

4.6.2 Block Copy DMA (BCDMA)

4.6.2.1 DMASS_BCDMA_0 Integration

Table 4-107. DMASS_BCDMA_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_BCDMA_0	✓		

4.6.3 Peripheral DMA (PDMA)

This section contains the integration details for the PDMA module on this device. For further information, see the *Peripheral DMA (PDMA)* section of the *Data Movement Architecture* chapter.

4.6.3.1 PDMA Unsupported Features

The following features are not supported on this family of devices:

- Dynamic transfer requests
- Cross-channel triggering

4.6.3.2 PDMA Integration

Table 4-108. PDMA Module Allocations

Instance	MAIN	MCU	WKUP
PDMA2	✓		
PDMA0	✓		
PDMA1	✓		

Table 4-109. Integration Attributes for PDMA

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
PDMA2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
PDMA0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
PDMA1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO

Table 4-110. Clock Integration for PDMA

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
PDMA2	FICLK	MAIN_SYSCLK0/2		None
PDMA0	VCLK	MAIN_SYSCLK0/4		None
PDMA1	VCLK	MAIN_SYSCLK0/4		None

Table 4-111. Reset Integration for PDMA

Module Instance	Source	Description
PDMA2	PSC0	PDMA2 reset
PDMA0	PSC0	PDMA0 reset
PDMA1	PSC0	PDMA1 reset

Table 4-112. Hardware Requests for PDMA

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
PDMA0	PDMA0_ecc_ded_pend_0	ESM0_esm_lvl_event_88	ESM0	PDMA0 interrupt request	level
PDMA0	PDMA0_ecc_sec_pend_0	ESM0_esm_lvl_event_15	ESM0	PDMA0 interrupt request	level
PDMA1	PDMA1_ecc_ded_pend_0	ESM0_esm_lvl_event_89	ESM0	PDMA1 interrupt request	level
PDMA1	PDMA1_ecc_sec_pend_0	ESM0_esm_lvl_event_28	ESM0	PDMA1 interrupt request	level

4.6.4 Packet DMA (PKTDMA)

4.6.4.1 Packet DMA (PKTDMA)

Table 4-113. PKTDMA Allocation Within Device Domains

Module Instance	Domain		
	WKUP	MCU	MAIN
DMSS_PKTDMA	-	-	✓ (DMSS)

Table 4-114. PKTDMA Parameters

Module Instance	Parameters	
	tchan_cnt	rchan_cnt
DMSS_PKTDMA	29	24

Table 4-115. PKTDMA TX Channel Configuration

Channel	Description	Flow Start	Flow Count
0	Periph Tx Ch 0	0	1
1	Periph Tx Ch 1	1	1
2	Periph Tx Ch 2	2	1
3	Periph Tx Ch 3	3	1
4	Periph Tx Ch 4	4	1
5	Periph Tx Ch 5	5	1
6	Periph Tx Ch 6	6	1
7	Periph Tx Ch 7	7	1
8	Periph Tx Ch 8	8	1
9	Periph Tx Ch 9	9	1
10	Periph Tx Ch 10	10	1
11	Periph Tx Ch 11	11	1
12	Periph Tx Ch 12	12	1
13	Periph Tx Ch 13	13	1
14	Periph Tx Ch 14	14	1
15	Periph Tx Ch 15	15	1
16	Periph Tx Ch 16	16	1
17	Periph Tx Ch 17	17	1
18	Periph Tx Ch 18	18	1
19	CPSW Tx Ch 0	19	8
20	CPSW Tx Ch 1	27	8
21	CPSW Tx Ch 2	35	8
22	CPSW Tx Ch 3	43	8
23	CPSW Tx Ch 4	51	8
24	CPSW Tx Ch 5	59	8
25	CPSW Tx Ch 6	67	8
26	CPSW Tx Ch 7	75	8
27	SAUL Tx Ch 0	83	8
28	SAUL Tx Ch 1	91	8

Table 4-116. PKTDMA RX Channel Configuration

Channel	Description	Flow Start	Flow Count
0	Periph Rx Ch 0	0	1
1	Periph Rx Ch 1	1	1
2	Periph Rx Ch 2	2	1

Table 4-116. PKTDMA RX Channel Configuration (continued)

Channel	Description	Flow Start	Flow Count
3	Periph Rx Ch 3	3	1
4	Periph Rx Ch 4	4	1
5	Periph Rx Ch 5	5	1
6	Periph Rx Ch 6	6	1
7	Periph Rx Ch 7	7	1
8	Periph Rx Ch 8	8	1
9	Periph Rx Ch 9	9	1
10	Periph Rx Ch 10	10	1
11	Periph Rx Ch 11	11	1
12	Periph Rx Ch 12	12	1
13	Periph Rx Ch 13	13	1
14	Periph Rx Ch 14	14	1
15	Periph Rx Ch 15	15	1
16	Periph Rx Ch 16	16	1
17	Periph Rx Ch 17	17	1
18	Periph Rx Ch 18	18	1
19	CPSW Rx Ch 0	19	16
20	SAUL Rx Ch 0	35	8
21	SAUL Rx Ch 1	35	8
22	SAUL Rx Ch 2	43	8
23	SAUL Rx Ch 3	43	8

4.6.4.2 DMASS_PKTDMA_0 Integration

Table 4-117. DMASS_PKTDMA_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_PKTDMA_0	✓		

4.6.5 Interrupt Aggregator (INTR_AGGR)

4.6.5.1 DMASS_INTAGGR_0 Integration

Table 4-118. DMASS_INTAGGR_0 Module Allocations

Instance	MAIN	MCU	WKUP
DMASS0_INTAGGR_0	✓		

Table 4-119. Hardware Requests for DMASS_INTAGGR_0

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_0	GICSS0_spi_64	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_0	C7X256V0_CLEC_gic_spi_32	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_1	GICSS0_spi_65	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_1	C7X256V0_CLEC_gic_spi_33	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_2	GICSS0_spi_66	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_2	C7X256V0_CLEC_gic_spi_34	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_3	GICSS0_spi_67	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_3	C7X256V0_CLEC_gic_spi_35	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_4	GICSS0_spi_68	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_4	C7X256V0_CLEC_gic_spi_36	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_5	GICSS0_spi_69	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_5	C7X256V0_CLEC_gic_spi_37	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_6	GICSS0_spi_70	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_6	C7X256V0_CLEC_gic_spi_38	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_7	GICSS0_spi_71	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_7	C7X256V0_CLEC_gic_spi_39	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_8	GICSS0_spi_72	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_8	C7X256V0_CLEC_gic_spi_40	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_9	GICSS0_spi_73	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_9	C7X256V0_CLEC_gic_spi_41	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_10	GICSS0_spi_74	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_10	C7X256V0_CLEC_gic_spi_42	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_11	GICSS0_spi_75	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_11	C7X256V0_CLEC_gic_spi_43	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_12	GICSS0_spi_76	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_12	C7X256V0_CLEC_gic_spi_44	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_13	GICSS0_spi_77	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_13	C7X256V0_CLEC_gic_spi_45	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_14	GICSS0_spi_78	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_14	C7X256V0_CLEC_gic_spi_46	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_15	GICSS0_spi_79	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_15	C7X256V0_CLEC_gic_spi_47	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_16	GICSS0_spi_80	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_16	C7X256V0_CLEC_gic_spi_48	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_17	GICSS0_spi_81	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_17	C7X256V0_CLEC_gic_spi_49	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_18	GICSS0_spi_82	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_18	C7X256V0_CLEC_gic_spi_50	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_19	GICSS0_spi_83	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_19	C7X256V0_CLEC_gic_spi_51	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_20	GICSS0_spi_84	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_20	C7X256V0_CLEC_gic_spi_52	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_21	GICSS0_spi_85	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_21	C7X256V0_CLEC_gic_spi_53	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_22	GICSS0_spi_86	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_22	C7X256V0_CLEC_gic_spi_54	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_23	GICSS0_spi_87	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_23	C7X256V0_CLEC_gic_spi_55	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_24	GICSS0_spi_88	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_24	C7X256V0_CLEC_gic_spi_56	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_25	GICSS0_spi_89	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_25	C7X256V0_CLEC_gic_spi_57	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_26	GICSS0_spi_90	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_26	C7X256V0_CLEC_gic_spi_58	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_27	GICSS0_spi_91	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_27	C7X256V0_CLEC_gic_spi_59	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_28	GICSS0_spi_92	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_28	C7X256V0_CLEC_gic_spi_60	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_29	GICSS0_spi_93	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_29	C7X256V0_CLEC_gic_spi_61	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_30	GICSS0_spi_94	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_30	C7X256V0_CLEC_gic_spi_62	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_31	GICSS0_spi_95	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_31	C7X256V0_CLEC_gic_spi_63	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_32	GICSS0_spi_96	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_32	C7X256V0_CLEC_gic_spi_64	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_33	GICSS0_spi_97	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_33	C7X256V0_CLEC_gic_spi_65	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_34	GICSS0_spi_98	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_34	C7X256V0_CLEC_gic_spi_66	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_35	GICSS0_spi_99	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_35	C7X256V0_CLEC_gic_spi_67	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_36	GICSS0_spi_100	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_36	C7X256V0_CLEC_gic_spi_68	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_37	GICSS0_spi_101	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_37	C7X256V0_CLEC_gic_spi_69	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_38	GICSS0_spi_102	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_38	C7X256V0_CLEC_gic_spi_70	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_39	GICSS0_spi_103	GICSS0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_39	C7X256V0_CLEC_gic_spi_71	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_40	WKUP_R5FSS0_CORE0_intr_64	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_41	WKUP_R5FSS0_CORE0_intr_65	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_42	WKUP_R5FSS0_CORE0_intr_66	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_43	WKUP_R5FSS0_CORE0_intr_67	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_44	WKUP_R5FSS0_CORE0_intr_68	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_45	WKUP_R5FSS0_CORE0_intr_69	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_46	WKUP_R5FSS0_CORE0_intr_70	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_47	WKUP_R5FSS0_CORE0_intr_71	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_48	WKUP_R5FSS0_CORE0_intr_72	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_49	WKUP_R5FSS0_CORE0_intr_73	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_50	WKUP_R5FSS0_CORE0_intr_74	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_51	WKUP_R5FSS0_CORE0_intr_75	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_52	WKUP_R5FSS0_CORE0_intr_76	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_53	WKUP_R5FSS0_CORE0_intr_77	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_54	WKUP_R5FSS0_CORE0_intr_78	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_55	WKUP_R5FSS0_CORE0_intr_79	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_56	WKUP_R5FSS0_CORE0_intr_80	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_57	WKUP_R5FSS0_CORE0_intr_81	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_58	WKUP_R5FSS0_CORE0_intr_82	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_59	WKUP_R5FSS0_CORE0_intr_83	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_60	WKUP_R5FSS0_CORE0_intr_84	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_61	WKUP_R5FSS0_CORE0_intr_85	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_62	WKUP_R5FSS0_CORE0_intr_86	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_63	WKUP_R5FSS0_CORE0_intr_87	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_64	WKUP_R5FSS0_CORE0_intr_88	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_65	WKUP_R5FSS0_CORE0_intr_89	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_66	WKUP_R5FSS0_CORE0_intr_90	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_67	WKUP_R5FSS0_CORE0_intr_91	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_68	WKUP_R5FSS0_CORE0_intr_92	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_69	WKUP_R5FSS0_CORE0_intr_93	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_70	WKUP_R5FSS0_CORE0_intr_94	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_71	WKUP_R5FSS0_CORE0_intr_95	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_72	WKUP_R5FSS0_CORE0_intr_8	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_73	WKUP_R5FSS0_CORE0_intr_9	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_74	WKUP_R5FSS0_CORE0_intr_10	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_75	WKUP_R5FSS0_CORE0_intr_11	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_76	WKUP_R5FSS0_CORE0_intr_12	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_77	WKUP_R5FSS0_CORE0_intr_13	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_78	WKUP_R5FSS0_CORE0_intr_14	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_79	WKUP_R5FSS0_CORE0_intr_15	WKUP_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_84	C7X256V0_CLEC_soc_events_in_16	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_85	C7X256V0_CLEC_soc_events_in_17	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_86	C7X256V0_CLEC_soc_events_in_18	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_87	C7X256V0_CLEC_soc_events_in_19	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_88	C7X256V0_CLEC_soc_events_in_20	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_89	C7X256V0_CLEC_soc_events_in_21	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_90	C7X256V0_CLEC_soc_events_in_22	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_91	C7X256V0_CLEC_soc_events_in_23	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_92	C7X256V0_CLEC_soc_events_in_24	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_93	C7X256V0_CLEC_soc_events_in_25	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_94	C7X256V0_CLEC_soc_events_in_26	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_95	C7X256V0_CLEC_soc_events_in_27	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_96	C7X256V0_CLEC_soc_events_in_28	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_97	C7X256V0_CLEC_soc_events_in_29	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_98	C7X256V0_CLEC_soc_events_in_30	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_99	C7X256V0_CLEC_soc_events_in_31	C7X256V0_CLEC	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_168	MCU_R5FSS0_CORE0_cpu0_intr_64	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_169	MCU_R5FSS0_CORE0_cpu0_intr_65	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_170	MCU_R5FSS0_CORE0_cpu0_intr_66	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_171	MCU_R5FSS0_CORE0_cpu0_intr_67	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_172	MCU_R5FSS0_CORE0_cpu0_intr_68	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_173	MCU_R5FSS0_CORE0_cpu0_intr_69	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_174	MCU_R5FSS0_CORE0_cpu0_intr_70	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_175	MCU_R5FSS0_CORE0_cpu0_intr_71	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_176	MCU_R5FSS0_CORE0_cpu0_intr_72	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_177	MCU_R5FSS0_CORE0_cpu0_intr_73	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_178	MCU_R5FSS0_CORE0_cpu0_intr_74	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_179	MCU_R5FSS0_CORE0_cpu0_intr_75	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level

Table 4-119. Hardware Requests for DMASS_INTAGGR_0 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_180	MCU_R5FSS0_CORE0_cpu0_intr_76	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_181	MCU_R5FSS0_CORE0_cpu0_intr_77	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_182	MCU_R5FSS0_CORE0_cpu0_intr_78	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_intaggr_vintr_pend_183	MCU_R5FSS0_CORE0_cpu0_intr_79	MCU_R5FSS0_CORE0	DMASS0_INTAGGR_0 interrupt request	level

4.7 Audio

4.7.1 Multichannel Audio Serial Port (MCASP)

This section contains the integration details for the MCASP module on this device. For further information, see the *Multichannel Audio Serial Port (MCASP)* section of the *Peripherals* chapter.

4.7.1.1 MCASP Unsupported Features

The following features are not supported on this family of devices:

- Muting output (AMUTE)
- Muting input (AMUTEIN)
- Instances may not support all pin options. See device specific Datasheet for details on pin support of each MCASP instance.

4.7.1.2 MCASP Integration

Table 4-120. MCASP Module Allocations

Instance	MAIN	MCU	WKUP
MCASP0	✓		
MCASP1	✓		
MCASP2	✓		

Table 4-121. Integration Attributes for MCASP

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCASP0	PSC0	GP_Core_CTL	LPSC_main_mcasp_0	17	OFF	YES	LPSC_main_IP
MCASP1	PSC0	GP_Core_CTL	LPSC_main_mcasp_1	18	OFF	YES	LPSC_main_IP
MCASP2	PSC0	GP_Core_CTL	LPSC_main_mcasp_2	19	OFF	YES	LPSC_main_IP

Table 4-122. Clock Integration for MCASP

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCASP0	AUX_CLK	MAIN_PLL2_HSDIV8_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL[0:0]=0	auxillary clock input. audio clocks are derived from this clock.
MCASP0	AUX_CLK	MAIN_PLL1_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL[0:0]=1	auxillary clock input. audio clocks are derived from this clock.
MCASP0	ACLKR_I	MCASP0_ACLKR (PIN)		receive audio data clock
MCASP0	ACLKX_I	MCASP0_ACLKX (PIN)		transmit audio data clock
MCASP0	AHCLKR_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[1:0]=0	receive audio high frequency clock
MCASP0	AHCLKR_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP0	AHCLKR_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP0	AHCLKR_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[1:0]=2	receive audio high frequency clock

Table 4-122. Clock Integration for MCASP (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCASP0	AHCLKR_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[1:0]=3	receive audio high frequency clock
MCASP0	AHCLKX_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[9:8]=0	transmit audio high frequency clock
MCASP0	AHCLKX_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[9:8]=1	transmit audio high frequency clock
MCASP0	AHCLKX_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[9:8]=1	transmit audio high frequency clock
MCASP0	AHCLKX_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[9:8]=2	transmit audio high frequency clock
MCASP0	AHCLKX_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL[9:8]=3	transmit audio high frequency clock
MCASP0	FICLK	MAIN_SYSCLK0/2		functional and interface clock
MCASP1	AUX_CLK	MAIN_PLL2_HSDIV8_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL[0:0]=0	auxillary clock input. audio clocks are derived from this clock.
MCASP1	AUX_CLK	MAIN_PLL1_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL[0:0]=1	auxillary clock input. audio clocks are derived from this clock.
MCASP1	ACLKR_I	MCASP1_ACLKR (PIN)		receive audio data clock
MCASP1	ACLKX_I	MCASP1_ACLKX (PIN)		transmit audio data clock
MCASP1	AHCLKR_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[1:0]=0	receive audio high frequency clock
MCASP1	AHCLKR_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP1	AHCLKR_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP1	AHCLKR_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[1:0]=2	receive audio high frequency clock
MCASP1	AHCLKR_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[1:0]=3	receive audio high frequency clock
MCASP1	AHCLKX_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[9:8]=0	transmit audio high frequency clock
MCASP1	AHCLKX_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[9:8]=1	transmit audio high frequency clock
MCASP1	AHCLKX_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[9:8]=1	transmit audio high frequency clock

Table 4-122. Clock Integration for MCASP (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCASP1	AHCLKX_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[9:8]=2	transmit audio high frequency clock
MCASP1	AHCLKX_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL[9:8]=3	transmit audio high frequency clock
MCASP1	FICLK	MAIN_SYSCLK0/2		functional and interface clock
MCASP2	AUX_CLK	MAIN_PLL2_HSDIV8_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL[0:0]=0	auxillary clock input. audio clocks are derived from this clock.
MCASP2	AUX_CLK	MAIN_PLL1_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL[0:0]=1	auxillary clock input. audio clocks are derived from this clock.
MCASP2	ACLKR_I	MCASP2_ACLKR (PIN)		receive audio data clock
MCASP2	ACLKX_I	MCASP2_ACLKX (PIN)		transmit audio data clock
MCASP2	AHCLKR_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[1:0]=0	receive audio high frequency clock
MCASP2	AHCLKR_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP2	AHCLKR_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[1:0]=1	receive audio high frequency clock
MCASP2	AHCLKR_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[1:0]=2	receive audio high frequency clock
MCASP2	AHCLKR_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[1:0]=3	receive audio high frequency clock
MCASP2	AHCLKX_I	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[9:8]=0	transmit audio high frequency clock
MCASP2	AHCLKX_I	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[9:8]=1	transmit audio high frequency clock
MCASP2	AHCLKX_I	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[9:8]=1	transmit audio high frequency clock
MCASP2	AHCLKX_I	AUDIO_EXT_REFCLK0 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[9:8]=2	transmit audio high frequency clock
MCASP2	AHCLKX_I	AUDIO_EXT_REFCLK1 (PIN)	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL[9:8]=3	transmit audio high frequency clock
MCASP2	FICLK	MAIN_SYSCLK0/2		functional and interface clock

Table 4-123. Reset Integration for MCASP

Module Instance	Source	Description
MCASP0	PSC0	MCASP0 reset
MCASP1	PSC0	MCASP1 reset

Table 4-123. Reset Integration for MCASP (continued)

Module Instance	Source	Description
MCASP2	PSC0	MCASP2 reset

Table 4-124. Hardware Requests for MCASP

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP0	MCASP0_rec_dma_event_req_0	PDMA2_mcasp_main_0_rx_0	PDMA2	MCASP0 interrupt request	pulse
MCASP0	MCASP0_rec_intr_pend_0	GICSS0_spi_267	GICSS0	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	WKUP_R5FSS0_CORE0_intr_98	WKUP_R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_120	MCU_R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_235	C7X256V0_CLEC	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_dma_event_req_0	PDMA2_mcasp_main_0_tx_0	PDMA2	MCASP0 interrupt request	pulse
MCASP0	MCASP0_xmit_intr_pend_0	GICSS0_spi_268	GICSS0	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	WKUP_R5FSS0_CORE0_intr_99	WKUP_R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_121	MCU_R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_236	C7X256V0_CLEC	MCASP0 interrupt request	level
MCASP1	MCASP1_rec_dma_event_req_0	PDMA2_mcasp_main_1_rx_0	PDMA2	MCASP1 interrupt request	pulse
MCASP1	MCASP1_rec_intr_pend_0	GICSS0_spi_269	GICSS0	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	WKUP_R5FSS0_CORE0_intr_165	WKUP_R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_122	MCU_R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_237	C7X256V0_CLEC	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_dma_event_req_0	PDMA2_mcasp_main_1_tx_0	PDMA2	MCASP1 interrupt request	pulse
MCASP1	MCASP1_xmit_intr_pend_0	GICSS0_spi_270	GICSS0	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	WKUP_R5FSS0_CORE0_intr_166	WKUP_R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_123	MCU_R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_238	C7X256V0_CLEC	MCASP1 interrupt request	level
MCASP2	MCASP2_rec_dma_event_req_0	PDMA2_mcasp_main_2_rx_0	PDMA2	MCASP2 interrupt request	pulse
MCASP2	MCASP2_rec_intr_pend_0	GICSS0_spi_271	GICSS0	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	WKUP_R5FSS0_CORE0_intr_170	WKUP_R5FSS0_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_124	MCU_R5FSS0_CORE0	MCASP2 interrupt request	level

Table 4-124. Hardware Requests for MCASP (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP2	MCASP2_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_239	C7X256V0_CLEC	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_dma_event_req_0	PDMA2_mcasp_main_2_tx_0	PDMA2	MCASP2 interrupt request	pulse
MCASP2	MCASP2_xmit_intr_pend_0	GICSS0_spi_272	GICSS0	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	WKUP_R5FSS0_CORE0_intr_209	WKUP_R5FSS0_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_125	MCU_R5FSS0_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_240	C7X256V0_CLEC	MCASP2 interrupt request	level

4.8 General Connectivity

4.8.1 General Purpose Input/Output (GPIO)

This section contains the integration details for the GPIO modules on this device. For further information, see the *General-Purpose Interface* section of the *Peripherals* chapter.

4.8.1.1 GPIO Unsupported Features

The following features are not supported on this family of devices:

- The following apply to MCU_GPIO0:
  - MCU_GPIO0_[143:24] are not pinned out.
  - Interrupts [143:24] are not pinned out.
  - Bank Interrupts [8:2] are not pinned out.
- The following apply to GPIO0:
  - GPIO0_[143:92] are not pinned out.
  - Interrupts [143:92] are not pinned out.
  - Bank Interrupts [8:6] are not pinned out.
- The following apply to GPIO1:
  - GPIO1_[143:52] are not pinned out.
  - Interrupts [143:52] are not pinned out.
  - Bank Interrupts [8:4] are not pinned out.

4.8.1.2 GPIO Integration

Table 4-125. GPIO Module Allocations

Instance	MAIN	MCU	WKUP
GPIO0	✓		
GPIO1	✓		
MCU_GPIO0		✓	

Table 4-126. Integration Attributes for GPIO

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
GPIO0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
GPIO1	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
MCU_GPIO0	WKUP_PSC0	GP_core_CTL_MCU	LPSC_mcu_alwayson	0	ON	NO	

Table 4-127. Clock Integration for GPIO

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
GPIO0	FICLK	MAIN_SYSCLK0/4		functional and interface clock
GPIO1	FICLK	MAIN_SYSCLK0/4		functional and interface clock
MCU_GPIO0	FICLK	MCU_SYSCLK0	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL[1:0]=0	functional and interface clock
MCU_GPIO0	FICLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL[1:0]=1	functional and interface clock
MCU_GPIO0	FICLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL[1:0]=2	functional and interface clock

Table 4-127. Clock Integration for GPIO (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_GPIO0	FICLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL[1:0]=3	functional and interface clock

Table 4-128. Reset Integration for GPIO

Module Instance	Source	Description
GPIO0	PSC0	GPIO0 reset
GPIO1	PSC0	GPIO1 reset
MCU_GPIO0	WKUP_PSC0	MCU_GPIO0 reset

Table 4-129. Hardware Requests for GPIO

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_0	MAIN_GPIOMUX_INTROUTER0_in_0	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_1	MAIN_GPIOMUX_INTROUTER0_in_1	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_2	MAIN_GPIOMUX_INTROUTER0_in_2	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_3	MAIN_GPIOMUX_INTROUTER0_in_3	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_4	MAIN_GPIOMUX_INTROUTER0_in_4	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_5	MAIN_GPIOMUX_INTROUTER0_in_5	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_6	MAIN_GPIOMUX_INTROUTER0_in_6	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_7	MAIN_GPIOMUX_INTROUTER0_in_7	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_8	MAIN_GPIOMUX_INTROUTER0_in_8	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_9	MAIN_GPIOMUX_INTROUTER0_in_9	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_10	MAIN_GPIOMUX_INTROUTER0_in_10	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_11	MAIN_GPIOMUX_INTROUTER0_in_11	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_12	MAIN_GPIOMUX_INTROUTER0_in_12	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_13	MAIN_GPIOMUX_INTROUTER0_in_13	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_14	MAIN_GPIOMUX_INTROUTER0_in_14	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_15	MAIN_GPIOMUX_INTROUTER0_in_15	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_16	MAIN_GPIOMUX_INTROUTER0_in_16	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_17	MAIN_GPIOMUX_INTROUTER0_in_17	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_18	MAIN_GPIOMUX_INTROUTER0_in_18	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_19	MAIN_GPIOMUX_INTROUTER0_in_19	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_20	MAIN_GPIOMUX_INTROUTER0_in_20	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_21	MAIN_GPIOMUX_INTROUTER0_in_21	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_22	MAIN_GPIOMUX_INTROUTER0_in_22	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_23	MAIN_GPIOMUX_INTROUTER0_in_23	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_24	MAIN_GPIOMUX_INTROUTER0_in_24	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_25	MAIN_GPIOMUX_INTROUTER0_in_25	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_26	MAIN_GPIOMUX_INTROUTER0_in_26	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_27	MAIN_GPIOMUX_INTROUTER0_in_27	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_28	MAIN_GPIOMUX_INTROUTER0_in_28	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_29	MAIN_GPIOMUX_INTROUTER0_in_29	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_30	MAIN_GPIOMUX_INTROUTER0_in_30	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_31	MAIN_GPIOMUX_INTROUTER0_in_31	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_32	MAIN_GPIOMUX_INTROUTER0_in_32	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_33	MAIN_GPIOMUX_INTROUTER0_in_33	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_34	MAIN_GPIOMUX_INTROUTER0_in_34	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_35	MAIN_GPIOMUX_INTROUTER0_in_35	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_36	MAIN_GPIOMUX_INTROUTER0_in_36	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_37	MAIN_GPIOMUX_INTROUTER0_in_37	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_38	MAIN_GPIOMUX_INTROUTER0_in_38	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_39	MAIN_GPIOMUX_INTROUTER0_in_39	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_40	MAIN_GPIOMUX_INTROUTER0_in_40	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_41	MAIN_GPIOMUX_INTROUTER0_in_41	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_42	MAIN_GPIOMUX_INTROUTER0_in_42	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_43	MAIN_GPIOMUX_INTROUTER0_in_43	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_44	MAIN_GPIOMUX_INTROUTER0_in_44	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_45	MAIN_GPIOMUX_INTROUTER0_in_45	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_46	MAIN_GPIOMUX_INTROUTER0_in_46	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_47	MAIN_GPIOMUX_INTROUTER0_in_47	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_48	MAIN_GPIOMUX_INTROUTER0_in_48	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_49	MAIN_GPIOMUX_INTROUTER0_in_49	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_50	MAIN_GPIOMUX_INTROUTER0_in_50	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_51	MAIN_GPIOMUX_INTROUTER0_in_51	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_52	MAIN_GPIOMUX_INTROUTER0_in_52	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_53	MAIN_GPIOMUX_INTROUTER0_in_53	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_54	MAIN_GPIOMUX_INTROUTER0_in_54	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_55	MAIN_GPIOMUX_INTROUTER0_in_55	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_56	MAIN_GPIOMUX_INTROUTER0_in_56	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_57	MAIN_GPIOMUX_INTROUTER0_in_57	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_58	MAIN_GPIOMUX_INTROUTER0_in_58	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_59	MAIN_GPIOMUX_INTROUTER0_in_59	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_60	MAIN_GPIOMUX_INTROUTER0_in_60	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_61	MAIN_GPIOMUX_INTROUTER0_in_61	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_62	MAIN_GPIOMUX_INTROUTER0_in_62	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_63	MAIN_GPIOMUX_INTROUTER0_in_63	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_64	MAIN_GPIOMUX_INTROUTER0_in_64	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_65	MAIN_GPIOMUX_INTROUTER0_in_65	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_66	MAIN_GPIOMUX_INTROUTER0_in_66	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_67	MAIN_GPIOMUX_INTROUTER0_in_67	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_68	MAIN_GPIOMUX_INTROUTER0_in_68	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_69	MAIN_GPIOMUX_INTROUTER0_in_69	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_70	MAIN_GPIOMUX_INTROUTER0_in_70	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_71	MAIN_GPIOMUX_INTROUTER0_in_71	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_72	MAIN_GPIOMUX_INTROUTER0_in_72	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_73	MAIN_GPIOMUX_INTROUTER0_in_73	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_74	MAIN_GPIOMUX_INTROUTER0_in_74	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_75	MAIN_GPIOMUX_INTROUTER0_in_75	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_76	MAIN_GPIOMUX_INTROUTER0_in_76	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_77	MAIN_GPIOMUX_INTROUTER0_in_77	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_78	MAIN_GPIOMUX_INTROUTER0_in_78	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_79	MAIN_GPIOMUX_INTROUTER0_in_79	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_80	MAIN_GPIOMUX_INTROUTER0_in_80	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_81	MAIN_GPIOMUX_INTROUTER0_in_81	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_82	MAIN_GPIOMUX_INTROUTER0_in_82	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_83	MAIN_GPIOMUX_INTROUTER0_in_83	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_84	MAIN_GPIOMUX_INTROUTER0_in_84	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_85	MAIN_GPIOMUX_INTROUTER0_in_85	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_86	MAIN_GPIOMUX_INTROUTER0_in_86	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_87	MAIN_GPIOMUX_INTROUTER0_in_87	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_88	MAIN_GPIOMUX_INTROUTER0_in_88	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_89	MAIN_GPIOMUX_INTROUTER0_in_89	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_90	MAIN_GPIOMUX_INTROUTER0_in_176	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_91	MAIN_GPIOMUX_INTROUTER0_in_177	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_0	MAIN_GPIOMUX_INTROUTER0_in_190	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_0	WKUP_R5FSS0_CORE0_intr_56	WKUP_R5FSS0_CORE0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_1	MAIN_GPIOMUX_INTROUTER0_in_191	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_1	WKUP_R5FSS0_CORE0_intr_57	WKUP_R5FSS0_CORE0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_2	MAIN_GPIOMUX_INTROUTER0_in_192	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_bank_3	MAIN_GPIOMUX_INTROUTER0_in_193	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_4	MAIN_GPIOMUX_INTROUTER0_in_194	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_5	MAIN_GPIOMUX_INTROUTER0_in_195	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO1	GPIO1_gpio_0	MAIN_GPIOMUX_INTROUTER0_in_90	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_1	MAIN_GPIOMUX_INTROUTER0_in_91	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_2	MAIN_GPIOMUX_INTROUTER0_in_92	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_3	MAIN_GPIOMUX_INTROUTER0_in_93	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_4	MAIN_GPIOMUX_INTROUTER0_in_94	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_5	MAIN_GPIOMUX_INTROUTER0_in_95	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_6	MAIN_GPIOMUX_INTROUTER0_in_96	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_7	MAIN_GPIOMUX_INTROUTER0_in_97	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_8	MAIN_GPIOMUX_INTROUTER0_in_98	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_9	MAIN_GPIOMUX_INTROUTER0_in_99	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_10	MAIN_GPIOMUX_INTROUTER0_in_100	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_11	MAIN_GPIOMUX_INTROUTER0_in_101	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_12	MAIN_GPIOMUX_INTROUTER0_in_102	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_13	MAIN_GPIOMUX_INTROUTER0_in_103	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_14	MAIN_GPIOMUX_INTROUTER0_in_104	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_15	MAIN_GPIOMUX_INTROUTER0_in_105	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_16	MAIN_GPIOMUX_INTROUTER0_in_106	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_17	MAIN_GPIOMUX_INTROUTER0_in_107	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_18	MAIN_GPIOMUX_INTROUTER0_in_108	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_19	MAIN_GPIOMUX_INTROUTER0_in_109	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_20	MAIN_GPIOMUX_INTROUTER0_in_110	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_21	MAIN_GPIOMUX_INTROUTER0_in_111	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_22	MAIN_GPIOMUX_INTROUTER0_in_112	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO1	GPIO1_gpio_23	MAIN_GPIOMUX_INTROUTER0_in_113	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_24	MAIN_GPIOMUX_INTROUTER0_in_114	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_25	MAIN_GPIOMUX_INTROUTER0_in_115	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_26	MAIN_GPIOMUX_INTROUTER0_in_116	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_27	MAIN_GPIOMUX_INTROUTER0_in_117	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_28	MAIN_GPIOMUX_INTROUTER0_in_118	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_29	MAIN_GPIOMUX_INTROUTER0_in_119	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_30	MAIN_GPIOMUX_INTROUTER0_in_120	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_31	MAIN_GPIOMUX_INTROUTER0_in_121	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_32	MAIN_GPIOMUX_INTROUTER0_in_122	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_33	MAIN_GPIOMUX_INTROUTER0_in_123	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_34	MAIN_GPIOMUX_INTROUTER0_in_124	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_35	MAIN_GPIOMUX_INTROUTER0_in_125	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_36	MAIN_GPIOMUX_INTROUTER0_in_126	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_37	MAIN_GPIOMUX_INTROUTER0_in_127	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_38	MAIN_GPIOMUX_INTROUTER0_in_128	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_39	MAIN_GPIOMUX_INTROUTER0_in_129	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_40	MAIN_GPIOMUX_INTROUTER0_in_130	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_41	MAIN_GPIOMUX_INTROUTER0_in_131	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_42	MAIN_GPIOMUX_INTROUTER0_in_132	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_43	MAIN_GPIOMUX_INTROUTER0_in_133	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_44	MAIN_GPIOMUX_INTROUTER0_in_134	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_45	MAIN_GPIOMUX_INTROUTER0_in_135	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_46	MAIN_GPIOMUX_INTROUTER0_in_136	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_47	MAIN_GPIOMUX_INTROUTER0_in_137	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_48	MAIN_GPIOMUX_INTROUTER0_in_138	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO1	GPIO1_gpio_49	MAIN_GPIOMUX_INTROUTER0_in_139	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_50	MAIN_GPIOMUX_INTROUTER0_in_140	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_51	MAIN_GPIOMUX_INTROUTER0_in_141	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_52	MAIN_GPIOMUX_INTROUTER0_in_142	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_53	MAIN_GPIOMUX_INTROUTER0_in_143	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_54	MAIN_GPIOMUX_INTROUTER0_in_144	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_55	MAIN_GPIOMUX_INTROUTER0_in_145	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_56	MAIN_GPIOMUX_INTROUTER0_in_146	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_57	MAIN_GPIOMUX_INTROUTER0_in_147	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_58	MAIN_GPIOMUX_INTROUTER0_in_148	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_59	MAIN_GPIOMUX_INTROUTER0_in_149	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_60	MAIN_GPIOMUX_INTROUTER0_in_150	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_61	MAIN_GPIOMUX_INTROUTER0_in_151	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_62	MAIN_GPIOMUX_INTROUTER0_in_152	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_63	MAIN_GPIOMUX_INTROUTER0_in_153	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_64	MAIN_GPIOMUX_INTROUTER0_in_154	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_65	MAIN_GPIOMUX_INTROUTER0_in_155	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_66	MAIN_GPIOMUX_INTROUTER0_in_156	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_67	MAIN_GPIOMUX_INTROUTER0_in_157	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_68	MAIN_GPIOMUX_INTROUTER0_in_158	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_69	MAIN_GPIOMUX_INTROUTER0_in_159	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_70	MAIN_GPIOMUX_INTROUTER0_in_160	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_71	MAIN_GPIOMUX_INTROUTER0_in_161	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_bank_0	MAIN_GPIOMUX_INTROUTER0_in_180	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_bank_1	MAIN_GPIOMUX_INTROUTER0_in_181	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_bank_2	MAIN_GPIOMUX_INTROUTER0_in_182	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO1	GPIO1_gpio_bank_3	MAIN_GPIOMUX_INTROUTER0_in_183	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_bank_4	MAIN_GPIOMUX_INTROUTER0_in_184	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_0	WKUP_MCU_GPIOMUX_INTROUTER0_in_0	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_1	WKUP_MCU_GPIOMUX_INTROUTER0_in_1	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_2	WKUP_MCU_GPIOMUX_INTROUTER0_in_2	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_3	WKUP_MCU_GPIOMUX_INTROUTER0_in_3	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_4	WKUP_MCU_GPIOMUX_INTROUTER0_in_4	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_5	WKUP_MCU_GPIOMUX_INTROUTER0_in_5	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_6	WKUP_MCU_GPIOMUX_INTROUTER0_in_6	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_7	WKUP_MCU_GPIOMUX_INTROUTER0_in_7	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_8	WKUP_MCU_GPIOMUX_INTROUTER0_in_8	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_9	WKUP_MCU_GPIOMUX_INTROUTER0_in_9	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_10	WKUP_MCU_GPIOMUX_INTROUTER0_in_10	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_11	WKUP_MCU_GPIOMUX_INTROUTER0_in_11	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_12	WKUP_MCU_GPIOMUX_INTROUTER0_in_12	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_13	WKUP_MCU_GPIOMUX_INTROUTER0_in_13	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_14	WKUP_MCU_GPIOMUX_INTROUTER0_in_14	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_15	WKUP_MCU_GPIOMUX_INTROUTER0_in_15	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_16	WKUP_MCU_GPIOMUX_INTROUTER0_in_16	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse

Table 4-129. Hardware Requests for GPIO (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_GPIO0	MCU_GPIO0_gpio_17	WKUP_MCU_GPIOMUX_INTROUTER0_in_17	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_18	WKUP_MCU_GPIOMUX_INTROUTER0_in_18	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_19	WKUP_MCU_GPIOMUX_INTROUTER0_in_19	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_20	WKUP_MCU_GPIOMUX_INTROUTER0_in_20	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_21	WKUP_MCU_GPIOMUX_INTROUTER0_in_21	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_22	WKUP_MCU_GPIOMUX_INTROUTER0_in_22	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_23	WKUP_MCU_GPIOMUX_INTROUTER0_in_23	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_bank_0	WKUP_MCU_GPIOMUX_INTROUTER0_in_30	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_bank_1	WKUP_MCU_GPIOMUX_INTROUTER0_in_31	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_lvl_0	WKUP_R5FSS0_CORE0_intr_18	WKUP_R5FSS0_CORE0	MCU_GPIO0 interrupt request	level
MCU_GPIO0	MCU_GPIO0_gpio_lvl_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_2	WKUP_DEEPSLEEP_SOURCES0	MCU_GPIO0 interrupt request	level

4.8.1.3 GPIO Register/Pin Mapping

Table 4-130. MCU.GPIO.0 GPIO Register/Pin Mapping

Signal	Bank	Register(1)	Register Bit
MCU_GPIO0_0	Bank 0	MCU_GPIO0_*_01	0
MCU_GPIO0_1	Bank 0	MCU_GPIO0_*_01	1
MCU_GPIO0_2	Bank 0	MCU_GPIO0_*_01	2
MCU_GPIO0_3	Bank 0	MCU_GPIO0_*_01	3
MCU_GPIO0_4	Bank 0	MCU_GPIO0_*_01	4
MCU_GPIO0_5	Bank 0	MCU_GPIO0_*_01	5
MCU_GPIO0_6	Bank 0	MCU_GPIO0_*_01	6
MCU_GPIO0_7	Bank 0	MCU_GPIO0_*_01	7
MCU_GPIO0_8	Bank 0	MCU_GPIO0_*_01	8
MCU_GPIO0_9	Bank 0	MCU_GPIO0_*_01	9
MCU_GPIO0_10	Bank 0	MCU_GPIO0_*_01	10
MCU_GPIO0_11	Bank 0	MCU_GPIO0_*_01	11
MCU_GPIO0_12	Bank 0	MCU_GPIO0_*_01	12
MCU_GPIO0_13	Bank 0	MCU_GPIO0_*_01	13

Table 4-130. MCU.GPIO.0 GPIO Register/Pin Mapping (continued)

Signal	Bank	Register[1]	Register Bit
MCU_GPIO0_14	Bank 0	MCU_GPIO0_*_01	14
MCU_GPIO0_15	Bank 0	MCU_GPIO0_*_01	15
MCU_GPIO0_16	Bank 1	MCU_GPIO0_*_01	16
MCU_GPIO0_17	Bank 1	MCU_GPIO0_*_01	17
MCU_GPIO0_18	Bank 1	MCU_GPIO0_*_01	18
MCU_GPIO0_19	Bank 1	MCU_GPIO0_*_01	19
MCU_GPIO0_20	Bank 1	MCU_GPIO0_*_01	20
MCU_GPIO0_21	Bank 1	MCU_GPIO0_*_01	21
MCU_GPIO0_22	Bank 1	MCU_GPIO0_*_01	22
MCU_GPIO0_23	Bank 1	MCU_GPIO0_*_01	23

(1) * Represents: DIR, OUT_DATA, SET_DATA, CLR_DATA, IN_DATA, SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, CLR_FAL_TRIG, and INSTAT

Table 4-131. MAIN.GPIO.0 GPIO Register/Pin Mapping

Signal	Bank	Register[1]	Register Bit
GPIO0_0	Bank 0	GPIO0_*_01	0
GPIO0_1	Bank 0	GPIO0_*_01	1
GPIO0_2	Bank 0	GPIO0_*_01	2
GPIO0_3	Bank 0	GPIO0_*_01	3
GPIO0_4	Bank 0	GPIO0_*_01	4
GPIO0_5	Bank 0	GPIO0_*_01	5
GPIO0_6	Bank 0	GPIO0_*_01	6
GPIO0_7	Bank 0	GPIO0_*_01	7
GPIO0_8	Bank 0	GPIO0_*_01	8
GPIO0_9	Bank 0	GPIO0_*_01	9
GPIO0_10	Bank 0	GPIO0_*_01	10
GPIO0_11	Bank 0	GPIO0_*_01	11
GPIO0_12	Bank 0	GPIO0_*_01	12
GPIO0_13	Bank 0	GPIO0_*_01	13
GPIO0_14	Bank 0	GPIO0_*_01	14
GPIO0_15	Bank 0	GPIO0_*_01	15
GPIO0_16	Bank 1	GPIO0_*_01	16
GPIO0_17	Bank 1	GPIO0_*_01	17
GPIO0_18	Bank 1	GPIO0_*_01	18
GPIO0_19	Bank 1	GPIO0_*_01	19
GPIO0_20	Bank 1	GPIO0_*_01	20
GPIO0_21	Bank 1	GPIO0_*_01	21
GPIO0_22	Bank 1	GPIO0_*_01	22
GPIO0_23	Bank 1	GPIO0_*_01	23
GPIO0_24	Bank 1	GPIO0_*_01	24
GPIO0_25	Bank 1	GPIO0_*_01	25
GPIO0_26	Bank 1	GPIO0_*_01	26
GPIO0_27	Bank 1	GPIO0_*_01	27
GPIO0_28	Bank 1	GPIO0_*_01	28
GPIO0_29	Bank 1	GPIO0_*_01	29

Table 4-131. MAIN.GPIO.0 GPIO Register/Pin Mapping (continued)

Signal	Bank	Register[1]	Register Bit
GPIO0_30	Bank 1	GPIO0_*_01	30
GPIO0_31	Bank 1	GPIO0_*_01	31
GPIO0_32	Bank 2	GPIO0_*_23	0
GPIO0_33	Bank 2	GPIO0_*_23	1
GPIO0_34	Bank 2	GPIO0_*_23	2
GPIO0_35	Bank 2	GPIO0_*_23	3
GPIO0_36	Bank 2	GPIO0_*_23	4
GPIO0_37	Bank 2	GPIO0_*_23	5
GPIO0_38	Bank 2	GPIO0_*_23	6
GPIO0_39	Bank 2	GPIO0_*_23	7
GPIO0_40	Bank 2	GPIO0_*_23	8
GPIO0_41	Bank 2	GPIO0_*_23	9
GPIO0_42	Bank 2	GPIO0_*_23	10
GPIO0_43	Bank 2	GPIO0_*_23	11
GPIO0_44	Bank 2	GPIO0_*_23	12
GPIO0_45	Bank 2	GPIO0_*_23	13
GPIO0_46	Bank 2	GPIO0_*_23	14
GPIO0_47	Bank 2	GPIO0_*_23	15
GPIO0_48	Bank 3	GPIO0_*_23	16
GPIO0_49	Bank 3	GPIO0_*_23	17
GPIO0_50	Bank 3	GPIO0_*_23	18
GPIO0_51	Bank 3	GPIO0_*_23	19
GPIO0_52	Bank 3	GPIO0_*_23	20
GPIO0_53	Bank 3	GPIO0_*_23	21
GPIO0_54	Bank 3	GPIO0_*_23	22
GPIO0_55	Bank 3	GPIO0_*_23	23
GPIO0_56	Bank 3	GPIO0_*_23	24
GPIO0_57	Bank 3	GPIO0_*_23	25
GPIO0_58	Bank 3	GPIO0_*_23	26
GPIO0_59	Bank 3	GPIO0_*_23	27
GPIO0_60	Bank 3	GPIO0_*_23	28
GPIO0_61	Bank 3	GPIO0_*_23	29
GPIO0_62	Bank 3	GPIO0_*_23	30
GPIO0_63	Bank 3	GPIO0_*_23	31
GPIO0_64	Bank 4	GPIO0_*_45	0
GPIO0_65	Bank 4	GPIO0_*_45	1
GPIO0_66	Bank 4	GPIO0_*_45	2
GPIO0_67	Bank 4	GPIO0_*_45	3
GPIO0_68	Bank 4	GPIO0_*_45	4
GPIO0_69	Bank 4	GPIO0_*_45	5
GPIO0_70	Bank 4	GPIO0_*_45	6
GPIO0_71	Bank 4	GPIO0_*_45	7
GPIO0_72	Bank 4	GPIO0_*_45	8
GPIO0_73	Bank 4	GPIO0_*_45	9
GPIO0_74	Bank 4	GPIO0_*_45	10

Table 4-131. MAIN.GPIO.0 GPIO Register/Pin Mapping (continued)

Signal	Bank	Register(1)	Register Bit
GPIO0_75	Bank 4	GPIO0_*_45	11
GPIO0_76	Bank 4	GPIO0_*_45	12
GPIO0_77	Bank 4	GPIO0_*_45	13
GPIO0_78	Bank 4	GPIO0_*_45	14
GPIO0_79	Bank 4	GPIO0_*_45	15
GPIO0_80	Bank 5	GPIO0_*_45	16
GPIO0_81	Bank 5	GPIO0_*_45	17
GPIO0_82	Bank 5	GPIO0_*_45	18
GPIO0_83	Bank 5	GPIO0_*_45	19
GPIO0_84	Bank 5	GPIO0_*_45	20
GPIO0_85	Bank 5	GPIO0_*_45	21
GPIO0_86	Bank 5	GPIO0_*_45	22
GPIO0_87	Bank 5	GPIO0_*_45	23
GPIO0_88	Bank 5	GPIO0_*_45	24
GPIO0_89	Bank 5	GPIO0_*_45	25
GPIO0_90	Bank 5	GPIO0_*_45	26
GPIO0_91	Bank 5	GPIO0_*_45	27

(1) * Represents: DIR, OUT_DATA, SET_DATA, CLR_DATA, IN_DATA, SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, CLR_FAL_TRIG, and INSTAT

Table 4-132. MAIN.GPIO.1 GPIO Register/Pin Mapping

Signal	Bank	Register(1)	Register Bit
GPIO1_0	Bank 0	GPIO1_*_01	0
GPIO1_1	Bank 0	GPIO1_*_01	1
GPIO1_2	Bank 0	GPIO1_*_01	2
GPIO1_3	Bank 0	GPIO1_*_01	3
GPIO1_4	Bank 0	GPIO1_*_01	4
GPIO1_5	Bank 0	GPIO1_*_01	5
GPIO1_6	Bank 0	GPIO1_*_01	6
GPIO1_7	Bank 0	GPIO1_*_01	7
GPIO1_8	Bank 0	GPIO1_*_01	8
GPIO1_9	Bank 0	GPIO1_*_01	9
GPIO1_10	Bank 0	GPIO1_*_01	10
GPIO1_11	Bank 0	GPIO1_*_01	11
GPIO1_12	Bank 0	GPIO1_*_01	12
GPIO1_13	Bank 0	GPIO1_*_01	13
GPIO1_14	Bank 0	GPIO1_*_01	14
GPIO1_15	Bank 0	GPIO1_*_01	15
GPIO1_16	Bank 1	GPIO1_*_01	16
GPIO1_17	Bank 1	GPIO1_*_01	17
GPIO1_18	Bank 1	GPIO1_*_01	18
GPIO1_19	Bank 1	GPIO1_*_01	19
GPIO1_20	Bank 1	GPIO1_*_01	20
GPIO1_21	Bank 1	GPIO1_*_01	21
GPIO1_22	Bank 1	GPIO1_*_01	22

Table 4-132. MAIN.GPIO.1 GPIO Register/Pin Mapping (continued)

Signal	Bank	Register(1)	Register Bit
GPIO1_23	Bank 1	GPIO1_*_01	23
GPIO1_24	Bank 1	GPIO1_*_01	24
GPIO1_25	Bank 1	GPIO1_*_01	25
GPIO1_26	Bank 1	GPIO1_*_01	26
GPIO1_27	Bank 1	GPIO1_*_01	27
GPIO1_28	Bank 1	GPIO1_*_01	28
GPIO1_29	Bank 1	GPIO1_*_01	29
GPIO1_30	Bank 1	GPIO1_*_01	30
GPIO1_31	Bank 1	GPIO1_*_01	31
GPIO1_32	Bank 2	GPIO1_*_23	0
GPIO1_33	Bank 2	GPIO1_*_23	1
GPIO1_34	Bank 2	GPIO1_*_23	2
GPIO1_35	Bank 2	GPIO1_*_23	3
GPIO1_36	Bank 2	GPIO1_*_23	4
GPIO1_37	Bank 2	GPIO1_*_23	5
GPIO1_38	Bank 2	GPIO1_*_23	6
GPIO1_39	Bank 2	GPIO1_*_23	7
GPIO1_40	Bank 2	GPIO1_*_23	8
GPIO1_41	Bank 2	GPIO1_*_23	9
GPIO1_42	Bank 2	GPIO1_*_23	10
GPIO1_43	Bank 2	GPIO1_*_23	11
GPIO1_44	Bank 2	GPIO1_*_23	12
GPIO1_45	Bank 2	GPIO1_*_23	13
GPIO1_46	Bank 2	GPIO1_*_23	14
GPIO1_47	Bank 2	GPIO1_*_23	15
GPIO1_48	Bank 3	GPIO1_*_23	16
GPIO1_49	Bank 3	GPIO1_*_23	17
GPIO1_50	Bank 3	GPIO1_*_23	18
GPIO1_51	Bank 3	GPIO1_*_23	19

(1) * Represents: DIR, OUT_DATA, SET_DATA, CLR_DATA, IN_DATA, SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, CLR_FAL_TRIG, and INSTAT

4.8.2 Inter-Integrated Circuit (I2C)

This section contains the integration details for the I2C module on this device. For further information, see the *Inter-Integrated Circuit (I2C)* section of the *Peripherals* chapter.

4.8.2.1 I2C Unsupported Features

The following features are not supported on this family of devices:

- Serial Camera Control Bus (SCCB) protocol
- DMA Mode
- Full I^2C electrical compliance for I2C modules using device pins with LVCMOS voltage buffers (Refer to chapter 4 of the device-specific Datasheet for details related to device *Terminal Configuration and Functions*)
- High-speed (3.4-Mbps) operation for I2C modules using device pins with LVCMOS voltage buffers (Refer to chapter 4 of the device-specific Datasheet for details related to device *Terminal Configuration and Functions*)
- Debug suspend mode
- Asynchronous wakeup (via IO Daisy Chain) for Main domain instances

- Serial Camera Control Bus (SCCB) protocol
- DMA Mode
- Debug suspend mode

4.8.2.2 I2C Integration

Table 4-133. I2C Module Allocations

Instance	MAIN	MCU	WKUP
I2C0	✓		
I2C1	✓		
I2C2	✓		
I2C3	✓		
MCU_I2C0		✓	
WKUP_I2C0			✓

Table 4-134. Integration Attributes for I2C

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
I2C0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
I2C1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
I2C2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
I2C3	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCU_I2C0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
WKUP_I2C0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-135. Clock Integration for I2C

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
I2C0	ICLK	MAIN_SYSCLK0/4		interface clock
I2C0	FCLK	MAIN_PLL1_HSDIV0_CLKOUT/2		functional clock
I2C1	ICLK	MAIN_SYSCLK0/4		interface clock
I2C1	FCLK	MAIN_PLL1_HSDIV0_CLKOUT/2		functional clock

Table 4-135. Clock Integration for I2C (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
I2C2	ICLK	MAIN_SYSCLK0/4		interface clock
I2C2	FCLK	MAIN_PLL1_HSDIV0_CLKOUT/2		functional clock
I2C3	ICLK	MAIN_SYSCLK0/4		interface clock
I2C3	FCLK	MAIN_PLL1_HSDIV0_CLKOUT/2		functional clock
MCU_I2C0	ICLK	MCU_SYSCLK0/4		interface clock
MCU_I2C0	FCLK	MCU_PLL0_HSDIV1_CLKOUT		functional clock
WKUP_I2C0	ICLK	DM_CLK/4		interface clock
WKUP_I2C0	FCLK	MCU_PLL0_HSDIV1_CLKOUT		functional clock

Table 4-136. Reset Integration for I2C

Module Instance	Source	Description
I2C0	PSC0	I2C0 reset
I2C1	PSC0	I2C1 reset
I2C2	PSC0	I2C2 reset
I2C3	PSC0	I2C3 reset
MCU_I2C0	WKUP_PSC0	MCU_I2C0 reset
WKUP_I2C0	PSC0	WKUP_I2C0 reset

Table 4-137. Hardware Requests for I2C

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C0	I2C0_pointrpend_0	GICSS0_spi_193	GICSS0	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	WKUP_R5FSS0_CORE0_intr_193	WKUP_R5FSS0_CORE0	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_193	MCU_R5FSS0_CORE0	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	C7X256V0_CLEC_gic_spi_161	C7X256V0_CLEC	I2C0 interrupt request	level
I2C1	I2C1_pointrpend_0	GICSS0_spi_194	GICSS0	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	WKUP_R5FSS0_CORE0_intr_194	WKUP_R5FSS0_CORE0	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_194	MCU_R5FSS0_CORE0	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	C7X256V0_CLEC_gic_spi_162	C7X256V0_CLEC	I2C1 interrupt request	level
I2C2	I2C2_pointrpend_0	GICSS0_spi_195	GICSS0	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	WKUP_R5FSS0_CORE0_intr_195	WKUP_R5FSS0_CORE0	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_195	MCU_R5FSS0_CORE0	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	C7X256V0_CLEC_gic_spi_163	C7X256V0_CLEC	I2C2 interrupt request	level
I2C3	I2C3_pointrpend_0	GICSS0_spi_196	GICSS0	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	WKUP_R5FSS0_CORE0_intr_196	WKUP_R5FSS0_CORE0	I2C3 interrupt request	level

Table 4-137. Hardware Requests for I2C (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C3	I2C3_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_196	MCU_R5FSS0_CORE0	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	C7X256V0_CLEC_gic_spi_164	C7X256V0_CLEC	I2C3 interrupt request	level
MCU_I2C0	MCU_I2C0_pointrpend_0	GICSS0_spi_139	GICSS0	MCU_I2C0 interrupt request	level
MCU_I2C0	MCU_I2C0_pointrpend_0	WKUP_R5FSS0_CORE0_intr_197	WKUP_R5FSS0_CORE0	MCU_I2C0 interrupt request	level
MCU_I2C0	MCU_I2C0_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_197	MCU_R5FSS0_CORE0	MCU_I2C0 interrupt request	level
MCU_I2C0	MCU_I2C0_pointrpend_0	C7X256V0_CLEC_gic_spi_107	C7X256V0_CLEC	MCU_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_143	WKUP_R5FSS0_CORE0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_0	WKUP_DEEPSLEEP_SOURCES0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	GICSS0_spi_197	GICSS0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	WKUP_R5FSS0_CORE0_intr_190	WKUP_R5FSS0_CORE0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	MCU_R5FSS0_CORE0_cpu0_intr_190	MCU_R5FSS0_CORE0	WKUP_I2C0 interrupt request	level

4.8.2.3 I2C Additional Integration Details

Additional Integration Details for I2C.

I2C HS Mode

The MCU_I2C0 and WKUP_I2C0 IOs are a special IIC Open Drain Cell I2C_OD_FS. This cell supports I2C High Speed Mode when operating at 1.8V. (Note: At 3.3V the IO does not operate in HS Mode

4.8.3 Multichannel Serial Peripheral Interface (MCSPI)

This section contains the integration details for the MCSPI module on this device. For further information, see the *Multichannel Serial Peripheral Interface (MCSPI)* section of the *Peripherals* chapter.

4.8.3.1 MCSPI Unsupported Features

The following features are not supported on this family of devices:

- Peripheral mode wakeup.
- Retention during power down

4.8.3.2 MCSPI Integration

Table 4-138. MCSPI Module Allocations

Instance	MAIN	MCU	WKUP
MCSPI0	✓		
MCSPI1	✓		
MCSPI2	✓		
MCU_MCSPI0		✓	
MCU_MCSPI1		✓	

Table 4-139. Integration Attributes for MCSPI

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCSPI0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCSPI1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCSPI2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCU_MCSPI0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
MCU_MCSPI1	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO

Table 4-140. Clock Integration for MCSPI

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCSPI0	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		functional clock
MCSPI0	ICLK	MAIN_SYSCLK0/4		interface clock
MCSPI1	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		functional clock
MCSPI1	ICLK	MAIN_SYSCLK0/4		interface clock
MCSPI2	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		functional clock
MCSPI2	ICLK	MAIN_SYSCLK0/4		interface clock
MCU_MCSPI0	FCLK	MCU_PLL0_HSDIV6_CLKOUT/8		functional clock
MCU_MCSPI0	ICLK	MCU_SYSCLK0/2		interface clock
MCU_MCSPI1	FCLK	MCU_PLL0_HSDIV6_CLKOUT/8		functional clock
MCU_MCSPI1	ICLK	MCU_SYSCLK0/2		interface clock

Table 4-141. Reset Integration for MCSPI

Module Instance	Source	Description
MCSPI0	PSC0	MCSPI0 reset
MCSPI1	PSC0	MCSPI1 reset
MCSPI2	PSC0	MCSPI2 reset
MCU_MCSPI0	WKUP_PSC0	MCU_MCSPI0 reset
MCU_MCSPI1	WKUP_PSC0	MCU_MCSPI1 reset

Table 4-142. Hardware Requests for MCSPI

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI0	MCSPI0_dma_read_event_0	PDMA0_spi_main_0_rx_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_1	PDMA0_spi_main_0_rx_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_2	PDMA0_spi_main_0_rx_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_3	PDMA0_spi_main_0_rx_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_0	PDMA0_spi_main_0_tx_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_1	PDMA0_spi_main_0_tx_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_2	PDMA0_spi_main_0_tx_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_3	PDMA0_spi_main_0_tx_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_intr_spi_0	GICSS0_spi_204	GICSS0	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	WKUP_R5FSS0_CORE0_intr_204	WKUP_R5FSS0_CORE0	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	MCU_R5FSS0_CORE0_cpu0_intr_204	MCU_R5FSS0_CORE0	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	C7X256V0_CLEC_gic_spi_172	C7X256V0_CLEC	MCSPI0 interrupt request	level
MCSPI1	MCSPI1_dma_read_event_0	PDMA0_spi_main_1_rx_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_1	PDMA0_spi_main_1_rx_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_2	PDMA0_spi_main_1_rx_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_3	PDMA0_spi_main_1_rx_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_0	PDMA0_spi_main_1_tx_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_1	PDMA0_spi_main_1_tx_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_2	PDMA0_spi_main_1_tx_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_3	PDMA0_spi_main_1_tx_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_intr_spi_0	GICSS0_spi_205	GICSS0	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	WKUP_R5FSS0_CORE0_intr_205	WKUP_R5FSS0_CORE0	MCSPI1 interrupt request	level

Table 4-142. Hardware Requests for MCSPI (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI1	MCSPI1_intr_spi_0	MCU_R5FSS0_CORE0_cpu0_intr_205	MCU_R5FSS0_CORE0	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	C7X256V0_CLEC_gic_spi_173	C7X256V0_CLEC	MCSPI1 interrupt request	level
MCSPI2	MCSPI2_dma_read_event_0	PDMA0_spi_main_2_rx_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_1	PDMA0_spi_main_2_rx_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_2	PDMA0_spi_main_2_rx_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_3	PDMA0_spi_main_2_rx_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_0	PDMA0_spi_main_2_tx_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_1	PDMA0_spi_main_2_tx_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_2	PDMA0_spi_main_2_tx_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_3	PDMA0_spi_main_2_tx_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_intr_spi_0	GICSS0_spi_206	GICSS0	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	WKUP_R5FSS0_CORE0_intr_206	WKUP_R5FSS0_CORE0	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	MCU_R5FSS0_CORE0_cpu0_intr_206	MCU_R5FSS0_CORE0	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	C7X256V0_CLEC_gic_spi_174	C7X256V0_CLEC	MCSPI2 interrupt request	level
MCU_MCSPI0	MCU_MCSPI0_intr_spi_0	GICSS0_spi_208	GICSS0	MCU_MCSPI0 interrupt request	level
MCU_MCSPI0	MCU_MCSPI0_intr_spi_0	WKUP_R5FSS0_CORE0_intr_207	WKUP_R5FSS0_CORE0	MCU_MCSPI0 interrupt request	level
MCU_MCSPI0	MCU_MCSPI0_intr_spi_0	MCU_R5FSS0_CORE0_cpu0_intr_207	MCU_R5FSS0_CORE0	MCU_MCSPI0 interrupt request	level
MCU_MCSPI0	MCU_MCSPI0_intr_spi_0	C7X256V0_CLEC_gic_spi_176	C7X256V0_CLEC	MCU_MCSPI0 interrupt request	level
MCU_MCSPI1	MCU_MCSPI1_intr_spi_0	GICSS0_spi_209	GICSS0	MCU_MCSPI1 interrupt request	level
MCU_MCSPI1	MCU_MCSPI1_intr_spi_0	WKUP_R5FSS0_CORE0_intr_208	WKUP_R5FSS0_CORE0	MCU_MCSPI1 interrupt request	level
MCU_MCSPI1	MCU_MCSPI1_intr_spi_0	MCU_R5FSS0_CORE0_cpu0_intr_208	MCU_R5FSS0_CORE0	MCU_MCSPI1 interrupt request	level
MCU_MCSPI1	MCU_MCSPI1_intr_spi_0	C7X256V0_CLEC_gic_spi_177	C7X256V0_CLEC	MCU_MCSPI1 interrupt request	level

4.8.4 Universal Asynchronous Receiver/Transmitter (UART)

This section contains the integration details for the UART module on this device. For further information, see the *Universal Asynchronous Receiver/Transmitter (UART)* section of the *Peripherals* chapter.

4.8.4.1 UART Unsupported Features

The following features are not supported on this family of devices:

- 12Mbps for MCU and WKUP domains
- Full modem handshaking is not available on all instances. See device Datasheet for instances supporting full modem handshaking.
- Synchronous mode: SCLK is not pinned out
- ISO7816 mode
- SCR DMA mode 2
- Multi-drop transmission
- 9-bit mode

4.8.4.2 UART Integration

Table 4-143. UART Module Allocations

Instance	MAIN	MCU	WKUP
UART0	✓		
UART1	✓		
UART2	✓		
UART3	✓		
UART4	✓		
UART5	✓		
UART6	✓		
MCU_UART0		✓	
WKUP_UART0			✓

Table 4-144. Integration Attributes for UART

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
UART0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART3	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART4	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART5	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
UART6	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCU_UART0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
WKUP_UART0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-145. Clock Integration for UART

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
UART0	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL[0:0]=0 USART0_CLK_CTRL[1:0]	functional clock
UART0	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL[0:0]=1	functional clock
UART0	ICLK	MAIN_SYSCLK0/4		interface clock
UART1	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL[0:0]=0 USART1_CLK_CTRL[1:0]	functional clock
UART1	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL[0:0]=1	functional clock
UART1	ICLK	MAIN_SYSCLK0/4		interface clock
UART2	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL[0:0]=0 USART2_CLK_CTRL[1:0]	functional clock
UART2	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL[0:0]=1	functional clock
UART2	ICLK	MAIN_SYSCLK0/4		interface clock
UART3	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL[0:0]=0 USART3_CLK_CTRL[1:0]	functional clock
UART3	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL[0:0]=1	functional clock
UART3	ICLK	MAIN_SYSCLK0/4		interface clock
UART4	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL[0:0]=0 USART4_CLK_CTRL[1:0]	functional clock
UART4	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL[0:0]=1	functional clock
UART4	ICLK	MAIN_SYSCLK0/4		interface clock
UART5	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL[0:0]=0 USART5_CLK_CTRL[1:0]	functional clock
UART5	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL[0:0]=1	functional clock
UART5	ICLK	MAIN_SYSCLK0/4		interface clock

Table 4-145. Clock Integration for UART (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
UART6	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL[0:0]=0 USART6_CLK_CTRL[1:0]	functional clock
UART6	FCLK	MAIN_PLL1_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL[0:0]=1	functional clock
UART6	ICLK	MAIN_SYSCLK0/4		interface clock
MCU_UART0	FCLK	MCU_PLL0_HSDIV2_CLKOUT		functional clock
MCU_UART0	ICLK	MCU_SYSCLK0/2		interface clock
WKUP_UART0	FCLK	MCU_PLL0_HSDIV2_CLKOUT		functional clock
WKUP_UART0	ICLK	DM_CLK/4		interface clock

Table 4-146. Reset Integration for UART

Module Instance	Source	Description
UART0	PSC0	UART0 reset
UART1	PSC0	UART1 reset
UART2	PSC0	UART2 reset
UART3	PSC0	UART3 reset
UART4	PSC0	UART4 reset
UART5	PSC0	UART5 reset
UART6	PSC0	UART6 reset
MCU_UART0	WKUP_PSC0	MCU_UART0 reset
WKUP_UART0	PSC0	WKUP_UART0 reset

Table 4-147. Hardware Requests for UART

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART0	UART0_usart_dma_0	PDMA1_usart_main_0_tx_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_dma_1	PDMA1_usart_main_0_rx_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_irq_0	GICSS0_spi_210	GICSS0	UART0 interrupt request	level
UART0	UART0_usart_irq_0	WKUP_R5FSS0_CORE0_intr_210	WKUP_R5FSS0_CORE0	UART0 interrupt request	level
UART0	UART0_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_210	MCU_R5FSS0_CORE0	UART0 interrupt request	level
UART0	UART0_usart_irq_0	C7X256V0_CLEC_gic_spi_178	C7X256V0_CLEC	UART0 interrupt request	level
UART1	UART1_usart_dma_0	PDMA1_usart_main_1_tx_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_dma_1	PDMA1_usart_main_1_rx_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_irq_0	GICSS0_spi_211	GICSS0	UART1 interrupt request	level
UART1	UART1_usart_irq_0	WKUP_R5FSS0_CORE0_intr_211	WKUP_R5FSS0_CORE0	UART1 interrupt request	level
UART1	UART1_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_211	MCU_R5FSS0_CORE0	UART1 interrupt request	level

Table 4-147. Hardware Requests for UART (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART1	UART1_usart_irq_0	C7X256V0_CLEC_gic_spi_179	C7X256V0_CLEC	UART1 interrupt request	level
UART2	UART2_usart_dma_0	PDMA1_usart_main_2_tx_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_dma_1	PDMA1_usart_main_2_rx_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_irq_0	GICSS0_spi_212	GICSS0	UART2 interrupt request	level
UART2	UART2_usart_irq_0	WKUP_R5FSS0_CORE0_intr_212	WKUP_R5FSS0_CORE0	UART2 interrupt request	level
UART2	UART2_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_212	MCU_R5FSS0_CORE0	UART2 interrupt request	level
UART2	UART2_usart_irq_0	C7X256V0_CLEC_gic_spi_180	C7X256V0_CLEC	UART2 interrupt request	level
UART3	UART3_usart_dma_0	PDMA1_usart_main_3_tx_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_dma_1	PDMA1_usart_main_3_rx_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_irq_0	GICSS0_spi_213	GICSS0	UART3 interrupt request	level
UART3	UART3_usart_irq_0	WKUP_R5FSS0_CORE0_intr_213	WKUP_R5FSS0_CORE0	UART3 interrupt request	level
UART3	UART3_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_213	MCU_R5FSS0_CORE0	UART3 interrupt request	level
UART3	UART3_usart_irq_0	C7X256V0_CLEC_gic_spi_181	C7X256V0_CLEC	UART3 interrupt request	level
UART4	UART4_usart_dma_0	PDMA1_usart_main_4_tx_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_dma_1	PDMA1_usart_main_4_rx_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_irq_0	GICSS0_spi_214	GICSS0	UART4 interrupt request	level
UART4	UART4_usart_irq_0	WKUP_R5FSS0_CORE0_intr_214	WKUP_R5FSS0_CORE0	UART4 interrupt request	level
UART4	UART4_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_214	MCU_R5FSS0_CORE0	UART4 interrupt request	level
UART4	UART4_usart_irq_0	C7X256V0_CLEC_gic_spi_182	C7X256V0_CLEC	UART4 interrupt request	level
UART5	UART5_usart_dma_0	PDMA1_usart_main_5_tx_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_dma_1	PDMA1_usart_main_5_rx_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_irq_0	GICSS0_spi_215	GICSS0	UART5 interrupt request	level
UART5	UART5_usart_irq_0	WKUP_R5FSS0_CORE0_intr_215	WKUP_R5FSS0_CORE0	UART5 interrupt request	level
UART5	UART5_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_215	MCU_R5FSS0_CORE0	UART5 interrupt request	level
UART5	UART5_usart_irq_0	C7X256V0_CLEC_gic_spi_183	C7X256V0_CLEC	UART5 interrupt request	level
UART6	UART6_usart_dma_0	PDMA1_usart_main_6_tx_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_dma_1	PDMA1_usart_main_6_rx_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_irq_0	GICSS0_spi_216	GICSS0	UART6 interrupt request	level

Table 4-147. Hardware Requests for UART (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART6	UART6_usart_irq_0	WKUP_R5FSS0_CORE0_intr_216	WKUP_R5FSS0_CORE0	UART6 interrupt request	level
UART6	UART6_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_216	MCU_R5FSS0_CORE0	UART6 interrupt request	level
UART6	UART6_usart_irq_0	C7X256V0_CLEC_gic_spi_184	C7X256V0_CLEC	UART6 interrupt request	level
MCU_UART0	MCU_UART0_usart_irq_0	GICSS0_spi_217	GICSS0	MCU_UART0 interrupt request	level
MCU_UART0	MCU_UART0_usart_irq_0	WKUP_R5FSS0_CORE0_intr_217	WKUP_R5FSS0_CORE0	MCU_UART0 interrupt request	level
MCU_UART0	MCU_UART0_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_217	MCU_R5FSS0_CORE0	MCU_UART0 interrupt request	level
MCU_UART0	MCU_UART0_usart_irq_0	C7X256V0_CLEC_gic_spi_185	C7X256V0_CLEC	MCU_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_144	WKUP_R5FSS0_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_1	WKUP_DEEPSLEEP_SOURCES0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	GICSS0_spi_218	GICSS0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	WKUP_R5FSS0_CORE0_intr_219	WKUP_R5FSS0_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_219	MCU_R5FSS0_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	C7X256V0_CLEC_gic_spi_186	C7X256V0_CLEC	WKUP_UART0 interrupt request	level

4.9 High-speed Serial Interfaces

4.9.1 Gigabit Ethernet Switch (CPSW)

This section contains the integration details for the CPSW module on this device. For further information, see the *Gigabit Ethernet Switch (CPSW)* section of the *Peripherals* chapter.

4.9.1.1 CPSW Unsupported Features

The following features are not supported on this family of devices:

- Maximum frame size of 9600 bytes
- MII
- GMII Mode
- SGMII Mode
- MACSEC
- Synchronous Ethernet

4.9.1.2 cpsw Integration

Table 4-148. CPSW Module Allocations

Instance	MAIN	MCU	WKUP
CPSW0	✓		

Table 4-149. Integration Attributes for cpsw

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
CPSW0	PSC0	PD_CPSW	LPSC_CPSW3G	42	OFF	YES	LPSC_main_IP

Table 4-150. Clock Integration for cpsw

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
CPSW0	CPPI_ICLK	MAIN_SYSCLK0/2		cppi streaming packet interface clock
CPSW0	CPTS_RFT_CLK	MAIN_PLL2_HSDIV5_CLKOUT	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=0	cpts reference clock
CPSW0	CPTS_RFT_CLK	MAIN_PLL0_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=1	cpts reference clock
CPSW0	CPTS_RFT_CLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=2	cpts reference clock
CPSW0	CPTS_RFT_CLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=4	cpts reference clock
CPSW0	CPTS_RFT_CLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=5	cpts reference clock
CPSW0	CPTS_RFT_CLK	MCU_SYSCLK0	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=6	cpts reference clock
CPSW0	CPTS_RFT_CLK	MAIN_SYSCLK0	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL[2:0]=7	cpts reference clock
CPSW0	GMII1_MR_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		gmii input receive reference clock
CPSW0	GMII1_MT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		gmii input transmit reference clock

Table 4-150. Clock Integration for cpsw (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
CPSW0	GMII2_MR_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		gmii input receive reference clock
CPSW0	GMII2_MT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		gmii input transmit reference clock
CPSW0	GMII_RFT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/2		gmii input 125-mhz reference clock
CPSW0	RGMII_MHZ_250_CLK	MAIN_PLL2_HSDIV1_CLKOUT		rgmii 250-mhz reference clock
CPSW0	RGMII_MHZ_50_CLK	MAIN_PLL2_HSDIV1_CLKOUT/5		rgmii 50-mhz reference clock
CPSW0	RGMII_MHZ_5_CLK	MAIN_PLL2_HSDIV1_CLKOUT/50		rgmii 5-mhz reference clock
CPSW0	RMII1_MHZ_50_CLK	RMII1_REF_CLK (PIN)		rmii 50-mhz reference clock
CPSW0	RMII2_MHZ_50_CLK	RMII2_REF_CLK (PIN)		rmii 50-mhz reference clock

Table 4-151. Reset Integration for cpsw

Module Instance	Source	Description
CPSW0	PSC0	CPSW0 reset

Table 4-152. Hardware Requests for cpsw

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_cpts_comp_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout_CP_GEMAC_CPTS0_TS_COMP_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout	CPSW0 interrupt request	level
CPSW0	CPSW0_cpts_comp_0	CMP_EVENT_INTROUTER0_in_24	CMP_EVENT_INTROUTER0	CPSW0 interrupt request	level
CPSW0	CPSW0_cpts_genf0_0	TIMESYNC_EVENT_ROUTER0_in_16	TIMESYNC_EVENT_ROUTER0	CPSW0 interrupt request	level
CPSW0	CPSW0_cpts_genf1_0	TIMESYNC_EVENT_ROUTER0_in_17	TIMESYNC_EVENT_ROUTER0	CPSW0 interrupt request	level
CPSW0	CPSW0_cpts_sync_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout_CP_GEMAC_CPTS0_TS_SYNC_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout	CPSW0 interrupt request	level
CPSW0	CPSW0_cpts_sync_0	TIMESYNC_EVENT_ROUTER0_in_18	TIMESYNC_EVENT_ROUTER0	CPSW0 interrupt request	level
CPSW0	CPSW0_ecc_ded_pend_0	ESM0_esm_lvl_event_67	ESM0	CPSW0 interrupt request	level
CPSW0	CPSW0_ecc_sec_pend_0	ESM0_esm_lvl_event_3	ESM0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	GICSS0_spi_134	GICSS0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	WKUP_R5FSS0_CORE0_intr_134	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_134	MCU_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	C7X256V0_CLEC_gic_spi_102	C7X256V0_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	GICSS0_spi_135	GICSS0	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	WKUP_R5FSS0_CORE0_intr_135	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level

Table 4-152. Hardware Requests for cpsw (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_mdio_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_135	MCU_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	C7X256V0_CLEC_gic_spi_103	C7X256V0_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	GICSS0_spi_136	GICSS0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	WKUP_R5FSS0_CORE0_intr_136	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_136	MCU_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	C7X256V0_CLEC_gic_spi_104	C7X256V0_CLEC	CPSW0 interrupt request	level

4.9.2 Universal Serial Bus Subsystem (USB)

This section contains the integration details for the USB module on this device. For further information, see the *Universal Serial Bus Subsystem (USBSS)* section of the *Peripherals* chapter.

4.9.2.1 USB2SS Unsupported Features

The following features are not supported on this family of devices:

- Battery Charger Support
- Accessory Charger Adaptor Support
- On-The-Go (OTG)
- No Virtualization Support
- SuperSpeed (5Gb/s) operation
- USB 2.0 ECN: Link Power Management (LPM)
- Low Speed operation in device mode
- Charger Detection

4.9.2.2 USB Integration

Table 4-153. USB Module Allocations

Instance	MAIN	MCU	WKUP
USB0	✓		
USB1	✓		

Table 4-154. Integration Attributes for USB

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
USB0	PSC0	GP_Core_CTL	LPSC_USB_0	23	OFF	YES	LPSC_main_IP
USB1	PSC0	GP_Core_CTL	LPSC_USB_1	24	OFF	YES	LPSC_main_IP

Table 4-155. Clock Integration for USB

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
USB0	BUS_CLK	MAIN_SYSCLK0/2		functional and vbusp interface clock
USB0	USB2_APB_PCLK	MAIN_SYSCLK0/4		None
USB0	USB2_REFCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL[0:0]=0	usb reference clock
USB0	USB2_REFCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL[0:0]=0	usb reference clock
USB0	USB2_REFCLK	MAIN_PLL0_HSDIV8_CLKOUT	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL[0:0]=1	usb reference clock
USB1	BUS_CLK	MAIN_SYSCLK0/2		functional and vbusp interface clock
USB1	USB2_APB_PCLK	MAIN_SYSCLK0/4		None
USB1	USB2_REFCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_USB1_CLKSEL[0:0]=0	usb reference clock
USB1	USB2_REFCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_USB1_CLKSEL[0:0]=0	usb reference clock
USB1	USB2_REFCLK	MAIN_PLL0_HSDIV8_CLKOUT	WKUP_CTRL_MMR_CFG0_USB1_CLKSEL[0:0]=1	usb reference clock

Table 4-156. Reset Integration for USB

Module Instance	Source	Description
USB0	PSC0	USB0 reset
USB1	PSC0	USB1 reset

Table 4-157. Hardware Requests for USB

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB0	USB0_a_ecc_aggr_corrected_err_level_0	ESM0_esm_lvl_event_35	ESM0	USB0 interrupt request	level
USB0	USB0_a_ecc_aggr_uncorrected_err_level_0	ESM0_esm_lvl_event_111	ESM0	USB0 interrupt request	level
USB0	USB0_host_system_error_0	ESM0_esm_lvl_event_32	ESM0	USB0 interrupt request	level
USB0	USB0_irq_0	GICSS0_spi_220	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_0	WKUP_R5FSS0_CORE0_intr_220	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_220	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_0	C7X256V0_CLEC_gic_spi_188	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_1	GICSS0_spi_221	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_1	WKUP_R5FSS0_CORE0_intr_221	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_1	MCU_R5FSS0_CORE0_cpu0_intr_221	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_1	C7X256V0_CLEC_gic_spi_189	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_2	GICSS0_spi_222	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_2	WKUP_R5FSS0_CORE0_intr_222	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_2	MCU_R5FSS0_CORE0_cpu0_intr_222	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_2	C7X256V0_CLEC_gic_spi_190	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_3	GICSS0_spi_223	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_3	WKUP_R5FSS0_CORE0_intr_223	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_3	MCU_R5FSS0_CORE0_cpu0_intr_223	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_3	C7X256V0_CLEC_gic_spi_191	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_4	GICSS0_spi_224	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_4	WKUP_R5FSS0_CORE0_intr_224	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_4	MCU_R5FSS0_CORE0_cpu0_intr_224	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_4	C7X256V0_CLEC_gic_spi_192	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_5	GICSS0_spi_225	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_5	WKUP_R5FSS0_CORE0_intr_225	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_5	MCU_R5FSS0_CORE0_cpu0_intr_225	MCU_R5FSS0_CORE0	USB0 interrupt request	level

Table 4-157. Hardware Requests for USB (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB0	USB0_irq_5	C7X256V0_CLEC_gic_spi_193	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_6	GICSS0_spi_226	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_6	WKUP_R5FSS0_CORE0_intr_226	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_6	MCU_R5FSS0_CORE0_cpu0_intr_226	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_6	C7X256V0_CLEC_gic_spi_194	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_7	GICSS0_spi_227	GICSS0	USB0 interrupt request	level
USB0	USB0_irq_7	WKUP_R5FSS0_CORE0_intr_227	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_7	MCU_R5FSS0_CORE0_cpu0_intr_227	MCU_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_7	C7X256V0_CLEC_gic_spi_195	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_misc_level_0	GICSS0_spi_228	GICSS0	USB0 interrupt request	pulse
USB0	USB0_misc_level_0	WKUP_R5FSS0_CORE0_intr_228	WKUP_R5FSS0_CORE0	USB0 interrupt request	pulse
USB0	USB0_misc_level_0	MCU_R5FSS0_CORE0_cpu0_intr_228	MCU_R5FSS0_CORE0	USB0 interrupt request	pulse
USB0	USB0_misc_level_0	C7X256V0_CLEC_gic_spi_196	C7X256V0_CLEC	USB0 interrupt request	pulse
USB0	USB0_usb_wakeup_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_61	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_usb_wakeup_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_9	WKUP_DEEPSLEEP_SOURCES0	USB0 interrupt request	level
USB1	USB1_a_ecc_aggr_corrected_err_level_0	ESM0_esm_lvl_event_146	ESM0	USB1 interrupt request	level
USB1	USB1_a_ecc_aggr_uncorrected_err_level_0	ESM0_esm_lvl_event_147	ESM0	USB1 interrupt request	level
USB1	USB1_host_system_error_0	ESM0_esm_lvl_event_33	ESM0	USB1 interrupt request	level
USB1	USB1_irq_0	GICSS0_spi_258	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_0	WKUP_R5FSS0_CORE0_intr_230	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_0	MCU_R5FSS0_CORE0_cpu0_intr_230	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_0	C7X256V0_CLEC_gic_spi_226	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_1	GICSS0_spi_259	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_1	WKUP_R5FSS0_CORE0_intr_231	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_1	MCU_R5FSS0_CORE0_cpu0_intr_231	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_1	C7X256V0_CLEC_gic_spi_227	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_2	GICSS0_spi_260	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_2	WKUP_R5FSS0_CORE0_intr_232	WKUP_R5FSS0_CORE0	USB1 interrupt request	level

Table 4-157. Hardware Requests for USB (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB1	USB1_irq_2	MCU_R5FSS0_CORE0_cpu0_intr_232	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_2	C7X256V0_CLEC_gic_spi_228	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_3	GICSS0_spi_261	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_3	WKUP_R5FSS0_CORE0_intr_233	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_3	MCU_R5FSS0_CORE0_cpu0_intr_233	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_3	C7X256V0_CLEC_gic_spi_229	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_4	GICSS0_spi_262	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_4	WKUP_R5FSS0_CORE0_intr_234	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_4	MCU_R5FSS0_CORE0_cpu0_intr_234	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_4	C7X256V0_CLEC_gic_spi_230	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_5	GICSS0_spi_263	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_5	WKUP_R5FSS0_CORE0_intr_235	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_5	MCU_R5FSS0_CORE0_cpu0_intr_235	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_5	C7X256V0_CLEC_gic_spi_231	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_6	GICSS0_spi_264	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_6	WKUP_R5FSS0_CORE0_intr_236	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_6	MCU_R5FSS0_CORE0_cpu0_intr_236	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_6	C7X256V0_CLEC_gic_spi_232	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_irq_7	GICSS0_spi_265	GICSS0	USB1 interrupt request	level
USB1	USB1_irq_7	WKUP_R5FSS0_CORE0_intr_237	WKUP_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_7	MCU_R5FSS0_CORE0_cpu0_intr_237	MCU_R5FSS0_CORE0	USB1 interrupt request	level
USB1	USB1_irq_7	C7X256V0_CLEC_gic_spi_233	C7X256V0_CLEC	USB1 interrupt request	level
USB1	USB1_misc_level_0	GICSS0_spi_266	GICSS0	USB1 interrupt request	pulse
USB1	USB1_misc_level_0	WKUP_R5FSS0_CORE0_intr_238	WKUP_R5FSS0_CORE0	USB1 interrupt request	pulse
USB1	USB1_misc_level_0	MCU_R5FSS0_CORE0_cpu0_intr_238	MCU_R5FSS0_CORE0	USB1 interrupt request	pulse
USB1	USB1_misc_level_0	C7X256V0_CLEC_gic_spi_234	C7X256V0_CLEC	USB1 interrupt request	pulse
USB1	USB1_usb_wakeup_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_62	WKUP_R5FSS0_CORE0	USB1 interrupt request	level

Table 4-157. Hardware Requests for USB (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB1	USB1_usb_wakeup_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_10	WKUP_DEEPSLEEP_SOURCES0	USB1 interrupt request	level

4.10 Memory Interfaces

4.10.1 Flash Subsystem (FSS)

This section contains the integration details for the Flash Subsystem on this device. For further information, see the *Flash Subsystem (FSS)* section of the *Peripherals* chapter.

4.10.1.1 FSS Unsupported Features

For more information, see Section 4.10.2.1 , *OSPI Unsupported Features*.

4.10.1.2 FSS Integration

Table 4-158. FSS Module Allocations

Instance	MAIN	MCU	WKUP
FSS0	✓		

4.10.1.3 FSS_FSAS_0 Integration

Table 4-159. FSS_FSAS_0 Module Allocations

Instance	MAIN	MCU	WKUP
FSS0_FSAS_0	✓		

Table 4-160. Clock Integration for FSS_FSAS_0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
FSS0_FSAS_0	FICLK	MAIN_SYSCLK0		functional and interface clock

Table 4-161. Hardware Requests for FSS_FSAS_0

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0_FSAS_0	FSS0_FSAS_0_ecc_intr_err_pend_0	ESM0_esm_lvl_event_141	ESM0	FSS0_FSAS_0 interrupt request	level

4.10.2 Octal Serial Peripheral Interface (OSPI)

This section contains the integration details for the OSPI module on this device. For further information, see the *Octal Serial Peripheral Interface (OSPI)* section of the *Peripherals* chapter.

4.10.2.1 OSPI Unsupported Features

The following features are not supported on this family of devices:

- OSPI PDMA. Use CPU-triggered block DMA
- OSPI Clock Phase/Polarity modes 1,2,3
- Reset pins OSPI0_RESET_OUT2, OSPI0_RESET_OUT3

4.10.2.2 FSS_OSPI_0 Integration

Table 4-162. FSS_OSPI_0 Module Allocations

Instance	MAIN	MCU	WKUP
FSS0_OSPI_0	✓		

Table 4-163. Clock Integration for FSS_OSPI_0

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
FSS0_OSPI_0	HCLK	MAIN_SYSCLK0		data transfer clock
FSS0_OSPI_0	PCLK	MAIN_SYSCLK0		configuration clock
FSS0_OSPI_0	RFCLK	MAIN_PLL0_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL[0:0]=0	functional reference clock
FSS0_OSPI_0	RFCLK	MAIN_PLL1_HSDIV5_CLKOUT	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL[0:0]=1	functional reference clock

Table 4-164. Hardware Requests for FSS_OSPI_0

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0_OSPI_0	FSS0_OSPI_0_ospi_ecc_corr_lvl_intr_0	ESM0_esm_lvl_event_11	ESM0	FSS0_OSPI_0 interrupt request	level
FSS0_OSPI_0	FSS0_OSPI_0_ospi_ecc_uncorr_lvl_intr_0	ESM0_esm_lvl_event_74	ESM0	FSS0_OSPI_0 interrupt request	level
FSS0_OSPI_0	FSS0_OSPI_0_ospi_lvl_intr_0	GICSS0_spi_171	GICSS0	FSS0_OSPI_0 interrupt request	level
FSS0_OSPI_0	FSS0_OSPI_0_ospi_lvl_intr_0	WKUP_R5FSS0_CORE0_intr_171	WKUP_R5FSS0_CORE0	FSS0_OSPI_0 interrupt request	level
FSS0_OSPI_0	FSS0_OSPI_0_ospi_lvl_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_171	MCU_R5FSS0_CORE0	FSS0_OSPI_0 interrupt request	level

4.10.3 General-Purpose Memory Controller (GPMC)

This section contains the integration details for the GPMC module on this device. For further information, see the *General-Purpose Memory Controller (GPMC)* section of the *Peripherals* chapter.

4.10.3.1 GPMC Unsupported Features

The following features are not supported on this family of devices:

- Pins GPMC_CS[7:4]n are not pinned out
- Pins GPMC_A[27:23] are not pinned out
- Pins GPMC_AD[31:16] are not pinned out
- Pins GPMC_WAIT[3:2] are not pinned out
- Pins GPMC_BE[3:2]n are not pinned out

4.10.3.2 GPMC Integration

Table 4-165. GPMC Module Allocations

Instance	MAIN	MCU	WKUP
GPMC0	✓		

Table 4-166. Integration Attributes for GPMC

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
GPMC0	PSC0	GP_Core_CTL	LPSC_GPMC	15	OFF	YES	LPSC_main_IP

Table 4-167. Clock Integration for GPMC

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
GPMC0	FICLK	GPMC_FCLK		functional and interface clock
GPMC0	ICLK	MAIN_SYSCLK0/2		None

Table 4-168. Reset Integration for GPMC

Module Instance	Source	Description
GPMC0	PSC0	GPMC0 reset

Table 4-169. Hardware Requests for GPMC

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPMC0	GPMC0_gpmc_sdmareq_0	DMASS0_INTAGGR_0_intaggr_levi_pend_26	DMASS0_INTAGGR_0	GPMC0 interrupt request	level
GPMC0	GPMC0_gpmc_sinterrupt_0	GICSS0_spi_138	GICSS0	GPMC0 interrupt request	level
GPMC0	GPMC0_gpmc_sinterrupt_0	WKUP_R5FSS0_CORE0_intr_103	WKUP_R5FSS0_CORE0	GPMC0 interrupt request	level
GPMC0	GPMC0_gpmc_sinterrupt_0	MCU_R5FSS0_CORE0_cpu0_intr_103	MCU_R5FSS0_CORE0	GPMC0 interrupt request	level
GPMC0	GPMC0_gpmc_sinterrupt_0	C7X256V0_CLEC_gic_spi_106	C7X256V0_CLEC	GPMC0 interrupt request	level

4.10.3.3 GPMC Additional Integration Details

When using synchronous interface protocols, the GPMC_CLK output only toggles during the read or write access cycle. In some applications, it may be desirable to have a continuous clock running at the GPMC interface clock frequency for clocking attached devices. This option is enabled by an optional clock path from the GPMC functional clock input (fclk) to the GPMC_CLKOUT pin. This clock output (GPMC_FCLK) can be selected through the standard MUXMODE selection of the GPMC_CLKOUT pin PADCONFIG control register

Note that when using synchronous interface protocols with the continuous clock option described above, the programmer should ensure that the GPMC outputs are timed to the same frequency. (GPMC_CONFIG1_x GPMCFCLKDIVIDER = 0).

4.10.4 Error Location Module (ELM)

This section contains the integration details for the ELM module on this device. For further information, see the *Error Location Module (ELM)* section of the *Peripherals* chapter.

4.10.4.1 ELM Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.10.4.2 ELM Integration

Table 4-170. ELM Module Allocations

Instance	MAIN	MCU	WKUP
ELM0	✓		

Table 4-171. Integration Attributes for ELM

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ELM0	PSC0	GP_Core_CTL	LPSC_GPMC	15	OFF	YES	LPSC_main_IP

Table 4-172. Clock Integration for ELM

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
ELM0	FICLK	MAIN_SYSCLK0/4		functional and interface clock

Table 4-173. Reset Integration for ELM

Module Instance	Source	Description
ELM0	PSC0	ELM0 reset

Table 4-174. Hardware Requests for ELM

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ELM0	ELM0_elm_porocpsinterrupt_lvl_0	GICSS0_spi_164	GICSS0	ELM0 interrupt request	level
ELM0	ELM0_elm_porocpsinterrupt_lvl_0	WKUP_R5FSS0_CORE0_intr_164	WKUP_R5FSS0_CORE0	ELM0 interrupt request	level
ELM0	ELM0_elm_porocpsinterrupt_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_164	MCU_R5FSS0_CORE0	ELM0 interrupt request	level
ELM0	ELM0_elm_porocpsinterrupt_lvl_0	C7X256V0_CLEC_gic_spi_132	C7X256V0_CLEC	ELM0 interrupt request	level

4.10.5 Multimedia Card Secure Digital (MMCSD)

This section contains the integration details for the MMCSD module on this device. For further information, see the *Multimedia Card Secure Digital (MMCSD*) section of the *Peripherals* chapter.

4.10.5.1 MMCSD Unsupported Features

The following features are not supported on this family of devices:

- The following apply to 4-bit MMCSD instances:
  - SD Card busy LED: Not pinned out
  - High Speed DDR
- The following apply to 8-bit MMCSD instances:
  - SD Card busy LED - Not pinned out
  - SD/SDIO/MMC Cards (Removable) - no support for 4-pin/8-pin muxing
  - SD Card Detect Pin - Not pinned out
  - SD Card Write Protect Pin - Not pinned out
  - Enhanced Strobe

4.10.5.2 MMCSD Integration

Table 4-175. MMCSD Module Allocations

Instance	MAIN	MCU	WKUP
MMCSD0	✓		

Table 4-176. Integration Attributes for MMCSD

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MMCSD0	PSC0	GP_Core_CTL	LPSC_emmc_8b	20	OFF	YES	LPSC_main_IP

Table 4-177. Clock Integration for MMCSD

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MMCSD0	ICLK	MAIN_SYSCLK0/2		interface clock
MMCSD0	FCLK	MAIN_PLL0_HSDIV5_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL[0:0]=0	functional clock
MMCSD0	FCLK	MAIN_PLL2_HSDIV2_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL[0:0]=1	functional clock

Table 4-178. Reset Integration for MMCSD

Module Instance	Source	Description
MMCSD0	PSC0	MMCSD0 reset

Table 4-179. Hardware Requests for MMCSD

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD0	MMCSD0_emmcsdss_intr_0	GICSS0_spi_165	GICSS0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	WKUP_R5FSS0_CORE0_intr_161	WKUP_R5FSS0_CORE0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_161	MCU_R5FSS0_CORE0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	C7X256V0_CLEC_gic_spi_133	C7X256V0_CLEC	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_rxmem_corr_err_lvl_0	ESM0_esm_lvl_event_54	ESM0	MMCSD0 interrupt request	level

Table 4-179. Hardware Requests for MMCSD (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD0	MMCSD0_emmcsdss_rxmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_55	ESM0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_txmem_corr_err_lvl_0	ESM0_esm_lvl_event_56	ESM0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_txmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_57	ESM0	MMCSD0 interrupt request	level

4.10.5.3 MMCSD4 Integration

Table 4-180. MMCSD4 Module Allocations

Instance	MAIN	MCU	WKUP
MMCSD1	✓		
MMCSD2	✓		

Table 4-181. Integration Attributes for MMCSD4

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MMCSD1	PSC0	GP_Core_CTL	LPSC_emmc_4b_0	21	OFF	YES	LPSC_main_IP
MMCSD2	PSC0	GP_Core_CTL	LPSC_emmc_4b_1	22	OFF	YES	LPSC_main_IP

Table 4-182. Clock Integration for MMCSD4

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MMCSD1	ICLK	MAIN_SYSCLK0/2		interface clock
MMCSD1	FCLK	MAIN_PLL0_HSDIV5_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL[0:0]=0	functional clock
MMCSD1	FCLK	MAIN_PLL2_HSDIV2_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL[0:0]=1	functional clock
MMCSD2	ICLK	MAIN_SYSCLK0/2		interface clock
MMCSD2	FCLK	MAIN_PLL0_HSDIV5_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL[0:0]=0	functional clock
MMCSD2	FCLK	MAIN_PLL2_HSDIV2_CLKOUT	MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL[0:0]=1	functional clock

Table 4-183. Reset Integration for MMCSD4

Module Instance	Source	Description
MMCSD1	PSC0	MMCSD1 reset
MMCSD2	PSC0	MMCSD2 reset

Table 4-184. Hardware Requests for MMCSD4

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD1	MMCSD1_emmcsdss_intr_0	GICSS0_spi_115	GICSS0	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_intr_0	WKUP_R5FSS0_CORE0_intr_162	WKUP_R5FSS0_CORE0	MMCSD1 interrupt request	level

Table 4-184. Hardware Requests for MMCSD4 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD1	MMCSD1_emmcsdss_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_162	MCU_R5FSS0_CORE0	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_intr_0	C7X256V0_CLEC_gic_spi_83	C7X256V0_CLEC	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_rxmem_corr_err_lvl_0	ESM0_esm_lvl_event_58	ESM0	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_rxmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_59	ESM0	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_txmem_corr_err_lvl_0	ESM0_esm_lvl_event_60	ESM0	MMCSD1 interrupt request	level
MMCSD1	MMCSD1_emmcsdss_txmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_61	ESM0	MMCSD1 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_intr_0	GICSS0_spi_114	GICSS0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_intr_0	WKUP_R5FSS0_CORE0_intr_163	WKUP_R5FSS0_CORE0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_intr_0	MCU_R5FSS0_CORE0_cpu0_intr_163	MCU_R5FSS0_CORE0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_intr_0	C7X256V0_CLEC_gic_spi_82	C7X256V0_CLEC	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_rxmem_corr_err_lvl_0	ESM0_esm_lvl_event_34	ESM0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_rxmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_36	ESM0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_txmem_corr_err_lvl_0	ESM0_esm_lvl_event_49	ESM0	MMCSD2 interrupt request	level
MMCSD2	MMCSD2_emmcsdss_txmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_65	ESM0	MMCSD2 interrupt request	level

4.11 Industrial and Control Interfaces

4.11.1 Modular Controller Area Network (MCAN)

This section contains the integration details for the MCAN module on this device. For further information, see the *Modular Controller Area Network (MCAN)* section of the *Peripherals* chapter.

4.11.1.1 MCAN Unsupported Features

The following features are not supported on this family of devices:

- Debug DMAs: DMA Ack is not supported by PDMA architecture. Debug messages can be traced through the RX FIFO.
- TX DMA channels 3-31 are not supported by the Main domain instance/s. Only TX_DMA[2:0] have associated PDMA channels.
- DMA is not supported by the MCU domain instance/s

4.11.1.2 MCAN Integration

Table 4-185. MCAN Module Allocations

Instance	MAIN	MCU	WKUP
MCAN0	✓		
MCU_MCAN0		✓	
MCU_MCAN1		✓	

Table 4-186. Integration Attributes for MCAN

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCAN0	PSC0	GP_Core_CTL	LPSC_main_mcanss_0	35	OFF	YES	LPSC_main_IP
MCU_MCAN0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_mcanss_0	7	OFF	YES	LPSC_MCU_common
MCU_MCAN1	WKUP_PSC0	PD_MCUSS	LPSC_MCU_mcanss_1	8	OFF	YES	LPSC_MCU_common

Table 4-187. Clock Integration for MCAN

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCAN0	FCLK	MAIN_PLL0_HSDIV4_CLKOUT	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1:0]=0	functional clock
MCAN0	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1:0]=1	functional clock
MCAN0	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1:0]=2	functional clock
MCAN0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1:0]=3	functional clock
MCAN0	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1:0]=3	functional clock
MCAN0	ICLK	MAIN_SYSCLK0/4		interface clock
MCU_MCAN0	FCLK	MCU_PLL0_HSDIV4_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=0	functional clock

Table 4-187. Clock Integration for MCAN (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_MCAN0	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=1	functional clock
MCU_MCAN0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=2	functional clock
MCU_MCAN0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=2	functional clock
MCU_MCAN0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=3	functional clock
MCU_MCAN0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL[1:0]=3	functional clock
MCU_MCAN0	ICLK	MCU_SYSCLK0/2		interface clock
MCU_MCAN1	FCLK	MCU_PLL0_HSDIV4_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=0	functional clock
MCU_MCAN1	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=1	functional clock
MCU_MCAN1	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=2	functional clock
MCU_MCAN1	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=2	functional clock
MCU_MCAN1	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=3	functional clock
MCU_MCAN1	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL[1:0]=3	functional clock
MCU_MCAN1	ICLK	MCU_SYSCLK0/2		interface clock

Table 4-188. Reset Integration for MCAN

Module Instance	Source	Description
MCAN0	PSC0	MCAN0 reset
MCU_MCAN0	WKUP_PSC0	MCU_MCAN0 reset
MCU_MCAN1	WKUP_PSC0	MCU_MCAN1 reset

Table 4-189. Hardware Requests for MCAN

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN0	MCAN0_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_16	ESM0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_78	ESM0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	GICSS0_spi_186	GICSS0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_186	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level

Table 4-189. Hardware Requests for MCAN (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_186	MCU_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_154	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_fe_0	PDMA0_mcanss_main_0_fe_0	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_fe_1	PDMA0_mcanss_main_0_fe_1	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_fe_2	PDMA0_mcanss_main_0_fe_2	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_mcan_lvl_int_0	GICSS0_spi_187	GICSS0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_0	WKUP_R5FSS0_CORE0_intr_187	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_187	MCU_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_0	C7X256V0_CLEC_gic_spi_155	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_1	GICSS0_spi_188	GICSS0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_1	WKUP_R5FSS0_CORE0_intr_188	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_1	MCU_R5FSS0_CORE0_cpu0_intr_188	MCU_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_1	C7X256V0_CLEC_gic_spi_156	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_tx_dma_0	PDMA0_mcanss_main_0_tx_0	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_tx_dma_1	PDMA0_mcanss_main_0_tx_1	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_tx_dma_2	PDMA0_mcanss_main_0_tx_2	PDMA0	MCAN0 interrupt request	pulse
MCU_MCAN0	MCU_MCAN0_mcanss_ecc_corr_lvl_int_0	WKUP_ESM0_esm_lvl_event_16	WKUP_ESM0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_ecc_uncorr_lvl_int_0	WKUP_ESM0_esm_lvl_event_17	WKUP_ESM0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_198	WKUP_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_ext_ts_rollover_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_42	MCU_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_mcan_lvl_int_0	WKUP_R5FSS0_CORE0_intr_199	WKUP_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_mcan_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_43	MCU_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_mcan_lvl_int_1	WKUP_R5FSS0_CORE0_intr_200	WKUP_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN0	MCU_MCAN0_mcanss_mcan_lvl_int_1	MCU_R5FSS0_CORE0_cpu0_intr_44	MCU_R5FSS0_CORE0	MCU_MCAN0 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_ecc_corr_lvl_int_0	WKUP_ESM0_esm_lvl_event_18	WKUP_ESM0	MCU_MCAN1 interrupt request	level

Table 4-189. Hardware Requests for MCAN (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCAN1	MCU_MCAN1_mcanss_ecc_uncorr_lvl_int_0	WKUP_ESM0_esm_lvl_event_19	WKUP_ESM0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_239	WKUP_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_ext_ts_rollover_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_45	MCU_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_mcan_lvl_int_0	WKUP_R5FSS0_CORE0_intr_247	WKUP_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_mcan_lvl_int_0	MCU_R5FSS0_CORE0_cpu0_intr_46	MCU_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_mcan_lvl_int_1	WKUP_R5FSS0_CORE0_intr_248	WKUP_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level
MCU_MCAN1	MCU_MCAN1_mcanss_mcan_lvl_int_1	MCU_R5FSS0_CORE0_cpu0_intr_47	MCU_R5FSS0_CORE0	MCU_MCAN1 interrupt request	level

4.11.2 Enhanced Capture (ECAP)

This section contains the integration details for the ECAP module on this device. For further information, see the *Enhanced Capture (ECAP)* section of the *Peripherals* chapter.

4.11.2.1 ECAP Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.11.2.2 ECAP Integration

Table 4-190. ECAP Module Allocations

Instance	MAIN	MCU	WKUP
ECAP0	✓		
ECAP1	✓		
ECAP2	✓		

Table 4-191. Integration Attributes for ECAP

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ECAP0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
ECAP1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
ECAP2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO

Table 4-192. Clock Integration for ECAP

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
ECAP0	FICLK	MAIN_SYSCLK0/4		functional and interface clock
ECAP1	FICLK	MAIN_SYSCLK0/4		functional and interface clock
ECAP2	FICLK	MAIN_SYSCLK0/4		functional and interface clock

Table 4-193. Reset Integration for ECAP

Module Instance	Source	Description
ECAP0	PSC0	ECAP0 reset
ECAP1	PSC0	ECAP1 reset
ECAP2	PSC0	ECAP2 reset

Table 4-194. Hardware Requests for ECAP

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECAP0	ECAP0_ecap_int_0	GICSS0_spi_145	GICSS0	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	WKUP_R5FSS0_CORE0_intr_120	WKUP_R5FSS0_CORE0	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	MCU_R5FSS0_CORE0_cpu0_intr_83	MCU_R5FSS0_CORE0	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	C7X256V0_CLEC_gic_spi_113	C7X256V0_CLEC	ECAP0 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	GICSS0_spi_146	GICSS0	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	WKUP_R5FSS0_CORE0_intr_121	WKUP_R5FSS0_CORE0	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	MCU_R5FSS0_CORE0_cpu0_intr_84	MCU_R5FSS0_CORE0	ECAP1 interrupt request	pulse

Table 4-194. Hardware Requests for ECAP (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECAP1	ECAP1_ecap_int_0	C7X256V0_CLEC_gic_spi_114	C7X256V0_CLEC	ECAP1 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	GICSS0_spi_147	GICSS0	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	WKUP_R5FSS0_CORE0_intr_122	WKUP_R5FSS0_CORE0	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	MCU_R5FSS0_CORE0_cpu0_intr_85	MCU_R5FSS0_CORE0	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	C7X256V0_CLEC_gic_spi_115	C7X256V0_CLEC	ECAP2 interrupt request	pulse

4.11.3 Enhanced Pulse Width Modulation (EPWM)

This section contains the integration details for the EPWM module on this device. For further information, see the *Enhanced Pulse Width Modulation (EPWM)* section of the *Peripherals* chapter.

4.11.3.1 EPWM Unsupported Features

The following features are not supported on this family of devices:

- EPWM digital comparators
- High resolution extension (delay-line based)

4.11.3.2 EPWM Integration

Table 4-195. EPWM Module Allocations

Instance	MAIN	MCU	WKUP
EPWM0	✓		
EPWM1	✓		
EPWM2	✓		

Table 4-196. Integration Attributes for EPWM

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
EPWM0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
EPWM1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
EPWM2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO

Table 4-197. Clock Integration for EPWM

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
EPWM0	FICLK	MAIN_SYSCLK0/2		functional and interface clock
EPWM1	FICLK	MAIN_SYSCLK0/2		functional and interface clock
EPWM2	FICLK	MAIN_SYSCLK0/2		functional and interface clock

Table 4-198. Reset Integration for EPWM

Module Instance	Source	Description
EPWM0	PSC0	EPWM0 reset
EPWM1	PSC0	EPWM1 reset
EPWM2	PSC0	EPWM2 reset

Table 4-199. Hardware Requests for EPWM

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM0	EPWM0_epwm_etint_0	GICSS0_spi_229	GICSS0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_123	WKUP_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_etint_0	MCU_R5FSS0_CORE0_cpu0_intr_36	MCU_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_etint_0	C7X256V0_CLEC_gic_spi_197	C7X256V0_CLEC	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_synco_o_0	TIMESYNC_EVENT_ROUTER0_in_8	TIMESYNC_EVENT_ROUTER0	EPWM0 interrupt request	level

Table 4-199. Hardware Requests for EPWM (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM0	EPWM0_epwm_syncout_0	EPWM1_epwm_syncin_0	EPWM1	EPWM0 interrupt request	level
EPWM0	EPWM0_epwm_tripzint_0	GICSS0_spi_230	GICSS0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_124	WKUP_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	MCU_R5FSS0_CORE0_cpu0_intr_80	MCU_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_198	C7X256V0_CLEC	EPWM0 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	GICSS0_spi_231	GICSS0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_125	WKUP_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	MCU_R5FSS0_CORE0_cpu0_intr_37	MCU_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	C7X256V0_CLEC_gic_spi_199	C7X256V0_CLEC	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_syncout_0	EPWM2_epwm_syncin_0	EPWM2	EPWM1 interrupt request	level
EPWM1	EPWM1_epwm_tripzint_0	GICSS0_spi_233	GICSS0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_126	WKUP_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	MCU_R5FSS0_CORE0_cpu0_intr_81	MCU_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_201	C7X256V0_CLEC	EPWM1 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	GICSS0_spi_234	GICSS0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_127	WKUP_R5FSS0_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	MCU_R5FSS0_CORE0_cpu0_intr_38	MCU_R5FSS0_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	C7X256V0_CLEC_gic_spi_202	C7X256V0_CLEC	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	GICSS0_spi_235	GICSS0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_148	WKUP_R5FSS0_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	MCU_R5FSS0_CORE0_cpu0_intr_82	MCU_R5FSS0_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_203	C7X256V0_CLEC	EPWM2 interrupt request	pulse

4.11.4 Enhanced Quadrature Encoder Pulse (EQEP)

This section contains the integration details for the EQEP module on this device. For further information, see the *Enhanced Quadrature Encoder Pulse (EQEP)* section of the *Peripherals* chapter.

4.11.4.1 EQEP Unsupported Features

The following features are not supported on this family of devices:

- EQEPA_i[15:1], EQEPB_i[15:1] are not pinned out.

4.11.4.2 EQEP Integration

Table 4-200. EQEP Module Allocations

Instance	MAIN	MCU	WKUP
EQEP0	✓		
EQEP1	✓		
EQEP2	✓		

Table 4-201. Integration Attributes for EQEP

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
EQEP0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
EQEP1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
EQEP2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO

Table 4-202. Clock Integration for EQEP

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
EQEP0	FICLK	MAIN_SYSCLK0/4		functional and interface clock
EQEP1	FICLK	MAIN_SYSCLK0/4		functional and interface clock
EQEP2	FICLK	MAIN_SYSCLK0/4		functional and interface clock

Table 4-203. Reset Integration for EQEP

Module Instance	Source	Description
EQEP0	PSC0	EQEP0 reset
EQEP1	PSC0	EQEP1 reset
EQEP2	PSC0	EQEP2 reset

Table 4-204. Hardware Requests for EQEP

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EQEP0	EQEP0_eqep_int_0	GICSS0_spi_148	GICSS0	EQEP0 interrupt request	pulse
EQEP0	EQEP0_eqep_int_0	WKUP_R5FSS0_CORE0_intr_244	WKUP_R5FSS0_CORE0	EQEP0 interrupt request	pulse
EQEP0	EQEP0_eqep_int_0	MCU_R5FSS0_CORE0_cpu0_intr_86	MCU_R5FSS0_CORE0	EQEP0 interrupt request	pulse
EQEP0	EQEP0_eqep_int_0	C7X256V0_CLEC_gic_spi_116	C7X256V0_CLEC	EQEP0 interrupt request	pulse
EQEP1	EQEP1_eqep_int_0	GICSS0_spi_149	GICSS0	EQEP1 interrupt request	pulse
EQEP1	EQEP1_eqep_int_0	WKUP_R5FSS0_CORE0_intr_245	WKUP_R5FSS0_CORE0	EQEP1 interrupt request	pulse
EQEP1	EQEP1_eqep_int_0	MCU_R5FSS0_CORE0_cpu0_intr_87	MCU_R5FSS0_CORE0	EQEP1 interrupt request	pulse

Table 4-204. Hardware Requests for EQEP (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EQEP1	EQEP1_eqep_int_0	C7X256V0_CLEC_gic_spi_117	C7X256V0_CLEC	EQEP1 interrupt request	pulse
EQEP2	EQEP2_eqep_int_0	GICSS0_spi_150	GICSS0	EQEP2 interrupt request	pulse
EQEP2	EQEP2_eqep_int_0	WKUP_R5FSS0_CORE0_intr_246	WKUP_R5FSS0_CORE0	EQEP2 interrupt request	pulse
EQEP2	EQEP2_eqep_int_0	MCU_R5FSS0_CORE0_cpu0_intr_88	MCU_R5FSS0_CORE0	EQEP2 interrupt request	pulse
EQEP2	EQEP2_eqep_int_0	C7X256V0_CLEC_gic_spi_118	C7X256V0_CLEC	EQEP2 interrupt request	pulse

4.12 Camera Subsystem

4.12.1 MIPI D-PHY Receiver (DPHY_RX)

This section contains the integration details for the DPHY_RX module on this device. For further information, see the *MIPI D-PHY Receiver (DPHY_RX)* section of the *Peripherals* chapter.

4.12.1.1 DPHY_RX Unsupported Features

The following features are not supported on this family of devices:

- Swapping of clock and data lanes

4.12.1.2 dphy_rx Integration

Table 4-205. DPHY_RX Module Allocations

Instance	MAIN	MCU	WKUP
DPHY_RX0	✓		

Table 4-206. Integration Attributes for dphy_rx

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DPHY_RX0	PSC0	GP_Core_CTL	LPSC_DPHY_0	26	OFF	YES	LPSC_main_IP

Table 4-207. Clock Integration for dphy_rx

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DPHY_RX0	RXCLKN	CSI0_RXCLKN (PIN)		clock lane differential pair in
DPHY_RX0	RXCLKP	CSI0_RXCLKP (PIN)		clock lane differential pair in
DPHY_RX0	MAIN_CLK	MAIN_SYSCLK0/4		clock for lane module state machine and analog reference clock

Table 4-208. Reset Integration for dphy_rx

Module Instance	Source	Description
DPHY_RX0	PSC0	DPHY_RX0 reset

4.13 Timer Modules

4.13.1 Global Timebase Counter (GTC)

This section contains the integration details for the GTC module on this device. For further information, see the *Global Timebase Counter (GTC)* section of the *Peripherals* chapter.

4.13.1.1 GTC Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.13.1.2 GTC Integration

Table 4-209. GTC Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_GTC0			✓

Table 4-210. Clock Integration for GTC

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_GTC0	FCLK	MAIN_PLL2_HSDIV5_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=0	None
WKUP_GTC0	FCLK	MAIN_PLL0_HSDIV6_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=1	None
WKUP_GTC0	FCLK	CP_GEMAC_CPTS_REF_CLK	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=2	None
WKUP_GTC0	FCLK	MCU_EXT_REFCLK0	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=4	None
WKUP_GTC0	FCLK	EXT_REFCLK1	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=5	None
WKUP_GTC0	FCLK	MCU_SYSCLK0	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=6	None
WKUP_GTC0	FCLK	MAIN_SYSCLK0	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL[2:0]=7	None
WKUP_GTC0	ICLK	DM_CLK/4		None

Table 4-211. Hardware Requests for GTC

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_GTC0	WKUP_GTC0_gtc_push_event_0	TIMESYNC_EVENT_ROUTER0_in_11	TIMESYNC_EVENT_ROUTER0	WKUP_GTC0 interrupt request	pulse

4.13.2 Real Time Interrupt (RTI)

This section contains the integration details for the RTI module on this device. For further information, see the *Real Time Interrupt (RTI)* section of the *Peripherals* chapter.

4.13.2.1 RTI Not Supported Features

The following features are not supported on this family of devices:

- Analog watchdog timer
- External clock supervision
- Periodic interrupt
- Timestamp (Capture registers)

4.13.2.2 RTI_CFG1 Integration

Table 4-212. RTI_CFG1 Module Allocations

Instance	MAIN	MCU	WKUP
RTI4	✓		
RTI0	✓		
RTI1	✓		
RTI2	✓		
RTI3	✓		
MCU_RTI0		✓	
WKUP_RTI0			✓

Table 4-213. Integration Attributes for RTI_CFG1

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
RTI4	PSC0	PD_C7x	LPSC_C7x_core	55	OFF	YES	LPSC_C7x_common
RTI0	PSC0	PD_A53_0	LPSC_A53_0	46	OFF	YES	LPSC_A53_cluster_0
RTI1	PSC0	PD_A53_1	LPSC_A53_1	47	OFF	YES	LPSC_A53_cluster_0
RTI2	PSC0	PD_A53_2	LPSC_A53_2	48	OFF	YES	LPSC_A53_cluster_0
RTI3	PSC0	PD_A53_3	LPSC_A53_3	49	OFF	YES	LPSC_A53_cluster_0
MCU_RTI0	WKUP_PSC0	PD_MCUSS	LPSC_mcu_r5	6	OFF	YES	LPSC_MCU_common
WKUP_RTI0	PSC0	GP_Core_CTL	LPSC_main_dm	1	OFF	YES	LPSC_main_alwayson

Table 4-214. Clock Integration for RTI_CFG1

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
RTI4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=0	functional clock
RTI4	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=0	functional clock
RTI4	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
RTI4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI4	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI4	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
RTI4	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
RTI4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=2	functional clock
RTI4	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL[1:0]=3	functional clock
RTI4	ICLK	MAIN_SYSCLK0/4		interface clock
RTI0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=0	functional clock
RTI0	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=0	functional clock
RTI0	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
RTI0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI0	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
RTI0	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
RTI0	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
RTI0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=2	functional clock
RTI0	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1:0]=3	functional clock
RTI0	ICLK	MAIN_SYSCLK0/4		interface clock
RTI1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=0	functional clock
RTI1	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=0	functional clock
RTI1	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
RTI1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI1	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI1	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
RTI1	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
RTI1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=2	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
RTI1	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1:0]=3	functional clock
RTI1	ICLK	MAIN_SYSCLK0/4		interface clock
RTI2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=0	functional clock
RTI2	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=0	functional clock
RTI2	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
RTI2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI2	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI2	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
RTI2	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
RTI2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=2	functional clock
RTI2	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL[1:0]=3	functional clock
RTI2	ICLK	MAIN_SYSCLK0/4		interface clock
RTI3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=0	functional clock
RTI3	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=0	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
RTI3	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
RTI3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI3	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
RTI3	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
RTI3	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
RTI3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=2	functional clock
RTI3	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL[1:0]=3	functional clock
RTI3	ICLK	MAIN_SYSCLK0/4		interface clock
MCU_RTI0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=0	functional clock
MCU_RTI0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=0	functional clock
MCU_RTI0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
MCU_RTI0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_RTI0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_RTI0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
MCU_RTI0	FCLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
MCU_RTI0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=2	functional clock
MCU_RTI0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL[1:0]=3	functional clock
MCU_RTI0	ICLK	MCU_SYSCLK0/4		interface clock
WKUP_RTI0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=0	functional clock
WKUP_RTI0	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=0	functional clock
WKUP_RTI0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
WKUP_RTI0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
WKUP_RTI0	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
WKUP_RTI0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock

Table 4-214. Clock Integration for RTI_CFG1 (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_RTI0	FCLK	LFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
WKUP_RTI0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=2	functional clock
WKUP_RTI0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL[1:0]=3	functional clock
WKUP_RTI0	ICLK	DM_CLK/4		interface clock

Table 4-215. Reset Integration for RTI_CFG1

Module Instance	Source	Description
RTI4	PSC0	RTI4 reset
RTI0	PSC0	RTI0 reset
RTI1	PSC0	RTI1 reset
RTI2	PSC0	RTI2 reset
RTI3	PSC0	RTI3 reset
MCU_RTI0	WKUP_PSC0	MCU_RTI0 reset
WKUP_RTI0	PSC0	WKUP_RTI0 reset

Table 4-216. Hardware Requests for RTI_CFG1

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event0_204	ESM0	RTI4 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event1_204	ESM0	RTI4 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event2_204	ESM0	RTI4 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	C7X256V0_CLEC_soc_events_in_4	C7X256V0_CLEC	RTI4 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event0_192	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event1_192	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event2_192	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	GICSS0_spi_252	GICSS0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	C7X256V0_CLEC_gic_spi_220	C7X256V0_CLEC	RTI0 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event0_193	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event1_193	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event2_193	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	GICSS0_spi_253	GICSS0	RTI1 interrupt request	pulse

Table 4-216. Hardware Requests for RTI_CFG1 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
RTI1	RTI1_intr_wwd_0	C7X256V0_CLEC_gic_spi_221	C7X256V0_CLEC	RTI1 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event0_209	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event1_209	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event2_209	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	GICSS0_spi_254	GICSS0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	C7X256V0_CLEC_gic_spi_222	C7X256V0_CLEC	RTI2 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event0_210	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event1_210	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event2_210	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	GICSS0_spi_255	GICSS0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	C7X256V0_CLEC_gic_spi_223	C7X256V0_CLEC	RTI3 interrupt request	pulse
MCU_RTI0	MCU_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event0_85	WKUP_ESM0	MCU_RTI0 interrupt request	pulse
MCU_RTI0	MCU_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event1_85	WKUP_ESM0	MCU_RTI0 interrupt request	pulse
MCU_RTI0	MCU_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event2_85	WKUP_ESM0	MCU_RTI0 interrupt request	pulse
MCU_RTI0	MCU_RTI0_intr_wwd_0	MCU_R5FSS0_CORE0_cpu0_intr_30	MCU_R5FSS0_CORE0	MCU_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event0_195	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event1_195	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event2_195	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	WKUP_R5FSS0_CORE0_intr_30	WKUP_R5FSS0_CORE0	WKUP_RTI0 interrupt request	pulse

4.13.3 Real-Time Clock (RTC)

This section contains the integration details for the RTC module on this device. For further information, see the *Real-Time Clock (RTC)* section of the *Peripherals* chapter.

4.13.3.1 RTC Unsupported Features

The following features are not supported on this family of devices:

- PMIC enable support
- Analog IP support
- External IO
- Two digital voltage domains

4.13.3.2 rtcss Integration

Table 4-217. RTCSS Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_rtcss0			✓

Table 4-218. Integration Attributes for rtcss

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_rtcss0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-219. Clock Integration for rtcss

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_rtcss0	ANA_OSC32K	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=0 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	None
WKUP_rtcss0	ANA_OSC32K	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=0 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	None
WKUP_rtcss0	ANA_OSC32K	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=0 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	None
WKUP_rtcss0	ANA_OSC32K	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=0 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	None
WKUP_rtcss0	ANA_OSC32K	LFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=0 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	None
WKUP_rtcss0	ANA_OSC32K	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL[0:0]=1	None

Table 4-219. Clock Integration for rtcss (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_rtcss0	ICLK	DM_CLK/8		None

Table 4-220. Reset Integration for rtcss

Module Instance	Source	Description
WKUP_rtcss0	PSC0	WKUP_rtcss0 reset

Table 4-221. Hardware Requests for rtcss

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	GICSS0_spi_132	GICSS0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	WKUP_R5FSS0_CORE0_intr_97	WKUP_R5FSS0_CORE0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_97	MCU_R5FSS0_CORE0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	WKUP_DEEPSLEEP_SOURCES0_Isam62_dm_wakeup_deepsleep_sources_7	WKUP_DEEPSLEEP_SOURCES0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	C7X256V0_CLEC_gic_spi_100	C7X256V0_CLEC	WKUP_rtcss0 interrupt request	level

4.13.4 Timer

This section contains the integration details for the Timer module on this device. For further information, see the *Timer* section of the *Peripherals* chapter.

4.13.4.1 Timer Unsupported Features

The following features are not supported on this family of devices:

- Cascading of timer instances

4.13.4.2 TIMER Integration

Table 4-222. TIMER Module Allocations

Instance	MAIN	MCU	WKUP
TIMER0	✓		
TIMER1	✓		
TIMER2	✓		
TIMER3	✓		
TIMER4	✓		
TIMER5	✓		
TIMER6	✓		
TIMER7	✓		
MCU_TIMER0		✓	
MCU_TIMER1		✓	
MCU_TIMER2		✓	
MCU_TIMER3		✓	
WKUP_TIMER0			✓
WKUP_TIMER1			✓

Table 4-223. Integration Attributes for TIMER

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
TIMER0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER1	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER2	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER3	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER4	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER5	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER6	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
TIMER7	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCU_TIMER0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
MCU_TIMER1	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
MCU_TIMER2	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO

Table 4-223. Integration Attributes for TIMER (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCU_TIMER3	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO
WKUP_TIMER0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
WKUP_TIMER1	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	

Table 4-224. Clock Integration for TIMER

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER0	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=0	functional clock
TIMER0	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=0	functional clock
TIMER0	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER0	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER0	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER0	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER0	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=10	functional clock
TIMER0	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=11	functional clock
TIMER0	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=12	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER0	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=2	functional clock
TIMER0	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=3	functional clock
TIMER0	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=4	functional clock
TIMER0	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=5	functional clock
TIMER0	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=7	functional clock
TIMER0	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=8	functional clock
TIMER0	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3:0]=9	functional clock
TIMER1	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=0	functional clock
TIMER1	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=0	functional clock
TIMER1	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER1	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER1	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER1	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER1	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=10	functional clock
TIMER1	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=11	functional clock
TIMER1	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=12	functional clock
TIMER1	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=2	functional clock
TIMER1	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=3	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER1	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=4	functional clock
TIMER1	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=5	functional clock
TIMER1	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=7	functional clock
TIMER1	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=8	functional clock
TIMER1	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3:0]=9	functional clock
TIMER1	FCLK	TIMER0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL[8:8]=1	functional clock
TIMER2	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=0	functional clock
TIMER2	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=0	functional clock
TIMER2	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER2	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER2	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER2	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER2	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=10	functional clock
TIMER2	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=11	functional clock
TIMER2	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=12	functional clock
TIMER2	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=2	functional clock
TIMER2	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=3	functional clock
TIMER2	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=4	functional clock
TIMER2	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=5	functional clock
TIMER2	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=7	functional clock
TIMER2	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=8	functional clock
TIMER2	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3:0]=9	functional clock
TIMER3	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=0	functional clock
TIMER3	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER3	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER3	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER3	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER3	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER3	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=10	functional clock
TIMER3	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=11	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER3	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=12	functional clock
TIMER3	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=2	functional clock
TIMER3	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=3	functional clock
TIMER3	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=4	functional clock
TIMER3	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=5	functional clock
TIMER3	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=7	functional clock
TIMER3	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=8	functional clock
TIMER3	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3:0]=9	functional clock
TIMER3	FCLK	TIMER2 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL[8:8]=1	functional clock
TIMER4	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=0	functional clock
TIMER4	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER4	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER4	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER4	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER4	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER4	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=10	functional clock
TIMER4	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=11	functional clock
TIMER4	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=12	functional clock
TIMER4	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=2	functional clock
TIMER4	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=3	functional clock
TIMER4	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=4	functional clock
TIMER4	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=5	functional clock
TIMER4	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=7	functional clock
TIMER4	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=8	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER4	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3:0]=9	functional clock
TIMER5	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER5	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=0	functional clock
TIMER5	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=0	functional clock
TIMER5	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER5	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER5	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER5	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER5	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER5	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=10	functional clock
TIMER5	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=11	functional clock
TIMER5	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=12	functional clock
TIMER5	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=2	functional clock
TIMER5	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=3	functional clock
TIMER5	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=4	functional clock
TIMER5	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=5	functional clock
TIMER5	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=7	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER5	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=8	functional clock
TIMER5	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3:0]=9	functional clock
TIMER5	FCLK	TIMER4 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL[8:8]=1	functional clock
TIMER6	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER6	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=0	functional clock
TIMER6	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=0	functional clock
TIMER6	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER6	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER6	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER6	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER6	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER6	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=10	functional clock
TIMER6	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=11	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER6	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=12	functional clock
TIMER6	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=2	functional clock
TIMER6	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=3	functional clock
TIMER6	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=4	functional clock
TIMER6	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=5	functional clock
TIMER6	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=7	functional clock
TIMER6	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=8	functional clock
TIMER6	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3:0]=9	functional clock
TIMER7	ICLK	MAIN_SYSCLK0/4		interface clock
TIMER7	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=0	functional clock
TIMER7	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=0	functional clock
TIMER7	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
TIMER7	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER7	FCLK	HFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
TIMER7	FCLK	CLK_32K_RC	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
TIMER7	FCLK	LFOSC0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
TIMER7	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=10	functional clock
TIMER7	FCLK	CPSW0 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=11	functional clock
TIMER7	FCLK	MAIN_PLL5_HSDIV1_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=12	functional clock
TIMER7	FCLK	MAIN_PLL0_HSDIV7_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=2	functional clock
TIMER7	FCLK	CLK_12M_RC	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=3	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
TIMER7	FCLK	MCU_EXT_REFCLK0	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=4	functional clock
TIMER7	FCLK	EXT_REFCLK1	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=5	functional clock
TIMER7	FCLK	CP_GEMAC_CPTS_REF_CLK	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=7	functional clock
TIMER7	FCLK	MAIN_PLL1_HSDIV3_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=8	functional clock
TIMER7	FCLK	MAIN_PLL2_HSDIV6_CLKOUT	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=0 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3:0]=9	functional clock
TIMER7	FCLK	TIMER6 (INSTANCE)	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL[8:8]=1	functional clock
MCU_TIMER0	ICLK	MCU_SYSCLK0/4		interface clock
MCU_TIMER0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=0	functional clock
MCU_TIMER0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=0	functional clock
MCU_TIMER0	FCLK	MCU_SYSCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=1	functional clock
MCU_TIMER0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=2	functional clock
MCU_TIMER0	FCLK	MCU_PLL0_HSDIV5_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=3	functional clock
MCU_TIMER0	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=4	functional clock
MCU_TIMER0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_TIMER0	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER0	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
MCU_TIMER0	FCLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
MCU_TIMER0	FCLK	CPSW0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=6	functional clock
MCU_TIMER0	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL[2:0]=7	functional clock
MCU_TIMER1	ICLK	MCU_SYSCLK0/4		interface clock
MCU_TIMER1	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=0	functional clock
MCU_TIMER1	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=0	functional clock
MCU_TIMER1	FCLK	MCU_SYSCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=1	functional clock
MCU_TIMER1	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=2	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_TIMER1	FCLK	MCU_PLL0_HSDIV5_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=3	functional clock
MCU_TIMER1	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=4	functional clock
MCU_TIMER1	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
MCU_TIMER1	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER1	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER1	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
MCU_TIMER1	FCLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_TIMER1	FCLK	CPSW0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=6	functional clock
MCU_TIMER1	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL[2:0]=7	functional clock
MCU_TIMER1	FCLK	MCU_TIMER0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL[8:8]=1	functional clock
MCU_TIMER2	ICLK	MCU_SYSCLK0/4		interface clock
MCU_TIMER2	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=0	functional clock
MCU_TIMER2	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=0	functional clock
MCU_TIMER2	FCLK	MCU_SYSCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=1	functional clock
MCU_TIMER2	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=2	functional clock
MCU_TIMER2	FCLK	MCU_PLL0_HSDIV5_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=3	functional clock
MCU_TIMER2	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=4	functional clock
MCU_TIMER2	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
MCU_TIMER2	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER2	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER2	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_TIMER2	FCLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
MCU_TIMER2	FCLK	CPSW0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=6	functional clock
MCU_TIMER2	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL[2:0]=7	functional clock
MCU_TIMER3	ICLK	MCU_SYSCLK0/4		interface clock
MCU_TIMER3	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=0	functional clock
MCU_TIMER3	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=0	functional clock
MCU_TIMER3	FCLK	MCU_SYSCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=1	functional clock
MCU_TIMER3	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=2	functional clock
MCU_TIMER3	FCLK	MCU_PLL0_HSDIV5_CLKOUT	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=3	functional clock
MCU_TIMER3	FCLK	MCU_EXT_REFCLK0	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=4	functional clock
MCU_TIMER3	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_TIMER3	FCLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER3	FCLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
MCU_TIMER3	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
MCU_TIMER3	FCLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
MCU_TIMER3	FCLK	CPSW0 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=6	functional clock
MCU_TIMER3	FCLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=0 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL[2:0]=7	functional clock
MCU_TIMER3	FCLK	MCU_TIMER2 (INSTANCE)	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL[8:8]=1	functional clock
WKUP_TIMER0	ICLK	DM_CLK/2		interface clock
WKUP_TIMER0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=0	functional clock
WKUP_TIMER0	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_TIMER0	FCLK	DM_CLK	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=1	functional clock
WKUP_TIMER0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=2	functional clock
WKUP_TIMER0	FCLK	MCU_PLL0_HSDIV5_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=3	functional clock
WKUP_TIMER0	FCLK	MCU_EXT_REFCLK0	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=4	functional clock
WKUP_TIMER0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
WKUP_TIMER0	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
WKUP_TIMER0	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
WKUP_TIMER0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
WKUP_TIMER0	FCLK	LFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
WKUP_TIMER0	FCLK	CPSW0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=6	functional clock
WKUP_TIMER0	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL[2:0]=7	functional clock
WKUP_TIMER1	ICLK	DM_CLK/2		interface clock
WKUP_TIMER1	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=0	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_TIMER1	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=0	functional clock
WKUP_TIMER1	FCLK	DM_CLK	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=1	functional clock
WKUP_TIMER1	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=2	functional clock
WKUP_TIMER1	FCLK	MCU_PLL0_HSDIV5_CLKOUT	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=3	functional clock
WKUP_TIMER1	FCLK	MCU_EXT_REFCLK0	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=4	functional clock
WKUP_TIMER1	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	functional clock
WKUP_TIMER1	FCLK	CLK_12M_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock
WKUP_TIMER1	FCLK	HFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	functional clock

Table 4-224. Clock Integration for TIMER (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_TIMER1	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	functional clock
WKUP_TIMER1	FCLK	LFOSC0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=5 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	functional clock
WKUP_TIMER1	FCLK	CPSW0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=6	functional clock
WKUP_TIMER1	FCLK	CLK_32K_RC	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=0 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL[2:0]=7	functional clock
WKUP_TIMER1	FCLK	WKUP_TIMER0 (INSTANCE)	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL[8:8]=1	functional clock

Table 4-225. Reset Integration for TIMER

Module Instance	Source	Description
TIMER0	PSC0	TIMER0 reset
TIMER1	PSC0	TIMER1 reset
TIMER2	PSC0	TIMER2 reset
TIMER3	PSC0	TIMER3 reset
TIMER4	PSC0	TIMER4 reset
TIMER5	PSC0	TIMER5 reset
TIMER6	PSC0	TIMER6 reset
TIMER7	PSC0	TIMER7 reset
MCU_TIMER0	WKUP_PSC0	MCU_TIMER0 reset
MCU_TIMER1	WKUP_PSC0	MCU_TIMER1 reset
MCU_TIMER2	WKUP_PSC0	MCU_TIMER2 reset
MCU_TIMER3	WKUP_PSC0	MCU_TIMER3 reset
WKUP_TIMER0	PSC0	WKUP_TIMER0 reset
WKUP_TIMER1	PSC0	WKUP_TIMER1 reset

Table 4-226. Hardware Requests for TIMER

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER0	TIMER0_intr_pend_0	GICSS0_spi_152	GICSS0	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	C7X256V0_CLEC_gic_spi_120	C7X256V0_CLEC	TIMER0 interrupt request	level
TIMER0	TIMER0_timer_pwm_0	TIMESYNC_EVENT_ROUTER0_in_0	TIMESYNC_EVENT_ROUTER0	TIMER0 interrupt request	pulse
TIMER1	TIMER1_intr_pend_0	GICSS0_spi_153	GICSS0	TIMER1 interrupt request	level
TIMER1	TIMER1_intr_pend_0	C7X256V0_CLEC_gic_spi_121	C7X256V0_CLEC	TIMER1 interrupt request	level
TIMER1	TIMER1_timer_pwm_0	TIMESYNC_EVENT_ROUTER0_in_1	TIMESYNC_EVENT_ROUTER0	TIMER1 interrupt request	pulse
TIMER2	TIMER2_intr_pend_0	GICSS0_spi_154	GICSS0	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	C7X256V0_CLEC_gic_spi_122	C7X256V0_CLEC	TIMER2 interrupt request	level
TIMER2	TIMER2_timer_pwm_0	TIMESYNC_EVENT_ROUTER0_in_2	TIMESYNC_EVENT_ROUTER0	TIMER2 interrupt request	pulse
TIMER3	TIMER3_intr_pend_0	GICSS0_spi_155	GICSS0	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	C7X256V0_CLEC_gic_spi_123	C7X256V0_CLEC	TIMER3 interrupt request	level
TIMER3	TIMER3_timer_pwm_0	TIMESYNC_EVENT_ROUTER0_in_3	TIMESYNC_EVENT_ROUTER0	TIMER3 interrupt request	pulse
TIMER4	TIMER4_intr_pend_0	GICSS0_spi_156	GICSS0	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	C7X256V0_CLEC_gic_spi_124	C7X256V0_CLEC	TIMER4 interrupt request	level
TIMER5	TIMER5_intr_pend_0	GICSS0_spi_157	GICSS0	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	C7X256V0_CLEC_gic_spi_125	C7X256V0_CLEC	TIMER5 interrupt request	level
TIMER6	TIMER6_intr_pend_0	GICSS0_spi_158	GICSS0	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	C7X256V0_CLEC_gic_spi_126	C7X256V0_CLEC	TIMER6 interrupt request	level
TIMER7	TIMER7_intr_pend_0	GICSS0_spi_159	GICSS0	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	C7X256V0_CLEC_gic_spi_127	C7X256V0_CLEC	TIMER7 interrupt request	level
MCU_TIMER0	MCU_TIMER0_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_28	MCU_R5FSS0_CORE0	MCU_TIMER0 interrupt request	level
MCU_TIMER1	MCU_TIMER1_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_29	MCU_R5FSS0_CORE0	MCU_TIMER1 interrupt request	level
MCU_TIMER2	MCU_TIMER2_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_138	MCU_R5FSS0_CORE0	MCU_TIMER2 interrupt request	level
MCU_TIMER3	MCU_TIMER3_intr_pend_0	MCU_R5FSS0_CORE0_cpu0_intr_139	MCU_R5FSS0_CORE0	MCU_TIMER3 interrupt request	level
WKUP_TIMER0	WKUP_TIMER0_intr_pend_0	WKUP_R5FSS0_CORE0_intr_138	WKUP_R5FSS0_CORE0	WKUP_TIMER0 interrupt request	level
WKUP_TIMER0	WKUP_TIMER0_timer_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_28	WKUP_R5FSS0_CORE0	WKUP_TIMER0 interrupt request	level
WKUP_TIMER0	WKUP_TIMER0_timer_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_5	WKUP_DEEPSLEEP_SOURCES0	WKUP_TIMER0 interrupt request	level
WKUP_TIMER1	WKUP_TIMER1_intr_pend_0	WKUP_R5FSS0_CORE0_intr_139	WKUP_R5FSS0_CORE0	WKUP_TIMER1 interrupt request	level

Table 4-226. Hardware Requests for TIMER (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_TIMER1	WKUP_TIMER1_timer_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_29	WKUP_R5FSS0_CORE0	WKUP_TIMER1 interrupt request	level
WKUP_TIMER1	WKUP_TIMER1_timer_clkstop_wakeup_0	WKUP_DEEPSLEEP_SOURCES0_lsam62_dm_wakeup_deepsleep_sources_6	WKUP_DEEPSLEEP_SOURCES0	WKUP_TIMER1 interrupt request	level

4.14 Internal Diagnostic Modules

4.14.1 Dual Clock Comparator (DCC)

This section contains the integration details for the DCC module on this device. For further information, see the *Dual Clock Comparator (DCC)* section of the *Peripherals* chapter.

4.14.1.1 DCC Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.14.1.2 DCC Integration

Table 4-227. DCC Module Allocations

Instance	MAIN	MCU	WKUP
DCC0	✓		
DCC1	✓		
DCC2	✓		
DCC3	✓		
DCC4	✓		
DCC5	✓		
DCC6	✓		
MCU_DCC0		✓	
MCU_DCC1		✓	

Table 4-228. Integration Attributes for DCC

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DCC0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC1	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC2	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC3	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC4	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC5	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
DCC6	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
MCU_DCC0	WKUP_PSC0	GP_core_CTL_MCU	LPSC_mcu_alwayson	0	ON	NO	
MCU_DCC1	WKUP_PSC0	GP_core_CTL_MCU	LPSC_mcu_alwayson	0	ON	NO	

Table 4-229. Clock Integration for DCC

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DCC0	DCC_CLKSRC0_CLK	MAIN_PLL0_HSDIV1_CLKOUT		counter1 clock source
DCC0	DCC_CLKSRC1_CLK	MAIN_PLL0_HSDIV2_CLKOUT		counter1 clock source

Table 4-229. Clock Integration for DCC (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DCC0	DCC_CLKSRC2_CLK	MAIN_PLL0_HSDIV3_CLKOUT		counter1 clock source
DCC0	DCC_CLKSRC3_CLK	MAIN_PLL0_HSDIV4_CLKOUT		counter1 clock source
DCC0	DCC_CLKSRC4_CLK	CLK_12M_RC		counter1 clock source
DCC0	DCC_CLKSRC4_CLK	HFOSC0 (INSTANCE)		counter1 clock source
DCC0	DCC_CLKSRC5_CLK	EXT_REFCLK1		counter1 clock source
DCC0	DCC_CLKSRC6_CLK	MAIN_SYSCLK0		counter1 clock source
DCC0	DCC_CLKSRC7_CLK	MAIN_PLL2_HSDIV8_CLKOUT		counter1 clock source
DCC0	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC0	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC0	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC0	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC0	DCC_INPUT10_CLK	MAIN_SYSCLK0/2		secondary oscillator clock
DCC0	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC1	DCC_CLKSRC0_CLK	MAIN_PLL0_HSDIV5_CLKOUT		counter1 clock source
DCC1	DCC_CLKSRC1_CLK	MAIN_PLL0_HSDIV6_CLKOUT		counter1 clock source
DCC1	DCC_CLKSRC2_CLK	MAIN_PLL0_HSDIV7_CLKOUT		counter1 clock source
DCC1	DCC_CLKSRC3_CLK	MAIN_PLL1_HSDIV1_CLKOUT		counter1 clock source
DCC1	DCC_CLKSRC4_CLK	MAIN_PLL15_HSDIV2_CLKOUT/4		counter1 clock source
DCC1	DCC_CLKSRC5_CLK	MAIN_PLL1_HSDIV0_CLKOUT		counter1 clock source
DCC1	DCC_CLKSRC6_CLK	CLK_12M_RC		counter1 clock source
DCC1	DCC_CLKSRC7_CLK	MAIN_PLL1_HSDIV2_CLKOUT		counter1 clock source
DCC1	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC1	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC1	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC1	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC1	DCC_INPUT10_CLK	MAIN_SYSCLK0/4		secondary oscillator clock
DCC1	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC2	DCC_CLKSRC0_CLK	MAIN_PLL1_HSDIV3_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC1_CLK	MAIN_PLL15_HSDIV0_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC2_CLK	MAIN_PLL1_HSDIV5_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC3_CLK	MAIN_PLL1_HSDIV6_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC4_CLK	MAIN_PLL5_HSDIV1_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC5_CLK	MAIN_PLL15_HSDIV1_CLKOUT		counter1 clock source

Table 4-229. Clock Integration for DCC (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DCC2	DCC_CLKSRC6_CLK	MAIN_PLL2_HSDIV2_CLKOUT		counter1 clock source
DCC2	DCC_CLKSRC7_CLK	RMII2_REF_CLK (PIN)		counter1 clock source
DCC2	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC2	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC2	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC2	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC2	DCC_INPUT10_CLK	MAIN_SYSCLK0/4		secondary oscillator clock
DCC2	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC3	DCC_CLKSRC0_CLK	MAIN_PLL1_HSDIV0_CLKOUT		counter1 clock source
DCC3	DCC_CLKSRC1_CLK	MAIN_PLL2_HSDIV5_CLKOUT		counter1 clock source
DCC3	DCC_CLKSRC2_CLK	C7X256V0_CLK (INSTANCE)		counter1 clock source
DCC3	DCC_CLKSRC3_CLK	MAIN_PLL2_HSDIV7_CLKOUT		counter1 clock source
DCC3	DCC_CLKSRC4_CLK	MAIN_PLL2_HSDIV6_CLKOUT		counter1 clock source
DCC3	DCC_CLKSRC5_CLK	MAIN_PLL2_HSDIV9_CLKOUT		counter1 clock source
DCC3	DCC_CLKSRC6_CLK	A53SS0 (INSTANCE)/4		counter1 clock source
DCC3	DCC_CLKSRC7_CLK	DDR32SS0 (INSTANCE)		counter1 clock source
DCC3	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC3	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC3	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC3	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC3	DCC_INPUT10_CLK	MAIN_SYSCLK0/4		secondary oscillator clock
DCC3	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC4	DCC_CLKSRC1_CLK	CP_GEMAC_CPTS_REF_CLK		counter1 clock source
DCC4	DCC_CLKSRC2_CLK	AUDIO_EXT_REFCLK1 (PIN)		counter1 clock source
DCC4	DCC_CLKSRC3_CLK	DPHY_RX0 (INSTANCE)		counter1 clock source
DCC4	DCC_CLKSRC4_CLK	MCU_EXT_REFCLK0		counter1 clock source
DCC4	DCC_CLKSRC5_CLK	RMII1_REF_CLK (PIN)/4		counter1 clock source
DCC4	DCC_CLKSRC7_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	counter1 clock source
DCC4	DCC_CLKSRC7_CLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source
DCC4	DCC_CLKSRC7_CLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source

Table 4-229. Clock Integration for DCC (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DCC4	DCC_CLKSRC7_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	counter1 clock source
DCC4	DCC_CLKSRC7_CLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	counter1 clock source
DCC4	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC4	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC4	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC4	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC4	DCC_INPUT10_CLK	MAIN_SYSCLK0/2		secondary oscillator clock
DCC4	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC5	DCC_CLKSRC0_CLK	MAIN_PLL0_HSDIV8_CLKOUT		counter1 clock source
DCC5	DCC_CLKSRC2_CLK	MAIN_PLL2_HSDIV1_CLKOUT		counter1 clock source
DCC5	DCC_CLKSRC3_CLK	MAIN_PLL2_HSDIV3_CLKOUT		counter1 clock source
DCC5	DCC_CLKSRC4_CLK	MAIN_PLL2_HSDIV4_CLKOUT		counter1 clock source
DCC5	DCC_CLKSRC5_CLK	MAIN_PLL5_HSDIV0_CLKOUT		counter1 clock source
DCC5	DCC_CLKSRC6_CLK	MAIN_PLL17_HSDIV0_CLKOUT		counter1 clock source
DCC5	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC5	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC5	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC5	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
DCC5	DCC_INPUT10_CLK	MAIN_SYSCLK0		secondary oscillator clock
DCC5	FICLK	MAIN_SYSCLK0/4		functional and interface clock
DCC6	DCC_CLKSRC0_CLK	VOUT0_EXTPCLKIN (PIN)		counter1 clock source
DCC6	DCC_CLKSRC1_CLK	MCASP0_ACLKX (PIN)		counter1 clock source
DCC6	DCC_CLKSRC2_CLK	MCASP0_ACLKR (PIN)		counter1 clock source
DCC6	DCC_CLKSRC3_CLK	MCASP1_ACLKX (PIN)		counter1 clock source
DCC6	DCC_CLKSRC4_CLK	MCASP1_ACLKR (PIN)		counter1 clock source
DCC6	DCC_CLKSRC5_CLK	MCASP2_ACLKX (PIN)		counter1 clock source
DCC6	DCC_CLKSRC6_CLK	MCASP2_ACLKR (PIN)		counter1 clock source
DCC6	DCC_CLKSRC7_CLK	AUDIO_EXT_REFCLK0 (PIN)		counter1 clock source
DCC6	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
DCC6	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
DCC6	DCC_INPUT01_CLK	EXT_REFCLK1		primary oscillator clock
DCC6	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock

Table 4-229. Clock Integration for DCC (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
DCC6	DCC_INPUT10_CLK	MAIN_SYSCLK0		secondary oscillator clock
DCC6	FICLK	MAIN_SYSCLK0/4		functional and interface clock
MCU_DCC0	DCC_CLKSRC0_CLK	MCU_PLL0_HSDIV0_CLKOUT		counter1 clock source
MCU_DCC0	DCC_CLKSRC1_CLK	MCU_PLL0_HSDIV1_CLKOUT		counter1 clock source
MCU_DCC0	DCC_CLKSRC2_CLK	MCU_PLL0_HSDIV2_CLKOUT		counter1 clock source
MCU_DCC0	DCC_CLKSRC3_CLK	MCU_PLL0_HSDIV3_CLKOUT/4		counter1 clock source
MCU_DCC0	DCC_CLKSRC4_CLK	MCU_PLL0_HSDIV4_CLKOUT		counter1 clock source
MCU_DCC0	DCC_CLKSRC5_CLK	CLK_32K_RC		counter1 clock source
MCU_DCC0	DCC_CLKSRC6_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	counter1 clock source
MCU_DCC0	DCC_CLKSRC6_CLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source
MCU_DCC0	DCC_CLKSRC6_CLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source
MCU_DCC0	DCC_CLKSRC6_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	counter1 clock source
MCU_DCC0	DCC_CLKSRC6_CLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	counter1 clock source
MCU_DCC0	DCC_CLKSRC7_CLK	MCU_EXT_REFCLK0		counter1 clock source
MCU_DCC0	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
MCU_DCC0	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
MCU_DCC0	DCC_INPUT01_CLK	CLK_32K_RC		primary oscillator clock
MCU_DCC0	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
MCU_DCC0	DCC_INPUT10_CLK	MCU_SYSCLK0/2		secondary oscillator clock
MCU_DCC0	FICLK	MCU_SYSCLK0/4		functional and interface clock
MCU_DCC1	DCC_CLKSRC0_CLK	MCU_PLL0_HSDIV5_CLKOUT		counter1 clock source
MCU_DCC1	DCC_CLKSRC1_CLK	MCU_PLL0_HSDIV6_CLKOUT		counter1 clock source
MCU_DCC1	DCC_CLKSRC5_CLK	CLK_32K_RC		counter1 clock source
MCU_DCC1	DCC_CLKSRC6_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=0	counter1 clock source
MCU_DCC1	DCC_CLKSRC6_CLK	CLK_12M_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source
MCU_DCC1	DCC_CLKSRC6_CLK	HFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=1	counter1 clock source
MCU_DCC1	DCC_CLKSRC6_CLK	CLK_32K_RC	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=2	counter1 clock source

Table 4-229. Clock Integration for DCC (continued)

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_DCC1	DCC_CLKSRC6_CLK	LFOSC0 (INSTANCE)	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL[1:0]=3	counter1 clock source
MCU_DCC1	DCC_CLKSRC7_CLK	MCU_EXT_REFCLK0		counter1 clock source
MCU_DCC1	DCC_INPUT00_CLK	CLK_12M_RC		primary oscillator clock
MCU_DCC1	DCC_INPUT00_CLK	HFOSC0 (INSTANCE)		primary oscillator clock
MCU_DCC1	DCC_INPUT01_CLK	CLK_32K_RC		primary oscillator clock
MCU_DCC1	DCC_INPUT02_CLK	CLK_12M_RC		primary oscillator clock
MCU_DCC1	DCC_INPUT10_CLK	MCU_SYSCLK0/2		secondary oscillator clock
MCU_DCC1	FICLK	MCU_SYSCLK0/4		functional and interface clock

Table 4-230. Reset Integration for DCC

Module Instance	Source	Description
DCC0	PSC0	DCC0 reset
DCC1	PSC0	DCC1 reset
DCC2	PSC0	DCC2 reset
DCC3	PSC0	DCC3 reset
DCC4	PSC0	DCC4 reset
DCC5	PSC0	DCC5 reset
DCC6	PSC0	DCC6 reset
MCU_DCC0	WKUP_PSC0	MCU_DCC0 reset
MCU_DCC1	WKUP_PSC0	MCU_DCC1 reset

Table 4-231. Hardware Requests for DCC

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC0	DCC0_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC0 interrupt request	level
DCC0	DCC0_intr_err_level_0	ESM0_esm_lvl_event_112	ESM0	DCC0 interrupt request	level
DCC1	DCC1_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC1 interrupt request	level
DCC1	DCC1_intr_err_level_0	ESM0_esm_lvl_event_113	ESM0	DCC1 interrupt request	level
DCC2	DCC2_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC2 interrupt request	level

Table 4-231. Hardware Requests for DCC (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC2	DCC2_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC2 interrupt request	level
DCC2	DCC2_intr_err_level_0	ESM0_esm_lvl_event_114	ESM0	DCC2 interrupt request	level
DCC3	DCC3_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC3 interrupt request	level
DCC3	DCC3_intr_err_level_0	ESM0_esm_lvl_event_115	ESM0	DCC3 interrupt request	level
DCC4	DCC4_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC4 interrupt request	level
DCC4	DCC4_intr_err_level_0	ESM0_esm_lvl_event_116	ESM0	DCC4 interrupt request	level
DCC5	DCC5_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC5 interrupt request	level
DCC5	DCC5_intr_err_level_0	ESM0_esm_lvl_event_117	ESM0	DCC5 interrupt request	level
DCC6	DCC6_intr_done_level_0	GICSS0_spi_128	GICSS0	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_109	WKUP_R5FSS0_CORE0	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_109	MCU_R5FSS0_CORE0	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	C7X256V0_CLEC_gic_spi_96	C7X256V0_CLEC	DCC6 interrupt request	level
DCC6	DCC6_intr_err_level_0	ESM0_esm_lvl_event_79	ESM0	DCC6 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_108	WKUP_R5FSS0_CORE0	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_108	MCU_R5FSS0_CORE0	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_err_level_0	WKUP_ESM0_esm_lvl_event_37	WKUP_ESM0	MCU_DCC0 interrupt request	level

Table 4-231. Hardware Requests for DCC (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_DCC1	MCU_DCC1_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_137	WKUP_R5FSS0_CORE0	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	MCU_R5FSS0_CORE0_cpu0_intr_137	MCU_R5FSS0_CORE0	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_err_level_0	WKUP_ESM0_esm_lvl_event_36	WKUP_ESM0	MCU_DCC1 interrupt request	level

4.14.1.3 DCC Input Source Clock Mapping (AM62D)

- DCC0 Input Source Clock Mapping
- DCC1 Input Source Clock Mapping
- DCC2 Input Source Clock Mapping
- DCC3 Input Source Clock Mapping
- DCC4 Input Source Clock Mapping
- DCC5 Input Source Clock Mapping
- DCC6 Input Source Clock Mapping
- MCU_DCC0 Input Source Clock Mapping
- MCU_DCC1 Input Source Clock Mapping

Table 4-232. DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC0	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC0	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC0	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC0	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC0	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC0	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0/2
DCC0	DCC_CLKSRC0_CLK	1	1	MAIN_PLL0_HSDIV1_CLKOUT
DCC0	DCC_CLKSRC1_CLK	1	2	MAIN_PLL0_HSDIV2_CLKOUT
DCC0	DCC_CLKSRC2_CLK	1	3	MAIN_PLL0_HSDIV3_CLKOUT
DCC0	DCC_CLKSRC3_CLK	1	4	MAIN_PLL0_HSDIV4_CLKOUT
DCC0	DCC_CLKSRC4_CLK	1	5	CLK_12M_RC
DCC0	DCC_CLKSRC4_CLK	1	5	HFOSC0 (INSTANCE)
DCC0	DCC_CLKSRC5_CLK	1	6	EXT_REFCLK1
DCC0	DCC_CLKSRC6_CLK	1	7	MAIN_SYSCLK0
DCC0	DCC_CLKSRC7_CLK	1	8	MAIN_PLL2_HSDIV8_CLKOUT
DCC0	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-233. DCC1 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC1	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC1	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC1	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC1	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC1	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC1	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0/4

Table 4-233. DCC1 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC1	DCC_CLKSRC0_CLK	1	1	MAIN_PLL0_HSDIV5_CLKOUT
DCC1	DCC_CLKSRC1_CLK	1	2	MAIN_PLL0_HSDIV6_CLKOUT
DCC1	DCC_CLKSRC2_CLK	1	3	MAIN_PLL0_HSDIV7_CLKOUT
DCC1	DCC_CLKSRC3_CLK	1	4	MAIN_PLL1_HSDIV1_CLKOUT
DCC1	DCC_CLKSRC4_CLK	1	5	MAIN_PLL15_HSDIV2_CLKOUT/4
DCC1	DCC_CLKSRC5_CLK	1	6	MAIN_PLL1_HSDIV0_CLKOUT
DCC1	DCC_CLKSRC6_CLK	1	7	CLK_12M_RC
DCC1	DCC_CLKSRC7_CLK	1	8	MAIN_PLL1_HSDIV2_CLKOUT
DCC1	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-234. DCC2 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC2	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC2	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC2	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC2	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC2	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC2	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0/4
DCC2	DCC_CLKSRC0_CLK	1	1	MAIN_PLL1_HSDIV3_CLKOUT
DCC2	DCC_CLKSRC1_CLK	1	2	MAIN_PLL15_HSDIV0_CLKOUT
DCC2	DCC_CLKSRC2_CLK	1	3	MAIN_PLL1_HSDIV5_CLKOUT
DCC2	DCC_CLKSRC3_CLK	1	4	MAIN_PLL1_HSDIV6_CLKOUT
DCC2	DCC_CLKSRC4_CLK	1	5	MAIN_PLL5_HSDIV1_CLKOUT
DCC2	DCC_CLKSRC5_CLK	1	6	MAIN_PLL15_HSDIV1_CLKOUT
DCC2	DCC_CLKSRC6_CLK	1	7	MAIN_PLL2_HSDIV2_CLKOUT
DCC2	DCC_CLKSRC7_CLK	1	8	RMII2_REF_CLK (PIN)
DCC2	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-235. DCC3 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC3	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC3	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC3	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC3	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC3	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC3	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0/4
DCC3	DCC_CLKSRC0_CLK	1	1	MAIN_PLL1_HSDIV0_CLKOUT
DCC3	DCC_CLKSRC1_CLK	1	2	MAIN_PLL2_HSDIV5_CLKOUT
DCC3	DCC_CLKSRC2_CLK	1	3	C7X256V0_CLK (INSTANCE)
DCC3	DCC_CLKSRC3_CLK	1	4	MAIN_PLL2_HSDIV7_CLKOUT
DCC3	DCC_CLKSRC4_CLK	1	5	MAIN_PLL2_HSDIV6_CLKOUT
DCC3	DCC_CLKSRC5_CLK	1	6	MAIN_PLL2_HSDIV9_CLKOUT

Table 4-235. DCC3 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC3	DCC_CLKSRC6_CLK	1	7	A53SS0 (INSTANCE)/4
DCC3	DCC_CLKSRC7_CLK	1	8	DDR32SS0 (INSTANCE)
DCC3	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-236. DCC4 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC4	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC4	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC4	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC4	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC4	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC4	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0/2
DCC4	DCC_CLKSRC1_CLK	1	2	CP_GEMAC_CPTS_REF_CLK
DCC4	DCC_CLKSRC2_CLK	1	3	AUDIO_EXT_REFCLK1 (PIN)
DCC4	DCC_CLKSRC3_CLK	1	4	DPHY_RX0 (INSTANCE)
DCC4	DCC_CLKSRC4_CLK	1	5	MCU_EXT_REFCLK0
DCC4	DCC_CLKSRC5_CLK	1	6	RMII1_REF_CLK (PIN)/4
DCC4	DCC_CLKSRC7_CLK	1	8	CLK_32K_RC
DCC4	DCC_CLKSRC7_CLK	1	8	CLK_12M_RC
DCC4	DCC_CLKSRC7_CLK	1	8	HFOSC0 (INSTANCE)
DCC4	DCC_CLKSRC7_CLK	1	8	CLK_32K_RC
DCC4	DCC_CLKSRC7_CLK	1	8	LFOSC0 (INSTANCE)
DCC4	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-237. DCC5 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC5	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC5	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC5	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC5	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC5	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC5	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0
DCC5	DCC_CLKSRC0_CLK	1	1	MAIN_PLL0_HSDIV8_CLKOUT
DCC5	DCC_CLKSRC2_CLK	1	3	MAIN_PLL2_HSDIV1_CLKOUT
DCC5	DCC_CLKSRC3_CLK	1	4	MAIN_PLL2_HSDIV3_CLKOUT
DCC5	DCC_CLKSRC4_CLK	1	5	MAIN_PLL2_HSDIV4_CLKOUT
DCC5	DCC_CLKSRC5_CLK	1	6	MAIN_PLL5_HSDIV0_CLKOUT
DCC5	DCC_CLKSRC6_CLK	1	7	MAIN_PLL17_HSDIV0_CLKOUT
DCC5	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-238. DCC6 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
DCC6	DCC_INPUT00_CLK	0	0	CLK_12M_RC
DCC6	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
DCC6	DCC_INPUT01_CLK	0	1	EXT_REFCLK1
DCC6	DCC_INPUT02_CLK	0	2	CLK_12M_RC
DCC6	DCC_INPUT03_CLK	0	3	MAIN_SYSCLK0/4
DCC6	DCC_INPUT10_CLK	1	0	MAIN_SYSCLK0
DCC6	DCC_CLKSRC0_CLK	1	1	VOUT0_EXTPCLKIN (PIN)
DCC6	DCC_CLKSRC1_CLK	1	2	MCASP0_ACLKX (PIN)
DCC6	DCC_CLKSRC2_CLK	1	3	MCASP0_ACLKR (PIN)
DCC6	DCC_CLKSRC3_CLK	1	4	MCASP1_ACLKX (PIN)
DCC6	DCC_CLKSRC4_CLK	1	5	MCASP1_ACLKR (PIN)
DCC6	DCC_CLKSRC5_CLK	1	6	MCASP2_ACLKX (PIN)
DCC6	DCC_CLKSRC6_CLK	1	7	MCASP2_ACLKR (PIN)
DCC6	DCC_CLKSRC7_CLK	1	8	AUDIO_EXT_REFCLK0 (PIN)
DCC6	FICLK	1	9	MAIN_SYSCLK0/4

Table 4-239. MCU_DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
MCU_DCC0	DCC_INPUT00_CLK	0	0	CLK_12M_RC
MCU_DCC0	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)
MCU_DCC0	DCC_INPUT01_CLK	0	1	CLK_32K_RC
MCU_DCC0	DCC_INPUT02_CLK	0	2	CLK_12M_RC
MCU_DCC0	DCC_INPUT03_CLK	0	3	MCU_SYSCLK0/4
MCU_DCC0	DCC_INPUT10_CLK	1	0	MCU_SYSCLK0/2
MCU_DCC0	DCC_CLKSRC0_CLK	1	1	MCU_PLL0_HSDIV0_CLKOUT
MCU_DCC0	DCC_CLKSRC1_CLK	1	2	MCU_PLL0_HSDIV1_CLKOUT
MCU_DCC0	DCC_CLKSRC2_CLK	1	3	MCU_PLL0_HSDIV2_CLKOUT
MCU_DCC0	DCC_CLKSRC3_CLK	1	4	MCU_PLL0_HSDIV3_CLKOUT/4
MCU_DCC0	DCC_CLKSRC4_CLK	1	5	MCU_PLL0_HSDIV4_CLKOUT
MCU_DCC0	DCC_CLKSRC5_CLK	1	6	CLK_32K_RC
MCU_DCC0	DCC_CLKSRC6_CLK	1	7	CLK_32K_RC
MCU_DCC0	DCC_CLKSRC6_CLK	1	7	CLK_12M_RC
MCU_DCC0	DCC_CLKSRC6_CLK	1	7	HFOSC0 (INSTANCE)
MCU_DCC0	DCC_CLKSRC6_CLK	1	7	CLK_32K_RC
MCU_DCC0	DCC_CLKSRC6_CLK	1	7	LFOSC0 (INSTANCE)
MCU_DCC0	DCC_CLKSRC7_CLK	1	8	MCU_EXT_REFCLK0
MCU_DCC0	FICLK	1	9	MCU_SYSCLK0/4

Table 4-240. MCU_DCC1 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
MCU_DCC1	DCC_INPUT00_CLK	0	0	CLK_12M_RC
MCU_DCC1	DCC_INPUT00_CLK	0	0	HFOSC0 (INSTANCE)

Table 4-240. MCU_DCC1 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Clock Source
MCU_DCC1	DCC_INPUT01_CLK	0	1	CLK_32K_RC
MCU_DCC1	DCC_INPUT02_CLK	0	2	CLK_12M_RC
MCU_DCC1	DCC_INPUT03_CLK	0	3	MCU_SYSCLK0/4
MCU_DCC1	DCC_INPUT10_CLK	1	0	MCU_SYSCLK0/2
MCU_DCC1	DCC_CLKSRC0_CLK	1	1	MCU_PLL0_HSDIV5_CLKOUT
MCU_DCC1	DCC_CLKSRC1_CLK	1	2	MCU_PLL0_HSDIV6_CLKOUT
MCU_DCC1	DCC_CLKSRC5_CLK	1	6	CLK_32K_RC
MCU_DCC1	DCC_CLKSRC6_CLK	1	7	CLK_32K_RC
MCU_DCC1	DCC_CLKSRC6_CLK	1	7	CLK_12M_RC
MCU_DCC1	DCC_CLKSRC6_CLK	1	7	HFOSC0 (INSTANCE)
MCU_DCC1	DCC_CLKSRC6_CLK	1	7	CLK_32K_RC
MCU_DCC1	DCC_CLKSRC6_CLK	1	7	LFOSC0 (INSTANCE)
MCU_DCC1	DCC_CLKSRC7_CLK	1	8	MCU_EXT_REFCLK0
MCU_DCC1	FICLK	1	9	MCU_SYSCLK0/4

4.14.2 Error Signaling Module (ESM)

This section contains the integration details for the ESM module on this device. For further information, see the *Error Signaling Module (ESM)* section of the *Peripherals* chapter.

4.14.2.1 ESM Unsupported Features

The following features are not supported on this family of devices:

- No Dedicated ERROR Pin for MAIN domain ESM. MAIN ESM error interrupts are routed to the MCU ESM - the MCU ESM drives the MCU_ERROR pin and can factor in errors from MAIN ESM if programmed to do so.

4.14.2.2 ESM Integration

Table 4-241. ESM Module Allocations

Instance	MAIN	MCU	WKUP
ESM0	✓		
WKUP_ESM0			✓

Table 4-242. Integration Attributes for ESM

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ESM0	PSC0	GP_Core_CTL	LPSC_main_alwayson	0	ON	NO	
WKUP_ESM0	WKUP_PSC0	GP_core_CTL_MCU	LPSC_mcu_alwayson	0	ON	NO	

Table 4-243. Clock Integration for ESM

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
ESM0	CLK	MAIN_SYSCLK0/4		None
WKUP_ESM0	FICLK	MCU_SYSCLK0/4		functional and interface clock

Table 4-244. Reset Integration for ESM

Module Instance	Source	Description
ESM0	PSC0	ESM0 reset
WKUP_ESM0	WKUP_PSC0	WKUP_ESM0 reset

Table 4-245. Hardware Requests for ESM

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ESM0	ESM0_esm_int_cfg_lvl_0	WKUP_ESM0_esm_lvl_event_0	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	GICSS0_spi_180	GICSS0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	WKUP_R5FSS0_CORE0_intr_167	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_167	MCU_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	C7X256V0_CLEC_gic_spi_148	C7X256V0_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	WKUP_ESM0_esm_lvl_event_1	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	GICSS0_spi_181	GICSS0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	WKUP_R5FSS0_CORE0_intr_168	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level

Table 4-245. Hardware Requests for ESM (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ESM0	ESM0_esm_int_hi_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_168	MCU_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	C7X256V0_CLEC_gic_spi_149	C7X256V0_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	WKUP_ESM0_esm_lvl_event_2	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	GICSS0_spi_182	GICSS0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	WKUP_R5FSS0_CORE0_intr_169	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_169	MCU_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	C7X256V0_CLEC_gic_spi_150	C7X256V0_CLEC	ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	ESM0_esm_lvl_event_37	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	WKUP_R5FSS0_CORE0_intr_140	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_140	MCU_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	ESM0_esm_lvl_event_38	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	WKUP_R5FSS0_CORE0_intr_141	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_141	MCU_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	ESM0_esm_lvl_event_39	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	WKUP_R5FSS0_CORE0_intr_142	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	MCU_R5FSS0_CORE0_cpu0_intr_142	MCU_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level

4.14.3 Memory Cyclic Redundancy Check (MCRC64)

This section contains the integration details for the MCRC64 module on this device. For further information, see the *Memory Cyclic Redundancy Check (MCRC)* section of the *Peripherals* chapter.

4.14.3.1 MCRC64 Unsupported Features

The following features are not supported on this family of devices:

- Data Trace Mode (Automatic PSA on CPU Instruction and Data TCM busses) - Wrapper only supports VBUSM Signature Analysis. ITCM, DTCM designed for Cortex R5F
- DMA is not supported by the MCU instances

4.14.3.2 MCRC64 Integration

Table 4-246. MCRC64 Module Allocations

Instance	MAIN	MCU	WKUP
MCRC64_0	✓		
MCU_MCRC64_0		✓	

Table 4-247. Integration Attributes for MCRC64

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCRC64_0	PSC0	GP_Core_CTL	LPSC_main_IP	34	ON	YES	LPSC_DM2main_infra_ISO
MCU_MCRC64_0	WKUP_PSC0	PD_MCUSS	LPSC_MCU_common	9	ON	YES	LPSC_DM2safe_ISO

Table 4-248. Clock Integration for MCRC64

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCRC64_0	FICLK	MAIN_SYSCLK0/2		None
MCU_MCRC64_0	FICLK	MCU_SYSCLK0		None

Table 4-249. Reset Integration for MCRC64

Module Instance	Source	Description
MCRC64_0	PSC0	MCRC64_0 reset
MCU_MCRC64_0	WKUP_PSC0	MCU_MCRC64_0 reset

Table 4-250. Hardware Requests for MCRC64

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCRC64_0	MCRC64_0_dma_event_0	DMASS0_INTAGGR_0_intaggr_levi_pend_28	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_1	DMASS0_INTAGGR_0_intaggr_levi_pend_29	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_2	DMASS0_INTAGGR_0_intaggr_levi_pend_30	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_3	DMASS0_INTAGGR_0_intaggr_levi_pend_31	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_int_mcrc_0	GICSS0_spi_166	GICSS0	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	WKUP_R5FSS0_CORE0_intr_119	WKUP_R5FSS0_CORE0	MCRC64_0 interrupt request	level

Table 4-250. Hardware Requests for MCRC64 (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCRC64_0	MCRC64_0_int_mcrc_0	MCU_R5FSS0_CORE0_cpu0_intr_119	MCU_R5FSS0_CORE0	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	C7X256V0_CLEC_gic_spi_134	C7X256V0_CLEC	MCRC64_0 interrupt request	level
MCU_MCRC64_0	MCU_MCRC64_0_int_mcrc_0	GICSS0_spi_192	GICSS0	MCU_MCRC64_0 interrupt request	level
MCU_MCRC64_0	MCU_MCRC64_0_int_mcrc_0	WKUP_R5FSS0_CORE0_intr_192	WKUP_R5FSS0_CORE0	MCU_MCRC64_0 interrupt request	level
MCU_MCRC64_0	MCU_MCRC64_0_int_mcrc_0	MCU_R5FSS0_CORE0_cpu0_intr_192	MCU_R5FSS0_CORE0	MCU_MCRC64_0 interrupt request	level
MCU_MCRC64_0	MCU_MCRC64_0_int_mcrc_0	C7X256V0_CLEC_gic_spi_160	C7X256V0_CLEC	MCU_MCRC64_0 interrupt request	level

4.14.4 ECC Aggregator (ECC_AGGR)

This section contains the integration details for the ECC_AGGR module on this device. For further information, see the *ECC Aggregator (ECC_AGGR)* section of the *Peripherals* chapter.

4.14.4.1 ECC_AGGR Integration

Table 4-251. ECC_AGGR Module Allocations

Instance	MAIN	MCU	WKUP
WKUP_ECC_AGGR0			✓
WKUP_ECC_AGGR1			✓
MCU_ECC_AGGR0		✓	
MCU_ECC_AGGR1		✓	
ECC_AGGR0	✓		
ECC_AGGR1	✓		
WKUP_ECC_AGGR2			✓

Table 4-252. Clock Integration for ECC_AGGR

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
WKUP_ECC_AGGR0	CLK	DM_CLK/2		None
WKUP_ECC_AGGR1	CLK	MCU_SYSCLK0/4		None
MCU_ECC_AGGR0	CLK	MCU_SYSCLK0/2		None
MCU_ECC_AGGR1	CLK	MCU_PLL0_HSDIV3_CLKOUT		None
ECC_AGGR0	CLK	MAIN_PLL15_HSDIV0_CLKOUT/2		None
ECC_AGGR1	CLK	MCU_SYSCLK0/4		None
WKUP_ECC_AGGR2	CLK	MCU_SYSCLK0/4		None

Table 4-253. Hardware Requests for ECC_AGGR

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_20	ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_corr_level_0	WKUP_ESM0_esm_lvl_event_23	WKUP_ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_21	ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_uncorr_level_0	WKUP_ESM0_esm_lvl_event_24	WKUP_ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_corr_level_0	ESM0_esm_lvl_event_104	ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_corr_level_0	WKUP_ESM0_esm_lvl_event_38	WKUP_ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_uncorr_level_0	ESM0_esm_lvl_event_105	ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_uncorr_level_0	WKUP_ESM0_esm_lvl_event_39	WKUP_ESM0	WKUP_ECC_AGGR1 interrupt request	level
MCU_ECC_AGGR0	MCU_ECC_AGGR0_corr_level_0	WKUP_ESM0_esm_lvl_event_14	WKUP_ESM0	MCU_ECC_AGGR0 interrupt request	level
MCU_ECC_AGGR0	MCU_ECC_AGGR0_uncorr_level_0	WKUP_ESM0_esm_lvl_event_15	WKUP_ESM0	MCU_ECC_AGGR0 interrupt request	level
MCU_ECC_AGGR1	MCU_ECC_AGGR1_corr_level_0	WKUP_ESM0_esm_lvl_event_40	WKUP_ESM0	MCU_ECC_AGGR1 interrupt request	level

Table 4-253. Hardware Requests for ECC_AGGR (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_ECC_AGGR1	MCU_ECC_AGGR1_uncorr_level_0	WKUP_ESM0_esm_lvl_event_41	WKUP_ESM0	MCU_ECC_AGGR1 interrupt request	level
ECC_AGGR0	ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_2	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_1	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR1	ECC_AGGR1_corr_level_0	ESM0_esm_lvl_event_106	ESM0	ECC_AGGR1 interrupt request	level
ECC_AGGR1	ECC_AGGR1_uncorr_level_0	ESM0_esm_lvl_event_107	ESM0	ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_corr_level_0	WKUP_ESM0_esm_lvl_event_20	WKUP_ESM0	WKUP_ECC_AGGR2 interrupt request	level
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_uncorr_level_0	WKUP_ESM0_esm_lvl_event_21	WKUP_ESM0	WKUP_ECC_AGGR2 interrupt request	level

4.14.4.2 Device Modules and Subsystems with ECC Aggregator

Table 4-254. Device Modules and Subsystems with ECC Aggregator

Instance Name	MAIN	MCU	WKUP
CSI_RX_IF0	✓		
MMCSD1	✓		
MMCSD2	✓		
MMCSD0	✓		
GICSS0	✓		
WKUP_VTM0			✓
MCAN0	✓		
MCU_MCAN0		✓	
MCU_MCAN1		✓	
PSRAMECC0	✓		
PSRAMECC1	✓		
R5FSS0			✓
PDMA0	✓		
PDMA1	✓		
VPAC0	✓		
USB0	✓		
USB1	✓		

4.14.4.3 ECC Aggregators Interconnect

EDC Checkers Information of ECC Aggregator Instance

- EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1_SAM62A_SEC_MCU_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K1_MSRAM32KX64E_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR
- EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR
- EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR

Properties of ECC Aggregator Instance

- Properties of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR

- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE0
- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE1
- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE2
- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE3
- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_COREPAC
- Properties of ECC Aggregator Instance CPSW0_CPSW_3GUSS_CORE_ECC_CPSW_ECC_AGGR
- Properties of ECC Aggregator Instance DMASS0_DMSS_AM62A_ECCAGGR
- Properties of ECC Aggregator Instance ECC_AGGR1_SAM62A_SEC_MCU_ECC_AGGR
- Properties of ECC Aggregator Instance FSS0_FSS_UL_OSPI0_OSPI_WRAP_ECC_AGGR
- Properties of ECC Aggregator Instance GICSS0_GIC500SS_1_4_ECC_AGGR
- Properties of ECC Aggregator Instance MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_MSRAM_256K1_MSRAM32KX64E_ECC_AGGR
- Properties of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR
- Properties of ECC Aggregator Instance MMCSD0_EMMCSD8SS_ECC_AGGR_RXMEM
- Properties of ECC Aggregator Instance MMCSD0_EMMCSD8SS_ECC_AGGR_TXMEM
- Properties of ECC Aggregator Instance MMCSD1_EMMCSD4SS_ECC_AGGR_RXMEM
- Properties of ECC Aggregator Instance MMCSD1_EMMCSD4SS_ECC_AGGR_TXMEM
- Properties of ECC Aggregator Instance MMCSD2_EMMCSD4SS_ECC_AGGR_RXMEM
- Properties of ECC Aggregator Instance MMCSD2_EMMCSD4SS_ECC_AGGR_TXMEM
- Properties of ECC Aggregator Instance MSRAM_64K0_MSRAM2KX256E_ECC_AGGR
- Properties of ECC Aggregator Instance PDMA0_SAM62_PDMA_SPI_ECCAGGR
- Properties of ECC Aggregator Instance PDMA1_SAM62_PDMA_UART_ECCAGGR
- Properties of ECC Aggregator Instance PSCSS0_SAM62A_MAIN_PSC_WRAP_ECC_AGGR
- Properties of ECC Aggregator Instance PSRAMECC0_PSRAM256X32E_ECC_AGGR
- Properties of ECC Aggregator Instance PSRAMECC1_PSRAM256X32E_ECC_AGGR
- Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR
- Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_SA_UL_ECC_AGGR
- Properties of ECC Aggregator Instance USB0_USB2SS_16FFC_USB2SS_CORE_ECC_AGGR
- Properties of ECC Aggregator Instance USB1_USB2SS_16FFC_USB2SS_CORE_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_PSRAMECC_8K0_PSRAM8KX32E_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_R5FSS0_PULSAR_UL_CPU0_ECC_AGGR
- Properties of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AC71_PMC_WRAP_PMC_MEMWRAP_EDC_CTRL_PARITY_0	0	0	37	Parity

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AC71_PMC_WRAP_PMC_MEMWRAP_EDC_CTRL_PARITY_0	0	1	37	Parity
AC71_PMC_WRAP_PMC_MEMWRAP_EDC_CTRL_PARITY_0	0	2	37	Parity
AC71_PMC_WRAP_PMC_MEMWRAP_EDC_CTRL_PARITY_0	0	3	37	Parity
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_TAG_CTL_TOP_DMC_TAG_CTL_EDC_CTRL_0	1	0	45	Parity
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_TAG_CTL_TOP_DMC_TAG_CTL_EDC_CTRL_0	1	1	45	Parity
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	0	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	1	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	2	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	3	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	4	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	5	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	6	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	7	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	8	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	9	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	10	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	11	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	12	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	13	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	14	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	15	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	16	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	17	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	18	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	19	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	20	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	21	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	22	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	23	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	24	8	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	25	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	26	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	27	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	28	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	29	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	30	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	31	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	32	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	33	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	34	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	35	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	36	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	37	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	38	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	39	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	40	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	41	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	42	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	43	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	44	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	45	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	46	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	47	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	48	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	49	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	50	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	51	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	52	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	53	8	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	54	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	55	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	56	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	57	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	58	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	59	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	60	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	61	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	62	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	63	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	64	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	65	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	66	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	67	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	68	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	69	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	70	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	71	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	72	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	73	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	74	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	75	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	76	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	77	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	78	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	79	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	80	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	81	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	82	8	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	83	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	84	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	85	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	86	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	87	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	88	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	89	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	90	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	91	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	92	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	93	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	94	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	95	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	96	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	97	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	98	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	99	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	100	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	101	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	102	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	103	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	104	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	105	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	106	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	107	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	108	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	109	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	110	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	111	8	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	112	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	113	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	114	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	115	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	116	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	117	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	118	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	119	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	120	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	121	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	122	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	123	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	124	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	125	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	126	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	127	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	128	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	129	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	130	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	131	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	132	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	133	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	134	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	135	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	136	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	137	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	138	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	139	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	140	8	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	141	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	142	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	143	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	144	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	145	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	146	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	147	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	148	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	149	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	150	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	151	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	152	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	153	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	154	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	155	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	156	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	157	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	158	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	159	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	160	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	161	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	162	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	163	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	164	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	165	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	166	8	Error Detect and Correct
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	167	8	Error Detect and Correct
DRU_R30_C_R_CORE_QUEUE_CMD_EDC_CTRL_0	3	0	256	Error Detect and Correct
DRU_R30_C_R_CORE_QUEUE_CMD_EDC_CTRL_0	3	1	256	Error Detect and Correct
DRU_R30_C_R_CORE_QUEUE_CMD_EDC_CTRL_0	3	2	25	Error Detect and Correct
DRU_R30_C_R_CORE_QUEUE_CMD_EDC_CTRL_0	3	3	256	Error Detect and Correct

Table 4-255. EDC Checkers Information of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DRU_R30_C_R_CORE_RD_BUFFER_CMD_EDC_CTRL_0	4	0	256	Error Detect and Correct
DRU_R30_C_R_CORE_CH_LOGIC_RING_MEM_RING_EDC_CTRL_0	5	0	256	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	0	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	1	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	2	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	3	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	4	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	5	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	6	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	7	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	8	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	9	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	10	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	11	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	12	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	13	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	14	128	Error Detect and Correct
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	15	128	Error Detect and Correct

Table 4-256. EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1_SAM62A_SEC_MCU_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	0	0	1	Redundant
AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	0	1	1	Redundant
AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	0	2	12	Parity
AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	0	3	3	Parity

Table 4-257. EDC Checkers Information of ECC Aggregator Instance MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CTRL_EDC_VBUSS	1	0	32	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	0	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	2	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	3	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	4	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	5	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	6	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	7	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	8	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	11	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	12	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	13	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	14	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	15	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	16	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	17	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	19	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	21	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	22	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	23	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	24	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	25	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	26	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	27	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	28	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	29	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	30	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	31	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	32	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	33	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	34	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	35	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	36	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	37	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	38	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	39	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	40	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	41	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	42	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	43	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	44	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	45	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	46	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	47	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	48	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	49	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	50	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	51	7	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	52	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	53	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	54	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	55	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	56	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	57	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	58	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	59	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	60	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	61	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	62	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	63	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	64	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	65	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	66	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	67	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	68	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	0	24	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	2	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	3	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	4	23	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	5	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	7	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	9	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	11	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	12	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	13	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	14	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	15	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	16	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	17	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	19	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	21	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	22	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	23	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	24	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	25	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	26	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	27	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	28	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	29	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	30	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	31	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	32	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	33	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	34	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	35	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	36	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	37	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	38	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	39	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	40	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	41	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	42	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	43	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	44	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	45	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	46	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	47	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	48	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	49	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	50	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	51	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	52	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	53	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	54	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	55	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	56	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	57	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	58	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	59	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	60	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	61	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	62	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	63	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	64	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	0	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	2	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	3	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	4	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	5	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	6	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	7	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	8	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	11	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	12	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	13	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	14	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	15	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	16	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	17	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	19	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	21	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	22	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	23	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	24	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	25	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	26	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	27	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	28	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	29	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	30	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	31	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	32	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	33	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	34	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	35	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	36	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	37	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	38	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	39	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	40	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	41	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	42	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	43	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	44	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	45	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	46	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	47	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	48	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	49	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	50	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	51	7	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	52	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	53	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	54	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	55	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	56	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	57	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	58	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	59	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	60	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	61	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	62	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	63	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	64	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	65	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	66	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	67	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	68	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	0	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	2	11	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	3	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	4	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	5	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	7	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	11	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	12	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	13	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	14	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_DST_BUSECC	4	0	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_DST_BUSECC	4	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_DST_BUSECC	4	2	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_DST_BUSECC	4	3	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	0	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	2	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	3	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	4	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	5	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	7	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	11	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	12	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	13	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	14	2	Parity
ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL	6	0	48	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	0	1	Redundant
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	1	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	2	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	3	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	4	32	Error Detect and Correct
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	5	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	6	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	7	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	8	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	9	30	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	10	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	11	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	12	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	13	12	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	14	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	15	3	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	16	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	17	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	18	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	19	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	20	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	21	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	22	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	23	12	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	24	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	25	3	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	26	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	27	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	28	3	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	29	3	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	30	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	31	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	32	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	33	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	34	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	35	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	36	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	37	1	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	38	30	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	39	6	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	40	6	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	41	6	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	42	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	43	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	44	5	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	45	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	46	16	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	47	9	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	48	16	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	49	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	50	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	51	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	52	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	53	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	54	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	55	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	56	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	57	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	58	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	59	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	60	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	61	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	62	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	63	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	64	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	65	20	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	66	20	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	67	10	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	68	3	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	69	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	70	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	71	5	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	72	4	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	73	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	74	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	75	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	76	2	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	77	55	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	78	55	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	79	8	Parity
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	80	8	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	0	1	Redundant
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	1	1	Redundant
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	2	1	Redundant
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	3	10	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	4	3	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	5	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	6	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	0	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	1	32	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	2	1	Redundant
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	3	1	Redundant
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	4	10	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	5	3	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	6	3	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	7	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	8	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	9	2	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_I AM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	10	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	11	1	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	12	10	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	13	5	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	14	3	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	15	4	Parity
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	16	2	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	0	1	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	1	32	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	2	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	3	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	4	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	5	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	6	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	7	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	8	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	9	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	10	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	11	1	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	12	1	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	0	1	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	1	32	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	2	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	3	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	4	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	5	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	6	1	Redundant
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	7	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	8	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	9	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	10	8	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	11	1	Parity
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	12	1	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	0	1	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	1	32	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	2	1	Redundant
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	3	1	Redundant
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	4	1	Redundant
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	5	1	Redundant
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	6	1	Redundant
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	7	8	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	8	8	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	9	8	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	10	8	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	11	1	Parity
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	12	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	0	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	1	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	2	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	3	10	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	4	3	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	5	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	6	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	0	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	1	32	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	2	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	3	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	4	10	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	5	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	6	3	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	7	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	8	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	9	2	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	10	3	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	11	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	12	10	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	13	5	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	14	3	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	15	4	Parity
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	16	2	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	0	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	1	32	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	2	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	3	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	4	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	5	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	6	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	7	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	8	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	9	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	10	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	11	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	12	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	0	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	1	32	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	2	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	3	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	4	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	5	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	6	1	Redundant
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	7	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	8	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	9	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	10	8	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	11	1	Parity
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	12	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	0	36	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	1	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	2	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	3	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	4	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	5	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	6	29	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	7	36	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	8	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	9	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	10	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	11	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	12	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	13	29	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	14	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	15	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	16	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	17	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	18	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	19	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	20	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	21	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	22	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	23	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	24	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	25	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	26	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	27	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	28	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	29	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	30	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	31	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	32	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	33	8	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	34	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	35	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	36	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	37	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	38	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	39	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	40	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	41	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	42	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	43	36	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	44	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	45	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	46	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	47	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	48	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	49	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	50	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	51	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	52	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	53	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	54	8	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	55	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	56	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	57	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	58	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	59	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	60	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	61	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	62	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	63	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	64	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	65	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	66	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	67	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	68	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	69	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	70	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	71	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	72	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	73	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	74	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	75	8	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	76	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	77	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	78	32	Error Detect and Correct

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	79	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	80	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	0	36	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	1	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	2	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	3	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	4	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	5	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	6	29	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	7	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	8	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	9	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	10	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	11	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	12	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	13	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	14	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	15	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	16	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	17	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	18	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	19	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	20	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	21	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	22	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	23	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	24	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	25	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	26	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	27	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	28	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	29	16	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	30	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	31	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	32	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	33	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	34	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	35	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	36	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	37	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	38	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	39	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	40	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	41	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	42	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	43	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	44	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	45	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	46	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	47	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	48	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	49	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	50	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	51	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	52	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	53	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	54	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	55	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	56	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	57	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	58	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	59	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	60	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	61	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	62	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	63	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	64	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	65	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	66	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	67	9	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	68	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	69	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	70	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	71	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	72	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	73	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	74	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	75	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	76	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	77	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	78	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	79	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	80	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	81	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	82	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	83	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	84	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	85	16	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	86	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	87	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	88	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	89	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	90	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	91	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	92	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	93	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	94	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	95	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	96	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	97	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	98	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	99	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	100	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	0	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	1	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	2	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	3	8	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	4	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	5	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	6	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	7	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	8	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	9	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	10	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	11	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	12	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	13	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	14	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	15	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	16	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	17	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	18	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	19	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	20	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	21	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	22	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	23	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	24	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	25	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	26	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	27	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	28	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	29	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	30	8	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	31	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	32	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	33	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	34	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	35	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	36	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	37	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	38	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	39	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	40	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	41	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	42	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	43	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	44	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	45	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	46	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	47	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	48	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	49	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	50	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	51	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	52	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	53	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	54	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	55	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	56	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	57	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	58	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	59	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	60	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	61	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	62	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	63	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	64	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	65	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	66	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	67	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	68	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	69	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	70	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	71	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	72	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	73	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	74	11	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	75	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	76	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	77	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	78	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	79	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	80	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	81	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	82	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	83	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	84	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	85	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	86	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	87	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	88	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	89	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	90	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	91	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	92	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	93	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	94	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	95	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	96	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	97	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	98	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	99	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	100	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	101	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	102	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	103	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	104	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	105	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	106	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	107	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	108	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	109	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	110	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	111	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	112	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	113	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	114	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	115	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	116	1	Redundant
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	117	32	Error Detect and Correct
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	118	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	119	11	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	120	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	121	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	122	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	123	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	124	10	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	125	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	126	4	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	127	12	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	128	2	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	129	3	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	130	2	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	131	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	132	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	133	1	Parity
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	134	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	0	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	1	36	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	2	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	3	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	4	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	5	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	6	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	7	2	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	8	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	9	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	10	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	11	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	12	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	13	36	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	14	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	15	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	16	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	17	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	18	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	19	2	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	20	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	21	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	22	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	23	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	24	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	25	36	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	26	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	27	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	28	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	29	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	30	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	31	2	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	32	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	33	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	34	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	35	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	36	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	37	36	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	38	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	39	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	40	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	41	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	42	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	43	2	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	44	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	45	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	46	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	47	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	48	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	49	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	50	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	51	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	52	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	53	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	54	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	55	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	56	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	57	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	58	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	59	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	60	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	61	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	62	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	63	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	64	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	65	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	66	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	67	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	68	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	69	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	70	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	71	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	72	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	73	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	74	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	75	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	76	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	77	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	78	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	79	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	80	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	81	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	82	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	83	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	84	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	85	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	86	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	87	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	88	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	89	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	90	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	91	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	92	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	93	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	94	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	95	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	96	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	97	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	98	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	99	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	100	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	101	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	102	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	103	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	104	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	105	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	106	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	107	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	108	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	109	10	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	110	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	111	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	112	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	113	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	114	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	115	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	116	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	117	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	118	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	119	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	120	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	121	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	122	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	123	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	124	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	125	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	126	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	127	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	128	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	129	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	130	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	131	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	132	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	133	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	134	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	135	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	136	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	137	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	138	12	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	139	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	140	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	141	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	142	12	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	143	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	144	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	145	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	146	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	147	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	148	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	149	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	150	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	151	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	152	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	153	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	154	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	155	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	156	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	157	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	158	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	159	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	160	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	161	15	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	162	9	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	163	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	164	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	165	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	166	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	167	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	168	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	169	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	170	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	171	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	172	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	173	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	174	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	175	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	176	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	177	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	178	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	179	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	180	15	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	181	9	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	182	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	183	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	184	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	185	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	186	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	187	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	188	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	189	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	190	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	191	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	192	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	193	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	194	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	195	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	196	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	197	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	198	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	199	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	200	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	201	39	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	202	7	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	203	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	204	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	205	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	206	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	207	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	208	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	209	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	210	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	211	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	212	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	213	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	214	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	215	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	216	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	217	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	218	11	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	219	9	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	220	44	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	221	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	222	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	223	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	224	29	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	225	26	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	226	7	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	227	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	228	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	229	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	230	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	231	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	232	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	233	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	234	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	235	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	236	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	237	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	238	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	239	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	240	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	241	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	242	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	243	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	244	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	245	29	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	246	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	247	7	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	248	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	249	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	250	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	251	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	252	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	253	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	254	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	255	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	0	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	1	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	2	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	3	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	4	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	5	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	6	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	7	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	8	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	9	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	10	29	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	11	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	12	7	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	13	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	14	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	15	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	16	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	17	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	18	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	19	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	20	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	21	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	22	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	23	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	24	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	25	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	26	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	27	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	28	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	29	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	30	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	31	19	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	32	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	33	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	34	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	35	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	36	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	37	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	38	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	39	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	40	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	41	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	42	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	43	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	44	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	45	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	46	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	47	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	48	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	49	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	50	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	51	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	52	24	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	53	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	54	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	55	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	56	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	57	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	58	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	59	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	60	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	61	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	62	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	63	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	64	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	65	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	66	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	67	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	68	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	69	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	70	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	71	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	72	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	73	24	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	74	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	75	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	76	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	77	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	78	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	79	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	80	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	81	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	82	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	83	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	84	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	85	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	86	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	87	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	88	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	89	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	90	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	91	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	92	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	93	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	94	24	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	95	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	96	6	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	97	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	98	4	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	99	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	100	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	101	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	102	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	103	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	104	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	105	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	106	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	107	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	108	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	109	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	110	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	111	8	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	112	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	113	3	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	114	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	115	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	116	26	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	117	7	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	118	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	119	5	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	120	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	121	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	122	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	123	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	124	1	Redundant
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	125	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	126	32	Error Detect and Correct
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	127	32	Error Detect and Correct
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	128	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	129	1	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	130	36	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	131	10	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	132	2	Parity
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	133	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	0	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	1	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	2	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	3	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	4	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	5	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	6	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	7	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	8	2	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	9	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	10	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	11	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	12	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	13	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	14	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	15	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	16	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	17	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	18	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	19	2	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	20	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	21	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	22	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	23	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	24	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	25	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	26	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	27	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	28	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	29	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	30	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	31	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	32	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	33	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	34	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	35	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	36	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	37	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	38	12	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	39	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	40	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	41	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	42	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	43	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	44	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	45	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	46	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	47	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	48	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	49	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	50	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	51	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	52	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	53	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	54	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	55	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	56	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	57	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	58	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	59	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	60	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	61	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	62	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	63	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	64	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	65	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	66	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	67	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	68	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	69	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	70	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	71	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	72	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	73	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	74	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	75	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	76	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	77	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	78	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	79	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	80	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	81	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	82	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	83	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	84	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	85	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	86	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	87	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	88	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	89	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	90	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	91	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	92	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	93	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	94	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	95	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	96	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	97	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	98	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	99	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	100	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	101	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	102	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	103	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	104	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	105	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	106	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	107	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	108	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	109	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	110	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	111	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	112	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	113	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	114	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	115	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	116	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	117	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	118	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	119	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	120	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	121	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	122	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	123	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	124	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	125	5	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	126	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	127	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	128	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	129	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	130	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	131	9	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	132	14	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	133	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	134	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	135	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	136	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	137	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	138	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	139	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	140	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	141	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	142	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	143	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	144	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	145	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	146	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	147	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	148	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	149	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	150	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	151	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	152	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	153	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	154	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	155	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	156	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	157	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	158	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	159	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	160	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	161	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	162	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	163	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	164	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	165	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	166	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	167	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	168	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	169	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	170	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	171	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	172	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	173	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	174	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	175	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	176	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	177	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	178	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	179	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	180	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	181	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	182	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	183	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	184	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	185	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	186	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	187	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	188	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	189	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	190	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	191	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	192	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	193	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	194	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	195	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	196	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	197	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	198	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	199	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	200	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	201	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	202	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	203	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	204	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	205	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	206	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	207	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	208	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	209	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	210	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	211	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	212	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	213	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	214	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	215	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	216	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	217	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	218	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	219	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	220	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	221	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	222	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	223	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	224	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	225	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	226	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	227	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	228	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	229	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	230	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	231	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	232	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	233	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	234	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	235	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	236	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	237	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	238	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	239	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	240	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	241	19	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	242	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	243	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	244	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	245	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	246	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	247	16	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	248	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	249	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	250	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	251	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	252	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	253	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	254	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	255	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	0	16	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	1	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	2	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	3	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	4	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	5	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	6	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	7	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	8	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	9	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	10	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	11	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	12	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	13	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	14	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	15	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	16	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	17	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	18	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	19	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	20	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	21	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	22	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	23	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	24	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	25	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	26	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	27	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	28	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	29	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	30	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	31	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	32	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	33	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	34	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	35	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	36	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	37	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	38	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	39	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	40	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	41	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	42	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	43	9	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	44	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	45	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	46	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	47	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	48	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	49	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	50	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	51	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	52	9	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	53	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	54	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	55	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	56	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	57	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	58	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	59	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	60	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	61	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	62	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	63	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	64	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	65	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	66	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	67	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	68	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	69	16	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	70	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	71	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	72	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	73	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	74	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	75	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	76	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	77	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	78	16	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	79	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	80	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	81	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	82	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	83	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	84	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	85	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	86	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	87	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	88	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	89	19	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	90	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	91	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	92	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	93	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	94	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	95	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	96	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	97	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	98	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	99	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	100	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	101	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	102	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	103	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	104	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	105	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	106	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	107	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	108	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	109	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	110	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	111	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	112	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	113	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	114	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	115	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	116	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	117	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	118	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	119	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	120	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	121	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	122	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	123	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	124	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	125	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	126	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	127	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	128	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	129	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	130	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	131	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	132	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	133	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	134	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	135	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	136	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	137	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	138	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	139	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	140	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	141	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	142	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	143	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	144	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	145	32	Error Detect and Correct
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	146	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	147	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	148	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	149	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	150	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	0	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	1	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	2	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	3	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	4	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	5	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	6	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	7	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	8	2	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	9	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	10	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	11	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	12	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	13	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	14	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	15	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	16	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	17	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	18	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	19	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	20	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	21	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	22	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	23	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	24	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	25	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	26	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	27	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	28	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	29	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	30	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	31	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	32	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	33	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	34	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	35	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	36	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	37	10	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	38	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	39	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	40	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	41	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	42	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	43	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	44	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	45	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	46	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	47	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	48	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	49	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	50	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	51	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	52	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	53	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	54	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	55	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	56	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	57	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	58	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	59	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	60	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	61	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	62	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	63	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	64	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	65	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	66	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	67	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	68	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	69	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	70	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	71	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	72	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	73	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	74	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	75	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	76	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	77	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	78	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	79	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	80	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	81	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	82	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	83	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	84	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	85	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	86	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	87	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	88	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	89	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	90	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	91	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	92	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	93	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	94	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	95	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	96	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	97	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	98	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	99	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	100	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	101	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	102	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	103	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	104	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	105	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	106	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	107	36	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	108	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	109	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	110	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	111	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	112	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	113	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	114	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	115	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	116	13	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	117	18	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	118	14	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	119	15	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	120	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	121	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	122	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	123	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	124	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	125	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	126	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	127	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	128	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	129	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	130	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	131	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	132	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	133	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	134	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	135	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	136	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	137	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	138	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	139	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	140	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	141	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	142	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	143	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	144	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	145	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	146	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	147	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	148	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	149	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	150	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	151	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	152	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	153	12	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	154	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	155	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	156	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	157	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	158	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	159	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	160	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	161	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	162	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	163	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	164	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	165	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	166	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	167	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	168	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	169	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	170	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	171	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	172	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	173	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	174	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	175	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	176	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	177	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	178	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	179	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	180	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	181	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	182	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	183	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	184	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	185	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	186	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	187	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	188	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	189	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	190	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	191	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	192	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	193	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	194	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	195	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	196	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	197	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	198	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	199	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	200	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	201	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	202	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	203	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	204	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	205	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	206	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	207	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	208	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	209	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	210	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	211	10	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	212	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	213	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	214	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	215	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	216	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	217	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	218	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	219	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	220	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	221	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	222	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	223	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	224	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	225	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	226	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	227	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	228	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	229	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	230	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	231	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	232	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	233	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	234	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	235	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	236	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	237	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	238	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	239	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	240	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	241	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	242	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	243	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	244	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	245	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	246	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	247	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	248	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	249	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	250	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	251	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	252	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	253	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	254	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	255	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	0	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	1	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	2	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	3	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	4	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	5	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	6	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	7	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	8	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	9	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	10	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	11	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	12	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	13	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	14	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	15	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	16	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	17	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	18	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	19	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	20	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	21	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	22	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	23	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	24	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	25	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	26	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	27	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	28	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	29	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	30	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	31	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	32	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	33	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	34	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	35	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	36	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	37	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	38	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	39	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	40	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	41	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	42	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	43	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	44	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	45	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	46	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	47	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	48	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	49	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	50	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	51	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	52	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	53	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	54	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	55	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	56	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	57	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	58	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	59	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	60	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	61	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	62	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	63	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	64	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	65	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	66	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	67	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	68	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	69	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	70	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	71	8	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	72	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	73	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	74	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	75	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	76	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	77	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	78	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	79	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	80	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	81	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	82	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	83	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	84	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	85	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	86	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	87	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	88	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	89	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	90	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	91	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	92	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	93	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	94	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	95	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	96	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	97	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	98	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	99	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	100	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	101	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	102	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	103	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	104	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	105	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	106	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	107	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	108	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	109	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	110	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	111	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	112	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	113	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	114	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	115	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	116	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	117	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	118	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	119	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	120	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	121	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	122	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	123	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	124	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	125	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	126	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	127	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	128	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	129	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	130	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	131	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	132	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	133	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	134	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	135	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	136	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	137	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	138	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	139	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	140	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	141	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	142	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	143	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	144	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	145	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	146	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	147	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	148	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	149	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	150	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	151	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	152	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	153	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	154	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	155	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	156	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	157	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	158	11	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	159	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	160	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	161	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	162	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	163	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	164	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	165	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	166	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	167	11	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	168	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	169	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	170	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	171	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	172	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	173	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	174	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	175	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	176	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	177	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	178	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	179	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	180	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	181	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	182	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	183	12	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	184	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	185	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	186	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	187	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	188	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	189	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	190	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	191	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	192	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	193	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	194	4	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	195	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	196	5	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	197	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	198	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	199	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	200	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	201	8	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	202	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	203	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	204	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	205	26	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	206	3	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	207	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	208	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	209	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	210	32	Error Detect and Correct
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	211	1	Redundant
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	212	1	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	213	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	214	10	Parity
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	215	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	0	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	1	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	3	4	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	4	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	5	10	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	6	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	7	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	8	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	9	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	10	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	11	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	12	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	13	4	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	0	32	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	1	32	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	3	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	4	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	5	1	Redundant
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	6	36	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	7	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	8	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	9	2	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	10	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	11	1	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	12	10	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	13	4	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	14	3	Parity
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	15	4	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	16	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	0	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	1	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	3	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	4	36	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	5	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	6	32	Error Detect and Correct
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	7	32	Error Detect and Correct
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	8	8	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	9	8	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	10	14	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	0	32	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	1	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	3	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	4	36	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	5	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	6	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	7	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	8	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	9	2	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	10	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	11	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	12	10	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	13	5	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	14	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	15	4	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	16	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	0	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	1	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	3	36	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	4	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	0	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	1	32	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	2	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	3	1	Redundant
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	4	36	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	5	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	6	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	7	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	8	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	9	2	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	10	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	11	1	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	12	10	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	13	5	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	14	3	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	15	4	Parity
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	16	2	Parity
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	0	1	Redundant
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	1	1	Parity
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	2	4	Parity
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	3	10	Parity
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	4	32	Error Detect and Correct
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	0	32	Parity
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	1	32	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	2	1	Redundant
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	3	1	Parity
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	4	4	Parity
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	5	12	Parity
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	6	4	Parity
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	7	32	Error Detect and Correct
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	0	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	1	15	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	2	1	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	3	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	4	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	5	1	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	6	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	7	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	8	2	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	9	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	10	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	11	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	12	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	13	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	14	12	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	15	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	16	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	17	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	18	10	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	19	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	20	12	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	21	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	22	1	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	23	4	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	24	7	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	25	2	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	26	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	27	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	28	26	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	29	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	30	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	31	26	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	32	3	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	33	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	34	1	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	35	1	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	36	32	Error Detect and Correct
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	37	1	Redundant
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	38	1	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	39	10	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	40	10	Parity
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	41	1	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	0	1	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	1	1	Redundant
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	2	1	Redundant
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	3	1	Redundant
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	4	12	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	5	3	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	6	3	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	7	1	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	8	1	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	9	2	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	10	3	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	11	1	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	12	10	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	13	5	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	14	3	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	15	4	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	16	2	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	17	12	Parity
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	18	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	0	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	1	10	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	2	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	3	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	4	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	5	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	6	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	7	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	8	2	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	9	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	10	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	11	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	12	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	13	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	14	12	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	15	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	16	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	17	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	18	10	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	19	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	20	12	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	21	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	22	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	23	4	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	24	7	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	25	2	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	26	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	27	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	28	26	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	29	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	30	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	31	26	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	32	3	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	33	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	34	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	35	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	36	32	Error Detect and Correct
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	37	1	Redundant
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	38	1	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	39	10	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	40	10	Parity
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	41	1	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	0	1	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	1	1	Redundant
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	2	1	Redundant
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	3	1	Redundant
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	4	10	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	5	3	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	6	3	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	7	1	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	8	1	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	9	2	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	10	3	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	11	1	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	12	10	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	13	5	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	14	3	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	15	4	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	16	2	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	17	10	Parity
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	18	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	0	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	1	1	Redundant

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	2	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	3	4	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	4	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	5	10	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	6	1	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	7	1	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	8	1	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	9	1	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	10	2	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	11	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	12	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	13	4	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	0	32	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	1	32	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	2	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	3	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	4	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	5	1	Redundant
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	6	36	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	7	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	8	3	Parity

Table 4-258. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	9	2	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	10	3	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	11	1	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	12	10	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	13	4	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	14	2	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	15	4	Parity
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	16	1	Parity
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	0	1	Redundant
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	1	32	Error Detect and Correct
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	2	1	Parity
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	3	10	Parity
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	4	4	Parity
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	5	3	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	0	24	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	2	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	3	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	4	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	5	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	7	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	9	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	11	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	12	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	13	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	14	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	15	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	16	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	17	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	19	1	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	21	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	22	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	23	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	24	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	25	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	26	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	27	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	28	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	29	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	30	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	31	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	32	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	33	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	34	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	35	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	36	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	37	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	38	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	39	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	40	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	41	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	42	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	43	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	44	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	45	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	46	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	47	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	48	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	49	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	50	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	51	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	52	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	53	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	54	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	55	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	56	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	57	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	58	7	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	59	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	60	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	61	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	62	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	63	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	64	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	65	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	66	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	67	4	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	68	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	0	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	2	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	3	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	4	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	5	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	6	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	7	23	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	8	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	11	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	12	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	13	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	14	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	15	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	16	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	17	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	19	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	21	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	22	9	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	23	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	24	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	25	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	26	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	27	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	28	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	29	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	30	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	31	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	32	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	33	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	34	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	35	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	36	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	37	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	38	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	39	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	40	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	41	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	42	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	43	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	44	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	45	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	46	1	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	47	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	48	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	49	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	50	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	51	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	52	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	53	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	54	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	55	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	56	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	57	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	58	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	59	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	60	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	61	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	62	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	63	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	64	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	0	24	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	1	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	2	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	3	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	4	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	5	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	7	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	9	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	11	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	12	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	13	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	14	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	15	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	16	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	17	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	18	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	19	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	20	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	21	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	22	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	23	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	24	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	25	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	26	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	27	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	28	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	29	1	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	30	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	31	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	32	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	33	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	34	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	35	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	36	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	37	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	38	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	39	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	40	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	41	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	42	8	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	43	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	44	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	45	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	46	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	47	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	48	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	49	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	50	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	51	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	52	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	53	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	54	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	55	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	56	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	57	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	58	7	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	59	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	60	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	61	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	62	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	63	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	64	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	65	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	66	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	67	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	68	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC	3	0	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC	3	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC	3	2	11	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC	3	3	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	0	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	2	36	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	3	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	4	3	Parity

Table 4-259. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	5	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	6	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	7	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	8	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	9	1	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	10	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	11	5	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	12	3	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	13	4	Parity
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	14	2	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_DST_BUSECC	5	0	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_DST_BUSECC	5	1	1	Redundant
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_DST_BUSECC	5	2	10	Parity
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_DST_BUSECC	5	3	3	Parity
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	0	1	Redundant
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	1	32	Error Detect and Correct
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	2	1	Parity
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	3	10	Parity
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	4	4	Parity
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	5	3	Parity

Table 4-260. EDC Checkers Information of ECC Aggregator Instance MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CTRL_EDC_VBUSS	1	0	32	Parity

Table 4-261. EDC Checkers Information of ECC Aggregator Instance MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CTRL_EDC_VBUSS	1	0	32	Parity

Table 4-262. EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	0	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	1	12	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	2	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	3	10	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	4	18	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	5	2	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	6	3	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	7	12	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	8	4	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	9	3	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	10	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	11	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	12	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	13	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	14	10	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	15	1	Parity

Table 4-262. EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	16	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	17	4	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	18	8	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	19	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	20	32	Error Detect and Correct
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	21	32	Error Detect and Correct
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	22	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	23	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	24	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	25	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	26	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	27	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	28	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	29	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	30	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	31	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	32	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	33	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	34	20	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	35	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	36	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	37	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	38	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	39	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	40	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	41	8	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	42	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	43	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	44	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	45	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	46	56	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	47	22	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	48	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	49	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	50	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	51	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	52	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	53	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	54	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	55	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	56	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	57	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	58	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	59	30	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	60	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	61	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	62	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	63	64	Parity

Table 4-262. EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	64	36	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	0	1	Redundant
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	1	32	Error Detect and Correct
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	2	1	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	3	10	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	4	4	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	5	3	Parity

Table 4-263. EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K1_MSRAM32KX64E_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	0	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	1	12	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	2	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	3	10	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	4	18	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	5	2	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	6	3	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	7	12	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	8	4	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	9	3	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	10	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	11	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	12	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	13	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	14	10	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	15	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	16	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	17	4	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	18	8	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	19	1	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	20	32	Error Detect and Correct
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	21	32	Error Detect and Correct
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	22	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	23	1	Redundant
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	24	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	25	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	26	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	27	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	28	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	29	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	30	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	31	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	32	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	33	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	34	20	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	35	58	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	36	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	37	64	Parity

Table 4-263. EDC Checkers Information of ECC Aggregator Instance MCU_MSRAM_256K1_MSRAM32KX64E_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	38	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	39	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	40	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	41	8	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	42	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	43	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	44	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	45	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	46	56	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	47	22	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	48	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	49	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	50	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	51	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	52	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	53	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	54	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	55	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	56	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	57	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	58	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	59	30	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	60	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	61	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	62	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	63	64	Parity
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	64	36	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	0	1	Redundant
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	1	32	Error Detect and Correct
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	2	1	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	3	10	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	4	4	Parity
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	5	3	Parity

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CPU0_VBUSM2AXI_EDC	28	0	1	Redundant
CPU0_VBUSM2AXI_EDC	28	1	12	Parity
CPU0_VBUSM2AXI_EDC	28	2	4	Parity
CPU0_VBUSM2AXI_EDC	28	3	12	Parity
CPU0_VBUSM2AXI_EDC	28	4	23	Parity
CPU0_VBUSM2AXI_EDC	28	5	1	Parity
CPU0_VBUSM2AXI_EDC	28	6	10	Parity
CPU0_VBUSM2AXI_EDC	28	7	2	Parity
CPU0_VBUSM2AXI_EDC	28	8	3	Parity
CPU0_VBUSM2AXI_EDC	28	9	1	Parity
CPU0_VBUSM2AXI_EDC	28	10	2	Parity
CPU0_VBUSM2AXI_EDC	28	11	2	Parity

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CPU0_VBUSM2AXI_EDC	28	12	1	Parity
CPU0_VBUSM2AXI_EDC	28	13	1	Parity
CPU0_VBUSM2AXI_EDC	28	14	1	Parity
CPU0_VBUSM2AXI_EDC	28	15	3	Parity
CPU0_VBUSM2AXI_EDC	28	16	4	Parity
CPU0_VBUSM2AXI_EDC	28	17	2	Parity
CPU0_VBUSM2AXI_EDC	28	18	2	Parity
CPU0_VBUSM2AXI_EDC	28	19	2	Parity
CPU0_VBUSM2AXI_EDC	28	20	1	Redundant
CPU0_VBUSM2AXI_EDC	28	21	32	Error Detect and Correct
CPU0_VBUSM2AXI_EDC	28	22	32	Error Detect and Correct
CPU0_VBUSM2AXI_EDC	28	23	8	Parity
CPU0_VBUSM2AXI_EDC	28	24	1	Redundant
CPU0_VBUSM2AXI_EDC	28	25	1	Redundant
CPU0_VBUSM2AXI_EDC	28	26	10	Parity
CPU0_VBUSM2AXI_EDC	28	27	64	Parity
CPU0_VBUSM2AXI_EDC	28	28	63	Parity
CPU0_VBUSM2AXI_EDC	28	29	17	Parity
CPU0_VBUSM2AXI_EDC	28	30	10	Parity
CPU0_VBUSM2AXI_EDC	28	31	7	Parity
CPU0_VBUSM2AXI_EDC	28	32	8	Parity
CPU0_VBUSM2AXI_EDC	28	33	8	Parity
CPU0_VBUSM2AXI_EDC	28	34	64	Parity
CPU0_VBUSM2AXI_EDC	28	35	56	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	0	1	Redundant
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	1	12	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	2	1	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	3	3	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	4	10	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	5	4	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	6	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	7	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	8	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	9	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	10	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	11	48	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	12	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	13	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	14	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	15	32	Error Detect and Correct
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	16	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	17	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	18	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	19	56	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	20	2	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	21	2	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	22	1	Redundant
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	23	1	Redundant

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	24	3	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	25	10	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	26	12	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	27	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	28	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	29	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	30	38	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	31	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	32	17	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	33	8	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	34	12	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	35	64	Parity
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	36	20	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	0	1	Redundant
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	1	1	Redundant
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	2	3	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	3	32	Error Detect and Correct
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	4	32	Error Detect and Correct
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	5	4	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	6	1	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	7	1	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	8	1	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	9	2	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	10	14	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	11	1	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	12	36	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	13	10	Parity
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	14	4	Parity
SCRP_EDC	32	0	11	Parity
SCRP_EDC	32	1	1	Redundant
SCRP_EDC	32	2	32	Error Detect and Correct
SCRP_EDC	32	3	1	Redundant
SCRP_EDC	32	4	8	Parity
SCRP_EDC	32	5	4	Redundant
SCRP_EDC	32	6	3	Parity
SCRP_EDC	32	7	12	Parity
SCRP_EDC	32	8	4	Redundant
SCRP_EDC	32	9	12	Error Detect and Correct
SCRP_EDC	32	10	2	Parity
SCRP_EDC	32	11	32	Parity
SCRP_EDC	32	12	4	Parity
SCRP_EDC	32	13	3	Parity
SCRP_EDC	32	14	12	Parity
SCRP_EDC	32	15	4	Parity
SCRP_EDC	32	16	1	Redundant
SCRP_EDC	32	17	1	Redundant
SCRP_EDC	32	18	32	Error Detect and Correct
SCRP_EDC	32	19	1	Parity

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
SCRP_EDC	32	20	32	Parity
SCRP_EDC	32	21	4	Parity
SCRP_EDC	32	22	3	Parity
SCRP_EDC	32	23	12	Parity
SCRP_EDC	32	24	4	Parity
SCRP_EDC	32	25	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	0	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	1	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	2	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	3	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	4	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	5	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	6	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	7	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	8	2	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	9	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	10	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	11	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	12	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	13	10	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	14	12	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	15	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	16	4	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	17	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	18	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	19	12	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	20	4	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	21	12	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	22	4	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	23	10	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	24	1	Redundant

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	25	12	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	26	4	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	27	12	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	28	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	29	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	30	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	31	4	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	32	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	33	5	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	34	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	35	5	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	36	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	37	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	38	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	39	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	40	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	41	5	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	42	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	43	5	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	44	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	45	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	46	8	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	47	7	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	48	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	49	4	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	50	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	51	26	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	52	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	53	3	Parity

Table 4-264. EDC Checkers Information of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	54	26	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	55	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	56	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	57	26	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	58	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	59	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	60	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	61	26	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	62	32	Error Detect and Correct
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	63	3	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	64	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	65	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	66	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	67	3	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	68	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	69	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	70	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	71	32	Error Detect and Correct
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	72	1	Redundant
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	73	1	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	74	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	75	10	Parity
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	76	1	Parity
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	0	1	Redundant
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	1	32	Error Detect and Correct
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	2	1	Parity
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	3	10	Parity
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	4	4	Parity
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	5	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_ECCAGGR_EDC_CTRL	0	0	1	Redundant

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_ECCAGGR_EDC_CTRL	0	1	32	Error Detect and Correct
DMSS_HSM_ECCAGGR_EDC_CTRL	0	2	1	Parity
DMSS_HSM_ECCAGGR_EDC_CTRL	0	3	10	Parity
DMSS_HSM_ECCAGGR_EDC_CTRL	0	4	4	Parity
DMSS_HSM_ECCAGGR_EDC_CTRL	0	5	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	0	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	1	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	2	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	3	18	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	4	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	5	6	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	6	6	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	7	18	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	8	18	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	9	18	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	10	18	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	11	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	12	16	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	13	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	14	16	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	15	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	16	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	17	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	18	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	19	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	20	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	21	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	22	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	23	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	24	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	25	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	26	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	27	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	28	10	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	29	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	30	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	31	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	32	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	33	5	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	34	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	35	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	36	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	37	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	38	12	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	39	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	40	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	41	14	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	42	8	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	43	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	44	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	45	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	46	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	47	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	48	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	49	4	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	50	32	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	51	10	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	52	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	53	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	54	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	55	4	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	56	2	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	57	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	58	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	59	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	60	8	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	61	32	Error Detect and Correct
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	62	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	63	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	64	10	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	65	10	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	66	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	67	1	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	68	3	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	69	4	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	70	2	Parity
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	71	3	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	0	3	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	1	2	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	2	58	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	3	58	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	4	64	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	5	50	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	6	58	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	7	58	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	8	56	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	9	58	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	10	64	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	11	50	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	12	64	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	13	12	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	14	2	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	15	2	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	16	8	Parity
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	17	28	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	0	1	Redundant

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	1	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	2	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	3	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	4	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	5	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	6	48	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	7	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	8	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	9	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	10	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	11	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	12	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	13	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	14	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	15	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	16	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	17	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	18	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	19	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	20	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	21	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	22	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	23	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	24	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	25	3	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	26	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	27	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	28	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	29	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	30	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	31	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	32	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	33	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	34	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	35	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	36	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	37	32	Error Detect and Correct
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	38	32	Error Detect and Correct
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	39	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	40	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	41	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	42	22	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	43	1	Redundant
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	44	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	45	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	46	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	47	1	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	48	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	49	3	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	50	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	51	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	52	32	Error Detect and Correct
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	53	32	Error Detect and Correct
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	54	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	55	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	56	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	57	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	58	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	59	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	60	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	61	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	62	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	63	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	64	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	65	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	66	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	67	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	68	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	69	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	70	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	71	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	72	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	73	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	74	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	75	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	76	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	77	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	78	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	79	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	80	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	81	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	82	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	83	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	84	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	85	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	86	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	87	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	88	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	89	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	90	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	91	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	92	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	93	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	94	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	95	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	96	12	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	97	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	98	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	99	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	100	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	101	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	102	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	103	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	104	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	105	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	106	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	107	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	108	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	109	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	110	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	111	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	112	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	113	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	114	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	115	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	116	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	117	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	118	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	119	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	120	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	121	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	122	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	123	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	124	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	125	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	126	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	127	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	128	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	129	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	130	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	131	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	132	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	133	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	134	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	135	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	136	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	137	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	138	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	139	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	140	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	141	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	142	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	143	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	144	12	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	145	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	146	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	147	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	148	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	149	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	150	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	151	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	152	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	153	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	154	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	155	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	156	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	157	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	158	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	159	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	160	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	161	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	162	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	163	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	164	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	165	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	166	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	167	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	168	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	169	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	170	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	171	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	172	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	173	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	174	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	175	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	176	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	177	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	178	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	179	9	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	180	32	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	181	2	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	182	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	183	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	184	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	185	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	186	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	187	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	188	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	189	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	190	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	191	8	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	192	1	Redundant

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	193	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	194	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	195	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	196	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	197	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	198	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	199	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	200	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	201	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	202	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	203	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	204	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	205	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	206	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	207	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	208	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	209	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	210	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	211	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	212	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	213	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	214	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	215	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	216	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	217	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	218	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	219	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	220	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	221	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	222	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	223	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	224	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	225	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	226	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	227	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	228	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	229	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	230	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	231	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	232	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	233	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	234	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	235	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	236	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	237	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	238	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	239	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	240	10	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	241	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	242	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	243	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	244	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	245	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	246	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	247	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	248	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	249	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	250	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	251	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	252	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	253	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	254	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	255	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	0	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	1	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	2	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	3	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	4	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	5	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	6	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	7	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	8	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	9	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	10	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	11	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	12	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	13	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	14	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	15	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	16	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	17	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	18	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	19	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	20	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	21	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	22	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	23	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	24	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	25	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	26	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	27	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	28	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	29	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	30	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	31	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	32	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	33	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	34	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	35	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	36	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	37	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	38	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	39	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	40	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	41	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	42	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	43	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	44	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	45	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	46	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	47	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	48	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	49	10	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	50	4	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	51	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	52	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	53	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	54	16	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	55	12	Parity
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	56	8	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	0	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	1	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	2	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	3	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	4	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	5	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	6	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	7	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	8	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	9	2	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	10	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	11	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	12	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	13	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	14	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	15	14	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	16	14	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	17	8	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	18	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	19	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	20	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	21	4	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	22	48	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	23	48	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	24	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	25	4	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	26	48	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	27	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	28	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	29	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	30	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	31	12	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	32	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	33	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	34	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	35	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	36	8	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	37	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	38	3	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	39	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	40	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	41	48	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	42	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	43	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	44	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	45	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	46	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	47	4	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	48	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	49	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	50	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	51	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	52	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	53	4	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	54	3	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	55	32	Error Detect and Correct
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	56	32	Error Detect and Correct
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	57	1	Redundant
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	58	10	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	59	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	60	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	61	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	62	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	63	1	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	64	16	Parity
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	65	32	Error Detect and Correct
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	66	32	Error Detect and Correct
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	0	24	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	1	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	2	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	3	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	4	23	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	5	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	6	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	7	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	8	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	9	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	10	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	11	9	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	12	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	13	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	14	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	15	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	16	23	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	17	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	18	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	19	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	20	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	21	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	22	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	23	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	24	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	25	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	26	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	27	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	28	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	29	9	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	30	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	31	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	32	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	33	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	34	4	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	35	9	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	36	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	37	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	38	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	39	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	40	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	41	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	42	1	Redundant
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	43	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	44	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	45	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	46	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	47	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	48	10	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	49	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	50	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	51	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	52	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	53	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	54	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	55	2	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	56	2	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	57	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	58	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	59	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	60	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	61	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	62	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	63	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	64	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	65	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	66	8	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	67	2	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	68	2	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	69	3	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	70	1	Parity
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	71	8	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	0	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	1	23	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	2	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	3	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	4	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	5	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	6	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	7	2	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	8	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	9	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	10	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	11	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	12	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	13	23	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	14	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	15	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	16	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	17	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	18	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	19	2	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	20	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	21	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	22	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	23	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	24	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	25	23	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	26	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	27	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	28	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	29	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	30	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	31	2	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	32	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	33	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	34	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	35	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	36	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	37	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	38	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	39	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	40	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	41	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	42	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	43	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	44	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	45	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	46	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	47	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	48	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	49	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	50	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	51	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	52	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	53	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	54	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	55	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	56	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	57	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	58	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	59	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	60	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	61	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	62	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	63	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	64	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	65	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	66	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	67	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	68	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	69	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	70	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	71	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	72	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	73	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	74	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	75	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	76	1	Redundant

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	77	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	78	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	79	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	80	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	81	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	82	12	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	83	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	84	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	85	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	86	7	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	87	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	88	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	89	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	90	7	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	91	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	92	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	93	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	94	7	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	95	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	96	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	97	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	98	19	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	99	26	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	100	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	101	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	102	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	103	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	104	26	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	105	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	106	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	107	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	108	19	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	109	26	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	110	5	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	111	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	112	3	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	113	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	114	26	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	115	6	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	116	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	117	4	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	118	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	119	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	120	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	121	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	122	1	Redundant
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	123	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	124	32	Error Detect and Correct

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	125	32	Error Detect and Correct
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	126	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	127	1	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	128	23	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	129	10	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	130	2	Parity
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	131	3	Parity
DMSS_HSM_IPCSS_CBASS_VD2GCLK_EDC_CTRL_0	23	0	48	Parity
DMSS_HSM_IPCSS_CBASS_VD2GCLK_EDC_CTRL_0	23	1	48	Parity
DMSS_HSM_IPCSS_CBASS_VD2GCLK_EDC_CTRL_0	23	2	48	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	0	1	Redundant
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	1	12	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	2	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	3	10	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	4	12	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	5	2	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	6	3	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	7	12	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	8	4	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	9	3	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	10	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	11	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	12	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	13	1	Redundant
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	14	10	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	15	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	16	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	17	4	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	18	8	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	19	1	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	20	32	Error Detect and Correct
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	21	32	Error Detect and Correct
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	22	1	Redundant
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	23	1	Redundant
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	24	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	25	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	26	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	27	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	28	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	29	38	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	30	54	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	31	46	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	32	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	33	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	34	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	35	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	36	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	37	64	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	38	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	39	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	40	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	41	34	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	42	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	43	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	44	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	45	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	46	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	47	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	48	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	49	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	50	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	51	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	52	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	53	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	54	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	55	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	56	34	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	57	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	58	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	59	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	60	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	61	64	Parity
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	62	36	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	0	1	Redundant
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	1	16	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	2	16	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	3	8	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	4	5	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	5	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	6	5	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	7	4	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	8	32	Error Detect and Correct
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	9	32	Error Detect and Correct
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	10	32	Error Detect and Correct
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	11	32	Error Detect and Correct
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	12	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	13	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	14	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	15	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	16	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	17	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	18	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	19	4	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	20	3	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	21	2	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	22	8	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	23	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	24	12	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	25	1	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	26	1	Redundant
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	27	1	Redundant
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	28	1	Redundant
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	29	1	Redundant
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	30	16	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	31	16	Parity
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	32	8	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	0	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	1	16	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	2	16	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	3	8	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	4	5	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	5	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	6	5	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	7	4	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	8	32	Error Detect and Correct
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	9	32	Error Detect and Correct
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	10	32	Error Detect and Correct
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	11	32	Error Detect and Correct
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	12	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	13	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	14	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	15	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	16	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	17	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	18	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	19	4	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	20	3	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	21	2	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	22	8	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	23	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	24	12	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	25	1	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	26	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	27	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	28	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	29	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	30	16	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	31	16	Parity
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	32	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	0	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	1	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	2	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	3	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	4	5	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	5	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	6	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	7	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	8	32	Error Detect and Correct
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	9	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	10	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	11	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	12	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	13	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	14	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	15	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	16	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	17	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	18	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	19	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	20	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	21	12	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	22	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	23	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	24	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	25	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	26	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	27	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	28	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	29	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	0	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	1	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	2	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	3	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	4	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	5	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	6	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	7	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	8	32	Error Detect and Correct
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	9	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	10	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	11	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	12	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	13	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	14	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	15	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	16	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	17	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	18	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	19	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	20	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	21	12	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	22	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	23	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	24	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	25	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	26	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	27	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	28	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	29	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	0	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	1	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	2	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	3	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	4	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	5	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	6	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	7	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	8	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	9	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	10	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	11	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	12	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	13	7	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	14	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	15	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	16	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	17	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	18	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	19	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	20	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	21	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	22	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	23	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	24	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	25	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	26	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	27	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	28	7	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	29	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	30	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	31	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	32	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	33	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	34	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	35	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	36	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	37	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	38	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	39	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	40	5	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	41	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	42	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	43	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	44	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	45	16	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	46	1	Redundant
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	47	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	48	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	49	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	50	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	51	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	52	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	53	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	54	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	55	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	56	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	57	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	58	7	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	59	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	60	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	61	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	62	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	63	7	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	64	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	65	7	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	66	5	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	67	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	68	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	69	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	70	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	71	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	72	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	73	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	74	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	75	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	76	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	77	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	78	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	79	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	80	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	81	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	82	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	83	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	84	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	85	4	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	86	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	87	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	88	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	89	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	90	8	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	91	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	92	2	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	93	1	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	94	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	95	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	96	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	97	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	98	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	99	3	Parity
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	100	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	0	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	1	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	2	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	3	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	4	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	5	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	6	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	7	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	8	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	9	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	10	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	11	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	12	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	13	7	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	14	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	15	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	16	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	17	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	18	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	19	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	20	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	21	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	22	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	23	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	24	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	25	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	26	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	27	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	28	7	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	29	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	30	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	31	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	32	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	33	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	34	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	35	8	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	36	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	37	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	38	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	39	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	40	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	41	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	42	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	43	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	44	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	45	16	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	46	1	Redundant
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	47	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	48	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	49	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	50	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	51	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	52	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	53	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	54	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	55	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	56	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	57	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	58	7	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	59	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	60	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	61	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	62	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	63	7	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	64	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	65	7	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	66	5	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	67	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	68	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	69	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	70	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	71	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	72	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	73	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	74	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	75	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	76	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	77	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	78	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	79	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	80	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	81	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	82	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	83	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	84	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	85	4	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	86	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	87	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	88	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	89	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	90	8	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	91	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	92	2	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	93	1	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	94	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	95	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	96	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	97	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	98	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	99	3	Parity
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	100	3	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	0	16	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	1	8	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	2	16	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	3	5	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	4	1	Redundant
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	5	4	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	6	5	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	7	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	8	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	9	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	10	10	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	11	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	12	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	13	4	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	14	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	15	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	16	32	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	17	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	18	48	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	19	2	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	20	2	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	21	2	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	22	2	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	23	5	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	24	4	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	25	12	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	26	16	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	27	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	28	1	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	29	12	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	30	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	31	3	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	32	16	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	33	16	Parity
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	34	8	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	0	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	1	8	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	2	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	3	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	4	1	Redundant
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	5	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	6	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	7	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	8	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	9	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	10	10	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	11	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	12	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	13	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	14	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	15	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	16	32	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	17	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	18	48	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	19	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	20	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	21	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	22	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	23	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	24	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	25	12	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	26	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	27	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	28	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	29	12	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	30	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	31	3	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	32	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	33	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	34	8	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	0	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	1	8	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	2	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	3	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	4	1	Redundant
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	5	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	6	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	7	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	8	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	9	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	10	10	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	11	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	12	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	13	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	14	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	15	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	16	32	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	17	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	18	48	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	19	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	20	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	21	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	22	2	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	23	5	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	24	4	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	25	12	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	26	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	27	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	28	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	29	12	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	30	1	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	31	3	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	32	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	33	16	Parity
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	34	8	Parity
DMSS_HSM_PSILSS_L2P_INTAGGR_EVT_EDC_CTRL_0	35	0	32	Parity
DMSS_HSM_PSILSS_L2P_INTAGGR_EVT_EDC_CTRL_0	35	1	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_INTAGGR_CEVT_EDC_CTRL_0	36	0	32	Parity
DMSS_HSM_PSILSS_L2P_INTAGGR_CEVT_EDC_CTRL_0	36	1	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_INTAGGR_MEVT_IN_EDC_CTRL_0	37	0	32	Parity
DMSS_HSM_PSILSS_L2P_INTAGGR_MEVT_IN_EDC_CTRL_0	37	1	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	0	16	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	1	8	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	2	16	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	3	5	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	4	1	Redundant
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	5	4	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	6	5	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	7	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	8	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	9	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	10	10	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	11	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	12	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	13	4	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	14	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	15	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	16	32	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	17	32	Error Detect and Correct
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	18	48	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	19	2	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	20	2	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	21	2	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	22	2	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	23	5	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	24	4	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	25	12	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	26	16	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	27	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	28	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	29	12	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	30	1	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	31	3	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	32	16	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	33	16	Parity
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	34	8	Parity
DMSS_HSM_PSILSS_CFG_EDC_CTRL_0	39	0	12	Parity
DMSS_HSM_PSILSS_CFG_EDC_CTRL_0	39	1	12	Parity
DMSS_HSM_PSILSS_CFG_EDC_CTRL_0	39	2	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	0	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	1	48	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	2	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	3	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	4	3	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	5	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	6	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	7	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	8	2	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	9	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	10	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	11	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	12	48	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	13	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	14	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	15	3	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	16	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	17	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	18	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	19	2	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	20	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	21	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	22	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	23	48	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	24	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	25	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	26	3	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	27	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	28	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	29	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	30	2	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	31	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	32	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	33	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	34	48	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	35	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	36	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	37	3	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	38	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	39	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	40	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	41	2	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	42	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	43	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	44	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	45	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	46	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	47	12	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	48	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	49	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	50	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	51	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	52	12	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	53	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	54	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	55	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	56	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	57	12	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	58	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	59	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	60	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	61	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	62	12	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	63	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	64	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	65	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	66	10	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	67	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	68	12	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	69	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	70	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	71	4	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	72	9	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	73	5	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	74	6	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	75	9	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	76	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	77	6	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	78	9	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	79	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	80	6	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	81	9	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	82	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	83	6	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	84	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	85	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	86	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	87	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	88	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	89	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	90	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	91	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	92	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	93	5	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	94	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	95	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	96	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	97	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	98	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	99	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	100	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	101	1	Redundant
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	102	1	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	103	10	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	104	10	Parity
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	105	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	0	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	1	32	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	2	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	3	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	4	3	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	5	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	6	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	7	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	8	2	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	9	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	10	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	11	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	12	32	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	13	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	14	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	15	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	16	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	17	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	18	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	19	2	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	20	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	21	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	22	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	23	32	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	24	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	25	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	26	3	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	27	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	28	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	29	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	30	2	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	31	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	32	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	33	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	34	32	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	35	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	36	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	37	3	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	38	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	39	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	40	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	41	2	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	42	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	43	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	44	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	45	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	46	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	47	12	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	48	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	49	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	50	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	51	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	52	12	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	53	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	54	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	55	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	56	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	57	12	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	58	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	59	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	60	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	61	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	62	12	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	63	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	64	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	65	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	66	10	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	67	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	68	12	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	69	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	70	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	71	4	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	72	9	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	73	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	74	6	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	75	9	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	76	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	77	6	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	78	9	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	79	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	80	6	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	81	9	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	82	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	83	6	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	84	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	85	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	86	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	87	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	88	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	89	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	90	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	91	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	92	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	93	5	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	94	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	95	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	96	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	97	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	98	1	Redundant
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	99	1	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	100	10	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	101	10	Parity
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	102	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	0	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	1	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	2	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	3	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	4	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	5	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	6	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	7	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	8	2	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	9	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	10	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	11	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	12	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	13	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	14	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	15	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	16	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	17	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	18	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	19	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	20	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	21	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	22	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	23	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	24	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	25	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	26	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	27	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	28	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	29	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	30	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	31	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	32	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	33	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	34	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	35	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	36	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	37	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	38	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	39	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	40	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	41	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	42	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	43	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	44	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	45	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	46	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	47	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	48	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	49	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	50	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	51	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	52	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	53	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	54	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	55	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	56	32	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	57	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	58	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	59	3	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	60	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	61	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	62	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	63	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	64	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	65	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	66	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	67	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	68	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	69	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	70	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	71	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	72	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	73	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	74	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	75	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	76	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	77	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	78	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	79	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	80	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	81	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	82	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	83	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	84	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	85	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	86	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	87	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	88	10	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	89	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	90	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	91	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	92	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	93	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	94	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	95	5	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	96	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	97	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	98	5	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	99	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	100	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	101	5	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	102	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	103	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	104	5	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	105	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	106	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	107	5	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	108	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	109	9	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	110	5	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	111	6	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	112	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	113	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	114	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	115	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	116	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	117	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	118	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	119	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	120	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	121	7	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	122	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	123	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	124	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	125	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	126	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	127	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	128	10	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	129	10	Parity
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	130	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	0	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	1	1	Redundant
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	2	32	Error Detect and Correct
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	3	1	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	4	32	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	5	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	6	2	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	7	12	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	8	4	Parity
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	9	12	Parity
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	0	1	Parity
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	1	1	Redundant
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	2	1	Redundant
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	3	1	Redundant
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	4	8	Parity
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	5	8	Parity
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	6	8	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	0	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	1	23	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	2	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	3	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	4	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	5	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	6	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	7	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	8	2	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	9	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	10	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	11	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	12	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	13	10	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	14	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	15	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	16	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	17	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	18	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	19	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	20	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	21	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	22	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	23	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	24	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	25	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	26	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	27	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	28	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	29	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	30	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	31	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	32	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	33	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	34	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	35	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	36	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	37	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	38	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	39	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	40	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	41	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	42	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	43	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	44	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	45	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	46	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	47	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	48	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	49	10	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	50	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	51	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	52	4	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	53	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	54	4	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	55	12	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	56	8	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	57	9	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	58	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	59	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	60	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	61	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	62	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	63	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	64	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	65	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	66	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	67	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	68	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	69	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	70	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	71	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	72	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	73	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	74	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	75	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	76	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	77	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	78	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	79	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	80	26	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	81	3	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	82	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	83	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	84	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	85	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	86	1	Redundant
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	87	1	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	88	10	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	89	10	Parity
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	90	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	0	48	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	1	1	Redundant
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	2	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	3	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	4	17	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	5	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	6	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	7	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	8	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	9	1	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	10	10	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	11	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	12	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	13	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	14	2	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	15	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	16	1	Redundant
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	17	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	18	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	19	22	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	20	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	21	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	22	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	23	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	24	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	25	10	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	26	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	27	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	28	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	29	2	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	30	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	31	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	32	1	Redundant
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	33	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	34	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	35	17	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	36	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	37	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	38	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	39	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	40	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	41	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	42	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	43	1	Redundant
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	44	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	45	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	46	9	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	47	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	48	3	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	49	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	50	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	51	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	52	1	Redundant
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	53	32	Error Detect and Correct
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	54	1	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	55	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	56	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	57	3	Parity

Table 4-265. EDC Checkers Information of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	58	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	59	4	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	60	12	Parity
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	61	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	0	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	1	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	2	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	3	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	4	48	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	5	2	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	6	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	7	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	8	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	9	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	10	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	11	2	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	12	8	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	13	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	14	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	15	2	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	16	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	17	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	18	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	19	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	20	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	21	8	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	22	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	23	32	Error Detect and Correct

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	24	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	25	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	26	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	27	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	28	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	29	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	30	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	31	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	32	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	33	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	34	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	35	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	36	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	37	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	38	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	39	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	40	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	41	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	42	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	43	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	44	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	45	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	46	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	47	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	48	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	49	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	50	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	51	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	52	1	Redundant

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	53	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	54	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	55	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	56	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	57	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	58	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	59	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	60	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	61	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	62	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	63	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	64	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	65	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	66	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	67	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	68	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	69	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	70	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	71	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	72	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	73	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	74	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	75	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	76	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS ECC	0	77	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	0	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	1	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	2	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	3	3	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	4	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	5	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	6	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	7	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	8	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	9	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	10	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	11	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	12	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	13	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	14	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	15	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	16	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	17	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	18	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	19	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	20	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	21	1	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	22	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	23	32	Error Detect and Correct
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	24	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	25	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	26	1	Redundant
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	27	4	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	28	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	29	12	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	30	10	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	31	3	Parity
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS ECC	1	32	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	0	1	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	1	32	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	2	1	Redundant
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	3	1	Redundant
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	4	1	Redundant
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	5	1	Redundant
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	6	1	Redundant
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	7	8	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	8	8	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	9	8	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	10	8	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	11	1	Parity
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	12	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	0	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	1	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	2	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	3	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	4	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	5	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	6	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	7	48	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	8	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	9	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	10	10	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	11	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	12	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	13	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	14	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	15	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	16	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	17	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	18	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	19	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	20	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	21	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	22	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	23	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	24	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	25	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	26	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	27	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	28	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	29	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	30	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	31	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	32	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	33	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	34	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	35	6	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	36	6	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	37	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	38	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	39	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	40	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	41	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	42	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	43	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	44	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	45	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	46	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	47	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	48	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	49	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	50	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	51	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	52	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	53	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	54	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	55	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	56	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	57	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	58	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	59	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	60	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	61	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	62	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	63	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	64	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	65	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	66	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	67	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	68	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	69	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	70	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	71	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	72	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	0	24	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	1	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	2	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	3	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	4	48	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	5	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	6	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	7	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	8	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	9	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	10	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	11	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	12	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	13	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	14	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	15	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	16	1	Redundant
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	17	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	18	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	19	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	20	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	21	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	22	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	23	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	24	10	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	25	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	26	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	27	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	28	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	29	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	30	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	31	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	32	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	33	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	34	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	35	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	36	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	37	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	38	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	39	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	40	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	41	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	42	8	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	43	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	44	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	45	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	46	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	47	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	48	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	49	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	50	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	51	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	52	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	53	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	54	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	55	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	56	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	57	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	58	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	59	3	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	60	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	61	8	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	62	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	63	4	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	64	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	65	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	66	4	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	67	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	68	9	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	69	1	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	70	5	Parity
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	71	5	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	0	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	1	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	2	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	3	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	4	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	5	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	6	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	0	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	1	32	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	2	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	3	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	4	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	5	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	6	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	7	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	8	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	9	2	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	10	3	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	11	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	12	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	13	5	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	14	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	15	4	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	16	4	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	0	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	1	32	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	2	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	3	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	4	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	5	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	6	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	7	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	8	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	9	2	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	10	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	11	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	12	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	13	5	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	14	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	15	4	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	16	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	0	24	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	1	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	2	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	3	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	4	36	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	5	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	6	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	7	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	8	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	9	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	10	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	11	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	12	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	13	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	14	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	15	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	16	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	17	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	18	10	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	19	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	20	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	21	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	22	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	23	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	24	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	25	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	26	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	27	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	28	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	29	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	30	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	31	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	32	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	33	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	34	8	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	35	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	36	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	37	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	38	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	39	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	40	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	41	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	42	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	43	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	44	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	45	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	46	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	47	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	48	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	49	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	50	5	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	51	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	52	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	53	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	54	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	55	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	56	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	57	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	58	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	59	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	60	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	61	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	62	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	63	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	64	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	65	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	66	9	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	67	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	68	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	69	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	0	24	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	1	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	2	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	3	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	4	36	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	5	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	6	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	7	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	8	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	9	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	10	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	11	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	12	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	13	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	14	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	15	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	16	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	17	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	18	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	19	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	20	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	21	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	22	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	23	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	24	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	25	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	26	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	27	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	28	3	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	29	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	30	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	31	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	32	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	33	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	34	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	35	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	36	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	37	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	38	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	39	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	40	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	41	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	42	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	43	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	44	1	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	45	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	46	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	47	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	48	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	49	2	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	50	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	51	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	52	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	53	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	54	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	55	2	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	56	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	57	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	58	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	59	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	60	3	Parity

Table 4-266. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	61	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	62	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	63	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	64	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	65	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	66	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	67	5	Parity
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	0	1	Redundant
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	1	32	Error Detect and Correct
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	2	1	Parity
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	3	10	Parity
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	4	4	Parity
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	5	3	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	0	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	1	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	2	1	Redundant
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	3	10	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	4	3	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	5	1	Parity
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	6	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	0	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	1	1	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	2	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	3	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	4	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	5	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	6	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	7	36	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	8	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	9	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	10	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	11	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	12	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	13	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	14	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	15	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	16	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	17	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	18	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	19	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	20	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	21	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	22	9	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	23	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	24	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	25	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	26	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	27	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	28	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	29	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	30	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	31	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	32	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	33	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	34	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	35	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	36	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	37	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	38	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	39	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	40	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	41	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	42	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	43	3	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	44	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	45	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	46	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	47	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	48	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	49	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	50	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	51	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	52	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	53	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	54	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	55	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	56	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	57	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	58	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	59	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	60	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	61	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	62	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	63	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	64	4	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	65	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	66	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	67	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	68	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	69	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	0	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	1	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	2	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	3	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	4	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	5	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	6	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	7	36	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	8	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	9	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	10	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	11	1	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	12	1	Redundant
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	13	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	14	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	15	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	16	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	17	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	18	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	19	10	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	20	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	21	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	22	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	23	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	24	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	25	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	26	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	27	1	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	28	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	29	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	30	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	31	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	32	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	33	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	34	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	35	6	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	36	6	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	37	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	38	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	39	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	40	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	41	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	42	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	43	8	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	44	2	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	45	2	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	46	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	47	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	48	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	49	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	50	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	51	2	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	52	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	53	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	54	3	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	55	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	56	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	57	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	58	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	59	1	Parity

Table 4-267. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	60	8	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	61	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	62	4	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	63	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	64	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	65	1	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	66	9	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	67	5	Parity
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	68	1	Parity
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	0	1	Redundant
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	1	32	Error Detect and Correct
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	2	1	Parity
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	3	10	Parity
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	4	4	Parity
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	5	3	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	0	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	1	28	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	2	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	3	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	4	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	5	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	6	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	7	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	8	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	9	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	10	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	11	4	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	12	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	13	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	14	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	15	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	16	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	17	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	18	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	19	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	20	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	21	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	22	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	23	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	24	8	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	25	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	26	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	27	8	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	28	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	29	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	30	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	31	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	32	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	33	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	34	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	35	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	36	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	37	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	38	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	39	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	40	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	41	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	42	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	43	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	44	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	45	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	46	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	47	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	48	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	49	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	50	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	51	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	52	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	53	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	54	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	55	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	56	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	57	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	58	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	59	2	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	60	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	61	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	62	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	63	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	64	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	65	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	66	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	67	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	68	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	69	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	70	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	71	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	72	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	73	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	74	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	75	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	76	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	77	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	78	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	79	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	80	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	81	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	82	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	83	14	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	84	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	85	21	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	86	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	87	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	88	30	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	89	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	90	8	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	91	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	92	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	93	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	94	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	95	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	96	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	97	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	98	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	99	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	100	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	101	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	102	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	103	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	104	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	105	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	106	31	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	107	32	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	108	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	109	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	110	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	111	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	112	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	113	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	114	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	115	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	116	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	117	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	118	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	119	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	120	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	121	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	122	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	123	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	124	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	125	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	126	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	127	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	128	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	129	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	130	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	131	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	132	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	133	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	134	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	135	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	136	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	137	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	138	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	139	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	140	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	141	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	142	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	143	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	144	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	145	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	146	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	147	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	148	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	149	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	150	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	151	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	152	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	153	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	154	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	155	3	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	156	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	157	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	158	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	159	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	160	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	161	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	162	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	163	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	164	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	165	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	166	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	167	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	168	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	169	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	170	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	171	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	172	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	173	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	174	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	175	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	176	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	177	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	178	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	179	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	180	5	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	181	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	182	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	183	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	184	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	185	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	186	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	187	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	188	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	189	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	190	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	191	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	192	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	193	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	194	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	195	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	196	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	197	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	198	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	199	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	200	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	201	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	202	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	203	12	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	204	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	205	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	206	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	207	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	208	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	209	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	210	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	211	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	212	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	213	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	214	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	215	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	216	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	217	12	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	218	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	219	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	220	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	221	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	222	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	223	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	224	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	225	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	226	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	227	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	228	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	229	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	230	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	231	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	232	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	233	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	234	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	235	8	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	236	8	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	237	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	238	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	239	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	240	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	241	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	242	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	243	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	244	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	245	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	246	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	247	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	248	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	249	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	250	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	251	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	252	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	253	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	254	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	255	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	0	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	1	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	2	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	3	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	4	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	5	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	6	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	7	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	8	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	9	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	10	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	11	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	12	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	13	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	14	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	15	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	16	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	17	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	18	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	19	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	20	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	21	7	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	22	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	23	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	24	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	25	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	26	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	27	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	28	4	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	29	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	30	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	31	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	32	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	33	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	34	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	35	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	36	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	37	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	38	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	39	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	40	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	41	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	42	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	43	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	44	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	45	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	46	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	47	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	48	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	49	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	50	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	51	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	52	6	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	53	3	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	54	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	55	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	56	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	57	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	58	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	59	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	60	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	61	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	62	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	63	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	64	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	65	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	66	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	67	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	68	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	69	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	70	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	71	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	72	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	73	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	74	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	75	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	76	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	77	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	78	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	79	2	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	80	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	81	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	82	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	83	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	84	1	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	85	32	Parity
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	86	32	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	0	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	1	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	2	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	3	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	4	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	5	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	6	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	7	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	8	12	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	9	24	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	10	6	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	11	3	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	12	3	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	13	12	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	14	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	15	3	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	16	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	17	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	18	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	19	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	20	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	21	8	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	22	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	23	5	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	24	4	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	25	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	26	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	27	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	28	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	29	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	30	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	31	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	32	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	33	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	34	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	35	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	36	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	37	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	38	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	39	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	40	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	41	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	42	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	43	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	44	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	45	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	46	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	47	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	48	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	49	7	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	50	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	51	1	Parity
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	52	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	0	32	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	1	32	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	2	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	3	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	4	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	5	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	6	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	7	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	8	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	9	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	10	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	11	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	12	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	13	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	14	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	15	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	16	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	17	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	18	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	19	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	20	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	21	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	22	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	23	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	24	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	25	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	26	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	27	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	28	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	29	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	30	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	31	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	32	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	33	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	34	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	35	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	36	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	37	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	38	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	39	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	40	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	41	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	42	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	43	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	44	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	45	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	46	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	47	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	48	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	49	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	50	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	51	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	52	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	53	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	54	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	55	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	56	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	57	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	58	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	59	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	60	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	61	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	62	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	63	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	64	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	65	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	66	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	67	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	68	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	69	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	70	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	71	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	72	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	73	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	74	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	75	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	76	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	77	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	78	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	79	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	80	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	81	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	82	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	83	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	84	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	85	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	86	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	87	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	88	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	89	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	90	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	91	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	92	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	93	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	94	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	95	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	96	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	97	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	98	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	99	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	100	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	101	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	102	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	103	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	104	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	105	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	106	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	107	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	108	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	109	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	110	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	111	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	112	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	113	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	114	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	115	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	116	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	117	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	118	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	119	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	120	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	121	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	122	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	123	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	124	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	125	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	126	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	127	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	128	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	129	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	130	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	131	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	132	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	133	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	134	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	135	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	136	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	137	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	138	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	139	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	140	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	141	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	142	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	143	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	144	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	145	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	146	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	147	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	148	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	149	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	150	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	151	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	152	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	153	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	154	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	155	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	156	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	157	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	158	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	159	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	160	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	161	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	162	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	163	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	164	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	165	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	166	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	167	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	168	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	169	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	170	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	171	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	172	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	173	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	174	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	175	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	176	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	177	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	178	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	179	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	180	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	181	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	182	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	183	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	184	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	185	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	186	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	187	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	188	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	189	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	190	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	191	2	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	192	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	193	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	194	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	195	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	196	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	197	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	198	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	199	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	200	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	201	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	202	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	203	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	204	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	205	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	206	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	207	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	208	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	209	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	210	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	211	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	212	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	213	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	214	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	215	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	216	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	217	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	218	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	219	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	220	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	221	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	222	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	223	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	224	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	225	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	226	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	227	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	228	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	229	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	230	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	231	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	232	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	233	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	234	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	235	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	236	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	237	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	238	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	239	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	240	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	241	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	242	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	243	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	244	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	245	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	246	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	247	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	248	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	249	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	250	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	251	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	252	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	253	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	254	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	255	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	0	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	1	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	2	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	3	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	4	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	5	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	6	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	7	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	8	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	9	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	10	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	11	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	12	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	13	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	14	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	15	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	16	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	17	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	18	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	19	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	20	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	21	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	22	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	23	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	24	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	25	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	26	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	27	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	28	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	29	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	30	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	31	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	32	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	33	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	34	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	35	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	36	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	37	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	38	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	39	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	40	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	41	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	42	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	43	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	44	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	45	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	46	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	47	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	48	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	49	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	50	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	51	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	52	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	53	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	54	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	55	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	56	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	57	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	58	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	59	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	60	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	61	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	62	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	63	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	64	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	65	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	66	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	67	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	68	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	69	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	70	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	71	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	72	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	73	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	74	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	75	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	76	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	77	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	78	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	79	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	80	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	81	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	82	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	83	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	84	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	85	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	86	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	87	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	88	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	89	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	90	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	91	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	92	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	93	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	94	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	95	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	96	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	97	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	98	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	99	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	100	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	101	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	102	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	103	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	104	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	105	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	106	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	107	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	108	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	109	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	110	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	111	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	112	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	113	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	114	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	115	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	116	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	117	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	118	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	119	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	120	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	121	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	122	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	123	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	124	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	125	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	126	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	127	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	128	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	129	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	130	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	131	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	132	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	133	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	134	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	135	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	136	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	137	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	138	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	139	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	140	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	141	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	142	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	143	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	144	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	145	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	146	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	147	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	148	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	149	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	150	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	151	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	152	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	153	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	154	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	155	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	156	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	157	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	158	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	159	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	160	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	161	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	162	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	163	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	164	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	165	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	166	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	167	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	168	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	169	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	170	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	171	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	172	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	173	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	174	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	175	2	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	176	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	177	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	178	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	179	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	180	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	181	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	182	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	183	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	184	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	185	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	186	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	187	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	188	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	189	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	190	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	191	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	192	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	193	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	194	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	195	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	196	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	197	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	198	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	199	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	200	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	201	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	202	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	203	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	204	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	205	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	206	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	207	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	208	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	209	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	210	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	211	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	212	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	213	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	214	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	215	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	216	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	217	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	218	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	219	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	220	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	221	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	222	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	223	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	224	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	225	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	226	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	227	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	228	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	229	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	230	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	231	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	232	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	233	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	234	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	235	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	236	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	237	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	238	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	239	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	240	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	241	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	242	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	243	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	244	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	245	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	246	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	247	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	248	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	249	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	250	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	251	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	252	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	253	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	254	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	255	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	0	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	1	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	2	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	3	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	4	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	5	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	6	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	7	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	8	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	9	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	10	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	11	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	12	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	13	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	14	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	15	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	16	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	17	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	18	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	19	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	20	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	21	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	22	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	23	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	24	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	25	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	26	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	27	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	28	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	29	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	30	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	31	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	32	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	33	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	34	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	35	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	36	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	37	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	38	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	39	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	40	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	41	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	42	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	43	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	44	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	45	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	46	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	47	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	48	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	49	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	50	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	51	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	52	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	53	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	54	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	55	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	56	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	57	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	58	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	59	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	60	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	61	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	62	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	63	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	64	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	65	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	66	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	67	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	68	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	69	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	70	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	71	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	72	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	73	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	74	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	75	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	76	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	77	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	78	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	79	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	80	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	81	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	82	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	83	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	84	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	85	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	86	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	87	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	88	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	89	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	90	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	91	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	92	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	93	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	94	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	95	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	96	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	97	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	98	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	99	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	100	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	101	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	102	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	103	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	104	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	105	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	106	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	107	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	108	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	109	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	110	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	111	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	112	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	113	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	114	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	115	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	116	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	117	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	118	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	119	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	120	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	121	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	122	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	123	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	124	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	125	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	126	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	127	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	128	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	129	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	130	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	131	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	132	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	133	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	134	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	135	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	136	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	137	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	138	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	139	2	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	140	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	141	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	142	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	143	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	144	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	145	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	146	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	147	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	148	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	149	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	150	4	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	151	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	152	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	153	3	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	154	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	155	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	156	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	157	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	158	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	159	2	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	160	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	161	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	162	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	163	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	164	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	165	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	166	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	167	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	168	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	169	1	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	170	32	Parity
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	171	32	Parity
ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL	6	0	48	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	0	1	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	1	32	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	2	1	Redundant
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	3	1	Redundant
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	4	1	Redundant
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	5	1	Redundant
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	6	1	Redundant
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	7	8	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	8	8	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	9	8	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	10	8	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	11	1	Parity
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	12	1	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	0	1	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	1	32	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	2	1	Redundant

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	3	1	Redundant
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	4	1	Redundant
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	5	1	Redundant
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	6	1	Redundant
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	7	8	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	8	8	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	9	8	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	10	8	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	11	1	Parity
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	12	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	0	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	1	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	2	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	3	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	4	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	5	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	6	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	7	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	8	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	9	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	10	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	11	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	12	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	13	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	14	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	15	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	16	9	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	17	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	18	3	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	19	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	20	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	21	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	22	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	23	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	24	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	25	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	26	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	27	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	28	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	29	17	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	30	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	31	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	32	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	33	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	34	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	35	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	36	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	37	8	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	38	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	39	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	40	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	41	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	42	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	43	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	44	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	45	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	46	15	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	47	4	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	48	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	49	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	50	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	51	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	52	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	53	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	54	8	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	55	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	56	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	57	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	58	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	59	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	60	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	61	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	62	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	63	8	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	64	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	65	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	66	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	67	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	68	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	69	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	70	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	71	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	72	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	73	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	74	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	75	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	76	12	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	77	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	78	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	79	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	80	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	81	10	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	82	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	83	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	84	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	85	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	86	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	87	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	88	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	89	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	90	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	91	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	92	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	93	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	94	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	95	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	96	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	97	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	98	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	99	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	100	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	101	2	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	102	8	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	103	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	104	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	105	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	106	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	107	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	108	1	Redundant
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	109	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	110	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	111	9	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	112	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	113	3	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	114	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	115	4	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	116	12	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	117	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	118	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	119	1	Parity
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	120	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	0	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	1	36	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	2	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	3	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	4	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	5	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	6	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	7	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	8	2	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	9	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	10	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	11	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	12	36	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	13	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	14	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	15	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	16	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	17	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	18	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	19	2	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	20	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	21	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	22	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	23	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	24	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	25	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	26	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	27	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	28	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	29	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	30	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	31	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	32	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	33	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	34	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	35	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	36	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	37	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	38	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	39	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	40	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	41	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	42	10	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	43	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	44	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	45	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	46	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	47	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	48	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	49	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	50	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	51	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	52	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	53	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	54	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	55	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	56	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	57	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	58	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	59	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	60	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	61	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	62	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	63	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	64	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	65	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	66	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	67	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	68	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	69	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	70	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	71	1	Redundant

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	72	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	73	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	74	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	75	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	76	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	77	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	78	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	79	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	80	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	81	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	82	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	83	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	84	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	85	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	86	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	87	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	88	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	89	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	90	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	91	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	92	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	93	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	94	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	95	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	96	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	97	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	98	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	99	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	100	36	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	101	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	102	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	103	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	104	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	105	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	106	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	107	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	108	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	109	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	110	15	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	111	11	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	112	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	113	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	114	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	115	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	116	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	117	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	118	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	119	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	120	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	121	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	122	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	123	36	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	124	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	125	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	126	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	127	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	128	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	129	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	130	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	131	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	132	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	133	15	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	134	11	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	135	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	136	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	137	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	138	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	139	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	140	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	141	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	142	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	143	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	144	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	145	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	146	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	147	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	148	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	149	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	150	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	151	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	152	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	153	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	154	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	155	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	156	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	157	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	158	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	159	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	160	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	161	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	162	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	163	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	164	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	165	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	166	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	167	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	168	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	169	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	170	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	171	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	172	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	173	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	174	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	175	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	176	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	177	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	178	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	179	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	180	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	181	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	182	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	183	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	184	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	185	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	186	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	187	8	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	188	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	189	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	190	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	191	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	192	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	193	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	194	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	195	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	196	9	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	197	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	198	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	199	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	200	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	201	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	202	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	203	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	204	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	205	9	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	206	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	207	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	208	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	209	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	210	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	211	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	212	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	213	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	214	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	215	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	216	19	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	217	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	218	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	219	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	220	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	221	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	222	17	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	223	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	224	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	225	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	226	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	227	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	228	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	229	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	230	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	231	17	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	232	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	233	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	234	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	235	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	236	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	237	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	238	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	239	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	240	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	241	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	242	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	243	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	244	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	245	1	Redundant

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	246	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	247	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	248	15	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	249	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	250	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	251	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	252	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	253	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	254	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	255	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	0	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	1	15	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	2	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	3	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	4	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	5	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	6	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	7	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	8	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	9	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	10	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	11	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	12	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	13	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	14	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	15	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	16	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	17	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	18	8	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	19	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	20	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	21	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	22	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	23	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	24	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	25	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	26	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	27	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	28	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	29	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	30	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	31	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	32	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	33	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	34	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	35	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	36	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	37	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	38	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	39	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	40	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	41	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	42	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	43	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	44	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	45	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	46	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	47	3	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	48	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	49	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	50	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	51	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	52	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	53	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	54	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	55	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	56	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	57	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	58	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	59	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	60	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	61	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	62	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	63	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	64	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	65	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	66	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	67	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	68	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	69	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	70	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	71	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	72	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	73	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	74	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	75	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	76	1	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	77	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	78	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	79	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	80	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	81	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	82	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	83	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	84	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	85	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	86	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	87	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	88	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	89	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	90	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	91	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	92	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	93	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	94	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	95	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	96	9	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	97	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	98	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	99	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	100	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	101	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	102	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	103	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	104	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	105	9	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	106	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	107	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	108	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	109	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	110	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	111	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	112	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	113	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	114	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	115	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	116	19	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	117	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	118	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	119	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	120	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	121	12	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	122	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	123	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	124	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	125	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	126	5	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	127	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	128	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	129	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	130	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	131	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	132	4	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	133	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	134	5	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	135	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	136	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	137	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	138	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	139	8	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	140	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	141	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	142	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	143	26	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	144	3	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	145	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	146	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	147	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	148	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	149	1	Redundant
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	150	1	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	151	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	152	10	Parity
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	153	1	Parity
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	0	1	Redundant
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	1	1	Parity
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	2	4	Parity
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	3	10	Parity
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	4	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	0	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	1	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	2	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	3	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	4	3	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	5	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	6	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	7	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	8	2	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	9	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	10	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	11	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	12	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	13	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	14	12	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	15	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	16	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	17	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	18	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	19	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	20	12	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	21	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	22	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	23	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	24	7	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	25	2	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	26	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	27	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	28	26	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	29	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	30	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	31	26	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	32	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	33	1	Redundant

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	34	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	35	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	36	32	Error Detect and Correct
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	37	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	38	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	39	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	40	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	41	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	0	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	1	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	2	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	3	1	Redundant
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	4	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	5	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	6	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	7	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	8	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	9	2	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	10	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	11	1	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	12	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	13	5	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	14	3	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	15	4	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	16	2	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	17	10	Parity
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	18	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	0	32	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	1	32	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	2	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	3	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	4	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	5	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	6	1	Redundant

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	7	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	8	36	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	9	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	10	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	11	2	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	12	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	13	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	14	10	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	15	4	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	16	2	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	17	4	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	18	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	19	1	Redundant
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	20	4	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	21	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	22	10	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	23	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	24	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	25	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	26	1	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	27	2	Parity

Table 4-268. EDC Checkers Information of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	28	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	29	3	Parity
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	30	4	Parity
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	0	1	Redundant
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	1	32	Error Detect and Correct
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	2	1	Parity
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	3	10	Parity
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	4	4	Parity
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	5	3	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	0	1	Redundant
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	1	32	Error Detect and Correct
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	2	1	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	3	10	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	4	4	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	5	3	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	0	1	Redundant
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	1	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	2	4	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	3	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	4	4	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	5	32	Error Detect and Correct
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	6	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	7	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	8	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	9	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	10	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	11	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	12	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	13	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	14	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	15	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	16	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	17	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	18	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	19	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	20	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	21	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	22	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	23	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	24	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	25	8	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	26	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	27	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	28	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	29	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	30	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	31	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	32	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	33	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	34	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	35	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	36	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	37	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	38	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	39	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	40	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	41	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	42	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	43	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	44	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	45	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	46	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	47	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	48	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	49	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	50	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	51	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	52	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	53	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	54	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	55	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	56	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	57	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	58	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	59	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	60	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	61	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	62	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	63	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	64	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	65	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	66	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	67	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	68	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	69	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	70	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	71	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	72	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	73	10	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	74	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	75	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	76	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	77	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	78	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	79	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	80	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	81	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	82	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	83	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	84	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	85	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	86	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	87	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	88	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	89	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	90	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	91	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	92	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	93	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	94	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	95	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	96	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	97	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	98	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	99	16	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	100	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	101	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	102	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	103	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	104	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	105	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	106	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	107	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	108	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	109	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	110	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	111	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	112	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	113	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	114	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	115	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	116	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	117	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	118	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	119	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	120	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	121	1	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	122	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	123	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	124	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	125	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	126	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	127	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	128	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	129	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	130	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	131	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	132	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	133	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	134	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	135	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	136	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	137	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	138	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	139	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	140	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	141	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	142	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	143	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	144	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	145	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	146	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	147	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	148	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	149	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	150	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	151	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	152	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	153	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	154	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	155	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	156	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	157	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	158	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	159	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	160	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	161	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	162	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	163	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	164	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	165	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	166	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	167	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	168	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	169	8	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	170	8	Parity
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	0	1	Redundant
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	1	1	Redundant
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	2	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	0	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	1	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	2	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	3	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	4	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	5	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	6	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	7	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	8	2	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	9	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	10	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	11	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	12	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	13	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	14	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	15	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	16	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	17	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	18	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	19	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	20	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	21	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	22	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	23	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	24	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	25	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	26	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	27	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	28	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	29	7	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	30	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	31	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	32	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	33	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	34	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	35	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	36	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	37	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	38	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	39	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	40	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	41	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	42	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	43	1	Parity

Table 4-269. EDC Checkers Information of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	44	32	Error Detect and Correct
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	45	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	46	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	47	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	48	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	49	1	Parity

Table 4-270. Properties of ECC Aggregator Instance C7X256V0_SAM62A_C7XV_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AC71_PMC_WRAP_PMC_MEMWRAP_EDC_CTRL_PARITY_0	0	EDC Interconnect See Table 4-255	Inject with error capture	No		
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_TAG_CTL_TOP_DMC_TAG_CTL_EDC_CTRL_0	1	EDC Interconnect See Table 4-255	Inject with error capture	No		
C7XV_256_DMC_WRAP_C7XV_256_DMC_CORE_DMC_DATA_RTN_DMC_DATA_RTN_EDC_CTRL_0	2	EDC Interconnect See Table 4-255	Inject with error capture	No		
DRU_R30_C_R_CORE_QUEUE_CMD_EDC_CTRL_0	3	EDC Interconnect See Table 4-255	Inject with error capture	No		
DRU_R30_C_R_CORE_RD_BUFFER_CMD_EDC_CTRL_0	4	EDC Interconnect See Table 4-255	Inject with error capture	No		
DRU_R30_C_R_CORE_CH_LOGIC_RING_MEM_RING_EDC_CTRL_0	5	EDC Interconnect See Table 4-255	Inject with error capture	No		
SAM62A_C7XV_CLEC_SRAM	6	ECC Wrapper	Inject with error capture	No	22	1 KB
C7XV_256_UMC_WRAP_C7XV_EL2_C7XV_EL2_CORE_C7XV_EL2_EDC_CTL_0	7	EDC Interconnect See Table 4-255	Inject with error capture	No		

Table 4-271. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	No	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	No	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	No	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	No	42	10 KB
CPU0_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	No	32	1 KB
CPU0_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	No	32	1 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	No	39	5 KB

Table 4-271. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	No	39	5 KB
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	No	31	496 B
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	No	31	496 B
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	No	31	496 B
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	No	31	496 B
CPU0_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	No	12	384 B
CPU0_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	No	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	No	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	No	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	No	117	3 KB
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	No	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	No	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	No	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	No	38	608 B

Table 4-272. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	No	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	No	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	No	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	No	42	10 KB
CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	No	32	1 KB
CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	No	32	1 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	No	39	5 KB

Table 4-272. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE1 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	No	39	5 KB
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	No	31	496 B
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	No	31	496 B
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	No	31	496 B
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	No	31	496 B
CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	No	12	384 B
CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	No	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	No	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	No	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	No	117	3 KB
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	No	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	No	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	No	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	No	38	608 B

Table 4-273. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE2

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU2_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	No	42	10 KB
CPU2_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	No	42	10 KB
CPU2_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	No	42	10 KB
CPU2_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	No	42	10 KB
CPU2_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	No	32	1 KB
CPU2_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	No	32	1 KB

Table 4-273. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE2 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	No	39	5 KB
CPU2_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	No	31	496 B
CPU2_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	No	31	496 B
CPU2_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	No	31	496 B
CPU2_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	No	31	496 B
CPU2_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	No	12	384 B
CPU2_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	No	117	3 KB
CPU2_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	No	117	3 KB
CPU2_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	No	117	3 KB
CPU2_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	No	117	3 KB
CPU2_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	No	38	608 B
CPU2_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	No	38	608 B
CPU2_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	No	38	608 B
CPU2_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	No	38	608 B

Table 4-274. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE3

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	No	42	10 KB
CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	No	42	10 KB
CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	No	42	10 KB

Table 4-274. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_CORE3 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	No	42	10 KB
CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	No	32	1 KB
CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	No	32	1 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	No	39	5 KB
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	No	31	496 B
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	No	31	496 B
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	No	31	496 B
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	No	31	496 B
CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	No	12	384 B
CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	No	117	3 KB
CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	No	117	3 KB
CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	No	117	3 KB
CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	No	117	3 KB
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	No	38	608 B
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	No	38	608 B
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	No	38	608 B
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	No	38	608 B

Table 4-275. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0_SAM62A_A53_512KB_WRAP_A53_DUAL_WRAP_CBA_WRAP_A53_DUAL_WRAP_CBA_COREPAC_ECC_AGGR_COREPAC

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY0_ECC_SVBUS	0	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY1_ECC_SVBUS	1	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY2_ECC_SVBUS	2	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY3_ECC_SVBUS	3	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY4_ECC_SVBUS	4	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY5_ECC_SVBUS	5	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY6_ECC_SVBUS	6	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY7_ECC_SVBUS	7	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY8_ECC_SVBUS	8	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY9_ECC_SVBUS	9	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY10_ECC_SVBUS	10	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY11_ECC_SVBUS	11	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY12_ECC_SVBUS	12	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY13_ECC_SVBUS	13	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY14_ECC_SVBUS	14	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY15_ECC_SVBUS	15	ECC Wrapper	Inject only	No	38	2 KB
A53_DUAL_U_L2_DATARAM_SPRAM_0_ECC_SVBUS	16	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_1_ECC_SVBUS	17	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_2_ECC_SVBUS	18	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_3_ECC_SVBUS	19	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_4_ECC_SVBUS	20	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_5_ECC_SVBUS	21	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_6_ECC_SVBUS	22	ECC Wrapper	Inject only	No	72	72 KB
A53_DUAL_U_L2_DATARAM_SPRAM_7_ECC_SVBUS	23	ECC Wrapper	Inject only	No	72	72 KB

Table 4-276. Properties of ECC Aggregator Instance CPSW0_CPSW_3GUSS_CORE_ECC_CPSW_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ALE_RAM	0	ECC Wrapper	Inject with error capture	No	568	4 KB
CPSW_3GU_CORE_ECC_CTRL1	1	ECC Wrapper	Inject with error capture	No	256	32 B
CPSW_3GU_CORE_ECC_CTRL2	2	ECC Wrapper	Inject with error capture	No	256	32 B
CPSW_3GU_CORE_ECC_CTRL3	3	ECC Wrapper	Inject with error capture	No	256	32 B
CPSW_3GU_CORE_ECC_CTRL4	4	ECC Wrapper	Inject with error capture	No	256	32 B
CPSW_3GU_CORE_ECC_CTRL5	5	ECC Wrapper	Inject with error capture	No	256	32 B
CPSW_3GU_CORE_ECC_CTRL6	6	ECC Wrapper	Inject with error capture	No	256	32 B

Table 4-276. Properties of ECC Aggregator Instance CPSW0_CPSW_3GUSS_CORE_ECC_CPSW_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EST_RAM	7	ECC Wrapper	Inject with error capture	No	22	704 B

Table 4-277. Properties of ECC Aggregator Instance DMASS0_DMSS_AM62A_ECCAGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
DMSS_AM62A_PKTDMA_CFG_CONFIG	0	ECC Wrapper	Inject with error capture	No	96	2 KB
DMSS_AM62A_PKTDMA_CFG_STATE	1	ECC Wrapper	Inject with error capture	No	220	1 KB
DMSS_AM62A_PKTDMA_TPCFIFO_F0	2	ECC Wrapper	Inject with error capture	No	141	3 KB
DMSS_AM62A_PKTDMA_TPCFIFO_F1	3	ECC Wrapper	Inject with error capture	No	141	3 KB
DMSS_AM62A_PKTDMA_RPCFIFO_F0	4	ECC Wrapper	Inject with error capture	No	128	2 KB
DMSS_AM62A_PKTDMA_RPCFIFO_F1	5	ECC Wrapper	Inject with error capture	No	128	2 KB
DMSS_AM62A_PKTDMA_RPCFIFO_WC	6	ECC Wrapper	Inject with error capture	No	22	792 B
DMSS_AM62A_PKTDMA_STATS_STST0	7	ECC Wrapper	Inject with error capture	No	96	348 B
DMSS_AM62A_PKTDMA_STATS_STSR0	8	ECC Wrapper	Inject with error capture	No	128	384 B
DMSS_AM62A_PKTDMA_RINGOCC_CNTR	9	ECC Wrapper	Inject with error capture	No	18	675 B
DMSS_AM62A_BCDMA_CFG_CONFIG	10	ECC Wrapper	Inject with error capture	No	86	1 KB
DMSS_AM62A_BCDMA_CFG_STATE	11	ECC Wrapper	Inject with error capture	No	400	6 KB
DMSS_AM62A_BCDMA_PCFIFO_DFIFO_F0	12	ECC Wrapper	Inject with error capture	No	128	3 KB
DMSS_AM62A_BCDMA_PCFIFO_DFIFO_F1	13	ECC Wrapper	Inject with error capture	No	128	3 KB
DMSS_AM62A_BCDMA_TPCFIFO_F0	14	ECC Wrapper	Inject with error capture	No	141	2 KB
DMSS_AM62A_BCDMA_TPCFIFO_F1	15	ECC Wrapper	Inject with error capture	No	141	2 KB
DMSS_AM62A_BCDMA_RPCFIFO_F0	16	ECC Wrapper	Inject with error capture	No	128	4 KB
DMSS_AM62A_BCDMA_RPCFIFO_F1	17	ECC Wrapper	Inject with error capture	No	128	4 KB
DMSS_AM62A_BCDMA_RPCFIFO_WC	18	ECC Wrapper	Inject with error capture	No	19	1 KB
DMSS_AM62A_BCDMA_STATS_STST0	19	ECC Wrapper	Inject with error capture	No	96	648 B
DMSS_AM62A_BCDMA_STATS_STSR0	20	ECC Wrapper	Inject with error capture	No	96	720 B
DMSS_AM62A_BCDMA_RINGOCC_CNTR	21	ECC Wrapper	Inject with error capture	No	18	369 B
DMSS_AM62A_INTAGGR_STATREG_SR_SPRAM_184X128_SWW_SR	22	ECC Wrapper	Inject with error capture	No	128	3 KB
DMSS_AM62A_INTAGGR_COMMON_IM_TPRAM_1531X34_SWW_SR	23	ECC Wrapper	Inject with error capture	No	34	6 KB
DMSS_AM62A_IPCSS_RINGACC_STRAM	24	ECC Wrapper	Inject with error capture	No	216	540 B
DMSS_AM62A_IPCSS_SEC_PROXY_BUF_STRAM	25	ECC Wrapper	Inject with error capture	No	91	865 B
DMSS_AM62A_IPCSS_SEC_PROXY_BUFRAM	26	ECC Wrapper	Inject with error capture	No	64	64 B
DMSS_AM62A_IPCSS_MSRAM_ECC0	27	ECC Wrapper	Inject with error capture	No	64	16 KB

Table 4-278. Properties of ECC Aggregator Instance ECC_AGGR1_SAM62A_SEC_MCU_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	0	EDC Interconnect See Table 4-256	Inject with error capture	No		

Table 4-279. Properties of ECC Aggregator Instance FSS0_FSS_UL_OSPI0_OSPI_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
OSPI_OSPI_WRAP_SRAM	0	ECC Wrapper	Inject with error capture	No	32	1 KB

Table 4-280. Properties of ECC Aggregator Instance GICSS0_GIC500SS_1_4_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ICB_RAMECC	0	ECC Wrapper	Inject only	Yes	16	640 B
ITE_RAMECC	1	ECC Wrapper	Inject only	Yes	58	464 B
LPI_RAMECC	2	ECC Wrapper	Inject only	Yes	26	208 B

Table 4-281. Properties of ECC Aggregator Instance MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MCANSS_MSGMEM_WRAP_MSGMEM_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	17 KB
CTRL_EDC_VBUSS	1	EDC Interconnect See Table 4-257	Inject with error capture	No		

Table 4-282. Properties of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_DST_BUSECC	0	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_SRC_BUSECC	1	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_DST_BUSECC	2	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC	3	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_DST_BUSECC	4	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_SRC_BUSECC	5	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL	6	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL	7	EDC Interconnect See Table 4-258	Inject with error capture	No		
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC	8	ECC Wrapper	Inject with error capture	No	76	38 B
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC	9	ECC Wrapper	Inject with error capture	No	76	152 B
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC	10	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC	11	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC	12	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC	13	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC	14	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC	15	EDC Interconnect See Table 4-258	Inject with error capture	No		

Table 4-282. Properties of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC	16	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	17	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC	18	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC	19	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC	20	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	21	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0	22	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1	23	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0	24	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1	25	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0	26	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1	27	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC	28	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC	29	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC	30	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC	31	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC	32	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC	33	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	34	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	35	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	36	EDC Interconnect See Table 4-258	Inject with error capture	No		

Table 4-282. Properties of ECC Aggregator Instance MCU_ECC_AGGR0_SAM62A_MCU_MCU_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	37	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	38	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	39	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC	40	EDC Interconnect See Table 4-258	Inject with error capture	No		
AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC	41	EDC Interconnect See Table 4-258	Inject with error capture	No		
SAM62A_MCU_ECC_AGGR_EDC_CTRL	42	EDC Interconnect See Table 4-258	Inject with error capture	No		

Table 4-283. Properties of ECC Aggregator Instance MCU_ECC_AGGR1_SAM62A_MCU_PULSAR_UL_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_RMST_SRC_BUSECC	0	EDC Interconnect See Table 4-259	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_SLV_DST_BUSECC	1	EDC Interconnect See Table 4-259	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_M2M_CPU0_WMST_SRC_BUSECC	2	EDC Interconnect See Table 4-259	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC	3	EDC Interconnect See Table 4-259	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_ICPU0_P2P_CPU0_PMST_SRC_BUSECC	4	EDC Interconnect See Table 4-259	Inject with error capture	No		
ISAM62A_MCU_PULSAR_UL_BR_IECC_AGGR_CFG_DST_BUSECC	5	EDC Interconnect See Table 4-259	Inject with error capture	No		
SAM62A_MCU_PULSAR_UL_ECC_AGGR_EDC_CTRL	6	EDC Interconnect See Table 4-259	Inject with error capture	No		

Table 4-284. Properties of ECC Aggregator Instance MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MCANSS_MSGMEM_WRAP_MSGMEM_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	17 KB
CTRL_EDC_VBUSS	1	EDC Interconnect See Table 4-260	Inject with error capture	No		

Table 4-285. Properties of ECC Aggregator Instance MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MCANSS_MSGMEM_WRAP_MSGMEM_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	17 KB
CTRL_EDC_VBUSS	1	EDC Interconnect See Table 4-261	Inject with error capture	No		

Table 4-286. Properties of ECC Aggregator Instance MCU_MSRAM_256K0_MSRAM32KX64E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	Yes	64	256 KB
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	EDC Interconnect See Table 4-262	Inject with error capture	No		
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	EDC Interconnect See Table 4-262	Inject with error capture	No		

Table 4-287. Properties of ECC Aggregator Instance MCU_MSRAM_256K1_MSRAM32KX64E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	Yes	64	256 KB
MSRAM32KX64E_MSRAM0_EDC_CTRL_0	1	EDC Interconnect See Table 4-263	Inject with error capture	No		
MSRAM32KX64E_ECC_AGGR_EDC_CTRL	2	EDC Interconnect See Table 4-263	Inject with error capture	No		

Table 4-288. Properties of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_ITAG_RAM0	0	ECC Wrapper	Inject only	No	28	896 B
CPU0_ITAG_RAM1	1	ECC Wrapper	Inject only	No	28	896 B
CPU0_ITAG_RAM2	2	ECC Wrapper	Inject only	No	28	896 B
CPU0_ITAG_RAM3	3	ECC Wrapper	Inject only	No	28	896 B
CPU0_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_DTAG_RAM0	8	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM1	9	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM2	10	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM3	11	ECC Wrapper	Inject only	No	28	896 B
CPU0_DDIRTY_RAM	12	ECC Wrapper	Inject only	No	28	896 B
CPU0_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_ULS_ATCM0_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_ULS_ATCM0_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_ULS_B0TCM0_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_ULS_B0TCM0_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_ULS_B1TCM0_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_ULS_B1TCM0_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
CPU0_KS_VIM_RAMECC	27	ECC Wrapper	Inject with error capture	No	30	960 B
CPU0_VBUSM2AXI_EDC	28	EDC Interconnect See Table 4-264	Inject with error capture	No		
CPU0_AXI2VBUSM_MEM_MST_RAMECC	29	ECC Wrapper	Inject with error capture	No	66	528 B

Table 4-288. Properties of ECC Aggregator Instance MCU_R5FSS0_PULSAR_ULS_CPU0_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PULSAR_ULS_MEM_MST0_EDC_CTRL_0	30	EDC Interconnect See Table 4-264	Inject with error capture	No		
PULSAR_ULS_PULSAR_AHB2VBUSP_CPU0_EDC_CTRL_0	31	EDC Interconnect See Table 4-264	Inject with error capture	No		
SCRP_EDC	32	EDC Interconnect See Table 4-264	Inject with error capture	No		
PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC	33	EDC Interconnect See Table 4-264	Inject with error capture	No		
PULSAR_ULS_CPU0_ECC_AGGR_EDC_CTRL	34	EDC Interconnect See Table 4-264	Inject with error capture	No		

Table 4-289. Properties of ECC Aggregator Instance MMCSD0_EMMCSD8SS_ECC_AGGR_RXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD8SS_SDHC_WRAP_RXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-290. Properties of ECC Aggregator Instance MMCSD0_EMMCSD8SS_ECC_AGGR_TXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD8SS_SDHC_WRAP_TXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-291. Properties of ECC Aggregator Instance MMCSD1_EMMCSD4SS_ECC_AGGR_RXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD4SS_SDHC_WRAP_RXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-292. Properties of ECC Aggregator Instance MMCSD1_EMMCSD4SS_ECC_AGGR_TXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD4SS_SDHC_WRAP_TXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-293. Properties of ECC Aggregator Instance MMCSD2_EMMCSD4SS_ECC_AGGR_RXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD4SS_SDHC_WRAP_RXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-294. Properties of ECC Aggregator Instance MMCSD2_EMMCSD4SS_ECC_AGGR_TXMEM

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD4SS_SDHC_WRAP_TXMEM	0	ECC Wrapper	Inject with error capture	No	64	4 KB

Table 4-295. Properties of ECC Aggregator Instance MSRAM_64K0_MSRAM2KX256E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM2KX256E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	Yes	256	64 KB

Table 4-296. Properties of ECC Aggregator Instance PDMA0_SAM62_PDMA_SPI_ECCAGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
SAM62_PDMA_SPI_PDMA_CORE_TF0_F0_TPRAM_60X128_SBW_SR	0	ECC Wrapper	Inject with error capture	No	128	960 B
SAM62_PDMA_SPI_PDMA_CORE_TF0_F1_TPRAM_60X128_SBW_SR	1	ECC Wrapper	Inject with error capture	No	128	960 B
SAM62_PDMA_SPI_PDMA_CORE_RF0_F0_TPRAM_60X144_SBW_SR	2	ECC Wrapper	Inject with error capture	No	144	1 KB
SAM62_PDMA_SPI_PDMA_CORE_RF0_F1_TPRAM_60X144_SBW_SR	3	ECC Wrapper	Inject with error capture	No	144	1 KB

Table 4-297. Properties of ECC Aggregator Instance PDMA1_SAM62_PDMA_UART_ECCAGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
SAM62_PDMA_UART_PDMA_CORE_TF0_F0_TPRAM_28X128_SBW_SR	0	ECC Wrapper	Inject with error capture	No	128	448 B
SAM62_PDMA_UART_PDMA_CORE_TF0_F1_TPRAM_28X128_SBW_SR	1	ECC Wrapper	Inject with error capture	No	128	448 B
SAM62_PDMA_UART_PDMA_CORE_RF0_F0_TPRAM_28X144_SBW_SR	2	ECC Wrapper	Inject with error capture	No	144	504 B
SAM62_PDMA_UART_PDMA_CORE_RF0_F1_TPRAM_28X144_SBW_SR	3	ECC Wrapper	Inject with error capture	No	144	504 B

Table 4-298. Properties of ECC Aggregator Instance PSCSS0_SAM62A_MAIN_PSC_WRAP_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_PSC_CHFW_CBASS_DST_FW_CH_VBUSP_TABLE	0	ECC Wrapper	Inject with error capture	No	78	49 B

Table 4-299. Properties of ECC Aggregator Instance PSRAMECC0_PSRAM256X32E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PSRAM256X32E_PSRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	1 KB

Table 4-300. Properties of ECC Aggregator Instance PSRAMECC1_PSRAM256X32E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PSRAM256X32E_PSRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	1 KB

Table 4-301. Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
DMSS_HSM_ECCAGGR_EDC_CTRL	0	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PKTDMA_CFG_CONFIG	1	ECC Wrapper	Inject with error capture	No	108	432 B
DMSS_HSM_PKTDMA_CFG_STATE	2	ECC Wrapper	Inject with error capture	No	256	192 B
DMSS_HSM_PKTDMA_TPCFIFO_F0	3	ECC Wrapper	Inject with error capture	No	141	212 B
DMSS_HSM_PKTDMA_TPCFIFO_F1	4	ECC Wrapper	Inject with error capture	No	141	212 B
DMSS_HSM_PKTDMA_RPCFIFO_F0	5	ECC Wrapper	Inject with error capture	No	128	384 B
DMSS_HSM_PKTDMA_RPCFIFO_F1	6	ECC Wrapper	Inject with error capture	No	128	384 B
DMSS_HSM_PKTDMA_RPCFIFO_WC	7	ECC Wrapper	Inject with error capture	No	22	132 B
DMSS_HSM_PKTDMA_STATS_STST0	8	ECC Wrapper	Inject with error capture	No	96	24 B
DMSS_HSM_PKTDMA_STATS_STSR0	9	ECC Wrapper	Inject with error capture	No	128	64 B
DMSS_HSM_PKTDMA_RINGOCC_CNTR	10	ECC Wrapper	Inject with error capture	No	18	144 B

Table 4-301. Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
DMSS_HSM_PKTDMA_EDC_CTRL_0	11	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_INTAGGR_EDC_CTRL_0	12	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_INTAGGR_STATREG_SR_SPRAM_8X128_SWW_SR	13	ECC Wrapper	Inject with error capture	No	128	128 B
DMSS_HSM_INTAGGR_COMMON_IM_TPRAM_158X34_SWW_SR	14	ECC Wrapper	Inject with error capture	No	34	672 B
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_0	15	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_RINGACC_EDC_CTRL_1	16	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_RINGACC_STRAM	17	ECC Wrapper	Inject with error capture	No	216	162 B
DMSS_HSM_IPCSS_SEC_PROXY_BUF_STRAM	18	ECC Wrapper	Inject with error capture	No	91	182 B
DMSS_HSM_IPCSS_SEC_PROXY_BUFRAM	19	ECC Wrapper	Inject with error capture	No	64	64 B
DMSS_HSM_IPCSS_SEC_PROXY_EDC_CTRL_0	20	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_CBASS_IPCSS_VBM_DST_M2M_BRIDGE_SRC_EDC_CTRL_0	21	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_CBASS_SCR_EDC_CTRL_0	22	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_CBASS_VD2GCLK_EDC_CTRL_0	23	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_IPCSS_MSRAM_ECC0	24	ECC Wrapper	Inject with error capture	No	64	4 KB
DMSS_HSM_IPCSS_MSRAM_EDC_CTRL_0	25	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_SAUL0_PSIL_SAFEG_EDC_CTRL_0	26	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_PKTDMA_STRM_SAFEG_EDC_CTRL_0	27	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_SAFEG_EDC_CTRL_0	28	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_SAFEG_EDC_CTRL_0	29	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_PKTDMA_CFGSTRM_BRIDGE_EDC_CTRL_0	30	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_PSILCFG_CFGSTRM_BRIDGE_EDC_CTRL_0	31	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_SAUL0_PSIL_EDC_CTRL_0	32	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_PKTDMA_STRM_EDC_CTRL_0	33	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_PKTDMA_CFGSTRM_EDC_CTRL_0	34	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_INTAGGR_EVT_EDC_CTRL_0	35	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_INTAGGR_CEVT_EDC_CTRL_0	36	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_INTAGGR_MEVT_IN_EDC_CTRL_0	37	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_L2P_PSILCFG_CFGSTRM_EDC_CTRL_0	38	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_CFG_EDC_CTRL_0	39	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_CBASS_DATA_SCR1_SCR_EDC_CTRL_0	40	EDC Interconnect See Table 4-265	Inject with error capture	No		

Table 4-301. Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_DMSS_ECCAGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
DMSS_HSM_PSILSS_CBASS_RESP_SCR2_SCR_EDC_CTRL_0	41	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_CBASS_ETL_SCR3_SCR_EDC_CTRL_0	42	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_PSILSS_CBASS_ETL_VD2GCLK_EDC_CTRL_0	43	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_CFG_CBASS_DMSS_CFG_P2P_BRIDGE_EDC_CTRL_0	44	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_CFG_CBASS_SCR_EDC_CTRL_0	45	EDC Interconnect See Table 4-265	Inject with error capture	No		
DMSS_HSM_CFG_CBASS_VD2GCLK_EDC_CTRL_0	46	EDC Interconnect See Table 4-265	Inject with error capture	No		

Table 4-302. Properties of ECC Aggregator Instance SA3_SS0_SA3SS_AM62A_SA_UL_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
SA3_UL_CM_PKTRAM0_ECC	0	ECC Wrapper	Inject with error capture	No	64	512 B
SA3_UL_CM_PKTRAM1_ECC	1	ECC Wrapper	Inject with error capture	No	64	512 B
SA3_UL_CM_PKA_PROG_RAM_ECC	2	ECC Wrapper	Inject with error capture	No	24	15 KB
SA3_UL_CM_ENCR_CTXRAM_BANK01_ECC	3	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_ENCR_CTXRAM_BANK23_ECC	4	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_ENCR_CTXRAM_BANK4_ECC	5	ECC Wrapper	Inject with error capture	No	256	128 B
SA3_UL_CM_AUTH_CTXRAM_BANK01_ECC	6	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_AUTH_CTXRAM_BANK23_ECC	7	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_AUTH_CTXRAM_BANK45_ECC	8	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_AUTH_CTXRAM_BANK67_ECC	9	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_AUTH_CTXRAM_BANK89_ECC	10	ECC Wrapper	Inject with error capture	No	256	256 B
SA3_UL_CM_AUTH_CTXRAM_BANK10_ECC	11	ECC Wrapper	Inject with error capture	No	256	128 B

Table 4-303. Properties of ECC Aggregator Instance USB0_USB2SS_16FFC_USB2SS_CORE_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
USB2SS_16FFC_USB2SS_CORE_AXI2VBUSM_MST_KSBUS_AXI2VBUSM_RDATA_BUFFER	0	ECC Wrapper	Inject with error capture	No	66	4 KB
USB2SS_16FFC_USB2SS_CORE_RAMS_MEM_CTRL_RAM0	1	ECC Wrapper	Inject with error capture	No	64	56 KB

Table 4-304. Properties of ECC Aggregator Instance USB1_USB2SS_16FFC_USB2SS_CORE_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
USB2SS_16FFC_USB2SS_CORE_AXI2VBUSM_MST_KSBUS_AXI2VBUSM_RDATA_BUFFER	0	ECC Wrapper	Inject with error capture	No	66	4 KB
USB2SS_16FFC_USB2SS_CORE_RAMS_MEM_CTRL_RAM0	1	ECC Wrapper	Inject with error capture	No	64	56 KB

Table 4-305. Properties of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC	0	EDC Interconnect See Table 4-266	Inject with error capture	No		

Table 4-305. Properties of ECC Aggregator Instance WKUP_ECC_AGGR0_SAM62A_DM_DM_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC	1	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC	2	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	3	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	4	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC	5	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC	6	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC	7	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	8	EDC Interconnect See Table 4-266	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC	9	EDC Interconnect See Table 4-266	Inject with error capture	No		
SAM62A_DM_ECC_AGGR_EDC_CTRL	10	EDC Interconnect See Table 4-266	Inject with error capture	No		

Table 4-306. Properties of ECC Aggregator Instance WKUP_ECC_AGGR1_SAM62A_DM_MCU_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC	0	EDC Interconnect See Table 4-267	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	1	EDC Interconnect See Table 4-267	Inject with error capture	No		
AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC	2	EDC Interconnect See Table 4-267	Inject with error capture	No		
SAM62A_DM_MCU_ECC_AGGR_EDC_CTRL	3	EDC Interconnect See Table 4-267	Inject with error capture	No		

Table 4-307. Properties of ECC Aggregator Instance WKUP_ECC_AGGR2_SAM62A_WKUP_SAFE_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	0	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	1	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	3	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	4	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2	5	EDC Interconnect See Table 4-268	Inject with error capture	No		
ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL	6	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC	7	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC	8	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC	9	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0	10	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1	11	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	12	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC	13	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	14	EDC Interconnect See Table 4-268	Inject with error capture	No		
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC	15	EDC Interconnect See Table 4-268	Inject with error capture	No		
SAM62A_WKUP_SAFE_ECC_AGGR_EDC_CTRL	16	EDC Interconnect See Table 4-268	Inject with error capture	No		

Table 4-308. Properties of ECC Aggregator Instance WKUP_PSRAMECC_8K0_PSRAM8KX32E_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PSRAM8KX32E_PSRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	32 KB

Table 4-309. Properties of ECC Aggregator Instance WKUP_R5FSS0_PULSAR_UL_CPU0_ECC_AGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_ITAG_RAM0	0	ECC Wrapper	Inject only	No	28	896 B
CPU0_ITAG_RAM1	1	ECC Wrapper	Inject only	No	28	896 B

Table 4-309. Properties of ECC Aggregator Instance WKUP_R5FSS0_PULSAR_UL_CPU0_ECC_AGGR (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_ITAG_RAM2	2	ECC Wrapper	Inject only	No	28	896 B
CPU0_ITAG_RAM3	3	ECC Wrapper	Inject only	No	28	896 B
CPU0_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_DTAG_RAM0	8	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM1	9	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM2	10	ECC Wrapper	Inject only	No	28	896 B
CPU0_DTAG_RAM3	11	ECC Wrapper	Inject only	No	28	896 B
CPU0_DDIRTY_RAM	12	ECC Wrapper	Inject only	No	28	896 B
CPU0_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_UL_ATCM0_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_UL_ATCM0_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_UL_B0TCM0_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_UL_B0TCM0_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_UL_B1TCM0_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_UL_B1TCM0_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_UL_PULSAR_KS_VIM_COMMON_CORE0_RAM	27	ECC Wrapper	Inject with error capture	No	30	960 B
PULSAR_UL_MEM_MST0_KSBUS_AXI2VBUSM_RDATA_BUFFER	28	ECC Wrapper	Inject with error capture	No	66	528 B

Table 4-310. Properties of ECC Aggregator Instance WKUP_VTM0_K3VTM_N16FFC_ECCAGGR

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	EDC Interconnect See Table 4-269	Inject with error capture	No		
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	EDC Interconnect See Table 4-269	Inject with error capture	No		
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	EDC Interconnect See Table 4-269	Inject with error capture	No		
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	EDC Interconnect See Table 4-269	Inject with error capture	No		

4.15 Debug Subsystem

4.15.1 debugss Integration

Table 4-311. DEBUGSS Module Allocations

Instance	MAIN	MCU	WKUP
DEBUGSS0	✓		

Table 4-312. Integration Attributes for debugss

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DEBUGSS0	PSC0	GP_Core_CTL	LPSC_debugss	33	ON	YES	LPSC_main_IP

Table 4-313. Reset Integration for debugss

Module Instance	Source	Description
DEBUGSS0	PSC0	DEBUGSS0 reset

Table 4-314. Hardware Requests for debugss

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	GICSS0_spi_201	GICSS0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	WKUP_R5FSS0_CORE0_intr_201	WKUP_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	MCU_R5FSS0_CORE0_cpu0_intr_201	MCU_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	C7X256V0_CLEC_gic_spi_169	C7X256V0_CLEC	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	GICSS0_spi_202	GICSS0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	WKUP_R5FSS0_CORE0_intr_202	WKUP_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	MCU_R5FSS0_CORE0_cpu0_intr_202	MCU_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	C7X256V0_CLEC_gic_spi_170	C7X256V0_CLEC	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_davdma_level_0	DMASS0_INTAGGR_0_intaggr_levi_pend_27	DMASS0_INTAGGR_0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_davdma_level_0	USB0_trace_inep_pkt_buff_avail_0	USB0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_davdma_level_0	USB1_trace_inep_pkt_buff_avail_0	USB1	DEBUGSS0 interrupt request	level

4.15.2 Debug Suspend Router Connections

Debug Suspend Router Connections are shown in Table 4-315 and Table 4-316.

Table 4-315. Debug Suspend Router Connections (Inputs)

Index	Connection
0	COMPUTE_CLUSTER0.CPU0
1	COMPUTE_CLUSTER0.CPU1
2	COMPUTE_CLUSTER0.CPU2
3	COMPUTE_CLUSTER0.CPU3
4-8	Reserved
9	C7X256V0
10-22	Reserved
23	WKUP_R5FSS0
24	MCU_R5FSS0
27-31	Reserved

Table 4-316. Debug Suspend Router Connections (Outputs)

Index	Connection
0	WKUP_GTC0
1	CPSW0
2	DMASS0
3	SA3_SS0
5-7	Reserved
8	TIMER0
9	TIMER1
10	TIMER2
11	TIMER3
12	TIMER4
13	TIMER5
14	TIMER6
15	TIMER7
16	MCU_TIMER0
17	MCU_TIMER1
18	MCU_TIMER2
19	MCU_TIMER3
20	Reserved
21	WKUP_TIMER0
22	WKUP_TIMER1
23	Reserved
24	EPWM0
25	EPWM1
26	EPWM2
27	Reserved
28	MCAN0
29	MCU_MCAN0
30	MCU_MCAN1
31	Reserved
32	MCRC64_0
33	MCU_MCRC64_0
34	Reserved
35	I2C0
36	I2C1
37	I2C2
38	I2C3
39	MCU_I2C0
40	WKUP_I2C0
41	Reserved
42	ECAP0
43	ECAP1
44	ECAP2
45	EQEP0
46	EQEP1

Table 4-316. Debug Suspend Router Connections (Outputs) (continued)

Index	Connection
47	EQEP2
48-49	Reserved
50	PDMA0
51	PDMA1
52	PDMA2
53	Reserved
54	RTI2
55	RTI3
56	RTI0
57	RTI1
58	RTI4
59	MCU_RTI0
60	WKUP_RTI0
61-63	Reserved

Chapter 5

Initialization

This chapter describes the steps for non-secure device initialization.

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5.1 Initialization Overview

Figure 5-1 is an overview of the initialization process and its steps:

- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip(s)
- **ROM code:** Responsible for finding, for downloading, and for executing the initial software (SBL)
- **Initial software:** Software that loads, prepares, and passes control to application software or to the high-level operating system (HLOS)
- **High-Level Operating System** or bare-metal application which runs on main processor(s)

Figure 5-1. Initialization Process

The first two steps in the initialization process are hardware-oriented; however, they require an understanding of the process of configuring these system interface pins (balls on the device), which have software-configurable functionality. This configuration is an essential part of the chip configuration and is application-dependent. This chapter discusses these system-interface pins, the associated configuration registers, and memory structures that are vital to the correct initialization of the device.

5.1.1 ROM Code Overview

ROM bootloader (or ROM Code) is a software that resides in a on-chip read-only memory (ROM) to assist the customer in transferring and executing their application code. The device has two ROM codes operating in tandem – the Public ROM code, and the M4 ROM code.

In order to accommodate various system scenarios, the ROM Code supports several boot modes. These boot modes can be broadly classified as:

- Host boot modes
- Memory boot modes.

During a host boot, the device is configured to receive code from a host via the selected interface. Either the host writes the application code directly into internal memory or the ROM Code receives the application code on the selected interface and stores it in internal memory.

During a memory boot, the device transfers code from non-volatile memory to internal memory for execution.

In all boot modes, the entire boot operation can be partitioned into two sections:

1. Hardware initialization phase
2. Boot process.

During initialization, the ROM Code configures the device resources (PLLs, peripherals, pins) as needed to support the boot process. The resources used depend on the boot mode requirements.

During the boot process the boot image can be loaded into device memory and executed, or executed in place, depending on the boot peripheral. M4 will perform code verification and allow, or forbid, the image execution.

Main configuration source for boot after power-up are the BOOTMODE pins sampled automatically after reset release and stored in device status registers. At ROM Code startup, these pin values are read from the registers to create the boot peripheral list and the boot configuration tables used later to initialize and startup the PLLs and boot peripherals.

5.1.2 Bootloader Modes

Table 5-1 shows the boot modes supported by ROM code.

Table 5-1. ROM Code Boot Modes

Boot Mode	Boot Media/Host	SoC Peripheral	Can be a Backup Mode?(1)	Notes
No-boot/Dev-boot	No media or host	None	N	No boot or development boot – debug modes
OSPI	OSPI flash	FSS0_OSPI0	N	On OSPI port
QSPI	QSPI flash	FSS0_OSPI0	N	On OSPI port
SPI	SPI flash	FSS0_OSPI0	Y	On OSPI port
Ethernet	External host	CPSW0	Y	In BOOTP mode. RGMII or RMII PHY
I2C	I^2C EEPROM	I2C0	Y	I2C target boot is not supported
UART	External host	UART0	Y	XMODEM protocol
MMCSD	MMCSD card	MMCSD0 (8bit) or MMCSD1 (4bit)	Y	Boot from User Data Area (UDA) in raw or file system mode
eMMC	eMMC flash	MMCSD0 (8bit)	N	Boot from boot partition
USB - target	USB boot from external host	USB0	Y	USB device mode boot using DFU (device firmware upgrade), Boot is running on USB2.0 speeds.
USB - host	USB mass storage	USB0	Y	USB2.0 host mode, boot from FAT32 filesystem
Serial Flash	Serial Flash	FSS0_OSPI0	N	On OSPI port
xSPI	xSPI flash	FSS0_OSPI0	N	On OSPI port
GPMC	NOR flash, NAND flash	GPMC0	N	CSn0 connected, 8 bit NAND flash only, 16-bit non-mux NOR flash only

(1) The peripheral can be selected also as a backup boot mode. A backup mode is tried if primary boot mode fails.

Note

Because different devices support different sets of peripherals, see the *device-specific Datasheet* to obtain the list of peripherals supported in your device.

5.1.3 Terminology

- **Boot Mode Pins:** Boot mode pins provide vital information to ROM code for boot. These pins must be properly set up before power ramp.
- **Bootstrap:** Initial software launched by the ROM code during the memory booting phase.
- **Boot Header:** Optional structure that precedes the initial software and allows the redefinition of the ROM code default settings.
- **Downloaded software:** Initial software downloaded into on-chip RAM by the ROM code during the peripheral booting phase.
- **eFuse:** A one-time programmable memory location usually set at the factory.
- **Flash loader:** Downloaded software launched by the ROM code during the preflashing stage. It also programs an image in external memories.
- **GP device:** General-purpose device (SoC) or a non-secure device.
- **Initial software:** Software executed by any of the ROM code mechanisms (memory booting or peripheral booting). Initial software is a generic term for bootstrap and downloaded software. This can be the SBL (secondary bootloader) responsible for loading an OS.
- **Memory booting:** ROM code mechanism that consists of executing initial software from external memory.

- **Controller CPU:** The Arm® Cortex® CPU for which CPU-ID is 0. It configures the multicore platform and starts the ROM code to ensure device booting from a mass storage memory (memory booting) or a peripheral interface (peripheral booting).
- **Peripheral booting:** ROM code mechanism that consists of polling selected interfaces, downloading, and executing initial software (in this case, downloaded software) in the internal RAM.
- **Preflashing:** A specific case of peripheral booting where the ROM code mechanism is used to program the external flash memory.
- **ROM Code:** or ROM bootloader (RBL), the on-chip software in device ROM that executes first and implements booting.
- **ROM Code-controlled Boot Phase:** This phase covers the sequence operations from the time the platform releases the reset to the time first user- or customer-owned software starts execution. This phase is fully controlled by the device ROM code.
- **Booting Parameter Table:** A logical structure stored in the on-chip RAM memory and contains information for the boot, such as the boot file name or an address to boot from.

5.2 Boot Process

5.2.1 Public ROM Code Architecture

The Public ROM code has the following components (see also Public ROM Code Architecture):

- Main
- Buffer manager
- X.509
- Log and Trace
- System
- Protocol
- Driver

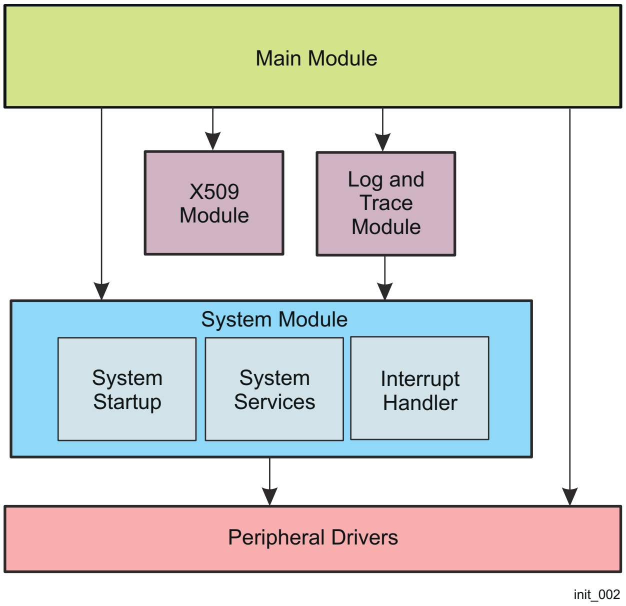

Figure 5-2. Public ROM Code Architecture

5.2.1.1 Main Module

The Main module contains the top level execution loop. This loop repeats until a boot image has been received or directed to sleep by the M4. The main loop has three different execution sub-paths based on the boot peripheral.

- **Image Path** This path is used by the OSPI, QSPI, SPI, and xSPI boot modes. In these cases the image data can be directly read by both the R5 and the M4 in place.
- **Block Path** This path is used by the I2C, USB-DFU, UART, eMMC, Ethernet, eMMC/SD cards in raw mode. In this mode data is received from the peripheral in blocks. Blocks are accumulated in the boot buffer until a full X.509 certificate header has been received, at which point this full certificate and any subsequent blocks are passed to the M4 as they arrive.
- **Filesystem Path** This path is used by the USB host (MSC) mode and eMMC/SD cards in filesystem mode. This mode executes exactly like in the block path, except that the boot image location is defined by a filesystem.

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images. In some cases, detection of an invalid image is done after the initial data buffer has been sent to the M4. In that case the R5 must inform the M4 that the image was in fact invalid and it will be looking for the next image and try again.

5.2.1.2 X509 Module

The X509 module parses the boot header. The boot header is an X.509 certificate as defined in RFC5280. Extensions specific to boot are described in Section 5.7.2 , *X.509 Certificate*.

This module also includes an OID decoder as well as defines OID values as C #define constants for any values that can be used during boot.

5.2.1.3 Buffer Manager Module

The buffer manager module is used to allocate buffers to hold boot data. The R5 code allocates a buffer when it is ready to read a block of data from the boot peripheral. Once the data is read the buffer ownership is passed to the M4. When the M4 has completed processing the data in the buffer ownership is returned to the R5, which then frees the buffer.

5.2.1.4 Log and Trace Module

The Log and Trace modules are not integral to the boot process. Instead, they provide ability to record operation of the ROM code and track unexpected occurrences.

Log and trace function is currently TI internal.

5.2.1.5 System Module

The system module provides services to other modules. These services are not directly related to boot drivers. The system module is the only module that operates in the supervisor mode of the R5 (a few services will run in user). The system module supports the following functions:

- Interrupt enable, disable, and service
- IPC
- Power
- Pinmux
- Clock
- Task switch

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images.

5.2.1.6 Protocol Module

The protocol modules provide implementation of high-level data transfer protocols. The BOOTP/TFTP and XMODEM protocols reside in this layer. These modules provide services as defined in well-known standards.

5.2.1.7 Driver Module

The driver module implements the low level peripheral drivers.

5.2.2 M4 ROM Description

In a general-purpose (GP) device, M4 ROM performs the following functions:

- Device management
- Configures the boot vectors (in BOOT_CFG) and controls reset release of R5 core. That is, M4 is the boot controller of R5 core.
- IPC configuration via Main DMSS rings and Secure Proxy
- PLL configuration (R5 and SA2UL)
- X509 certificate parsing
- SA2UL configuration to SHA512 for image integrity checks
- M4 firmware loading

5.2.3 Boot Process Flow

The R5 boot process flow is shown in Figure 5-3.

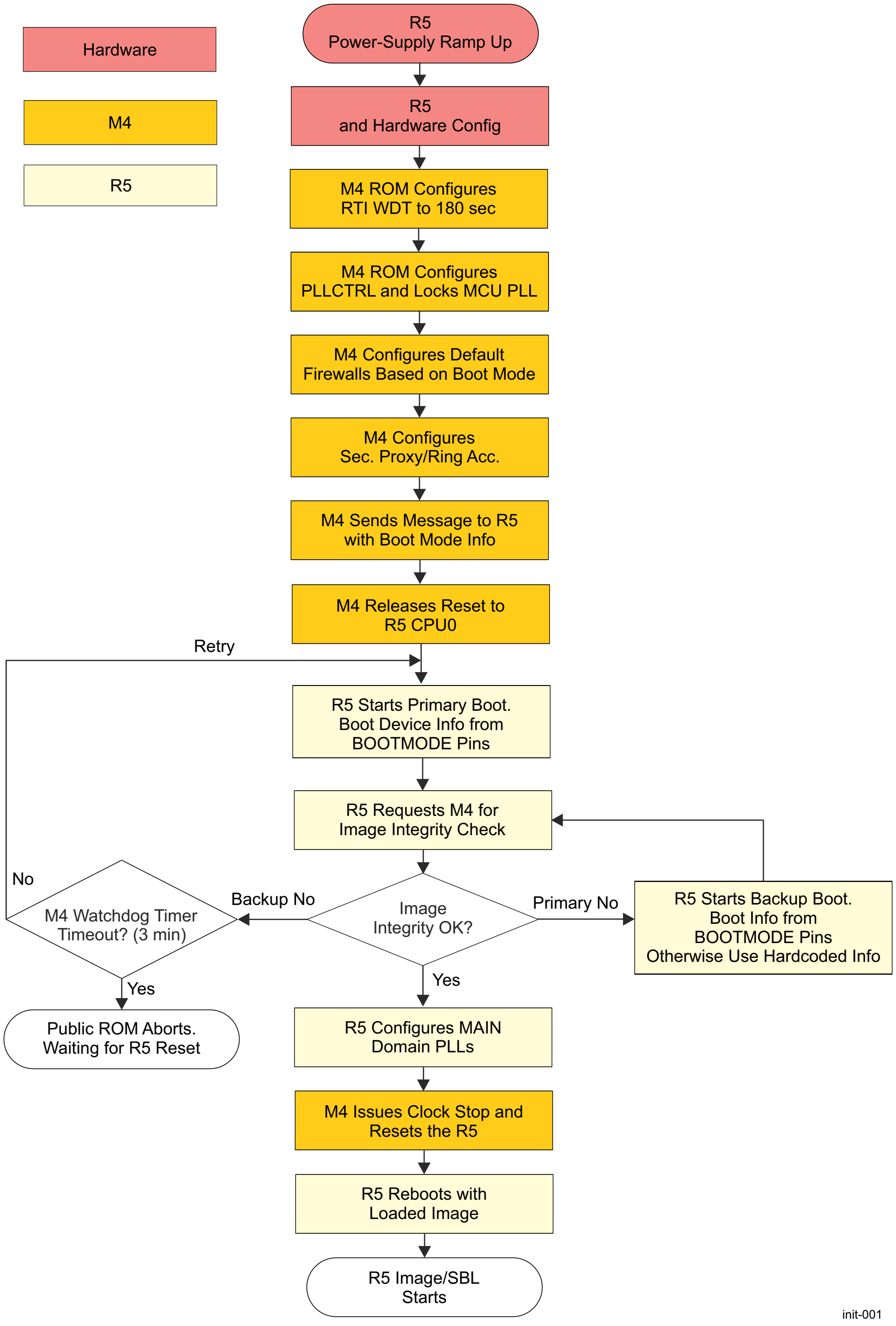

Figure 5-3. Boot Process

The values of BOOTMODE[15:0] pins are latched into the Device Status register CTRLMMR_MAIN_DEVSTAT[15:0] by hardware as the device comes out of global cold reset, sampled after MCU_PORz deassertion. For more information how to set BOOTMODE pins, see Section 5.3 , *Boot Mode Pins*.

The M4 is the boot controller for the Public ROM. M4 performs the necessary configurations and releases R5's reset for CPU0.

The R5 checks the boot mode pins and then configures the apropriate peripheral interface to get access to a boot image. A cursory check of the image is made, and the image is passed to M4. M4 ROM then will perform code verification and route the boot image to the on-chip RAM. Once the image has been received, R5 enters a clean state and idles. M4 ROM code will assert reset to the R5, redirect the boot vector to the newly loaded image, and release the reset. This restarts the R5 with the Public ROM code fully disconnected.

The Public ROM code executes after a cold or warm reset.

Note

M4 ROM sets up a 3-minute watchdog timer (RTI0) timeout. During this time, the R5 boot needs to get completed, otherwise a WDT reset will occur. Once the R5 image is loaded (SBL/SPL), M4 ROM will restart the watchdog timer for additional 3 minutes upon entering the R5 SBL. The customer-provided R5 image needs to load and install the TI-provided SYSFW image into the M4, which will manage the watchdog timer during run time.

Note

The following system conditions must be met at POR to perform device boot:

- USB cable plug must be inserted
- Ethernet PHY is powered up and out of reset
- The SD card cage must be powered before entering the SD card boot mode. A SD/MMC card with pre-loaded image must be inserted
- Memory devices must be up and ready (power ramped up and reset completed) at device startup:
  - eMMC
  - xSPI/OSPI/QSPI/SPI and Serial flash
  - I2C EEPROM
  - NOR/NAND flash

Failing to meet these requirements may result in boot fail and performing a backup boot (if available for that mode).

Figure 5-4 describes the external bootloader (SBL) typical tasks.

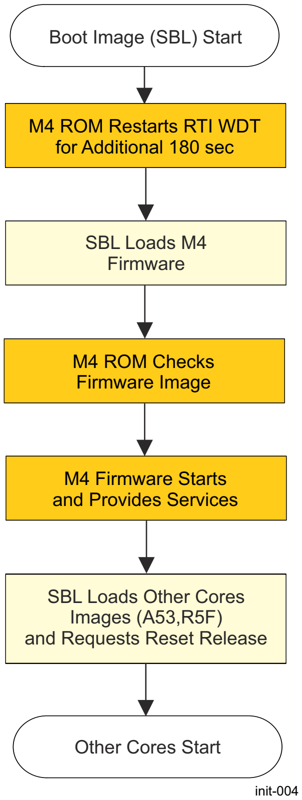

Figure 5-4. External Bootloader Tasks

Upon R5 reset and SBL execution start, M4 ROM restarts the RTI watchdog timer for additional 180 seconds of timeout. During that time, SBL must load the M4 firmware provided by TI otherwise an R5 reset will occur as a preventive measure against software misbehavior.

One of the SBL's main tasks is to load the M4 firmware. Only after this task is performed, SBL can load the other processors' image and request a reset release from M4 firmware for those cores.

5.3 Boot Mode Pins

Boot Mode pins provide means to select the boot mode and options before the device is powered up. After every POR, they are the main source to populate the Boot Parameter Tables. See Section 5.6 , *Boot Parameter Tables* for table list and description.

Boot mode pins can be divided into the following categories:

- **BOOTMODE[02:00]** – Denote system clock frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration.
- **BOOTMODE[06:03]** – Select the requested boot (primary) mode after POR, that is, the peripheral/memory to boot from.
- **BOOTMODE[09:07]** – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected.
- **BOOTMODE[12:10]** – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
- **BOOTMODE[13]** – This pin provides optional configurations for the backup boot devices.
- **BOOTMODE[15:14]** – Reserved pins.

Note

It is user's responsibility to set the boot mode pins (via pullups or pulldowns, and jumpers/switches) depending on the desired boot scenario.

5.3.1 BOOTMODE Pin Mapping

The ROM execution is directed through the main boot mode pins. This provides more flexibility and more booting peripherals to boot from. The Main domain must be powered and functional.

Main boot mode pins are shown in Table 5-2.

Any Bootmode pins marked as Reserved or not used must be tied high or low with pull resistors. They should not be left floating.

Table 5-2. BOOTMODE Pin Mapping

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

Table 5-3 describes the BOOTMODE pins that need to be set according to the system clock provided to the device.

The ROM Code will configure any PLLs required during the boot process.

Note

Reference clock selections may be limited by the device. Please consult the device specific datasheet to determine which system clock frequencies are valid.

Table 5-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	**B1**	**B0**	
0	1	1	25

5.3.1.1 Primary Boot Mode Selection and Configuration

The primary boot mode is the first mode attempted after reset. Table 5-4 lists all possible primary boot modes. All pins marked as reserved can be either 0 or 1. All boot mode signals must be pulled low or high through a pull resistor on the board, they must not be left floating

Note

All BOOTMODE[15:00] signals must be pulled high through a resistor to VDDSHV3, or pulled low to ground, including Reserved signals. Reserved BOOTMODE signals must not be left floating.

Table 5-4. Primary Boot Mode Selection

Primary Boot Mode Config							Primary Boot Mode
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	
Reserved	Read Mode 2	Read Mode 1	0	0	0	0	Serial NAND
Reserved	Reserved	Csel	0	0	0	1	OSPI
Reserved	Reserved	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
0	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot

Table 5-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Reserved	1	1	0	1	Reserved
SFDP	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	ARM/Thumb	No/Dev	1	1	1	1	No-boot/Dev boot

5.3.1.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. Table 5-5 lists all possible backup boot modes.

Table 5-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	**B12**	**B11**	**B10**	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD Boot (SD Card Boot or eMMC Boot)
Reserved	1	1	0	SPI
Reserved	1	1	1	I2C

5.4 Boot Modes

5.4.1 Boot with OSPI Controller

The following apply to all or multiple boot modes that are SPI related.

- Octal SPI flash memories support various protocols, however, the OSPI boot mode of the device will only support a specific protocol defined in OSPI Bootloader Operation. If the flash memory is complaint with JEDEC xSPI standards JESD251 and JESD216D, then xSPI boot mode is additionally supported. Please refer to xSPI boot mode description for further details.
- Command protocols follow the JEDEC spec definition and indicate the number of active pins used for the instruction, address, and data, and also the data rate used for each (S = Single Data Rate, D= Double Data Rate). For example, 1S-1S-8S describes a protocol which uses 1 signal (D0) for command in SDR mode, 1 signal (D0) for address in SDR mode, and 8 signals (D7:D0) for data in SDR mode
- When using a OSPI\xSPI\QSPI\SPI flash device greater than 128Mb which supports 3-byte and 4-byte addressing modes, a flash device package with a RESET signal (NOR type memories only) must be used. The reason is that the ROM only uses 3 byte addressing mode (address is 24bits). To address the full memory address range, software will typically switch to 4-byte addressing mode. If a reset to the processor occurs (eg, due to a warm reset), the ROM will execute expecting 3-byte addressing mode, but the flash will have been left in 4-byte addressing mode. In order for the flash device to return to 3-byte addressing mode, it must be reset using this signal. This typically can be achieved by using the RESET signal on the flash memory device. The ROM does not issue a software reset command.
  - If a flash device without a RESET signal is used, there is risk that the flash will be left in an incompatible state for the ROM after a warm reset. To mitigate this, if a warm reset is expected then the flash should be placed into a good state compatible with the ROM before the warm reset is issued. This can be done by waiting for any pending writes and erases to finish, then issuing a software reset command to the flash (if that flash device has an opcode for a software reset) or sequencing the flash to a configuration where it will be compatible with the ROM. For an expected warm reset this can be added to the overall software sequencing before the warm reset is issued.
  - An unexpected warm reset with a device that does not have RESET signal cannot be fully mitigated if the configuration after boot is not compatible with the ROM. This is a system level implication after boot and requires the system to only use the flash with settings compatible with the ROM. Most flash devices do not follow any strict standards, so this will have to be considered on a memory by memory basis for the system. Some memories have additional commands that do not require or result in modifying volatile registers to use features (like 4 byte addressing or dual data rate transfers); this means the configuration of the flash does not have to be touched to use these features and could stay ROM compatible. If these options not possible due to system limitations/requirements, then a flash device with a RESET signal should be used to fully mitigate the risk of an unexpected warm reset.
  - ROM compatible settings depend on the bootmode (xSPI/OSPI/QSPI/SPI) selected, please refer to the bootmode's specific section for details on what commands the ROM sends and the formatting they require.

5.4.1.1 OSPI Boot

Table 5-6 shows configuration pins assignment to functions when boot mode is the Octal SPI using the OSPI module.

Table 5-6. OSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 5-7 summarizes the OSPI pin configuration done by ROM code for OSPI boot device.

Table 5-7. OSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0(1)	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1(1)	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

(1) OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but OSPI boot only uses the chip select output selected via BOOTMODE[7].

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.1.1 OSPI Bootloader Operation

Please refer to Section 5.4.1 for more information that applies to OSPI boot mode

The OSPI boot mode supports 1S-1S-8S mode only. The ROM will issue a Read Command (0x8B) followed by a 24 bit (3 byte) address (the starting address is all zeros), followed by 8 dummy cycles. The flash device should then respond with 8-bit data. The frequency of operation during the read portion is 50 MHz.

5.4.1.1.1.1 OSPI Initialization Process

In the OSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the OSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See Section 5.4.1.1 , *OSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the OSPI boot parameter table and the boot configuration definitions are listed in Section 5.6.3 , *OSPI Boot Parameter Table*.

5.4.1.1.1.2 OSPI Loading Process

OSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.1.2 xSPI Boot

Table 5-8 shows configuration pins assignment to functions when boot mode is xSPI using the OSPI module.

Table 5-8. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	SFDP	0	SFDP disabled
		1	SFDP enabled
8	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

Table 5-9 summarizes the OSPI pin configuration done by ROM code for xSPI boot device on port 0.

Table 5-9. xSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0(1)	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1(1)	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

(1) Both OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but xSPI boot only uses OSPI0_CSn0. It is not possible to select OSPI0_CSn1 as a chip select option for xSPI boot.

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.2.1 xSPI Bootloader Operation

Please refer to Section 5.4.1 for more information that applies to xSPI boot mode

The xSPI protocol defines 1S-1S-1S mode for general backwards compatibility, and 8D-8D-8D for maximum throughput.

For 1S-1S-1S mode of operation, the ROM will issue a Fast Read Output command (0x0B) followed by a 24 bit (3 byte) address (the starting address is all zeros), followed by 8 dummy cycles. The frequency of operation is 50 MHz.

For 8D-8D-8D mode of operation, the ROM will issue a Fast Read command (0x0B or 0xEE, depending on BOOTMODE signal), followed by a 32 bit (4 byte) address (the starting address is all zeros). The frequency of operation will be 25MHz for device silicon revisions that are affected by errata i2420, or 20MHz for device silicon revisions which are not affected by i2420. Please refer to device specific errata documentation for more information.

When SFDP is enabled using a BOOTMODE signal, the ROM starts operation in 1S-1S-1S mode reads SFDP header from flash memory to get 8D-8D-8D switching sequence, Read Command, CMD Extension and Byte Order. SFDP parsing of ROM is described below and on successful parsing ROM will issue 8D-8D-8D command switching sequence and then will read the boot image in 8D-8D-8D mode with read command specified in SFDP header

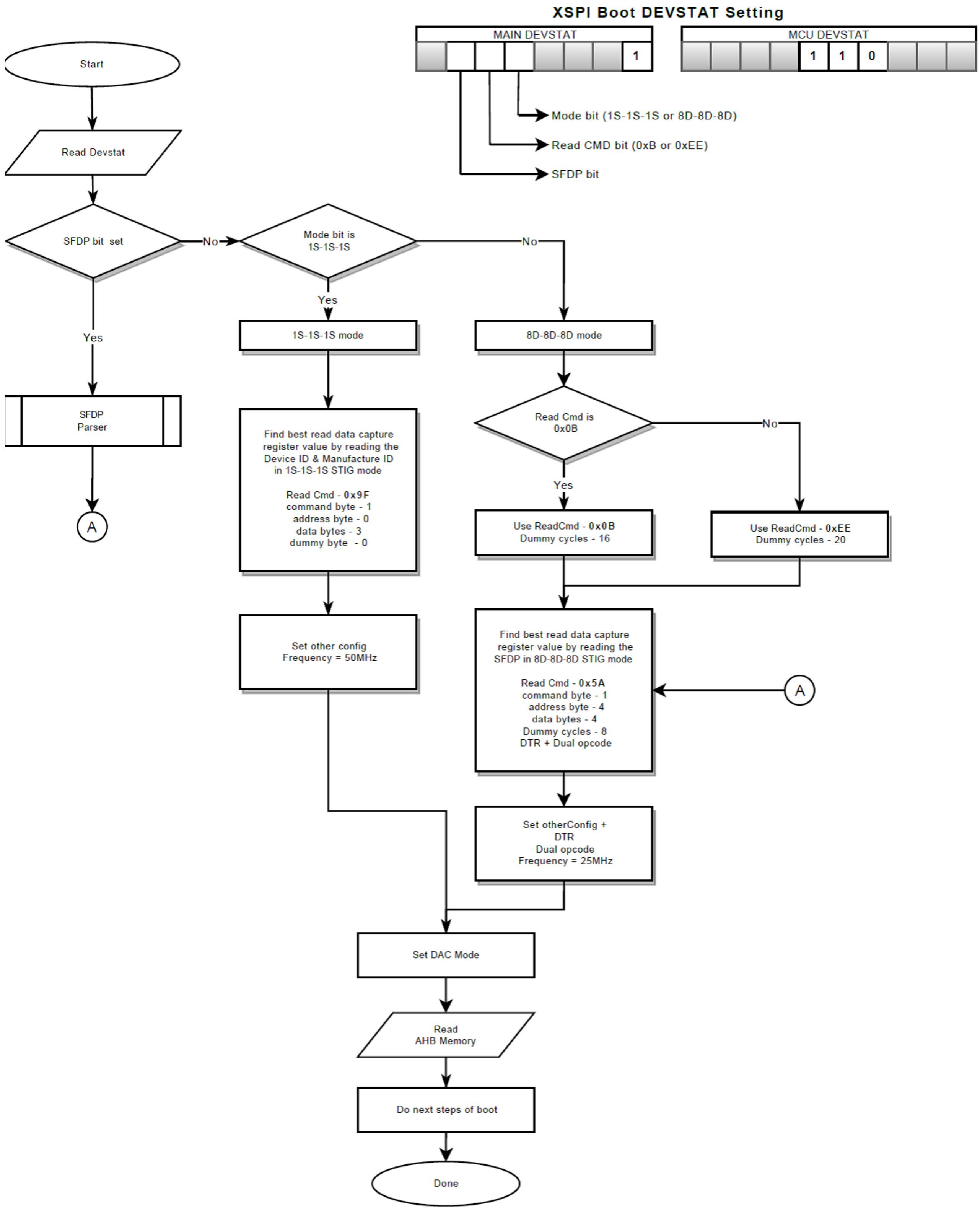

Figure 5-5. xSPI Flow Chart

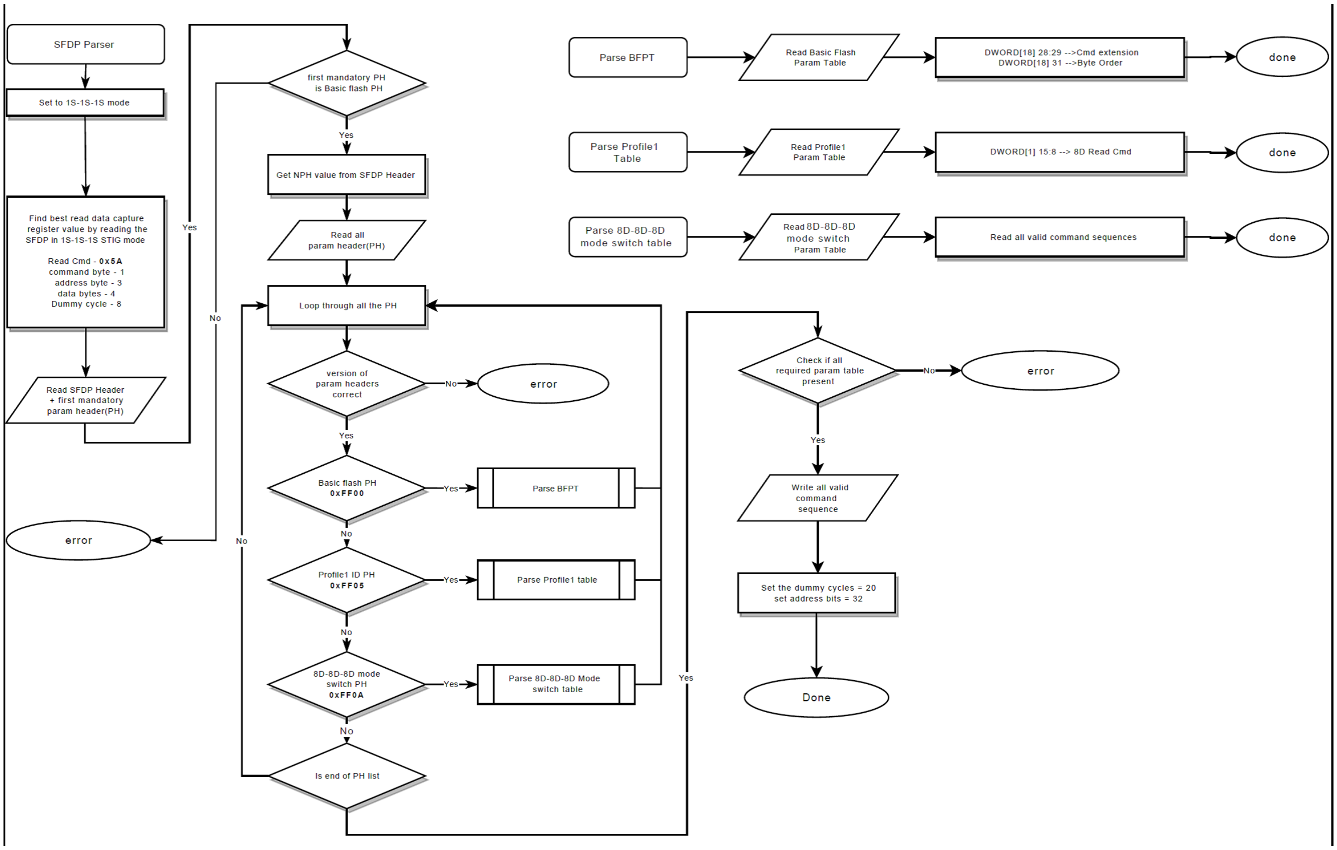

Figure 5-6. ROM SFDP Parser Flow

5.4.1.2.2 xSPI Initialization Process

In the xSPI boot mode, the ROM Code initializes the xSPI module and the image is read from the xSPI flash connected. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM.

5.4.1.3 QSPI Boot

Table 5-10 shows configuration pins assignment to functions when boot mode is QSPI using the OSPI module.

Table 5-10. QSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 5-11 summarizes the OSPI pin configuration done by ROM code for QSPI boot device on port 0.

Table 5-11. QSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Strength Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_CSn0(1)	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1(1)	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

(1) OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but QSPI boot only uses the chip select output selected via BOOTMODE[7].

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.3.1 QSPI Bootloader Operation

Please refer to Section 5.4.1 for more information that applies to QSPI boot mode

The QSPI boot mode supports the 1S-1S-4S mode only. The ROM will issue a Fast Read Quad Output command (0x6B) followed by a 24 bit (3 byte) address (the starting address is all zeros), followed by 8 dummy cycles. The flash device should then respond with 4-bit data. The frequency of operation during the quad read portion is 50 MHz.

5.4.1.3.1.1 QSPI Initialization Process

In the QSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the QSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See Section 5.4.1.3 , *QSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the QSPI boot parameter table and the boot configuration definitions are listed in Section 5.6.3 , *QSPI Boot Parameter Table*.

5.4.1.3.1.2 QSPI Loading Process

QSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.1.4 SPI Boot

Table 5-12 shows configuration pins assignment to functions when boot mode is SPI using the OSPI module.

Table 5-12. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8	Mode	0	SPI Mode 0
		1	SPI Mode 3
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 5-13 summarizes the OSPI pin configuration done by ROM code for SPI boot device on port 0.

Table 5-13. SPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_CSn0(1)	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1(1)	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

(1) OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but SPI boot only uses the chip select output selected via BOOTMODE[7].

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.4.1 SPI Bootloader Operation

Please refer to Section 5.4.1 for more information that applies to SPI boot mode

The SPI boot mode supports the 1S-1S-1S mode only. The Read Command is 8-bits (0x03) followed by a 24 bit (3 byte) address. There are no dummy cycles issued after the read command. The frequency of operation supported is 6.250 MHz. OSPI0_D0 will have data transfers **FROM** the processor **TO** the flash device, and OSPI0_D1 will have data transfers **TO** the processor **FROM** the flash device

5.4.1.4.1.1 SPI Initialization Process

In the SPI boot mode, the ROM Code initializes the OSPI peripheral to SPI mode and the image is read from the flash memory connected to the corresponding OSPI port and chip-select. A detailed summary of the SPI boot parameter table and the boot configuration definitions are listed in Section 5.6.3 , *OSPI/QSPI/SPI Boot Parameter Table*. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM.

5.4.1.4.1.2 SPI Loading Process

SPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.1.5 Serial NAND Boot

Serial NAND Configuration Fields table shows configuration pins assignment to functions when boot mode is Serial NAND.

Table 5-14. Serial NAND Configuration Fields

BOOTMODE Pins	Field	Value	Description
8	Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1
		1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)
7	Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)
		1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)

Serial NAND Pin Usage table summarizes the pin configuration done by ROM code for the Serial NAND device.

Table 5-15. Serial NAND Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0(1)	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1(1)	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

(1) Both OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but Serial NAND boot only uses OSPI0_CSn0. It is not possible to select OSPI0_CSn1 as a chip select option for Serial NAND boot.

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.5.1 Serial NAND Bootloader Operation

Serial NAND defines 1S-1S-1S mode for general backwards compatibility, and 1S-1S-8S for maximum throughput (S here means *S*ingle Data rate). Serial NAND memory array is organized into pages of size 2KB/4KB. Read is a two-step process where a complete page is first read into flash's internal buffer/cache using Page read command and then the host controller reads from internal buffer in 1- or 4- or 8-bit mode using the read commands. Page read command that is issued is 0x13, followed by 24 address bits. The frequency of operation supported is 50 MHz.

For 1S-1S-1S mode of operation (Bit-width =1, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x0B, followed by address bits and 8 dummy cycles.

For 1S-1S-8S mode of operation (Bit-width =8, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x8B, followed by address bits and 8 dummy cycles. Additionally, flash is configured in 8-bit mode after POR through volatile configuration register if the manufacturer is Winbond.

For 1S-1S-4S mode of operation (Bit-width =4, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x6B, followed by address bits and 8 dummy cycles. Note that in 8-bit mode pin mux is done for all 8 OSPI data lines and in 4-bit/1-bit mode pin mux is done for 4 OSPI data lines. This is done to disable the HOLD functionality feature in 1-bit mode.

Serial NAND boot expects ECC to be auto-managed by the flash. Most of the flashes have the ECC enabled by default and can do 1-bit correction and 2-bit detection for ECC errors. ROM checks for 2-bit ECC error via status register 3 (address 0xC0) bit 5 after every page load. In case of 2-bit ECC error the boot will fail and ROM will take the fallback option.

Serial NAND boot also manages bad blocks that can be present in the flash at time of shipment or develop during the lifetime. Bad block marker is a non-FFh data byte stored at Byte 0 of spare area of Page 0 for each bad block and ROM checks for the same while reading the first page of a memory block. ROM will skip the particular block if it is marked as bad and move to the next one.

The Serial NAND driver in ROM does not support devices that have multiple planes as they require special handling to read even numbered blocks

5.4.1.5.2 Serial NAND Initialization Process

In the OSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the OSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See Section 5.4.1.1 , *OSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the OSPI boot parameter table and the boot configuration definitions are listed in Section 5.6.3 , *OSPI Boot Parameter Table*.

5.4.1.5.3 Serial NAND Loading Process

OSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.2 I2C Boot

Table 5-16 shows configuration pins assignment to functions when boot mode is the I2C mode.

Table 5-16. I2C Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Bus reset	0	Hung bus reset attempt after 1 ms
		1	No hung bus reset attempted
7	Address	0	EEPROM's address is 0x50
		1	EEPROM's address is 0x51

The I^2C bus is considered inactive if the data line is low and clock remains high for the specified timeout time. Recovery consists of driving the clock a stop condition is detected. A stop condition is a transition on the data line from 0 to 1 while the clock line is high. If the clock line is stuck low there is no way to take control of the bus.

Table 5-17 summarizes the I2C pin configuration done by ROM code for I^2C boot device.

Table 5-17. I2C Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
I2C0_SCL	I2C0_SCL	Disable	NA	0	Enable	0	PADCONFIG120
I2C0_SDA	I2C0_SDA	Disable	NA	0	Enable	0	PADCONFIG121

5.4.2.1 I2C Bootloader Operation

5.4.2.1.1 I2C Initialization Process

In the I2C boot mode, the ROM Code configures the Main Domain I2C0 in controller mode.

The boot controller drives the I^2C target device where the image is stored. The image is copied to internal RAM, and is executed from there. If the image is not recognized, the ROM will attempt to read the image at offset 0x8000. This is the only redundant image supported by the ROM.

A detailed summary of the I^2C boot parameter table and the BOOTMODE pins definitions are listed in Section 5.6.5 , *I2C Boot Parameter Table* and Section 5.4.2 , *I2C Boot Device Configuration*.

5.4.2.1.1.1 Block Size

ROM code will read 0x800 bytes before processing the data. The last block must be padded to the next 0x800 byte boundary and it must be padded with zeros.

5.4.2.1.1.2 Addressing

The boot code does not support byte address to bus address wrapping. So the maximum image size that can be access is 64 kbytes. For example, if the read address is 0xFF00, the read size is 0x200 and the I^2C bus address is 0x50, then 0x100 bytes will be read from 0xFF00 at bus address 0x50, followed by 0x100 bytes from 0x0000 at bus address 0x50. The bus address does not increment when the address rolls over.

5.4.2.1.2 I2C Loading Process

5.4.2.1.2.1 Loading a Boot Image From EEPROM

In this mode, the Main Domain I2C0 peripheral is configured as I^2C controller.

ROM Code will start reading from the I^2C EEPROM at the specified I^2C bus address. This read will be done beginning at the specified base address offset. Data will be read in 2-KB chunks. The data will be stored at the address specified in the boot header. It will continue reading image data until a complete image has been read. When the complete image has been read, the ROM Code will branch to the start address of the image.

5.4.3 SD Card Boot

Table 5-18 shows configuration pins assignment to functions when boot mode is the SD card boot mode.

Table 5-18. SD Card Boot Configuration Fields

SD Card Boot Configuration Fields			
BOOTMODE Pins	**Field**	**Value**	**Description**
9 (13[1])	Port	0	Reserved
		1	MMC Port 1 (4 bit width). This bit must be set to 1
7	FS/Raw	0	Filesystem mode
		1	Raw Mode

[1] When MMCSD is the backup mode.

Table 5-19 summarizes the MMCSD pin configuration done by ROM code for SD Card boot on port1 (MMCSD1). SD Card boot on Port 0 (MMCSD0) is not supported.

Table 5-19. SD Card (MMCSD1) Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
MMC1_DAT3	MMC1_DAT3	Disable	NA	0	Enable	0	PADCONFIG137
MMC1_DAT2	MMC1_DAT2	Disable	NA	0	Enable	0	PADCONFIG138
MMC1_DAT1	MMC1_DAT1	Disable	NA	0	Enable	0	PADCONFIG139
MMC1_DAT0	MMC1_DAT0	Disable	NA	0	Enable	0	PADCONFIG140
MMC1_CLK	MMC1_CLK	Disable	NA	0	Enable	0	PADCONFIG141
MMC1_CLKLB	MMC1_CLKLB	Disable	NA	0	Enable	0	PADCONFIG142
MMC1_CMD	MMC1_CMD	Disable	NA	0	Enable	0	PADCONFIG143
MMC1_SDCD	MMC1_SDCD	Disable	NA	0	Enable	0	PADCONFIG144

Note

MMC1_CLKLB signal is not pinned out on the device. The pinmux configuration enables the input buffer of the internal loopback clock.

Note

MMC1_SDWP is not configured by ROM since the ROM never writes to the SD card.

5.4.3.1 SD Card Bootloader Operation

SD Card boot is only available on Port 1 of the MMCSD controller (MMCSD1). The ROM will boot from SD cards using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode

The ROM is capable of booting from any size SD card because the MMCSD controller is responsible for addressing. Only single data rate with backward compatible interface timing is supported.

The MMCSD module depends on proper voltage level on the SD card detect signal (SDCD). If SDCD=1, the ROM will assume the card is not present and will fail the boot mode.The SDCD must be 0 for the ROM to continue to attempt to boot. Card detect using DAT3 is not supported. If the card is detected, the initial discovery phase is performed:

1. Send CMD 0. (GO IDLE, both for MMC and SD)

2. Send CMD 55. If the card responds then the card type is assumed to be SD. On timeout the code sends CMD 1. If there is a response then the card type is MMC.

The ROM Code will start reading from the MMCSD memory boot sector, or filesystem, as specified by the BOOTMODE pin (FS/Raw). Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When SD Card boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

5.4.4 eMMC Boot

Table 5-20 shows configuration pins assignment to functions when boot mode is the eMMC Boot using a UDA boot mode (BOOTMODE[6:3]=1000b). Note that eMMC Boot using alternate eMMC Boot (BOOTMODE[6:3]=1001b) does not have any extra bootmode configuration fields. See Section 5.4.4.1 for more information.

Table 5-20. eMMC Boot Configuration Fields (UDA mode)

eMMC Boot Configuration Fields			
BOOTMODE Pins	**Field**	**Value**	**Description**
9 (13[1])	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
		1	Reserved
7	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD Boot is the backup mode.

Table 5-21 summarizes the MMCSD pin configuration done by ROM code for eMMC boot on port0 (MMCSD0). eMMC boot on Port 1 (MMCSD1) is not supported.

Table 5-21. eMMC (MMCSD Port 0) Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
MMC0_DAT7	MMC0_DAT7	Enable	Up	0	Enable	0	PADCONFIG126
MMC0_DAT6	MMC0_DAT6	Enable	Up	0	Enable	0	PADCONFIG127
MMC0_DAT5	MMC0_DAT5	Enable	Up	0	Enable	0	PADCONFIG128
MMC0_DAT4	MMC0_DAT4	Enable	Up	0	Enable	0	PADCONFIG129
MMC0_DAT3	MMC0_DAT3	Enable	Up	0	Enable	0	PADCONFIG130
MMC0_DAT2	MMC0_DAT2	Enable	Up	0	Enable	0	PADCONFIG131
MMC0_DAT1	MMC0_DAT1	Enable	Up	0	Enable	0	PADCONFIG132
MMC0_DAT0	MMC0_DAT0	Disable	NA	0	Enable	0	PADCONFIG133
MMC0_CLK	MMC0_CLK	Disable	NA	0	Enable	0	PADCONFIG134
MMC0_CLKLB	MMC0_CLKLB	Disable	NA	0	Enable	0	PADCONFIG135
MMC0_CMD	MMC0_CMD	Disable	NA	0	Enable	0	PADCONFIG136

Note

MMC0_CLKLB signal is not pinned out on the device. The pinmux configuration enables the input buffer of the internal loopback clock.

5.4.4.1 eMMC Bootloader Operation

Booting from an eMMC device is only available on Port 0 of the MMCSD controller (MMCSD0). Booting from an eMMC device is not available on Port1 (MMCSD1)

The ROM will boot from eMMC devices using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode
- eMMC bootmode (alternate)

A special alternate boot mode is available with eMMC devices which allows the ROM to boot from an image that is in a separate boot partition in the eMMC. To boot from this mode, choose "eMMC Boot" (see Table 5-4).

To boot from UDA in either raw or filesystem mode, choose bootmode "MMCSD Boot" (see Table 5-4).

The ROM Code will start reading from the memory boot sector, or filesystem, as specified by the BOOTMODE pin (FS/Raw). Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When eMMC device is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

5.4.4.2 eMMC Flash

To support eMMC boot mode across a device warm reset, eMMC flash has the following requirements:

1. The reset line must be connected to the eMMC flash input reset pin.
2. The eMMC flash ext_csd[162] RST_n_ENABLE must be set to the expected configuration for the warm-reset signal to propagate to the flash device for the boot process to succeed. Possible configurations are shown in Table 5-22.

> **Note**
>
> For warm_reset eMMC boot to function correctly, 0x1 must be written to RST_n_ENABLE in the ext_csd[162] Register. This will enable the RST_n signal.

Table 5-22. ext_csd[162] Register

Bit	Field	Type	Description
7:2	Reserved		Reserved
1:0	RST_n_ENABLE	R/W	0x0: RST_n signal is temporarily disabled (default) 0x1: RST_n signal is permanently enabled 0x2 RST_n signal is permanently disabled 0x3: Reserved

5.4.5 Ethernet Boot

Table 5-23 shows configuration pins assignment to functions when boot mode is the Ethernet RGMII mode.

Table 5-23. Ethernet RGMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Clkout	0	Must be set to 0 to choose external clock
		1	Reserved
8	Delay	0	Must be set to 0 for RGMII with internal Tx delay
		1	Reserved
7	Link info	0	MDIO PHY scan used for link parameters.
		1	Link parameters programmed by the ROM

Table 5-24 shows configuration pins assignment to functions when boot mode is the Ethernet RMII mode.

Table 5-24. Ethernet RMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Clkout	0	50 MHz clock not generated on CLKOUT0
		1	50 MHz clock generated on CLKOUT0
8	Clk src	0	External clock source for RMII1_REF_CLK
		1	Internal clock source for RMII1_REF_CLK
7	RMII	0	This bit must be set to 0
		1	Reserved

Table 5-25. Ethernet RMII Clocking

BOOTMODE Pin 9 (Clk out)	BOOTMODE Pin 8 (Clk src)	Description
0	0	50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused) These are the recommended settings
0	1	Not a valid configuration
1	0	CLKOUT0 is configured to 50MHz and connect to both RMII1_REF_CLK and to external Ethernet PHY input clock
1	1	Not a valid configuration

Table 5-26 shows configuration pins assignment to functions when the backup boot mode Ethernet. The Interface configuration field chooses which interface will be used (RGMII or RMII)

Table 5-26. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13	Interface	0	RGMII with internal TX delay
		1	RMII with external clock source

Table 5-27 summarizes the RGMII pin configuration done by ROM code for Ethernet boot device on RGMII port.

Table 5-27. RGMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_TX_CTL	RGMII1_TX_CTL	Disable	NA	0	Disable	0	PADCONFIG75
RGMII1_TXC	RGMII1_TXC	Disable	NA	0	Disable	0	PADCONFIG76
RGMII1_TD0	RGMII1_TD0	Disable	NA	0	Disable	0	PADCONFIG77

Table 5-27. RGMII Pin Usage (continued)

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_TD1	RGMII1_TD1	Disable	NA	0	Disable	0	PADCONFIG78
RGMII1_TD2	RGMII1_TD2	Disable	NA	0	Disable	0	PADCONFIG79
RGMII1_TD3	RGMII1_TD3	Disable	NA	0	Disable	0	PADCONFIG80
RGMII1_RX_CTL	RGMII1_RX_CTL	Disable	NA	0	Enable	0	PADCONFIG81
RGMII1_RXC	RGMII1_RXC	Disable	NA	0	Enable	0	PADCONFIG82
RGMII1_RD0	RGMII1_RD0	Disable	NA	0	Enable	0	PADCONFIG83
RGMII1_RD1	RGMII1_RD1	Disable	NA	0	Enable	0	PADCONFIG84
RGMII1_RD2	RGMII1_RD2	Disable	NA	0	Enable	0	PADCONFIG85
RGMII1_RD3	RGMII1_RD3	Disable	NA	0	Enable	0	PADCONFIG86
MDIO0_MDIO	MDIO0_MDIO	Disable	NA	0	Enable	0	PADCONFIG87
MDIO0_MDC	MDIO0_MDC	Disable	NA	0	Disable	0	PADCONFIG88

Table 5-28 summarizes the RMII pin configuration done by ROM code for Ethernet boot device on RMII port.

Table 5-28. RMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_RX_CTL	RMII1_RX_ER	Disable	NA	0	Enable	1	PADCONFIG81
RGMII1_RXC	RMII1_REF_CLK	Disable	NA	0	Enable	1	PADCONFIG82
RGMII1_RD0	RMII1_RXD0	Disable	NA	0	Enable	1	PADCONFIG83
RGMII1_RD1	RMII1_RXD1	Disable	NA	0	Enable	1	PADCONFIG84
RGMII1_TD0	RMII1_TXD0	Disable	NA	0	Disable	1	PADCONFIG77
RGMII1_TD1	RMII1_TXD1	Disable	NA	0	Disable	1	PADCONFIG78
RGMII1_TX_CTL	RMII1_TX_EN	Disable	NA	0	Disable	1	PADCONFIG75
RGMII1_TXC	RMII1_CRS_DV	Disable	NA	0	Enable	1	PADCONFIG76
EXT_REFCLK1(1)	CLKOUT0	Disable	NA	0	Disable	5	PADCONFIG124
MDIO0_MDIO	MDIO0_MDIO	Disable	NA	0	Enable	0	PADCONFIG87
MDIO0_MDC	MDIO0_MDC	Disable	NA	0	Disable	0	PADCONFIG88

(1) Enabled when CLKOUT0 option is selected from boot pin selection.

5.4.5.1 Ethernet Bootloader Operation

5.4.5.1.1 Ethernet Initialization Process

When the device is set to boot through the Ethernet mode, the ROM Code configures the Ethernet module and the interface mode (RMII, RGMII) according the the BOOTMODE pin settings, see Section 5.4.5 , *Ethernet Boot Device Configuration*. Also consult the boot parameter table for the Ethernet boot, see Section 5.6.7 , *Ethernet Boot Parameter Table*.

When Link Info = 0, the link parameters are read using MDIO scan. This is the typical setting when using an external PHY. With these parameters, the ROM identifies the PHY and establishes link with the supported speed and duplex mode.

When Link Info = 1, no MDIO scan is performed, and the link parameters are programmed by the ROM based on the RGMII status register. This is the typical setting when configured as a MAC to MAC RGMII interface whereby RGMII pins of two devices can be connected diretly and establish link in force mode. The chosen configuration will be Gigabit, full duplex mode.

Note that booting from RGMII requires that an attached PHY be configured for RGMII-ID Mode immediately upon exiting reset. The ROM will not make this configuration change to the PHY.

The ROM will setup RGMII mode enabling internal delay mode.

5.4.5.1.2 Ethernet Loading Process

After device configuration, the bootloader performs a standard BOOTP/TFTP boot. The device sends a BOOTP request with its MAC address to a host TFTP server to be assigned an IP from a pool of addresses. The timeout for each BOOTP packet is 4 seconds, and the ROM will attempt 10 BOOTP retries, after which the boot mode will fail. If the connection is established, the device initiates a TFTP download and is able to receive image data encapsulated in Ethernet packets, see Section 5.4.5.1.2.1 . There is a timeout of 1 second to receive a response for the READ request, and the ROM will retry the READ request 10 times, after which the boot mode will fail. If TFTP download is successful, data received is stripped of its network headers and the boot data is stored in internal RAM. When the transfer completes and the image is found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.5.1.2.1 Ethernet Boot Data Formats

Ethernet boot uses the BOOTP/TFTP protocol for downloads. Only IPv4 is supported.

5.4.5.1.2.1.1 Limitations

- Received packets cannot be IP fragmented (should not be a problem in most systems since the BOOTP/TFTP packets have fixed lengths of small size)
- Only DIX Ethernet headers are supported.
  - 802.3 with SNAP/LLC not supported
  - DIX Ethernet with VLAN not supported
  - 802.3 with VLAN and SNAP/LLC not supported

5.4.5.1.2.1.2 BOOTP Request

5.4.5.1.2.1.2.1 MAC Header (DIX)

- Destination MAC = value from parameter table (default is broadcast)
- Source MAC = value from parameter table (default is e-fuse value)
- Type = IPv4 (0x0800)

5.4.5.1.2.1.2.2 IPv4 Header

- Version = 4
- Header length = 0
- TOS = 0
- Len = computed during operation
- ID = 0x0001
- Flags + Fragment offset = 0
- TTL = 0x10
- Protocol = UDP (17)
- Header checksum = Computed during operation
- SRC IP = 0.0.0.0
- Dest IP = 255.255.255.255

5.4.5.1.2.1.2.3 UDP Header

- Source port = BOOTP client (68 decimal)
- Destination Port = BOOTP server (67 decimal)
- Length = computed during operation
- Checksum = computed during operation

5.4.5.1.2.1.2.4 BOOTP Payload

- Opcode = Request (1)
- HW Type = Ethernet (1)
- HW Addr Len = 6
- Hop Count = 0
- Transaction ID = 1
- Number of seconds = 0
- Client IP = 0.0.0.0
- Your IP = 0.0.0.0
- Server IP = 0.0.0.0
- Gateway IP = 0.0.0.0
- Client HW Address = Device MAC address (from parameter table)
- Server hostname = NULL
- Filename = NULL
- Option 60, Vendor ID string, from parameter table
- Option 61, Client ID string, from parameter table

5.4.5.1.2.1.2.5 TFTP

There are no ROM code specific TFTP configurations.

5.4.5.1.3 Ethernet Hand Over Process

Once the ROM Code receives the valid packet, it decodes it to get the image sections and loads them in the appropriate memory location. After the image is loaded and validated, the ROM Code starts the boot image execution.

5.4.6 USB Boot

Table 5-29 shows configuration pins assignment to functions when boot mode is the USB mode.

Table 5-29. USB Boot Configuration Fields

USB Configuration Fields for Primary Boot Mode			
BOOTMODE Pins	**Field**	**Value**	**Description**
9	CoreVoltage	0	0.85V core voltage
		1	0.75V core voltage
8 (13[1])	Mode	0	DFU (USB device firmware upgrade)
		1	Host (MSC boot)
7	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

[1] When USB is the backup mode.

Table 5-30 summarizes the USB pin configuration done by ROM code for USB boot device on port 0.

Table 5-30. USB Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
USB0_DRVVBUS	USB0_DRVVBUS	Disable	NA	0	Disable	0	PADCONFIG149

Note

Note that other USB pins do not have pin mux options. USB_DRVVBUS is configured in DFU mode even though it is not used.

Note on USB backup boot:

- Lane Swap (D+/D- lines) are not allowed

Configurability (pins) of these options do not exist in the USB backup boot mode.

CAUTION

A USB Type-AB connector should not be connected to another host when the device is booting as a USB Host. This will prevent two USB power sources from being connected together.

5.4.6.1 USB Bootloader Operation

The USB boot mode is used to read the boot image from external USB host.

See Section 5.4.6 , *USB Boot Device Configuration* and Section 5.6.10 , *USB Boot Parameter Table* for the available configuration options.

More information about USB DFU protocol can be found at http://www.usb.org/sites/default/files/DFU_1.1.pdf.

In DFU mode, the ROM will attempt an enumeration for 60 seconds, after which the boot mode will fail. If a successful enumeration is achieved, the ROM Code will start reading from the external host as specified by the BOOTMODE pins. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.6.1.1 USB-Specific Attributes

5.4.6.1.1.1 DFU Device Mode

- Vendor ID = 0x451
- Product ID = 0x6165

- Device ID = 0

5.4.7 UART Boot

ROM Code always configures the UART port to 115200 kbaud, 8-n-1 mode, and the XMODEM protocol is used to transfer the boot data.

Table 5-31 summarizes the UART pin configuration done by ROM code for UART host on port 0.

Table 5-31. UART Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
UART0_TXD	UART0_TXD	Disable	NA	0	Disable	0	PADCONFIG115
UART0_RXD	UART0_RXD	Disable	NA	0	Enable	0	PADCONFIG114

5.4.7.1 UART Bootloader Operation

5.4.7.1.1 Initialization Process

In the UART boot mode, the selected UART module (port) is the only peripheral configured. The baud rate, data, parity, and stop bits are configured based on the information in the UART boot parameter table. The boot parameter table definitions and the boot configuration values that can be set are in Section 5.4.7 , *UART Boot Device Configuration* and Section 5.6.4 , *UART Boot Parameter Table*.

Once the ROM Code configures the UART, it sends the UART pings for few seconds, which can be seen in the host. The pings consist of an ASCII capital *C* character. The UART boot mode supports only the CRC mode of XMODEM and does not support CHECKSUM mode. Both 128 and 1024 byte block sizes are supported.

5.4.7.1.2 UART Loading Process

Before the ping from the device stops, load the boot image from the host using the XMODEM protocol.

5.4.7.1.2.1 UART XMODEM

The XMODEM protocol is used to transfer boot data. Only CRC mode is supported (not checksum), with both 128- and 1024-byte block sizes. The general, format of received frames is shown in Table 5-32 and Table 5-33.

Table 5-32. XMODEM 1024- and 128-byte Data Frames

STX	Block Num	Inv Block Num	1024 data bytes	CRC	CRC	
SOH	Block Num	Inv Block Num	128 data bytes	CRC	CRC	

Table 5-33. XMODEM Data Frame Fields

Field	Value	Description
STX	0x02	The start character for 1024-byte CRC data blocks
SOH	0x01	The start character for 128-byte CRC data block
Block Num	0x01-0xFF – 0x00	The block number. The first block has value 1, and the block number wraps around 0xFF to 0
Inv Block Num	0xFE-0x00	The inverse block number (bit inverse of the block number)
CRC	Calculated	The 16-bit CRC generated from the polynomial 0x1021

The XMODEM protocol is implemented as a half-duplex protocol as shown in Table 5-34.

Table 5-34. Example of XMODEM Transfer protocol

Transmitter Sends		Receiver Sends
	←	Ping (‘C’)
Frame 1	→	
	←	ACK (or NACK)
Frame 2	→	
	←	ACK (or NACK)
EOT	→	

Table 5-34. Example of XMODEM Transfer protocol (continued)

Transmitter Sends		Receiver Sends
	←	ACK (or NACK)

5.4.7.1.3 UART Hand-Over Process

Once the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.8 GPMC NOR Boot

There are no configuration fields for this boot mode. GPMC NOR boot only supports 16-bit non-mux memory.

Table 5-35 summarizes the GPMC pin configuration done by ROM code for GPMC NOR boot.

Table 5-35. GPMC NOR Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
GPMC0_AD0	GPMC0_AD0	Disable	NA	0	Enable	0	PADCONFIG15
GPMC0_AD1	GPMC0_AD1	Disable	NA	0	Enable	0	PADCONFIG16
GPMC0_AD2	GPMC0_AD2	Disable	NA	0	Enable	0	PADCONFIG17
GPMC0_AD3	GPMC0_AD3	Disable	NA	0	Enable	0	PADCONFIG18
GPMC0_AD4	GPMC0_AD4	Disable	NA	0	Enable	0	PADCONFIG19
GPMC0_AD5	GPMC0_AD5	Disable	NA	0	Enable	0	PADCONFIG20
GPMC0_AD6	GPMC0_AD6	Disable	NA	0	Enable	0	PADCONFIG21
GPMC0_AD7	GPMC0_AD7	Disable	NA	0	Enable	0	PADCONFIG22
GPMC0_AD8	GPMC0_AD8	Disable	NA	0	Enable	0	PADCONFIG23
GPMC0_AD9	GPMC0_AD9	Disable	NA	0	Enable	0	PADCONFIG24
GPMC0_AD10	GPMC0_AD10	Disable	NA	0	Enable	0	PADCONFIG25
GPMC0_AD11	GPMC0_AD11	Disable	NA	0	Enable	0	PADCONFIG26
GPMC0_AD12	GPMC0_AD12	Disable	NA	0	Enable	0	PADCONFIG27
GPMC0_AD13	GPMC0_AD13	Disable	NA	0	Enable	0	PADCONFIG28
GPMC0_AD14	GPMC0_AD14	Disable	NA	0	Enable	0	PADCONFIG29
GPMC0_AD15	GPMC0_AD15	Disable	NA	0	Enable	0	PADCONFIG30
VOUT0_DATA0	GPMC_A0	Disable	NA	0	Disable	1	PADCONFIG46
VOUT0_DATA1	GPMC_A1	Disable	NA	0	Disable	1	PADCONFIG47
VOUT0_DATA2	GPMC_A2	Disable	NA	0	Disable	1	PADCONFIG48
VOUT0_DATA3	GPMC_A3	Disable	NA	0	Disable	1	PADCONFIG49
VOUT0_DATA4	GPMC_A4	Disable	NA	0	Disable	1	PADCONFIG50
VOUT0_DATA5	GPMC_A5	Disable	NA	0	Disable	1	PADCONFIG51
VOUT0_DATA6	GPMC_A6	Disable	NA	0	Disable	1	PADCONFIG52
VOUT0_DATA7	GPMC_A7	Disable	NA	0	Disable	1	PADCONFIG53
VOUT0_DATA8	GPMC_A8	Disable	NA	0	Disable	1	PADCONFIG54
VOUT0_DATA9	GPMC_A9	Disable	NA	0	Disable	1	PADCONFIG55
VOUT0_DATA10	GPMC_A10	Disable	NA	0	Disable	1	PADCONFIG56
VOUT0_DATA11	GPMC_A11	Disable	NA	0	Disable	1	PADCONFIG57
VOUT0_DATA12	GPMC_A12	Disable	NA	0	Disable	1	PADCONFIG58
VOUT0_DATA13	GPMC_A13	Disable	NA	0	Disable	1	PADCONFIG59
VOUT0_DATA14	GPMC_A14	Disable	NA	0	Disable	1	PADCONFIG60
VOUT0_DATA15	GPMC_A15	Disable	NA	0	Disable	1	PADCONFIG61
VOUT0_HSYNC	GPMC_A16	Disable	NA	0	Disable	1	PADCONFIG62
VOUT0_DE	GPMC_A17	Disable	NA	0	Disable	1	PADCONFIG63
VOUT0_VSYNC	GPMC_A18	Disable	NA	0	Disable	1	PADCONFIG64
VOUT0_PCLK	GPMC_A19	Disable	NA	0	Disable	1	PADCONFIG65
GPMC0_CSn3	GPMC_A20	Disable	NA	0	Disable	2	PADCONFIG45
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	Disable	NA	0	Disable	0	PADCONFIG33
GPMC0_OEn_REN	GPMC0_OEn_Ren	Disable	NA	0	Disable	0	PADCONFIG34
GPMC0_WEN	GPMC0_WEN	Disable	NA	0	Disable	0	PADCONFIG35

Table 5-35. GPMC NOR Boot Pin Usage (continued)

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
GPMC0_BE0n_CLE	GPMC0_BEOn_CLE	Disable	NA	0	Disable	0	PADCONFIG36
GPMC0_BE1n	GPMC0_BE1n	Disable	NA	0	Disable	0	PADCONFIG37
GPMC0_CSn0	GPMC0_CSn0	Disable	NA	0	Disable	0	PADCONFIG42

Note

Only 21 address lines (GPMC0_A0 – GPMC0_A20) are used because the GPMC0_A21 and GPMC0_A22 lines are muxed with GPMC0_WAIT1 and GPMC0_WPn respectively.

GPMC0_A20 is muxed with GPMC0_CSn3, and ROM uses GPMC0_A20 for this address line. Thus, no CSn3 support when using GPMC NOR boot.

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.8.1 GPMC NOR Bootloader Operation

In this mode, the ROM Code configures the GPMC interface based on the configuration parameters specified in the boot parameter table for the GPMC NOR boot mode Section 5.6.11 , see*GPMC NOR Boot Parameter Table*.

Timing registers are programmed as follows for NOR flash boot:

Table 5-36. GPMC NOR Timing Configuration

GPMC register	Value
GPMC_CONFIG1	0x00001010
GPMC_CONFIG2	0x00101c01
GPMC_CONFIG3	0x23060917
GPMC_CONFIG4	0x1005bc1a
GPMC_CONFIG5	0x011b111e
GPMC_CONFIG6	0x8f070000
GPMC_CONFIG7	0x00000c50

GPMC NOR boot mode is not executable-in-place (XIP). ROM code first copies boot image into on-chip RAM and then executes it. Only non-muxed memory is supported. If the initial image at offset 0x0 is not recognized, the ROM will attempt to read a redundant image from offset 0x100000. This is the only redundant image supported by the ROM.

5.4.9 GPMC NAND Boot

Table 5-37 summarizes the GPMC pin configuration done by ROM code for NAND boot.

Table 5-37. GPMC NAND Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
GPMC0_AD0	GPMC0_AD0	Disable	NA	0	Enable	0	PADCONFIG15
GPMC0_AD1	GPMC0_AD1	Disable	NA	0	Enable	0	PADCONFIG16
GPMC0_AD2	GPMC0_AD2	Disable	NA	0	Enable	0	PADCONFIG17
GPMC0_AD3	GPMC0_AD3	Disable	NA	0	Enable	0	PADCONFIG18
GPMC0_AD4	GPMC0_AD4	Disable	NA	0	Enable	0	PADCONFIG19
GPMC0_AD5	GPMC0_AD5	Disable	NA	0	Enable	0	PADCONFIG20
GPMC0_AD6	GPMC0_AD6	Disable	NA	0	Enable	0	PADCONFIG21
GPMC0_AD7	GPMC0_AD7	Disable	NA	0	Enable	0	PADCONFIG22
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	Disable	NA	0	Disable	0	PADCONFIG33
GPMC0_OEn_Ren	GPMC0_OEn_Ren	Disable	NA	0	Disable	0	PADCONFIG34
GPMC0_Wen	GPMC0_Wen	Disable	NA	0	Disable	0	PADCONFIG35
GPMC0_BEOn_CLE	GPMC0_BEOn_CLE	Disable	NA	0	Disable	0	PADCONFIG36
GPMC0_WAIT0	GPMC0_WAIT0	Disable	NA	0	Enable	0	PADCONFIG38
GPMC0_CSn0	GPMC0_CSn0	Disable	NA	0	Disable	0	PADCONFIG42

5.4.9.1 GPMC NAND Bootloader Operation

Timing registers are programmed as follows for NAND flash boot:

Table 5-38. GPMC NAND Timing Configuration

GPMC register	Value
GPMC_CONFIG1	0x00000813
GPMC_CONFIG2	0x00080b00
GPMC_CONFIG3	0x22080810
GPMC_CONFIG4	0x05006890
GPMC_CONFIG5	0x0107080b
GPMC_CONFIG6	0x80000180
GPMC_CONFIG7	0x00000f50

GPMC NAND boot only supports boot from ONFI 1.0 compatible 8 bit parallel NAND memory up to 2Gbytes in size connected to GPMC CS0 with the following geometries:

- 2Kbyte page and spare area of at least 64 bytes or
- 4Kbyte page size and spare area of at least 128 bytes.
- Non-ECC part only:
  - ROM uses ELM to handle ECC
  - ECC is BCH8 using D[7:0] for data
  - The param page CRC is checked and in case of failure the redundant page is used

GPMC is setup to comply with mode 0 timing for NAND flash.

5.4.10 No boot/Development boot

Table 5-39 shows configuration pins assignment to functions when boot mode is the No-boot mode.

Table 5-39. No-boot/Dev-boot Configuration Fields

Field	Value	Description
No/Dev	0	Development Boot
	1	No boot
ARM/Thumb	0	ARM mode
	1	Thumb mode

These boot modes are useful for debugging purposes to preclude the execution of the ROM.

During the Development boot (BOOTMODE[7] = 0), the SMS M4F ROM code will act as if boot of the primary image has completed, and the SMS M4F ROM then will be waiting for a firmware load message from DM R5. Thus the user can load a standard u-boot/SPL image to the DM R5 RAM. U-boot/SPL will then load the SMS firmware and complete the full boot.

In No-boot (BOOTMODE[7] = 1), both the SMS M4F and DM R5 ROMs are bypassed and both CPUs are held in a dummy branch-to-self loop. No-boot is the most minimal device touch state by the ROM - only minimal hardware configurations are done and none of the PLLs is locked/configured. No-boot is suitable if user wants to load his own PLL, Pad config, and other basic settings.

5.5 PLL Configuration

ROM code must be aware of the reference clock provided to PLLs. That is, the speed of the quartz crystal, or the clock supplied by an external clock oscillator. On how to indicate the PLL reference clock, see PLL Reference Clock Selection

ROM code configures only PLLs which are required during boot. Therefore, if a PLL is required for the backup boot mode but not the primary boot mode, and if the backup boot mode never executes, then the PLLs required for backup boot are not enabled.

The following tables show the HSDIV values that are programmed by the R5 ROM if a boot mode uses it. A value of NA means that the ROM does not program that HSDIV

Table 5-40. MAIN_PLL0 (MAIN PLL) (2000MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	4	500	MAIN SYSCLK0
0	HSDIV1	10	200	OSPI
0	HSDIV2	0	NA	WKUP_CLKOUT
0	HSDIV3	15	133	GPMC NOR/GPMC NAND
0	HSDIV4	0	NA	MCAN
1	HSDIV5	5	200	eMMC0
1	HSDIV6	0	NA	CPTS
1	HSDIV7	4	250	TIMER
1	HSDIV8	0	NA	USB0
1	HSDIV9	0	NA	PRUSS-M

Table 5-41. MAIN_PLL1 (PER0 PLL) (1920MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	10	192	UART
0	HSDIV1	12	160	UART
0	HSDIV2	0	NA	WKUP_CLKOUT
0	HSDIV3	0	NA	TIMER
0	HSDIV4	0	NA	Reserved
1	HSDIV5	0	NA	OSPI
1	HSDIV6	0	NA	McASP

Table 5-42. MAIN_PLL2 (PER1 PLL) (2000MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	0	NA	PRUSS-M core
0	HSDIV1	8	250	CP_GEMAC
0	HSDIV2	10	200	eMMC1
0	HSDIV3	0	NA	DebugSS
0	HSDIV4	0	NA	GPU
1	HSDIV5	0	NA	PRUSS-M IEP
1	HSDIV6	0	NA	TIMER
1	HSDIV7	0	NA	GPMC
1	HSDIV8	0	NA	McASP
1	HSDIV9	0	NA	WKUP_CLKOUT

Table 5-43. MAIN_PLL15 (2400MHz)

HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
HSDIV0	5	400	HSM/SMS
HSDIV1	5	400	SA3_UL PKA
HSDIV5	3	800	DM

Note

All other PLLs are not used or programmed by the ROM

Note

The bringup and configuration of bootmode-specific PLLs by ROM code will result in a bootmode-specific device clocking setup which for example has an impact on which peripheral modules can readily be clocked and used by SBL/SPL prior to loading and bringing up System Firmware (SYSFW)

5.6 Boot Parameter Tables

The boot parameter tables direct the main module boot process. On cold boot the tables are created based on pin strapped values (see Section 5.3 , *Boot Mode Pins*) and built-in data. The ROM Code supports two parameter tables stored as an array in a fixed memory address in the MSRAM, each of size 512 bytes. The ROM will attempt to boot using the primary table. On boot failure, ROM Code will retry using the second table.

Using two tables handles two cases.

- The first is in initial board manufacture where the primary boot table specifies boot from a flash device, and the flash is blank. ROM Code would then switch to the secondary boot mode which would receive the image externally (Ethernet, USB, UART) and this image would flash the boot image.
- The second case is failure due to total flash corruption. In all flash parameter tables there exist backup addresses within the primary boot mode. This covers the problem of a flash update failure with a backup image present on the same flash device.

The boot tables reside at a fixed location in memory which is described in Section 5.8.2 , *Global Memory Addresses Used by ROM Code*.

5.6.1 Common Header

These boot parameter tables have certain parameters common across all the boot modes, while the rest of the parameters are unique to the boot modes. The common entries in the boot parameter table are shown in Table 5-44.

Table 5-44. Boot Parameter Table Common Header

Byte Offset	Size (bytes)	Name	Description
0	2	Length	The length of the table
2	2	Checksum	Ones complement checksum over length bytes in the table. If 0 the checksum is not validated.
4	2	Peripheral	Identifies the boot peripheral and format of the table after the common header. See Table 5-45
6	2	Reserved	Reserved
8	4	Timeout	Timeout for this boot mode, in milliseconds
12	4	Magic	Magic value 0x01AD0911
16	40	PLL Config 0	PLL Configuration 0. See Table 5-46
56	40	PLL Config 1	PLL Configuration 1
96	40	PLL Config 2	PLL Configuraiton 2
136	40	PLL Config 3	PLL Configuration 3
176	40	PLL Config 4	PLL Configuration 4
216	40	PLL Config 5	PLL Configuration 5

Table 5-45 lists the possible boot modes used in the boot parameter tables.

Table 5-45. Boot Peripheral Selection

Peripheral Field Value	Description
0	Sleep (No boot)
10	Ethernet Reserved
20	Ethernet BOOTP/TFTP (general)
21	Ethernet RGMII specific
22	Ethernet RMII specific
30	Reserved
31	Reserved
32	Reserved
40	I2C

Table 5-45. Boot Peripheral Selection (continued)

Peripheral Field Value	Description
50	SPI
60	UART
70	USB DFU
71	USB Reserved
72	USB Host MSC
80	QSPI
85	OSPI
90	Reserved
100	MMCSD Card (general)
101	eMMC (general)
102	MMC 1-bit
103	MMC 4-bit
104	MMC 8-bit
110	GPMC NOR
120	Reserved
130	xSPI
140	GPMC NAND

5.6.2 PLL Setup

Table 5-46 through Table 5-50 describe the PLL configuration fields.

Table 5-46. Boot Parameter Table PLL Configuration

Byte Offset	Size (bytes)	Name	Description
0	1	Domain/cfg	See Table 5-47
1	1	Pll number	PLL number indexed from 0.
2	1	Input source	See Table 5-49
3	1	Pll Type	This field must be 1 to indicate an SCPLL
4	4	Input Ref Clock	The PLL input clock, in Q16.16 format
8	4	Feed back divider, integer part	Integer value of feedback divider
12	4	Feed back divider, fractional part	Fractional portion of feedback divider. Total divider is the Integer part + (Fractional part / 2^{24})
16	1	Ref divider	Input clock pre-divider
17	1	Post divider 1	Output post divider 1
18	1	Post divider 2	Output post divider 2
19	1	Reserved	Reserved
20	2	Hsdiv Enable	Bit map. A set bit indicates that the corresponding hsdiv is enabled.
22	2	Reserved	Reserved
24	16	Hsdiv[16]	Array of hs divider values.

Table 5-47. PLL Domain and Enable Configuration

7	6	5	4	3	2	1	0
Reserved		Enable		Reserved			Domain

Table 5-48. PLL Domain and Enable Field Description

Field	Value	Description
Enable	0	PLL not configured
	1	PLL enabled only if currently disabled or in bypass

Table 5-48. PLL Domain and Enable Field Description (continued)

Field	Value	Description
	2	PLL is unconditionally enabled. If currently enabled with a different configuration the PLL is first disabled
	3	PLL is unconditionally disabled
Domain	0	PLL is in the MCU domain
	1	PLL is in the MAIN domain

Table 5-49. PLL Reference Source Bit Fields

7	6	5	4	3	2	1	0
Source Type				Source Index			

Table 5-50. PLL Reference Source Field Description

Field	Value	Description
Source Type	0	Source is HFOSC
	1	Source is external pin
	2	Reserved
	3-7	Reserved
Source Index	0-31	Source index (HFOSC[0-31] or pin[0-31], depending on Source Type) HFOSC[0] – WKUP_HFOSC0 HFOSC[1] – HFOSC1 (in MAIN domain) PIN[1] – EXT_REFCLK1 pin (not all PLLs, see *Clocking*

5.6.3 OSPI/QSPI/SPI Boot Parameter Table

Table 5-51 shows the boot parameter table for OSPI, QSPI, or SPI boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-51. OSPI/QSPI/SPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 2, 4, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 2, 4, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 2, 4, 8)
261	1	Address Size	24	24, and 32 bits are the valid address sizes
262	1	Mode	0	OSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	Reserved	0	Reserved
270	2	Module Freq	0	The OSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The OSPI bus frequency, in kHz
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command
280	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.

Table 5-51. OSPI/QSPI/SPI Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
284	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
288	4	notDAC	From pins	When 0, DAC mode is used
292	4	Read Index	0	Index to the active read address (0-1)
296	4	Read Addr 0	0x000000	The initial flash read address
300	4	Read Addr 1	0x400000 (0x4000 SPI)	Backup read address
304	4	Reserved	0	Reserved
308	4	Reserved	0	Reserved

5.6.4 UART Boot Parameter Table

Table 5-52 shows the boot parameter table for UART boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-52. UART Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Magic	0x49	Required Magic value
257	1	Protocol	63 (0x3F)	Specifies the transfer protocol = XMODEM
258	2	Reserved	0	Reserved
260	1	Max error Count	10	Error count resulting in boot abort
261	1	Ack timeout	3	Timeout in seconds on ack
262	1	Char timeout	20	Inter-character timeout in milliseconds
263	1	Reserved	0	Reserved
264	4	Port	From Pins	Physical port number
268	4	Mod Ref Clk	48000	Module reference clock, in kHz
272	4	Data Rate	115200	Baud rate (bps)
276	1	Parity	0	0=none, 1=odd, 2=even
277	1	Data bits	8	Only 8 data bit width is supported
278	1	Stop bits	2	Stop bits in Q7.1 format (2 = 1 stop bit)
279	1	Flow Control	0	0=none, 1= RTS/CTS
280	1	Over sample	16	Only 16× and 13× oversample are supported
281	1	Magic 2	0xB7	Required magic value

5.6.5 I2C Boot Parameter Table

Table 5-53 shows the boot parameter table for I2C boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-53. I2C Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode	From Pins	0x4E = I2C Controller, 0x72 = I2C target
258	1	Dev Addr	From Pins	I2C address when target mode (0x10 or 0x11)
259	1	Reserved	0	Reserved
260	4	Mod Clock	0	I2C Module input clock. If 0, it is computed by ROM code.
264	2	Bus Freq	400	I2C Controller mode bus frequency, in kHz
266	2	Bus Addr	From Pins	I2C Controller mode storage device's address (0x50 or 0x51)

Table 5-53. I2C Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
268	2	Read Index	0	Index to the active read offset (0 or 1)
270	2	Read Offset 0	0x0000	I2C Controller mode read offset
272	2	Read Offset 1	0x8000	I2C Controller mode backup read offset
274	2	Reserved	0	Reserved
276	2	Reserved	0	Reserved
280	2	Busy Timeout	From pins	Number of µs before a bus recovery is attempted. In units of microseconds in Q3 number format. Value of 0 disables bus recovery attempts.

5.6.6 MMCSD/eMMC Boot Parameter Table

MMCSD/eMMC Boot Parameter Table shows the boot parameter table for eMMC, MMC or SD card boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-54. MMCSD/eMMC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	From Pins	Physical port number
257	1	eMMC	From Pins	0 = SD/MMC, else eMMC
258	1	bootAck	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode the controller expects a boot ack from the eMMC
259	1	Media	1 for eMMC 0 for SD/MMC	0 = auto detect card type 1 = MMC 2 = SD
260	1	busWidth	8 for eMMC From Pins for SD/MMC	Number of data pins (1, 4, or 8). If 0, max supported pins of the port are used.
261	1	bootAlt	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode, the controller uses the alt boot method (CMD1 with arg 0xFFFF_FFFA) to initiate data transfer
262	1	sigVolt	0x18 for port0 0x33 for port1	Sets the signal voltage for the controller. 0x18 = 1.8V 0x33 = 3.3V
263	1	Reserved	0	Reserved
264	4	Max Bus Freq	0	Max bus frequency in kHz. If 0, the value is determined by reading the CSD register from the card (still maxes out at 25 MHz)
268	4	refClkkHz	0	Module reference clock frequency, in kHz. If 0, the ROM code computes the value.
272	4	respTimeout	40000	The timeout period on initial card read, in milli-seconds, Q3 number format
276	128	Filename	"\tiboot3.bin"	For SD/MMC, boot filename in 16-bit Unicode characters (max 64)
404	4	Mode	0x1144D091	0x1144D091 = file system boot 0x1144C180 = raw image boot
408	4	CardIsInit	0	0 = card not yet initialized 1 = card has been initialized
412	4	Rsvd	0	Reserved
416	4	RawIndex	0	Current active read offset (0 or 1)
420	4	Rsvd	0	Reserved

Table 5-54. MMCSD/eMMC Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
424	4	Raw Offset 0	0x000000	Raw read offset
428	4	Raw Offset 1	0x400000	Backup raw read offset
432	4	Rsvd	0	Reserved
436	4	Rsvd	0	Reserved

5.6.7 Ethernet Boot Parameter Table

Table 5-55 is shown segmented into four sections:

1. The first section contains information required to configure the device hardware
2. The second section contains information used by the top level Ethernet module to execute the boot
3. The third section contains information for the Ethernet stack code.
4. The fourth section contains information for creating the BOOTP packet (vendor string, ID string and debug string), and holds information returned in the BOOTP response (Default route and file name)

Table 5-55 shows the boot parameter table for Ethernet boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-55. Ethernet Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
		Hardware Configuration Options		
256	2	Mod Freq	0	Module clock frequency, kHz. If 0, ROM code computes the value.
258	1	Port Num	0	Physical port number
259	1	Interface	From Pins	0 = RGMII with internal delay 1 = RGMII with external delay 2 = RMII
260	1	Init Level	0	0 = Initialize only not enabled modules 1 = Full ethernet sub-system initialization
261	1	Clock out enable	From pins	0x10 = CLKOUT0 enable 0x11 = CLKOUT0 disable
262	1	Clk out freq	From pins	0x20 = CLKOUT0 25 MHz (RGMII) 0x21 = CLKOUT0 50 MHz (RMII)
263	1	RMII Clk In	From pins	0x60 = RMII internal (SoC) clock 0x61 = RMII external clock
264	1	Port Enable	0x01	Bit map. A set bit indicates that the corresponding physical port will be enabled
265	1	Phy Query	From pins	0x30 = speed/duplex determined from RGMII status register 0x31 = MDIO used to query PHY 0x32 = Use fixed speed/duplex values from offset 266/267.
266	1	Speed		0x40 = full speed (1Gbit for RGMII, 100Mbit for RMII) 0x41 = slow speed (100Mbit for RGMII, 10Mbit for RMII)
267	1	Duplex		0x50 = full duplex 0x51 = half duplex
		Main Level Boot Control		
268	1	Bootp enable	1	0 = Image information already in this structure 1 = Use BOOTP to get boot image information
269	1	Reserved	0	Reserved
270	2	Bootp Timeout	4000	BOOTP timeout in milli-seconds

Table 5-55. Ethernet Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
272	2	TFTP timeout	1000	TFTP timeout in milli-seconds
274	2	Bootp retries	10	Number of BOOTP retries before fail
276	2	TFTP retries	10	Number of TFTP retries before fail
278	2	Reserved	0	Reserved
Network Stack Configuration (plus TFTP server ID)				
280	6	MAC Address	From E-fuse	MAC address of the device
286	2	Reserved	0	Reserved
288	4	Device IP	0	IP address of the device. Valid only if BOOTP not enabled
292	4	Net Mask	0	Net mask. Valid only if BOOTP not enabled
296	4	Tftp server IP	0	TFTP server IP. Valid only if BOOTP not enabled
BOOTP send and receive Information				
300	20	Vendor String	"TI K3 Bootp Boot"	BOOTP request vendor string. Valid only if BOOTP not enabled
320	9	Client ID	1-mac-address-0	Client ID. See RFC1700
329	1	ID len	7	Client ID length
330	45	Debug array	SOC ID up to size available	Debug array output
375	1	Debug len	Varies	The number of valid bytes in debug array
376	4	Next hop	0	Next hop IP address. Valid only if bootp not enabled
380	4	Default Route	0	IP default route IP address. Valid only if bootp not enabled
384	128	Boot filename	0	Boot filename. Valid only if bootp not enabled

5.6.8 xSPI Boot Parameter Table

xSPI Boot Parameter Table shows the boot parameter table for xSPI boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-56. xSPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 8)
261	1	Address Size	24	24 and 32 bits are the valid address sizes
262	1	Mode	0	QSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	ddrEnable	From pins	OSPI DDR mode operation
270	2	Module Freq	0	The QSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The QSPI bus frequency, in kHz

Table 5-56. xSPI Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command
280	1	SFDP	From Pins	Enables SFDP parser for 1S-1S-1S to 8D-8D-8D switching
282	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
286	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
290	4	inDAC	From pins	When 0, XIP mode is used
294	4	Read Index	0	Index to the active read address
298	4	Read Addr 0	0x000000	The initial flash read address
302	4	Read Addr 1	0x400000	Backup read address

5.6.9 USB DFU Boot Parameter Table

USB DFU Boot Parameter Table shows the boot parameter table for USB DFU boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-57. USB DFU Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6165	USB product ID. Read from control registers.
280	2	BCD Device	0x200	Binary Coded Decimal device release number
284	4	String Table addr	0x4182A76C	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	32	Offset to product string in string table
292	2	Serial num string offset	64	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	4	Block Size	4096	DFU Block Size

5.6.10 USB MSC Boot Parameter Table

USB MSC Boot Parameter Table shows the boot parameter table for USB boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-58. USB MSC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.

Table 5-58. USB MSC Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6164	USB product ID. Read from control registers.
280	2	BCD Device	0	Binary Coded Decimal device release number
284	4	String Table addr	0x4182BCA8	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	0	Offset to product string in string table
292	2	Serial num string offset	0	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	64	FileName	tiboot3.bin	Boot file name

5.6.11 GPMC NOR Boot Parameter Table

Table 5-59 shows the boot parameter table for GPMC NOR boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-59. GPMC NOR Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	refClkkHz	0	The module functional clock frequency, in kHz. 0 = ROM code computes the value.
260	4	csSizeMb	64	The size of each chip-select, in MB
264	1	Csel	From pins	The chip-select to use (0-3)
265	1	adMux	From pins	The address/data multiplexing used. 0 = A/D parallel, 1 = A/A/D mux, 2 = A/D mux
266	1	Width	16	Data bus width
267	1	Reserved	0	Reserved
268	4	Read index	0	The currently active read offset (0-1)
272	4	Read offset 0	0x000000	Read address offset 0
276	4	Read offset 1	0x400000	Backup read address offset 1
280	4	Reserved	0	Reserved
284	4	Reserved	0	Reserved

5.6.12 GPMC NAND Boot Parameter Table

GPMC NAND Boot Parameter Table shows the boot parameter table for GPMC NAND boot. Must be preceded with the common boot parameters described in Table 5-44.

Table 5-60. GPMC NAND Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Ref Clk kHz	From pins	Specifies the module ref clock.
260	4	Page Size	0	Page size in bytes 2048 or 4096
264	1	Chip Select	0	Chip Select
265	1	Ad Mux	0	Address/data multiplexing
266	1	Data Bus Width	8	Data bus width. Valid values are 8 and 16
267	1	AD rows	0	Number of Row address
268	1	AD columns	0	Number of Column address cycles
269	1	ECC Nibbles	0	Size of BCH remainder in nibbles. 0 if no ECC, 26 for BCH8
270	2	Current Valid Block	0xFFFF	Block number of last known good block
272	2	Pages per Block	0	Number of pages in a block
274	2	Reserved	0	Reserved
276	4	Current Read Index	0	Active read index
280	4	Read Offset[0]	0	Offsets from base of GPMC NAND memory
284	4	Read Offset[1]	0x400000	Offsets from base of GPMC NAND memory

5.7 Boot Image Format

5.7.1 Overall Structure

The boot image consists of an X.509 Certificate, which is optional for GP devices, followed immediately by a boot image blob.

X.509 Certificate (Variable Size) (Optional)
Boot Image Blob (Variable Size)

5.7.2 X.509 Certificate

The X.509 certificate is described in RFC5280. Section 4.1 of the specification describes the format.

The X.509 fields relevant to the public boot (taken from RFC5280) are shown below.

```
Certificate  ::=   SEQUENCE  {
        tbsCertificate       TBSCertificate,
        signatureAlgorithm   AlgorithmIdentifier,
        signatureValue       BIT STRING  }
   TBSCertificate  ::=  SEQUENCE  {
        version         [0]  EXPLICIT Version DEFAULT v1,
        serialNumber         CertificateSerialNumber,
        signature            AlgorithmIdentifier,
        issuer               Name,
        validity             Validity,
        subject              Name,
        subjectPublicKeyInfo SubjectPublicKeyInfo,
        issuerUniqueID  [1]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        subjectUniqueID [2]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        extensions      [3]  EXPLICIT Extensions OPTIONAL
                             -- If present, version MUST be v3
        }
  Extensions  ::=  SEQUENCE SIZE (1..MAX) OF Extension
   Extension  ::=  SEQUENCE  {
        extnID      OBJECT IDENTIFIER,
        critical    BOOLEAN DEFAULT FALSE,
        extnValue   OCTET STRING
                    -- contains the DER encoding of an ASN.1 value
                    -- corresponding to the extension type identified
                    -- by extnID
        }
```

In general, an X.509 certificate contains a public key which has been signed by a private key. The public ROM code does not directly use the keys. In non-secure devices, the public key value is in general a don’t care condition. The exception is certificates containing a degenerate RSA public key. GP devices with a degenerate RSA key allow for integrity checking of most (but not all) of the certificate.

The public ROM only needs to extract some of information from the X.509 formatted structure:

- The total size of the X.509 Certificate
- The total size of the boot image

The total size of the X.509 Certificate is determined by reading the length of the sequence containing the certificate. The length of the image is determined by parsing the certificate to find the extension field which holds the image length.

The ROM defines several extensions that are used only by TI for boot. These are placed in the extensions field of the TBS certificate.

5.7.3 Organizational Identifier (OID)

OID (organizational identifier) values are represented as a tree structure. TI has the following node registered:

1.3.6.1.4.1.294: iso(1), identified-organization(3), dod(6), internet(1), private(4), enterprise(1), Texas Instruments(294)

ROM code adds the following branch after *Texas Instruments*: *device-boot(1)*. The OID values shown in this section are leaves off the device boot branch.

5.7.4 X.509 Extensions Specific to Boot

These values are not defined in any standard, but created by TI for boot.

5.7.4.1 Boot Info (OID 1.3.6.1.4.1.294.1.1)

This extension must be present on all boot images. It is from this extension that the image length is extracted.

```
bootInfo ::=  SEQUENCE {
   cert_type: INTEGER,-- identifies the certificate type
   boot_core:INTEGER,-- identifies the boot core
   core_opts:INTEGER,-- 32 or 64 bit boot core target
   load_addr:OCTET STRING,-- Global address image destination
   image_size:INTEGER,-- Image size in bytes
}
```

Table 5-61. Certificate Type Values

Value	Description
0x0000_0001	Primary boot image
0x0000_0002	Firmware image

Table 5-62. Boot Core Values

Value	Description
0x00	Firmware (M4) image
0x08	M4 certificate
0x10	R5 image
0x20	Reserved

Table 5-63. Core Options Bit Fields

31	2	1	0
Reserved		Split	Mode

Table 5-64. Core Options Field Description

Bits	Field	Value	Description
1	Split	0	Dual MCU set to lockstep (two cores in lockstep)
		1	Dual MCU set to split mode (two independent cores)
0	Mode	0	MCU starts execution in Arm® mode
		1	MCU starts execution in Thumb® mode

5.7.4.2 Image Integrity (OID 1.3.6.1.4.1.294.1.2)

```
imageIntegrity ::= SEQUENCE {
   sha_type:OID,-- Identifies the SHA type
   hash:OCTET STRING-- The SHA of the boot image
}
```

5.7.5 Extended Boot Info Extension

The ROM supports a combined boot image boot flow. In this flow, a boot binary blob has both Secondary bootloader (SBL) and System Firmware (SYS-FW) embedded in the boot image with a single X509 certificate. This method helps with the following situations:

- Allows ROM to load and run both the bootloader and SYS-FW in parallel without any dependency.
- Optimizes ROM boot time by minimizing different x509 certificate parsing and authentication.

To support this combined boot format, ROM employs a new X509 extension called: ext_boot_info. It supports multiple boot components with a single certificate. It allows up to 5 components as part of this extension:

- Component1: Mandatory and should point to info about SBL binary
- Component2: Optional and if present should point to SYS-FW binary in all device types
- Component3: Optional (Load section to SBL, new certType)
- Component4: Optional (Load section to SYS-FW, new certType)
- Component5:
  - HS-FS and HS-SE non Prime devices. Mandatory and should point to SYS-FW Inner certificate
  - GP and HS-SE Prime devices. Optional (Load Section to SBL or SYS-FW)

This extended boot info extension replaces boot_seq (boot_info) and image_integrity extensions from the previous sections, and these should be exclusive in any given certificate.

ROM supports other extensions, such as sw_rev and debug_info, in both formats.

ROM selects the combined image flow based on the presence of ext_boot_info extension in the certificate and skips boot_seq (boot_info) and image_integrity extensions boot flow.

Having one component in ext_boot_info is same as legacy flow (that is, flow using boot_seq and image_integrity); for two or more components, ROM starts both SBL and SYS-SW, the third and fourth components are loaded by ROM to the allowed loading memory range of SBL and SYS-FW if there is no overlap in load address with executable binary info.

Each of the components can independently specify hash value of the binary, and ROM validates the hash on HS and GP if RSA degenerate key is used for signing.

Additionally, ROM rejects the full image if hash of any single component mismatches.

5.7.5.1 Impact on HS Device

For HS devices, ROM supports encryption of images optionally when specified with the Encryption extenstion.

Encryption - Encryption of the components must be specified with a new extension called ext_boot_enc. This is an optional extension that must be specified only if any of the components are encrypted with a customer key set. Specify a component number followed by encryption extension details for ROM to decrypt the given components. This extension is used only with combined boot image format (that is, using Extended Boot Info Extension).

Prime vs Non-Prime - The main difference between HS prime and non-prime devices is the presence of the SYS-FW Inner certificate. Extended boot info extension supports both prime and non-prime devices. ROM supports SYS-FW binary as Comp#2 in all device types; for HS-SE non-prime and HS-FS devices, the SYS-FW inner certificate is expected as another optional component in #3, 4, or 5.

5.7.5.2 Extended Boot Info Details

```
1.3.6.1.4.1.294.1.9=ASN1:SEQUENCE:ext_boot_info
[ ext_boot_info ]
 extImgSize = INTEGER:470656
 numComp = INTEGER:4
 sbl=SEQUENCE:comp1
 fw=SEQUENCE:comp2
 bd1=SEQUENCE:comp3
 bd2=SEQUENCE:comp4

[ comp1 ]
 compType = INTEGER:1
 bootCore = INTEGER:16
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:41c00000
 compSize = INTEGER:237376
 shaType = OID:2.16.840.1.101.3.4.2.3
```

```
 shaValue =
FORMAT:HEX,OCT:6779fdb2b2c27169737c184085b97938bd77bdf698245840f166ca30c7125c29a6675139a25a0a2a3f00a
76d43d082df238c12cb6b293ec0eeb5990bcd603a23

[ comp2 ]
 compType = INTEGER:2
 bootCore = INTEGER:0
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:00040000
 compSize = INTEGER:196608
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:47f27fb24b81927a928845a4c2b993e6a3d5bdfe5ed01c0ec4f96a7ead991c69bf4ed4b9b958fd36a75f3
3aba04d2c28602a85ca737ee75617d6a9a41f4353a3

[ comp3 ]
 compType = INTEGER:18
 bootCore = INTEGER:0
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:00072000
 compSize = INTEGER:16384
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:2d165ec1d8a38acb977d9298e8a6a27491c62d6daa31f921db9135f9a68779b30b384573c6e4e8203de5f
0a47191c3ff9a35b52a911874e07615f10b4b2f5829

[ comp4 ]
 compType = INTEGER:17
 bootCore = INTEGER:16
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:41c40000
 compSize = INTEGER:20288
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:12d5be5b2b9774d1b0cad21cbf1dbcdbd7c310657f4334902e3cc6228cf2d8fc844139dae4db6041c38cd
a502d6a900d57039322d360032268a13445021b04a7
```

5.7.5.3 Certificate / Component Types

ROM supports only the following component types; all other component types will be rejected.

- CompType 0x1 for SBL binary - compType = INTEGER:1
- CompType 0x2 for SYS_FW binary - compType = INTEGER:2
- CompType 0x3 for SYS_FW Inner Certificate - compType = INTEGER:3
- CompType 0x11 for SBL Memory load section - compType = INTEGER:17

Primary Image load section, that can be loaded in to SBL allowed memory range:

- CompType 0x12 for SYS_FW Memory load section - compType = INTEGER:18

SYS-FW load section, that can be loaded in to SYS-FW allowed memory range

5.7.5.4 Extended Boot Encryption Info

Extended Boot Encryption Info specifies the imageEncryption extension per component basis. This extension is not applicable for GP or HS-FS devices, and is optional for HS-SE devices if any components in the image are encrypted. In HS-FS and HS-SE non-prime devices, the SYS-FW binary encryption details are part of SYS-FW Inner certificate. This extension is applicable if either SBL, SYS-FW binary in HS-SE prime, or any binary blobs are encrypted in HS-SE devices.

```
1.3.6.1.4.1.294.1.10=ASN1:SEQUENCE:ext_enc_info

[ ext_enc_info ]
 numComp = INTEGER:2
 esbl=SEQUENCE:enc1
 efw=SEQUENCE:enc2

[ enc1 ]
 compNum = INTEGER:1
 iv = FORMAT:HEX,OCT:474bfd801866beecc7ab6d4c61490e1a
 randString = FORMAT:HEX,OCT:772fc5810fa36f516e595ad8adf19260f47a8461f193892746692fbb932727a1
 iterationCnt = INTEGER:0
```

```
 salt = FORMAT:HEX,OCT:42ea40851298339c8baa84f29d6b68d0

[ enc2 ]
 compNum = INTEGER:2
 iv = FORMAT:HEX,OCT:aaaaaaaaaaaabeecc7ab6d4c61490e1a
 randString = FORMAT:HEX,OCT:bbbbbbbbbbbbbbbbbe595ad8adf19260f47a8461f193892746692fbb932727a1
 iterationCnt = INTEGER:2
 salt = FORMAT:HEX,OCT:ccccccccccccccccccaa84f29d6b68d0
```

5.7.5.5 Component Ordering

ROM supports fixed Component ordering for SBL- Binary and SYS-FW Cert and Binary.

For GP and HS-SE Prime devices, Comp#1 should be SBL binary, and Comp#2 should be SYS-FW binary.

For HS-FS and HS-SE non-Prime devices, Comp#1 should be SBL binary, Comp#2 should be SYS-FW Inner Certificate, and Comp#3 should be SYS-FW binary.

5.7.5.6 Memory Load Sections Overlap with Executable Components

Memory load sections for SBL and SYS-FW (CompType 0x11 and 0x12) the destination address and size should not overlap with the corresponding load and execute sections, and should also fall in the allowed memory range by ROM.

5.7.5.7 Device Type and Extended Boot Extension

X509 Extension	Component	GP Device	HS-FS	HS-SE non-prime	HS-SE Prime Device
ext_boot_info	Comp#1	SBL Binary	SBL Binary	SBL Binary	SBL Binary
	Comp#2	SYS-FW binary	SYS-FW binary	SYS-FW binary	SYS-FW binary
	Comp#3	SBL mem load section	SBL mem load section	SBL mem load section	SBL mem load section
	Comp#4	SysFW mem load section	SysFW mem load section	SysFW mem load section	SysFW mem load section
	Comp#5	N/A	SysFW inner certificate	SysFW inner certificate	N/A
ext_enc_info	Comp#1	N/A	N/A1	SBL encryption	SBL encryption
	Comp#2			N/A	SYS FW encryption
	Comp#3			SBL memory load Encryption	SBL memory load encryption
	Comp#4			Sys-FW memory load encryption	Sys-FW memory load encryption
	Comp#5			N/A1	NA

1. SYS-FW encryption in HS-FS and HS-SE (non Prime) are handled in SYS-FW Inner certificate and they are not part of the extended boot info extensions.

5.7.6 Generating X.509 Certificates

X.509 Certificates are generated using OpenSSL and a configuration script to supply values in the extension fields.

5.7.6.1 Key Generation

The SBL must always be signed with a given OpenSSL key - Secure and GP devices. Secure must have encryption and authentication, GP device must only have authentication. The key used for authentication can be random or specific. If a random key is generated and SBL is signed with this,the ROM will copy the SBL image for authentication using memcopy. With this key, ROM code will be directed to use DMA to load the SBL for authentication which saves boot time.

5.7.6.1.1 Degenerate RSA Keys

Degenerate RSA keys are valid RSA keys with the private exponent set to 1. This results in the signature field being equal to the digest, since in RSA:

$$\text{Signature} = \text{digestprivExp mod nprivExp mod n}^{\text{privExp}} \quad (1)$$

Where n is the key size. Since the hash used is SHA-512 and the signature is an ASN.1 sequence containing the OID defining which has was used as well as the hash value, the degenerate RSA must have a value of n greater than the maximum digest size. Typically 1024-bit is chosen.

The following sequence is used to generate degenerate RSA keys:

1. Create a random RSA key:

```
openssl genrsa -out key.pm 1024
```

2. Convert to text:

```
openssl rsa -in key.pem -text -noout > key.txt
```

3. Create an asn1 template for the degenerate key called degenerateKey.txt. Simply copy the values for modulus, prime (listed as p in key.txt), prime 2 (listed as q), and coefficient (listed as coeff). Set the public and private key exponents to 1, as well as the values for e1 and e2. See the example below.
4. Convert the template to DER:

```
openssl asn1parse -genconf degenerateKey.txt -out degenerateKey.der
```

5. Sanity check the key:

```
 openssl rsa -in degenerateKey.der -inform der -text -check
```

6. If there are no errors create the degenerate key pem file:

```
openssl rsa -in degenerateKey.der -inform der -outform pem -out degenerateKey.pem
```

An example degenerateKey.txt file is shown.

```
asn1=SEQUENCE:rsa_key
[rsa_key]
version=INTEGER:0
modulus=INTEGER<copied from key.txt>
pubExp=INTEGER:1
privExp=INTEGER:1
p=INTEGER:<copied from key.txt>
q=INTEGER<copied from key.txt>
e1=INTEGER:1
e2=INTEGER:1
coeff=INTEGER<copied from key.txt>
```

Note that when copying the multi-byte fields from key.txt it is necessary to remove the colons, catenate the lines and add a preceding 0x.

5.7.6.2 Configuration Script

An example openssl configuration script is shown below. Not all extensions are required, but all possible are shown.

```
[ req ]
distinguished_name = req_distinguished_name
x509_extensions = v3_ca
prompt = no
dirstring_type = nobmp
[ req_distinguished_name ]
C = GB
ST = HI
L = Boston
O = Texas Instruments., Inc.
```

```
OU = DSP
CN = Bob
emailAddress = Bob@hou.ti.com
[ v3_ca ]
basicConstraints = CA:true
1.3.6.1.4.1.294.1.1 = ASN1:SEQUENCE:boot_seq
1.3.6.1.4.1.294.1.2 = ASN1:SEQUENCE:image_integrity
1.3.6.1.4.1.294.1.3 = ASN1:SEQUENCE:swrv
1.3.6.1.4.1.294.1.4 = ASN1:SEQUENCE:encryption
1.3.6.1.4.1.294.1.5 = ASN1:SEQUENCE:key_derivation
1.3.6.1.4.1.294.1.7 = ANSI:SEQUENCE:pllControl
1.3.6.1.4.1.294.1.8 = ANSI:SEQUENCE:debug
[ boot_seq ]
certType =INTEGER:1
bootCore = INTEGER:16
bootArchWidth = INTEGER:32
destAddr = FORMAT:HEX,OCT:bc934b00
imageSize = INTEGER:0x00004860
[ image_integrity ]
shaType = OID:1.3.14.3.2.26
shaValue = FORMAT:HEX,OCT:4cf4d59ef77b5d9ab28d2ceb3c9fe83cb52ae6d2
[ swrv ]
rollback = INTEGER:0x00010001
[ encryption ]
Iv =FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
Rstring = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff101112131415161718191a1b1c1d1e1f
Icount = INTEGER:1
Salt = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
[ pllControl ]
pll0_num = INTEGER:0
pll0_cfg = FORMAT:HEX,OCT:00345678900
pll1_num = INTEGER:1
pll0_cfg = FORMAT:HEX,OCT:00345678900
[ debug ]
uid = FORMAT:HEX,OCT:00345678900
type = INTEGER:1
dbgE = INTEGER:0
secDbgEn = INTEGER:0
```

The certificate is then generated using the following openssl command:

```
openssl req -new -x509 -key <private_key_pem_file> -nodes -out <output_X.509_pem_file> -config
<config_file> -sha512
```

If a delegate key is being signed, then add the option -signkey <sign_key_pem_file> to the command above.

5.7.6.3 Image Data

The image data (blob) is considered simply as a byte stream. On devices that are multiple bytes wide the image must be formatted so that all multi-byte fields match the endianness of the device. The R5 will always run in little endian mode.

5.8 Boot Memory Maps

5.8.1 Memory Layout/MPU

Memory Layout/MPU shows an overview of the MPU configuration. In the R5 MPU, higher numbered regions have priority, therefore in the table, where two regions overlap, the region on the right defines the memory attributes.

5.8.2 Global Memory Addresses Used by ROM Code

The ROM code uses several global memory addresses that are useful for debugging. They are shown in Global Memory Addresses.

Table 5-65. Global Memory Addresses

Group	Address	Size (bytes)	Content
SMS0_HSM_SRAM0_0	0x43c00000	0x3e000	Loadable memory space for SBL
Warning/Error logs	0x43c3e480	0x200	Warning Entries
Warning/Error logs	0x43c3e680	0x200	Severe Entries
Warning/Error logs	0x43c3e880	0x100	Critical Entries
Warning/Error logs	0x43c3eb80	0x14	Circular message buffer
Warning/Error logs	0x43c3eb98	0x50	Boot log context
Trace	0x43c3ebe8	0x18	Boot trace context
Trace	0x43c3ec00	0x400	Boot trace entry buffers
Parameter tables	0x43c3f290	0x4	Parameter tables index for R5 bootloader
Parameter tables	0x43c3f298	0x400	Boot Parameter table for R5 bootloader
Parameter tables	0x43c3f1e0	0xb0	Extended boot data for R5 bootloader

The ROM code version information is a structure shown in Table 5-66

Table 5-66. ROM Code Version

Field	Address	Size (bytes)	Value for PG1
Version Number	0x4182_FF80	0x4	TBD
Version Date	0x4182_FF84	0x8	"TBD"
Device Name	0x4182_FF8C	0xC	"TBD"
Commit ID	0x4182_FF98	0x28	"TBD"

Chapter 6

Device Configuration

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6.1 Control Module

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

6.1.1 Memory Mapped Control Register Modules (CTRL_MMR)

This chapter covers three categories of device level control register modules:

- General-Purpose Control Register Modules
- Pad Configuration Register Modules
- Security Control Register Modules

Each category of module is described in its own section, along with detailed register descriptions for each module.

6.1.2 General Purpose Control Register Modules Functional Description

6.1.2.1 Description for General Purpose Control Register Module Register Types

The following sub-sections provide summary and description for most of the registers which are part of the CTRL_MMR0, WKUP_CTRL_MMR0 and MCU_CTRL_MMR0 modules memory spaces. The rest of the registers are described in the corresponding chapters where the functionality associated with particular register is covered in more detail.

6.1.2.1.1 Pad Configuration Registers

The pad configuration registers are used to configure most of the device pads. Each pad configuration register is associated with one pad and has bits as described in *Pad Configuration Register Functional Description*.

Many of the device pads support pad multiplexing. This means that their function can be independently chosen from two or more options. The selection of functions available on each pad is enumerated in table “Pin Multiplexing” of the device-specific Datasheet. The desired function is selected via the MUXMODE field of the associated pad configuration register.

The PADCFG_CTRL0_MMR_CFG0_PADCONFIGx registers control the signal multiplexing of modules in the device MAIN domain.

Note

It is recommended to first configure the PADCONFIG and debounce, as well as the debounce counter values in the SoC MMR, prior to enabling the IP.

6.1.2.1.2 Kick Protection Registers

There are Kick and Proxy registers associated with each CTRL_MMR register partition. This section describes the Kick registers. For information about the Proxy registers see Proxy Addressing Registers.

The Kick registers provide a protection mechanism which prevents spurious writes from changing the values of its registers. The LOCKi_KICK0 and LOCKi_KICK1 registers are used for this purpose. A write is required first to the LOCKi_KICK0[31-1] KEY field and then to the LOCKi_KICK1[31-0] KEY field with exact data values to unlock the protection mechanism. Once released then all registers within Partition "i" having write permissions can be written to. The read only registers are still read only. An indication for unlocked Partition "i" is when the LOCKi_KICK0[0] UNLOCKED bit is set to 1h. When the protection mechanism is locked (indicated by LOCKi_KICK0[0] UNLOCKED = 0h) none of the registers within Partition "i" can be written to. They can only be read..

The key values for all partitions are:

- LOCKi_KICK0 Key: 68EF 3490h
- LOCKi_KICK1 Key: D172 BC5Ah

See *Kick Protection Registers* for Partition Unlock Values.

Writing any other data value to either of these registers locks the protection mechanism and blocks any writes to the registers that reside in Partition "i".

Note

In order to ensure that all registers from all partitions are write protected, software must always re-lock the protection mechanism after completing the register writes.

6.1.2.1.3 I/O Debounce Control Registers

Some device pads have debounce logic. The following MCU_CTRL_MMR0 registers are used to configure the debounce period as shown in Table 6-1.

Table 6-1. Debounce period

MCU_CTRL_MMR Debounce Register	PADCONFIGx[13-11] DEBOUNCE_SEL setting
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1	1h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2	2h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3	3h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4	4h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5	5h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6	6h

Note

The debounce logic is not associated with all signals that can be multiplexed on a pad. Only certain signals can use it.

For information about each signal that has associated debounce logic, see Signal Descriptions in the device Datasheet.

Note

It is recommended to first configure the PADCONFIG and debounce, as well as the debounce counter values in the SoC MMR, prior to enabling the IP.

For information about the PADCONFIGx registers, see *Pad Configuration Registers*.

Table 6-2 shows the debounce period values to load in the MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5-0] DB_CFG field.

Note

The debounce clock selection should happen before the consumer of the debounced signals is enabled as the clock multiplexers for the debounce logic are NOT glitch-free.

Table 6-2. Debounce Period Values

MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (32.768kHz(1))	Fast Inputs (25MHz(1))	MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (25MHz(1))	Fast Inputs (250MHz(1))
	Delay[ms]	Delay[µs]		Delay[µs]	Delay[ns]
0	bypassed	n/a	32	0.04	4
1	1.95	2.56	33	0.08	8
2	2.93	3.84	34	0.12	12
3	3.91	5.12	35	0.16	16
4	4.88	6.40	36	0.20	20
5	5.86	7.68	37	0.24	24
6	6.84	8.96	38	0.28	28
7	7.81	10.24	39	0.32	32
8	8.79	11.52	40	0.36	36
9	9.77	12.80	41	0.40	40
10	10.74	14.08	42	0.44	44
11	11.72	15.36	43	0.48	48
12	12.7	16.64	44	0.52	52

Table 6-2. Debounce Period Values (continued)

MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (32.768kHz(1))	Fast Inputs (25MHz(1))	MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (25MHz(1))	Fast Inputs (250MHz(1))
	Delay[ms]	Delay[μs]		Delay[μs]	Delay[ns]
13	13.67	17.92	45	0.56	56
14	14.65	19.20	46	0.60	60
15	15.63	20.48	47	0.64	64
16	16.6	21.76	48	0.68	68
17	17.58	23.04	49	0.72	72
18	18.55	24.32	50	0.76	76
19	19.53	25.60	51	0.80	80
20	20.51	26.88	52	0.84	84
21	21.48	28.16	53	0.88	88
	Delay[ms]	Delay[μs]		Delay[μs]	Delay[μs]
22	15.63	20.48	54	20.48	2.048
23	31.25	40.96	55	40.96	4.096
24	46.88	61.44	56	61.44	6.144
25	62.5	81.92	57	81.92	8.192
26	78.13	102.40	58	102.40	10.24
27	93.75	122.88	59	122.88	12.288
28	109.38	143.36	60	143.36	14.336
29	125	163.84	61	163.84	16.384
30	140.63	184.32	62	184.32	18.432
31	156.25	204.80	63	204.80	20.48

(1) These are the debounce logic clock frequencies.

6.1.2.1.4 Proxy Addressing Registers

There are Kick and Proxy registers associated with each CTRL_MMR partition. This section describes the Proxy registers. For information about the Kick registers see Kick Protection Registers.

The Proxy registers provide proxy addressing, allowing each of the CTRL_MMR registers to be accessed through two different addresses - Proxy0 and Proxy1. Each partition is 16KB. The first 8KB are for Proxy0 addresses, and the second 8KB are for Proxy1 addresses. The Proxy0 address is intended as the normal read and write access address. The Proxy1 address provides exclusive register write control.

When a bit from the P**x**_CLAIM**y**[31-0] PROXY1_CLAIMED field is set to 1h, a register becomes read-only at its Proxy0 address and may only be written through its Proxy1 address. The Proxy registers themselves may always be read through their Proxy0 address but may only be written through their Proxy1 address.

The **x** (representing the partition) and **y** indices can be calculated through the following equations:

- **x** = INT(HEX2DEC(address_offset)/16384))
- **y** = INT(MOD(HEX2DEC(address_offset),16384)/128)

where:

- INT() rounds down to the nearest integer
- HEX2DEC() converts from hexadecimal to decimal
- MOD() returns the reminder of HEX2DEC(address_offset)/16384

6.1.3 Security Control Register Modules

The following sections describe the CTRL_MMR0 and PADCFG_CTRL0_CFG0 modules.

6.1.3.1 Security Control Register Modules Overview

There are three Security Control Register Modules on the Device:

- MAIN_SEC_MMR0 for the MAIN domain
- MCU_SEC_MMR0 for the MCU domain
- WKUP_SEC_MMR0 for the WKUP domain

6.2 Power

This chapter describes the power-management architecture implemented in the device.

6.2.1 Power Management Overview

To provide a versatile architecture that supports multiple power-management techniques, the power management framework is built with three levels of resource management: clock, power, and voltage.

These management levels are enforced by defining the managed entities or building blocks of the power management architecture, called the clock, power, and voltage domains. A domain is a group of modules or subsections of the device that share a common entity (for example, common clock source, common voltage source, or common power switch).

To minimize device power consumption, the clocks can be gated (turned off), or the power to the modules can be switched off, when they are not in use. Independent power and clock control of sections of the device allows for turning on and off specific sections of the device without affecting other sections.

6.2.2 Power Control Modules

The Power Control Modules are divided into two sections, dependent on their functionality - Power Sleep Controller section and Device Manager section.

6.2.2.1 Power Sleep Controller (PSC)

6.2.2.1.1 PSC Architecture

Power Sleep Controller (PSC) is a control component to manage the power domain and module’s clock and reset transition. Each PSC module contains multiple power domains, within each power domain, it can contain multiple LPSC. Each LPSC can be used to manage the one or multiple module’s reset and clock stop status, see Figure 6-1.

Each power domain has a unique index, starting from number 0. The power domain 0 is a special power domain, which is always on. The status of power domain 0 can’t be changed after the device is out of reset.

Each power domain can have one or more Local Power Sleep Control (LPSC). Each LPSC in the same PSC has a unique index value as well. LPSC 0 is special, which user can’t change its status. LPSC 0 is always set to be enabled after the device is out of reset.

One LPSC can be used to control the reset and clock status for one or more modules. Some of the LPSC can be used to provide local reset function for the processors, such as A53 and R5 core. LPSC can also be used to manage the clock stop interface for the interfaces between two interconnect IPs. This is mainly used for providing isolation features required by some special features such as security isolation, functional safety isolation or reset isolation between different parts of the SoC.

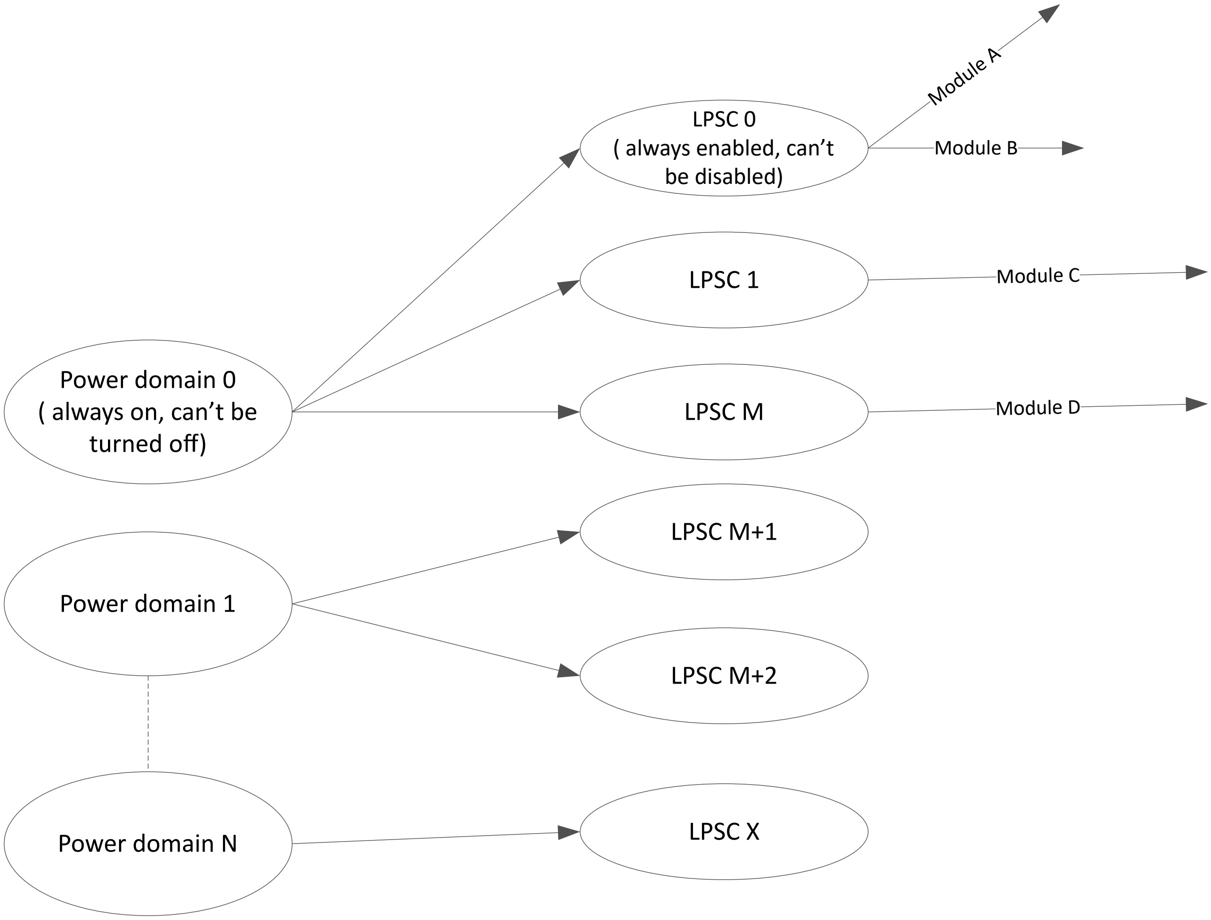

Figure 6-1. PSC Architecture

Note

PSC functions are controlled via Device Manager. For more information how to use Device Manager, see TISCI API available at ti.com.

6.2.2.1.2 PSC0 LPSC Features

Table 6-3. PSC0 LPSC Features

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CMP_EVENT_INTROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CTRL_MMR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAIN_GPIOMUX_INTROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PLL0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMESYNC_EVENT_ROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_CTRL_MMR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_WKUP_SEC_MMR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PADCFG_CTRL0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CPT2_AGGR1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC4

Table 6-3. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC6
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_TIMER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_TIMER1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ESM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GPIO0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GPIO1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_GTC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DDPA0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_VTM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_I2C0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PSRAMECC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PSRAMECC1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_PSRAMECC_8K0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_ROM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_RTCSS0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EFUSE0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	WKUP_UART0
PSC0	GP_CORE_CTL	LPSC_MAIN_DM	1	OFF	YES	WKUP_R5FSS0_CORE0
PSC0	GP_CORE_CTL	LPSC_MAIN_DM	1	OFF	YES	WKUP_RTI0
PSC0	GP_CORE_CTL	LPSC_DM_PBIST	2	ON	YES	WKUP_PBIST0
PSC0	GP_CORE_CTL	LPSC_DM_PBIST_1	8	ON	YES	WKUP_PBIST1
PSC0	GP_CORE_CTL	LPSC_MAIN_TEST	14	ON	YES	DFTSS0
PSC0	GP_CORE_CTL	LPSC_GPMC	15	OFF	YES	ELM0
PSC0	GP_CORE_CTL	LPSC_GPMC	15	OFF	YES	GPMC0
PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_0	17	OFF	YES	MCASP0
PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_1	18	OFF	YES	MCASP1
PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_2	19	OFF	YES	MCASP2
PSC0	GP_CORE_CTL	LPSC_EMMC_8B	20	OFF	YES	MMCSD0
PSC0	GP_CORE_CTL	LPSC_EMMC_4B_0	21	OFF	YES	MMCSD1
PSC0	GP_CORE_CTL	LPSC_EMMC_4B_1	22	OFF	YES	MMCSD2
PSC0	GP_CORE_CTL	LPSC_USB_0	23	OFF	YES	USB0
PSC0	GP_CORE_CTL	LPSC_USB_1	24	OFF	YES	USB1
PSC0	GP_CORE_CTL	LPSC_DPHY_0	26	OFF	YES	DPHY_RX0
PSC0	GP_CORE_CTL	LPSC_SMS_COMMON	27	ON	YES	MAIN_SEC_MMR0
PSC0	GP_CORE_CTL	LPSC_SMS_COMMON	27	ON	YES	MAILBOX0_MAILBOX_CLUSTER_0
PSC0	GP_CORE_CTL	LPSC_SMS_COMMON	27	ON	YES	SPINLOCK0
PSC0	GP_CORE_CTL	LPSC_FSS_OSPI	28	ON	YES	FSS0_FSAS_0
PSC0	GP_CORE_CTL	LPSC_FSS_OSPI	28	ON	YES	FSS0_OSPI_0
PSC0	GP_CORE_CTL	LPSC_SA3UL	31	ON	YES	SA3_SS0_DMSS_HSM_0
PSC0	GP_CORE_CTL	LPSC_SA3UL	31	ON	YES	SA3_SS0_SA_UL_0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	33	ON	YES	DBGSUSPENDROUTER0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	33	ON	YES	STM0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	33	ON	YES	DEBUGSS_WRAP0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	33	ON	YES	DEBUGSS0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	CPT2_AGGR0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_BCDMA_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_CBASS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_ECC_AGGR_0

Table 6-3. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_INTAGGR_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_IPCSS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_PKTDMA_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_PSILCFG_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_PSILSS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_RINGACC_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	DMASS0_SEC_PROXY_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER3
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER4
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER5
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER6
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	TIMER7
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	ECAP0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	ECAP1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	ECAP2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EQEP0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EQEP1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EQEP2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EPWM0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EPWM1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	EPWM2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	MCRC64_0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	I2C0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	I2C1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	I2C2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	I2C3
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	MSRAM_64K0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	PDMA2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	PDMA0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	PDMA1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	MCSPI0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	MCSPI1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	MCSPI2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART0
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART1
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART2
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART3
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART4
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART5
PSC0	GP_CORE_CTL	LPSC_MAIN_IP	34	ON	YES	UART6
PSC0	GP_CORE_CTL	LPSC_MAIN_MCANSS_0	35	OFF	YES	MCAN0
PSC0	GP_CORE_CTL	LPSC_GIC	36	ON	YES	GICSS0
PSC0	GP_CORE_CTL	LPSC_MAIN_PBIST	37	ON	YES	PBIST0
PSC0	PD_CPSW	LPSC_CPSW3G	42	OFF	YES	CPSW0
PSC0	PD_A53_CLUSTER_0	LPSC_A53_CLUSTER_0	43	OFF	YES	A53SS0
PSC0	PD_A53_CLUSTER_0	LPSC_A53_CLUSTER_0_PBIST_0	44	OFF	YES	COMPUTE_CLUSTER0_PBIST_0

Table 6-3. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	PD_A53_0	LPSC_A53_0	46	OFF	YES	RTI0
PSC0	PD_A53_0	LPSC_A53_0	46	OFF	YES	A53SS0_CORE_0
PSC0	PD_A53_1	LPSC_A53_1	47	OFF	YES	RTI1
PSC0	PD_A53_1	LPSC_A53_1	47	OFF	YES	A53SS0_CORE_1
PSC0	PD_A53_2	LPSC_A53_2	48	OFF	YES	RTI2
PSC0	PD_A53_2	LPSC_A53_2	48	OFF	YES	A53SS0_CORE_2
PSC0	PD_A53_3	LPSC_A53_3	49	OFF	YES	RTI3
PSC0	PD_A53_3	LPSC_A53_3	49	OFF	YES	A53SS0_CORE_3
PSC0	PD_C7X	LPSC_C7X_CORE	55	OFF	YES	RTI4
PSC0	PD_C7X	LPSC_C7X_CORE	55	OFF	YES	C7X256V0_C7XV_CORE_0
PSC0	PD_C7X	LPSC_C7X_PBIST	56	OFF	YES	C7X256V0_PBIST
PSC0	PD_C7X	LPSC_C7X_COMMON	57	OFF	YES	C7X256V0_CORE0
PSC0	PD_DDR	LPSC_EMIF_LOCAL	60	OFF	YES	DDR32SS0

6.2.2.1.3 WKUP_PSC0 LPSC Features

Table 6-4. WKUP_PSC0 LPSC Features

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_CTRL_MMR0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	WKUP_MCU_GPIOMUX_INTROUTER0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	WKUP_PLL0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_MCU_SEC_MMR0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_PADCFG_CTRL0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_DCC0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_DCC1
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	WKUP_ESM0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_GPIO0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_R5	6	OFF	YES	MCU_R5FSS0_CORE0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_R5	6	OFF	YES	MCU_RTI0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_MCANSS_0	7	OFF	YES	MCU_MCAN0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_MCANSS_1	8	OFF	YES	MCU_MCAN1
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_CPT2_AGGR0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_TIMER0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_TIMER1
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_TIMER2
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_TIMER3
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_MCRC64_0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_I2C0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_MSRAM_256K0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_MSRAM_256K1
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_MCSPI0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_MCSPI1
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	MCU_UART0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_PBIST	10	ON	YES	MCU_PBIST0

6.2.2.1.4 Software Sequence to enable an IP through PSC

In order to enable a module, user needs to program the PSC to put LPSC into enable state. There is dependence between power domain and LPSC and among different LPSC controls.

First of all, in order to enable any LPSC, the power domain which that LPSC belongs needs to be enabled first. The LPSC can't put into any state other than disable if the power domain is not enabled.

Among different LPSC, there is also a special sequence needs to be followed to make sure the device is not getting into undefined state.

Similarly, a special sequence shall be followed to disable the LPSC to prevent device getting into undefined states. Before a power domain can be turned off, all the LPSCs within that power domain shall be disabled first. Normally, user can turn off the power domain to save power. However, it is not necessary to turn off the power domain when all the LPSCs inside that power domain are disabled.

Figure 6-2 shows how to understand the dependent relationship between two LPSCs. In order to enable LPSC_2, LPSC_1 shall be enabled first.

If user wants to disable LPSC_1, LPSC_2 shall be disabled first.

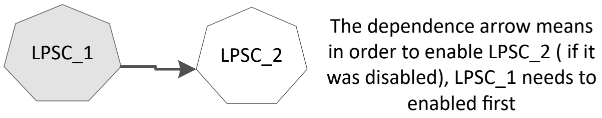

The dependence arrow means in order to enable LPSC_2 (if it was disabled), LPSC_1 needs to enabled first

Figure 6-2. LPSC Dependence

Figure 6-3 shows the dependent relationship among all the LPSCs in the device.

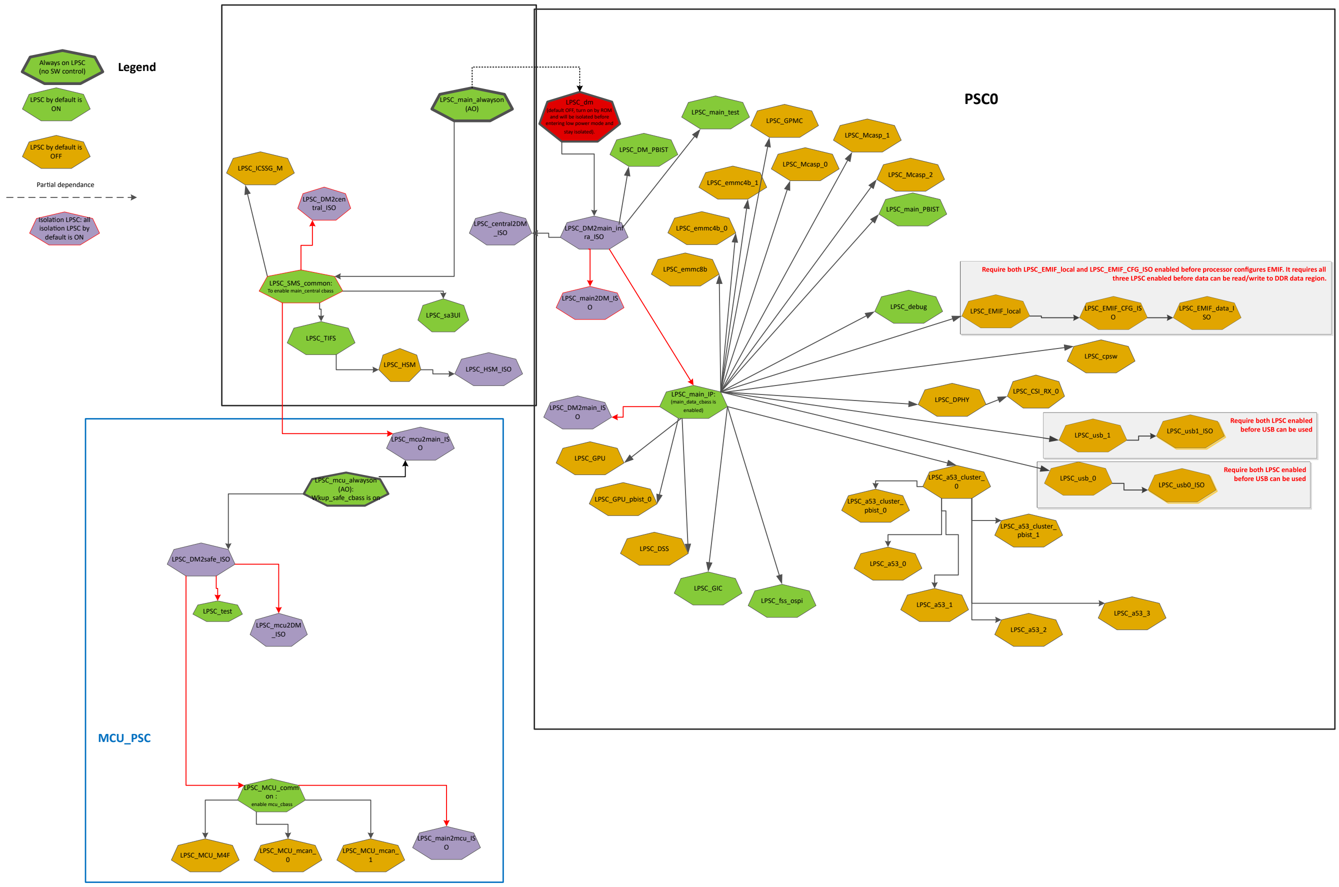

Figure 6-3. LPSC Dependency Tree

6.2.2.2 Device Manager

The device has one Device Manager located in WKUP domain. Device Manager is responsible for entry/exit to low power modes. Also, Device Manager hosts RM/PM (Resource Manager/Power Manager) SYSFW code for providing RM/PM services to HLOS. As part of boot, public ROM is executed over Device Manager.

Device Manager Features

- Single Core Cortex-R5 subsystem
  - ARMv7-R architecture with following extensions
    - Advanced SIMD extension for integer and floating-point vector operations
    - Vector Floating Point Version 3 (VFPv3)
  - L1 memory architecture
    - 32KB I-cache with 64-bit ECC error checking
    - 32KB D-cache with 64-bit ECC error checking
  - 64Kbyte TCM(L2) with 32-bit ECC error checking
  - 32-bit AXI3 initiator interface for accessing local peripherals
- 1x RTI/WWDT
- 2x Timer
- 1x UART
- 1x I2C
- Wake-up logic
- Public ROM
- RTC digital
- VTM
- LFOSC

Note

PSC functions are controlled via Device Manager. For more information how to use Device Manager, see TISCI API available at ti.com.

6.2.3 Power Management Techniques

The following section describes the power management techniques supported by the processor.

6.2.3.1 Dynamic Frequency Scaling (DFS)

DFS is a power management technique where the operating frequency is dynamically scaled across device Operating Performance Points (OPP). An OPP is a voltage/frequency pair that defines a specific power consumption operating condition (specific power state.) For each OPP, software controls clock frequency in order to adjust the performance and power to the optimum point. The Device supports DFS for Cortex-A53 only.

6.2.3.2 OPP Low

The device supports lower bus frequency operation as OPP Low. The OPP Low must be configured at boot time. In OPP Low, the main CBASS clock frequency is reduced in half in order to lower active power consumption with reduced performance. The performance of some peripheral modules is limited or not available in this operating condition.

Refer to the device datasheet to determine the supported features and the clock frequency of cores, modules, and peripheral I/Os in OPP Low.

6.2.4 Power Modes

The following sections describe a high-level description of the different power modes of the device. Specific values are detailed in the device-specific data sheet. Note that not all modes are supported by software packages supplied by Texas Instruments.

Table 6-5. Low Power Modes

Low Power Modes	Wakeup Sources	Application State and Use Case
Partial IO	CANUART I/O Bank pins	The entire SoC is OFF except I/O pins in CANUART I/O Bank to maintain I/O wakeup capability from CANUART I/O Bank I/O pins.

Table 6-6. Voltage, Power and Clock Domain Status

Low Power Modes	Voltage Domain				Power Domain								Clocks		DDR
	VDD_CORE / VDDR_CORE	VDDS_DDR	1.8 Analog Rails	1.8V/3.3V I/O Rails	GP_Core_CTL	PD_ICSSM	PD_CPSW	PD_A53_cluster_0	PD_A53_x	PD_GPU	PD_DSS	GP_Core_CTL_MCU	Main OSC	DPLLs	
Partial IO	OFF	OFF	OFF	Partial On	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

6.2.4.1 Partial IO

In Partial IO, I/O pins and small logics in the CANUART I/O Bank are active, and the rest of the SoC is turned off. The user can use the I/O pins to aggregate multiple I/O wakeup events and toggle PMIC_LPM_EN pin to enable PMIC or discrete power solution when an I/O wakeup event is triggered. The information on the I/O wakeup event is logged in the MMR in the CANUART I/O bank and helps the software to distinguish between cold boot and wakeup to respond to the wakeup event faster.

6.2.4.2 IO Only + DDR

I/O only + DDR minimizes processor power by turning off all processor power supplies except the LVCMOS I/O power supply while keeping LPDDR4 in self-refresh. System power state transitions, including power supply control, can be performed by a single interface signal (PMIC_LPM_EN signal) with PMIC register programming. The implementation of I/O only + DDR mode is shown in Figure 6-4

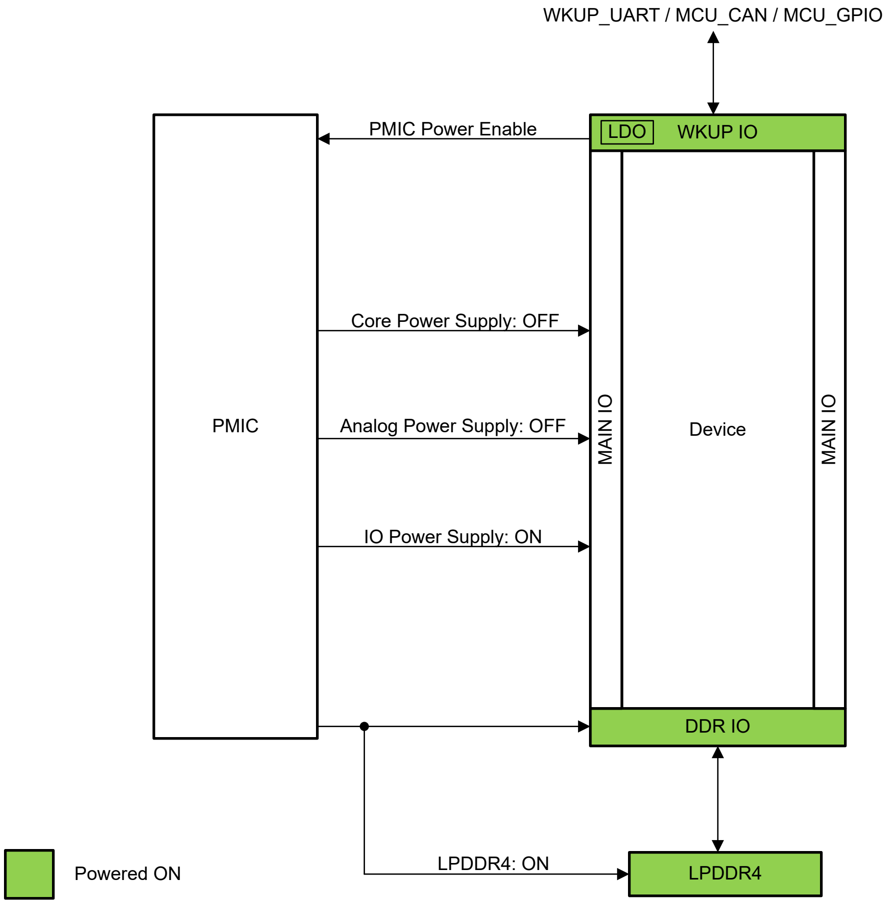

Figure 6-4. IO Only + DDR SR Mode

I/O Only + DDR Self Refresh Features:

- On a signal toggle at a pin in the wakeup IO bank, PMIC power enable signal is toggled to start PMIC power up sequence to power up SoC to active state.
- Suspend to RAM with the lowest system power
  - Processor with only I/O power supply ON
  - PMIC in suspend state
  - DDR in self refresh
- System can resume back to the state before suspend
- Suspend Events: Linux suspend command with programming PMIC and a wakeup I/O register
- Resume Events: Wakeup I/O toggle (WKUP_UART, MCU_CAN, and select MCU_GPIO)

6.2.4.3 Wakeup Sources/Events

Table 6-7 shows the wake sources supported in each low power mode.

Table 6-7. Low Power Mode Wakeup Events

Low Power Modes	Wakeup Events
Partial IO	CANUART I/O Bank pins

6.2.5 Power Supply Modules

6.2.5.1 Power OK (POK) Modules

Note

All POK modules are in MCU domain regardless of the domain of the voltage they monitor.

Note

In this family of devices, the Power-on-reset module is used only for voltage monitoring, as three additional POK modules. For more information about POK functionality in POR module - voltage being monitored and type (under voltage or over voltage), see Section 6.2.5.2 .

POK modules are responsible for accurately detecting the voltage levels. Each module is trimmed to account for process and temperature variations. The trim values are provided by eFuse chains enabled by a POR/Reset Generator (PRG) module.

Two types of POK modules are implemented in this family of devices - POK and POK_SA. See Table 6-8 about the type of a POK and the voltage it is monitoring. More information about the two types of POKs is given further in this section.

Table 6-8. POK Module Overview

POK Module Instance Name	PRG Index (3)	POK Index (1)	Voltage Monitored	Module Type	OV/ UV(2)	Description
IPOK_VDD_CORE_OV	PRG0	4	VDD_CORE	POK_CORE	OV	Voltage Monitor for VDD_CORE
IPOK_VDDA_PMIC_IN_UV	PRG0	3	VMON_ER_VSYS	POK_SA	UV	Voltage Monitor for PMIC_IN
IPOK_VDDS_DDRIO	PRG1	4	VDDS_DDR	POK_CORE	UV/OV	Voltage Monitors for DDRIO
IPOK_VDDR_CORE	PRG1	3	VDDR_CORE	POK_CORE	UV/OV	Voltage Monitors for VDDR_CORE
IPOK_VDDS_CAP_MCU	PRG1	2	CAP_VDDS_MCU	POK_CORE	UV/OV	Voltage Monitors for MCU mid-rail
IPOK_VDDS_MCU_1P8	PRG1	1	VMON_1P8_SOC	POK_1P8	UV/OV	Voltage Monitors for 1.8-V I/O supply in MCU
IPOK_VDDSHV_MCU_3P3	PRG1	0	VMON_3P3_SOC	POK_3P3	UV/OV	Voltage Monitors for 3.3-V I/O supply in MCU

(1) The POK Index also represents the mapping index for relevant under and overvoltage status and interrupts where applicable.

(2) UV: POK is set for undervoltage detection. OV: POK is set for overvoltage detection. UV/OV: POK monitors both OV and UV through a Ping-Pong mechanism.

(3) Ping-pong mechanism is only applicable to PRG1.

Figure 6-5 and Figure 6-6 represent the block diagrams of the two POK types.

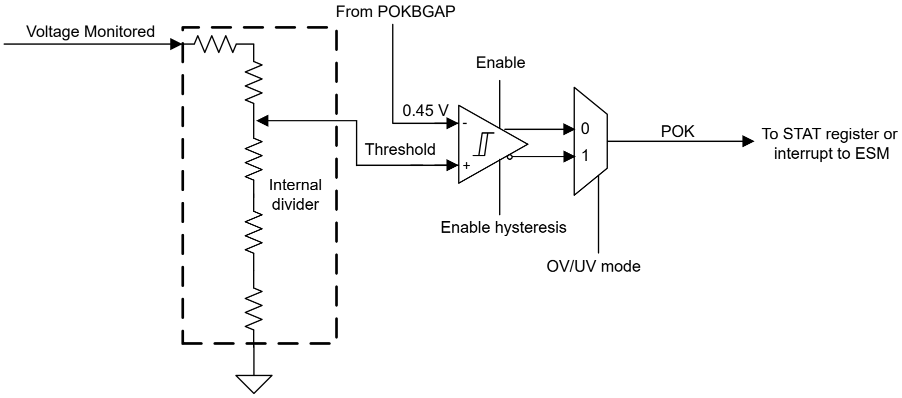

Figure 6-5. POK Block Diagram

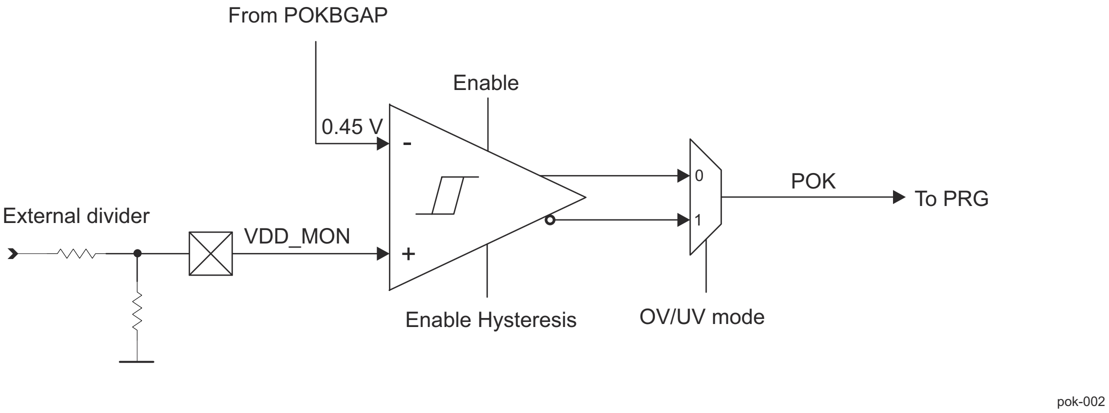

Figure 6-6. POK_SA Block Diagram

Vref for both POK and POK_SA types in Figure 6-5 and Figure 6-6 is supplied from POK module, see Section 6.2.5.2

6.2.5.1.1 Configuration Registers

Configuration registers needed for POK (Supervisor Module) are given in Table 6-9. For each POK there is one comparator that is controlled through the registers. These registers decide the functionality of the POK Comparator. It decides if it is UV/OV mode and also the threshold voltages.

Comparator threshold levels and corresponding configuration register settings are given in the following tables:

- POK_CORE: Table 6-10
- POK_1P8: Table 6-11
- POK_3P3: Table 6-12

Table 6-9. POK Configuration Registers

Register Name	POK Type
MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL[7:0]	POK_CORE

Table 6-10. Bit Settings of POK_CORE with VMON Threshold Values

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	000 0000	0.4743
	0	000 0001	0.4875
	0	000 0010	0.5000
	0	000 0011	0.5125
	0	000 0100	0.5250
	0	000 0101	0.5375
	0	000 0110	0.5513
	0	000 0111	0.5631
	0	000 1000	0.5754
	0	000 1001	0.5883
	0	000 1010	0.6017
	0	000 1011	0.6122
	0	000 1100	0.6268
	0	000 1101	0.6382
	0	000 1110	0.6500
	0	000 1111	0.6623
	0	001 0000	0.6750
	0	001 0001	0.6882
	0	001 0010	0.7020
	0	001 0011	0.7115
	0	001 0100	0.7262
	0	001 0101	0.7363
	0	001 0110	0.7521
	0	001 0111	0.7630
	0	001 1000	0.7742
	0	001 1001	0.7858
	0	001 1010	0.7977
	0	001 1011	0.8100
	0	001 1100	0.8226
	0	001 1101	0.8356
	0	001 1110	0.8491
	0	001 1111	0.8630
	0	010 0000	0.8774
	0	010 0001	0.8848
	0	010 0010	0.8999
	0	010 0011	0.9155
	0	010 0100	0.9235
	0	010 0101	0.9400
	0	010 0110	0.9485
	0	010 0111	0.9659
	0	010 1000	0.9748
	0	010 1001	0.9839

Table 6-10. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	010 1010	1.0030
	0	010 1011	1.0120
	0	010 1100	1.0220
	0	010 1101	1.0320
	0	010 1110	1.0530
	0	010 1111	1.0630
	0	011 0000	1.0740
	0	011 0001	1.0850
	0	011 0010	1.0970
	0	011 0011	1.1140
	0	011 0100	1.1260
	0	011 0101	1.1380
	0	011 0110	1.1510
	0	011 0111	1.1630
	0	011 1000	1.1760
	0	011 1001	1.1900
	0	011 1010	1.1960
	0	011 1011	1.2100
	0	011 1100	1.2240
	0	011 1101	1.2380
	0	011 1110	1.2530
	0	011 1111	1.2610
	0	100 0000	1.2760
	0	100 0001	1.2920
	0	100 0010	1.3000
	0	100 0011	1.3160
	0	100 0100	1.3240
	0	100 0101	1.3410
	0	100 0110	1.3500
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	000 0000	0.7262
	1	000 0001	0.7363
	1	000 0010	0.7521
	1	000 0011	0.7630
	1	000 0100	0.7743
	1	000 0101	0.7858
	1	000 0110	0.7977
	1	000 0111	0.8100
	1	000 1000	0.8226
	1	000 1001	0.8357
	1	000 1010	0.8491
	1	000 1011	0.8630
	1	000 1100	0.8774

Table 6-10. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	000 1101	0.8848
	1	000 1110	0.8999
	1	000 1111	0.9155
	1	001 0000	0.9236
	1	001 0001	0.9400
	1	001 0010	0.9485
	1	001 0011	0.9659
	1	001 0100	0.9748
	1	001 0101	0.9839
	1	001 0110	1.0030
	1	001 0111	1.0120
	1	001 1000	1.0220
	1	001 1001	1.0320
	1	001 1010	1.0530
	1	001 1011	1.0630
	1	001 1100	1.0740
	1	001 1101	1.0850
	1	001 1110	1.0970
	1	001 1111	1.1140
	1	010 0000	1.1260
	1	010 0001	1.1380
	1	010 0010	1.1510
	1	010 0011	1.1630
	1	010 0100	1.1760
	1	010 0101	1.1900
	1	010 0110	1.1960
	1	010 0111	1.2100
	1	010 1000	1.2240
	1	010 1001	1.2380
	1	010 1010	1.2530
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	010 1011	1.2610
	1	010 1100	1.2760
	1	010 1101	1.2920
	1	010 1110	1.3000
	1	010 1111	1.3160
	1	011 0000	1.3240
	1	011 0001	1.3410
	1	011 0010	1.3500
	1	011 0011	1.3670
	1	011 0100	1.3760
	1	011 0101	1.3850
	1	011 0110	1.4040

Table 6-10. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	011 0111	1.4130
	1	011 1000	1.4230
	1	011 1001	1.4420
	1	011 1010	1.4520
	1	011 1011	1.4620
	1	011 1100	1.4720
	1	011 1101	1.4830
	1	011 1110	1.5040
	1	011 1111	1.5150
	1	100 0000	1.5260
	1	100 0001	1.5370
	1	100 0010	1.5480
	1	100 0011	1.5600
	1	100 0100	1.5710
	1	100 0101	1.5830
	1	100 0110	1.5950
	1	100 0111	1.6070
	1	100 1000	1.6200
	1	100 1001	1.6320
	1	100 1010	1.6450

Table 6-11. Bit Settings of POK_1P8 with VMON Threshold Values

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	0	010 0000	1.44
	0	010 0001	1.452
	0	010 0010	1.477
	0	010 0011	1.502
	0	010 0100	1.515
	0	010 0101	1.543
	0	010 0110	1.556
	0	010 0111	1.585
	0	010 1000	1.6
	0	010 1001	1.615
	0	010 1010	1.645
	0	010 1011	1.661
	0	010 1100	1.677
	0	010 1101	1.694
	0	010 1110	1.728
	0	010 1111	1.745
	0	011 0000	1.763
	0	011 0001	1.781
	0	011 0010	1.799
	0	011 0011	1.828
	0	011 0100	1.848
	0	011 0101	1.868
	0	011 0110	1.888
	0	011 0111	1.909
	0	011 1000	1.93
	0	011 1001	1.952
	0	011 1010	1.963
	0	011 1011	1.986
	0	011 1100	2.009
	0	011 1101	2.032
	0	011 1110	2.056
	0	011 1111	2.069
	0	100 0000	2.094
	0	100 0001	2.12
	0	100 0010	2.133
	0	100 0011	2.159
	0	100 0100	2.173
POK_1P8 (Under Voltage Detection) hys_en=0	1	000 1100	1.44
	1	000 1101	1.452
	1	000 1110	1.477
	1	000 1111	1.502
	1	001 0000	1.515

Table 6-11. Bit Settings of POK_1P8 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	1	001 0001	1.543
	1	001 0010	1.556
	1	001 0011	1.585
	1	001 0100	1.6
	1	001 0101	1.615
	1	001 0110	1.645
	1	001 0111	1.661
	1	001 1000	1.677
	1	001 1001	1.694
	1	001 1010	1.728
	1	001 1011	1.745
	1	001 1100	1.763
	1	001 1101	1.781
	1	001 1110	1.799
	1	001 1111	1.828
	1	010 0000	1.848
	1	010 0001	1.868
	1	010 0010	1.888
	1	010 0011	1.909
	1	010 0100	1.93
	1	010 0101	1.952
	1	010 0110	1.963
	1	010 0111	1.986
	1	010 1000	2.009
	1	010 1001	2.032
	1	010 1010	2.056
	1	010 1011	2.069
	1	010 1100	2.094
	1	010 1101	2.12
	1	010 1110	2.133
	1	010 1111	2.159
	1	011 0000	2.173

Table 6-12. Bit Settings of POK_3P3 with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	000 0000	1.427
	0	000 0001	1.466
	0	000 0010	1.501
	0	000 0011	1.545
	0	000 0100	1.576
	0	000 0101	1.616
	0	000 0110	1.658
	0	000 0111	1.694
	0	000 1000	1.731
	0	000 1001	1.769
	0	000 1010	1.81
	0	000 1011	1.841
	0	000 1100	1.885
	0	000 1101	1.919
	0	000 1110	1.955
	0	000 1111	1.992
	0	001 0000	2.03
	0	001 0001	2.07
	0	001 0010	2.111
	0	001 0011	2.14
	0	001 0100	2.184
	0	001 0101	2.215
	0	001 0110	2.262
	0	001 0111	2.295
	0	001 1000	2.329
	0	001 1001	2.363
	0	001 1010	2.399
	0	001 1011	2.436
	0	001 1100	2.474
	0	001 1101	2.513
	0	001 1110	2.554
	0	001 1111	2.596
	0	010 0000	2.639
	0	010 0001	2.661
	0	010 0010	2.706
	0	010 0011	2.753
	0	010 0100	2.778
	0	010 0101	2.827
	0	010 0110	2.853
	0	010 0111	2.905
	0	010 1000	2.932
	0	010 1001	2.959

Table 6-12. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	010 1010	3.015
	0	010 1011	3.044
	0	010 1100	3.074
	0	010 1101	3.104
	0	010 1110	3.166
	0	010 1111	3.198
	0	011 0000	3.231
	0	011 0001	3.264
	0	011 0010	3.298
	0	011 0011	3.35
	0	011 0100	3.386
	0	011 0101	3.423
	0	011 0110	3.46
	0	011 0111	3.498
	0	011 1000	3.538
	0	011 1001	3.577
	0	011 1010	3.598
	0	011 1011	3.639
	0	011 1100	3.681
	0	011 1101	3.724
	0	011 1110	3.769
	0	011 1111	3.791
	0	100 0000	3.837
	0	100 0001	3.884
	0	100 0010	3.908
	0	100 0011	3.957
	0	100 0100	3.982
POK_3P3 (Over Voltage Detection) hys_en=0	1	000 0000	2.184
	1	000 0001	2.215
	1	000 0010	2.262
	1	000 0011	2.295
	1	000 0100	2.329
	1	000 0101	2.363
	1	000 0110	2.399
	1	000 0111	2.436
	1	000 1000	2.474
	1	000 1001	2.513
	1	000 1010	2.554
	1	000 1011	2.596
	1	000 1100	2.639
	1	000 1101	2.661
	1	000 1110	2.707

Table 6-12. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Over Voltage Detection) hys_en=0	1	000 1111	2.754
	1	001 0000	2.778
	1	001 0001	2.827
	1	001 0010	2.853
	1	001 0011	2.905
	1	001 0100	2.932
	1	001 0101	2.959
	1	001 0110	3.016
	1	001 0111	3.045
	1	001 1000	3.074
	1	001 1001	3.104
	1	001 1010	3.166
	1	001 1011	3.198
	1	001 1100	3.231
	1	001 1101	3.264
	1	001 1110	3.298
	1	001 1111	3.35
	1	010 0000	3.386
	1	010 0001	3.423
	1	010 0010	3.46
	1	010 0011	3.499
	1	010 0100	3.538
	1	010 0101	3.578
	1	010 0110	3.598
	1	010 0111	3.639
	1	010 1000	3.682
	1	010 1001	3.725
	1	010 1010	3.769
	1	010 1011	3.792
	1	010 1100	3.838
	1	010 1101	3.885
	1	010 1110	3.909
	1	010 1111	3.958

6.2.5.2 Power on Reset (POR) Module

This section describes the Power on Reset (POR) module.

6.2.5.2.1 POR Overview

POR module in this family of devices is responsible for detecting proper operating voltage levels on VDDA_MCU (under voltage), and both under and over voltages for analog supply in MCU domain.

Table 6-13 shows POR modules allocation within device domains.

Table 6-13. POR Modules Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
POR0	✓	-

6.2.5.2.2 POR Integration

The device supports one instance of a Power on Reset (POR) module - MCU_POR0. MCU_POR0 is located in MCU domain. Figure 6-7 shows the integration of MCU_POR0.

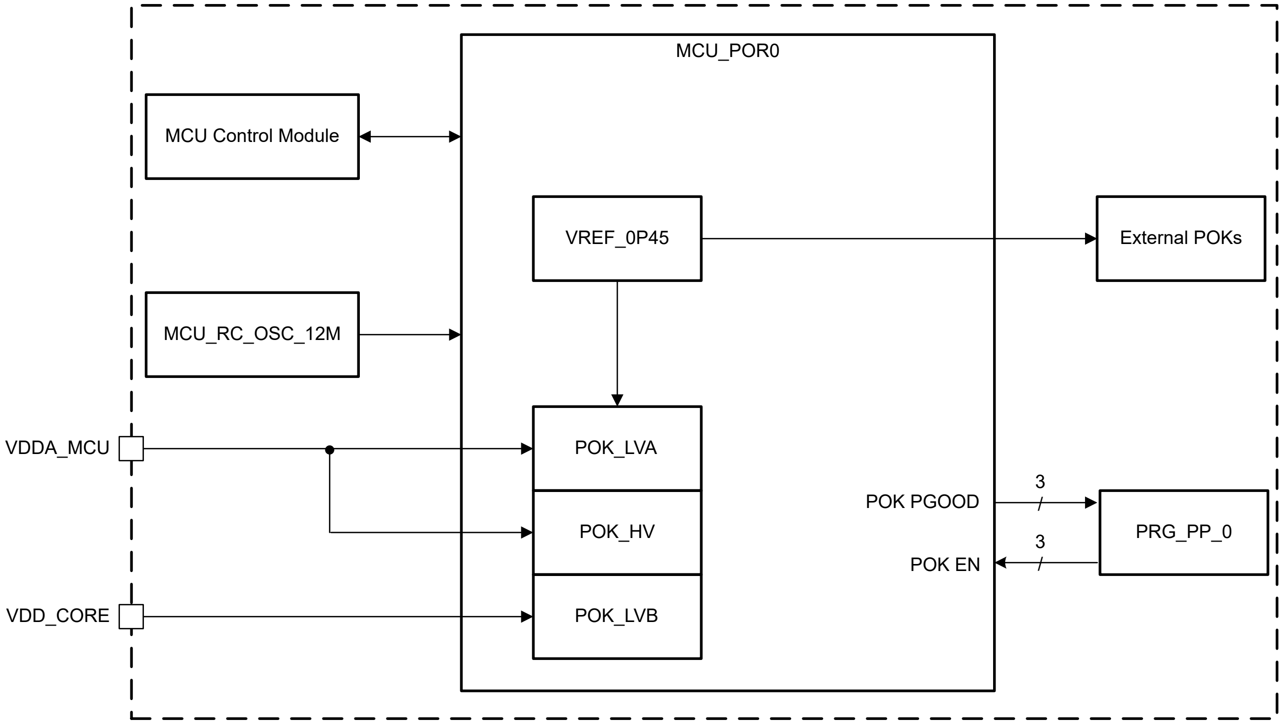

Figure 6-7. POR Integration

Table 6-14. POR Modules

POR Module Instance Name	PRG Index	POK Index	Voltage Monitored	Module Type	OV/ UV[(1)]	Description
POKHV	PRG0	2	VDDA_MCU	POR	UV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE
POKLVA	PRG0	1	VDDA_MCU	POR	OV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE
POKLVB	PRG0	0	VDD_CORE	POR	UV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE

(1) UV: POK is set for under voltage detection. OV: POK is set for over voltage detection. UV/OV: POK monitors both OV and UV via Ping-Pong mechanism.

6.2.5.3 PoR/Reset Generator (PRG) Modules

6.2.5.3.1 PRG Overview

A PRG module is responsible for implementing enable/disable controls and event/interrupt masking logic on all POK outputs.

Figure 6-8 shows the PRG module overview.

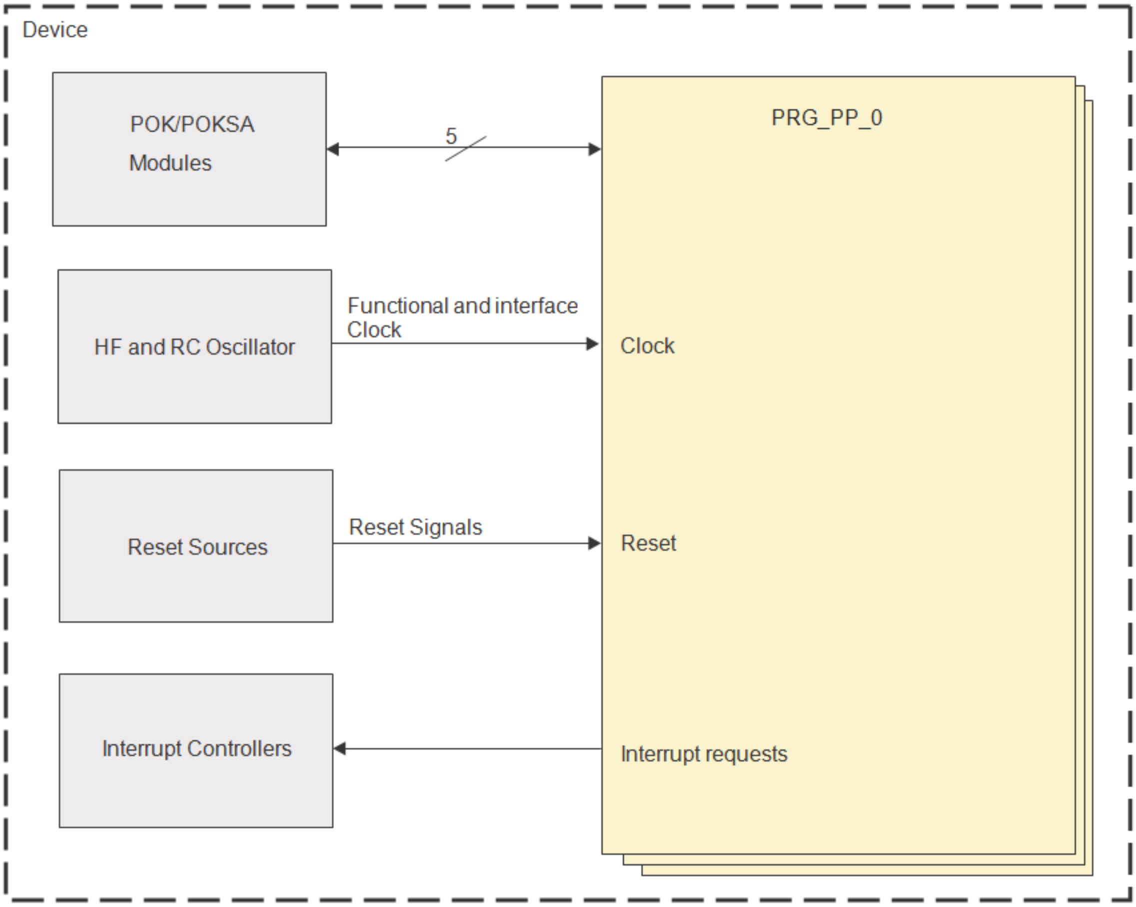

Figure 6-8. PRG0 Overview

Figure 6-9 shows the PRG module overview.

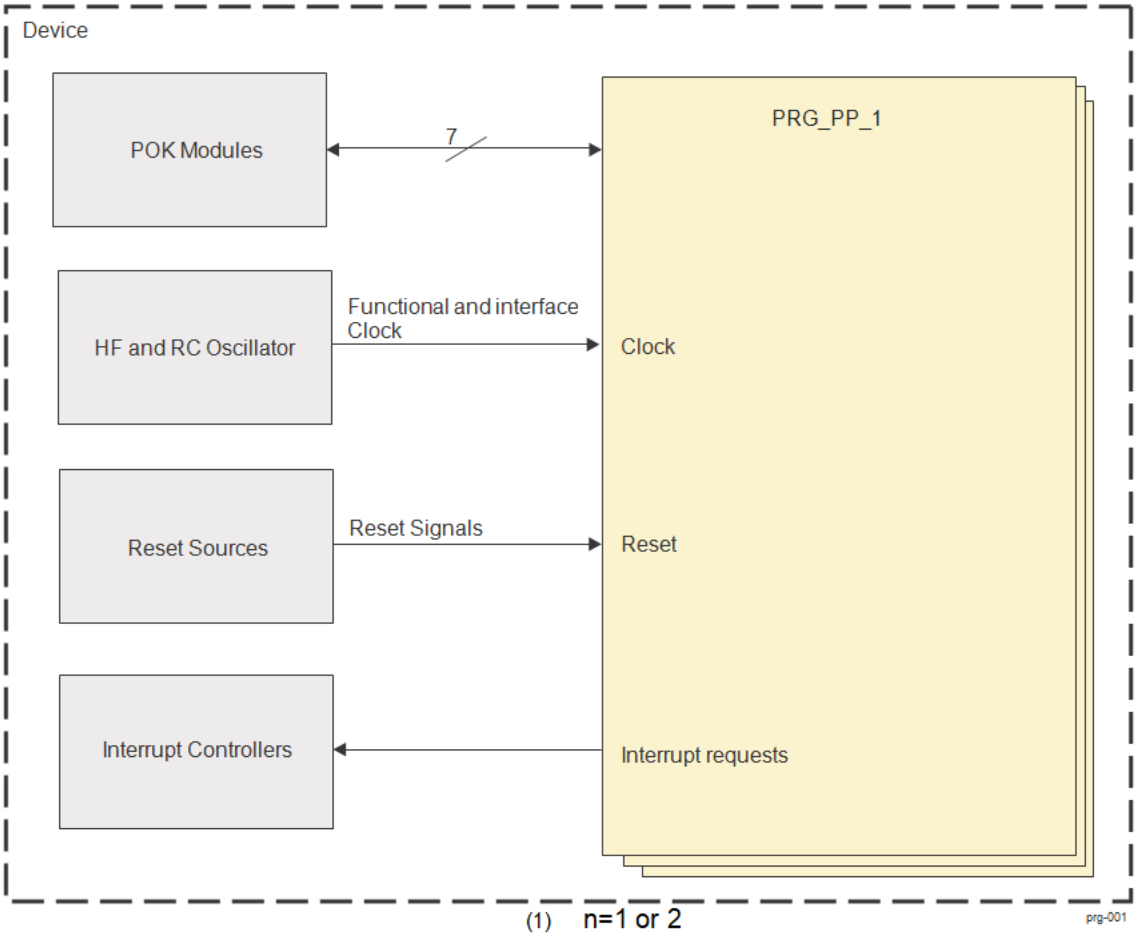

Figure 6-9. PRG1 Overview

6.2.5.4 Power Glitch Detect (PGD) Modules

A Power Glitch Detect (PGD) circuit is used to detect short duration “glitches” on the core and MPU power supplies. The PGD provides a low output when no glitch is detected and a high output when a glitch is detected.

Table 6-15 shows PGD modules allocation within device domains.

Table 6-15. PGD Allocation within Device Domains

Module Instance	Domain		
	WKUP	MCU	MAIN
IPGD_VDD_CORE	-	✓	-

Figure 6-10 shows the PGD block diagram.

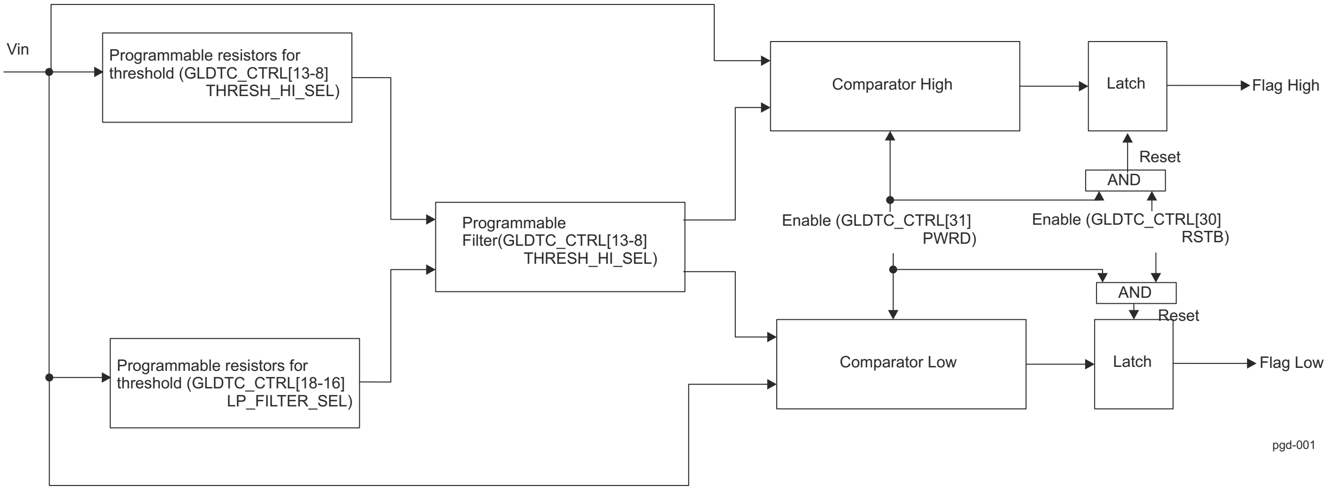

Figure 6-10. PGD Block Diagram

Table 6-16 Summarizes the PGD integration.

Table 6-16. PGD Integration Summary

Module Instance	Monitored Voltage	PGD Control/Status Registers(1)
IPGD_VDD_CORE	VDD_CORE	

(1) For more information about control registers, see , *Control Module (CTRL_MMR)*.

Note

A flag status bit in corresponding STAT register is cleared by clearing the [30] RSTB bit in the corresponding CTRL register, see for STAT and CTRL registers for a certain PGD module.

Note

For more information on the interconnects, see , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within , *Device Configuration*.

For more information on the device interrupt controllers, see , *Interrupt Controllers*.

6.2.5.5 Voltage and Thermal Manager (VTM)

6.2.5.5.1 VTM Overview

This section describes the Voltage and Thermal Manager (VTM) module in the device.

The VTM module supports voltage and thermal management of the device by providing control of on-chip temperature sensors.

The device supports a single VTM module, VTM0, which is located in the WKUP domain. VTM0 has three associated temperature monitors, Temp_Sensor_Main_0, Temp_Sensor_Main_1, and Temp_Sensor_Main_2, each of which are located near hotspots in the device die.

Figure 6-11 shows VTM module allocation within device domains.

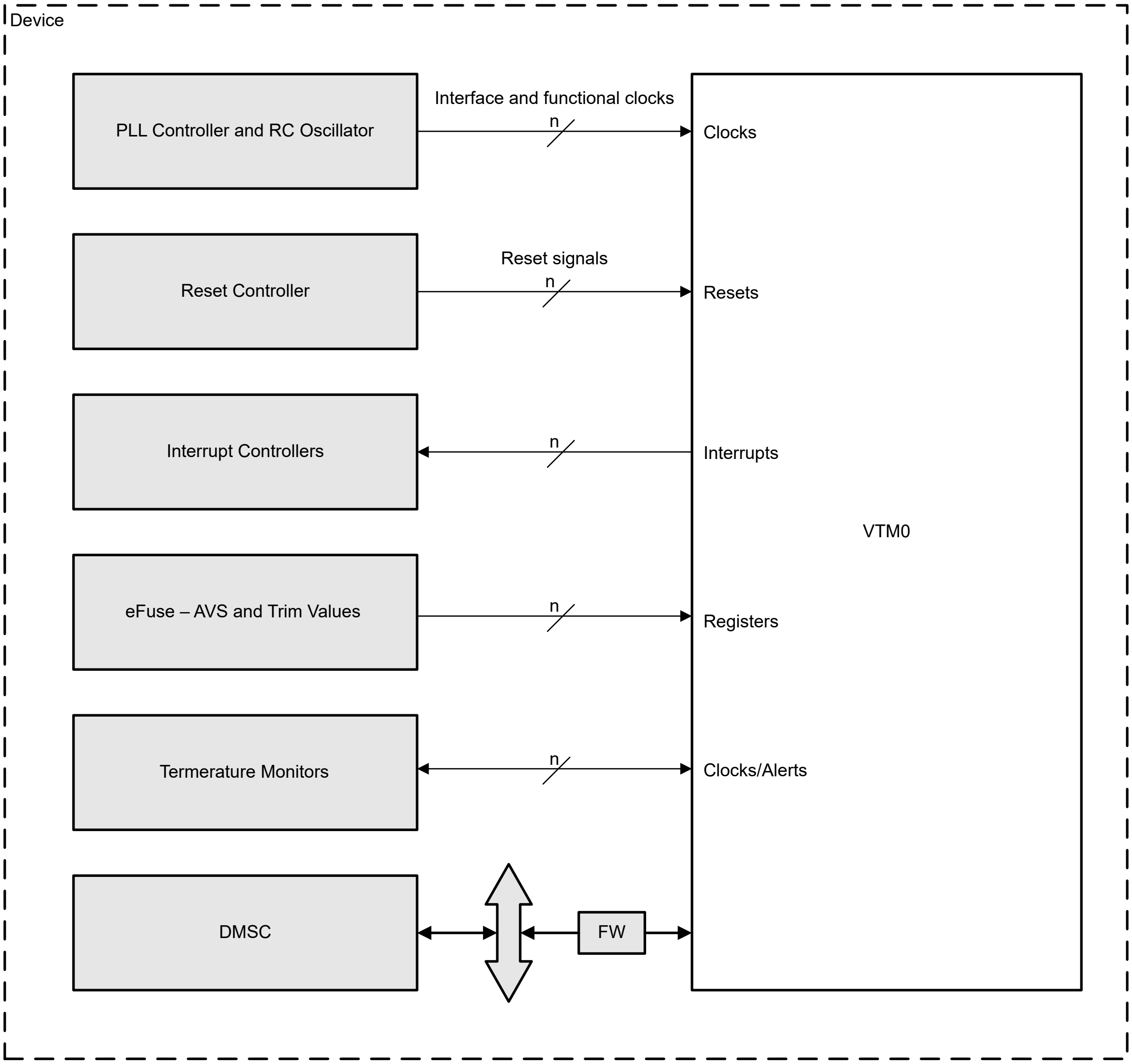

Figure 6-11. VTM Overview

6.2.5.5.1.1 VTM Features

VTM module supports the following features:

- Programming of temperature-crossing thresholds
- Signals when programed thresholds are exceeded - up to 3 alerts:
  - Three full reference 10-bit temperature threshold points, THPT1, THPT2 and THPT0.

  - Two relative 4-bit delta values vs THPT1 (one an increment and another a decrement), each able to set additional threshold point, THPT2 and THPT0.
- Supports up to 8 temperature monitors
- Allows resolution of 0.5°C for temperature reading and threshold point temperature alert/interrupt generation.
- Supports PMIC/LDO set-up with Class-0 VDD-VID settings
- Support of tentative customization of OPP voltage per device (in support of multiple OPPs)
- Maximum temperature alert
- Supports one shot sampling mode and continuous monitoring mode for the sensors
- Contains registers with reset defaults from e-fuse values needed to supports SR-Class0 via e-fuse/ manufacturing calibration and firmware and/or software using those values to program the PMIC/LDO with the Class-0 VDD-VID setting.
- Contains registers with reset defaults from e-fuse values per SOC for a tentative customization of OPP voltage per device (in support of multiple OPPs/DVFS).
- Core voltage domains that don't require any SR-Class0 or thermal management shall not be controlled or map to any of the MCU_VTM0 voltage domain group.
- Contains registers with reset defaults from e-fuse values or TIE-OFFs to provide control for temperature monitors and interrupt generation needed to support thermal management customized if necessary in a per voltage domain basis.
- Provides register control, status and interrupt generation, and alerts for up to 8 temperature monitors.
- Stores in the registers the defaults for temperature detection threshold points and other temperature monitor control values for Firmware usage.
- Samples, captures, and allows for register read of the on-die temperature monitor present reading.
- Provides interrupt and status for out of range temperature reading.
- Provides one full reference 10-bit temperature threshold point, THPT1.
- Provides 2 relative 3-bit delta values versus THPT1, one an increment and another a decrement, which yields 2 additional threshold points, THPT2 and THPT0, in close proximity to THPT1.
- Provides 3 temperature threshold point alert signals (level), GT_TH1_ALERT, GT_TH2_ALERT and LT_TH0_ALERT, for each one of the up to 8 temperature monitors.
- Provides 3 temperature threshold point interrupt flags, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, for each one of the up to 8 voltage domains.
- Provides 3 temperature threshold point interrupts (level-only) for the entire MCU_VTM0, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, which are driven out of MCU_VTM0 and are shared by the 8 voltage domains. The output port interrupts correspond to the OR function of the contributions of the 8 voltage domains.
- Software must read the corresponding flags in each of the 8 voltage domains to identify which voltage domain is active.
- Allows for temperature reading and threshold point temperature alert and interrupt generation with 0.5°C of resolution.

6.2.5.5.1.2 VTM Not Supported Features

- No support for AVS-Class0 with temperature compensation (AVS0 + TC)
- No support for K1 or K2 4/6-bit VCNTL/VID parallel or 2-step interfaces.
- No integrated I2C inside VTM
- No direct hardware triggering of I2C transactions by VTM. Only interrupt and event generation is supported.
- No support for voltage and thermal management of I/O voltage domains. Only core domain voltage/thermal management is supported.
- VTM0 does not contain or support register groups or control hooks for I/O voltage domains.
- Core voltage domains that do not require any voltage or thermal management are not controlled or mapped to any of the VTM0 voltage domain groups.
- Everything else not explicitly listed in Section 6.2.5.5.1.1 is not supported.
- No oversampling of the temperature reading
- No support for eFuse defaults of all register values

6.2.5.5.2 VTM Functional Description

6.2.5.5.2.1 VTM Temperature Status and Thermal Management

VTM module provides temperature reading and interrupt/alert information for thermal management.

6.2.5.5.2.1.1 10-bit Temperature Values Versus Temperature

Table 6-17 shows a table lookup method for translating code to temperature from temperature monitors which correspond to the temperature measured read from the VTM0_VTM_TMPSENS_STAT_J [9-0] DATA_OUT bitfields. Table 6-17 also provides the values for the temperatures coded in VTM0_VTM_MISC_CTRL2 [25-16] MAXT_OUTRG_ALERT_THR0 and VTM0_VTM_MISC_CTRL2 [9-0] MAXT_OUTRG_ALERT_THR thresholds.

Table 6-17. Temperature Translation Table

Parameter Type	Value								
Temperature [°C] (rounded)	-40	-25	0	25	50	75	100	125	150
Temperature [°C] (unrounded)	-40.03	-24.95	0.01	25.02	49.94	75.03	100.02	124.97	150.00
DATA_OUT Code	28	77	164	260	366	485	620	773	949

Table 6-18 shows a table that gives coefficients of polynomial to calculate code or temperature. The equation to calculate code or temperature is:

$y = a4 \times x^4 + a3 \times x^3 + a2 \times x^2 + a1 \times x + a0$

Table 6-18. Equation Method to Calculate Code or Temperature

Function	Unit	Coefficient				
		a4	**a3**	**a2**	**a1**	**a0**
Code = f(Temperature)	Decimal value of code	4.9847E-08	1.6972E-05	6.8759E-03	3.6509E+00	1.6407E+02
Temperature = f(Code)	°C	-9.2627E-12	6.0373E-08	-1.7058E-04	3.2512E-01	-4.9002E+01

6.2.5.5.2.2 VTM Temperature Driven Alerts and Interrupts

All 3 alerts from the temperature monitors are available as inputs of the mask and alert merging logic block of each voltage domain, such that the temperature monitors that are relevant to each voltage domain can be selected as the contributors to the generation of the 3 combined interrupts in each voltage domain (5 shown in sketch; 3). This logic is presented in Figure 6-12. The THERM_MAXTEMP_OUTRANGE_ALERT is not shown in this figure. Notice that the same temperature sensor can contribute to more than one voltage domain and each voltage domain can have multiple sensors contributing to the interrupt generation in that VD, see VTM_CFG1_VD_EVT_SET_j and VTM_CFG1_VD_EVT_CLR_j registers.

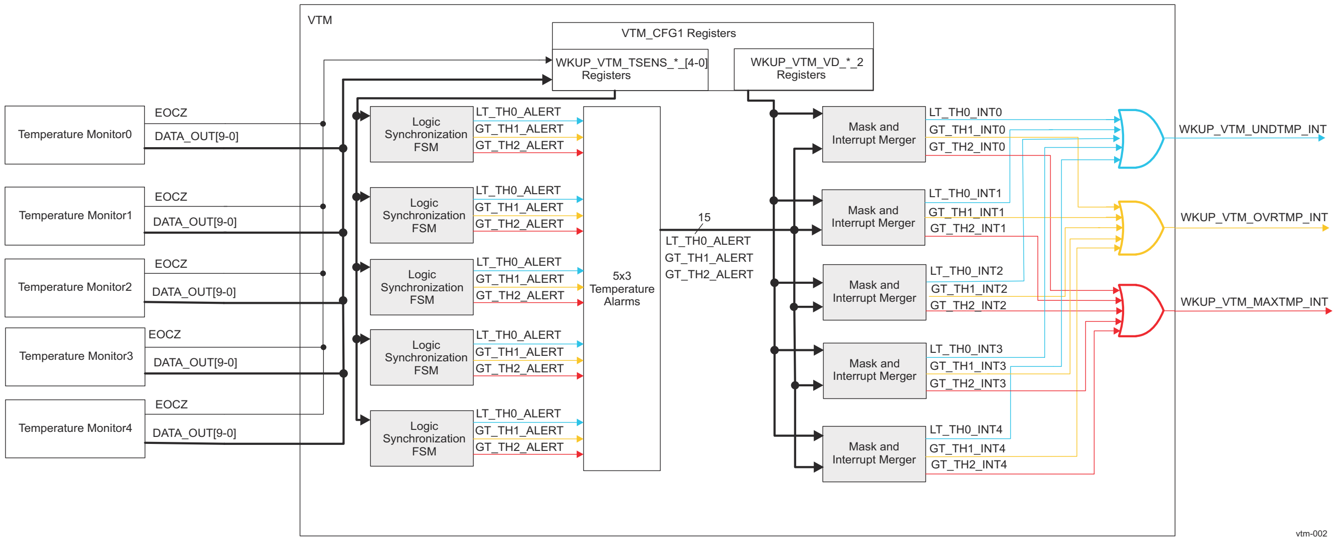

Figure 6-12. VTM Alert and Interrupt Generation

Note

The interrupts are only active when the sensor is in continuous mode. A one-shot sampling of the sensor will not trigger any interrupts.

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presents the connection of VTM TEMPSENSOR registers groups to voltage domains.

6.2.5.5.2.3 VTM VID Voltage Domains

Table 6-19 presents the connection of VTM VD registers groups to voltage domains.

Table 6-19. VTM VD Register Groups Mapping to Voltage Domains

Register Group	Voltage Domain
WKUP_VTM_*_VD_*[1-0]	Not-used.
WKUP_VTM_*_VD_*_2	Maps to VD_CC
WKUP_VTM_*_VD_*_[7-3]	Not-used.

Table 6-20 shows the relation between the VID bit-field values and voltage.

Table 6-20. VID Bit-field Values and Their Corresponding Voltage

VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V
0x0-0x1D	Invalid Values	0x3B	0.745	0x59	0.895	0x77	1.045
0x1E	0.6	0x3C	0.75	0x5A	0.9	0x78	1.05
0x1F	0.605	0x3D	0.755	0x5B	0.905	0x79	1.055
0x20	0.61	0x3E	0.76	0x5C	0.91	0x7A	1.06
0x21	0.615	0x3F	0.765	0x5D	0.915	0x7B	1.065
0x22	0.62	0x40	0.77	0x5E	0.92	0x7C	1.07
0x23	0.625	0x41	0.775	0x5F	0.925	0x7D	1.075
0x24	0.63	0x42	0.78	0x60	0.93	0x7E	1.08
0x25	0.635	0x43	0.785	0x61	0.935	0x7F	1.085
0x26	0.64	0x44	0.79	0x62	0.94	0x80	1.09
0x27	0.645	0x45	0.795	0x63	0.945	0x81	1.095

Table 6-20. VID Bit-field Values and Their Corresponding Voltage (continued)

VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V
0x28	0.65	0x46	0.8	0x64	0.95	0x82	1.1
0x29	0.655	0x47	0.805	0x65	0.955	0x83	1.11
0x2A	0.66	0x48	0.81	0x66	0.96	0x84	1.12
0x2B	0.665	0x49	0.815	0x67	0.965	0x85	1.13
0x2C	0.67	0x4A	0.82	0x68	0.97	0x86	1.14
0x2D	0.675	0x4B	0.825	0x69	0.975	0x87	1.15
0x2E	0.68	0x4C	0.83	0x6A	0.98	0x88	1.16
0x2F	0.685	0x4D	0.835	0x6B	0.985	0x89	1.17
0x30	0.69	0x4E	0.84	0x6C	0.99	0x8A	1.18
0x31	0.695	0x4F	0.845	0x6D	0.995	0x8B	1.19
0x32	0.7	0x50	0.85	0x6E	1	0x8C	1.2
0x33	0.705	0x51	0.855	0x6F	1.005	0x8D	1.21
0x34	0.71	0x52	0.86	0x70	1.01	0x8E	1.22
0x35	0.715	0x53	0.865	0x71	1.015	0x8F	1.23
0x36	0.72	0x54	0.87	0x72	1.02	0x90	1.24
0x37	0.725	0x55	0.875	0x73	1.025	0x91	1.25
0x38	0.73	0x56	0.88	0x74	1.03	0x92-0xFF	Invalid Values
0x39	0.735	0x57	0.885	0x75	1.035		
0x3A	0.74	0x58	0.89	0x76	1.04		

6.2.5.5.2.4 VTM Clocking

The VTM has 2 reference clock inputs, WKUP_VTM0_FIX_REF_CLK and WKUP_VTM0_FIX_REF2_CLK. The WKUP_VTM0_FIX_REF_CLK is the high precision clock that is used for the sensors. The WKUP_VTM0_FIX_REF2_CLK is a lower precision clock that can be used during low power scenarios to keep the sensors running when the WKUP_VTM0_FIX_REF_CLK is shut off. WKUP_VTM_CLK_CTRL[31] TSENS_CLK_SEL and WKUP_VTM_CLK_CTRL[4-0] TSENS_CLK_DIV are used to switch between the clocks and to choose the divider value. All the sensors in all VDs controlled by this VTM will run off of the same reference clock.

Note

Software must disable all sensors before switching the reference clock.

For more information about propagation sequence of the sensor changes, see Section 6.2.5.5.2.7.3 , *Sensors Programming Sequences*.

6.2.5.5.2.5 VTM Retention Interface

VTM has a general purpose retention interface, consistent of 16 sets of 3 signals that can operate totally independently in order to provide retention for 16 signals in the SoC:

- LPMODE_SLEEP_RETIN[15:0]
- LPMODE_SLEEP_RETEN[15:0]
- LPMODE_SLEEP_RETOUT[15:0]

The input LPMODE_SLEEP_RETIN[n] is sampled and synchronized continuously while LPMODE_SLEEP_RETEN[n] = 0. The synchronized output is send out via LPMODE_SLEEP_RETOUT[n]. Once LPMODE_SLEEP_RETEN[n] = 1, then the synchronizer will latch the value and continue providing that latched value via LPMODE_SLEEP_RETOUT[n].

6.2.5.5.2.6 VTM ECC Aggregator

Note

For more information about ECC Aggregator functionality, see *ECC Aggregator*.

6.2.5.5.2.7 VTM Programming Model

6.2.5.5.2.7.1 VTM Maximum Temperature Outrange Alert

THERM_MAXTEMP_OUTRANGE_ALERT is used at the device level in order to generate device warm reset. The alert is asserted when the device overheats and exceeds the maximum temperature limit specified for the device, namely 125°C.

The following is the sequence to assert the THERM_MAXTEMP_OUTRANGE_ALERT:

1. For the output to go active (‘1’), the VTM has to be configured to operate with at least one of its temperature sensors enabled, and VTM_CFG1_TMPSENS_CTRL_j[11] MAXT_OUTRG_EN = 1 for the corresponding enabled sensor.
2. In addition, VTM_CFG2_MISC_CTRL[0] ANYMAXT_OUTRG_ALERT_EN has to be set to ‘1’.
3. With the previous configuration set and at least one of the temperature sensors properly configured, and enabled, if the temperature of the die ever exceeds the programmed value in VTM_CFG2_MISC_CTRL2, the VTM output will be driven ‘1’ once the sensor detects the programmed maximum temperature.
4. At the device level the VTM output, THERM_MAXTEMP_OUTRANGE_ALERT, will drive the PLL controllers into warm reset state with the PLL controllers entering condition, at the same time that all the PLLs go into clock bypass mode.
5. By the actions described in No.4, the device will considerably reduce its power consumption, which over the passing of a few seconds will cause the device to reduce its temperature.
6. The VTM sensor continues to read the temperature and once the code corresponding to the programmed value in VTM_CFG2_MISC_CTRL2[25-16] MAXT_OUTRG_ALERT_THR0 is detected the VTM drives THERM_MAXTEMP_OUTRANGE_ALERT = 0.
7. After No.6 is fulfilled, the PLL controllers no longer have the THERM_MAXTEMP_OUTRANGE_ALERT driving the request and thus the PLL controllers bring the SoC out of reset and the boot sequence re-starts. At the same time the PLLs get out of bypass mode and start with their target programmed frequencies for the boot process.

Note

THERM_MAXTEMP_OUTRANGE_ALERT output of VTM is mapped to VTM_CFG2_MISC_CTRL[0] ANY_MAXT_OUTRG_ALERT_EN.

Notice that exceeding of the programmed value in VTM_CFG2_MISC_CTRL2[9-0] MAXT_OUTRG_ALERT_THR boundary doesn’t result in a PORz (cold reset) event, but instead a event. Otherwise if cold reset is applied to the MCU/WKUP domains of the device, the VTM will be fully reset and the output THERM_MAXTEMP_OUTRANGE_ALERT will be cleared to ‘0’ immediately.

6.2.5.5.2.7.2 Temperature Monitor during Low Power Modes

For more information about device Low Power Modes (LPM), see *Device Power States*.

The following sequence has to be follow in LPM:

1. During MCU_ONLY LPM VD_CORE is OFF and VD_MCU and VD_WKUP are ON, so:
   - WKUP_VTM_TMPSENS_CTRL_1[1] TMPSOFF needs to be programmed for the sensor to be disabled and WKUP_VTM_TMPSENS_CTRL_1, and VTM_TMPSENS_TRIM_1 registers settings for this sensor to go to its reset state.

2. If the exit from low power modes in the device results in the VD_CORE also being ON, then at that point the remaining TMPSENS modules can be enabled (WKUP_VTM_TMPSENS_CTRL_1, WKUP_VTM_TMPSENS_TRIM_1 registers).

6.2.5.5.2.7.3 Sensors Programming Sequences

Sensors Control Modifications Sequence:

1. Write changes to registers.
2. Wait for 900ns to 1us (long enough for sensor period of slowest 1.15 MHz sensor clock plus some extra).
3. New changes can be written to registers.

Reset Sensors Sequence:

1. Set the WKUP_VTM_TMPSENS_CTRL_j[6] CLRZ bit to enable the sensor (so that it has the ENA input high).
2. Wait for 900ns to 1us for the sensor clock to toggle and register the updated ENA pin.
3. Clear WKUP_VTM_TMPSENS_CTRL_j[6] CLRZ to disable and reset the sensor (as it requires an ENA transition from 1 to 0 to reset initially) .
4. Wait for 900ns to 1us for the sensor clock to toggle and register the updated ENA pin.
5. Now the sensor can be configured and enabled normally.

6.2.5.5.2.8 AVS-Class0

Adaptive Voltage Scaling (AVS) Class 0 is a procedure for lowering the voltage on certain device power rails. AVS Class 0 attempts to normalize the power consumption across all devices. The optimal voltage for each AVS supported rail of each device is determined after analysis in the factory, based on the strength of the device during manufacturing. This value is written in the device eFuse where it can be read through dedicated registers.

AVS can be enabled by system software after primary boot. Refer to *AVS Support* on how to enable AVS based on these registers.

6.3 Reset

This chapter describes the device reset signals and contains details on reset management.

6.3.1 Overview

Reset Introduction

A reset is designed to bring a device or subsystem into a known state. Resets occur after power up events, as well as through software and hardware reset requests. This section introduces the device reset capabilities and functionality.

Device Resets

The Device Power-on-Reset (POR) is controlled by the external pin MCU_PORz. This pin is driven by an external (off-chip) "Power-Good" Circuit or Power Management IC (PMIC). The MCU_PORz pin should be held active LOW (0) during the entire power-up phase. The device should be held in reset until all power supplies are stable with an additional delay for the High Frequency Oscillator (HFOSC0) clock to stabilize.

The SoC is divided into two separate functional Reset Domains: MCU Reset Domain and MAIN Reset Domain (each containing specific processing cores and peripherals).

- MCU Reset Domain: Managed by the MCU Domain, PLLCTRL and PSC, this includes ARM® Cortex®- R5F MCU Processor (R5FSS).
- MAIN Reset Domain: Managed by the MAIN Domain, PLLCTRL and PSC, this includes the high performance application Arm Cortex-A53 cores (A53SS), Device Management and Low Power Management (DM R5F), Security Controller (SMS0) .

Both MCU and Main domains have independent Warm Reset MCU_RESETz & MAIN_RESETz_REQ pins. All MCU domain resets act as controller resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets). The following section outlines the various resets coming from pins and software MMR bits and their behavior.

AM62Dx also supports Low Power & Deepsleep modes where parts of the device are switched-off through Power-Domain switches. To support these low power modes the device is partitioned so that only a small region is kept active (Wake-up) and the rest can be powered off through power-down switches.

Figure 6-13 illustrates the high-level reset domain partition.

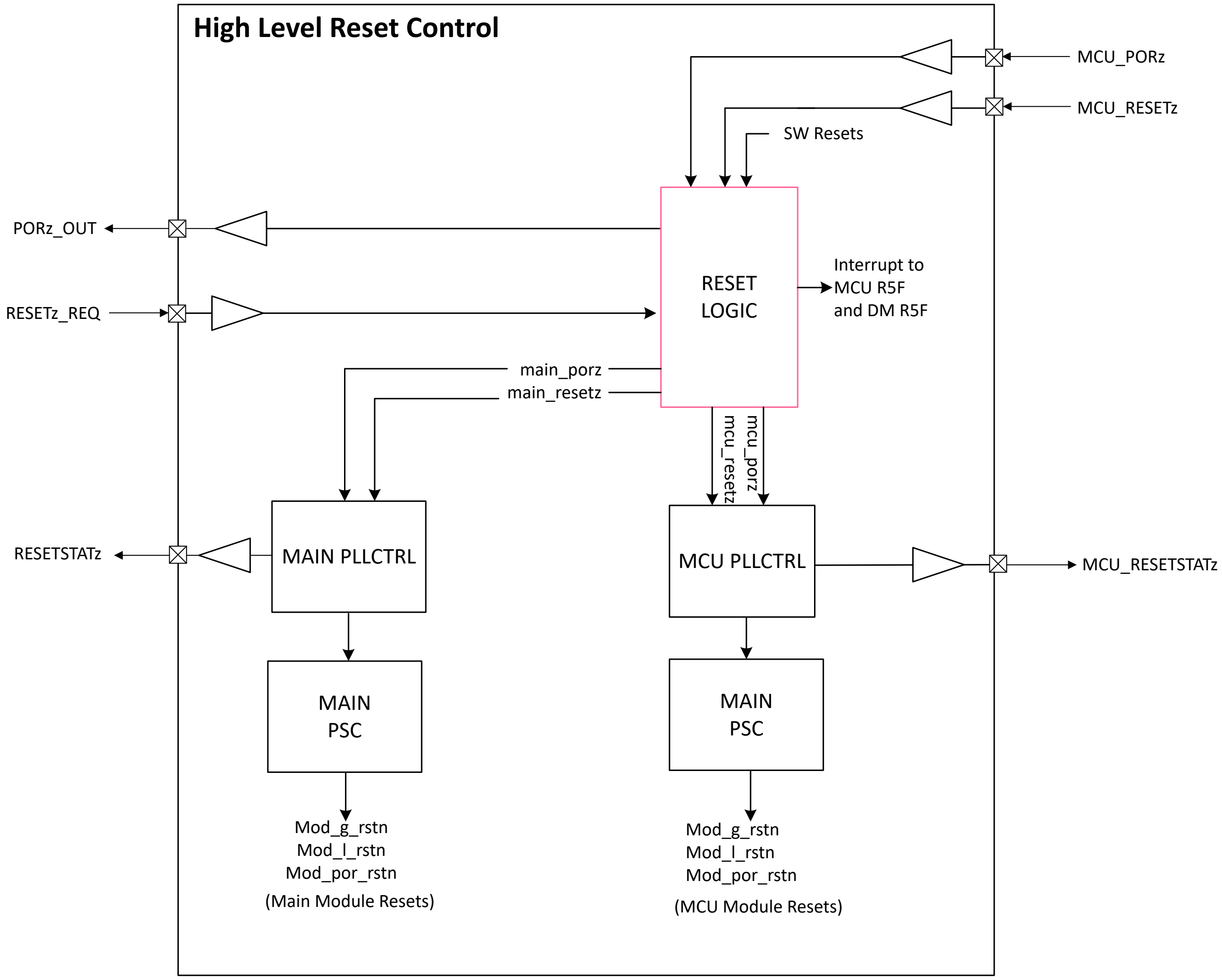

Figure 6-13. High Level Reset Control

6.3.1.1 MCU Domain Supported Resets

- Power-On-Resets
  - MCU_PORx device pin: This power-on-reset will reset the entire device including MCU and MAIN domains.
- Warm Resets
  - MCU_RESETz device pin
  - MCU domain software warm reset
  - MCU domain ESM error reset
  - SMS cold reset

  The warm resets listed above will reset the entire device including MCU and MAIN domains.
- Local Module Resets
  - MCU domain LPSC module local reset: This reset is generated by the MCU PSC to locally reset the R5F CPU core

6.3.1.2 MAIN Domain Supported Resets

- Power-On-Resets
  - MAIN domain software POR reset
  - MAIN domain hardware POR reset generated by MCU_PORz
- Warm Resets
  - RESETz_REQ device pin
  - MAIN domain ESM error reset
  - MAIN domain software warm reset
  - SMS cold reset
  - MCU domain warm reset will also generate a MAIN domain warm reset
- Local Module Resets
  - MAIN domain LPSC module local reset: This reset is generated by the MAIN PSC to locally reset the Processor cores (A53, SMS R5F, DM R5F, PRUSS)

The device can be configured via software such that a Main domain resets can be isolated from MCU domain. When the MCU domain is configured for reset isolation, MAIN domain resets will only reset the MAIN domain and the MCU domain will remain unaffected by all MAIN domain resets. All MCU domain resets will cause a reset to the entire device (including MAIN and MCU domains).

6.3.1.3 High-Level Reset Flow

High Level Reset Flow explains the high-level device power-up and reset use cases.

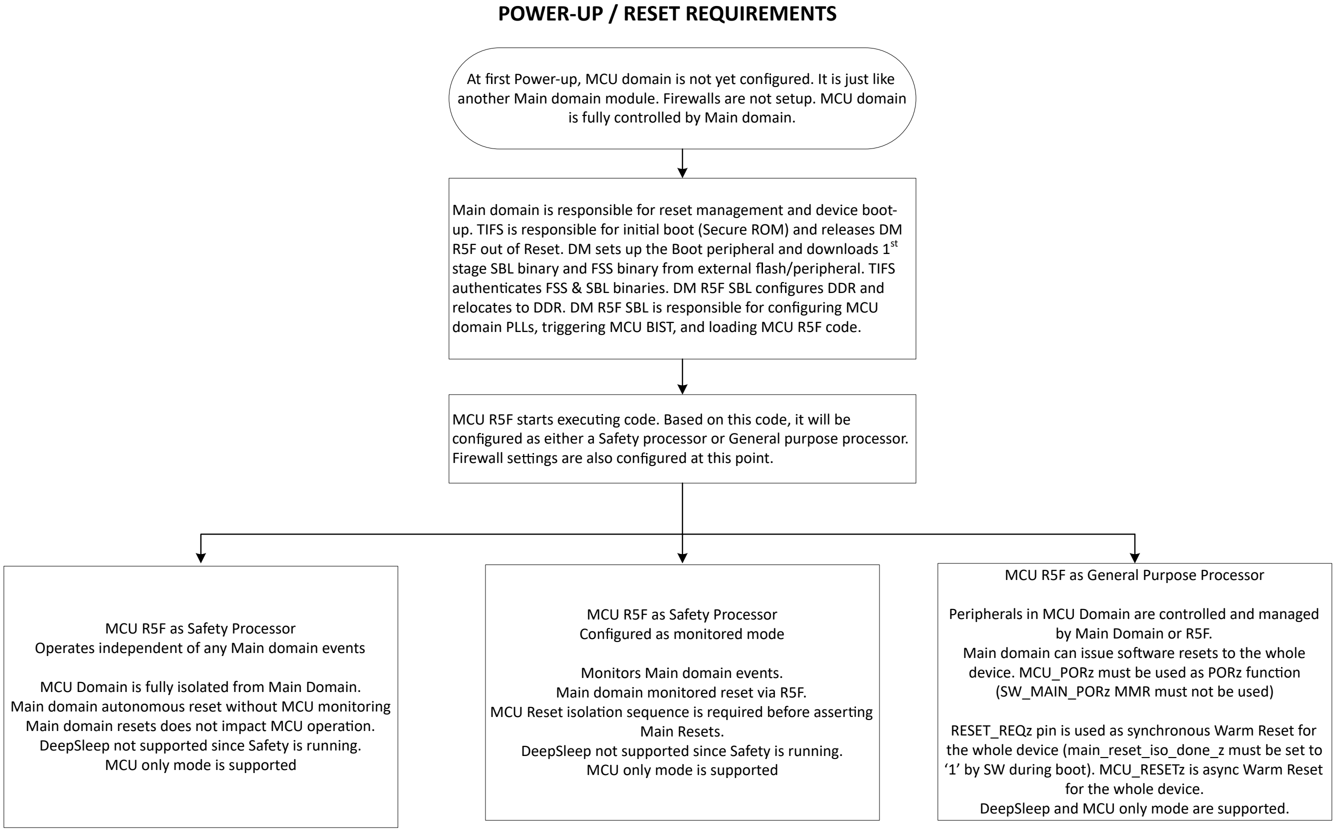

At first Power-up, MCU domain is not yet configured. It is just like another Main domain module. Firewalls are not setup. MCU domain is fully controlled by Main domain.

Main domain is responsible for reset management and device boot-up. TIFS is responsible for initial boot (Secure ROM) and releases DM R5F out of Reset. DM sets up the Boot peripheral and downloads 1^{st} stage SBL binary and FSS binary from external flash/peripheral. TIFS authenticates FSS & SBL binaries. DM R5F SBL configures DDR and relocates to DDR. DM R5F SBL is responsible for configuring MCU domain PLLs, triggering MCU BIST, and loading MCU R5F code.

MCU R5F starts executing code. Based on this code, it will be configured as either a Safety processor or General purpose processor. Firewall settings are also configured at this point.

MCU R5F as Safety Processor
Operates independent of any Main domain events

MCU Domain is fully isolated from Main Domain.
Main domain autonomous reset without MCU monitoring
Main domain resets does not impact MCU operation.
DeepSleep not supported since Safety is running.
MCU only mode is supported

MCU R5F as Safety Processor
Configured as monitored mode

Monitors Main domain events.
Main domain monitored reset via R5F.
MCU Reset isolation sequence is required before asserting Main Resets.
DeepSleep not supported since Safety is running.
MCU only mode is supported

MCU R5F as General Purpose Processor

Peripherals in MCU Domain are controlled and managed by Main Domain or R5F.
Main domain can issue software resets to the whole device. MCU_PORz must be used as PORz function (SW_MAIN_PORz MMR must not be used)

RESET_REQz pin is used as synchronous Warm Reset for the whole device (main_reset_iso_done_z must be set to ‘1’ by SW during boot). MCU_RESETz is async Warm Reset for the whole device.
DeepSleep and MCU only mode are supported.

Figure 6-14. High Level Reset Flow

6.3.1.4 Reset Terminology

DM	Device Management (including Low Power Management)
POR	Power-On-Reset
ESM	Error Signaling Module
Reset Isolation	The module or domain is exempt from specific resets
PSC	Power Sleep Controller
LPSC	Local Power Sleep Controller
PD	Power Domain
VD	Voltage Domain
PRG	Power Reset Generator
POK	Power OK
PGD	Power Glitch Detector
PLLCTRL	PLL and Reset Controller
HHV	High Heating Value mode (IO Pin Fail-safe Control (Tri-State Output))
VTM	Voltage and Temperature Monitor
HFOSC	Internal Device High-Frequency Oscillator
SMS	Security Management Subsystem
TIFS	Texas Instruments Foundational Security
HSM	Hardware Security Module

6.3.1.5 Reset Architecture

6.3.1.5.1 Reset Architecture Block Diagram

Reset Architecture Block Diagram shows the device reset architecture block diagram. It describes the device reset sub-modules and critical internal signal interconnections.

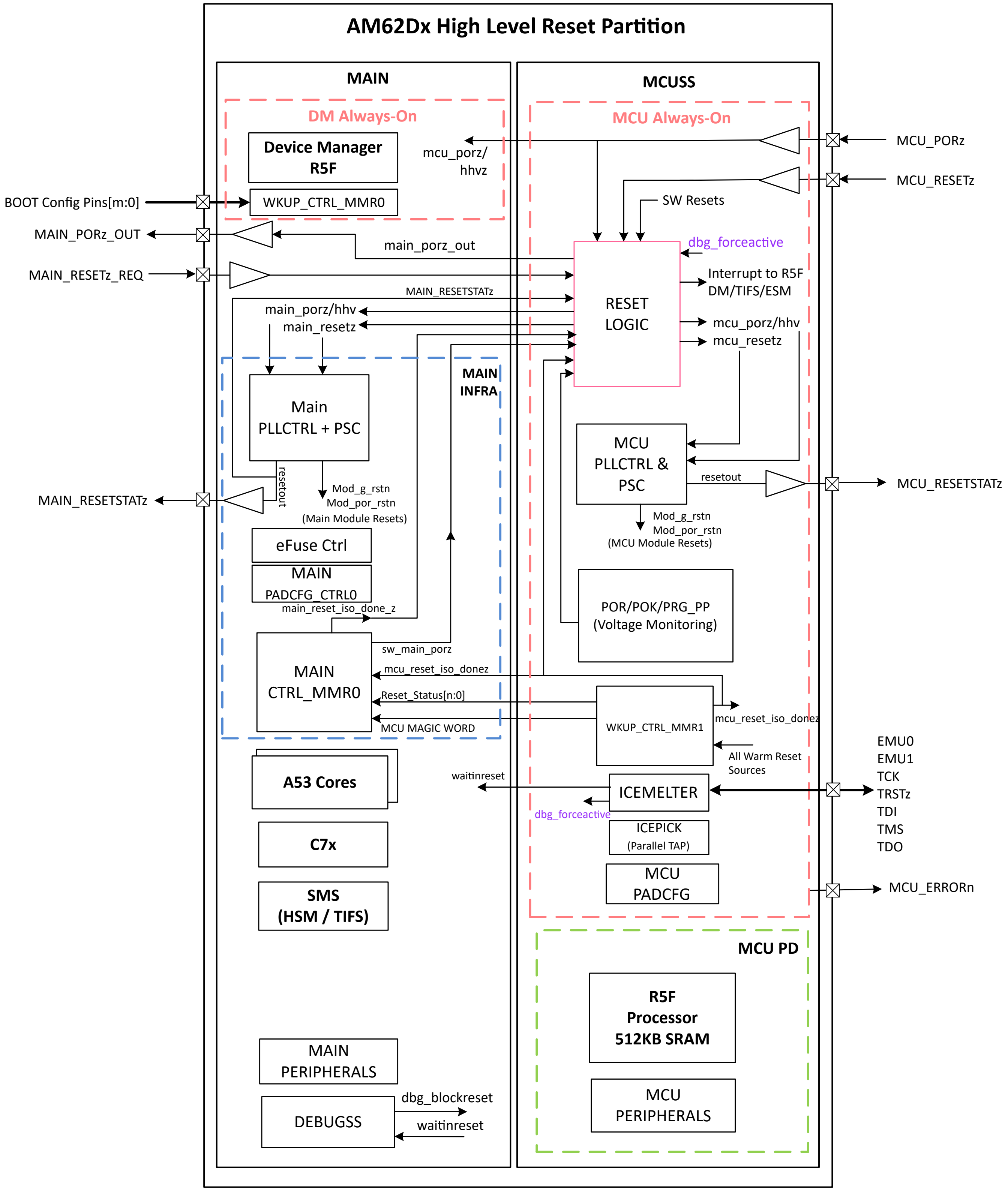

Figure 6-15. Reset Architecture Block Diagram

6.3.1.5.2 SoC Reset Hardware Logic Diagram

SoC Reset Hardware Logic Diagram shows the reset hardware logic diagram. It describes the MAIN and MCU reset domains and processors connections as well as the available reset sources including reset pins and CTRLMMRs.

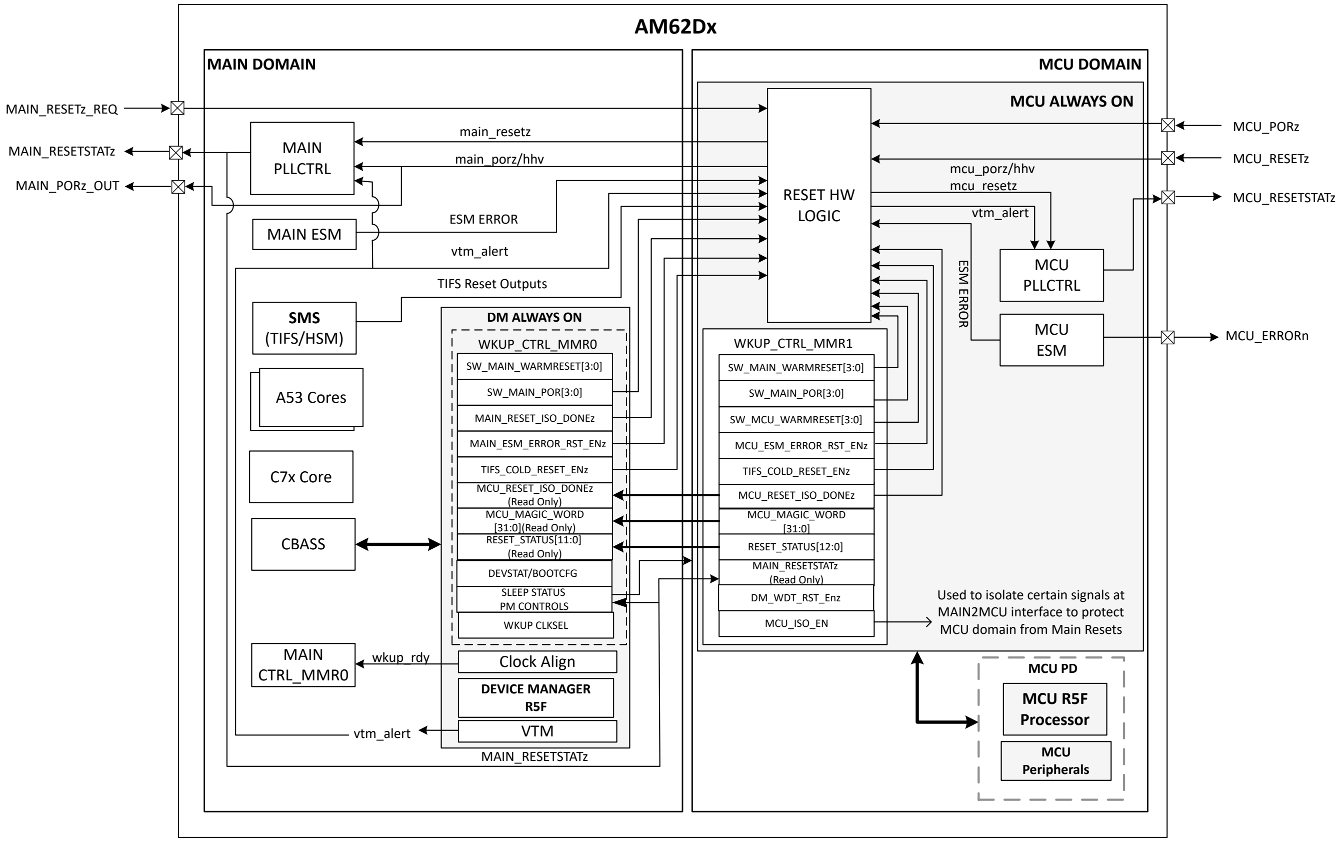

Figure 6-16. SoC Reset Hardware Logic Diagram

6.3.1.5.3 MCU Domain Reset Hardware Logic Diagram

MCU Domain Reset Hardware Logic Diagram shows the external and internal signals associated with the MCU domain resets.

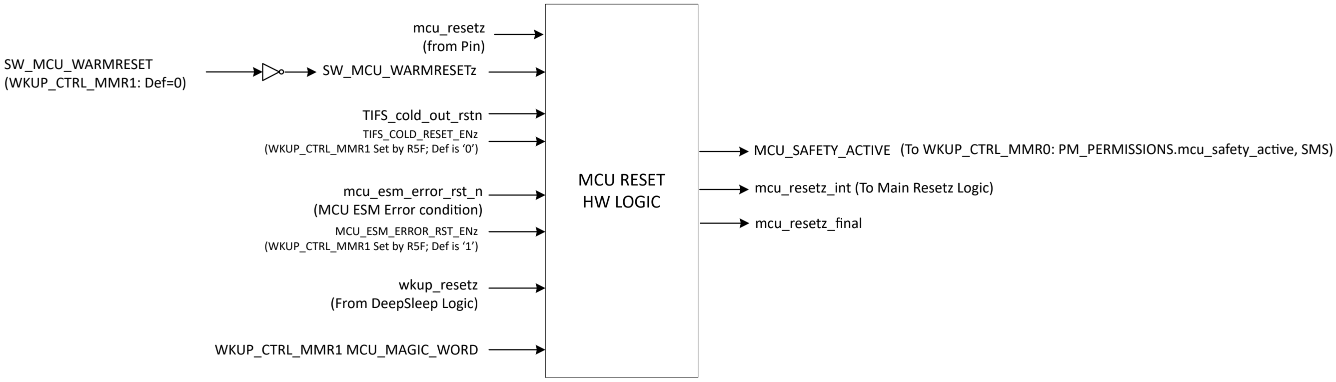

Figure 6-17. MCU Domain Reset Hardware Logic Diagram

6.3.1.5.4 MAIN Domain Reset and PORz Hardware Logic Diagrams

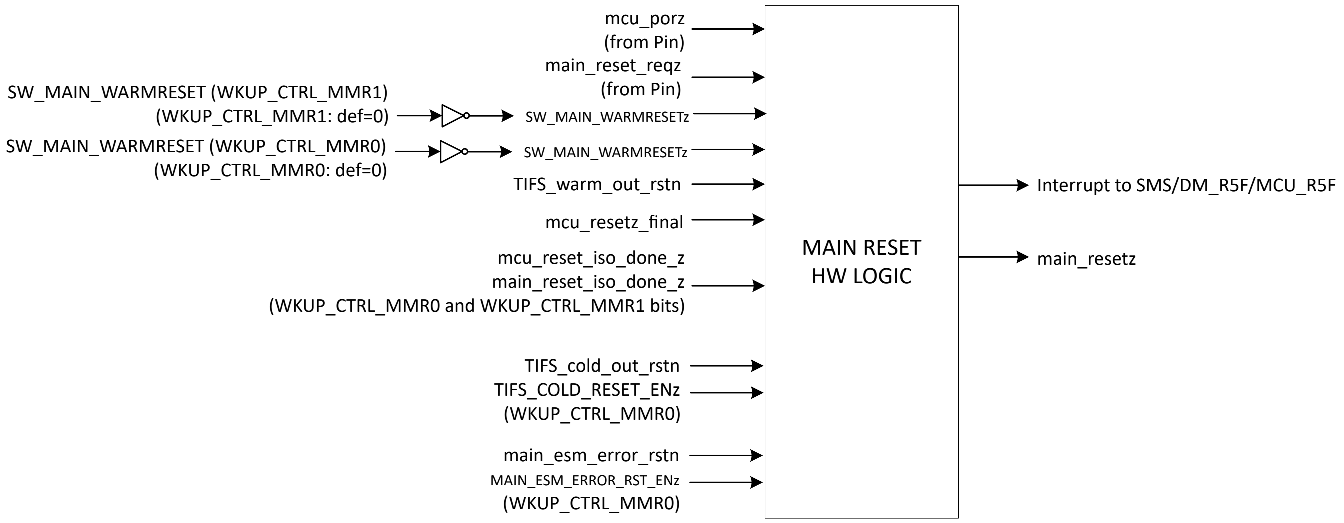

Figure 6-18. MAIN Domain Resetz Hardware Logic Diagram

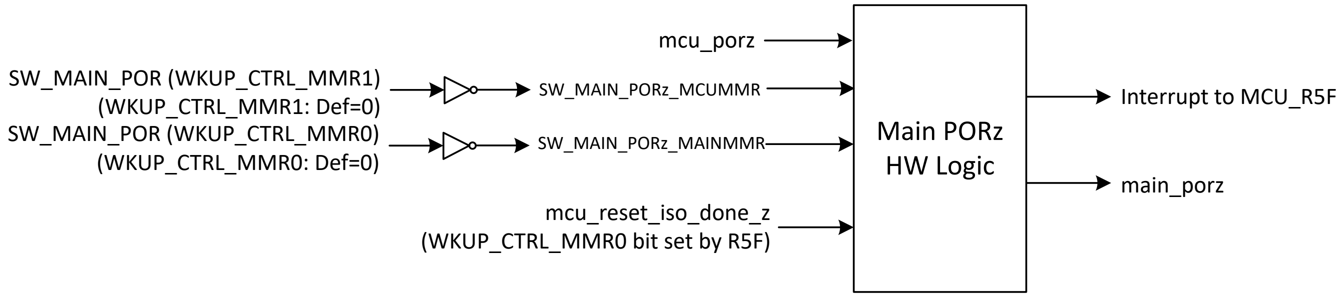

Figure 6-19. MAIN Domain PORz Hardware Logic Diagram

6.3.2 Reset Sources

Device Reset Sources summarizes the available reset sources that are supported by the device.

Table 6-21. Device Reset Sources

Reset Name	Device Domain	Reset Type	Sync/ Async	Pin/ Register/ Internal	Details
MCU_PORz	MCU MAIN	Hardware POR	Async	MCU_PORz HW Pin	MCU_PORz Details
SW_MAIN_PORz	MAIN	Software POR	Sync	MMR	SW_MAIN_PORz Details
MCU_RESETz	MCU MAIN	Hardware warm reset	Async	MCU_RESETz HW Pin	MCU_RESETz Details
SW_MCU_WARMRSTz	MCU MAIN	Software warm reset	Sync	MMR	SW_MCU_WARMRSTz Details
MAIN_RESETz_REQ	MAIN	Hardware warm reset	Sync	RESETz_REQ HW Pin	MAIN_RESETz_REQ Details
SW_MAIN_WARMRSTz	MAIN	Software warm reset	Sync	MMR	SW_MAIN_WARMRSTz Details
VTM Thermal Reset	MCU MAIN	Thermal error warm reset	Async	Internal Signal	VTM Thermal Alert Reset Details
ESM_ERRORz	MCU MAIN	ESM error warm reset	Async	Internal Signal	ESM_ERRORz Reset Details
SMS_COLD_OUT_RST_n	MCU MAIN	SMS0 cold reset	Async	Internal Signal	SMS Reset Details
SMS_WARM_OUT_RST_n	MAIN	SMS0 warm reset	Async	Internal Signal	SMS Reset Details
DM_WDT_RST_n	MCU MAIN	DM Watchdog Timeout Reset during Deepsleep	Async	Internal Signal	MCU_RESETz Details

6.3.3 Reset Status

Reset Status shows the Reset Status functionality. An output pin or software bit is used to represent the status of a specific individual reset.

Table 6-22. Reset Status

Reset Status Name	Reset Status Source	Reset Status Info	Signal Active Level	Reset Signal Details
MCU_CTRL_MMR_CFG0_RST_STAT Status Register	Register	4 bits in CTRLMMR on MCU warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	
WKUP_CTRL_MMR_CFG0_RST_STAT Status Register	Register	4 bits in CTRLMMR on WKUP warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	
PORz_OUTz	Output Pin	On/Off pin status of MAIN PORz reset	Active LOW (0)	MAIN_PORz_OUT Status Pin
RESETSTATz	Output Pin	On/Off pin status of MAIN warm reset	Active LOW (0)	MAIN_RESETSTATz Status Pin
MCU_RESETSTATz	Output Pin	On/Off pin status of MCU PORz reset	Active LOW (0)	MCU_RESETSTATz Status Pin
MCU_ERRORn	Output Pin	On/Off pin status of MCU ESM_ERROR reset	Active LOW (0)	MCU_SAFETY_ERRORn Status Pin

6.3.3.1 Reset Source Status Registers

All warm reset sources which trigger a device/domain warm reset are captured in the MCU domain CTRLMMR reset status register **MCU_CTRL_MMR_CFG0_RST_SRC**. This register is only reset on MCU_PORz.

The MCU domain CTRLMMR **MCU_CTRL_MMR_CFG0_RST_SRC** register is shadowed in WKUP domain CTRLMMR **WKUP_CTRL_MMR_CFG0_RST_SRC** so that MAIN domain processors can read it without directly accessing the MCU domain CTRLMMR.

After recovery from warm reset, software can read the CTRLMMR reset source register **WKUP_CTRL_MMR_CFG0_RST_SRC** to identify the source of previous reset. After reading this reset source register, software must clear the register by writing to the MCU domain CTRLMMR, **MCU_CTRL_MMR_CFG0_RST_SRC**.

Reset status bits read active HIGH (1) when a particular reset is triggered.

The following reset sources, which cause MCU and MAIN domain resets, are captured in the MCU domain CTRLMMR reset source register:

- MCU_RESETz (Reset by Hardware Pin)
- SW_MCU_WARMRSTz (Reset by MCU domain CTRLMMR[1])
- SW_MAIN_PORz_MCUMMR (Reset by MCU domain CTRLMMR[1])
- SW_MAIN_PORz_MAINMMR (Reset by MAIN domain CTRLMMR[1])
- MAIN_RESET_REQz (Reset by Hardware Pin)
- SW_MAIN_WARMRSTz_MCUMMR (Reset by MCU domain CTRLMMR[1])
- SW_MAIN_WARMRSTz_MAINMMR (Reset by MAIN domain CTRLMMR[1])
- SMS_COLD_OUT_RST_n (Reset by SMS)
- SMS_WARM_OUT_RST_n (Reset by SMS)
- THERM_MAXTEMP_OUTRANGE_ALERT (Reset by VTM Max Temperature Alert)
- SYSR_ASSERTRESET_n (Reset by DEBUGSS)
- ESM_ERROR_RST_n (Reset by ESM Error)
- DM_WDT RST_n (Reset by WKUP WDT Timeout during Deepsleep mode)
- DM_MAIN_PORz (Reset by DS_MAIN_POR_PDOFF a WKUP domain CTRLMMR[1] during deepsleep)
  - MCU ESM Error will reset entire device
  - MAIN ESM Error will only reset MAIN domain when MCU domain is isolated. When MCU domain is not isolated, it will warm reset both MCU and MAIN domains.

Note

1. MAIN domain software WARMRSTz and PORz control registers are defined in both WKUP domain CTRLMMR and MCU domain CTRLMMR.

When the MCU domain is isolated from MAIN domain, MCU R5FSS processor can reset the MAINdomain, by programming the reset control registers defined in the MCU domain CTRLMMR. This way MCU R5FSS does not need to access MAIN domain CTRLMMR for MAIN domain reset action.

Whena MAIN domain processor (A53, SMS, R5F) needs to issue resets to MAIN domain on error detection they will use the WARMRESETz and PORz MMR bits defined in the WKUP domain CTRLMMR.

6.3.3.2 MCU_RESETSTATz Status Pin

The MCU_RESETSTATz pin indicates the internal reset status of the device (active LOW). When LOW, it indicates that the MCU and MAIN domains are in warm reset state. When HIGH, it indicates that the MCU is out of warm reset state. Refer to Section 6.3.3.4 for MAIN domain reset status.

6.3.3.3 MCU_ERRORn Status Pin

The MCU_ERRORn pin indicates the MCU domain ESM status. This Output is used to signal an external agent that it needs to (or may need to) intervene because of an error. The Error Pin Output is active Low or PWM, based on the ESM Error Pin Control register pwm_en field (Refer ESM IP) . This pwm_en field should only be modified when the ESM is disabled, based on the Global Enable register. Refer ESM chapter for details.

While in Power-On-Reset, the Error Pin is active (asserted low). SoC drives a Low via a weak internal pull-down. After Power-On-Reset condition is removed, ESM will drive the Error Pin. During a Warm Reset the state of the Error Pin is unchanged (i.e. the Error Pin logic is only reset by asserting MCU_PORz low).

When MCU_ERRORn output pin is configured to operate in level mode, a LOW indicates the MCU ESM module has registered an error. A HIGH indicates that there are no MCU ESM errors.

When MCU_ERRORn output pin is configured to operate in PWM mode, no error is indicated by continuous toggle according to programmable MMR widths for high and low periods. When an error occurs, the error pin stops toggling and remains constant until the error is cleared. An external device (such as a PMIC) that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external device.

Note

This signal can be used by external safety devices to determine the device status and assert MCU_PORz if necessary.

6.3.3.4 RESETSTATz Status Pin

This pin indicates warm reset status (active LOW) of the MAIN domain.

When LOW, it indicates that the MAIN domain is in a warm reset state.

When HIGH, it indicates that the MAIN domain is out of reset.

The status of this signal will be captured in WKUP_CTRL_MMR1 registers.

6.3.3.5 PORz_OUT Status Pin

This pin indicates the POR status of the MAIN domain (active LOW).

When LOW, it indicates the MAIN domain is in the POR state.

When HIGH, it indicates the MAIN domain is out of the POR state.

Note

PORz_OUT may be used to enable and/or disable output buffers of attached devices that share pins associated with BOOTMODE inputs, such that appropriate boot configuration values are allowed to propagate into the device without contention.

6.3.4 Reset Controls

The reset control registers enable, disable, and adjust specific reset operations. This section explains how to control certain device resets.

6.3.4.1 Reset Control Registers

MCU Domain Reset Control Registers shows the CTRLMMR registers that are able to enable and disable reset abilities and options.

Table 6-23. MCU Domain Reset Control Registers

Control Name	Control Action	Control Register
MCU_ESM_ERROR_RST_ENz	Enable MCU ESM_ERRORz reset	**MCU_CTRL_MMR_CFG0_RST_CTRL**
SMS_COLD_RESET_ENz	Enable SMS cold reset of MCU domain	**MCU_CTRL_MMR_CFG0_RST_CTRL**

Table 6-24. MAIN Domain Reset Control Registers

Control Name	Control Action	Control Register
MAIN_ESM_ERROR_RST_ENz	Enable MAIN ESM_ERRORz Reset	**WKUP_CTRL_MMR_CFG0_RST_CTRL**
SMS_COLD_RESET_ENz	Enable SMS Cold Reset of MAIN Domain	**WKUP_CTRL_MMR_CFG0_RST_CTRL**

Note

For more information, see *Control Module (CTRLMMR)*.

6.3.4.2 Reset Isolation

Reset Isolation Introduction

It is possible to isolate certain SoC modules and subsystems and prevent them from undergoing an arbitrarily generated warm reset. This is known as Reset Isolation. This section describes the device reset isolation capabilities.

Simple Reset Isolation Sequence Diagram shows a simple description of the device reset isolation sequence.

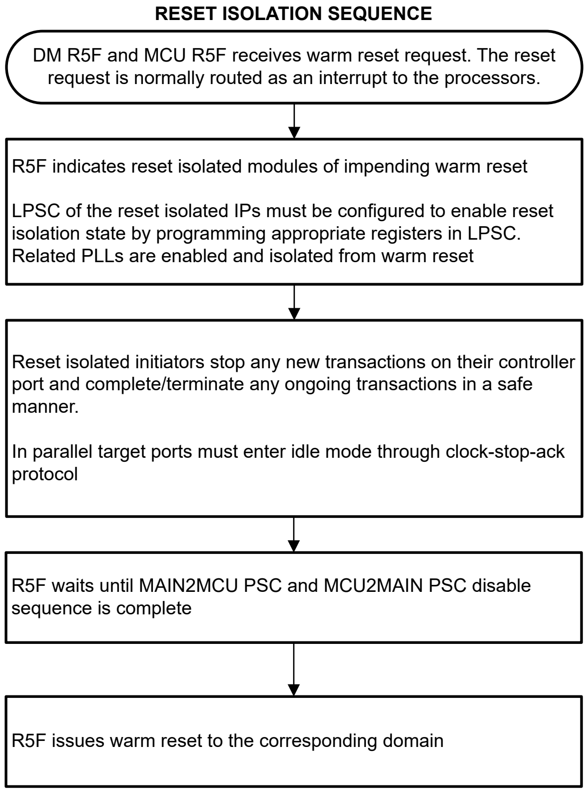

DM R5F and MCU R5F receives warm reset request. The reset request is normally routed as an interrupt to the processors.

R5F indicates reset isolated modules of impending warm reset

LPSC of the reset isolated IPs must be configured to enable reset isolation state by programming appropriate registers in LPSC. Related PLLs are enabled and isolated from warm reset

Reset isolated initiators stop any new transactions on their controller port and complete/terminate any ongoing transactions in a safe manner.

In parallel target ports must enter idle mode through clock-stop-ack protocol

R5F waits until MAIN2MCU PSC and MCU2MAIN PSC disable sequence is complete

R5F issues warm reset to the corresponding domain

Figure 6-20. Simple Reset Isolation Sequence Diagram

MCU Reset Isolation Details

Detailed Reset Isolation Sequence Diagram shows a detailed description of the MCU reset isolation sequences.

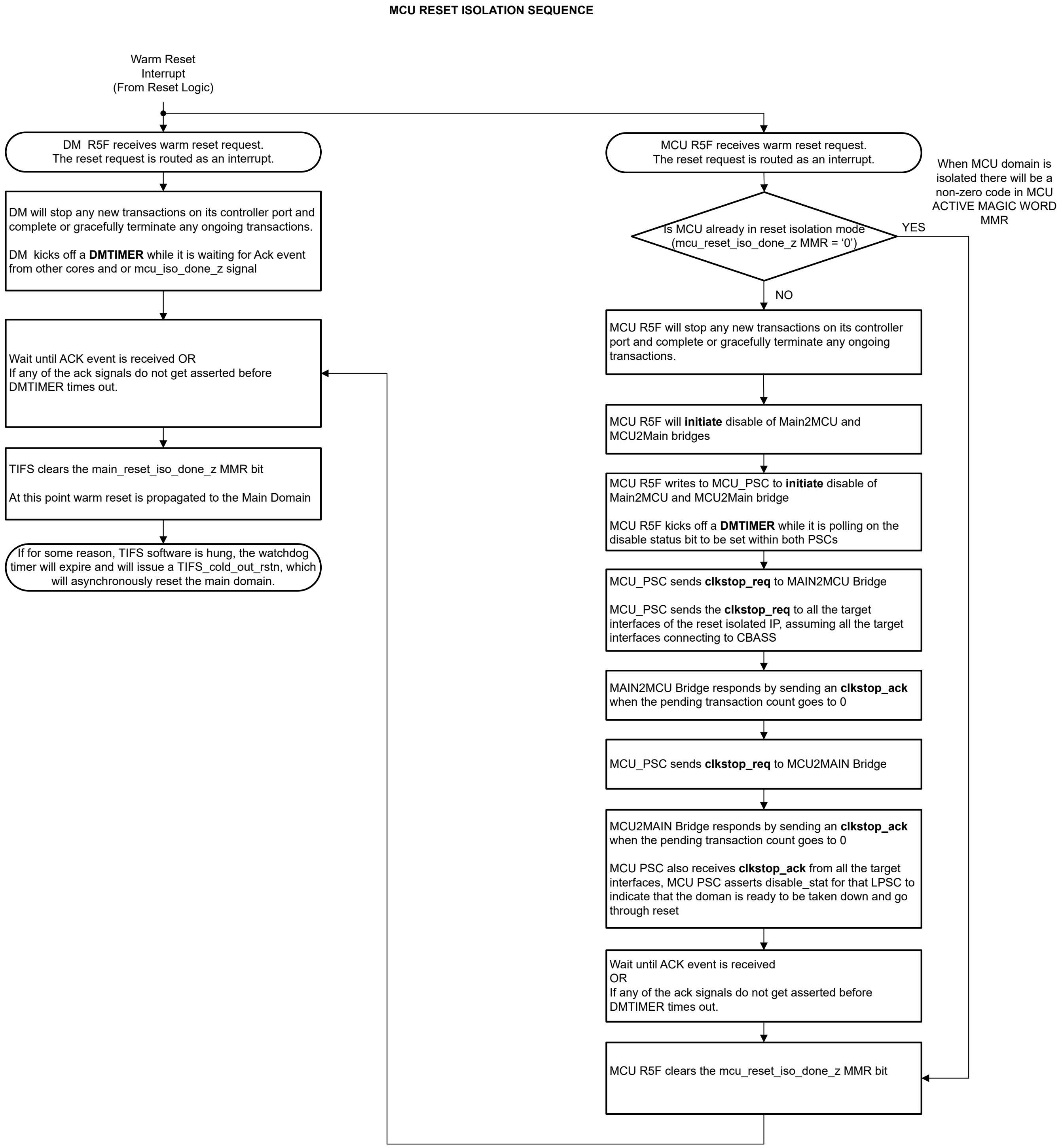

Figure 6-21. Detailed Reset Isolation Sequence Diagram

6.3.5 Reset Details

Reset Details Introduction

The Reset Details section will break down the available device resets and explain operating details such as sequencing and reset logic diagrams. It also includes any additional information related to the device resets.

6.3.5.1 POR Resets

6.3.5.1.1 SW_MAIN_PORz Reset

Reset Overview

This reset is a software controlled MAIN domain POR reset defined in **WKUP_CTRL_MMR_CFG0_RST_CTRL** and **MCU_CTRL_MMR_CFG0_RST_CTRL**.

This software reset will generate a MAIN domain PORz.

R5FSS processor in MCU domain can trigger PORz to the MAIN domain by writing to the **MCU_CTRL_MMR_CFG0_RST_CTRL** register.

MAIN domain processors can reset the MAIN domain by writing to the **WKUP_CTRL_MMR_CFG0_RST_CTRL** register.

When the MCU domain is configured as a safety domain it must be isolated from SW_MAIN_PORz.

A reset isolation sequence for the MCU domain must be complete prior to reset propagation.

WKUP_CTRL_MMR_CFG0_RST_CTRL and **MCU_CTRL_MMR_CFG0_RST_CTRL** define a 4-bit field, SW_MAIN_POR[7:4], for generating a software-controlled POR for the MAIN domain (SW_MAIN_PORz).

When SW_MAIN_POR [7:4] field is set to “0110”, the MAIN domain is in POR reset state (SW_MAIN_PORz = LOW).

When SW_MAIN_POR [7:4] is set to any other value, the MAIN domain is out of POR reset state (SW_MAIN_PORz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

MCU Domain Effect

When MCU domain is configured as an independent domain, then the entire MCU domain is reset isolated. When MCU domain is not configured as independent domain then this SW_MAIN_PORz must not be used. Instead MCU_PORz pin functions should be used.

MCU IOs are not affected.

MAIN Domain Effect

All modules in MAIN domain are reset (including reset isolated modules).

IOs will enter safe state (as defined in the BALL STATE DURING RESET column of the Datasheet Pin Attributes table while this reset is active.

MAIN domain CTRLMMR boot configuration register is reset.

Device BOOTMODE pins will be re-latched after this reset is de-asserted.

Device will re-boot. During boot-up, R5FSS (secondary boot loader) will poll the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and configure MCU domain/R5FSS processor accordingly.

Additional Details

PORz_OUT:

This pin indicates POR status output of the MAIN domain (active LOW).

When LOW, it indicates the MAIN domain is in POR state.

When HIGH, it indicates that the MAIN domain is out of POR state.

Note

PORz_OUT may be used to enable and/or disable output buffers of attached devices that share IOs associated with BOOTMODE inputs, such that appropriate boot configuration values are allowed to propagate into the device without contention

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Note

The boot mode pins are latched internally on the rising edge of PORz_OUT and are reset isolated from all other device resets.

6.3.5.1.2 MCU_PORz Reset

Reset Overview

This is the POR reset signal (active LOW) for the entire device, controlled by the MCU_PORz HW Pin.

When LOW, it performs a POR reset on the entire device (MCU and MAIN domains) and puts IOs in a safe state (as defined in the BALL STATE DURING RESET column of the datasheet Pin Attributes table).

MCU Domain Effect

All modules in MCU domain are reset.

MCU IOs are in HHV state (Reset State).

When MCU_PORz is de-asserted, MCU IOs will enter the default state defined in the device Datasheet. MCU domain will be reconfigured by the device boot processor (secondary boot loader).

MAIN Domain Effect

All modules in the MAIN domain are reset.

MAIN domain IOs are in HHV state (as defined in the BALL STATE DURING RESET column of the datasheet Pin Attributes table).

When MCU_PORz is de-asserted, the MAIN domain IOs will enter default state as defined in the BALL STATE AFTER RESET column of the datasheet Pin Attributes table.

The device boot processor (secondary boot loader) will setup R5FSS as Safety or General-Purpose Processor.

6.3.5.2 Warm Resets

6.3.5.2.1 MAIN Domain Warm Reset Sequence Flow

MAIN Domain Warm Reset Sequence Flowchart explains the process for a typical MAIN domain warm reset.

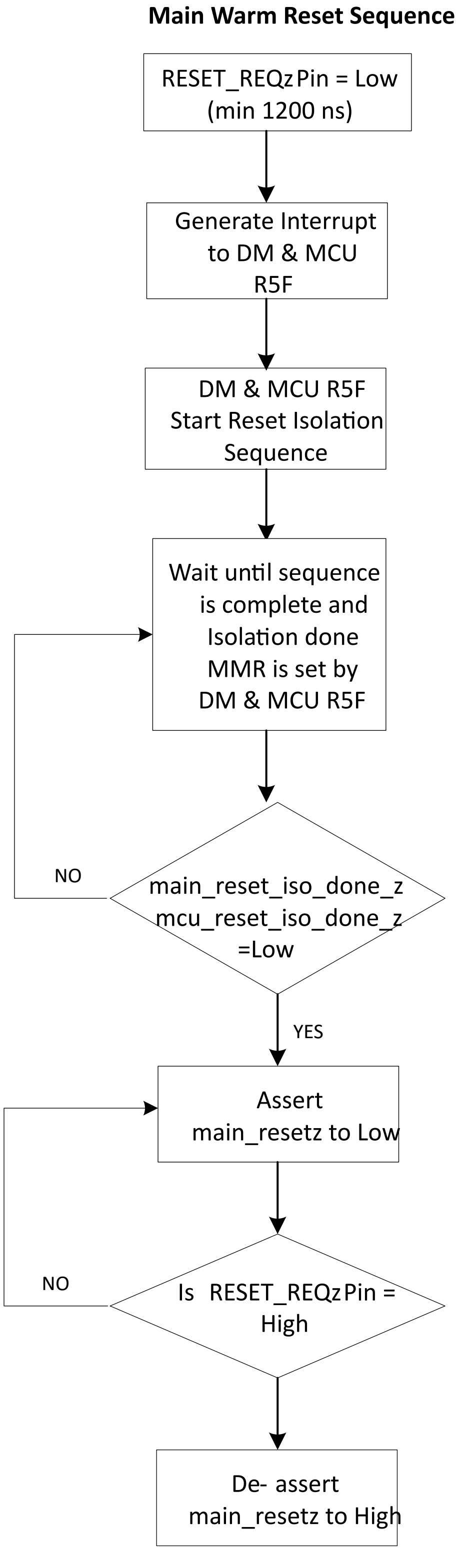

Figure 6-22. MAIN Domain Warm Reset Sequence Flowchart

6.3.5.2.2 MAIN_RESETz_REQ Reset

Reset Overview

This reset signal is the MAIN domain warm reset request (active LOW) controlled by the RESET_REQz HW pin.

When LOW is detected, reset hardware generates an interrupt to processors (A53SS/R5FSS) so they can complete the reset isolation sequence before reset is propagated.

MCU Domain Effect

When MCU domain is configured to operate independently, MCU domain reset isolation sequence is completed before propagating the RESETz to MAIN domain.

MCU IOs are not affected.

When MCU domain is not configured as independent, then this reset will also warm reset MCU domain.

MAIN Domain Effect

This is a MAIN domain warm reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for warm reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

Reason for this reset is captured in the CTRLMMR reset source register **WKUP_CTRL_MMR_CFG0_RST_SRC**. After reset is de-asserted, device will boot-up. During device boot-up, DM R5F secondary boot loader will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU R5F processor accordingly.

Reset Sequence

The RESET_REQz reset sequence is described below.

RESET_REQz Sequence shows the timing between the RESET_REQz reset signal and the internal RESETz (MAIN domain warm reset) signal. Refer to the datasheet for timing and pulse width requirements.

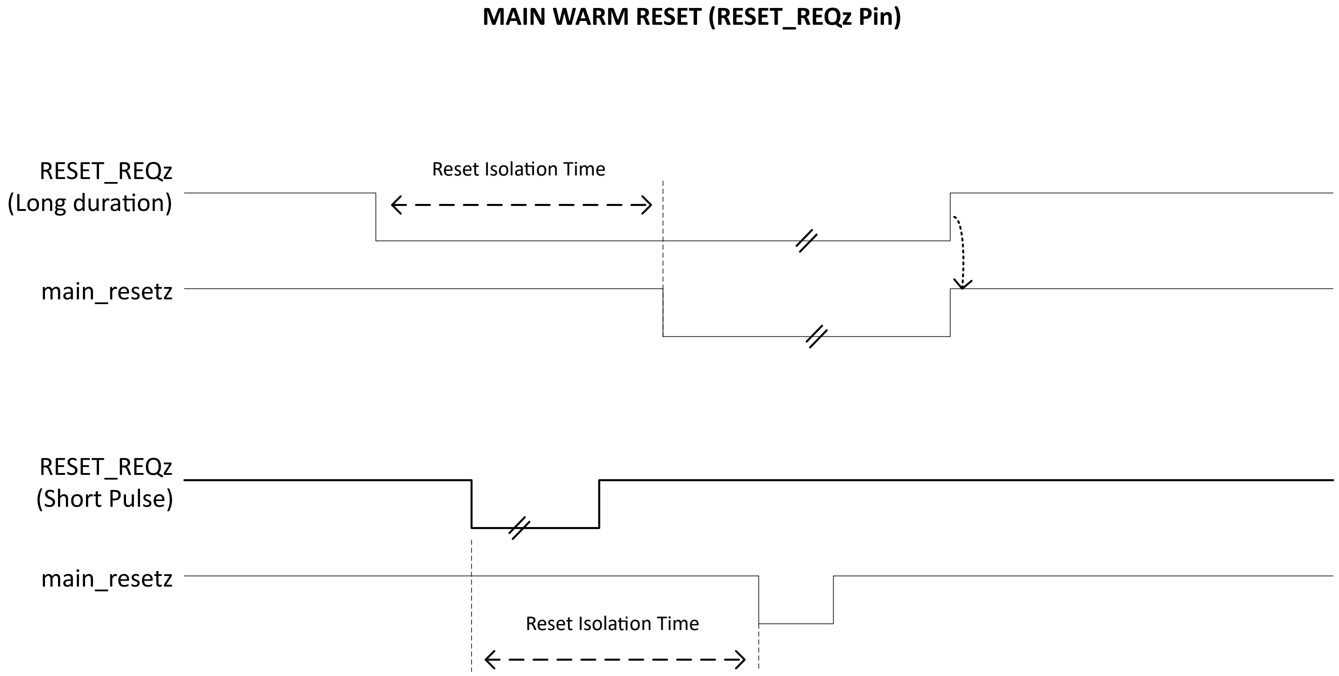

Figure 6-23. RESET_REQz Sequence

Additional Reset Details

RESETSTATz:

The RESETSTATz pin indicates the MAIN domain internal reset status (active LOW). This is a reflection of the reset status after the RESET_REQz reset signal (RESET_REQz HW Pin) is asserted.

When LOW, it indicates that the MAIN domain is in internal reset state.

When HIGH, it indicates that the MAIN domain is out of internal reset state.

RESETSTATz Timing shows the timing between the RESET_REQz reset signal and the RESETSTATz output. Refer to the datasheet for timing and pulse width requirements.

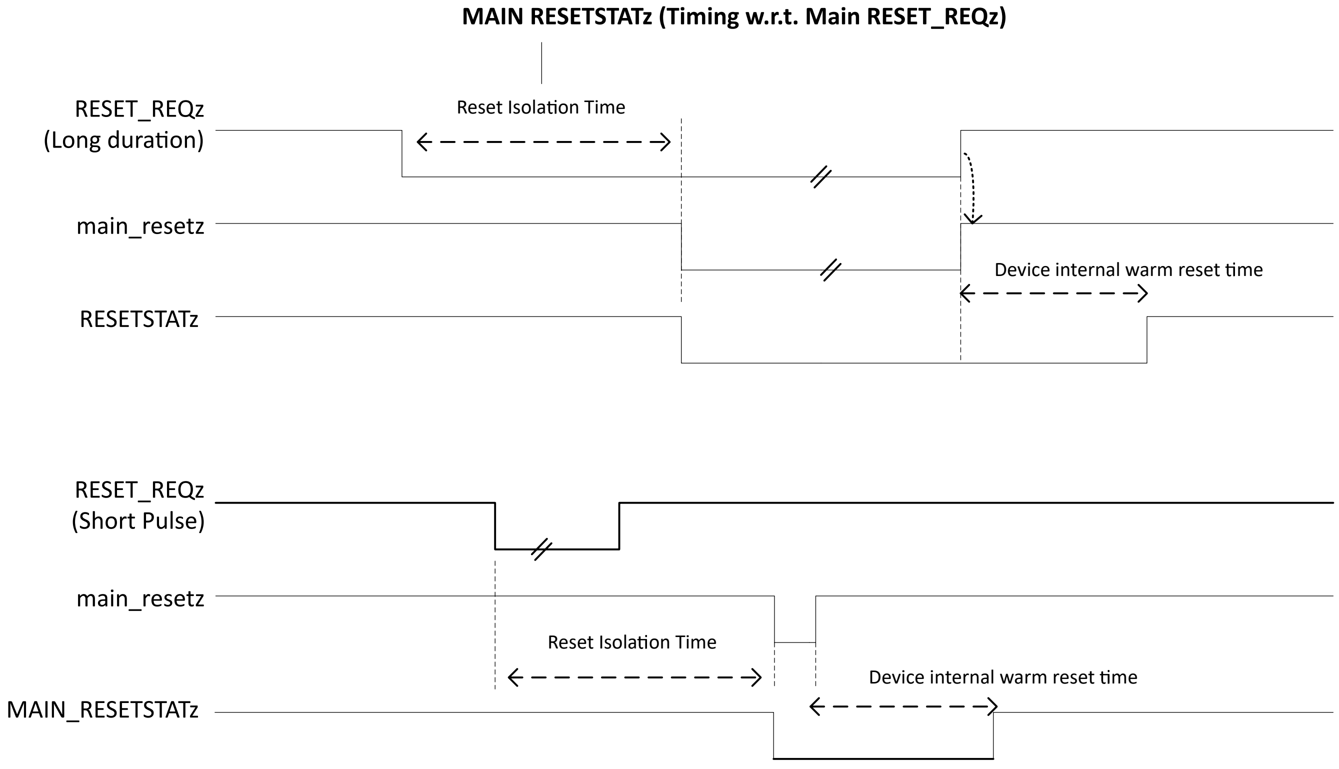

Figure 6-24. RESETSTATz Timing

Note

For more details see MAIN_RESETSTATz Status Pin.

6.3.5.2.3 SW_MAIN_WARMRSTz Reset

Reset Overview

This reset is software controlled MAIN domain warm reset defined in **WKUP_CTRL_MMR_CFG0_RST_CTRL** and **MCU_CTRL_MMR_CFG0_RST_CTRL**.

The R5FSS can issue a warm reset to the MAIN domain, by writing to the MCU domain CTRLMMR register.

The MAIN domain processors can issue a warm reset the WKUP domain, by writing to the MAIN domain CTRLMMR register.

Note

When R5FSS is configured as safety processor it must be reset isolated from this MAIN domain warm reset.

A reset isolation sequence for MCU domain has to be complete prior to this reset propagation.

WKUP domain CTRLMMR and MCU domain CTRLMMR registers define a 4-bit field, SW_MAIN_WARMRST[3:0] for generating a software controlled warm reset for the MAIN domain (SW_MAIN_WARMRSTz).

When SW_MAIN_WARMRST[3:0] field is set to “0110”, a MAIN domain warm reset is active (SW_MAIN_WARMRSTz = LOW).

When SW_MAIN_WARMRST[3:0] is set to any other value, the MAIN domain warm reset is inactive (SW_MAIN_WARMRSTz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

Note

This software reset is equivalent to RESET_REQz reset signal (RESET_REQz HW Pin) functionality.

MCU Domain Effect

When MCU domain is configured to operate independently, MCU domain reset isolation sequence is completed before propagating the RESETz to main domain.

MCU IOs are not affected.

When MCU domain is not configured as independent then, this reset will also warm reset MCU domain.

MAIN Domain Effect

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

Reason for this reset is captured in MAIN domain CTRLMMR reset status register **WKUP_CTRL_MMR_CFG0_RST_STAT**. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.2.4 MCU_RESETz Reset

Reset Overview

The MCU_RESETz signal is the warm reset input (active low) to the entire device, controlled by the MCU_RESETz HW Pin.

When active, it resets all modules in the MCU and MAIN domains.

MCU_RESETz will not reset selected **WKUP_CTRL_MMR_CFG0_RST_CTRL** and **MCU_CTRL_MMR_CFG0_RST_CTRL** register bits. These bits are only reset by PORz.

MCU Domain Effect

All modules in MCU domain are reset except for **MCU_CTRL_MMR_CFG0_RST_CTRL** bits which are reset only on MCU_PORz.

IOs are not affected.

R5FSS is reset.

When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only by PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in the CTRLMMR reset source register **MCU_CTRL_MMR_CFG0_RST_SRC**.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/R5FSS processor accordingly.

Additional Details

MCU_RESETSTATz:

This pin indicates internal MCU_RESETz reset status (active LOW).

When LOW, it indicates that the device, both MCU and MAIN domains, are in internal reset state.

When HIGH, it indicates that the device MAIN domains, are is out of internal reset state.

Note

In order for the MAIN domain to come out of reset, RESETz_REQ (RESET_REQz HW Pin) must also be de-asserted.

Note

For more details see MCU_RESETSTATz Status Pin.

6.3.5.2.5 SW_MCU_WARMRSTz Reset

Reset Overview

This is a software MCU domain warm reset defined in MCU domain CTRLMMR.

MCU CTRLMMR defines a 4-bit field, SW_MCU_WARMRST[11:8] for generating a software warm reset in the MCU domain (SW_MCU_WARMRSTz).

When SW_MCU_WARMRST[11:8] field is set to “0110”, MCU warm reset is active (SW_MCU_WARMRSTz = LOW).

When SW_MCU_WARMRST[11:8] is set to any other value, MCU warm reset is inactive (SW_MCU_WARMRSTz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

Note

This software reset is equivalent to MCU_RESETz warm reset signal (MCU_RESETz HW Pin) functionality.

MCU Domain Effect

All modules in the MCU domain are reset except for MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not affected.

R5FSS processor is reset.

When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in CTRLMMR reset source register**WKUP_CTRL_MMR_CFG0_RST_SRC**.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.3 SMS Resets

6.3.5.3.1 SMS_WARM_OUT_RST_n Reset (MAIN Domain)

Reset Overview

The SMS will issue this reset upon a security error.

When this reset is enabled in MAIN domain, it causes a MAIN domain warm reset.

This is a synchronous reset type (needs to complete reset isolation sequence).

Note

This reset behavior is same as the RESETz_REQ reset signal (RESET_REQz HW Pin).

MCU Domain Effect

When MCU domain is configured to operate independently, MCU domain reset isolation sequence is completed before propagating the RESETz to main domain.

MCU IOs are not affected.

When MCU domain is not configured as independent then, this reset will also warm reset MCU domain.

MAIN Domain Effect

This is a MAIN domain warm reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for CTRLMMR register bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

Reason for this reset is captured in CTRLMMR reset source status register **WKUP_CTRL_MMR_CFG0_RST_SRC**. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.3.2 SMS_COLD_OUT_RST_n Reset (MAIN Domain)

Reset Overview

This reset is a MAIN domain warm reset that is executed from the SMS. This is an asynchronous reset type (takes effect immediately). This SMS reset of the Main domain is enabled only when the SMS_COLD_RESET_EN_z bit in WKUP domain CTRLMMR is '0'.

Note

This reset behavior is same as the RESETz_REQ reset signal (RESET_REQz HW Pin) with the exception that it takes effect immediately without need for any reset isolation sequence.

MCU Domain Effect

When MCU domain is configured to operate independently, MCU domain reset isolation sequence is completed before propagating the RESETz to main domain.

MCU IOs are not affected.

When MCU domain is not configured as independent then, this reset will also warm reset MCU domain.

MAIN Domain Effect

This is a MAIN domain asynchronous warm reset. Propagates immediately wihout any reset isolation sequence.

All modules in MAIN domain are reset except CTRLMMR register bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

Reason for this reset is captured in CTRLMMR reset status register. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.3.3 SMS_COLD_OUT_RST_n Reset (MCU Domain)

Reset Overview

The device SMS will issue this reset upon a security error.

When this reset is enabled in MCU domain, it causes a whole device warm reset.

This SMS reset of the MCU domain is enabled only when the SMS_COLD_RESET_ENz bit in MCU domain CTRLMMR is '0'.

When the R5FSS is configured as a safety processor, it can block this reset from resetting the MCU domain.

This is an asynchronous reset type (takes effect immediately)

Note

This reset behavior is same as MCU_RESETz reset signal (MCU_RESETz HW Pin).

MCU Domain Effect

All modules in MCU domain are reset except for CTRLMMR bits which are reset only on MCU_PORz.

IOs are not affected.

R5FSS is reset.

When MCU_RESETz is de-asserted, the MCU domain will be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in the CTRLMMR reset source register **WKUP_CTRL_MMR_CFG0_RST_SRC**.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.4 VTM Thermal Alert Reset

Reset Overview

The VTM has a hardware alert signal that indicates a fault when any of the sensors listed in *Voltage and Thermal Manager Locations* detect that the device is nearing the maximum temperature allowed.

This alert can be used to reset the device or part of the device to reduce the temperature. This alert is not a standard interrupt and so it does not include the usual set, clear and enable features. It does include an overall enable MMR bit, VTM_CFG2_MISC_CTRL, along with enables per sensor from VTM_CFG1 Registers.

The VTM module outputs an alert signal (THERM_MAXTEMP_OUTRANGE_ALERT), when the device temperature goes beyond a maximum threshold.

This reset signal creates a MCU domain warm reset.

VTM alert will be active as long as the error condition (Device Temperature > Maximum Temperature Threshold) is still TRUE.

When the error goes away, VTM alert will be de-asserted and device will come out of warm reset.

Note

This signal, when asserted HIGH, will cause a device warm reset similar to MCU_RESETz.

MCU Domain Effect

All modules in MCU domain are reset except for MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not affected.

This reset is active as long as the VTM alert is active.

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the MCU domain needs to be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not affected.

All processor cores are reset (A53SS and R5FSS).

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the device goes through full initialization procedure. The reason for this reset is captured in the CTRLMMR reset source register **WKUP_CTRL_MMR_CFG0_RST_SRC**.

Additional Reset Details

VTM alert use-case example:

VTM sends out a warning signal before generating the Max Temp Alert.

There are 2 different threshold settings for max temperature limits.

The first one has a lower threshold which will generate an interrupt to the processor for taking action to reduce frequency, turn-off power domains, etc. This should eventually lower the temperature and avoid the Max Temp Alert.

If the interrupt does not fix the rising temperature, then VTM will issue a Max Temp Alert. This will cause a device warm reset. The VTM Max Temp Alert will be active as long as die temperature is above the programmed threshold.

Device warm reset will default certain power domains to off mode (default at power-up). This should eventually lower the die temperature further.

Software can read the reset status register to poll on the cause of the warm reset. If it is from VTM, then it can wait for additional time before turning on the power domains.

6.3.5.5 MAIN ESM_ERRORz Reset

Reset Overview

This reset is issued when a MAIN domain processor (A53SS, SMS, or R5FSS) detects a catastrophic software error or a MAIN domain WDT timeout event occurs.

Errors in the MAIN domain cause the MAIN ESM module to trigger ESM_ERRORz.

This is routed as internal MAIN domain warm reset when enabled by the WKUP domain CTRLMMR reset control bit (MAIN_ESM_ERROR_RST_ENz).

This is an asynchronous reset type (takes effect immediately).

Reset MCU Domain Effect

When MCU domain is configured to operate independently, MCU domain reset isolation sequence is completed before propagating the RESETz to main domain.

MCU IOs are not affected.

When MCU domain is not configured as independent then, this reset will also warm reset MCU domain.

Reset MAIN Domain Effect

All modules in MAIN domain are reset except for MAIN domain CTRLMMR bits which are reset only on PORz.

IOs are not affected.

The device will re-boot. During boot-up, the R5FSS (secondary boot loader) will poll the CTRLMMR reset registers and reconfigure the MCU domain/R5FSS processor accordingly.

Note

If the device boot fails, and the MCU_ERRORn level is still LOW, then an external safety device should issue the MCU_PORz Reset to allow the device to recover from this error.

6.3.5.6 MCU ESM_ERRORz Reset

Reset Overview

This reset is issued when the R5FSS detects a catastrophic safety error or a MCU WDT timeout occurs.

Errors in the MCU domain cause the MCU ESM module to trigger error output.

This is routed as a device warm reset when enabled by the MCU domain WKUP_CTRL_MMR1 bit (MCU_ESM_ERROR_RST_ENz).

This is an asynchronous reset type (takes effect immediately).

MCU Domain Effect

All modules in MCU domain are reset except for MCU domain WKUP_CTRL_MMR1 bits which are reset only on PORz.

IOs are not affected.

Error is reported on MCU_ERRORn pin.

When SAFETY_ERROR_RST_n is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

External hardware (PMIC or secondary MCU safety channel) must issue MCU_PORz to recover from this error.

MAIN Domain Effect

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain WKUP_CTRL_MMR0 bits which are reset only on PORz.

IOs are not affected.

Device will re-boot. During boot-up, the R5FSS (secondary boot loader) will poll the CTRLMMR reset source register and configure the MCU domain/R5FSS processor accordingly.

If the device boot fails, and MCU_ERRORn level is still LOW, then an external safety device should issue the MCU_PORz reset to allow the device to recover from the error.

6.3.5.7 DM_WDT_RST_n Reset

Reset Overview

During Deeplseep resume sequence if the Device Manager is unable to respond due to a software bug, the WKUP domain WDT timer will issue this reset signal.

When this reset is enabled in MCU domain, it causes a whole device warm reset.

This WKUP WDT reset is enabled only when the DM_WDT_RST_EN_z bit in MCU domain CTRLMMR is '0'.

When the R5FSS is configured as a safety processor, it can block this reset from resetting the MCU domain. This is an asynchronous reset type (takes effect immediately)

Note

This reset behavior is same as MCU_RESETz reset signal (MCU_RESETz HW Pin).

MCU Domain Effect

All modules in MCU domain are reset except for MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not affected. R5FSS is reset.

When this reset is de-asserted, the MCU domain will be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (A53SS, SMS, and R5FSS).

When this reset is de-asserted, the device goes through full boot. The reason for this reset is captured inthe CTRLMMR reset source register.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain/R5FSS processor accordingly.

6.3.5.8 HHV

IOs support HHV mode during power up. HHV is active when PORz signal is driven LOW.

HHV allows IO cells to be tri-stated and is an IO feature. All IO cells have HHV which is asserted (driven) by HHV generated during PORz assertion. There are default pull values during this HHV/PORz assertion specified in the device Datasheet for each pin. All HHV logic controlling the buffer output enable and associated default internal pull for each IO will be applied.

HHV Timing Diagram demonstrates the timing sequence for the device HHV signals.

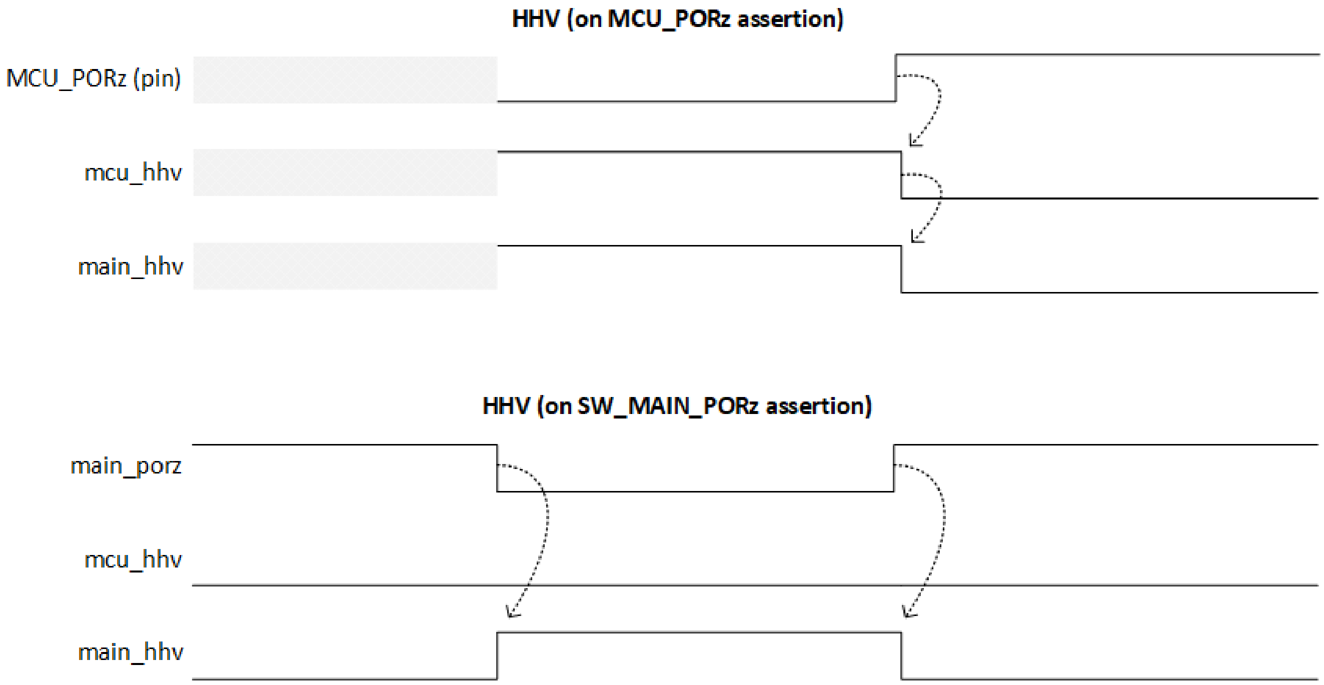

Figure 6-25. HHV Timing Diagram

6.3.5.9 BOOTMODE Pin Latching

This device requires several Boot Mode controls to enable device boot. The BOOTMODE inputs are not implemented on dedicated pins. They are multiplexed with other signal functions, where pins associated with the BOOTMODE inputs are defined in the Pin Attributes table. The logic state of the BOOTMODE inputs are latched on the rising edge of PORz_OUT. Valid logic states must be maintain as long as PORz_OUT is held low. The latched values are reflected in WKUP CTRL MMRs for read/write access.

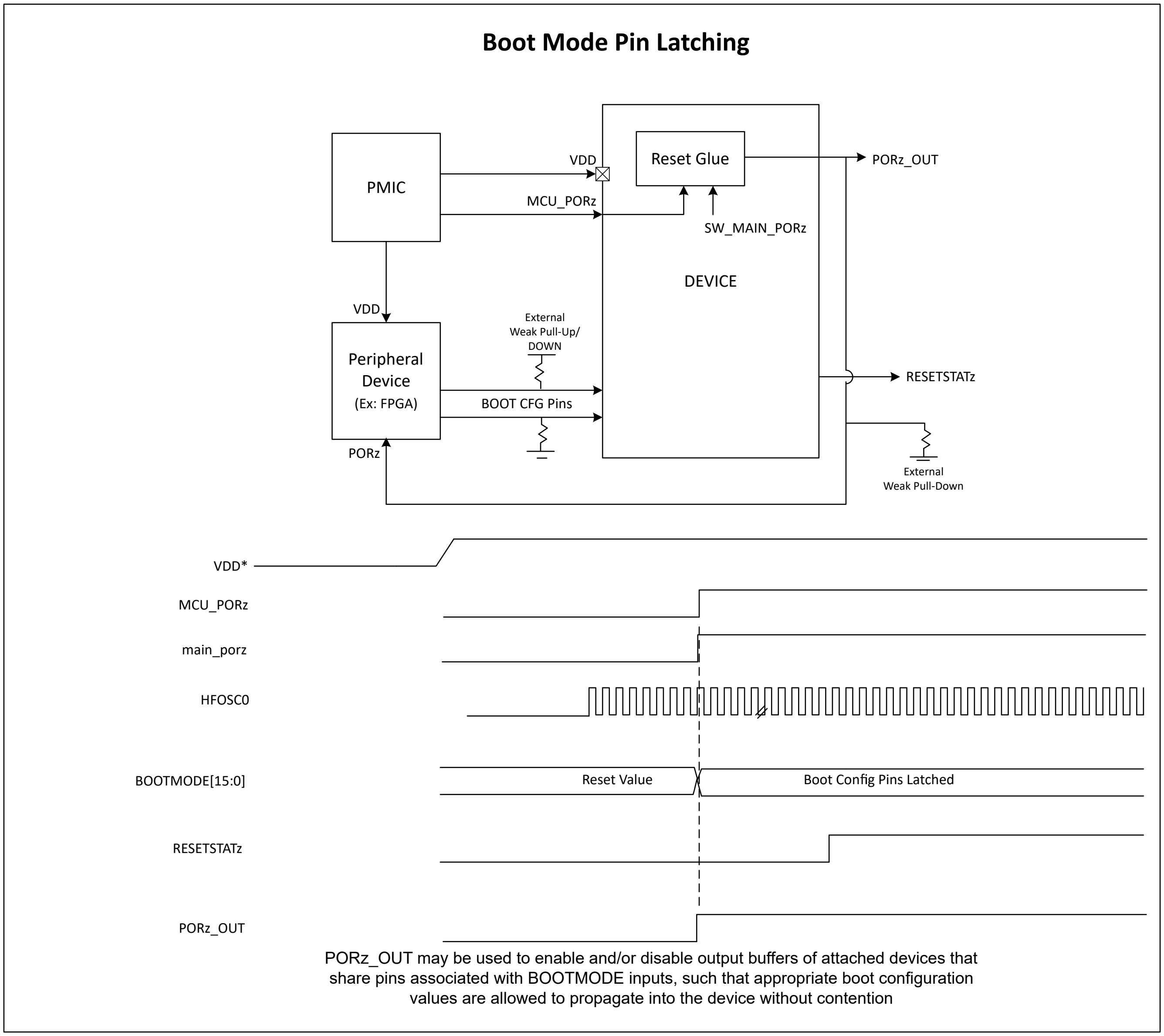
Boot Mode Pin Latching

PORz_OUT may be used to enable and/or disable output buffers of attached devices that share pins associated with BOOTMODE inputs, such that appropriate boot configuration values are allowed to propagate into the device without contention

Figure 6-26. BOOTMODE Pin Latching

6.3.5.10 Power-on-Reset Sequence

Figure 6-27 and Figure 6-28 give a high-level overview of the device power-up sequence.

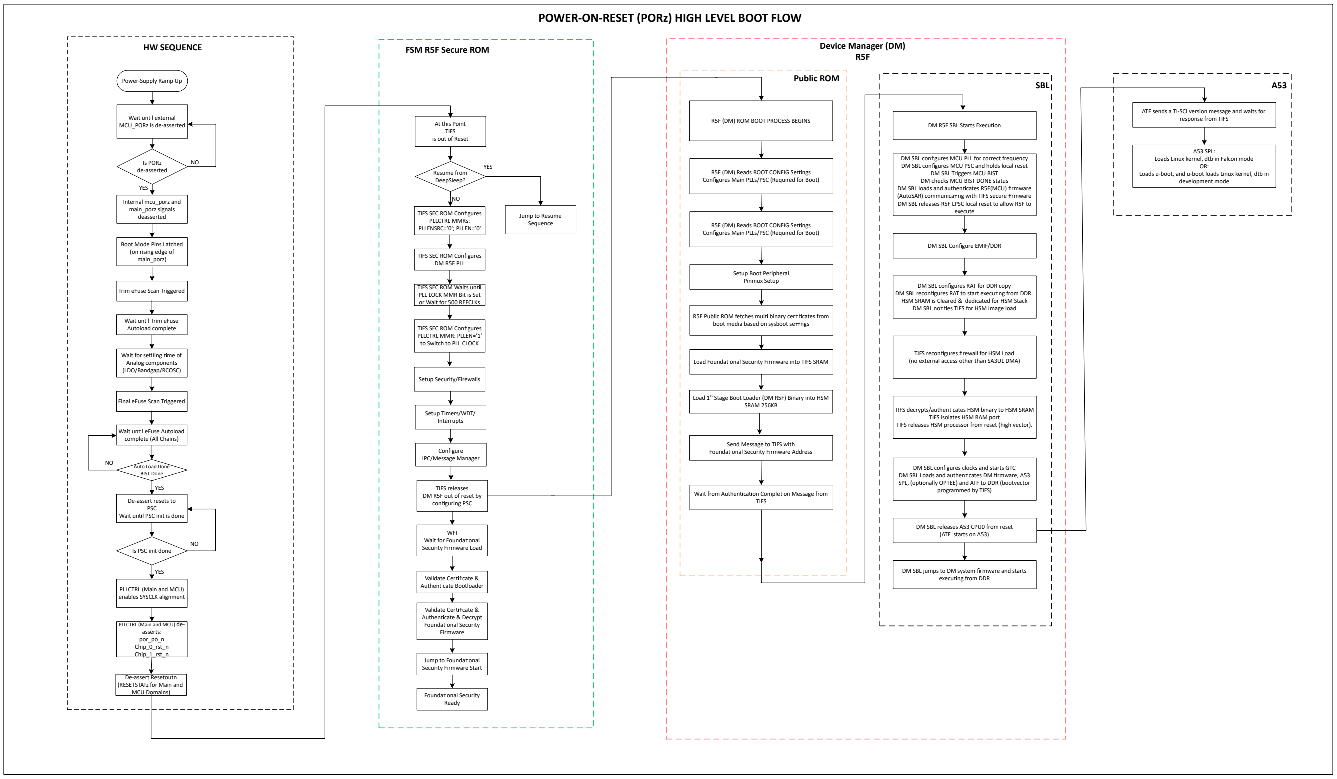

Figure 6-27. Power-up/Boot Flow Chart

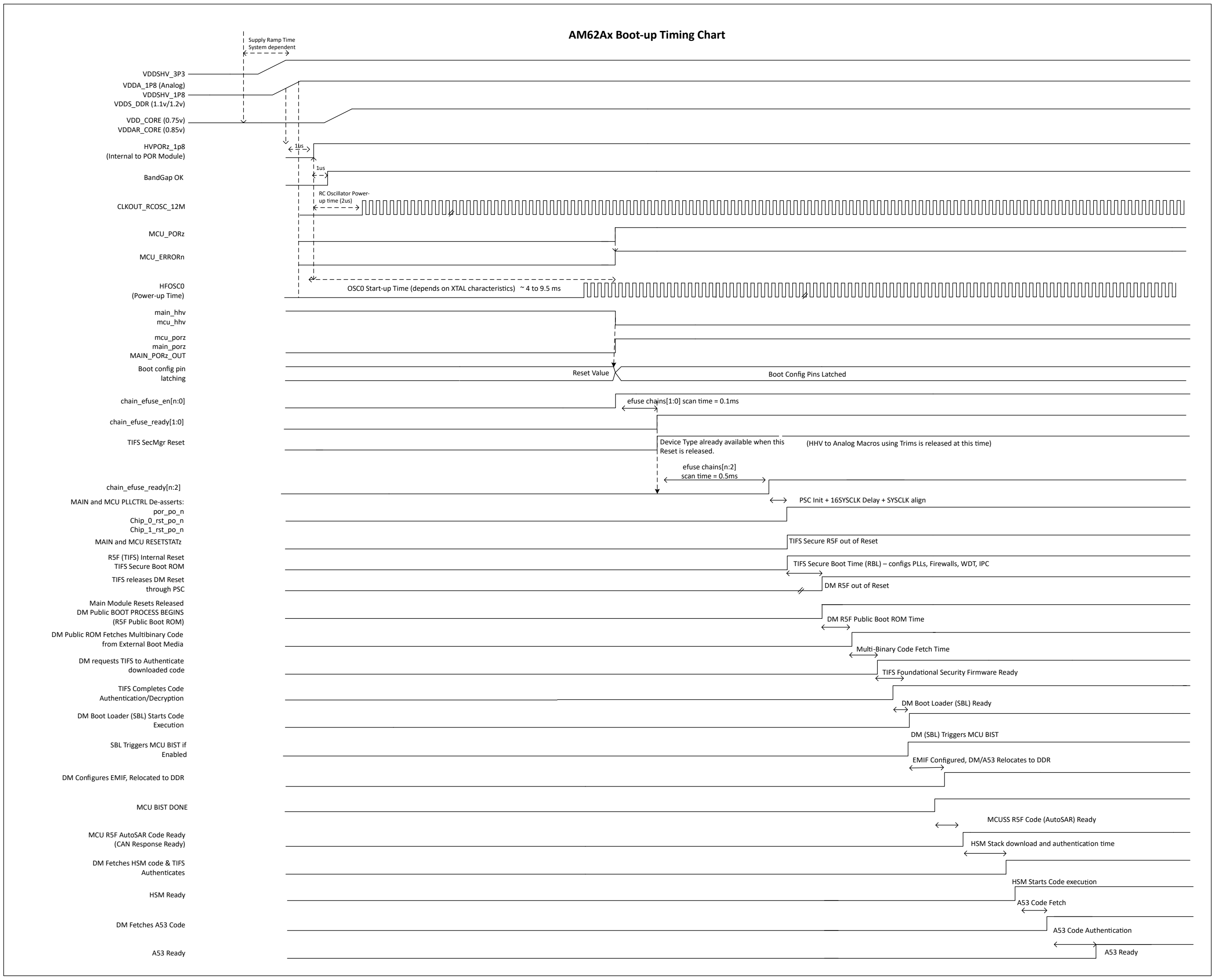

Figure 6-28. Power-up/Boot Timing Chart

6.3.5.11 Low Power Mode Reset Handling

This device supports Low Power & Deepsleep modes where parts of the device are switched-off through internal Power-Domain switches. To support these low power modes the device is partitioned so that only a small region is kept active (Wake-up) and the rest can be powered off through power-down switches. During deepsleep mode, several power-domains in Main domain are powered off and its PORz will be asserted.

Figure 6-29 shows the high-level overview of Power domain partitions.

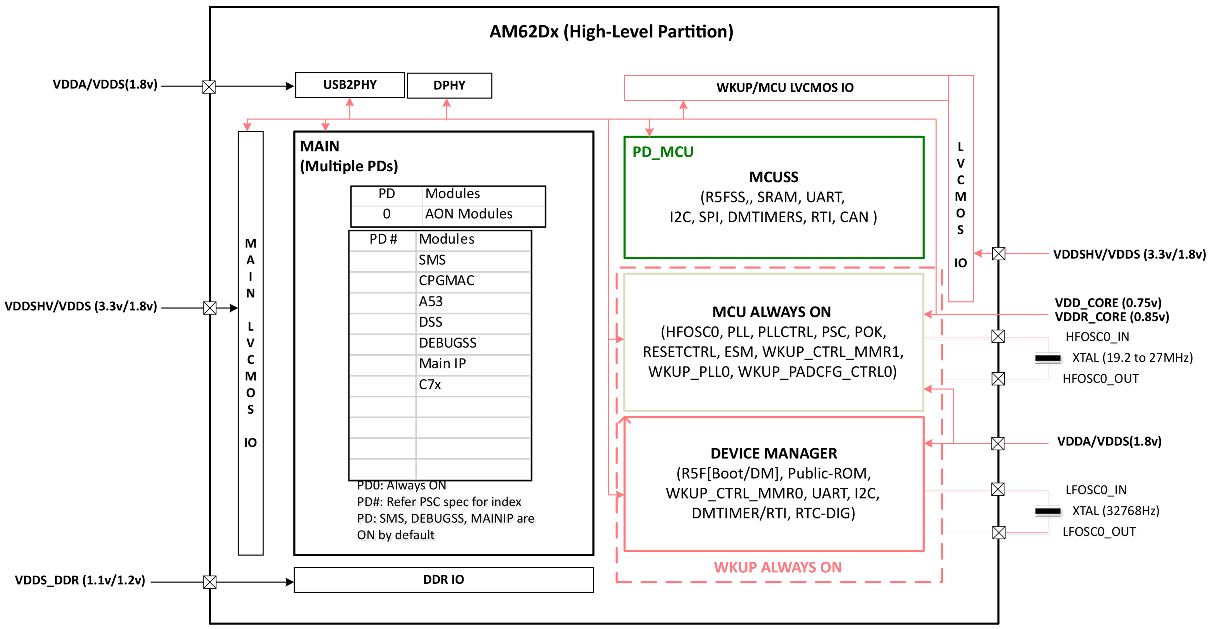

Figure 6-29. Power Domain Partitions

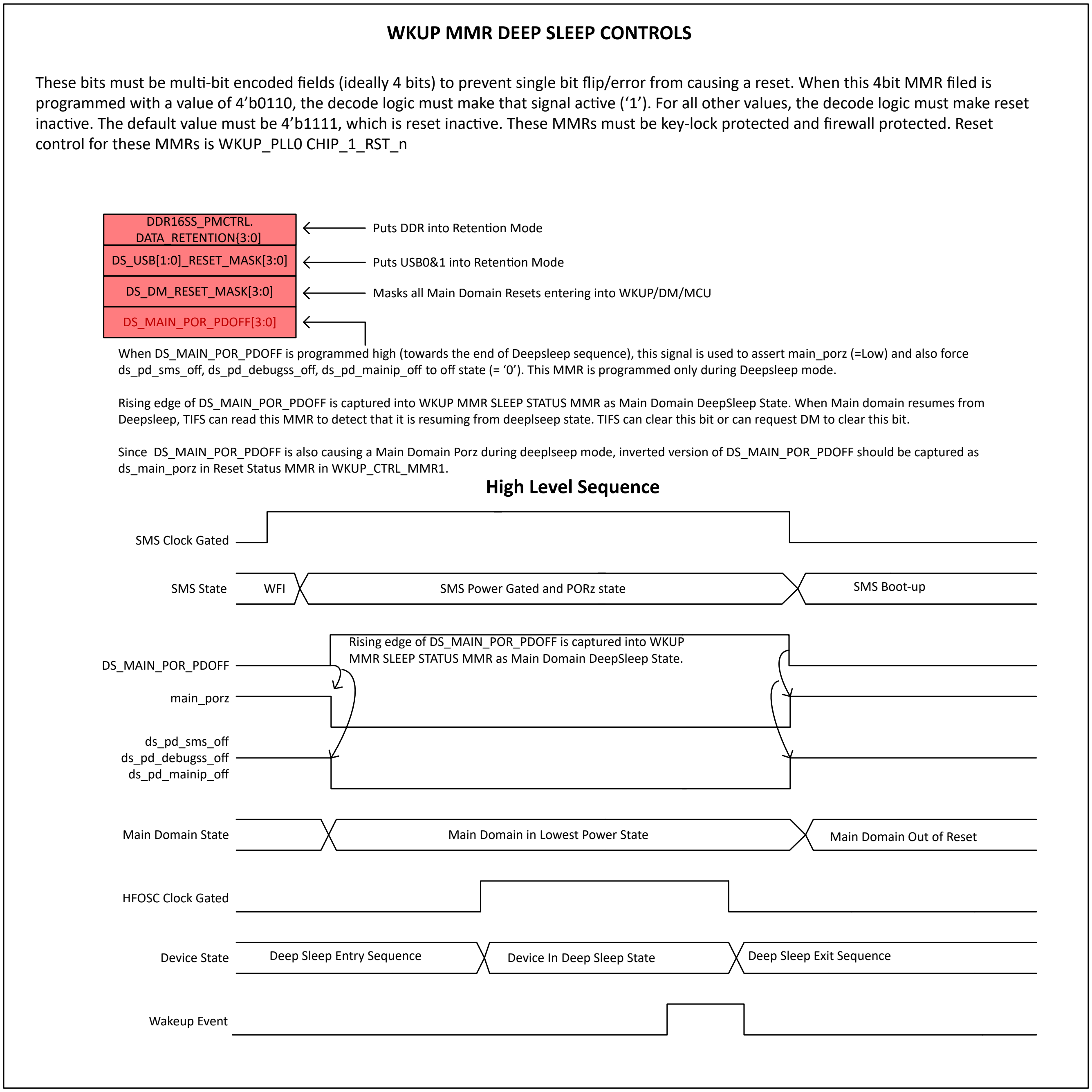

WKUP MMR DEEP SLEEP CONTROLS

These bits must be multi-bit encoded fields (ideally 4 bits) to prevent single bit flip/error from causing a reset. When this 4bit MMR filed is programmed with a value of 4’b0110, the decode logic must make that signal active (‘1’). For all other values, the decode logic must make reset inactive. The default value must be 4’b1111, which is reset inactive. These MMRs must be key-lock protected and firewall protected. Reset control for these MMRs is WKUP_PLL0 CHIP_1_RST_n

When DS_MAIN_POR_PDOFF is programmed high (towards the end of Deepsleep sequence), this signal is used to assert main_porz (=Low) and also force ds_pd_sms_off, ds_pd_debugss_off, ds_pd_mainip_off to off state (= ‘0’). This MMR is programmed only during Deepsleep mode.

Rising edge of DS_MAIN_POR_PDOFF is captured into WKUP MMR SLEEP STATUS MMR as Main Domain DeepSleep State. When Main domain resumes from Deepsleep, TIFS can read this MMR to detect that it is resuming from deeplseep state. TIFS can clear this bit or can request DM to clear this bit.

Since DS_MAIN_POR_PDOFF is also causing a Main Domain Porz during deeplseep mode, inverted version of DS_MAIN_POR_PDOFF should be captured as ds_main_porz in Reset Status MMR in WKUP_CTRL_MMR1.

Figure 6-30. High-level Power Domain Partitions

Figure 6-31 depicts a high-level deep-sleep sequence. For more details please refer to Low Power Management Chapter.

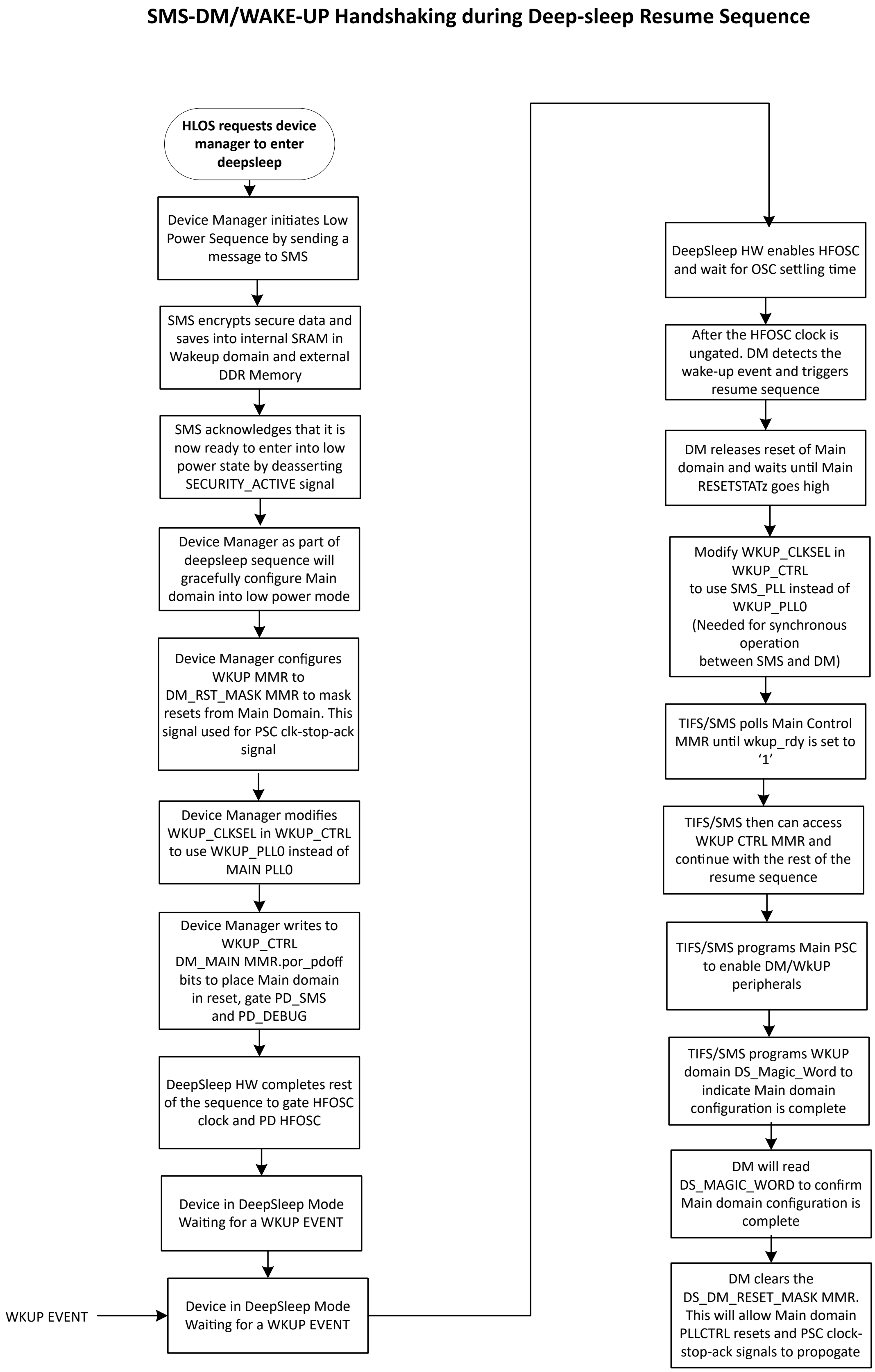

Figure 6-31. Deepsleep Reset Handling

6.4 Clocking

This chapter describes the clock architecture of the device.

6.4.1 Overview

To satisfy the various subsystems requirements, the device features multiple clock sources and clock generators:

- External Crystal Driver
- Internal Oscillator
- Phase-Locked Loop circuits (PLLs)
- Dividers

Figure 6-32 shows the device top-level clock diagram. The clocking is divided into three clocking domains - WKUP, MCU and MAIN.

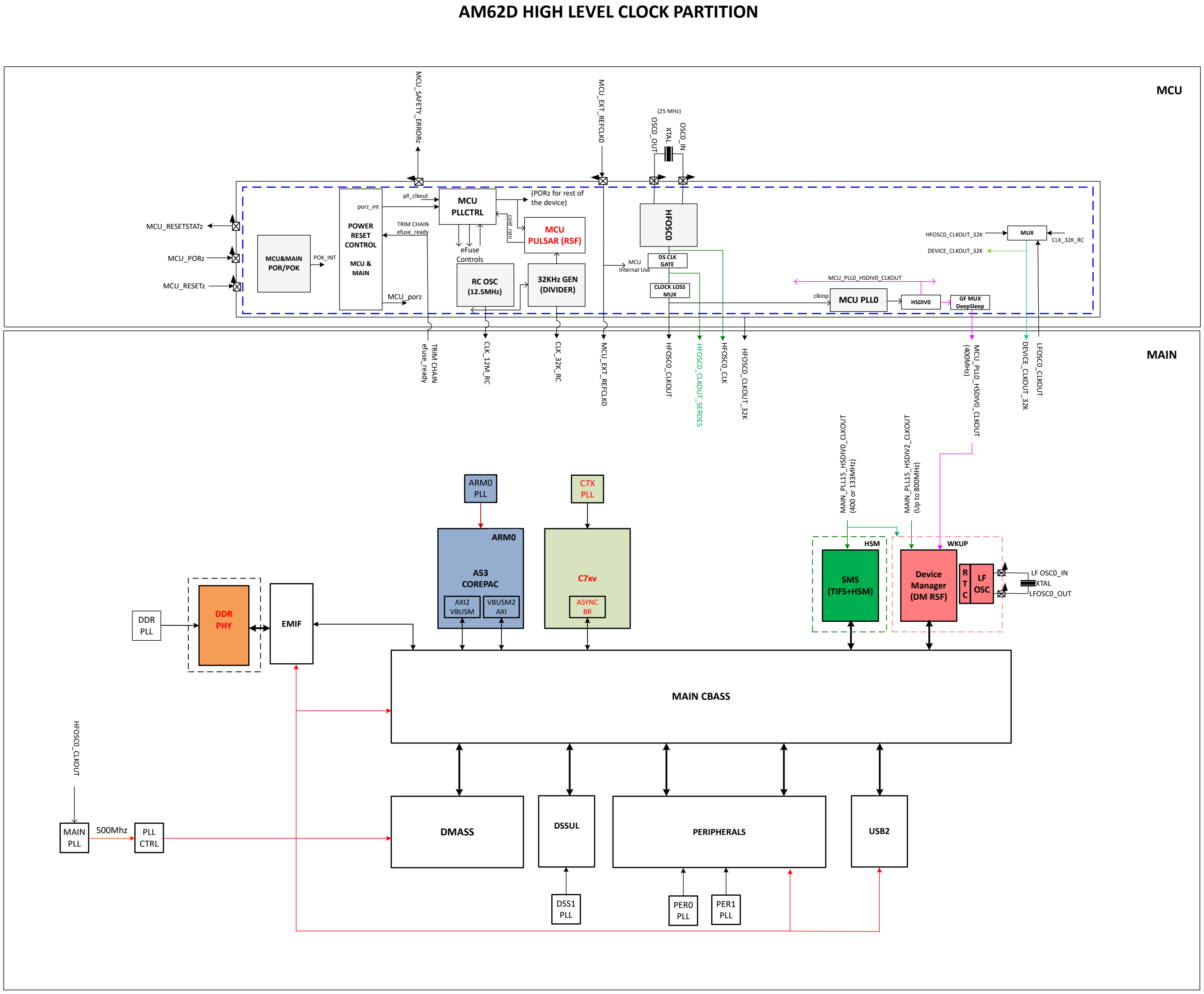

Figure 6-32. Top-Level Clock Diagram

6.4.2 Clock Inputs

6.4.2.1 Overview

Various external clock inputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators
  - MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins of the internal oscillator which sources a reference clock. Provides reference clock to PLLs within MCU and MAIN domain.
- Low frequency oscillators
  - LSOSC0_IN/LFOSC0_OUT - external 32.768KHz crystal interface pins of the internal oscillator which sources a reference clock. Provides reference clock to RTC and Timers within MCU and MAIN domain.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock input (MCU domain).
  - EXT_REFCLK1— optional external system clock input (MAIN domain).
- External CPTS reference clock inputs
  - CP_GEMAC_CPTS0_RFT_CLK — CPTS reference clock input for CPSW and Timers in MAIN.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[1:0] — optional McASP high-frequency input clocks when configured to operate as an input.

Note

Other clock inputs that are routed directly to the subsystems are described in the respective subsystem chapters.

6.4.3 Clock Outputs

The device provides several system clock outputs. Summary of these output clock signals is as follows:

- MCU_SYSCLKOUT0
- MCU_OBSCLK0
- SYSCLKOUT0
- OBSCLK0
- OBSCLK1
- WKUP_CLKOUT0
- CLKOUT0
- AUDIO_EXT_REFCLK[1:0]

Other clock outputs, that are routed directly from subsystems to device pins, are described in the respective module chapter.

Observation clock pins - MCU_OBSCLK0, OBSCLK0 and OBSCLK1 serve the following purposes:

- During testing, PLLs on the device are configured to output all operating frequencies desired by each module to characterize PLL performance.
- System debug: during debug, clocks from various PLLs can be inspected for possible clues. Example clock glitches, lock loss etc.

Note

Maximum frequency supported on both MCU_OBSCLK0, OBSCLK0 and OBSCLK1 pins is 200 MHz. Hence the divider at the output of each OBSCLK mux must be programmed to meet this limitation.

Unlike the OBSCLK pins which can select several different clocks for output, system clock pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources (see Section 6.4.3.2)

6.4.3.1 Observation Clock Pins

6.4.3.1.1 MCU_OBSCLK0 Pin

MCU_OBSCLK0 output is controlled by MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL register in the MCU_CTRL_MMR0 module; for more information about control registers, refer to *Control Module (CTRL_MMR)*. Two muxes are connected in series - MCU_OBSCLK0_MUX0 and MCU_OBSCLK0_MUX1, see Figure 6-33.

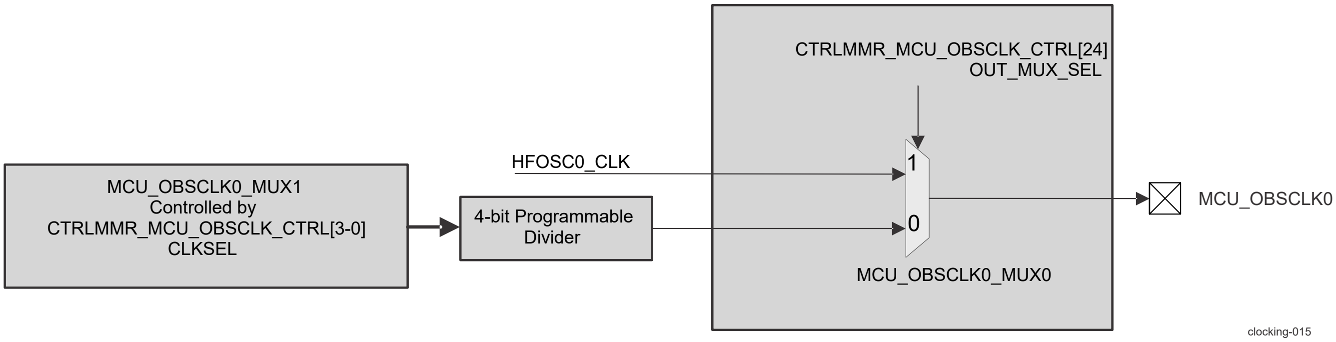

Figure 6-33. MCU_OBSCLK Muxes Diagram

How to select the output of MCU_OBSCLK0_MUX1 is described in Table 6-25.

Table 6-25. MCU_OBSCLK0_MUX1 Output Clock Selection

MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[2][3-0] CLK_SEL	MCU_OBSCLK0_MUX1 Output Clock Selection[1]
0x0	CLK_12M_RC
0x1	0 (GND)[3]

Table 6-25. MCU_OBSCLK0_MUX1 Output Clock Selection (continued)

MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[2][3-0] CLK_SEL	MCU_OBSCLK0_MUX1 Output Clock Selection[1]
0x2	MCU_PLL0_HSDIV0_CLKOUT
0x3	MCU_PLL0_HSDIV4_CLKOUT
0x4	MCU_PLLCTRL0_PLL_CTRL_OBSCLK_CLK
0x5	CLK_32K_RC
0x6	HFOSC0_CLKOUT
0x7	HFOSC0_CLKOUT_32K
0x8	MCU_SYSCLK0
0x9	DEVICE_CLKOUT_32K
0xA-0xF	RESERVED[3]

(1) Software-controlled 4-bit divider is used to obtain the divided versions of the clocks passed to MCU_OBSCLK1 mux

(2) For more information about control registers, refer to *Control Module (CTRL_MMR)*.

(3) GND - ground

The value of the software-controlled 4-bit divider is determined by the MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[11-8] CLK _DIV field; for more information about control registers, see *Control Module (CTRL_MMR)*.

Note

MCU_OBSCLK1_MUX0 is provided as a low jitter output for HFOSC0_CLK. In this configuration, MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[3-0] should be configured as 0x1 (1, selecting a logical low signal) and MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[24] should be configured as 0x1.

6.4.3.1.2 OBSCLK0 Pin

The OBSCLK0 output pin is controlled by MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL register in the CTRL_MMR0 module; for more information about control registers, refer to *Control Module (CTRL_MMR)*. Figure 6-34 shows a block diagram of internal OBSCLK0 mux connections.

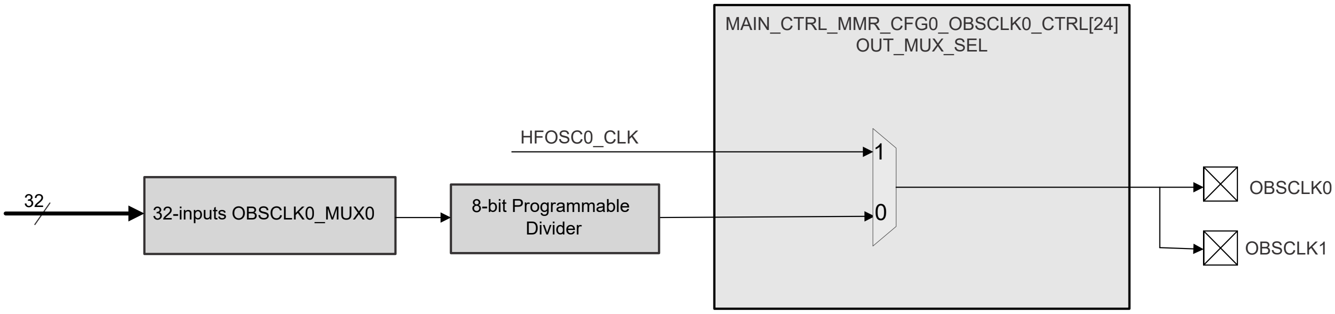

Figure 6-34. OBSCLK0 Muxes Diagram

Table 6-26. OBSCLK0 Clock Selection

MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[2][4-0] CLK_SEL	OBSCLK0 Selection [1]
0x0	MAIN_PLL0_HSDIV0_CLKOUT
0x1	MAIN_PLL1_HSDIV0_CLKOUT
0x2	MAIN_PLL2_HSDIV0_CLKOUT
0x3	A53_DIVH_CLK4_OBSCLK_OUT_CLK
0x4	DDRSS_DDR_PLL_CLK_DIV4

Table 6-26. OBSCLK0 Clock Selection (continued)

MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL(2)[4-0] CLK_SEL	OBSCLK0 Selection (1)
0x5	CLK_12M_RC
0x6	HFOSC0_CLKOUT_32K
0x7	PLLCTRL0_PLL_CTRL_OBSCLK_CLK
0x8	HFOSC0_CLKOUT
0x9	CLK_32K_RC
0xA	CPSW0_CPTS_GENF0
0xB	CPSW0_CPTS_GENF1
0xC	MCU_PLL0_HSDIV0_CLKOUT
0xD	MAIN_PLL15_HSDIV0_CLKOUT
0xF	MAIN_PLL17_HSDIV0_CLKOUT
0x10	MAIN_SYSCLK0
0x11	DEVICE_CLKOUT_32K
0x12	MAIN_PLL5_HSDIV0_CLKOUT
0x13	C7XV_DIVH_CLK4_OBSCLK_OUT_CLK
0x14-0x1F	RESERVED(3)

(1) Software-controlled 8-bit divider is used to obtain the divided versions of the clocks passed to output pins

(2) For more information about control registers, refer to *Control Module (CTRL_MMR)*.

(3) GND - ground

The value of the software-controlled 8-bit divider is determined by register MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[15-8] CLK_DIV; for more information about control registers, refer to *Control Module (CTRL_MMR)*.

6.4.3.2 System Clock Pins

6.4.3.2.1 MCU_SYSCLKOUT0

MCU_SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (MCU_SYSCLKOUT0). This signal can be used to test if the specific device clock is functioning or not.

Note

MCU_SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

6.4.3.2.2 SYSCLKOUT0

SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the specific device clock is functioning or not.

Note

SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

6.4.3.2.3 WKUP_CLKOUT0

The WKUP_CLKOUT0 output pin is controlled by the WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL register in the WKUP_CTRL_MMR0 module; for more information about control registers, refer Control Module (CTRL_MMR). Figure 6-35 shows a block diagram of internal WKUP_CLKOUT0 mux connections.

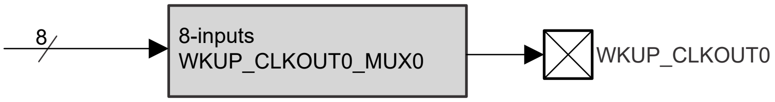

Figure 6-35. WKUP_CLKOUT0 Mux Diagram

Table 6-27. WKUP_CLKOUT0_MUX Output Clock Selection

WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL[2][2-0] WKUP_CLKOUT_SEL	WKUP_CLKOUT0_MUX Output Clock Selection[1]
0x0	HFOSC0_CLK
0x1	LFOSC0_CLKOUT
0x2	MAIN_PLL0_HSDIV2_CLKOUT
0x3	MAIN_PLL1_HSDIV2_CLKOUT
0x4	MAIN_PLL2_HSDIV9_CLKOUT
0x5	DEVICE_CLKOUT_32K
0x6	CLK_12M_RC
0x7	HFOSC0_CLKOUT

(1) Software-controlled 8-bit divider is used to obtain the divided versions of the clocks passed to output pins.

(2) For more information about control registers, refer Control Module (CTRL_MMR).

6.4.4 Device Oscillators

The device has the possibility to source clocks of an external high-frequency oscillator - HFOSC0 and external 32.768KHz oscillator - LFOSC0. The device has also one internal RC oscillator - CLK_12M_RC.

6.4.4.1 Device Oscillators Integration

6.4.4.1.1 High-Frequency Oscillator with External Crystal

By default, HFOSC0 is enabled after PORz. It supports a bypass mode. In this mode, an external clock can be driven on the XI Pin.

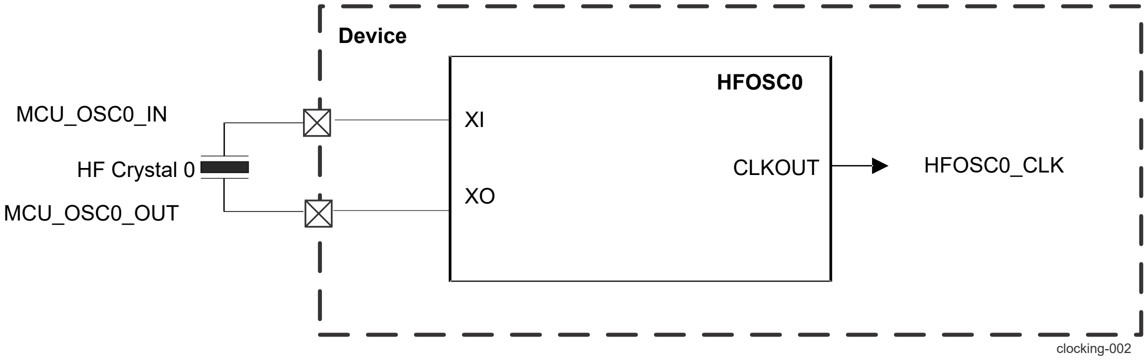

Figure 6-36. HFOSC0 Integration Diagram

6.4.4.1.2 Low-Frequency Oscillator with External Crystal

By default, LFOSC0 is disabled after PORz. It supports a bypass mode. In this mode, an external clock can be driven on the XI Pin.

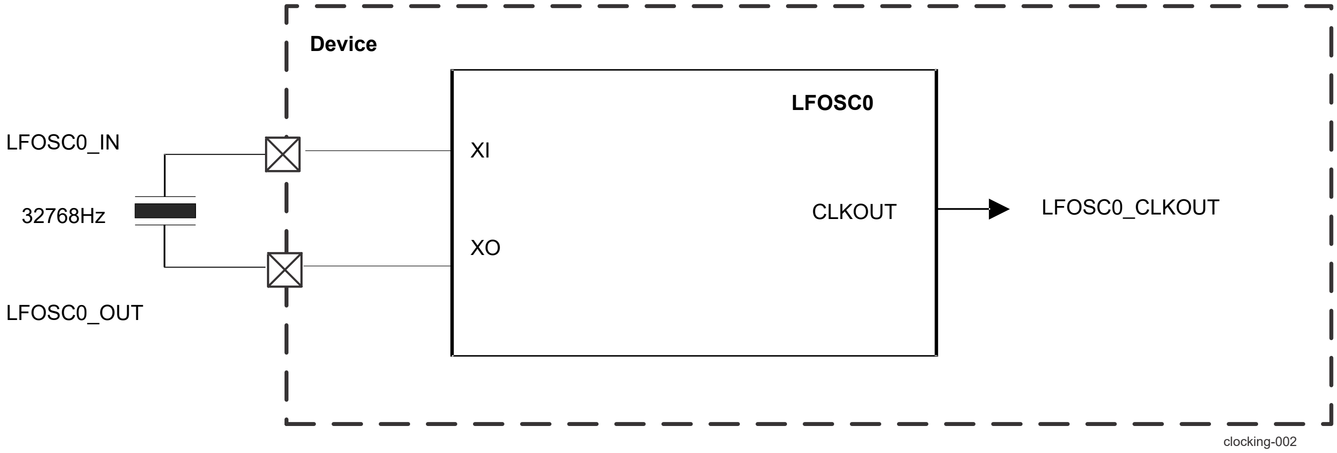

Figure 6-37. LFOSC0 Integration Diagram

6.4.4.1.3 Internal RC Oscillator

CLK_12M_RC in always oscillate mode.

The 12.5-MHz RC clock output (CLK_12M_RC) is used by the on-chip Reset Glue logic, Power Reset Generator (PRG) circuits, HFOSC0 Loss Circuits, Dual Clock Comparator (DCC) and Timer Modules.

Note

An output clock of CLK_12M_RC is further divided down to generate a 32-kHz clock (CLK_32K_RC). This clock is used by SMS and Timer Modules.

The actual value of the derived CLK_32K_RC will vary with PVT variations.

6.4.4.2 Oscillator Clock Loss Detection

The device supports HFOSC0 clock loss circuitry to detect when HFOSC0_CLK stops toggling. Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN is set , the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the device to operate with a slower clock. The HFOSC0_CLK clock loss condition is reported as an error to MCU_ESM0 regardless of the value of MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN. Integration diagram of HFOSC0 clock loss detection is presented in Figure 6-38.

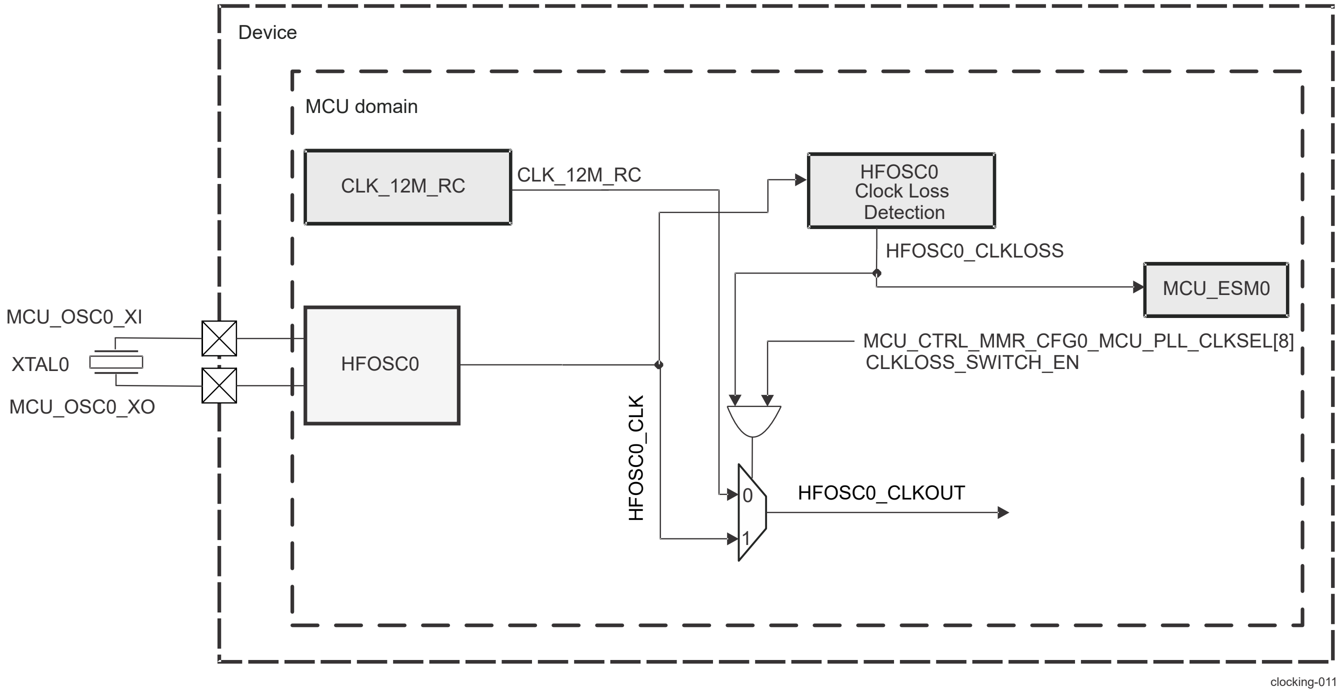

Figure 6-38. HFOSC0 Clock Loss Detection Integration Diagram

MCU_ESM0 can optionally generate an interrupt to MCU_R5FSS and DM_R5FSS0 so they can save some critical contents such as error logging to scratch pad memory or external flash. ESM must also be configured to report this error on the MCU_ERRORn pin.

HFOSC0 clock loss is a catastrophic failure since this clock is the most critical system clock. During the clock loss condition an external system intervention is required.

The clock loss mux is not a glitch free mux. The mux control is synchronized to the CLK_12M_RC clock. Since HFOSC0_CLK has stopped switching the mux should transition to RC Clock without producing glitches.

During clock-loss condition, the device reports the error to the external device through MCU_ERRORn pin - the pin is driven Low. The recovery mechanism is up to the external system (such as a PMIC to take action). For example, it can try a full system power cycle to see if the system recovers. If the system does not recover then, it has to take some other action such as to check system clocks, external crystal or supply rails.

Device PLLs will lose lock when clock loss is detected. During this time 12.5-MHz RC clock is output through the bypass muxes. The PLL will relock to a new frequency based on 12.5 MHz RC clock.

In an event of clock glitch which may potentially hang the device, then the SMS watchdog timer will expire and will generate an internal reset for the whole device.

6.4.5 PLLs

Phase-Locked Loop circuits (PLLs) in the device are clock generator PLLs, which multiply the lower-frequency reference clock up to the operating frequency of the respective subsystem(s).

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

6.4.5.1 MCU Domain PLL Overview

MCU_PLL0 (MCU PLL) with MCU_PLLCTRL0 are present in the device in MCU domain. An overview is shown on Figure 6-39. For more specific information about PLLs see Section 6.4.5.5 , *PLLs Device-Specific Information*.

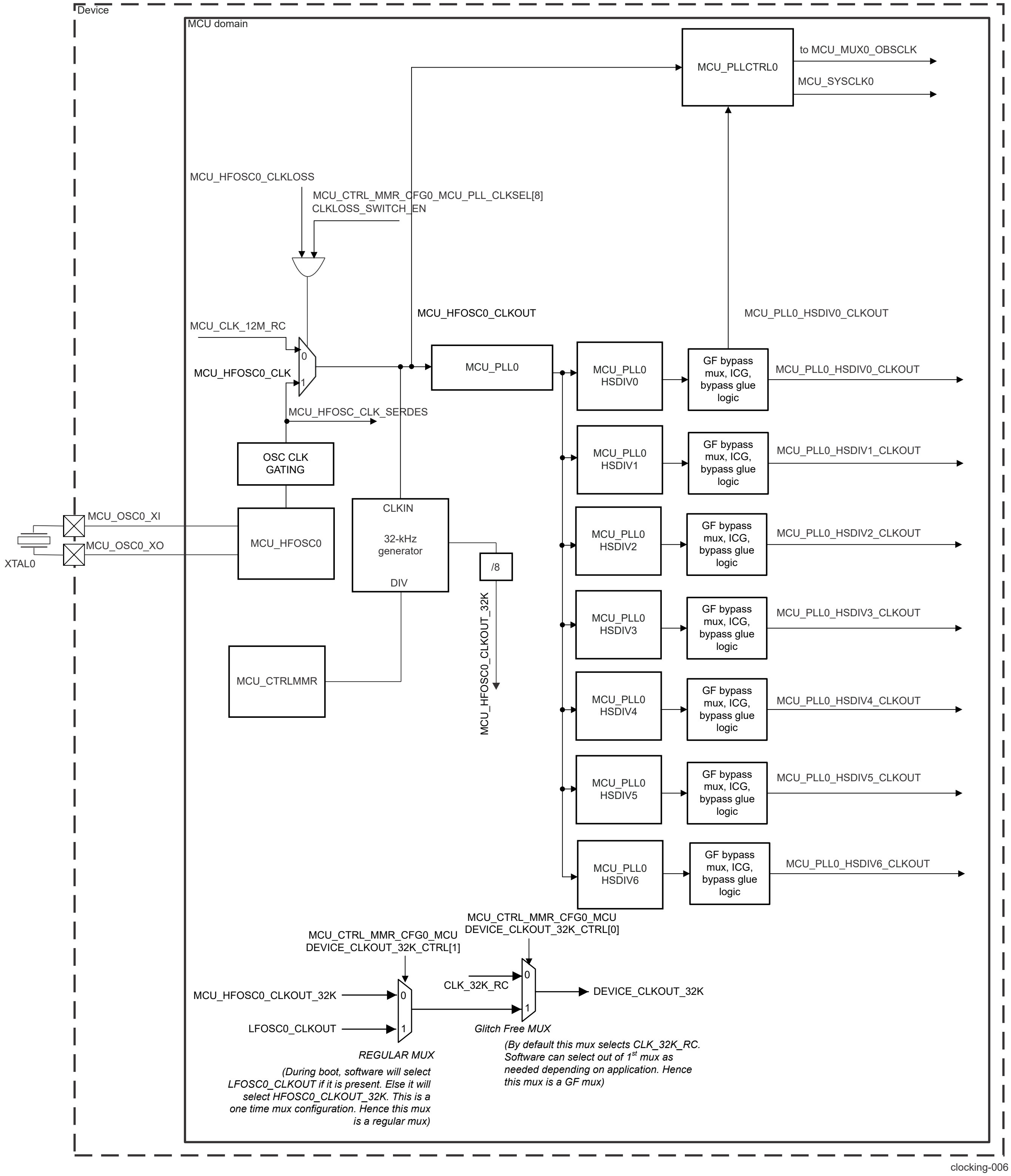

Figure 6-39. MCU Domain PLLs Integration

6.4.5.2 MAIN Domain PLLs Overview

The following are the PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0

- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL5
- PLL7 (C7x PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL15 (SMS PLL)
- PLL17

Overview of the device PLLs with their reference clock options in MAIN domain is shown on Figure 6-40. For more specific information about PLLs see Section 6.4.5.5 , *PLLs Device-Specific Information*.

Note

The external muxes of choosing the reference clocks are glitch-free muxes.

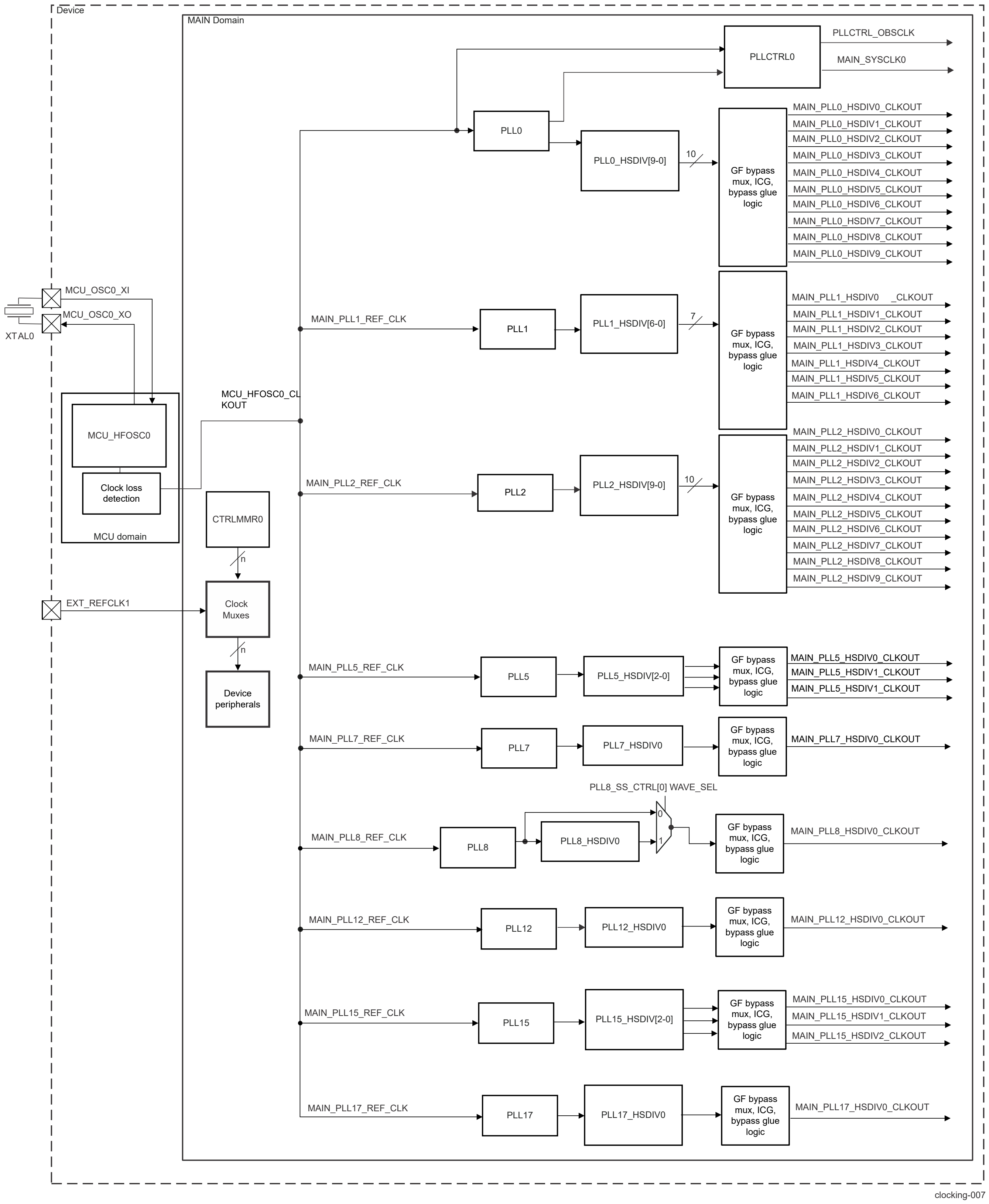

Figure 6-40. MAIN Domain PLLs Integration

6.4.5.3 PLL Reference Clocks

6.4.5.3.1 PLLs in MCU Domain

The reference clock MCU_PLL0_REF_CLK for the PLL in MCU domain is chosen between the internal high-frequency (HF) oscillator with external crystal (HFOSC0) and 12.5-MHz free-running RC oscillator. The selection is made through MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN, see Table 6-28.

Table 6-28. PLL MCU Domain Reference Clock Selection - HFOSC0_CLKOUT Selection

MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL(1)[8] CLKLOSS_SWTCH_EN	MCU_PLL0_REF_CLK
0 (default)	HFOSC0_CLK
1	CLK_12M_RC if clock loss is detected or HFOSC0_CLK if clock loss is not detected

(1) For more information about control registers, see *Control Module (CTRL_MMR)*.

6.4.5.3.2 PLLs in MAIN Domain

Each PLL in MAIN domain has a dedicated register (**MAIN_CTRL_MMR_CFG0_MAIN_PLLn_CLKSEL**, n = 0 to 2, 8, 12,15, 16, 17) in CTRL_MMR0 that contains associated control bits.

6.4.5.4 Generic PLL Overview

To generate high-frequency clocks, the device supports multiple on-chip PLLs controlled directly by the Top-level Clocking. Their type is Fractional PLL with Calibration (PLLTS16FFCLAFRACF2).

Note

This chapter discusses only the PLLs that are directly controlled by the Top-level Clocking. The other PLLs embedded in and managed by other subsystems are described in their respective subsystems.

6.4.5.4.1 PLLs Output Clocks Parameters

Figure 6-41 shows the functional architecture of a generic PLL for PLLTS16FFCLAFRACF2 type.

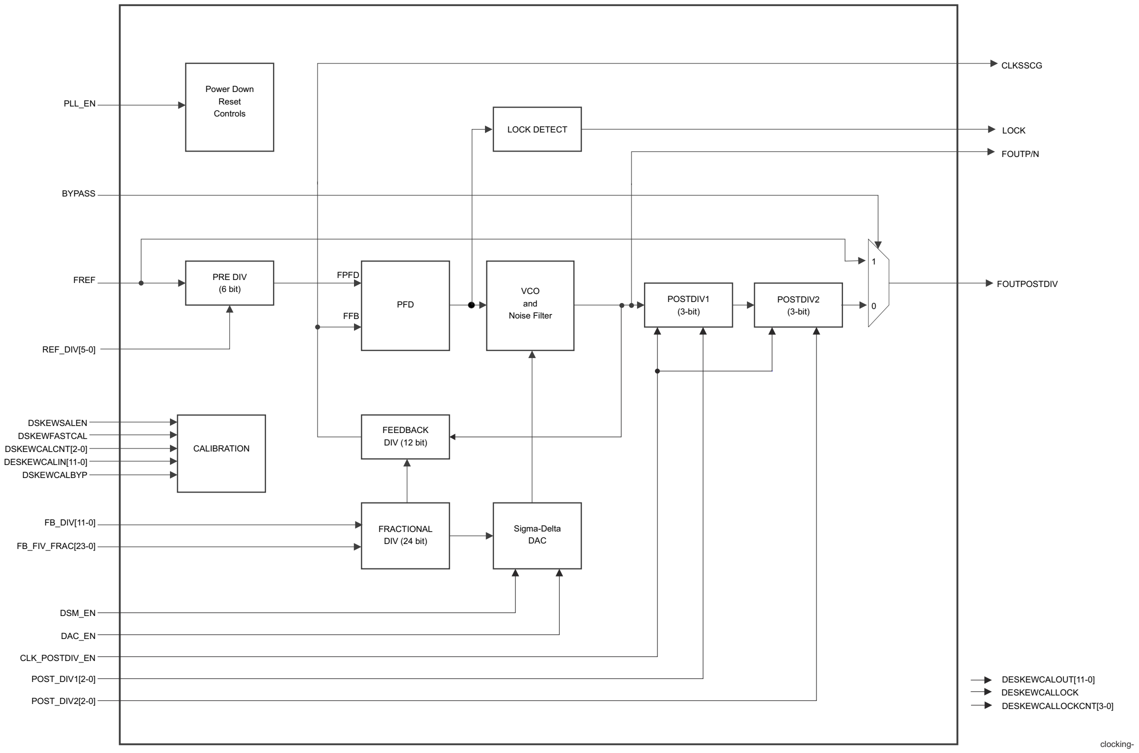

Figure 6-41. Generic PLL Functional Diagram for PLLTS16FFCLAFRACF2 Type

6.4.5.4.1.1 PLLs Input Clocks

As shown in Figure 6-41 the reference clock (FREF) input is used to generate the synthesized clock, but can also be used as the bypass clock for some outputs of the PLL whenever the PLL enters bypass mode. It is mandatory for the PLL clock synthesis.

6.4.5.4.1.2 PLL Output Clocks

6.4.5.4.1.2.1 PLLTS16FFCLAFRACF2 Type Output Clocks

Table 6-29 describes the output clocks of PLLTS16FFCLAFRACF2.

Table 6-29. PLLTS16FFCLAFRACF2 Output Clocks

Output	Description	Frequency
FOUTP	Positive phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTN	Negative phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTPOSTDIV	VCO-divided clock output.	FOUTP / (POST_DIV1*POST_DIV2)

Where:

- REF_DIV is the software-configured division ratio binary value.
- FB_DIV is the software-configured division ratio binary value.
- FB_DIV_FRAC is the software-configured fractional division.
- POST_DIV1 is the software-configured division ratio binary value.
- POST_DIV2 is the software-configured division ratio binary value.

Note

POST_DIV1 and POST_DIV2 valid values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater than POST_DIV2.

Note

For device-specific information about clock output parameters and synthesized clocks, see Table 6-33 and Table 6-34.

6.4.5.4.1.2.2 PLL Lock

PLL module outputs a lock status signal to indicate that the PLL has achieved frequency lock. When the PLL detects no cycle slips between the feedback clock (FFB) and reference clock FPFD (FREF/ REF_DIV[5-0]) for 128 consecutive cycles, it asserts the lock signal high. When the PLL detects any cycle slip, lock signal will go low and stays low until it detects no cycle slip for 128 consecutive cycles. This lock signal is captured in <PLL_name>_STAT[0] LOCK bit. Software can read this bit to determine if the PLL has achieved frequency lock before selecting the PLL clock through external bypass mux.

When PLL losses lock, there is a hardware mechanism to automatically bypass the PLL clock to the reference clock (FREF) using the external glitch free mux. BYP_ON_LOCKLOSS bit in <PLL_name>_CTRL register enables this automatic bypass mode on PLL lock loss. When the PLL re-locks, the glitch free mux switches to PLL clock out.

The PLL Lock signal is also routed to ESM module for error reporting. ESM can be configured to generate interrupts to MCU_R5FSS and R5FSS0/1 and assert Low on MCU_ERRORn pin on PLL Lock loss for further action.

6.4.5.4.1.2.3 HSDIVIDER

A PLL may contain up to 10 HSDIVIDER modules to produce more clocks with divided ratio based on the PLL synthesized clock frequency. HSDIVIDER provides only one output. The HSDIVIDER output clock frequency is given by the equations in Table 6-30.

Table 6-30. HSDIV_CLKOUT Frequency With PLL State

Equation	PLL Mode
HSDIV_CLKOUT = FOUTP / (HSDIV + 1)	Locked
HSDIV_CLKOUT = FREF	Before lock or during relock

Where:

- FOUTP is the PLL lock frequency.
- HSDIV is the software-configured division ratio binary value.

Figure 6-42 describes the connection between a HSDIV and a specific type of PLL. Signals related only to this connections are shown in both figures.

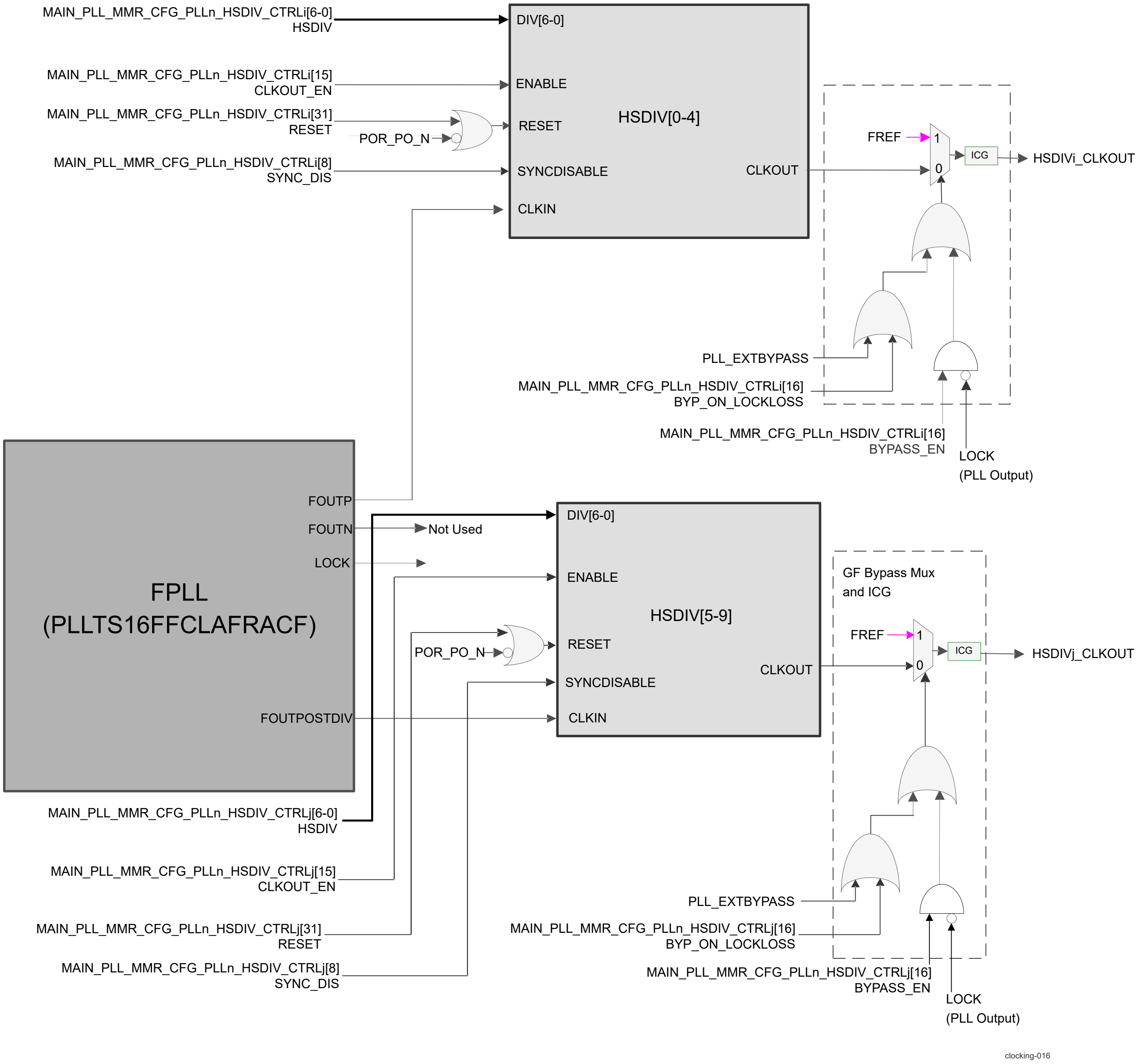

Note

(1)i = 0 to 4; j = 5 to 9

Figure 6-42. PLLTS16FFCLAFRACF2 and HSDIV Connection

6.4.5.4.1.2.4 ICG Module

ICG module ensures that when a particular HSDIV is not enabled the HSDIV clock output is gated off. This is a hardware module with no software control.

6.4.5.4.1.2.5 PLL Power Down

PLLTS16FFCLAFRACF2 is disabled with MCU_PLL_MMR_CFG_PLL0_CTRL[15] PLL_EN or MAIN_PLL_MMR_CFG_PLLn_CTRL[15] PLL_EN.

6.4.5.4.1.2.6 PLL Calibration

PLLTS16FFCLAFRACF2 has calibration feature. The calibration settings are done via <PLL_Name>_CAL_CTRL register. The calibration status can be monitored by reading <PLL_Name>_CAL_STAT register. For more information about device-specific information about calibration feature, see Table 6-35.

6.4.5.5 PLLs Device-Specific Information

Table 6-31 lists the basic information of the MCU PLL.

Table 6-31. Basic Information of MCU_PLL0

PLL name	Type	HSDIV Available	Input clock	Comments
MCU_PLL0	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4	HFOSC0_CLKOUT	See (1), (2), and (3)

---

(1) See Figure 6-41, *Generic PLL Functional Diagram for PLLTS16FFCLAFRACF2 type* for overview of the PLL.
(2) See Section 6.4.5.5.1 for synthesized clock parameters.
(3) See Section 6.4.5.5.2 for clock output parameters.

Table 6-32 lists the basic information of each of the MAIN PLLs.

Table 6-32. Basic Information of MAIN Domain PLLs

PLL name	Type	HSDIV Available	Input clock	Comments
PLL0	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6, HSDIV7, HSDIV8, HSDIV9		See (1), (2), and (3)
PLL1	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6		See (1), (2), and (3)
PLL2	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6, HSDIV7, HSDIV8, HSDIV9		See (1), (2), and (3)
PLL5	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2	MAIN_PLL5_REF_CLK	(1), (2), and (3)
PLL7	PLLTS16FFCLAFRACF2	HSDIV0	MAIN_PLL7_REF_CLK	(1), (2), and (3)
PLL8	PLLTS16FFCLAFRACF2	HSDIV0		See (1), (2), and (3)
PLL12	PLLTS16FFCLAFRACF2	HSDIV0		See (1), (2), and (3)
PLL15	PLLTS16FFCLAFRACF2	HSDIV0, HSDIV1, HSDIV2		See (1), (2), and (3)
PLL17	PLLTS16FFCLAFRACF2	HSDIV0		See (1), (2), and (3)

---

(1) See Figure 6-41, *Generic PLL Functional Diagram for PLLTS16FFCLAFRACF2 type* for overview of the PLL.
(2) See Section 6.4.5.5.1 for synthesized clock parameters.
(3) See Section 6.4.5.5.2 for clock output parameters.

6.4.5.5.1 Clock Synthesis Inputs to the PLLs

Table 6-33 lists the clock synthesis parameters for PLLTS16FFCLAFRACF2 type.

Table 6-33. Clock synthesis Parameters for PLLTS16FFCLAFRACF2 Type

Parameter Name	Register
FB_DIV	<PLL_name>_FREQ_CTRL0[11-0] FB_DIV_INT (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL0[11-0] FB_DIV_INT)
FB_DIV_FRAC	<PLL_name>_FREQ_CTRL1[23-0] FB_DIV_FRAC (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL1[23-0] FB_DIV_FRAC)
POST_DIV2	<PLL_name>_DIV_CTRL[26-24] POST_DIV2 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[26-24] POST_DIV2)
POST_DIV1	<PLL_name>_DIV_CTRL[18-16] POST_DIV1 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[18-16] POST_DIV1)
REF_DIV	<PLL_name>_DIV_CTRL[5-0] REF_DIV (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[5-0] REF_DIV)

Note

For PLLTS16FFCLAFRACF2 type - POST_DIV1 and POST_DIV2 values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2.

6.4.5.5.2 Clock Output Parameter

Table 6-34 lists the control/status bit fields for output clocks.

Table 6-34. Clock Output Parameter for PLLTS16FFCLAFRACF2 Type

Clock Output/Divider	Parameter Name	Control/Status Bit Field
<PLL_name>_CLKOUT, <PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_CTRL[31] BYPASS_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[31] BYPASS_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_HSDIV_CTRLj[15] CLKOUT_EN (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[15] CLKOUT_EN and MCU_PLL0_HSDIV_CTRL1[15] CLKOUT_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Divider control	<PLL_name>_HSDIV_CTRLj[6-0] HSDIV (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[6-0] HSDIV and MCU_PLL0_HSDIV_CTRL1[6-0] HSDIV)
PLL bypass mux	Control	<PLL_name>_CTRL[16] BYP_ON_LOCKLOSS (For example, MCU_PLL0 - MCU_PLL0_CTRL[16] BYP_ON_LOCKLOSS)
Enable 4-phase clock generator	Control	<PLL_name>_CTRL[5] CLK_4PH_EN (ignored if <PLL_name>_CTRL[4] CLK_POSTDIV_EN = 0) (For example, MCU_PLL0 - MCU_PLL0_CTRL[5] CLK_4PH_EN)
Post divide CLK enable	Control	<PLL_name>_CTRL[4] CLK_POSTDIV_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[4] CLK_POSTDIV_EN)
Delta-Sigma modulator enable	Control	<PLL_name>_CTRL[1] DSM_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[1] DSM_EN)

Table 6-34. Clock Output Parameter for PLLTS16FFCLAFRACF2 Type (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
Enable fractional noise canceling DAC	Control	<PLL_name>_CTRL[0] DAC_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[0] DAC_EN)

(1) j is the number of HSDIV for the current PLL.

6.4.5.5.3 Calibration Related Bitfields

Table 6-35 lists the calibration related bitfields/bits.

Table 6-35. Recalibration Feature Parameters

Recalibration feture	Parameter Name	Control/Status Bit Field
Calibration enable to actively adjust for input skew	Control	<PLL_name>_CAL_CTRL[31] CAL_EN (For example, PLL12 - PLL12_CAL_CTRL[31] CAL_EN)
Fast calibration enabled	Control	<PLL_name>_CAL_CTRL[20] FAST_CAL (For example, PLL12 - PLL12_CAL_CTRL[20] FAST_CAL)
Calibration loop programmable counter	Control	<PLL_name>_CAL_CTRL[18-16] CAL_CNT (For example, PLL12 - PLL12_CAL_CTRL[18-16] CAL_CNT)
Calibration bypass	Control	<PLL_name>_CAL_CTRL[15] CAL_BYP (For example, PLL12 - PLL12_CAL_CTRL[15] CAL_BYP)
Calibration input	Control	<PLL_name>_CAL_CTRL[11-0] CAL_IN (For example, PLL12 - PLL12_CAL_CTRL[11-0] CAL_IN)
Output of the calibration block	Status	<PLL_name>_CAL_STAT[11-0] CAL_OUT (For example, PLL12 - PLL12_CAL_STAT[11-0] CAL_OUT)

6.4.5.6 PLL Controller (PLLCTRL)

The PLLCTRL manages clock alignment of CBASS clocks to the peripherals in Main and MCU domains. In addition PLLCTRL is also responsible for controlling reset propagation through the chip and providing DFT hooks for testability. Two PLL Controllers are implemented in the device - PLLCTRL0 and MCU_PLLCTRL0. They are respectively related to PLL0 and MCU_PLL0.

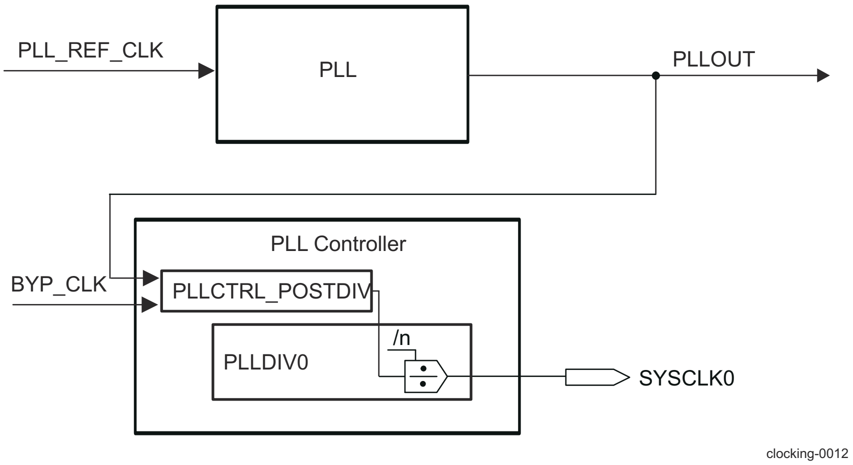

Figure 6-43. PLL Controller

Note

PLLCTRL_POSTDIV is not supported in this family of devices.

Note

The PLL Controllers registers can be accessed by any controller in the device.

A SYSCLK0 clock out of a PLLCTRL is the only synchronous clock in that domain. That means - MCU_SYSCLK0 out of MCU_PLLCTRL is the synchronous CBASS clock in MCU domain and SYSCLK0 out of Main PLLCTRL is the synchronous CBASS clock in Main domain.

6.4.5.7 PLL, PLLCTRL, and HSDIV Controllers Programming Guide

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

6.4.5.7.1 PLL Initialization

6.4.5.7.1.1 Kick Protection Mechanism

Note

PLL configuration registers are write-protected at power-up. Software must first un-lock the PLLn_LOCKKEY0 and PLLn_LOCKKEY1 registers prior to writing to any chip-level registers.

The un-lock process shall follow the steps:

1. Write value 0x68EF3490 to PLLn_LOCKKEY0 register.
2. Write value 0xD172BC5A to PLLn_LOCKKEY1 register.

After these two steps a write access to the PLL registers is allowed. Writing any other data value to either of these two registers locks the kicker mechanism and blocks any writes to the PLL registers.

Note

In order to ensure that all PLL registers are write protected, software must always re-lock the kicker mechanism after completing the register writes.

6.4.5.7.1.2 PLLCTRL Initialization

Note

For validated set of parameters that can be programmed to PLLs, please refer to the device-specific Datasheet.

Initially, the device powers up in PLL bypass mode. The bypass mux is a glitch free mux and is located outside the PLL module. BYPASS_EN bit controls the bypass mux section. During Power-up, the bypass mux defaults to select FREF clock (PLL clock bypass mode).

The following shows the PLL initialization sequence.

1. Wait until supplies are stable and PORz is de-asserted. By this time the reference clock source must be up and running.

2. Default controls settings:
    - By default PLL_EN signal is Low provided by <PLL_name>_CTRL register default state. This signal behaves like a reset control to the PLL.
    - By default INTL_BYP_EN signal is low provided by <PLL_name>_CTRL register default state.
    - By default BYPASS_EN signal is high provided by PLL MMR CTRL default state. PLL clock will be bypassed externally by a glitch free mux. The output of the mux will be the reference clock FREF.
    - LOCK output of PLL will be Low.
3. Program the PLL to a valid setting that runs the VCO within the specified range. The following bits/bitfields must be programmed appropriately by software: DSM_EN, DAC_EN, CLK_POSTDIV_EN, CLK_4PH_EN, REF_DIV[5-0], FB_DIV[11-0], FB_DIV_FRAC[23-0], POST_DIV1[2-0], POST_DIV2[2-0].
4. Wait for 1 µs to allow the PLL internal reset to complete (PLL powerdown switch pulls the loop filter voltage from rail-to-rail, which ensures the PLL will be completely powered down from any state).
5. Assert PLL_EN to a High (by writing a '1' into PLL_EN bit in <PLL_name>_CTRL register).
6. Wait for PLL Lock output to go high. Software can read the LOCK bit in <PLL_name>_STATS register to check if PLL has locked.
7. De-assert BYPASS_EN signal to a Low by writing 0 into BYPASS_EN bit in <PLL_name>_CTRL register.
8. Glitch free mux safely switches to the PLL clock output.

Note

In the case of brown out (supply dips below datasheet minimum) or loss of the reference clock, the state of the PLL will be undetermined. A full reset sequence should be initiated.

Changing PLL setting: During normal operation, before changing PLL settings, the PLL clock must be bypassed by setting BYPASS_EN control to a high. Then follow steps 2 to 8 from the above sequence.

6.4.5.7.1.3 PLL Programming Requirements

- A PLL VCO frequency must be set to > 1500 MHz
    - For best PLL performance, maximize VCO frequency where possible.
- A PLL must always operate in Fractional Mode (DAC_EN and DSM_EN set to ‘1’). This is true even when the FB_DIV is a integer.
- A PLL Reference clock frequency must be > 10 MHz.
- REF_DIV[5:0] must be set to “000001”.
- Calibration procedures for FRACF PLLs in integer mode or fractional mode:
    - **Programming FRACF in Integer Mode with calibration (Static or Auto Calibration)**
        - Set all the common PLL settings (PREDIV, FBDIV, …)
        - DACEN: 0
        - DSMEN = 0 (INT MODE)
        - FASTCAL=1
        - CALBYPASS=0
        - CALCNT[2:0]=2
        - CALIN[11:0]=0
        - CAL_EN=1
        - SET PLL_EN = 1
        - WAIT FOR PLL_LOCK AND CAL_LOCK GO HI
        - CAPTURE AND STORE CALCODE WHEN CAL_LOCK GOES HI IF IT WILL BE USED LATER
        - IF CAL_LOCK times out (> 2 ms) then continue
        - CAL_EN=0 (OPTIONAL, THIS WILL FREEZE CALIBRATION & INTERNAL CALCODE)
    - **Programming FRACF in Fractional Mode (with Static Calcode)**
        - Set all common PLL settings to nearest integer (PREDIV, FBDIV,...)
        - Run calibration as outlined in integer mode
        - CAPTURE AND STORE CALCODE WHEN CAL_LOCK GOES HI IF IT WILL BE USED LATER
        - IF CAL_LOCK times out (> 2 ms) then continue
        - CAL_EN=0 (THIS WILL FREEZE CALIBRATION & INTERNAL CALCODE)

        - IF CAL_LOCK timed out, keep CALBYPASS=0
        - IF CAL_LOCK IS ASSERTED AND CALCODE IS CAPTURED APPLY CALCODE TO CALIN
        - CALBYPASS=1 CALCODE IS SET BY CALIN
        - ENABLE FRACTIONAL MODE
    - **Programming FRACF in Fractional Mode (Auto-Calibration Not Allowed)**
        - Set all the common PLL settings (PREDIV, FBDIV, …)
        - DACEN=1
        - DSMEN=1 (FRAC MODE)
        - FASTCAL =X
        - CALBYPASS=1 CALCODE IS SET BY CALIN
        - CALCNT[2:0]=XX
        - CALIN[11:0] = 0 (OR DESIRED CALCODE)
        - CAL_EN = 0
        - SET PLL_EN = 1
        - WAIT FOR PLL_LOCK

PLL Integer mode with Calibration enabled is recommended for applications sensitive to phase noise or jitter: Examples include Refclk for SerDes, PHY, DDR etc. See individual product datasheets for specific SoC requirements. Calibration can be bypassed for digital clocks like ARM. If Calibration is bypassed, CALIN needs to be set to 0.

When Calibration is enabled, PLL Lock time will be longer since SOC needs to wait for CAL_LOCK. Applications sensitive to phase noise must wait for CAL_LOCK to go high.

6.4.5.7.2 HSDIV PLL Programming

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 0 cleanly disables the HSDIV output clock

<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV = <value> for divider

<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0 insures that the divider changes occur synchronously to the internal divider of the HSDIV block.

when the clock is required,

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1 cleanly enables the HSDIV output clock

6.4.5.7.3 PLL Controllers Programming - Dividers PLLDIVn and GO Operation

The GO operation is required to change the divider ratios of the PLLDIVn registers. Section 6.4.5.7.3.1 , *GO Operation*, discusses the GO operation. Section 6.4.5.7.3.2 , *Software Steps to Modify PLLDIVn Ratios*, provides the software steps required to change the divider ratios.

6.4.5.7.3.1 GO Operation

The GO operation writes to the RATIO field in the PLLDIVn. Registers do not change the dividers' divide ratios immediately. The PLLDIV dividers change to the new RATIO rates only during a GO operation. This section discusses the GO operation and alignment of the SYSCLKs.

The PLL Controller clock align control register (ALNCTL) determines which SYSCLKs must be aligned. Before a GO operation, program ALNCTL so that the appropriate clocks are aligned during the GO operation.

A GO operation is initiated by setting the GOSET bit in PLLCMD to 1. During a GO operation:

- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL and SYS *n* bit in DCHANGE set to 1 is paused at the low edge. Then the PLL Controller restarts all these SYSCLKs simultaneously, aligned at the rising edge. When the SYSCLKs are restarted, SYSCLK *n* toggles at the rate programmed in the RATIO field in PLLDIVn.
- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL cleared and the SYS *n* bit in DCHANGE set immediately changes to the new rate programmed in the RATIO field.
- The GOSTAT bit in PLLSTAT is set throughout the duration of a GO operation.

CAUTION

To help prevent errors, all device operation must be stopped before the GO operation.

6.4.5.7.3.2 Software Steps to Modify PLLDIV Ratios

Perform the following steps to modify PLLDIV.

1. Check that the GOSTAT bit in PLLSTAT is cleared to show that no GO operation is currently in progress.
2. Program the RATIO field in PLLDIVn to the desired new divide-down rate. If the RATIO field changed, the PLL Controller will flag the change in the corresponding bit of DCHANGE.
3. Set the respective ALN *n* bits in ALNCTL to align any SYSCLKs after the GO operation.
4. Set the GOSET bit in PLLCMD to initiate the GO operation to change the divide values and align the SYSCLKs as programmed.
5. Read the GOSTAT bit in PLLSTAT to make sure the bit returns to 0 to indicate that the GO operation has completed.

6.4.5.7.4 Entire Sequence for Programming PLLCTRL, HSDIV, and PLL

Table 6-36 shows the entire sequence of programming PLLCTRL, HSDIV, and PLL from an unknown state to a defined non-spread-spectrum state.

Table 6-36. Programming Sequence of PLLCTRL, HSDIV, and PLL

Step	Description
Unlock PLL registers	<PLL_Name>_LOCKKEY0 (= 0x68EF3490)
	<PLL_Name>_LOCKKEY1 (= 0xD172BC5A)
If PLL0	Configure PLLCTRL block into bypass mode
	PLLCTL[0]PLLEN = 0
	PLLCTL[5] PLLENSRC = 0
Configure external bypass so that no transient clock propagates	<PLL_Name>_CTRL[31] BYPASS_EN = 1
Delay	
Disable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN =0
Delay	
Disable PLL	<PLL_Name>_CTRL[15] PLL_EN =0
Delay	
Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 1
If PLL0	Check PLLSTAT[0] GOSTAT to make sure that divider change is not currently in-progress GOSTAT should equal 0.
	Clear GOSET bit PLLCMD[0] GOSET = 0
	Configure divider in PLLCTRL to /1 PLLDIV1 = 0x8000 (enable divider and divide by 1) PLLDIV2 = 0x00 (disable divider and divide by 1)
	Set alignment control bits ALNCTL = 3
	Set GOSET bit to initiate the divider change PLLCMD[0] GOSET = 1
	Check PLLSTAT[0] GOSTAT to make sure that divider change has completed GOSTAT should equal 0.
Configure HSDIV(s) divider value	<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV (=val)
Clear HSDIV(s) SYNC_DIS	<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0
Delay	

Table 6-36. Programming Sequence of PLLCTRL, HSDIV, and PLL (continued)

Step	Description
Clear Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 0
Configure PLL multiplier	Integer portion of divider <PLL_Name>_FREQ_CTRL0[11-0] (=val) Fractional portion of divider <PLL_Name>_FREQ_CTRL1[23-0] (=val)
Configure PLL dividers	Reference clock divider <PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	Post divider 1 <PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1
	Post divider 2 <PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
Configure “random” PLL controls	<PLL_Name>_CTRL[8] INTL_BYP_EN = 0
	<PLL_Name>_CTRL[5] CLK_4PH_EN = 0
	<PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
	<PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1
	<PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	<PLL_Name>_CTRL[1] DSM_EN = 1
	<PLL_Name>_CTRL[0] DAC_EN = 1
	<PLL_Name>_CTRL[4] CLK_POSTDIV_EN – if PLL has more than 5 HSDIV blocks, 1; else 0.
	<PLL_Name>_CTRL[16] BYP_ON_LOCKLOSS (= {0, 1})
Delay	
Enable PLL	<PLL_Name>_CTRL[15] PLL_EN = 1
Wait for Lock	Wait for MCU_PLL0_STAT[0] LOCK = 1
Enable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1
Delay	
Configure external bypass to pass PLL	<PLL_Name>_CTRL[31] BYPASS_EN = 0
Delay	
If PLL0	Configure PLLCTRL block into PLL mode PLLCTL[0] PLLEN = 0
Lock PLL registers	<PLL_Name>_LOCKKEY0 (= any value)
	<PLL_Name>_LOCKKEY1 (= any value)

6.4.5.7.5 Dual Clock Comparator (DCC)

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference. Internal 12.5 MHz RC oscillator clock is used to validate HFOSC0_CLKOUT. Then HFOSC0_CLKOUT (most accurate clock) is used to validate/track all other clocks in the device. An additional use of this module is to measure the frequency of a selectable clock source, using an external input clock source of known frequency (MCU_EXT_REFCLK0, EXT_REFCLK1 pins). There is one instance of DCC module in MCU domain and seven instances of DCC modules in Main domain to monitor critical clocks. Refer to DCC chapter for details.

6.4.5.7.6 DeepSleep Clock Gating

This device supports deepsleep mode where the HFOSC0_CLK is synchronously gated during deep-sleep entry sequence. HFOSC0 Clock loss detection mux control must be disabled during Deepsleep entry mode. (CLKLOSS_SWITCH_EN must be ‘0’).

In addition, HFOSC0 can be put into Power-down mode. When exiting deep-sleep mode, HFOSC0 is powered-up, wait until clock is stabilized and disable the clock gating so clock can propagate to PLL and Wake-up domain. This function is handled by Deep-sleep Hardware logic in Wake-up Domain.

6.4.5.7.6.1 Software responsibility of clock settings during deeplseep mode

- Before going into deepsleep mode, software must ensure to configure the clock mux controls of modules in MCU domain such that when it resumes from sleep mode these modules will have a functional clock when MCU domain reset is de-asserted. Examples of such modules are: TIMER, WDT/RTI, SPI, MCAN and UART. This is a very important requirement to ensure a proper reset of MCU domain modules coming out of deeplseep mode.
- For modules in Wake-up domain, during deepsleep resume, DM/Pulsar must ensure to first enable the functional clocks before accessing the modules in wake-up domain. This requirement is also applicable during normal mode of operation.

Chapter 7

Processors and Accelerators

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7.1 Arm® Cortex®-A53 Subsystem (A53SS)

This section describes the Arm® Cortex®-A53 Subsystem (A53SS) in the device.

7.1.1 A53SS Overview

7.1.1.1 A53SS Introduction

The SoC implements one cluster of quad-core Arm® Cortex® A53 MPCore™, with 32KB L1 instruction, 32KB L1 data, per core and 512KB L2 shared cache.

The Cortex®-A53 cores are general-purpose processors that can be used for running customer applications.

Note

Notes on references used in this document:

- A53SS is also referred to as Arm® CorePac.
- Cortex®-A53 is often shortened to A53.

The A53SS is built around the Cortex®-A53 MPCore™ (Arm® A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is an in-order, 8-stage, dual-issue pipeline with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

The Arm®v8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers. The A53 processor is Arm's first Arm®v8-A processor aimed at providing power-efficient 64-bit processing. It features an in-order, 8-stage, dual-issue pipeline, and improved integer, Arm® Neon™, Floating-Point Unit (FPU) and memory performance.

The A53 CPU supports two execution states: AArch32 and AArch64. The AArch64 state gives the A53 CPU its ability to execute 64-bit applications, while the AArch32 state allows the processor to execute existing Arm®v7-A applications.

7.1.1.2 A53SS Features

The A53SS module supports the following features:

- Quad Core A53 Cluster
  - Full Arm®v8-A Architecture Compliant
    - AArch32 and AArch64 Execution States
    - All exception levels EL0-3
    - A32 Instruction Set (Previously Arm instruction set)
    - T32 instruction set (Previously Thumb instruction set)
    - A64 Instruction Set
  - Data Coherency within Cluster (L1/L2 caches)
  - Advanced SIMD and Floating Point Extensions (Arm® Neon™)
  - Arm®v8 Cryptography Extensions
  - Arm GICv3 architecture
  - In-order pipeline with symmetric dual-issue of most instructions
  - Harvard L1 with system MMU
    - 32 KB Instruction Cache
    - 32 KB Data Cache
  - 512KB Shared L2 Cache
  - Generic Timer(s)
  - Debug
- 128-Bit VBUSM Initiator Interfaces (for axi_r and axi_r channels)
- 128-Bit VBUSM Target Interface (for Accelerator Coherency Port)
- 64-bit Grey-coded system input time
- 48-bit Grey-coded debug input time
- 48-bit Grey-coded debug input time

- Integrated PBIST controller with BISOR

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

7.1.2 A53SS Functional Description

7.1.2.1 A53SS Block Diagram

7.1.2.2 Arm Cortex-A53 Cluster

The Arm Cortex-A53 Cluster is provided by Arm and configured by TI. Table 7-1 summarizes the configuration of the Arm Cortex-A53 Cluster on this SoC.

Table 7-1. Arm A53 Cluster Configuration

Parameter	Value
Core Type	A53
Core Revision	r0p4
Number of Cores	4
Bus Width	256
L1 Instruction Cache Size	32K
L1 Data Cache Size	32K
L2 Cache Size	512K
SCU-L2 Cache Protection	Included
Advanced SIMD and Floating Point Extension	Included
Cryptography Extension	Included
CPU Cache Protection	Included
AMBA5 CHI or AMBA4 ACE Interface	AMBA4 ACE (configured for AXI using tie-offs)
Accelerator Coherency Port (ACP)	Included
V7 or v8 Debug Memory Map	v8

Note

For a brief list of features supported by the Arm Cortex-A53 Cluster, see A53SS Features.

For detailed description of the Arm® A53 Cluster, see the *Arm®Cortex®-A53 MPCore™ Processor Technical Reference Manual*.

7.1.2.3 A53SS Interfaces and Async Bridges

The A53SS has the following main interfaces:

- 64-bit graycoded system input time
  - Graycode value provided by Global Timebase Counter (GTC)
  - Dedicated decoder (64-bit input) for graycode-to-binary conversion
- 48-bit graycoded debug input time
  - Graycode value provided by GTC
  - Dedicated decoder (48-bit input) for graycode-to-binary conversion
- 32-bit VBUSP target interface for debug
  - Supported by VBUSP2APB Bridge, which performs VBUSP-to-APB conversion (for controlling the Arm A53 Cluster internal debug logic)
- 32-bit ATB output port for debug/trace
  - Supported by ATB Bridge, which performs clock and voltage level conversion on the combined ATB interface
  - Connected to the Debug Subsystem
- Cross Trigger Interface (CTI) for debug
  - Connected to the Debug Subsystem
- Interface(s) with Arm GIC-500 Interrupt Controller

  - Supported by GIC AXI Streaming Bridge, which performs clock and voltage level conversion on the AXI streaming protocol
  - Interrupts (PPIs) from Arm A53 Cluster to GIC-500
  - Interrupts (IRQ, FIQ, VIRQ, VFIQ) from GIC-500 to Arm A53 Cluster
- Power/clock interface(s)
  - Dedicated PLL for each Arm A53 Cluster
  - Dedicated LPSC for each Arm A53 Cluster, and also for each A53 core

7.1.2.4 A53SS Interrupts

7.1.2.4.1 A53SS Interrupt Inputs

The A53 CPU recieves interrupts at its inputs (IRQ, FIQ, VIRQ, VFIQ) via the dedicated Arm GIC-500 Interrupt Controller, which resides at the SoC level (MAIN Domain) and is integrated inside the GIC0 Subsystem. The GIC-500 supports all four A53 cores in the system.

The GIC-500 is compliant to the Arm GICv3 standard and supports four types of interrupts:

- *Software Generated Interrupts (SGI)*
  - There are 16 SGIs (ID0-ID15)
  - These are inter-processor interrupts
- *Private Peripheral Interrupts (PPI)*
  - There are 16 PPIs (ID16-ID31)
  - These are wired interrupts dedicated to a specific CPU
  - Many are reserved to specific functions via convention
- *Shared Peripheral Interrupts (SPIs)*
  - There are 256 SPIs (ID32-ID288)
  - These are wired interrupts that can be routed to any core or cluster, based on the programming of that interrupt in the GIC500
- *Locality-Specific Peripheral Interrupts (LPI)*
  - There are 57,344 LPIs
  - These interrupts are used for message-based interrupts from a peripheral

The mapping of PPIs and SPIs to the GIC-500 interrupt inputs can be found in *Interrupts*.

Note

For a brief list of features supported by the GIC-500 module, see the *Interrupts* chapter.

For detailed description of the GIC-500 module, see the *Arm®CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

7.1.2.4.2 A53SS Interrupt Outputs

A53SS Interrupt Outputs lists the interrupts generated by the A53SS.

Table 7-2. A53SS Interrupt Outputs

Interrupt Name (TI)(1)	Interrupt Name (Arm)	Interrupt Description
A53 Core Interrupts (PPIs)(2)		
A53_COREy_VCPUMNTIRQ	VCPUMNTIRQn	This interrupt indicates that a Virtual CPU Interface on the corresponding core needs serviced. This interrupt is serviced by software switching to the virtual CPU and finding what specific service needs done.
A53_COREy_CNTHPIRQ	CNTHPIRQn	This interrupt indicates a physical timer event at the EL2 (Hypervisor) exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL2 and service accordingly.

Table 7-2. A53SS Interrupt Outputs (continued)

Interrupt Name (TI)(1)	Interrupt Name (Arm)	Interrupt Description
A53_COREy_CNTPNSIRQ	CNTPNSIRQn	This interrupt indicates a physical timer event at the EL1 Non-Secure exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL1 Non-Secure and service accordingly.
A53_COREy_CNTPSIRQ	CNTPSIRQn	This interrupt indicates a physical timer event at the EL1 Secure exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL1 Secure and service accordingly.
A53_COREy_CNTVIRQ	CNTVIRQn	This interrupt indicates a Virtual timer event. Service of this interrupt is dependent on what the timer was set for. Software should take exception and service accordingly.
A53_COREy_PMUIRQ	PMUIRQn	This interrupt is generated by the Performance Monitor Unit (PMU). The PMU can generate an interrupt based on several conditions, depending on programming. Software should take exception and query the PMU as to the cause of the interrupt, and act accordingly.
A53_COREy_DCCIRQ	COMMIRQn	Communications Channel receive or transmit interrupt
A53_COREy_CTIIRQ	CTIIRQn	Cross Trigger Interface interrupt

(1) In this column, *y* is the A53 Core index (0 or 1)

(2) These are 'per core' interrupts

Note

The mapping of these interrupts in the system is summarized in *A53SS Integration*, and can also be found in *Interrupts*.

For more detailed description of these interrupts and their handling, see the *Arm®Cortex®-A53 MPCore™ Processor Technical Reference Manual*.

7.1.2.5 A53SS Power Management and Clocking

7.1.2.5.1 A53SS Power Management

Each Arm A53 Cluster and each A53 CPU reside in a separate power domain, as follows:

There is a dedicated Local Power Sleep Controller (LPSC) for each Arm A53 Cluster, and for each A53 core, as well. The LPSC assignment is as follows:

For more details on these LPSCs, including power-up/down sequences, see *Power*.

7.1.2.5.2 A53SS Clocking

There is a dedicated PLL for each Arm A53 Cluster. The PLL assignment is as follows:

- PLL8 (ARM0 PLL): Dedicated for Arm A53 Cluster 0

For more details on these PLLs, see *Clocking*.

7.1.2.6 A53SS Debug

The A53SS supports the standard Arm debug architecture. Details on Arm debug can be found in the *On-chip Debug* chapter and the relevant Arm specifications.

7.1.2.7 A53SS Global and Debug Timestamps

The A53SS has two timebase input interfaces:

- 64-bit global timestamp: Used for synchronizing the Arm internal timers (via the ARM CNTVALUEB [63:0] bus)

- 48-bit debug timestamp: Can be embedded in Arm trace streams at periodic and strategic locations, allowing the temporal relationship of different trace sources to be determined

Both of them are fed by the Global Timebase Counter (GTC), which provides a 64-bit graycode value. The A53SS includes two graycode decoders (for global time and debug time, respectively), which take the asynchronous graycoded times, synchronize them to the appropriate clock, and convert them to binary time, as required by Arm.

Note

Both graycode decoders are 64-bit but the one dedicated to debug time has a 48-bit input (the upper 16 bits are tied to 0).

For more details on the GTC, see *Global Timebase Counter (GTC)*.

7.1.2.8 A53SS Watchdog

The A53SS does not have an integrated watchdog timer. Instead, this feature is provided externally by the Real Time Interrupt Module (RTI) module, which implements a windowed watchdog timer capable of issuing warm reset to the SoC, when necessary.

For more details on the RTI windowed watchdog feature, see *Real Time Interrupt Module (RTI/WWDT)*.

7.1.2.9 A53SS Functional Safety - ECC Error Injection Support

In the quad A53 CBA subsystem, there are five ECC aggregators – one for each core and one for the corepac level. Debug domain is not safety critical.

No CBASS/Bridge interconnect safety is supported. Only RAM safety is supported.

The following A53SS ECC Aggregator instances are instantiated:

- A53SS0_ECC_AGGR0: ECC Aggregator for Arm A53 Cluster 0, Core 0
- A53SS0_ECC_AGGR1: ECC Aggregator for Arm A53 Cluster 0, Core 1
- A53SS0_ECC_AGGR2: ECC Aggregator for Arm A53 Cluster 0, Core 2
- A53SS0_ECC_AGGR3: ECC Aggregator for Arm A53 Cluster 0, Core 3
- A53SS0_ECC_AGGR_COREPAC: ECC Aggregator for Arm A53 Cluster 0

7.1.2.9.1 A53 ECC Aggregators During Low Power States

- When a cpu core is in WFI/WFE, the corresponding core ECC Aggregator MMR regions is not accessible and will return error status.
- Similarly when L2 is in WFI, the corepac ECC Aggregator MMR region is not accessible and will return error status.

7.1.2.9.2 Auto-initialization of Memories

All A53 L1 and L2 memory initialization is handled by the Arm core. The TI ECC aggregator is used in inject-only mode and this cannot be used for initialization. The Arm CPU will initialize the cache memories after reset.

There are no other memories in the A53 subsystem beside the cache memories

7.1.2.9.3 A53 SRAM Safety

The Arm A53 Cluster natively supports ECC/parity protection on A53 SRAMs and error injection on few memories. The A53SS adds error injection capability on all internal SRAM. This is a valuable TI addition to the Arm native implementation.

Table 7-3. A53 SRAM Safety Support

RAM	A53 Error Injection Support	TI Error Injection Support
L1 I-Cache Data	No	Single error injection
L1 I-Cache Tag	No	Single error injection
L1 D-Cache Data	Double error injection	Single and double error injection

Table 7-3. A53 SRAM Safety Support (continued)

RAM	A53 Error Injection Support	TI Error Injection Support
L1 D-Cache Tag	No	Single error injection
L1 Data Dirty	No	Single error injection
TLB RAM	No	Single error injection
SCU Duplicate Tag	No	Single and double error injection
L2 Tag RAM	Double error injection	Single and double error injection
L2 Data RAM	Double error injection	Single and double error injection

The ECC Aggregator for the cores stimulates errors in the following RAMs:

- L1 I-Cache Data RAM
- L1 I-Cache Tag RAM
- L1 D-Cache Data RAM
- L1 D-Cache Tag RAM
- L1 D-Cache Dirty RAM
- TLB RAM
- L1 SCU L1-D Duplicate Tag RAM

The ECC Aggregator for the L2 cache stimulates errors in the following RAMs:

- L2 Data RAM
- L2 Tag RAM

7.1.2.9.4 A53 SRAM ECC Aggregator Configurations

There are several schemas of memory protection employed inside of the processors. The tables below describe the schema and arrangement. This describes what bits are protected, how they are protected, the behavior when an error is detected and what bits can be disturbed for ECC testing purposes. This also lists the RAMID associated with each memory to the corresponding ECC Aggregator.

The key for the protection schemes is as follows:

- Parity – Parity Bit(s) to protect data
- ECC – Error Correction Code to protect Data
- SED – Single Error Detection
- SECDED – Single Error Correction, Double Error Detection
- SEDSEC – Single Error Detection, Single Error Correction

Table 7-4. CPU Memories Safety Details

Memory	Protection	RAM Arrangement	CPU (Core ECC Aggr) Rams Ram ID	Notes
L1 I-Cache Data	Parity SED	41 – Parity for 40:21 40:21 – Instruction 20 – Parity for 19:0 19:0 – Instruction	0-3	Error detection results in both lines being invalidated then refetched from L2 or memory
L1 I-Cache Tag	Parity SED	31 – Parity for 30:0 30:0 – Data	4-5	Error detection results in both lines being invalidated, then line refetched from L2 or memory
L1 D-cache Data	ECC SECDED	38:32 – ECC 31:0 – Data	6-13	Error results in line being cleaned and invalidated from L1 with single bit errors corrected as part of eviction. Line refetched from L2 or memory
L1 D-Cache Tag	Parity SED	30 – Parity for 29:0	14-17	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Error results in line cleaned

Table 7-4. CPU Memories Safety Details (continued)

Memory	Protection	RAM Arrangement	CPU (Core ECC Aggr) Rams Ram ID	Notes
		29:0 – Tag		and invalidated from L1. SCU duplicate tags are used to get the correct address. Line refetched from L2 or memory
L1 D-cache Dirty	Parity SEDSEC	11:10 – Way 1/3 Dirty copy 2 and 1. Parity for 4 9:8 – Way 0/2 Dirty copy 2 and 1. Parity for 0 7 – Way 1/3 Outer Allocation Hint 6 – Way 1/3 Age 5:4 – Way 1/3 Partial MOESI 3 – Way 0/2 Outer Allocation Hint 2 – Way 0/2 Age 1:0 – Way 0/2 Partial MOESI	18	Error results in line cleaned and invalidated from L1 with single bit errors corrected as part of the eviction. Only dirty bit is protected. Other bits are just performance hints
TLB	Parity SED	116 – parity for 113:62 115 – Parity for 61:31 114 – Parity for 30:0 113:62 – Page Attributes 61:31 – Entry Identifiers 30:0 – Address	19-22	Error detection results in entry invalidated, new pagewalk to refetch.
SCU L1 Duplicate Tag	ECC SECDED	37:31 - ECC for 30:0 30:0 - Duplicate Tag	23-26 (accessed by each Core's ecc_aggr)	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Corretable Error – Tag rewritten with correct value, access retried Uncorrectable Error – Tag is invalidated

Table 7-5. L2 Memories Safety Details

Memory	Protection	RAM Arrangement	RAM_ID (L2 Cache RAMs)	Notes
L2 Tag	ECC SECDED	37:31 – ECC for 30:0 30:0 - Tag	0-15	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Corretable Error – Tag rewritten with correct value, access retried. Uncorrectable Error – Tag is invalidated
L2 Victim	None	–	–	Performance Hint Only – Error has no functional impact
L2 Data	ECC SECDED	71:64 – ECC for 63:0 63:0 – Data	16-23	Error results in Data corrected inline, access may stall for 1-2 cycles. After correction, line might be evicted
Branch Predictor	None	–	–	Performance Hint Only – Error has no functional impact

7.1.2.10 A53SS Boot

For A53SS boot sequence and any other A53SS boot details, see *Control Module (CTRL_MMR)*.

7.1.2.11 A53SS Interprocessor Communication

The Arm A53 core(s) can communicate with other device cores by supporting interrupt generation to and from these cores. The interprocessor communication (IPC) interrupts are assigned in the corresponding BOOTCFG0 memory-mapped registers (MMRs) called IPC_SETx / IPC_CLRx. For more information, see *Control Module (CTRL_MMR)*.

7.2 Cortex R5F Subsystem (R5FSS)

This chapter describes the Arm Cortex R5F real-time microcontroller unit subsystem (R5FSS) in the device.

7.2.1 R5FSS Overview

The R5FSS is a single-core implementation of the Arm® Cortex®-R5F processor that acts as the Device Manager responsible for boot, resource management, and power management functions. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm CoreSight™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

Note

The Cortex-R5F processor is a Cortex-R5 processor that includes the optional floating point unit (FPU) extension. In this TRM, all references to the Cortex-R5 processor apply to the Cortex-R5F processor by default.

7.2.1.1 R5FSS Features

The R5FSS supports the following features:

- Single-core Arm Cortex-R5F
  - Core revision: r1p3
  - Armv7-R profile
  - L1 memory system
    - 32KB instruction cache
      - 4x8KB ways
      - SECDED ECC protected per 64 bits
    - 32KB data cache
      - 4x8KB ways
      - SECDED ECC protected per 32 bits
    - 64KB tightly-coupled memory (TCM)
      - SECDED ECC protected per 32 bits
      - TCM hard error cache Implemented in CPU
      - Readable/writable from system
      - TCMs initialized (to 0's) at reset
      - Split into A and B banks (with B further splitting into B0 and B1 interleaved banks)
        - 32KB TCMA (ATCM)
        - 16KB TCMB0 (B0TCM)
        - 16KB TCMB1 (B1TCM)
  - Low interrupt latency with restartable instructions
  - Non-maskable interrupt (NMI)
  - Full-precision floating point (VFPv3)
  - 16 region memory protection unit (MPU)
  - 8 breakpoints
  - 8 watchpoints
  - Dynamic branch prediction with global history buffer and 4-entry return stack
  - CoreSight debug access port (DAP)
  - CoreSight embedded trace macrocell (ETM-R5) interface
  - Performance monitoring unit (PMU)
- Interfaces
  - 64-bit VBUSM initiator pair (1 read, 1 write) for L3 memory accesses

  - 64-bit VBUSM target for TCM access
    - Also allows access to cache for debug purposes
  - 32-bit VBUSP initiator for peripheral access
  - 32-bit VBUSP target configuration port
  - 32-bit VBUSP target debug port
    - Allows access to all R5FSS internal debug logic
- Synchronous clock domain crossing on all interfaces
  - Interfaces can run at an integer multiple of the core frequency
- 32-bit to 36-bit region-based address translation (RAT) on memory access initiators
  - 4 regions
    - Base address + size
    - Must be size aligned
- Integrated vectored interrupt manager (VIM)
  - 256 interrupts
    - Each interrupt programmable as either IRQ or FIQ
    - Each interrupt has a programmable enable mask
    - Each interrupt has a programmable 4-bit priority
  - Priority interrupt supported
  - Vectored interrupt interface
    - Compatible with R5F VIC port
    - Programmable 32-bit vector address per interrupt
      - Address is SECDED error protected
      - Default vector addresses provided on DED
    - Software interrupt generation
- Integrated ECC aggregators
  - Support for error injection to all supported ECC memory blocks to test ECC functionality (add-on function from TI)
  - One ECC aggregator to cover all RAMs and caches
- Standard Arm CoreSight debug and trace architecture at the R5FSS level
  - Cross triggering: Supported by cross trigger interface (CTI) (per CPU) and cross trigger matrix (CTM) components
  - Processor trace: Supported by embedded trace macrocell (ETM) (per CPU) and advanced trace bus (ATB) funnel components
- Boot
  - From ROM only

See Section 7.2.2 for a functional block diagram and more details on the R5FSS.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

7.2.2 R5FSS Functional Description

7.2.2.1 R5FSS Block Diagram

Figure 7-2 shows the R5FSS block diagram.

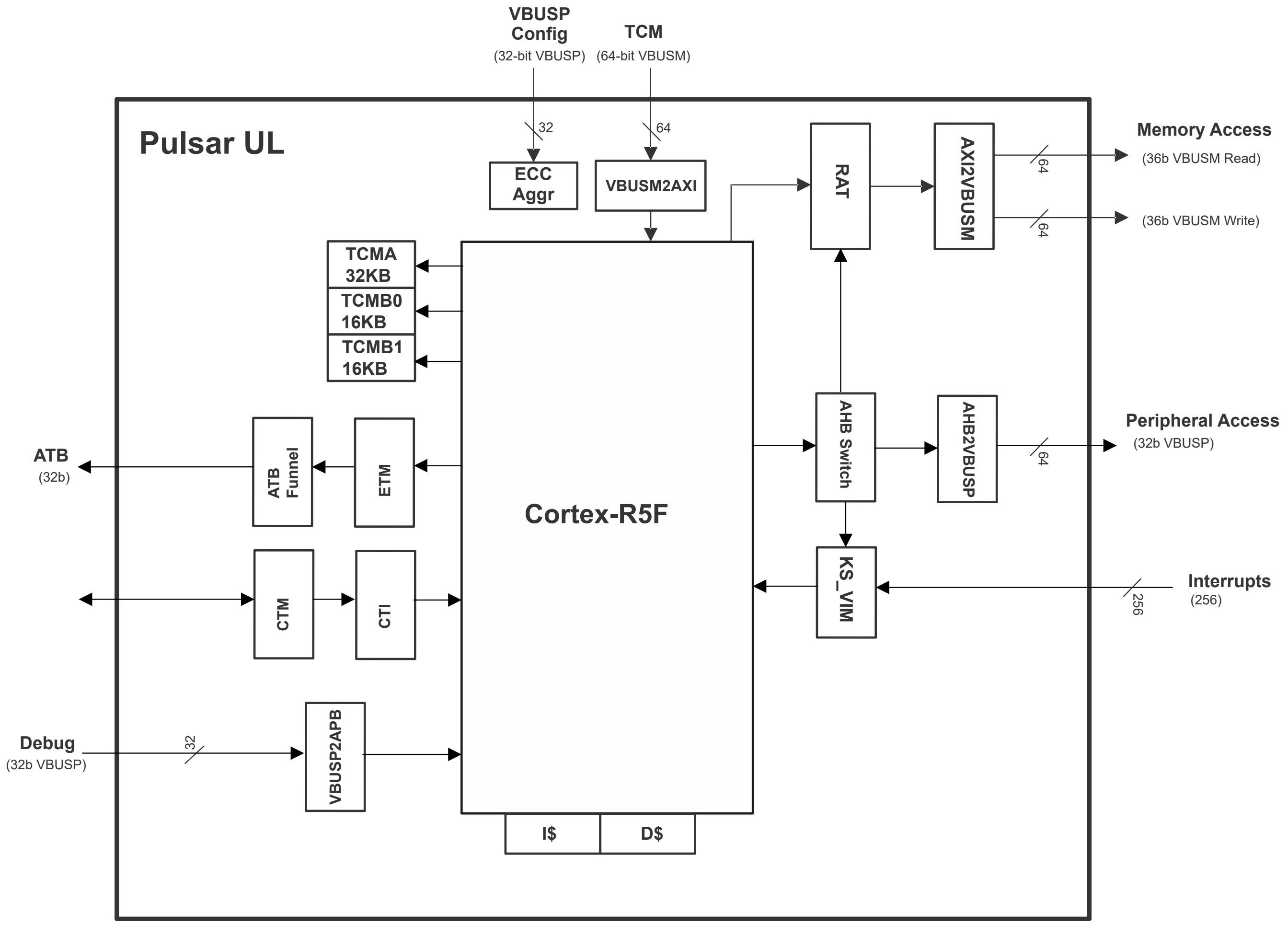

Figure 7-2. R5FSS Block Diagram

7.2.2.2 R5FSS Cortex-R5F Core

The Cortex-R5F is a processor from Arm, which is based on the Armv7-R profile.

For a brief list of features supported by the R5F processor in this device, see Section 7.2.1.1 . For more detailed description of this processor, see the *Arm Cortex-R5 Technical Reference Manual*.

7.2.2.2.1 L1 Caches

The R5F has a Harvard cache architecture, which means it has an independent L1 instruction cache (16KB) and L1 data cache (16KB). The instruction cache is protected by SECDED ECC per 64 bits. The data cache is protected by SECDED ECC per 32 bits.

7.2.2.2.2 Tightly-Coupled Memories (TCMs)

The R5F has two tightly-coupled memories (TCMs), ATCM and BTCM. The BTCM is further broken down into two interleaved banks, B0TCM and B1TCM.

TCMs are low-latency, tightly integrated memories for the R5F to use. Either TCM can be used for any combination of instruction and/or data. TCM performance is equal to performance on instructions/data that are in cache. However, TCMs have some additional advantages over cache. TCMs can be loaded with instructions that do not cache well (such as ISRs) or preloaded with code by an external source, before that code is needed, to save cache miss time. TCMs are also a good place for blocks of data for intense processing. They can be loaded (or pre-loaded by an external source) before the data is needed, saving cache miss time. The data can then be directly accessed by an external source, instead of needing to do cache evicts.

As mentioned, TCMs can be accessed (either read or written) by an external source over the TCM VBUSM target interface. This allows instructions or data to be preloaded, or for data to be read out after the R5F has processed it. The VBUSM target has a lower priority to accessing TCMs than the R5F but care must be taken to keep an external source from reading or writing TCM data that the R5F is working on. This handshaking is external to any of the R5FSS hardware.

TCMs are protected by ECC per 32 bits. For this to work, ECC must be enabled before data is written in to the TCMs (either externally or from the R5F). ECC is enabled via the following R5F system control bits: ACTLR.ATCMPCEN, ACTLR.B0TCMPCEN, and ACTLR.B1TCMPCEN, respectively.

Whether or not the TCMs are enabled is controlled by the ENABLE bit in the corresponding ATCM/BTCM region register. The default (reset) value of this bit is determined by the CPUn_INITRAMA and CPUn_INITRAMB bootstraps, respectively. Both ATCM and BTCM are configured for a size of 32KB in this device. Note that the BTCM size is the total of both B0TCM and B1TCM (16KB each).

If a TCM is not enabled, then it does not appear in the R5F's memory view, but it can be accessed by an external source. If a TCM is enabled, then its place in the R5F memory map is determined by a combination of bootstrap signal and system register. If the CPUn_LOCZRAMA bootstrap signal is high, then the initial base address of ATCM is 0x0000_0000 and the initial address of BTCM is 20'h41010. If the CPUn_LOCZRAMA bootstrap signal is low, then the initial base address of BTCM is 0x0000_0000 and the initial base address of ATCM is 20'h41010.

Note

This base address of 0x41010 for ATCM/BTCM based on the CPUn_LOCZRAMA bootstrap only affects the R5F's memory view. The SoC will see the ATCM/BTCM based on the TCM target interface regions, as defined in Section 7.2.2.3.2 . The base address of either TCM may be overwritten via the ATCM or BTCM region register. Care must be taken not to move the base address of a TCM when it may be being accessed.

It is possible to preload a TCM with instructions and boot from it. See Section 7.2.2.11 for details on TCM booting.

7.2.2.2.3 R5FSS Special Signals

Table 7-6 lists some R5FSS features associated with special signals.

Table 7-6. R5FSS Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 0 (ID = 0x0)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x2FFF_0000
CPUn RAT base address	0x2FFE_0000
CPUn RAT accesses ID	0x4 (CPU0)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state

Table 7-6. R5FSS Special Features (continued)

Feature	Comment
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_2000_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	64MB for MAIN peripherals (0x0_2000_0000 to 0x0_2FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Not used
CPUn VBUSM normal peripheral port size	Not used
CPUn VBUSM virtual peripheral port base address	Not used
CPUn VBUSM virtual peripheral port size	Not used
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

7.2.2.3 R5FSS Interfaces

7.2.2.3.1 Initiator Interfaces

The R5FSS has several initiator interfaces:

- 64-bit VBUSM initiator pair (1 read - "RMST", 1 write - "WMST") for L3 memory accesses; this is the main memory interface
  - Includes region-based address translation (RAT)
- 32-bit VBUSP initiator "PMST" for peripheral access
  - Includes logic that provides the R5F CPU with a private access to VIM and RAT
  - Enabled at reset

7.2.2.3.2 Target Interfaces

The R5FSS has several target interfaces that define its internal memory space:

- 32-bit VBUSP configuration target
  - Region [0]: ECC aggregator block
- 64-bit TCM target
  - Region [0]: ATCM
  - Region [1]: BTCM
  - Region [2]: Instruction cache RAMs
  - Region [3]: Data cache RAMs
- 32-bit VBUSP debug target
  - Provides access to all R5FSS internal debug logic

Regions [0] and [1] of the TCM target interface provide direct access to the TCM RAMs. Access to the RAMs is arbitrated with access from the R5F's L1 memory system. Excessive access while the R5F is also attempting access will degrade performance.

Regions [2] and [3] of the TCM target interface provide access to the cache RAMs for testing purposes. Access to the cache RAMs can only be done while the caches are disabled and should only be done for test purposes.

In addition to the target interfaces, there are peripherals (RAT and VIM) that are only accessible by the R5F. The R5F has an access to these modules via the VBUSP peripheral interface.

7.2.2.4 R5FSS Power, Clocking and Reset

7.2.2.4.1 R5FSS Power

The following R5FSS power considerations should be noted:

- R5FSS has a single power domain for all its internal logic

For more details on R5FSS power management, including power-up and power-down sequences, see *Power*.

7.2.2.4.2 R5FSS Clocking

The R5FSS has four clock inputs:

- CPU0_CLK: This is the clock for CPU0 logic
- CPU0_ICLK: This is the clock for CPU0 interfaces

CPU0_CLK is the clock for all of the internal CPU logic, while CPU0_ICLK is the clock for all of the interfaces for their associated CPU (for example: VBUSM and VBUSP bridges, exception generation, debug and trace logic).

The interface clock is an integer ratio of the CPU clock. The exact ratio for this device is 1:1.

7.2.2.4.3 R5FSS Reset

The R5FSS has two reset inputs:

- CPU0_RST: This is the reset for the non-debug logic of CPU0
- CPU0_DBG_RST: This resets the CPU0 debug logic, excluding the APB interface

In addition to the reset signals, there is one halt signal:

- CPU0_HALT

These halt signals keep the CPUs from fetching instructions when they come out of reset. The main use is to have the CPUs halted until the TCMs are loaded (when booting from TCM), though halt could be used for any other purpose.

7.2.2.5 R5FSS Vectored Interrupt Manager (VIM)

7.2.2.5.1 VIM Overview

The VIM aggregates device interrupts and sends them to the R5F CPU. It can be used in either split or single-core configuration.

The VIM module supports the following features:

- 256 interrupt inputs for the R5F core
- Each interrupt has its own 4-bit programmable priority
  - Defined via the R5FSS_VIM_PRI_INT_j register
  - The VIM provides support for priority interruption of interrupts
- Each interrupt has its own enable mask
  - Interrupt enable is done via the R5FSS_VIM_INTR_EN_SET_j register
  - Interrupt disable is done via the R5FSS_VIM_INTR_EN_CLR_j register
- Each interrupt can be programmed as either an IRQ or FIQ
  - Defined via the R5FSS_VIM_INTMAP_j register
- Each interrupt has its own programmable 32-bit vector address associated with it
  - Defined via the R5FSS_VIM_VEC_INT_j register
  - Protected with SECDED
- One IRQn and one FIQn output per core
- Vectored interrupt interface
  - Compatible with R5F VIC port
- Default vector provided when a double-bit error is detected

- Software interrupt generation

7.2.2.5.2 VIM Interrupt Inputs

The VIM supports 256 interrupt inputs per core. Each interrupt can be either a level or a pulse (both active-high). The interrupt mapping for the R5F core can be found in *Interrupt Sources*.

7.2.2.5.3 VIM Interrupt Outputs

The VIM has two interrupt outputs per core:

- *CoreN_IRQn*: This is a normal interrupt for core *N* (active-low level). It can be serviced via the VIC interface or through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (via the R5FSS_VIM_INTMAP_j register) and is enabled (via the R5FSS_VIM_INTR_EN_SET_j register), then it will cause an IRQ to assert
- *CoreN_FIQn*: This is a fast (or non-maskable) interrupt for core *N* (active-low level). FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ and is enabled, then it will cause an FIQ to assert

7.2.2.5.4 VIM Interrupt Vector Table (VIM RAM)

For each VIM interrupt core, there is an associated interrupt vector table (VIM RAM) that is used to store the address of ISRs. During register vectored interrupt and hardware vectored interrupt, VIM accesses the interrupt vector table using the vector value to fetch the address of the corresponding ISR. Note that both interrupt vector tables are identical in their memory organization.

The VIM RAM is basically comprised of a set of interrupt vector registers (R5FSS_VIM_VEC_INT_j). Hence, the interrupt vector table is organized in 256 words of 30 bits, with a base address corresponding to the physical address of the first register in the group.

Note

The lower two bits of the 32-bit interrupt vector are always 0s.

Figure 7-3 shows the VIM RAM interrupt vector map.

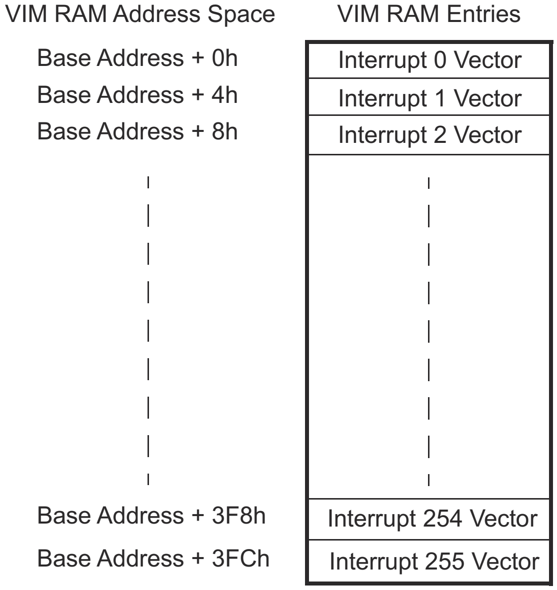

Figure 7-3. VIM RAM Interrupt Vector Map

The interrupt vector table has protection by ECC to indicate corruption due to soft errors. The ECC logic inside VIM supports SECDED. See Table 7-9 for the VIM RAM ID in the ECC aggregator map.

7.2.2.5.5 VIM Interrupt Prioritization

The VIM supports the interruption of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate but both use the same mechanism.

When an interrupt goes from pending to active (FIQ: reading the R5FSS_VIM_FIQVEC register; IRQ: reading the R5FSS_VIM_IRQVEC register, or the *coreN_IRQACK* going high), then the interrupt is loaded into the corresponding active register (R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ), and all interrupts of an equal or lesser priority are masked (discarded). If prior to this interrupt being cleared (by writing to the R5FSS_VIM_FIQVEC register, or R5FSS_VIM_IRQVEC register) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. If the CPU switches this interrupt to active (by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register), then the currently active interrupt will be pushed onto a stack. When an interrupt is cleared by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register, if there are any interrupts on the stack, the first entry is popped off and put back into the R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ register, so that software may continue where it left off.

7.2.2.5.6 VIM ECC Support

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the R5FSS_VIM_DEDVEC register is used to provide the default vector for the *coreN_IRQADDRV* signal, the R5FSS_VIM_IRQVEC register, and the R5FSS_VIM_FIQVEC register. The R5FSS_VIM_DEDVEC should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling.

Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
    a. Potentially switch to a completely software interrupt handler in the mean time
2. Restart the application from scratch
3. Reset the device
4. Sit in a loop (or WFI) while something external (for example, the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

Note

An interrupt that has an uncorrectable vector error (and thus uses the DED vector) will still have the priority of the original interrupt . This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by the R5FSS ECC aggregator.

7.2.2.5.7 VIM IDLE State

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface.

7.2.2.5.8 VIM Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM the software wants to take advantage of.

For IRQs, it is recommended to use the procedure in Section 7.2.2.5.8.1 , but the procedures in Section 7.2.2.5.8.2 or Section 7.2.2.5.8.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives.

For FIQs, it is recommended to use the procedure in Section 7.2.2.5.8.4 , but the procedure in Section 7.2.2.5.8.5 may be used as an alternative.

Note

These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

7.2.2.5.8.1 Servicing IRQ Through Vector Interface

If the associated CPU has the vector (VIC) interface enabled, then the following method is used for servicing IRQs:

1. Hardware handshake
    a. CPU asserts *coreN_IRQACK* high
    b. VIM asserts *coreN_IRQADDRV* to indicate that the *coreN_IRQADDR* bus is stable with the correct vector address
    c. CPU reads *coreN_IRQADDR*, jumps to that address, and de-asserts *coreN_IRQACK* low
    d. VIM de-asserts *coreN_IRQn* and *coreN_IRQADDRV*, VIM masks (discards) all IRQs with the same or lower priority
    e. VIM loads the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field (which corresponds to the vector address) into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, which causes the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTIRQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register
        ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt
4. Write any value to the R5FSS_VIM_IRQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.2.2.5.8.2 Servicing IRQ Through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the vector interface:

1. Read the R5FSS_VIM_IRQVEC register and jump to that address to service the ISR
    a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_IRQn* output. If another interrupt of a higher priority becomes available, the *coreN_IRQn* will re-assert, allowing priority interruption of an interrupt
    b. Reading this register will cause the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, and the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse

        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        ii. Clear the interrupt at the source
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

4. Write any value to the R5FSS_VIM_IRQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.2.2.5.8.3 Servicing IRQ Through MMR Interface (Alternative)

If a user does not want to use the R5FSS_VIM_IRQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_IRQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    a. Read the R5FSS_VIM_PRIIRQ register to determine which interrupt is the highest priority IRQ currently asserted, OR
    b. Optionally read the R5FSS_VIM_IRQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_IRQSTS_j register and use a software prioritization scheme to determine which IRQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

7.2.2.5.8.4 Servicing FIQ

When an FIQ interrupt is received, the CPU should follow these steps:

1. Read the R5FSS_VIM_FIQVEC register and jump to that address to service the ISR
    a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_FIQn* output. If another interrupt of a higher priority becomes available, the *coreN_FIQn* will re-assert, allowing priority interruption of an interrupt.
    b. Reading this register will cause the value from the R5FSS_VIM_PRIFIQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_PRIFIQ[9:0] NUM bit field, and the R5FSS_VIM_ACTFIQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTFIQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse

        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt

4. Write any value to the R5FSS_VIM_FIQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTFIQ[31] VALID bit

7.2.2.5.8.5 Servicing FIQ (Alternative)

If a user does not want to use the R5FSS_VIM_FIQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_FIQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    a. Read the R5FSS_VIM_FIQVEC register to determine which interrupt is the highest priority FIQ currently asserted, OR
    b. Optionally read the R5FSS_VIM_FIQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_FIQSTS_j register and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register.

7.2.2.6 R5FSS Region Address Translation (RAT)

The R5F is a 32-bit processor, which means it can only access 4GB of directly addressable memory. The R5FSS includes a region-based address translation (RAT) unit per core, which allows the R5F to access higher address ranges. The R5FSS RAT module translates a 32-bit input address into a 36-bit output address. It supports 4 regions. For more details on RAT functionality, refer to *Region-based Address Translation (RAT) Module*.

7.2.2.6.1 WKUP R5FSS Usage

R5 is a micro controller with 32b address, which is only able to access up to 4GB address space. However, Sitara™ SoC supports 36b address and majority of the memory region beyond lower 4GB are implemented. Region based address translation block, called RAT, is introduced to allow R5 core to access full 36b SoC memory map.

Each R5 core has its own RAT block, and only R5 core itself is able to program the RAT.

Figure 7-4 shows the main R5's default 32b memory map view when main R5 is out of reset.

The full RAT functionality is described in Section 7.2.2.6.2 , *RAT Function*.

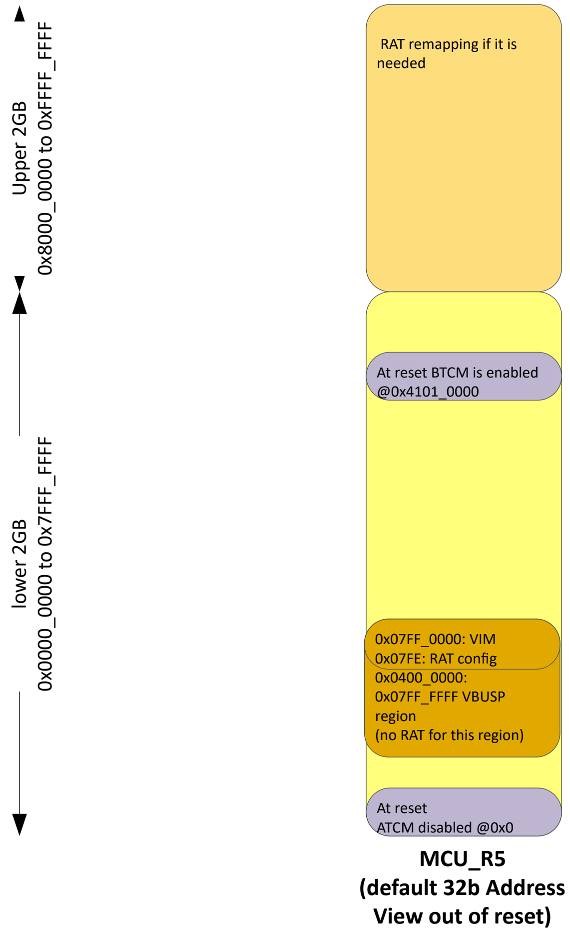

Figure 7-4. R5 Core Default Memory Map View

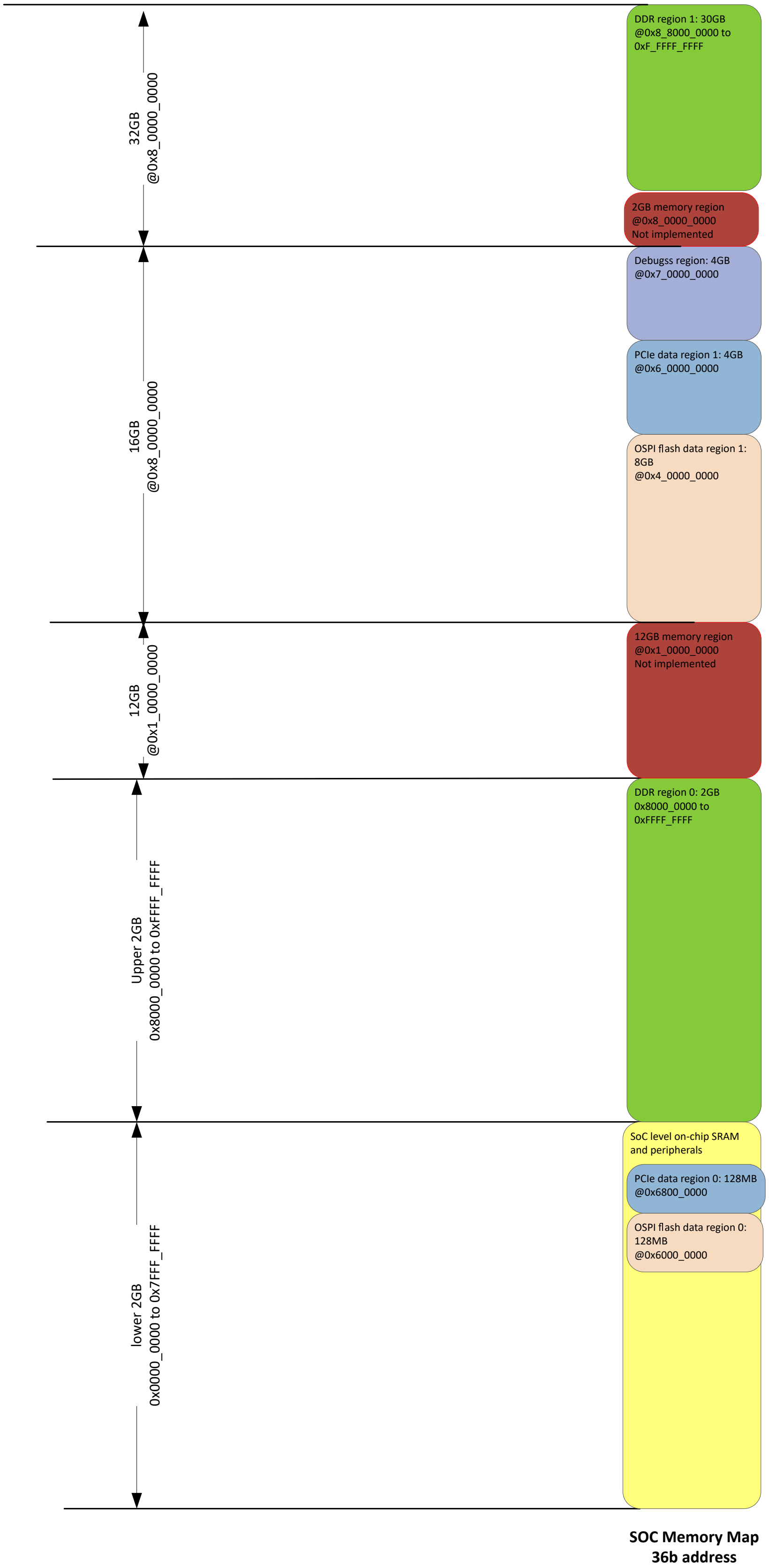

Figure 7-5. Typical Sitara SoC Memory Map View

RAT block enables R5 core to have full access on the SoC memory map including the memory region at and above 0x1_0000_0000.

Figure 7-6 shows how R5 access various end points, including its own ATCM, BTCM, VIM and SoC memory and peripherals. R5's ATCM is by default at address 0x0, and its BTCM is at address 0x4101_0000. R5 uses address 0x07FF_0000 to access its VIM and 0x07FE_0000 to access the RAT configuration region and all the other transactions between address range 0x0400_0000 to 0x07FF_FFFF are sent to the 32b peripheral interface to access the peripherals in SoC. The transactions with the rest of address are sent to RAT block, which could go through address remapping function from original R5's 32b address to 36b SoC address.

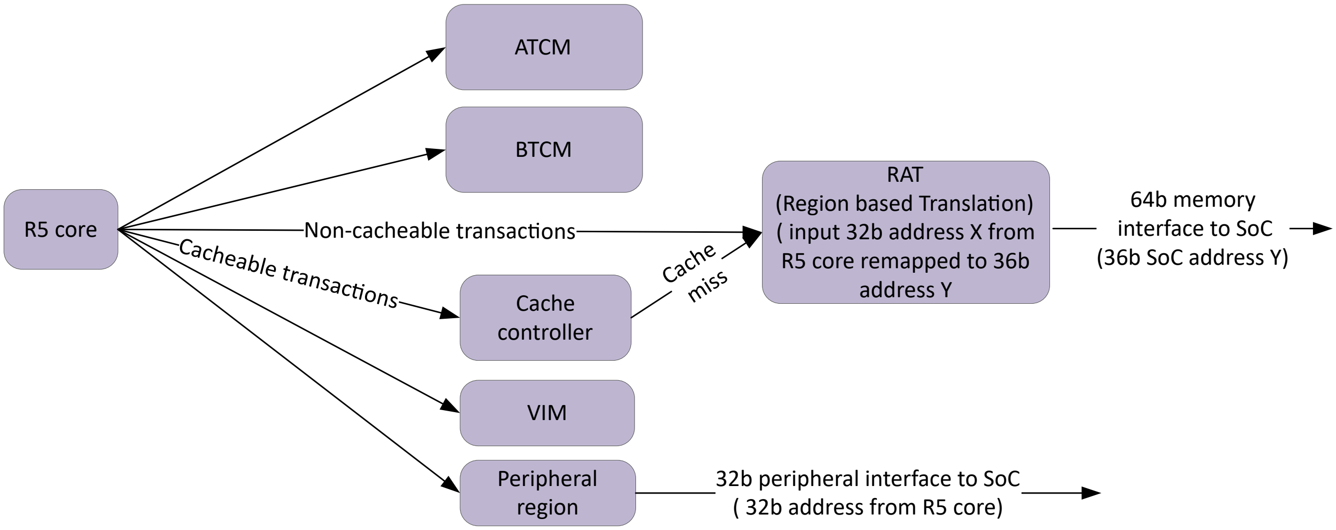

Figure 7-6. R5 Internal Address Decoding

7.2.2.6.2 RAT Function

RAT block is responsible to do a region based address translation. For each region, user can define the starting address and size of the region and remapping the transactions to use a new address range.

The starting address and region size need to be aligned. For example, if the region size is 16KB, the starting address for that region needs to be 16KB aligned. And region size should be minimum 4KB or larger to avoid transactions cross the region boundaries.

Each RAT block supports multiple programmable regions. And it is important that those regions are not overlapping with each other.

RAT block is by default disabled, which means RAT block does not do address remapping. The 32b address coming from R5 core is directly sent out to the SoC level. The user can program each RAT remapping region individually. For the transactions does not hit any remapping region, RAT block just simply forwards the transactions to the SoC level with its original address.

7.2.2.6.3 How to use RAT Block in R5

Table 7-7 shows the default R5 memory map view. Without enabling RAT function, all the regions beyond 4GB address space will not be accessible by R5.

Sitara™ SoC memory map is constructed the way to allow R5 and high level application processor such as A53 have similar memory map as possible. This methodology enables that R5 and ARM A53 core have a common memory map for all the SoC level memories and SoC level peripherals except a few exceptions:

- DDR's data space beyond 32b address, basically upper DDR data space beyond 2GB
- PCIe data space beyond 32b address
- OSPI data space beyond 32b address
- Debug configuration region

Table 7-7. R5 Memory map by Default

	R5 Memory Map(32b)	SoC Memory Map (36b)
SoC Level peripheral and on-chip SRAM	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF
2GB DDR region	Same as SoC memory map: 0x8000_0000 to 0xFFFF_FFFF	0x80000_0000 to 0xFFFF_FFFF
Additional DDR region	Not accessible	0x8_8000_0000 (30GB)
Additional 8GB OSP Space	Not accessible	0x4_0000_0000 (4GB) 0x5_0000_0000 (4GB)
Additional PCIe data space	Not accessible	0x6_000_0000
Debug configuration region	Not accessible	0x7_0000_0000

Even though all the transactions other than going to ATCM/BTCM and transactions between address range 0x0400_0000 to 0x07FF_FFFF could use RAT block to remap to different address, it is recommended that only use RAT block to remap the R5 transactions with address between 0x8000_0000 to 0xFFFF_FFFF.

- Any transactions from R5 with address between 0x0 to 0x7FFF_FFFF are sent out to SoC directly (unless it is targeted to its internal end points such as A/B TCM, its VIM and RAT configuration)
- Only enable RAT to remap the transactions with address between 0x8000_0000 to 0xFFFF_FFFF if R5 needs to access the following address space:
  - PCIe data space at address 0x6_0000_0000
  - OSPI data space address 0x4_0000_0000 and 0x5_0000_0000
  - Debug configuration region at address 0x7_0000_0000
  - DDR data space at address 0x8_8000_0000

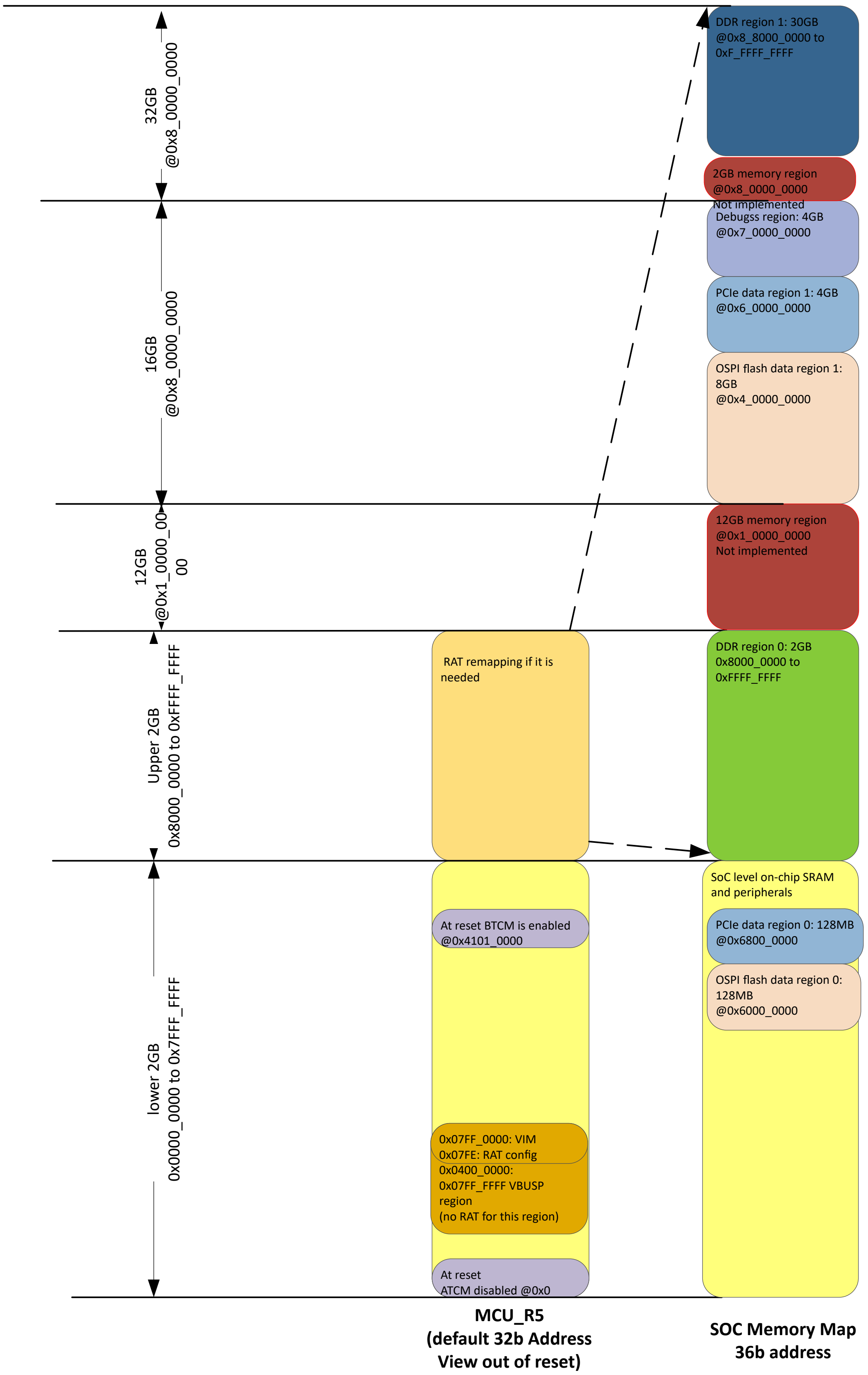

Figure 7-7. Example of Using RAT to Access Full 36b SoC Memory Map

7.2.2.6.4 Example of Using RAT to Access Full 36b SoC Memory Map

This section shows an example on how to utilize RAT block to allow R5 to access 36 SoC Memory Map. The RAT block inside R5 has up to 8 address remapping regions.

Assuming R5 needs to access the following region:

- All the SoC level on-chip SRAM
- All the SoC level peripherals
- Access 512MB OSPI region at address 0x4_0000_0000
- Access 1GB DDR region at address 0x9_0000_0000
- Access 512MB DDR region at address 0x8000_0000

First of all, we need to construct 32b R5 memory map as following and how those memory spaces are mapped to SoC level, shown in Table 7-8. Users can define where the OSPI and DDR data space placed inside R5's memory map and how they should be mapped to SoC level address map. Table 7-8 just shows one of the many possible ways to construct the memory map.

Table 7-8. Example of R5 Address Mapping

	R5 Memory Map(32b)	**SoC Memory Map (36b)**	**RAT Remapping**
SoC Level peripheral and on-chip SRAM (This is guaranteed by SoC Hardware design. No user configuration is needed)	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF	Not RAT Remapping
512MB OSPI data region (user defined)	0x8000_0000 to 0x9FFF_FFFF	0x4_0000_0000 to 0x4_1FFF_FFFF	Using RAT remapping region 0
512MB DDR space (user defined)	0xA000_0000 to 0xBFFF_FFFF	0x8000_0000 to 0x9FFF_FFFF	Using RAT remapping region 1
Additional 1GB DDR Space (user defined)	0xC000_0000 to 0xFFFF_FFFF	0x9_0000_0000 to 0x9_3FFF_FFFF	Using RAT remapping region 2

In this example, only three RAT regions are needed:

- Region 0 is used to remap R5's address between 0x8000_0000 to 0x9FFF_FFFF to SoC level address 0x4_0000_0000 to 0x4_1FFF_FFFF
- Region 1 is used to remap R5's address between 0xA000_0000 to 0xBFFF_FFFF to 0x8000_0000 to 0x9FFF_FFFF
- Region 2 is used to remap R5's address 0xc000_0000 to 0xFFFF_FFFF to 0x9_0000_0000 to 0x9_3FFF_FFFF.

In order achieving those mappings, those are the setting of the RAT configuration registers:

	Region 0	**Region 1**	**Region 2**	**Other regions**
Region control register	Enabled, size set to 512MB	Enabled, size set to 512MB	Enabled, size set to 1GB	disabled
Region base(32b)	0x8000_0000	0xA000_0000	0xc000_0000	Don't care
Region translated lower address(32b)	0x0000_0000	0x8000_0000	0x0000_0000	Don't care
Region translated upper address	0x4	0x0	0x9	Don't care

Figure 7-8 shows how RAT is remapping the address between R5's 32b address to 36b SoC address.

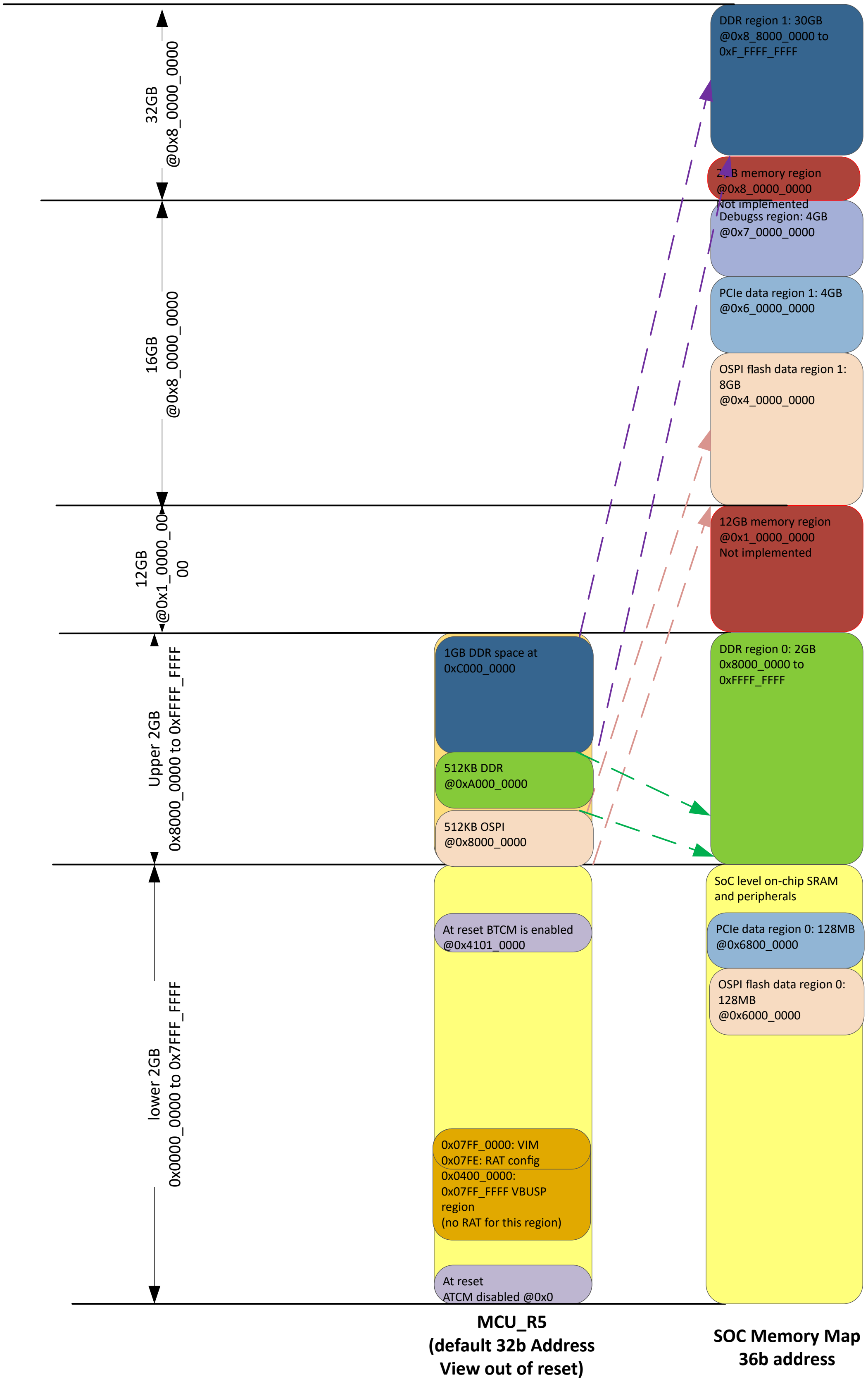

Figure 7-8. RAT Configuration Example

7.2.2.7 R5FSS ECC Support

The R5F provides native ECC and parity support on all related memories, generating and checking the redundancy automatically. The methods for checking and reporting errors are available in the *Arm Cortex-R5 Technical Reference Manual*.

The R5FSS adds the capability of testing this logic by allowing errors (single and double bit) to be injected into memories (for testing purposes) via an ECC aggregator (per core). Note that because the R5FSS ECC aggregator is only used in error-injection mode, it only supports a subset of the generic ECC aggregator functionality in the device.

For a detailed description of the generic ECC aggregator functionality, see *ECC Aggregator*. For register descriptions of the R5FSS aggregators, see R5FSS_CPU0_ECC_AGGR_CFG_REGS Registers and R5FSS_CPU1_ECC_AGGR_CFG_REGS Registers, respectively.

Table 7-9 provides the RAM ID. This is needed for bit field [10-0] ECC_VECTOR in the corresponding R5FSS_CPU0_VECTOR register (part of the ECC aggregator register space).

Table 7-9. RAM ID Map for ECC Aggregator (Per Core)

RAM ID	Memory Name
0	CPU0 ITAG RAM0
1	CPU0 ITAG RAM1
2	CPU0 ITAG RAM2
3	CPU0 ITAG RAM3
4	CPU0 IDATA BANK0
5	CPU0 IDATA BANK1
6	CPU0 IDATA BANK2
7	CPU0 IDATA BANK3
8	CPU0 DTAG RAM0
9	CPU0 DTAG RAM1
10	CPU0 DTAG RAM2
11	CPU0 DTAG RAM3
12	CPU0 DDIRTY RAM
13	CPU0 DDATA RAM0
14	CPU0 DDATA RAM1
15	CPU0 DDATA RAM2
16	CPU0 DDATA RAM3
17	CPU0 DDATA RAM4
18	CPU0 DDATA RAM5
19	CPU0 DDATA RAM6
20	CPU0 DDATA RAM7
21	CPU0 ATCM BANK0
22	CPU0 ATCM BANK1
23	CPU0 B0TCM BANK0
24	CPU0 B0TCM BANK1
25	CPU0 B1TCM BANK0
26	CPU0 B1TCM BANK1
27	CPU0 VIM RAM

7.2.2.8 R5FSS Memory View

The memory view of the R5F (that is, the memory map as seen by each R5F) is a function of several things:

- Exception vector bootstrap: The R5F exception table (including boot vector) is always 32 bytes at address 0x00000000 as seen by the R5F. If not booting from a TCM, then boot is done over the main memory interface. The exception vector bootstrap is under software control, which allows these 32 bytes at address 0x00000000 to be remapped somewhere else in the SoC memory map.
- TCM locations: TCMs can be enabled or disabled and located at different places in the memory map, depending on bootstrap configuration. For more details, see Section 7.2.2.2.2 .
- Peripheral interface locations: The RF5 natively supports three interfaces for peripheral access. Each can be enabled/disabled and located based on bootstrap configuration. Note that the VBUSP peripheral interface must be enabled in order to use RAT and VIM.
- RAT base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- VIM base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- RAT programming: The RAT can take regions of memory accessible by the main memory interface and map them to different addresses.

The combination of the above determines what the R5F sees where in the memory map, and over what interface different transactions come out. Every transaction that does not directly address a TCM or a peripheral interface comes over the main memory interface. Transactions on the main memory interface can be further remapped with the RAT.

See *Memory Map*, for the complete R5F memory view for this device.

7.2.2.9 R5FSS Interrupts

All interrupts that are generated by the R5FSS are summarized in *Module Integration*, along with their mapping. They can be divided into the following groups:

- R5F CPU internal interrupts: These are described in *Arm Cortex-R5 Technical Reference Manual*.
- ECC aggregator interrupts: These are described in the *ECC Aggregator* chapter.
- RAT exception interrupt: This is described in Section 7.2.2.6 .

7.2.2.10 R5FSS Debug and Trace

The R5FSS supports standard Arm CoreSight debug and trace architecture. For more details, see the *On-chip Debug* chapter.

7.2.2.11 R5FSS Boot Options

There are two methods of booting the R5F, or rather, two methods of placing the exception vectors (of which the boot vector is one).

The first method is to have the exception vectors external to the R5F. The user can place the exception vectors at the address indicated by the exception vector bootstrap and then program the boot vector there. When the processor exits reset, it will fetch the boot vector from this location.

The second method is to boot from a TCM. To do this, software should take the following steps:

1. Assert the correct bootstraps
    a. To boot from ATCM, set CPUn_INITRAMA (or CPUn_INITRAMB to boot from BTCM)
    b. Assert CPUn_LOCZRAMA properly for the desired TCM
2. Assert CPUn_HALT
3. Release the CPU from reset
4. Load the desired code into the TCM via the TCM target port
    a. Exception vectors should be located at address 0x00000000 of the TCM
5. De-assert CPUn_HALT

7.2.2.12 R5FSS Core Memory ECC Events

The R5F core generates several events as part of event bus that can be monitored by the PMU for debugging. The memory ECC related events from the event bus are exported to ESM for monitoring.

There are two ECC interrupts to the ESM that aggregate different categories of ECC events – CPU single error, CPU multi error. Each ECC event has a 2-bit event bus counter associated with it. Everytime an event occurs, the counter is incremented by 1 till it reaches the max value of 3. The interrupt is asserted if the bus counter of any event associated with the interrupt is non-zero.

Each event bus counter has a MMR decrement control to decrement the counter by 1. So, for example, if a counter value is 2, the MMR to decrement the counter would need to be written 2 times to decrement the counter to 0. The reason decrement control has been added instead of clear control is if a new error occurs between the time the status register is read and the clear MMR is written, the new error would be lost. Write-to-decrement ensures that this does not happen.

When all event bus counters of an associated interrupt are zero, the interrupt is cleared. It takes three clock cycles for the event bus counter to be decremented once the write to the decrement control MMR presents itself at the R5FSS boundary.

Since each of the four ECC interrupts have single bit control to set the interrupt but multiple bits for clearing it, note that once an interrupt is set using the R5FSS_EVNT_BUS_ESM_SET register, it can be cleared by setting all the bits of the R5FSS_EVNT_BUS_ESM_CLR register that correspond to that particular interrupt. For example, if bit [0] of the R5FSS_EVNT_BUS_ESM_SET register is set, it can be cleared by setting bits [7-0] of the R5FSS_EVNT_BUS_ESM_CLR register to clear the interrupt.

The R5F core event bus only signals event when it is enabled. Non-invasive or invasive debug mode needs to be enabled to enable the PMU counters.

The export of the events to the event bus can be enabled by setting the X bit in the Performance Monitor Control Register of the R5F core. For more details, refer to Arm R5 TRM.

Table 7-10. R5F Event Bus Single-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
22	Instruction cache tag RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0
23	Instruction cache data RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1
24	Data cache tag or dirty RAM parity error or correctable ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2
25	Data cache data RAM parity error or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3
40	ATCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4
41	B0TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5
42	B1TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6
43	TCM correctable ECC error reported by load/ store unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7
44	TCM correctable ECC error reported by prefetch unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8

Table 7-11. R5F Event Bus Multi-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
26	TCM fatal ECC error reported from the prefetch unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0

Table 7-11. R5F Event Bus Multi-Bit Error Events (continued)

Event Bus Bit #	Description	Associated Status Register
27	TCM fatal ECC error reported from the load/ store unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1
33	Data cache data RAM fatal ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2
34	Data caches tag/dirty RAM fatal ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3
37	ATCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4
38	B0TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5
39	B1TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6

7.2.3 Vectored Interrupt Manager (VIM)

This section describes the VIM module in the device.

7.2.3.1 VIM Overview

The Vectored Interrupt Manager (VIM) aggregates interrupts to a CPU. It is intended for use with a Cortex R5 from ARM. The VIM has up to 1024 interrupt inputs, which may be either level or pulse. Each interrupt has a programmable priority (0-highestthrough 15-lowest). Each interrupt may also be mapped as an IRQ or FIQ (FIQ is also often denoted as Non-Maskable Interrupt, or NMI).

7.2.3.1.1 VIM Features

- 32-1024 Interrupt inputs
  - Configurable by groups of 32
- Each interrupt has its own 4-bit programmable priority
  - Supports Priority interruption of interrupts
- Each interrupt has its own enable mask
- Each interrupt can be programmed as either an IRQ or FIQ
- Each interrupt has its own programmable 32-bit Vector address associated with it
  - Protected with SECDED
- One IRQn and FIQn output
- Vectored Interrupt Interface
  - Compatible with ARM Cortex R5 VIC Port
- Default Vector provided when a Double-Bit error is detected
- Provides clock phase inputs so VIM can run at CPU clock while interface runs at a different, synchronous clock

7.2.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

7.2.3.2 VIM Functional Description

7.2.3.2.1 Block Diagram

Figure 7-9 shows the Vectored Interrupt Manager block diagram.

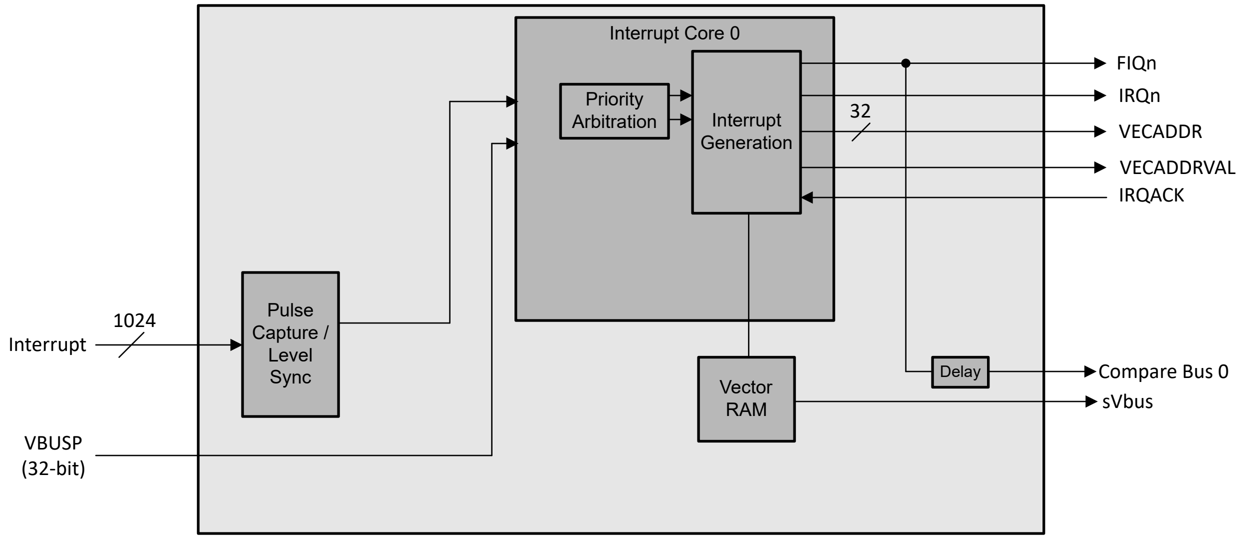

Figure 7-9. VIM Block Diagram

7.2.3.2.2 Interrupt Inputs

The VIM can have up to 1024 interrupt inputs, build-time configurable by multiples of 32 (*num_interrupts* parameter). Each interrupt can be either a level or a pulse (both active high).

Level interrupts are synchronized to the VIM clock. This synchronized value is captured in to a flop.

Pulse interrupts use rising edge detection. Each input has its own edge detection circuit. It is recommended that if pulses are pipelined between the source and the VIM, that the pipe stage replicates the pipe flop and ORs the output in order to protect against transient errors in the pipeline flop. Once an edge has been detected, the raw status is set.

There is no minimum pulse width, as true edge detection is used. The input signal should, however, be glitch free.

7.2.3.2.3 Interrupt Outputs

The VIM has two interrupt outputs, core*N*_IRQn and core*N*_FIQn (active low levels). Each interrupt input for core *N* can be programmed to influence either the core*N*_IRQn or core*N*_FIQn output via the Group *M* Interrupt Map Register (Base Address + 0x200 + *N**0x20 + 0x18).

7.2.3.2.4 Priority Interrupt / Nested Interrupts

Each interrupt has a priority number assigned to it (set using the 4.1.20 Interrupt *Q* Priority Register (Base Address + 0x1000 + *Q**0x4) register). Legal values are 0 to 15 where 0 is the highest priority and 15 is the lowest priority. The highest priority interrupt is the pending interrupt with the smallest priority number. If two pending interrupts have the same priority, the interrupt lowest numerically (0 through maximum number of interrupts) is prioritized. IRQs and FIQs are prioritized separately.

The VIM supports the interrupt of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate, but both use the same mechanism. When an interrupt goes from pending to active (FIQ: reading the FIQ Vector Address (Base Address + 0x1C), IRQ: reading the IRQ Vector Address (Base Address + 0x18) or the core*N*_IRQACK going high), then the interrupt is loaded into the corresponding Active Register, and all interrupts of an equal or lesser priority are masked off (see note below). If, before this interrupt is cleared (writing the FIQ Vector Address (Base Address + 0x1C) or IRQ Vector Address (Base Address + 0x18)) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. The CPU may or may not service the higher priority interrupt. If the CPU switches this interrupt to active, by reading the corresponding Vector Address Register (or core*N*_IRQACK going high for an IRQ) , then the currently active interrupt will be pushed on to a stack. When an interrupt is cleared by writing the Vector Address Register, if there are any interrupts on the stack, the first entry is popped off and put back into the Active

Register, so that software may continue where it left off. Note that the IRQVEC/FIQVEC address registers are *not* repopulated with the old vector as it's assumed that the ISR is picking back up where it left off. Only the interrupt number and priority are restored to the ACTIRQ/ACTFIQ registers. If software needs the vector again, it will have to read it by using the interrupt number.

Note

"Masked off" means that they are masked off from priority arbitration to interrupt the currently active interrupt, it does NOT mean that the status bits in the regsiters are masked off. That is, this priority masking has NO EFFECT on whether the status bits are visible in the masked registers such as the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04).

7.2.3.2.5 VIC Port

The VIM is designed to work with the VIC interface of an ARM Cortex R5.

7.2.3.2.6 Latency

There are several factors that go in to the speed of processing an interrupt: the interrupt controller, the processor, and the system latency.

The VIM behaves deterministically (except for synchronizer delay). Table 7-12 shows the latency of the VIM.

Table 7-12. VIM Latency

Step	Cycles	Note
Edge Detection	2-3	Synchronizing to VIM Clock
Interrupt Capture	1	
Prioritization and Vector Read	1	IRQ Could be stalled here if an FIQ is reading the Vector RAM
		IRQ/FIQ output asserted

The next factor is the processor itself

Table 7-13. Processor Interrupt Latency

Step	Cycles(1)	Note
Take Exception		
Store State		Stack system registers etc
Read Vector	1	Through MMR or VIC interface (for IRQ. VIC interface will be faster)
Jump to Vector		

(1) These steps are dependent on the processor. See R5 spec for details.

The final factor is system latency to access the actually instructions for the ISR. This will be dependent on where the instructions are (cache, TCM, system memory etc) and dependent on the system latency to reach those memories (1 cycle for cache/TCM, System dependent for external memory)

7.2.3.2.7 Safety

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the DED Vector Address (Base Address + 0x30) is used instead for the core*N*_IRQADDRV, IRQ Vector Address (Base Address + 0x18), and FIQ Vector Address (Base Address + 0x1C). The DED Vector Address should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling. Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
    a. Potentially switch to a completely software interrupt handler in the mean time
2. Restart the application from scratch

3. Reset the device
4. Sit in a loop (or WFI) while something external (say the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

An interrupt that has an uncorrectable vector error and thus uses the DED Vector, will still have the priority of the original interrupt (that is for masking purposes). This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by an external ECC aggregator through sVbus ports.

7.2.3.2.8 IDLE

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface because it does not have a clock IPG. To clock stop the sub-system that includes the VIM, disable (mask) all interrupts and wait for the IDLE signal to assert.

7.2.3.3 Interrupt Conditions

7.2.3.3.1 CPU Interrupts

See Table 7-14 for the interrupts generated by the module.

Table 7-14. Interrupts

Interrupt	Description
core0_IRQn	IRQ Interrupt (Active Low)
core0_FIQn	FIQ Interrupt (Active Low)

7.2.3.3.2 Interrupt Description

7.2.3.3.2.1 coreN_IRQn

This is a normal interrupt, active low level, for Core N. It can be serviced via the VIC interface or through the MMR interface.

7.2.3.3.2.2 coreN_FIQn

This is a fast (or non-maskable) interrupt, active low level, for Core N. FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface.

7.2.3.3.3 Interrupt Condition Control

7.2.3.3.3.1 coreN_IRQn

Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (Group *N* Interrupt Map Register (Base Address + 0x200 + N*0x20 + 0x18)) and is enabled (Group *N* Interrupt Enabled Set Register (Base Address + 0x200 + N*0x20 + 0x08)), and its priority is not masked (4.1.11 IRQ Priority Mask Register (Base Address + 0x28), and it is not masked because of nested interrupt priority masking (2.2.5 Priority Interrupt / Nested Interrupts), then it will cause an IRQ to assert.

7.2.3.3.3.2 coreN_FIQn

Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ (Group *N* Interrupt Map Register (Base Address + 0x200 + N*0x20 + 0x18)) and is enabled (Group *N* Interrupt Enabled Set Register (Base Address + 0x200 + N*0x20 + 0x08)), and its priority is not masked (4.1.12 FIQ Priority Mask Register (Base Address + 0x2C)), and it is not masked because of nested interrupt priority masking (2.2.5 Priority Interrupt / Nested Interrupts), then it will cause an FIQ to assert.

7.2.3.3.4 Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM software wants to take advantage of. For IRQs, it is recommended to use 3.4.1 IRQ through the Vector

Interface, but 3.4.2 or 3.4.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives. For FIQs, it is recommended to use 3.4.4 FIQ, but 3.4.5 may be used as an alternative.

Note

These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

7.2.3.3.4.1 IRQ through the Vector Interface

If the attached CPU has the Vector Interface enabled, then the following method is used for servicing IRQs

1. Hardware handshake
   a. CPU asserts coreN_IRQACK signal high
   b. VIM asserts coreN_IRQADDRV to indicate that the coreN_IRQADDR bus is stable with the correct Vector Address
   c. CPU reads the coreN_IRQADDR, jumps to that address, and de-asserts coreN_IRQACK signal low
   d. VIM de-asserts coreN_IRQn_intr and coreN_IRQADDRV, VIM masks all IRQs with the same or lower priority
   e. VIM loads the value from the Prioritized IRQ (Base Address + 0x08) (which corresponds to the vector address) to be loaded into the Active IRQ (Base Address + 0x20) and the valid bit to be set
2. Service an interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active IRQ (Base Address + 0x20) to determine number and reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group M Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group M Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group M Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group M Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

4. 4. Write any value to the IRQ Vector Address (Base Address + 0x18)
   a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
   b. This will clear the valid bit of the Active IRQ (Base Address + 0x20)

7.2.3.3.4.2 IRQ through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the Vector Interface.

1. Read the IRQ Vector Address (Base Address + 0x18) and jump to that address to service the ISR

    a. Reading this register will mask all interrupts of an equal or lower priority and de-assert the IRQn output. If another interrupt of a higher priority becomes available, the IRQn will re-assert, allowing priority interruption of an interrupt.
    b. Reading this register will cause the value from the Prioritized IRQ (Base Address + 0x08) (which corresponds to the vector address) to be loaded into the Active IRQ (Base Address + 0x20) and the valid bit to be set

2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active IRQ (Base Address + 0x20) to determine number and reading the Group M Type Map Register (Base Address + 0x200 + M*0x20 + 0x1C) to determine type)
    a. Pulse
        i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
        ii. Clear the interrupt at the source
            1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
            1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
            2. If the source maintains the level, then it means there is another interrupt
4. Write any value to the IRQ Vector Address (Base Address + 0x18)
    a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
    b. This will clear the valid bit of the Active IRQ (Base Address + 0x20)

7.2.3.3.4.3 IRQ through MMR Interface (Alternative)

If a user does not want to use the Vector Address registers, the VIM may be used as a more traditional interrupt controller. Note that in this mode, priority masking will not work if route 1b is used (below) as the hardware prioritization may not match the software prioritization scheme. In this case, software would be responsible for doing all priority operations

1. Determine which interrupt to service
    a. Read the Prioritized IRQ (Base Address + 0x08) to determine which interrupt is the highest priority IRQ currently asserted OR
    b. Optionally read the IRQ Group Status (Base Address + 0x10) to determine which groups have IRQs pending, then read the Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10) and use a software prioritization scheme to determine which IRQ to service
2. Service the interrupt
3. Read the IRQ Vector Address (Base Address + 0x18)
    a. Note, this step can be done any time before step 4
    b. Value is ignored
4. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)

  a. Pulse
    i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
    ii. Clear the interrupt at the source
      1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

  b. Level
    i. Clear the interrupt at the source
    ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
      1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
      2. If the source maintains the level, then it means there is another interrupt

5. Write any value to the IRQ Vector Address (Base Address + 0x18)

7.2.3.3.4.4 FIQ

When an FIQ interrupt is received, the CPU should follow these steps.

1. Read the FIQ Vector Address (Base Address + 0x1C) and jump to that address to service the ISR
  a. Reading this register will mask all interrupts of an equal or lower priority and de-assert the FIQn output. If another interrupt of a higher priority becomes available, the FIQn will re-assert, allowing priority interruption of an interrupt.
  b. Reading this register will cause the value from the Prioritized FIQ (Base Address + 0x0C) (which corresponds to the vector address) to be loaded into the Active FIQ (Base Address + 0x24) and the valid bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active FIQ (Base Address + 0x24) to determine number and reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
  a. Pulse
    i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
    ii. Clear the interrupt at the source
      1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

  b. Level
    i. Clear the interrupt at the source
    ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
      1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
      2. If the source maintains the level, then it means there is another interrupt

4. Write any value to the FIQ Vector Address (Base Address + 0x1C)

   a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
   b. This will clear the valid bit of the Active FIQ (Base Address + 0x24)

7.2.3.3.4.5 FIQ (Alternative)

If a user does not want to use the Vector Address registers, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the FIQ Vector Address (Base Address + 0x1C) is never read). Software would be responsible for doing all priority operations

1. Determine which interrupt to service
   a. Read the Prioritized FIQ (Base Address + 0x0C) to determine which interrupt is the highest priority FIQ currently asserted OR
   b. Optionally read the FIQ Group Status (Base Address + 0x14) to determine which groups have IRQs pending, then read the Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14) and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

7.2.3.4 Memory Map

Each Interrupt Core (*N* = 0) has its own MMR interface with its own independent memory map

Table 7-15. Core *N* Memory Map

Address Offset	Register
0x00	Revision Register
0x04	Info Register
0x08	Prioritized IRQ
0x0C	Prioritized FIQ
0x10	IRQ Group Status
0x14	FIQ Group Status
0x18	IRQ Vector Address
0x1C	FIQ Vector Address
0x20	Active IRQ
0x24	Active FIQ
0x28-0x2F	*Reserved*

Table 7-15. Core *N* Memory Map (continued)

Address Offset	Register
0x30	DED Vector Address
0x34-0x1FF	*Reserved*
0x400 + *M**0x20 + 0x00	Group *M* Interrupt Raw Status/Set Register
0x400 + *M**0x20 + 0x04	Group *M* Interrupt Enabled Status/Clear Register
0x400 + *M**0x20 + 0x08	Group *M* Interrupt Enabled Set Register
0x400 + *M**0x20 + 0x0C	Group *M* Interrupt Enabled Clear Register
0x400 + *M**0x20 + 0x10	Group *M* Interrupt IRQ Enabled Status/Clear Register
0x400 + *M**0x20 + 0x14	Group *M* Interrupt FIQ Enabled Status/Clear Register
0x400 + *M**0x20 + 0x18	Group *M* Interrupt Map Register
0x400 + *M**0x20 + 0x1C	Group *M* Type Map Register
0x1000 + *Q**0x4 – 00x1FFF	Interrupt *Q* Priority Register
0x2000 + *Q**0x4 – 0x2FFF	Interrupt *Q* Vector Register

There are *M* interrupt groups (0 through *num_groups*-1) with 32 interrupts per group.

There are *Q* interrupt inputs where *Q* = *M* * 32.

Accesses to the Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4) must be word-aligned, 32-bit accesses. Any write received with no bytes enabled will be ignored. Any writes receive with all bytes enabled will be executed. Any other write will not execute and will return an error status of Addressing Error.

7.2.3.5 Module I/O

7.2.3.5.1 Clocks, Reset, Emulation

Table 7-16. Clocks, Reset, Emulation

Pin Name	Type	Function
core0_clk	In	Clock for Core 0
core0_phase	In	Phase Indicator for Core 0
core0_srst_n	In	Sync Module Reset for Core 0
core0_arst_n	In	Async Module Reset for Core 0
core0_clkstop_idle	Out	Clock Stop Idle

7.2.3.5.2 VBUSP Target Interface

(N=0). Core0 interface is used for interrupt core 0.

Table 7-17. VBUSP Target Interface

Pin Name	Type	Function
core*N*_cfg_req	In	Request
core*N*_cfg_address[13:0]	In	Address (byte address)
core*N*_cfg_dir	In	Direction (read or write)
core*N*_cfg_xcnt[2:0]	In	Transaction Count
core*N*_cfg_byten[3:0]	In	Byte enables
core*N*_cfg_wdata[31:0]	In	Write data
core*N*_cfg_rdatap[31:0]	Out	Read data
core*N*_cfg_rready	Out	Read ready
core*N*_cfg_wready	Out	Write ready
core*N*_cfg_rstatus[2:0]	Out	Read Status

Table 7-17. VBUSP Target Interface (continued)

Pin Name	Type	Function
core*N*_cfg_emudbg	In	Emulation Debug

7.2.3.5.3 Interrupt Inputs

Core0 interface is used for interrupt core 0.

Table 7-18. Interrupt Inputs

Pin Name	Type	Function
core0_in_intr[Q-1:0]	In	Core 0 Interrupt Inputs

7.2.3.5.4 Interrupt Outputs

Table 7-19. Interrupt Outputs

Pin Name	Type	Function
core0_IRQn_intr	Out	IRQ Interrupt for core 0– Active Low Level
core0_FIQn_intr	Out	FIQ Interrupt for core 0 – Active Low Level

7.2.3.5.5 VIC Interfaces

(*N*=0). Core0 interface is used for interrupt core 0.

Table 7-20. VIC Interfaces

Pin Name	Type	Function
core*N*_vic_IRQADDRV	Out	IRQ Address Valid
core*N*_vic_IRQADDR[31:2]	Out	IRQ Address
core*N*_vic_IRQACK	In	Interrupt Acknowledge

7.2.3.5.6 Compare Outputs

These pins will never be on an isolation boundary and therefore their isolation values are don't-care. *Y* is dependent on the configuration

Table 7-21. Compare Outputs

Pin Name	Type	Function
core0_compare_bus[*Y*:0]	Out	Comparison Bus for Core0 to CCMR5

7.2.3.5.7 ECC Control and Status Bus

(*N*=0). Core0 interface is used for interrupts for core 0.

Table 7-22. ECC Control and Status Bus

Signal Name	Dir	Default Val	Description
core*N*_ramecc_strb	In	1'b0	Strobe to sample the incoming serial data
core*N*_ramecc_txd	In	1'b0	Output serial data
core*N*_ramecc_rxd	Out	1'b0	Input serial data
core*N*_ramecc_pend[1:0]	Out	2'd0	Level Interrupt source

7.2.3.5.8 DFT

Table 7-23. DFT

Signal Name	Dir	Default Val	Description
dft_clk_force_en	In	1'b0	DFT Clock Force Enable
dft_partition_enn	In	1'b0	DFT Clock Partition Enable
dft_scan_en	In	1'b0	DFT Scan Enable

Table 7-23. DFT (continued)

Signal Name	Dir	Default Val	Description
dft_async_rst_sel	In	1’b0	DFT Async Reset Select
dft_test_async_rst_n	In	1’b0	DFT Async Test Reset
dft_tft_mcp_dis	In	1’b0	DFT MCP Disable
dft_local_clk_en	In	1’b0	DFT Local Clock Enable

7.2.3.5.9 RAM GPIO

Table 7-24. RAM GPIO

Signal Name	Dir	Default Val	Description
core*N*_ramdft_gpi[255:0]	In	256’d0	RAM GPI
core*N*_ramdft_gpo[255:0]	Out	256’d0	RAM GPO

7.2.3.6 Programmer's Guide

7.2.3.6.1 Initialization Sequence

At initialization, the following tasks should be performed:

1. Program the DED Vector Address (Base Address + 0x30)
2. Program Group *M* Interrupt Map Register (Base Address + 0x200 + *M**0x20 + 0x18)
3. Program Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C)
4. Program Interrupt *Q* Priority Register (Base Address + 0x1000 + *Q**0x4)
5. Program Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4)
6. Enable interrupts via the Group *M* Interrupt Enabled Set Register (Base Address + 0x400 + *M**0x20 + 0x08)

Note that the Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4) for each interrupt that will be enabled must be written before the interrupt is enabled, even if software is not going to use the vector. Whenever an interrupt is prioritized, the RAM location for the interrupt is read, and if that location is un-initialized, an ECC error will be reported. If the vectors aren’t being used, then the RAM can be initialized by writing 0x0 to every location.

7.2.3.6.2 DED Behavior

Whenever there is 2-bit error detect on a Vector Address, the DED Vector Address (Base Address + 0x30) overrides all other vectors. Software should provide an ISR to handle this scenario at this address.

7.2.3.6.3 Power Up/Down Sequence

Before a clean power down, software should check that there are no pending interrupts, disable all interrupts, and wait for the clkstop_idle output.

7.3 Device Manager Cortex R5F Subsystem (WKUP_R5FSS)

This chapter describes the Arm Cortex R5F real-time microcontroller unit subsystem (WKUP_R5FSS) in the device.

7.3.1 WKUP_R5FSS Overview

The WKUP_R5FSS is a single-core implementation of the Arm® Cortex®-R5F processor that acts as the Device Manager responsible for boot, resource management, and power management functions. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm CoreSight™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

Note

The Cortex-R5F processor is a Cortex-R5 processor that includes the optional floating point unit (FPU) extension. In this TRM, all references to the Cortex-R5 processor apply to the Cortex-R5F processor by default.

There is one WKUP_R5FSS subsystem in the device. Table 7-25 shows WKUP_R5FSS allocation across device domains.

Table 7-25. R5FSS Allocation Across Device Domains

Module Instance	Domain		
	MCU	MAIN	WKUP
WKUP_R5FSS	–	–	✓

7.3.1.1 WKUP_R5FSS Features

The WKUP_R5FSS supports the following features:

- Single-core Arm Cortex-R5F
  - Core revision: r1p3
  - Armv7-R profile
  - L1 memory system
    - 32KB instruction cache
      - 4x8KB ways
      - SECDED ECC protected per 64 bits
    - 32KB data cache
      - 4x8KB ways
      - SECDED ECC protected per 32 bits
    - 64KB tightly-coupled memory (TCM)
      - SECDED ECC protected per 32 bits
      - TCM hard error cache Implemented in CPU
      - Readable/writable from system
      - TCMs initialized (to 0's) at reset
      - Split into A and B banks (with B further splitting into B0 and B1 interleaved banks)
        - 32KB TCMA (ATCM)
        - 16KB TCMB0 (B0TCM)
        - 16KB TCMB1 (B1TCM)
  - Low interrupt latency with restartable instructions
  - Non-maskable interrupt (NMI)
  - Full-precision floating point (VFPv3)
  - 16 region memory protection unit (MPU)
  - 8 breakpoints
  - 8 watchpoints
  - Dynamic branch prediction with global history buffer and 4-entry return stack
  - CoreSight debug access port (DAP)
  - CoreSight embedded trace macrocell (ETM-R5) interface
  - Performance monitoring unit (PMU)
- Interfaces
  - 64-bit VBUSM initiator pair (1 read, 1 write) for L3 memory accesses
  - 64-bit VBUSM target for TCM access
    - Also allows access to cache for debug purposes
  - 32-bit VBUSP initiator for peripheral access
  - 32-bit VBUSP target configuration port
  - 32-bit VBUSP target debug port

    - Allows access to all WKUP_R5FSS internal debug logic
  - ECC/Parity support on all internal SoC bus interfaces
  - ECC/Parity support on internal SoC bus bridges
- Synchronous clock domain crossing on all interfaces
  - Interfaces can run at an integer multiple of the core frequency
- 32-bit to 36-bit region-based address translation (RAT) on memory access initiators
  - 4 regions
    - Base address + size
    - Must be size aligned
- Integrated vectored interrupt manager (VIM)
  - 256 interrupts
    - Each interrupt programmable as either IRQ or FIQ
    - Each interrupt has a programmable enable mask
    - Each interrupt has a programmable 4-bit priority
  - Priority interrupt supported
  - Vectored interrupt interface
    - Compatible with R5F VIC port
    - Programmable 32-bit vector address per interrupt
      - Address is SECDED error protected
      - Default vector addresses provided on DED
    - Software interrupt generation
- Integrated ECC aggregators
  - Support for error injection to all supported ECC memory blocks to test ECC functionality (add-on function from TI)
  - One ECC aggregator to cover all RAMs and caches
- Standard Arm CoreSight debug and trace architecture at the R5FSS level
  - Cross triggering: Supported by cross trigger interface (CTI) (per CPU) and cross trigger matrix (CTM) components
  - Processor trace: Supported by embedded trace macrocell (ETM) (per CPU) and advanced trace bus (ATB) funnel components
- Boot
  - From ROM only

See Section 7.3.2 for a functional block diagram and more details on the WKUP_R5FSS.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

7.3.2 WKUP_R5FSS Functional Description

7.3.2.1 WKUP_R5FSS Block Diagram

Figure 7-10 shows the WKUP_R5FSS block diagram.

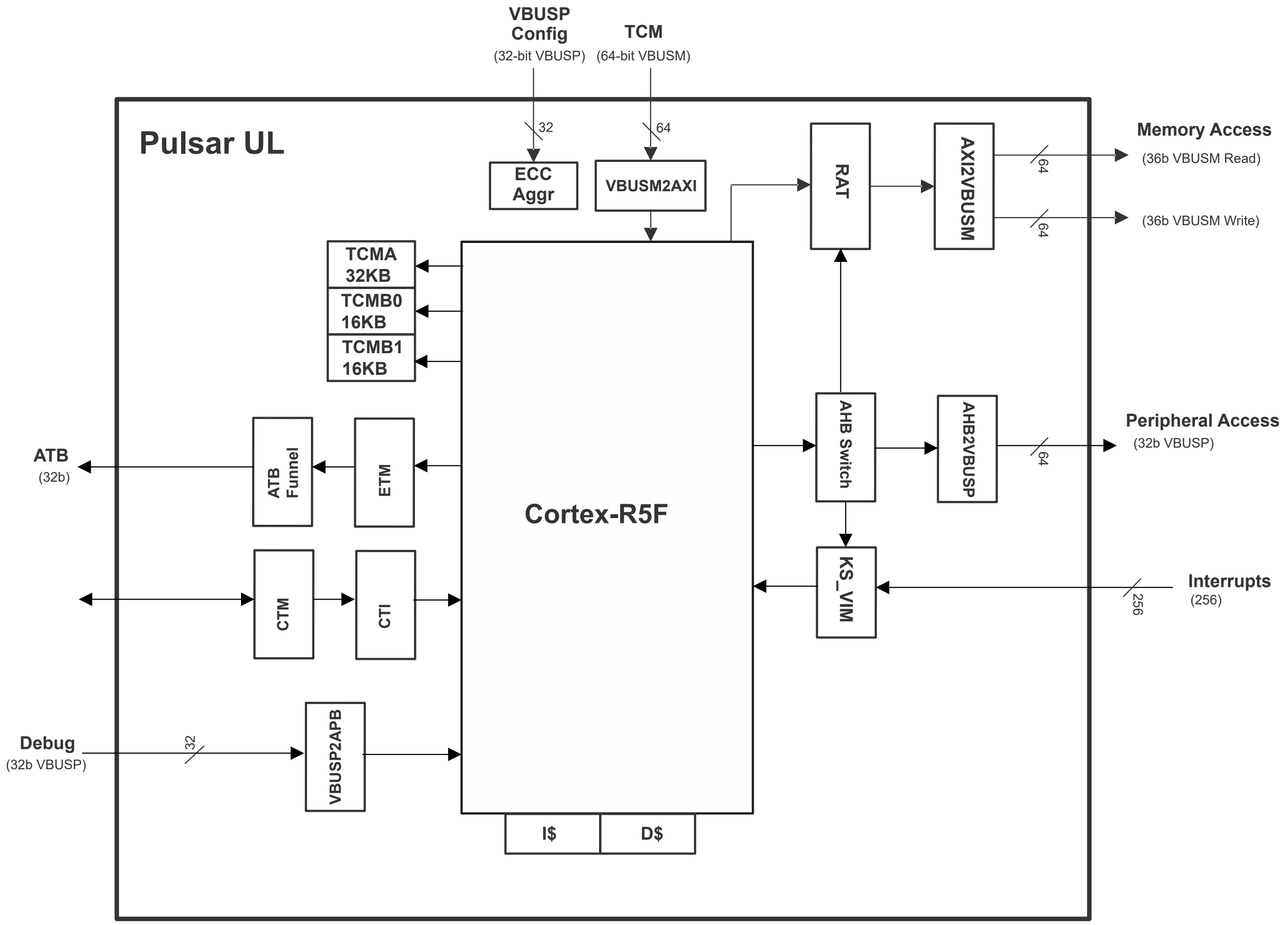

Figure 7-10. WKUP_R5FSS Block Diagram

7.3.2.2 WKUP_R5FSS Cortex-R5F Core

The Cortex-R5F is a processor from Arm, which is based on the Armv7-R profile.

For a brief list of features supported by the R5F processor in this device, see Section 7.3.1.1 . For more detailed description of this processor, see the *Arm Cortex-R5 Technical Reference Manual*.

7.3.2.2.1 L1 Caches

The R5F has a Harvard cache architecture, which means it has an independent L1 instruction cache (16KB) and L1 data cache (16KB). The instruction cache is protected by SECDED ECC per 64 bits. The data cache is protected by SECDED ECC per 32 bits.

7.3.2.2.2 Tightly-Coupled Memories (TCMs)

The R5F has two tightly-coupled memories (TCMs), ATCM and BTCM. The BTCM is further broken down into two interleaved banks, B0TCM and B1TCM.

TCMs are low-latency, tightly integrated memories for the R5F to use. Either TCM can be used for any combination of instruction and/or data. TCM performance is equal to performance on instructions/data that are in cache. However, TCMs have some additional advantages over cache. TCMs can be loaded with instructions that do not cache well (such as ISRs) or preloaded with code by an external source, before that code is needed, to save cache miss time. TCMs are also a good place for blocks of data for intense processing. They can be loaded (or pre-loaded by an external source) before the data is needed, saving cache miss time. The data can then be directly accessed by an external source, instead of needing to do cache evicts.

As mentioned, TCMs can be accessed (either read or written) by an external source over the TCM VBUSM target interface. This allows instructions or data to be preloaded, or for data to be read out after the R5F has processed it. The VBUSM target has a lower priority to accessing TCMs than the R5F but care must be taken to keep an external source from reading or writing TCM data that the R5F is working on. This handshaking is external to any of the R5FSS hardware.

TCMs are protected by ECC per 32 bits. For this to work, ECC must be enabled before data is written in to the TCMs (either externally or from the R5F). ECC is enabled via the following R5F system control bits: ACTLR.ATCMPCEN, ACTLR.B0TCMPCEN, and ACTLR.B1TCMPCEN, respectively.

Whether or not the TCMs are enabled is controlled by the ENABLE bit in the corresponding ATCM/BTCM region register. The default (reset) value of this bit is determined by the CPUn_INITRAMA and CPUn_INITRAMB bootstraps, respectively. Both ATCM and BTCM are configured for a size of 32KB in this device. Note that the BTCM size is the total of both B0TCM and B1TCM (16KB each).

If a TCM is not enabled, then it does not appear in the R5F’s memory view, but it can be accessed by an external source. If a TCM is enabled, then its place in the R5F memory map is determined by a combination of bootstrap signal and system register. If the CPUn_LOCZRAMA bootstrap signal is high, then the initial base address of ATCM is 0x0000_0000 and the initial address of BTCM is 20’h41010. If the CPUn_LOCZRAMA bootstrap signal is low, then the initial base address of BTCM is 0x0000_0000 and the initial base address of ATCM is 20’h41010.

Note

This base address of 0x41010 for ATCM/BTCM based on the CPUn_LOCZRAMA bootstrap only affects the R5F’s memory view. The SoC will see the ATCM/BTCM based on the TCM target interface regions, as defined in Section 7.3.2.3.2 . The base address of either TCM may be overwritten via the ATCM or BTCM region register. Care must be taken not to move the base address of a TCM when it may be being accessed.

It is possible to preload a TCM with instructions and boot from it. See Section 7.3.2.11 for details on TCM booting.

7.3.2.2.3 WKUP_R5FSS Special Signals

Table 7-26 lists some WKUP_R5FSS features associated with special signals.

Table 7-26. WKUP_R5FSS Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 0 (ID = 0x0)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x2FFF_0000
CPUn RAT base address	0x2FFE_0000
CPUn RAT accesses ID	0x4 (CPU0)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state

Table 7-26. WKUP_R5FSS Special Features (continued)

Feature	Comment
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_2000_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	64MB for MAIN peripherals (0x0_2000_0000 to 0x0_2FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Not used
CPUn VBUSM normal peripheral port size	Not used
CPUn VBUSM virtual peripheral port base address	Not used
CPUn VBUSM virtual peripheral port size	Not used
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

7.3.2.3 WKUP_R5FSS Interfaces

7.3.2.3.1 Initiator Interfaces

The WKUP_R5FSS has several initiator interfaces:

- 64-bit VBUSM initiator pair (1 read - "RMST", 1 write - "WMST") for L3 memory accesses; this is the main memory interface
  - Includes region-based address translation (RAT)
- 32-bit VBUSP initiator "PMST" for peripheral access
  - Includes logic that provides the R5F CPU with a private access to VIM and RAT
  - Enabled at reset

7.3.2.3.2 Target Interfaces

The WKUP_R5FSS has several target interfaces that define its internal memory space:

- 32-bit VBUSP configuration target
  - Region [0]: ECC aggregator block
- 64-bit TCM target
  - Region [0]: ATCM
  - Region [1]: BTCM
  - Region [2]: Instruction cache RAMs
  - Region [3]: Data cache RAMs
- 32-bit VBUSP debug target
  - Provides access to all R5FSS internal debug logic

Regions [0] and [1] of the TCM target interface provide direct access to the TCM RAMs. Access to the RAMs is arbitrated with access from the R5F’s L1 memory system. Excessive access while the R5F is also attempting access will degrade performance.

Regions [2] and [3] of the TCM target interface provide access to the cache RAMs for testing purposes. Access to the cache RAMs can only be done while the caches are disabled and should only be done for test purposes.

In addition to the target interfaces, there are peripherals (RAT and VIM) that are only accessible by the R5F. The R5F has an access to these modules via the VBUSP peripheral interface.

7.3.2.4 WKUP_R5FSS Power, Clocking and Reset

7.3.2.4.1 WKUP_R5FSS Power

The following WKUP_R5FSS power considerations should be noted:

- WKUP_R5FSS has a single power domain for all its internal logic

For more details on WKUP_R5FSS power management, including power-up and power-down sequences, see *Power*.

7.3.2.4.2 WKUP_R5FSS Clocking

The WKUP_R5FSS has four clock inputs:

- CPU0_CLK: This is the clock for CPU0 logic
- CPU0_ICLK: This is the clock for CPU0 interfaces

CPU0_CLK is the clock for all of the internal CPU logic, while CPU0_ICLK is the clock for all of the interfaces for their associated CPU (for example: VBUSM and VBUSP bridges, exception generation, debug and trace logic).

The interface clock is an integer ratio of the CPU clock. The exact ratio for this device is 1:1.

7.3.2.4.3 WKUP_R5FSS Reset

The R5FSS has two reset inputs:

- CPU0_RST: This is the reset for the non-debug logic of CPU0
- CPU0_DBG_RST: This resets the CPU0 debug logic, excluding the APB interface

In addition to the reset signals, there is one halt signal:

- CPU0_HALT

These halt signals keep the CPUs from fetching instructions when they come out of reset. The main use is to have the CPUs halted until the TCMs are loaded (when booting from TCM), though halt could be used for any other purpose.

7.3.2.5 WKUP_R5FSS Vectored Interrupt Manager (VIM)

7.3.2.5.1 VIM Overview

The VIM aggregates device interrupts and sends them to the R5F CPU. It can be used in either split or single-core configuration.

The VIM module supports the following features:

- 256 interrupt inputs for the R5F core
- Each interrupt has its own 4-bit programmable priority
  - Defined via the R5FSS_VIM_PRI_INT_j register
  - The VIM provides support for priority interruption of interrupts
- Each interrupt has its own enable mask
  - Interrupt enable is done via the R5FSS_VIM_INTR_EN_SET_j register
  - Interrupt disable is done via the R5FSS_VIM_INTR_EN_CLR_j register
- Each interrupt can be programmed as either an IRQ or FIQ
  - Defined via the R5FSS_VIM_INTMAP_j register
- Each interrupt has its own programmable 32-bit vector address associated with it
  - Defined via the R5FSS_VIM_VEC_INT_j register
  - Protected with SECDED
- One IRQn and one FIQn output per core
- Vectored interrupt interface
  - Compatible with R5F VIC port

- Default vector provided when a double-bit error is detected
- Software interrupt generation

7.3.2.5.2 VIM Interrupt Inputs

The VIM supports 256 interrupt inputs per core. Each interrupt can be either a level or a pulse (both active-high). The interrupt mapping for the R5F core can be found in *Interrupt Sources*.

7.3.2.5.3 VIM Interrupt Outputs

The VIM has two interrupt outputs per core:

- *CoreN_IRQn*: This is a normal interrupt for core *N* (active-low level). It can be serviced via the VIC interface or through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (via the R5FSS_VIM_INTMAP_j register) and is enabled (via the R5FSS_VIM_INTR_EN_SET_j register), then it will cause an IRQ to assert
- *CoreN_FIQn*: This is a fast (or non-maskable) interrupt for core *N* (active-low level). FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ and is enabled, then it will cause an FIQ to assert

7.3.2.5.4 VIM Interrupt Vector Table (VIM RAM)

For each VIM interrupt core, there is an associated interrupt vector table (VIM RAM) that is used to store the address of ISRs. During register vectored interrupt and hardware vectored interrupt, VIM accesses the interrupt vector table using the vector value to fetch the address of the corresponding ISR. Note that both interrupt vector tables are identical in their memory organization.

The VIM RAM is basically comprised of a set of interrupt vector registers (R5FSS_VIM_VEC_INT_j). Hence, the interrupt vector table is organized in 256 words of 30 bits, with a base address corresponding to the physical address of the first register in the group.

Note

The lower two bits of the 32-bit interrupt vector are always 0s.

Figure 7-11 shows the VIM RAM interrupt vector map.

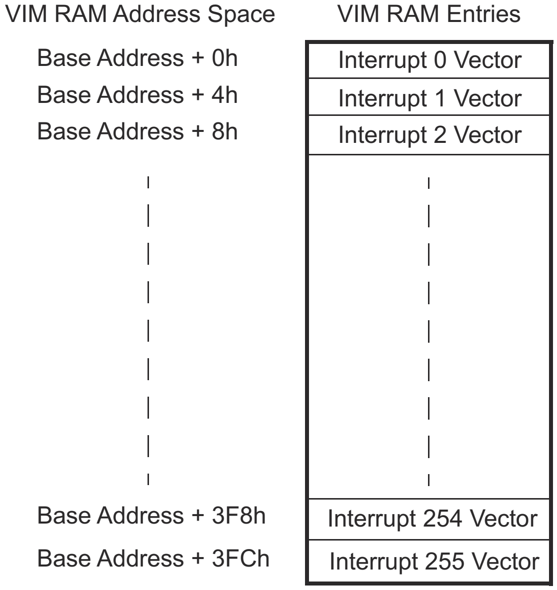

Figure 7-11. VIM RAM Interrupt Vector Map

The interrupt vector table has protection by ECC to indicate corruption due to soft errors. The ECC logic inside VIM supports SECDED. See Table 7-29 for the VIM RAM ID in the ECC aggregator map.

7.3.2.5.5 VIM Interrupt Prioritization

The VIM supports the interruption of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate but both use the same mechanism.

When an interrupt goes from pending to active (FIQ: reading the R5FSS_VIM_FIQVEC register; IRQ: reading the R5FSS_VIM_IRQVEC register, or the *coreN_IRQACK* going high), then the interrupt is loaded into the corresponding active register (R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ), and all interrupts of an equal or lesser priority are masked (discarded). If prior to this interrupt being cleared (by writing to the R5FSS_VIM_FIQVEC register, or R5FSS_VIM_IRQVEC register) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. If the CPU switches this interrupt to active (by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register), then the currently active interrupt will be pushed onto a stack. When an interrupt is cleared by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register, if there are any interrupts on the stack, the first entry is popped off and put back into the R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ register, so that software may continue where it left off.

7.3.2.5.6 VIM ECC Support

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the R5FSS_VIM_DEDVEC register is used to provide the default vector for the *coreN_IRQADDRV* signal, the R5FSS_VIM_IRQVEC register, and the R5FSS_VIM_FIQVEC register. The R5FSS_VIM_DEDVEC should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling.

Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
   a. Potentially switch to a completely software interrupt handler in the mean time
2. Restart the application from scratch
3. Reset the device
4. Sit in a loop (or WFI) while something external (for example, the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

Note

An interrupt that has an uncorrectable vector error (and thus uses the DED vector) will still have the priority of the original interrupt . This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by the R5FSS ECC aggregator.

7.3.2.5.7 VIM IDLE State

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface.

7.3.2.5.8 VIM Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM the software wants to take advantage of.

For IRQs, it is recommended to use the procedure in Section 7.3.2.5.8.1 , but the procedures in Section 7.3.2.5.8.2 or Section 7.3.2.5.8.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives.

For FIQs, it is recommended to use the procedure in Section 7.3.2.5.8.4 , but the procedure in Section 7.3.2.5.8.5 may be used as an alternative.

Note

These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

7.3.2.5.8.1 Servicing IRQ Through Vector Interface

If the associated CPU has the vector (VIC) interface enabled, then the following method is used for servicing IRQs:

1. Hardware handshake
   a. CPU asserts *coreN_IRQACK* high
   b. VIM asserts *coreN_IRQADDRV* to indicate that the *coreN_IRQADDR* bus is stable with the correct vector address
   c. CPU reads *coreN_IRQADDR*, jumps to that address, and de-asserts *coreN_IRQACK* low
   d. VIM de-asserts *coreN_IRQn* and *coreN_IRQADDRV*, VIM masks (discards) all IRQs with the same or lower priority
   e. VIM loads the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field (which corresponds to the vector address) into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, which causes the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTIRQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
   a. Pulse
      i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register
      ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt
4. Write any value to the R5FSS_VIM_IRQVEC register
   a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
   b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.3.2.5.8.2 Servicing IRQ Through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the vector interface:

1. Read the R5FSS_VIM_IRQVEC register and jump to that address to service the ISR
   a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_IRQn* output. If another interrupt of a higher priority becomes available, the *coreN_IRQn* will re-assert, allowing priority interruption of an interrupt
   b. Reading this register will cause the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, and the R5FSS_VIM_ACTIRQ[31] VALID bit to be set

2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        ii. Clear the interrupt at the source
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
4. Write any value to the R5FSS_VIM_IRQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.3.2.5.8.3 Servicing IRQ Through MMR Interface (Alternative)

If a user does not want to use the R5FSS_VIM_IRQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_IRQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    a. Read the R5FSS_VIM_PRIIRQ register to determine which interrupt is the highest priority IRQ currently asserted, OR
    b. Optionally read the R5FSS_VIM_IRQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_IRQSTS_j register and use a software prioritization scheme to determine which IRQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

7.3.2.5.8.4 Servicing FIQ

When an FIQ interrupt is received, the CPU should follow these steps:

1. Read the R5FSS_VIM_FIQVEC register and jump to that address to service the ISR
    a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_FIQn* output. If another interrupt of a higher priority becomes available, the *coreN_FIQn* will re-assert, allowing priority interruption of an interrupt.
    b. Reading this register will cause the value from the R5FSS_VIM_PRIFIQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTFIQ[9:0] NUM bit field, and the R5FSS_VIM_ACTFIQ[31] VALID bit to be set
2. Service the interrupt

3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTFIQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt
4. Write any value to the R5FSS_VIM_FIQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTFIQ[31] VALID bit

7.3.2.5.8.5 Servicing FIQ (Alternative)

If a user does not want to use the R5FSS_VIM_FIQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_FIQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    a. Read the R5FSS_VIM_FIQVEC register to determine which interrupt is the highest priority FIQ currently asserted, OR
    b. Optionally read the R5FSS_VIM_FIQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_FIQSTS_j register and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register.

7.3.2.6 WKUP_R5FSS Region Address Translation (RAT)

7.3.2.6.1 WKUP R5FSS Usage

R5 is a micro controller with 32b address, which is only able to access up to 4GB address space. However, Sitara™ SoC supports 36b address and majority of the memory region beyond lower 4GB are implemented. Region based address translation block, called RAT, is introduced to allow R5 core to access full 36b SoC memory map.

Each R5 core has its own RAT block, and only R5 core itself is able to program the RAT.

Figure 7-12 shows the main R5's default 32b memory map view when main R5 is out of reset.

The full RAT functionality is described in Section 7.2.2.6.2 , *RAT Function*.

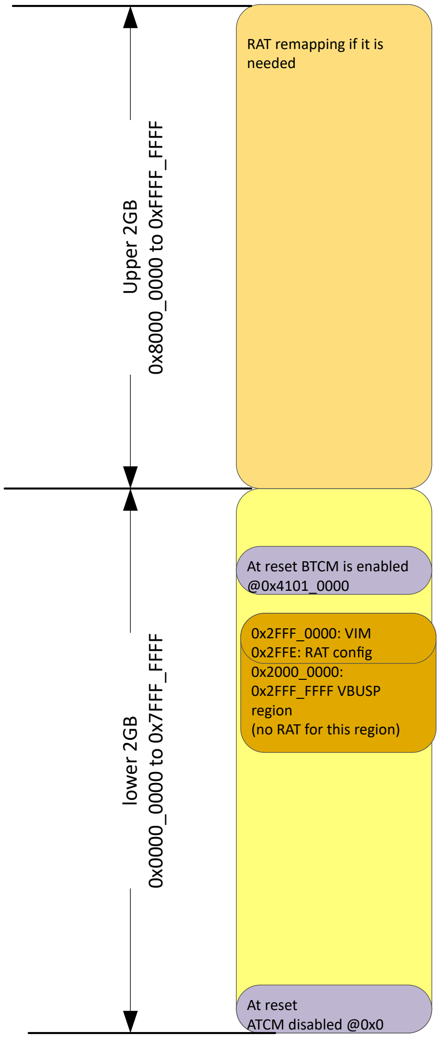

Figure 7-12. R5 Core Default Memory Map View

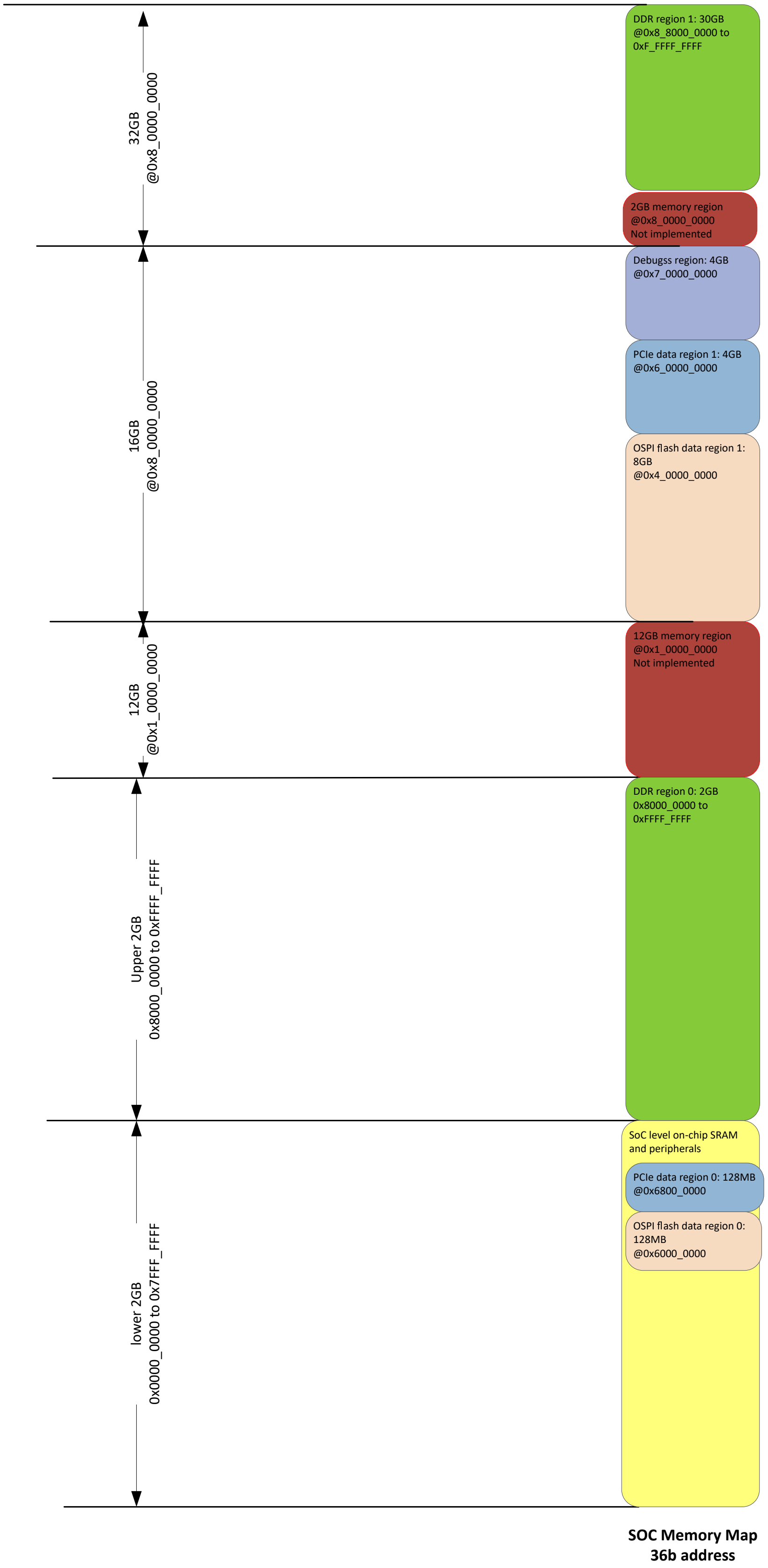

Figure 7-13. Typical Sitara SoC Memory Map View

RAT block enables R5 core to have full access on the SoC memory map including the memory region at and above 0x1_0000_0000.

Figure 7-14 shows how R5 access various end points, including its own ATCM, BTCM, VIM and SoC memory and peripherals. R5's ATCM is by default at address 0x0, and its BTCM is at address 0x4101_0000. R5 uses address 0x2FFF_0000 to access its VIM and 0x2FFE_0000 to access the RAT configuration region and all the other transactions between address range 0x2000_0000 to 0x2FFF_FFFF are sent to the 32b peripheral interface to access the peripherals in SoC. The transactions with the rest of address are sent to RAT block, which could go through address remapping function from original R5's 32b address to 36b SoC address.

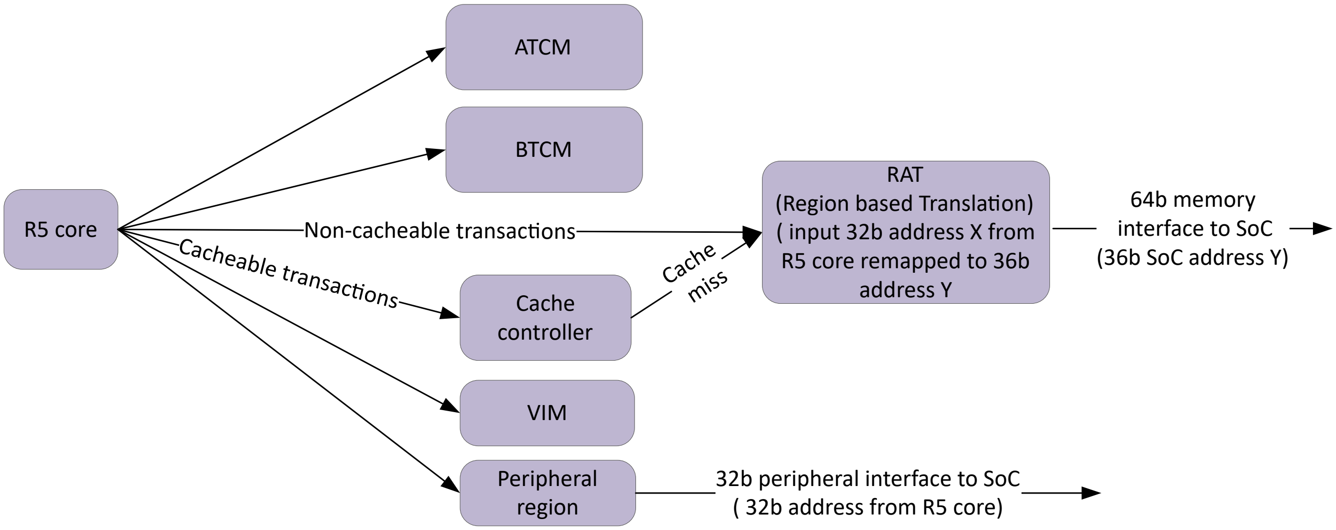

Figure 7-14. R5 Internal Address Decoding

7.3.2.6.2 RAT Function

RAT block is responsible to do a region based address translation. For each region, user can define the starting address and size of the region and remapping the transactions to use a new address range.

The starting address and region size need to be aligned. For example, if the region size is 16KB, the starting address for that region needs to be 16KB aligned. And region size should be minimum 4KB or larger to avoid transactions cross the region boundaries.

Each RAT block supports multiple programmable regions. And it is important that those regions are not overlapping with each other.

RAT block is by default disabled, which means RAT block does not do address remapping. The 32b address coming from R5 core is directly sent out to the SoC level. The user can program each RAT remapping region individually. For the transactions does not hit any remapping region, RAT block just simply forwards the transactions to the SoC level with its original address.

7.3.2.6.3 How to use RAT Block in R5

Table 7-27 shows the default R5 memory map view. Without enabling RAT function, all the regions beyond 4GB address space will not be accessible by R5.

Sitara™ SoC memory map is constructed the way to allow R5 and high level application processor such as A53 have similar memory map as possible. This methodology enables that R5 and ARM A53 core have a common memory map for all the SoC level memories and SoC level peripherals except a few exceptions:

- DDR's data space beyond 32b address, basically upper DDR data space beyond 2GB
- PCIe data space beyond 32b address
- OSPI data space beyond 32b address
- Debug configuration region

Table 7-27. R5 Memory map by Default

	R5 Memory Map(32b)	SoC Memory Map (36b)
SoC Level peripheral and on-chip SRAM	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF
2GB DDR region	Same as SoC memory map: 0x8000_0000 to 0xFFFF_FFFF	0x80000_0000 to 0xFFFF_FFFF
Additional DDR region	Not accessible	0x8_8000_0000 (30GB)
Additional 8GB OSP Space	Not accessible	0x4_0000_0000 (4GB) 0x5_0000_0000 (4GB)
Additional PCIe data space	Not accessible	0x6_000_0000
Debug configuration region	Not accessible	0x7_0000_0000

Even though all the transactions other than going to ATCM/BTCM and transactions between address range 0x2000_0000 to 0x2FFF_FFFF could use RAT block to remap to different address, it is recommended that only use RAT block to remap the R5 transactions with address between 0x8000_0000 to 0xFFFF_FFFF.

- Any transactions from R5 with address between 0x0 to 0x7FFF_FFFF are sent out to SoC directly (unless it is targeted to its internal end points such as A/B TCM, its VIM and RAT configuration)
- Only enable RAT to remap the transactions with address between 0x8000_0000 to 0xFFFF_FFFF if R5 needs to access the following address space:
  - PCIe data space at address 0x6_0000_0000
  - OSPI data space address 0x4_0000_0000 and 0x5_0000_0000
  - Debug configuration region at address 0x7_0000_0000
  - DDR data space at address 0x8_8000_0000

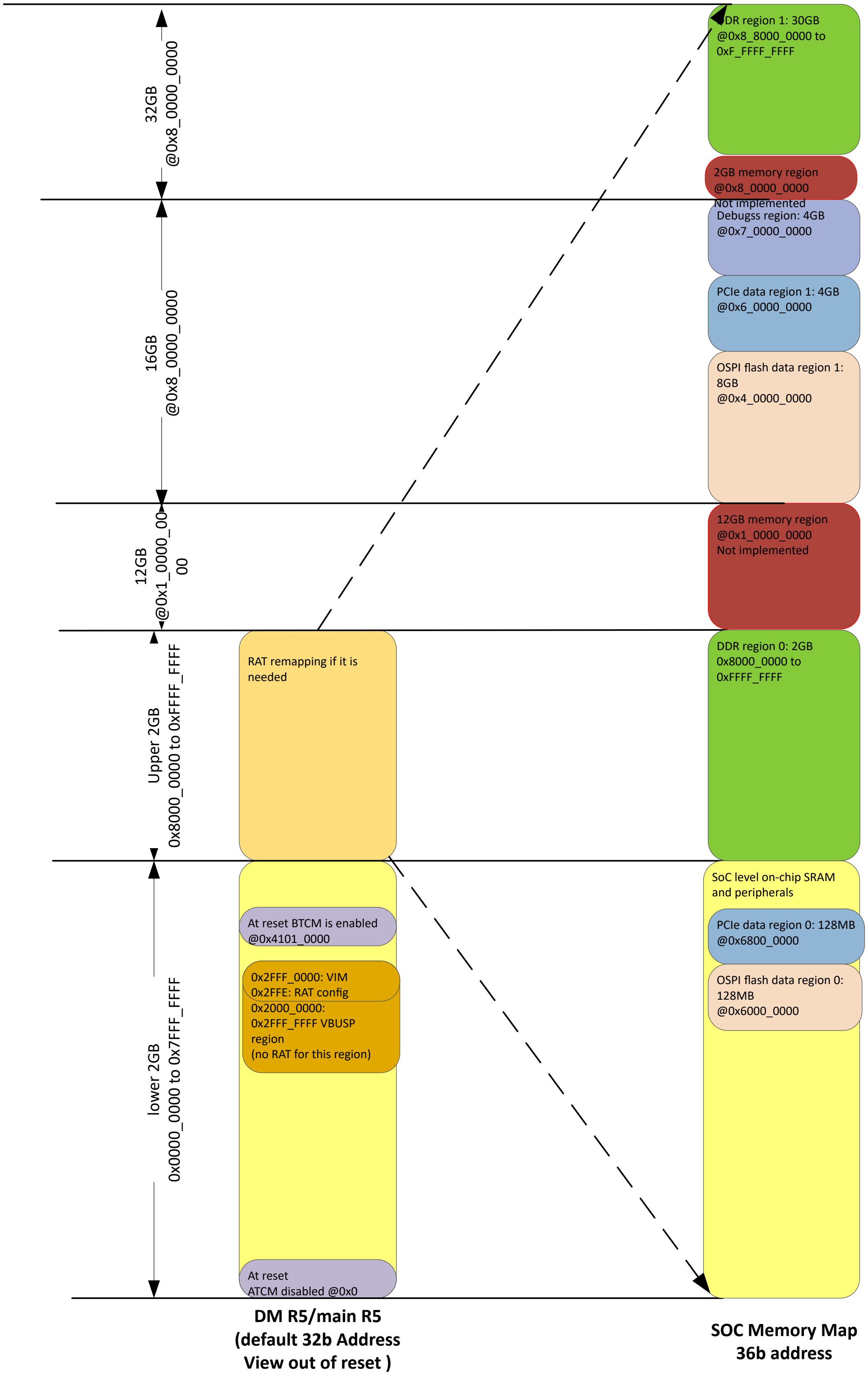

Figure 7-15. Example of Using RAT to Access Full 36b SoC Memory Map

7.3.2.6.4 Example of Using RAT to Access Full 36b SoC Memory Map

This section shows an example on how to utilize RAT block to allow R5 to access 36 SoC Memory Map. The RAT block inside R5 has up to 8 address remapping regions.

Assuming R5 needs to access the following region:

- All the SoC level on-chip SRAM
- All the SoC level peripherals
- Access 512MB OSPI region at address 0x4_0000_0000
- Access 1GB DDR region at address 0x9_0000_0000
- Access 512MB DDR region at address 0x8000_0000

First of all, we need to construct 32b R5 memory map as following and how those memory spaces are mapped to SoC level, shown in Table 7-28. Users can define where the OSPI and DDR data space placed inside R5's memory map and how they should be mapped to SoC level address map. Table 7-28 just shows one of the many possible ways to construct the memory map.

Table 7-28. Example of R5 Address Mapping

	R5 Memory Map(32b)	**SoC Memory Map (36b)**	**RAT Remapping**
SoC Level peripheral and on-chip SRAM (This is guaranteed by SoC Hardware design. No user configuration is needed)	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF	Not RAT Remapping
512MB OSPI data region (user defined)	0x8000_0000 to 0x9FFF_FFFF	0x4_0000_0000 to 0x4_1FFF_FFFF	Using RAT remapping region 0
512MB DDR space (user defined)	0xA000_0000 to 0xBFFF_FFFF	0x8000_0000 to 0x9FFF_FFFF	Using RAT remapping region 1
Additional 1GB DDR Space (user defined)	0xC000_0000 to 0xFFFF_FFFF	0x9_0000_0000 to 0x9_3FFF_FFFF	Using RAT remapping region 2

In this example, only three RAT regions are needed:

- Region 0 is used to remap R5's address between 0x8000_0000 to 0x9FFF_FFFF to SoC level address 0x4_0000_0000 to 0x4_1FFF_FFFF
- Region 1 is used to remap R5's address between 0xA000_0000 to 0xBFFF_FFFF to 0x8000_0000 to 0x9FFF_FFFF
- Region 2 is used to remap R5's address 0xc000_0000 t0 0xFFFF_FFFF to 0x9_0000_0000 to 0x9_3FFF_FFFF.

In order achieving those mappings, those are the setting of the RAT configuration registers:

	Region 0	**Region 1**	**Region 2**	**Other regions**
Region control register	Enabled, size set to 512MB	Enabled, size set to 512MB	Enabled, size set to 1GB	disabled
Region base(32b)	0x8000_0000	0xA000_0000	0xc000_0000	Don't care
Region translated lower address(32b)	0x0000_0000	0x8000_0000	0x0000_0000	Don't care
Region translated upper address	0x4	0x0	0x9	Don't care

Figure 7-16 shows how RAT is remapping the address between R5’s 32b address to 36b SoC address.

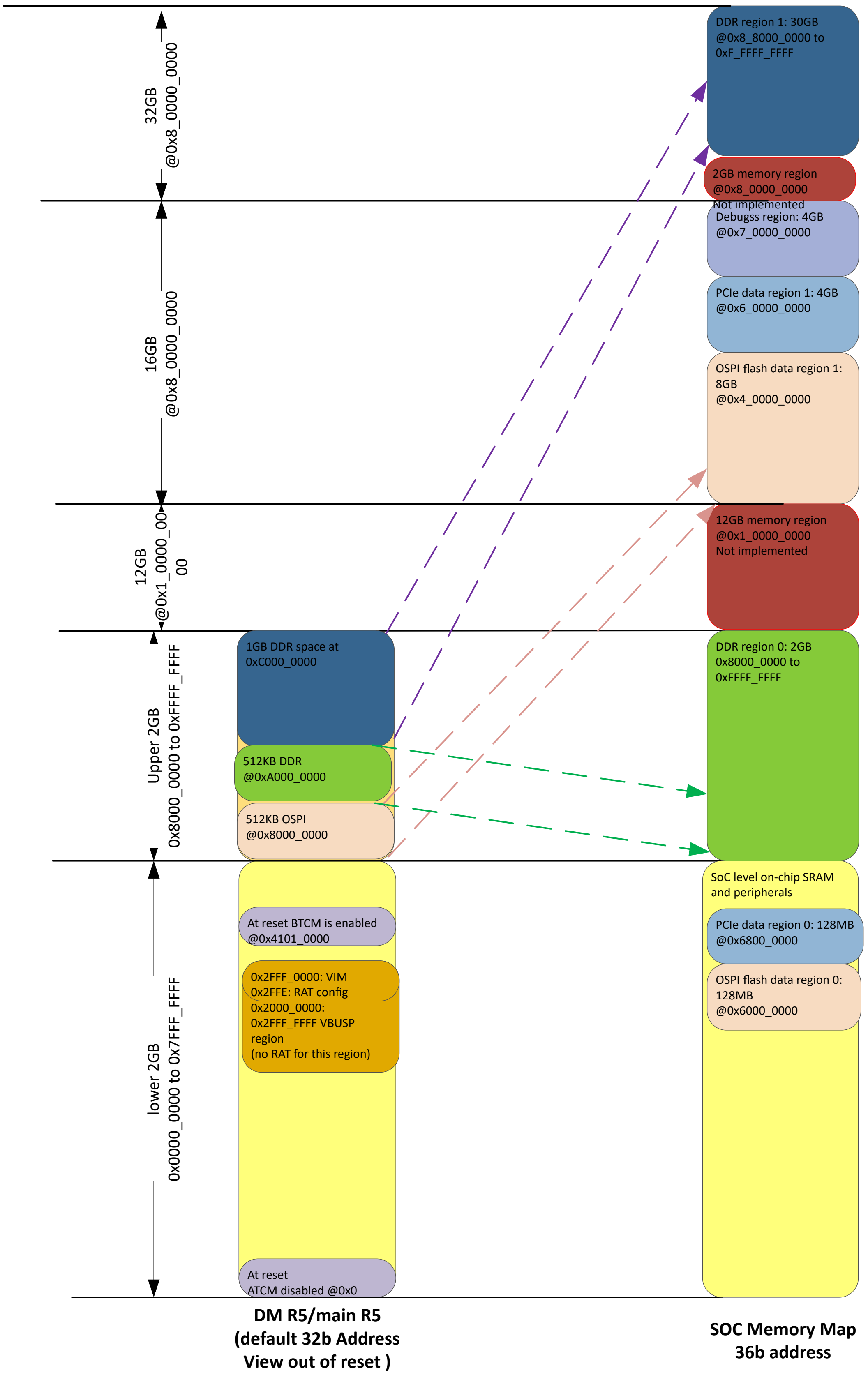

Figure 7-16. RAT Configuration Example

7.3.2.7 WKUP_R5FSS ECC Support

The R5F provides native ECC and parity support on all related memories, generating and checking the redundancy automatically. The R5F can also monitor any ECC errors on it's SoC buses and bridges through the ECC aggregator. The methods for checking and reporting errors are available in the *Arm Cortex-R5 Technical Reference Manual*.

The R5FSS adds the capability of testing this logic by allowing errors (single and double bit) to be injected into memories (for testing purposes) via an ECC aggregator (per core). Note that because the R5FSS ECC aggregator is only used in error-injection mode, it only supports a subset of the generic ECC aggregator functionality in the device.

For a detailed description of the generic ECC aggregator functionality, see *ECC Aggregator*. For register descriptions of the WKUP_R5FSS aggregators, see R5FSS_CPU0_ECC_AGGR_CFG_REGS Registers and R5FSS_CPU1_ECC_AGGR_CFG_REGS Registers, respectively.

Table 7-29 provides the RAM ID. This is needed for bit field [10-0] ECC_VECTOR in the corresponding R5FSS_CPU0_VECTOR**R5FSS_CPU0_VECTOR** register (part of the ECC aggregator register space).

Table 7-29. RAM ID Map for ECC Aggregator (Per Core)

RAM ID	Memory Name
0	CPU0 ITAG RAM0
1	CPU0 ITAG RAM1
2	CPU0 ITAG RAM2
3	CPU0 ITAG RAM3
4	CPU0 IDATA BANK0
5	CPU0 IDATA BANK1
6	CPU0 IDATA BANK2
7	CPU0 IDATA BANK3
8	CPU0 DTAG RAM0
9	CPU0 DTAG RAM1
10	CPU0 DTAG RAM2
11	CPU0 DTAG RAM3
12	CPU0 DDIRTY RAM
13	CPU0 DDATA RAM0
14	CPU0 DDATA RAM1
15	CPU0 DDATA RAM2
16	CPU0 DDATA RAM3
17	CPU0 DDATA RAM4
18	CPU0 DDATA RAM5
19	CPU0 DDATA RAM6
20	CPU0 DDATA RAM7
21	CPU0 ATCM BANK0
22	CPU0 ATCM BANK1
23	CPU0 B0TCM BANK0
24	CPU0 B0TCM BANK1
25	CPU0 B1TCM BANK0
26	CPU0 B1TCM BANK1
27	CPU0 VIM RAM

7.3.2.8 WKUP_R5FSS Memory View

The memory view of the R5F (that is, the memory map as seen by each R5F) is a function of several things:

- Exception vector bootstrap: The R5F exception table (including boot vector) is always 32 bytes at address 0x00000000 as seen by the R5F. If not booting from a TCM, then boot is done over the main memory interface. The exception vector bootstrap is under software control, which allows these 32 bytes at address 0x00000000 to be remapped somewhere else in the SoC memory map.
- TCM locations: TCMs can be enabled or disabled and located at different places in the memory map, depending on bootstrap configuration. For more details, see Section 7.3.2.2.2 .
- Peripheral interface locations: The RF5 natively supports three interfaces for peripheral access. Each can be enabled/disabled and located based on bootstrap configuration. Note that the VBUSP peripheral interface must be enabled in order to use RAT and VIM.
- RAT base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- VIM base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- RAT programming: The RAT can take regions of memory accessible by the main memory interface and map them to different addresses.

The combination of the above determines what the R5F sees where in the memory map, and over what interface different transactions come out. Every transaction that does not directly address a TCM or a peripheral interface comes over the main memory interface. Transactions on the main memory interface can be further remapped with the RAT.

See *Memory Map* for the complete R5F memory view for this device.

7.3.2.9 WKUP_R5FSS Interrupts

All interrupts that are generated by the WKUP_R5FSS are summarized in *Module Integration*, along with their mapping. They can be divided into the following groups:

- R5F CPU internal interrupts: These are described in *Arm Cortex-R5 Technical Reference Manual*.
- ECC aggregator interrupts: These are described in the *ECC Aggregator* chapter.
- RAT exception interrupt: This is described in Section 7.3.2.6 .

7.3.2.10 WKUP_R5FSS Debug and Trace

The WKUP_R5FSS supports standard Arm CoreSight debug and trace architecture. For more details, see the *On-chip Debug* chapter.

7.3.2.11 WKUP_R5FSS Boot Options

There are two methods of booting the R5F, or rather, two methods of placing the exception vectors (of which the boot vector is one).

The first method is to have the exception vectors external to the R5F. The user can place the exception vectors at the address indicated by the exception vector bootstrap and then program the boot vector there. When the processor exits reset, it will fetch the boot vector from this location.

The second method is to boot from a TCM. To do this, software should take the following steps:

1. Assert the correct bootstraps
    a. To boot from ATCM, set CPUn_INITRAMA (or CPUn_INITRAMB to boot from BTCM)
    b. Assert CPUn_LOCZRAMA properly for the desired TCM
2. Assert CPUn_HALT
3. Release the CPU from reset
4. Load the desired code into the TCM via the TCM target port
    a. Exception vectors should be located at address 0x00000000 of the TCM
5. De-assert CPUn_HALT

7.3.2.12 WKUP_R5FSS Core Memory ECC Events

The R5F core generates several events as part of event bus that can be monitored by the PMU for debugging. The memory ECC related events from the event bus are exported to ESM for monitoring.

There are two ECC interrupts to the ESM that aggregate different categories of ECC events – CPU single error, CPU multi error. Each ECC event has a 2-bit event bus counter associated with it. Everytime an event occurs, the counter is incremented by 1 till it reaches the max value of 3. The interrupt is asserted if the bus counter of any event associated with the interrupt is non-zero.

Each event bus counter has a MMR decrement control to decrement the counter by 1. So, for example, if a counter value is 2, the MMR to decrement the counter would need to be written 2 times to decrement the counter to 0. The reason decrement control has been added instead of clear control is if a new error occurs between the time the status register is read and the clear MMR is written, the new error would be lost. Write-to-decrement ensures that this does not happen.

When all event bus counters of an associated interrupt are zero, the interrupt is cleared. It takes three clock cycles for the event bus counter to be decremented once the write to the decrement control MMR presents itself at the WKUP_R5FSS boundary.

Since each of the four ECC interrupts have single bit control to set the interrupt but multiple bits for clearing it, note that once an interrupt is set using the R5FSS_EVNT_BUS_ESM_SET register, it can be cleared by setting all the bits of the R5FSS_EVNT_BUS_ESM_CLR register that correspond to that particular interrupt. For example, if bit [0] of the R5FSS_EVNT_BUS_ESM_SET register is set, it can be cleared by setting bits [7-0] of the R5FSS_EVNT_BUS_ESM_CLR register to clear the interrupt.

The R5F core event bus only signals event when it is enabled. Non-invasive or invasive debug mode needs to be enabled to enable the PMU counters.

The export of the events to the event bus can be enabled by setting the X bit in the Performance Monitor Control Register of the R5F core. For more details, refer to Arm R5 TRM.

Table 7-30. R5F Event Bus Single-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
22	Instruction cache tag RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0
23	Instruction cache data RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1
24	Data cache tag or dirty RAM parity error or correctable ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2
25	Data cache data RAM parity error or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3
40	ATCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4
41	B0TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5
42	B1TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6
43	TCM correctable ECC error reported by load/store unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7
44	TCM correctable ECC error reported by prefetch unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8

Table 7-31. R5F Event Bus Multi-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
26	TCM fatal ECC error reported from the prefetch unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0

Table 7-31. R5F Event Bus Multi-Bit Error Events (continued)

Event Bus Bit #	Description	Associated Status Register
27	TCM fatal ECC error reported from the load/ store unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1
33	Data cache data RAM fatal ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2
34	Data caches tag/dirty RAM fatal ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3
37	ATCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4
38	B0TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5
39	B1TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6

7.3.3 Vectored Interrupt Manager (VIM)

This section describes the VIM module in the device.

7.3.3.1 VIM Overview

The Vectored Interrupt Manager (VIM) aggregates interrupts to a CPU. It is intended for use with a Cortex R5 from ARM. The VIM has up to 1024 interrupt inputs, which may be either level or pulse. Each interrupt has a programmable priority (0-highestthrough 15-lowest). Each interrupt may also be mapped as an IRQ or FIQ (FIQ is also often denoted as Non-Maskable Interrupt, or NMI).

7.3.3.1.1 VIM Features

- 32-1024 Interrupt inputs
  - Configurable by groups of 32
- Each interrupt has its own 4-bit programmable priority
  - Supports Priority interruption of interrupts
- Each interrupt has its own enable mask
- Each interrupt can be programmed as either an IRQ or FIQ
- Each interrupt has its own programmable 32-bit Vector address associated with it
  - Protected with SECDED
- One IRQn and FIQn output
- Vectored Interrupt Interface
  - Compatible with ARM Cortex R5 VIC Port
- Default Vector provided when a Double-Bit error is detected
- Provides clock phase inputs so VIM can run at CPU clock while interface runs at a different, synchronous clock

7.3.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

7.3.3.2 VIM Functional Description

7.3.3.2.1 Block Diagram

Figure 7-17 shows the Vectored Interrupt Manager block diagram.

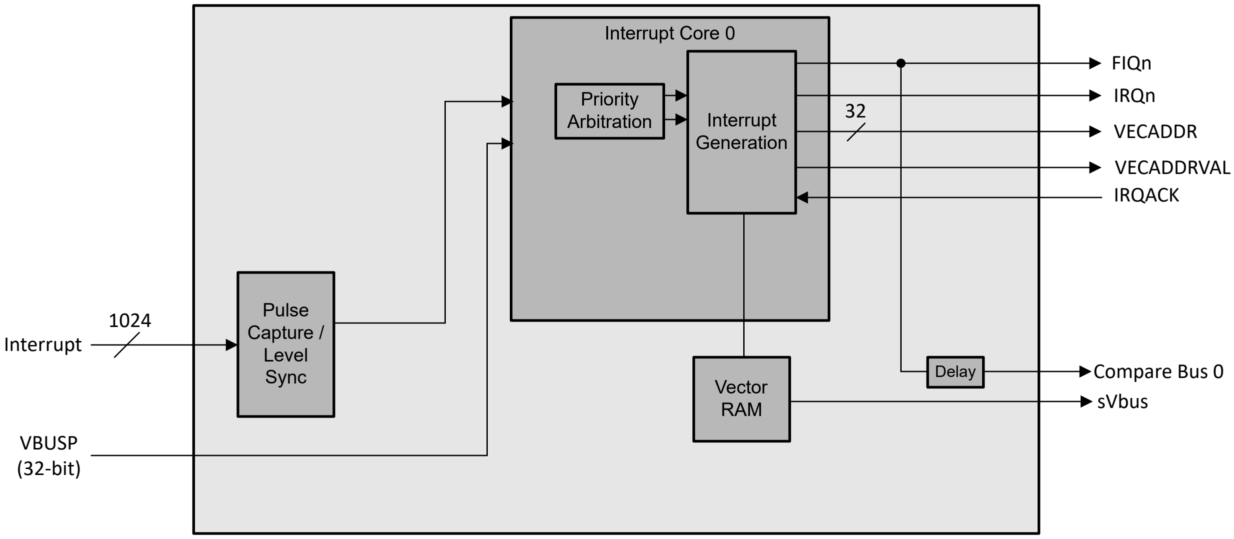

Figure 7-17. VIM Block Diagram

7.3.3.2.2 Interrupt Inputs

The VIM can have up to 1024 interrupt inputs, build-time configurable by multiples of 32 (*num_interrupts* parameter). Each interrupt can be either a level or a pulse (both active high).

Level interrupts are synchronized to the VIM clock. This synchronized value is captured in to a flop.

Pulse interrupts use rising edge detection. Each input has its own edge detection circuit. It is recommended that if pulses are pipelined between the source and the VIM, that the pipe stage replicates the pipe flop and ORs the output in order to protect against transient errors in the pipeline flop. Once an edge has been detected, the raw status is set.

There is no minimum pulse width, as true edge detection is used. The input signal should, however, be glitch free.

7.3.3.2.3 Interrupt Outputs

The VIM has two interrupt outputs, core*N*_IRQn and core*N*_FIQn (active low levels). Each interrupt input for core *N* can be programmed to influence either the core*N*_IRQn or core*N*_FIQn output via the Group *M* Interrupt Map Register (Base Address + 0x200 + *N**0x20 + 0x18).

7.3.3.2.4 Priority Interrupt / Nested Interrupts

Each interrupt has a priority number assigned to it (set using the 4.1.20 Interrupt *Q* Priority Register (Base Address + 0x1000 + *Q**0x4) register). Legal values are 0 to 15 where 0 is the highest priority and 15 is the lowest priority. The highest priority interrupt is the pending interrupt with the smallest priority number. If two pending interrupts have the same priority, the interrupt lowest numerically (0 through maximum number of interrupts) is prioritized. IRQs and FIQs are prioritized separately.

The VIM supports the interrupt of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate, but both use the same mechanism. When an interrupt goes from pending to active (FIQ: reading the FIQ Vector Address (Base Address + 0x1C), IRQ: reading the IRQ Vector Address (Base Address + 0x18) or the core*N*_IRQACK going high), then the interrupt is loaded into the corresponding Active Register, and all interrupts of an equal or lesser priority are masked off (see note below). If, before this interrupt is cleared (writing the FIQ Vector Address (Base Address + 0x1C) or IRQ Vector Address (Base Address + 0x18)) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. The CPU may or may not service the higher priority interrupt. If the CPU switches this interrupt to active, by reading the corresponding Vector Address Register (or core*N*_IRQACK going high for an IRQ) , then the currently active interrupt will be pushed on to a stack. When an interrupt is cleared by writing the Vector Address Register, if there are any interrupts on the stack, the first entry is popped off and put back into the Active

Register, so that software may continue where it left off. Note that the IRQVEC/FIQVEC address registers are *not* repopulated with the old vector as it's assumed that the ISR is picking back up where it left off. Only the interrupt number and priority are restored to the ACTIRQ/ACTFIQ registers. If software needs the vector again, it will have to read it by using the interrupt number.

Note

"Masked off" means that they are masked off from priority arbitration to interrupt the currently active interrupt, it does NOT mean that the status bits in the regsiters are masked off. That is, this priority masking has NO EFFECT on whether the status bits are visible in the masked registers such as the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04).

7.3.3.2.5 VIC Port

The VIM is designed to work with the VIC interface of an ARM Cortex R5.

7.3.3.2.6 Latency

There are several factors that go in to the speed of processing an interrupt: the interrupt controller, the processor, and the system latency.

The VIM behaves deterministically (except for synchronizer delay). Table 7-32 shows the latency of the VIM.

Table 7-32. VIM Latency

Step	Cycles	Note
Edge Detection	2-3	Synchronizing to VIM Clock
Interrupt Capture	1	
Prioritization and Vector Read	1	IRQ Could be stalled here if an FIQ is reading the Vector RAM
		IRQ/FIQ output asserted

The next factor is the processor itself

Table 7-33. Processor Interrupt Latency

Step	Cycles(1)	Note
Take Exception		
Store State		Stack system registers etc
Read Vector	1	Through MMR or VIC interface (for IRQ. VIC interface will be faster)
Jump to Vector		

(1) These steps are dependent on the processor. See R5 spec for details.

The final factor is system latency to access the actually instructions for the ISR. This will be dependent on where the instructions are (cache, TCM, system memory etc) and dependent on the system latency to reach those memories (1 cycle for cache/TCM, System dependent for external memory)

7.3.3.2.7 Safety

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the DED Vector Address (Base Address + 0x30) is used instead for the core*N*_IRQADDRV, IRQ Vector Address (Base Address + 0x18), and FIQ Vector Address (Base Address + 0x1C). The DED Vector Address should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling. Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
    a. Potentially switch to a completely software interrupt handler in the mean time
2. Restart the application from scratch

3. Reset the device
4. Sit in a loop (or WFI) while something external (say the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

An interrupt that has an uncorrectable vector error and thus uses the DED Vector, will still have the priority of the original interrupt (that is for masking purposes). This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by an external ECC aggregator through sVbus ports.

7.3.3.2.8 IDLE

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface because it does not have a clock IPG. To clock stop the sub-system that includes the VIM, disable (mask) all interrupts and wait for the IDLE signal to assert.

7.3.3.3 Interrupt Conditions

7.3.3.3.1 CPU Interrupts

See Table 7-34 for the interrupts generated by the module.

Table 7-34. Interrupts

Interrupt	Description
core0_IRQn	IRQ Interrupt (Active Low)
core0_FIQn	FIQ Interrupt (Active Low)

7.3.3.3.2 Interrupt Description

7.3.3.3.2.1 coreN_IRQn

This is a normal interrupt, active low level, for Core N. It can be serviced via the VIC interface or through the MMR interface.

7.3.3.3.2.2 coreN_FIQn

This is a fast (or non-maskable) interrupt, active low level, for Core N. FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface.

7.3.3.3.3 Interrupt Condition Control

7.3.3.3.3.1 coreN_IRQn

Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (Group *N* Interrupt Map Register (Base Address + 0x200 + N*0x20 + 0x18)) and is enabled (Group *N* Interrupt Enabled Set Register (Base Address + 0x200 + N*0x20 + 0x08)), and its priority is not masked (4.1.11 IRQ Priority Mask Register (Base Address + 0x28), and it is not masked because of nested interrupt priority masking (2.2.5 Priority Interrupt / Nested Interrupts), then it will cause an IRQ to assert.

7.3.3.3.3.2 coreN_FIQn

Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ (Group *N* Interrupt Map Register (Base Address + 0x200 + N*0x20 + 0x18)) and is enabled (Group *N* Interrupt Enabled Set Register (Base Address + 0x200 + N*0x20 + 0x08)), and its priority is not masked (4.1.12 FIQ Priority Mask Register (Base Address + 0x2C)), and it is not masked because of nested interrupt priority masking (2.2.5 Priority Interrupt / Nested Interrupts), then it will cause an FIQ to assert.

7.3.3.3.4 Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM software wants to take advantage of. For IRQs, it is recommended to use 3.4.1 IRQ through the Vector

Interface, but 3.4.2 or 3.4.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives. For FIQs, it is recommended to use 3.4.4 FIQ, but 3.4.5 may be used as an alternative.

> **Note**
>
> These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

7.3.3.3.4.1 IRQ through the Vector Interface

If the attached CPU has the Vector Interface enabled, then the following method is used for servicing IRQs

1. Hardware handshake
   a. CPU asserts coreN_IRQACK signal high
   b. VIM asserts coreN_IRQADDRV to indicate that the coreN_IRQADDR bus is stable with the correct Vector Address
   c. CPU reads the coreN_IRQADDR, jumps to that address, and de-asserts coreN_IRQACK signal low
   d. VIM de-asserts coreN_IRQn_intr and coreN_IRQADDRV, VIM masks all IRQs with the same or lower priority
   e. VIM loads the value from the Prioritized IRQ (Base Address + 0x08) (which corresponds to the vector address) to be loaded into the Active IRQ (Base Address + 0x20) and the valid bit to be set
2. Service an interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active IRQ (Base Address + 0x20) to determine number and reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group M Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group M Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group M Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group M Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

4. 4. Write any value to the IRQ Vector Address (Base Address + 0x18)
   a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
   b. This will clear the valid bit of the Active IRQ (Base Address + 0x20)

7.3.3.3.4.2 IRQ through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the Vector Interface.

1. Read the IRQ Vector Address (Base Address + 0x18) and jump to that address to service the ISR

    a. Reading this register will mask all interrupts of an equal or lower priority and de-assert the IRQn output. If another interrupt of a higher priority becomes available, the IRQn will re-assert, allowing priority interruption of an interrupt.
    b. Reading this register will cause the value from the Prioritized IRQ (Base Address + 0x08) (which corresponds to the vector address) to be loaded into the Active IRQ (Base Address + 0x20) and the valid bit to be set

2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active IRQ (Base Address + 0x20) to determine number and reading the Group M Type Map Register (Base Address + 0x200 + M*0x20 + 0x1C) to determine type)
    a. Pulse
        i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
        ii. Clear the interrupt at the source
            1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
            1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
            2. If the source maintains the level, then it means there is another interrupt
4. Write any value to the IRQ Vector Address (Base Address + 0x18)
    a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
    b. This will clear the valid bit of the Active IRQ (Base Address + 0x20)

7.3.3.3.4.3 IRQ through MMR Interface (Alternative)

If a user does not want to use the Vector Address registers, the VIM may be used as a more traditional interrupt controller. Note that in this mode, priority masking will not work if route 1b is used (below) as the hardware prioritization may not match the software prioritization scheme. In this case, software would be responsible for doing all priority operations

1. Determine which interrupt to service
    a. Read the Prioritized IRQ (Base Address + 0x08) to determine which interrupt is the highest priority IRQ currently asserted OR
    b. Optionally read the IRQ Group Status (Base Address + 0x10) to determine which groups have IRQs pending, then read the Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10) and use a software prioritization scheme to determine which IRQ to service
2. Service the interrupt
3. Read the IRQ Vector Address (Base Address + 0x18)
    a. Note, this step can be done any time before step 4
    b. Value is ignored
4. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)

   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt IRQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x10)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

5. Write any value to the IRQ Vector Address (Base Address + 0x18)

7.3.3.3.4.4 FIQ

When an FIQ interrupt is received, the CPU should follow these steps.

1. Read the FIQ Vector Address (Base Address + 0x1C) and jump to that address to service the ISR
   a. Reading this register will mask all interrupts of an equal or lower priority and de-assert the FIQn output. If another interrupt of a higher priority becomes available, the FIQn will re-assert, allowing priority interruption of an interrupt.
   b. Reading this register will cause the value from the Prioritized FIQ (Base Address + 0x0C) (which corresponds to the vector address) to be loaded into the Active FIQ (Base Address + 0x24) and the valid bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Active FIQ (Base Address + 0x24) to determine number and reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

4. Write any value to the FIQ Vector Address (Base Address + 0x1C)

   a. This will clear the priority mask and all interrupts to be re-evaluated for the new highest priority interrupt.
   b. This will clear the valid bit of the Active FIQ (Base Address + 0x24)

7.3.3.3.4.5 FIQ (Alternative)

If a user does not want to use the Vector Address registers, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the FIQ Vector Address (Base Address + 0x1C) is never read). Software would be responsible for doing all priority operations

1. Determine which interrupt to service
   a. Read the Prioritized FIQ (Base Address + 0x0C) to determine which interrupt is the highest priority FIQ currently asserted OR
   b. Optionally read the FIQ Group Status (Base Address + 0x14) to determine which groups have IRQs pending, then read the Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14) and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (Determined by reading the Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C) to determine type)
   a. Pulse
      i. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
      ii. Clear the interrupt at the source
         1. This way, the source can generate another pulse if it needs to and the VIM will process this as a new interrupt

   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a 1 to the appropriate bit in the Group *M* Interrupt Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x04) or Group *M* Interrupt FIQ Enabled Status/Clear Register (Base Address + 0x400 + *M**0x20 + 0x14)
         1. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt
         2. If the source maintains the level, then it means there is another interrupt

7.3.3.4 Memory Map

Each Interrupt Core (*N* = 0) has its own MMR interface with its own independent memory map

Table 7-35. Core *N* Memory Map

Address Offset	Register
0x00	Revision Register
0x04	Info Register
0x08	Prioritized IRQ
0x0C	Prioritized FIQ
0x10	IRQ Group Status
0x14	FIQ Group Status
0x18	IRQ Vector Address
0x1C	FIQ Vector Address
0x20	Active IRQ
0x24	Active FIQ
0x28-0x2F	*Reserved*

Table 7-35. Core *N* Memory Map (continued)

Address Offset	Register
0x30	DED Vector Address
0x34-0x1FF	*Reserved*
0x400 + *M**0x20 + 0x00	Group *M* Interrupt Raw Status/Set Register
0x400 + *M**0x20 + 0x04	Group *M* Interrupt Enabled Status/Clear Register
0x400 + *M**0x20 + 0x08	Group *M* Interrupt Enabled Set Register
0x400 + *M**0x20 + 0x0C	Group *M* Interrupt Enabled Clear Register
0x400 + *M**0x20 + 0x10	Group *M* Interrupt IRQ Enabled Status/Clear Register
0x400 + *M**0x20 + 0x14	Group *M* Interrupt FIQ Enabled Status/Clear Register
0x400 + *M**0x20 + 0x18	Group *M* Interrupt Map Register
0x400 + *M**0x20 + 0x1C	Group *M* Type Map Register
0x1000 + *Q**0x4 – 00x1FFF	Interrupt *Q* Priority Register
0x2000 + *Q**0x4 – 0x2FFF	Interrupt *Q* Vector Register

There are *M* interrupt groups (0 through *num_groups*-1) with 32 interrupts per group.

There are *Q* interrupt inputs where *Q* = *M* * 32.

Accesses to the Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4) must be word-aligned, 32-bit accesses. Any write received with no bytes enabled will be ignored. Any writes receive with all bytes enabled will be executed. Any other write will not execute and will return an error status of Addressing Error.

7.3.3.5 Module I/O

7.3.3.5.1 Clocks, Reset, Emulation

Table 7-36. Clocks, Reset, Emulation

Pin Name	Type	Function
core0_clk	In	Clock for Core 0
core0_phase	In	Phase Indicator for Core 0
core0_srst_n	In	Sync Module Reset for Core 0
core0_arst_n	In	Async Module Reset for Core 0
core0_clkstop_idle	Out	Clock Stop Idle

7.3.3.5.2 VBUSP Target Interface

(N=0). Core0 interface is used for interrupt core 0.

Table 7-37. VBUSP Target Interface

Pin Name	Type	Function
core*N*_cfg_req	In	Request
core*N*_cfg_address[13:0]	In	Address (byte address)
core*N*_cfg_dir	In	Direction (read or write)
core*N*_cfg_xcnt[2:0]	In	Transaction Count
core*N*_cfg_byten[3:0]	In	Byte enables
core*N*_cfg_wdata[31:0]	In	Write data
core*N*_cfg_rdatap[31:0]	Out	Read data
core*N*_cfg_rready	Out	Read ready
core*N*_cfg_wready	Out	Write ready
core*N*_cfg_rstatus[2:0]	Out	Read Status

Table 7-37. VBUSP Target Interface (continued)

Pin Name	Type	Function
core*N*_cfg_emudbg	In	Emulation Debug

7.3.3.5.3 Interrupt Inputs

Core0 interface is used for interrupt core 0.

Table 7-38. Interrupt Inputs

Pin Name	Type	Function
core0_in_intr[Q-1:0]	In	Core 0 Interrupt Inputs

7.3.3.5.4 Interrupt Outputs

Table 7-39. Interrupt Outputs

Pin Name	Type	Function
core0_IRQn_intr	Out	IRQ Interrupt for core 0– Active Low Level
core0_FIQn_intr	Out	FIQ Interrupt for core 0 – Active Low Level

7.3.3.5.5 VIC Interfaces

(*N*=0). Core0 interface is used for interrupt core 0.

Table 7-40. VIC Interfaces

Pin Name	Type	Function
core*N*_vic_IRQADDRV	Out	IRQ Address Valid
core*N*_vic_IRQADDR[31:2]	Out	IRQ Address
core*N*_vic_IRQACK	In	Interrupt Acknowledge

7.3.3.5.6 Compare Outputs

These pins will never be on an isolation boundary and therefore their isolation values are don't-care. *Y* is dependent on the configuration

Table 7-41. Compare Outputs

Pin Name	Type	Function
core0_compare_bus[*Y*:0]	Out	Comparison Bus for Core0 to CCMR5

7.3.3.5.7 ECC Control and Status Bus

(*N*=0). Core0 interface is used for interrupts for core 0.

Table 7-42. ECC Control and Status Bus

Signal Name	Dir	Default Val	Description
core*N*_ramecc_strb	In	1'b0	Strobe to sample the incoming serial data
core*N*_ramecc_txd	In	1'b0	Output serial data
core*N*_ramecc_rxd	Out	1'b0	Input serial data
core*N*_ramecc_pend[1:0]	Out	2'd0	Level Interrupt source

7.3.3.5.8 DFT

Table 7-43. DFT

Signal Name	Dir	Default Val	Description
dft_clk_force_en	In	1'b0	DFT Clock Force Enable
dft_partition_enn	In	1'b0	DFT Clock Partition Enable
dft_scan_en	In	1'b0	DFT Scan Enable

Table 7-43. DFT (continued)

Signal Name	Dir	Default Val	Description
dft_async_rst_sel	In	1'b0	DFT Async Reset Select
dft_test_async_rst_n	In	1'b0	DFT Async Test Reset
dft_tft_mcp_dis	In	1'b0	DFT MCP Disable
dft_local_clk_en	In	1'b0	DFT Local Clock Enable

7.3.3.5.9 RAM GPIO

Table 7-44. RAM GPIO

Signal Name	Dir	Default Val	Description
core*N*_ramdft_gpi[255:0]	In	256'd0	RAM GPI
core*N*_ramdft_gpo[255:0]	Out	256'd0	RAM GPO

7.3.3.6 Programmer's Guide

7.3.3.6.1 Initialization Sequence

At initialization, the following tasks should be performed:

1. Program the DED Vector Address (Base Address + 0x30)
2. Program Group *M* Interrupt Map Register (Base Address + 0x200 + *M**0x20 + 0x18)
3. Program Group *M* Type Map Register (Base Address + 0x200 + *M**0x20 + 0x1C)
4. Program Interrupt *Q* Priority Register (Base Address + 0x1000 + *Q**0x4)
5. Program Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4)
6. Enable interrupts via the Group *M* Interrupt Enabled Set Register (Base Address + 0x400 + *M**0x20 + 0x08)

Note that the Interrupt *Q* Vector Register (Base Address + 0x2000 + *Q**0x4) for each interrupt that will be enabled must be written before the interrupt is enabled, even if software is not going to use the vector. Whenever an interrupt is prioritized, the RAM location for the interrupt is read, and if that location is un-initialized, an ECC error will be reported. If the vectors aren't being used, then the RAM can be initialized by writing 0x0 to every location.

7.3.3.6.2 DED Behavior

Whenever there is 2-bit error detect on a Vector Address, the DED Vector Address (Base Address + 0x30) overrides all other vectors. Software should provide an ISR to handle this scenario at this address.

7.3.3.6.3 Power Up/Down Sequence

Before a clean power down, software should check that there are no pending interrupts, disable all interrupts, and wait for the clkstop_idle output.

Chapter 8

Inter-processor Communication Scheme (IPC)

Device has multiple hardware mechanisms to provide inter-processor level communication.

8.1 Mailbox.......... 703
8.2 Spinlock.......... 710
8.3 Secure Proxy (SEC_PROXY).......... 715

8.1 Mailbox

This chapter describes the Mailbox module of the device.

8.1.1 Mailbox Overview

Mailbox module serves to facilitate the communication between the various on-chip processors of the device by providing a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors (users) through a set of registers and associated interrupt signals.

8.1.1.1 Mailbox Features

Each mailbox module supports the following features:

- Parameters configured at design time:
  - Number of mailbox clusters
    - Each mailbox cluster has the same configuration
    - Clusters are accessed via separate VBUS regions. Clusters can be treated as mailbox module instances.
  - Number of users
  - Number of mailbox message queues
  - Number of messages (FIFO depth) for each message queue
- 32-bit message width
- Partial writes do not advance the FIFO pointers
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

8.1.2 Mailbox Functional Description

The mailbox module provides a means of communication through message queues among the users. The individual mailbox modules, or FIFOs, can associate (or de-associate) with any of the processors using the MAILBOX_IRQ_ENABLE_SET_j (or MAILBOX_IRQ_ENABLE_CLR_j) register.

Each user has a dedicated interrupt signal from the corresponding mailbox module instance and dedicated interrupt enabling and status registers.

Each MAILBOX_IRQ_STATUS_RAW_j/MAILBOX_IRQ_STATUS_CLR_j interrupt status register corresponds to a particular user.

8.1.2.1 Mailbox Block Diagram

Figure 8-1 shows the mailbox internal block diagram.

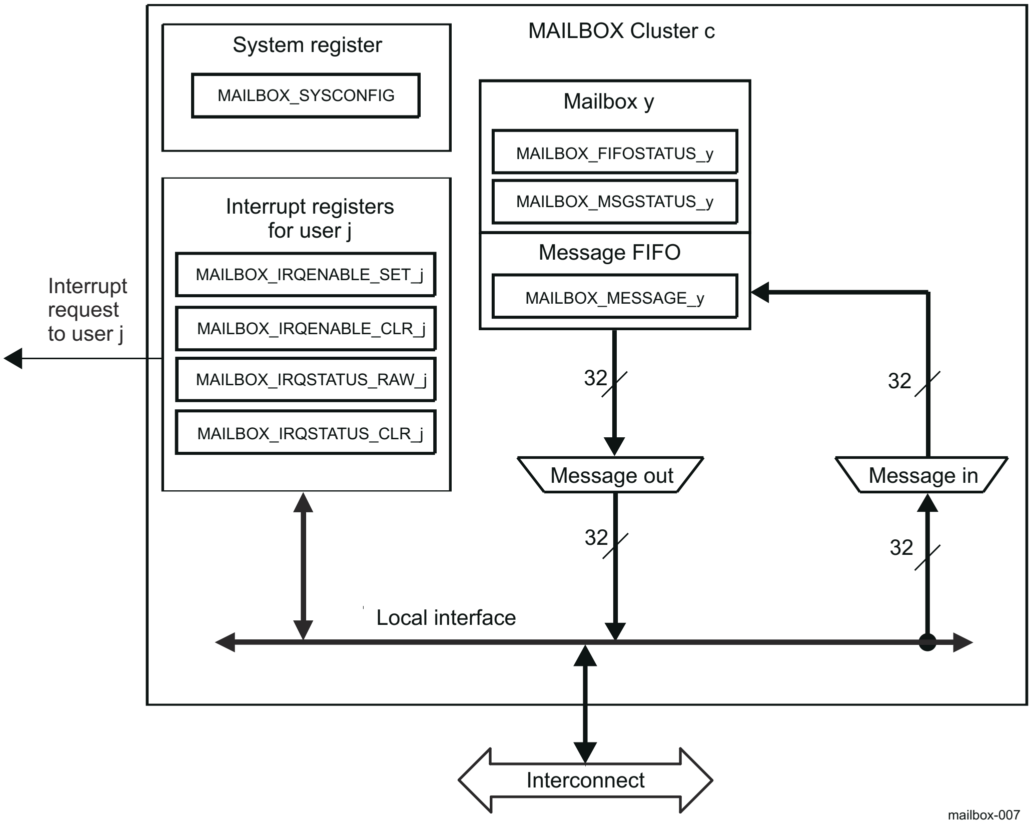

Figure 8-1. Mailbox Block Diagram

c = 0 to 11

j = 0 to 3

y = 0 to 15

8.1.2.2 Mailbox Software Reset

The mailbox module supports a software reset through the MAILBOX_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Reading the MAILBOX_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: the software reset is on-going.
- Read 0: the software reset is complete.

The software must ensure that the software reset completes before doing mailbox operations.

8.1.2.3 Mailbox Power Management

The clkstop_idle will be asserted if all of the following are true:

- The VBUSP interface is inactive
- All mailboxes are empty
- There are no enabled events or outstanding interrupts

An enabled event means there is pending action required from one of the users, and it means one or more mailboxes still expect data.

8.1.2.4 Mailbox Interrupt Requests

An interrupt request allows the user of the mailbox to be notified when a message is received or when the message queue is not full. There is one interrupt per user.

Table 8-1 lists the event flags, and their mask, that can cause module interrupts.

Table 8-1. Interrupt Events

Non-Maskable Event Flag[1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MAILBOX_IRQ_STATUS_RAW_j[0+y*2] NEWMSGSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[0+y*2] NEWMSG_STATUSMBy	Mailbox *y* receives a new message.
MAILBOX_IRQ_STATUS_RAW_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[1+y*2] NOTFULLSTATUSMBy	Mailbox *y* message queue is not full.

(1) MAILBOX_IRQ_STATUS_RAW_j register is mostly used for debug purposes.

CAUTION

Once an event generating the interrupt request has been processed by the software, it must be cleared by writing a logical 1 in the corresponding bit of the MAILBOX_IRQ_STATUS_CLR_j register.

Writing a logical 1 in a bit of the MAILBOX_IRQ_STATUS_CLR_j register will also clear to 0 the corresponding bit in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

An event can generate an interrupt request when a logical 1 is written to the corresponding unmask bit in the MAILBOX_IRQ_ENABLE_SET_j register. Events are reported in the appropriate MAILBOX_IRQ_ENABLE_CLR_j and MAILBOX_IRQ_STATUS_RAW_j registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MAILBOX_IRQ_ENABLE_CLR_j register. Events are only reported in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

In case of the MAILBOX_IRQ_STATUS_RAW_j register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

8.1.2.5 Mailbox Assignment

8.1.2.5.1 Description

To assign a receiver to a mailbox, set the new message interrupt enable bit corresponding to the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register. The receiver reads the MAILBOX_MESSAGE_y register to retrieve a message from the mailbox.

An alternate method for the receiver that does not use the interrupts is to poll the MAILBOX_FIFO_STATUS_y and/or MAILBOX_MSG_STATUS_y registers to know when to send or retrieve a message to or from the mailbox. This method does not require assigning a receiver to a mailbox. Because this method does not include the explicit assignment of the mailbox, the software must avoid having multiple receivers use the same mailbox, which can result in incoherency.

To assign a sender to a mailbox, set the queue-not-full interrupt enable bit of the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register, where *u* is the number of the sending user. However, direct allocation of a mailbox to a sender is not recommended because it can cause the sending processor to be constantly interrupted.

It is recommended that register polling be used to:

- Check the status of either the MAILBOX_FIFO_STATUS_y or MAILBOX_MSG_STATUS_y registers
- Write the message to the corresponding MAILBOX_MESSAGE_y register, if space is available.

The sender might use the queue-not-full interrupt when the initial mailbox status check indicates the mailbox is full. In this case, the sender can enable the queue-not-full interrupt for its mailbox in the appropriate MAILBOX_IRQ_ENABLE_SET_j register. This allows the sender to be notified by interrupt only when a FIFO queue has at least one available entry.

Reading the MAILBOX_IRQ_STATUS_CLR_j register determines the status of the new message and the queue-not-full interrupts for a particular user. Writing 1 to the corresponding bit in the MAILBOX_IRQ_STATUS_CLR_j register acknowledges, and subsequently clears, an interrupt.

CAUTION

Assigning multiple senders or multiple receivers to the same mailbox is not recommended.

8.1.2.6 Sending and Receiving Messages

8.1.2.6.1 Description

When a 32-bit message is written to the MAILBOX_MESSAGE_y register, the message is appended into the FIFO queue. This queue holds four messages. If the queue is full, the message is discarded.

Queue overflow can be avoided by first reading the MAILBOX_FIFO_STATUS_y register to check that the mailbox message queue is not full before writing a new message to it.

Reading the MAILBOX_MESSAGE_y register returns the message at the beginning of the FIFO queue and removes it from the queue. If the FIFO queue is empty when the MAILBOX_MESSAGE_y register is read, the value 0 is returned.

The new message interrupt is asserted when at least one message is in the mailbox message FIFO queue. To determine the number of messages in the mailbox message FIFO queue, read the MAILBOX_MSG_STATUS_y register.

8.1.2.7 Example of Communication

Figure 8-2 shows an example of communication between two processors.

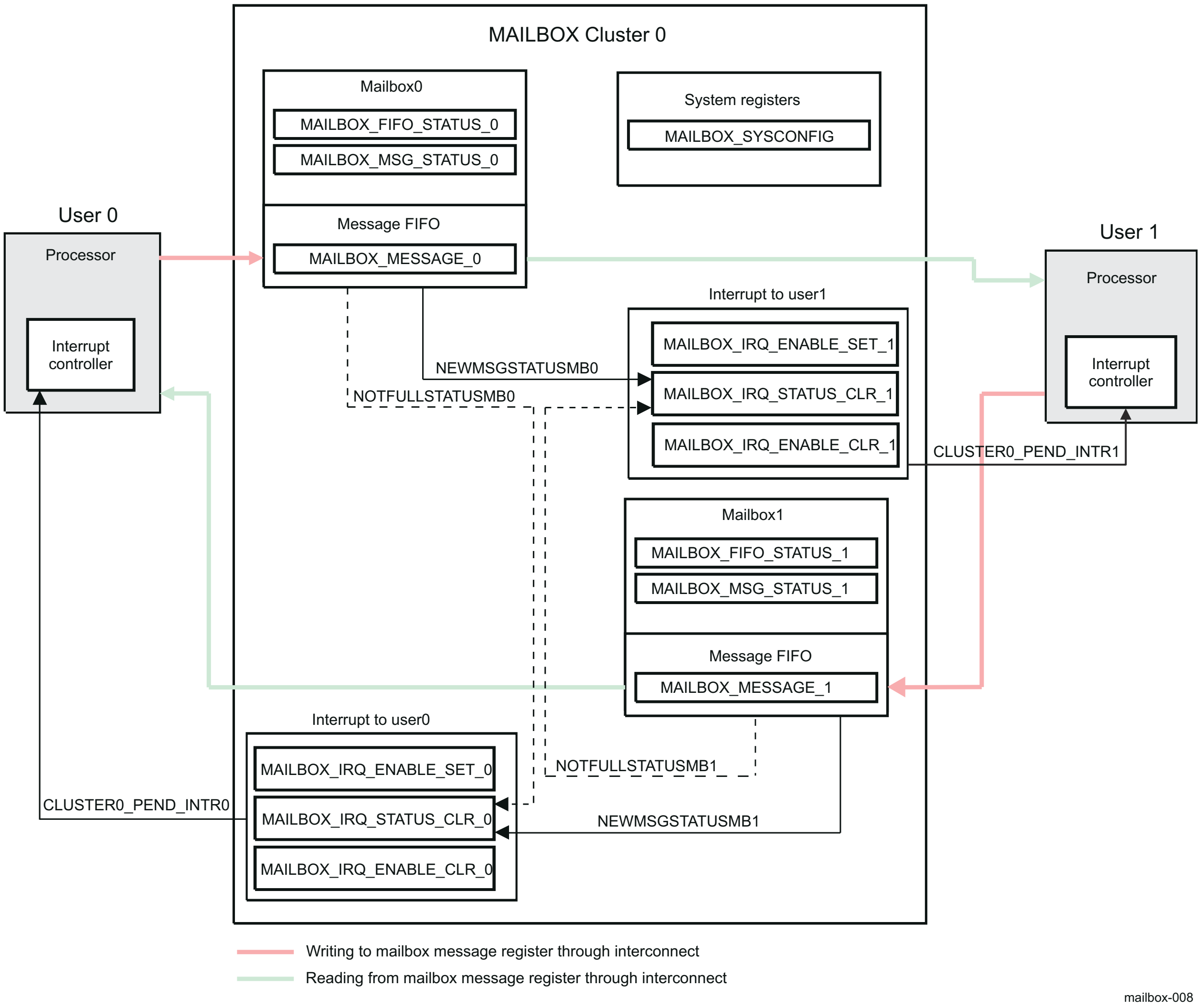

Figure 8-2. Example of Communication

8.1.3 Mailbox Programming Guide

8.1.3.1 Mailbox Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the mailbox module.

8.1.3.1.1 Global Initialization

8.1.3.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the mailbox module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the mailbox.

See *Mailbox Integration*, for further information.

Table 8-2. Global Initialization of Surrounding Modules for MAILBOX

Surrounding Modules	Comments
LPSC	The MAILBOX functional and interface clock must be enabled.
Interrupt Controllers	Processor's (user's) interrupt controller must be configured to enable the interrupt request generation.

8.1.3.1.1.2 Mailbox Global Initialization

8.1.3.1.1.2.1 Main Sequence - Mailbox Global Initialization

This procedure initializes the mailbox module after a power-on or software reset.

Table 8-3. Mailbox Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset	MAILBOX_SYSCONFIG[0] SOFT_RESET	0x1
Wait until reset is complete	MAILBOX_SYSCONFIG[0] SOFT_RESET	=0x0

8.1.3.1.2 Mailbox Operational Modes Configuration

8.1.3.1.2.1 Mailbox Processing modes

8.1.3.1.2.1.1 Main Sequence - Sending a Message (Polling Method)

Table 8-4. Sending a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y[0] FULL	=0x1
Wait until at least one message slot is available	MAILBOX_FIFO_STATUS_y[0] FULL	=0x0
ELSE		
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

8.1.3.1.2.1.2 Main Sequence - Sending a Message (Interrupt Method)

Table 8-5. Sending a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y**MAILBOX_FIFO_STATUS_y**[0] FULL	=0x1
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j**MAILBOX_IRQ_ENABLE_SET_j**[1+ y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 8.1.3.1.3.1 for interrupt handling in sending mode		
ELSE		

Table 8-5. Sending a Message (Interrupt Method) (continued)

Step	Register/Bit Field/Programming Model	Value
Write message	MAILBOX_MESSAGE_y**MAILBOX_MESSAGE_y**[31:0] VALUE	0x-
ENDIF		

8.1.3.1.2.1.3 Main Sequence - Receiving a Message (Polling Method)

Table 8-6. Receiving a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Number of messages is not equal to 0	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

8.1.3.1.2.1.4 Main Sequence - Receiving a Message (Interrupt Method)

Table 8-7. Receiving a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j[0 + y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 8.1.3.1.3.2 for interrupt handling in receiving mode		

8.1.3.1.3 Mailbox Events Servicing

8.1.3.1.3.1 Events Servicing in Sending Mode

Table 8-8 describes the events servicing in sending mode.

Table 8-8. Events Servicing in Sending Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1

8.1.3.1.3.2 Events Servicing in Receiving Mode

Table 8-9 describes the events servicing in receiving mode.

Table 8-9. Events Servicing in Receiving Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
IF: Number of messages is not equal to 0?	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
ELSE		
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
ENDIF		

8.2 Spinlock

This chapter describes the Spinlock module of the device.

8.2.1 Spinlock Overview

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device.

The Spinlock module implements 256 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

Figure 8-3 shows an overview of the Spinlock module.

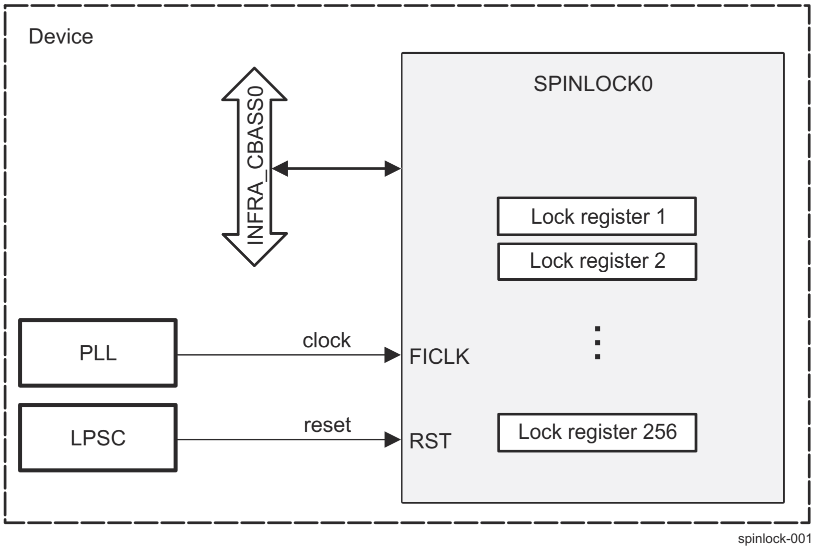

Figure 8-3. Spinlock Overview

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

8.2.2 Spinlock Functional Description

8.2.2.1 Spinlock Software Reset

The Spinlock module can be reset by software through the SPINLOCK_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. The SPINLOCK_SYSTATUS[0] RESETDONE bit can be polled to check the reset status (reading 1 indicates that reset sequence is done; reading 0 indicates that reset sequence is in progress). The software must ensure that the software reset completes before doing Spinlock operations.

8.2.2.2 Spinlock Power Management

The Spinlock module supports the Power Idle interface. Software must arrange to only power off the Spinlock module when no locks would be lost. In general, the steps to powering down the Spinlock module are:

1. Software must check that all controllers that may be using the Spinlock module are either:
    a. Already powered off (all in-use flags are 0)
    b. Notified that Spinlock is not available and the notification is acknowledged
2. If desired, check that no locks are currently held in the Spinlock module. The status of each bank of 32 locks can be read from the SPINLOCK_SYSTATUS register. If any locks are held, they are orphaned because

they are not held by any controller that is still active. Alternatively, you may decide to wait a timeout period to allow any active controller to clean up its locks before powering down.

The Spinlock module may now be powered off.

8.2.2.3 About Spinlocks

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems.

Spinlocks are not the best way to synchronize between tasks or threads on one CPU. Instead, spinlocks are for use in synchronization between different subsystems in the device that don't have any other means of hardware-based synchronization.

Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1. The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2. The locking task cannot be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3. The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If these conditions are met, then the locking code can retry a failed attempt to acquire the lock until success.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

8.2.2.4 Spinlock Functional Operation

The Spinlock module supports 256 spinlocks. It accepts only a single command at a time and processes the command fully before accepting the next command. A lock is requested by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit. There are two states: Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 1) or Not Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 0), where y = 0h to FFh.

When the status of lock *y* (where y = 0 to 255) is Not Taken (free), a read from the SPINLOCK_LOCK_REG_y register returns 0 and sets the lock to Taken (locked). When the status of lock *y* is Taken, a read returns 1 and does not change the state of the lock.

A write to the SPINLOCK_LOCK_REG_y register does not change the state of lock, unless when writing 0 when the lock is in Taken state. By doing this, the requester frees the lock.

Figure 8-4 shows the SPINLOCK_LOCK_REG_y register state diagram.

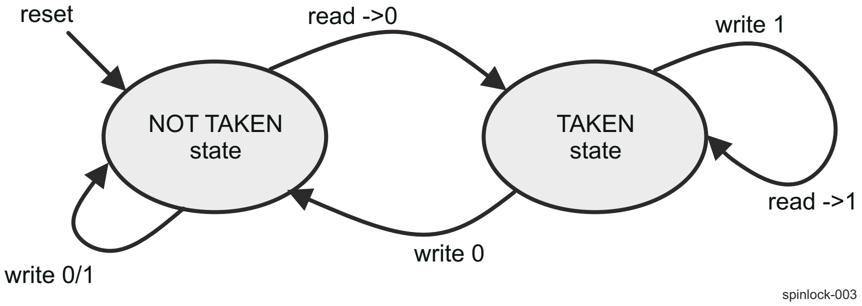

Figure 8-4. Lock Register State Diagram

Note

- There is no support to ensure that a lock register is locked and unlocked by the same process. This must be ensured in software.
- There is no support to check that the same initiator that acquired the lock is the one that is freeing the lock.

8.2.3 Spinlock Programming Guide

8.2.3.1 Spinlock Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

8.2.3.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Spinlock module is used for the first time after a device reset.

Table 8-10. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC	Spinlock functional and interface clock must be enabled. For more information, see *Clocking*

8.2.3.1.2 Basic Spinlock Operations

The main Spinlock operations are:

- Clear all the Taken spinlocks (only after a system bug recovery)
- Take a spinlock
- Release spinlock

8.2.3.1.2.1 Spinlocks Clearing After a System Bug Recovery

Module initialization (after reset) is not needed, except after system bug recovery. The following table presents the Spinlock initialization after a system bug recovery. Software should store 0 into each of the SPINLOCK_LOCK_REG_y registers at system startup to insure that all locks are initialized to Not Taken.

Table 8-11. Spinlock System Bug Recovery

Step	Register	Value
IF: SPINLOCK_SYSTATUS[0] IU0 = 1?	SPINLOCK_SYSTATUS[0] IU0	=1
Free the 256 locks	SPINLOCK_LOCK_REG_y[0] TAKEN (y = 0 to 255)	0x0
END		

8.2.3.1.2.2 Take and Release Spinlock

This procedure configures the take and release (free) operations for the Spinlock module. A spinlock should only be held with interrupts disabled. So, before attempting to obtain the spinlock, software must disable interrupts. Then it must read the SPINLOCK_LOCK_REG_y[0] TAKEN bit to attempt to obtain the lock. If it succeeds, it must proceed directly through the critical section then unlock and re-enable interrupts. If the acquisition attempt fails, the acquisition must be reattempted. To prevent unknown interrupt disabled time, interrupts must be re-enabled and then disabled before reattempting to acquire the lock. Figure 8-5 shows the described above procedure.

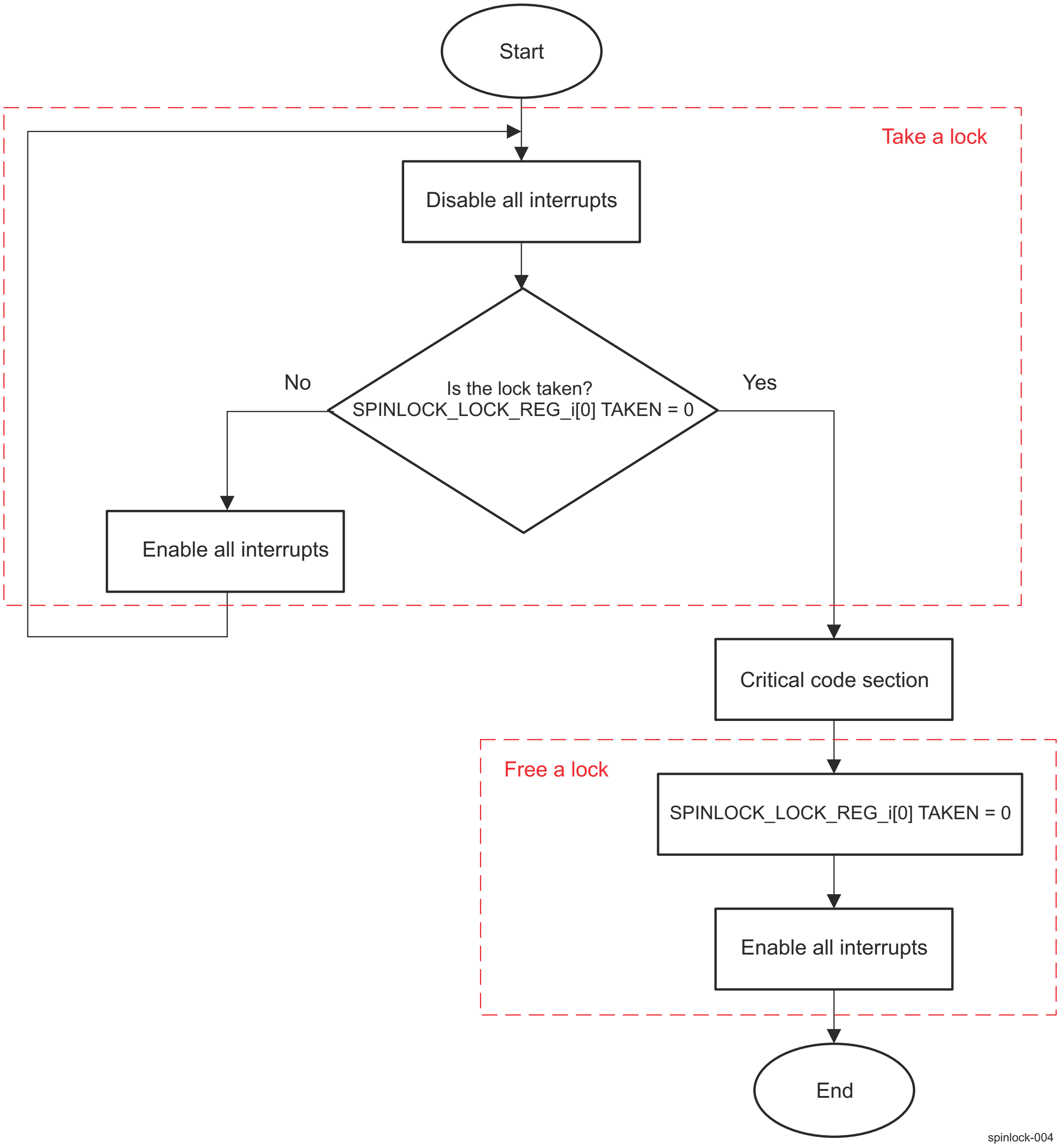

Figure 8-5. Take and Release Spinlock

Table 8-12. Register Call Summary

Register Name
SPINLOCK_LOCK_REG_y[0] TAKEN

Table 8-13. Subprocess Call Summary

Subprocess Name	Description
Disable (Mask) All Interrupts	For information about disabling/enabling all interrupts in an Arm® processor, refer to Arm *Technical Reference Manual*, available at infocenter.arm.com/help/index.jsp. For information about disabling/enabling all interrupts in other processors, refer to the corresponding processor chapter.
Enable (Unmask) All Interrupts	

8.3 Secure Proxy (SEC_PROXY)

The third IPC hardware mechanism is to use SEC_PROXY, which provides an IPC mechanism which carries a large message for complex communications among processors. It allows processors to read and write a message in small chunks.

There are two sets of SEC_PROXY in the device, one SEC_PROXY is dedicated for IPC for HSM M4F, and the second SEC_PROXY is for the rest. When the SEC_PROXY generates events, an IPC message is received or sent, and events are sent to interrupt aggregators before those events are converted into interrupts to the processors. The utilization of SEC_PROXY is user defined through memory map allocation. Each processor can be allocated with its own SEC_PROXY region to receive and send IPC messages.

Chapter 9

Memory Controllers

9.1 DDR Subsystem (DDRSS)......717

9.2 Region-based Address Translation (RAT) Module......730

9.1 DDR Subsystem (DDRSS)

This section describes the DDR Subsystem (DDRSS) for the device.

9.1.1 DDRSS Overview

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via CBASS0 interconnect.

The DDRSS0 supports:

- Memory Types:
  - LPDDR4 up to 3733MT/s @ 0.75V or 0.85V VDD_CORE
- Memory Bus Features:
  - Up to 32-bit width with in-line ECC
  - Up to 2 ranks
  - LPDDR4 densities up to 8GBytes (4GBytes each rank)
- Two System Bus Interfaces - one for real time and another for non-real time traffic:
  - 256-bit data width
  - Little endian only
  - Address aliasing prevention to block accesses to unpopulated SDRAM region
  - Clock asynchronous to DDR clock
- Configuration Bus Interface:
  - 32-bit data width
  - Linear incrementing addressing mode
  - 32-bit aligned accesses only
  - Little endian only
  - Clock asynchronous to DDR clock
- Key Features:
  - Full coherency across all commands
  - Bank interleaving
  - Priority based scheduling
  - Scheduling based on bank openness
  - Class of Service (CoS) - Three latency classes supported
  - Leaky bucket function to avoid blocking of Low Priority Thread
  - Drain function to expedite execution of reads in the controller
  - Read/write scheduling to avoid turn-around time
  - Prioritized refresh scheduling
  - Dynamic change of refresh rate via software for extended temperatures
  - Statistical counters for performance management
- SDRAM ECC Features:
  - In-line ECC
  - 64-byte ECC calculated over 512-byte data
  - Read-modify-write ECC for sub-word writes
  - Support ECC cache to improve in-line ECC performance
  - Support 64 cache-lines each 512-byte wide
  - In-line ECC performance impact shall be minimum of 12.5% for linear cached traffic
  - ECC address error logging
  - Statistical counters for counting ECC errors
- Low Power Features:
  - All power modes defined by JEDEC (clock stop for LPDDR4, self-refresh, power-down, etc.)
  - Self-refresh entry and exit via software or hardware clock stop request/acknowledge
  - System bus clock stop via hardware clock stop request/acknowledge when controller is idle

  - Automatic idle power saving mode when no or low activity is detected
  - DDR and system bus clock frequency change using self-refresh via software or hardware clock stop request/acknowledge
  - Turning off SoC power after DDR is put into self-refresh (DDR reset and CKE I/O retention)
  - Tri-stating of all DDR I/O cells via software while driving CKE and RESETn pins during self-refresh
  - LPDDR4 Frequency Set Point (FSP)
  - Support power switches on DDR subchip for low leakage power in low-power modesSupport power switches on DDR subchip for low leakage power in low-power modes
- Functional Safety Features:
  - VBUSM2AXI bridge AXI bus timeout
  - DDR4 command bus parity
- DDR PHY Features:
  - Automatic and software controllable initialization and calibration (ZQ) for the DDR PHY and I/O cells
  - Automatic and software controllable delay line calibrations with Voltage and Temperature (VT) compensation
  - Automatic and software controllable write levelling with VT compensation
  - Automatic read DQS gate training per rank with VT compensation
  - Automatic and software controllable DQ/DQS eye training per rank
  - Automatic and software controllable read and write data bit deskew
  - Automatic and software controllable Command/Address (CA) levelling with VT compensation for LPDDR4
  - Automatic and software controllable CA bit deskew for LPDDR4
  - Refreshes to SDRAM during leveling and training
  - No seeding requirement based on board topology for any of the leveling and training algorithms
  - Dynamic/automatic I/O Receiver disable when read transfer is not on going
  - Capability of disabling data macros and I/O cells when not in use

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

9.1.2 DDRSS Environment

Please refer to the AM62Ax DDR Board Design and Layout Guidelines application note for detailed information on DDR interface connections to LPDDR4 and DDR4 memory devices

Table 9-1 describes the DDRSS0 I/O signals used for connection to SDRAM devices.

Table 9-1. DDRSS0 I/O signals

Module Pin	Device Level Signal	I/O[1]	Description
RESETN	DDR0_RESET0_n	O	SDRAM reset
CK	DDR0_CK0	O	SDRAM differential clock pair
CKN	DDR0_CK0_n	O	
ALERTN	DDR0_ALERT_n	IO	SDRAM parity error output
A[13-0]	DDR0_A[13-0]	O	SDRAM address and command bus
WEN	DDR0_WE_n	O	SDRAM write enable
CASN/CSN[3]	DDR0_CAS_n/DDR0_CS3_n	O	SDRAM column address strobe (DDR4). SDRAM chip select (LPDDR4)
RASN/CSN[2]	DDR0_RAS_n/DDR0_CS2_n	O	SDRAM row address strobe(DDR4). SDRAM chip select(LPDDR4)
ACTN	DDR0_ACT_n	O	SDRAM activate
BA[1-0]	DDR0_BA[1-0]	O	SDRAM bank address
BG[1-0]	DDR0_BG[1-0]	O	SDRAM bank group
PAR	DDR0_PAR	O	SDRAM command parity
CSN[1-0]	DDR0_CS[1-0]_n	O	SDRAM chip select
ODT[1-0]	DDR0_ODT[1-0]	O	SDRAM on-die termination
CKE[1-0]	DDR0_CKE[1-0]	O	SDRAM CKE
DQ[31-0]	DDR0_DQ[31-0]	IO	SDRAM data bus
DM[3-0]	DDR0_DM[3-0]	IO	SDRAM data and mask/DBI
DQS[3-0]	DDR0_DQS[3-0]	IO	SDRAM data strobe
DQSN[3-0]	DDR0_DQS[3-0]_n	IO	SDRAM data strobe invert

(1) I = Input; O = Output

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

9.1.3 DDRSS Functional Description

9.1.3.1 Real Time and Non-Real Time Threads

The VBUSM2AXI supports two VBUSM interfaces:

- Real Time High Priority Thread (HPT)
- Non-Real Time Low Priority Thread (LPT)

HPT will have priority over LPT. In addition to the thread priority, the bridge will also reorder commands within a particular thread based on VBUSM priority. Therefore, the execution of commands from the command FIFO can be out-of-order. As a result, the read data can also be returned out-of-order.

The bridge will NOT maintain data coherency across threads. However, coherency within a particular thread will be maintained.

For low area implementation, the same FIFO resources are shared between HPT and LPT for write status and read data return interfaces. Therefore, system must ensure that there is no pushback on the write status and read data return interfaces by LPT to guarantee execution of HPT is not blocked.

9.1.3.2 Class of Service (CoS)

Commands arriving on LPT and HPT to the DDRSS0 carry the VBUSM priority whereas the DDR controller uses AXI priority. The VBUSM2AXI bridge has the following registers for flexible mapping of the VBUSM priority to DDR controllers's priority:

- Range match registers:
  - EMIF_SSCFG_V2A_R1_MAT_REG
  - EMIF_SSCFG_V2A_R2_MAT_REG
  - EMIF_SSCFG_V2A_R3_MAT_REG
- Priority map registers:
  - EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG
  - EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG
  - EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG
  - EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG
  - EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG
  - EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG
  - EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG
  - EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG

This allows the system to essentially create different classes of service based on the initiator (Route ID) and the priority of the commands.

Each thread has a set of corresponding Priority Map Registers to map the incoming priority on that thread to appropriate AXI priority. The default values of these registers are such that inherently the HPT traffic will have higher priority than the LPT traffic inside the controller. However, these settings can be changed via software per system needs.

The controller performs command arbitration based on AXI priority and the state of the DDR device (openness of banks, etc.). Commands with higher priority will be given execution preference over commands with lower priority. However, due to the state of the DDR device (openness of banks, etc.), a command with higher priority may not be executed before a lower priority command. Therefore, transactions within a thread can be reordered. In addition, the controller does not have any information on the thread type of the transactions. Therefore, commands can also be reordered between thread types. However, at all times the controller maintains coherency across all commands within a given thread.

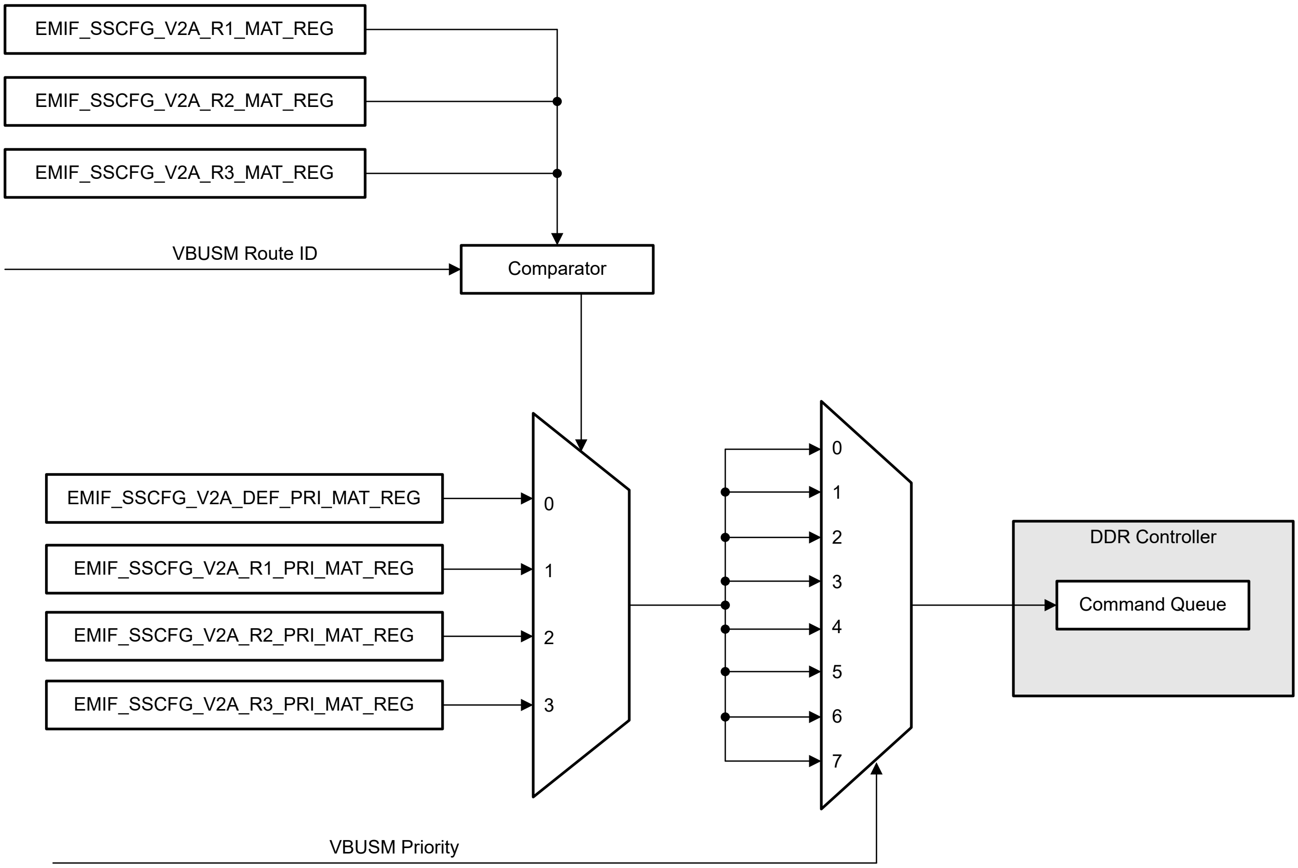

Figure 9-1. DDRSS CoS Mapping Diagram

9.1.3.3 AXI Write Data All-Strobes

The DDR controller data path is connected to the VBUSM2AXI bridge through AXI interface. To enable higher performance and lower latency, the bridge drives the AXI AWALLSTRB signal to a "1" when the AXI write data does not have any byte enable holes. This allows the DDR controller to accept and start processing the write command as soon as possible without waiting for all data. The AXI0_ALL_STROBES_USED_ENABLE bit in the DDR Controller must be set to a 0x1 to utilize this feature. The controller ignores the AWALLSTRB signal if AXI0_ALL_STROBES_USED_ENABLE is set to 0x0.

9.1.3.4 Inline ECC for SDRAM Data

For SDRAM data integrity, the VBUSM2AXI bridge supports inline ECC on the data written to or read from the SDRAM. ECC is enabled by programming the bits in the EMIF_SSCFG_ECC_CTRL_REG register. ECC is stored together with the data so that a dedicated SDRAM device for ECC is not required.

8-bit single error correction double error detection (SECDED) ECC is calculated over 64-bit data quanta. For every 512-byte data block 64 bytes of ECC is stored inline. Thus 1/9th of the total SDRAM space is used for ECC storage and the rest 8/9th is available for system use. From system point of view that 8/9th of the SDRAM data space are seen as consecutive byte addresses. Even if there are non-ECC protected regions the previously described 1/9th-8/9th rule still applies and consecutive byte addresses are seen from system point of view. Note that 8/9 of the total SDRAM space is available for system use regardless of the size of the ECC region(s). In other words, only 8/9 of the memory is available even in non-ECC regions when ECC is enabled.

The ECC is calculated for all accesses that are within the address ranges protected by ECC. The address ranges are specified through the following registers:

- EMIF_SSCFG_ECC_R0_STR_ADDR_REG
- EMIF_SSCFG_ECC_R0_END_ADDR_REG

- EMIF_SSCFG_ECC_R1_STR_ADDR_REG
- EMIF_SSCFG_ECC_R1_END_ADDR_REG
- EMIF_SSCFG_ECC_R2_STR_ADDR_REG
- EMIF_SSCFG_ECC_R2_END_ADDR_REG

Note that the addresses in these address range registers should be in terms of the DDRSS address space, not the SoC memory space. Even though the SoC memory space for DDR may be split into multiple regions, the DDRSS address space is continuous.

For example, if the beginning of DDR is in SoC memory space 0x8000_0000 to 0xFFFF_FFFF, this corresponds to DDRSS address space 0x00000000 to 0x7FFFFFFF. If the SoC has greater DDR address reach, even at a discontinuous address, the address range for these registers would be continuous (eg, if the next DDR address at the SoC level is 0x880000000, the corresponding address would be continuous at 0x80000000)

Note that the value programmed in the ECC range start/end registers does not include the lower 16 bits of the address. For example, to represent an address of 0x40000000, the register contents would be 0x4000.

The ECC is read and verified during reads if both the EMIF_SSCFG_ECC_CTRL_REG[0] ECC_EN and EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK bits are set to 0x1. For 1-bit ECC error, the bridge corrects the data and returns it to the requestor. Although the error is corrected on the returned data, the SDRAM is not corrected. It is responsibility of the system software to correct the ECC error at that location.

It is also responsibility of the system software to pre-load the ECC protected region with known data before functional reads and writes are performed. This can be done by writing to the SDRAM with ECC enabled (EMIF_SSCFG_ECC_CTRL_REG[0] ECC_EN = 0x1 and EMIF_SSCFG_ECC_CTRL_REG[1] RMW_EN = 0x1) and ECC check disabled (EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK = 0x0). Once the data is loaded in the SDRAM, ECC check must be enabled (EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK = 0x1) before using the DDR interface.

9.1.3.4.1 ECC Cache

The VBUSM2AXI bridge implements a 64-line deep ECC cache for improving inline ECC performance. Each cache line can be allocated to an initiator in the system based on its Route ID. The Route ID allocation to cache line can be done by writing to the EMIF_SSCFG_ECC_RID_INDX_REG and EMIF_SSCFG_ECC_RID_VAL_REG registers. Since the bridge uses unallocated cache lines for all read accesses without Route ID allocation, one or more locations in the cache should be kept unallocated for better performance. To ensure that at least one cache line remains unallocated, in the case all cache lines are allocated by software, the bridge automatically unallocates the 63rd cache line. Write accesses without Route ID allocation result in ECC and data writes to the SDRAM, when the EMIF_SSCFG_ECC_CTRL_REG[4] WR_ALLOC bit is set to 0x0. When EMIF_SSCFG_ECC_CTRL_REG[4] WR_ALLOC is set to 0x1, an unassigned cache-line is allocated to write accesses without Route ID allocation.

9.1.3.4.2 ECC Cache Flush

For low power modes, the bridge supports flushing the cache when DDRSS stop clock request is asserted. When a clock stop is requested, the bridge will start issuing writes to the DRAM until all dirty cache locations are written to the DRAM. Once the writes are complete, the bridge asserts an acknowledge signal to let the subsystem know that the operation is complete. The subsystem uses this acknowledge signal along with acknowledgments from other submodules to generate the final DDRSS stop clock acknowledge to the system.

9.1.3.4.3 ECC Statistics

For 1-bit ECC error, the bridge logs the address location for the error in an internal 2-level deep FIFO. It stores the first two 1-bit ECC errors. The EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG register shows the address on top of the internal FIFO. Software should write 0x1 to the EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG[29-0] ECC_1B_ERR_ADR field to pop the FIFO and display the next address stored. The FIFO is loaded with the address for the next 1-bit ECC error if it is not full. No address comparison will be performed, that is, if a single address is associated with more than one ECC error, that address is logged twice.

The number of 1-bit ECC errors can be counted using the EMIF_SSCFG_ECC_1B_ERR_CNT_REG register. The bridge also supports programming a threshold in the EMIF_SSCFG_ECC_1B_ERR_THRSH_REG register. When the 1-bit error count is equal to or greater than the programmed threshold, the bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR bit and also triggers the DDR0_DDRSS_DRAM_ECC_CORR_ERR_LVL_0 interrupt. When servicing the interrupt, software needs to clear the error count otherwise further interrupts will not be triggered. For 2-bit ECC errors, the bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR bit and also triggers the DDR0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0 interrupt. The bridge does not correct the data for these uncorrectable errors. Along with generating the interrupt, the bridge also reports an error to the requesting initiatior and sends all zeros for the data. The bridge also logs the address location for the error in the EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG register.

The bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[5] ECCM1BERR bit and triggers the DDR0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0 interrupt whenever it receives multiple 1-bit errors in different data words of the same SDRAM burst. This is done because the probability of receiving multiple 1-bit errors in different data words of the same SDRAM burst is very low. If this occurs, the chances are that there were multi-bit errors in each data word. Therefore, for reliability, pessimistic approach is taken to report these as a fatal error. The threshold for the number of 1-bit errors that result in an uncorrected error, reporting can be set by writing to the EMIF_SSCFG_ECC_CTRL_REG[11-8] COR_ECC_THRESH field. For reliability, the threshold is always kept at 0/1 meaning 1-bit error in 2 or more data words is reported as a 2-bit error. For debug, the threshold can be changed to a higher value. Note that since these are multiple 1-bit errors, the statistic logging is done in the EMIF_SSCFG_ECC_1B_ERR_CNT_REG and EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG registers.

9.1.3.5 Address Alias Prevention

The VBUSM2ZXI bridge checks the VBUSM address received against the valid SDRAM address space programmed in the EMIF_SSCFG_V2A_CTL_REG register. If the VBUSM address for an access falls outside the programmed range the bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR bit and also triggers the DDR0_DDRSS_V2A_OTHER_ERR_LVL_0 interrupt. The address and the Route ID for the command that caused error are logged in the EMIF_SSCFG_V2A_AERR_LOG1_REG and EMIF_SSCFG_V2A_AERR_LOG2_REG registers.

The bridge fragments all incoming transactions into 64-byte accesses aligned at a 64-byte boundary. Therefore, for commands greater than 64 bytes with an address error, each fragment will report an error. This can cause multiple interrupts to be reported if software clears the error interrupt for the first fragment while other fragments are being executed. The address log register will always log the address for the fragment which caused the last interrupt. The valid address range can be programmed using the EMIF_SSCFG_V2A_CTL_REG[9-5] SDRAM_IDX and EMIF_SSCFG_V2A_CTL_REG[4-0] REGION_IDX fields.

Table 9-2 summarizes the scenarios for determining valid address range and interrupt generation.

Table 9-2. REGION_IDX and SDRAM_IDX Scenarios

Condition	Description
REGION_IDX = SDRAM_IDX	DDR region size is equal to the connected SDRAM size. It is the SoC responsibility to ensure that the addresses received by the DDR subsystem do not fall outside the region size. No address error is generated if the address received falls outside the region size.
REGION_IDX < SDRAM_IDX	DDR region size is less than the connected SDRAM size. It is SoC responsibility to ensure that the addresses received by the DDR subsystem do not fall outside the region size. No address error is generated if the address received falls outside the region size.
REGION_IDX > SDRAM_IDX	DDR region size is greater than the connected SDRAM size. Address error is generated if the address received falls outside the connected SDRAM size.

A write access outside the programmed range is discarded. A write error associated status is sent back to the VBUSM interface.

A read access outside the programmed range is executed on the SDRAM interface as a normal read, but data will contain all zeroes before forwarding it to the VBUSM interface. A read error associated status is sent back to the VBUSM interface along with the read data containing all zeroes.

When inline ECC is enabled, the available SDRAM size is reduced by 1/9th of the size programmed in the SDRAM_IDX field. Therefore, the bridge reports an error if an access falls outside the reduced SDRAM size when inline ECC is enabled. The reduced SDRAM size limit applies to all accesses, both to the protected and non-protected ECC regions.

9.1.3.6 AXI Bus Timeout

The VBUSM2AXI bridge has a timeout counter that expires when no AXI transaction can be sent to the DDR controller or no AXI response is received from the controller for a programmed time interval. The counter only counts when there are pending commands in the bridge and the AXI bus is idle. Therefore, the bridge will not time out during low-power modes. The time interval can be programmed by writing to the EMIF_SSCFG_V2A_BUS_TO[23-0] BUS_TIMER field.

Upon the expiry of the counter, the bridge terminates all pending commands in its internal FIFOs, returns error responses, sets the EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR bit and triggers the DDR0_DDRSS_V2A_OTHER_ERR_LVL_0 interrupt.

After a timeout occurs, the bridge terminates any new commands received and returns error response. Writing a value of 0x0 to the EMIF_SSCFG_V2A_BUS_TO[23-0] BUS_TIMER field exits the timeout mode. The other method to exit the timeout mode is to reset the DDRSS0, thus resetting the VBUSM2ZXI bridge, the DDR controller, and the DDR PHY.

9.1.3.7 Leaky Bucket Function

The VBUSM2AXI bridge implements a leaky bucket mechanism at each LPT-HPT arbitration point. This will prevent LPT commands from getting stuck in the pipe forever due to overload of HPT commands.

A programmable system threshold will be used to trigger leaky bucket. This can be programmed in the EMIF_SSCFG_V2A_LEAKY_THRESH_REG. The threshold determines how many HPT commands can be sent in a row before a single LPT command is forwarded.

9.1.3.8 Drain Function

The VBUSM2AXI bridge implements a mechanism to drain the DDR controller. The drain action will temporarily pause the submission of commands to the controller until the read command(s) that triggered the drain operation have been resolved.

Each read going to the DDR controller will have an associated internal counter that starts at zero. This counter will increment for each write or read command given to the controller after that particular read is sent. If any read command counter exceeds the programmed threshold the bridge will start a drain action. The threshold can be programmed in EMIF_SSCFG_V2A_DRAIN_THRESH_REG.

9.1.3.9 DDRSS Interrupts

The VBUSM2AXI bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR bit, if the VBUSM address for an access that falls outside the DDR space programmed in the EMIF_SSCFG_V2A_CTL_REG register.

The VBUSM2AXI bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR bit, if it detects a hang on its interface to the DDR controller.

The VBUSM2AXI bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR bit, if the threshold for 1-bit ECC errors is met.

The VBUSM2AXI bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR bit, in case of 2-bit errors for a read access performed within the SDRAM address range protected by ECC.

The DDRSS0 asserts particular interrupt line only if the interrupts are enabled by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_SET_REG register. The interrupts can be disabled by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_CLR_REG register.

When interrupts are enabled, the corresponding bits in the EMIF_SSCFG_V2A_INT_STAT_REG register are also set if an interrupt condition occurs. The interrupts can be cleared once serviced by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_STAT_REG register as well as writing to the EMIF_SSCFG_V2A_EOI_REG register. The subsystem will send an interrupt pulse, if there are any bits set in the Interrupt Status register (EMIF_SSCFG_V2A_INT_STAT_REG) when the End of Interrupt register (EMIF_SSCFG_V2A_EOI_REG) is written.

VBUSM2AXI Bridge Events shows the events that are generated by the VBUSM2AXI bridge.

Table 9-3. VBUSM2AXI Bridge Events

Event Flag	Event Mask	Description
EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR EMIF_SSCFG_V2A_INT_STAT_REG[4] ECC2BERR	EMIF_SSCFG_V2A_INT_SET_REG[4] ECC2BERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[4] ECC2BERR_EN	Generated in case of 2-bit errors for a read access within the ECC protected SDRAM address range. For more information, see Section 9.1.3.4.3 .
EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR EMIF_SSCFG_V2A_INT_STAT_REG[3] ECC1BERR	EMIF_SSCFG_V2A_INT_SET_REG[3] ECC1BERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[3] ECC1BERR_EN	Generated in case of meeting the threshold for 1-bit ECC errors. For more information, see Section 9.1.3.4.3 .
EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR EMIF_SSCFG_V2A_INT_STAT_REG[2] TOERR	EMIF_SSCFG_V2A_INT_SET_REG[2] TOERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[2] TOERR_EN	Generated in case of a hang of the interface between the bridge and the DDR controller. For more information, see Section 9.1.3.6 .
EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR EMIF_SSCFG_V2A_INT_STAT_REG[1] AERR	EMIF_SSCFG_V2A_INT_SET_REG[1] AERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[1] AERR_EN	Generated if the VBUSM address for an access falls outside the programmed range. For more information, see Section 9.1.3.5 .

9.1.3.10 DDRSS Memory Regions

Table 9-4 shows all memory regions associated with the DDRSS0.

Table 9-4. DDRSS0 Memory Regions

Region	Start Address	End Address	Region Size
DDRSS0 wrapper logic registers	0x00F300000	0x00F3001FF	512 B
DDR controller registers	0x00F308000	0x00F309FFF	8 KB
DDR PHY independent module registers	0x00F30A000	0x00F30BFFF	8 KB
DDR PHY registers	0x00F30C000	0x00F30FFFF	16 KB
External SDRAM data space	0x080000000	0x0FFFFFFFF	2 GB
	0x880000000	0xFFFFFFFFF	30 GB

9.1.3.11 DDRSS Dynamic Frequency Change Interface

This interface is used for handshaking between DDRSS0 and CTRL_MMR0 to dynamically change DDR clock frequency to support LPDDR4 Frequency Set Point (FSP). The frequency change can be initiated either by a SoC processor or by the DDRSS0.

The associated CTRL_MMR0 registers for processor initiated frequency change are:

- CTRLMMR_CHNG_DDR4_FSP_REQ
- CTRLMMR_CHNG_DDR4_FSP_ACK

The associated CTRL_MMR0 registers for DDRSS0 initiated frequency change are:

- CTRLMMR_DDR4_FSP_CLKCHNG_REQ
- CTRLMMR_DDR4_FSP_CLKCHNG_ACK

The sequence for an SoC processor initiated frequency change is as follows:

1. The processor writes the desired frequency to the CTRLMMR_CHNG_DDR4_FSP_REQ[1-0] REQ_TYPE field.
2. The processor sets to 0x1 the CTRLMMR_CHNG_DDR4_FSP_REQ[8] REQ bit to initiate frequency change.
3. The processor programs PLL12 according to the CTRLMMR_CHNG_DDR4_FSP_REQ[1-0] REQ_TYPE value.
4. The processor polls the CTRLMMR_CHNG_DDR4_FSP_ACK[7] ACK and CTRLMMR_CHNG_DDR4_FSP_ACK[0] ERROR bits to check if the frequency change has been completed successfully.

The sequence for DDRSS0 initiated frequency change is as follows:

1. DDRSS0 requests frequency change by asserting the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[7] REQ bit and the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[1-0] REQ_TYPE field. The REQ bit is also connected to the DDR0_DDRSS_PLL_FREQ_CHANGE_REQ_0 interrupt.
2. Software reads the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[1-0] REQ_TYPE value and programs PLL12 accordingly.
3. After the DDRSS0_FCLK has been changed software should set to 0x1 the CTRLMMR_DDR4_FSP_CLKCHNG_ACK[0] ACK bit.

9.1.3.12 DDR Controller Functional Description

Figure 9-2 shows the DDR controller blocks along with the DDR PHY and VBUSM2AXI bridge.

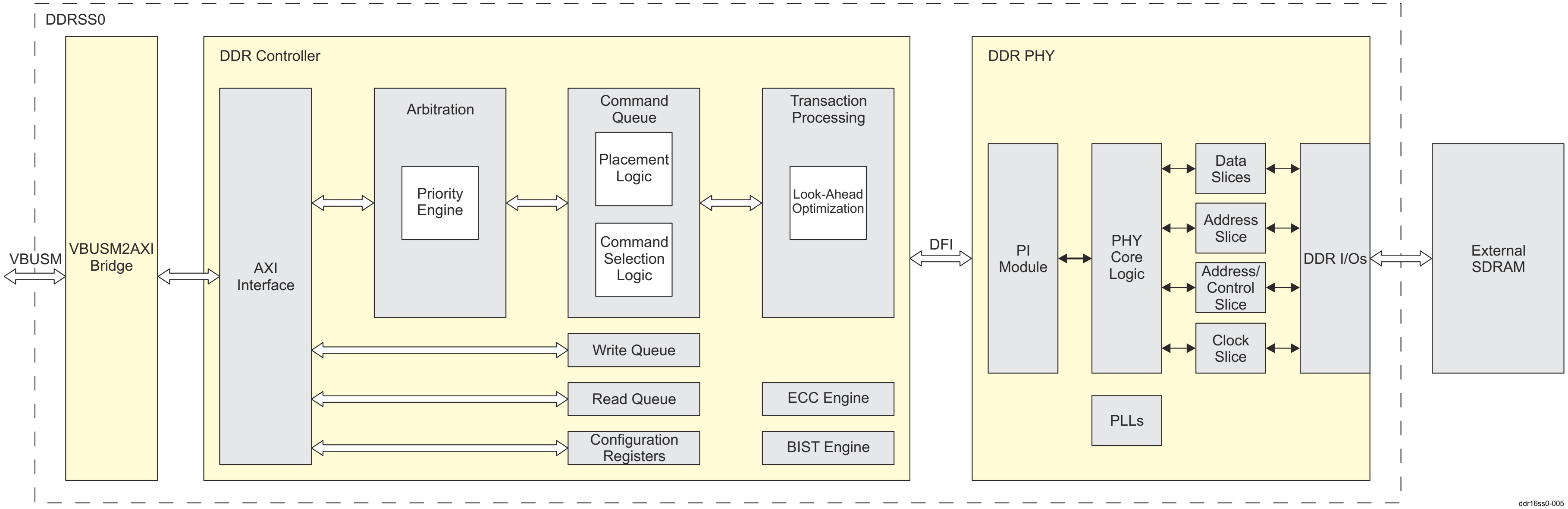

Note

The ECC Engine block of the DDR controller is not supported.

Figure 9-2. DDR Controller Functional Blocks

9.1.3.12.1 DDR PHY Interface (DFI)

The DDR controller and DDR PHY are connected via DDR PHY Interface (DFI) which is used for transferring control information and data between the PHY and the controller. For more information about DFI, see http://www.ddr-phy.org/.

9.1.3.12.2 Command Queue

The DDR controller contains a command queue which uses a placement algorithm to determine the order of commands to be placed into the command queue. The placement logic follows many rules to determine where new commands should be inserted into the queue, relative to the contents of the command queue at a time. Placement is determined by considering address collisions, source collisions, data collisions, command types and priorities. The placement logic also attempts to maximize efficiency of the DDR controller through command grouping and bank splitting.

9.1.3.12.2.1 Placement Logic

The placement logic is a 2-stage queue which determines the order of commands that run in the DDR controller. The placement logic follows rules for determining placement of new commands into the queue, relative to the contents of the command queue at that time. Placement is determined by considering coherency, address collisions, source collisions, data collisions, user assigned priority, latency, age, and command type to offer low latency for critical controllers while optimizing bandwidth for all controllers. A second reordering stage allows ready-to-run commands to start even if the head-of-queue command is not yet ready to run. In addition, the queue can be disabled completely, resulting in an in-line queue that services requests in the order that they arrive.

The DDR controller also has a full look-ahead facility that reduces the effect of page misses by pre-conditioning rows for upcoming requests by using “spare” cycles in preceding transactions.

9.1.3.12.2.2 Command Selection Logic

After a command is in the command queue, command selection logic determines the method of pulling commands from the queue for running. On each clock cycle, the selection logic scans the entries of the command queue for determining the command to run. Commands for running are based on bank readiness, availability of at least 1 burst of data (writes), availability of storage for at least 1 burst of data (reads), bus turnaround timing, and conflicts. Similar to the placement rules, a command does not run before a command that was placed ahead of it in the command queue if it conflicts with address, source ID, or bank commands. Lower priority commands can run ahead of higher priority commands if the higher priority commands are not ready to run, as long as they do not conflict with commands that are ahead in the command queue.

9.1.3.12.3 Transaction Processing

The transaction command processing logic is used to process the commands in the command queue. The logic organizes the commands to the memories in such a way that data throughput is maximized. Bank opening and closing cycles are used for data transfers. The logic reviews the entire command queue for look-ahead of which banks have to be accessed in the future and ensures that the programed memory timing conditions are met. This flexibility allows the controller to be tuned to extract the maximum performance out of memories. During processing, the controller examines the commands and issues the appropriate set of signals to the memory.

9.1.3.12.4 Paging Policy

The DDR controller offers a flexible paging policy that allows open page operation, closed page operation, or an auto-precharge-per-command option that allows both modes simultaneously. Auto-precharge-per-command allows marking a particular controller or transaction (for example, a CPU cache) as a closed-page transaction. This type of transaction reduces power and improves latency for the next transaction to a different row in the same SDRAM bank. Other transactions can be marked as open page transactions. This type of transaction reduces power and improves latency and bandwidth to the next transaction to the same row in the same SDRAM bank.

9.1.3.12.5 DDR Controller Initialization

Once the power to the SDRAM and SoC is stable, the DDR controller must be initialized. It then automatically initializes the external memory. Please refer to the Processor SDK for the software drivers to initalize the DDR registers and memory

---

Note

To facilitate the programming of these registers, refer to the device-specific DDR Subsystem Register Configuration Tool available at http://dev.ti.com/sysconfig.

9.2 Region-based Address Translation (RAT) Module

9.2.1 RAT Functional Description

9.2.1.1 RAT Operation

The RAT module performs a region based address translation. It translates a 32-bit input address into a 48-bit output address. Any input transaction that starts inside of a programmed region will have its address translated, if the region is enabled. Any disabled region is ignored from the translation lookup.

RAT has 16 regions, with each region having dedicated registers that define its attributes:

- Base address of the region, via the RAT_BASE_k register.
- Size of the region, via the RAT_CTRL_k register.
- Translated base address (48-bit). It is defined by 32-bit lower address via the RAT_TRANS_L_k register, and 16-bit upper address via the RAT_TRANS_U_k register.

The input addresses are compared against all the enabled regions in parallel. The region size defines how many of the lowest address bits are included in the region space, starting from a 1B space to a 4GB space. Then the upper bits not part of the region are used for the lookup and comparison, matching those bits of the input addresses against the region base address. The region matches when it is enabled and the compare matches. The first region that matches has the output address set with the region translated base address upper bits. The lower bits that are part of the region size are copied from the input address to the output address. If there are no region matches then the input address is copied to the output address entirely.

RAT does not automatically correct transactions that cross region boundaries, that is, start inside of a region and end outside of it, or start outside of a region and end inside of it. If a boundary crossing transaction is detected, then RAT annuls the transaction as illegal, generates an interrupt and logs an error, as explained in *RAT Error Logging*.

Note

The region base address and translated base address must be aligned to the defined region size. For example, if the defined region size is 64KB, then the two addresses must be 64KB aligned. This is software responsibility as RAT does not perform such alignment check. Regions that are not aligned have unpredictable results.

Moreover, multiple region definitions must not overlap in their covered address space. RAT does not check for this, so it is software responsibility to take care of it. Overlapping regions may lead to unpredictable results.

9.2.1.2 RAT Error Logging

The error log consists of a series of registers that capture the details of the transaction, including the input address that caused the error. These registers are the following:

- RAT_EXCEPTION_LOGGING_HEADER0 and RAT_EXCEPTION_LOGGING_HEADER1
- RAT_EXCEPTION_LOGGING_DATA0 through RAT_EXCEPTION_LOGGING_DATA3

The RAT module can capture one error before it is cleared by software. The error logging is enabled by default, but can be disabled via the RAT_EXCEPTION_LOGGING_CONTROL[0] DISABLE_F bit. Upon error logging an interrupt is also generated. To clear the log, software must either read the final error logging register, or manually clear the RAT_EXCEPTION_PEND_CLEAR[0] PEND_CLR bit by setting it to 0x1. This will clear the error status, and not the actual log registers, but it does allow the next error to be captured into the log registers. If the status is not cleared and additional errors are detected, they are not logged.

After an error occurs and is cleared (whether by reading the final error logging register or by clearing the status bit), the RAT_EOI_REG register must be written to guarantee the next interrupt pulse will be produced.

Chapter 10

Interrupts

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10.2 Interrupt Controllers....743
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10.4 Interrupt Connections Summary....748
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10.1 Interrupt Architecture

AM62D Interrupt Architecture includes information on how to utilize various interrupts and events in the system and relationships between interrupts and events.

An interrupt is defined as a physical signal which can be routed to the interrupt controller of various processors, which can cause the Interrupt Service Routine (ISR). This physical signal can be either a pulse or level and the polarity can be either negative or positive. And an interrupt is correspondent to an individual wire.

An event is defined as information transported by the event bus or PSI_L bus. Events are coded using an event index. The same event bus or PSI_L bus is used to transport multiple events. An event can also be routed and multiplexed to different locations. Events can’t trigger a processor’s ISR directly. They must go through the Interrupt Aggregator (IA) to convert the event into an interrupt line. For more information, see Interrupt Aggregator (INTAGGR), *Interrupt Aggregator (INTAGGR)*

The DMA transfer using BCDMA and PktDMA in AM62D can only be triggered using an event. The SoC level interrupt could be used as a BCDMA trigger using L2G logic. Interrupts in the SoC level can’t be used to trigger a pktDMA transfer.

Each type of processor has its unique interrupt controller. All A53 cores share a single Generic Interrupt Controller (GIC). Each M4F micro controller has its own dedicated interrupt controller, called Nested Vector Interrupt Controller (NVIC). Each R5 micro controller has its own dedicated interrupt controller, called Vectored Interrupt Manager (VIM). Please refer to Table 10-1 for the detailed usage.

Table 10-1. Interrupt Controllers

Processors	Interrupt Controllers
A53 core 0	All four A53 cores share the same GICSS
A53 core 1	
A53 core 2	
A53 core 3	
R5 core inside R5FSS	Dedicated VIM inside R5FSS
TIFS	Dedicated NVIC for TIFS
HSM	Dedicated NVIC for HSM. HSM receives the same sets of interrupt as TIFS

AM62D also contains multiple SoC level interrupt routers. The main function of those SoC level interrupt routers is to provide flexibility to select interrupt sources from a large group of interrupt sources. Many places use this feature, such as GPIO interrupts and some time synchronization related interrupts.

AM62D contains two ESM modules. ESM is used to consolidate/monitor the error events in the device. In this document, ESM may also be referred to as ESM0.

AM62D also has some chip level glue logic to convert some miscellaneous signals used as interrupt sources. Those miscellaneous signals are normally self-clear signals and do not need to clear after the Interrupt Service Routine (ISR) like the normal interrupts generated by the peripherals.

Figure 10-1 shows the high level interrupt architecture in AM62D.

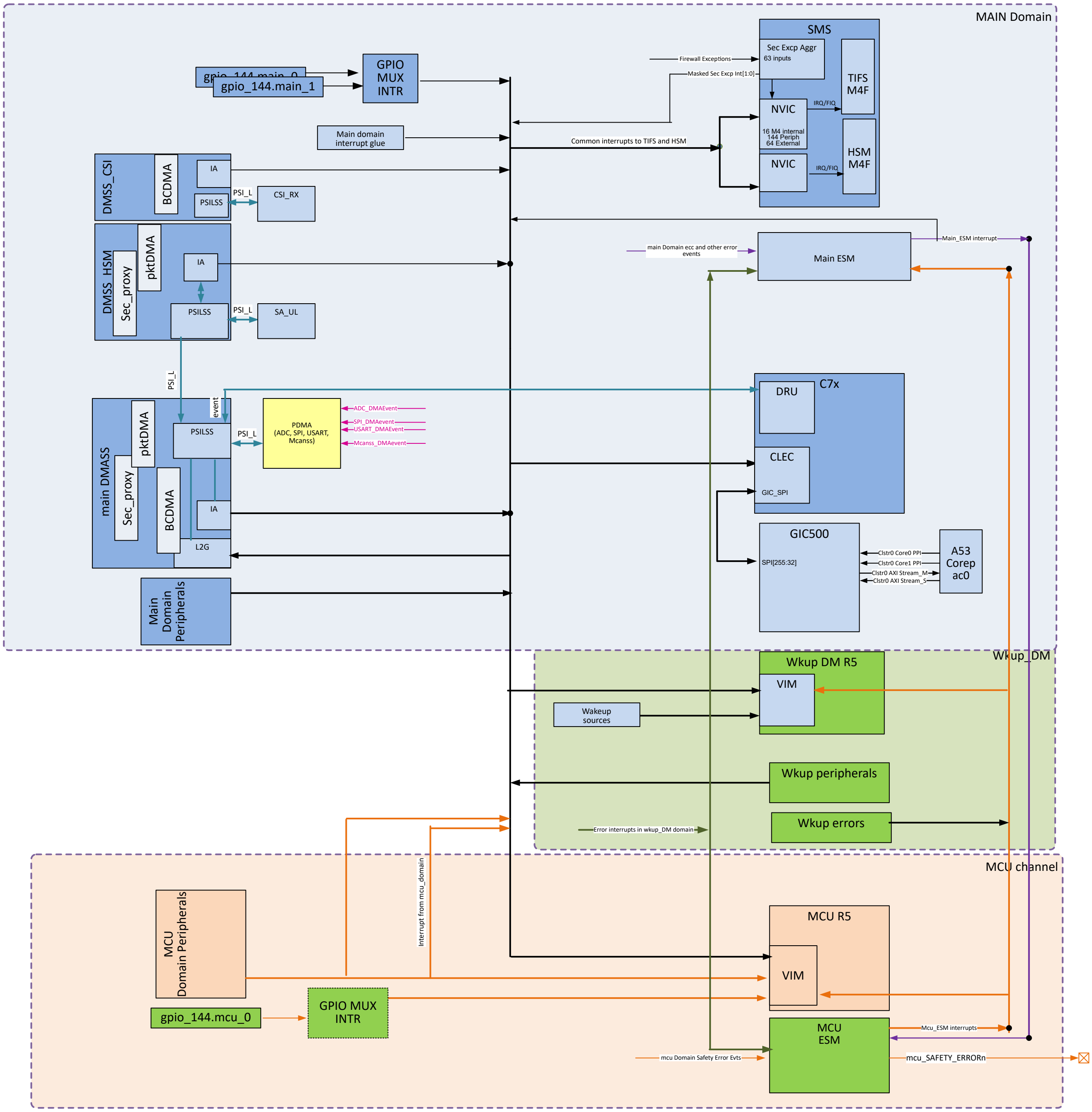

Figure 10-1. AM62D Interrupt Architecture

10.1.1 ESM Connectivity

AM62D contains two ESM modules to consolidate the error interrupts in SoC. One is in the MAIN domain and one is in the WKUP domain. Figure 10-2 shows how error interrupts are connected to these two ESM. See also *Interrupts (Inputs)* and *Interrupts (Outputs)*.

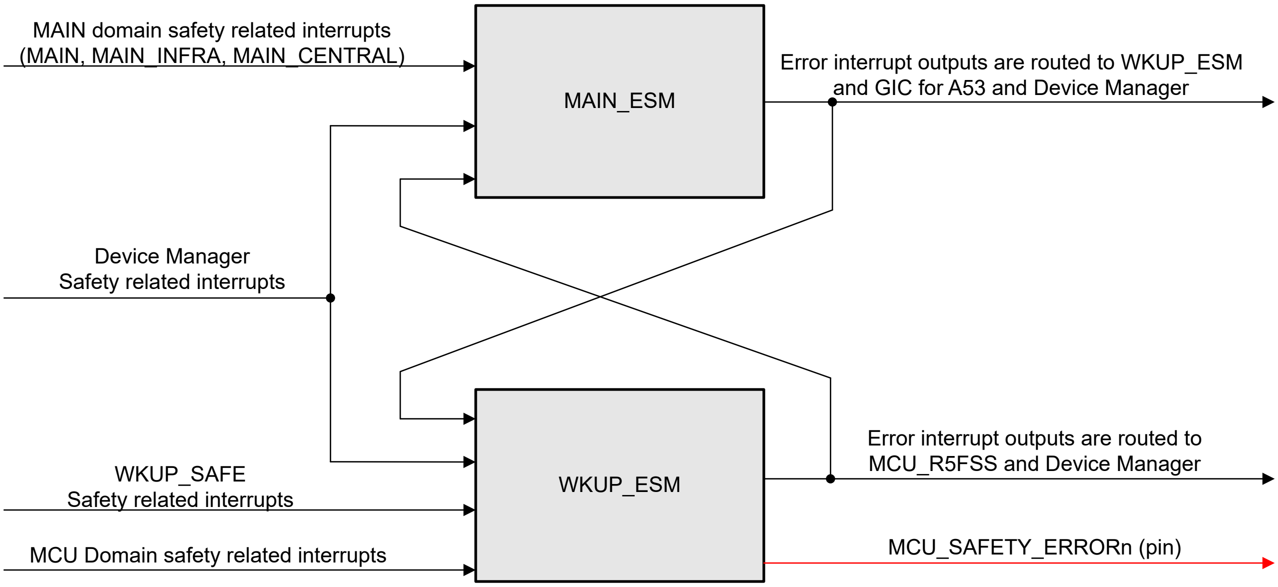

Figure 10-2. ESM Connections

The error interrupts from the WKUP_R5FSS domain are routed to both MAIN_ESM and WKUP_ESM. Users can configure ESM to cause ESM generating interrupt output from the interrupt inputs. The interrupt outputs of the MAIN_ESM are routed as interrupt inputs to the WKUP_ESM. The interrupt outputs of the WKUP_ESM are routed as the interrupt inputs to the MAIN_ESM. This means that user can configure the device to use one ESM to monitor the error interrupts for the whole device. AM62D supports the following three use cases.

10.1.1.1 Using WKUP_ESM to Monitor All Error Events in SoC

In this use case, the MAIN_ESM is used to consolidate all the error interrupts in the MAIN domain and the WKUP_R5FSS domain as MAIN_ESM's interrupt outputs, which are routed as interrupt inputs to the WKUP_ESM.

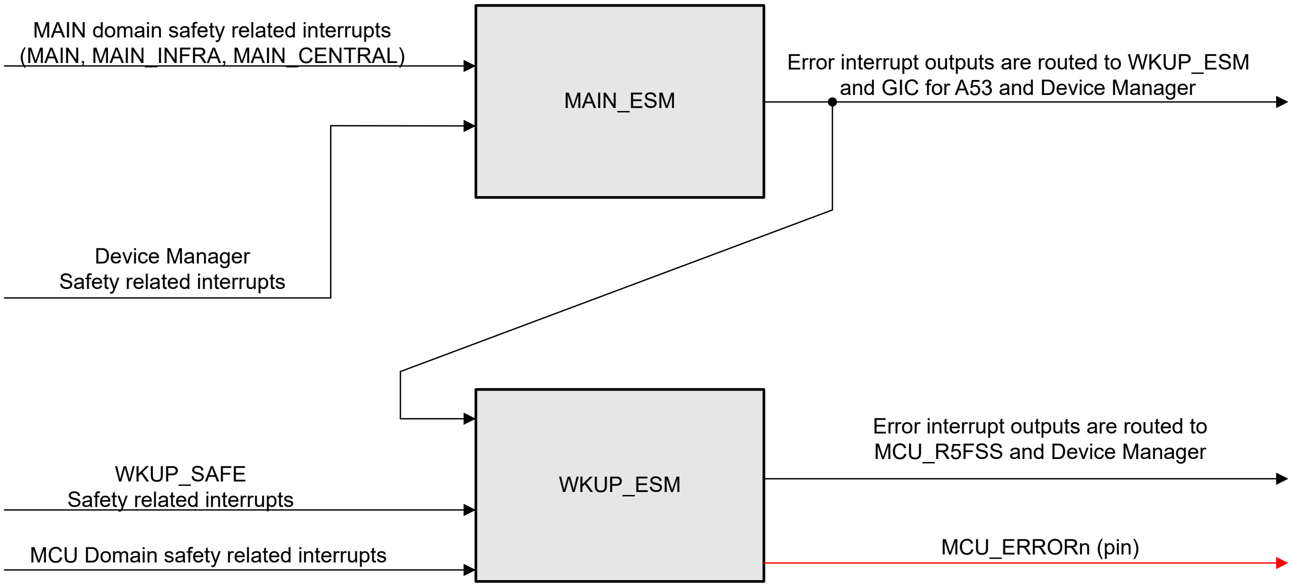

Figure 10-3. Using WKUP_ESM for All Error Interrupts in SoC

In this use case, the MAIN_ESM should be configured to disable the interrupt inputs coming from the WKUP_ESM interrupts. If those interrupt inputs are not disabled by the MAIN_ESM, the dependence loop will be formed as following:

1. Error interrupts in the MAIN domain are routed to MAIN_ESM trigger interrupt outputs generated by the MAIN_ESM
2. The error interrupt outputs from the MAIN_ESM are routed to the WKUP_ESM as interrupt inputs
3. Those error interrupt inputs trigger the WKUP_ESM generating its error interrupts outputs
4. Those interrupt outputs from the WKUP_ESM are routed back to the MAIN_ESM as interrupt inputs. If those interrupts are not disabled at the MAIN_ESM, they trigger MAIN_ESM generating interrupt outputs in the MAIN_ESM again. Going back to step 1 again.

In addition, since WKUP_R5FSS error events are already routed to the MAIN_ESM, so the input events in the WKUP_ESM connecting to those error events from the WKUP_R5FSS domain shall be disabled, otherwise those events can trigger the interrupt in both the MAIN_ESM as well as the WKUP_ESM

10.1.1.2 Using MAIN_ESM to Monitor All Error Interrupts in SoC

In this configuration, the WKUP_ESM is used to consolidate all the error interrupts from the WKUP domain and the WKUP_safe domain as interrupt outputs, and those interrupt outputs from the WKUP_ESM are routed as interrupt inputs to the MAIN_ESM. In order to avoid the interrupt dependence loop, the WKUP_ESM shall disable the interrupt inputs from ESM0.

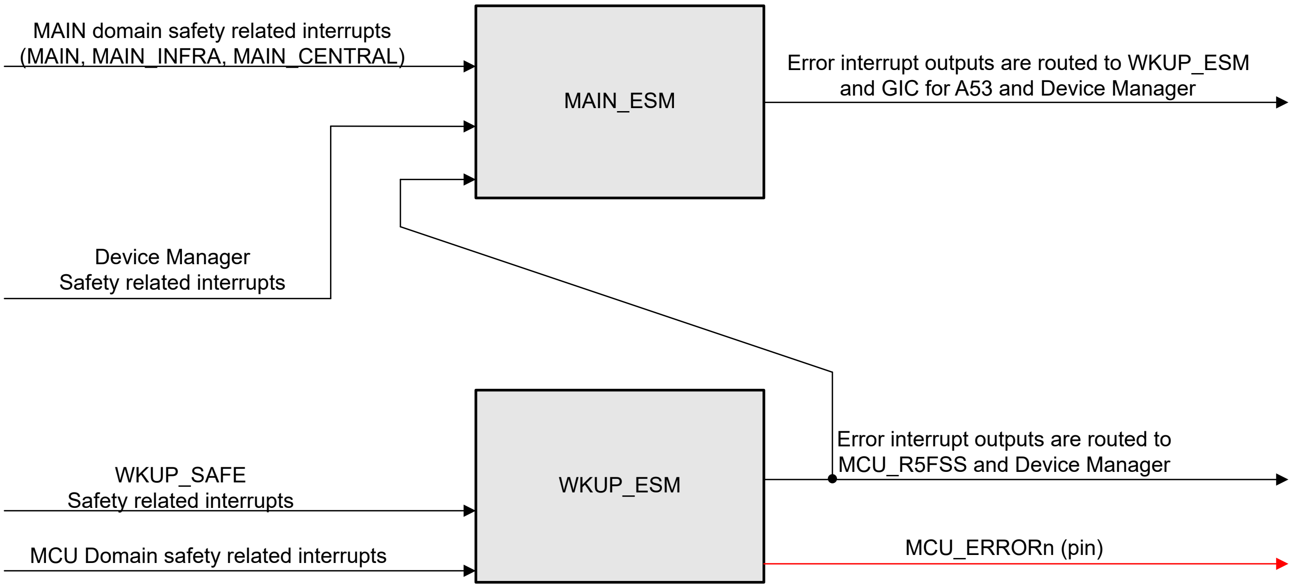

Figure 10-4. Using MAIN_ESM to Monitor All Error Interrupts in SoC

10.1.1.3 ESM Configuration During Deep Sleep Mode

When device is in deep sleep mode, only the components in the WKUP_R5FSS domain and the WKUP_SAFE are available. The MAIN domain is powered off, so the MAIN_ESM is no longer available. Since WKUP_ESM is located in the WKUP_SAFE domain, the WKUP_ESM is monitoring all of the error events during the deep sleep mode and informs the device manager.

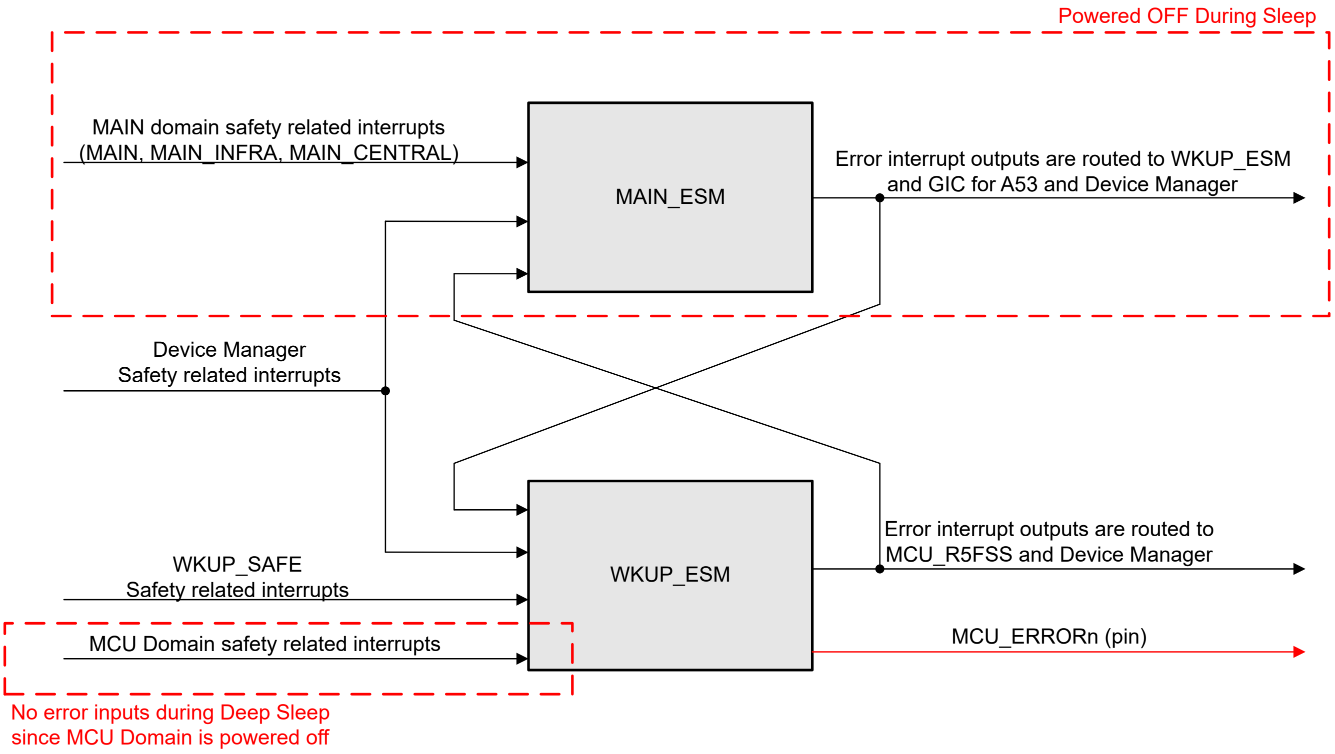

Figure 10-5. Deep Sleep Use Case

10.1.2 PSIL Events

PSIL Events are mainly generated by the BCDMA and the pktDMA. In addition, the SEC_PROXY IPC module also generates event outputs. PSIL Events can be directly utilized by the BCDMA and the pktDMA. If those events need to be processed by processor, the events need to be converted to interrupts through the Interrupt Aggregator (IA) Module. Refer to , *Interrupt Aggregator (INTAGGR)* for information on how IA is used. Figure 10-6 shows which modules generates events and how the events are converted to the interrupt.

BCDMA transfer can only be triggered through an event or by software. There are 32 SoC level interrupt signals that can be used to trigger a BCDMA transfer.

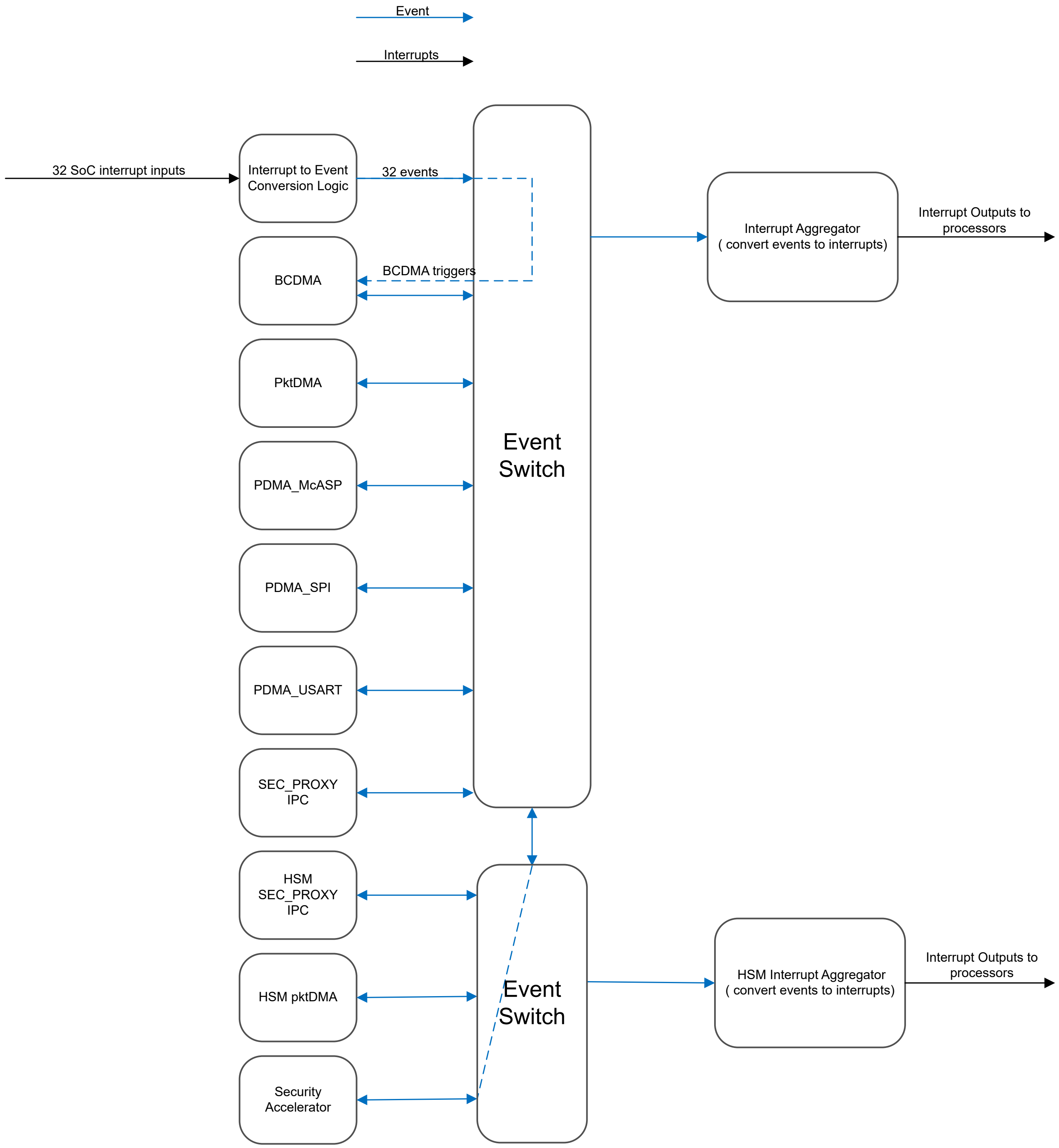

Figure 10-6. Event Handling

Table 10-2 shows all the possible interrupt sources which can be used as BCDMA triggers.

10.1.2.1 BCDMA Event Triggers

Table 10-2. BCDMA Event Triggers

Input Index	Interrupt Sources
0	CMP_EVENT_INTROUTER0.OUTP.24

Table 10-2. BCDMA Event Triggers (continued)

Input Index	Interrupt Sources
1	CMP_EVENT_INTROUTER0.OUTP.25
2	CMP_EVENT_INTROUTER0.OUTP.26
3	CMP_EVENT_INTROUTER0.OUTP.27
4	CMP_EVENT_INTROUTER0.OUTP.28
5	CMP_EVENT_INTROUTER0.OUTP.29
6	CMP_EVENT_INTROUTER0.OUTP.30
7	CMP_EVENT_INTROUTER0.OUTP.31
8	TIMESYNC_EVENT_ROUTER0.OUTL.0
9	TIMESYNC_EVENT_ROUTER0.OUTL.1
10	TIMESYNC_EVENT_ROUTER0.OUTL.2
11	TIMESYNC_EVENT_ROUTER0.OUTL.3
12	TIMESYNC_EVENT_ROUTER0.OUTL.4
13	TIMESYNC_EVENT_ROUTER0.OUTL.5
14	TIMESYNC_EVENT_ROUTER0.OUTL.6
15	TIMESYNC_EVENT_ROUTER0.OUTL.7
16	MAIN_GPIOMUX_INTROUTER0.OUTP.24
17	MAIN_GPIOMUX_INTROUTER0.OUTP.25
18	MAIN_GPIOMUX_INTROUTER0.OUTP.26
19	MAIN_GPIOMUX_INTROUTER0.OUTP.27
20	MAIN_GPIOMUX_INTROUTER0.OUTP.28
21	MAIN_GPIOMUX_INTROUTER0.OUTP.29
22	MAIN_GPIOMUX_INTROUTER0.OUTP.30
23	MAIN_GPIOMUX_INTROUTER0.OUTP.31
24	MAIN_GPIOMUX_INTROUTER0.OUTP.22
25	MAIN_GPIOMUX_INTROUTER0.OUTP.23
26	GPMC0.GPMC_SDMAREQ.0
27	DEBUGSS0.DAVDMA_LEVEL.0
28	MCRC64_0.DMA_EVENT.0
29	MCRC64_0.DMA_EVENT.1
30	MCRC64_0.DMA_EVENT.2
31	MCRC64_0.DMA_EVENT.3

10.1.3 GPIO Interrupt Handling

There are three GPIO modules in the device, which could generate almost 200 interrupts. Those GPIO interrupt outputs are routed to the GPIO interrupt router first before they are routed to the final interrupt destination. The GPIO interrupt router allows each output to select each GPIO interrupt independently.

The two GPIO modules in the Main domain use one GPIO interrupt router while the GPIO module in MCU domain has its own dedicated GPIO router. See Figure 10-7. See also *Interrupts (Inputs)* and *Interrupts (Outputs)*.

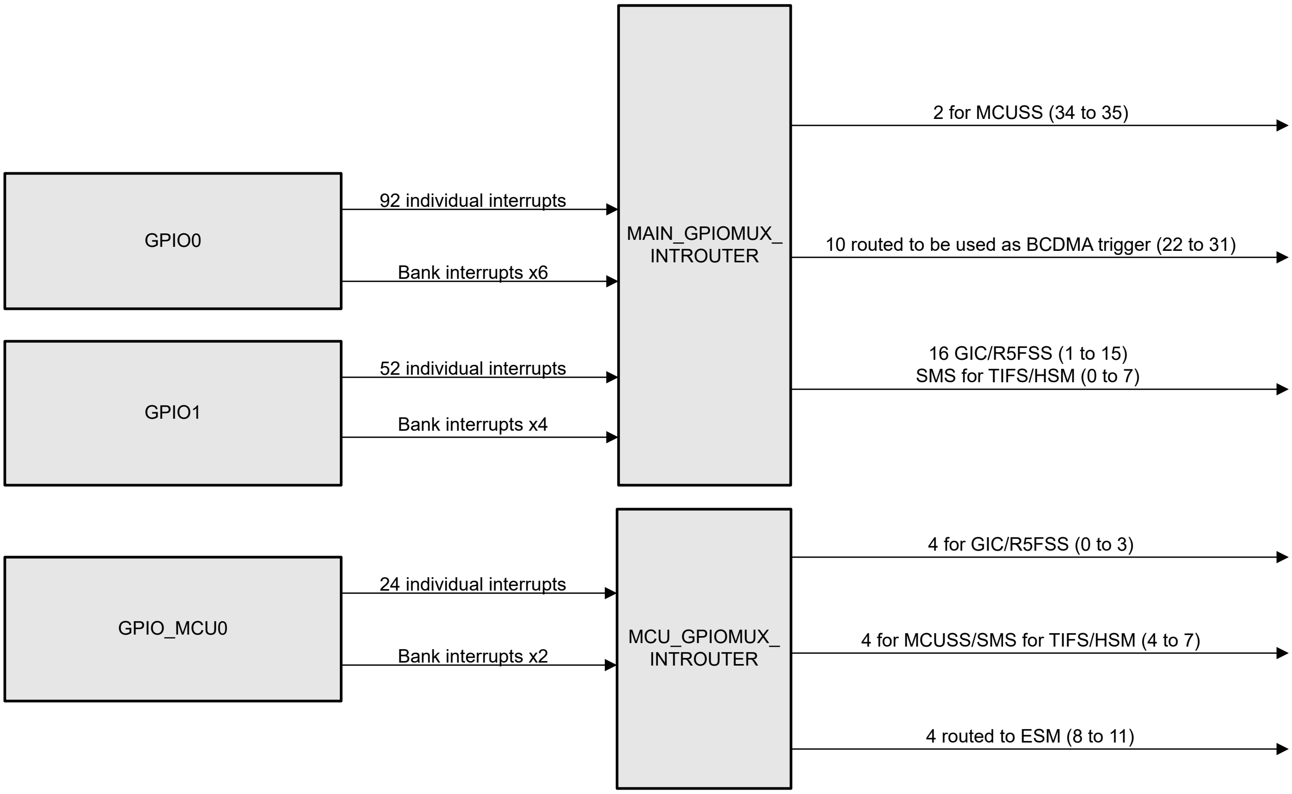

Figure 10-7. GPIO Interrupt Routing

10.1.4 Utilizing Miscellaneous Signals as Interrupt

Some of the signals are aggregated through glue logic and need to be handled separately.

10.1.4.1 Aggregated Interrupt from Timeout Gasket

There are multiple timeout gaskets in SoC, some of them are inserted at the initiator side and the others are inserted at the target interface side. Each timeout gasket module generates its own interrupt. Instead of routing the interrupt from each timeout gasket individually to the processor, the interrupts from all the timeout gasket inserted at the target sides are aggregated together (ORed), and all the interrupts from all the timeout gasket inserted at the initiator sides are aggregated together (ORed). The status of each interrupt status is captured by the TOG_STAT registers in both WKUP_CTRL_MMR and MCU_CTRL_MMR. Refer to Figure 10-8.

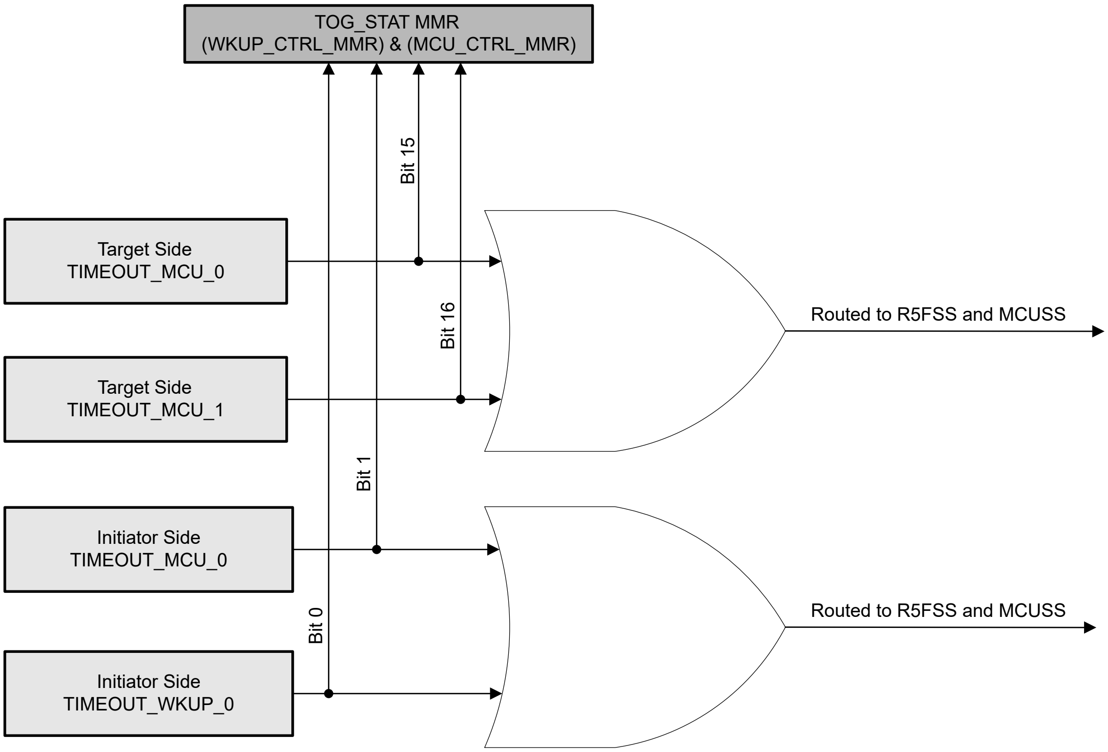

Figure 10-8. Interrupt from Timeout Gaskets

10.1.4.2 Aggregated DCC Interrupt

There are multiple DCC modules in the main domain and each DCC module generates its own DCC_done interrupt. The DCC_done interrupt from all the DCC modules in the main domain are aggregated (ORed) together before it is routed to all the processors, refer to Figure 10-9.

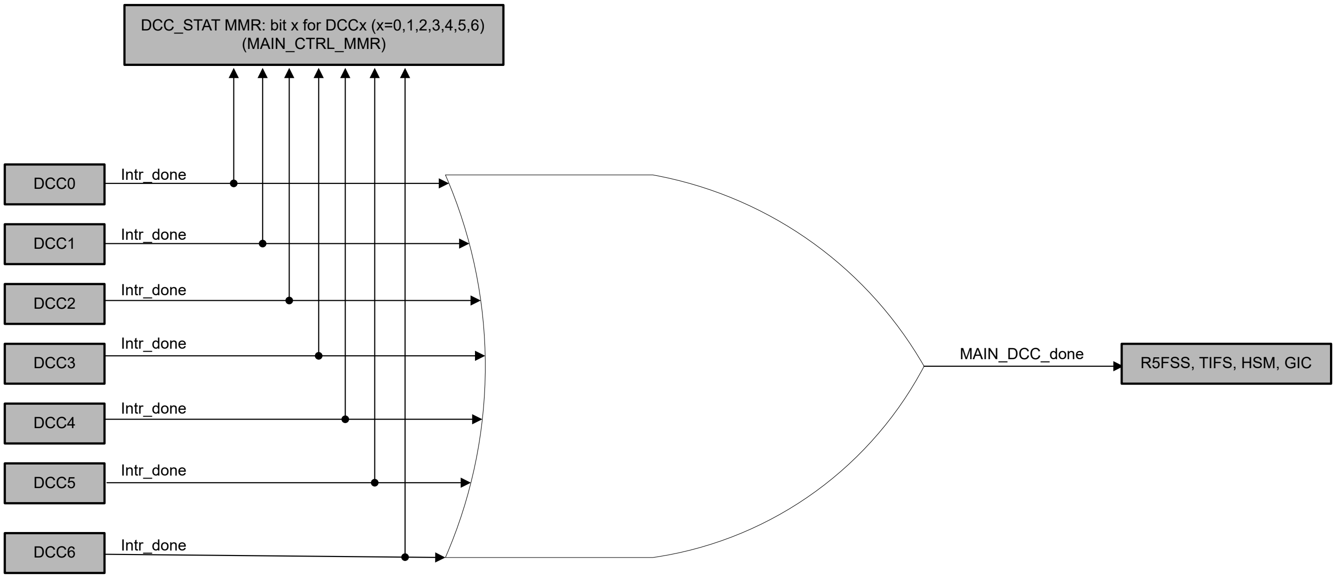

Figure 10-9. DCC Intr_done Interrupt Aggregation

10.1.4.3 Aggregated Access Error Interrupt from CBASS

CBASS modules are the interconnection blocks on the SoC level to provide access path between initiators and targets. When the transaction is not completed successfully, an interrupt is generated by the CBASS and the error transaction is logged by the CBASS module.

There are multiple CBASS modules on the SoC level to provide three layers of interconnect: the data plane, security configuration plane and debug configuration plane. The CBASS access error from the security configuration plane is only routed to TIFS and HSM, and the other CBASS access errors are aggregated before routing it to the processors, refer to Figure 10-10.

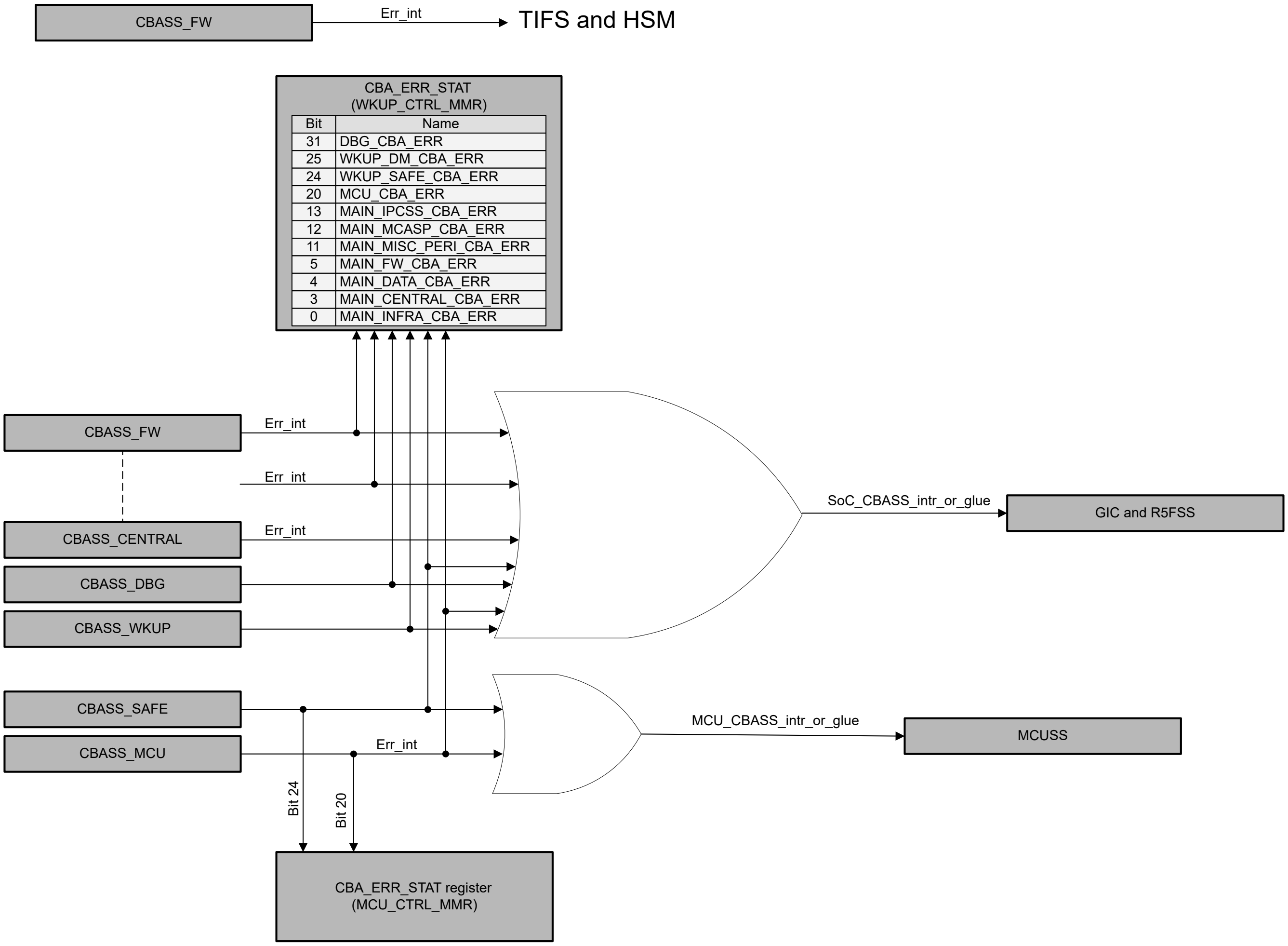

Bit	Name
31	DBG_CBA_ERR
25	WKUP_DM_CBA_ERR
24	WKUP_SAFE_CBA_ERR
20	MCU_CBA_ERR
13	MAIN_IPCSS_CBA_ERR
12	MAIN_MCASP_CBA_ERR
11	MAIN_MISC_PERI_CBA_ERR
5	MAIN_FW_CBA_ERR
4	MAIN_DATA_CBA_ERR
3	MAIN_CENTRAL_CBA_ERR
0	MAIN_INFRA_CBA_ERR

Figure 10-10. Aggregated CBASS Access Error

10.1.4.4 Access Error to Control Register Block Interrupt Aggregation

There are multiple register blocks on the SoC level, and each register block generates an error interrupt when there is an access error. Those access error interrupts are aggregated together before they are routed to processor, refer to Figure 10-11.

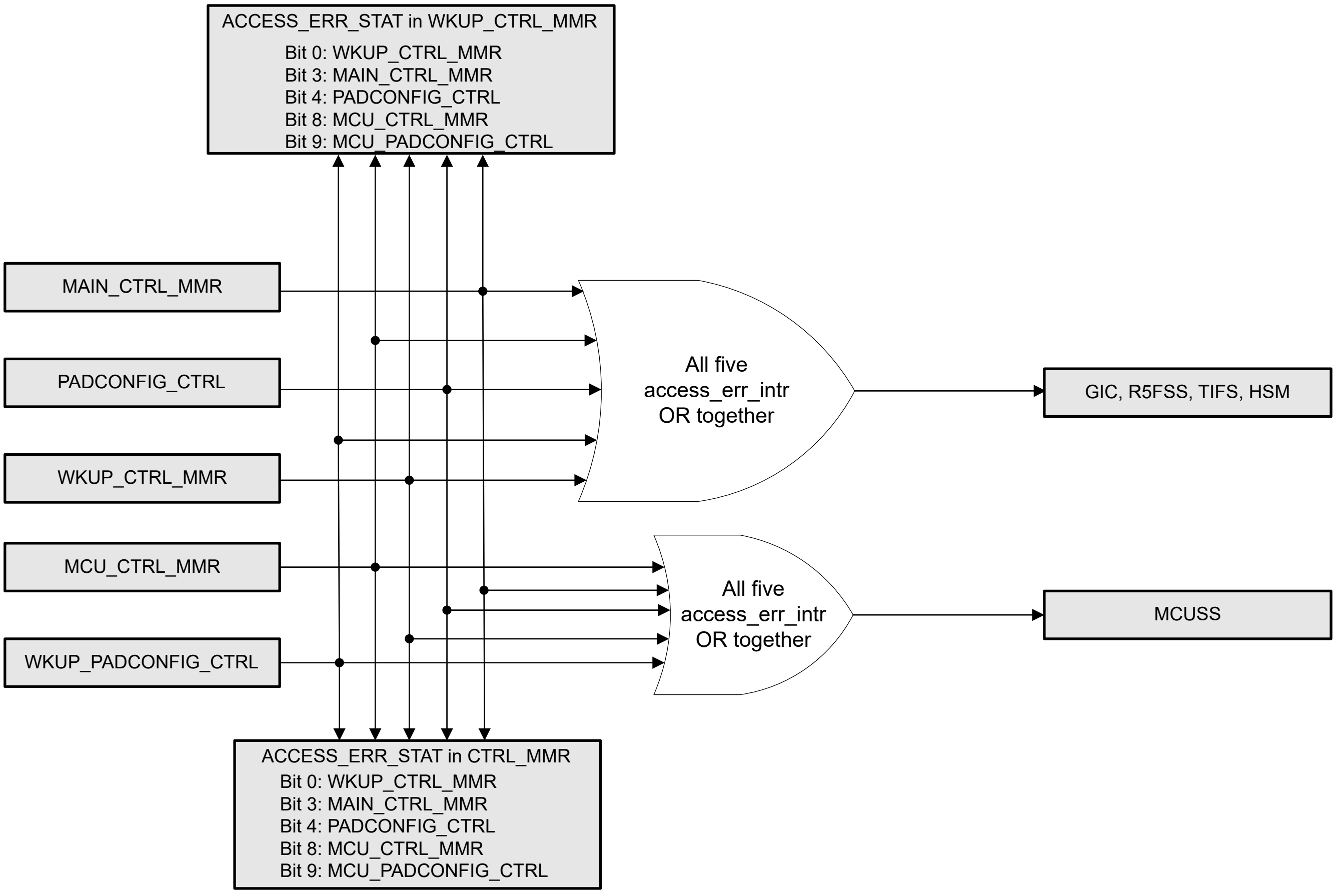

Figure 10-11. Access Error Aggregation

10.1.4.4.1 EPWM Trip Signal Aggregation

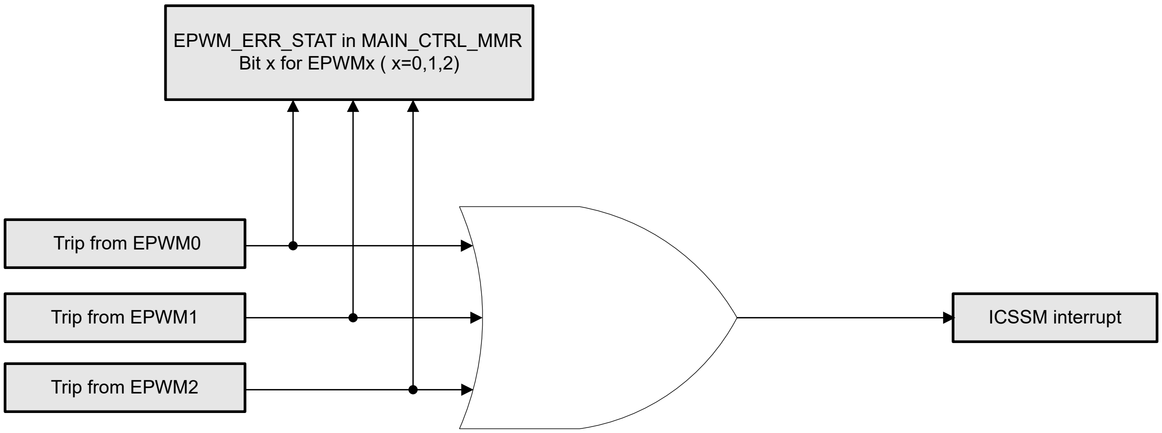

Figure 10-12. EPWM Trip Signal Aggregation as Interrupt

10.2 Interrupt Controllers

10.2.1 Generic Interrupt Controller (GICSS)

This section describes the Generic Interrupt Controller (GICSS) module in the device.

10.2.1.1 GICSS Overview

The device GICSS is a TI module that is based on the Arm GIC-500 interrupt controller. The Arm GIC-500 is a high-performance, area-optimized, built-time configurable interrupt controller which detects, manages, and distributes system interrupts to the Arm Cortex-A53 processors in the Compute Cluster.

The Arm GIC-500 is compliant to the Arm GICv3 standard. It only supports cores (such as A53) that implement the Armv8 architecture and the GIC CPU interface with the standard GIC Stream Protocol Interface. The GICSS includes additional logic (TI wrapper) to fully integrate the Arm GIC-500 into the SoC.

10.2.1.1.1 GICSS Features

Note

This chapter provides only a brief description of the GICSS functionality and features. For more details on this module, refer to the *Arm®CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

The Arm GIC-500 supports the following features in the device:

- Module revision: r1p1
- Supports both cores in the dual-A53 MPU cluster
- 16 software generated interrupts (SGIs) per core
- 16 private peripheral interrupts (PPIs) per core
- 256 shared peripheral interrupts (SPIs)
- Locality-specific peripheral interrupts (LPIs), used for message-based interrupts
- Interrupt translation service (ITS)
  - Device isolation
  - ID translation for message-based interrupts
  - This allows virtual machines to program devices directly
- Interrupt masking and prioritization
- Programmable, affinity-based interrupt routing
- 32 priorities for each interrupt
- Three different interrupt groups
  - Group 0
  - Non-secure group 1
  - Secure group 1

Additionally, the GICSS wrapper logic provides the following features:

- Synchronizes interrupt inputs to GICSS clock
- Implements AXI2VBUSM and VBUSM2AXI bridges
  - Used for bus protocol conversion (AXI-to-VBUSM and VBUSM-to-AXI, respectively)
- Implements an integrated ECC aggregator
  - Only used to inject errors (for testing purposes)

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

10.2.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

10.2.1.2 GICSS Integration

See GICSS in the Module Integration section for information about clocks, resets, and hardware requests.

10.2.1.3 GICSS Functional Description

Note

This chapter provides only a brief description of the GICSS functionality and features. For more details on this module, refer to the *Arm®CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

10.2.1.3.1 GICSS Block Diagram

Figure 10-13 shows the GICSS block diagram.

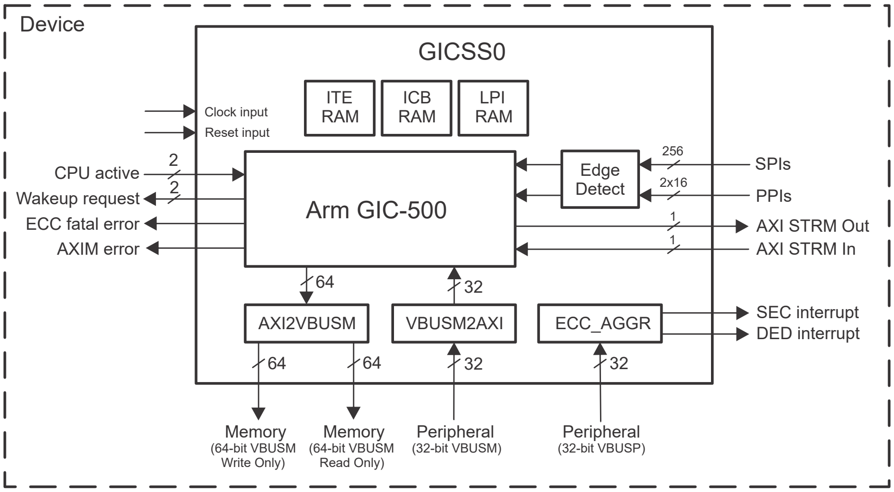

Figure 10-13. GICSS Block Diagram

10.2.1.3.2 Arm GIC-500

The Arm GIC-500 is responsible for detecting, managing and communicating system interrupts to the dual-core A53 cluster. The main difference between the Arm GIC-500 and previous Arm GIC versions is the direct communication with the CPU(s). Previously, an interrupt controller would set a pending bit to a CPU and that CPU would then have to query an interrupt controller MMR to find out what to do. Now, the Arm GIC-500 sends interrupts to a CPU via a dedicated message interface and the CPU communicates back about interrupts through the same interface. The CPU now uses writes and reads to system registers instead of over the memory interface. This leads to reduced latency and the ability to route interrupts to different CPUs based on a set of rules.

The Arm GIC-500 is divided into three main sections:

- **Distributor**: The Distributor receives interrupts from the wire interrupts and the programming interface. It is responsible for prioritizing these interrupts and sending them to the CPU interface via the GIC Stream Protocol Interface.
- **Redistributor**: There is one Redistributor per core. Each Redistributor holds the state that is individual to a particular core (such as the settings for PPIs and SGIs). It also stores the LPIs for that core after they have been generated using the ITS.
- **ITS**: The ITS is responsible for translating message-based interrupts from device peripherals into LPIs. The user can also use the ITS to manage existing LPIs. Note that the ITS is not used for other types of interrupt

10.2.1.3.3 GICSS Interrupt Types

The GICSS supports four types of interrupts:

- *Software Generated Interrupts (SGIs)*: There are 16 SGIs (ID0-ID15). These are inter-processor interrupts. SGIs can be sent using either Arm system registers or by writing to the Software Generated Interrupt Register (GICD_SGIR).

- *Private Peripheral Interrupts (PPIs)*: There are 16 PPIs (ID16-ID31). These are wired interrupts dedicated to a specific CPU. Many are reserved to specific functions via convention. These can be either active-low levels (by default), or rising edge triggered (software programmable).
- *Shared Peripheral Interrupts (SPIs)*: There are 256 SPIs (ID32-ID288). These are wired interrupts that can be routed to any core or cluster, based on the programming of that interrupt in the GICSS. These are active-high levels (by default), or rising edge triggered (software programmable).
- *Locality-Specific Peripheral Interrupts (LPIs)*: There are 57,344 of these. These interrupts are used for message-based interrupts from a peripheral. They are generated through writes to the GICSS peripheral interface. The information associated with these is located in memory. The GICSS keeps a small 64-entries cache on-board in order to reduce latency either for specific interrupts or for most-recently-used. LPIs can be routed to different CPUs based on programmed rules.

10.2.1.3.4 GICSS Interfaces

The GICSS has the following main interfaces:

- A pair of 64-bit VBUSM write-only and read-only controller interfaces
  - AXI2VBUSM bridge converts the standard 64-bit AXI4 controller interface into this pair of interfaces
  - The AXI4 controller interface allows the GICSS ITS and redistributors to access main memory
- 32-bit VBUSM peripheral interface
  - Provides access to Arm GIC-500 internal resources
  - Handles all message-based interrupts. Message-based interrupts can generate SPIs or LPIs, depending on the register that is written
  - VBUSM2AXI bridge converts this interface into an 32-bit AXI4 peripheral interface
- 32-bit VBUSP peripheral interface
  - Provides access to internal ECC aggregator
- Physical interrupt and power signals
  - Inputs: CPU active signals, SPIs and PPIs (can be programmed as either level-sensitive, or edge-triggered)
  - Outputs: Error signals and wake-up requests
- GIC Stream Protocol Interface
  - Consists of a pair of AXI4-Stream interfaces (one upstream and one downstream 16-bit AXI4-Stream interface) that the GICSS uses to send interrupts to the core and receive notifications when the core activates interrupts
  - There is a pair of physical interfaces, one in each direction, for each cluster

10.2.1.3.5 GICSS Interrupt Outputs

Table 10-3 lists the interrupts that are generated by the GICSS.

Table 10-3. GICSS Interrupt Outputs

Interrupt Name	Description
GICSS0_AXIM_ERR_0	GICSS bus error interrupt. This interrupt is triggered if the GICSS receives an error on a bus transaction, such as a decode or protection error. This is a pulse-high interrupt. If this interrupt occurs, the GICSS might lose interrupts and must be reset. If it is not reset, behavior becomes unpredictable.
GICSS0_ECC_FATAL_0	GICSS uncorrectable ECC error interrupt. Indicates an uncorrectable 2-bit error detected in one of the ITS cache memories. This is a pulse-high interrupt. If this interrupt occurs, the GICSS might lose interrupts and must be reset. If it is not reset, behavior becomes unpredictable.
GICSS0_ECC_AGGR_CORR_LEVEL_0	GICSS ECC aggregator correctable (SEC) error interrupt
GICSS0_ECC_AGGR_UNCORR_LEVEL_0	GICSS ECC aggregator uncorrectable (DED) error interrupt
GICSS0_GIC_PWR0_WAKE_REQUEST_0	GICSS wake requests for A53 cores. Asserted state indicates that an interrupt is pending for a processor that has set the PROCESSORSLEEP bit in the GICR_WAKER register. This bit indicates that the SoC should wake up the indicated CPU so that it can process the interrupt.
GICSS0_GIC_PWR0_WAKE_REQUEST_1	

10.2.1.3.6 GICSS ECC Support

The Arm GIC-500 has built-in SECDED ECC on its memories to protect against errors. The syndrome generation and checking is done internally.

Additionally, the GICSS wrapper integrates an ECC aggregator (GICSS0_ECC_AGGR) in order to allow errors to be injected for testing purposes. The generic ECC aggregator functionality is described in *ECC Aggregator*. Note that the GICSS0_ECC_AGGR supports only a subset of this functionality.

Table 10-4 shows the memory ID for each ECC endpoint. The corresponding memory ID needs to be written in the GICSS0_ECC_AGGR_VECTOR[10-0] ECC_VECTOR bit field for proper operation.

Table 10-4. GICSS0_ECC_AGGR Memory ID Mapping

ECC Aggregator	Memory ID	ECC Endpoint
GICSS0_ECC_AGGR	0	ICB RAM
	1	ITE RAM
	2	LPI RAM
	3	VBUSM2AXI bridge
	4	AXI2VBUSM read bridge
	5	AXI2VBUSM write bridge

10.2.1.3.7 GICSS AXI2VBUSM and VBUSM2AXI Bridges

The GICSS uses the AXI4 controller interface to allow the ITS and redistributors to access main memory. It is expected that the main memory (attached to a CBASS VBUSM port) holds the following:

- ITS translation tables
- ITS command queue, which is written by software in order to program the ITS
- LPI configuration table, which holds the priorities and enable bits for LPIs
- LPI pending tables, which can hold information on whether each LPI is pending on each core

The AXI2VBUSM bridge converts the standard 64-bit AXI4 controller interface into a pair of 64-bit VBUSM write-only and read-only controller interfaces. AXI4 has a separate command channel for read and write, and the AXI2VBUSM bridge keeps them separate, so that the system may prioritize or arbitrate the traffic between them as appropriate.

The GICSS uses the AXI4 peripheral interface to provide access to the programming interfaces of all its parts (distributor, redistributors, ITS). The VBUSM2AXI bridge converts the standard 32-bit VBUSM controller interface into an 32-bit AXI4 peripheral interface.

Note

The AXI2VBUSM and VBUSM2AXI bridges do not implement any MMRs.

10.3 Interrupt Router (INTROUTER)

10.3.1 INTROUTER Integration

See the Interrupts section of the Module Integration Chapter for details on clocks, resets and hardware requests.

10.4 Interrupt Connections Summary

Table 10-5. Interrupt Connections Summary

	GIC / C7x CLEC	Device Manager R5	MCU R5	SMS
SPI: MAIN Domain	Y	Y	Y	Y

Table 10-5. Interrupt Connections Summary (continued)

	GIC / C7x CLEC	Device Manager R5	MCU R5	SMS
SPI: MCU Domain	Y	Y	Y	Y
UART: MAIN Domain	Y	Y	Y	Y
UART: WKUP Domain	Y	Y	Y	N
UART: MCU Domain	Y	Y	Y	Y
I2C: MAIN Domain	Y	Y	Y	Y
I2C: WKUP Domain	Y	Y	Y	N
I2C: MCU Domain	Y	Y	Y	Y
DMTimer: MAIN Domain	Y	N	N	N
DMTimer: WKUP Domain	N	Y	N	N
DMTimer: MCU Domain	N	N	Y	N
MCANSS: MAIN Domain	Y	Y	Y	Y
MCANSS: MCU Domain	N	Y	Y	Y
ECAP	Y	Y	Y	Y
EQEP	Y	Y	Y	Y
PWM	Y	Y	Y	Y
McASP	Y	Y	Y	Y
USB	Y	Y	Y	N
emmc4b	Y	Y	Y	N
emmc8b	Y	Y	Y	N
GPMC	Y	Y	Y	N
ELM	Y	Y	Y	N
MCRC: MAIN Domain	Y	Y	Y	Y
MCRC:MCU Domain	Y	Y	Y	N
debug_cell	Y	Y	Y	N
wakeup signals from peripherals	N	Y	N	N
GIC wake up	N	Y	N	Y
DDR frequency scaling	Y	Y	Y	Y
Other DDR interrupt	Y	Y	Y	N
FSS: OSPI	Y	Y	Y	Y
CPSW	Y	Y	Y	N
DSS	Y	Y	Y	N
CSI_RX	Y	Y	Y	N
MAIN Domain DMSS	Y	Y	Y	Y
DMSS_HSM	Y	Y	Y	Y
DDPA	Y	Y	Y	Y
VTM	Y	Y	Y	Y
RTC	Y	Y	Y	N
ESM: MAIN Domain	Y	Y	Y	Y
ESM: MCU Domain	Y	Y	Y	Y
sa3_UL	Y	Y	Y	Y
GPIO: MAIN Domain	Y	Y	Y	Y
GPIO: MCU Domain	Y	Y	Y	Y
Pbist: MAIN Domain	N	Y	Y	Y
PBIST: WKUP Domain	N	Y	Y	Y

Table 10-5. Interrupt Connections Summary (continued)

	GIC / C7x CLEC	Device Manager R5	MCU R5	SMS
PBIST: MCU Domain	N	Y	Y	Y
DCC: MAIN Domain	Y	Y	Y	Y
DCC: MCU Domain	N	Y	Y	Y
PSC MAIN Domain	Y	Y	Y	Y
PSC: MCU Domain	N	Y	Y	Y
SMS	Y	Y	Y	N/A
C71x+MMA	Y	Y	Y	Y
DMSS_CSI	Y	Y	Y	N
Timeout gasket	N	Y	Y	N
Mailbox	Y	Y	Y	Y

10.5 Interrupt Sources

10.5.1 Interrupts (Inputs)

Table 10-6. Interrupts (Inputs)

Instance	Interrupt Input Line	Source Interrupt
PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0	CPSW0_CPTS_COMP_OUT_0
PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0	CPSW0_CPTS_SYNC_OUT_0
PINFUNCTION_SYNC0_OUTout	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_20
PINFUNCTION_SYNC1_OUTout	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_21
PINFUNCTION_SYNC2_OUTout	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_22
PINFUNCTION_SYNC3_OUTout	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_23
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_IN_IN_24	CPSW0_CPTS_COMP_OUT_0
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0	GPIO0_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_1	GPIO0_GPIO_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_2	GPIO0_GPIO_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_3	GPIO0_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_4	GPIO0_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_5	GPIO0_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_6	GPIO0_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_7	GPIO0_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_8	GPIO0_GPIO_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_9	GPIO0_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_10	GPIO0_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_11	GPIO0_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_12	GPIO0_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_13	GPIO0_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_14	GPIO0_GPIO_OUT_14
	MAIN_GPIOMUX_INTROUTER0_IN_IN_15	GPIO0_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_16	GPIO0_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_17	GPIO0_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_18	GPIO0_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_19	GPIO0_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_20	GPIO0_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_21	GPIO0_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_22	GPIO0_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_23	GPIO0_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_24	GPIO0_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_25	GPIO0_GPIO_OUT_25

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_26	GPIO0_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_27	GPIO0_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_28	GPIO0_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_29	GPIO0_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_30	GPIO0_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_31	GPIO0_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_32	GPIO0_GPIO_OUT_32
	MAIN_GPIOMUX_INTROUTER0_IN_IN_33	GPIO0_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_34	GPIO0_GPIO_OUT_34
	MAIN_GPIOMUX_INTROUTER0_IN_IN_35	GPIO0_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_36	GPIO0_GPIO_OUT_36
	MAIN_GPIOMUX_INTROUTER0_IN_IN_37	GPIO0_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_38	GPIO0_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_39	GPIO0_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_40	GPIO0_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_41	GPIO0_GPIO_OUT_41
	MAIN_GPIOMUX_INTROUTER0_IN_IN_42	GPIO0_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_43	GPIO0_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_44	GPIO0_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_45	GPIO0_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_46	GPIO0_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_47	GPIO0_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_48	GPIO0_GPIO_OUT_48
	MAIN_GPIOMUX_INTROUTER0_IN_IN_49	GPIO0_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_50	GPIO0_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_51	GPIO0_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_52	GPIO0_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_53	GPIO0_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_54	GPIO0_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_55	GPIO0_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_56	GPIO0_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_57	GPIO0_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_58	GPIO0_GPIO_OUT_58

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_59	GPIO0_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_60	GPIO0_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_61	GPIO0_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_62	GPIO0_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_63	GPIO0_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_64	GPIO0_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_65	GPIO0_GPIO_OUT_65
	MAIN_GPIOMUX_INTROUTER0_IN_IN_66	GPIO0_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_67	GPIO0_GPIO_OUT_67
	MAIN_GPIOMUX_INTROUTER0_IN_IN_68	GPIO0_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_69	GPIO0_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_70	GPIO0_GPIO_OUT_70
	MAIN_GPIOMUX_INTROUTER0_IN_IN_71	GPIO0_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_72	GPIO0_GPIO_OUT_72
	MAIN_GPIOMUX_INTROUTER0_IN_IN_73	GPIO0_GPIO_OUT_73
	MAIN_GPIOMUX_INTROUTER0_IN_IN_74	GPIO0_GPIO_OUT_74
	MAIN_GPIOMUX_INTROUTER0_IN_IN_75	GPIO0_GPIO_OUT_75
	MAIN_GPIOMUX_INTROUTER0_IN_IN_76	GPIO0_GPIO_OUT_76
	MAIN_GPIOMUX_INTROUTER0_IN_IN_77	GPIO0_GPIO_OUT_77
	MAIN_GPIOMUX_INTROUTER0_IN_IN_78	GPIO0_GPIO_OUT_78
	MAIN_GPIOMUX_INTROUTER0_IN_IN_79	GPIO0_GPIO_OUT_79
	MAIN_GPIOMUX_INTROUTER0_IN_IN_80	GPIO0_GPIO_OUT_80
	MAIN_GPIOMUX_INTROUTER0_IN_IN_81	GPIO0_GPIO_OUT_81
	MAIN_GPIOMUX_INTROUTER0_IN_IN_82	GPIO0_GPIO_OUT_82
	MAIN_GPIOMUX_INTROUTER0_IN_IN_83	GPIO0_GPIO_OUT_83
	MAIN_GPIOMUX_INTROUTER0_IN_IN_84	GPIO0_GPIO_OUT_84
	MAIN_GPIOMUX_INTROUTER0_IN_IN_85	GPIO0_GPIO_OUT_85
	MAIN_GPIOMUX_INTROUTER0_IN_IN_86	GPIO0_GPIO_OUT_86
	MAIN_GPIOMUX_INTROUTER0_IN_IN_87	GPIO0_GPIO_OUT_87
	MAIN_GPIOMUX_INTROUTER0_IN_IN_88	GPIO0_GPIO_OUT_88
	MAIN_GPIOMUX_INTROUTER0_IN_IN_89	GPIO0_GPIO_OUT_89
	MAIN_GPIOMUX_INTROUTER0_IN_IN_90	GPIO1_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_91	GPIO1_GPIO_OUT_1

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_92	GPIO1_GPIO_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_93	GPIO1_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_94	GPIO1_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_95	GPIO1_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_96	GPIO1_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_97	GPIO1_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_98	GPIO1_GPIO_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_99	GPIO1_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_100	GPIO1_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_101	GPIO1_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_102	GPIO1_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_103	GPIO1_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_104	GPIO1_GPIO_OUT_14
	MAIN_GPIOMUX_INTROUTER0_IN_IN_105	GPIO1_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_106	GPIO1_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_107	GPIO1_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_108	GPIO1_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_109	GPIO1_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_110	GPIO1_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_111	GPIO1_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_112	GPIO1_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_113	GPIO1_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_114	GPIO1_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_115	GPIO1_GPIO_OUT_25
	MAIN_GPIOMUX_INTROUTER0_IN_IN_116	GPIO1_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_117	GPIO1_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_118	GPIO1_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_119	GPIO1_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_120	GPIO1_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_121	GPIO1_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_122	GPIO1_GPIO_OUT_32
	MAIN_GPIOMUX_INTROUTER0_IN_IN_123	GPIO1_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_124	GPIO1_GPIO_OUT_34

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_125	GPIO1_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_126	GPIO1_GPIO_OUT_36
	MAIN_GPIOMUX_INTROUTER0_IN_IN_127	GPIO1_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_128	GPIO1_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_129	GPIO1_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_130	GPIO1_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_131	GPIO1_GPIO_OUT_41
	MAIN_GPIOMUX_INTROUTER0_IN_IN_132	GPIO1_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_133	GPIO1_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_134	GPIO1_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_135	GPIO1_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_136	GPIO1_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_137	GPIO1_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_138	GPIO1_GPIO_OUT_48
	MAIN_GPIOMUX_INTROUTER0_IN_IN_139	GPIO1_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_140	GPIO1_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_141	GPIO1_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_142	GPIO1_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_143	GPIO1_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_144	GPIO1_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_145	GPIO1_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_146	GPIO1_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_147	GPIO1_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_148	GPIO1_GPIO_OUT_58
	MAIN_GPIOMUX_INTROUTER0_IN_IN_149	GPIO1_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_150	GPIO1_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_151	GPIO1_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_152	GPIO1_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_153	GPIO1_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_154	GPIO1_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_155	GPIO1_GPIO_OUT_65
	MAIN_GPIOMUX_INTROUTER0_IN_IN_156	GPIO1_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_157	GPIO1_GPIO_OUT_67

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_158	GPIO1_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_159	GPIO1_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_160	GPIO1_GPIO_OUT_70
	MAIN_GPIOMUX_INTROUTER0_IN_IN_161	GPIO1_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_176	GPIO0_GPIO_OUT_90
	MAIN_GPIOMUX_INTROUTER0_IN_IN_177	GPIO0_GPIO_OUT_91
	MAIN_GPIOMUX_INTROUTER0_IN_IN_180	GPIO1_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_181	GPIO1_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_182	GPIO1_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_183	GPIO1_GPIO_BANK_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_184	GPIO1_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_190	GPIO0_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_191	GPIO0_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_192	GPIO0_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_193	GPIO0_GPIO_BANK_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_194	GPIO0_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_195	GPIO0_GPIO_BANK_OUT_5
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_0	MCU_GPIO0_GPIO_OUT_0
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_1	MCU_GPIO0_GPIO_OUT_1
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_2	MCU_GPIO0_GPIO_OUT_2
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_3	MCU_GPIO0_GPIO_OUT_3
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_4	MCU_GPIO0_GPIO_OUT_4
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_5	MCU_GPIO0_GPIO_OUT_5
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_6	MCU_GPIO0_GPIO_OUT_6
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_7	MCU_GPIO0_GPIO_OUT_7
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_8	MCU_GPIO0_GPIO_OUT_8
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_9	MCU_GPIO0_GPIO_OUT_9
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_10	MCU_GPIO0_GPIO_OUT_10
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_11	MCU_GPIO0_GPIO_OUT_11
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_12	MCU_GPIO0_GPIO_OUT_12
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_13	MCU_GPIO0_GPIO_OUT_13
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_14	MCU_GPIO0_GPIO_OUT_14
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_15	MCU_GPIO0_GPIO_OUT_15

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_16	MCU_GPIO0_GPIO_OUT_16
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_17	MCU_GPIO0_GPIO_OUT_17
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_18	MCU_GPIO0_GPIO_OUT_18
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_19	MCU_GPIO0_GPIO_OUT_19
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_20	MCU_GPIO0_GPIO_OUT_20
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_21	MCU_GPIO0_GPIO_OUT_21
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_22	MCU_GPIO0_GPIO_OUT_22
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_23	MCU_GPIO0_GPIO_OUT_23
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_30	MCU_GPIO0_GPIO_BANK_OUT_0
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_31	MCU_GPIO0_GPIO_BANK_OUT_1
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_IN_IN_0	TIMER0_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_1	TIMER1_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_2	TIMER2_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_3	TIMER3_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_8	EPWM0_EPWM_SYNCO_O_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_11	WKUP_GTC0_GTC_PUSH_EVENT_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_16	CPSW0_CPTS_GENF0_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_17	CPSW0_CPTS_GENF1_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_18	CPSW0_CPTS_SYNC_OUT_0
CPSW0	CPSW0_CPTS_HW1_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_10
	CPSW0_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_11
	CPSW0_CPTS_HW3_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_12
	CPSW0_CPTS_HW4_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_13
	CPSW0_CPTS_HW5_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_14
	CPSW0_CPTS_HW6_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_15
	CPSW0_CPTS_HW7_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_16
	CPSW0_CPTS_HW8_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_17
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_24
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1	CMP_EVENT_INTROUTER0_OUTP_OUT_25
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2	CMP_EVENT_INTROUTER0_OUTP_OUT_26
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3	CMP_EVENT_INTROUTER0_OUTP_OUT_27

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4	CMP_EVENT_INTROUTER0_OUTP_OUT_28
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5	CMP_EVENT_INTROUTER0_OUTP_OUT_29
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6	CMP_EVENT_INTROUTER0_OUTP_OUT_30
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7	CMP_EVENT_INTROUTER0_OUTP_OUT_31
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_1
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_2
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_3
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_4
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_5
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_6
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_7
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_26	GPMC0_GPMC_SDMAREQ_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27	DEBUGSS0_DAVDMA_LEVEL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28	MCRC64_0_DMA_EVENT_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29	MCRC64_0_DMA_EVENT_OUT_1
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30	MCRC64_0_DMA_EVENT_OUT_2
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31	MCRC64_0_DMA_EVENT_OUT_3
ESM0	ESM0_ESM_LVL_EVENT_IN_1	ECC_AGGR0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_2	ECC_AGGR0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_3	CPSW0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_5	MSRAM_64K0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_6	MSRAM_64K0_ECC_UNCORR_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_8	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_9	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_10	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_11	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_12	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_13	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_15	PDMA0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_16	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_17	PLLFRACF2_SSMOD_16FFT5_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_18	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_20	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_21	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_22	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_23	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_24	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_25	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_26	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_28	PDMA1_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_29	PSRAMECC0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_30	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_32	USB0_HOST_SYSTEM_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_33	USB1_HOST_SYSTEM_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_34	MMCSD2_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_35	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_36	MMCSD2_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_37	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_38	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_39	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_40	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_42	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_44	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_45	A53SS0_ECC_ECCAGGR2_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_46	A53SS0_ECC_ECCAGGR2_UNCORRECTED_ERR_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_47	A53SS0_ECC_ECCAGGR3_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_48	A53SS0_ECC_ECCAGGR3_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_49	MMCSD2_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_54	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_55	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_56	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_57	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_58	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_59	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_60	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_61	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_65	MMCSD2_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_67	CPSW0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_74	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_75	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_78	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_79	DCC6_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_88	PDMA0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_89	PDMA1_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_90	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_91	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_93	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_94	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_95	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_98	DFTSS0_DFT_SAFETY_123_OUT_0
	ESM0_ESM_LVL_EVENT_IN_99	DFTSS0_DFT_SAFETY_MULTI_OUT_0
	ESM0_ESM_LVL_EVENT_IN_100	DFTSS0_DFT_SAFETY_ONE_OUT_0
	ESM0_ESM_LVL_EVENT_IN_101	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_102	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_104	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_105	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_106	ECC_AGGR1_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_107	ECC_AGGR1_UNCORR_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_108	PSRAMECC1_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_109	PSRAMECC1_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_111	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_112	DCC0_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_113	DCC1_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_114	DCC2_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_115	DCC3_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_116	DCC4_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_117	DCC5_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_118	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_119	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_120	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_121	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_124	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_128	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_129	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_130	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_131	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_132	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_133	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_134	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_135	HFOSC0_CLKLOSS_DETECT_CIRCUIT_REF_CLK_LOSS_DETECT_OUT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_136	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_137	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_138	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_139	WKUP_VTM0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_140	WKUP_VTM0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_141	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_144	A53SS0_EXTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_145	A53SS0_INTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_146	USB1_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_147	USB1_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_149	C7X256V0_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_152	MCU_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_157	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_158	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_159	WKUP_PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_160	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_161	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1
	ESM0_ESM_LVL_EVENT_IN_162	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2
	ESM0_ESM_LVL_EVENT_IN_163	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3
	ESM0_ESM_LVL_EVENT_IN_164	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4
	ESM0_ESM_LVL_EVENT_IN_165	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5
	ESM0_ESM_LVL_EVENT_IN_166	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6
	ESM0_ESM_LVL_EVENT_IN_167	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7
	ESM0_ESM_LVL_EVENT_IN_174	DDR32SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_175	DDR32SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_176	DDR32SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_192	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_193	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_194	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_195	WKUP_RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_196	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_198	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_199	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_201	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_202	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_203	MCU_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_204	RTI4_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_208	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_209	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_210	RTI3_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_192	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_193	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_194	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_195	WKUP_RTI0_INTR_WWD_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_PLS_EVENT1_IN_196	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_198	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_199	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_201	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_202	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_203	MCU_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_204	RTI4_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_208	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_209	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_210	RTI3_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_192	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_193	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_194	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_195	WKUP_RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_196	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_198	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_199	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_201	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_202	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_203	MCU_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_204	RTI4_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_208	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_209	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_210	RTI3_INTR_WWD_OUT_0
WKUP_ESM0	WKUP_ESM0_ESM_LVL_EVENT_IN_0	ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_1	ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_2	ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_4	MCU_R5FSS0_CPU0_ECC_AGGR_0_CPU0_ECC_CORRECTED_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_5	MCU_R5FSS0_CPU0_ECC_AGGR_0_CPU0_ECC_UNCORRECTED_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_8	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_9	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_10	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_11	WKUP_VTM0_CORR_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_LVL_EVENT_IN_12	WKUP_VTM0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_13	HFOSC0_CLKLOSS_DETECT_CIRCUIT_REF_CLK_LOSS_DETECT_OUT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_14	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_15	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_16	MCU_MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_17	MCU_MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_18	MCU_MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_19	MCU_MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_20	WKUP_ECC_AGGR2_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_21	WKUP_ECC_AGGR2_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_23	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_24	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_26	WKUP_TIMEOUT1_TIMED_OUT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_26	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_27	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_28	MCU_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_29	MCU_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_30	MCU_R5FSS0_CORE0_CPU0_EXP_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_32	MCU_MSRAM_256K0_ECC_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_33	MCU_MSRAM_256K0_ECC_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_34	MCU_MSRAM_256K1_ECC_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_35	MCU_MSRAM_256K1_ECC_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_36	MCU_DCC1_INTR_ERR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_37	MCU_DCC0_INTR_ERR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_38	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_39	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_40	MCU_ECC_AGGR1_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_41	MCU_ECC_AGGR1_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_42	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_43	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_54	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_55	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_56	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_LVL_EVENT_IN_57	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_58	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_59	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_60	PLLFRACF2_SSMOD_16FFT5_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_61	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_63	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT0_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT0_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT0_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT0_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT0_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT0_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_ESM0_ESM_PLS_EVENT1_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT1_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_PLS_EVENT1_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT1_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT1_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT1_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT1_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_ESM0_ESM_PLS_EVENT2_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT2_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT2_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT2_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT2_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT2_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT2_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_PPI0_0_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_0_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_0_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_0_IN_22	A53SS0_COMMIRQ0_OUT_0
	GICSS0_PPI0_0_IN_23	A53SS0_PMUIRQ0_OUT_0
	GICSS0_PPI0_0_IN_24	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_0_IN_25	A53SS0_VCPUMNTIRQ0_OUT_0
	GICSS0_PPI0_0_IN_26	A53SS0_CNTHPIRQ0_OUT_0
	GICSS0_PPI0_0_IN_27	A53SS0_CNTVIRQ0_OUT_0
	GICSS0_PPI0_0_IN_29	A53SS0_CNTPSIRQ0_OUT_0
	GICSS0_PPI0_0_IN_30	A53SS0_CNTPNSIRQ0_OUT_0
	GICSS0_PPI0_1_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_1_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_1_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_1_IN_22	A53SS0_COMMIRQ1_OUT_0
	GICSS0_PPI0_1_IN_23	A53SS0_PMUIRQ1_OUT_0
	GICSS0_PPI0_1_IN_24	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_1_IN_25	A53SS0_VCPUMNTIRQ1_OUT_0
	GICSS0_PPI0_1_IN_26	A53SS0_CNTHPIRQ1_OUT_0
	GICSS0_PPI0_1_IN_27	A53SS0_CNTVIRQ1_OUT_0
	GICSS0_PPI0_1_IN_29	A53SS0_CNTPSIRQ1_OUT_0
	GICSS0_PPI0_1_IN_30	A53SS0_CNTPNSIRQ1_OUT_0
	GICSS0_PPI0_2_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_2_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_2_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_2_IN_22	A53SS0_COMMIRQ2_OUT_0
	GICSS0_PPI0_2_IN_23	A53SS0_PMUIRQ2_OUT_0
	GICSS0_PPI0_2_IN_24	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_2_IN_25	A53SS0_VCPUMNTIRQ2_OUT_0
	GICSS0_PPI0_2_IN_26	A53SS0_CNTHPIRQ2_OUT_0
	GICSS0_PPI0_2_IN_27	A53SS0_CNTVIRQ2_OUT_0
	GICSS0_PPI0_2_IN_29	A53SS0_CNTPSIRQ2_OUT_0
	GICSS0_PPI0_2_IN_30	A53SS0_CNTPNSIRQ2_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_PPI0_3_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_3_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_3_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_3_IN_22	A53SS0_COMMIRQ3_OUT_0
	GICSS0_PPI0_3_IN_23	A53SS0_PMUIRQ3_OUT_0
	GICSS0_PPI0_3_IN_24	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_3_IN_25	A53SS0_VCPUMNTIRQ3_OUT_0
	GICSS0_PPI0_3_IN_26	A53SS0_CNTHPIRQ3_OUT_0
	GICSS0_PPI0_3_IN_27	A53SS0_CNTVIRQ3_OUT_0
	GICSS0_PPI0_3_IN_29	A53SS0_CNTPSIRQ3_OUT_0
	GICSS0_PPI0_3_IN_30	A53SS0_CNTPNSIRQ3_OUT_0
	GICSS0_SPI_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	GICSS0_SPI_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	GICSS0_SPI_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_5

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_56	CMP_EVENT_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_57	CMP_EVENT_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_58	CMP_EVENT_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_59	CMP_EVENT_INTROUTER0_OUTP_OUT_11
	GICSS0_SPI_IN_60	CMP_EVENT_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_61	CMP_EVENT_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_62	CMP_EVENT_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_63	CMP_EVENT_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
	GICSS0_SPI_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
	GICSS0_SPI_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
	GICSS0_SPI_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
	GICSS0_SPI_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
	GICSS0_SPI_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
	GICSS0_SPI_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
	GICSS0_SPI_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
	GICSS0_SPI_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
	GICSS0_SPI_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
	GICSS0_SPI_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
	GICSS0_SPI_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
	GICSS0_SPI_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
	GICSS0_SPI_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
	GICSS0_SPI_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
	GICSS0_SPI_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
	GICSS0_SPI_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
	GICSS0_SPI_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
	GICSS0_SPI_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
	GICSS0_SPI_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
	GICSS0_SPI_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
	GICSS0_SPI_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
	GICSS0_SPI_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
	GICSS0_SPI_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
	GICSS0_SPI_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
	GICSS0_SPI_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
	GICSS0_SPI_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
	GICSS0_SPI_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
	GICSS0_SPI_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
	GICSS0_SPI_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
	GICSS0_SPI_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
	GICSS0_SPI_IN_96	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
	GICSS0_SPI_IN_97	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
	GICSS0_SPI_IN_98	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
	GICSS0_SPI_IN_99	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
	GICSS0_SPI_IN_100	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
	GICSS0_SPI_IN_101	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
	GICSS0_SPI_IN_102	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
	GICSS0_SPI_IN_103	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
	GICSS0_SPI_IN_104	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_105	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_106	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_107	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_108	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_0
	GICSS0_SPI_IN_109	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_0
	GICSS0_SPI_IN_112	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4
	GICSS0_SPI_IN_113	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5
	GICSS0_SPI_IN_114	MMCSD2_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_115	MMCSD1_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_128	DCC0_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC1_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC2_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC3_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC4_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC5_INTR_DONE_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_128	DCC6_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_129	CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_132	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	GICSS0_SPI_IN_133	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_134	CPSW0_EVNT_PEND_OUT_0
	GICSS0_SPI_IN_135	CPSW0_MDIO_PEND_OUT_0
	GICSS0_SPI_IN_136	CPSW0_STAT_PEND_OUT_0
	GICSS0_SPI_IN_138	GPMC0_GPMC_SINTERRUPT_OUT_0
	GICSS0_SPI_IN_139	MCU_I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_140	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_0
	GICSS0_SPI_IN_141	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_0
	GICSS0_SPI_IN_145	ECAP0_ECAP_INT_OUT_0
	GICSS0_SPI_IN_146	ECAP1_ECAP_INT_OUT_0
	GICSS0_SPI_IN_147	ECAP2_ECAP_INT_OUT_0
	GICSS0_SPI_IN_148	EQEP0_EQEP_INT_OUT_0
	GICSS0_SPI_IN_149	EQEP1_EQEP_INT_OUT_0
	GICSS0_SPI_IN_150	EQEP2_EQEP_INT_OUT_0
	GICSS0_SPI_IN_151	DDR32SS0_DDRSS_CONTROLLER_OUT_0
	GICSS0_SPI_IN_152	TIMER0_INTR_PEND_OUT_0
	GICSS0_SPI_IN_153	TIMER1_INTR_PEND_OUT_0
	GICSS0_SPI_IN_154	TIMER2_INTR_PEND_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_155	TIMER3_INTR_PEND_OUT_0
	GICSS0_SPI_IN_156	TIMER4_INTR_PEND_OUT_0
	GICSS0_SPI_IN_157	TIMER5_INTR_PEND_OUT_0
	GICSS0_SPI_IN_158	TIMER6_INTR_PEND_OUT_0
	GICSS0_SPI_IN_159	TIMER7_INTR_PEND_OUT_0
	GICSS0_SPI_IN_160	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	GICSS0_SPI_IN_161	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	GICSS0_SPI_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	GICSS0_SPI_IN_165	MMCSD0_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_166	MCRC64_0_INT_MCRC_OUT_0
	GICSS0_SPI_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	GICSS0_SPI_IN_172	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	GICSS0_SPI_IN_177	DDPA0_DDPA_INTR_OUT_0
	GICSS0_SPI_IN_180	ESM0_ESM_INT_CFG_LVL_OUT_0
	GICSS0_SPI_IN_181	ESM0_ESM_INT_HI_LVL_OUT_0
	GICSS0_SPI_IN_182	ESM0_ESM_INT_LOW_LVL_OUT_0
	GICSS0_SPI_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	GICSS0_SPI_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	GICSS0_SPI_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	GICSS0_SPI_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	GICSS0_SPI_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	GICSS0_SPI_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	GICSS0_SPI_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	GICSS0_SPI_IN_193	I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_194	I2C1_POINTRPEND_OUT_0
	GICSS0_SPI_IN_195	I2C2_POINTRPEND_OUT_0
	GICSS0_SPI_IN_196	I2C3_POINTRPEND_OUT_0
	GICSS0_SPI_IN_197	WKUP_I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	GICSS0_SPI_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	GICSS0_SPI_IN_203	PSC0_PSC_ALLINT_OUT_0
	GICSS0_SPI_IN_204	MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_205	MCSPI1_INTR_SPI_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_206	MCSPI2_INTR_SPI_OUT_0
	GICSS0_SPI_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	GICSS0_SPI_IN_210	UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_211	UART1_USART_IRQ_OUT_0
	GICSS0_SPI_IN_212	UART2_USART_IRQ_OUT_0
	GICSS0_SPI_IN_213	UART3_USART_IRQ_OUT_0
	GICSS0_SPI_IN_214	UART4_USART_IRQ_OUT_0
	GICSS0_SPI_IN_215	UART5_USART_IRQ_OUT_0
	GICSS0_SPI_IN_216	UART6_USART_IRQ_OUT_0
	GICSS0_SPI_IN_217	MCU_UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_218	WKUP_UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_220	USB0_IRQ_OUT_0
	GICSS0_SPI_IN_221	USB0_IRQ_OUT_1
	GICSS0_SPI_IN_222	USB0_IRQ_OUT_2
	GICSS0_SPI_IN_223	USB0_IRQ_OUT_3
	GICSS0_SPI_IN_224	USB0_IRQ_OUT_4
	GICSS0_SPI_IN_225	USB0_IRQ_OUT_5
	GICSS0_SPI_IN_226	USB0_IRQ_OUT_6
	GICSS0_SPI_IN_227	USB0_IRQ_OUT_7
	GICSS0_SPI_IN_228	USB0_MISC_LEVEL_OUT_0
	GICSS0_SPI_IN_229	EPWM0_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_230	EPWM0_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_231	EPWM1_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_233	EPWM1_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_234	EPWM2_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_235	EPWM2_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_252	RTI0_INTR_WWD_OUT_0
	GICSS0_SPI_IN_253	RTI1_INTR_WWD_OUT_0
	GICSS0_SPI_IN_254	RTI2_INTR_WWD_OUT_0
	GICSS0_SPI_IN_255	RTI3_INTR_WWD_OUT_0
	GICSS0_SPI_IN_256	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	GICSS0_SPI_IN_258	USB1_IRQ_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_259	USB1_IRQ_OUT_1
	GICSS0_SPI_IN_260	USB1_IRQ_OUT_2
	GICSS0_SPI_IN_261	USB1_IRQ_OUT_3
	GICSS0_SPI_IN_262	USB1_IRQ_OUT_4
	GICSS0_SPI_IN_263	USB1_IRQ_OUT_5
	GICSS0_SPI_IN_264	USB1_IRQ_OUT_6
	GICSS0_SPI_IN_265	USB1_IRQ_OUT_7
	GICSS0_SPI_IN_266	USB1_MISC_LEVEL_OUT_0
	GICSS0_SPI_IN_267	MCASP0_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_268	MCASP0_XMIT_INTR_PEND_OUT_0
	GICSS0_SPI_IN_269	MCASP1_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_270	MCASP1_XMIT_INTR_PEND_OUT_0
	GICSS0_SPI_IN_271	MCASP2_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_272	MCASP2_XMIT_INTR_PEND_OUT_0
	GICSS0_SPI_IN_280	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0
	GICSS0_SPI_IN_281	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1
	GICSS0_SPI_IN_282	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2
	GICSS0_SPI_IN_283	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3
	GICSS0_SPI_IN_284	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4
	GICSS0_SPI_IN_285	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5
	GICSS0_SPI_IN_286	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6
	GICSS0_SPI_IN_287	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7
EPWM0	EPWM0_EPWM_SYNCIN_IN_0	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0
	EPWM0_EPWM_SYNCIN_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_32
	EPWM0_EPWM_SYNCIN_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_19
EPWM1	EPWM1_EPWM_SYNCIN_IN_0	EPWM0_EPWM_SYNCOUT_OUT_0
EPWM2	EPWM2_EPWM_SYNCIN_IN_0	EPWM1_EPWM_SYNCOUT_OUT_0
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_4	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_5	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_6	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73
	WKUP_R5FSS0_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74
	WKUP_R5FSS0_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75
	WKUP_R5FSS0_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76
	WKUP_R5FSS0_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77
	WKUP_R5FSS0_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78
	WKUP_R5FSS0_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79
	WKUP_R5FSS0_CORE0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_18	MCU_GPIO0_GPIO_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_23	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_27	WKUP_DEEPSLEEP_SOURCES0_WAKEUP_EVENT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_28	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_29	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_30	WKUP_RTI0_INTR_WWD_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_R5FSS0_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_R5FSS0_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_R5FSS0_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_R5FSS0_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	WKUP_R5FSS0_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	WKUP_R5FSS0_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	WKUP_R5FSS0_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	WKUP_R5FSS0_CORE0_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_16
	WKUP_R5FSS0_CORE0_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_17

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_18
	WKUP_R5FSS0_CORE0_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_19
	WKUP_R5FSS0_CORE0_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_20
	WKUP_R5FSS0_CORE0_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_21
	WKUP_R5FSS0_CORE0_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_22
	WKUP_R5FSS0_CORE0_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_23
	WKUP_R5FSS0_CORE0_INTR_IN_56	GPIO0_GPIO_BANK_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_57	GPIO0_GPIO_BANK_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_58	WKUP_R5FSS0_CORE0_PMU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_59	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_60	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_61	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_62	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
	WKUP_R5FSS0_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
	WKUP_R5FSS0_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42
	WKUP_R5FSS0_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
	WKUP_R5FSS0_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
	WKUP_R5FSS0_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45
	WKUP_R5FSS0_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
	WKUP_R5FSS0_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
	WKUP_R5FSS0_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
	WKUP_R5FSS0_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
	WKUP_R5FSS0_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
	WKUP_R5FSS0_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
	WKUP_R5FSS0_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
	WKUP_R5FSS0_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
	WKUP_R5FSS0_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
	WKUP_R5FSS0_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
	WKUP_R5FSS0_CORE0_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
	WKUP_R5FSS0_CORE0_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
	WKUP_R5FSS0_CORE0_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
	WKUP_R5FSS0_CORE0_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
	WKUP_R5FSS0_CORE0_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
	WKUP_R5FSS0_CORE0_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
	WKUP_R5FSS0_CORE0_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
	WKUP_R5FSS0_CORE0_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
	WKUP_R5FSS0_CORE0_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
	WKUP_R5FSS0_CORE0_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
	WKUP_R5FSS0_CORE0_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
	WKUP_R5FSS0_CORE0_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
	WKUP_R5FSS0_CORE0_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69
	WKUP_R5FSS0_CORE0_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70
	WKUP_R5FSS0_CORE0_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
	WKUP_R5FSS0_CORE0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_98	MCASP0_REC_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_99	MCASP0_XMIT_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_103	GPMC0_GPMC_SINTERRUPT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_104	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_105	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_106	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_107	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_110	MCU_PBIST0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_113	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_114	PBIST0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_115	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_116	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_118	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_120	ECAP0_ECAP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_121	ECAP1_ECAP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_122	ECAP2_ECAP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_123	EPWM0_EPWM_ETINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_124	EPWM0_EPWM_TRIPZINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_125	EPWM1_EPWM_ETINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_126	EPWM1_EPWM_TRIPZINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_127	EPWM2_EPWM_ETINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	CTRL_MMR0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_138	WKUP_TIMER0_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_139	WKUP_TIMER1_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_143	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_144	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_146	PSC0_PSC_ALLINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_148	EPWM2_EPWM_TRIPZINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_151	DDR32SS0_DDRSS_CONTROLLER_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_152	WKUP_TIMEOUT1_TIMED_OUT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_152	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_153	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_154	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_155	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_156	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_157	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_162	MMCSD1_EMMCSDSS_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_163	MMCSD2_EMMCSDSS_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_165	MCASP1_REC_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_166	MCASP1_XMIT_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_170	MCASP2_REC_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_175	WKUP_R5FSS0_CORE0_CTI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_181	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_197	MCU_I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_198	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_199	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_200	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_207	MCU_MCSPI0_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_208	MCU_MCSPI1_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_209	MCASP2_XMIT_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_224	USB0_IRQ_OUT_4

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_230	USB1_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_231	USB1_IRQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_232	USB1_IRQ_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_233	USB1_IRQ_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_234	USB1_IRQ_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_235	USB1_IRQ_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_236	USB1_IRQ_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_237	USB1_IRQ_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_238	USB1_MISC_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_239	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_244	EQEP0_EQEP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_245	EQEP1_EQEP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_246	EQEP2_EQEP_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_247	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_248	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12
	WKUP_R5FSS0_CORE0_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13
	WKUP_R5FSS0_CORE0_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14
	WKUP_R5FSS0_CORE0_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_4	MCU_R5FSS0_CORE0_CPU0_EXP_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_28	MCU_TIMER0_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_29	MCU_TIMER1_INTR_PEND_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_30	MCU_RTI0_INTR_WWD_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_31	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_36	EPWM0_EPWM_ETINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_37	EPWM1_EPWM_ETINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_38	EPWM2_EPWM_ETINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39	CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_42	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_43	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_44	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_45	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_46	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_47	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_58	CMP_EVENT_INTROUTER0_OUTP_OUT_34
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_59	CMP_EVENT_INTROUTER0_OUTP_OUT_35
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_60	CMP_EVENT_INTROUTER0_OUTP_OUT_36
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_61	CMP_EVENT_INTROUTER0_OUTP_OUT_37
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_80	EPWM0_EPWM_TRIPZINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_81	EPWM1_EPWM_TRIPZINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_82	EPWM2_EPWM_TRIPZINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_83	ECAP0_ECAP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_84	ECAP1_ECAP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_85	ECAP2_ECAP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_86	EQEP0_EQEP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_87	EQEP1_EQEP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_88	EQEP2_EQEP_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_90	MCU_R5FSS0_CORE0_COMMRX_LEVEL_0_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_91	MCU_R5FSS0_CORE0_COMMTX_LEVEL_0_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_94	MCU_R5FSS0_CORE0_CPU0_PMU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_95	MCU_R5FSS0_CORE0_CPU0_VALFIQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_96	MCU_R5FSS0_CORE0_CPU0_VALIRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_103	GPMC0_GPMC_SINTERRUPT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_104	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_105	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_106	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_107	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_110	MCU_PBIST0_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_113	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_114	PBIST0_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_115	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_116	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_118	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_120	MCASP0_REC_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_121	MCASP0_XMIT_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_122	MCASP1_REC_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_123	MCASP1_XMIT_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_124	MCASP2_REC_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_125	MCASP2_XMIT_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128	CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_138	MCU_TIMER2_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_139	MCU_TIMER3_INTR_PEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_146	PSC0_PSC_ALLINT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_151	DDR32SS0_DDRSS_CONTROLLER_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_152	WKUP_TIMEOUT1_TIMED_OUT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_152	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_153	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_162	MMCSD1_EMMCSDSS_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_163	MMCSD2_EMMCSDSS_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_175	MCU_R5FSS0_CORE0_CPU0_CTI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_181	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_196	I2C3_POINTRPEND_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_197	MCU_I2C0_POINTRPEND_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_207	MCU_MCSPI0_INTR_SPI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_208	MCU_MCSPI1_INTR_SPI_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_210	UART0_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_211	UART1_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_212	UART2_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_213	UART3_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_214	UART4_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_215	UART5_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_216	UART6_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_220	USB0_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_221	USB0_IRQ_OUT_1
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_222	USB0_IRQ_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_223	USB0_IRQ_OUT_3
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_224	USB0_IRQ_OUT_4
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_225	USB0_IRQ_OUT_5
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_226	USB0_IRQ_OUT_6
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_227	USB0_IRQ_OUT_7
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_230	USB1_IRQ_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_231	USB1_IRQ_OUT_1
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_232	USB1_IRQ_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_233	USB1_IRQ_OUT_3
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_234	USB1_IRQ_OUT_4
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_235	USB1_IRQ_OUT_5

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_236	USB1_IRQ_OUT_6
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_237	USB1_IRQ_OUT_7
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_238	USB1_MISC_LEVEL_OUT_0
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_2
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10
	MCU_R5FSS0_CORE0_CPU0_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11
WKUP_DEEPSLEEP_SOURCES0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_0	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_1	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_2	MCU_GPIO0_GPIO_LVL_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_3	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_5	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_6	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_7	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_9	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_10	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
PDMA2	PDMA2_MCASP_MAIN_0_RX_IN_0	MCASP0_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_0_TX_IN_0	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_1_RX_IN_0	MCASP1_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_1_TX_IN_0	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_2_RX_IN_0	MCASP2_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_2_TX_IN_0	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0
PDMA0	PDMA0_MCANSS_MAIN_0_FE_IN_0	MCAN0_MCANSS_FE_OUT_0
	PDMA0_MCANSS_MAIN_0_FE_IN_1	MCAN0_MCANSS_FE_OUT_1
	PDMA0_MCANSS_MAIN_0_FE_IN_2	MCAN0_MCANSS_FE_OUT_2
	PDMA0_MCANSS_MAIN_0_TX_IN_0	MCAN0_MCANSS_TX_DMA_OUT_0
	PDMA0_MCANSS_MAIN_0_TX_IN_1	MCAN0_MCANSS_TX_DMA_OUT_1
	PDMA0_MCANSS_MAIN_0_TX_IN_2	MCAN0_MCANSS_TX_DMA_OUT_2
	PDMA0_SPI_MAIN_0_RX_IN_0	MCSPI0_DMA_READ_EVENT_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PDMA0	PDMA0_SPI_MAIN_0_RX_IN_1	MCSPI0_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_RX_IN_2	MCSPI0_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_RX_IN_3	MCSPI0_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_0_TX_IN_0	MCSPI0_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_0_TX_IN_1	MCSPI0_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_TX_IN_2	MCSPI0_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_TX_IN_3	MCSPI0_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_RX_IN_0	MCSPI1_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_RX_IN_1	MCSPI1_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_RX_IN_2	MCSPI1_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_RX_IN_3	MCSPI1_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_TX_IN_0	MCSPI1_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_TX_IN_1	MCSPI1_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_TX_IN_2	MCSPI1_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_TX_IN_3	MCSPI1_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_2_RX_IN_0	MCSPI2_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_RX_IN_1	MCSPI2_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_RX_IN_2	MCSPI2_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_RX_IN_3	MCSPI2_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_2_TX_IN_0	MCSPI2_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_TX_IN_1	MCSPI2_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_TX_IN_2	MCSPI2_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_TX_IN_3	MCSPI2_DMA_WRITE_EVENT_OUT_3
PDMA1	PDMA1_USART_MAIN_0_RX_IN_0	UART0_USART_DMA_OUT_1
	PDMA1_USART_MAIN_0_TX_IN_0	UART0_USART_DMA_OUT_0
	PDMA1_USART_MAIN_1_RX_IN_0	UART1_USART_DMA_OUT_1
	PDMA1_USART_MAIN_1_TX_IN_0	UART1_USART_DMA_OUT_0
	PDMA1_USART_MAIN_2_RX_IN_0	UART2_USART_DMA_OUT_1
	PDMA1_USART_MAIN_2_TX_IN_0	UART2_USART_DMA_OUT_0
	PDMA1_USART_MAIN_3_RX_IN_0	UART3_USART_DMA_OUT_1
	PDMA1_USART_MAIN_3_TX_IN_0	UART3_USART_DMA_OUT_0
	PDMA1_USART_MAIN_4_RX_IN_0	UART4_USART_DMA_OUT_1
	PDMA1_USART_MAIN_4_TX_IN_0	UART4_USART_DMA_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PDMA1	PDMA1_USART_MAIN_5_RX_IN_0	UART5_USART_DMA_OUT_1
	PDMA1_USART_MAIN_5_TX_IN_0	UART5_USART_DMA_OUT_0
	PDMA1_USART_MAIN_6_RX_IN_0	UART6_USART_DMA_OUT_1
	PDMA1_USART_MAIN_6_TX_IN_0	UART6_USART_DMA_OUT_0
COMPUTE_CLUSTER0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTI_IN_0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTO_OUT_0
	COMPUTE_CLUSTER0_CPU_EVNT_EVENTI_IN_0	C7X256V0_CLEC_ARM_0_EVENTI_OUT_OUT_0
C7X256V0_CLEC	C7X256V0_CLEC_ARM_0_EVENTO_IN_IN_0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTO_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_6	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	C7X256V0_CLEC_GIC_SPI_IN_7	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	C7X256V0_CLEC_GIC_SPI_IN_8	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	C7X256V0_CLEC_GIC_SPI_IN_9	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	C7X256V0_CLEC_GIC_SPI_IN_10	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	C7X256V0_CLEC_GIC_SPI_IN_11	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	C7X256V0_CLEC_GIC_SPI_IN_12	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	C7X256V0_CLEC_GIC_SPI_IN_13	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	C7X256V0_CLEC_GIC_SPI_IN_14	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	C7X256V0_CLEC_GIC_SPI_IN_15	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	C7X256V0_CLEC_GIC_SPI_IN_16	CMP_EVENT_INTROUTER0_OUTP_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_17	CMP_EVENT_INTROUTER0_OUTP_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_18	CMP_EVENT_INTROUTER0_OUTP_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_19	CMP_EVENT_INTROUTER0_OUTP_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_20	CMP_EVENT_INTROUTER0_OUTP_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_21	CMP_EVENT_INTROUTER0_OUTP_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_22	CMP_EVENT_INTROUTER0_OUTP_OUT_6
	C7X256V0_CLEC_GIC_SPI_IN_23	CMP_EVENT_INTROUTER0_OUTP_OUT_7
	C7X256V0_CLEC_GIC_SPI_IN_24	CMP_EVENT_INTROUTER0_OUTP_OUT_8
	C7X256V0_CLEC_GIC_SPI_IN_25	CMP_EVENT_INTROUTER0_OUTP_OUT_9

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_26	CMP_EVENT_INTROUTER0_OUTP_OUT_10
	C7X256V0_CLEC_GIC_SPI_IN_27	CMP_EVENT_INTROUTER0_OUTP_OUT_11
	C7X256V0_CLEC_GIC_SPI_IN_28	CMP_EVENT_INTROUTER0_OUTP_OUT_12
	C7X256V0_CLEC_GIC_SPI_IN_29	CMP_EVENT_INTROUTER0_OUTP_OUT_13
	C7X256V0_CLEC_GIC_SPI_IN_30	CMP_EVENT_INTROUTER0_OUTP_OUT_14
	C7X256V0_CLEC_GIC_SPI_IN_31	CMP_EVENT_INTROUTER0_OUTP_OUT_15
	C7X256V0_CLEC_GIC_SPI_IN_32	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_33	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_34	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_35	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_36	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_37	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_38	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
	C7X256V0_CLEC_GIC_SPI_IN_39	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
	C7X256V0_CLEC_GIC_SPI_IN_40	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
	C7X256V0_CLEC_GIC_SPI_IN_41	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
	C7X256V0_CLEC_GIC_SPI_IN_42	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
	C7X256V0_CLEC_GIC_SPI_IN_43	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
	C7X256V0_CLEC_GIC_SPI_IN_44	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
	C7X256V0_CLEC_GIC_SPI_IN_45	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
	C7X256V0_CLEC_GIC_SPI_IN_46	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
	C7X256V0_CLEC_GIC_SPI_IN_47	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
	C7X256V0_CLEC_GIC_SPI_IN_48	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
	C7X256V0_CLEC_GIC_SPI_IN_49	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
	C7X256V0_CLEC_GIC_SPI_IN_50	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
	C7X256V0_CLEC_GIC_SPI_IN_51	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
	C7X256V0_CLEC_GIC_SPI_IN_52	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
	C7X256V0_CLEC_GIC_SPI_IN_53	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
	C7X256V0_CLEC_GIC_SPI_IN_54	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
	C7X256V0_CLEC_GIC_SPI_IN_55	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
	C7X256V0_CLEC_GIC_SPI_IN_56	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
	C7X256V0_CLEC_GIC_SPI_IN_57	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
	C7X256V0_CLEC_GIC_SPI_IN_58	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_59	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
	C7X256V0_CLEC_GIC_SPI_IN_60	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
	C7X256V0_CLEC_GIC_SPI_IN_61	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
	C7X256V0_CLEC_GIC_SPI_IN_62	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
	C7X256V0_CLEC_GIC_SPI_IN_63	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
	C7X256V0_CLEC_GIC_SPI_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
	C7X256V0_CLEC_GIC_SPI_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
	C7X256V0_CLEC_GIC_SPI_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
	C7X256V0_CLEC_GIC_SPI_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
	C7X256V0_CLEC_GIC_SPI_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
	C7X256V0_CLEC_GIC_SPI_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
	C7X256V0_CLEC_GIC_SPI_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
	C7X256V0_CLEC_GIC_SPI_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
	C7X256V0_CLEC_GIC_SPI_IN_72	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_73	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_74	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_75	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_76	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_77	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_80	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_81	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_82	MMCSD2_EMMCSDSS_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_83	MMCSD1_EMMCSDSS_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC0_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC1_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC2_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC3_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC4_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC5_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_96	DCC6_INTR_DONE_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_97	CTRL_MMR0_ACCESS_ERR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_97	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_97	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_97	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_97	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_100	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_101	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_102	CPSW0_EVNT_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_103	CPSW0_MDIO_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_104	CPSW0_STAT_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_106	GPMC0_GPMC_SINTERRUPT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_107	MCU_I2C0_POINTRPEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_108	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_109	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_113	ECAP0_ECAP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_114	ECAP1_ECAP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_115	ECAP2_ECAP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_116	EQEP0_EQEP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_117	EQEP1_EQEP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_118	EQEP2_EQEP_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_119	DDR32SS0_DDRSS_CONTROLLER_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_120	TIMER0_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_121	TIMER1_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_122	TIMER2_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_123	TIMER3_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_124	TIMER4_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_125	TIMER5_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_126	TIMER6_INTR_PEND_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_127	TIMER7_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_128	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_129	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_132	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_133	MMCSD0_EMMCSDSS_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_134	MCRC64_0_INT_MCRC_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_140	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_145	DDPA0_DDPA_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_148	ESM0_ESM_INT_CFG_LVL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_149	ESM0_ESM_INT_HI_LVL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_150	ESM0_ESM_INT_LOW_LVL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_151	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_152	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_153	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_154	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_155	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_156	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_160	MCU_MCRC64_0_INT_MCRC_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_161	I2C0_POINTRPEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_162	I2C1_POINTRPEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_163	I2C2_POINTRPEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_164	I2C3_POINTRPEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_169	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_170	DEBUGSS0_CTM_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_171	PSC0_PSC_ALLINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_172	MCSPI0_INTR_SPI_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_173	MCSPI1_INTR_SPI_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_174	MCSPI2_INTR_SPI_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_176	MCU_MCSPI0_INTR_SPI_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_177	MCU_MCSPI1_INTR_SPI_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_178	UART0_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_179	UART1_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_180	UART2_USART_IRQ_OUT_0

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_181	UART3_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_182	UART4_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_183	UART5_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_184	UART6_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_185	MCU_UART0_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_186	WKUP_UART0_USART_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_188	USB0_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_189	USB0_IRQ_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_190	USB0_IRQ_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_191	USB0_IRQ_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_192	USB0_IRQ_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_193	USB0_IRQ_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_194	USB0_IRQ_OUT_6
	C7X256V0_CLEC_GIC_SPI_IN_195	USB0_IRQ_OUT_7
	C7X256V0_CLEC_GIC_SPI_IN_196	USB0_MISC_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_197	EPWM0_EPWM_ETINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_198	EPWM0_EPWM_TRIPZINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_199	EPWM1_EPWM_ETINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_201	EPWM1_EPWM_TRIPZINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_202	EPWM2_EPWM_ETINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_203	EPWM2_EPWM_TRIPZINT_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_220	RTI0_INTR_WWD_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_221	RTI1_INTR_WWD_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_222	RTI2_INTR_WWD_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_223	RTI3_INTR_WWD_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_224	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_226	USB1_IRQ_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_227	USB1_IRQ_OUT_1
	C7X256V0_CLEC_GIC_SPI_IN_228	USB1_IRQ_OUT_2
	C7X256V0_CLEC_GIC_SPI_IN_229	USB1_IRQ_OUT_3
	C7X256V0_CLEC_GIC_SPI_IN_230	USB1_IRQ_OUT_4
	C7X256V0_CLEC_GIC_SPI_IN_231	USB1_IRQ_OUT_5
	C7X256V0_CLEC_GIC_SPI_IN_232	USB1_IRQ_OUT_6

Table 10-6. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_GIC_SPI_IN_233	USB1_IRQ_OUT_7
	C7X256V0_CLEC_GIC_SPI_IN_234	USB1_MISC_LEVEL_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_235	MCASP0_REC_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_236	MCASP0_XMIT_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_237	MCASP1_REC_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_238	MCASP1_XMIT_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_239	MCASP2_REC_INTR_PEND_OUT_0
	C7X256V0_CLEC_GIC_SPI_IN_240	MCASP2_XMIT_INTR_PEND_OUT_0
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_0	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_1
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_1	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_1
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_2	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_1
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_3	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_1
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_4	RTI4_INTR_WWD_OUT_0
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_5	CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_16	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_17	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_18	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_19	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_20	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_21	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_22	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_23	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_24	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_25	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_26	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_27	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_28	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_29	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_30	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98
	C7X256V0_CLEC_SOC_EVENTS_IN_IN_31	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99
USB0	USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0	DEBUGSS0_DAVDMA_LEVEL_OUT_0
USB1	USB1_TRACE_INEP_PKT_BUFF_AVAIL_IN_0	DEBUGSS0_DAVDMA_LEVEL_OUT_0

10.5.2 Interrupts (Outputs)

Table 10-7. Interrupts (Outputs)

Instance	Interrupt Output Line	Destination Interrupt
hfosc0_clkloss_detect_circuit	HFOSC0_CLKLOSS_DETECT_CIRCUIT_REF_CLK_LOSS_DETECT_OUT_OUT_0	ESM0_ESM_LVL_EVENT_IN_135
	HFOSC0_CLKLOSS_DETECT_CIRCUIT_REF_CLK_LOSS_DETECT_OUT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_13
PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_12
PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_13
PINFUNCTION_EHRPWM0_SYNCIin	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0	EPWM0_EPWM_SYNCIN_IN_0
PINFUNCTION_EXTINTnin	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	GICSS0_SPI_IN_256
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_203
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_203
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_224
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_16
	CMP_EVENT_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_17
	CMP_EVENT_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_18
	CMP_EVENT_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_19
	CMP_EVENT_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_20
	CMP_EVENT_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_21
	CMP_EVENT_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_22
	CMP_EVENT_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_23
	CMP_EVENT_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_56
	CMP_EVENT_INTROUTER0_OUTP_OUT_8	C7X256V0_CLEC_GIC_SPI_IN_24
	CMP_EVENT_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_57
	CMP_EVENT_INTROUTER0_OUTP_OUT_9	C7X256V0_CLEC_GIC_SPI_IN_25
	CMP_EVENT_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_58
	CMP_EVENT_INTROUTER0_OUTP_OUT_10	C7X256V0_CLEC_GIC_SPI_IN_26
	CMP_EVENT_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_59
	CMP_EVENT_INTROUTER0_OUTP_OUT_11	C7X256V0_CLEC_GIC_SPI_IN_27

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_60
	CMP_EVENT_INTROUTER0_OUTP_OUT_12	C7X256V0_CLEC_GIC_SPI_IN_28
	CMP_EVENT_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_61
	CMP_EVENT_INTROUTER0_OUTP_OUT_13	C7X256V0_CLEC_GIC_SPI_IN_29
	CMP_EVENT_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_62
	CMP_EVENT_INTROUTER0_OUTP_OUT_14	C7X256V0_CLEC_GIC_SPI_IN_30
	CMP_EVENT_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_63
	CMP_EVENT_INTROUTER0_OUTP_OUT_15	C7X256V0_CLEC_GIC_SPI_IN_31
	CMP_EVENT_INTROUTER0_OUTP_OUT_16	WKUP_R5FSS0_CORE0_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_17	WKUP_R5FSS0_CORE0_INTR_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_18	WKUP_R5FSS0_CORE0_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_19	WKUP_R5FSS0_CORE0_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_20	WKUP_R5FSS0_CORE0_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_21	WKUP_R5FSS0_CORE0_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_22	WKUP_R5FSS0_CORE0_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_23	WKUP_R5FSS0_CORE0_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_24	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_25	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1
	CMP_EVENT_INTROUTER0_OUTP_OUT_26	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2
	CMP_EVENT_INTROUTER0_OUTP_OUT_27	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3
	CMP_EVENT_INTROUTER0_OUTP_OUT_28	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4
	CMP_EVENT_INTROUTER0_OUTP_OUT_29	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5
	CMP_EVENT_INTROUTER0_OUTP_OUT_30	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6
	CMP_EVENT_INTROUTER0_OUTP_OUT_31	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7
	CMP_EVENT_INTROUTER0_OUTP_OUT_32	EPWM0_EPWM_SYNCIN_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_34	MCU_R5FSS0_CORE0_CPU0_INTR_IN_58
	CMP_EVENT_INTROUTER0_OUTP_OUT_35	MCU_R5FSS0_CORE0_CPU0_INTR_IN_59
	CMP_EVENT_INTROUTER0_OUTP_OUT_36	MCU_R5FSS0_CORE0_CPU0_INTR_IN_60
	CMP_EVENT_INTROUTER0_OUTP_OUT_37	MCU_R5FSS0_CORE0_CPU0_INTR_IN_61
CBASS_IPCSS0	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CBASS_CENTRAL2	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
CTRL_MMR0	CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0	C7X256V0_CLEC_SOC_EVENTS_IN_IN_5
	CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39
	CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
	CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128
	CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_97
CBASS0	CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
CBASS_DBG0	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_4

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_6
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_7
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_R5FSS0_CORE0_INTR_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	C7X256V0_CLEC_GIC_SPI_IN_8
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_R5FSS0_CORE0_INTR_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	C7X256V0_CLEC_GIC_SPI_IN_9
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_R5FSS0_CORE0_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	C7X256V0_CLEC_GIC_SPI_IN_10
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_R5FSS0_CORE0_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	C7X256V0_CLEC_GIC_SPI_IN_11
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	WKUP_R5FSS0_CORE0_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	C7X256V0_CLEC_GIC_SPI_IN_12
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	WKUP_R5FSS0_CORE0_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	C7X256V0_CLEC_GIC_SPI_IN_13
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	WKUP_R5FSS0_CORE0_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	C7X256V0_CLEC_GIC_SPI_IN_14
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	WKUP_R5FSS0_CORE0_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	C7X256V0_CLEC_GIC_SPI_IN_15

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34	MCU_R5FSS0_CORE0_CPU0_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35	MCU_R5FSS0_CORE0_CPU0_INTR_IN_33
CBASS_INFRA1	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
CBASS_MCASP0	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
CBASS_MISC_PERI0	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
MCU_CBASS0	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_31
MCU_CTRL_MMR0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_0
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_CTRL_MMR0	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_97
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_104
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_104
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_72
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_105
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_105
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_73
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_106
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_106
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_74
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_107
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_107
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_75
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4	MCU_R5FSS0_CORE0_CPU0_INTR_IN_104
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5	MCU_R5FSS0_CORE0_CPU0_INTR_IN_105
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6	MCU_R5FSS0_CORE0_CPU0_INTR_IN_106
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7	MCU_R5FSS0_CORE0_CPU0_INTR_IN_107
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT0_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT1_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT2_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT0_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT1_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT2_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT0_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT1_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT2_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT0_IN_91
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT1_IN_91
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT2_IN_91
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_4	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_5	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_6	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_7	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_10	CPSW0_CPTS_HW1_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_11	CPSW0_CPTS_HW2_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_12	CPSW0_CPTS_HW3_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_13	CPSW0_CPTS_HW4_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_14	CPSW0_CPTS_HW5_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_15	CPSW0_CPTS_HW6_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_16	CPSW0_CPTS_HW7_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_17	CPSW0_CPTS_HW8_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_19	EPWM0_EPWM_SYNCIN_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_20	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_21	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_22	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_23	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_97
WKUP_CBASS0	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_101
WKUP_CBASS_SAFE1	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_31
PADCFG_CTRL0	PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_97

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_PADCFG_CTRL0	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_39
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_128
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_97
CPSW0	CPSW0_CPTS_COMP_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0
	CPSW0_CPTS_COMP_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_24
	CPSW0_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_16
	CPSW0_CPTS_GENF1_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_17
	CPSW0_CPTS_SYNC_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0
	CPSW0_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_18
	CPSW0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_67
	CPSW0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_3
	CPSW0_EVNT_PEND_OUT_0	GICSS0_SPI_IN_134
	CPSW0_EVNT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_134
	CPSW0_EVNT_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_134
	CPSW0_EVNT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_102
	CPSW0_MDIO_PEND_OUT_0	GICSS0_SPI_IN_135
	CPSW0_MDIO_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_135
	CPSW0_MDIO_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_135
	CPSW0_MDIO_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_103
	CPSW0_STAT_PEND_OUT_0	GICSS0_SPI_IN_136
	CPSW0_STAT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_136
	CPSW0_STAT_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_136
	CPSW0_STAT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_104
DCC0	DCC0_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC0_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC0_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC0_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_112
DCC1	DCC1_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC1_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC1_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DCC1	DCC1_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC1_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_113
DCC2	DCC2_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC2_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC2_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_114
DCC3	DCC3_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC3_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC3_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_115
DCC4	DCC4_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC4_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC4_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_116
DCC5	DCC5_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC5_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC5_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_117
DCC6	DCC6_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC6_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_96
	DCC6_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_79
MCU_DCC0	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_108
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_108
	MCU_DCC0_INTR_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_37
MCU_DCC1	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_137
	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_137
	MCU_DCC1_INTR_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_36

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_9
	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_10
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	GICSS0_SPI_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_32
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	GICSS0_SPI_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_33
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	GICSS0_SPI_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_34
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	GICSS0_SPI_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_35
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	GICSS0_SPI_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_36
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	GICSS0_SPI_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_37
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	GICSS0_SPI_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_38
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	GICSS0_SPI_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_39
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	GICSS0_SPI_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	C7X256V0_CLEC_GIC_SPI_IN_40
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	GICSS0_SPI_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	C7X256V0_CLEC_GIC_SPI_IN_41
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	GICSS0_SPI_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	C7X256V0_CLEC_GIC_SPI_IN_42
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	GICSS0_SPI_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	C7X256V0_CLEC_GIC_SPI_IN_43
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	GICSS0_SPI_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	C7X256V0_CLEC_GIC_SPI_IN_44
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	GICSS0_SPI_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	C7X256V0_CLEC_GIC_SPI_IN_45
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	GICSS0_SPI_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	C7X256V0_CLEC_GIC_SPI_IN_46
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	GICSS0_SPI_IN_79

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	C7X256V0_CLEC_GIC_SPI_IN_47
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	GICSS0_SPI_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	C7X256V0_CLEC_GIC_SPI_IN_48
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	GICSS0_SPI_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	C7X256V0_CLEC_GIC_SPI_IN_49
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	GICSS0_SPI_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	C7X256V0_CLEC_GIC_SPI_IN_50
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	GICSS0_SPI_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	C7X256V0_CLEC_GIC_SPI_IN_51
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	GICSS0_SPI_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	C7X256V0_CLEC_GIC_SPI_IN_52
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	GICSS0_SPI_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	C7X256V0_CLEC_GIC_SPI_IN_53
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	GICSS0_SPI_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	C7X256V0_CLEC_GIC_SPI_IN_54
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	GICSS0_SPI_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	C7X256V0_CLEC_GIC_SPI_IN_55
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	GICSS0_SPI_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	C7X256V0_CLEC_GIC_SPI_IN_56
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	GICSS0_SPI_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	C7X256V0_CLEC_GIC_SPI_IN_57
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	GICSS0_SPI_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	C7X256V0_CLEC_GIC_SPI_IN_58
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	GICSS0_SPI_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	C7X256V0_CLEC_GIC_SPI_IN_59
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	GICSS0_SPI_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	C7X256V0_CLEC_GIC_SPI_IN_60
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	GICSS0_SPI_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	C7X256V0_CLEC_GIC_SPI_IN_61
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	GICSS0_SPI_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	C7X256V0_CLEC_GIC_SPI_IN_62
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	GICSS0_SPI_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	C7X256V0_CLEC_GIC_SPI_IN_63

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	GICSS0_SPI_IN_96
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	C7X256V0_CLEC_GIC_SPI_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	GICSS0_SPI_IN_97
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	C7X256V0_CLEC_GIC_SPI_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	GICSS0_SPI_IN_98
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	C7X256V0_CLEC_GIC_SPI_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	GICSS0_SPI_IN_99
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	C7X256V0_CLEC_GIC_SPI_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	GICSS0_SPI_IN_100
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	C7X256V0_CLEC_GIC_SPI_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	GICSS0_SPI_IN_101
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	C7X256V0_CLEC_GIC_SPI_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	GICSS0_SPI_IN_102
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	C7X256V0_CLEC_GIC_SPI_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	GICSS0_SPI_IN_103
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	C7X256V0_CLEC_GIC_SPI_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	WKUP_R5FSS0_CORE0_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	WKUP_R5FSS0_CORE0_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	WKUP_R5FSS0_CORE0_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	WKUP_R5FSS0_CORE0_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	WKUP_R5FSS0_CORE0_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	WKUP_R5FSS0_CORE0_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	WKUP_R5FSS0_CORE0_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	WKUP_R5FSS0_CORE0_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	WKUP_R5FSS0_CORE0_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	WKUP_R5FSS0_CORE0_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	WKUP_R5FSS0_CORE0_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	WKUP_R5FSS0_CORE0_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	WKUP_R5FSS0_CORE0_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	WKUP_R5FSS0_CORE0_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	WKUP_R5FSS0_CORE0_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	WKUP_R5FSS0_CORE0_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	WKUP_R5FSS0_CORE0_INTR_IN_80

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	WKUP_R5FSS0_CORE0_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	WKUP_R5FSS0_CORE0_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	WKUP_R5FSS0_CORE0_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	WKUP_R5FSS0_CORE0_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	WKUP_R5FSS0_CORE0_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	WKUP_R5FSS0_CORE0_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	WKUP_R5FSS0_CORE0_INTR_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	WKUP_R5FSS0_CORE0_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	WKUP_R5FSS0_CORE0_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	WKUP_R5FSS0_CORE0_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	WKUP_R5FSS0_CORE0_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	WKUP_R5FSS0_CORE0_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	WKUP_R5FSS0_CORE0_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	WKUP_R5FSS0_CORE0_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	WKUP_R5FSS0_CORE0_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72	WKUP_R5FSS0_CORE0_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73	WKUP_R5FSS0_CORE0_INTR_IN_9
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74	WKUP_R5FSS0_CORE0_INTR_IN_10
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75	WKUP_R5FSS0_CORE0_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76	WKUP_R5FSS0_CORE0_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77	WKUP_R5FSS0_CORE0_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78	WKUP_R5FSS0_CORE0_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79	WKUP_R5FSS0_CORE0_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84	C7X256V0_CLEC_SOC_EVENTS_IN_IN_16
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85	C7X256V0_CLEC_SOC_EVENTS_IN_IN_17
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86	C7X256V0_CLEC_SOC_EVENTS_IN_IN_18
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87	C7X256V0_CLEC_SOC_EVENTS_IN_IN_19
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88	C7X256V0_CLEC_SOC_EVENTS_IN_IN_20
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89	C7X256V0_CLEC_SOC_EVENTS_IN_IN_21
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90	C7X256V0_CLEC_SOC_EVENTS_IN_IN_22
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91	C7X256V0_CLEC_SOC_EVENTS_IN_IN_23
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92	C7X256V0_CLEC_SOC_EVENTS_IN_IN_24
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93	C7X256V0_CLEC_SOC_EVENTS_IN_IN_25

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94	C7X256V0_CLEC_SOC_EVENTS_IN_IN_26
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95	C7X256V0_CLEC_SOC_EVENTS_IN_IN_27
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96	C7X256V0_CLEC_SOC_EVENTS_IN_IN_28
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97	C7X256V0_CLEC_SOC_EVENTS_IN_IN_29
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98	C7X256V0_CLEC_SOC_EVENTS_IN_IN_30
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99	C7X256V0_CLEC_SOC_EVENTS_IN_IN_31
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168	MCU_R5FSS0_CORE0_CPU0_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169	MCU_R5FSS0_CORE0_CPU0_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170	MCU_R5FSS0_CORE0_CPU0_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171	MCU_R5FSS0_CORE0_CPU0_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172	MCU_R5FSS0_CORE0_CPU0_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173	MCU_R5FSS0_CORE0_CPU0_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174	MCU_R5FSS0_CORE0_CPU0_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175	MCU_R5FSS0_CORE0_CPU0_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176	MCU_R5FSS0_CORE0_CPU0_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177	MCU_R5FSS0_CORE0_CPU0_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178	MCU_R5FSS0_CORE0_CPU0_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179	MCU_R5FSS0_CORE0_CPU0_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180	MCU_R5FSS0_CORE0_CPU0_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181	MCU_R5FSS0_CORE0_CPU0_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182	MCU_R5FSS0_CORE0_CPU0_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183	MCU_R5FSS0_CORE0_CPU0_INTR_IN_79
TIMER0	TIMER0_INTR_PEND_OUT_0	GICSS0_SPI_IN_152
	TIMER0_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_120
	TIMER0_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_0
TIMER1	TIMER1_INTR_PEND_OUT_0	GICSS0_SPI_IN_153
	TIMER1_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_121
	TIMER1_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_1
TIMER2	TIMER2_INTR_PEND_OUT_0	GICSS0_SPI_IN_154
	TIMER2_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_122
	TIMER2_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_2
TIMER3	TIMER3_INTR_PEND_OUT_0	GICSS0_SPI_IN_155
	TIMER3_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_123

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMER3	TIMER3_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_3
TIMER4	TIMER4_INTR_PEND_OUT_0	GICSS0_SPI_IN_156
	TIMER4_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_124
TIMER5	TIMER5_INTR_PEND_OUT_0	GICSS0_SPI_IN_157
	TIMER5_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_125
TIMER6	TIMER6_INTR_PEND_OUT_0	GICSS0_SPI_IN_158
	TIMER6_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_126
TIMER7	TIMER7_INTR_PEND_OUT_0	GICSS0_SPI_IN_159
	TIMER7_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_127
MCU_TIMER0	MCU_TIMER0_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_28
MCU_TIMER1	MCU_TIMER1_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_29
MCU_TIMER2	MCU_TIMER2_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_138
MCU_TIMER3	MCU_TIMER3_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_139
WKUP_TIMER0	WKUP_TIMER0_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_138
	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_28
	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_5
WKUP_TIMER1	WKUP_TIMER1_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_139
	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_29
	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_6
ECAP0	ECAP0_ECAP_INT_OUT_0	GICSS0_SPI_IN_145
	ECAP0_ECAP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_120
	ECAP0_ECAP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_83
	ECAP0_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_113
ECAP1	ECAP1_ECAP_INT_OUT_0	GICSS0_SPI_IN_146
	ECAP1_ECAP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_121
	ECAP1_ECAP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_84
	ECAP1_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_114
ECAP2	ECAP2_ECAP_INT_OUT_0	GICSS0_SPI_IN_147
	ECAP2_ECAP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_122
	ECAP2_ECAP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_85
	ECAP2_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_115
ELM0	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	GICSS0_SPI_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_164

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
ELM0	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_132
MMCSD1	MMCSD1_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_115
	MMCSD1_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_162
	MMCSD1_EMMCSDSS_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_162
	MMCSD1_EMMCSDSS_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_83
	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_58
	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_59
	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_60
	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_61
MMCSD2	MMCSD2_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_114
	MMCSD2_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_163
	MMCSD2_EMMCSDSS_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_163
	MMCSD2_EMMCSDSS_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_82
	MMCSD2_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_34
	MMCSD2_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_36
	MMCSD2_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_49
	MMCSD2_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_65
MMCSD0	MMCSD0_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_165
	MMCSD0_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_161
	MMCSD0_EMMCSDSS_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_161
	MMCSD0_EMMCSDSS_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_54
	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_55
	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_56
	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_57
EQEP0	EQEP0_EQEP_INT_OUT_0	GICSS0_SPI_IN_148
	EQEP0_EQEP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_244
	EQEP0_EQEP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_86
	EQEP0_EQEP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_116
EQEP1	EQEP1_EQEP_INT_OUT_0	GICSS0_SPI_IN_149
	EQEP1_EQEP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_245
	EQEP1_EQEP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_87

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EQEP1	EQEP1_EQEP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_117
EQEP2	EQEP2_EQEP_INT_OUT_0	GICSS0_SPI_IN_150
	EQEP2_EQEP_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_246
	EQEP2_EQEP_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_88
	EQEP2_EQEP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_118
ESM0	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_0
	ESM0_ESM_INT_CFG_LVL_OUT_0	GICSS0_SPI_IN_180
	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_148
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_1
	ESM0_ESM_INT_HI_LVL_OUT_0	GICSS0_SPI_IN_181
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_149
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_2
	ESM0_ESM_INT_LOW_LVL_OUT_0	GICSS0_SPI_IN_182
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_150
WKUP_ESM0	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_37
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_140
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_140
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_38
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_141
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_141
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_39
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_142
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_142
FSS0_FSAS_0	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_141
FSS0_OSPI_0	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_11
	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_74
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	GICSS0_SPI_IN_171

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
FSS0_OSPI_0	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_171
GICSS0	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT0_IN_198
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT1_IN_198
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT2_IN_198
	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_12
	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_75
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT0_IN_199
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT1_IN_199
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT2_IN_199
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_154
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_155
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_156
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_157
GPIO0	GPIO0_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0
	GPIO0_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_1
	GPIO0_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_2
	GPIO0_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_3
	GPIO0_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_4
	GPIO0_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_5
	GPIO0_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_6
	GPIO0_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_7
	GPIO0_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_8
	GPIO0_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_9
	GPIO0_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_10
	GPIO0_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_11
	GPIO0_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_12
	GPIO0_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_13
	GPIO0_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_14
	GPIO0_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_15
	GPIO0_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_16
	GPIO0_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_17
	GPIO0_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_18

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_19
	GPIO0_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_20
	GPIO0_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_21
	GPIO0_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_22
	GPIO0_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_23
	GPIO0_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_24
	GPIO0_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_25
	GPIO0_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_26
	GPIO0_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_27
	GPIO0_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_28
	GPIO0_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_29
	GPIO0_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_30
	GPIO0_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_31
	GPIO0_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_32
	GPIO0_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_33
	GPIO0_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_34
	GPIO0_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_35
	GPIO0_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_36
	GPIO0_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_37
	GPIO0_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_38
	GPIO0_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_39
	GPIO0_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_40
	GPIO0_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_41
	GPIO0_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_42
	GPIO0_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_43
	GPIO0_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_44
	GPIO0_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_45
	GPIO0_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_46
	GPIO0_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_47
	GPIO0_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_48
	GPIO0_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_49
	GPIO0_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_50
	GPIO0_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_51

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_52
	GPIO0_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_53
	GPIO0_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_54
	GPIO0_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_55
	GPIO0_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_56
	GPIO0_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_57
	GPIO0_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_58
	GPIO0_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_59
	GPIO0_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_60
	GPIO0_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_61
	GPIO0_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_62
	GPIO0_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_63
	GPIO0_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_64
	GPIO0_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_65
	GPIO0_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_66
	GPIO0_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_67
	GPIO0_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_68
	GPIO0_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_69
	GPIO0_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_70
	GPIO0_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_71
	GPIO0_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_72
	GPIO0_GPIO_OUT_73	MAIN_GPIOMUX_INTROUTER0_IN_IN_73
	GPIO0_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_74
	GPIO0_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_75
	GPIO0_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_76
	GPIO0_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_77
	GPIO0_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_78
	GPIO0_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_79
	GPIO0_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_80
	GPIO0_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_81
	GPIO0_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_82
	GPIO0_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_83
	GPIO0_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_84

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_85
	GPIO0_GPIO_OUT_86	MAIN_GPIOMUX_INTROUTER0_IN_IN_86
	GPIO0_GPIO_OUT_87	MAIN_GPIOMUX_INTROUTER0_IN_IN_87
	GPIO0_GPIO_OUT_88	MAIN_GPIOMUX_INTROUTER0_IN_IN_88
	GPIO0_GPIO_OUT_89	MAIN_GPIOMUX_INTROUTER0_IN_IN_89
	GPIO0_GPIO_OUT_90	MAIN_GPIOMUX_INTROUTER0_IN_IN_176
	GPIO0_GPIO_OUT_91	MAIN_GPIOMUX_INTROUTER0_IN_IN_177
	GPIO0_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_190
	GPIO0_GPIO_BANK_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_56
	GPIO0_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_191
	GPIO0_GPIO_BANK_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_57
	GPIO0_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_192
	GPIO0_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_193
	GPIO0_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_194
	GPIO0_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_195
GPIO1	GPIO1_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_90
	GPIO1_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_91
	GPIO1_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_92
	GPIO1_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_93
	GPIO1_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_94
	GPIO1_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_95
	GPIO1_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_96
	GPIO1_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_97
	GPIO1_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_98
	GPIO1_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_99
	GPIO1_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_100
	GPIO1_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_101
	GPIO1_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_102
	GPIO1_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_103
	GPIO1_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_104
	GPIO1_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_105
	GPIO1_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_106
	GPIO1_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_107

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_108
	GPIO1_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_109
	GPIO1_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_110
	GPIO1_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_111
	GPIO1_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_112
	GPIO1_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_113
	GPIO1_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_114
	GPIO1_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_115
	GPIO1_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_116
	GPIO1_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_117
	GPIO1_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_118
	GPIO1_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_119
	GPIO1_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_120
	GPIO1_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_121
	GPIO1_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_122
	GPIO1_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_123
	GPIO1_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_124
	GPIO1_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_125
	GPIO1_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_126
	GPIO1_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_127
	GPIO1_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_128
	GPIO1_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_129
	GPIO1_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_130
	GPIO1_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_131
	GPIO1_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_132
	GPIO1_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_133
	GPIO1_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_134
	GPIO1_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_135
	GPIO1_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_136
	GPIO1_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_137
	GPIO1_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_138
	GPIO1_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_139
	GPIO1_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_140

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_141
	GPIO1_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_142
	GPIO1_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_143
	GPIO1_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_144
	GPIO1_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_145
	GPIO1_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_146
	GPIO1_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_147
	GPIO1_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_148
	GPIO1_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_149
	GPIO1_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_150
	GPIO1_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_151
	GPIO1_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_152
	GPIO1_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_153
	GPIO1_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_154
	GPIO1_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_155
	GPIO1_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_156
	GPIO1_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_157
	GPIO1_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_158
	GPIO1_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_159
	GPIO1_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_160
	GPIO1_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_161
	GPIO1_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_180
	GPIO1_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_181
	GPIO1_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_182
	GPIO1_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_183
	GPIO1_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_184
MCU_GPIO0	MCU_GPIO0_GPIO_OUT_0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_0
	MCU_GPIO0_GPIO_OUT_1	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_1
	MCU_GPIO0_GPIO_OUT_2	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_2
	MCU_GPIO0_GPIO_OUT_3	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_3
	MCU_GPIO0_GPIO_OUT_4	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_4
	MCU_GPIO0_GPIO_OUT_5	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_5
	MCU_GPIO0_GPIO_OUT_6	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_6

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_GPIO0	MCU_GPIO0_GPIO_OUT_7	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_7
	MCU_GPIO0_GPIO_OUT_8	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_8
	MCU_GPIO0_GPIO_OUT_9	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_9
	MCU_GPIO0_GPIO_OUT_10	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_10
	MCU_GPIO0_GPIO_OUT_11	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_11
	MCU_GPIO0_GPIO_OUT_12	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_12
	MCU_GPIO0_GPIO_OUT_13	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_13
	MCU_GPIO0_GPIO_OUT_14	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_14
	MCU_GPIO0_GPIO_OUT_15	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_15
	MCU_GPIO0_GPIO_OUT_16	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_16
	MCU_GPIO0_GPIO_OUT_17	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_17
	MCU_GPIO0_GPIO_OUT_18	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_18
	MCU_GPIO0_GPIO_OUT_19	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_19
	MCU_GPIO0_GPIO_OUT_20	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_20
	MCU_GPIO0_GPIO_OUT_21	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_21
	MCU_GPIO0_GPIO_OUT_22	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_22
	MCU_GPIO0_GPIO_OUT_23	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_23
	MCU_GPIO0_GPIO_BANK_OUT_0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_30
	MCU_GPIO0_GPIO_BANK_OUT_1	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_31
	MCU_GPIO0_GPIO_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_18
	MCU_GPIO0_GPIO_LVL_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_2
GPMC0	GPMC0_GPMC_SDMAREQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_26
	GPMC0_GPMC_SINTERRUPT_OUT_0	GICSS0_SPI_IN_138
	GPMC0_GPMC_SINTERRUPT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_103
	GPMC0_GPMC_SINTERRUPT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_103
	GPMC0_GPMC_SINTERRUPT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_106
WKUP_GTC0	WKUP_GTC0_GTC_PUSH_EVENT_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_11
WKUP_icemelter0	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_23
	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_3
DDPA0	DDPA0_DDPA_INTR_OUT_0	GICSS0_SPI_IN_177
	DDPA0_DDPA_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_177
	DDPA0_DDPA_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_177
	DDPA0_DDPA_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_145

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EPWM0	EPWM0_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_229
	EPWM0_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_123
	EPWM0_EPWM_ETINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_36
	EPWM0_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_197
	EPWM0_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_8
	EPWM0_EPWM_SYNCOUT_OUT_0	EPWM1_EPWM_SYNCIN_IN_0
	EPWM0_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_230
	EPWM0_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_124
	EPWM0_EPWM_TRIPZINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_80
	EPWM0_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_198
EPWM1	EPWM1_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_231
	EPWM1_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_125
	EPWM1_EPWM_ETINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_37
	EPWM1_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_199
	EPWM1_EPWM_SYNCOUT_OUT_0	EPWM2_EPWM_SYNCIN_IN_0
	EPWM1_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_233
	EPWM1_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_126
	EPWM1_EPWM_TRIPZINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_81
	EPWM1_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_201
EPWM2	EPWM2_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_234
	EPWM2_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_127
	EPWM2_EPWM_ETINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_38
	EPWM2_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_202
	EPWM2_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_235
	EPWM2_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_148
	EPWM2_EPWM_TRIPZINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_82
	EPWM2_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_203
PBIST0	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_196
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_196
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_196
	PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_114
	PBIST0_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_114
	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_157

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_PBIST0	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_202
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_202
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_202
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_115
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_115
	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_158
WKUP_PBIST1	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_201
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_201
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_201
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_118
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_118
	WKUP_PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_159
MCU_PBIST0	MCU_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_203
	MCU_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_203
	MCU_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_203
	MCU_PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_110
	MCU_PBIST0_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_110
	MCU_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_152
WKUP_VTM0	WKUP_VTM0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_139
	WKUP_VTM0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_11
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_137
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_8
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	GICSS0_SPI_IN_183
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_183
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_183
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_151
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_138
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_10
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	GICSS0_SPI_IN_184
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_184
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_184
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_152
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_136

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_VTM0	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_9
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	GICSS0_SPI_IN_185
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_185
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_185
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_153
	WKUP_VTM0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_140
	WKUP_VTM0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_12
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_0	GICSS0_SPI_IN_108
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_76
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_1	C7X256V0_CLEC_SOC_EVENTS_IN_IN_0
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER0_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_0	GICSS0_SPI_IN_109
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_77
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_1	C7X256V0_CLEC_SOC_EVENTS_IN_IN_1
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER1_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_0	GICSS0_SPI_IN_140
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_108
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_1	C7X256V0_CLEC_SOC_EVENTS_IN_IN_2
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER2_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_0	GICSS0_SPI_IN_141
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_109
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_1	C7X256V0_CLEC_SOC_EVENTS_IN_IN_3
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_243
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER3_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_243
MCAN0	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_16
	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_78
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	GICSS0_SPI_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_154

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCAN0	MCAN0_MCANSS_FE_OUT_0	PDMA0_MCANSS_MAIN_0_FE_IN_0
	MCAN0_MCANSS_FE_OUT_1	PDMA0_MCANSS_MAIN_0_FE_IN_1
	MCAN0_MCANSS_FE_OUT_2	PDMA0_MCANSS_MAIN_0_FE_IN_2
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	GICSS0_SPI_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_155
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	GICSS0_SPI_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	MCU_R5FSS0_CORE0_CPU0_INTR_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_156
	MCAN0_MCANSS_TX_DMA_OUT_0	PDMA0_MCANSS_MAIN_0_TX_IN_0
	MCAN0_MCANSS_TX_DMA_OUT_1	PDMA0_MCANSS_MAIN_0_TX_IN_1
	MCAN0_MCANSS_TX_DMA_OUT_2	PDMA0_MCANSS_MAIN_0_TX_IN_2
MCU_MCAN0	MCU_MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_16
	MCU_MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_17
	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_198
	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_42
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_199
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_43
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_200
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	MCU_R5FSS0_CORE0_CPU0_INTR_IN_44
MCU_MCAN1	MCU_MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_18
	MCU_MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_19
	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_239
	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_45
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_247
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_46
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_248
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	MCU_R5FSS0_CORE0_CPU0_INTR_IN_47
MCASP0	MCASP0_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_RX_IN_0
	MCASP0_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_267
	MCASP0_REC_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_98

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCASP0	MCASP0_REC_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_120
	MCASP0_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_235
	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_TX_IN_0
	MCASP0_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_268
	MCASP0_XMIT_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_99
	MCASP0_XMIT_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_121
	MCASP0_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_236
MCASP1	MCASP1_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_RX_IN_0
	MCASP1_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_269
	MCASP1_REC_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_165
	MCASP1_REC_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_122
	MCASP1_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_237
	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_TX_IN_0
	MCASP1_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_270
	MCASP1_XMIT_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_166
	MCASP1_XMIT_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_123
	MCASP1_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_238
MCASP2	MCASP2_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_RX_IN_0
	MCASP2_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_271
	MCASP2_REC_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_170
	MCASP2_REC_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_124
	MCASP2_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_239
	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_TX_IN_0
	MCASP2_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_272
	MCASP2_XMIT_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_209
	MCASP2_XMIT_INTR_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_125
	MCASP2_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_240
MCRC64_0	MCRC64_0_DMA_EVENT_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28
	MCRC64_0_DMA_EVENT_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29
	MCRC64_0_DMA_EVENT_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30
	MCRC64_0_DMA_EVENT_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31
	MCRC64_0_INT_MCRC_OUT_0	GICSS0_SPI_IN_166
	MCRC64_0_INT_MCRC_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_119

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCRC64_0	MCRC64_0_INT_MCRC_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_119
	MCRC64_0_INT_MCRC_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_134
MCU_MCRC64_0	MCU_MCRC64_0_INT_MCRC_OUT_0	GICSS0_SPI_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_160
I2C0	I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_193
	I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_161
I2C1	I2C1_POINTRPEND_OUT_0	GICSS0_SPI_IN_194
	I2C1_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_162
I2C2	I2C2_POINTRPEND_OUT_0	GICSS0_SPI_IN_195
	I2C2_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_163
I2C3	I2C3_POINTRPEND_OUT_0	GICSS0_SPI_IN_196
	I2C3_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_164
MCU_I2C0	MCU_I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_139
	MCU_I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_197
	MCU_I2C0_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_197
	MCU_I2C0_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_107
WKUP_I2C0	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_143
	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_0
	WKUP_I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_197
	WKUP_I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_190
	WKUP_I2C0_POINTRPEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_190
MSRAM_64K0	MSRAM_64K0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_5
	MSRAM_64K0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_6

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_MSRAM_256K0	MCU_MSRAM_256K0_ECC_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_32
	MCU_MSRAM_256K0_ECC_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_33
MCU_MSRAM_256K1	MCU_MSRAM_256K1_ECC_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_34
	MCU_MSRAM_256K1_ECC_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_35
pllfracf2_ssmod_16fft0	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_128
	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_54
pllfracf2_ssmod_16fft1	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_129
	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_55
pllfracf2_ssmod_16fft12	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_132
	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_58
pllfracf2_ssmod_16fft15	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_133
	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_59
pllfracf2_ssmod_16fft2	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_130
	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_56
pllfracf2_ssmod_16fft5	PLLFRACF2_SSMOD_16FFT5_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_17
	PLLFRACF2_SSMOD_16FFT5_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_60
pllfracf2_ssmod_16fft7	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_18
	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_61
pllfracf2_ssmod_16fft8	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_131
	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_57
MCU_pllfracf2_ssmod_16fft0	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_134
	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_63
PSRAMECC0	PSRAMECC0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_29
	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_90
PSRAMECC1	PSRAMECC1_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_108
	PSRAMECC1_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_109
WKUP_PSRAMECC_8K0	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_8
	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_42
	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_13
	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_43
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_CTI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_175
	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_30
	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_91

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_124
	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_4
	WKUP_R5FSS0_CORE0_PMU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_58
	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_59
	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_60
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_5
	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_6
	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_40
	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_42
MCU_R5FSS0_CORE0	MCU_R5FSS0_CORE0_COMMRX_LEVEL_0_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_90
	MCU_R5FSS0_CORE0_COMMTX_LEVEL_0_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_91
	MCU_R5FSS0_CORE0_CPU0_CTI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_175
	MCU_R5FSS0_CORE0_CPU0_EXP_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_30
	MCU_R5FSS0_CORE0_CPU0_EXP_INTR_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_4
	MCU_R5FSS0_CORE0_CPU0_PMU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_94
	MCU_R5FSS0_CORE0_CPU0_VALFIQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_95
	MCU_R5FSS0_CORE0_CPU0_VALIRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_96
MCU_R5FSS0_COMMON0	MCU_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_28
	MCU_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_29
MCU_R5FSS0_CPU0_ECC_AGGR_0	MCU_R5FSS0_CPU0_ECC_AGGR_0_CPU0_ECC_CORRECTED_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_4
	MCU_R5FSS0_CPU0_ECC_AGGR_0_CPU0_ECC_UNCORRECTED_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_5
WKUP_rtcss0	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	GICSS0_SPI_IN_132
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_97
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_97
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_7
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_100
RTI4	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_204
	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_204
	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_204
	RTI4_INTR_WWD_OUT_0	C7X256V0_CLEC_SOC_EVENTS_IN_IN_4
RTI0	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_192
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_192
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_192

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
RTI0	RTI0_INTR_WWD_OUT_0	GICSS0_SPI_IN_252
	RTI0_INTR_WWD_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_220
RTI1	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_193
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_193
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_193
	RTI1_INTR_WWD_OUT_0	GICSS0_SPI_IN_253
	RTI1_INTR_WWD_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_221
RTI2	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_209
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_209
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_209
	RTI2_INTR_WWD_OUT_0	GICSS0_SPI_IN_254
	RTI2_INTR_WWD_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_222
RTI3	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_210
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_210
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_210
	RTI3_INTR_WWD_OUT_0	GICSS0_SPI_IN_255
	RTI3_INTR_WWD_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_223
MCU_RTI0	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_30
WKUP_RTI0	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_195
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_195
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_195
	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_30
SA3_SS0_DMSS_ECCAGGR_0	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_118
	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_119
SA3_SS0_INTAGGR_0	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4	GICSS0_SPI_IN_112
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_80
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5	GICSS0_SPI_IN_113
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_81
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	MCU_R5FSS0_CORE0_CPU0_INTR_IN_7

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
SA3_SS0_SA_UL_0	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_120
	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_121
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	GICSS0_SPI_IN_160
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	GICSS0_SPI_IN_161
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
WKUP_DEEPSLEEP_SOURCES0	WKUP_DEEPSLEEP_SOURCES0_WAKEUP_EVENT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_27
PDMA0	PDMA0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_88
	PDMA0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_15
PDMA1	PDMA1_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_89
	PDMA1_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_28
COMPUTE_CLUSTER0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTO_OUT_0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTI_IN_0
	COMPUTE_CLUSTER0_CPU_EVNT_EVENTO_OUT_0	C7X256V0_CLEC_ARM_0_EVENTO_IN_IN_0
A53SS0	A53SS0_CNTHPIRQ0_OUT_0	GICSS0_PPI0_0_IN_26
	A53SS0_CNTHPIRQ1_OUT_0	GICSS0_PPI0_1_IN_26
	A53SS0_CNTHPIRQ2_OUT_0	GICSS0_PPI0_2_IN_26
	A53SS0_CNTHPIRQ3_OUT_0	GICSS0_PPI0_3_IN_26
	A53SS0_CNTPNSIRQ0_OUT_0	GICSS0_PPI0_0_IN_30
	A53SS0_CNTPNSIRQ1_OUT_0	GICSS0_PPI0_1_IN_30
	A53SS0_CNTPNSIRQ2_OUT_0	GICSS0_PPI0_2_IN_30
	A53SS0_CNTPNSIRQ3_OUT_0	GICSS0_PPI0_3_IN_30
	A53SS0_CNTPSIRQ0_OUT_0	GICSS0_PPI0_0_IN_29
	A53SS0_CNTPSIRQ1_OUT_0	GICSS0_PPI0_1_IN_29
	A53SS0_CNTPSIRQ2_OUT_0	GICSS0_PPI0_2_IN_29
	A53SS0_CNTPSIRQ3_OUT_0	GICSS0_PPI0_3_IN_29
	A53SS0_CNTVIRQ0_OUT_0	GICSS0_PPI0_0_IN_27
	A53SS0_CNTVIRQ1_OUT_0	GICSS0_PPI0_1_IN_27
	A53SS0_CNTVIRQ2_OUT_0	GICSS0_PPI0_2_IN_27
	A53SS0_CNTVIRQ3_OUT_0	GICSS0_PPI0_3_IN_27

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
A53SS0	A53SS0_COMMIRQ0_OUT_0	GICSS0_PPI0_0_IN_22
	A53SS0_COMMIRQ1_OUT_0	GICSS0_PPI0_1_IN_22
	A53SS0_COMMIRQ2_OUT_0	GICSS0_PPI0_2_IN_22
	A53SS0_COMMIRQ3_OUT_0	GICSS0_PPI0_3_IN_22
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_0_IN_24
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_1_IN_17
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_2_IN_17
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_3_IN_17
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_0_IN_18
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_1_IN_24
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_2_IN_18
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_3_IN_18
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_0_IN_19
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_1_IN_19
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_2_IN_24
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_3_IN_19
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_0_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_1_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_2_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_3_IN_24
	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_24
	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_94
	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_25
	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_93
	A53SS0_ECC_ECCAGGR2_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_45
	A53SS0_ECC_ECCAGGR2_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_46
	A53SS0_ECC_ECCAGGR3_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_47
	A53SS0_ECC_ECCAGGR3_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_48
	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_26
	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_95
	A53SS0_EXTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_144
	A53SS0_INTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_145
	A53SS0_PMUIRQ0_OUT_0	GICSS0_PPI0_0_IN_23

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
A53SS0	A53SS0_PMUIRQ1_OUT_0	GICSS0_PPI0_1_IN_23
	A53SS0_PMUIRQ2_OUT_0	GICSS0_PPI0_2_IN_23
	A53SS0_PMUIRQ3_OUT_0	GICSS0_PPI0_3_IN_23
	A53SS0_VCPUMNTIRQ0_OUT_0	GICSS0_PPI0_0_IN_25
	A53SS0_VCPUMNTIRQ1_OUT_0	GICSS0_PPI0_1_IN_25
	A53SS0_VCPUMNTIRQ2_OUT_0	GICSS0_PPI0_2_IN_25
	A53SS0_VCPUMNTIRQ3_OUT_0	GICSS0_PPI0_3_IN_25
COMPUTE_CLUSTER0_PBIST_0	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_208
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_208
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_208
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_113
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_44
C7X256V0_CLEC	C7X256V0_CLEC_ARM_0_EVENTI_OUT_OUT_0	COMPUTE_CLUSTER0_CPU_EVNT_EVENTI_IN_0
	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_194
	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_194
	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_194
	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_116
	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_116
	C7X256V0_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_149
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_160
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1	ESM0_ESM_LVL_EVENT_IN_161
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2	ESM0_ESM_LVL_EVENT_IN_162
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3	ESM0_ESM_LVL_EVENT_IN_163
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4	ESM0_ESM_LVL_EVENT_IN_164
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5	ESM0_ESM_LVL_EVENT_IN_165
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6	ESM0_ESM_LVL_EVENT_IN_166
	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7	ESM0_ESM_LVL_EVENT_IN_167
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0	GICSS0_SPI_IN_280
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1	GICSS0_SPI_IN_281
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2	GICSS0_SPI_IN_282
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3	GICSS0_SPI_IN_283
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4	GICSS0_SPI_IN_284

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
C7X256V0_CLEC	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5	GICSS0_SPI_IN_285
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6	GICSS0_SPI_IN_286
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7	GICSS0_SPI_IN_287
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8	MCU_R5FSS0_CORE0_CPU0_INTR_IN_249
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9	MCU_R5FSS0_CORE0_CPU0_INTR_IN_250
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10	MCU_R5FSS0_CORE0_CPU0_INTR_IN_254
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11	MCU_R5FSS0_CORE0_CPU0_INTR_IN_255
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12	WKUP_R5FSS0_CORE0_INTR_IN_249
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13	WKUP_R5FSS0_CORE0_INTR_IN_250
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14	WKUP_R5FSS0_CORE0_INTR_IN_254
	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15	WKUP_R5FSS0_CORE0_INTR_IN_255
DDR32SS0	DDR32SS0_DDRSS_CONTROLLER_OUT_0	GICSS0_SPI_IN_151
	DDR32SS0_DDRSS_CONTROLLER_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_151
	DDR32SS0_DDRSS_CONTROLLER_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_151
	DDR32SS0_DDRSS_CONTROLLER_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_119
	DDR32SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_174
	DDR32SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_175
	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	GICSS0_SPI_IN_172
	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_181
	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_181
	DDR32SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_140
	DDR32SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_176
DEBUGSS0	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	GICSS0_SPI_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_169
	DEBUGSS0_CTM_LEVEL_OUT_0	GICSS0_SPI_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_170
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	USB1_TRACE_INEP_PKT_BUFF_AVAIL_IN_0

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DFTSS0	DFTSS0_DFT_SAFETY_123_OUT_0	ESM0_ESM_LVL_EVENT_IN_98
	DFTSS0_DFT_SAFETY_MULTI_OUT_0	ESM0_ESM_LVL_EVENT_IN_99
	DFTSS0_DFT_SAFETY_ONE_OUT_0	ESM0_ESM_LVL_EVENT_IN_100
WKUP_TIMEOUT1	WKUP_TIMEOUT1_TIMED_OUT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_26
	WKUP_TIMEOUT1_TIMED_OUT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_152
	WKUP_TIMEOUT1_TIMED_OUT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_152
WKUP_TIMEOUT0	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_26
	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_152
	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_152
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_20
	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_23
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_21
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_24
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_104
	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_38
	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_105
	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_39
PSC0_ECC_AGGR_0	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_22
	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_23
PSC0	PSC0_PSC_ALLINT_OUT_0	GICSS0_SPI_IN_203
	PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_146
	PSC0_PSC_ALLINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_146
	PSC0_PSC_ALLINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_171
MCU_TIMEOUT0	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_27
	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_153
	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_153
MCU_MCU_16FF0	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_101
	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_102
MCU_ECC_AGGR0	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_14
	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_15
WKUP_PSC0	WKUP_PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_145
	WKUP_PSC0_PSC_ALLINT_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_145
MCU_ECC_AGGR1	MCU_ECC_AGGR1_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_40

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_ECC_AGGR1	MCU_ECC_AGGR1_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_41
MCU_PRG_MCU_5POKS0	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_77
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_77
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_77
MCU_PRG_MCU0	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_78

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_PRG_MCU0	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_82
ECC_AGGR0	ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_2
	ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_1
ECC_AGGR1	ECC_AGGR1_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_106
	ECC_AGGR1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_107
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_20
	WKUP_ECC_AGGR2_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_21
MCSPI0	MCSPI0_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_0_RX_IN_0
	MCSPI0_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_0_RX_IN_1
	MCSPI0_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_0_RX_IN_2
	MCSPI0_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_0_RX_IN_3
	MCSPI0_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_0_TX_IN_0
	MCSPI0_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_0_TX_IN_1
	MCSPI0_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_0_TX_IN_2
	MCSPI0_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_0_TX_IN_3
	MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_204
	MCSPI0_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_172
MCSPI1	MCSPI1_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_1_RX_IN_0
	MCSPI1_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_1_RX_IN_1

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCSPI1	MCSPI1_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_1_RX_IN_2
	MCSPI1_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_1_RX_IN_3
	MCSPI1_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_1_TX_IN_0
	MCSPI1_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_1_TX_IN_1
	MCSPI1_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_1_TX_IN_2
	MCSPI1_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_1_TX_IN_3
	MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_205
	MCSPI1_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_173
MCSPI2	MCSPI2_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_2_RX_IN_0
	MCSPI2_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_2_RX_IN_1
	MCSPI2_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_2_RX_IN_2
	MCSPI2_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_2_RX_IN_3
	MCSPI2_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_2_TX_IN_0
	MCSPI2_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_2_TX_IN_1
	MCSPI2_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_2_TX_IN_2
	MCSPI2_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_2_TX_IN_3
	MCSPI2_INTR_SPI_OUT_0	GICSS0_SPI_IN_206
	MCSPI2_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_174
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_207
	MCU_MCSPI0_INTR_SPI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_207
	MCU_MCSPI0_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_176
MCU_MCSPI1	MCU_MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_208
	MCU_MCSPI1_INTR_SPI_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_208
	MCU_MCSPI1_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_177
UART0	UART0_USART_DMA_OUT_0	PDMA1_USART_MAIN_0_TX_IN_0
	UART0_USART_DMA_OUT_1	PDMA1_USART_MAIN_0_RX_IN_0
	UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_210

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
UART0	UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_210
	UART0_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_210
	UART0_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_178
UART1	UART1_USART_DMA_OUT_0	PDMA1_USART_MAIN_1_TX_IN_0
	UART1_USART_DMA_OUT_1	PDMA1_USART_MAIN_1_RX_IN_0
	UART1_USART_IRQ_OUT_0	GICSS0_SPI_IN_211
	UART1_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_179
UART2	UART2_USART_DMA_OUT_0	PDMA1_USART_MAIN_2_TX_IN_0
	UART2_USART_DMA_OUT_1	PDMA1_USART_MAIN_2_RX_IN_0
	UART2_USART_IRQ_OUT_0	GICSS0_SPI_IN_212
	UART2_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_180
UART3	UART3_USART_DMA_OUT_0	PDMA1_USART_MAIN_3_TX_IN_0
	UART3_USART_DMA_OUT_1	PDMA1_USART_MAIN_3_RX_IN_0
	UART3_USART_IRQ_OUT_0	GICSS0_SPI_IN_213
	UART3_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_181
UART4	UART4_USART_DMA_OUT_0	PDMA1_USART_MAIN_4_TX_IN_0
	UART4_USART_DMA_OUT_1	PDMA1_USART_MAIN_4_RX_IN_0
	UART4_USART_IRQ_OUT_0	GICSS0_SPI_IN_214
	UART4_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_182
UART5	UART5_USART_DMA_OUT_0	PDMA1_USART_MAIN_5_TX_IN_0
	UART5_USART_DMA_OUT_1	PDMA1_USART_MAIN_5_RX_IN_0
	UART5_USART_IRQ_OUT_0	GICSS0_SPI_IN_215
	UART5_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_183

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
UART6	UART6_USART_DMA_OUT_0	PDMA1_USART_MAIN_6_TX_IN_0
	UART6_USART_DMA_OUT_1	PDMA1_USART_MAIN_6_RX_IN_0
	UART6_USART_IRQ_OUT_0	GICSS0_SPI_IN_216
	UART6_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_216
	UART6_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_216
	UART6_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_184
MCU_UART0	MCU_UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_217
	MCU_UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_217
	MCU_UART0_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_217
	MCU_UART0_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_185
WKUP_UART0	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_144
	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_1
	WKUP_UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_218
	WKUP_UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_186
USB0	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_35
	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_111
	USB0_HOST_SYSTEM_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_32
	USB0_IRQ_OUT_0	GICSS0_SPI_IN_220
	USB0_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_220
	USB0_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_220
	USB0_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_188
	USB0_IRQ_OUT_1	GICSS0_SPI_IN_221
	USB0_IRQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_221
	USB0_IRQ_OUT_1	MCU_R5FSS0_CORE0_CPU0_INTR_IN_221
	USB0_IRQ_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_189
	USB0_IRQ_OUT_2	GICSS0_SPI_IN_222
	USB0_IRQ_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_222
	USB0_IRQ_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_222
	USB0_IRQ_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_190
	USB0_IRQ_OUT_3	GICSS0_SPI_IN_223
	USB0_IRQ_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_223

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB0	USB0_IRQ_OUT_3	MCU_R5FSS0_CORE0_CPU0_INTR_IN_223
	USB0_IRQ_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_191
	USB0_IRQ_OUT_4	GICSS0_SPI_IN_224
	USB0_IRQ_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_224
	USB0_IRQ_OUT_4	MCU_R5FSS0_CORE0_CPU0_INTR_IN_224
	USB0_IRQ_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_192
	USB0_IRQ_OUT_5	GICSS0_SPI_IN_225
	USB0_IRQ_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_225
	USB0_IRQ_OUT_5	MCU_R5FSS0_CORE0_CPU0_INTR_IN_225
	USB0_IRQ_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_193
	USB0_IRQ_OUT_6	GICSS0_SPI_IN_226
	USB0_IRQ_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_226
	USB0_IRQ_OUT_6	MCU_R5FSS0_CORE0_CPU0_INTR_IN_226
	USB0_IRQ_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_194
	USB0_IRQ_OUT_7	GICSS0_SPI_IN_227
	USB0_IRQ_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_227
	USB0_IRQ_OUT_7	MCU_R5FSS0_CORE0_CPU0_INTR_IN_227
	USB0_IRQ_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_195
	USB0_MISC_LEVEL_OUT_0	GICSS0_SPI_IN_228
	USB0_MISC_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_228
	USB0_MISC_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_228
	USB0_MISC_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_196
	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_61
	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_9
USB1	USB1_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_146
	USB1_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_147
	USB1_HOST_SYSTEM_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_33
	USB1_IRQ_OUT_0	GICSS0_SPI_IN_258
	USB1_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_230
	USB1_IRQ_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_230
	USB1_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_226
	USB1_IRQ_OUT_1	GICSS0_SPI_IN_259
	USB1_IRQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_231

Table 10-7. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB1	USB1_IRQ_OUT_1	MCU_R5FSS0_CORE0_CPU0_INTR_IN_231
	USB1_IRQ_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_227
	USB1_IRQ_OUT_2	GICSS0_SPI_IN_260
	USB1_IRQ_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_232
	USB1_IRQ_OUT_2	MCU_R5FSS0_CORE0_CPU0_INTR_IN_232
	USB1_IRQ_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_228
	USB1_IRQ_OUT_3	GICSS0_SPI_IN_261
	USB1_IRQ_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_233
	USB1_IRQ_OUT_3	MCU_R5FSS0_CORE0_CPU0_INTR_IN_233
	USB1_IRQ_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_229
	USB1_IRQ_OUT_4	GICSS0_SPI_IN_262
	USB1_IRQ_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_234
	USB1_IRQ_OUT_4	MCU_R5FSS0_CORE0_CPU0_INTR_IN_234
	USB1_IRQ_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_230
	USB1_IRQ_OUT_5	GICSS0_SPI_IN_263
	USB1_IRQ_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_235
	USB1_IRQ_OUT_5	MCU_R5FSS0_CORE0_CPU0_INTR_IN_235
	USB1_IRQ_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_231
	USB1_IRQ_OUT_6	GICSS0_SPI_IN_264
	USB1_IRQ_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_236
	USB1_IRQ_OUT_6	MCU_R5FSS0_CORE0_CPU0_INTR_IN_236
	USB1_IRQ_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_232
	USB1_IRQ_OUT_7	GICSS0_SPI_IN_265
	USB1_IRQ_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_237
	USB1_IRQ_OUT_7	MCU_R5FSS0_CORE0_CPU0_INTR_IN_237
	USB1_IRQ_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_233
	USB1_MISC_LEVEL_OUT_0	GICSS0_SPI_IN_266
	USB1_MISC_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_238
	USB1_MISC_LEVEL_OUT_0	MCU_R5FSS0_CORE0_CPU0_INTR_IN_238
	USB1_MISC_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_234
	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_62
	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_10

Chapter 11
Data Movement Architecture

This chapter describes the data movement architecture of the device.

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11.2 Data Movement Subsystem (DMSS)........ 908
11.3 Peripheral DMA (PDMA)........ 940

11.1 Data Movement Architecture Overview

This chapter is a high-level summary of the data movement architecture implemented in the device.

11.1.1 Overview

The primary goal of the device Data Movement Architecture and related Subsystems is to ensure that data can be efficiently transferred from a producer to a consumer while meeting the real time requirements of the system can be met.

The Data Movement Subsystem (DMSS) aims to facilitate direct memory access (DMA) and provides a consistent Application Programming Interface (API) to the host software.

Data movement tasks are commonly offloaded from the host processor to peripheral hardware to increase system performance. Significant performance gains may result from careful design of the interface between the host software and the underlying acceleration hardware. In networking applications, packet transmission and reception are critical tasks. In general purpose compute, ping pong buffer prefetch and store are critical tasks as well as general mis-aligned block copy operations.

The design goals for the device Data Movement Architecture and are as follows:

- Minimize cost
- Minimize host overhead
- Maximize memory use efficiency
- Maximize bus burst efficiency
- Maximize symmetry between transmit/receive operations
- Maximize scalability for number of connections / buffer sizes / queue sizes / protocols supported
- Minimize protocol specific features
- Minimize complexity

11.1.1.1 Ring Accelerator (RINGACC)

The ring accelerator (RINGACC or RA) is a hardware module that is responsible for accelerating management of various types of queues in the system. The RINGACC accelerates passing of packets between a producer and consumer in normal system memory (including cached memory). The RINGACC is capable of accelerating the read/write pointer maintenance and occupancy tracking operations.

The ring accelerator operates like a bus infrastructure bridge in that it passes transactions through it between a source and destination interface. As transactions are passed, the RINGACC modifies the address, byte count, and transaction identifiers and internally updates the occupancies/pointers.

Each queue that the RINGACC provides can operate in either exposed-ring-mode or private-queue-mode.

- The exposed ring mode allows software to directly access the underlying ring structure to add or remove items from the tail or head of the ring respectively. Whenever items are added or removed from a ring, the host software is required to write to a corresponding doorbell register (RINGRT[a]_RT_DB) to increment or decrement the ring occupancy. When using the exposed ring mode, no proxy is required between the software and the RINGACC but all queue add operations require a memory fence to be performed to ensure that the data has landed in a snoopable cache before the doorbell register is written.
- The private queue mode provides an abstract view of the ring so that the host software does not need to know the actual physical address location or current read or write indexes of the ring. The private queue mode provides a memory window for each ring which when written redirects the write to the address pointed to by the write pointer and when read redirects the read to the address pointed to by the read pointer. The same address range is always used to push or pop elements from a given queue.

Rings are an implementation of a logical queue with the following limitations:

- Each ring has a finite size. When rings are used in exposed ring mode the following conditions apply:
  - A separate operation is required to write/read the contents of a ring and to update the occupancy of the ring

- It is not straightforward to allow multiple producers to write to a ring or multiple consumers to read from a ring. Additional synchronization and pointer passing is required since rings require software to manage one of the pointers for the queue.
- An exposed ring cannot be used when software or hardware needs to both read and write the same queue (such as for a DMA RX free queue where errors can have the DMA write the element back onto the same RX free queue). Since software owns one side of the pointers and hardware owns the other, they cannot be kept coherent if either side needs to update either at any time.

The RINGACC allows each ring to be configured to a different primary element size. Element sized chunks of data are placed onto and retrieved from rings when queuing or de-queueing occurs. Element sizes can be as small as 4 bytes or as large as 256 bytes.

11.1.1.2 Secure Proxy (SEC_PROXY)

A proxy provides a mechanism for software to access the RINGACC coherently when the processor does not support large bursts. The RINGACC requires a single burst for each operation so that it maintains atomicity and coherence by relying on the atomicity of the bursts on the bus interconnect fabric, since it only delivers a single burst to the RINGACC before the next. Since processors are usually limited in the size of a burst they can deliver natively, such as 32 to 128 bits, they cannot be used directly with the data access region of the RINGACC for larger element sizes. The proxy solves this gap by providing a temporary space for the software to form a larger burst of data before it is sent to the RINGACC. The proxy allows smaller processor accesses to the data and only forwards to the RINGACC when the entire data burst is complete, as directed by the software.

Each proxy hardware can support multiple threads of software (whether on the same or different processors) operating on bursts at the same time, and they do not interfere with each other, as long as each thread of software only operates on its thread in the proxy. Each proxy thread also supports access to any RINGACC queue via different offsets similar to how the RINGACC provides access to the queues via different offsets.

A special version of a proxy is the Secure Proxy that provides secured access to RINGACC queues for communication to the security initiator of the system. It provides basically the same function as a normal proxy. The data burst size is fixed for message sizes to the security initiator, so there is no support for all the element sizes of the RINGACC. The security initiator locks down the RINGACC queue to access and direction for each proxy thread so that the software cannot access anything they shouldn’t, so the software only sees a single queue (unlike the normal proxy), and any attempts to access another queue or access it in violation of how the security initiator defined and an error will be flagged. This allows for a much more controlled setup for passing messages to the security initiator.

11.1.1.3 Interrupt Aggregator (INTAGGR)

The interrupt aggregator (INTAGGR or INTA) is a hardware module which provides a persistent view of the real time status of various DMA components within the overall SoC DMA system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

The INTA block provides the following functions:

- Conversion of local event signal lines into global events
- Performing an 'Y-split' operation of global events
- Counting global events
- Steering and aggregation of global events into specified bit positions in one of N interrupt cause registers
- SoC interrupt-architecture-compliant set/clear and mask set/clear functionality to cover interrupt cause registers

11.1.1.4 Packet DMA (PKTDMA)

The PKTDMA module supports the transmission and reception of various packet types. The PKTDMA is architected to facilitate the segmentation and reassembly of DMA data structure compliant packets to/from smaller data blocks that are natively compatible with the specific requirements of each connected peripheral. Multiple Tx and Rx channels are provided within the DMA which allow multiple segmentation or reassembly operations to be ongoing. The DMA controller maintains state information for each of the channels which allows packet segmentation and reassembly operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs for Transmit operations. The ordering and rate of Receive operations is indirectly controlled by the order in which blocks are pushed into the DMA on the Rx PSI-L interface.

A block diagram of the PKTDMA Controller is shown below:

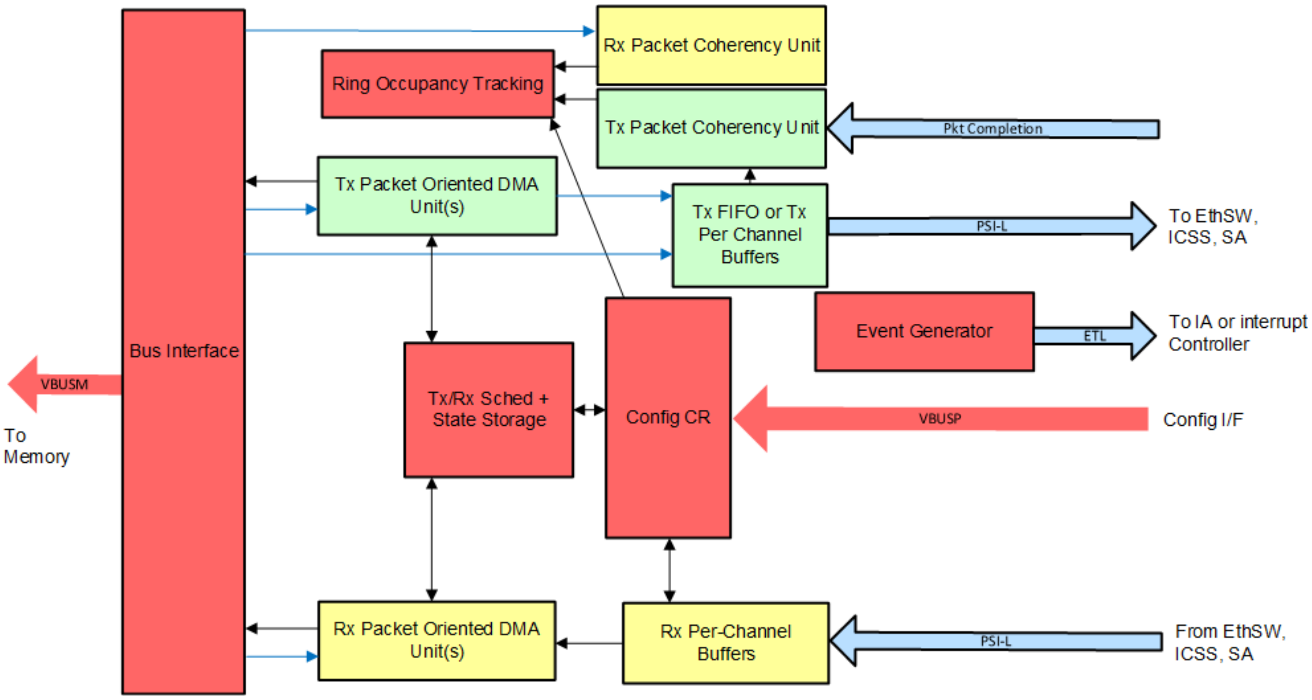

Figure 11-1. PKTDMA Block Diagram

11.1.1.4.1 PKTDMA Submodule Descriptions

11.1.1.4.1.1 Bus Interface Unit

The Bus Interface Unit is responsible for merging and buffering all of the transactions that originate from the various initiator blocks inside the DMA controller into the 4 separate VBUSM initiator interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.4.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.4.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Tx Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Tx PKTDMA core blocks, and writing back the updated state returned from those same DMA core blocks.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the Rx DMA functions including the default settings for the free descriptor and destination queues. For modularity and high speed pipelining reasons, the Rx traffic is looped through the Configuration Registers block where the original stream information is merged with information from the configuration registers on its way to the Rx DMA unit module. This prevents the Rx DMA Core from having to spend cycles accessing the channel configuration information for the channel.

11.1.1.4.1.3.1 RX State Mapping

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">sop_descriptor_ptr[35:4]</td></tr>
<tr><td colspan="32">0x80</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="12">sop_descriptor_ptr[35:4]</td><td colspan="4">sop_descriptor_asel</td><td colspan="16">curr_descriptor_ptr</td></tr>
<tr><td colspan="32">0x84</td></tr>
<tr><td>64</td><td>65</td><td>66</td><td>67</td><td>68</td><td>69</td><td>70</td><td>71</td><td>72</td><td>73</td><td>74</td><td>75</td><td>76</td><td>77</td><td>78</td><td>79</td><td>80</td><td>81</td><td>82</td><td>83</td><td>84</td><td>85</td><td>86</td><td>87</td><td>88</td><td>89</td><td>90</td><td>91</td><td>92</td><td>93</td><td>94</td><td>95</td></tr>
<tr><td colspan="28">curr_descriptor_ptr</td><td colspan="4">curr_descriptor_asel</td></tr>
<tr><td colspan="32">0x88</td></tr>
<tr><td>96</td><td>97</td><td>98</td><td>99</td><td>100</td><td>101</td><td>102</td><td>103</td><td>104</td><td>105</td><td>106</td><td>107</td><td>108</td><td>109</td><td>110</td><td>111</td><td>112</td><td>113</td><td>114</td><td>115</td><td>116</td><td>117</td><td>118</td><td>119</td><td>120</td><td>121</td><td>122</td><td>123</td><td>124</td><td>125</td><td>126</td><td>127</td></tr>
<tr><td colspan="32">curr_buffer_ptr</td></tr>
<tr><td colspan="32">0x8C</td></tr>
<tr><td>128</td><td>129</td><td>130</td><td>131</td><td>132</td><td>133</td><td>134</td><td>135</td><td>136</td><td>137</td><td>138</td><td>139</td><td>140</td><td>141</td><td>142</td><td>143</td><td>144</td><td>145</td><td>146</td><td>147</td><td>148</td><td>149</td><td>150</td><td>151</td><td>152</td><td>153</td><td>154</td><td>155</td><td>156</td><td>157</td><td>158</td><td>159</td></tr>
<tr><td colspan="16">curr_buffer_ptr</td><td colspan="4">curr_buffer_asel</td><td colspan="12">curr_buffer_length</td></tr>
<tr><td colspan="32">0x90</td></tr>
<tr><td>160</td><td>161</td><td>162</td><td>163</td><td>164</td><td>165</td><td>166</td><td>167</td><td>168</td><td>169</td><td>170</td><td>171</td><td>172</td><td>173</td><td>174</td><td>175</td><td>176</td><td>177</td><td>178</td><td>179</td><td>180</td><td>181</td><td>182</td><td>183</td><td>184</td><td>185</td><td>186</td><td>187</td><td>188</td><td>189</td><td>190</td><td>191</td></tr>
<tr><td colspan="10">curr_buffer_length</td><td colspan="22">curr_buffer_offset</td></tr>
<tr><td colspan="32">0x94</td></tr>
<tr><td>192</td><td>193</td><td>194</td><td>195</td><td>196</td><td>197</td><td>198</td><td>199</td><td>200</td><td>201</td><td>202</td><td>203</td><td>204</td><td>205</td><td>206</td><td>207</td><td>208</td><td>209</td><td>210</td><td>211</td><td>212</td><td>213</td><td>214</td><td>215</td><td>216</td><td>217</td><td>218</td><td>219</td><td>220</td><td>221</td><td>222</td><td>223</td></tr>
<tr><td>curr_buffer_eop</td><td colspan="21">pkt_length</td><td>flush</td><td colspan="6">ps_wordcnt</td><td>flowid_is_default</td><td colspan="2">drop_flush</td></tr>
<tr><td colspan="32">0x98</td></tr>
<tr><td>224</td><td>225</td><td>226</td><td>227</td><td>228</td><td>229</td><td>230</td><td>231</td><td>232</td><td>233</td><td>234</td><td>235</td><td>236</td><td>237</td><td>238</td><td>239</td><td>240</td><td>241</td><td>242</td><td>243</td><td>244</td><td>245</td><td>246</td><td>247</td><td>248</td><td>249</td><td>250</td><td>251</td><td>252</td><td>253</td><td>254</td><td>255</td></tr>
<tr><td colspan="7">ps offset</td><td colspan="4">ps_flags</td><td colspan="13">pktid_data</td><td colspan="4">orderid</td><td colspan="3">priority</td><td></td></tr>
<tr><td colspan="32">0x9C</td></tr>
</table>

Table 11-1. RX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
213 - 193	21 - 1	0x98	pkt_length	The size of the packet length
214	22	0x98	flush	The packet is being flushed
220 - 215	28 - 23	0x98	ps_wordcnt	protocol specific word count
221	29	0x98	flowid_is_default	Use default flow id
223 - 222	31 - 30	0x98	drop_flush	The flush is a drop condition
230 - 224	6 - 0	0x9C	ps offset	protocol specific offset
234 - 231	10 - 7	0x9C	ps_flags	protocol specific flags
247 - 235	23 - 11	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.3.2 TX State Mapping

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">sop_descriptor_ptr[35:4]</td></tr>
<tr><td colspan="32">0x80</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="12">sop_descriptor_ptr[35:4]</td><td colspan="4">sop_descriptor_asel</td><td colspan="16">curr_descriptor_ptr</td></tr>
<tr><td colspan="32">0x84</td></tr>
<tr><td>64</td><td>65</td><td>66</td><td>67</td><td>68</td><td>69</td><td>70</td><td>71</td><td>72</td><td>73</td><td>74</td><td>75</td><td>76</td><td>77</td><td>78</td><td>79</td><td>80</td><td>81</td><td>82</td><td>83</td><td>84</td><td>85</td><td>86</td><td>87</td><td>88</td><td>89</td><td>90</td><td>91</td><td>92</td><td>93</td><td>94</td><td>95</td></tr>
<tr><td colspan="28">curr_descriptor_ptr</td><td colspan="4">curr_descriptor_asel</td></tr>
<tr><td colspan="32">0x88</td></tr>
<tr><td>96</td><td>97</td><td>98</td><td>99</td><td>100</td><td>101</td><td>102</td><td>103</td><td>104</td><td>105</td><td>106</td><td>107</td><td>108</td><td>109</td><td>110</td><td>111</td><td>112</td><td>113</td><td>114</td><td>115</td><td>116</td><td>117</td><td>118</td><td>119</td><td>120</td><td>121</td><td>122</td><td>123</td><td>124</td><td>125</td><td>126</td><td>127</td></tr>
<tr><td colspan="32">curr_buffer_ptr</td></tr>
<tr><td colspan="32">0x8C</td></tr>
<tr><td>128</td><td>129</td><td>130</td><td>131</td><td>132</td><td>133</td><td>134</td><td>135</td><td>136</td><td>137</td><td>138</td><td>139</td><td>140</td><td>141</td><td>142</td><td>143</td><td>144</td><td>145</td><td>146</td><td>147</td><td>148</td><td>149</td><td>150</td><td>151</td><td>152</td><td>153</td><td>154</td><td>155</td><td>156</td><td>157</td><td>158</td><td>159</td></tr>
<tr><td colspan="16">curr_buffer_ptr</td><td colspan="4">curr_buffer_asel</td><td colspan="12">curr_buffer_length</td></tr>
<tr><td colspan="32">0x90</td></tr>
<tr><td>160</td><td>161</td><td>162</td><td>163</td><td>164</td><td>165</td><td>166</td><td>167</td><td>168</td><td>169</td><td>170</td><td>171</td><td>172</td><td>173</td><td>174</td><td>175</td><td>176</td><td>177</td><td>178</td><td>179</td><td>180</td><td>181</td><td>182</td><td>183</td><td>184</td><td>185</td><td>186</td><td>187</td><td>188</td><td>189</td><td>190</td><td>191</td></tr>
<tr><td colspan="10">curr_buffer_length</td><td colspan="22">curr_buffer_offset</td></tr>
<tr><td colspan="32">0x94</td></tr>
<tr><td>192</td><td>193</td><td>194</td><td>195</td><td>196</td><td>197</td><td>198</td><td>199</td><td>200</td><td>201</td><td>202</td><td>203</td><td>204</td><td>205</td><td>206</td><td>207</td><td>208</td><td>209</td><td>210</td><td>211</td><td>212</td><td>213</td><td>214</td><td>215</td><td>216</td><td>217</td><td>218</td><td>219</td><td>220</td><td>221</td><td>222</td><td>223</td></tr>
<tr><td>curr_buffer_eop</td><td colspan="22">rem_length</td><td>info_present</td><td>truncated_non_eop</td><td colspan="7">psbytes_rem</td></tr>
<tr><td colspan="32">0x98</td></tr>
<tr><td>224</td><td>225</td><td>226</td><td>227</td><td>228</td><td>229</td><td>230</td><td>231</td><td>232</td><td>233</td><td>234</td><td>235</td><td>236</td><td>237</td><td>238</td><td>239</td><td>240</td><td>241</td><td>242</td><td>243</td><td>244</td><td>245</td><td>246</td><td>247</td><td>248</td><td>249</td><td>250</td><td>251</td><td>252</td><td>253</td><td>254</td><td>255</td></tr>
<tr><td>psbytes_rem</td><td colspan="8">psbytes_off</td><td colspan="13">wptr_data</td><td colspan="2">pktid_data</td><td colspan="4">orderid</td><td colspan="3">priority</td><td></td></tr>
<tr><td colspan="32">0x9C</td></tr>
</table>

Table 11-2. TX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
214 - 193	22 - 1	0x98	rem_length	The remaining length in the buffer
215	23	0x98	info_present	The packet has info present
216	24	0x98	truncated_non_eop	Eop if packet length is greater than the total buffer length
223 - 217	31 - 25	0x98	psbytes_rem	Number of protocol specific bytes remaining
224	0	0x9C	psbytes_rem	Number of protocol specific bytes remaining
232 - 225	8 - 1	0x9C	psbytes_off	The offset of the protocol specific bytes
245 - 233	21 - 9	0x9C	wptr_data	The current write pointer in the data fifo
247 - 246	23 - 22	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.4 Tx Packet DMA Unit

The Tx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Host Tx protocol. The Tx Packet DMA unit initiates VBUSM transactions in order to read descriptor pointers from the memory mapped Tx ring, read descriptors from memory, and read data from buffers in memory.

11.1.1.4.1.5 Tx Packet Coherency Unit

The Tx Packet Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the Tx DMA unit(s) and that all previous packets on that channel/flow have also completed prior to incrementing the reverse ring occupancy for the channel/flow.

11.1.1.4.1.6 Tx Per Channel Buffers

The Tx Per Channel Buffers implement a FIFO for each Tx DMA channel that is used for buffering packet control and payload data that has been fetched by the Tx Packet DMA units. The buffers are byte oriented on write so that the data from the DMA units which may not be full words can be packed properly. The buffers are block oriented on read and each Tx (source) channel in the PKTDMA controller maps directly onto a thread in the Tx PSI interface. The Tx Per Channel Buffer block outputs queue fullness information to the Tx Scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Tx Per Channel Buffer will initiate transfers to the target whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Transmit PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.1.1.4.1.7 Rx Per Channel Buffers

The Rx Per Channel Buffers implement a FIFO for each Rx DMA channel that is used for buffering packet control and payload data that has been pushed into the DMA from the Rx PSI-L interface. The Rx Per Channel Buffers also includes an arbitration unit which determines which Rx DMA channel should be serviced next.

11.1.1.4.1.8 Rx Packet DMA Unit

The Rx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Rx protocol for Host descriptor types. The Rx Packet DMA Unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read buffer descriptor information, write descriptors to memory, and write data to buffers in memory.

11.1.1.4.1.9 Rx Packet Coherency Unit

The Rx Packet Coherency Unit is responsible for ensuring that all control structures and data have been written by the Rx DMA unit(s) and that all previous packets on that channel/flow have completed prior to incrementing the reverse ring occupancy for the channel/flow. This unit ensures that the ordering of the Packet Descriptor pointer writes to the return queue directly matches the ordering in which those packets were fetched from the Rx free queues. Writes are not considered complete by this unit until the entire write status has been returned for all outstanding transactions for a given packet ID.

11.1.1.4.1.10 Event Handler

The Event Handler block is responsible for generating channel completion and error events.

11.1.1.4.2 Channel Classes

Not all channels within the PKTDMA require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the PKTDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

PKTDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.1.5 Block Copy DMA (BCDMA)

The Block Copy DMA is intended to perform similar functions as an Embedded DMA (EDMA) and the UDMA-P. The BCDMA module moves data from a memory mapped source address set to a corresponding memory mapped address. The BCDMA maintains state information for each of the channels which allows data copy operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs.

A block diagram of the Block Copy DMA Controller is shown below:

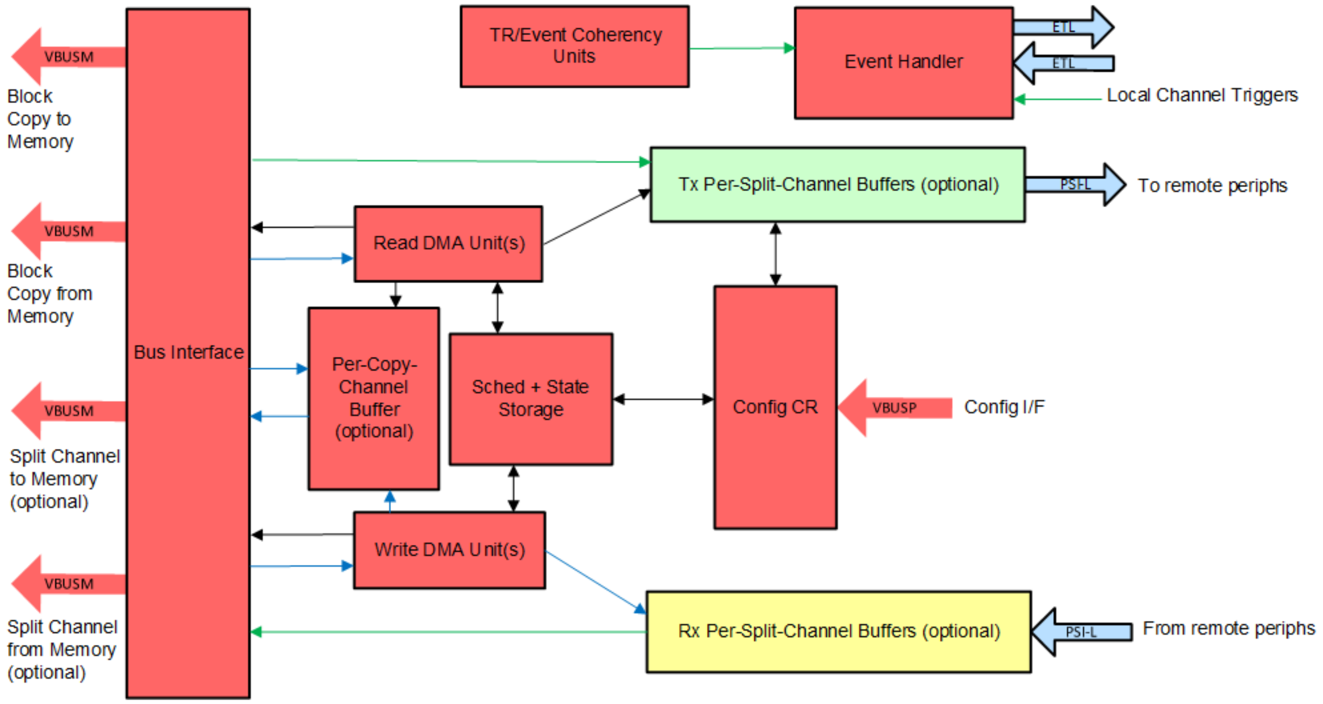

Figure 11-2. Block Copy DMA Block Diagram

11.1.1.5.1 BCDMA Submodule Descriptions

11.1.1.5.1.1 Bus Interface Unit

The Bus Interface Unit is reponsible for merging and buffering all of the transactions that originate from the various controller blocks inside the DMA controller into the 4 seperate VBUSM controller interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.5.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.5.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Read and Write DMA units, and writing back the updated state returned from those same DMA units.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the DMA channels.

11.1.1.5.1.3.1 BCDMA Mapping Table

Table 11-3 applies to TX, RX and BC Mapping.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
reload_count				waitcomp	event_size		trigger0		trigger0_type		trigger1_type		trigger1_type		spflags				eop	eol			reload_count								
0x80																															
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
tr_dim1																															
0x84																															
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
tr_dim2																															
0x88																															
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
tr_dim3																															
0x8C																															
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
tr_icnt0																tr_icnt1															
0x90																															
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
tr_icnt2																tr_icnt3															
0x94																															
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
icnt1																icnt2															
0x98																															
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
icnt3																rem_icnt0															
0x9C																															
256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
tr_addr																															
0xA0																															
288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
tr_addr				tr_asel				descriptor_ptr																							
0xA4																															
320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
descriptor_ptr												RVSD				curr_index														last_index	
0xA8																															
352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
last_index												nom_elsize			reload_index						curr_wptr										
0xAC																															
384		385		386		387		388		389		390		391		392		393		394		395		396		397		398		399	

curr_wptr	pktid	orderid	priority	trid	evtid	sot
0xB0						

Table 11-3. BCDMA Mapping Table

Total Bits	Bits	Register Offset	Field	Description
3 - 0	3 - 0	0x80	reload_count	
4	4	0x80	waitcomp	
6 - 5	6 - 5	0x80	event_size	
8 - 7	8 - 7	0x80	trigger0	
10 - 9	10 - 9	0x80	trigger0_type	
12 - 11	12 - 11	0x80	trigger1_type	
14 - 13	14 - 13	0x80	trigger1_type	
18 - 15	18 - 15	0x80	spflags	
19	19	0x80	eop	
22 - 20	22 - 20	0x80	eol	
31 - 23	31 - 23	0x80	reload_count	
63 - 32	31 - 0	0x84	tr_dim1	
95 - 64	31 - 0	0x88	tr_dim2	
127 - 96	31 - 0	0x8C	tr_dim3	
143 - 128	15 - 0	0x90	tr_icnt0	
159 - 144	31 - 16	0x90	tr_ictn1	
175 - 160	15 - 0	0x94	tr_ictn2	
191 - 176	31 - 16	0x94	tr_icnt3	
207 - 192	15 - 0	0x98	icnt1	
223 - 208	31 - 16	0x98	icnt2	
239 - 224	15 - 0	0x9C	icnt3	
255 - 240	31 - 16	0x9C	rem_icnt0	
287 - 256	31 - 0	0xA0	tr_addr	
291 - 288	3 - 0	0xA4	tr_addr	
295 - 292	7 - 4	0xA4	tr_asel	
319 - 296	31 - 8	0xA4	descriptor_ptr	
331 - 320	11 - 0	0xA8	descriptor_ptr	
349 - 336	29 - 16	0xA8	curr_index	
363 - 350	11 - 30	0xA8	last_index	
366 - 364	14 - 12	0xAC	nom_elsize	
372 - 367	20 - 15	0xAC	reload_index	
385 - 373	1 - 21	0xAC	curr_wptr	
387 - 386	3 - 2	0xB0	pktid	
391 - 388	7 - 4	0xB0	orderid	
394 - 392	10 - 8	0xB0	priority	
396 - 395	12 - 11	0xB0	trid	
398 - 397	14 - 13	0xB0	evtid	

Table 11-3. BCDMA Mapping Table (continued)

Total Bits	Bits	Register Offset	Field	Description
399	15	0xB0	sot	

11.1.1.5.1.4 Read Unit(s)

The Read Units implement all of the state machine functionality necessary to perform the read transfers defined in the SW supplied Transfer Request records. The read DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors, Transfer Request records, and payload data from memory.

11.1.1.5.1.5 TR Coherency Unit

The TR Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the BCDMA unit(s) and all prior TRs have completed prior to incrementing the reverse ring occupancy for the flow/channel.

11.1.1.5.1.6 Per-Copy-Channel Buffers

The Per-Copy-Channel Buffers implement a FIFO for each BCDMA generic block copy channel and is used for buffering payload data that has been fetched by read DMA unit modules. The write DMA units issue write transfers from the Per Channel Buffers to specified addresses in memory. The buffers are byte oriented on both write and read so that the data from the DMA units which may not be full words can be packed and unpacked properly. This unit is optional and is only present if one or more generic block copy channels are configured in the BCDMA instance.

11.1.1.5.1.7 Tx Per-Split-Channel Buffers

The Tx Per-Split-Channel Buffers implement a FIFO for each BCDMA Tx split mode channel and is used for buffering payload data that has been fetched by read DMA unit modules. Data is transferred from the buffer to the remote peripheral via a PSI-L interface. This unit is optional and is only present if one or more Tx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.8 Rx Per-Split-Channel Buffers

The Rx Per-Split-Channel Buffers implement a FIFO for each BCDMA Rx split mode channel and is used for buffering payload data that has been received from remote peripherals via a PSI-L interface. Data is read from these FIFOs and written out to memory as directed by the write DMA unit modules. This unit is optional and is only present if one or more Rx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.9 Write Unit(s)

The Write Units implement all of the state machine functionality necessary to perform the write transfers defined in the SW supplied Transfer Request records. The write DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors and/or Transfer Request records from memory mapped rings, read descriptor and Transfer Request records, and write payload data to memory.

11.1.1.5.1.10 Event Coherency Unit

The Event Coherency Unit is responsible for ensuring that all writes have completed prior to signaling an output event for a channel/flow.

11.1.1.5.1.11 Event Handler

The Event Handler block is responsible for generating channel completion and error events and for accepting and tracking channel triggering.

11.1.1.5.2 Channel Classes

Not all channels within a DMA controller require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the BCDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor and TR prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor and TR prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

BCDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.2 Definition of Terms

Host— The host is an intelligent system resource that configures and manages each communications control module. The host is responsible for allocating memory, initializing all data structures, and responding to port interrupts.

Channel— A channel refers to the sub-division of information (flows) that is transported across a DMA engine. Each channel has associated state information. Channels are used to segregate information flows based on the protocol used, scheduling requirements (for example, CBR, VBR, ABR), or concurrency requirements (that is, blocking avoidance). Information flow within a channel is a stream of strongly ordered information.

Data Buffer— A data buffer is a single data structure that contains payload information for transmission to or reception from a channel.

Buffer Descriptor— A buffer descriptor is a single data structure that contains information about one or more data buffers.

Packet Descriptor— A packet descriptor is another name for the first buffer descriptor within a packet. Some fields within a data buffer descriptor are only valid when it is a packet descriptor including the tags, packet length, packet type, and flags. All Monolithic type descriptors are packet descriptors (and are also a Data Buffer).

Queue— A queue is a list of strongly ordered entries which is typically used to pass work between a producer and a consumer. Queue entries in most cases are references to a work payload which is being passed, but in some cases, (Transfer Request Packets for example) queue entries may actually contain data which is being transferred. Queues are used throughout DMA whenever communication is required between entities. Queues can have multiple different implementations and DMA uses two of the most common: linked lists and rings.

Linked list— A linked list is a data structure in which each entry stores not only the entry data but also a chaining pointer to the next entry in the list. The last entry in each list has its chaining pointer set to NULL (typically encoded as 0x0). The list manager maintains a pointer to the head element on the list and to the tail element on the list. Since the chaining pointer is stored with the entry data, linked lists have a length which is dynamically changeable and limited only by the ability to allocate additional entries which are to be queued/de-queued. Linked lists are present in Host Descriptors to chain multiple descriptors to form a packet.

Ring— A ring is a data structure in which a contiguous memory block defined by M N-byte entries (total size is M × N bytes) is statically allocated and sequentially written/read in order to pass data or data references. Rings are also referred to as circular buffers because when the last element in the contiguous memory array is written, the pointers wrap back to the beginning address for the ring and start the process all over again. The Ring Accelerator component uses rings in order to implement logical queues.

Free Descriptor/Buffer Queue— A free descriptor/buffer queue is a list of available descriptors with prelinked empty buffers that are to be used by the receive ports for host type descriptors. Free Descriptor/Buffer Queues are implemented by the Ring Accelerator.

Free Descriptor Queue— A free descriptor queue is a list of available descriptors that are not yet linked with buffers that are to be used by the receive ports for monolithic type descriptors. Free Descriptor Queues are implemented by the Ring Accelerator.

Packet Queue— A packet queue is a list of valid (that is, populated) packet descriptors that is used for forwarding a packet from one entity to another for any number of purposes. Packet Queues are implemented by the Ring Accelerator.

Memory— Memory is an area of data storage managed by the host. This area is visible to the port as a 64-bit addressable area.

Device Driver— A device driver is application independent software that runs on the host for purposes abstracting the low level hardware so that upper level software can use the hardware without knowing every bit field location or initialization sequence. General device driver functions include port initialization, transmit packet queuing, and receive packet processing.

SOP— Start of Packet. This refers to the descriptor/buffer that is the first buffer in a packet.

MOP— Middle of Packet. This refers to the descriptors/buffers that are neither the first or last buffers in a packet.

EOP— End of Packet. This refers to the descriptor/buffer that is the last buffer in a packet.

11.1.3 DMSS Hardware/Software Interface

The intent of the Data Movement architecture is to provide a uniform HW/SW interface which includes a rich set of mechanisms that SW can make use of to transfer data with low overhead and reasonable complexity. To this goal, the number of components which SW is required to interact with on an ongoing real time basis has been kept to a minimum and is as follows (in order of anticipated frequency of access):

- Interrupt Aggregator
- Packet DMA
- Block Copy DMA

When interrupts are used, the interrupt aggregator will provide the vast majority of interrupt sources from all DMA components in the system. Each non-exception/non-debug packet and TR completion signaling originates from the Interrupt Aggregator and the IA provides a uniform set of MMRs that can be queried to quickly determine the cause of a specific interrupt. Events from PSI-L/ETL components are all routed to the host via the Interrupt Aggregator.

Each PKTDMA and BCDMA instance includes an inbuilt ring control mechanism which is the primary means by which work is sent to or received from these DMAs. Each DMA instance also includes both static configuration type memory mapped registers and some real-time accessible memory mapped registers for monitoring and control of each individual channel.

Memory mapped data structures are used anytime information needs to be passed between components in the system. These components may be hardware or software. The following sections describe the data structures which are used within the DMSS for passing information. These data structures include data buffers, packet descriptors, buffer descriptors, queues (including transmit queues, transmit completion queues, and receive queues) and the configuration MMRs that are provided in the various components. The following sections provide a detailed description of these data structures.

11.1.3.1 Data Buffers

A data buffer is a byte aligned contiguous block of memory used to store payload data. Each buffer is described in an entry in either a packet descriptor or in a buffer descriptor. A data buffer may hold any portion of a packet and may be linked together (via descriptors) with other buffers to form packets. Data buffers may be allocated anywhere within the 64-bit memory space.

The Buffer Length field of the packet/buffer descriptor indicates the number of valid data bytes in the buffer. There may be from 1 to 4M-1 valid data bytes in each buffer.

11.1.3.2 Descriptors

Descriptors are so named because their primary function is to describe other data structures.

The PKTDMA architecture provides for 2 basic types of descriptors whose characteristics are shown in PKTDMA Descriptor Types and Attributes.

Table 11-4. PKTDMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descriptors Within Same Packet	Description
Host Packet Descriptor	✓	1	✓	✓	Used to describe packet and SOP buffer in applications that require Host OS compatible data structures (i.e. applications where the descriptors and buffers cannot be managed independently but must instead be pre-linked by the Host software). These applications inherently require a separate descriptor for each buffer.
Host Buffer Descriptor		1		✓	Used to describe non-SOP buffers in applications that require Host OS compatible data structures

As the above table shows, the Host Packet Descriptor provides packet level information that is useful to both the ports and the Host in order to properly process the packet. These descriptors are referred to as Packet Descriptors and will always appear as the first descriptor within a packet.

The PKTDMA allows descriptors to be allocated on 16-byte address boundaries. This is intended to allow for better memory utilization by allowing on-chip descriptors which are not a power of 2 in length to be packed into arrays with little wasted memory space.

Even though descriptors and buffers may be allocated on any 16-byte alignment, careful consideration of the alignment effects should be made based on the storage location and any cache related affects that may exist. If data structures are placed in off-chip SDRAM the burst size and alignment restrictions of the memory devices must be considered in order to avoid performance issues related to continually fetching mis-aligned blocks. In this case, the memory efficiency can be reduced to 50% because 2 memory bank lines are read for every line sized data fetch. Similarly, placing more than one descriptor or buffer object within a single cache line can cause the adjacent object to become corrupted during cache line writeback operations.

Software/application specific control information may be added to the end of any of the packet descriptor types using as many extra words as necessary but the above alignment rules still apply.

The Block Copy DMA architecture provides a single descriptor type whose characteristics are shown in Block Copy DMA Descriptor Types and Attributes.

Table 11-5. Block Copy DMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descriptors Within Same Packet	Description
Transfer Request Packet Descriptor		0			Used to feed transfer request sequences to the BCDMA

11.1.3.2.1 Host Packet Descriptor

Host Packet Descriptors are designed to be used when the application requires support for true, unlimited fragment count scatter/gather type operations. The Host Packet Descriptor contains the following information:

- Indicator which identifies the descriptor as a Host Packet Descriptor
- Source and Destination Tags
- Packet Type
- Packet Length
- Protocol Specific Region Size
- Protocol Specific Control / Status Bits
- Pointer to the first valid byte in the SOP data buffer
- Length of the SOP data buffer
- Pointer to the next buffer descriptor in the packet
- Software specific information

Host Packet Descriptors always contain 48 bytes of required information and may also contain optional software specific information and protocol specific information. How much optional information (and therefore the allocated size of the descriptors) is required is application dependent.

The Host Packet descriptor layout is shown below.

Table 11-6. Host Packet Descriptor Layout

Packet Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)
Extended Packet Info Block (Optional) Includes Timestamp and Software Data (16 bytes)
Protocol Specific Data (Optional) (0 to M bytes where M is a multiple of 4)

Table 11-6. Host Packet Descriptor Layout (continued)

Other SW Data (Optional and User Defined)

Host Packet Descriptors may be linked with zero or more additional Host Buffer Descriptors in a singly linked list fashion to form packets. Each Host Packet consists of a single Host Packet Descriptor followed by a chain of zero or more Host Buffer Descriptors linked together using the Next Descriptor Pointer fields in the descriptors. The last descriptor in a Host packet has a zero Next Descriptor Pointer.

The ‘Other SW Data’ portion of the descriptor exists after all of the defined words and is reserved for use by the host software to store completely private data. This region is not used in any way by HW components in a PKTDMA system and these modules will not modify any bytes within this region.

The contents of the Host Packet Descriptor words are detailed in Table 11-7 through Table 11-23

Table 11-7. Host Packet Descriptor Packet Information Word 0 (PD Word 0)

Bits	Name	Description	Rx Overwrite
31:30	2’d1	64-bit Host Packet Descriptor Type Identifier	Yes
29	Extended Packet Info Block Present	This field indicates the presence of the Extended Packet Info Block in the descriptor. 0 = EPIB is not present 1 = 16 byte EPIB is present	Yes
28	RESERVED	-	*Yes*
27:22	Protocol Specific Valid Word Count	This field indicates the valid # of 32-bit words in the protocol specific region. This is encoded in increments of 4 bytes as follows: 0 = 0 bytes 1 = 4 bytes … 16 = 64 bytes ... 32 = 128 bytes 33-63 = RESERVED	Yes

Table 11-7. Host Packet Descriptor Packet Information Word 0 (PD Word 0) (continued)

Bits	Name	Description	Rx Overwrite
21:0	Packet Length	The length of the packet in bytes. If the Packet Length is less than the sum of the buffer lengths, then the packet data will be truncated. A Packet Length greater than the sum of the buffers is an error. The valid range for an exact packet length is 0 to 4M-1 bytes. If the packet length is set to 0, the port will not actually transmit any information.	Yes

Table 11-8. Host Packet Descriptor Packet Information Word 1 (PD Word 1)

Bits	Name	Description	Rx Overwrite
31:28	Error Flags	This field contains error flags that can be assigned based on the packet type	Yes
27:24	Protocol Specific Flags	This field contains protocol specific flags / information that can be assigned based on the packet type.	Yes
23:14	RESERVED	-	Yes
13:0	Flow ID	Flow ID within which this packet is being transported. The FlowID is used by downstream blocks to make decisions about packet steering and resource allocations. FlowIDs are also used to allow specific packets to be received into specific sets of buffers.	Yes

Table 11-9. Host Packet Descriptor Packet Information Word 2 (PD Word 2)

Bits	Name	Description	Rx Overwrite
31:27	Packet Type	This field indicates the type of this packet and is encoded as follows: 0-31 = Application specific	Yes
26:16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-10. Host Packet Descriptor Packet Information Word 3 (PD Word 3)

Bits	Name	Description	Rx Overwrite
31:24	Source Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 15:8.	Yes
23:16	Source Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 7:0.	Yes
15:8	Dest Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 15:8.	Yes
7:0	Dest Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 7:0	Yes

Table 11-11. Host Packet Descriptor Linking Word 0 (PD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-12. Host Packet Descriptor Linking Word 1 (PD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No

Table 11-12. Host Packet Descriptor Linking Word 1 (PD Word 5) (continued)

Bits	Name	Description	Rx Overwrite
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-13. Host Packet Descriptor Buffer 0 Info Word 0 (PD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception. These are the 32 LSBs of the 48-bit buffer pointer. **THIS Value along with the MSB bits cannot be 0 or the buffer will be seen as a NULL PTR**	Yes

Table 11-14. Host Packet Descriptor Buffer 0 Info Word 1 (PD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		Yes

Table 11-14. Host Packet Descriptor Buffer 0 Info Word 1 (PD Word 7) (continued)

Bits	Name	Description	Rx Overwrite
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	Yes
15:0	Buffer 0 Pointer MSB	The 16 MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	Yes

Table 11-15. Host Packet Descriptor Buffer 0 Info Word 2 (PD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED	Written to 0	Yes
21:0	Buffer 0 Length	The Buffer Length field indicates how many valid data bytes are in the buffer.	Yes

Table 11-16. Host Packet Descriptor Reserved Word 0 (PD Word 9)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-17. Host Packet Descriptor Reserved Word 1 (PD Word 10)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-18. Host Packet Descriptor Reserved Word 2 (PD Word 11)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
15:0	RESERVED		No

This word is only present if the Extended Packet Info Block present bit is set in Word 0

Table 11-19. Host Packet Descriptor Extended Packet Info Block Word 0 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Timestamp Info	This field contains an application specific timestamp which can be used for traffic shaping in a QoS enabled system.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-20. Host Packet Descriptor Extended Packet Info Block Word 1 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 0	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-21. Host Packet Descriptor Extended Packet Info Block Word 2 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 1	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-22. Host Packet Descriptor Extended Packet Info Block Word 3 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 2	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

Table 11-23. Host Packet Descriptor Protocol Specific Word N (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Protocol Specific Data N	This field stores information which varies depending on the block and packet type.	Configurable

11.1.3.2.2 Host Buffer Descriptor

The Host Buffer Descriptor is identical in size and organization to a Host Packet Descriptor but does not include valid information in the packet level fields and does not include a populated region for protocol specific information. Host Buffer Descriptors are designed to be linked onto a Host Packet Descriptor or another Host Buffer Descriptor to provide support for unlimited scatter / gather type operations. Host Buffer Descriptors provide information about a single corresponding data buffer. Every Host buffer descriptor stores the following information:

- Pointer to the first valid byte in the data buffer
- Length of the data buffer
- Pointer to the next buffer descriptor in the packet

Host Buffer Descriptors always contain 48 bytes of required information. Since it is a requirement that it is possible to convert a Host descriptor between a Buffer Descriptor and a Packet Descriptor (by filling in the appropriate fields) in practice, Host Buffer Descriptors will be allocated using the same sizes as Host Packet Descriptors. The Host Buffer Descriptor layout is shown below.

Table 11-24. Host Buffer Descriptor Layout

Buffer Reclamation Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)

A Host Packet Descriptor and zero or more Host Buffer Descriptors may be linked together using the Next Descriptor Pointer fields to form packets. The last descriptor in a packet has a zero Next Descriptor Pointer. Each Host Buffer descriptor also points to a single data buffer.

The contents of the Host Buffer Descriptor words are detailed in : Table 11-25 through Table 11-33

Table 11-25. Host Buffer Descriptor Reserved Word 0 (BD Word 0)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-26. Host Buffer Descriptor Reserved Word 1 (BD Word 1)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-27. Host Buffer Descriptor Reserved Word 2 (BD Word 2)

Bits	Name	Description	Rx Overwrite
31:16	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-28. Host Buffer Descriptor Reserved Word 3 (BD Word 3)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-29. Host Buffer Descriptor Linking Word 0 (BD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-30. Host Buffer Descriptor Linking Word 1 (BD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No

Table 11-30. Host Buffer Descriptor Linking Word 1 (BD Word 5) (continued)

Bits	Name	Description	Rx Overwrite
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-31. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception. These are the 32 LSBs of the 48-bit buffer pointer.	No

Table 11-32. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	No
15:0	Buffer 0 Pointer MSB	The MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-33. Host Buffer Descriptor Buffer N Info Word 2 (BD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED		No

Table 11-33. Host Buffer Descriptor Buffer N Info Word 2 (BD Word 8) (continued)

Bits	Name	Description	Rx Overwrite
21:0	Buffer N Length	The Buffer Length field indicates how many valid data bytes are in the buffer. Unused or protocol specific bytes at the beginning of the buffer are not counted in the Buffer Length field. This value will be overwritten during reception.	No

11.1.3.2.3 Transfer Request Descriptor

The Transfer Request Descriptor contains the following information:

- Indicator which identifies the descriptor as a TR Descriptor
- Set of one or more Transfer Request Records
- Set of one or more Transfer Response Records

Transfer Request Packet Descriptors always contain 16 bytes of required information and a variable number of Transfer Request / Transfer Response Records (request and response counts match).

The Transfer Request descriptor layout is shown below.

Table 11-34. Transfer Request Packet Descriptor Layout

Packet Info Given via Transfer Request Packet Descriptor Word 0-3 (16 bytes)
Null (0-102 bytes to bring start of TR request array into natural alignment for memory fetch efficiency)
Array of Transfer Request Records
Array of Transfer Response Records

Table 11-35. Transfer Request Packet Descriptor Word 0

Bits	Name	Description	Rx Overwrite
31:30	2’d3	TR Packet Descriptor type.	No
29	RESERVED		No

Table 11-35. Transfer Request Packet Descriptor Word 0 (continued)

Bits	Name	Description	Rx Overwrite
28:20	Reload Count	Specifies what to do when the last entry is processed in this packet. This field specifies how many times to return to the Reload Index upon reaching the Last Entry. When an internal count is incremented to this value and the TR indicated by the Last Entry has been processed, this packet will be considered complete and the descriptor will be placed back on the return queue specified in Word 2. A value of 0x1FF indicates that a perpetual loop is desired. In this case, the loop count is considered infinite and the internal count will not be incremented. A teardown operation on the channel will cause the loop to be broken at the nearest iteration boundary.	No
19:14	Reload Index	Specifies the value to set the current processing index to when the last entry is processed and the Reload Enable is set to 1. This is basically an absolute index to jump to on the 2**nd** and following passes through the TR packet.	No
13:0	Last Entry	Specifies the index of the last valid entry in this packet	No

Table 11-36. Transfer Request Packet Descriptor Word 1

Bits	Name	Description	Rx Overwrite
31:28	RESERVED	-	No
27	RESERVED		No

Table 11-36. Transfer Request Packet Descriptor Word 1 (continued)

Bits	Name	Description	Rx Overwrite
26:24	Transfer Request Nominal Element Size	Specifies the stride between TR entries. The value in this field must be set large enough that any TR in the buffer will fit within the given dimension. TRs are expected to be placed on boundaries as given in this dimension. This field is also used to calculate the location where the Transfer Responses will be written back. This field is encoded as follows: 0 = 16-byte Transfer Request record size 1 = 32-byte Transfer Request record size 2 = 64-byte Transfer Request record size 3 = 128-byte Transfer Request record size 4-7 = RESERVED	No
23:14	RESERVED	-	No
13:0	RESERVED	-	No

Table 11-37. Transfer Request Packet Descriptor Word 2

Bits	Name	Description	Rx Overwrite
31:17	RESERVED		Yes
16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-38. Transfer Request Packet Descriptor Word 3

Bits	Name	Description	Rx Overwrite
31:24	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-39. Transfer Request Packet Descriptor Payload Words 0-N

Bits	Name	Description	Rx Overwrite
31:0	Transfer Control Record Array	Transfer Control Records. This is an array of records which encapsulate the Transfer Request and Transfer Response messages which are used by the BCDMA	Yes (partial)

11.1.3.3 Transfer Request Record

11.1.3.3.1 Overview

This section describes the standard transfer request (TR) format to initiate a DMA transfer. The TRs can support both half and full duplex with multiple dimensions. Each TR will also generate a TR response. A TR can be sent to the BCDMA either through a TR descriptor using a pass-by-reference ring or as a Direct TR submission using a pass-by-value ring.

Table 11-40. Terms and Definitions

Term	Definition
TR	A transfer request to move data.
CR	A cache operation request. A request to send messages to a specified cache controller to prepare the cache for a future operation.

11.1.3.3.2 Addressing Algorithm

For a basic TR request the same algorithm is used. The innermost loop always consumes physically contiguous elements from memory. Its implicit dimension is 1 byte. The pointer itself moves from fetch to fetch on the maximum byte alignments specified for the BCDMA, in increasing order. In each level outside the inner loop, the loop moves the pointer to a new location based on the size of that loop level's dimension.

11.1.3.3.2.1 Linear Addressing (Forward)

The following code illustrates the basic algorithm for a 4-level loop nest block move. This model assumes that it transfers data 1 byte at a time and the input and output block are the same size in all dimensions.

```
// sptr is a byte pointer.
// dptr is a byte pointer.
// Source address is indirect
if (TR_ISA) {
    sptr = *sptr;
}
// Destination address is indirect
if (TR_IDA) {
    dptr = *dptr;
}
// TR_TRIGX can be selected to come from Global events, Local event, or none.
// Check for trigger of TYPE0
if (TR_TRIG0_TYPE == TYPE0) while(!TR_TRIG0);
if (TR_TRIG1_TYPE == TYPE0) while(!TR_TRIG1);
for (i3 = 0; i3 < ICNT3; i3++)
{
    sptr3 = sptr; // save current position before entering next level
    dptr3 = dptr; // save current position before entering next level
    // Check for trigger of TYPE1
    if (TR_TRIG0_TYPE == TYPE1) while(!TR_TRIG0);
    if (TR_TRIG1_TYPE == TYPE1) while(!TR_TRIG1);
    for (i2 = 0; i2 < ICNT2; i2++) {
        sptr2 = sptr; // save current position before entering next level
```

```
        dptr2 = dptr; // save current position before entering next level
        // Check for trigger of TYPE2
        if (TR_TRIG0_TYPE == TYPE2) while(!TR_TRIG0);
        if (TR_TRIG1_TYPE == TYPE2) while(!TR_TRIG1);
        for (i1 = 0; i1 < ICNT1; i1++) {
            sptr1 = sptr; // save current position before entering next level
            dptr1 = dptr; // save current position before entering next level
            // Check for trigger of TYPE3
            if(TR_TRIG0_TYPE == TYPE3) while(!TR_TRIG0);
            if(TR_TRIG1_TYPE == TYPE3) while(!TR_TRIG1);
            for (i0 = 0; i0 < ICNT0; i0++) {
                // BCDMA can combine these in optimized burst aligned accesses.
                *dptr = *sptr;
                sptr = sptr++;
                dptr = dptr++;
            }
        // Update based on saved pointer for this level
        sptr = sptr1 + SDIM1;
        dptr = dptr1 + DDIM1;
        }
    // Update based on saved pointer for this level
    sptr = sptr2 + SDIM2;
    dptr = dptr1 + DDIM2;
    }
```

This form of addressing allows programs to specify regular paths through memory in a small number of parameters. Additionally, it allows for various stall points through the loop to allow for hardware or software induced pausing of the transfer. The following section defines these parameters in detail.

11.1.3.3.3 Transfer Request Formats

The BCDMA defines a four-level loop nest for addressing elements within the TR, using the algorithms described in the Addressing algorithm. Most of the fields in the TR template map directly to the parameters in those algorithms.

Table 11-41. Transfer Request Fields

Field Name	Description	Size
FLAGS	TR flags that specify type of TR and how the TR should be handled. It also supports the TR triggering and output events.	32 bits
ICNT0	Total loop iteration count for level 0 (innermost)	16 bits
ICNT1	Total loop iteration count for level 1	16 bits
ADDR	Starting address for the source data or destination data if it is a half-duplex write.	64 bits
DIM1	Signed dimension for loop level 1 for the source data	32 bits
ICNT2	Total loop iteration count for level 2	16 bits
ICNT3	Total loop iteration count for level 3 (outermost)	16 bits
DIM2	Signed dimension for loop level 2	32 bits
DIM3	Signed dimension for loop level 3	32 bits

Table 11-41. Transfer Request Fields (continued)

Field Name	Description	Size
DDIM1	Signed dimension for loop level 1 for the destination data	32 bits
DADDR	Starting address for the destination of the data	64 bits
DDIM2	Signed dimension for loop level 2 for the destination data	32 bits
DDIM3	Signed dimension for loop level 3 for the destination data	32 bits
DICNT0	Total loop iteration count for level 0 (innermost) used for destination	16 bits
DICNT1	Total loop iteration count for level 1 used for destination	16 bits
DICNT2	Total loop iteration count for level 2used for destination	16 bits
DICNT3	Total loop iteration count for level 3 used for destination	16 bits

The TR assumes all iteration counts as unsigned integers, and all dimensions as signed integers representing byte offsets.

The template above fully specifies the type of elements, length, and dimensions of the transfer.

Since all transfers will not require all the fields the TRs have the type field which allow the number of words required to be sent for the TR to be reduced.

11.1.3.3.4 Flags Field Definition

The next diagram expands the 32-bit FLAGS field. The numbers above each field here indicate bit numbers within the field.

Table 11-42. Transfer Request Template FLAGS Field

<table>
<tr><td colspan="4">31 24</td><td colspan="4">23 16</td></tr>
<tr><td colspan="4">CONFIGURATION SPECIFIC FLAGS</td><td colspan="4">Reserved</td></tr>
<tr><td colspan="4">15 8</td><td colspan="2">7 5</td><td>4</td><td>3 0</td></tr>
<tr><td>TRIGGER_SIZE1</td><td>TRIGGER1</td><td>TRIGGER_SIZE0</td><td>TRIGGER0</td><td>EVENT_SIZE</td><td>WAIT</td><td>STATIC</td><td>TYPE</td></tr>
</table>

The flags field fills in the remaining details about the stream, as follows:

Table 11-43. FLAGS Field Descriptions

Bit	Field	Description
0-3	**TYPE**	The TYPE of TR that is being sent 0: One dimensional data move 1: Two dimensional data move 2: Three dimensional data move 3: Four dimensional data move 4: Four dimensional data move with data formatting 5: Four dimensional Cache Warm 6-7: Reserved 8: Four Dimensional Block Move 9: Four Dimensional Block Move with Repacking 10: Two Dimensional Block Move 11: Two Dimensional Block Move with Repacking 12-14: Reserved 15 Four Dimensional Block Move with Repacking and Indirection
4	Reserved	Reserved for Future use.
5	**WAIT**	This field is only valid on Type 15 TRs. This field indicates whether or not this TR should ensure it completes before allowing the next TR to start on this channel. The encoding is as follows: 0 = Allow next TR to start immediately 1 = Wait for this TR to complete before allowing next TR to start When set, the next TR will not be considered triggered (regardless of any other trigger conditions) until all write status responses for the current TR have landed.

Table 11-43. FLAGS Field Descriptions (continued)

Bit	Field	Description
6-7	**EVENT_SIZE**	This is how often the TR will generate an output event. 0: Event is only generated with the TR is complete 1: Event is generated when the second inner most loop (ICNT1) is decremented by 1. 2: Event is generated when the third inner most loop (ICNT2) is decremented by 1. 3: Event is generated when the outer most loop (ICNT3) is decremented by 1.
8-9	**TRIGGER0**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER0_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel
10-11	**TRIGGER0_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
12-13	**TRIGGER1**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER1_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel This field is reserved for a Direct TR.

Table 11-43. FLAGS Field Descriptions (continued)

Bit	Field	Description
14-15	**TRIGGER1_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
16-23	Reserved	Reserved for Future use.
24-31	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation.

The following sections expand on each of these fields.

11.1.3.3.4.1 Type: TR Type Field

The TR Type field gives the size of the TR and which fields are expected in the TR. Based on the type the number of words required to be sent to complete the TR can be decreased. The tables below show the minimum size for each TR as well if any fields will be treated as reserved.

Table 11-44. Transfer Request Minimum Size Type 0 One Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0	ADDR		RESERVED/NOT REQUIRED											

Table 11-45. Transfer Request Minimum Size Type 1 Two Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	RESERVED/NOT REQUIRED										

Table 11-46. Transfer Request Minimum Size Type 2 Three Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	ICNT2	DIM2	RESERVED/NOT REQUIRED								

Table 11-47. Transfer Request Minimum Size Type 3 Four Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	ICNT2/3	DIM2	DIM3	RESERVED/NOT REQUIRED							

Table 11-48. Transfer Request Minimum Size Type 15 Four Dimensional Block Copy with Repacking and Indirection Support

w0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	ICNT2/3	DIM2	DIM3	RESERVED	DDIM1	DADDR		DDIM2	DDIM3	DICNT 0/1	DICNT 2/3

11.1.3.3.4.2 EVENT_SIZE: Event Generation Definition

The BCDMA allows for an event to be generated at specified intervals for each TR. As the TR passes through the various loops in the addressing algorithm it will generate an event that then can be routed to other event receivers, such as other channels or interrupts to processors.

Table 11-49. Event Size Encoding

Value	Event Type	When it Fires
0	Completion Event	When the TR is complete and all status for the TR has been received.
1	ICNT1 Decrement	Type 0: When the last data transaction is sent for the TR. Type 1-11: When ICNT1 is decremented
2	ICNT2 Decrement	Type 0 – 1,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT2 is decremented
3	ICNT3 Decrement	Type 0 – 2,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT3 is decremented

11.1.3.3.4.3 TRIGGER_INFO: TR Triggers

The TR allows for two different triggers to be set to allow for the data transfer to be prevented or halted through the process of transferring the data. The triggers are specified by selecting a type of trigger and the size of the transfer that can be allowed for the receipt of a given trigger. The triggers themselves in the BCDMA are collected on a per channel basis and for each of three sources. Anytime the trigger event is received the internal counter is incremented. The trigger event will not be cleared until the specified block has started its transfer and it will **only** clear the triggers that are active.

CAUTION

This does allow for one TR in the channel to use global event 0 and the next TR to use global event 1. If while the first TR is running global event 0 can increment and will decrement each time the TR reaches the specified level. At the same time global event 1 will be incremented whenever it is received but it will not decrement until the next TR runs. If the global event 1 counter reaches overflows then an error event will NOT be generated but the event will be lost.

11.1.3.3.4.4 TRIGGERX_TYPE: Trigger Type

The trigger type sets the value of TR_TRIGX as shown in the addressing algorithm description. The TR_TRIGX value allows for the temporary halting of the TR until the expected event has been received. After the given loop has been entered the selected trigger will be decremented.

11.1.3.3.4.5 TRIGGERX: Trigger Selection

The TR is able to select up to 2 of 3 trigger sources for a given TR. The events can come from the dedicated local event on the BCDMA itself or from two assigned global events that come from the PSI-L interface on the BCDMA. The trigger counters are always enabled so that events can be received prior to the TR getting loaded. The trigger counters are only decremented when the trigger is active and the TR has scheduled the first transfer of the transaction.

11.1.3.3.4.6 Configuration Specific Flags Definition

The configuration specific flags are specific to a given TR type. If a TR type does not require additional flags the field should be filled with 0's. Currently only Types 0-4 and Type 15 support the following configuration specific flags:

Bit	Field	Description
0	**ISA**	Indirect Source Address 0: Source address in TR is a directly usable pointer to the data 1: Source address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
1	**IDA**	Indirect Destination Address 0: Destination address in TR is a directly usable pointer to the data 1: Destination address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
2	**SUPR_EVT**	Suppress Event Output: 0 = Output events will be generated according to FLAGS.EVENT_SIZE field 1 = No output events will be generated for the duration of this TR execution This field is only valid on split and type 15 TRs (Type 0-3,15)
3	**Reserved**	Reserved for Future use.

Bit	Field	Description
6:4	**EOL**	This field is only valid on split TRs (Type 0-3). On source (Read) split TRs, this field specifies whether or not the EOL delimiters should be produced on the Tx PSI-L bus. The encodings of this field for source split TRs is as follows: 0 = SOL/EOL match SOP/EOP 1 = SOL/EOL boundaries are each ICNT0 bytes 2 = SOL/EOL boundaries are each ICNT0*ICNT1 bytes 3 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2 bytes 4 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2*ICNT3 bytes On destination (Write) split TRs, this field specifies how to handle EOL delimiters when they are encountered on the Rx (write) side of a TR. EOL delimiters can be produced from the Tx (read) side of a block copy operation or from a remotely paired peripheral when operating in split TR mode. The encodings of this field are as follows: 0: Ignore EOL 1: Line length is icnt0 bytes. Clear any remaining ICNT0 bytes and increment ICNT1 by 1 2: Line length is icnt0*icnt1 bytes. Clear any remaining ICNT0/1 bytes and increment ICNT2 by 1 3: Line length is icnt0*icnt1*icnt2 bytes. Clear any remaining ICNT0/1/2 bytes and increment ICNT3 by 1 4: Line length is icnt0*icnt1*icnt2*icnt3 bytes. Move on to next TR 5-7: RESERVED

Bit	Field	Description
7	**EOP**	This TR should generate an EOP on the streaming interface for any downstream packet oriented consumers to denote that a ‘packet’ of data is complete 0: No EOP flag will accompany the last PSI-L data phase associated with transfers from this TR 1: On egress the DMA will set the EOP flag coincident with transferring the last of the data for this TR. If the TR data does not complete an entire PSI-L data phase then the remaining bytes in the data phase will be skipped and the internal FIFO pointer will be updated to begin packing new data on a new data phase boundary.

11.1.3.3.5 TR Address and Size Attributes

The fields described below all describe the data transfer that needs to be made as described in the Linear Memory Addressing Block Move Algorithm.

11.1.3.3.5.1 ICNT0

The ICNT0 is the number of elements to transfer in the inner loop of the TR. If the TR type does not contain a FMTFLAGS field then this count is assumed to be the number of bytes to transfer. If the FMTFLAGS field is included in the types then the number of bytes to be transferred will be ICNT0 times the Element size rounded up to the nearest byte.

11.1.3.3.5.2 ICNT1

The ICNT1 field is the loop count for the second innermost loop count as defined in the Addressing algorithm.

11.1.3.3.5.3 ADDR

The address location is the initial address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register.

While the ADDR field is 64 bits wide, the usable extent of the address is up to 48 bits of absolute offset plus a 4-bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the ADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved

Bits	Subfield	Description
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.
47:0	Address	The 48-bit source or source starting address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.4 DIM1

This is the offset of the address from the initial address for the first access of the second loop. This will be added to the address from the loop before. This is a signed value so that the address can be both above and below the initial address.

11.1.3.3.5.5 ICNT2

This is the count for the third innermost loop in the addressing algorithm.

11.1.3.3.5.6 ICNT3

This is the count for the outermost loop in the addressing.

11.1.3.3.5.7 DIM2

This is the offset of the address from the initial address to the next address in the third innermost loop. This is a signed value so that the address can be both above and below the previous address.

11.1.3.3.5.8 DIM3

This is the offset of the address from the initial address to the next address in the outermost loop. This is a signed value so that the address can be both above and below the previous address.

11.1.3.3.5.9 DDIM1

This is the offset of the destination address from the initial destination address for the first access of the second loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.10 DADDR

The destination address location is the initial destination address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register

While the DADDR field is 64 bits wide, the usable extent of the address on a KSLC system is up to 48 bits of absolute offset plus a 4 bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the DADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.
47:0	Address	The 48-bit starting destination address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.11 DDIM2

This is the offset of the destination address from the initial destination address for the first access of the third loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.12 DDIM3

This is the offset of the destination address from the initial destination address for the first access of the outer loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.13 DICNT0

This is the number of elements to use in the destination if the TR is repacking the data. This number reflects the number of elements to be transferred.

11.1.3.3.5.14 DICNT1

This is the number of times to execute the second loop to use in the destination transfer.

11.1.3.3.5.15 DICNT2

This is the number of times to execute the third loop to use in the destination transfer.

11.1.3.3.5.16 DICNT3

This is the number of times to execute the fourth loop to use in the destination transfer. The value of DICNT0 x DICNT1 x DICNT2 x DICNT3 must equal ICNT0 x ICNT1 x ICNT2 x ICNT3. If any of the values are zero they are NOT included in the multiplication.

11.1.3.4 Transfer Response Record

Upon completing a TR, the BCDMA will send back a TR Response. The BCDMA TR response format is a single 32 bit word as shown in the Table 11-51 below.

Table 11-50. Transfer Request Response Template STATUS FLAGS Field

31 24	23 16	
CONFIGURATION SPECIFIC STATUS	RESERVED	
15 8	7 7 4	3 0
RESERVED	STATUS_INFO	STATUS_TYPE

Table 11-51. STATUS FLAGS Field Descriptions

Bit	Field	Description
3:0	**STATUS_TYPE**	The completion status of the TR.
7:4	**STATUS_INFO**	Information that is unique based on the STATUS_TYPE returned
15:8	**Reserved**	Reserved for Future use
23:16	**Reserved**	Reserved for Future use
31:24	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation. For BCDMA channels which are capable of interfacing to endpoint peripherals (or via a PDMA) the format of these flags are as follows: 31:28 error_flags – the error_flags field as is provided across PSI-L 27:24 ps_flags – the ps_flags field as is provided across PSI-L

11.1.3.4.1 STATUS Field Definition

The Status field is made up of two sub-fields STATUS_TYPE and STATUS_INFO. A value of 0 means it completed as requested any other value means an error has occurred. The Table below states the legal STATUS_TYPEs and the use of the STATUS_INFO in each case.

11.1.3.4.1.1 STATUS_TYPE Definitions

The STATUS_TYPE field is used to determine what type of status is being returned. Depending on the type of Status it might additionally have information in the STATUS_INFO to give more details about the specific reason why the status was returned.

Table 11-52. STATUS_TYPE Encoded Values

Value	Error Type	Completion	STATUS INFO Definition
0	None	Complete	None
1	Transfer Error	None to Partial	CBA Non-Complete Status Received
2	Aborted Error	None to Partial	None
3	Submission Error	None	Submission Error Type
4	Unsupported Feature	None	Feature Type
5	Transfer Exception	Partial	Exception Type
6	Teardown Flush	None	None
7-15	Reserved	Unknown	Reserved

11.1.3.4.1.1.1 Transfer Error

A transfer error occurs anytime that one of the CBA transactions performed by the BCDMA returns a status other than complete. The BCDMA may continue the transfer or may abort the transfer and return back to an IDLE state. Once the transfer is finished (aborted or complete) the BCDMA will send back the TR Response with the STATUS TYPE of Transfer Error. The STATUS INFO will contain the 3 bit CBA Status field the upper bit specifies if it was a read status (1) or a write status (0).

11.1.3.4.1.1.2 Aborted Error

An aborted error occurs if the PSI-L interface asserts the drop signal prior to the completion of the TR. The BCDMA will return back to an IDLE state and send back the TR Response with the STATUS TYPE. If the BCDMA receives a transfer error after receiving the abort the transfer error should be reported instead of the abort error.

11.1.3.4.1.1.3 Submission Error

A submission error is returned for a TR that is received that cannot be run. The STATUS_INFO field specifies the type of submission errors.

Table 11-53. Submission Error STATUS_INFO Encodings

Value	Submission Error Type
0	ICNT0 was 0
1	Channel FIFO was full when TR received
2	Channel is not owned by the submitter. Either CC submitting to Direct or Direct submitting to a CC channel

Table 11-53. Submission Error STATUS_INFO Encodings (continued)

Value	Submission Error Type
3	Reserved
4	Reserved
5	Bad descriptor type
6-15	Reserved

11.1.3.4.1.1.4 Unsupported Feature

An unsupported feature error is returned for a TR that is received that cannot be run because it specifies a feature that is optional and not supported by the BCDMA that received the TR. The STATUS INFO specifies the feature that was not supported. If it specifies multiple features that were not supported the BCDMA implementation can determine which type it wants to return.

Table 11-54. Unsupported Feature STATUS_INFO Encodings

Value	Submission Error Type
0	TR Type not supported
1	STATIC not supported
2	EOL not supported
3	CONFIGURATION SPECIFIC not supported
4	AMODE not supported
5	ELTYPE not supported
6	DFMT not supported
7	SECTR not supported
8	AMODE SPECIFIC Field not supported
9-15	Reserved

11.1.3.4.1.1.5 Transfer Exception

A transfer exception is returned for a TR that completed but experienced a known exception during reception. The STATUS_INFO field specifies the type of transfer exception that was encountered.

Table 11-55. Transfer Exception STATUS_INFO Encodings

Value	Transfer Exception Type
0	EOP on incoming data stream was encountered prematurely (short packet)
1	EOP on incoming data stream was encountered late (long packet)
2-15	Reserved

11.1.3.4.1.1.6 Teardown Flush

Split mode BCDMA Rx channels (write channels) can respond with a teardown flush in the case that they have received a teardown message, all data has been transferred , and TRs have been prefetched (in anticipation of more data being received). In this case, the BCDMA will simply return the prefetched TR to the completion queue with the status type set to teardown flush.

11.1.3.5 Channels

Each DMA controller instance contains one or more channels. A channel represents a single thread of strongly ordered operations whose purpose is to move data from one interface to another. Operations between channels are orthogonal and have no assumption of ordering but operations within a channel must be completed in order. The DMA controller uses time division multiplexing to allow work from channels to momentarily use shared data transfer units and data paths.

11.1.3.6 Flows

Each DMA channel will provide one or more flows which allow communication with one or more SW hosts. Each flow contains a single queue pair implemented within a shared circular buffer (ring) in memory. One queue provides uni-directional communication from SW to the DMA while the other queue provides uni-directional communication from the DMA back to SW. Flows are intended to allow traffic which is produced or consumed by a different Host SW process or traffic which is on different priorities to share a single physical DMA channel. A DMA channel will perform time division multiplexing between flows on specific work boundaries. Once a channel is in work on a specific flow, that entire unit of work will be completed before allowing work from a different flow to begin.

11.1.3.7 Queues

Queues are used to hold either values or references that need to be passed between SW and HW components in the system. Queues are implemented in the PKTDMA and BCDMA modules using memory mapped rings. Each ring is comprised of a single contiguous memory block which contains an array of elements. Each element is 8 bytes. The size of the ring is selectable from 1 entry up to 64K entries with single entry granularity. Each ring is used to implement a forward and a reverse queue which share the same data elements but which have independent pointers and occupancies. The forward queue is used to pass work from SW to HW and the reverse queue is used to pass completed work back from HW to SW. A doorbell MMR is provided per ring to allow SW to add elements to the forward queue. A separate doorbell MMR is provided per ring to allow SW to acknowledge the popping of elements from the reverse queue. An occupancy MMR is provided for the reverse queue so that SW can know how many entries are currently completed. Entries are returned on the reverse queue in the exact same order and in the exact same index as the work was provided on the forward queue and because of this, the DMA controllers do not actually modify the ring entry for completion operations (the only exception being for acknowledgement of a teardown operation). Completion is indicated by incrementing of the reverse occupancy only.

11.1.3.7.1 Queue Types

11.1.3.7.1.1 Transmit Queues

Tx channels use packet queues referred to as “transmit queues” to store the packets that are waiting to be transmitted. Tx Queues only pass a pointer to a descriptor. For the PKTDMA, Tx Queues contain pointers to Host descriptors. For the BCDMA, pass Tx Queues contain a pointer to a TR packet descriptor. Transmit Queues are implemented as the forward queue on the shared ring structure for a Tx flow.

11.1.3.7.1.2 Transmit Completion Queues

Tx channels also use packet queues referred to as “transmit completion queues” to return packets to the host after they are transmitted. A Tx Completion Queue is provided for each Tx Queue. The DMA controllers do not actually write anything back to completion queues (except for a teardown acknowledgement) but instead just increment the reverse occupancy. Transmit completion queues are implemented as the reverse queue on the shared ring structure for a Tx flow.

11.1.3.7.1.3 Free Descriptor / Buffer Queues

Free descriptor/buffer queues pass an empty list of pre-chained descriptors, each pointing to a single buffer, from SW to the DMA to use for receiving incoming packets. Free Descriptor/Buffer Queues are implemented as the forward queue on the shared ring structure for an Rx flow.

11.1.3.7.1.4 Receive Queues

Rx queues pass a packet which has been received from the DMA back to the SW. Receive queues are implemented as the reverse queue on the shared ring structure for an Rx flow.

11.1.3.7.1.5 Ring Based Queues Implementation

Work packets which are stored in a queue are shown in the following diagram:

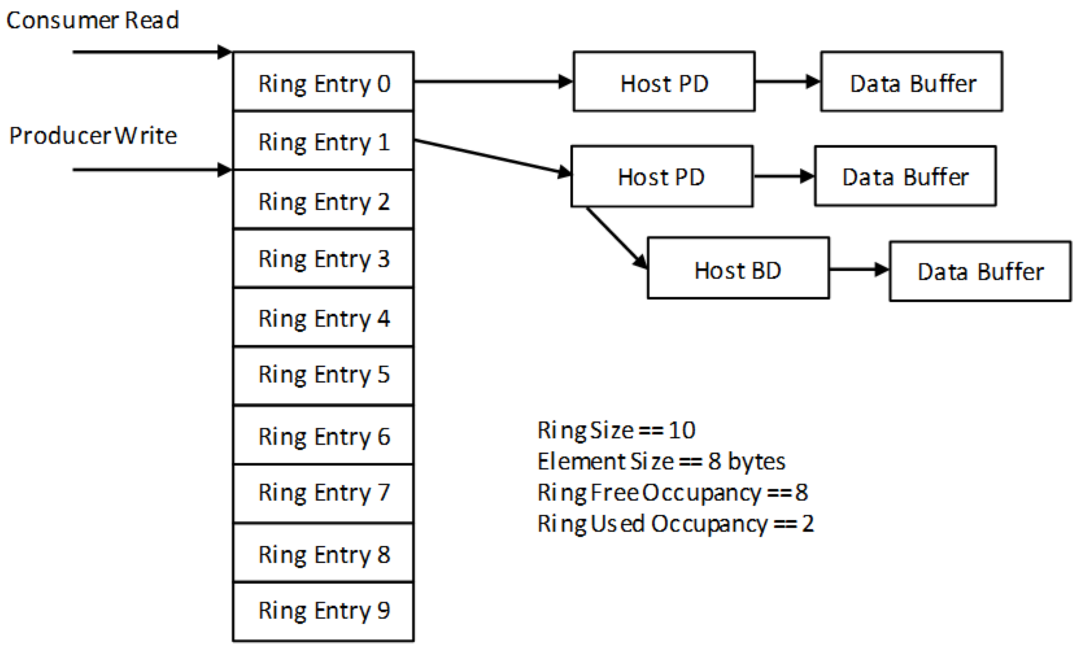

Figure 11-3. Ring Based Queue Structure

11.1.4 Operational Description

11.1.4.1 Resource Allocation

Rings, memory, interrupts, DMA channels, and flow table entries are shared resources within the data movement architecture and their ownership and use must be managed in order to provide stable, safe, and secure operation. The DMSS provides channelized firewalls which can be used to protect arrayed resources (like rings, channel control MMRs, etc.) from unwanted/unauthorized use as well as restricted access to the firewall configurations themselves. It is outside the scope of this document to define how the resource management system functions but it is assumed that all of these resources are isolate-able and secure-able.

11.1.4.2 PKTDMA/BCDMA - Ring Operation

11.1.4.2.1 Queue Initialization

The base address and size for each ring must be initialized via the provided MMRs prior to using the ring. Ring initialization is typically done only on channel / flow setup as once initialized the rings can be used indefinitely.

11.1.4.2.2 Queueing Entries

Entries can only be queued by SW onto the forward queue of a ring. To queue an entry the producer will write the entry contents (typically a pointer to the Packet Descriptor or a TR) to the memory location pointed to by the current write pointer and will decrement its internally maintained free entry occupancy. After the producer has confirmed that the data has actually landed it memory, it will then write to the forward doorbell register (RINGRT[a]_RT_FDB) for the ring to increment the pending forward occupancy count for the ring.

More than one entry can be queued with a single doorbell write as the entry count in the doorbell write indicates how many entries have been queued.

11.1.4.2.3 De-queueing Entries

Entries can only be de-queued by SW from the reverse queue of a ring. The consumer (entity which is going to de-queue an entry from the ring) maintains a current read pointer for each ring it controls. To de-queue an entry the consumer will read the occupancy from the reverse occupancy register (RINGRT[a]_RT_ROCC) and will then read the entry contents from the memory location pointed to by the current read pointer. The consumer will then write a decrement value to the reverse doorbell register (RINGRT[a]_RT_ROCC) for the ring to decrement the waiting occupancy count for the reverse queue within the ring and will increment its internally maintained free entry occupancy for the ring.

11.1.4.3 PKTDMA/BCDMA - Output Event Generation

Each channel and flow within a DMA has the ability to generate specific types of events which can be routed to the IA in the system and from there re-routed to any event consumer. Events are output from the DMA controllers using a simple integer encoding. Up to 4 events can be generated from any given channel but only event types which have functional value are supported on each specific type of channel. The DMA channel event types are listed as follows:

Table 11-56. Per-Channel/Flow Event Support and Encoding

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
Ring Entry Zero/Non-zero	Asserts an up event anytime the ring transitions to a non-zero occupancy / teardown state. Asserts a down event anytime the ring transitions to a zero occupancy / teardown state.	Flow	X	X	X	X	X
Channel Error	Asserts an up event anytime an error occurs on the channel. Asserts a down event when the channel error bit is cleared.	Channel	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only

Table 11-56. Per-Channel/Flow Event Support and Encoding (continued)

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
Rx Starvation	Asserts an up event when starvation occurs on a flow. Asserts a down event when entries are added to the ring for that flow.	Flow					First flow in channel only
RX Flow FW Error	Asserts an up event when a flow id arrives on the RX interface that is not between the flowid_start and flowid end values for the channel. Asserts a down event when the RX Flow ID Firewall Status Register pend bit is cleared	Pktdma					X
Data Events	Asserts an up event when the selected loop counter has decremented. If the suppress event bit is not set in the TR	Channel	X	X	X		

Each BCDMA/PKTDMA instance will provide an event transport-lane (ETL) interface to pass outgoing events. The index field on this ETL will be calculated based on the event type and channel or flow offset. Each PKTDMA or BCDMA instance is configured with base values to which a channel or flow index is added for each type of event which can be generated. These base index values are listed in the specification for that specific instantiation of each DMA and are named as follows:

Table 11-57. BCDMA/PKTDMA Event Base Index Parameters

DMA	Event Base Parameter Name	Function	Offset
PKTDMA	tcomp_evtbase	Base index for Tx flow reverse ring completion events	Tx flow number

Table 11-57. BCDMA/PKTDMA Event Base Index Parameters (continued)

DMA	Event Base Parameter Name	Function	Offset
	rcomp_evtbase	Base index for Rx flow reverse ring completion events	Rx flow number
	terr_evtbase	Base index for Tx channel error events	Tx channel number
	rerr_evtbase	Base index for Rx channel error events	Rx channel number
	rstarve_evtbase	Base index for Rx flow starvation events	Rx flow number
	rflowfw_evtbase	Base index for Rx Flow Firewall event	None
BCDMA	tcomp_evtbase	Base index for split Tx flow reverse ring completion events	Tx flow number
	rcomp_evtbase	Base index for split Rx flow reverse ring completion events	Rx flow number
	bcomp_evtbase	Base index for normal Block Copy flow reverse ring completion events	BC flow number
	terr_evtbase	Base index for split Tx channel error events	Tx channel number
	rerr_evtbase	Base index for split Rx channel error events	Rx channel number
	berr_evtbase	Base index for normal Block Copy channel error events	BC channel number
	tdcomp_evtbase	Base index for Tx channel TR data completion events	Tx channel number
	rdcomp_evtbase	Base index for Rx channel TR data completion events	Tx channel number
	bdcomp_evtbase	Base index for Block Copy channel TR data completion events	BC channel number

Example:

The producer event map is set up so that the Tx flows from a PKTDMA instance are to start at 64 and proceed upward from there. The tcomp_evtbase for that PKTDMA instance is set to 64. In this configuration, the reverse ring entry completion event for flow 0 will produce an event on index 64, flow 1 will produce an event on index 65, etc. The terr_evtbase for the same PKTDMA instance is set to 128. In this configuration, error events for channel 2 would produce events with an index of 130.

11.1.4.4 PKTDMA - Transmit Channel Setup

This section describes the setup procedure for Tx channels within the PKTDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHAN[a]_TCFG). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (TCHAN[a]_TCFG) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.5 PKTDMA - Transmit Channel Pause

Setting the tx_pause bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL > [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.6 PKTDMA - Transmit Channel Teardown

This section describes the teardown procedure for internal Tx channels within the PKTDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL > [30] TX_TEARDOWN).

Once the host has written the tx_teardown bit, the PKTDMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed.
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues an Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host can determine that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.7 PKTDMA - Transmit Operation

After a channel has been set up it can begin to be used to transmit packets. Packet transmission involves the following steps:

1. The Host is made aware of one or more chunks of data in memory that need to be transmitted as a packet. This may involve directly sourcing data from the Host or it may involve data which has been forwarded from another data source in the system.
2. The Host allocates and populates a host packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to Host).
    b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.
    c. Source Tag.
    d. Destination Tag.
    e. Packet Type.
    f. Any protocol specific flags for the given packet type.
    g. Buffer Pointer with the byte aligned address of the first chunk of buffer data.
    h. Buffer Length with the number of bytes in the first chunk of buffer data.
    i. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.
    j. Any protocol specific descriptor sections that are required for the given packet type or system configuration.
3. The Host allocates and populates host buffer descriptors as necessary to point to any remaining chunks of data that belong to this packet. The host will initialize the following fields within the host buffer descriptor:
    a. Buffer Pointer with the byte aligned address of the given chunk of buffer data.
    b. Buffer Length with the number of bytes in the given chunk of buffer data.
    c. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.
4. The Host writes queues the packet onto one of the Transmit Queues for the desired DMA channel. Channels may provide more than one Tx Queue (if more than 1 flow is provided) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
5. The PKTDMA internally generates a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
6. The PKTDMA Tx engine is eventually brought into context for the corresponding channel and begins to process the packet.
7. The PKTDMA reads the packet descriptor pointer from the memory mapped ring for that channel/flow.
8. The PKTDMA reads the packet descriptor from memory.
9. The PKTDMA empties each buffer in sequence by transmitting the contents in one or more block data moves. The size of these blocks is application specific. The PKTDMA module specification is intended to document the block size used by a given implementation. As each buffer is emptied, the PKTDMA will read the next buffer descriptor to obtain the pointer and size of the data buffer as well as the pointer to the next descriptor in the chain.
10. When all data for the packet has been transmitted as specified in the packet size field, the DMA will increment the occupancy of the reverse queue (Tx Completion Queue).
11. After the occupancy is incremented, the PKTDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the PKTDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.

15. The PKTDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line.

11.1.4.8 PKTDMA - Receive Free Descriptor / Buffer Queue Setup

The Host is ultimately responsible for providing all of the free descriptors and buffers that the port uses as it receives packets. Each entry on the Rx Free Descriptor/Buffer Queue consists of one or more descriptors chained together with each descriptor also pointing to a single contiguous buffer. Each entry on the Rx Free Descriptor/Buffer queue is intended to receive one packet of data. All chaining of descriptors within a packet is performed prior to placing the Rx resources onto the free queues.

Before the Host adds each Rx buffer descriptor chain to the queue, it must first initialize the Rx buffer descriptor values as follows:

- Write the Buffer Pointer with the byte aligned address of the buffer data
- Write the Buffer Size
- Write the next descriptor pointer to the next descriptor in the chain (non-eop) or to 0x0 (eop)

All other fields in the Descriptor do not need to be initialized as they will be overwritten by the Port on reception.

11.1.4.9 PKTDMA - Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel's Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<RCHANRT[a]_RRT_CTL> [31] RX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.10 PKTDMA - Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread). Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register 0x408 . This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the PKTDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL> [30] RX_TEARDOWN).

Once a teardown has been initiated, the PKTDMA will do the following:

1. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
2. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL> [31] RX_ENABLE)**>**.
3. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
4. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register to indicate that a teardown has completed (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE).
5. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
6. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the PKTDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.11 PKTDMA - Receive Channel Pause

Setting the rx_pause bit in the Rx Channel N Control Register (<RCHANRT[a]_TRT_CTL> [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.12 PKTDMA - Receive Operation

When packet reception begins on a given channel, the port will begin by fetching the descriptor and buffer from the ring for the channel / flow. If the SOP Buffer Offset in the Rx Flow Table entry is nonzero, then the port will begin writing data after the offset number of bytes in the SOP buffer. The port will then continue filling that buffer and will fill additional descriptors + buffers as needed using the pre-linked buffers in the packet.

A detailed summary is as follows:

1. Host allocates, populates, and places pointers to free descriptor/buffer structures onto Rx Free Descriptor/Buffer Queues
2. PKTDMA fetches packet descriptor pointer from forward queue of ring for specified channel.
3. PKTDMA reads the packet descriptor to obtain the packet info, buffer pointer, buffer size, and next descriptor pointer.
4. PKTDMA fills the buffer with received data

If packet is not complete and the rx_chan_type field in the Rx Channel Configuration Register (<RCHAN[a]_RCFG> [19:16] RX_CHAN_TYPE) is set to 2 (Normal Rx Host Mode). The machine will proceed to step 5 and will repeat steps 5-6 until all packet data is received at which point the Rx engine proceeds to step 8. If the rx_desc_type is set to 3 (Single Buffer Packet Host Mode) the Rx engine will proceed directly to step 7 regardless of whether or not an end of packet terminator has been reached on the incoming data stream. The current packet will be completed following the sequence through step 12 and a new packet will be started back at step 1.

5. PKTDMA fetches next buffer descriptor using next descriptor pointer obtained from previous descriptor.

6. PKTDMA fills the buffer with received data.

The PKTDMA performs the following operations when the entire packet has been received:

7. PKTDMA writes the packet descriptor to memory. This includes the following fields:

a. Descriptor Type (set to Host)

b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.

c. Source Tag

d. Destination Tag

e. Packet Type

f. Any protocol specific flags for the given packet type

g. Any protocol specific words that are required for the given packet type

h. Extended Packet Information (optional)

8. PKTDMA increments the occupancy of the reverse queue for the channel / flow.

9. Once the occupancy is incremented it will send an up event to the Interrupt Aggregator

10. The Interrupt Aggregator upon receiving the up event will set the appropriate bit in the Interrupt Status Register (VINT[a]_STATUS_SET) indicated by the interrupt mapping table which will cause an interrupt to be asserted to the Host

11.The Host will pop the packet pointer from the Rx Queue by reading the ring contents and then pushing a decrement to the reverse occupancy for the ring.

12. If the pop causes the queue to become empty, the PKTDMA will send a down event to the Interrupt Aggregator thus causing the associated bit to be cleared and also potentially clearing the interrupt to the Host.

11.1.4.13 BCDMA - Block Copy Channel Setup

This section describes the setup procedure for channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Port DMA State. The host initializes the channel Port DMA State by initializing all of the channel flow entries and then writing to the Block Copy Channel Configuration Register A (BCHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Block Copy Channel Configuration Register A (<BCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a channel has been set up, packets can be added to the Queues for the channel to begin the copy operation.

For general purpose block copy channels, only the Block Copy DMA configuration, flow, and real-time registers will be present. For split mode channels, separate Tx and Rx configuration, flow, and real-time registers are provided. In all cases, configuration of all fields must be completed before a channel is enabled.

11.1.4.14 BCDMA - Block Copy Channel Pause

Setting the pause bit in the Channel N Control Register (<BCHANRT[a]_TRT_CTL> [29] TX_PAUSE]) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.15 BCDMA - Block Copy Channel Teardown

This section describes the teardown procedure for generic block copy channels within the BCDMA. A channel teardown is initiated by the host by writing the teardown bit in the Channel N Real-time Control Register (<BCHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the forced_teardown bit in the Channel N Real-time Control Register (<BCHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN).

If the forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/data fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Channel N Global Configuration Register (<BCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the BC Flow Reverse Ring Occupancy register to indicate that a teardown has completed.
7. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current BC Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.

9. If the forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:
   a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
   b. Completes any packets which have been fetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).
   c. Clears the channel enable in the Channel Global Configuration Register.
   d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
   e. Sets bit 31 of the BC Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
   f. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

   The host may issue a teardown on any channel at any time, regardless of whether the channel is actively transferring data or not.

   The Host determines that a teardown using either of the following methods:

   a. Periodically polling the teardown and enable bits for the channel
   b. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

   Note that the teardown message will actually be written to the next available location in the ring following the last completed packet.

11.1.4.16 BCDMA - Block Copy Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a type 15 TR packet descriptor. The host will initialize the following fields within the packet descriptor:
   a. Descriptor Type (set to TR)
   b. Reload Enable to 1 if looping is required, otherwise 0
   c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
   d. Last Entry to TR count minus 1
   e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
   f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Block Copy Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/ scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.

8. All of the data transfers specified in a TR will be completed as a series of reads followed later on by a set of corresponding writes (which may or may not be the same size based on the parameters in the block copy TR).
9. The BCDMA will wait until write status returns for the final write operation that was initiated for each TR. When the final write status is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel/flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line

11.1.4.17 BCDMA - Block Copy Error/Exception Handling

There are 3 specific errors which may be encountered during generic block copy operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-58. BCDMA Generic Block Copy Mode Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable(1)	Yes	No	Just that TR	No
Unsupported TR Type	Selectable(1)	Yes	No	Just that TR	No
Bus Errors	Selectable(1)	Yes	Yes	No	Yes

(1) If pause_on_error bit is set in channel configuration

11.1.4.17.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Block Copy engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Block Copy engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.18 BCDMA - Split Transmit Channel Setup

This section describes the setup procedure for split Tx channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.19 BCDMA - Split Transmit Operation Pause

Setting the pause bit in the Channel N Control Register (<TCHANRT[a]_TRT_CTL> [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.20 BCDMA - Split Transmit Channel Teardown

This section describes the teardown procedure for split mode Tx channels within the BCDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the tx_forced_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN) .

If the tx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the DMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. If the tx_forced_teardown bit is set (only valid on BCDMA), a destructive teardown has been initiated. In this case, the BCDMA will do the following:

1. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
2. Completes any packets which have been prefetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).

3. Clears the channel enable in the Tx Channel Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel’s default flow (first flow in channel) reverse occupancy register (RINGRT[a]_RT_ROCC) for the channel.

11.1.4.21 BCDMA - Split Transmit Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Transmit Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/ scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.
8. All of the data transfers specified in a TR will be completed as a series of reads.
9. The BCDMA will wait until data returns for each read operation that has been initiated. When the final read operation is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel / flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.

12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_ENABLE_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line.

11.1.4.22 BCDMA - Split Transmit Error / Exception Handling

There are 3 specific errors which may be encountered during Tx split operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-59. BCDMA Tx Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable(1)	Yes	No	Just that TR	No
Unsupported TR Type	Selectable(1)	Yes	No	Just that TR	No
Bus Errors	Selectable(1)	Yes	Yes	No	Yes

(1) If pause_on_error bit is set in channel configuration

11.1.4.22.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Block Copy engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Block Copy engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.23 BCDMA - Split Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel's Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.24 BCDMA - Split Receive Channel Pause

Setting the pause bit in the Channel N Control Register (<RCHANRT[a]_RRT_CTL > [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.25 BCDMA - Split Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread). Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register 0x408 . This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the BCDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL > [30] RX_TEARDOWN).

Upon seeing the rx_teardown bit asserted the port can perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the rx_forced_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL > [28] RX_FORCED_TEARDOWN).

If the rx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional prefetches for the channel (TR mode channels)
2. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
3. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
7. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
8. If the rx_forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:

    a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
    b. Completes any packets which may be pending in the ingress port buffers with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation) . Packets will be drained from the Rx FIFO either using ‘null’ write transfers or real transfers and the Packet Descriptors will be returned with an accurate accounting of actual bytes transferred.
    c. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).
    d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
    e. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
    f. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the BCDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.26 BCDMA - Split Receive Operation (TR Packet)

Packet reception in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Rx TR Queues for the desired BCDMA channel. Channels may provide more than one Rx TR Queue (one per flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
3. The Ring Accelerator provides a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves.
8. All of the data transfers specified in a TR will be completed as a series of writes and a Transfer Response will be returned indicating the completion and status of the transfer.
9. The BCDMA will wait until Transfer Responses have been returned for each Transfer Request that it issued. As each Transfer Response is returned, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the DMSS will write the pointer to the packet descriptor to the queue specified in the return queue number fields of the packet descriptor.
11. After the Packet Descriptor pointer has been written, the Ring Accelerator indicates the status of the Rx Completion Queues to other ports / processors / prefetcher blocks using events sent to the Interrupt Aggregator. These events are then converted into standard interrupts.

11.1.4.27 BCDMA - Split Receive Error / Exception Handling

Several types of errors/exceptions may be encountered during reception of split Rx data. The following table outlines the various errors and exceptions that can occur:

Table 11-60. Rx Error / Exception Handling

Condition	Channel Type	Severity	Pauses Channel	Error Flag Set	Data Transfer	Data Flush	TR Flush	Event Output
Descriptor Starvation	All Packet	Exception	No	No	Option	Option	-	No
Protocol Errors	All Packet	Info	No	No	Normal	No	-	No
Drop	Host – normal	Exception	No	No	Partial(1)	Until EOP	-	No
EOP Asserted Late (Long Packet)	BCDMA – single ended	Exception	No	No	Partial	Excess	No	Yes
TR null icnt0	All BCDMA	Error	Selectable(1)	Yes	No	No	Just that TR	No
Unsupported TR Type	All BCDMA	Error	Selectable(1)	Yes	No	No	Just that TR	No

(1) Data will not be transferred after drop is detected. All data after that point is guaranteed to be flushed and some data prior to the exact data phase on PSI-L where drop was asserted may also be flushed since data is constantly accumulated so it can be transferred in chunks.

11.1.4.27.1 PKTDMA Exception Conditions

There are a few cases which can occur when processing incoming packets which are not considered errors but which will require handling in order to avoid locking up the PKTDMA engines.

Packet mode channel exceptions include:

- Descriptor Starvation
- Protocol Errors
- Dropped Packets
- Long Packets

11.1.4.27.1.1 Descriptor Starvation

Descriptor starvation occurs when the Port needs to fetch a free descriptor from the RX ring and none are available. When the port detects that descriptor starvation has occurred it will react based on the value of the rx_error_handling bit which was programmed into the Rx Flow N Configuration Register A (<RFLOW[a]_RFA> [28] RX_ERROR_HANDLING).

If the rx_error_handling bit is cleared:

- The Port will increment an internal per-channel starvation counter and will then flush the packet.

If the rx_error_handling bit is set:

- The Port will assert a RX descriptor starvation event (which may cause an interrupt to the Host) and will then wait for the doorbell for the selected flow to be written with a positive value. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that when in this mode, if data loss is not desired that the host will guarantee that a chain of buffers will be provided that can receive the entire packet.

11.1.4.27.1.2 Protocol Errors

Protocol errors occur when the port logic detects that the received packet did not pass protocol specific criteria that was checked during reception of the packet. Examples of protocol errors include packet length errors, CRC errors, or alignment errors.

When protocol errors are detected, the port may choose whether or not it will drop the packet. The mechanism that is used to determine which packets to drop and which to forward is application specific. If the port determines that it needs to forward the packet to the Host, it will set the Packet Error bit in the Descriptor indicating that this is a packet which experienced a protocol related error. The type of protocol related error is generally indicated in either the Protocol Specific bits in the Host descriptor or in the Protocol Specific bytes region. The packet length information and certain portions of the Protocol Specific region may not be correct for packets which encounter errors.

11.1.4.27.1.3 Dropped Packets

Packets can be dropped within an Rx Port for any number for reasons which with the exception of the starvation case which was covered above are application specific.

When a Port determines that it needs to drop a packet after reception of the packet has begun, it must flush the remainder of the packet, increment the dropped packets statistic, and rewind any fetched descriptor/buffer chain so that the it can be use the same descriptor/buffer chain on the next packet.

11.1.4.27.1.4 Long Packet

For Rx channels which are not configured in single buffer mode, if the host provides a buffer chain whose total length is insufficient to receive the entire packet, whatever portion of the packet which has not been received will be flushed until an end of packet indicator is received on the PSI-L interface. This behavior will occur regardless of which error handling mode has been selected for the channel.

11.1.4.27.2 BCDMA Exception Conditions

Since the TR mode engine performs transfer sequencing using a count based mechanism it is susceptible to becoming out of synchronization if the source of the data and the destination for the data do not exactly match in their expectations for how much data will be transferred. The following sections outline these scenarios.

TR mode channel exceptions include:

- Reception of EOL delimiter
- Short Packets
- Long Packets
- Descriptor Starvation

11.1.4.27.2.1 Reception of EOL Delimiter

If an end of line delimiter is received by the Rx (write) side of the BCDMA the EOL_ADV field in the TR application specific flags field is used to advance the appropriate indices of the TR to the next level. Each EOL that is received will cause the TR to advance to the next specified loop iteration breaking as many intermediate loops as are required.

11.1.4.27.2.2 EOP Asserted Prematurely (Short Packet)

Split TR mode channels can experience an incoming packet whose length is shorter than what was expected based on one or more TRs which form the control description for the expected packet. If an EOP is received for a TR and the TR has not been completely executed, the port is required to receive as much data as is actually provided in the incoming data placing it in accordance with the instructions in the TR and the to continue executing any remaining TR(s) such that the required events are produced to keep downstream consumers in sync. In this case, no data will be transferred to the buffers described by the TR beyond what was provided in the incoming packet.

11.1.4.27.2.3 EOP Asserted Late (Long Packets)

Split TR mode channels can experience an incoming packet whose length is longer than what was expected based on one or more TRs which form the control description for the expected packet. If a TR completes and is marked as EOP but the incoming packet is not finished, then the port must throw away any additional received data until the incoming packet reaches an EOP condition. At this point, reception will start with a new TR and a new incoming packet.

11.1.4.27.2.4 Descriptor Starvation

Descriptor starvation occurs when the Port receives enough data for a burst but the ring for the channel is currently empty. This causes push back on the receive port and can cause lost data.

The Port will assert a starvation bit in the RX Receive Channel Status register (RCHANRT[a]_RRT_STATUS[1-0]). When the doorbell register (RINGRT[a]_RT_DB) is written to populate the ring the starvation bit will clear. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that if data loss is not desired that the host will guarantee that a descriptor is present.

11.2 Data Movement Subsystem (DMSS)

This chapter describes the Data Movement Subsystem (DMSS) module in the device.

11.2.1 Data Movement Subsystem (DMSS)

This chapter describes the features and functions of the Data Movement Subsystem (DMSS) hardware modules in the device.

11.2.1.1 DMSS Overview

The DMSS module on provides data movement (DMA) and bridges between the CBA switched interconnect and the packet streaming fabric (network on chip) on the device.

The Data Movement Subsystem (DMSS) consists of DMA/Queue Management components and Peripherals:

- Packet DMA
- Block Copy DMA
- Ring Accelerator
- Packet Streaming Interface (PSILSS)
- Infrastructure components such as CBASS, secure proxy, and an interrupt aggregator

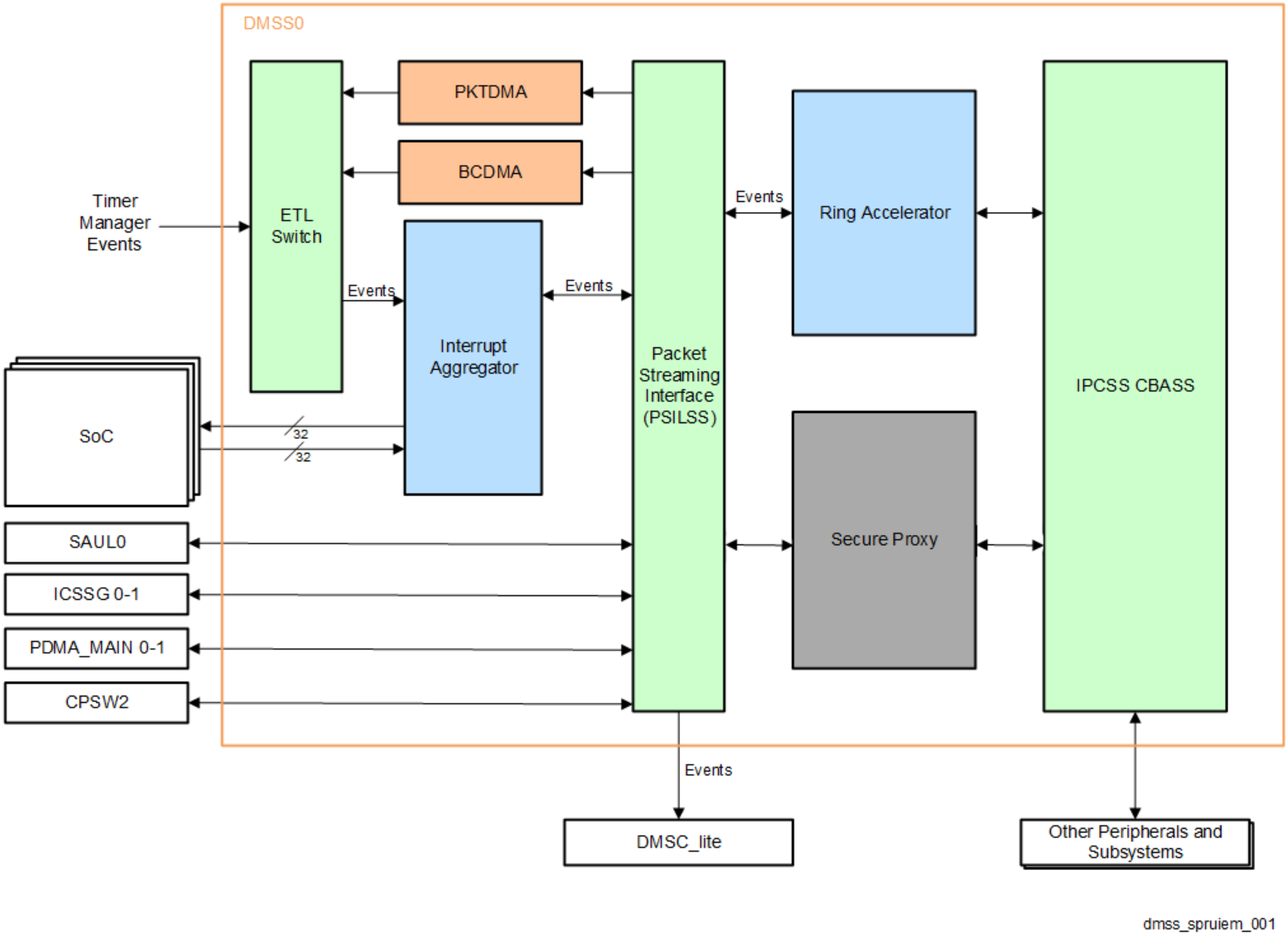

Figure 11-4. DMSS Top-Level Block Diagram

Table 11-61. DMSS Allocation Within Device Domain

Module Instance	Domain	
	MCU	MAIN
DMSS0	-	✓(DMSS)

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

11.2.1.2 DMSS Functional Description

See Section Chapter 11 , DMSS Architecture, for the TI Data Movement Architecture (DMA) specification.

See the following sections for the respective module description:

- PKTDMA - Section 11.1.1.4
- BCDMA - Section 11.1.1.5
- Ring Accelerator:
  - See Section 11.1.1.1 for a summary overview of the Ring accelerator.
  - SeeSection 11.2.2 for a full chapter breakdown of the Ring accelerator.
  - See Section 11.2.2.1 for a block diagram overview.
  - See Section 11.2.2.1.1 for a list of features.
  - See Section 11.2.2.2 for a functional description of the Ring Accelerator.
- Infrastructure Components:
  - CBASS - Chapter 3
  - Secure Proxy:
    - See Section 11.1.1.2 for a summary overview of the Secure Proxy.
    - See Section 11.2.3 for a full chapter breakdown of the Secure Proxy.
    - SeeSection 11.2.3.1.1 for a list of features.
    - See Section 11.2.3.2 for a functional description of the Secure Proxy.
  - Interrupt Aggregator
    - See Section 11.1.1.3 for a summary overview of the Interrupt Aggregator.
    - See Section 11.2.4 for a full chapter breakdown of the Interrupt Aggregator.
    - SeeSection 11.2.4.1.1 for a list of features.
    - See Section 11.2.4.2 for a functional description of the Interrupt Aggregator.

11.2.1.3 DMSS Interrupt Configuration

This section describes the actions needed to configure interrupts within the DMSS.

Table 11-62. DMSS Parameters

Parameter	Value DMSS	Description
RA_RING_CNT	20	Number of total rings supported (specific to each ring accelerator)
IA_SEVI	1536	Interrupt Aggregator Source Event Input (SEVI) count (specific to each interrupt aggregator)
IS_VINTR	184	Interrupt Aggregator Virtual Interrupt (VINTR) count (specific to each interrupt aggregator)

Table 11-62. DMSS Parameters (continued)

Parameter	Value DMSS	Description
EO	See *Global Event Map* in Module Integration	Event offset

DMSS Software Variables lists software-configurable variables used in the examples and descriptions.

Table 11-63. DMSS Software Variables

Variable	Valid Range	Description
R#	0 to RA_RING_CNT-1	Ring number
E#	0 to (destination module specific)	Event number
GE#	= EO + E#	Global event number
SB#	0 to IA_SEVI-1	Interrupt aggregator status bit number
VI#	0 to IA_VINTR-1	Virtual interrupt number

11.2.1.3.1 DMSS Event and Interrupt Flow

DMSS Interrupt Flow illustrates the event and interrupt flow within the DMSS and output interrupts to a CPU.

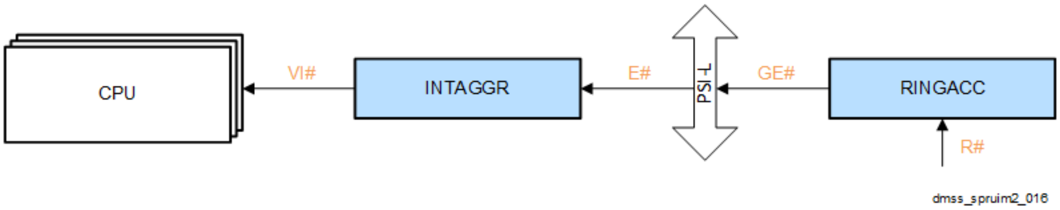

Figure 11-5. DMSS Interrupt Flow

11.2.1.3.1.1 DMSS Interrupt Description

This section describes the interrupt-related information that flows within DMSS and how this information is configured or generated.

1. **Ring Number (R#):**
   - Data is read from and written to a specific Ring Accelerator ring using direct ring-mode, or secure proxy access
   - The Ring Accelerator has specific ring number ranges for specific purposes. The R# must match the intended purpose of the ring (see Table 10-578, RINGACC Ring Mapping)
2. **Global Event and Event Numbers (GE# and E#):**
   - GE# = EO + E#
   - EO determines the destination module for the event. The PSILSS will route the GE# to the destination module per the DMSS event mapping, removing EO in the process. The destination module sees only E#. See *Global Event Map* in *Module Integration* for details.
   - For the INTAGGR module, E# ranges from 0 to (IA_SEVI - 1)
3. **Virtual Interrupt (VI#)**
   - The INTAGGR maps E# (via software configuration) to any SB#
   - ranges from 0 to (IA_SEVI - 1)
   - Each VI# (0 – (IA_VINTR-1)) is driven by a group of 64 contiguous SB# numbers (VI# driven by SB#'s VI#×64 – (VI#×64)+63)

11.2.1.3.1.2 DMSS Event Description

1. Interrupt aggregator includes three orthogonal functions:

    a. Event mapping block which converts local/umapped events to global events, and sends those events out.
    b. Aggregating global events and convert them into interrupt outputs.
    c. L2G block: This is a block to convert the event/interrupt from SoC level into global events. L2G block takes wired signal from SoC (interrupt signal or DMA signal) converted into local events.

2. L2G Block: This block converts the event/interrupt from SoC level into global events. L2G block takes wired signal from SoC (interrupt signal or DMA signal) converted into local events. Those local events are sent to ETL and sent to event mapping logic inside interrupt aggregator to convert them into global event. And then those global events are sent out again.
3. PSIL and ETL: PSIL is a streaming protocol which carries both data information and event information. ETL is the PSIL portion which only carries event. PSIL data is transported independently. When you see PSIL, it must include ETL.
4. Local events and unmapped events are in the same category. All those unmapped/local events are routed to the mapping block inside Interrupt aggregator to be converted into global events
5. Other than L2G block, Currently there are only three components generating unmapped events: BCDMA, PktDMA and timer manager. All those unmapped events are routed to the event mapping block inside interrupt aggregator first. All the other components produce global events.
6. After the local/unmapped events are mapped to global events in interrupt aggregator, those global events are sent out by interrupt aggregator and can be transported to different locations (for example, BCDMA to trigger BCDMA or pktDMA or going back to interrupt aggregator's aggregating global events into interrupts.

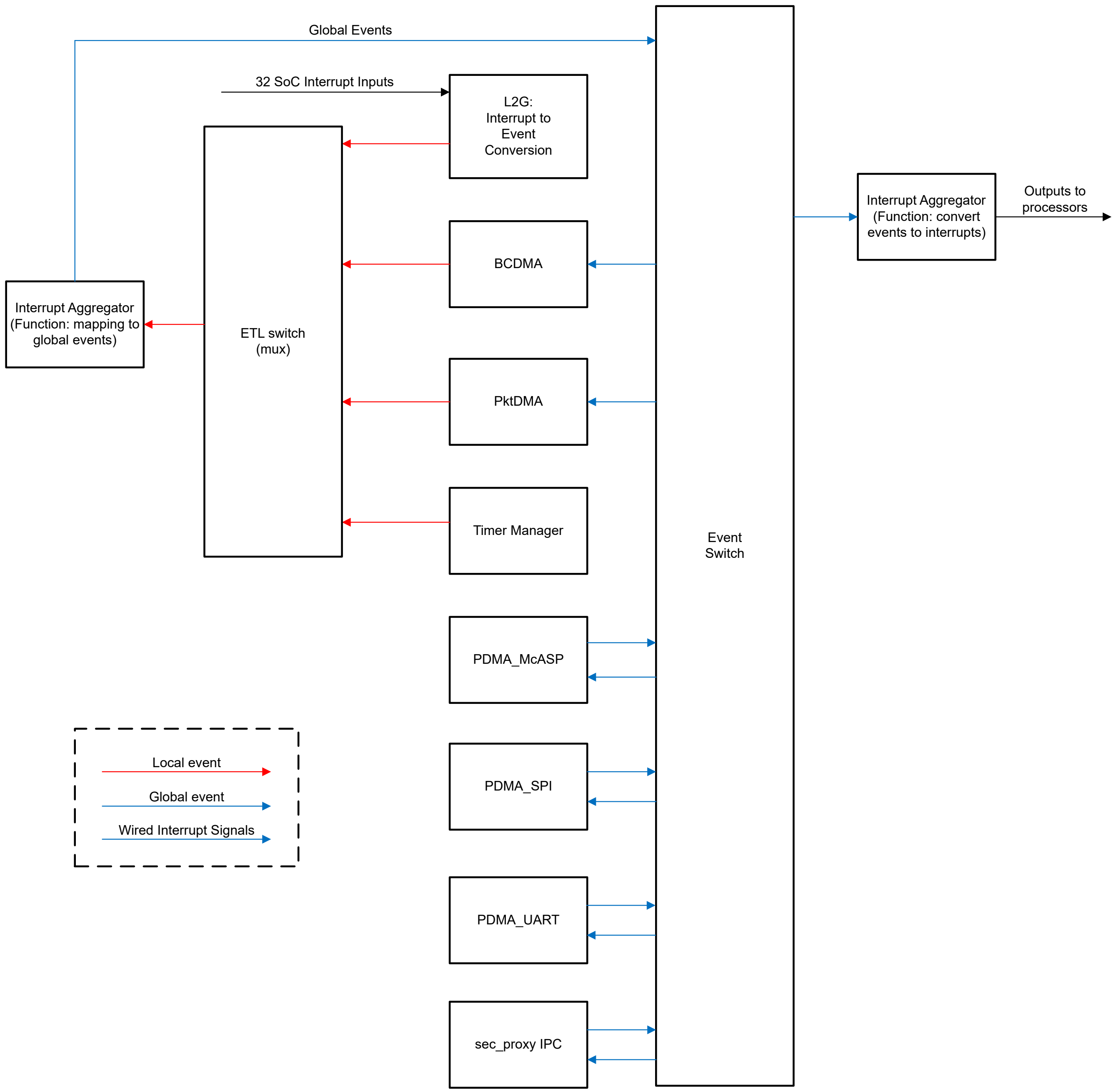

Figure 11-6. DMSS Event Flow

11.2.2 Ring Accelerator (RINGACC)

This chapter describes the RINGACC module, part of the DMSS.

Note

Not all of the RINGACC Functions specified in the document are supported in the device. Updates will be included in the next revision to reflect only supported modes of operation.

11.2.2.1 RINGACC Overview

The Ring Accelerator (RINGACC or RA) provides hardware acceleration to enable straightforward passing of work between a producer and a consumer.

Table 11-64. RINGACC Allocation Within Device Domain

Module Instance	Domain	
	MCU	MAIN
DMSS0_RINGACC0	-	✓(DMSS)

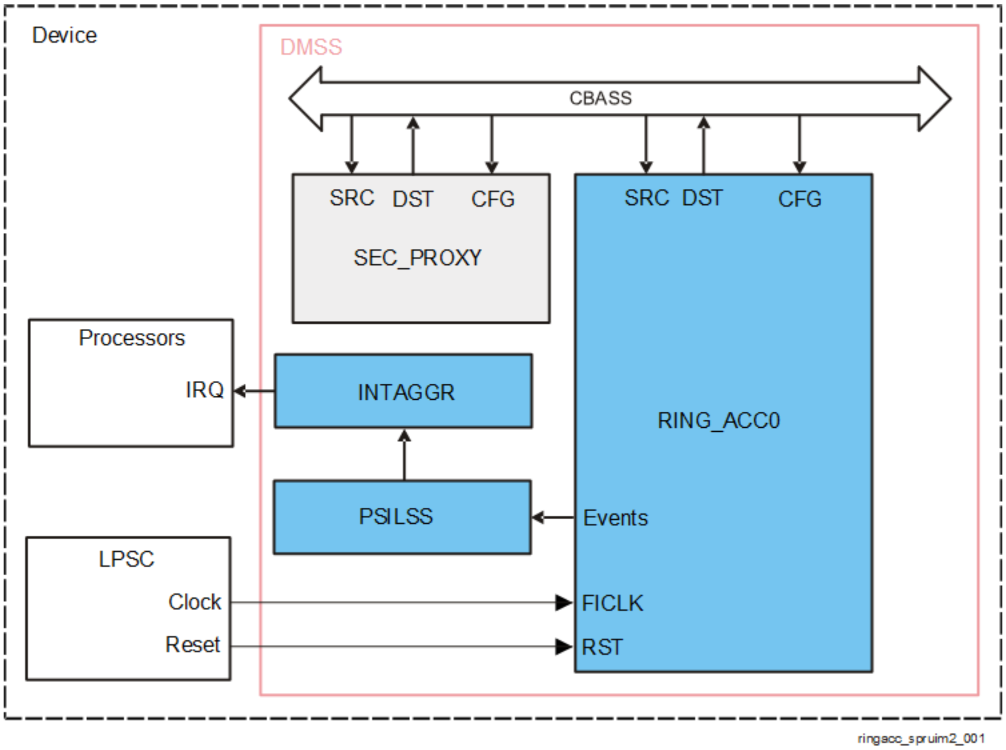

Figure 11-7. RINGACC Overview

11.2.2.1.1 RINGACC Features

- Ring Accelerator implementation
  - Supports up to 32 independent memory mapped ring structure
  - Supports various modes for each ring based on usage and compatibility
  - Provides single word deep shared incoming Transfer Response FIFO
  - Optionally supports dynamic clock gating
  - Provides bit wide source VBUSM read/write target interface for accesses from DMA controller entities
    - Provides 2 word deep command FIFO

- Provides 2 word deep write data FIFO
- Provides 2 word deep read data FIFO
- Provides 2 word deep write status FIFO
- Provides bit wide destination VBUSM read/write initiator interface for accesses to ring structures in memory
- Supports up to 16 outstanding writes
- Supports up to 16 outstanding reads
- Provides 2 word deep command FIFO
- Provides 2 word deep write data FIFO
- Provides 2 word deep read data FIFO
- Provides 2 word deep write status FIFO
- Source interface provides an array of 32x512-byte long address windows (four for each ring) which are packed into a single contiguous address range.
  - Read and write addresses which target a specific window are mangled to redirect the read or write transaction to an effective address calculated from the base address for the ring plus current ring offset.
  - Each read or write access presented on VBUSM target interface is modified and bridged onto the VBUSM initiator interface.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

11.2.2.1.2 RINGACC Parameters

RINGACC Configuration Parameters shows the RINGACC configuration parameters in this SoC

Table 11-65. RINGACC Configuration Parameters

Module Instance	Parameters		
	Ring Count	Number of Monitors	Proxy Target Base
DMSS0_RINGACC0	32	0	0x4e000000

11.2.2.2 RINGACC Functional Description

The Ring Accelerator (RINGACC) converts constant-address read and write accesses to equivalent read or write accesses to a circular data structure in memory. The RINGACC eliminates the need for each DMA controller which needs to access ring elements from having to know the current state of the ring (base address, current offset). The DMA controller performs a read or write access to a specific address range (which maps to the source interface on the RINGACC) and the RINGACC replaces the address for the transaction with a new address which corresponds to the head or tail element of the ring (head for reads, tail for writes). Since the RINGACC maintains the state, multiple DMA controllers or channels are allowed to coherently share the same rings as applicable. The RINGACC serves a very similar function to the Queue Manager in the earlier SoCs. The RINGACC uses less memory and is able to place data which is destined towards software into cached memory directly.

11.2.2.2.1 Block Diagram

Ring Accelerator Block-Diagram shows ring accelerator's main internal components.

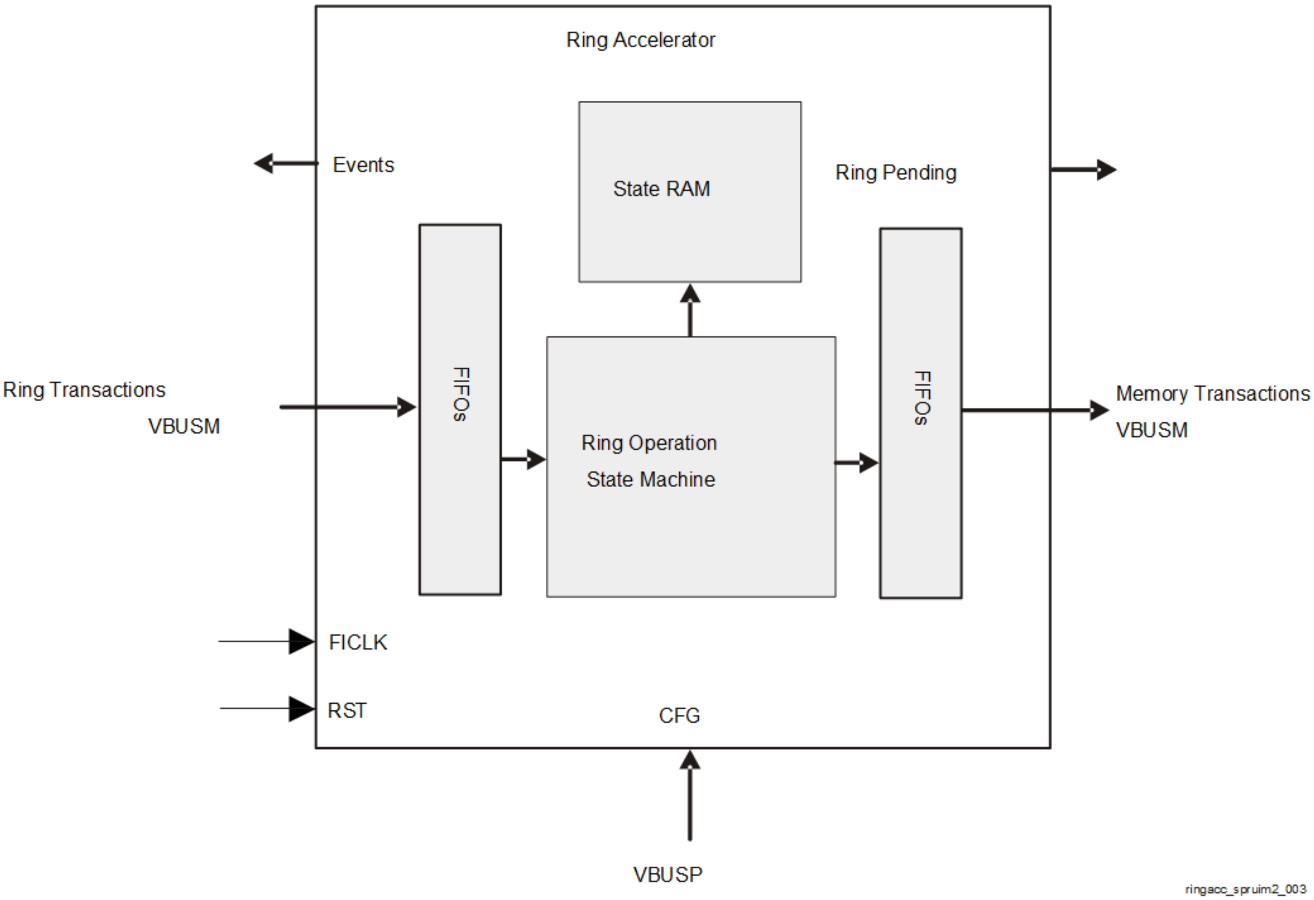

Figure 11-8. Ring Accelerator Block-Diagram

11.2.2.2.1.1 Configuration Registers

The Configuration Registers block is responsible for providing memory mapped registers for configuration of the RINGACC functions. The configuration registers are divided into:

- Static configuration fields , which are typically initialized and then left at specified values for long time periods (or until a reset occurs)
- Real-time (RT) registers , which are modified frequently during runtime. Configuration registers are listed and described in *RINGACC Registers*.

11.2.2.2.1.2 Source Command FIFO

The Source Command FIFO buffers VBUSM command phases which are accepted from the VBUSM source interface.

11.2.2.2.1.3 Source Write Data FIFO

The Source Write Data FIFO buffers VBUSM write data phases which are accepted from the VBUSM source interface.

11.2.2.2.1.4 Source Read Data FIFO

The Source Read Data FIFO buffers VBUSM read data phases which have been returned from the VBUSM destination interface (via the main state machine) and which are to be output on the VBUSM source interface.

11.2.2.2.1.5 Source Write Status FIFO

The Source Write Status FIFO buffers VBUSM write status data phases which have been returned from the VBUSM destination interface and which are to be output on the VBUSM source interface.

11.2.2.2.1.6 Main State Machine

The Main State Machine (MSM) block implements all of the control logic which is necessary to accept a command from the source interface, perform a lookup into the ring state RAM, determine the effective address for the destination interface transaction, modify the address (and byte count for reads) for the transaction, and place that modified transaction into the outgoing destination FIFOs. The MSM block is also responsible for updating the ring index and occupancy values and for producing output status to indicate changes to the ring state. The MSM also modifies the ring state whenever the read data or write status for a previous ring transaction return and forwards those responses back to the originating initiator.

11.2.2.2.1.7 Destination Command FIFO

The Destination Command FIFO stores VBUSM transaction commands which are output from the MSM as modified versions of transactions that were popped from the Source Command FIFO. The Destination command FIFO allocates a new command ID for each read or write command that is pushed to the FIFO. Read IDs are allocated from a scoreboard maintained in the Destination Read Data FIFO. Write IDs are allocated from a scoreboard maintained in the Destination Write Status FIFO. When a new command is allocated, the Destination Command FIFO also pushes the original cid and crouteid values from the source side transaction into a scoreboard in either the Destination Read Data or Destination Write Status FIFOs depending on the applicable transaction direction. The read interface of the Destination Command FIFO directly drives commands onto the destination VBUSM command interface.

11.2.2.2.1.8 Destination Write Data FIFO

The Destination Write Data FIFO stores write data phases for write commands that are passing through the RINGACC towards memory. The write interface of the Destination Write Data FIFO is directly connected to the read interface of the Source Write Data FIFO and the read interface directly drives write data onto the destination VBUSM write data interface.

11.2.2.2.1.9 Destination Read Data FIFO

The Destination Read Data FIFO provides a read command translation scoreboard and also stores read data phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the Destination Read Data FIFO is directly connected to the destination VBUSM read data interface. As read data passes through the Destination Read Data FIFO, the *rid* and *rrouteid* are changed back to their original values using information which was stored in read command translation scoreboard.

11.2.2.2.1.10 Destination Write Status FIFO

The Destination Write Status FIFO provides a write command translation scoreboard and also stores write status phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the Destination Writes Status FIFO is directly connected to the destination VBUSM write status interface. As write status words pass through the Destination Write Status FIFO, the *sid* and *srouteid* are changed back to their original values using information which was stored in the write command translation scoreboard.

11.2.2.2.2 RINGACC Functional Operation

11.2.2.2.2.1 Queue Modes

Each ring or queue can be in one of four modes that determines how it must be accessed and the compatibility it has with hardware and software.

11.2.2.2.2.1.1 Ring Mode

Ring mode is used when software owns one side of the ring, and hardware or another software owns the other side. This mode allows the software that owns a side of the ring to control that side including accessing the memory directly rather than going through hardware, and software updates the hardware on any changes through the Doorbell registers. These doorbell accesses indicate when software has pushed or popped entries, allowing the entity on the other side of the ring to know when there are elements ready. The ring mode has limitations that the exposed side of the ring is completely under software control, and any atomicity needed must also be performed by software, which is why the exposed side of a ring is usually owned by a single thread of software. This limitation also means that any hardware configuration that would normally access the same ring for both pushes and pops cannot use ring mode as hardware cannot access the exposed side of the ring, such as free queues that are normally read by hardware but could also be pushed by hardware on an error.

When software is popping from the ring, it must guarantee that it never pops more elements through the Doorbell register (RINGRT[a]_RT_DB) than what is valid in the Ring Occupancy (RINGRT[a]_RT_OCC) register, which holds how many elements are ready for software consumption. There could be some elements which have data written to memory but have not received status back from memory and those are not considered ready to pop yet as the ring status has not fully updated. Therefore, just reading from memory to determine the number of elements to pop is not sufficient. If software attempts to pop more than the RINGRT[a]_RT_OCC register value, then the occupancies could go negative resulting in missed down events and spurious interrupts. An optimization for software is to read the RINGRT[a]_RT_OCC register less frequently and keep a local copy which guarantees the maximum number of allowed pops. When the software copy of RINGRT[a]_RT_OCC reaches 0, or periodically, the software can read the register to refresh the value. This must reduce the frequency of register reads instead of reading the register for every software pop.

11.2.2.2.2.1.2 Messaging Mode

Messaging mode requires that all accesses to the queue must go through RINGACC so that all accesses to the memory are controlled and ordered. RINGACC then controls the entire state of the queue, and software has no directly control, such as through doorbells and cannot access the storage memory directly. This is particularly useful when more than one software or hardware entity can be the producer and/or consumer at the same time. Software must access the data through bus accesses to the RINGACC. As with the earlier example, if there are free queues that need the hardware to both push and pop, then they must be configured as at least messaging mode (or a later mode) and not ring mode.

11.2.2.2.2.1.3 Credentials Mode

Credentials mode adds per element credentials storage to messaging mode. This allows multiple producers with their own credentials to have those credentials stored with the element. This allows the consumer to inherit the credentials of each element rather than a single set for the entire queue, such as for DMA TR credential inheritance. This mode requires each operation to use two elements of storage since the credentials are stored in the second element, so the element count must be scaled appropriately. The credentials field is located in the same location as all modes, the word just before the first word of the message.

11.2.2.2.2.1.4 Peek Support

All modes except ring mode allow the peek operations so that software can view the next element without actually popping it from the queue. This is done by reading from a different offset from the normal pop operation. All the same fields are read but the element is not actually popped off of the queue. This is useful for algorithms that need to know about the overall queue and head element to make decisions but have not yet decided to pop from the queue.

11.2.2.2.2.1.5 Index Register Operation

In ring mode, the Index (RINGRT[a]_RT_INDX) register follows the software control of the ring through the doorbell registers, while the hardware index (RINGRT[a]_RT_HWINDX) register follows the hardware access of the ring through bus transactions. It works for a ring in either direction as the doorbell register (RINGRT[a]_RT_DB) update indicates whether elements were produced or consumed. But in the other queue modes, there is no simple manner to determine which index is for software or hardware since they both use bus transactions which the module cannot differentiate. So for these other queue modes, the index register is always the read index, and the hardware index register is the write index.

11.2.2.2.2.2 VBUSM Target Ring Operations

Each ring contains four memory spaces on the VBUSM target bus for access, each of which is 512 bytes long, with a total of 4 kB per ring. Each ring space starts immediately after the preceding ring. The allocation per ring is as in Table 11-66.

Table 11-66. Ring Memory Partition

Offset	Operation	Supported Ring Modes
0x0 - 0x1FF	Reads pop from head. Writes push to head.	Read supported in all modes, write supported in all modes except Ring mode
0x200 - 0x3FF	Writes push to tail. Reads pop from tail.	Write supported in all modes, read supported in all modes except Ring mode
0x400 - 0x5FF	Reads peek from head. Writes ignored.	All modes except for Ring mode.
0x600 - 0x7FF	Reads peek from tail. Writes ignored.	All modes except for Ring mode.
0x800 - 0xFFF	Reserved	Reserved

Within each 512-byte (0x200) space, the message data is right justified so that the last byte is always the 511-th byte. The element size of the ring defines which words are valid. The word just before the first valid message word is the credentials field. Access must not be made before the credentials register (CRED[a]_CRED).

11.2.2.2.2.3 VBUSM Initiator Interface Command ID Selection

The RINGACC keeps a transaction command scoreboard for reads and writes. Each scoreboard tracks which command indexes are currently outstanding from the RINGACC and which are free to use. When a read or write is requested by the Main State Machine, the scoreboard corresponding to the specified direction (read/write) is queried starting at index 0 and extending up to the maximum index for that scoreboard. The lowest index that is found and which is not currently allocated is selected and is directly used as the command ID (*cid*) for the outgoing transaction on the destination interface. 15 is the maximum index value for each scoreboard. Entries are freed for re-use in a write scoreboard when write status responses are received which account for all of the outstanding write data. Entries are freed for re-use in the read scoreboard only when all data has been returned for the read.

11.2.2.2.2.4 Ring Push Operation (VBUSM Write to Source Interface)

The following sequence will occur for each VBUSM write which is sent to the source interface:

1. RINGACC extracts ring number from incoming write transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective write address using *ring base* + *ring_index*
4. RINGACC re-evaluates pending bit for ring
5. RINGACC increments HW index and HW occupancy for ring
6. RINGACC allocates *cid* from scoreboard and places original *crouteid, cid, and ring number* into scoreboard

7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note *routeid* is not included)

At a later time when write status returns:

1. RINGACC recovers original *cid, crouteid,* and *ring number* from scoreboard
2. RINGACC increments SW index and occupancy for ring
3. RINGACC pushes restored *srouteid, sid*, and unaltered write status to output write status FIFO

11.2.2.2.2.5 Ring Pop Operation (VBUSM Read from Source Interface)

The following sequence will occur for each VBUSM read which is sent to the source interface:

1. RINGACC extracts ring number from incoming read transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective read address using *ring base* + *ring_index*
4. RINGACC increments HW index and decrements HW occupancy for ring
5. RINGACC re-evaluates pending bit for ring
6. RINGACC munges *cid* to add indicator in 4 MSBs to reconstitute *routeid* for returning read data
7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

At a later time when read data returns:

1. RINGACC recovers original *cid, crouteid*, and *ring number* from scoreboard
2. RINGACC increments SW index and decrements SW occupancy for ring
3. RINGACC pushes restored *rrouteid, rid,* and unaltered read data, status, and other control signals to output read FIFO

11.2.2.2.2.6 Host Doorbell Access

The following sequence will occur for each VBUSP write to the doorbell register (RINGRT[a]_RT_DB) for a ring:

1. RINGACC extracts ring number from config address
2. RINGACC looks up ring state using ring number
3. RINGACC adds doorbell ring value to both HW and SW occupancies for ring
4. RINGACC re-evaluates pending bit for ring

11.2.2.2.2.7 Queue Push Operation (VBUSM Write to Source Interface)

The following sequence will occur for each VBUSM write which is sent to the source interface:

1. RINGACC extracts ring number from incoming write transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective write address using *ring base* + *ring_index*
4. RINGACC re-evaluates pending bit for ring
5. RINGACC increments WR index and RD and WR occupancy for ring
6. RINGACC allocates *cid* from scoreboard and places original *crouteid, cid*, and *ring number* into scoreboard
7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

At a later time when write status returns:

1. RINGACC recovers original *cid, crouteid*, and ring number from scoreboard
2. RA pushes restored srouteid, sid, and unaltered write status to output write status FIFO

11.2.2.2.2.8 Queue Pop Operation (VBUSM Read from Source Interface)

The following sequence will occur for each VBUSM read which is sent to the source interface:

- RINGACC extracts ring # from incoming read transaction address
- RINGACC looks up ring state using *ring number*
- RINGACC calculates effective read address using *ring base* + *ring_index*
- RINGACC increments RD index and decrements RD and WR occupancy for ring
- RINGACC re-evaluates pending bit for ring
- RINGACC munges cid to add indicator in 4 MSBs to reconstitute routeid for returning read data
- RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

1. At a later time when read data returns:

- RINGACC recovers original *cid, crouteid*, and *ring number* from scoreboard
- RINGACC pushes restored *rrouteid, rid*, and unaltered read data, status, and other control signals to output read FIFO

11.2.2.2.2.9 Mismatched Element Size Handling

When less data is written than defined by the element size for the ring for RING or MESSAGE modes, only the written data is stored in the memory and any remaining bytes maintain their old values. The index and occ are still incremented normally, and any special fields that are unwritten are assumed to be 0 (such as the length for QM mode rings).

Writing less data for CREDENTIALS mode is illegal, as those types need the full data to append the additional words to the correct offsets in memory.

When more data is written than defined by the element size for the ring, it will be an error and the write will be ignored and no index or occ increments occur. The only exception is for writes to an 8 byte element size ring, where the additional fields up to another 8 bytes are allowed but not written (for old Queue Manager compatibility).

When less data is read than defined by the element size for the ring, only the read data is fetched from memory, and any remaining bytes are lost. The index and occ are still incremented normally.

When more data is read than defined by the element size for the ring, it will be an error and the read will not affect the ring, the read data will be 0s, and no index or occ decrements occur. Access beyond the credentials word should not be attempted and can result in unpredictable behavior.

All accesses must be for multiples of 32 bit words, and partial bytes are not supported for all ring modes.

11.2.2.2.3 Events

The module outputs events about queue levels that can be used by an external module for statistics or interrupts.

Each queue has:

- an up event when the queue goes from 0 elements to 1 or more elements
- and a down event when the queue goes from 1 or more elements to 0 elements. The event number is programmable per queue in the RING[a]_EVT register. This event occurs when the state machine updates the final occupancy for the queue. In ring mode this is when the response from the memory access returns, while in other queue modes this is when the operation is processed.

An event number programmed to 0xFFFF indicates to not produce an event for that ring when an event is not necessary. The register event number fields reset to 0xFFFF, so they must be programmed to a valid value before events will be generated. This applies to the monitor event number fields as well.

11.2.2.2.4 Bus Error Handling

If a bus error is detected on a response to a ring memory transaction, an error event is triggered to alert software. Since the ring contents may be corrupted as the push or pop was not completed correctly, software should consider resetting the ring and any software or hardware elements using the ring. A log register

(RINGACC_ERROR_LOG) captures the ring that had the error and whether it was from a push or pop, and an error up event is sent to the programmed event number. After an error is logged, another will not be captured until the first is read out. When read, if an error is pending an error down event is sent to clear any interrupt, and then the next bus error log can be captured. A read of the RINGACC_ERROR_LOG register when there is no error log pending will not produce any down events. The event that is triggered is also programmable. Only legal push and pop operations will capture this error, and not for any peek, emudbg read, flush command, or any operations that is illegal and causes the resulting memory access to be flushed.

11.2.2.2.5 Monitors

Monitors can be configured that allow various functions to be tracked of programmed queues. Each monitor is programmed to monitor a particular queue, the function to provide, and the data source to operate on. The supported functions are: to check the queue against programmed thresholds, to keep track of watermarks of the queue, to keep track of starvation occurrences (a read of an empty queue), or statistics capture. The supported data sources are: the queue element count, the head element size value, or the accumulated size value. Each monitor can also be programmed to produce an event should it have a triggering condition.

11.2.2.2.5.1 Threshold Monitor

A threshold monitor uses a programmed low threshold value and a programmed high threshold value to track the data source in the queue and cause an interrupt or status when a threshold is broken, either below the low value or above the high value. This is useful for software to replenish empty buffers when a queue has too few, or for a queue to accumulate enough elements so that software must start processing them, or for debug. The threshold being broken will cause the up or down event.

11.2.2.2.5.2 Watermark Monitor

A watermark monitor tracks the low and high values of the data source since the last read of the monitor. After initial setup or clearing, the watermark values will load the current value of the data source as the low and high. Then for successive operations if the resulting data source of the queue is below the low watermark, or above the high watermark, the associated watermark will be updated. When the monitor value registers are read, the value is cleared and starts tracking again using the current data source value. This can be useful for tracking low and high values of queue element counts or sizes for data tracking, debug or future optimizations, such as allocating items to a queue or buffer sizes based on counts.

11.2.2.2.5.3 Starvation Monitor

A starvation monitor tracks the number of starvation events (a read to an empty queue) that occurred on the queue. The data source is ignored, and the starvation count is always incremented whenever there is a read to the queue and the queue is empty. The count is cleared when the monitor value is read. This can be useful to trigger if any starvation event occurs, or to track how many of these events occur in a timeframe, and can be used for future optimizations or debug.

11.2.2.2.5.4 Statistics Monitor

The statistics monitor can track some simple statistics on the queue operations. The data source is ignored. The first value is the count of the number of writes to the queue, and the second value is the count of the number of reads from the queue. The counts are cleared when the monitor values are read. This can be useful to track the activity on a queue, and can be used for future optimizations or debug.

11.2.2.2.5.5 Overflow

RINGACC provides an overflow function where a push to a full ring will result in a push to a special overflow ring, rather than just losing the pushed data. The overflow ring is defined through RINGACC_OVERFLOW register, and that ring must be defined with a large enough element size to cover the element size of any other ring, as well as enough elements to hold enough overflow data (as an overflow to the overflow ring will be lost). When there is a push to a full ring, there will be two elements written to the overflow ring, first the push data, and then the ring number that was full. A supervisor entity can own the overflow ring and perform what actions are needed from the overflow data. The size of the overflow ring must be an even number since two elements will be pushed for each overflow event. The overflow ring must be configured in ring or message modes.

An overflow queue value of 0xFFFF will disable the overflow function and will not record queue overflows. (SR2.0)

11.2.2.2.5.6 Ring Update Port

To enhance performance for DMAs, the RINGACC provides a bus that indicates when ring updates occur, allowing the DMA to track their own rings and detect updates before the responses arrive. The bus will go valid whenever there is an update to the state of a ring, which can be from a push, pop, or doorbell write. It will not go valid for a peek, an emudbg pop, or a push to a full ring, as those do not update the ring state. When the bus is valid, the other signals are valid and indicate whether the operation was a push or a pop, whether the resulting state of the ring is empty, the ring number, and the number of elements updated to the ring (the push determines whether it is subtracted or added to the current count). One special case is a pop from an empty ring, which indicates an update but the element count is 0 since no items were actually popped, but a DMA using the cnt to add or subtract must handle this correctly by default. The bus will go valid once the operation command has been completed, and not after the response has been received, even for ring mode rings, allowing the DMA to see the update as soon as it is known by the RINGACC even before it is known to software.

11.2.2.2.5.7 Tracing

This module provides a trace output of all operations so that the traffic can be viewed at a later time. The trace uses a simple write-only 32-bit VBUSP bus, with a defined packet header. The msgtype field defines the type of operation, and the message data is simply the data involved in the operation. It is likely the trace output will be read slower than new operations could provide data, so there will be a trace buffer able to hold two complete messages plus trace headers. If a new operation starts while the trace buffer does not have enough space, then that trace message will not be sent. And RINGACC_TRACE_CTL register controls whether to enable the trace output, whether to trace a single queue or all queues, and whether to include the message data in the trace output.

Table 11-67 shows the trace message for a push.

Table 11-67. Trace Message for a Push

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x1	Msgtype for push
1	8:0	0x009	Standard Trace Header
2	31	push_to_head	Push to head flag, 0 = to tail, 1 = to head
2	30:16	0x0	Unused
2	15:0	queue	Queue for push
3-N	31:0	message data	Optional message data for push, length dependent on message size

Table 11-68 shows the trace message for a pop.

Table 11-68. Trace Message for a Pop

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware

Table 11-68. Trace Message for a Pop (continued)

Word	Bits	Data	Comment
1	15:9	0x2	Msgtype for pop
1	8:0	0x009	Standard Trace Header
2	31	empty	empty pop, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for pop
3-N	31:0	message data	Optional message Data for pop, length dependent on message size

Table 11-69 shows the trace message for a peek

Table 11-69. Trace Message for a Peek

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x3	Msgtype for peek
1	8:0	0x009	Standard Trace Header
2	31	empty	empty peek, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for peek
3-N	31:0	message data	Optional message Data for peek, length dependent on message size

11.2.3 Secure Proxy (SEC_PROXY)

This chapter describes the Secure Proxy (SEC_PROXY) module in the DMSS.

11.2.3.1 Secure Proxy Overview

The Secure Proxy module provides proxy buffers for hosts that need to create large data bursts but can only perform small accesses.

11.2.3.1.1 Secure Proxy Features

Secure Proxy supports the following features:

- Provides proxy function to store large data bursts that a host can only access in smaller amounts
- Supports a configurable number of threads, where each has their own independent proxy function
- Keeps the large data burst coherent until the complete data has been accessed
- Allows for interleaved access between multiple hosts or tasks using multiple proxy threads
- Supports a configurable target resource. The target has a configurable number of channels, size of each channel and base address
- Supports a programmable fixed queue for each proxy thread
- Supports multiple producers all writing to the same queue
- Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
- Supports programmable thresholds for when to generate events
- Optionally supports dynamic clock gating

Table 11-70. Secure Proxy Allocation Within Device Domain

Module Instance	Domain	
	MCU	MAIN
DMSS0_SEC_PROXY0	-	✓(DMSS)

11.2.3.1.2 Secure Proxy Parameters

Secure Proxy Configuration Parameters shows the Secure Proxy configuration parameters set during SoC design.

Table 11-71. Secure Proxy Configuration Parameters

Module Instance	Parameters				
	Proxies(1)	Message Size(2)	Target	Channels(3)	Sizes(4)
DMSS0_SEC_PROXY0	76	64	DMSS0_RINGACC	20	4096

(1) Number of proxy threads supported. Can be read off from the SEC_PROXY_CONFIG read-only register
(2) Number of bytes for message. Can be read off from the SEC_PROXY_CONFIG read-only register
(3) Number of channels for the target
(4) Number of bytes per channel supported for the target

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

11.2.3.2 Secure Proxy Functional Description

This module provides proxy functions for hosts that need to create large data bursts but can only perform small accesses. Examples of this need are:

- large messages (for power control, security control, or IPC)
- data descriptors that are more than a pointer
- DMA Transfer Requests (TR)

All of these require larger data sets, from 12 to 128 bytes, and the storage hardware requires the entire data on the bus in a single burst. Unfortunately, many CPUs cannot produce bursts to device memory, such as registers, and the largest CPU access is typically 8 bytes. So the proxy provides the ability to access the hardware with a single burst, and at the same time allows the CPU to access the same data in smaller accesses. The proxy itself does not contain the resources, but will front other hardware that do contain the resources. The proxy will access this other hardware with the entire data in a single burst, once the host has completed the data.

Secure Proxy Block Diagram describes Secure Proxy major building block

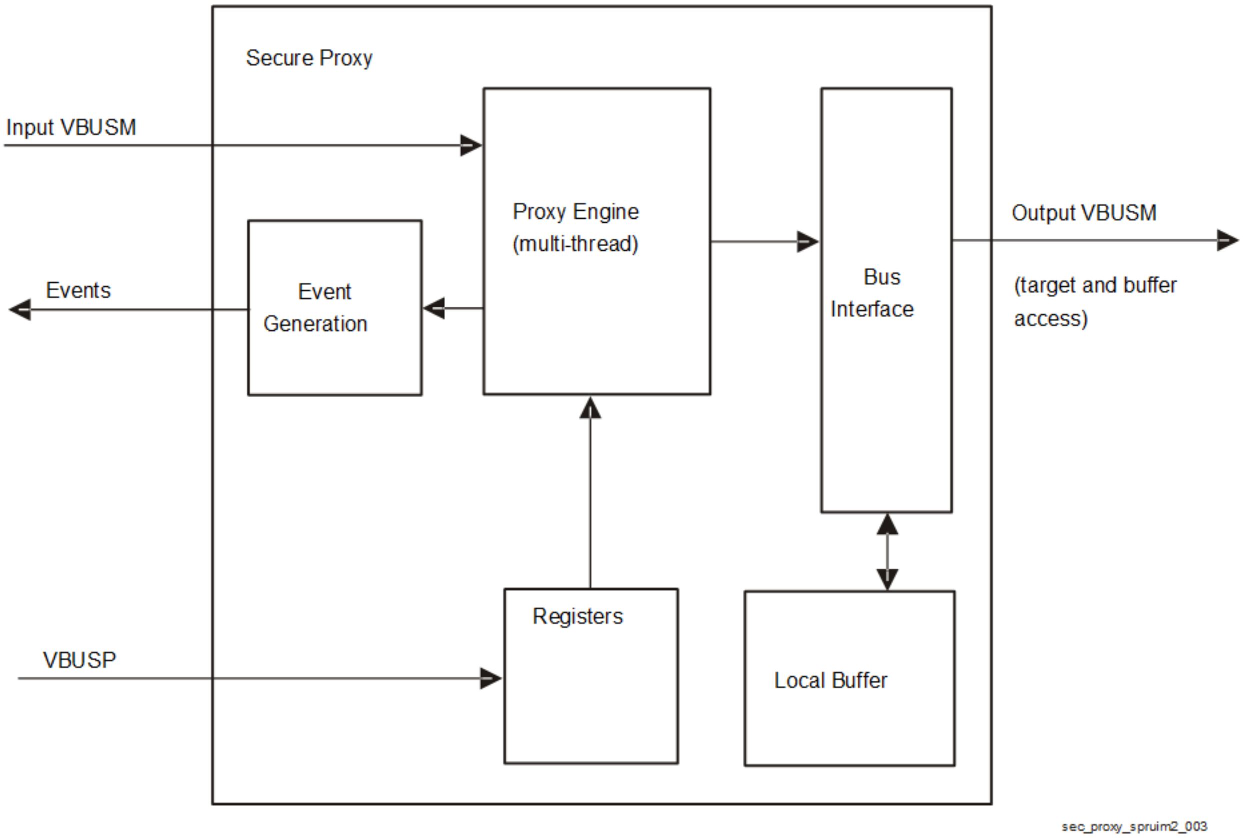

Figure 11-9. Secure Proxy Block Diagram

11.2.3.2.1 Targets

11.2.3.2.1.1 Ring Accelerator

The RINGACC provides four distinct offsets to use per ring/queue shown in RINGACC Offset per Ring/Queue, totaling 4 KB space per ring/queue.

Secure Proxy always writes to tail, which is the offsets from 0x200 to 0x3FF. Secure Proxy always reads from the head, which is the offsets from 0x000 to 0x1FF. The latter two offsets in RINGACC are not used by this proxy. And if the proxy message size is less than 512 bytes, then it always accesses the upper bytes of those regions, so that the message always ends on the last byte of each region, byte 511.

Table 11-72. RINGACC Offsets per Ring/Queue

Offset	Operation
0x0 - 0x1FF	Reads pop from head. Writes push to head.
0x200 - 0x3FF	Writes push to tail. Reads pop from tail.
0x400 - 0x5FF	Reads peek from head. Writes ignored.
0x600 - 0x7FF	Reads peek from tail. Writes ignored.
0x800 - 0xFFF	Reserved.

This means that target writes will use the following calculation:

target base address + (queue × 4KB) + 0x400 - msg_size (17), and burst until offset 0x3FF.

And target reads will use the following calculation:

target base address + (queue × 4KB) + 0x200 - msg_size (18), and burst until offset 0x1FF.

11.2.3.2.2 Buffers

The proxy does not store all the buffers internally. It is programmed with a buffer base address (SEC_PROXY_BUFFER_L, SEC_PROXY_BUFFER_H), and all accesses to the buffer are made through the output VBUSM port using that base. The external buffer must be enough to store one msg_size per proxy thread. The proxy only includes a small temporary buffer to save one entire message when accessing the target. Otherwise all host accesses are made to the external buffer. This buffer storage must be considered private for the proxy hardware, so any other access can cause unpredictable results.

11.2.3.2.2.1 Proxy Credits

To support outbound proxy limits, the proxy will use internal credits for tracking resource usage. SEC_PROXY_THREAD[a]_CTL register sets the max credits each outbound proxy thread contains. When a proxy thread sends a message, the current credit count (SEC_PROXY_THREAD[a]_STATUS) decrements by 1. If the current credit count is 0, then the proxy thread is not allowed to send any more messages, and they just remain inside the proxy (so that the host can come back later when a credit has become available and quickly send the same message). When a message that was send by this proxy thread is read by an inbound proxy thread then the credit is returned to this proxy thread and the current credit count increments by 1.

For inbound proxy threads, the credits are used to track pending messages. When an outbound proxy thread sends a message that is read by this proxy thread, then the current credit count of this proxy thread is incremented by 1. A current credit count that is non zero indicates a message is pending and can be read. When the proxy thread completes the read of a message the current credit count is decremented by 1. If the current credit count is zero, then the proxy thread will read an empty message where all the data is 0s. The credit count saturates at 255, so if there can be more messages in the system for that proxy thread than 255 then multiple proxy threads should be used, or the count can become mismatched after a saturate.

11.2.3.2.2.2 Proxy Private Word

To support tracking of credits from each proxy thread, the proxy will extract the first word from the total message size for private tracking usage. This will include saving the proxy thread ID used within the proxy. This is necessary so that when a proxy reads a new message from the target it can inspect this word and return the credit to the source proxy thread. This allows the outbound proxy threads to have a set number of message credits, which decrement when a new message is written, and increment when a message from that proxy thread is read, thus keeping the credits in the system coherent. Any data written to this first word of the message will be ignored, so software should not write to the first word of messages through the proxy. Consumer software can use the first word to identify the source proxy thread of the message (SEC_PROXY_DATA_j).

11.2.3.2.2.3 Completion Byte

The proxy completes a message when the completion byte is accessed. This completion byte is the final byte in the full size of the message. This byte can be written by any size access, whether byte, 32-bit, or 64-bit word. The write of a message is not complete until this final byte of the message is written, and only then will the message be sent to the target. The read of a message is not complete until this final byte of the message is read by the host, and only then will reading a new message be allowed. Even if the final byte of the message is not needed, it must be accessed to complete the message inside the proxy hardware.

11.2.3.2.3 Proxy Thread Sizes

There are a configurable number of proxy threads in the module. Each thread has its own address space to the module and determining which proxy thread is being accessed is simply based on the address bits above the final size of each proxy thread space. Since each proxy thread will be programmed to a single resource, the only space requirement is that for using 4 KB to match typically used MMU page sizes. Only the first N bytes, matching the target channel size, is usable.

11.2.3.2.4 Proxy Thread Interleaving

Each proxy thread must have a single owner, as each proxy thread only has a single buffer to work on the current data. If there are multiple owners in the system, they must each use their own proxy thread. Then they will have their own buffer and each can access a different resource at the same time. Each proxy thread is completely independent and kept coherent regardless of accesses to other proxy threads or regardless of the order of accesses. So the proxy support interleaving of multiple hosts' accesses.

11.2.3.2.5 Proxy States

Each proxy thread uses a simple state machine to track the currently usage by that host. This state machine is used to track when a proxy thread is in use or not, but also for error detection. The proxy thread always starts in idle state, when there is no currently activity. There is a write state for when the proxy thread has been written and contains data that has yet to be written to a resource. There is a read state for when the proxy thread has read data from a resource and that entire data has not been fully read by the host. When a proxy thread access completes, final write or final read, then the state will go back to idle. The following sections show the utilization of these states.

11.2.3.2.6 Proxy Host Access

A proxy thread begins in an idle state, where there is no data in the buffer. In this state the proxy thread will accept an access to the resource.

11.2.3.2.6.1 Proxy Host Writes

The first write to an idle proxy thread puts the proxy thread into write mode for the selected channel. Further legal writes are stored in the buffer for the enabled bytes and offset within the buffer. A write to a previously written location will overwrite the previous data. The buffer is not cleared initially, so if a byte is not written, the message will include previous buffer data. When there is a legal write to the last byte of the resource, then the entire data is written by the proxy to the target and channel as a single write burst. The proxy will wait for the write status from the target write before it sends the write status for this final byte host write. This allows the host to use the write status to guarantee the entire write data from the proxy has landed at the target. The proxy thread is then put back into idle state. A write completion when there are no credits available results in the message not being written to the resource and the proxy thread remains in write mode (so that the message can be quickly completed when a credit becomes available).

11.2.3.2.6.2 Proxy Host Reads

When in idle state, the first read to the proxy thread will put the proxy into read state, and the proxy will read the target and channel requested in a single burst of the target's channel size. When the data is returned it is stored in the buffer and the accessed part is returned to the host. Further legal reads are allowed and return the accessed data in the buffer. When there is a legal read to the last byte of the resource, the accessed data is returned, and the proxy thread is put back into idle state. If an initial read is made and there are no pending messages, the proxy thread will return an empty message, where the data is all 0s.

11.2.3.2.6.3 Buffer Accesses

Each read or write will actually trigger a read or write to the external buffer space allocated for that proxy thread, where the real message data is stored. In addition, when a write message completes, the external buffer will be read for the entire message for that proxy thread so that it can then be written to the target. Similarly, after a read causes a read from the target to get a new message, the entire message is written to the external buffer to store the message to the buffer.

11.2.3.2.6.4 Target Access

After the write has completed and the external buffer read for the entire message, the entire message is then written to the target as a single burst. Similarly, for a read that needs a new message, the target is read for a full message as a single burst.

11.2.3.2.6.5 Error State

If an error is detected in a proxy thread, the proxy will put that proxy thread into error state, and the current buffer will be lost. A status bit will be set that indicates the proxy thread is in error. All accesses to that proxy thread will be ignored until the status bit is cleared. Once cleared the proxy thread is put back into idle state. Errors are an access to an offset beyond the length of the message, or a mismatch in the direction of access against what was programmed such as reading an outbound thread or writing an inbound thread.

11.2.3.2.7 Permission Inheritance

The proxy will automatically inherit the permissions from the access and pass these to the target upon the target burst access. The exact transactions that are inherited from are the final byte write or the first read, and these exact permissions are used on the output bus transaction that accesses the target.

11.2.3.2.8 Resource Association

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the resource within the target that the proxy thread is mapped to. The host has no ability to access any other resource in the target. This allows the setup of the proxy to determine the resources that all the hosts use.

11.2.3.2.9 Direction

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the direction for access. It can either be an outbound proxy thread for writing messages to resources. Or it can be an inbound proxy thread for reading messages from resources. The host must match the direction programmed or it will result in a proxy thread error.

11.2.3.2.10 Threshold Events

Each proxy thread can produce events based on the state of the resource it uses. For outbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to write. For inbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to read. These threshold values are programmed in SEC_PROXY_EVT_MAP_j, allowing the host to determine how often it gets events. Programming the count values while the threshold is set to 0 will not trigger events, but if the threshold is not 0 then programming the counts will trigger events based on whether the threshold is reached or not. No event is generated if the event is programmed to 0xFFFF.

11.2.3.2.11 Error Events

Each proxy thread can produce an event when it has detected an error. This error occurs when the host violates the programmed setup of the proxy thread or accesses beyond the message size. There is a separate status bit per proxy thread for these errors. No event is generated if the event is programmed to 0xFFFF.

11.2.3.2.12 Bus Error and Credits

If a target read for a message returns a bus error, this indicates the read was bad and the data is corrupt and usually 0s. Because the private word in contained in the message, if the private word is corrupted then the source proxy thread is not valid and the credit return will not be correct. Since the data is usually 0, this means the credit would be returned to proxy thread 0 incorrectly most of the time. And the credit will be lost for the actual source proxy thread of the message that was not read correctly. The hardware has no way to correct for this, as the message from the target is corrupt so it does not know the correct owner of the credit. If software detects that a read message is corrupt, it can attempt to correct the situation by resetting the affected proxy threads using that queue, to restore their credit counts back to the default. Software may also want to reset proxy thread 0 since it may be getting extra credits.

11.2.3.2.13 Debug

When the transaction has the emudbg set for a read, all side effects will not occur. This means that the read will not cause a target read since that would affect the target, and instead current buffer will be read even if the previous message has completed.

11.2.4 Interrupt Aggregator (INTAGGR)

This chapter describes the INTAGGR module, part of DMSS

11.2.4.1 INTAGGR Overview

The Interrupt Aggregator (INTAGGR or INTA) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane (ETL) bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

Table 11-73. INTAGGR Allocation Within Device Domain

Module Instance	Parameters	
	MCU	MAIN
DMSS0_INTAGGR0	-	✓(DMSS)

11.2.4.1.1 INTAGGR Features

The DMSS0_INTAGGR0 supports the following features:

- 64-bit VBUSP target using 64-bit registers
- Provides a set of TI Interrupt Architecture compliant interrupt status and mask register sets which are used to pass specific event status to one or more Host blocks.
  - Maps a collection of DMA Messaged Events which are input through an Event Transport Lane into specific bit locations in one or more interrupt cause registers
  - Mapping is performed based on a programmable table which provides a single location for each ordinal input event number (0 through sevt_cnt-1)
    - Table specifies a specific bit in a specific cause register that the event should set or clear depending on the type of event (up vs down)
    - Tracks a single 'event up' / 'event down' condition. There is no event counting. (The 'cnt' field of the ETL is ignored.)
  - Tracked status interrupts are presented to the user through a standard interrupt register interface.
    - Provides separate 'enable set' and 'enable clear' registers.
    - Provides both masked and unmasked interrupt status.
    - Interrupt status bits can be manually cleared using 'write 1 to clear'.
- Provides an optional set of Unmapped Event (UNMAP) which can take an 'unmapped' event from the ingress ETL and generate a Global event on the egress Event Transport Lane (ETL) interface.
  - Each ingress event can generate an egress Global event on the egress ETL, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) counters which can count events which were delivered via an ingress Event Transport Lane (ETL).
  - Each counted event provides an MMR by which the count can be read and an MMR by which a specified amount can be decremented by the host.
  - Each counted event generates an egress Global event on a zero to non-zero and non-zero to zero transition, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on the egress ETL interface.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.

- Provides an optional set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL.
  - Each ingress event index provides a configurable 'pulse' or 'rising edge' bit, plus the configurable index of the generated Global event.
- Supports dynamic clock gating via

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

11.2.4.1.2 INTAGGR Parameters

Interrupt Aggregators Parameters shows the Interrupt Aggregator 0, parameters set during design time.

Table 11-74. Interrupt Aggregators Parameters

Module Instance	Parameters				
	VINTR[1]	SEVI[2]	GEVI[3]	LEVI[4]	MEVI[5]
DMSS0_INTAGGR0	184	1536	256	32	128

(1) VINTR – Number of Virtual Interrupt outputs. These are connected to the interrupt router inputs. Value can be read from INTAGGR_INTCAP register.

(2) SEVI – Number of Main (Steerable) Events. Value can be read from INTAGGR_INTCAP register.

(3) GEVI – Number of Countable Events. Value can be read from INTAGGR_AUXCAP register.

(4) LEVI – Number of Local Event inputs. Value can be read from INTAGGR_AUXCAP register.

(5) MEVI – Number of Multicast Events. Value can be read from INTAGGR_AUXCAP register.

11.2.4.2 INTAGGR Functional Description

The Interrupt Aggregator (INTAGGR) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the Host(s) in the system. Both the signaling and content of TI system events are incompatible with standard interrupt controllers. The INTAGGR provides mechanisms which convert the TI proprietary system events to standard level sensitive pending bits which can be used by all downstream interrupt infrastructure. Events can be presented to the INTAGGR in two different forms:

- Events may be active high pulses, or clock synchronous rising edges, which are input on separate orthogonal pins. These are called 'Local Events'.
  - Local event signals that are used in pulse counting mode must be sourced by the same clock as the interrupt aggregator.
  - Local event signals that are used in edge counting mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the interrupt aggregator clock, and they must remain high for at least 1 'slow' clock cycle.
- Events may be messages which are input in time division multiplexed sequential order from an Event Transport Lane. These are called 'Global Events'.

In both cases, these events need to be conditioned to transition them from a transient indicator that something occurred to a persistent and reliable indication of the current state of the system. The IA is architected to perform this conversion in an efficient and cost effective manner.

11.2.4.2.1 Submodule Descriptions

11.2.4.2.1.1 Status/Mask Registers

The Status and Mask Registers block is responsible for providing persistent storage for the interrupt status and mask bits and for formatting those in a way that is compliant to the TI Interrupt Architecture requirements. These requirements include the ability to set and clear bits orthogonally and to provide a masked version of the status register that corresponds to the supplied bit mask for each register.

11.2.4.2.1.2 Interrupt Mapping Block

The Interrupt Mapping Block accepts ordinally numbered events (0-N) and converts those ordinal event numbers into a status register number and bit number pair that is then used to manipulate the specified bit in the Status Registers block.

11.2.4.2.1.3 Global Event Input (GEVI) Counters

The GEVI Counters block is responsible for accepting an Event Transport Lane events and summing the total message counts for each received event index. The module creates global egress events for zero to non-zero count up' events and non-zero to zero 'count down' events. The egress global event index is configured via GEVI[a]_MCMAP register, so count status egress events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.1.4 Local Event Input (LEVI) to Global Event Conversion

The Local to Global event block is responsible for accepting an array of input pins and independently counting the number of cycles for which those pins are asserted high, or by counting individual clock synchronous rising edge events. The counting mode is configurable on a 'per pin' basis. The events are converted to egress Global events on an egress ETL. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.1.5 Global Event Multicast

The Global event multicast block takes an ingress global event from an ingress ETL, and maps it into two egress Global events on two egress ETL interfaces. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.2 General Functionality

11.2.4.2.2.1 Event to Interrupt Bit Steering

Each time an event message is received on the Main Event Transport Lane interface, the interrupt mapping block performs a direct lookup into an SRAM using the event number as the address. The SRAM stores a corresponding interrupt status (INTR_STATUSM) register and bit number within that register (VINT[a]_STATUS_MSKD) which are to be manipulated anytime a message is received indicating something occurred on that specific event. When an up event is received, the specified bit in the [a] Status register will be set. When a down event is received, that same bit will be cleared. This block is what allows flexible aggregation of various system events into an array of bits in the interrupt status registers. It is intended that this mapping is essentially static - set up when a resource is allocated and left untouched until the resource is no longer needed. Note that the 'cnt' field of the ETL is ignored and no interrupt counting is performed here. When 'UpDn=1', the interrupt flag bit is set, and when 'UpDn=0', the flag bit is cleared.

11.2.4.2.2.2 Interrupt Status

The event messages which are generated from the event to interrupt bit steering logic are input to the Interrupt Status registers. Each time an event is received, the interrupt status registers machine will assert or de-assert the specified bit in the specified register. The assertion and de-assertion in the interrupt status register is unaffected by the interrupt enable state. When an up event is received, the corresponding bit is set and when a down event is received, the corresponding bit is cleared. Some sources of input events will not include the ability to send a down event. In these cases, the interrupt router provides the ability to clear the status bits through the Interrupt Source Clear register (VINT[a]_STATUS). The host will write a one to the specific bit in the register which is to be cleared and the interrupt status machine will clear the bit internally. It is not intended that the Host directly clear bits which are automatically cleared via down events from the source itself.

11.2.4.2.2.3 Interrupt Masked Status

Interrupt enable bits are used in conjunction with the interrupt status bits to create the interrupt masked status register values. The interrupt masked status register (VINT[a]_STATUS_MSKD) contains the value of the interrupt status ANDed with the value of the interrupt enable register (VINT[a]_ENABLE_SET). Each time a new event message is received from the event to interrupt bit steering logic or the interrupt enable register is modified, the interrupt masked status register is re-evaluated.

11.2.4.2.2.4 Enabling/Disabling Individual Interrupt Source Bits

Separate (VINT[a]_ENABLE_SET and VINT[a]_ENABLE_CLR) registers are provided to allow individual enable bits to be enabled or disabled without the need for a read-modify-write operation. When the VINT[a]_ENABLE_SET register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be set. When the VINT[a]_ENABLE_CLEAR register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be cleared.

11.2.4.2.2.5 Global Event Counting

When enabled, the INTAGGR will provide a set of counters which will track how many outstanding messages have been observed for each ingress event index from the ingress Counted Global Event Transport Lane (ETL) interface. For each message received where the 'UpDn' flag is set, the corresponding counter will be incremented by value of the 'cnt' field of ingress message. Events where the 'UpDn' flag is cleared are ignored. The counter is made visible to software in the GEVI[a]_COUNT register. When software has read the count, it can acknowledge that count has been seen and processed by writing back an integer value specifying the amount by which the counter should be decremented, and the counter will subtract that value from the current count (which may have updated since it was read). The count will saturate at a value of 0xFFFFFFFF. Writing a count 'ack' value higher than the one read is not supported and will produce non-deterministic results.

When a count transitions from zero to a non-zero value, a Global Up 'UpDn=1' event is sent out an egress ETL interface. When a count transitions from a non-zero value to zero, a down 'UpDn=0' event will be sent. The index of the Global event is mappable on a 'per-counter' basis, using the GEVI[a]_MAP register. The event may be mapped such that it then re-enters INTAGGR's 'Event to Interrupt Bit Steering Block' to generate an interrupt to the host. The event routing is handled by an external event switch fabric. Note that writing a new egress event index via the GEVI[a]_MAP register does not alter the stored event count for the ingress event register index.

11.2.4.2.2.6 Local Event to Global Event Conversion

When enabled, the INTAGGR will provide a set of Local to Global event conversion registers. Local events may be discrete clock synchronous pulses or clock synchronous rising edges. The counting mode is configurable on a 'per pin' basis. In pulsed mode, the module will track how many outstanding clock cycle long pulses have been observed on each of the provided levi interface pins. For each cycle in which a LEVI input pending bit is asserted the corresponding counter will be incremented by 1. In 'rising edge' mode, the number of rising edge transitions on the pin is counted.

The module will generate egress Global events on its egress ETL, with a different global index configured for each ingress LEVI pin. The LEVI pins numbers (1-N) are converted to arbitrary global event indices via the global event mapping LEVI[a]_MAP registers. The egress Global events can themselves be mapped to re-enter the INTAGGR's Global Event Counting block, so that the counts can then be made visible to software in the GEVI count registers as described in Section 10.2.7.3.1.3. The event routing is handled by an external event switch fabric.

11.2.4.2.2.7 Global Event Multicast

In DMSS0_INTAGGR0, the INTAGGR will provide a set of Global event multicast (GEVI[a]_MCMAP) registers. These registers allow an ingress Global event on its ingress ETL interface to be mapped into two egress Global events on two separate egress ETL interfaces. A set of registers map the ingress Global event index (1-N) into two arbitrary egress event indices.

11.2.5 Packet Streaming Interface Link (PSI-L)

This section describes the Packet Streaming Interface Link (PSI-L) for the device.

11.2.5.1 PSI-L Overview

PSI-L is a packet based protocol used to transfer data between several device modules. Each transaction is routed based on thread ID value instead of physical address. All PSI-L interfaces are point to point direct connections to DMSS0. All switching functions among the PSI-L based interfaces are done inside DMSS0.

The PSI-L also has an event interface referred to as ETL, which is purely used to transfer event information.

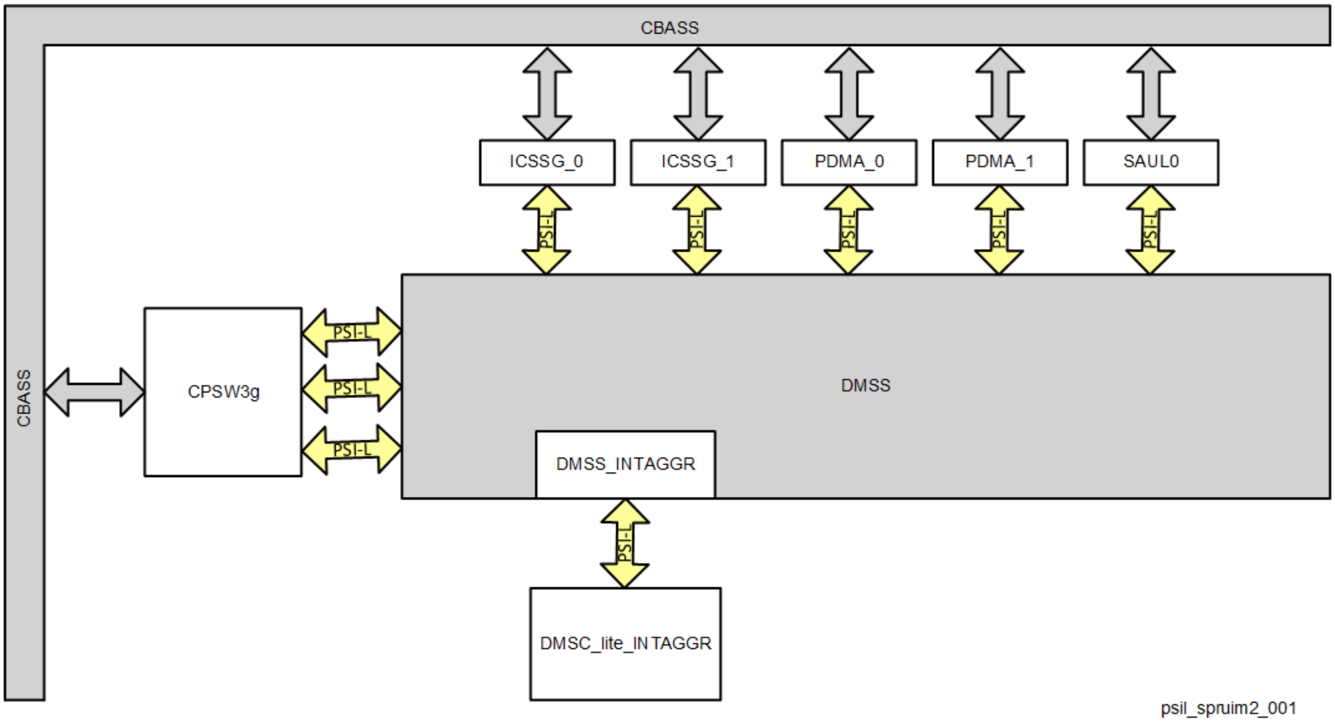

Figure 11-10. PSI-L Overview

11.2.5.2 PSI-L Functional Description

11.2.5.2.1 PSI-L Introduction

The PSI-L is used to transfer words of packet data and control information between two peer entities via direct connection. There are credits used for flow control to guarantee that blocking does not occur between threads. Multiple packet transfers can be ongoing simultaneously across a PSI-L interface each on a separate logical thread but all sharing a single data path through time division multiplexing. Each packet which is transferred is accompanied by a destination thread ID which indicates the logical destination thread to which the packet is being sent.

There is low level hardware handshake between PSI-L initiator and target used for transferring data. As it is blocking by nature, a higher level protocol is also used in which credits are maintained for each thread connection. Moments of non-readiness are allowed on the interface but there is no possibility that one thread can block another for an indefinite time since a thread must have credit for the destination before it is allowed to use the interface.

PSI-L Connection illustrates the point to point PSI-L connection.

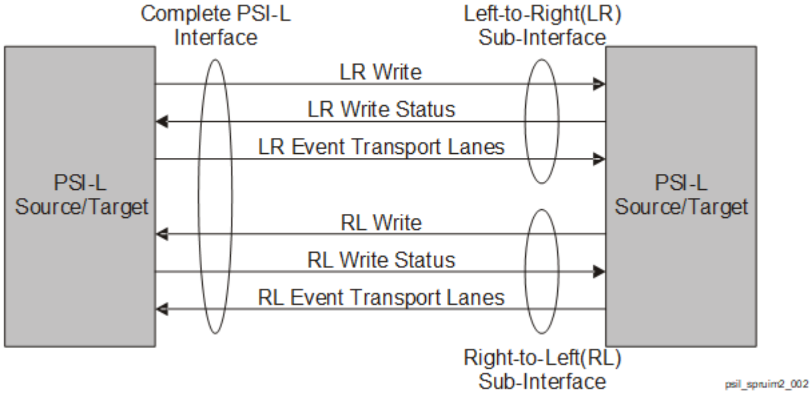

Figure 11-11. PSI-L Connection

PSI-L is intended to be a versatile interface which can carry various types of communications. The following table describes several types of threads which have been defined.

Table 11-75. Types of PSI-L Threads

Type	Description	Example Endpoints
Queue Management (QM) Messaging	Provides transport for queue push, pop, and divert messages to support distributed queue based work passing	Centralized queue manager or message manager and distributed DMA clients
Direct IO	Allows for tunneling CBASS compatible bus transactions through a PSI interconnect	Module which has no CBASS initiator to a remote proxy block
DMA Control Transport	Provides transport for DMA transfer descriptions from a source thread to a destination thread	DMA channel controller to DMA transfer controller
DMA Data Transport	Provides transport for packed data from a source thread to a destination thread	Packet oriented module like networking adapters to or from centralized DMA

Each thread on PSI-L is established between a single thread initiator and a single thread target using a connection oriented transfer mechanism. A thread initiator and a thread target are "paired" to create a logical connection between them referred to as a thread. Pairing is accomplished using a Pair Configuration Message which is valid in all thread types. Pairing can only occur between a thread initiator and a thread target of the same type.

11.2.5.2.2 PSI-L Operation

The PSI-L allows multiple independent streams of packet data (threads) to share a single interface using data phase granularity time division multiplexing. This time division multiplexing is accomplished by dividing each stream into single data transfers. In this way a stream is comprised of a sequence of strongly ordered data transfers but packet transfers between different streams are allowed to be interleaved. Each data phase is qualified with a type identifier which indicates whether the data is packet info, direct IO write or read info, timestamp, software info, control data, payload data, or status.

11.2.5.2.3 Event Transport

PSI-L provides a mechanism by which events can be transported within one or more optional subinterfaces on a link. These sub-interfaces are referred to as event transport lanes (ETLs) and are independent of any PSI-L packet or message transfers which may be ongoing on the other interfaces within the PSI-L. A maximum of one event can be transferred on each event transport lane in each clock cycle. The event transport protocol is a simple request-ready type of hardware handshake.

11.2.5.2.4 Threads

A thread is a complete flow-controlled stream of communication. The PSI-L thread space is divided into a 32K contiguous region representing all of the source threads (0x0000 - 0x7FFF) and a 32K contiguous region representing all of the destination threads (0x8000 - 0x8FFF).

Source threads are responsible for sending request transactions, accepting response transactions, and sending data transfer transactions. Destination threads are responsible for accepting request transactions, sending response transactions, and accepting data transfer transactions. A given thread generally performs only a single class of transactions (see PSI-L Defined Threads). Both source and destination threads may act as initiators for transfers on one of the PSI-L write sub-interfaces but in this case source threads are actually initiating data transfers while destination threads are only responding to a previous request issued by a source request. Source threads only transfer to destination threads and destination threads only transfer to source threads. Transfers between same thread types do not occur.

The following types of message transfers always originate from source threads and terminate in destination threads:

- Configuration write message
- Configuration read message
- QM push message
- QM pop message
- QM divert message
- Direct read operation message
- Direct write operation message
- DMA transfer request message
- DMA data message

The following types of message transfers always originate in destination threads and terminate in source threads:

- Configuration write response message
- Configuration read response message
- QM push response message
- QM pop response message
- QM divert response message
- DMA transfer response message

11.2.5.2.5 Arbitration Protocol

On each cycle, an arbiter built into the initiator side of each interface decides on which thread to transfer data in the next clock cycle. Both forward (from source threads) and reverse (from destination threads) direction transfers can occur across the same physical interface so the arbiter must ensure that sustained blocking of any thread can occur.

The decision about which thread to allow using the interface is based on the following factors:

1. Whether data is ready at the source to be sent
2. Whether credit exists for the thread such that it is guaranteed there is a place for the data to land in the destination endpoint. For reverse direction transfers (response messages), it is assumed that credit always exists.
3. The relative priority of the traffic that the thread is carrying for the given packet duration
4. Whether the transfer is for a forward or reverse direction thread (requests versus responses).

No thread can be considered for inclusion in arbitration unless both data is available and credit exists in the destination endpoint. For each thread which can be considered in the current arbitration cycle, the arbiter should then pick the thread with the highest priority. Reverse transfers should be considered higher priority than forward transfers.

11.2.5.2.6 Thread Configuration

Each source thread has programmable registers for configuring the pairing with a corresponding destination thread and for enabling data flow. Each destination thread has programmable registers for reporting the buffering capability of the thread and for enabling data flow. These registers are accessed using configuration read and write messages from a configuration host.

Each configuration write message sent from a configuration host is acknowledged with a configuration write response message from the addressed endpoint. Each configuration read message sent from a configuration host is acknowledged with a configuration read response message from the addressed endpoint.

11.2.5.2.6.1 Thread Pairing

Depending on the type of traffic that each source thread carries it may or may not have a fixed pairing with a destination thread.

11.2.5.2.6.1.1 Configuration Transaction Pairing

Configuration write and read transactions are only initiated by a special module called configuration proxy (PSILCFG_PROXY). Each configuration proxy in the system uses a single source thread which can initiate configuration write and read transactions to the configuration registers of every other source and destination thread in the PSI-L system. The PSILCFG_PROXY registers are described in *DMASS_PSILCFG_0 Registers*, located in *DMA Controller Registers*.

Each source thread routes to a single target thread and this pairing is specified by programming a required pairing register set for each thread. A source has no ability to change what target thread it talks to. If a source must be able to talk to different targets (or target threads), then it can either have multiple threads or a streaming switch that can be programmed to route the transfers appropriately based on specific packet fields.

11.2.5.2.6.2 Configuration Registers Region

The configuration registers region contains static configuration information including the settings for linking a thread source to a thread destination. These registers are described in *DMA Controller Registers*. The thread ID mapping is shown in *PSI-L System Thread Map*, located in *Module Integration*.

11.3 Peripheral DMA (PDMA)

This chapter describes the PDMA architecture in the device.

11.3.1 PDMA Controller

11.3.1.1 PDMA Overview

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured transfer request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer DMSS destination channel which then performs the movement of the data into memory. Likewise, a remote DMSS source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (DMSS + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

The PDMA is linked to the DMSS through a direct PSI-L connection. For more details, refer to *Packet Streaming Interface Link (PSI-L)*.

11.3.1.1.1 PDMA Features

11.3.1.1.1.1 PDMA0 - SPI Features

The PDMA0 - SPI module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 15 simultaneous destination (Tx) channels
- Supports negative credit monitoring on Tx channels
- Supports up to 15 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transfer modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

11.3.1.1.1.2 PDMA1 - UART Features

The PDMA1 - UART module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 7 simultaneous destination (Tx) channels
- Supports negative credit monitoring on Tx channels
- Supports up to 7 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transter modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

11.3.1.1.1.3 PDMA2 - McASP Features

The PDMA2 - McASP module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (X-Y FIFO transfer mode only)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (X-Y FIFO transfer mode only)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 3 simultaneous destination (Tx) channels
- Supports up to 3 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transter modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

11.3.1.2 Functional Description - SPI

11.3.1.2.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.2.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels in order to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below.

11.3.1.2.2.1 Submodule Descriptions

11.3.1.2.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.2.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.2.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.2.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer will initiate transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.3.1.2.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.2.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.2.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-76.

Table 11-76. Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.2.2.2.2 Clock Stop

The clock stop interface is a request/acknowledge interface used to coordinate the handshaking of properly stopping the main clock to the IP. Before attempting to perform a clock stop operation, software is required to teardown all active channels (via UDMAP 'real time' registers in the UDMAP, or PSIL register 0x408 in PSIL based peripherals), and after this is complete, also clear the global enable bit for all channels (via PSIL register 0x2 in both the UDMAP and PSIL based peripherals). Attempting a clock stop on the IP without first performing the channel teardowns or clearing of global enable bits will result in IP specific behavior that may be UNDEFINED.

The PDMA will not drive clock stop IDLE or clock stop ACK while the global enable (PSIL register 0x2) is set for any channel.

11.3.1.2.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.2.2.2.4 Dynamic Clock Gating

The PDMA includes up to two mid level clock gates using ksdw_pm_clkgate(). One is on the main clock of the PDMA while the other is on the interal ecc_aggr (when RAM is used). These clock gates turn off the clock to their corresponding IP under idle conditions, and then turn the clock back on when work is to be done. Detecting work is done via internal state, or activity on the PSIL or DMA triggers. The DMA triggers are thus always monitored, even when the clocking to the rest of the IP is disabled.

The dynamic clock gating can be disabled through an external port called pwr_disable_nogate. No additional signaling is needed to support the dynamic clock gate, although the PDMA supports the 'early wake' pins on PSIL and VBUSP.

11.3.1.2.2.3 Events and Flow Control

The following sections describe the simplified mechanism that is provided on the Peripheral DMA for triggering.

11.3.1.2.2.3.1 Channel Triggering

Channels must be triggered in order for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, etc.). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2 bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.2.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.2.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.2.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.2.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA will start out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8 byte header on each 64 byte chunk that is transmitted and to remove the header from each 64 byte chunk (other than the first block) that is received.

11.3.1.2.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following addition details apply to the PDMA in AASRC mode:

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps

  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This allows each channel to use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address.

11.3.1.2.2.4 Transmit Operation

11.3.1.2.2.4.1 Destination (Tx) Channel Allocation

A total of 15 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as in the following table.

Table 11-77. Tx Channel Allocation

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	SPI 0 Tx Ch 0	XY	edge	000020100138	000000000000	000000000000
8001	SPI 0 Tx Ch 1	XY	edge	00002010014C	000000000000	000000000000
8002	SPI 0 Tx Ch 2	XY	edge	000020100160	000000000000	000000000000
8003	SPI 0 Tx Ch 3	XY	edge	000020100174	000000000000	000000000000
8004	SPI 1 Tx Ch 0	XY	edge	000020110138	000000000000	000000000000
8005	SPI 1 Tx Ch 1	XY	edge	00002011014C	000000000000	000000000000
8006	SPI 1 Tx Ch 2	XY	edge	000020110160	000000000000	000000000000
8007	SPI 1 Tx Ch 3	XY	edge	000020110174	000000000000	000000000000
8008	SPI 2 Tx Ch 0	XY	edge	000020120138	000000000000	000000000000
8009	SPI 2 Tx Ch 1	XY	edge	00002012014C	000000000000	000000000000
800a	SPI 2 Tx Ch 2	XY	edge	000020120160	000000000000	000000000000
800b	SPI 2 Tx Ch 3	XY	edge	000020120174	000000000000	000000000000
800c	MCAN 0 Tx Ch 0	XY	pulse	000002708000	0000027010D0	000000000000
800d	MCAN 0 Tx Ch 1	XY	pulse	000002708048	0000027010D0	000000000000
800e	MCAN 0 Tx Ch 2	XY	pulse	000002708090	0000027010D0	000000000000

11.3.1.2.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

Table 11-78. Tx Channel Out of Band Signals

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet

Table 11-78. Tx Channel Out of Band Signals (continued)

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.2.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.2.2.4.3.1 PSI-L Destination Thread Pairing Registers

11.3.1.2.2.4.3.1.1 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the TX channel is disabled. When disabled, the channel discards all ingress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.2.2.4.3.1.2 Local Capabilities Register (PSIL Address 0x040)

Bits	Field	Reset	Description
31:29	-	0x0	Reserved.
28:24	LocalThreadWidth	0x2	Read only element width for the local thread used for pairing purposes. This field is encoded as follows: 0 = 4 bytes, 1 = 8 bytes, 2 = 16 bytes.
23:8	-	0x0	Reserved.
7:0	LocalCreditCnt	0x7	Read only local thread free entry count used for pairing purposes.

11.3.1.2.2.4.3.2 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P will send all their data to the destination channel in the PDMA and the destination channel in the PDMA will never see any data other than data from the source channel in the UDMA-P.

11.3.1.2.2.4.3.3 PSI-L Destination Thread Realtime Enable/Count Registers

11.3.1.2.2.4.3.3.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the TX channel is disabled. When disabled, it discards all held data. It clears DMA event counts and ignores all future DMA events from the peripheral. It maintains data exchange with the UDMA-P so that credit handshake is not disrupted. A 'hard teardown' can be performed by directly clearing this bit. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	tdown	0x0	When set, the channel will commence a TX channel teardown procedure. To perform a TX teardown, the teardown bit should be set in the UDMA-P and it will automatically propagate to this register bit with the normal flow of peripheral data. Once the channel is fully stopped and ready to be reused (including returning all credits), the enable bit is cleared.
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume.
28	flush	0x0	When set, causes all TX channel data to be discarded instead of being written to the peripheral. It essentially allows the TX engine to 'free run' without DMA requests from the peripheral (it will also override 'pause'). This bit should be set only when a channel fails to complete its teardown procedure normally, because a peripheral is no longer functioning or because data flow was halted on a boundary that is not compatible with the static TR configuration.
27:3	-	0x0	Reserved.
2	error	0x0	When set, the channel has encountered a PSIL protocol violation. The error bit can only be set by hardware, and can only be cleared by software. Once this bit is set, the channel should be fully reset and re-initialized via the PSIL pairing registers.
1	idle	0x0	This is a read-only bit that signifies that the disabled channel is also idle. This bit is read only and can only become set if the enable bit in the RT enable register is cleared.
0	free	0x0	When cleared, the channel honors the emudbg suspend signal. When set, the channel will free run, regardless of the value of emudbg suspend.

11.3.1.2.2.4.3.3.2 Destination Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been written to the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.2.2.4.3.4 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.2.2.4.3.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.

Param	PSIL Addr	Field	Description
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.4.4 AASRC TxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this TX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.2.2.4.3.4.5 AASRC TxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	TX FIFO Index for slot 7
27:24	Entry6	6	TX FIFO Index for slot 6
23:20	Entry5	5	TX FIFO Index for slot 5
19:16	Entry4	4	TX FIFO Index for slot 4
15:12	Entry3	3	TX FIFO Index for slot 3
11:8	Entry2	2	TX FIFO Index for slot 2
7:4	Entry1	1	TX FIFO Index for slot 1
3:0	Entry0	0	TX FIFO Index for slot 0

11.3.1.2.2.4.3.4.6 AASRC TxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	TX FIFO Index for slot 15
27:24	Entry14	14	TX FIFO Index for slot 14
23:20	Entry13	13	TX FIFO Index for slot 13
19:16	Entry12	12	TX FIFO Index for slot 12
15:12	Entry11	11	TX FIFO Index for slot 11
11:8	Entry10	10	TX FIFO Index for slot 10
7:4	Entry9	9	TX FIFO Index for slot 9
3:0	Entry8	8	TX FIFO Index for slot 8

11.3.1.2.2.4.3.5 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled in order to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.2.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.2.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the Tx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.2.2.4.4.2 MCAN Mode Channel

The PDMA channel will remain idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA will immediately start copying packet bytes into the MCAN TX buffer corresponding the PDMA/ MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA will transfer ownership of the buffer to MCAN by performing an MCAN register write. The PDMA will then wait to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA will continue with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA will skip over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.2.2.4.4.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.2.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.4.5 Transmit PSI-L Interface Transactions

The PDMA will accept data across the Tx PSI-L Interface in accordance with the physical handshaking protocol as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.2.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.2.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel that is paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state will be reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel will be cleared in the PSI-L RT enable register, but the teardown bit will remain high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing will occur until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to guarantee that all data can be properly flushed from the internal pipe.

11.3.1.2.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.2.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in the following table.

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.

Name	PSIL Addr	Field	Description
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.2.2.5 Receive Operation

11.3.1.2.2.5.1 Source (Rx) Channel Allocation

A total of 15 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as in Table 11-79.

Table 11-79. Rx Channel Allocation

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	SPI 0 Rx Ch 0	XY	edge	00002010013C	000000000000	000000000000
1	SPI 0 Rx Ch 1	XY	edge	000020100150	000000000000	000000000000
2	SPI 0 Rx Ch 2	XY	edge	000020100164	000000000000	000000000000
3	SPI 0 Rx Ch 3	XY	edge	000020100178	000000000000	000000000000
4	SPI 1 Rx Ch 0	XY	edge	00002011013C	000000000000	000000000000
5	SPI 1 Rx Ch 1	XY	edge	000020110150	000000000000	000000000000
6	SPI 1 Rx Ch 2	XY	edge	000020110164	000000000000	000000000000
7	SPI 1 Rx Ch 3	XY	edge	000020110178	000000000000	000000000000
8	SPI 2 Rx Ch 0	XY	edge	00002012013C	000000000000	000000000000
9	SPI 2 Rx Ch 1	XY	edge	000020120150	000000000000	000000000000
10	SPI 2 Rx Ch 2	XY	edge	000020120164	000000000000	000000000000
11	SPI 2 Rx Ch 3	XY	edge	000020120178	000000000000	000000000000
12	MCAN 0 Rx Ch 0	XY	pulse	000002708900	000002701098	000000000000
13	MCAN 0 Rx Ch 1	XY	pulse	000002708990	000002701098	000000000000
14	MCAN 0 Rx Ch 2	XY	pulse	000002708A20	000002701098	000000000000

11.3.1.2.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.2.2.5.2.1 PSI-L Source Thread Pairing Registers

11.3.1.2.2.5.2.1.1 Peer Thread ID Register (PSIL Address 0x000)

Bits	Field	Reset	Description
31:29	ThreadPriority	0x0	This field is hard coded to 0x0 and is not writable
28:24	PeerThreadWidth	0x0	Datapath width of paired peer destination thread. This field is encoded as follows: 0 = 32-bit, 1 = 64-bit, 2 = 128 bit, 3 = 256 bit, 4 = 512 bit
23:16	-	0x0	Reserved.
15:0	Peer ThreadID	0x0	Thread ID to which all non-Transfer Response, non-Config messages from this thread will be sent.

11.3.1.2.2.5.2.1.2 Peer Credit Register (PSIL Address 0x001)

Bits	Field	Reset	Description
31:8	-	0x0	Reserved.
7:0	CreditCnt	0x0	Free entries in destination thread. Legal range is 0 - 128 in number of elements.

11.3.1.2.2.5.2.1.3 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.2.2.5.2.2 PSI-L Source Thread Realtime Enable/Count Registers

11.3.1.2.2.5.2.2.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all DMA events from the peripheral. It maintains proper data transfers with the UDMA-P such that the credit handshake is not disrupted. However, unlike teardown, it does not close out the current open packet. Thus the teardown bit should always be used to disable an RX channel instead of manually clearing this bit. Failing to use teardown may result in stale data remaining in the internal RX FIFO, which would also prevent the channel from going idle without a channel reset. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.

Bits	Field	Reset	Description
30	tdown	0x0	When set, the channel will commence a RX channel teardown procedure. It will stop on the next FIFO boundary. It then clears the DMA event count and ignores all future DMA events from the peripheral. After stopping peripheral reads, the PDMA sends a teardown message to the UDMA-P that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP. The EOP teardown message may or may not contain final packet data. Once the channel teardown is complete and ready to be reused, the enable bit is cleared.
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume. Pause will not stop teardown from completing.
28:2	-	0x0	Reserved.
1	idle	0x0	This is a read-only bit that signifies that the Paused or Disabled channel is also idle. This bit is read only and can only become set if pause is set or enable is cleared.
0	free	0x0	Free Run: 0 = channel honors the emudbg suspend signal, 1 = channel will free run, regardless of the value of emudbg suspend.

11.3.1.2.2.5.2.2.2 Source Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.2.2.5.2.3 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA will send all their data to the source channel in the UDMA-P and the destination channel in the UDMA-P will never see any data other than data from the source channel in the PDMA.

11.3.1.2.2.5.2.4 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.2.2.5.2.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.2.2.5.2.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.

Param	PSIL Addr	Field	Description
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.2.2.5.2.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.2.2.5.2.4.4 AASRC RxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this RX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.

Bits	Field	Reset	Description
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.2.2.5.2.4.5 AASRC RxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	RX FIFO Index for slot 7
27:24	Entry6	6	RX FIFO Index for slot 6
23:20	Entry5	5	RX FIFO Index for slot 5
19:16	Entry4	4	RX FIFO Index for slot 4
15:12	Entry3	3	RX FIFO Index for slot 3
11:8	Entry2	2	RX FIFO Index for slot 2
7:4	Entry1	1	RX FIFO Index for slot 1
3:0	Entry0	0	RX FIFO Index for slot 0

11.3.1.2.2.5.2.4.6 AASRC RxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	RX FIFO Index for slot 15

Bits	Field	Reset	Description
27:24	Entry14	14	RX FIFO Index for slot 14
23:20	Entry13	13	RX FIFO Index for slot 13
19:16	Entry12	12	RX FIFO Index for slot 12
15:12	Entry11	11	RX FIFO Index for slot 11
11:8	Entry10	10	RX FIFO Index for slot 10
7:4	Entry9	9	RX FIFO Index for slot 9
3:0	Entry8	8	RX FIFO Index for slot 8

11.3.1.2.2.5.2.5 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.2.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.2.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.2.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.2.2.5.3.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.2.2.5.3.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.2.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer will be initiated for that channel/thread on the Rx PSI-L interface and the data will be popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.2.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.2.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA will not stop reading peripheral data until it reaches a FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. It will always attempt to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA will then clear the enable bit in the pairing register, however the teardown bit will remain set. No further packet processing will occur until the Host re-configures the channel. The teardown process will propagate to the UDMA-P and its final status can be checked there.

11.3.1.2.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.2.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as follows.

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.

Name	PSIL Addr	Field	Description
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.3 Functional Description - UART

11.3.1.3.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.3.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels in order to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below.

11.3.1.3.2.1 Submodule Descriptions

11.3.1.3.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.3.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.3.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.3.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer will initiate transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.3.1.3.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.3.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.3.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-80.

Table 11-80. Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.3.2.2.2 Clock Stop

The clock stop interface is a request/acknowledge interface used to coordinate the handshaking of properly stopping the main clock to the IP. Before attempting to perform a clock stop operation, software is required to teardown all active channels (via UDMAP 'real time' registers in the UDMAP, or PSIL register 0x408 in PSIL based peripherals), and after this is complete, also clear the global enable bit for all channels (via PSIL register 0x2 in both the UDMAP and PSIL based peripherals). Attempting a clock stop on the IP without first performing the channel teardowns or clearing of global enable bits will result in IP specific behavior that may be UNDEFINED.

The PDMA will not drive clock stop IDLE or clock stop ACK while the global enable (PSIL register 0x2) is set for any channel.

11.3.1.3.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.3.2.2.4 Dynamic Clock Gating

The PDMA includes up to two mid level clock gates using ksdw_pm_clkgate(). One is on the main clock of the PDMA while the other is on the interal ecc_aggr (when RAM is used). These clock gates turn off the clock to their corresponding IP under idle conditions, and then turn the clock back on when work is to be done. Detecting work is done via internal state, or activity on the PSIL or DMA triggers. The DMA triggers are thus always monitored, even when the clocking to the rest of the IP is disabled.

The dynamic clock gating can be disabled through an external port called pwr_disable_nogate. No additional signaling is needed to support the dynamic clock gate, although the PDMA supports the 'early wake' pins on PSIL and VBUSP.

11.3.1.3.2.3 Events and Flow Control

The following sections describe the simplified mechanism that is provided on the Peripheral DMA for triggering.

11.3.1.3.2.3.1 Channel Triggering

Channels must be triggered in order for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, etc.). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2 bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.3.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.3.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.3.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.3.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA will start out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8 byte header on each 64 byte chunk that is transmitted and to remove the header from each 64 byte chunk (other than the first block) that is received.

11.3.1.3.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following addition details apply to the PDMA in AASRC mode:

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This allows each channel to use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address.

11.3.1.3.2.4 Transmit Operation

11.3.1.3.2.4.1 Destination (Tx) Channel Allocation

A total of 7 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as shown in Table 11-81.

Table 11-81. Tx Channel Allocation

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	USART 0 Tx Ch 0	XY	edge	000002800000	000000000000	000000000000
8001	USART 1 Tx Ch 0	XY	edge	000002810000	000000000000	000000000000
8002	USART 2 Tx Ch 0	XY	edge	000002820000	000000000000	000000000000
8003	USART 3 Tx Ch 0	XY	edge	000002830000	000000000000	000000000000
8004	USART 4 Tx Ch 0	XY	edge	000002840000	000000000000	000000000000
8005	USART 5 Tx Ch 0	XY	edge	000002850000	000000000000	000000000000

Table 11-81. Tx Channel Allocation (continued)

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8006	USART 6 Tx Ch 0	XY	edge	000002860000	000000000000	000000000000

11.3.1.3.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

Table 11-82. Tx Channel Out of Band Signals

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.3.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.3.2.4.3.1 PSI-L Destination Thread Pairing Registers

11.3.1.3.2.4.3.1.1 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.3.2.4.3.1.2 Local Capabilities Register (PSIL Address 0x040)

Bits	Field	Reset	Description
31:29	-	0x0	Reserved.
28:24	LocalThreadWidth	0x2	Read only element width for the local thread used for pairing purposes. This field is encoded as follows: 0 = 4 bytes, 1 = 8 bytes, 2 = 16 bytes.
23:8	-	0x0	Reserved.
7:0	LocalCreditCnt	0x7	Read only local thread free entry count used for pairing purposes.

11.3.1.3.2.4.3.2 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P will send all their data to the destination channel in the PDMA and the destination channel in the PDMA will never see any data other than data from the source channel in the UDMA-P.

11.3.1.3.2.4.3.3 PSI-L Destination Thread Realtime Enable/Count Registers

11.3.1.3.2.4.3.3.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the TX channel is disabled. When disabled, it discards all held data. It clears DMA event counts and ignores all future DMA events from the peripheral. It maintains data exchange with the UDMA-P so that credit handshake is not disrupted. A 'hard teardown' can be performed by directly clearing this bit. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	tdown	0x0	When set, the channel will commence a TX channel teardown procedure. To perform a TX teardown, the teardown bit should be set in the UDMA-P and it will automatically propagate to this register bit with the normal flow of peripheral data. Once the channel is fully stopped and ready to be reused (including returning all credits), the enable bit is cleared.
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume.
28	flush	0x0	When set, causes all TX channel data to be discarded instead of being written to the peripheral. It essentially allows the TX engine to 'free run' without DMA requests from the peripheral (it will also override 'pause'). This bit should be set only when a channel fails to complete its teardown procedure normally, because a peripheral is no longer functioning or because data flow was halted on a boundary that is not compatible with the static TR configuration.
27:3	-	0x0	Reserved.
2	error	0x0	When set, the channel has encountered a PSIL protocol violation. The error bit can only be set by hardware, and can only be cleared by software. Once this bit is set, the channel should be fully reset and re-initialized via the PSIL pairing registers.
1	idle	0x0	This is a read-only bit that signifies that the disabled channel is also idle. This bit is read only and can only become set if the enable bit in the RT enable register is cleared.
0	free	0x0	When cleared, the channel honors the emudbg suspend signal. When set, the channel will free run, regardless of the value of emudbg suspend.

11.3.1.3.2.4.3.3.2 Destination Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been written to the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.3.2.4.3.4 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.3.2.4.3.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.4.4 AASRC TxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this TX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Bits	Field	Reset	Description
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.3.2.4.3.4.5 AASRC TxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	TX FIFO Index for slot 7
27:24	Entry6	6	TX FIFO Index for slot 6
23:20	Entry5	5	TX FIFO Index for slot 5
19:16	Entry4	4	TX FIFO Index for slot 4
15:12	Entry3	3	TX FIFO Index for slot 3
11:8	Entry2	2	TX FIFO Index for slot 2
7:4	Entry1	1	TX FIFO Index for slot 1
3:0	Entry0	0	TX FIFO Index for slot 0

11.3.1.3.2.4.3.4.6 AASRC TxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	TX FIFO Index for slot 15
27:24	Entry14	14	TX FIFO Index for slot 14
23:20	Entry13	13	TX FIFO Index for slot 13
19:16	Entry12	12	TX FIFO Index for slot 12
15:12	Entry11	11	TX FIFO Index for slot 11
11:8	Entry10	10	TX FIFO Index for slot 10
7:4	Entry9	9	TX FIFO Index for slot 9
3:0	Entry8	8	TX FIFO Index for slot 8

11.3.1.3.2.4.3.5 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled in order to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.3.2.4.4 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.3.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.3.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.3.2.4.4.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used

CAN FE2	CAN FE1	CAN FE0	Description
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.3.2.4.4.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.2.4.5 Transmit PSI-L Interface Transactions

The PDMA will accept data across the Tx PSI-L Interface in accordance with the physical handshaking protocol as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.

Pin	Output Value / Source From PDMA
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.3.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.3.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel that is paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state will be reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel will be cleared in the PSI-L RT enable register, but the teardown bit will remain high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing will occur until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to guarantee that all data can be properly flushed from the internal pipe.

11.3.1.3.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in the following table.

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.

Name	PSIL Addr	Field	Description
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.3.2.5 Receive Operation

11.3.1.3.2.5.1 Source (Rx) Channel Allocation

A total of 7 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as shown in Table 11-83.

Table 11-83. Rx Channel Allocation

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	USART 0 Rx Ch 0	XY	edge	000002800000	000000000000	000000000000
1	USART 1 Rx Ch 0	XY	edge	000002810000	000000000000	000000000000
2	USART 2 Rx Ch 0	XY	edge	000002820000	000000000000	000000000000
3	USART 3 Rx Ch 0	XY	edge	000002830000	000000000000	000000000000
4	USART 4 Rx Ch 0	XY	edge	000002840000	000000000000	000000000000
5	USART 5 Rx Ch 0	XY	edge	000002850000	000000000000	000000000000
6	USART 6 Rx Ch 0	XY	edge	000002860000	000000000000	000000000000

11.3.1.3.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.3.2.5.2.1 PSI-L Source Thread Pairing Registers

11.3.1.3.2.5.2.1.1 Peer Thread ID Register (PSIL Address 0x000)

Bits	Field	Reset	Description
31:29	ThreadPriority	0x0	This field is hard coded to 0x0 and is not writable
28:24	PeerThreadWidth	0x0	Datapath width of paired peer destination thread. This field is encoded as follows: 0 = 32-bit, 1 = 64-bit, 2 = 128 bit, 3 = 256 bit, 4 = 512 bit
23:16	-	0x0	Reserved.
15:0	Peer ThreadID	0x0	Thread ID to which all non-Transfer Response, non-Config messages from this thread will be sent.

11.3.1.3.2.5.2.1.2 Peer Credit Register (PSIL Address 0x001)

Bits	Field	Reset	Description
31:8	-	0x0	Reserved.

Bits	Field	Reset	Description
7:0	CreditCnt	0x0	Free entries in destination thread. Legal range is 0 - 128 in number of elements.

11.3.1.3.2.5.2.1.3 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.3.2.5.2.2 PSI-L Source Thread Realtime Enable/Count Registers

11.3.1.3.2.5.2.2.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all DMA events from the peripheral. It maintains proper data transfers with the UDMA-P such that the credit handshake is not disrupted. However, unlike teardown, it does not close out the current open packet. Thus the teardown bit should always be used to disable an RX channel instead of manually clearing this bit. Failing to use teardown may result in stale data remaining in the internal RX FIFO, which would also prevent the channel from going idle without a channel reset. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	tdown	0x0	When set, the channel will commence a RX channel teardown procedure. It will stop on the next FIFO boundary. It then clears the DMA event count and ignores all future DMA events from the peripheral. After stopping peripheral reads, the PDMA sends a teardown message to the UDMA-P that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP. The EOP teardown message may or may not contain final packet data. Once the channel teardown is complete and ready to be reused, the enable bit is cleared.

Bits	Field	Reset	Description
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume. Pause will not stop teardown from completing.
28:2	-	0x0	Reserved.
1	idle	0x0	This is a read-only bit that signifies that the Paused or Disabled channel is also idle. This bit is read only and can only become set if pause is set or enable is cleared.
0	free	0x0	Free Run: 0 = channel honors the emudbg suspend signal, 1 = channel will free run, regardless of the value of emudbg suspend.

11.3.1.3.2.5.2.2.2 Source Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.3.2.5.2.3 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA will send all their data to the source channel in the UDMA-P and the destination channel in the UDMA-P will never see any data other than data from the source channel in the PDMA.

11.3.1.3.2.5.2.4 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.3.2.5.2.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED

Param	PSIL Addr	Field	Description
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.3.2.5.2.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.3.2.5.2.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.

Param	PSIL Addr	Field	Description
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.3.2.5.2.4.4 AASRC RxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this RX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Bits	Field	Reset	Description
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.3.2.5.2.4.5 AASRC RxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	RX FIFO Index for slot 7
27:24	Entry6	6	RX FIFO Index for slot 6
23:20	Entry5	5	RX FIFO Index for slot 5
19:16	Entry4	4	RX FIFO Index for slot 4
15:12	Entry3	3	RX FIFO Index for slot 3
11:8	Entry2	2	RX FIFO Index for slot 2
7:4	Entry1	1	RX FIFO Index for slot 1
3:0	Entry0	0	RX FIFO Index for slot 0

11.3.1.3.2.5.2.4.6 AASRC RxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	RX FIFO Index for slot 15
27:24	Entry14	14	RX FIFO Index for slot 14
23:20	Entry13	13	RX FIFO Index for slot 13
19:16	Entry12	12	RX FIFO Index for slot 12
15:12	Entry11	11	RX FIFO Index for slot 11
11:8	Entry10	10	RX FIFO Index for slot 10
7:4	Entry9	9	RX FIFO Index for slot 9
3:0	Entry8	8	RX FIFO Index for slot 8

11.3.1.3.2.5.2.5 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.3.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.3.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.3.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.3.2.5.3.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used

CAN FE2	CAN FE1	CAN FE0	Description
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.3.2.5.3.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer will be initiated for that channel/thread on the Rx PSI-L interface and the data will be popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.3.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.3.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA will not stop reading peripheral data until it reaches a FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. It will always attempt to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA will then clear the enable bit in the pairing register, however the teardown bit will remain set. No further packet processing will occur until the Host re-configures the channel. The teardown process will propagate to the UDMA-P and its final status can be checked there.

11.3.1.3.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as follows.

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.4 Functional Description - McASP

11.3.1.4.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.4.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA, which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below:

11.3.1.4.2.1 Submodule Descriptions

11.3.1.4.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.4.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.4.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.4.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block, which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer initiates transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block simultaneously monitors the status of all of the threads and performs a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer is included in the arbitration.

11.3.1.4.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.4.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.4.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-84.

Table 11-84. PDMA Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.4.2.2.2 Clock Stop

The clock stop interface is used to instruct the PDMA to stop issuing commands on its external interfaces. Note that the PDMA will report a clock stop idle if all its DMA channels have been previously disabled by software using the enable bit in PSIL register 2 for each channel.

11.3.1.4.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.4.2.3 Events and Flow Control

The following sections describe the simplified mechanism provided on the Peripheral DMA for triggering.

11.3.1.4.2.3.1 Channel Triggering

Channels must be triggered for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, and so forth). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2-bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.4.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.4.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.4.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.4.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA starts out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8-byte header on each 64-byte chunk that is transmitted and to remove the header from each 64-byte chunk (other than the first block) that is received.

11.3.1.4.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following additional details apply to the PDMA in AASRC mode.

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This lets each channel use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address

11.3.1.4.2.4 Transmit Operation

11.3.1.4.2.4.1 Destination (Tx) Channel Allocation

A total of 3 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as follows:

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	McASP 0 Tx Ch 0	XY	edge	000002B08000	000000000000	000000000000
8001	McASP 1 Tx Ch 0	XY	edge	000002B18000	000000000000	000000000000
8002	McASP 2 Tx Ch 0	XY	edge	000002B28000	000000000000	000000000000

11.3.1.4.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.4.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA is idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.4.2.4.3.1 PSI-L Destination Thread Pairing Registers

11.3.1.4.2.4.3.1.1 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the TX channel is disabled. When disabled, the channel discards all ingress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.4.2.4.3.1.2 Peer Credit Register (PSIL Address 0x040)

Bits	Field	Reset	Description
31:29	-	0x0	Reserved.
28:24	LocalThreadWidth	0x2	Read only element width for the local thread used for pairing purposes. This field is encoded as follows: 0 = 4 bytes, 1 = 8 bytes, 2 = 16 bytes.
23:8	-	0x0	Reserved.
7:0	LocalCreditCnt	0x8	Read only local thread free entry count used for pairing purposes.

11.3.1.4.2.4.3.2 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P send all their data to the destination channel in the PDMA, and the destination channel in the PDMA never sees any data other than data from the source channel in the UDMA-P.

11.3.1.4.2.4.3.3 PSI-L Destination Thread Realtime Enable/Count Registers

11.3.1.4.2.4.3.3.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the TX channel is disabled. When disabled, it discards all held data. It clears DMA event counts and ignores all future DMA events from the peripheral. It maintains data exchange with the UDMA-P so that credit handshake is not disrupted. A 'hard teardown' can be performed by directly clearing this bit. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	tdown	0x0	When set, the channel will commence a TX channel teardown procedure. To perform a TX teardown, the teardown bit should be set in the UDMA-P and it will automatically propagate to this register bit with the normal flow of peripheral data. Once the channel is fully stopped and ready to be reused (including returning all credits), the enable bit is cleared.
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume.
28	flush	0x0	When set, causes all TX channel data to be discarded instead of being written to the peripheral. It essentially allows the TX engine to 'free run' without DMA requests from the peripheral (it will also override 'pause'). This bit should be set only when a channel fails to complete its teardown procedure normally, because a peripheral is no longer functioning or because data flow was halted on a boundary that is not compatible with the static TR configuration.
27:3	-	0x0	Reserved.
2	error	0x0	When set, the channel has encountered a PSIL protocol violation. The error bit can only be set by hardware, and can only be cleared by software. Once this bit is set, the channel should be fully reset and re-initialized via the PSIL pairing registers.
1	idle	0x0	This is a read-only bit that signifies that the disabled channel is also idle. This bit is read only and can only become set if the enable bit in the RT enable register is cleared.

Bits	Field	Reset	Description
0	free	0x0	When cleared, the channel honors the emudbg suspend signal. When set, the channel will free run, regardless of the value of emudbg suspend.

11.3.1.4.2.4.3.3.2 Destination Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been written to the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.4.2.4.3.4 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.4.2.4.3.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.

Param	PSIL Addr	Field	Description
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.4.4 AASRC TxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this TX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Bits	Field	Reset	Description
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.4.2.4.3.4.5 AASRC TxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	TX FIFO Index for slot 7
27:24	Entry6	6	TX FIFO Index for slot 6
23:20	Entry5	5	TX FIFO Index for slot 5
19:16	Entry4	4	TX FIFO Index for slot 4
15:12	Entry3	3	TX FIFO Index for slot 3
11:8	Entry2	2	TX FIFO Index for slot 2
7:4	Entry1	1	TX FIFO Index for slot 1
3:0	Entry0	0	TX FIFO Index for slot 0

11.3.1.4.2.4.3.4.6 AASRC TxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	TX FIFO Index for slot 15
27:24	Entry14	14	TX FIFO Index for slot 14
23:20	Entry13	13	TX FIFO Index for slot 13
19:16	Entry12	12	TX FIFO Index for slot 12
15:12	Entry11	11	TX FIFO Index for slot 11
11:8	Entry10	10	TX FIFO Index for slot 10
7:4	Entry9	9	TX FIFO Index for slot 9
3:0	Entry8	8	TX FIFO Index for slot 8

11.3.1.4.2.4.3.5 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.4.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.4.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible given availability of data in the Tx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address increments throughout the burst
- Bursts are sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.4.2.4.4.2 MCAN Mode Channel

The PDMA channel remains idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA immediately starts copying packet bytes into the MCAN TX buffer corresponding the PDMA/MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA transfers ownership of the buffer to MCAN by performing an MCAN register write. The PDMA then waits to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA continues with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA skips over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.4.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible, given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.4.5 Transmit PSI-L Interface Transactions

The PDMA accepts data across the Tx PSI-L Interface in accordance with the physical handshaking protocol, as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.4.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.4.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state is reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel is cleared in the PSI-L RT enable register, but the teardown bit remains high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing occurs until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to ensure that all data can be properly flushed from the internal pipe.

11.3.1.4.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.4.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in Table 11-85.

Table 11-85. Tx Debug/State Register

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.4.2.5 Receive Operation

11.3.1.4.2.5.1 Source (Rx) Channel Allocation

A total of 3 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as follows.

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	McASP 0 Rx Ch 0	XY	edge	000002B08000	000000000000	000000000000
1	McASP 1 Rx Ch 0	XY	edge	000002B18000	000000000000	000000000000
2	McASP 2 Rx Ch 0	XY	edge	000002B28000	000000000000	000000000000

11.3.1.4.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.4.2.5.2.1 PSI-L Source Thread Pairing Registers

11.3.1.4.2.5.2.1.1 Peer Thread ID Register (PSIL Address 0x000)

Bits	Field	Reset	Description
31:29	ThreadPriority	0x0	This field is hard coded to 0x0 and is not writable
28:24	PeerThreadWidth	0x0	Datapath width of paired peer destination thread. This field is encoded as follows: 0 = 32-bit, 1 = 64-bit, 2 = 128 bit, 3 = 256 bit, 4 = 512 bit
23:16	-	0x0	Reserved.
15:0	Peer ThreadID	0x0	Thread ID to which all non-Transfer Response, non-Config messages from this thread will be sent.

11.3.1.4.2.5.2.1.2 Peer Credit Register (PSIL Address 0x001)

Bits	Field	Reset	Description
31:8	-	0x0	Reserved.
7:0	CreditCnt	0x0	Free entries in destination thread. Legal range is 0 - 128 in number of elements.

11.3.1.4.2.5.2.1.3 Enable Register (PSIL Address 0x002)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one to zero transition on this bit fully resets the channel.
30:0	-	0x0	Reserved.

11.3.1.4.2.5.2.2 PSI-L Source Thread Realtime Enable/Count Registers

11.3.1.4.2.5.2.2.1 RT Enable Register (PSIL Address 0x408)

Bits	Field	Reset	Description
31	enable	0x0	When set, the channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all DMA events from the peripheral. It maintains proper data transfers with the UDMA-P such that the credit handshake is not disrupted. However, unlike teardown, it does not close out the current open packet. Thus the teardown bit should always be used to disable an RX channel instead of manually clearing this bit. Failing to use teardown may result in stale data remaining in the internal RX FIFO, which would also prevent the channel from going idle without a channel reset. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.

Bits	Field	Reset	Description
30	tdown	0x0	When set, the channel will commence a RX channel teardown procedure. It will stop on the next FIFO boundary. It then clears the DMA event count and ignores all future DMA events from the peripheral. After stopping peripheral reads, the PDMA sends a teardown message to the UDMA-P that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP. The EOP teardown message may or may not contain final packet data. Once the channel teardown is complete and ready to be reused, the enable bit is cleared.
29	pause	0x0	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals, but will not act on them. The pause bit can be cleared and data will resume. Pause will not stop teardown from completing.
28:2	-	0x0	Reserved.
1	idle	0x0	This is a read-only bit that signifies that the Paused or Disabled channel is also idle. This bit is read only and can only become set if pause is set or enable is cleared.
0	free	0x0	Free Run: 0 = channel honors the emudbg suspend signal, 1 = channel will free run, regardless of the value of emudbg suspend.

11.3.1.4.2.5.2.2.2 Source Thread Byte Count Register (PSIL Address 0x404)

Bits	Field	Reset	Description
31:0	bytes	0x0	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write to decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

11.3.1.4.2.5.2.3 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA send all their data to the source channel in the UDMA-P, and the destination channel in the UDMA-P never sees any data other than data from the source channel in the PDMA.

11.3.1.4.2.5.2.4 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.4.2.5.2.4.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.

Param	PSIL Addr	Field	Description
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.4.2.5.2.4.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.4.2.5.2.4.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.

Param	PSIL Addr	Field	Description
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.4.2.5.2.4.4 AASRC RxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this RX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.4.2.5.2.4.5 AASRC RxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	RX FIFO Index for slot 7
27:24	Entry6	6	RX FIFO Index for slot 6
23:20	Entry5	5	RX FIFO Index for slot 5
19:16	Entry4	4	RX FIFO Index for slot 4
15:12	Entry3	3	RX FIFO Index for slot 3
11:8	Entry2	2	RX FIFO Index for slot 2
7:4	Entry1	1	RX FIFO Index for slot 1
3:0	Entry0	0	RX FIFO Index for slot 0

11.3.1.4.2.5.2.4.6 AASRC RxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	RX FIFO Index for slot 15
27:24	Entry14	14	RX FIFO Index for slot 14
23:20	Entry13	13	RX FIFO Index for slot 13
19:16	Entry12	12	RX FIFO Index for slot 12
15:12	Entry11	11	RX FIFO Index for slot 11
11:8	Entry10	10	RX FIFO Index for slot 10
7:4	Entry9	9	RX FIFO Index for slot 9
3:0	Entry8	8	RX FIFO Index for slot 8

11.3.1.4.2.5.2.5 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.4.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what happens for the different channel types.

11.3.1.4.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the Rx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.4.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. For example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts are sub-divided to fit into a 64-byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.4.2.5.3.2 MCAN Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA starts copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN skips the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example, the following two filter entries set up a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0.

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.4.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the TX channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer is initiated for that channel/thread on the Rx PSI-L interface, and the data is popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in Table 11-86.

Table 11-86. PSI-L Interface Output Pins

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.

Table 11-86. PSI-L Interface Output Pins (continued)

Pin	Output Value / Source From PDMA
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.4.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.4.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA does not stop reading peripheral data until it reaches a FIFO boundary, as configured through the 'X' and 'Y' parameters in the static TR. It always attempts to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA then clears the enable bit in the pairing register; however, the teardown bit remains set. No further packet processing occurs until the Host re-configures the channel. The teardown process propagates to the UDMA-P and its final status can be checked there.

11.3.1.4.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.4.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as in Table 11-87.

Table 11-87. Rx Debug/State Register

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.

Table 11-87. Rx Debug/State Register (continued)

Name	PSIL Addr	Field	Description
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

Chapter 12

Peripherals

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12.1 Audio Peripherals

12.1.1 Multichannel Audio Serial Port (MCASP)

This section describes the Multichannel Audio Serial Port (MCASP).

12.1.1.1 MCASP Overview

This section introduces the Multichannel Audio Serial Port (MCASP) module and describes its main functions and connections in the device.

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

Figure 12-1 shows the MCASP modules overview.

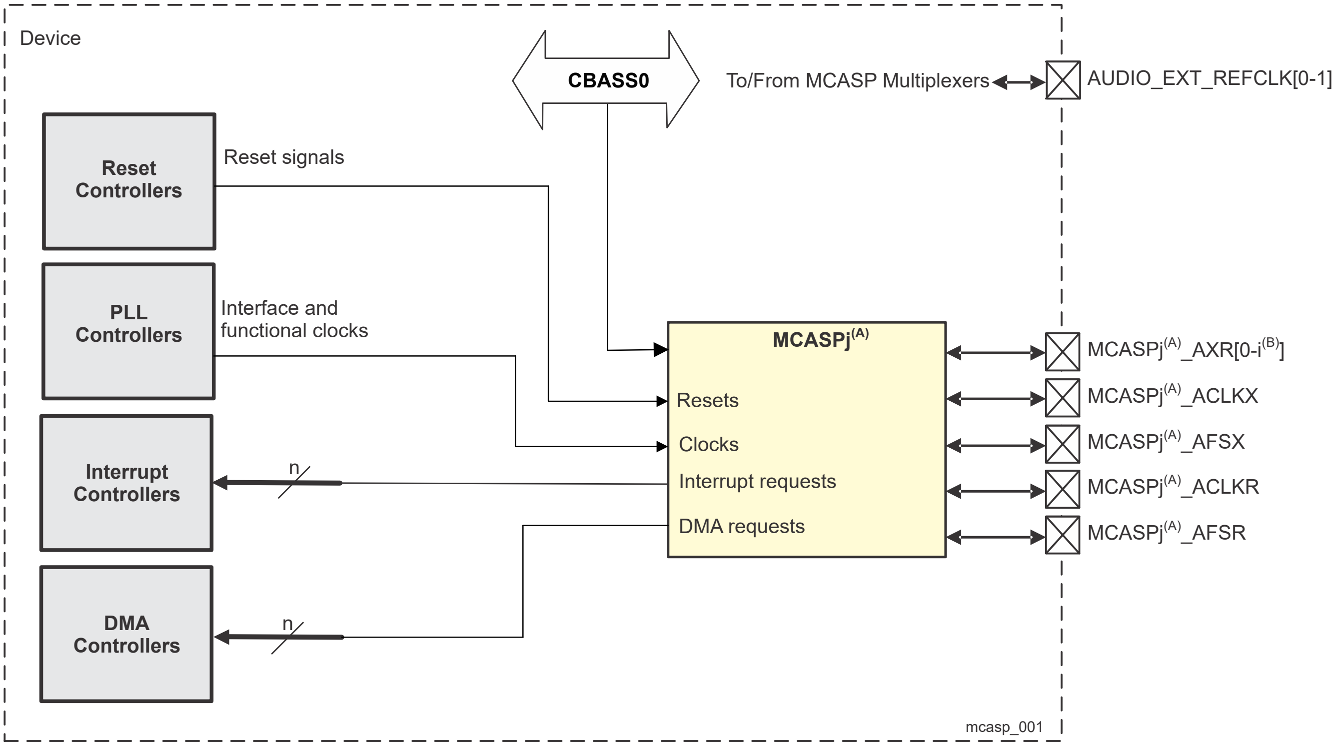

Note

j represents a valid instance of MCASP in a domain

Note

i represents the maximum number of MCASPj_AXR signals - 1.

Figure 12-1. MCASP Modules Overview

12.1.1.1.1 MCASP Features

Each MCASP module includes the following main features:

- Independent serializer for each AXRx channel of each MCASP module

- Clock stop request/acknowledge protocol
- A single 32-bit buffer per serializer for transmit and receive operations
- Interconnect interface port for CBASS0
- Two independent clock generator modules for transmit and receive (clocking flexibility allows the MCASP to receive and transmit at different rates. For example, the MCASP can receive data at 48 kHz, but output up-sampled data at 96 kHz or 192 kHz)
- Each MCASP module functional clock can be generated:
  - Internally (controller mode)
  - Supplied over MCASP serial interface (target mode)
  - Has a controllable functional clock divide ratio
- Independent transmit and receive modules, each includes:
  - Programmable clock and frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Glueless connection to audio Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT):
  - S/PDIF, IEC60958-1, AES-3 formats
  - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
  - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the MCASP receive section
- Support for 2 × DMA requests (one per direction):
  - 1 level-sensitive transmit direct memory access (DMA) request common for all of the MCASP serializers
  - 1 level-sensitive receive direct memory access (DMA) request common for all of the MCASP serializers
  - All transmit DMA requests are mapped to the device DMA controllers
- One transmit interrupt request common for all serializers
- One receive interrupt request common for all serializers
- Each of the Rx and Tx interrupts is propagated to different host processors via the device Interrupts

Note

Because a serializer receive and transmit channels data is shared on the same MCASP data pin, user can choose to have either Tx or Rx function from a serializer, not both at the same time.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.1.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

12.1.1.2 MCASP Environment

This section describes the MCASP application fields from an environment point of view (external connections). This section also lists the possible interfaces and describes the protocol and data format used in each case.

12.1.1.2.1 MCASP Signals

Figure 12-2 shows all of the MCASP interface signals.

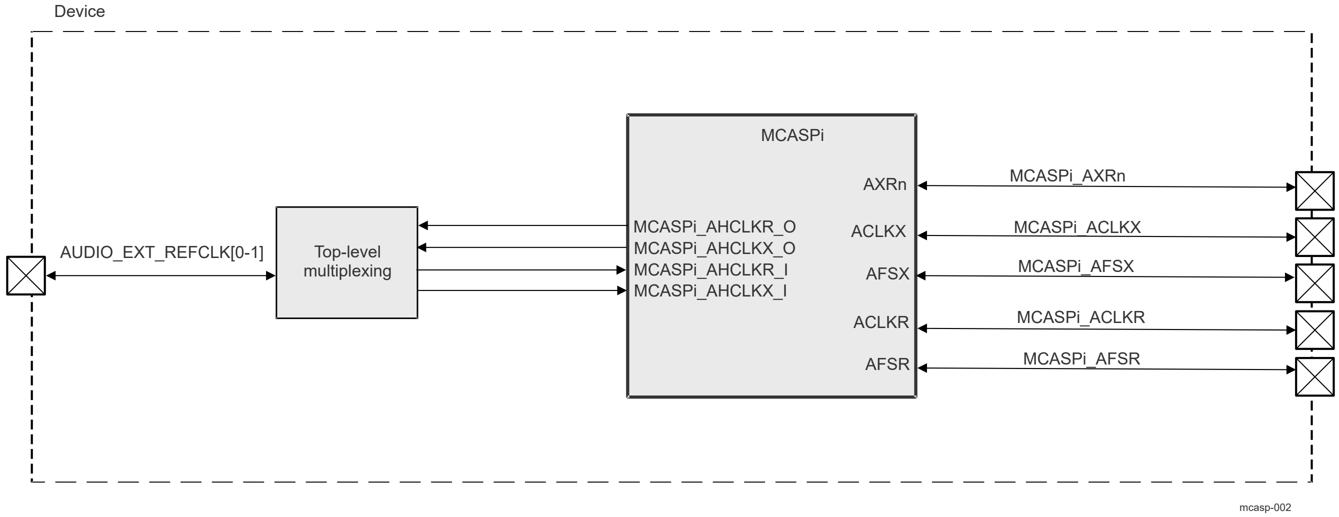

Note

i represents a MCASP instance. See the device datasheet for available domains and MCASP instances.

n represents a AXR signal from a MCASP instance. See the device datasheet for available domains and MCASP instances.

Figure 12-2. MCASP Interface Signals

Table 12-1 describes the MCASP I/O signals.

Table 12-1. MCASP I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		MCASPi[3] module		
AXR0	MCASPi[3]_AXR0	I/O	Audio transmit/receive data - channel 0	HiZ
AXR1	MCASPi[3]_AXR1	I/O	Audio transmit/receive data - channel 1	HiZ
AXR2	MCASPi[3]_AXR2	I/O	Audio transmit/receive data - channel 2	HiZ
AXR3	MCASPi[3]_AXR3	I/O	Audio transmit/receive data - channel 3	HiZ
AXR4	MCASPi[3]_AXR4	I/O	Audio transmit/receive data - channel 4	HiZ
AXR5	MCASPi[3]_AXR5	I/O	Audio transmit/receive data - channel 5	HiZ
AXR6	MCASPi[3]_AXR6	I/O	Audio transmit/receive data - channel 6	HiZ
AXR7	MCASPi[3]_AXR7	I/O	Audio transmit/receive data - channel 7	HiZ
AXR8	MCASPi[3]_AXR8	I/O	Audio transmit/receive data - channel 8	HiZ
AXR9	MCASPi[3]_AXR9	I/O	Audio transmit/receive data - channel 9	HiZ
AXR10	MCASPi[3]_AXR10	I/O	Audio transmit/receive data - channel 10	HiZ
AXR11	MCASPi[3]_AXR11	I/O	Audio transmit/receive data - channel 11	HiZ
AXR12	MCASPi[3]_AXR12	I/O	Audio transmit/receive data - channel 12	HiZ

Table 12-1. MCASP I/O Signals (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
AXR13	MCASPi(3)_AXR13	I/O	Audio transmit/receive data - channel 13	HiZ
AXR14	MCASPi(3)_AXR14	I/O	Audio transmit/receive data - channel 14	HiZ
AXR15	MCASPi(3)_AXR15	I/O	Audio transmit/receive data - channel 15	HiZ
ACLKX	MCASPi(3)_ACLKX	I/O	Transmit bit clock	HiZ
AFSX	MCASPi(3)_AFSX	I/O	Transmit frame synchronization	HiZ
ACLKR	MCASPi(3)_ACLKR	I/O	Receive bit clock	HiZ
AFSR	MCASPi(3)_AFSR	I/O	Receive frame synchronization	HiZ
MCASPi(3)_AHCLKX_I/O	AUDIO_EXT_REFCLK[0-1]	I/O	Transmit high-frequency controller clock. See *Module Integration*	HiZ
MCASPi(3)_AHCLKR_I/O	AUDIO_EXT_REFCLK[0-1]	I/O	Receive high-frequency controller clock. See *Module Integration*	HiZ

(1) I = Input; O = Output; I/O = Bidirectional

(2) HiZ = High Impedance

(3) i represents a MCASP instance. See the device datasheet for available domains and MCASP instances.

Note

MCASPi_AHCLKR_I/O and MCASPi_AHCLKX_I/O signals are multiplexed to AUDIO_EXT_REFCLK[0-1] device pins.

Note

For MCASPi_ACLKR_I/O, MCASPi_ACLKX_I/O, MCASPi_AHCLKR_I/O and MCASPi_AHCLKX_I/O signals to work properly, the RXACTIVE bit of the appropriate PADCFG_CTRL_MMR_CFG0_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

Note

A serializer AXR data pin is shared between the transmit and receive logic of that serializer. The direction of data is determined in the *MCASP_PDIR* register and the function (Tx or Rx) is selected in the corresponding serializer control register MCASP_SRCTLn (n = 0 to 15).

12.1.1.2.2 MCASP Protocols and Data Formats

12.1.1.2.2.1 Protocols Supported

The MCASP supports a wide variety of protocols:

- Transmit section supports:
  - Wide variety of I2S and similar bit-stream formats
  - TDM streams from 2 to 32 time slots
  - S/PDIF, IEC60958-1, AES-3 formats
- Receive section supports:

  - Wide variety of I2S and similar bit-stream formats
  - TDM streams from 2 to 32 time slots
  - TDM stream of 384 time slots specifically designed for easy interface to external digital interface receiver (DIR) device transmitting DIR frames to MCASP using the I2S protocol (one time slot for each DIR subframe)

The transmit and receive sections of the module may be individually programmed to support the following options on the basic serial protocol:

- Programmable clock and frame sync polarity (rising or falling edge): ACLKR/X, AFSR/X and AHCLKR/X_I/O
- Slot length (number of bits per time slot): 2, 4, 8, 12, 16, 20, 24, 28, 32 bits supported
- Word length (bits per word): 2, 4, 8, 12, 16, 20, 24, 28, 32 bits; always less than or equal to the time slot length
- First-bit data delay: 0, 1, 2 bit clocks
- Left/right alignment of word inside slot
- Bit order: MSB first or LSB first
- Bit mask/pad/rotate function
  - Automatically aligns data internally in either Q31 or integer formats
  - Automatically masks nonsignificant bits (sets to 0, 1, or extends value of another bit)

Note

In I2S mode, the transmit and receive sections can support simultaneous transfers on up to all serial data pins operating as 192 kHz stereo channels.

In DIT mode for MCASP, additional features of the transmitters are:

- Transmit-only mode 384 time slots (subframe) per frame
- Biphase encoded 3.3 V Output
- Channel status RAM (384 bits)
- User data RAM (384 bits)
- Support for consumer and professional applications
- Separate valid bit (V) for subframe A, B
- Stereo Support Only (Mono means send data 2 × via software)

In DIT mode, the transmitter can support a 192 kHz frame rate (stereo) on up to all serial data pins simultaneously (note that the internal bit clock for DIT runs two times faster than the equivalent bit clock for I2S mode, due to the need to generate Biphase Mark Encoded Data).

Note

The MCASP does NOT natively support DIR-mode reception (this is, receiving in the S/PDIF format). To allow this, the MCASP can use a DIR-input to I2S-output converter implemented by an external device (this is, external DIR component). To facilitate reception in this case, the TDM mode of MCASP receivers logic is extended to support a non-standard 384-slot TDM stream.

Note

An external transceiver must be connected to the MCASP port in the device to translate the electrical signals delivered by the MCASP (1.2 V or 1.8 V LVCMOS levels) to the electrical levels of the S/PDIF standard.

12.1.1.2.2.2 Definition of Terms

The serial bitstream transmitted or received by a MCASP serializer is a long sequence of 1s and 0s on an audio transmit/receive pins AXRn. However, the sequence has a hierarchical organization that can be described in terms of frames of data, slots, words, and bits.

A basic synchronous serial interface consists of three important components: clock, frame sync, and data. Figure 12-3 shows two of the three basic components: the clock signal (ACLKX/ACLKR) and the data signals AXRn. Figure 12-3 does not specify whether the clock is for transmit (ACLKX) or receive (ACLKR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter and receiver uses the signals ACLKX and ACLKR as serial clock, respectively. Optionally, a receiver can use ACLKX as the serial clock when a transmitter and receiver (not from the same serializer) of the MCASP are configured to operate synchronously.

- Bit:

  A bit is the smallest entity in the serial data stream. The beginning and end of each bit is marked by an edge of the serial clock. The duration of a bit is a serial clock period. A '1' is represented by a logic high on AXRn pins for the entire duration of the bit. A 0 is represented by a logic low on an AXRn pin for the entire duration of the bit.
- Word:

  A word is a group of bits that make up the data being transferred between the MCASP and the external device. Figure 12-3 shows an 8-bit word.
- Slot:

  A slot consists of the bits that make up the word and can consist of additional bits used to pad the word to a convenient number of bits for the interface between the MCASP and the external device. In Figure 12-3, the audio data consists of only 8 bits of useful data (8-bit word), but it is padded with four 0s (12-bit slot) to satisfy the desired protocol in interfacing to an external device. Within a slot, the bits can be shifted out of the MCASP on an AXRn pin with either MSB or LSB first.

  When the word size is smaller than the slot size, the word can be aligned to the left of the slot (beginning) or to the right of the slot (end). The additional bits in the slot not belonging to the word can be padded with 0, 1, or with one of the bits (typically, the MSB or LSB) from the data word, this is, left-aligned words within a slot are terminated with padding bits and right-aligned words within a slot are preceded by padding bits to fit in the slot size. Figure 12-4 shows these options.

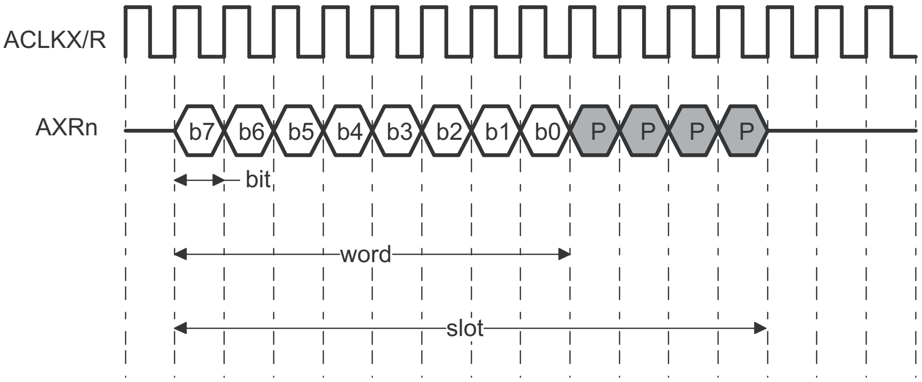

(1) b7:b0 - bits. Bits b7 to b0 form a word.

(2) P - pad bits. Bits b7 to b0, together with the 4 pad bits, form a slot.

(3) In this example, the data is transmitted MSB first, left-aligned.

mcasp-003

Figure 12-3. Definition of Bit, Word, and Slot

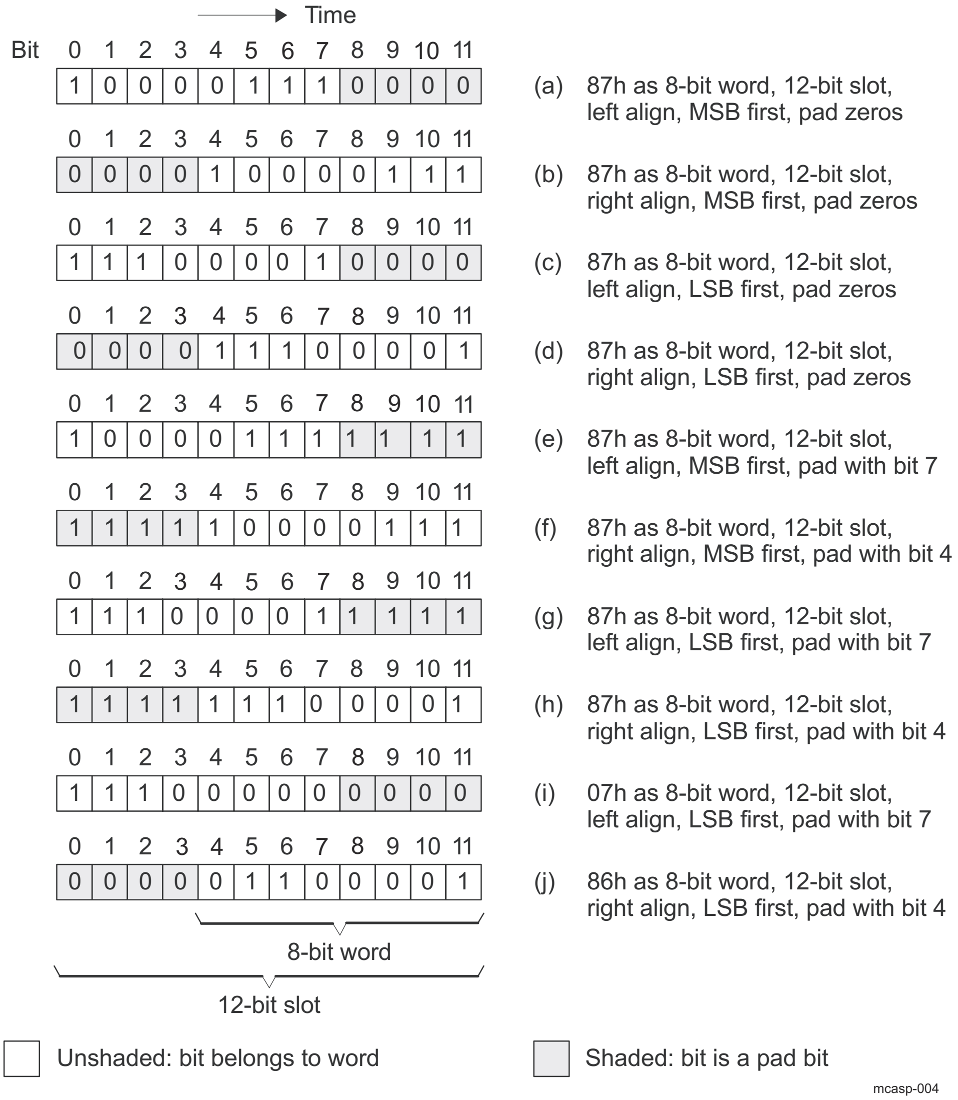

Figure 12-4. Bit Order and Word Alignment Within a Slot Examples

- Frame

  The third basic element of a synchronous serial interface is the frame synchronization signal, also referred to as frame sync in this chapter. A frame contains one or multiple slots, as determined by the desired protocol. Figure 12-5 shows an example frame of data and the frame definitions. In operation, the transmitter uses AFSX, and the receiver - AFSR signal. Figure 12-5 does NOT specify whether the frame sync (FS) is for transmit (AFSX) or receive (AFSR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter/receiver uses AFSX/AFSR as a frame synchronization signal, respectively. Optionally, the receiver can use AFSX as the frame sync when the transmitter and receiver of the MCASP are configured to operate synchronously. This example shows two slots in a frame (I2S format) and a frame-sync (FS) duration of a slot length.

  This section shows only the generic definition of the frame sync. For more information about the frame-sync formats required for the transfer modes and protocols (TDM-mode and DIT-mode supported formats), see Section 12.1.1.2.2.3 , *TDM Format* and Section 12.1.1.2.2.5 , *S/PDIF-Coding Format*.

Note

All of the MCASP serializers share the same, device pad accessible, clock and frame signals, as follows:

– AHCLKX_I/O, ACLKX and AFSX for the transmitting section
– AHCLKR_I/O, ACLKR and AFSR for the receiving section

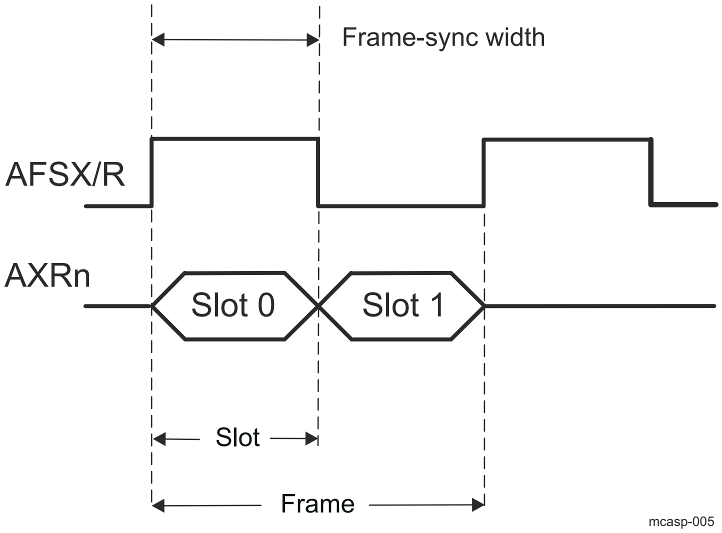

Figure 12-5. Definition of Frame and Frame-Sync Width

The following terms are used throughout this chapter:

- TDM: Time-division multiplexed. See Section 12.1.1.2.2.3 , *TDM Format* for details on the TDM protocol.
- I2S: Inter-Integrated Sound protocol, commonly used on audio interfaces. The MCASP supports the I2S protocol as part of the TDM mode (when configured as a 2-slot frame).
- DIT: Digital audio interface transmit. The MCASP supports transmitting in S/PDIF format on each AXRn data pin.
- DIR: Digital audio interface receive. The MCASP does NOT natively support receiving in S/PDIF format on AXRn data pins and requires an external DIR-to-TDM or DIR-to-I2S converter chip for a DIR-frame reception.
- Slot or time slot: For DIT/DIR format, a MCASP time slot corresponds to a DIT/DIR subframe.

12.1.1.2.2.3 TDM Format

The TDM format is used to transfer data between the host CPU and one or more analog-to-digital converter (ADC), digital-to-analog converter (DAC), or S/PDIF receiver (DIR) devices. An example for a 6-slot (channel) TDM transmission on one MCASP data pin - AXRn is illustrated on Figure 12-6.

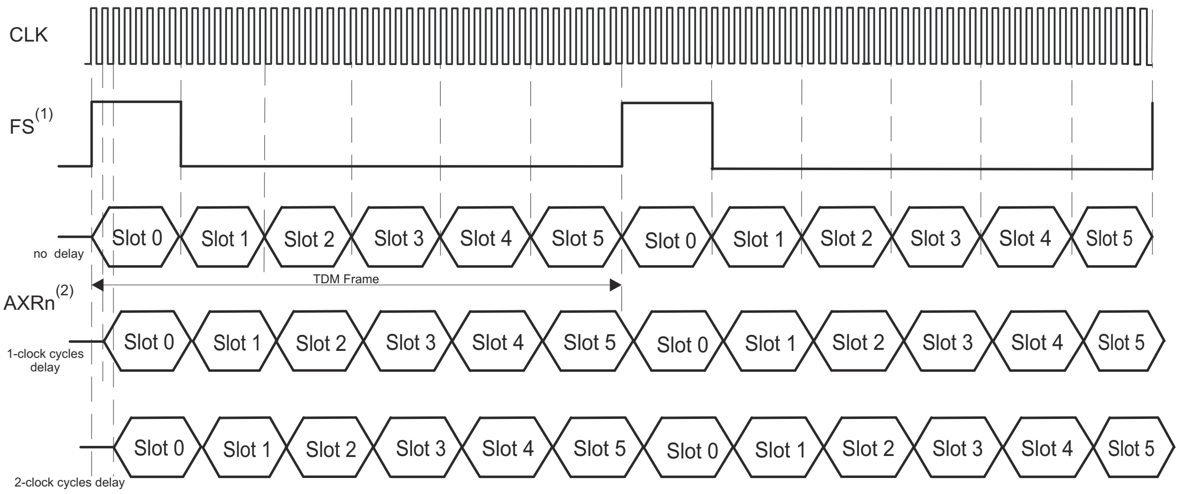

(1) - Frame sync duration of 1 slot - length is shown. A single bit - duration of FS is also supported

(2) - Slot 0 of AXRn stream is being offset with 0-, 1-, and 2- clock cycle delay from the frame sync, respectively.

mcasp-006

Figure 12-6. TDM Format - 6 channel example

The TDM format uses three signals in a basic synchronous serial interface: data (AXRn), clock (CLK) and frame sync (FS). The data signal present on AXRn pin is fully synchronous to the serial clock (ACLKX or ACLKR). The data bits are grouped into words and slots (see also Section 12.1.1.2.2.2), the latter being also refered to as the "time-slots" or "channels" in TDM terminology. A frame consists of multiple time-slots. Each TDM frame is marked by the frame sync signal (AFSX or AFSR). The TDM transfer is continuous and periodic, with no delays between slots.

Within a certain frame, the last bit of slot N is followed immediately on the next serial clock with the first bit of the next slot N+1. On the boundary between two adjacent TDM-frames, the last bit of the last slot from the frame M, is followed immediately on the next clock cycle with the first bit of the first slot from the next frame M+1. For MCASP, there is an option to offset the first bit of the first slot with a 0-,1- or 2-cycle delay from the frame sync signal.

The frame sync - AFSX/AFSR only marks the beginning of slot 0 and start of a new frame. Since it does not determine the boundaries of a slot, there is a requirement for a connected transmitter and receiver to agree on the number of transferred bits per slot.

In a typical audio system involving MCASP module, a single TDM data frame is transferred during each sample period Ts of a data converter. The user has following choices to implement multiple channels:

- Use more data slots (on a price of higher speed serial clock) per frame transmitted/received on just one of the available MCASP data pins AXRn.
- Use less number of slots per TDM frame (requires a slower serial clock), making them available on several of the MCASP pins AXRn.

12.1.1.2.2.4 I2S Format

The TDM transfer mode of the MCASP supports the I2S format when frame is configured to have 2 slots. The I2S format is specifically designed to transfer a stereo channel (left and right) over a single data pin AXRn. The "Slots" are also commonly referred to as "channels". The frame width duration in the I2S format equals size of a slot. The frame signal is also referred to as "word select" in the I2S format.

The I2S protocol is illustrated on Figure 12-7.

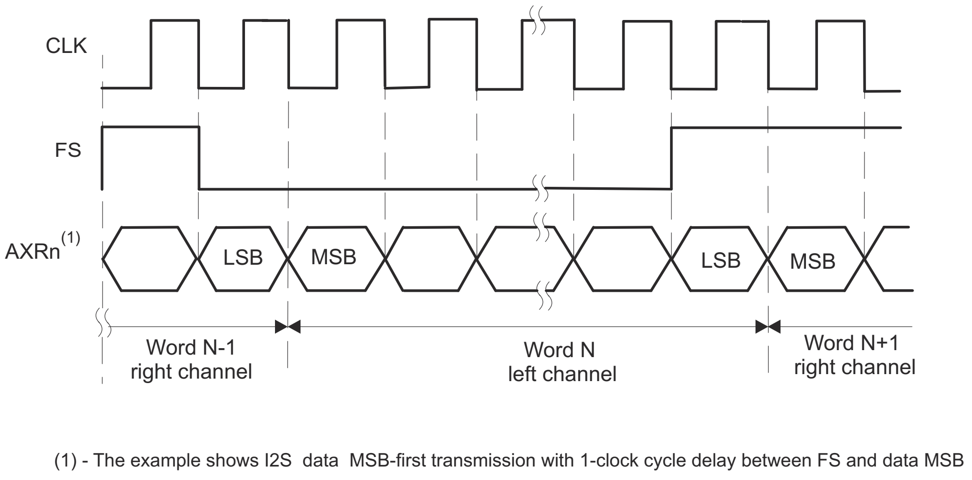

Figure 12-7. I2S Format Overview

12.1.1.2.2.5 S/PDIF Coding Format

The MCASP transmitter supports the S/PDIF format with 3.3 V biphase-mark encoded output. The S/PDIF format is supported by the DIT- transfer mode of the MCASP. This section briefly discusses the S/PDIF coding format.

Note

The DIR- reception of S/PDIF format frames is NOT natively supported from the device MCASP. For this purpose, an external DIR-to-TDM transfer mode adapter can be used between the remote device S/PDIF transmitter output and the MCASP TDM-only compatible receiver input.

12.1.1.2.2.5.1 Biphase-Mark Code

In S/PDIF format, the digital signal is coded using the biphase-mark code (BMC). For each serializer transmitter n, the clock, frame, and data are embedded in only one signal - the data signal AXRn. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. These two logical states form a cell. The duration of the cell, which equals the duration of the data bit, is called a time interval. A logical 1 is represented by two transitions of the signal within a time interval, which corresponds to a cell with logical states 01 or 10. A logical 0 is represented by one transition within a time interval, which corresponds to a cell with logical states 00 or 11. In addition, the logical level at the start of a cell is inverted from the level at the end of the previous cell. Figure 12-8 and Table 12-2 show how data is encoded to the BMC format.

As shown in Figure 12-8, the clock frequency is twice the unencoded data bit rate. In addition, the clock is always programmed to 128 × f_S, where f_S is the sample rate (see Section 12.1.1.2.2.5.3 , *Frame Format*, for details on how this clock rate is derived based on the S/PDIF format). The device receiving in S/PDIF format can recover the clock and frame information from the BMC signal.

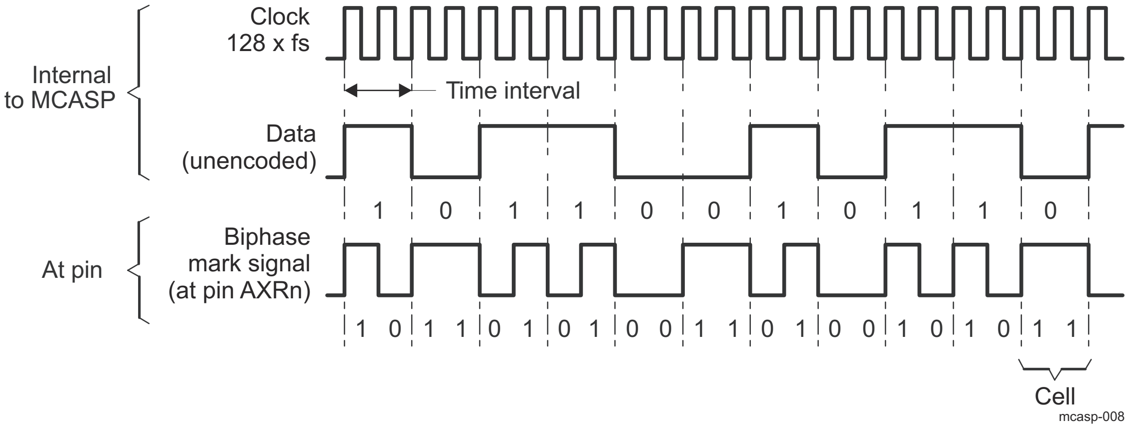

Figure 12-8. Biphase-Mark Code

Table 12-2. Biphase-Mark Encoder

Data (Unencoded)	Previous State at Pin AXRn	BMC-Encoded Cell Output at Pin AXRn
0	0	11
0	1	00
1	0	10
1	1	01

12.1.1.2.2.5.2 S/PDIF Subframe Format

Every audio sample transmitted in a subframe consists of 32 S/PDIF time intervals (or cells), numbered 0 to 31. Figure 12-9 shows a subframe.

- Time intervals 0–3 carry one of the three permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row. See Table 12-3.
- Time intervals 4–27 carry the audio sample word in linear 2s-complement representation. The MSB is carried by time interval 27. When a 24-bit coding range is used, the LSB is in time interval 4. When a 20-bit coding range is used, time intervals 8-27 carry the audio sample word with the LSB in time interval 8. Time intervals 4–7 may be used for other applications and are designated auxiliary sample bits.
- If the source provides fewer bits than the interface allows (20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field can carry any other information.
- Time interval 28 carries the validity bit (V) associated with the main data field in the subframe.
- Time interval 29 carries the user data channel (U) associated with the main data field in the subframe.
- Time interval 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.
- Time interval 31 carries a parity bit (P) such that time intervals 4–31 carry an even number of 1s and an even number of 0s (even parity). As listed in Table 12-3, the preambles (time intervals 0–3) are also defined with even parity.

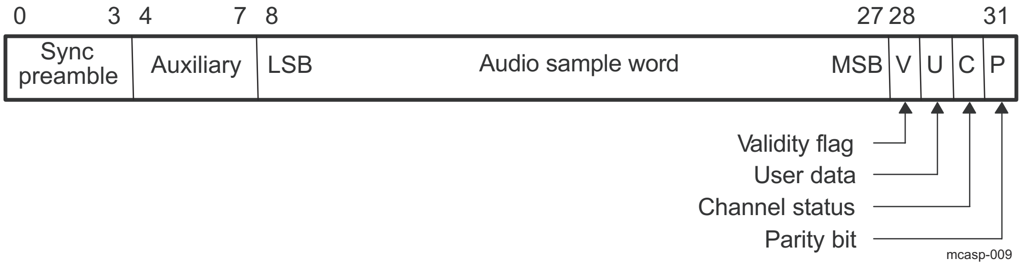

Figure 12-9. S/PDIF Subframe Format

As listed in Table 12-3, the MCASP DIT generates only one polarity of preambles, and it assumes the previous logical state is 0. This is because the MCASP assures an even-polarity encoding scheme when transmitting in DIT mode. If an underrun condition occurs, the DIT resynchronizes to the correct logic level on the AXRn pin before continuing with the next transmission.

Table 12-3. Preamble Codes

Preamble Code(1)	Previous Logical State	Logical States on pin AXRn(2)	Description
B (or Z)	0	1110 1000	Start of a block and subframe 1
M (or X)	0	1110 0010	Subframe 1
W (or Y)	0	1110 0100	Subframe 2

(1) Historically, preamble codes are referred to as B, M, and W. For use in professional applications, preambles are referred to as Z, X, and Y, respectively.

(2) The preamble is not BMC-encoded. Each logical state is synchronized to the serial clock. These eight logical states make up time slots (cells) 0 to 3 in the S/PDIF stream.

12.1.1.2.2.5.3 Frame Format

An S/PDIF frame is composed of two subframes (see Figure 12-10). For linear coded audio applications, the rate of frame transmission normally corresponds exactly to the source sampling frequency f_S. The S/PDIF format clock rate is therefore 128 × f_S (128 = 32 cells per subframe × 2 clocks per cell × 2 subframes per sample). For example, for an S/PDIF stream at a 192-kHz sampling frequency, the serial clock is 128 × 192 kHz = 24.58 MHZ.

In 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive subframes. Both subframes contain valid data (cell 28 validity bits for A- and B- channels, both set to '0'). The first subframe (left or A channel in stereophonic operation and primary channel in monophonic operation) normally starts with preamble M. However, the preamble of the first subframe changes to preamble B once every 192 frames to identify the start of the block structure used to organize the channel status information. The second subframe (right or B channel in stereophonic operation and secondary channel in monophonic operation) always starts with preamble W.

In single-channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried in the first subframe and may be duplicated in the second subframe. If the second subframe is not carrying duplicate data, cell 28 (validity bit) is set to logical 1.

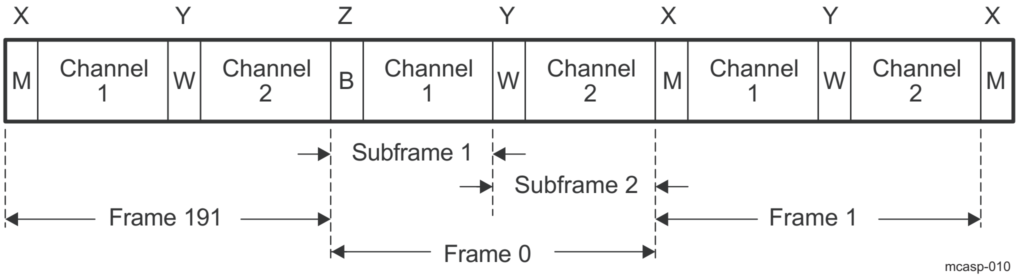

Figure 12-10. S/PDIF Frame Format

12.1.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.1.1.4 MCASP Functional Description

In the text throughout this section a single instance of MCASP is described assuming that all modules are functionally identical. For module availability and integration differences, see Section 12.1.1.2 , *MCASP Environment*, and *Module Integration*.

12.1.1.4.1 MCASP Block Diagram

Figure 12-11 shows the major blocks of the MCASP module.

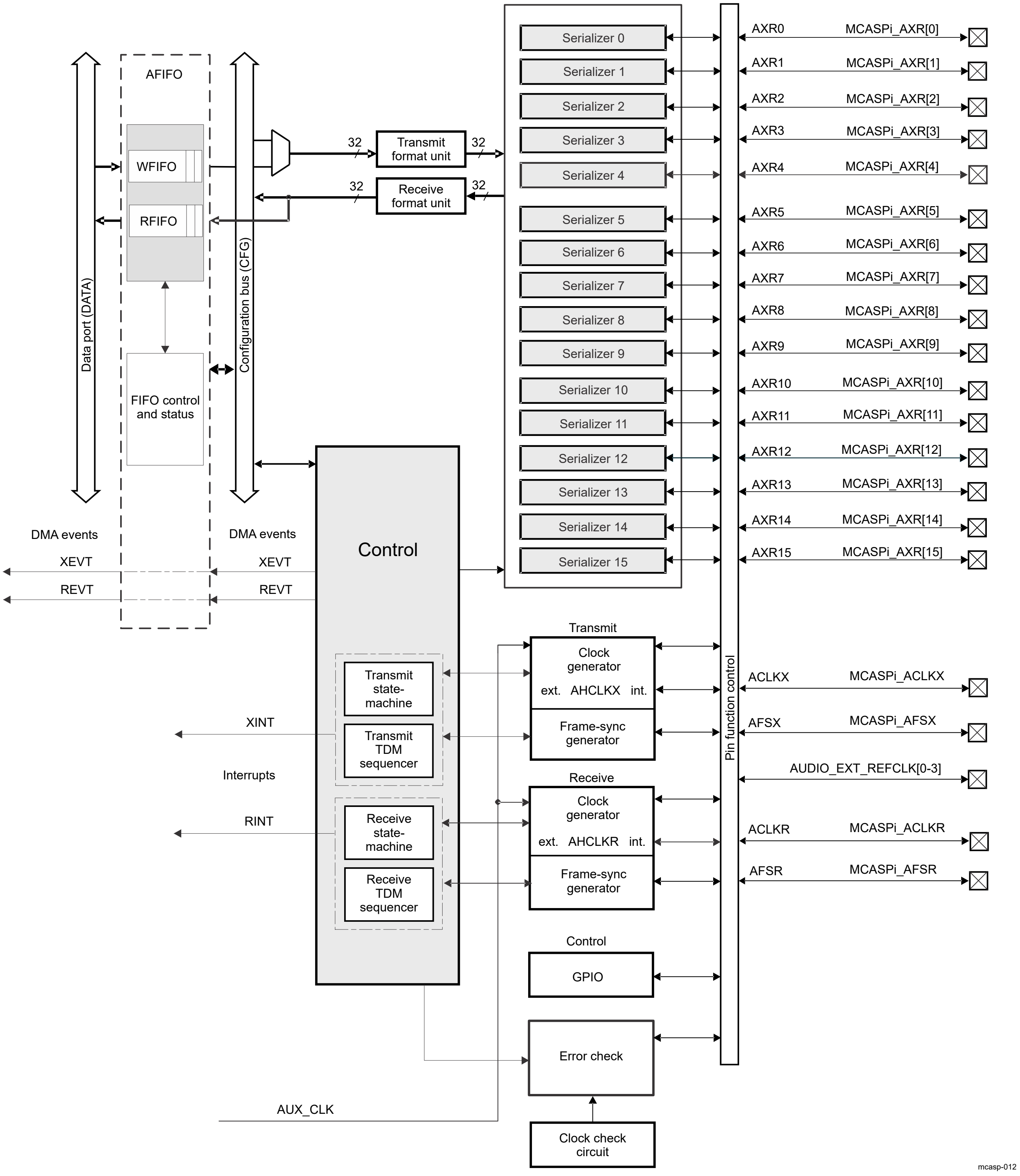

Note

i represents a valid instance of MCASP in a domain. See the device datasheet for valid instances.

Note

All signals might not be valid for an instance. See the device datasheet for specifics.

Figure 12-11. MCASP Module Block Diagram

Note

The internal and external clocks mentioned in this section are with respect to clock and frame-sync generator modules.

12.1.1.4.2 MCASP Clock and Frame-Sync Configurations

There are three scenarios to provide clock source signals for the Tx part and four scenarios for the Rx part of the MCASP serializers. The first three scenarios are identical between the Tx and Rx part of the MCASP. They feature an asynchronous operation between receiver and transmitter channels using independent Tx/Rx bit rate clock sources (either internal or external).

In the first scenario, the transmit - XCLK and receive - RCLK serial clocks (clock at the bit rate) are generated internally by passing through a couple of clock dividers off the internal functional clock source (AUXCLK). In this case, the bit rate clock is generated internally and is driven out on the pin ACLKX for the Tx part and pin ACLKR for the Rx part, respectively. An internally generated high-frequency clock can be optionally driven out onto the AHCLKX pin for the Tx part to serve as a reference clock for other components in the system.

In the second scenario, an external for the device clock, is passed on the ACLKX (for the TX part) and ACLKR (for the RX part) pins which are configured as inputs. In this case the Rx- /Tx- high-speed clock logic is bypassed for the XCLK/RCLK generation.

In the third (mixed) scenario, an externally driven (controller) high-frequency clock is applied on the AHCLKX (for the TX part) pin, which is configured as input. In this case the AHCLKX clock frequency can be divided down via programming the ACLKX associated divider to produce the necessary bit rate clock. The high-speed clock divider can NOT be used.

In the fourth clock generation scenario the bit rate clock for MCASP receivers - RCLK is derived from the bit rate clock of the MCASP transmitters - XCLK for a synchronous operation between transmitters and receivers. Hence, the whole receiver clock generator logic is bypassed.

A typical role of the MCASP frame sync signal is to carry the left/right clock (LRCLK) signal when transmitting and receiving stereo data.

For an asynchronous operation, the AFSX (Tx part) and AFSR (Rx part) frame synchronization signals can be sourced internally or delivered externally independently for the Tx and Rx channels. During synchronous operation the receive frame sync - AFSR signal is derived from the transmit frame sync - AFSX signal. A synchronous and asynchronous mode applies to bit rate clock and frame sync signals at the same time.

12.1.1.4.2.1 MCASP Transmit Clock

The transmit high-speed and transmit clock configuration is controlled by the following registers:

- *MCASP_ACLKXCTL*
- *MCASP_AHCLKXCTL*

In case, the transmit bit clock, ACLKX, is generated internally, the *MCASP_ACLKXCTL*[5] CLKXM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the *MCASP_ACLKXCTL*[4-0] CLKXDIV bit field) from the source signal.

If the transmit high-frequency controller clock, AHCLKX, is also sourced internally (that is first scenario described in Section 12.1.1.4.2 , the *MCASP_AHCLKXCTL*[15] HCLKXM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the *MCASP_AHCLKXCTL*[11-0] HCLKXDIV bit field) from the MCASP internal clock source AUXCLK.

Internally, the MCASP always shifts transmit data at the rising edge of the internal transmit clock - XCLK, (see Figure 12-12). The CLKXP mux determines if ACLKX needs to be inverted to become XCLK. If *MCASP_ACLKXCTL*[7] CLKXP = 0, the CLKXP mux directly passes ACLKX signal to XCLK. As a result, the MCASP shifts transmit data at the rising edge of ACLKX. If *MCASP_ACLKXCTL*[7] CLKXP = 1, the CLKX mux passes the inverted version of ACLKX to XCLK. As a result, the MCASP shifts transmit data at the falling edge of ACLKX.

It can be seen in Figure 12-12 that XCLK is propagated to the Rx clock logic, to allow an internally synchronous operation between MCASP transmitters and receivers. This is used for example in the MCASP loopback mode.

Note

The polarity of ACLKX can be controlled in the *MCASP_ACLKXCTL*[7] CLKXP bit, regardless of ACLKX signal being internally or externally sourced.

In addition, there is an option to invert polarity of the AHCLKX controller high speed clock via writing the *MCASP_AHCLKXCTL*[14] HCLKXP bit.

Note

In a similar way, the polarity of AHCLKX clock can be controlled in the *MCASP_AHCLKXCTL*[14] HCLKXP bit, regardless of the AHCLKX signal being internally or externally sourced.

Figure 12-12 presents the block diagram of the transmit clock generator.

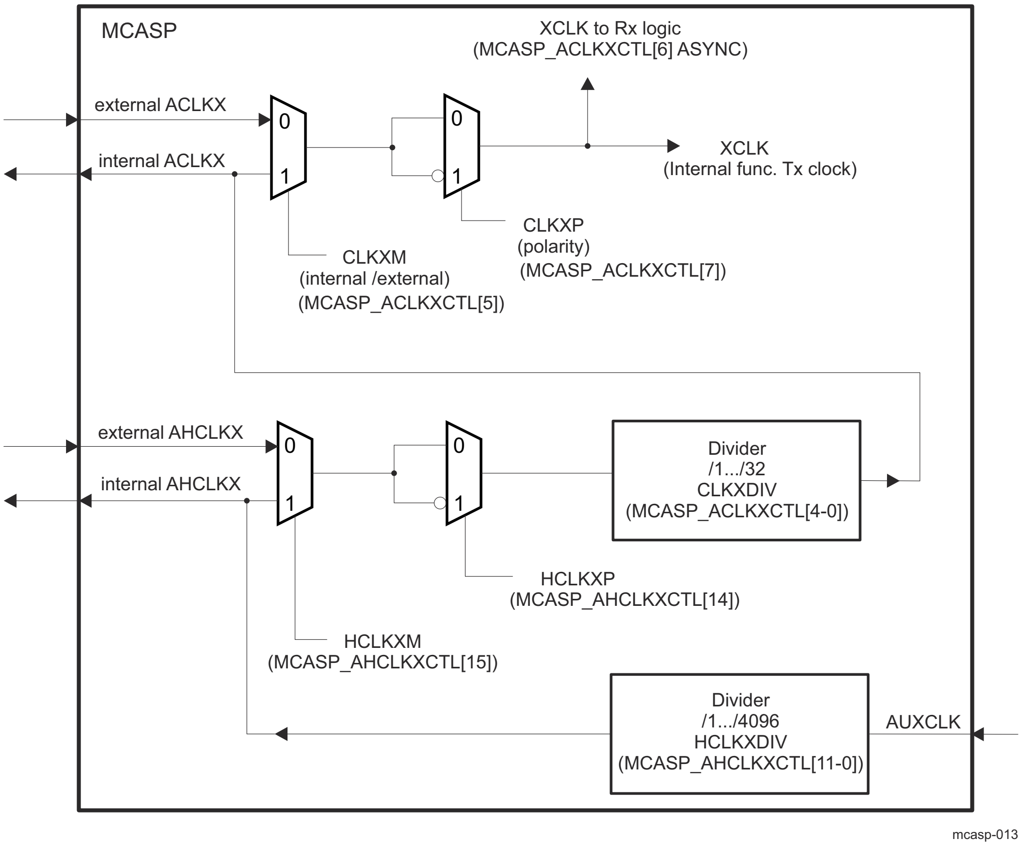

Figure 12-12. Transmit Clock Generator Block Diagram

Note

In this device:

- ACLKX is mapped on the device ball ACLKX
- internal AHCLKX is mapped on the device balls AUDIO_EXT_REFCLK[0-1]
- external AHCLKX is mapped on MCASPi_AHCLKX clock from the Device Configuration

For more information about MCASP integration, see Section 12.1.1.2 , *MCASP Environment*, and *Module Integration*.

12.1.1.4.2.2 MCASP Receive Clock

The MCASP receive clock generator is built on a very similar to the transmit clock generator (but independent) circuit.

The receive clock configuration is controlled by the following registers:

- *MCASP_ACLKRCTL*
- *MCASP_AHCLKRCTL*

In case, the receive bit clock, ACLKR, is generated internally (but asynchronously to XCLK), the *MCASP_ACLKRCTL*[5] CLKRM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the *MCASP_ACLKRCTL*[4-0] CLKRDIV bit field) from the source signal.

If the receive high-frequency controller clock, AHCLKR, is also sourced internally (that is, first scenario described in Section 12.1.1.4.2) and the *MCASP_AHCLKRCTL*[15] HCLKRM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the *MCASP_AHCLKRCTL*[11-0] HCLKRDIV bit field) from the MCASP internal clock source AUXCLK.

Note

The polarity of ACLKR can be controlled in the *MCASP_ACLKRCTL*[7] CLKRP bit, regardless of ACLKR signal being internally or externally sourced.

In a similar way, the polarity of AHCLKR clock can be controlled in the *MCASP_AHCLKRCTL*[14] HCLKRP bit, regardless of the AHCLKR signal being internally or externally sourced.

There is an option for the MCASP receiver to be configured to operate synchronously to the ACLKX and AFSX signals. The XCLK output of the Tx Clock generator (see Figure 12-12 and Figure 12-13) becomes source of the receive clock (RCLK output), when the *MCASP_ACLKRCTL*[6] ASYNC bit in the transmit clock control register is set to '0b0'. For more information, refer to Section 12.1.1.4.2.4 .

Figure 12-13 presents the block diagram of the receive clock generator.

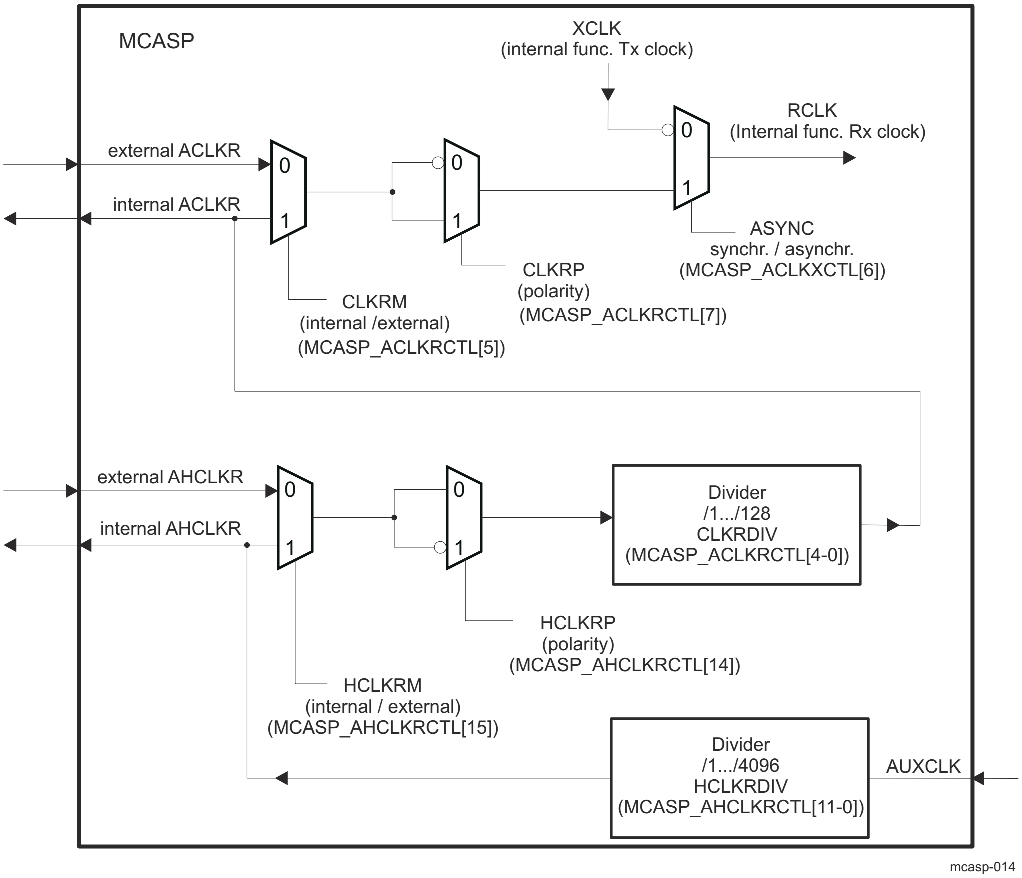

Figure 12-13. Receive Clock Generator Block Diagram

Note

In this device:

- ACLKR is mapped on the device ball ACLKR
- internal AHCLKX is mapped on the device balls AUDIO_EXT_REFCLK[0-1]
- external AHCLKR is mapped on Device Configuration MCASPi_AHCLKR from Device Configuration

For more information about MCASP integration, see Section 12.1.1.2 , *MCASP Environment*, and , *Module Integration*.

12.1.1.4.2.3 Frame-Sync Generator

There are two different modes for frame sync: burst and TDM. The MCASP frame sync generator logic is illustrated in Figure 12-14.The I/O buffers are not part of the MCASP module, and are not shown in the figure.

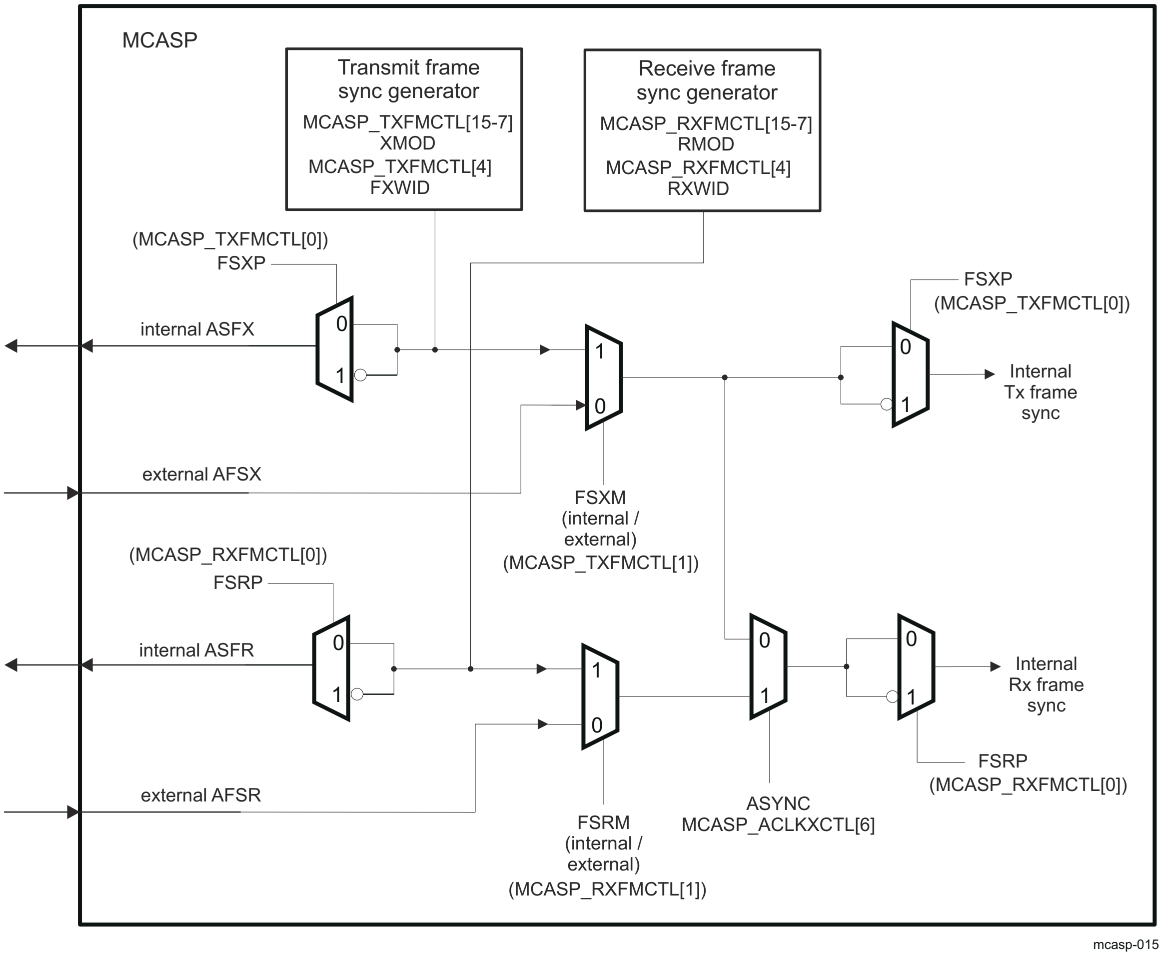

Figure 12-14. Frame Sync Generator Block Diagram

Note

For more on MCASP integration, see Section 12.1.1.2 , *MCASP Environment*, and *Module Integration*.

For the transmit logic, following frame-sync generator configurations can be selected:

- Internally/externally generated frame-sync via configuring MCASP_AFSXCTL[1] FSXM bit
- Frame-sync polarity: Rising edge or falling edge via configuring MCASP_AFSXCTL[0] FSXP bit
- Frame-sync width: "single bit" or "single word" via configuring MCASP_AFSXCTL[4] FXWID bit
- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the MCASP_AFSXCTL[15-7] XMOD bit field, as follows:
  - For DIT mode (384 slots) - MCASP_AFSXCTL[15-7] XMOD = 0x180
  - For I2S mode (2 TDM slots) - MCASP_AFSXCTL[15-7] XMOD = 0x2
  - For TDM mode (from 3 to 32 TDM slots) - MCASP_AFSXCTL[15-7] XMOD bit field set in range 0x3 - 0x20
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in MCASP_XFMT[17-16] XDATDLY bit field

For the receive logic, following frame-sync generator configurations can be selected:

- Internally/externally generated frame-sync via configuring MCASP_AFSRCTL[1] FSRM bit
- Frame-sync polarity: Rising edge or falling edge via configuring MCASP_AFSRCTL[0] FSRP bit
- Frame-sync width: "single bit" or "single word" via configuring MCASP_AFSRCTL[4] FRWID bit

- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the MCASP_AFSRCTL[15-7] RMOD bit field, as follows:
    - For I2S mode (2 TDM slots) - MCASP_AFSRCTL[15-7] RMOD = 0x2
    - For TDM mode (from 3 to 32 TDM slots) - MCASP_AFSRCTL[15-7] RMOD set in range 0x3 - 0x20
    - For the special 384-slot TDM mode - MCASP_AFSRCTL[15-7] RMOD = 0x180
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in the MCASP_RFMT[17-16] RDATDLY bit field
- Selecting the source (AFSX or AFSR) of receiver internal frame synchronization. This is done in the same bit - *MCASP_ACLKXCTL*[6] ASYNC, used to define the receiver internal clock source. For more details, refer to Section 12.1.1.4.2.4 , *Synchronous and Asynchronous Transmit and Receive Operations*.

Regardless of the AFSX/AFSR being internally generated or externally sourced, the polarity of AFSX/AFSR is determined by FSXP/FSRP, respectively, to be either rising or falling edge. If FSXP/FSRP = 0, the frame sync polarity is rising edge. If FSXP/FSRP = 1, the frame sync polarity is falling edge.

Note

Certain restrictions apply to the receive and transmit logic settings, when the *MCASP_ACLKXCTL*[6] ASYNC bit is set to 0b0. They are described in Section 12.1.1.4.2.4 .

12.1.1.4.2.4 Synchronous and Asynchronous Transmit and Receive Operations

Synchronous Transmit and Receive Operations -

When the *MCASP_ACLKXCTL*[6] ASYNC bit is written to 0b0, the transmit and receive sections operate synchronously to the transmit section clock and transmit frame sync signals.

Though Rx section may have a different data format, it has to be configured to have the same slot size than the transmit section one. As shown on the Figure 12-13, with the ASYNC bit set to 0b0, the RCLK becomes an inverted version of the transmit clock generator XCLK output.

When the *MCASP_ACLKXCTL*[6] ASYNC = 0b0, both Rx and Tx sections use the same clock and frame sync signals. For this reason, they must be aligned on the following settings:

- MCASP_DITCTL[0] DITEN = 0 (that is, transmission in TDM mode is enabled)
- The total number of bits per frame must be the same (that is, RSSZ * RMOD product value must equal XSSZ * XMOD product value)
- The settings in the *MCASP_ACLKRCTL* register are NOT considered
- FSXM must match FSRM
- FXWID must match FRWID

For all other settings, the transmit and receive sections may be programmed independently.

Asynchronous Transmit and Receive Operations -

When the *MCASP_ACLKXCTL*[6] ASYNC = 0b1, Tx and Rx operate independently from each other with separate clock and frame sync signals.

Note

Synchronous transmit and receive operations are allowed only in the MCASP TDM (I2S) mode (this is, when MCASP_DITCTL[0] DITEN = 0b0).

12.1.1.4.3 MCASP Serializers

The MCASP serializers shift serial data in (Rx) and out (Tx) of the MCASP. A given serializer n consists of a shift register (XRSRn) with a single-entry data buffer XRBUFn used either for transmitting (write accessible in the MCASP_XBUFn register) or for receiving (read accessible in the MCASP_RBUFn register) data. In addition, each serializer has a dedicated control register (MCASP_SRCTLn) and a serial bidirectional data pin - AXRn.

The register MCASP_SRCTLn allows n-th serializer to be configured as a transmitter, receiver, or as inactive. There are transmit and receive data formatting units to support data alignment options of the MCASP which are shared between all Tx and Rx serializers, respectively.

A given serializer XRSRn shifter configured as a receiver in the MCASP_SRCTLn register, shifts in data through MCASP corresponding device level bidirectional data pad AXRn. A given serializer XRSRn shifter configured as a transmitter in the MCASP_SRCTLn register, shifts out data on MCASP corresponding device level bidirectional data pad AXRn (n = 0 to 15).

The serializer is clocked from the transmit section clock (ACLKX signal) if configured to transmit or clocked from the receive section clock (ACLKR signal) if configured to receive. A serializer configured to transmit and receive operates in lockstep, which means that for MCASP there are at most a couple of zones, one for transmit and one for receive.

Figure 12-15 shows the serializer block diagram.

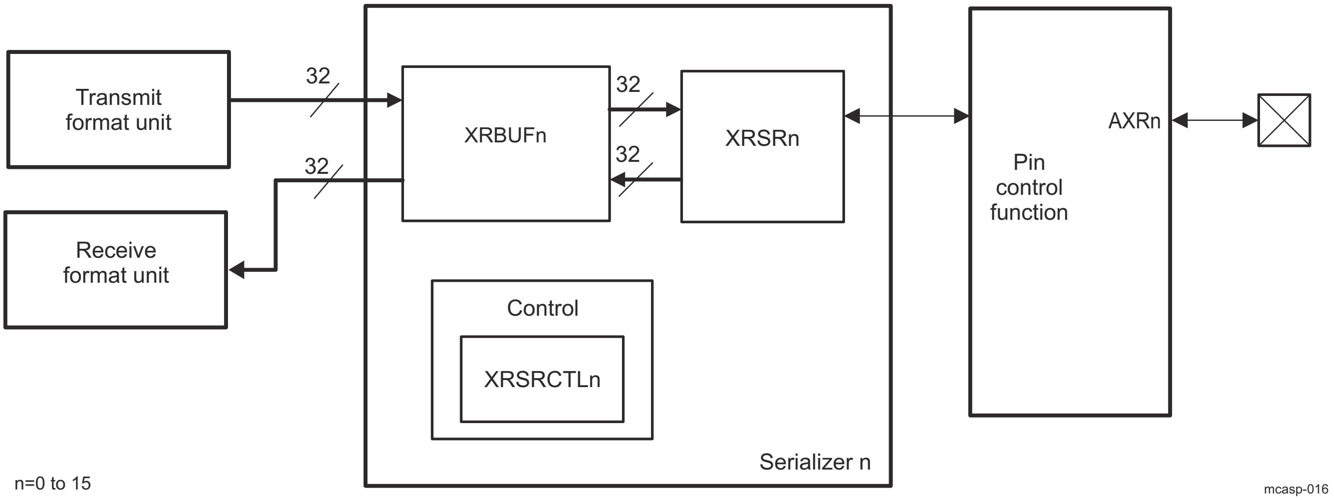

Figure 12-15. Individual Serializer and Connections Within MCASP

Transmission on the n-th serializer is performed as follows:

The MCASP is serviced by writing data into the MCASP_XBUFn register, which is an alias of the serializer data buffer - XRBUFn for transmit function. The data automatically passes through the transmit format unit before reaching the XRBUFn register in the serializer. The data is then copied from the XRBUFn to XRSRn and shifted out from AXRn synchronously to the serial clock.

Reception from the n-th serializer is performed as follows:

The data is shifted into the MCASP XRSRn serializer register through the AXRn pin, bit by bit. Once the entire slot becomes available within the XRSRn shift register, the data is copied into the serializer data buffer - XRBUFn, and can be accessed in the MCASP_RBUFn register, which is an alias of the serializer data buffer - XRBUFn for receive function. When software reads the data from this register, the MCASP passes the data through the receive format unit, hence it returns the formatted data.

Serializer controls:

A serializer n is configured as inactive via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x0.

For a transmitting serializer, the MCASP_SRCTLn[3-2] DISMOD bitfield, defines the AXRn pin output state, during inactive slots (HIGH, LOW or Hi-Z).

Transmit function for the n-th serializer is selected via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x1.

Receive function for the n-th serializer is selected via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x2 (n = 0 to 15).

In the DIT-transmission mode (that is S/PDIF format data transmission): in addition to the data, the serializer shifts out other DIT-specific information accordingly (preamble, user data, etc.). For more information, see Section 12.1.1.2.2.5 , *S/PDIF Coding Format*.

12.1.1.4.4 MCASP Format Units

The MCASP has one transmit data formatting unit and one receive data formatting unit, shared between the device MCASP serializers. These units automatically remap the data bits within the transmitted or received words between a natural format for the device processors (for example, a Q31 representation) and the required format for the external serial device (for example I2S format). During the remapping process, the format unit can also mask off certain bits.

Since all transmitters share the same data formatting unit, the MCASP only supports one transmit format at a time. For example, the MCASP does NOT transmit in "I2S format" on serializer 0, while transmitting "Left Justified" on serializer 1. Likewise, the receiver section of the MCASP only supports one data format at a time, and this format applies to all receiving serializers.

Note

The MCASP can transmit in one format while receiving in a completely different format.

The bit mask and pad stage of each of Tx and Rx format units includes a full 32-bit mask register, allowing selected individual bits to either pass through the stage unchanged, or be masked off. The bit mask and pad then pad the value of the masked off bits by inserting either a 0, a 1, or one of the original 32 bits as the pad value. The last option allows for sign-extension when the sign bit is selected to pad the remaining bits. The rotate right stage performs bitwise rotation by a multiple of 4 bits (between 0 and 28 bits), programmable by the MCASP_RFMT/MCASP_XFMT register. Note that this is a rotation process, not a shifting process, so bit 0 gets shifted back into bit 31 during the rotation. The bit order - reversal stage either passes all 32 bits directly through, or swaps them. This allows for either MSB or LSB first data formats. If bit order reversal is not enabled, then the MCASP will naturally transmit and receive in an LSB first order. Finally, note that the RDATDLY/XDATDLY bits in the MCASP_RFMT/MCASP_XFMT also determine the data format. For example, the difference between I2S format and left-justified is determined by the delay between the frame sync edge and the first data bit of a given time slot. For I2S format, RDATDLY/XDATDLY should be set to a 1-bit delay, whereas for left-justified format, it should be set to a 0-bit delay. The combination of all the options in the MCASP_RFMT/MCASP_XFMT register means that the MCASP supports a wide variety of data formats, both on the serial data lines, and in the device CPU data representation.

12.1.1.4.4.1 Transmit Format Unit

The MCASP transmit formatting unit consists of three stages :

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB-first or LSB-first)

Figure 12-16 shows the transmit formatting unit.

The MCASP transmitter supports serial formats of:

- Slot (or Time slot) size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size ≤ Slot size
- Alignment: when more bits/slot than bits/words, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:

  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

Hardware support for these serial formats comes from the programmable options in the bitstream format register - MCASP_XFMT:

- XRVRS: bit reverse (1) or no bit reverse (0)
- XROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- XSSZ: transmit slot size of 8, 12, 16, 20, 24, 28, or 32 bits

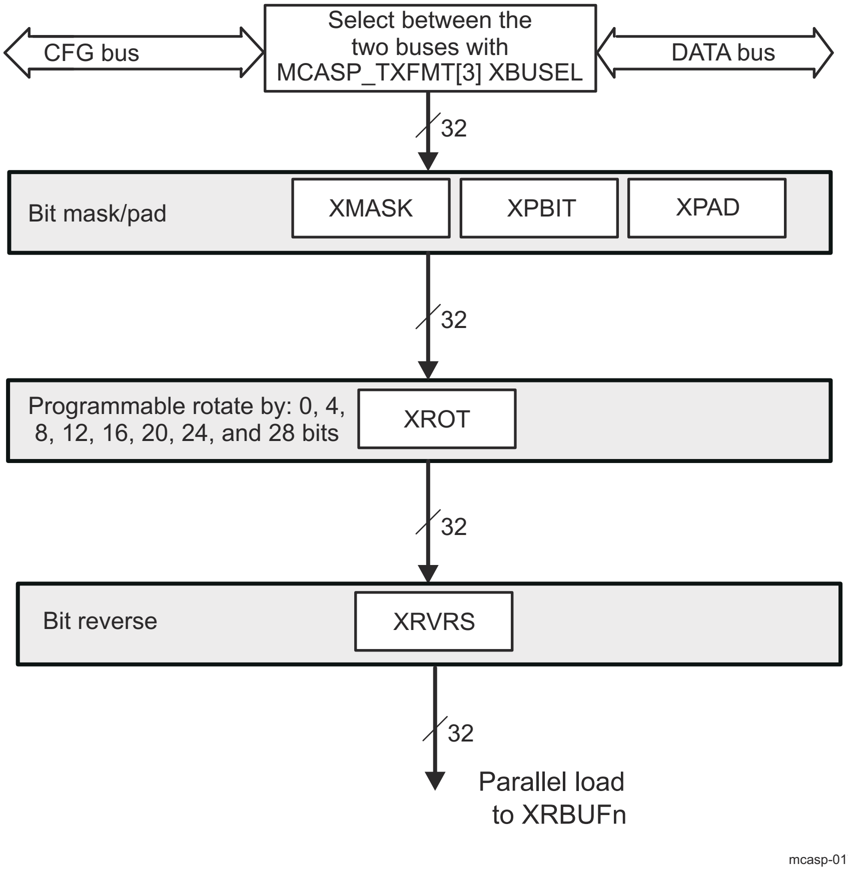

Figure 12-16. Transmit Format Unit

As shown in Figure 12-16, the data to the transmit format unit can come from the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_XFMT[3] XBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 12.1.1.4.10.1.3 , *Transfers Through the DATA Port*, and Section 12.1.1.4.10.1.4 , *Transfers Through the Configuration (CFG) Bus*.

In the transmit format unit (TFU), the input data bits are first masked-off with the MCASP_XMASK[31-0] XMASK contents. The masked data is then right-rotated to the MCASP_XFMT[2-0] XROT bit field positions, to produce the output word for a TDM- or DIT- transmission.

The bit mask stage includes a full 32-bit mask register, allowing selected individual bits to pass through the stage unchanged or be masked off.

12.1.1.4.4.1.1 TDM Mode Transmission Data Alignment Settings

The TDM-mode transmission settings are relevant for I2S-protocol and protocols using more than 2 TDM-slots.

XSSZ should always be programmed to match the slot size of the serial stream.

Note

Note that, TDM word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the XROT field.

The Table 12-4 show the XRVRS and XROT fields for each serial format and for both integer and Q31 fractional internal representations.

The Table 12-4 assumes that all slot size (SLOT in Table 12-4) and word size (WORD in Table 12-4) options are multiples of 4, since the transmit rotate right unit only supports rotation by multiples of 4. However, the bit mask/pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be transmitted in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1.

The transmit bit mask/pad unit operates on data as an initial step of the transmit format unit, and the data is aligned in the same representation as it is written to the transmitter (typically Q31 or integer).

Table 12-4. MCASP TFU TDM Mode Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_XFMT bits	
			XROT[1]	XRVRS
MSB first[2]	Left aligned	Q31 fraction	0	1
MSB first	Right aligned	Q31 fraction	SLOT - WORD	1
LSB first	Left aligned	Q31 fraction	32 - WORD	0
LSB first	Right aligned	Q31 fraction	32 - SLOT	0
MSB first[2]	Left aligned	Integer	WORD	1
MSB first	Right aligned	Integer	SLOT	1
LSB first	Left aligned	Integer	0	0
LSB first	Right aligned	Integer	(32 - (SLOT - WORD)) % 32	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator

(2) To transmit in I2S format, select MSB first, left aligned, and also select XDATDLY = 01 (1 bit delay)

12.1.1.4.4.1.2 DIT Mode Transmission Data Alignment Settings

In case of a DIT-mode (S/PDIF protocol) transmission, while left-aligned Q31 data should be right-rotated to a multiple by 4 positions, no right-rotation is required for a right-aligned Q31 data. Because this is a rotation process, not a shifting process, bit 0 gets shifted back into bit 31 during the process.

The MCASP_XFMT[17-16] XDATDLY bit field must be set to a 0-bit delay (0x0 value).

For left-aligned Q31 data, the following transmit format unit settings process the data into right-aligned data, ready for transmission:

- MCASP_XFMT[2-0] XROT =
  - 0x2 (rotate right by 8 bits) - for a 24-bit output audio data
  - 0x3 (rotate right by 12 bits) - for a 20-bit output audio data
  - 0x4 (rotate right by 16 bits) - for a 16-bit output audio data
- MCASP_XFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_XMASK[32] XMASK = 0xFFFFFF00 – 0xFFFF0000
- MCASP_XFMT[14-13] XPAD = 0x0 (Pad extra bits with 0s.)

For right-aligned data, the following transmit format unit settings process the data into right-aligned audio data ready for transmission:

- MCASP_XFMT[2-0] XROT = 0x0 (rotate right by 0 bits regardless of the audio word length)
- MCASP_XFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_XMASK[32] XMASK = 0x00FFFFFF – 0x0000FFFF
- MCASP_XFMT[14-13] XPAD = 0x0 (Pad extra bits with 0s.)

The example settings provided in Table 12-5 should be applied to MCASP in cases of DIT-transmitting a Q31 data as a 24-bit, 20-bit and 16-bit left- or right- aligned audio word, respectively. Note that the listed settings let the MCASP TFU preserve the most significant bits and cut only the LSBs of the original Q31 CPU data:

Table 12-5. MCASP TFU DIT-Mode Example Settings

Output Audio Word Alignment	Audio Word Length	Right-rotation (multiple of 4-bit positions)	XMASK	XROT
LEFT	16	16	0xFFFF0000	0x4
LEFT	20	12	0xFFFFF000	0x3
LEFT	24	8	0xFFFFFF00	0x2
RIGHT	16	0	0x0000FFFF	0x0
RIGHT	20	0	0x000FFFFF	0x0
RIGHT	24	0	0x00FFFFFF	0x0

Assuming that a Q31 data word 0xFA5AFxxx (where x-marked nibbles of the data are applied as padding bits of the word) is generated on the MCASP CFG (peripheral) port. To transmit a left-aligned 20-bit version of same word, preserving the MSBs, according to the Table 12-5, the user must set XMASK = 0xFFFFF000, and to select a right-rotation to 12 positions (XROT = 0x3).

- After applying 0-s (XPAD = 0) as masking-off bits at the first TFU stage, word is transformed to the word 0xFA5AF000.
- After a rotation by 12 positions to the right is performed in TFU, the 20-bit output word obtained is: 0x000FA5AF. Thus the word gets ready for transmission being mapped with its LS-bit as bit 8 and its MS-bit as bit 27 within a S/PDIF bitstream. This word is shifted in a LSB-to-MSB order (XRVRS = 0x0) out of the XRSR register during a DIT-transmission.

Assuming that a right-aligned Q31 data word - 0x yyyyE4B4 is generated by software on the MCASP CFG (peripheral) port (with the presumption that y-marked nibbles of the input data are applied as padding bits). To transmit a right-aligned 16-bit version of same word, preserving the MSBs, according to the table MCASP TFU Example Settings, user is supposed to set XMASK = 0x0000FFFF, and to select right-rotation to 0 positions (XROT = 0x0).

- After masking-off with 0s at first TFU stage, word is transformed to 0x0000E4B4.
- Since no rotation is applied, the 16-bit output word obtained is actually the one obtained in the masking stage – 0x0000E4B4.

The above examples use internal representation in integer and Q31 notation, but other fractional notations are also possible.

12.1.1.4.4.2 Receive Format Unit

The MCASP receive formatting unit consists of three stages:

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB first or LSB first)

Figure 12-17 shows the receive format unit (RFU).

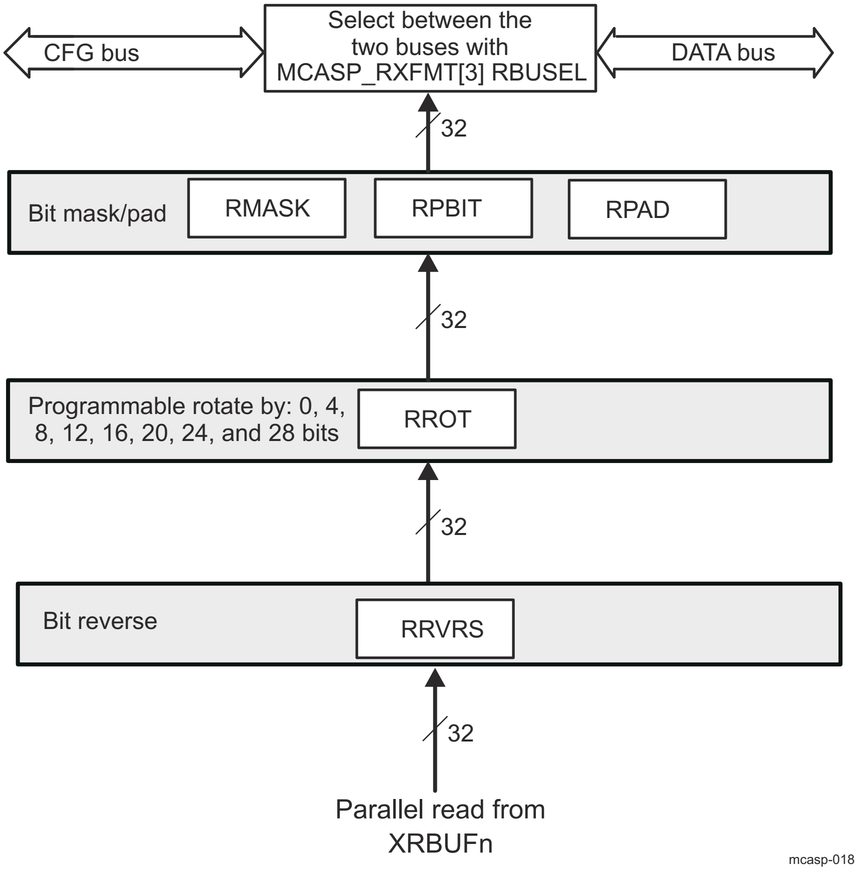

Figure 12-17. Receive Format Unit

The MCASP receiver supports serial formats of:

- Slot or time slot size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size ≤ Slot size
- Alignment when more bits are available per slot than bits per word within the slot, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:
  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

Hardware support for these serial formats comes from the programmable options in the receive bitstream format register - MCASP_RFMT:

- RRVRS: bit reverse (1) or no bit reverse (0)
- RROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- RSSZ: receive slot size of 8, 12, 16, 20, 24, 28, or 32 bits

As shown on Figure 12-17, the data processed in the RFU can be output to host CPU through the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_RFMT[3] RBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 12.1.1.4.10.1.3 , *Transfers Through the DATA Port*, and Section 12.1.1.4.10.1.4 , *Transfers Through the Configuration (CFG) Bus*.

12.1.1.4.4.2.1 TDM Mode Reception Data Alignment Settings

RSSZ should always be programmed to match the slot size of the serial stream.

Note

Note that the word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the RROT field.

Table 12-6 shows the RRVRS and RROT fields for each serial format and for both integer and Q31 fractional internal representations.

Table 12-6. MCASP RFU Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_RFMT bits	
			RROT[1]	RRVRS
MSB first[2]	Left aligned	Q31 fraction	SLOT	1
MSB first	Right aligned	Q31 fraction	WORD	1
LSB first	Left aligned	Q31 fraction	(32 - (SLOT - WORD)) % 32	0
LSB first	Right aligned	Q31 fraction	0	0
MSB first[2]	Left aligned	Integer	SLOT - WORD	1
MSB first	Right aligned	Integer	0	1
LSB first	Left aligned	Integer	32 - SLOT	0
LSB first	Right aligned	Integer	32 - WORD	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator

(2) To receive in I2S format, select MSB first, left aligned, and also select RDATDLY = 01 (1 bit delay)

The Table 12-6 assumes that all slot size and word size options are multiples of 4; since the receive rotate right unit only supports rotation by multiples of 4. However, the bit mask/pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be received in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1. The receive bit mask/pad unit operates on data as the final step of the receive format unit (see Figure 12-17), and the data is aligned in the same representation as it is read from the receiver (typically Q31 or integer).

12.1.1.4.5 MCASP State-Machines

The receive and transmit sections have independent state machines.

Each state-machine controls the interactions between the various units in the MCASP Rx and Tx sections, respectively. In addition, each state-machine keeps track of error conditions and serial port status. No serial transfers can occur until the RX/TX state-machine is released from reset.

The transmit state-machine is controlled by the transmit bitstream format register (MCASP_XFMT) and it reports the MCASP status and error conditions in the transmitter status register (MCASP_XSTAT).

Similarly, the receive state-machine is controlled by the receive bitstream format register (MCASP_RFMT) and it reports the MCASP status and error conditions in the receiver status register (MCASP_RSTAT).

12.1.1.4.6 MCASP TDM Sequencers

There are separate TDM sequencers for the transmit section and the receive section. Each TDM sequencer keeps track of the slot count. In addition, the TDM sequencer checks the bits of the MCASP_RTDM/ MCASP_XTDM register and determines if the MCASP should receive/transmit in that time slot.

There are two possibilities for a slot: The MCASP either performs Rx/Tx operations during the time slot (transmit/ receive bit is active), or the MCASP skips Rx/Tx operations during the time slot (transmit/receive bit is inactive).

In the latter case, no transfers between the XRBUF and XRSR registers in the serializer would occur during that time slot.

In addition, during time of inactive slots, the serializers programmed as transmitters place their data output pins - AXRn in a predetermined state - logic low, high, or high impedance (tri-stated) as programmed in each serializer control MCASP_SRCTLn[3-2] DISMOD register. Refer also to Section 12.1.1.4.9.2.1 , *TDM Time Slots Generation and Processing*, for details on how DMA event or interrupt generations are handled during inactive time slots in TDM mode.

In case of a DIT-transmission (S/PDIF transfers): the time division multiplexing (TDM) sequencer is used to count the 384 subframes (slots) in the DIT block. If currently transmitting slot 1, slot 2 (next value of the TDM slot counter) should be used during the encode phase to select the appropriate C, V, and U bit, because the data encoded and written to a MCASP_XBUFn register during the current time slot (slot 1) is actually shifted out on the next time slot (n = 0 to 15).

The transmit TDM sequencer is controlled by the MCASP_XTDM register and reports the current transmit slot to the MCASP_XTDMSLOT[9-0] XSLOTCNT bit field.

12.1.1.4.7 MCASP Software Reset

The MCASP can be put into reset through the global transmit and receive control register (*MCASP_GBLCTL*). A valid serial clock must be supplied to the MCASP to assert the software reset bits in the *MCASP_GBLCTL* register.

12.1.1.4.8 MCASP Power Management

Table 12-7 describes power-management features available to the MCASP.

Table 12-7. Local Power-Management Features

Feature	Registers	Description
Target clock stop modes	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	Force-clock stop, no-clock stop, and smart-clock stop modes are available.

CAUTION

No wakeup schema is supported for the MCASP. To ensure a correct behavior after enabling MCASP at device Device Configuration level, the user software is strongly recommended to choose *No Idle* mode, setting *MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE bit field to 0x1. Before disabling MCASP at device Device Configuration level, user software is strongly recommended to choose a *Smart-Idle* mode, setting *MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE bit field to 0x2.

12.1.1.4.9 MCASP Transfer Modes

12.1.1.4.9.1 Burst Transfer Mode

The MCASP supports a burst transfer mode, which is useful for nonaudio data such as passing control information between two processors. Burst transfer mode uses a synchronous serial format similar to the TDM mode. The frame sync generation is not periodic or time-driven as in TDM mode, but data driven, and the frame sync is generated for each data word transferred.

When operating in burst frame sync mode (see Figure 12-18), as specified for transmit (MCASP_AFSXCTL[15-7] = 0) and receive (MCASP_AFSRCTL[15-7] RMOD = 0), one slot is shifted for each active edge of the frame sync signal that is recognized. Additional clocks after the slot and before the next frame sync edge are ignored.

In burst frame sync mode, the frame sync delay may be specified as 0, 1, or 2 serial clock cycles. This is the delay between the frame sync active edge and the start of the slot. The frame sync signal lasts for a single bit clock duration (MCASP_AFSRCTL[4] FRWID = 0, MCASP_AFSXCTL[4] FXWID = 0).

For transmit, when generating the transmit frame sync internally, the frame sync begins when the previous transmission has completed and when all the XBUFn (for every serializer set to operate as a transmitter) has been updated with new data.

For receive, when generating the receive frame sync internally, frame sync begins when the previous transmission has completed and when all the RBUFn (for every serializer set to operate as a receiver) has been read.

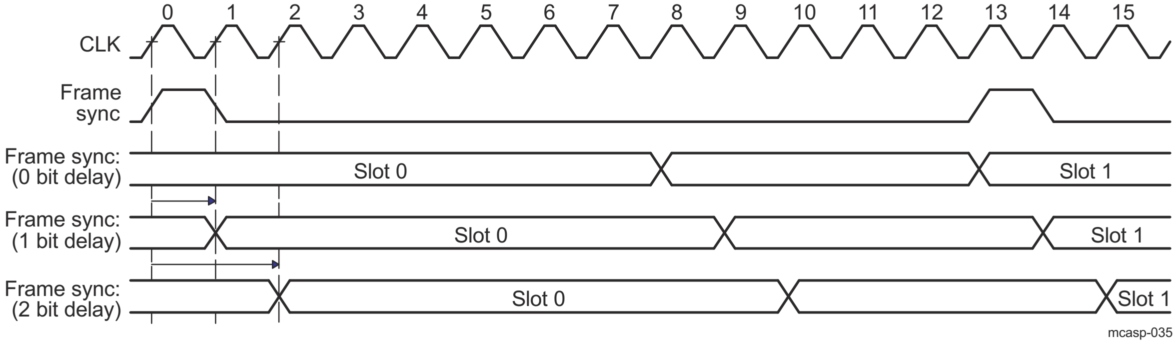

Figure 12-18. Burst Frame Sync Mode

The control registers must be configured as follows for the burst transfer mode. The burst mode specific bit fields are in bold face:

- *MCASP_PFUNC*: The clock, frame, data pins must be configured for MCASP function.
- *MCASP_PDIR*: The clock, frame, data pins must be configured to the direction desired.
- *MCASP_PDOUT*, *MCASP_PDIN*, *MCASP_PDCLR*: Not applicable. Leave at default.
- *MCASP_GBLCTL*: Follow the initialization sequence in Section 12.1.1.5.1.2 , *MCASP Global Initialization*, to configure this register.
- *MCASP_AMUTE*: Not applicable. Leave at default.
- MCASP_DLBCTL: If loopback mode is desired, configure this register according to Section 12.1.1.4.14 , *MCASP Loopback Modes*, otherwise leave this register at default.
- MCASP_DITCTL: DITEN must be left at default 0 to select non-DIT mode. Leave the register at default.
- MCASP_RMASK/MCASP_XMASK: Mask desired bits according to Section 12.1.1.4.4 , *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Program all fields according to data format desired. See Section 12.1.1.4.4 , *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Clear RMOD/XMOD bits to 0 to indicate burst mode. Clear FRWID/FXWID bits to 0 for single bit frame sync duration. Configure other fields as desired.
- *MCASP_ACLKRCTL/MCASP_ACLKXCTL*: Program all fields according to bit clock desired. See Section 12.1.1.4.2 , *MCASP Clock and Frame-Sync Configurations*.
- *MCASP_AHCLKRCTL/MCASP_AHCLKXCTL*: Program all fields according to high-frequency clock desired. See Section 12.1.1.4.2 , *MCASP Clock and Frame-Sync Configurations*.
- MCASP_RTDM/MCASP_XTDM: Program RTDMS0/XTDMS0 to 1 to indicate one active slot only. Leave other fields at default.
- MCASP_RINTCTL/MCASP_XINTCTL: Program all fields according to interrupts desired.
- MCASP_RCLKCHK/MCASP_XCLKCHK: Not applicable. Leave at default.
- MCASP_SRCTLn: Program SRMOD to inactive/transmitter/receiver as desired. DISMOD is not applicable and should be left at default (n = 0 to 15).
- MCASP_DITCSRAi, MCASP_DITCSRBi, MCASP_DITUDRAi, MCASP_DITUDRBi: Not applicable. Leave at default (i = 0 to 5).

12.1.1.4.9.2 Time-Division Multiplexed (TDM) Transfer Mode

The MCASP time-division multiplexed (TDM) transfer mode supports the TDM format discussed in Section 12.1.1.2.2.3 , *TDM Format*.

Transmitting data in the TDM transfer mode requires a minimum set of pins:

- ACLKX - transmit bit clock
- AFSX - transmit frame sync (or commonly called left/right clock)
- One or more serial data pins, AXRn, whose serializers are configured to transmit

For more details on MCASP transmitting serializers clock and frame sync options, refer to the Section 12.1.1.4.2.1 , *Transmit Clock*, and Section 12.1.1.4.2.3 , *Frame-Sync Generator*.

Similarly, to receive data in the TDM transfer mode requires a minimum set of pins:

- ACLKR - receive bit clock
- AFSR - receive frame sync (or commonly called left/right clock)
- One or more serial data pins, AXRn, whose serializers are configured to receive

For more details on MCASP receiving serializers clock and frame sync options, refer to Section 12.1.1.4.2.2 , *Receive Clock*, and Section 12.1.1.4.2.3 , *Frame-Sync Generator*.

The control registers must be configured as follows for the TDM mode. The TDM mode specific bit fields are highlighted in bold:

- *MCASP_PFUNC*: The clock, frame, data pins must be configured for MCASP function.
- *MCASP_PDIR*: The clock, frame, data pins must be configured to the direction desired.
- *MCASP_PDOUT*, *MCASP_PDIN*, *MCASP_PDCLR*: Not applicable. Leave at default.
- *MCASP_GBLCTL*: Follow the initialization sequence is described in the Section 12.1.1.5.2 , *MCASP Operational Modes Configuration*.
- *MCASP_AMUTE*: Leave this register at default state.
- MCASP_DLBCTL: If loopback mode is desired, configure this register according to Section 12.1.1.4.14 , otherwise leave this register at default.
- MCASP_DITCTL: DITEN must be left at default 0 to select TDM mode (transmitters only).
- MCASP_RMASK/MCASP_XMASK: Mask desired bits according to Section 12.1.1.4.4 , *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Program all fields according to data format desired. See the Section 12.1.1.4.4 , *MCASP Format Units*.
- MCASP_AFSRCTL/MCASP_AFSXCTL: Set RMOD/XMOD bits to (0x2 - 0x20) for Rx/Tx (2- 32 slots) TDM mode. In addition, set RMOD to 0x180 if 384-slot TDM stream has to be received by MCASP. Configure other fields as desired.
- *MCASP_ACLKRCTL/MCASP_ACLKXCTL*: Program all fields according to bit clock desired. For more inforamtion, refer to Section 12.1.1.4.2 , *MCASP Clock and Frame-Sync Configurations*.
- *MCASP_AHCLKRCTL/MCASP_AHCLKXCTL*: Program all fields according to high-frequency clock desired. For more details, refer to Section 12.1.1.4.2 , *MCASP Clock and Frame-Sync Configurations*.
- MCASP_RTDM/MCASP_XTDM: Program all fields according to the time slot characteristics desired.
- MCASP_XINTCTL: Program all fields according to transmit interrupts desired.
- MCASP_RCLKCHK/MCASP_XCLKCHK: Program all fields according to clock checking desired.
- MCASP_SRCTLn: Program all fields according to serializer operation desired (n = 0 to 15).

Note

The MCASP_DITCSRAi, MCASP_DITCSRBi, MCASP_DITUDRAi, MCASP_DITUDRBi (i = 0 to 5) settings are NOT applicable in TDM transfer modes. They have to be kept at their default values.

12.1.1.4.9.2.1 TDM Time Slots Generation and Processing

TDM mode on the MCASP can extend to support multiprocessor applications, with up to 32 time slots per frame. For each of the time slots, the MCASP may be configured to participate or to be inactive by configuring MCASP_XTDM and/or MCASP_RTDM registers.

The TDM sequencer (separate ones for transmit and receive) functions in this mode. The TDM sequencer counts the slots beginning with the frame sync. For each slot, the TDM sequencer checks the respective bit in either MCASP_XTDM or MCASP_RTDM register to determine if the MCASP transmits/receives in that time slot.

Note

If a MCASP_XTDM/MCASP_RTDM bit defines an active slot (number of slot matches the bit position), the MCASP functions normally during that time slot; otherwise, the MCASP is inactive during that time slot; no update to the buffer occurs, and no event is generated. MCASP (transmit only) data pins are automatically set to a high-impedance state, 0, or 1 during that slot, as determined by bitfield MCASP_SRCTLn[3-2] DISMOD (n = 0 to 15).

Figure 12-19 shows when the transmit DMA event - XINT is generated. See Section 12.1.1.4.10.1 , *Data Ready Status and Event/Interrupt Generation* for details on data ready and the initialization period indication. The transmit DMA event for an active time slot (slot N) is generated during the previous time slot (slot N - 1), regardless of the previous time slot (slot N - 1) being active or inactive.

During an active transmit time slot (slot N), if the next time slot (slot N + 1) is configured to be active, the copy from XRBUFn to XRSRn generates the DMA event for time slot N + 1. If the next time slot (slot N + 1) is configured to be inactive, then the DMA event will be delayed to time slot M - 1. In this case, slot M is the next active time slot. The DMA event for time slot M is generated during the first bit time of slot M - 1.

The receive DMA event is generated after data is received in the buffer (looks back in time). If a time slot is disabled, then no data is copied to the buffer for that time slot and no DMA event is generated.

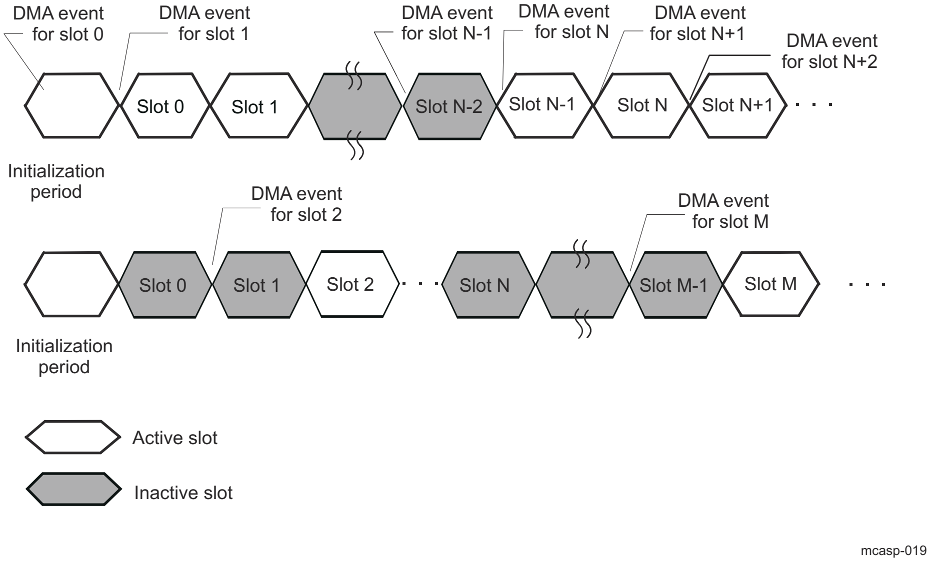

Figure 12-19. Transmit DMA Event (XINT) Generation in TDM Time Slots

12.1.1.4.9.2.2 Special 384-Slot TDM Mode for Connection to External DIR

The MCASP receiver also supports a 384 time slot TDM mode (DIR mode), to support S/PDIF receiver ICs whose natural block (block corresponds to MCASP frame) size is 384 samples. The receive TDM time slot register (MCASP_RTDM) should be programmed to all 1s during reception of a DIR block. Other TDM functionalities (for example, inactive slots) are not supported (only the slot counter counts the 384 subframes in a block). To receive data in DIR mode, the following pins are typically needed:

- ACLKR - receive bit clock
- AFSR - receive frame sync (or commonly called left/right clock)
- In this mode, AFSR should be connected to a DIR which outputs a start of block signal, instead of LRCLK

- One or more serial data pins, AXRn, whose serializers have been configured to receive
- For this special DIR mode, the control registers can be configured just as for TDM mode, except set MCASP_AFSRCTL[15-7] RMOD bit field to 384 (0x180) to receive 384 time slots

12.1.1.4.9.3 DIT Transfer Mode

The DIT transfer mode of the MCASP also supports transmission of audio data in S/PDIF, AES-3, and IEC-60958 formats. These formats are designed to carry audio data between different systems through an optical or coaxial cable. The DIT mode applies only to a serializer configured as transmitter, not as receiver. For a description of the S/PDIF format, see Section 12.1.1.2.2.5 , *S/PDIF Coding Format*.

12.1.1.4.9.3.1 Transmit DIT Encoding

When the MCASP operates in DIT mode, the data transmitted is output as a biphase-mark encoded bitstream, with preamble, channel status, user data, validity, and parity automatically stuffed into the bitstream by the MCASP. The MCASP includes separate validity bits for even/odd subframes and two 384-bit RAM modules to hold channel status and user data bits.

Note

The transmit TDM time slot register (MCASP_XTDM) should be programmed to all 1s during DIT mode. TDM functionality is not supported in DIT mode, except that the TDM slot counter counts the DIT subframes.

To transmit data in DIT mode, the following pins are typically required:

- AHCLKX – transmit high-frequency controller clock (The internal clock source can be used instead.)
- One serial data pin (AXRn) of a serializer n configured to transmit.

For DIT Mode Transmission Data Alignment Settings see Section 12.1.1.4.4.1.2 , *DIT Mode Transmission Data Alignment Settings*.

If the MCASP is configured to transmit in the DIT mode on more than one serial data pin, the bit streams on all pins will be synchronized. In addition, although they will carry unique audio data, they will carry the same channel status, user data, and validity information.

The actual 24-bit audio data must always be in bit positions 23–0 after passing through the first three stages of the transmit format unit.

12.1.1.4.9.3.2 Transmit DIT Clock and Frame-Sync Generation

The DIT transmitter works only in the following configuration:

- In the transmit frame control register (MCASP_AFSXCTL):
  - Internally generated transmit frame sync, FSXM = 1
  - Rising-edge frame sync, FSXP = 0
  - Bit-width frame sync, FXWID = 0
  - 384-slot TDM, XMOD = 1 1000 0000b
- In the transmit clock control register (*MCASP_ACLKXCTL*), ASYNC = 1
- In the transmit bitstream format register (MCASP_XFMT), XSSZ = 1111 (32-bit slot size)

All combinations of AHCLKX and ACLKX are supported.

The following summarizes the register configurations required for DIT mode. DIT mode-specific bit fields are in bold face:

- *MCASP_PFUNC*: The data pin - AXRn must be configured for MCASP function. If AHCLKX is used, it must also be configured for MCASP function. Other pins can be configured to function as GPIOs, if desired.
- *MCASP_PDIR*: The data pin must be configured as output. If internal clock source AUXCLK is used as the reference clock, it may be output as the AHCLKX device level signal by configuring AHCLKX pin as an output.

- *MCASP_GBLCTL*: Global initialization
- *MCASP_AMUTE*: Leave this register at default state.
- MCASP_DITCTL: The DITEN bit must be set to 0b1 to enable DIT mode. Configure other bits as desired.
- MCASP_XMASK: Mask the desired bits, depending upon left-aligned or right-aligned internal data.
- MCASP_XFMT: XDATDLY = 0. XRVRS = 0. XPAD = 0. XSSZ = Fh (32-bit slot). XBUSEL = configured as desired. The XROT bit is configured, as described in the Section 12.1.1.4.4.1.2 .
- MCASP_AFSXCTL: Configure the bits according to former discussions.
- *MCASP_ACLKXCTL*: ASYNC = 1. Program the CLKXDIV bits to obtain the bit clock rate desired. CLKXM = 1.
- *MCASP_AHCLKXCTL*: Program the HCLKXDIV bits to obtain the high-frequency bit clock rate desired.
- MCASP_XTDM: Set to FFFF FFFFh for all active slots for DIT transfers.
- MCASP_XINTCTL: Program all fields according to the interrupts desired.
- MCASP_XCLKCHK: Program all fields according to the clock checking desired.
- MCASP_SRCTLn: Set SRMOD = 1 (transmitter) for the DIT pins (n = 0 to 15).
- MCASP_DITCSRAi and MCASP_DITCSRBi: Program the channel status bits as desired (i = 0 to 5).
- MCASP_DITUDRAi and MCASP_DITUDRBi: Program the user data bits as desired (i = 0 to 5).

Note

In DIT mode, the transmitter can support a 192 kHz frame rate (stereo) on up to 2 serial data pins simultaneously (note that the internal bit clock for DIT runs two times faster than the equivalent bit clock for TDM (I2S) mode, due to the need to generate Biphase Mark Encoded Data - see Section 12.1.1.2.2.5.1 , *Biphase-Mark Code*).

12.1.1.4.9.3.3 DIT Channel Status and User Data Register Files

The channel status registers (MCASP_DITCSRAi and MCASP_DITCSRBi) and user data registers (MCASP_DITUDRAi and MCASP_DITUDRBi) are not double-buffered. Typically, programmers use one of the synchronizing interrupts, such as the last slot, to create an event at a safe time so the register may be updated. In addition, the software reads the transmit TDM slot counter to determine which word of the register is being used (i = 0 to 5).

It is a software requirement to avoid writing to the word of user data and channel status that are being used to encode the current time slot; otherwise, it is undetermined whether old or new data is used to encode the bitstream.

The DIT subframe format is defined in Section 12.1.1.2.2.5.2 , *S/PDIF Subframe Format*. The channel status information (C) and user data (U) are defined in the following DIT control registers:

- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the channel status information for the left channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the channel status information for the right channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the user data information for the left channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the user data information for the right channel within each frame.
- The S/PDIF block format is shown in Figure 12-10. There are 192 frames within a block (frame 0 to frame 191). There are two subframes within each frame (subframes 1 and 2 for the left and right channels, respectively).

The channel status and user data information sent on each subframe is summarized in Table 12-8.

Table 12-8. Channel Status and User Data for Each DIT Block

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
Defined by DITCSRA0, DITCSRB0, DITUDRA0, DITUDRB0				
0	1 (L)	B	DITCSRA0[0]	DITUDRA0[0]

Table 12-8. Channel Status and User Data for Each DIT Block (continued)

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
0	2 (R)	W	DITCSRB0[0]	DITUDRB0[0]
1	1 (L)	M	DITCSRA0[1]	DITUDRA0[1]
1	2 (R)	W	DITCSRB0[1]	DITUDRB0[1]
2	1 (L)	M	DITCSRA0[2]	DITUDRA0[2]
2	2 (R)	W	DITCSRB0[2]	DITUDRB0[2]
…	…	…	…	…
31	1 (L)	M	DITCSRA0[31]	DITUDRA0[31]
31	2 (R)	W	DITCSRB0[31]	DITUDRB0[31]
Defined by DITCSRA1, DITCSRB1, DITUDRA1, DITUDRB1				
32	1 (L)	M	DITCSRA1[0]	DITUDRA1[0]
32	2 (R)	W	DITCSRB1[0]	DITUDRB1[0]
…	…	…	…	…
63	1 (L)	M	DITCSRA1[31]	DITUDRA1[31]
63	2 (R)	W	DITCSRB1[31]	DITUDRB1[31]
Defined by DITCSRA2, DITCSRB2, DITUDRA2, DITUDRB2				
64	1 (L)	M	DITCSRA2[0]	DITUDRA2[0]
64	2 (R)	W	DITCSRB2[0]	DITUDRB2[0]
…	…	…	…	…
95	1 (L)	M	DITCSRA2[31]	DITUDRA2[31]
95	2 (R)	W	DITCSRB2[31]	DITUDRB2[31]
Defined by DITCSRA3, DITCSRB3, DITUDRA3, DITUDRB3				
96	1 (L)	M	DITCSRA3[0]	DITUDRA3[0]
96	2 (R)	W	DITCSRB3[0]	DITUDRB3[0]
…	…	…	…	…
127	1 (L)	M	DITCSRA3[31]	DITUDRA3[31]
127	2 (R)	W	DITCSRB3[31]	DITUDRB3[31]
Defined by DITCSRA4, DITCSRB4, DITUDRA4, DITUDRB4				
128	1 (L)	M	DITCSRA4[0]	DITUDRA4[0]
128	2 (R)	W	DITCSRB4[0]	DITUDRB4[0]
…	…	…	…	…
159	1 (L)	M	DITCSRA4[31]	DITUDRA4[31]
159	2 (R)	W	DITCSRB4[31]	DITUDRB4[31]
Defined by DITCSRA5, DITCSRB5, DITUDRA5, DITUDRB5				
160	1 (L)	M	DITCSRA5[0]	DITUDRA5[0]
160	2 (R)	W	DITCSRB5[0]	DITUDRB5[0]
…	…	…	…	…
191	1 (L)	M	DITCSRA5[31]	DITUDRA5[31]
191	2 (R)	W	DITCSRB5[31]	DITUDRB5[31]

12.1.1.4.10 MCASP Data Transmission and Reception

The MCASP is serviced by writing data to the MCASP_XBUFn registers for transmit operations, and by reading data from the MCASP_RBUFn registers for receive operations. The MCASP sets status flags and notifies the software whenever data is ready to be serviced. The Section 12.1.1.4.10.1 , *Data Ready Status and Event/ Interrupt Generation*, discusses data-ready status in details (n = 0 to 15).

The MCASP transmit/receive XRBUFn buffer can be accessed through one of the two peripheral ports of the device:

- DATA port: This port is dedicated to DMA initiated data transfers on the device for MCASP transmit (Tx) purposes.
- Configuration bus (CFG): The configuration bus- CFG port is used for peripheral configuration control and receive/transmit data transfers initiated by the host CPU in the device.

Section 12.1.1.4.10.1.3 , *Transfers Through the Data Port (DATA)*, and Section 12.1.1.4.10.1.4 , *Transfers Through the Configuration Bus (CFG),* discuss how to perform transfers through the data port (DATA) and the configuration port (CFG), respectively.

A device CPU and DMA usages are discussed in Section 12.1.1.4.10.1.5 , *Using the device CPUs for MCASP Servicing*, and Section 12.1.1.4.10.1.6 , *Using the DMA for MCASP Servicing*, respectively.

MCASP DATA port allows DMAs to access the MCASP transmit buffer more efficiently on the CBASS0, using burst transfers. The physical addresses to access these registers are listed in *DMA Registers*.

12.1.1.4.10.1 Data Ready Status and Event/Interrupt Generation

12.1.1.4.10.1.1 Transmit Data Ready

The transmit data ready flag - XDATA in the MCASP_XSTAT register reflects the data ready status of XRBUFn buffers for all of the active slot transmitting serializers. The XDATA flag is set whenever data is transferred from a transmitting serializer buffer - XRBUFn to its corresponding XRSRn shift register. Thus, the XDATA bit indicates the global event that some of the serializers data buffer - XRBUFn is emptied and ready to accept new data from the host (CPU or DMA). The transmit data ready event is individually indicated per serializer in its corresponding control register MCASP_SRCTLn[4] XRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Tx buffer must be serviced (written). When MCASP_XBUFn is written to by the host, the MCASP_SRCTLn[4] XRDY is deasserted to 0b0. As XDATA global flag is an OR-event of all active serializers XRDY flags, it indicates to software the moment, when write service operation has to be initiated by the MCASP host (XDATA=0b1). The XRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_XBUFn register has to be currently written. Once all requested MCASP_XBUFn are written, the serializers control XRDY flags are cleared to 0b0. As a consequence, XDATA flag is deasserted to 0b0, to indicate to SW that write operation is completed for all serializers.

The global XDATA flag can be cleared when the MCASP_XSTAT[5] XDATA bit is written to 0b1, or once MCASP_XBUFn registers of all the serializers, that have previously raised their XRDY flags, are written with corresponding active slot data by the host.

Whenever XDATA is set, the XINT event is automatically generated on MCASP[0-2]_XMIT_DMA_EVT line (if enabled in the *MCASP_XEVTCTL* register) to notify the DMA of the MCASP_XBUFn empty status. An interrupt - MCASP[0-2]_XMIT_INTR_PEND can be also generated if the XDATA interrupt is enabled in the MCASP_XINTCTL register (for details, see Section 12.1.1.4.12.1 , *Transmit Data Ready Interrupt*).

For DMA requests, the MCASP does not require that MCASP_XSTAT register be read between DMA events. This means that, even if MCASP_XSTAT register already has the XDATA flag set to 1 from a previous request, the next transfer triggers another DMA request.

Because the serializer acts in lockstep, only one DMA event is generated to indicate that the transmit serializer is ready to be written to with new data.

Figure 12-20 shows the timing details of when XINT is generated at the MCASP boundary. In this example, as soon as the last bit (A0) of word A is transmitted, the MCASP sets the XDATA flag and generates an XINT event. However, it takes up to five MCASP interface clocks (XINT latency) before XINT is active at the MCASP boundary. Upon XINT, the CPU can begin servicing the MCASP by writing word C into the MCASP_XBUFn (service time). The CPU must write word C into the MCASP_XBUFn within the setup time required by the MCASP (setup time) (n = 0 to 15).

The maximum service time (see Figure 12-20) can be calculated as:

Service Time = Time Slot – XINT Latency –Setup Time

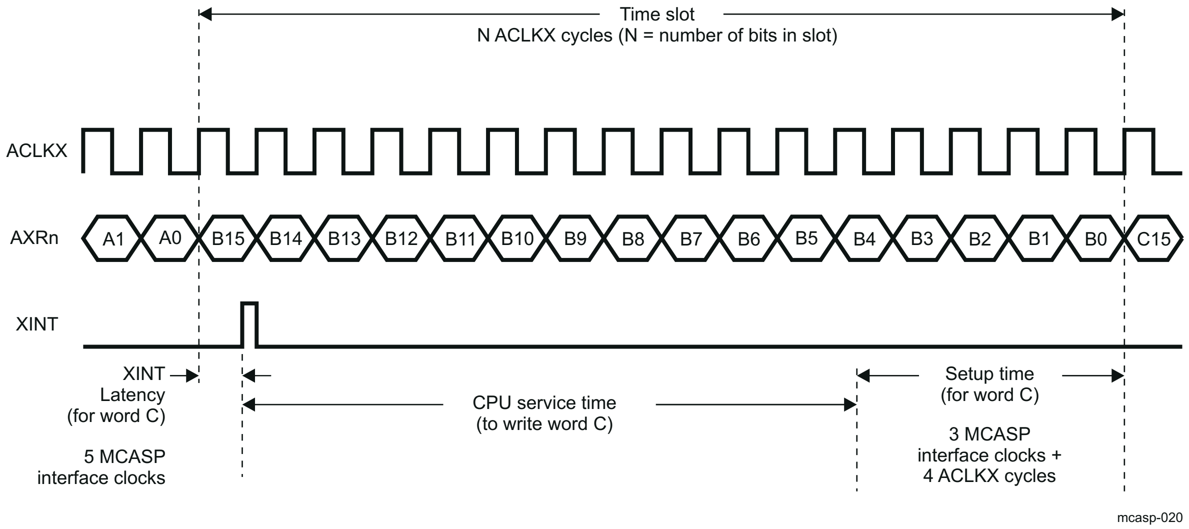

Figure 12-20. Service Time Upon Transmit DMA Event (XINT)

12.1.1.4.10.1.2 Receive Data Ready

Similarly, the receive data ready flag - RDATA in the MCASP_RSTAT register reflects the data ready status of XRBUFn buffers for all of the active slot receiving serializers. The RDATA flag is set whenever data is transferred from a receiving serializer shift register XRSRn to its corresponding XRBUFn data buffer. Thus, the RDATA bit indicates the global event that some of the receivers data buffer - RXBUFn already contains received data (this is, a buffer is full) and is ready to transfer it to the host. The receive data ready event is individually indicated per serializer in its corresponding control register MCASP_SRCTLn [5] RRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Rx buffer must be serviced (read). When MCASP_RBUFn register is read from the host, the MCASP_SRCTLn [5] RRDY bit is deasserted to 0b0. As RDATA global flag is an OR-event of all active serializers RRDY flags, it indicates to software the moment, when read service operation has to be initiated by the MCASP host (RDATA = 0b1). The RRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_RBUFn register has to be currently read. Once all requested MCASP_RBUFn registers are read, the serializers control RRDY flags are cleared to 0b0. As a consequence, RDATA flag is deasserted to 0b0, to indicate to SW that read operation is completed for all serializers.

The global RDATA flag can be cleared when the MCASP_RSTAT[5] RDATA bit is written to 0b1, or once MCASP_RBUFn registers of all the serializers, that have previously raised their RRDY flags, are read by the host.

Whenever RDATA flag is set, the RINT event is automatically generated on MCASP[0-2]_REC_DMA_EVT line (if enabled in the MCASP_PIDTCTL register) to notify the DMA of the MCASP_RBUFn full status. An interrupt - MCASP[0-2]_REC_INTR_PEND can be also generated if the RDATA interrupt is enabled in the MCASP_RINTCTL register (for details, see Section 12.1.1.4.12.1 , *Receive Data Ready Interrupt*).

Figure 12-21 shows the timing details of when RINT event is generated at the MCASP boundary. In this example, as soon as the last bit (bit A0) of Word A is received, the MCASP sets the RDATA flag and generates an RINT event. However, it takes up to five MCASP interface clocks (RINT Latency) before RINT is active at the MCASP boundary. Upon RINT, the CPU can begin servicing the MCASP by reading Word A from the MCASP_RBUFn (service time). The CPU must read Word A from the MCASP_RBUFn register no later than the setup time required by the MCASP (Setup Time) (n = 0 to 15).

The maximum service time (see Figure 12-21) can be calculated as:
Service Time = Time Slot - RINT Latency - Setup Time

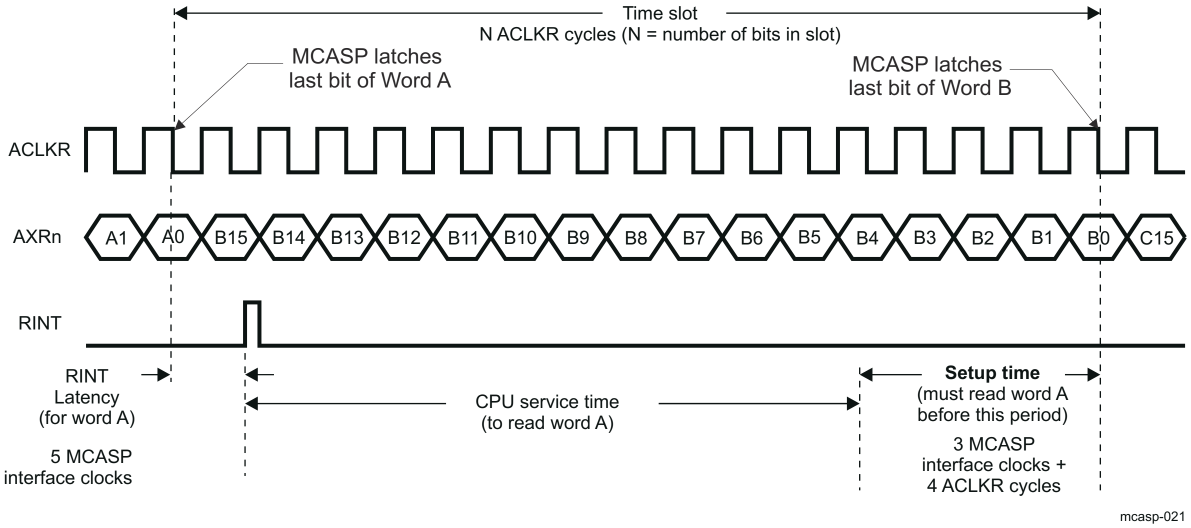

Figure 12-21. CPU Service Time Upon Receive Event (RINT)

12.1.1.4.10.1.3 Transfers Through the Data Port (DATA)

CAUTION

To perform internal transfers through the DATA port, clear the XBUSEL/RBUSEL bit to 0b0 in the MCASP_XFMT/MCASP_RFMT register, respectively. Failure to do so may result in software malfunction.

In a typical MCASP transfer scenario, the DMA Controller write accesses the XRBUFn transmit buffer through the MCASP data port (DATA) on CBASS0 Interconect. CPU hosts can access both XRBUFn transmit and receive data buffers on their corresponding DATA port address via DATA port corresponding address. To perform transfers through the DATA port, simply have the DMA Controller write the MCASP Tx buffer through Interconect DATA port location. Refer to *DMA Registers*. Although the transfer is passed through an integrated AFIFO transmit/receive buffer, the host (DMA or CPU) must follow the described below procedure to access the data buffers of each serializer, regardless the AFIFO is enabled or disabled. The AFIFO operation is described in Section 12.1.1.4.11 .

For accesses through the DATA port, the DMA/CPU services all the serializers through accessing only a single address. In addition, as can be seen in *DMA Registers*, the same physical DATA port address is used regardless of a read or write access is performed. The MCASP automatically cycles through the active slot transmitting/ receiving serializers, internally generating the appropriate offsets.

Note

DATA port allows the DMA/CPU to automatically access only the data buffers. There is no way for DMA/CPU to access the MCASP configuration registers addressing their corresponding MCASP DATA port.

For transmit operations through the DATA port, the host must always write to the same transmit buffer DATA port address (which is same than the receive buffer DATA port adress) to service all of the active slot transmitting serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the destination address to match the DATA port location of TXBUF buffer (See *DMA Registers*).

In addition, the DMA/CPU must write the buffers of all transmitting serializers in incremental (although not necessarily consecutive) order. For example, if only serializers 1 and 3 are set up as active transmitters, to the same transmit buffer DATA port address twice - first data for serializer 1 and second data for serializer 3 upon each transmit data ready event. This exact servicing order must be followed so that data appears in the appropriate serializers.

Note

For write transfers through MCASP DATA port it is preferable to use DMA on corresponding Interconect. This is because DMAs initiated traffic gets better advantage of the burst transfers supported by DATA port.

For receive operations through the DATA port, the DMA/CPU must always read from the same receive buffer DATA port address (which is same than the transmit buffer DATA port adress) to service all of the active slot receiving serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the DMA/CPU source address to match the DATA port location of RXBUF buffer (See *DMA Registers*).

In addition, reads from the receive buffer for all active slot receiving serializers through the Rx DATA port return data in incremental (although not necessarily consecutive) order. For example, if serializers 0, 1 and 3 are set up as active receivers, the CPU should read from the same receive buffer DATA port address three times to obtain data for serializers 0,1 and 3 in this exact order, upon each receive data ready event.

Note

To service a serializer for a transmit or receive operation through the MCASP DATA port, the initiator always writes (preferably DMA) and reads from the same address (refer to *DMA Registers*), respectively.

Note

When transmitting through the DATA port, the DMA/CPU must write data (at the same address) to each serializer configured as *active* (active slot selected in MCASP_XTDM) and *transmit* (Tx enabled in MCASP_SRCTLn) within each time slot. Failure to do so results in a buffer underrun condition (see Section 12.1.1.4.15.1 , *Buffer Underrun Error - Transmitter*). Similarly, when DMA/CPU receives, data must be read from each serializer configured as *active* (active slot selected in MCASP_RTDM) and *receive* (Rx enabled in MCASP_SRCTLn) within each time slot. Failure to do results in a buffer overrun condition (see Section 12.1.1.4.15.2 , *Buffer Overrun Error - Receiver*) (n = 0 to 15).

12.1.1.4.10.1.4 Transfers Through the Configuration Bus (CFG)

CAUTION

To perform internal transfers through the configuration bus, set the XBUSEL/RBUSEL bit to 1 in the MCASP_XFMT/MCASP_RFMT registers, respectively. Failure to do so may result in software malfunction.

Note

MCASP[0-2] whose data ports are accessible directly via CBASS0 do not support FIFO/constant addressing modes. Incrementing transfers must be used instead.

In this method, the CPU accesses the XRBUFn transmit or receive buffer through corresponding configuration bus (CFG) address.

The exact XRBUFn transmit/receive buffer physical address for any particular serializer is determined by adding the transmit/receive buffer alias register offset for that particular serializer to the base address of MCASP CFG port actual for CBASS0 accesses. The XRBUFn buffer of the n-th serializer configured as a transmitter is aliased - MCASP_XBUFn in the CFG port address space. For example, the XRBUF2 transmit buffer is mapped as the MCASP_XBUF2 register. Similarly, the XRBUFn buffer of the n-th serializer configured as a receiver is aliased - MCASP_RBUFn in the CFG port address space. For example, the XRBUF3 receive buffer is mapped as the MCASP_RBUF3 register.

Accessing the XRBUF through the DATA port (see Section 12.1.1.4.10.1.3) is different than CFG port accesses because the DATA port access demands the same physical address, regardless of transfer direction or current channel index , while accessing through the peripheral configuration port - CFG, the CPU must provide the exact MCASP_XBUFn or MCASP_RBUFn address upon accessing n-th serializer TX or RX buffer, respectively. For more details about MCASP_XBUFn and MCASP_RBUFn addresses corresponding to MCASP CFG port, see *CFG Registers* (n = 0 to 15).

12.1.1.4.10.1.5 Using a Device CPU for MCASP Servicing

The device CPUs can be used to service the MCASP transmit channels through interrupts (upon MCASP[0-2]_XMIT_INTR_PEND and MCASP[0-2]_REC_INTR_PEND interrupts). Because these interrupt events are connected to device COMPUTE_CLUSTER0, PRUSS, MAIN2MCU_LVL_INTRTR0, R5FSS0/1_INTRTR0, C66SS0/1_INTRTR0, R5FSS0/1 modules, they could be software mapped to input interrupt lines of any device CPU. Another way to service the transmit and receive channels, a polling of the XDATA bit in the MCASP_XSTAT register and RDATA bit in the MCASP_RSTAT register can be performed by device CPUs, respectively. As discussed in Section 12.1.1.4.10.1.3 , *Transfers Through the Data Port (DATA)*, and Section 12.1.1.4.10.1.4 , *Transfers Through the Configuration Bus (CFG)*, the device CPUs can access MCASP XRBUF serializer buffer through their corresponding DATA and CFG port locations.

To use the device CPUs to service the MCASP through interrupts, the XDATA/RDATA bit must be enabled in the respective MCASP_XINTCTL/MCASP_RINTCTL registers, to generate interrupts MCASP[0-2]_XMIT_INTR_PEND/MCASP[0-2]_REC_INTR_PEND to the device CPUs upon data ready

12.1.1.4.10.1.6 Using the DMA for MCASP Servicing

Note

The associated static Transfer Request (TR) operations of PDMA0, located in front of MCASP, must be configured to match the MCASP configuration. For more information, refer to chapter *DMA Controllers*.

The typical scenario is to use the DMA to service the MCASP transmit and receive logic through the DATA port. The transfer passes through integrated AFIFO transmit/receive buffer. If AFIFO is enabled, DMA requests are collected and fed to a device DMA controller (see Figure 12-11). The data transfer is managed by the AFIFO according to generated transmit and receive events in the MCASP and data is fed to transmit buffers and fetched from receive buffers as described in Section 12.1.1.4.11 , *MCASP Audio FIFO (AFIFO)*. The generation of transmit and receive request is described below. After generation of transmit/receive DMA events from MCASP module, these events are collected in AFIFO and on specific AFIFO conditions described in Section 12.1.1.4.11 , *MCASP Audio FIFO (AFIFO)* the requests (transmit or receive) are forwarded to a DMA controller via MCASP[0-2]_XMIT_DMA_EVT and MCASP[0-2]_REC_DMA_EVT outputs. If the AFIFO is disabled (default state) it is transperrant for the MCASP module and all request are directly sent to the DMA controller.

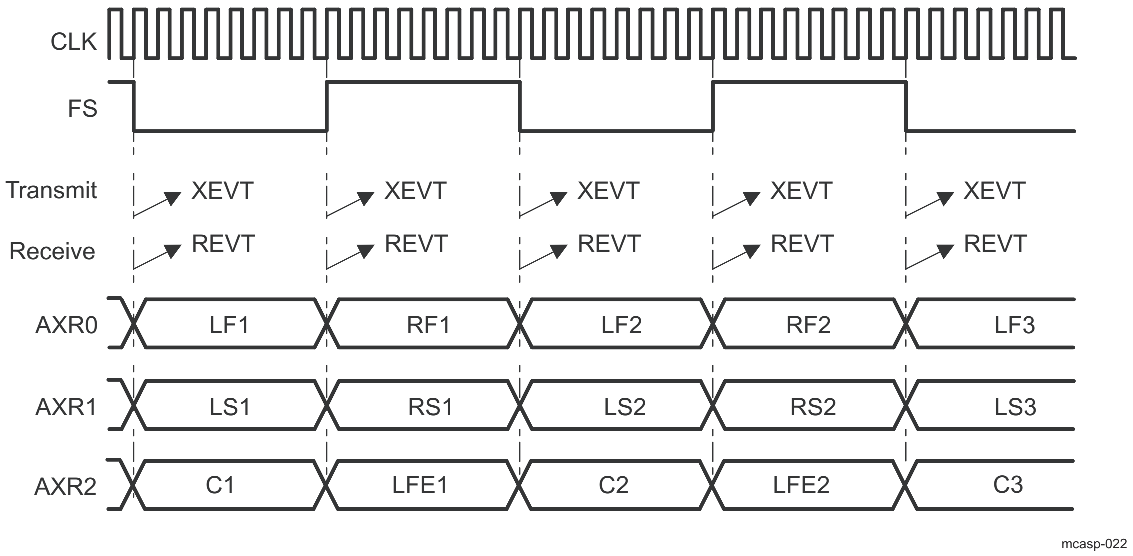

Figure 12-22. DMA Transmit and Receive Event in an Audio Example – One Event

In transmit mode, the DMA event - XINT (MCASP[0-2]_XMIT_DMA_EVT output), which is triggered upon each XDATA transition from 0 to 1, is used to service the MCASP TXBUFn transmit buffers. In receive mode, the DMA event RINT (MCASP[0-2]_REC_DMA_EVT output) which is triggered upon each RDATA transition from 0 to 1, is used to service the MCASP RXBUFn receive buffers.

Figure 12-22 is an example of an audio system with six audio channels (LF, RF, LS, RS, C and LFE) transmitted or received through the MCASP signals - AXR0, AXR1 and AXR2. It shows the points at which events XINT/ RINT are triggered.

In Figure 12-22, a Tx DMA event XINT is triggered on each time slot. In the example, XINT is triggered for each of the transmit audio channel time slot (time slot for channels LF, LS, and C; and time slot for channels RF, RS, LFE). Transmit DMA events are generated automatically upon transmit data ready, provided that DMA TX requests generation is enabled in the *MCASP_XEVTCTL* register. Similarly, Rx DMA event RINT is triggered for each of the receive audio channel time slot. Receive DMA events are generated automatically upon receive data ready, provided that DMA RX requests generation is enabled in the MCASP_PIDTCTL register.

12.1.1.4.11 MCASP Audio FIFO (AFIFO)

The AFIFO contains two FIFOs: one Read FIFO (RFIFO), and one Write FIFO (WFIFO). The RFIFO and the WFIFO are the same size: 64 32-bit Words. To ensure backward compatibility with existing software, both the Read and Write FIFOs are disabled by default. See Figure 12-23 for a high-level block diagram of the AFIFO. The AFIFO may be enabled/disabled and configured via the MCASP_WFIFOCTL and MCASP_RFIFOCTL registers. Note that if the Read or Write FIFO is to be enabled, it must be enabled prior to initializing the receive/ transmit section of the MCASP.

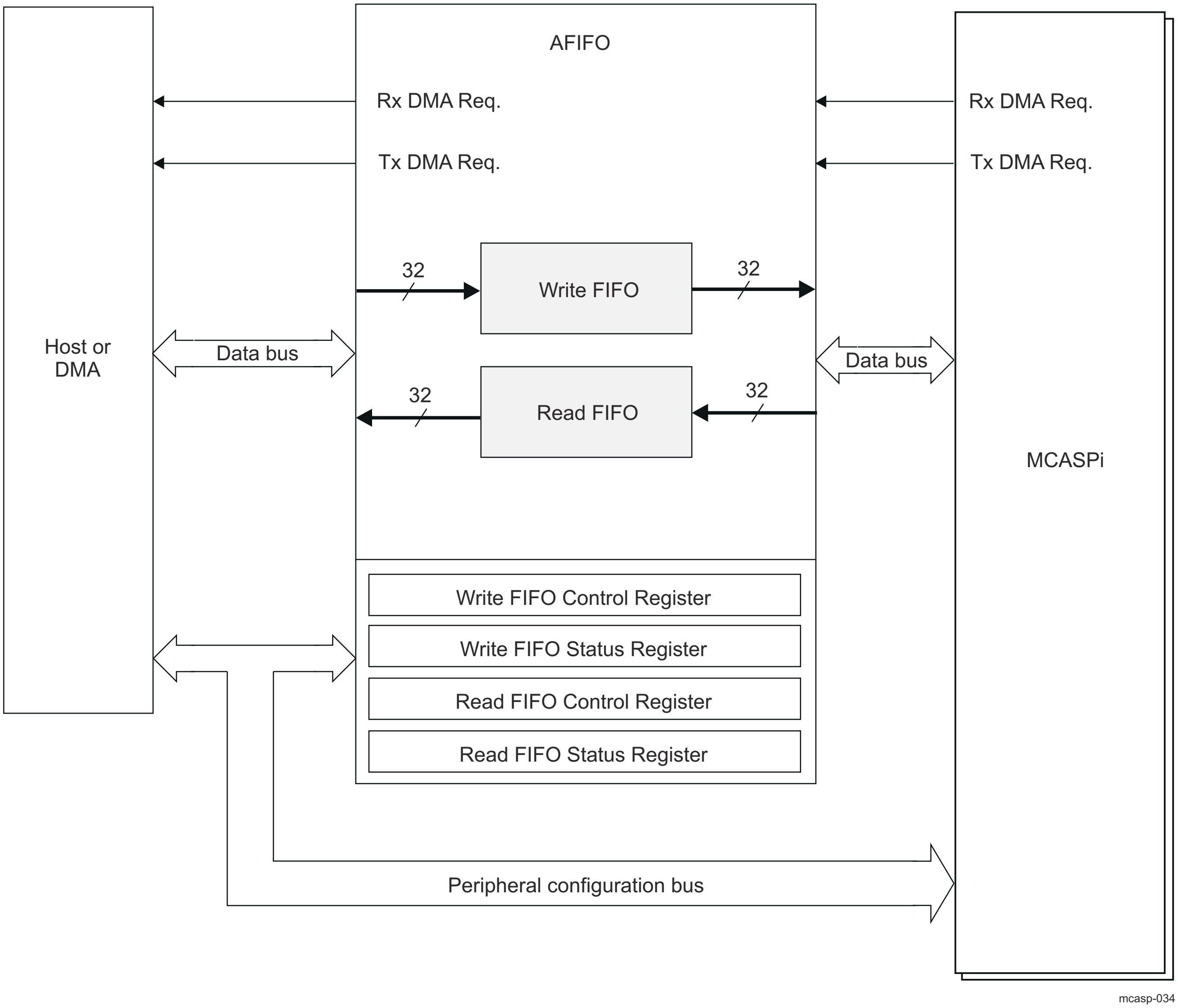

Figure 12-23. MCASP Audio FIFO (AFIFO) Block Diagram

12.1.1.4.11.1 AFIFO Data Transmission

When the Write FIFO is disabled, transmit DMA requests pass through directly from the MCASP to the host/DMA controller. Whether the WFIFO is enabled or disabled, the MCASP generates transmit DMA requests as needed; the AFIFO is “invisible” to the MCASP. When the Write FIFO is enabled, transmit DMA requests from the MCASP are sent to the AFIFO, which in turn generates transmit DMA requests to the host/DMA controller. If the Write FIFO is enabled, upon a transmit DMA request from the MCASP, the WFIFO writes WNUMDMA 32-bit words to the MCASP if and when there are at least WNUMDMA words in the Write FIFO. If there are not, the WFIFO waits until this condition has been satisfied. At that point, it writes WNUMDMA words to the MCASP (see description for the MCASP_WFIFOCTL[7-0] WNUMDMA). If the host CPU writes to the Write FIFO, independent of a transmit DMA request, the WFIFO will accept host writes until full. After this point, excess data will be discarded. Note that when the WFIFO is first enabled, it will immediately issue a transmit DMA request to the host. This is because it begins in an empty state, and is therefore ready to accept data.

12.1.1.4.11.1.1 Transmit DMA Event Pacer

The AFIFO may be configured to delay making a transmit DMA request to the host until the Write FIFO has enough space for a specified number of words. In this situation, the number of transmit DMA requests to the host or DMA controller is reduced. If the Write FIFO has space to accept WNUMEVT 32-bit words, it generates a transmit DMA request to the host and then waits for a response. Once WNUMEVT words have been written to the FIFO, it checks again to see if there is space for WNUMEVT 32-bit words. If there is space, it generates another transmit DMA request to the host, and so on. In this fashion, the Write FIFO will attempt to stay filled. Note that if transmit DMA event pacing is desired, MCASP_WFIFOCTL[15-8] WNUMEVT bit field should be set to a non-zero integer multiple of the value in MCASP_WFIFOCTL[7-0] WNUMDMA bit field. If transmit DMA event pacing is not desired, then the value in MCASP_WFIFOCTL[15-8] WNUMEVT bit field should be set equal to the value in MCASP_WFIFOCTL[7-0] WNUMDMA bit field.

12.1.1.4.11.2 AFIFO Data Reception

When the Read FIFO is disabled, receive DMA requests pass through directly from MCASP to the host/DMA controller. Whether the RFIFO is enabled or disabled, the MCASP generates receive DMA requests as needed; the AFIFO is “invisible” to the MCASP. When the Read FIFO is enabled, receive DMA requests from the MCASP are sent to the AFIFO, which in turn generates receive DMA requests to the host/DMA controller. If the Read FIFO is enabled and the MCASP makes a receive DMA request, the RFIFO reads RNUMDMA 32-bit words from the MCASP, if and when the RFIFO has space for RNUMDMA words. If it does not, the RFIFO waits until this condition has been satisfied; at that point, it reads RNUMDMA words from the MCASP (see description for theMCASP_RFIFOCTL[7-0] RNUMDMA). If the host CPU reads the Read FIFO, independent of a receive DMA request, and the RFIFO at that time contains less than RNUMEVT words, those words will be read correctly, emptying the FIFO.

12.1.1.4.11.2.1 Receive DMA Event Pacer

The AFIFO may be configured to delay making a receive DMA request to the host until the Read FIFO contains a specified number of words. In this situation, the number of receive DMA requests to the host or DMA controller is reduced. If the Read FIFO contains at least RNUMEVT 32-bit words, it generates a receive DMA request to the host and then waits for a response. Once RNUMEVT 32-bit words have been read from the RFIFO, the RFIFO checks again to see if it contains at least another RNUMEVT words. If it does, it generates another receive DMA request to the host, and so on. In this fashion, the Read FIFO will attempt to stay empty. Note that if receive DMA event pacing is desired, MCASP_RFIFOCTL[15-8] RNUMEVT bit field should be set to a non-zero integer multiple of the value in MCASP_RFIFOCTL[7-0] RNUMDMA bit field. If receive DMA event pacing is not desired, then the value in MCASP_RFIFOCTL[15-8] RNUMEVT bit field should be set equal to the value in MCASP_RFIFOCTL[7-0] RNUMDMA bit field.

12.1.1.4.11.3 Arbitration Between Transmit and Receive DMA Requests

If both the WFIFO and the RFIFO are enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the transmit DMA request. Once a transfer is in progress, it is allowed to complete. If only the WFIFO is enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the transmit DMA request. Once a transfer is in progress, it is allowed to complete. If only the RFIFO is enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the receive DMA request. Once a transfer is in progress, it is allowed to complete.

12.1.1.4.12 MCASP Events and Interrupt Requests

Table 12-9 lists all the transmit event flags. Table 12-10 lists all the Receive event flags. Source of each of these TX/RX events can be a TX/RX channel from any MCASP serializer configured as transmitter or receiver respectively.

Table 12-9. TX Events

Event Mask(1)	Event Flag	Map to (1)	Description
MCASP_XINTCTL[0] XUNDRN	MCASP_XSTAT[0] XUNDRN	MCASP[0-2]_XMIT_INTR_PEND	Transmit buffer underrun
MCASP_XINTCTL[1] XSYNCERR	MCASP_XSTAT[1] XSYNCERR	MCASP[0-2]_XMIT_INTR_PEND	Unexpected transmit frame sync
MCASP_XINTCTL[2] XCKFAIL	MCASP_XSTAT[2] XCKFAIL	MCASP[0-2]_XMIT_INTR_PEND	Transmit clock failure

Table 12-9. TX Events (continued)

Event Mask[1]	Event Flag	Map to [1]	Description
MCASP_XINTCTL[3] XDMAERR	MCASP_XSTAT[7] XDMAERR	MCASP[0-2]_XMIT_INTR_PEND	DATA port transmit error
MCASP_XINTCTL[4] XLAST	MCASP_XSTAT[4] XLAST	MCASP[0-2]_XMIT_INTR_PEND	Transmit last slot interrupt
MCASP_XINTCTL[5] XDATA	MCASP_XSTAT[5] XDATA	MCASP[0-2]_XMIT_INTR_PEND	Transmit data-ready interrupt
MCASP_XINTCTL[7] XSTAFRM	MCASP_XSTAT[6] XSTAFRM	MCASP[0-2]_XMIT_INTR_PEND	Transmit start of frame interrupt
n.a.	MCASP_XSTAT[8] XERR	n.a.	OR-event of all Tx-error events: (XDMAERR | XCKFAIL | XUNDRN | XSYNCERR). It is cleared ONLY when all error flags are cleared
n.a.	MCASP_XSTAT[3] XTDMSLOT	n.a.	Qualifies the current TDM slot as an odd or an even slot.

(1) Every MCASP module generates separate interrupt event.

Table 12-10. RX Events

Event Mask[1]	Event Flag	Map to[1]	Description
MCASP_RINTCTL[0] ROVRN	MCASP_RSTAT[0] ROVRN	MCASP[0-2]_REC_INTR_PEND	Receive buffer overrun
MCASP_RINTCTL[1] RSYNCERR	MCASP_RSTAT[1] RSYNCERR	MCASP[0-2]_REC_INTR_PEND	Unexpected receive frame sync
MCASP_RINTCTL[2] RCKFAIL	MCASP_RSTAT[2] RCKFAIL	MCASP[0-2]_REC_INTR_PEND	Receive clock failure
MCASP_RINTCTL[3] RDMAERR	MCASP_RSTAT[7] RDMAERR	MCASP[0-2]_REC_INTR_PEND	DATA port receive error
MCASP_RINTCTL[4] RLAST	MCASP_RSTAT[4] RLAST	MCASP[0-2]_REC_INTR_PEND	Receive last slot
MCASP_RINTCTL[5] RDATA	MCASP_RSTAT[5] RDATA	MCASP[0-2]_REC_INTR_PEND	Receive data-ready
MCASP_RINTCTL[7] RSTAFRM	MCASP_RSTAT[6] RSTAFRM	MCASP[0-2]_REC_INTR_PEND	Receive start of frame
n.a.	MCASP_RSTAT[8] RERR	n.a.	OR-event of all Rx-error events: (RDMAERR | RCKFAIL | ROVRN | RSYNCERR). RERR event is cleared once all error flags are cleared.
n.a.	MCASP_RSTAT[3] RTDMSLOT	n.a.	Qualifies the current TDM slot as an odd or an even slot.

(1) Every MCASP module generates separate interrupt event.

Software has to read the MCASP_XSTAT/MCASP_RSTAT register to determine which event occurs at a global level for MCASP Tx/Rx logic. In addition user software has to scan the XRDY/RRDY read-only flags in the MCASP_SRCTLn registers to determine which active serializer is the actual source of the event.

A Tx interrupt line (MCASP[0-2]_XMIT_INTR_PEND) is asserted (active high) when one of the MCASP_XSTAT notified events occurs, provided that it is enabled in its corresponding MCASP_XINTCTL bit. Similarly, a Rx interrupt line (MCASP[0-2]_REC_INTR_PEND) is asserted (active high) when one of MCASP_RSTAT notified events occurs, provided that it is enabled in its corresponding MCASP_RINTCTL bit. See also Section 12.1.1.4.12.4 , *Multiple Interrupts* and the Section 12.1.1.4.10.1 , *Data Ready Status and Event/Interrupt Generation* (n = 0 to 15).

12.1.1.4.12.1 Transmit Data Ready Event and Interrupt

The transmit data-ready interrupt (XDATA) is generated if the MCASP_XSTAT[5] XDATA bit is 1 and MCASP_XINTCTL[5] XDATA bit is enabled. The Section 12.1.1.4.10.1 , *Data Ready Status and Event/Interrupt Generation*, provides details on when XDATA is set in the MCASP_XSTAT register.

A transmit-start-of-frame interrupt (XSTAFRM) is triggered by the recognition of a transmit frame sync.

A transmit-last-slot interrupt (XLAST) is a qualified version of the data-ready interrupt (XDATA). It has the same behavior than the data-ready interrupt, but is further qualified by having the data requested belonging to the last slot (the slot that just ended is the next-to-last TDM slot, the current slot is the last slot).

12.1.1.4.12.2 Receive Data Ready Event and Interrupt

The receive data-ready interrupt (RDATA) is generated if the MCASP_RSTAT[5] RDATA bit is 1 and MCASP_RINTCTL[5] RDATA bit is enabled. The Section 12.1.1.4.10.1 , *Data Ready Status and Event/Interrupt Generation*, provides details on when the MCASP_RSTAT[5] RDATA bit is set.

A receiver start of frame (RSTAFRM) interrupt is triggered by the recognition of a receiver frame sync.

A receiver last slot (RLAST) interrupt is a qualified version of the data ready interrupt (RDATA). It has the same behavior as the data ready interrupt, but is further qualified by having the data in the buffer come from the last TDM time slot (the slot that just ended was last TDM slot).

12.1.1.4.12.3 Error Interrupt

Upon detection, the following error conditions generate interrupt flags:

In the transmit status register (MCASP_XSTAT):

- Transmit underrun (XUNDRN)
- Unexpected transmit frame sync (XSYNCERR)
- Transmit clock failure (XCKFAIL)
- Transmit DATA port error (XDMAERR)

Each interrupt source also has a corresponding enable bit in the transmit interrupt control register (MCASP_XINTCTL). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_XSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

In the receive status register (MCASP_RSTAT) :

- Receiver overrun (ROVRN)
- Unexpected receive frame sync (RSYNCERR)
- Receive clock failure (RCKFAIL)
- Receive DATA port error (RDMAERR)

Each interrupt source also has a corresponding enable bit in the receive interrupt control register (MCASP_RINTCTL). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_RSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

12.1.1.4.12.4 Multiple Interrupts

This only applies to interrupts and not to DMA requests. The following terms are defined:

- **Active Interrupt Request:** a flag in MCASP_XSTAT is set and the interrupt is enabled in MCASP_XINTCTL.
- **Outstanding Interrupt Request:** An interrupt request has been issued on one of the MCASP transmit interrupt port, but that request has not yet been serviced.
- **Serviced:** The CPUs write to MCASP_XSTAT to clear one or more of the active interrupt request flags.

The first interrupt request to become active for the serializer with the interrupt flag set in MCASP_XSTAT/ MCASP_RSTAT and the interrupt enabled in MCASP_XINTCTL/MCASP_RINTCTL generates a request on the MCASP transmit or receive interrupt port.

If more than one interrupt request becomes active in the same cycle, a single interrupt request is generated on the MCASP transmit or receive interrupt port. Subsequent interrupt requests that become active while the first interrupt request is outstanding do not immediately generate a new request pulse on the MCASP transmit or receive interrupt port.

The interrupt is serviced with the CPU writing to MCASP_XSTAT/MCASP_RSTAT. If any interrupt requests are active after the write, a new request is generated on the MCASP transmit or receive interrupt port.

One outstanding interrupt request is allowed on each port, so a transmit and a receive interrupt request may both be outstanding at the same time.

12.1.1.4.13 MCASP DMA Requests

The MCASP can generate one DMA request to the DMA controller to transmit (MCASP[0-2]_XMIT_DMA_EVT) or receive (MCASP[0-2]_REC_DMA_EVT) data. A DMA request to transmit data is generated if the *MCASP_XEVTCTL*[0] XDATDMA bit is cleared. A DMA request to receive data is generated if the MCASP_PIDTCTL[0] RDATDMA bit is cleared.

12.1.1.4.14 MCASP Loopback Modes

The MCASP features a digital loopback mode (DLB) that allows loopback test transfers in TDM mode between MCASP transmitters and receivers within the same device. In loopback mode, the output of a transmit serializer is connected internally to the input of a receive serializer. Therefore, a receiver data can be checked against a transmitter data to ensure that the MCASP settings are correct. Digital loopback mode applies to TDM mode only (2 to 32 slots in a frame). It does not apply to DIT mode (XMOD = 0x180) or burst mode (XMOD = 0).

Figure 12-24 shows the basic logical connection of the serializers in loopback mode.

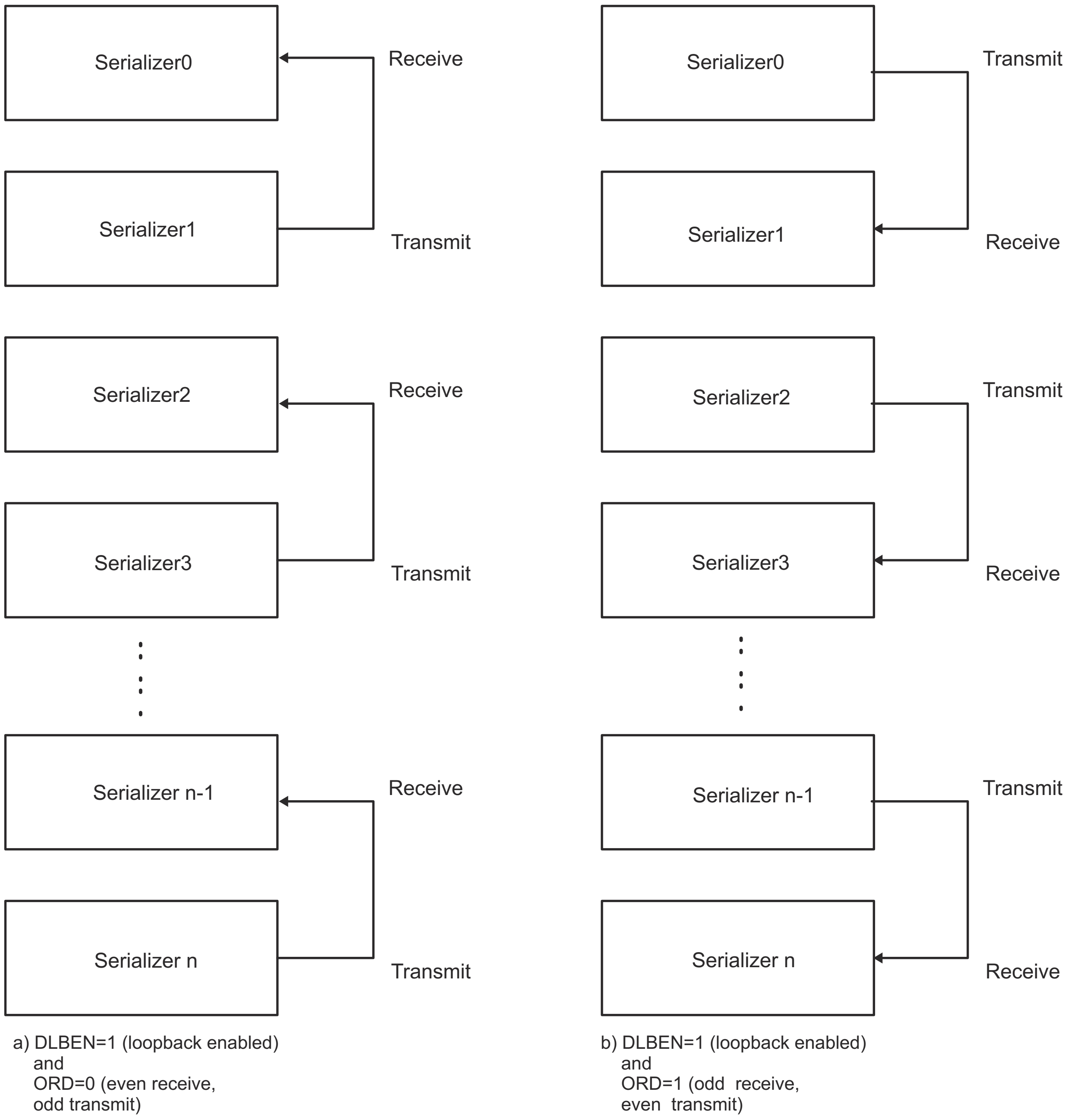

mcasp-023

Figure 12-24. MCASP Serializers Operation in Loopback Mode

Two types of loopback connections are possible, selected by the ORD bit in the digital loopback control register - MCASP_DLBCTL as follows:

- ORD = 0: Outputs of odd serializers are connected to inputs of even serializers. If this mode is selected, the odd serializers must be configured as transmitters and even serializers as receivers.
- ORD = 1: Outputs of even serializers are connected to inputs of odd serializers. If this mode is selected, the even serializers must be configured as transmitters and odd serializers as receivers.

User can choose in software (the MCASP_DLBCTL[4] IOLBEN bit) between a MCASP module internal loopback and a device I/O level loopback.

When a **MCASP internal loopback** is selected (MCASP_DLBCTL[4] IOLBEN = 0b0), it is NOT necessary to configure *MCASP_PFUNC* and *MCASP_PDIR* registers for MCASP pin settings. Nevertheless, data can be optionally made externally visible at the I/O pin of the transmit serializer, if the pin is configured as a MCASP output pin by setting the corresponding *MCASP_PFUNC* bit to 0 (this is, to function as MCASP, not GPIO) and *MCASP_PDIR* bit to 1 (output).

When a **device I/O level loopback** is selected (MCASP_DLBCTL[4] IOLBEN = 0b1), the *MCASP_PFUNC* and *MCASP_PDIR* registers must be configured with the appropriate settings for all AXRn pins, according to ORD bit configuration.

In case of device I/O loopback, the connectivity is externally applied between device pads (this is, reaching device I/O buffers).

When in loopback mode, the transmit clock and frame sync are used by both the transmit and receive sections of the MCASP. The transmit and receive sections operate synchronously. This is achieved by setting the MCASP_DLBCTL[3-2] MODE bit field to 0x1 and the *MCASP_ACLKXCTL*[6] ASYNC bit to 0b0.

12.1.1.4.14.1 Loopback Mode Configurations

This is a summary of the settings required for digital loopback mode for TDM format :

- The MCASP_DLBCTL[0] DLBEN bit must be set to 0b1 to enable a loopback mode. It must be kept at 0b0 during normal MCASP operation.
- The MCASP_DLBCTL[4] IOLBEN bit must be set to select between internal (MCASP local) loopback mode or device I/O level loopback mode.
- The MCASP_DLBCTL[3-2] MODE bit field must be set to 0x1 for both the transmit and receive sections to use the transmit clock and frame sync generator.
- The MCASP_DLBCTL[1] ORD bit must be programmed appropriately to select odd or even serializers to be transmitters or receivers.
- The corresponding serializers must be configured accordingly.
- The *MCASP_ACLKXCTL*[6] ASYNC bit must be cleared to 0b0 to ensure synchronous transmit and receive operations.
- The MCASP_AFSRCTL[15-7] RMOD bit field and MCASP_AFSXCTL[15-7] XMOD bit field must be set within range (0x2 - 0x20) to indicate TDM mode.

Note

Loopback mode does not apply to DIT or burst mode, because MCASP receivers do NOT natively support DIR - reception.

12.1.1.4.15 MCASP Error Reporting

The MCASP includes error-checking capability for the serial protocol and data underrun. In addition, the MCASP includes a timer that continually measures the high-frequency controller clock every 32 AHCLKX clock cycles. The value of the timer can be read to get a measurement of the clock frequency and has a minimum and maximum range setting that can set an error flag if the controller clock goes out of a specified range.

When one or more errors (software selectable) are detected, an interrupt can be generated if desired, based on one or more error sources.

12.1.1.4.15.1 Buffer Underrun Error -Transmitter

A buffer underrun occurs when a serializer is instructed by the transmit state-machine to transfer data from XRBUFn buffer to XRSRn shift register, but the corresponding (MCASP_XBUFn) register has not yet been written with new data since the last time the transfer occurred. When this occurs, the transmit state-machine sets the XUNDRN flag.

An underrun is checked only once per time slot. The MCASP_XSTAT[0] XUNDRN flag is set when an underrun condition occurs. Once set, the XUNDRN flag remains set until the host explicitly writes 1 to the XUNDRN bit to clear it (n = 0 to 15).

In DIT mode, a pair of BMC zeros is shifted out when an underrun occurs (four bit times at 128 bfs). By shifting out a pair of zeros, a clock can be recovered on the receiver. To recover, reset the MCASP and restart with the proper initialization.

In TDM mode, during an underrun case, a long stream of zeros are shifted out causing the DACs to mute. To recover, reset the MCASP and start again with the proper initialization.

12.1.1.4.15.2 Buffer Overrun Error-Receiver

A buffer overrun occurs when a serializer is instructed to transfer data from XRSRn shift register to XRBUFn receiver buffer, but the corresponding MCASP_RBUFn register has not yet been read since the last time the transfer occured. When this occurs, the receiver state machine sets the overrun flag - ROVRN. However, the individual serializer writes over the data in the XRBUFn buffer register (destroying the previous sample) and continues shifting (n = 0 to 15).

An overrun is checked only once per time slot. The MCASP_RSTAT[0] ROVRN flag is set when an overrun condition occurs. It is possible that an overrun occurs on one time slot but then the host catches up and does not cause an overrun on the following time slots. However, once the ROVRN flag is set, it remains set until the host explicitly writes a 1 to the ROVRN bit to clear the ROVRN bit.

12.1.1.4.15.3 DATA Port Error - Transmitter

A transmit DATA port error, as indicated by the MCASP_XSTAT[7] XDMAERR bit, occurs when the DMA or device CPU writes more words to the DATA port of the MCASP than it should.

The MCASP_XSTAT[7] XDMAERR = 0b1 indicates that the DMA or device CPU wrote too many words to the MCASP DATA port for a given transmit DMA event. Writing too few words results in a transmit underrun error setting the MCASP_XSTAT[0] XUNDRN bit.

While XDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the DMA or device CPU. The MCASP transmitter and the DMA must be reinitialized to resynchronize them.

12.1.1.4.15.4 DATA Port Error - Receiver

A receive DATA port error, as indicated by the MCASP_RSTAT[7] RDMAERR bit, occurs when the DMA or device CPU reads more words from the DATA port of the MCASP than it should.

The MCASP_RSTAT[7] RDMAERR bit indicates that the DMA or device CPU read too many words from the MCASP DATA port for a given receive RINT event. Reading too few words results in a receiver overrun error setting the MCASP_RSTAT[0] ROVRN bit.

While RDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the DMA or device CPU. The MCASP receiver and the DMA must be reinitialized to resynchronize them.

12.1.1.4.15.5 Unexpected Frame Sync Error

An unexpected frame sync occurs in when:

- in burst mode and TDM mode, the next active edge of the frame sync occurs early such that the current slot will not be completed by the time the next slot is scheduled to begin.
- in TDM mode, an unexpected frame sync occurs also if the frame sync does NOT occur exactly during the correct bit clock (not a cycle earlier or later) and before slot 0.

When an unexpected frame sync occurs, there are two possible actions depending upon when the unexpected frame sync occurs:

1. **Early:** An early unexpected frame sync occurs when the MCASP is in the process of completing the current frame and a new frame sync is detected (not including overlap that occurs due to a 1 or 2 bit frame sync delay). When an early unexpected frame sync occurs:
   - Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
   - Current frame is not resynchronized. The number of bits in the current frame is completed. The next frame sync, which occurs after the current frame is completed, will be resynchronized.
2. **Late:** A late unexpected frame sync occurs when there is a gap or delay between the last bit of the previous frame and the first bit of the next frame. When a late unexpected frame sync occurs (as soon as the gap is detected):
   - Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
   - Resynchronization occurs upon the arrival of the next frame sync.

Late frame sync is detected the same way in burst mode and TDM mode. However, in burst mode, late frame sync is not meaningful and its interrupt enable should not be set.

12.1.1.4.15.6 Clock Failure Detection

12.1.1.4.15.6.1 Clock Failure Check Startup

It is initially expected of the clock failure circuits to generate an error until at least one measurement is taken. Therefore, the clock failure interrupts, clock switch, and mute functions should not be enabled immediately, but only after a specific startup procedure.

To start the transmit clock failure check procedure:

1. Configure the transmit clock failure detect logic (XMIN, XMAX, XPS) in the transmit clock check control register (MCASP_XCLKCHK).
2. Clear the transmit clock failure flag (XCKFAIL) in the transmit status register (MCASP_XSTAT).
3. Wait until the first measurement is taken (> 32 AHCLKX clock periods).
4. Verify that no clock failure is detected.
5. Repeat Step 2 through Step 4 until the clock is running and is no longer issuing clock failure errors.
6. After the transmit clock is measured and falls within the acceptable range, the following can be enabled:
   a. The transmit clock failure interrupt enable bit (XCKFAIL) in the transmitter interrupt control register (MCASP_XINTCTL)

To start the receive clock failure check procedure:

1. Configure receive clock failure detect logic (RMIN, RMAX, RPS) in the receive clock check control register (MCASP_RCLKCHK).
2. Clear receive clock failure flag (RCKFAIL) in the receive status register (MCASP_RSTAT).
3. Wait until first measurement is taken (> 32 AHCLKR clock periods).
4. Verify no clock failure is detected.
5. Repeat steps 2–4 until clock is running and is no longer issuing clock failure errors.
6. After the receive clock is measured and falls within the acceptable range, the following may be enabled:
   a. the receive clock failure (RCKFAIL) interrupt enable bit in the receive interrupt control register (MCASP_RINTCTL)

12.1.1.4.15.6.2 Transmit Clock Failure Check and Recovery

The transmit clock failure check circuit (see Figure 12-25) works off the internal MCASP interface clock and the external high-frequency serial clock (AHCLKX). It continually counts the number of interface clocks for every 32 high-rate serial clock (AHCLKX) periods, and stores the count in XCNT of the transmit clock check control register (MCASP_XCLKCHK) every 32 high-rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (XMIN), and automatically flags an interrupt (the MCASP_XSTAT[2] XCKFAIL bit) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is less than XMIN. The logic continually compares the current count (from the running interface clock counter) to the maximum allowable boundary (XMAX). This is so that if the external clock completely stops, the counter value is not copied to XCNT. An out-of-range maximum condition occurs when the count is greater than XMAX. The XMIN and XMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

For the transmit clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

If a clock failure is detected, the MCASP_XSTAT[2] XCKFAIL transmit clock failure flag is set. This causes an interrupt if the MCASP_XINTCTL[2] XCKFAIL transmit clock failure interrupt enable bit is set.

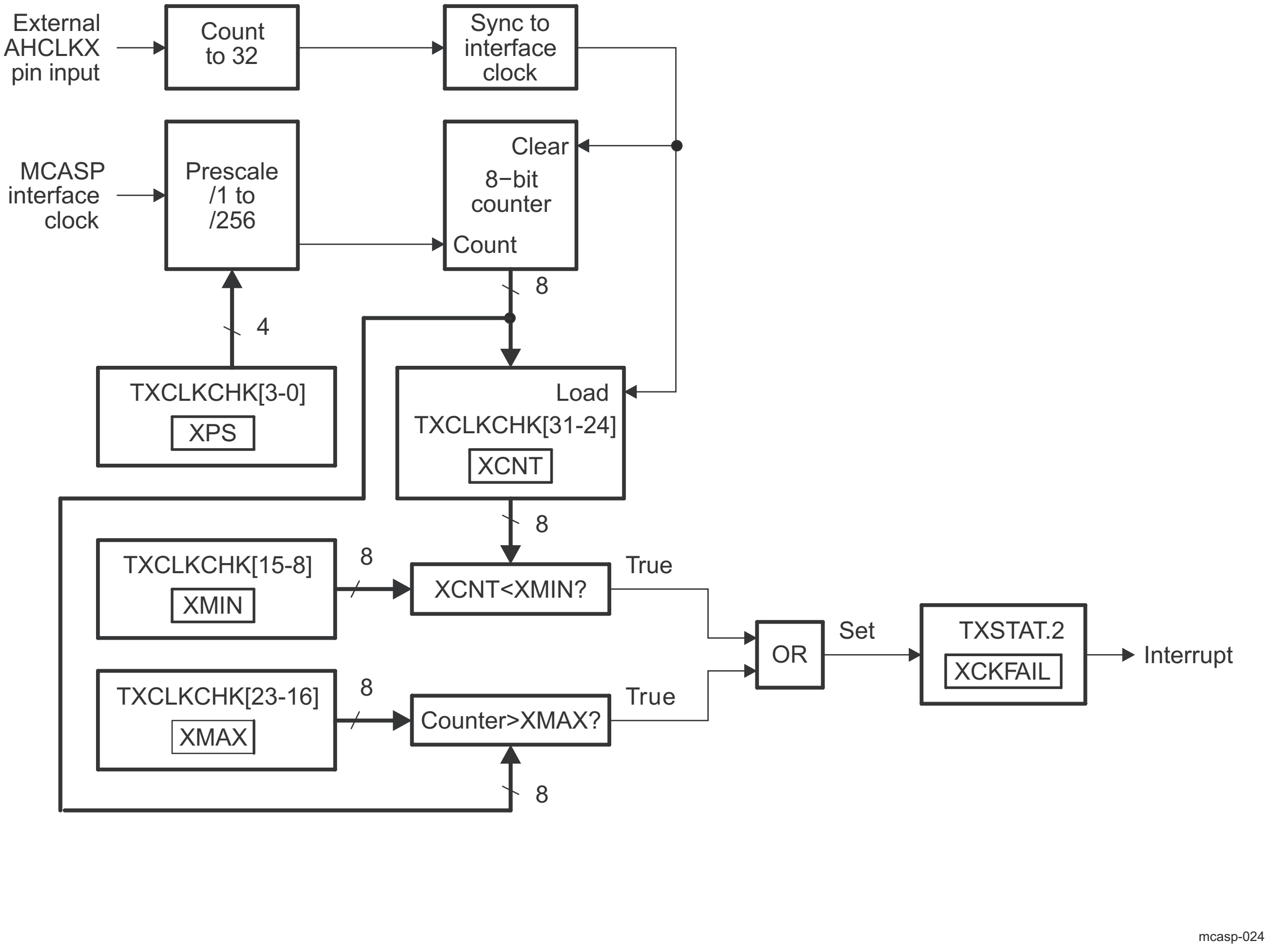

Figure 12-25. Transmit Clock Failure Detection Circuit Block Diagram

12.1.1.4.15.6.3 Receive Clock Failure Check and Recovery

The receive clock failure check circuit (see Figure 12-26) works off both the internal MCASP interface clock and the external high-frequency serial clock (AHCLKR). It continually counts the number of interface clocks for every 32 high rate serial clock (AHCLKR) periods, and stores the count in RCNT of the receive clock check control register (MCASP_RCLKCHK) every 32 high rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (RMIN) and automatically flags an event (the MCASP_RSTAT[2] RCKFAIL bit) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is smaller than RMIN. The logic continually compares the current count (from the running interface clock counter) against the maximum allowable boundary (RMAX). This is in case the external clock completely stops, so that the counter value is not copied to RCNT. An out-of-range maximum condition occurs when the count is greater than RMAX. Note that the RMIN and RMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate either that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

In order for the receive clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

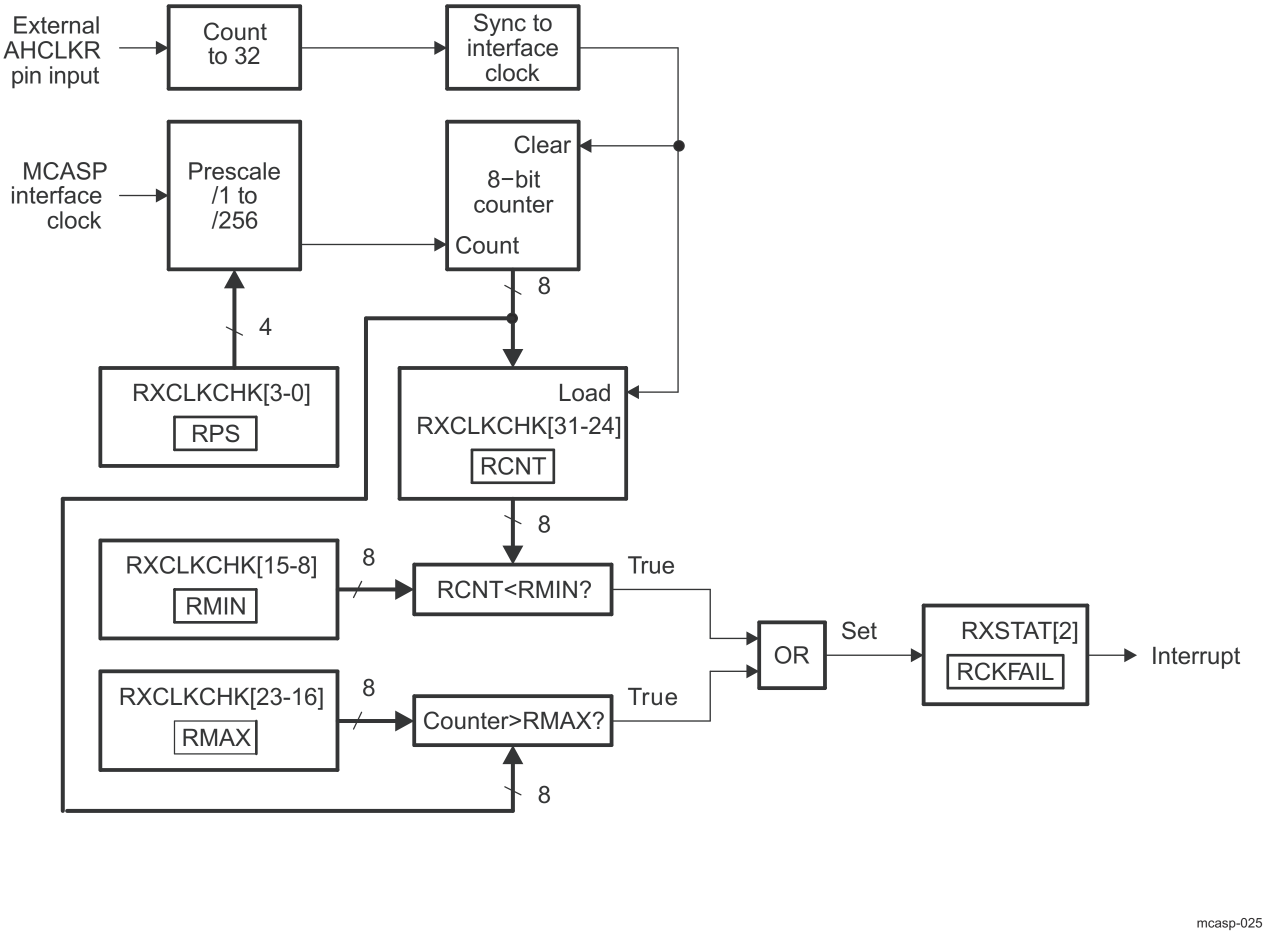

Figure 12-26. Receive Clock Failure Detection Circuit Block Diagram

12.1.1.5 MCASP Programming Guide

This section describes the low-level hardware programming sequences for the configuration and use of the MCASP module.

12.1.1.5.1 MCASP Global Initialization

12.1.1.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCASP module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCASP (for more information, see *Module Integration*, and *MCASP Environment*).

Table 12-11 describes the global initialization of surrounding modules.

Table 12-11. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC3	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	PLLCTRL0 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
PLL4	PLL4 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
PLL2	PLL2 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
ATL	ATL configuration must be done to enable the clocks to the MCASP modules, see *Audio Tracking Logic (ATL)*.
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts, see *Interrupts*.
MAIN2MCU_LVL_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MAIN2MCU_LVL_INTRTR0 interrupts, see *Interrupts*.
R5FSS0_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0_CORE0/1 interrupts, see *Interrupts*.
PDMA0_MCASP_G0	PDMA0_MCASP_G0 controllers configuration must be done to enable the module PDMA0_MCASP_G0 channel request, see *PDMA Controller*.
Interconnects	For information about the CBASS0 interconnects configuration, see *System Interconnect*.

Note

NAVSS configuration (UMDA channel set-up) must be done in order to move data from/to MCASP via the PDMA Controller. For more information, see *Navigator Subsystem (NAVSS)*.

Note

The COMPUTE_CLUSTER0, MAIN2MCU_LVL_INTRTR0, R5FSS0_CORE0/1, and the PDMA0_MCASP_G0 configurations are required when the interrupt and DMA-based communication modes are used. Further initialization of the selected interrupt and DMA controllers of the host CPU must be done for full functionality of the MCASP DMA and interrupt lines.

12.1.1.5.1.2 MCASP Global Initialization

12.1.1.5.1.2.1 Main Sequence – MCASP Global Initialization for DIT-Transmission

The procedure in Table 12-12 initializes the MCASP serializers transmitters to operate in DIT-mode (S/PDIF-transmission protocol) after a power-on reset (POR).

CAUTION

Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Table 12-12. MCASP Transmitters Global Initialization for DIT-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP components.	*MCASP_GBLCTL*[12-8]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[12-8]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1
4. Configure the transmit format unit.	See Section 12.1.1.5.1.2.1.1 .	
5. Configure the transmit frame sync generator.	See Section 12.1.1.5.1.2.1.2 .	
6. Configure the transmit clock generator.	See Section 12.1.1.5.1.2.1.3 .	
7. Configure the TDM sequencer—set all slots active.	MCASP_XTDM[31-0] XTDMS	0xFFFF FFFF
8. Configure the desired n-th serializer (n=0 to 3) for transmit mode operation.(3)	MCASP_SRCTLn [1-0] SRMOD; n = 0 to 15	0x1
9. Configure the MCASP pins functionality.	See Section 12.1.1.5.1.2.1.4 .	
10. Enable the MCASP DIT - transmission mode.	MCASP_DITCTL[0] DITEN	0x1(2)
11. Configure DIT-specific subframe fields.	See Table 12-17.	
12. Release from reset state the divider that outputs the AHCLKX clock.(1)	*MCASP_GBLCTL*[9] XHCLKRST	0x1
13. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[9] XHCLKRST	=0x1
14. Release from reset state the divider that outputs the ACLKX clock.(1)	*MCASP_GBLCTL*[8] XCLKRST	0x1
15. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[8] XCLKRST	=0x1

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKXCTL* and *MCASP_ACLKXCTL* registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.

(2) This globally configures all active transmitters to operate in DIT-mode.

(3) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).

12.1.1.5.1.2.1.1 Subsequence – Transmit Format Unit Configuration for DIT-Transmission

The procedure in Table 12-13 configures the transmit frame format unit of the MCASP module for a DIT-transmission.

Note

- The first transmit data bit always has a 0-bit delay.
- The bitstream is always transmitted in least-significant-bit (LSB)-first order.
- Pad value for extra bits in a certain slot is always 0.

Table 12-13. Transmit Format Unit Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the slot size to 32 bits.	MCASP_XFMT[7-4] XSSZ	0xF
IF: the data to transmit is left- aligned	Software test condition	
Set data mask in the range 0xFFFF FF00 – 0xFFFF 0000.	MCASP_XMASK[31-0] XMASK	0x-(1)
Rotate data right by a multiple-of-4- bit positions.	MCASP_XFMT[2-0] XROT	0x-(1)
ELSE		
Set data mask in the range 0x00FF FFFF– 0x0000 FFFF.	MCASP_XMASK[31-0] XMASK	0x-(1)
Rotate data right by 0-bit positions.	MCASP_XFMT[2-0] XROT	0x0

Table 12-13. Transmit Format Unit Configuration for DIT-Transmission (continued)

Step	Register/Bit Field/Programming Model	Value
ENDIF		
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_XFMT[3] XBUSEL	0x-

(1) Refer to Section 12.1.1.4.4.1 , *Transmit Fromat Unit* and Section 12.1.1.4.4.1.2 , *DIT-Mode Transmission Data Alignment Settings*.

12.1.1.5.1.2.1.2 Subsequence – Transmit Frame Synchronization Generator Configuration for DIT-Transmission

The procedure in Table 12-14 configures the transmit frame synchronization generator of the MCASP module.

Note

The frame synchronization signal is always rising-edge active and always has a single-bit width.

Table 12-14. Transmit Frame-Synchronization Generator Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Select 384-slot size block.	MCASP_AFSXCTL[15-7] XMOD	0x180
Select internally-generated transmit frame sync.	MCASP_AFSXCTL[1] FSXM	0x1

12.1.1.5.1.2.1.3 Subsequence – Transmit Clock Generator Configuration for DIT-Transmission

Note

By default, the ACLKX and AHCLKX clocks are generated only from the MCASP internal clock source.

The procedure in Table 12-15 configures the transmit clock generator of the MCASP module.

Table 12-15. Transmit Clock Generator Configuration in DIT-Mode

Step	Register/Bit Field/Programming Model	Value
Set the divisor for the internally generated high frequency clock– AHCLKX.	*MCASP_AHCLKXCTL*[11-0] HCLKXDIV	0x-
Set he divisor for the internally generated transmission clock– ACLKX.	*MCASP_ACLKXCTL*[4-0] CLKXDIV	0x-
Configure the transmit clock failure detect logic.	See Section 12.1.1.4.15.6.1 , *Clock Failure Check Startup*.	

12.1.1.5.1.2.1.4 Subsequence - MCASP Pins Functional Configuration

The procedure in Table 12-16 configures the MCASP pins for MCASP functionality.

Table 12-16. MCASP Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins as outputs: AFSX AHCLKX ACLKX Desired i-th MCASP data pin AXRi is configured as an output for DIT-transmission.	*MCASP_PDIR*[28] AFSX; *MCASP_PDIR*[27] AHCLKX; *MCASP_PDIR*[26] ACLKX; *MCASP_PDIR*[i] AXRi	0x1 0x1 0x1 0x1

12.1.1.5.1.2.1.5 Subsequence – DIT-specific Subframe Fields Configuration

The procedure in Table 12-17 configures the DIT-specific subframe fields as part of the S/PDIF format data.

Table 12-17. DIT-Specific Subframe Fields Configuration

Step	Register/Bit Field/Programming Model	Value
Configure the valid bit value for odd time slots.	MCASP_DITCTL[3] VB	0x-
Configure the valid bit value for even time slots.	MCASP_DITCTL[2] VA	0x-
Configure the user data bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITUDRAi[31-0] DITUDRAi, where i = 0 to 5 MCASP_DITUDRBi[31-0] DITUDRBi, where i = 0 to 5	0x- 0x-
Configure the channel status bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITCSRAi[31-0], where i = 0 to 5 MCASP_DITCSRBi[31-0], where i = 0 to 5	0x- 0x-

12.1.1.5.1.2.2 Main Sequence – MCASP Global Initialization for TDM-Reception

The procedure in Table 12-18 initializes a MCASP serializer n receiver(s) to operate in TDM-mode (the only mode supported by MCASP receivers) after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols reception.

CAUTION

Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Note

The MCASP receivers support only TDM-frames (including 384-TDM frames) reception. DIT-frames reception (this is, S/PDIF stream) can be implemented indirectly via an external DIR-chip converter with DIT-input and TDM (I2S)-compatible output connected to device MCASP receiver input (TDM-only compatible).

Table 12-18. MCASP Receivers Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP receive components.	*MCASP_GBLCTL*[4-0]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[4-0]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1
4. Configure the receive format unit.	See Section 12.1.1.5.1.2.2.1 .	
5. Configure the receive frame sync generator.	See Section 12.1.1.5.1.2.2.2 .	
6. Configure the receive clock generator.	See Section 12.1.1.5.1.2.2.3 .	
7. Program all bits - RTDMSk (where k = 0 to 31) according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_RTDM[k] RTDMSk , where k = 0 to 31	0x-
8. Configure the desired n-th serializer for receive mode operation.(4)	MCASP_SRCTLn [1-0] SRMOD; n = 0 to 15	0x2
9. Configure the MCASP pins functionality.	See Section 12.1.1.5.1.2.2.4 .	
10. Optional: Configure a MCASP Rx channel for a loopback operation (TDM mode only) in MCASP_DLBCTL [31-0].	See Section 12.1.1.4.14.1 , *Loopback Mode Configurations*.	0x-(5)
11. Release from reset state the divider that outputs the AHCLKR clock.(1) See also(2).	*MCASP_GBLCTL*[1] RHCLKRST	0x1
12. Poll the bit to ensure that it is successfully latched in the register. See also(2).	*MCASP_GBLCTL*[1] RHCLKRST	=0x1

Table 12-18. MCASP Receivers Global Initialization for TDM-Mode Operation (continued)

Step	Register/Bit Field/Programming Model	Value
13. Release from reset state the divider that outputs the ACLKR clock. (1) See also(3).	*MCASP_GBLCTL*[0] RCLKRST	0x1
14. Poll the bit to ensure that it is successfully latched in the register. See also(3).	*MCASP_GBLCTL*[0] RCLKRST	=0x1

---

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKRCTL* and *MCASP_ACLKRCTL* registers are ignored; hence, the reception clock does not stop during the reset state of the dividers.

(2) This step is necessary even if external high-frequency serial clocks are used.

(3) This step can be skipped if external serial clocks are used and they are running.

(4) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).

(5) In this case the receiver clock and frame sync are derived from the MCASP transmitter logic, so *MCASP_ACLKXCTL*[6] ASYNC must be set to 0b0. Neither MCASP internal receiver clock and frame sync generators, nor external clock and frame sync source are used.

12.1.1.5.1.2.2.1 Subsequence – Receive Format Unit Configuration in TDM Mode

The procedure in Table 12-19 configures the receive frame format unit of the MCASP module for TDM slots reception.

Table 12-19. Receive Format Unit Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_RFMT[7-4] RSSZ	0x-(1)
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_RMASK[31-0] RMASK	0x-(2)
Select a padding value for masked-out bits.	MCASP_RFMT[14-13] RPAD	0x-
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_RBUFn which value to be used as a pad value in case MCASP_RFMT[14-13] RPAD = 0x2. (n = 0 to 15)	MCASP_RFMT[12-8] RPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_RFMT[2-0] RROT	0x-(3)
Received stream bit order (LSB- or MSB-first). Must be set to 0x1 for an I2S stream reception (MSB-first).	MCASP_RFMT[15] RRVRS	0x-(3)
Specify a delay between frame sync and first bit of data in number of bits. Must be set to 0x1 for an I2S stream reception.	MCASP_RFMT[17-16] RDATDLY	0x-
Select to read data from active serializers receive buffers using peripheral (CFG) or DATA port	MCASP_RFMT[3] RBUSEL	0x-

---

(1) Refer to Section 12.1.1.4.4.2 , *Receive Format Unit*, regarding options for received TDM-slot sizes.

(2) For more details on Rx masking value, refer to Section 12.1.1.4.4.2.1 , *TDM - Mode Reception Data Alignment Settings*

(3) For more details on rotation and received TDM stream bit order, refer to Section 12.1.1.4.4.2.1 , *TDM - Mode Reception Data Alignment Settings* and Table 12-6, *MCASP RFU Settings*.

12.1.1.5.1.2.2.2 Subsequence – Receive Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 12-20 configures the transmit frame synchronization generator of the MCASP module.

Note

The same bit - *MCASP_ACLKXCTL*[6] ASYNC which is used to determine if MCASP receivers and transmitters work synchronously on the same clock, is also used to define if receiver frame sync is derived from the transmit frame sync generator, or generated independently in the receiver (either inernally or externally sourced). Hence, the settings in below table Table 12-20 have no effect, if *MCASP_ACLKXCTL*[6] ASYNC = 0.

Table 12-20. Receive Frame-Synchronization Generator Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame. Must be set to 0x2, in case of an I2S-reception. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 .	MCASP_AFSRCTL[15-7] RMOD	0x-[(1)]
Choose the receive frame sync width -single bit/single word. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 .	MCASP_AFSRCTL[4] FRWID	0x-
Select start of received frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 .	MCASP_AFSRCTL[0] FSRP	0x-
IFreceive frame sync - FS is internally generated	Software test condition	
Select internally- generated receive frame sync. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 .	MCASP_AFSRCTL[1] FSRM	0b1
If MCASP receiver is required to output internally generated frame, AFSR pin must be set as an output in step 9 of the sequence documented in the Table 12-18. This must not be done in current step because the frame control register - MCASP_AFSXCTL must be appropriately configured prior to AFSR pin outputting a frame to an external device.	*MCASP_PDIR*[31] AFSR	0b1
ELSE		
Select externally- generated receive frame sync. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 .	MCASP_AFSRCTL[1] FSRM	0b0
Setup the AFSR pin as input (device level: MCASPi_AFSR)	*MCASP_PDIR*[31] AFSR	0b0
ENDIF		
To generate MCASP receive frame sync in receiver logic, select an asynchronous frame sync.	*MCASP_ACLKXCTL*[6] ASYNC	0b1

(1) Must be set to 0x180 in case of 384-TDM slot frame reception from a DIR component I2S-output. For more details on TDM-frame settings, refer to *Module Integration*.

12.1.1.5.1.2.2.3 Subsequence – Receive Clock Generator Configuration

The procedure in Table 12-21 configures the receive clock generator of the MCASP module.

> **Note**
>
> The settings in below table Table 12-21 have no effect, if *MCASP_ACLKXCTL*[6] ASYNC = 0 (this is, receive clock is sourced from the inverted version of the transmit clock). For example, such is the case when MCASP loopback mode is used.

Table 12-21. Receive Clock Generator Configuration

Step	Register/Bit Field/Programming Model	Value
To use the MCASP receive clock generator, select an asynchronous receiver clock schema (ASYNC = 1). Otherwise an inverted version of transmit clock XCLK is used (receiver synchronized with transmitter).	*MCASP_ACLKXCTL*[6] ASYNC	0b1
IF receive clock - RCLK is internally generated	Software test condition	
The high-speed receive clock - AHCLKR is internally generated based on AUXCLK		

Table 12-21. Receive Clock Generator Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Select an internally-generated high-frequency clock.	*MCASP_AHCLKXCTL*[15] HCLKRM	0b1
Select the internal high-speed clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKRP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKR in range (1 - 4096).	*MCASP_AHCLKXCTL*[11-0] HCLKRDIV	0x-
Select an internally-generated receive clock.	*MCASP_ACLKXCTL*[5] CLKRM	0b1
Receiver samples on rising/falling edge. Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKRP	0x-
Set the divisor for the internally generated receive clock– ACLKR in range (1 - 32).	*MCASP_ACLKXCTL*[4-0] CLKRDIV	0x-
Optional: If MCASP receiver is required to output internally generated clock, ACLKR pin must be set as an output in step 9 of the sequence documented in the Table 12-18. This must not be done in current step because the clock control register - *MCASP_ACLKRCTL* must be appropriately configured prior to ACLKR pin outputting a receive clock to an external device.	*MCASP_PDIR*[29] ACLKR	0b1
ELSE		
Select an externally-generated receive clock. Note that in this case the AHCLKR signal path and the CLKRDIV divider are NOT used.	*MCASP_ACLKXCTL*[5] CLKRM	0b0
Receiver samples on rising/falling edge. Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKRP	0x-
Setup an input direction for the ACLKR pin	*MCASP_PDIR*[29] ACLKR	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 12.1.1.4.15.6.1 , *Clock Failure Check Startup*.	

12.1.1.5.1.2.2.4 Subsequence—MCASP Receiver Pins Functional Configuration

The procedure in Table 12-22 configures the MCASP pins for MCASP functionality.

Table 12-22. MCASP Receiver Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins direction: AFSR ACLKR Desired n-th MCASP data pin AXRn is configured as an input for receiving.	*MCASP_PDIR*[31] AFSR; *MCASP_PDIR*[29] ACLKR; *MCASP_PDIR*[n] AXRn;	0x-(1) 0x-(2) 0x0

(1) See Table 12-20.

(2) For more details on MCASP clock configurations, refer to Table 12-21.

12.1.1.5.1.2.3 Main Sequence – MCASP Global Initialization for TDM -Transmission

The procedure in Table 12-23 initializes a MCASP serializer n transmitter(s) to operate in TDM-mode after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols transmission.

CAUTION

Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Table 12-23. MCASP Transmitters Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP transmit components.	*MCASP_GBLCTL*[12-8]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[12-8]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1
4. Configure the transmit format unit.	See Section 12.1.1.5.1.2.3.1 .	
5. Configure the transmit frame sync generator.	See Section 12.1.1.5.1.2.3.2 .	
6. Configure the transmit clock generator.	See Section 12.1.1.5.1.2.3.3 .	
7. Program all bits - XTDMSk, where k = 0 to 31, according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_XTDM[k] XTDMSk, where k = 0 to 31(4)	0x-
8. Configure the desired n-th serializer for transmit mode operation.(3)	MCASP_SRCTLn[1-0] SRMOD; n = 0 to 15	0x1
9. Setup all active transmitters to operate in TDM mode.	MCASP_DITCTL[0] DITEN	0x0(2)
10. Configure the MCASP pins functionality.	See Section 12.1.1.5.1.2.3.4 .	
11. Optional: Configure a MCASP Tx channel for loopback operation (TDM mode only) in MCASP_DLBCTL [31-0].	See Section 12.1.1.4.14.1 , *Loopback Mode Configurations*.	0x-
12. Release from reset state the divider that outputs the AHCLKR clock. See(1)	*MCASP_GBLCTL*[9] XHCLKRST	0x1
13. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[9] XHCLKRST	=0x1
14. Release from reset state the divider that outputs the ACLKR clock. See(1)	*MCASP_GBLCTL*[8] XCLKRST	0x1
15. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[8] XCLKRST	=0x1

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKXCTL* and *MCASP_ACLKXCTL* registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.

(2) All active transmit channels operate either in TDM mode or in DIT mode depending on DITEN value. There is no option to choose Tx Mode between DIT and TDM separately per serializer transmitter.

(3) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).

(4) Appropriately program in the MCASP_SRCTLn[3-2] DISMOD bit field, the desired level (high-impedance state, 0, or 1) at AXRn output, during time of inactive slots. Note, that this setting does NOT apply when all slots are programmed to be active within a frame (in particular DIT-mode) (n = 0 to 15).

12.1.1.5.1.2.3.1 Subsequence – Transmit Format Unit Configuration in TDM Mode

The procedure in Table 12-24 configures the transmit frame format unit of the MCASP module for TDM slots transmission.

Table 12-24. Transmit Format Unit Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_XFMT[7-4] XSSZ	0x-(1)

Table 12-24. Transmit Format Unit Configuration for TDM-Transmission (continued)

Step	Register/Bit Field/Programming Model	Value
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_XMASK[31-0] XMASK	0x-[2]
Select a padding value for masked-out bits.	MCASP_XFMT[14-13] XPAD	0x-
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_XBUFn which value to be used as a pad value in case MCASP_XFMT[14-13] XPAD = 0x2 (n = 0 to 15).	MCASP_XFMT[12-8] XPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_XFMT[2-0] XROT	0x-[3]
transmitted stream bit order (LSB- or MSB-first). Must be set to 0x1 for an I2S stream transmission (MSB-first).	MCASP_XFMT[15] XRVRS	0x-[3]
Specify a delay between frame sync and first bit of data in number of bits. Must be set to 0x1 for an I2S stream transmission.	MCASP_XFMT[17-16] XDATDLY	0x-
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_XFMT[3] XBUSEL	0x-

(1) Refer to Section 12.1.1.4.4.1 , *Transmit Format Unit* , regarding options for transmitted TDM-slot sizes.

(2) For more details on Tx masking value, refer to Section 12.1.1.4.4.1.1 , *TDM - Mode Transmission Data Alignment Settings*

(3) For more details on rotation and transmitd TDM stream bit order, refer to Section 12.1.1.4.4.1.1 , *TDM - Mode Transmission Data Alignment Settings* and Table 12-4, *MCASP TFU TDM Mode Settings*.

12.1.1.5.1.2.3.2 Subsequence – Transmit Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 12-25 configures the transmit frame synchronization generator of the MCASP module.

Table 12-25. Transmit Frame-Synchronization Generator Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame (2 - 32). Must be set to 0x2, in case of an I2S-transmission. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 , *Frame-Sync Generator*.	MCASP_AFSXCTL[15-7] XMOD	0x-
Choose the transmit frame sync width -single bit/single word. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 , *Frame-Sync Generator*.	MCASP_AFSXCTL[4] FXWID	0x-
Select start of transmit frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 , *Frame-Sync Generator*.	MCASP_AFSXCTL[0] FSXP	0x-
IF transmit frame sync - FS is internally generated	Software test condition	
Select internally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 , *Frame-Sync Generator*.	MCASP_AFSXCTL[1] FSXM	0b1
If MCASP transmitter is required to output internally generated frame, AFSX pin must be set as an output in step 10 of the sequence documented in the Table 12-23. This must NOT be done in current step because the frame control register - MCASP_AFSXCTL must be appropriately configured prior to AFSX pin outputting a frame sync to an external device.	*MCASP_PDIR*[28] AFSX	0b1
ELSE		
Select externally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 12.1.1.4.2.3 , *Frame-Sync Generator*.	MCASP_AFSXCTL[1] FSXM	0b0
Setup the AFSX pin as input	*MCASP_PDIR*[28] AFSX	0b0

12.1.1.5.1.2.3.3 Subsequence – Transmit Clock Generator Configuration for TDM Cases

The procedure in Table 12-26 configures the transmit clock generator of the MCASP module.

Table 12-26. Transmit Clock Generator Configuration for TDM Cases

Step	Register/Bit Field/Programming Model	Value
IF transmit clock - XCLK is internally generated	Software test condition	
IF high-speed transmit clock - AHCLKX is internally generated based on AUXCLK	Software test condition	
Select an internally-generated high-frequency clock.	*MCASP_AHCLKXCTL*[15] HCLKXM	0b1
Select the high-frequency clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKXP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKX in range (1 - 4096).	*MCASP_AHCLKXCTL*[11-0] HCLKXDIV	0x-
Optional: If MCASP transmitter is required to output internally generated high-frequency clock, AHCLKX pin must be set as an output in step 10 of the sequence documented in the Table 12-23. This must NOT be done in current step because the clock control register - *MCASP_AHCLKXCTL* must be appropriately configured prior to AHCLKX pin outputting a high-speed clock to an external device.	*MCASP_PDIR*[27] AHCLKX	0b1
ELSE		
Select an externally-generated high frequency clock (HCLKXDIV divider can not be used).	*MCASP_AHCLKXCTL*[15] HCLKXM	0b0
Select the high-speed transmit clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKXP	0x-
Setup an input directon for the AHCLKX pin	*MCASP_PDIR*[27] AHCLKX	0b0
ENDIF		
Select an internally-generated transmit clock.	*MCASP_ACLKXCTL*[5] CLKXM	0b1
Transmitter samples on rising/falling edge. Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKXP	0x-
Set the divisor for the internally generated transmit clock– ACLKX in range (1 - 32).	*MCASP_ACLKXCTL*[4-0] CLKXDIV	0x-
Optional: If MCASP transmitter is required to output internally generated clock, ACLKX pin) must be set as an output in step 10 of the sequence documented in the Table 12-23. This must NOT be done in current step because the clock control register - *MCASP_ACLKXCTL* must be appropriately configured prior to ACLKX pin outputting a transmit clock to an external device.	*MCASP_PDIR*[26] ACLKX	0b1
ELSE		
Select an externally-generated transmit clock. Note that in this case the AHCLKX signal path and the CLKXDIV divider are NOT used.	*MCASP_ACLKXCTL*[5] CLKXM	0b0
Transmitter samples on rising/falling edge. Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKXP	0x-
Setup an input directon for the ACLKX pin	*MCASP_PDIR*[26] ACLKX	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 12.1.1.4.15.6.1 , *Clock Failure Check Startup*.	

12.1.1.5.1.2.3.4 Subsequence—MCASP Transmit Pins Functional Configuration

The procedure in Table 12-27 configures the MCASP pins for MCASP functionality.

Table 12-27. MCASP Transmit Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins direction: AFSX AHCLKX ACLKX Desired n-th MCASP data pin AXRn is configured as an ouput for transmission.	*MCASP_PDIR*[28] AFSR; *MCASP_PDIR*[27] AHCLKR; *MCASP_PDIR*[26] ACLKR; *MCASP_PDIR*[n] AXRn	0x-(1) 0x-(2) 0x-(2) 0x1

(1) See Table 12-25.

12.1.1.5.2 MCASP Operational Modes Configuration

12.1.1.5.2.1 MCASP Transmission Modes

12.1.1.5.2.1.1 Main Sequence – MCASP DIT- /TDM- Polling Transmission Method

Figure 12-27 shows the MCASP DIT-/TDM- polling method.

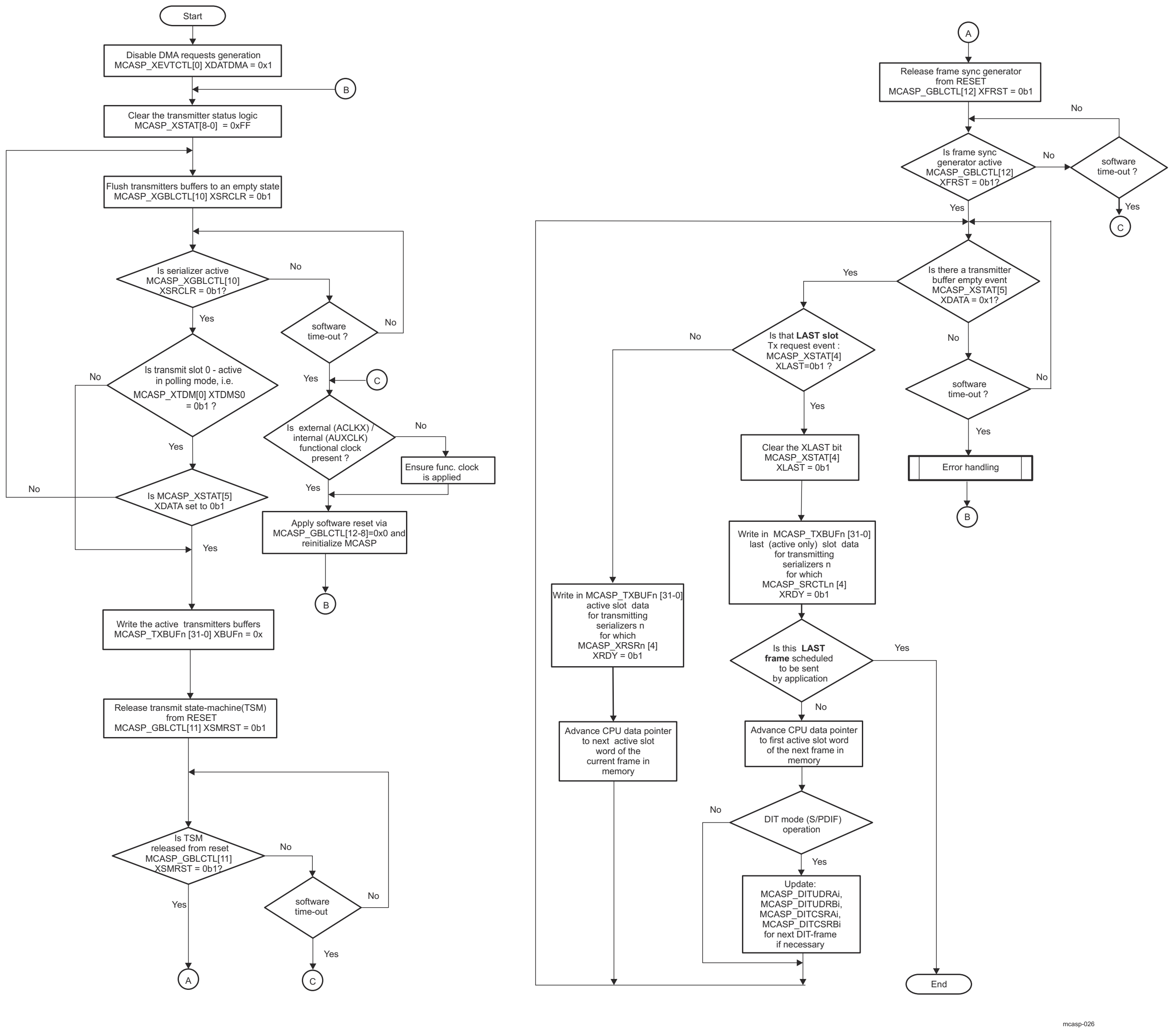

Figure 12-27. MCASP DIT- /TDM- Transmission Polling Method

These registers are for MCASP DIT-/TDM- transmission polling method: *MCASP_XEVTCTL*, MCASP_XSTAT, *MCASP_GBLCTL*, MCASP_XTDM, MCASP_XBUFn, MCASP_SRCTLn, MCASP_DITUDRAi, MCASP_DITUDRBi, MCASP_DITCSRAi, MCASP_DITCSRBi (n = 0 to 15 and i = 0 to 5).

Table 12-28 summarizes the subprocess call for the DIT-/TDM- transmission polling mode.

Table 12-28. Subprocess Call Summary for Main Sequence – MCASP DIT-/TDM- Transmission Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 12-33

12.1.1.5.2.1.2 Main Sequence – MCASP DIT- /TDM - Interrupt Transmission Method

Figure 12-28 shows the initial setup for interrupt-based transmission.

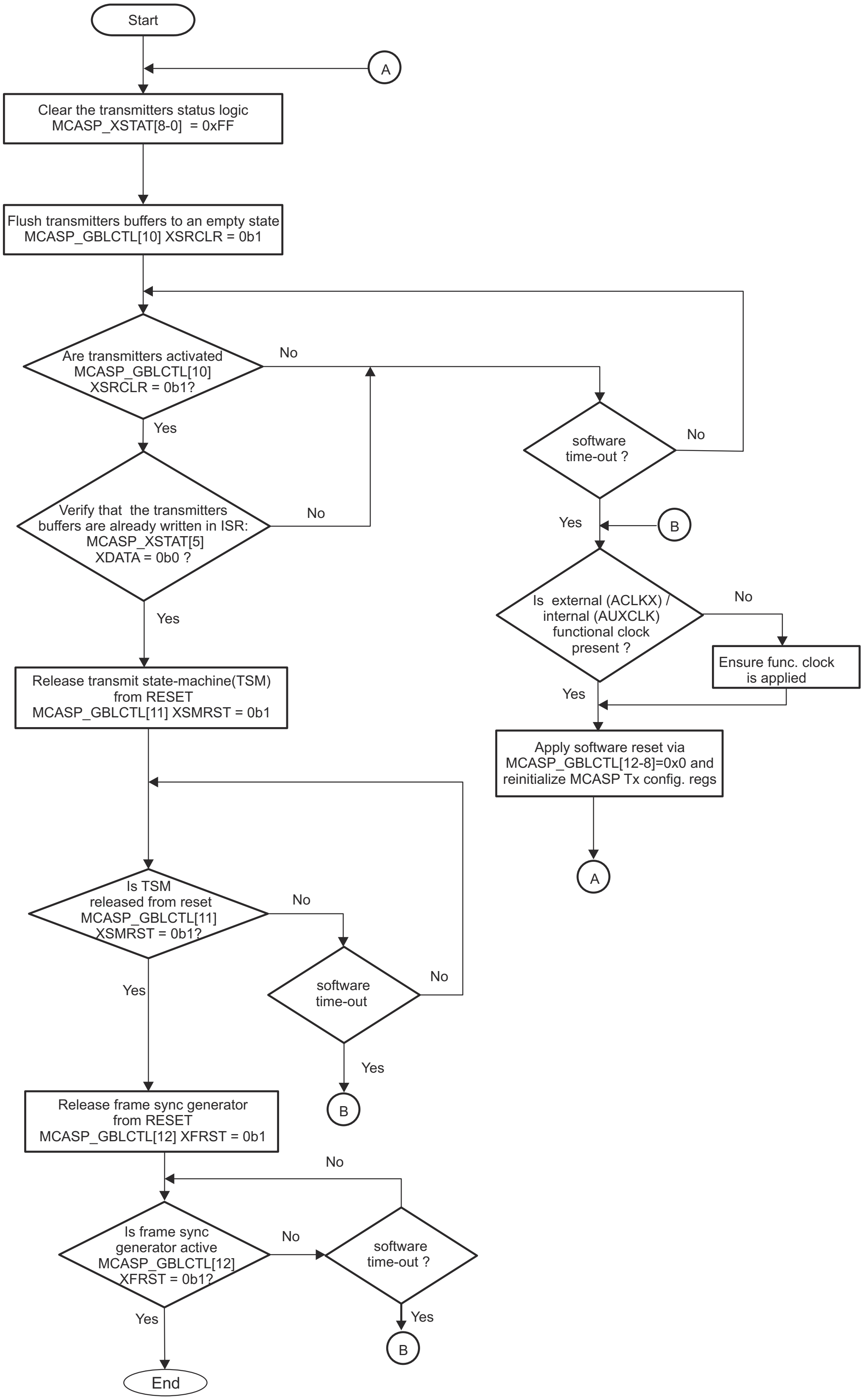

Figure 12-28. Subsequence – DIT-/TDM- Transmission Startup Procedure

Table 12-29 shows the configuration of the MCASP using an interrupt method for DIT-/TDM- transmission.

Table 12-29. MCASP DIT-/TDM- Interrupt Transmission Model

Step	Register/Bit Field/Programming Model	Value
Disable Tx DMA requests generation.	*MCASP_XEVTCTL*[0] XDATDMA	0x1
Enable the data ready event transmit interrupt.	MCASP_XINTCTL[5] XDATA	0x1
Optional: Enable the transmit error event interrupts.	MCASP_XINTCTL[2] XCKFAIL MCASP_XINTCTL[1] XSYNCERR MCASP_XINTCTL[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt (useful for DIT user data/ channel status next S/PDIF frame info update).	MCASP_XINTCTL[7] XSTAFRM MCASP_XINTCTL[4] XLAST	0x1 0x1
IFwrite transfer is through the MCASP DATA port (MCASP_XFMT[3] XBUSEL is set to 0b0).	Software test condition (setting is done in step4 of the *MCASP Transmitters Global Initialization* - see Table 12-12)	
Enable the DATA port error based interrupt.	MCASP_XINTCTL[3] XDMAERR	0x1
ELSE		
Disable the DATA port error based interrupt.	MCASP_XINTCTL[3] XDMAERR	0x0
ENDIF		
DIT/TDM - Transmission Startup Procedure	See Figure 12-28.	

These registers are for MCASP DIT-/TDM- transmission startup procedure: *MCASP_GBLCTL*, *MCASP_XSTAT*.

12.1.1.5.2.1.3 Main Sequence –MCASP DIT- /TDM - Mode DMA Transmission Method

Table 12-30 shows the configuration of the ↓ using the DMA method for transmission. Possible interrupt error event servicing is also considered. shows the initial setup for DMA - based transmission.

Note

Because of the DATA port burst access capability with the DMA method, it is strongly recommended that DMA transfers are initiated through the MCASP DATA port.

Table 12-30. MCASP DMA Transmission Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Recommended: Select DATA port to access the transmit buffers.	MCASP_XFMT[3] XBUSEL	0x0
Enable the Tx DMA requests generation.	*MCASP_XEVTCTL*[0] XDATDMA	0x0
Enable the Tx DMA error event, because of MCASP DATA port usage.	MCASP_XINTCTL[3] XDMAERR	0x1
Optional: Enable the transmit error event interrupts.	MCASP_XINTCTL[2] XCKFAIL MCASP_XINTCTL[1] XSYNCERR MCASP_XINTCTL[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_XINTCTL[7] XSTAFRM MCASP_XINTCTL[4] XLAST	0x1 0x1
Disable the data ready event transmit interrupt, as DMA is used to service this request.	MCASP_XINTCTL[5] XDATA	0x0
DMA startup transmission procedure. This procedure is identical than the one shown in Figure 12-28. The only difference is that DMA automatically services all the XINT events raised by the MCASP, and no CPU data processing intervention is required. The CPU is involved only in error handling shown in Figure 12-31.	See Figure 12-28.	

12.1.1.5.2.2 MCASP Reception Modes

12.1.1.5.2.2.1 Main Sequence – MCASP Polling Reception Method

Figure 12-29 shows the MCASP polling reception method.

Note

The MCASP polling reception model considers thedevice CPUs as the accessor of audio data from the MCASP receive buffers.

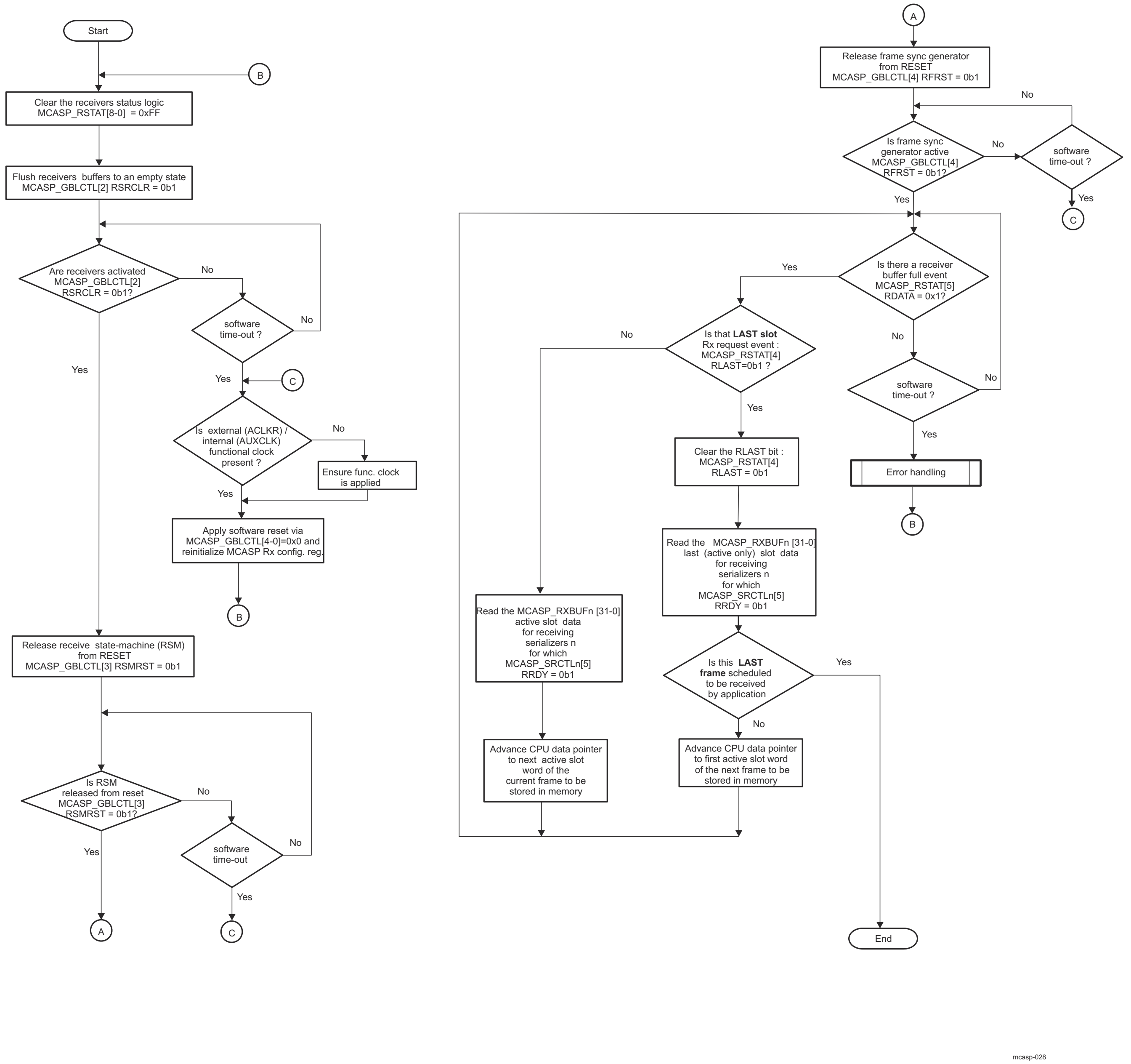

Figure 12-29. MCASP Polling Reception Method

These registers are for MCASP reception polling method: MCASP_RSTAT, MCASP_XGBLCTL, MCASP_RBUFn, MCASP_SRCTLn (n = 0 to 15).

Table 12-31 summarizes the subprocess call for the polling mode.

Table 12-31. Subprocess Call Summary for Main Sequence – MCASP Reception Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 12-34

12.1.1.5.2.2.2 Main Sequence – MCASP TDM - Interrupt Reception Method

Figure 12-30 shows the initial setup for interrupt-based reception.

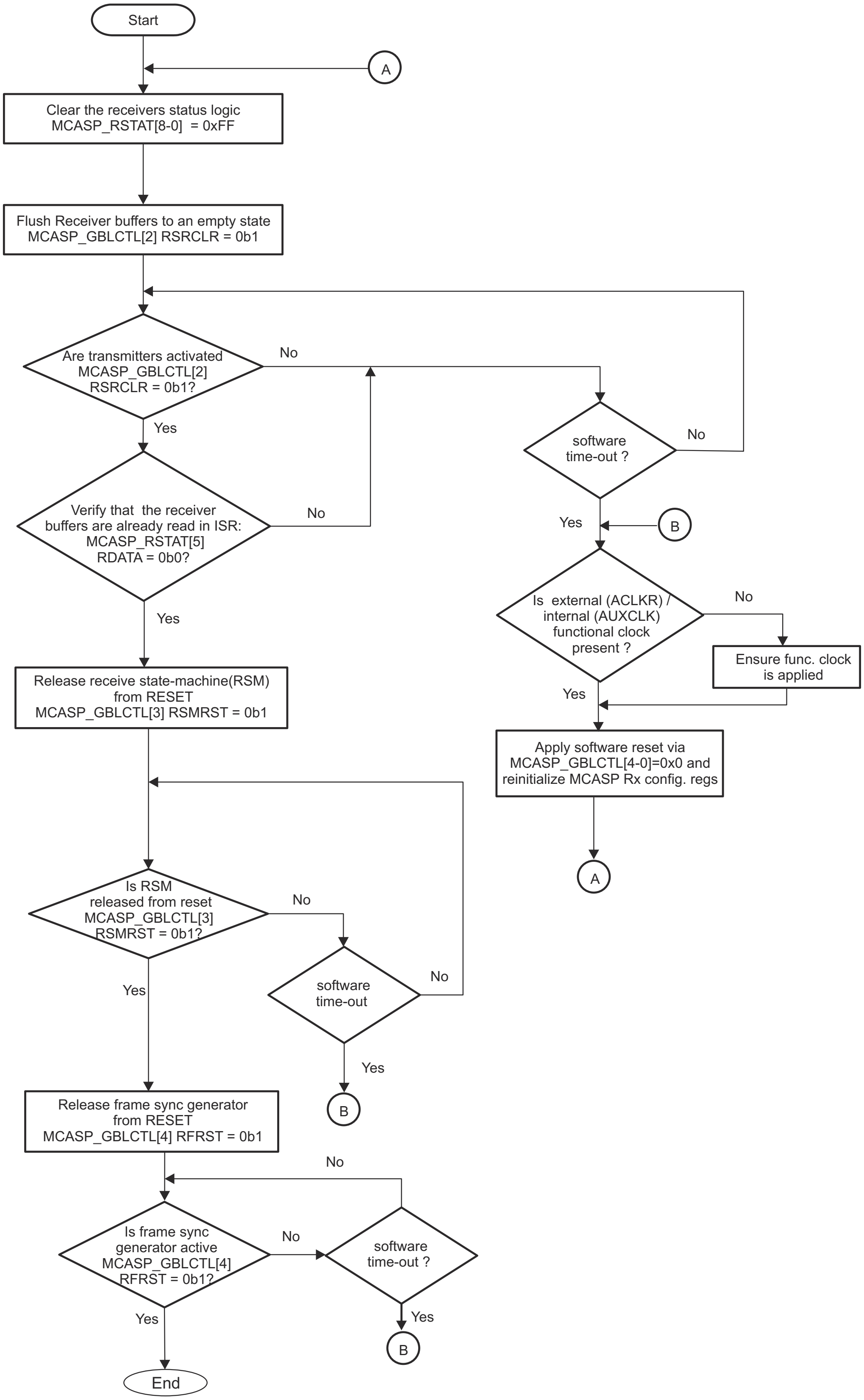

Figure 12-30. Subsequence – TDM - Reception Startup Procedure

Table 12-32 shows the configuration of the MCASP using an interrupt method for TDM- reception.

Table 12-32. MCASP TDM- Interrupt Reception Model

Step	Register/Bit Field/Programming Model	Value
Disable Rx DMA requests generation.	MCASP_PIDTCTL[0] RDATDMA	0x1
Enable the data ready event receive interrupt.	MCASP_RINTCTL[5] RDATA	0x1
Optional: Enable the receive error event interrupts.	MCASP_RINTCTL[2] RCKFAIL MCASP_RINTCTL[1] RSYNCERR MCASP_RINTCTL[0] ROVRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt	MCASP_RINTCTL[7] RSTAFRM MCASP_RINTCTL[4] RLAST	0x1 0x1
IF read transfer is through the MCASP DATA port (MCASP_RFMT[3] RBUSEL is set to 0b0).	Software test condition (setting is done in step4 of the *MCASP Receivers Global Initialization for TDM-Mode Operation* - see Table 12-18)	
Enable the DATA port error based interrupt.	MCASP_RINTCTL[3] RDMAERR	0x1
ELSE		
Disable the DATA port error based interrupt.	MCASP_RINTCTL[3] RDMAERR	0x0
ENDIF		
TDM - Transmission Startup Procedure	See Figure 12-30.	

These registers are for MCASP TDM- interrupt reception model: MCASP_XGBLCTL, MCASP_RSTAT.

12.1.1.5.2.2.3 Main Sequence – MCASP TDM - Mode DMA Reception Method

Table 12-33 shows the configuration of the MCASP using the DMA method for reception. Possible interrupt error event servicing is also considered. shows the initial setup for DMA - based transmission.

Note

Because of the DATA port burst access capability with the DMA method, it is strongly recommended that DMA transfers are initiated through the MCASP DATA port.

Table 12-33. MCASP DMA Reception Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Recommended: Select DATA port to access the transmit buffers.	MCASP_RFMT[3] RBUSEL	0x0
Enable the Rx DMA requests generation.	MCASP_PIDTCTL[0] RDATDMA	0x0
Enable the Rx DMA error event, because of MCASP DATA port usage.	MCASP_RINTCTL[3] RDMAERR	0x1
Optional: Enable the receive error event interrupts.	MCASP_RINTCTL[2] RCKFAIL MCASP_RINTCTL[1] RSYNCERR MCASP_RINTCTL[0] ROVRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_RINTCTL[7] RSTAFRM MCASP_RINTCTL[4] RLAST	0x1 0x1
Disable the data ready event receive interrupt, as DMA is used to service this request.	MCASP_RINTCTL[5] RDATA	0x0
DMA startup reception procedure. This procedure is identical than the one shown in Figure 12-30. The only difference is that DMA automatically services all the RINT events raised by the MCASP, and no CPU data processing intervention is required. The CPU is involved only in error handling shown in Figure 12-32.	See Figure 12-30.	

12.1.1.5.2.3 MCASP Event Servicing

12.1.1.5.2.3.1 MCASP DIT-/TDM- Transmit Interrupt Events Servicing

Figure 12-31 shows the flow of DIT-/TDM- mode transmit interrupt events servicing for the MCASP module.

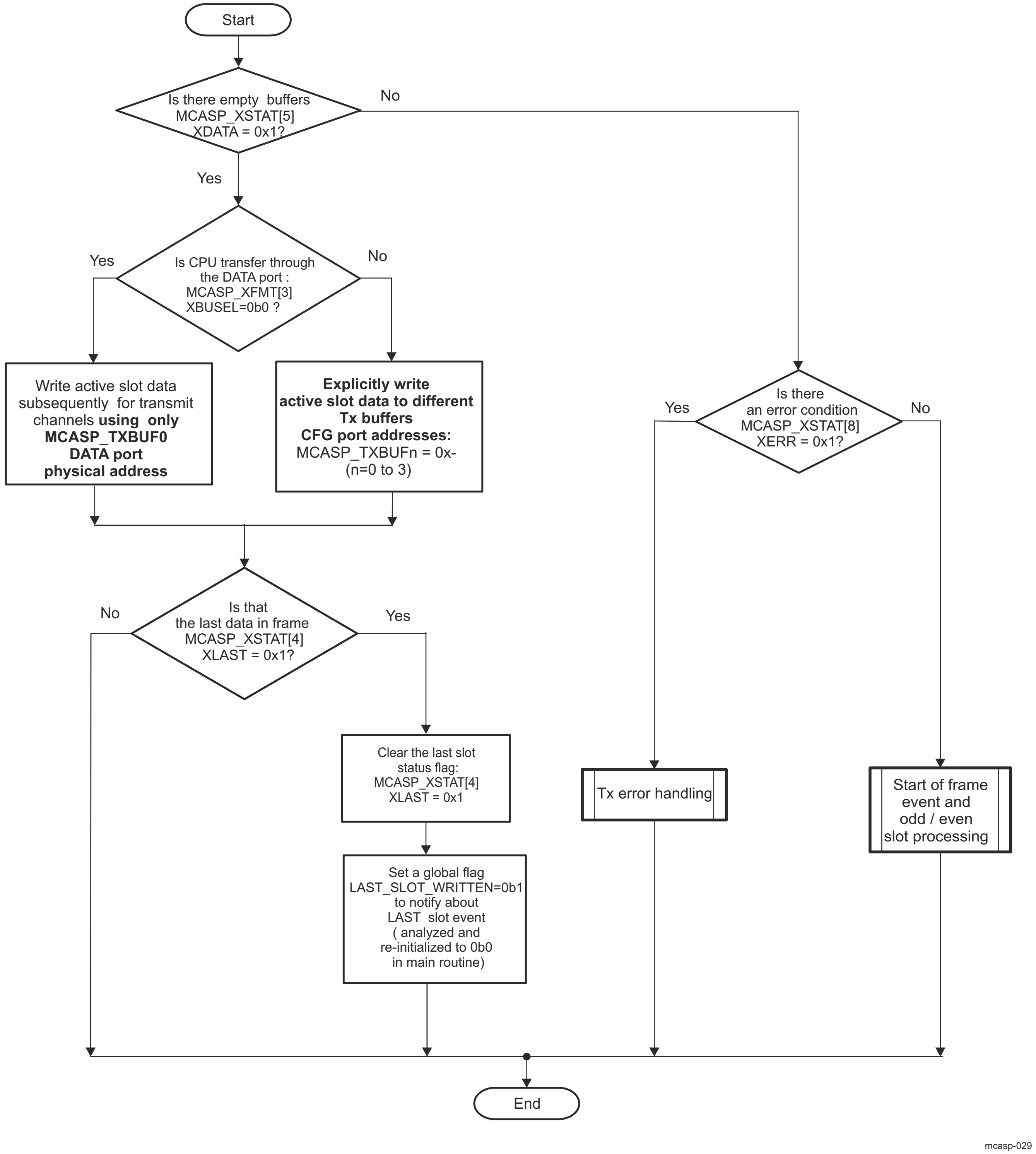

Figure 12-31. MCASP Transmit Interrupt Events Servicing

12.1.1.5.2.3.2 MCASP TDM- Receive Interrupt Events Servicing

Figure 12-32 shows the flow of DIT-/TDM- mode transmit interrupt events servicing for the MCASP module.

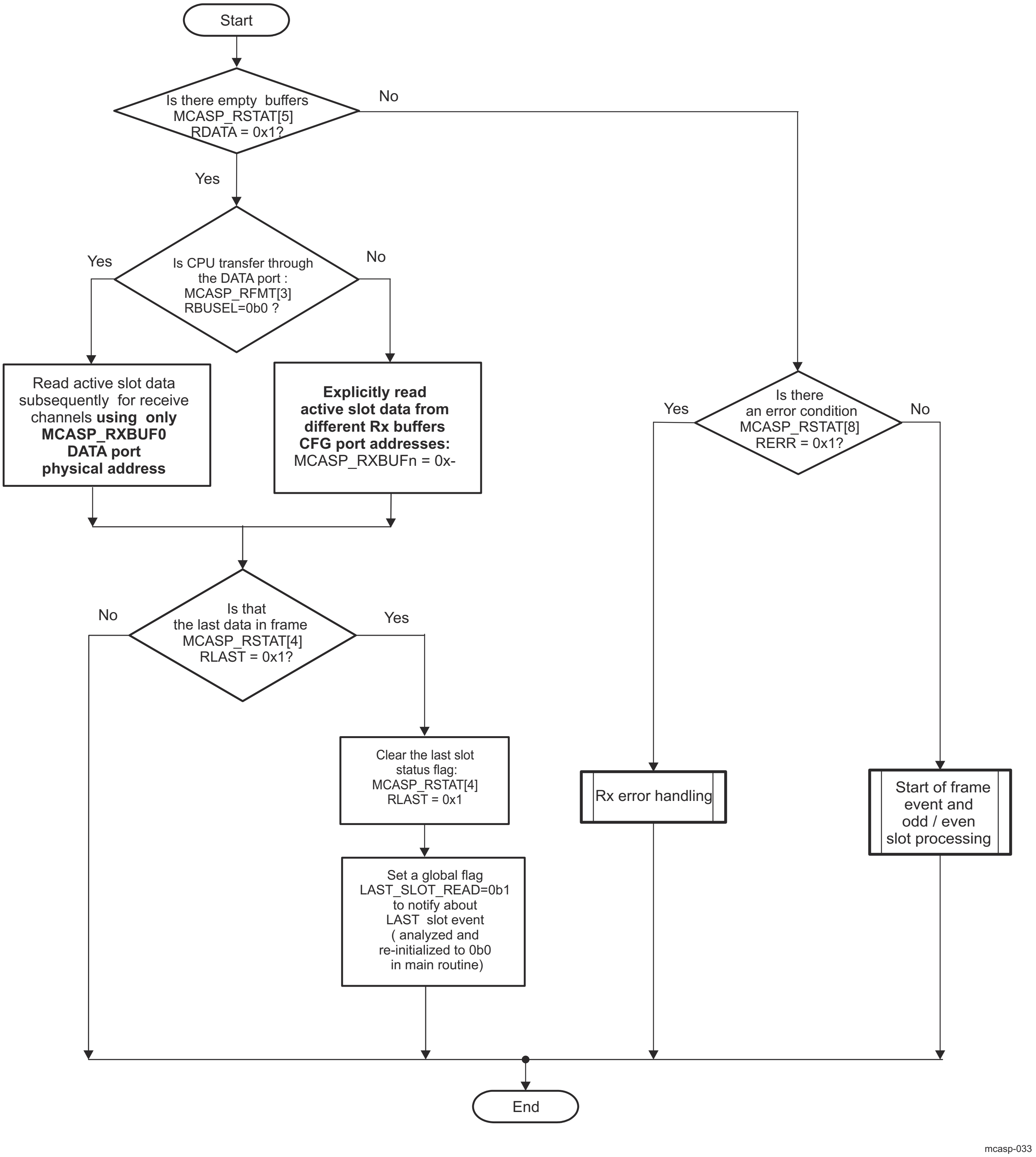

Figure 12-32. MCASP Receive Interrupt Events Servicing

These registers are for MCASP receive interrupt events servicing: MCASP_RSTAT, MCASP_RBUFn, MCASP_RFMT (n = 0 to 15).

Table 12-34 lists the subprocess call summary for receive interrupt events servicing.

Table 12-34. Subprocess Call Summary for Receive Interrupt Events Servicing

Subprocess Name	Cross-Reference
MCASP receive error handling	Figure 12-34
Start of frame handling	Section 12.1.1.4.12.2 , *Receive Data Ready Event and Interrupt*

12.1.1.5.2.3.3 Subsequence – MCASP DIT-/TDM -Modes Transmit Error Handling

Figure 12-33 shows the transmit error handling schema for the MCASP, which can be implemented as part of the Tx interrupt service routine or as part of the Tx polling sequence.

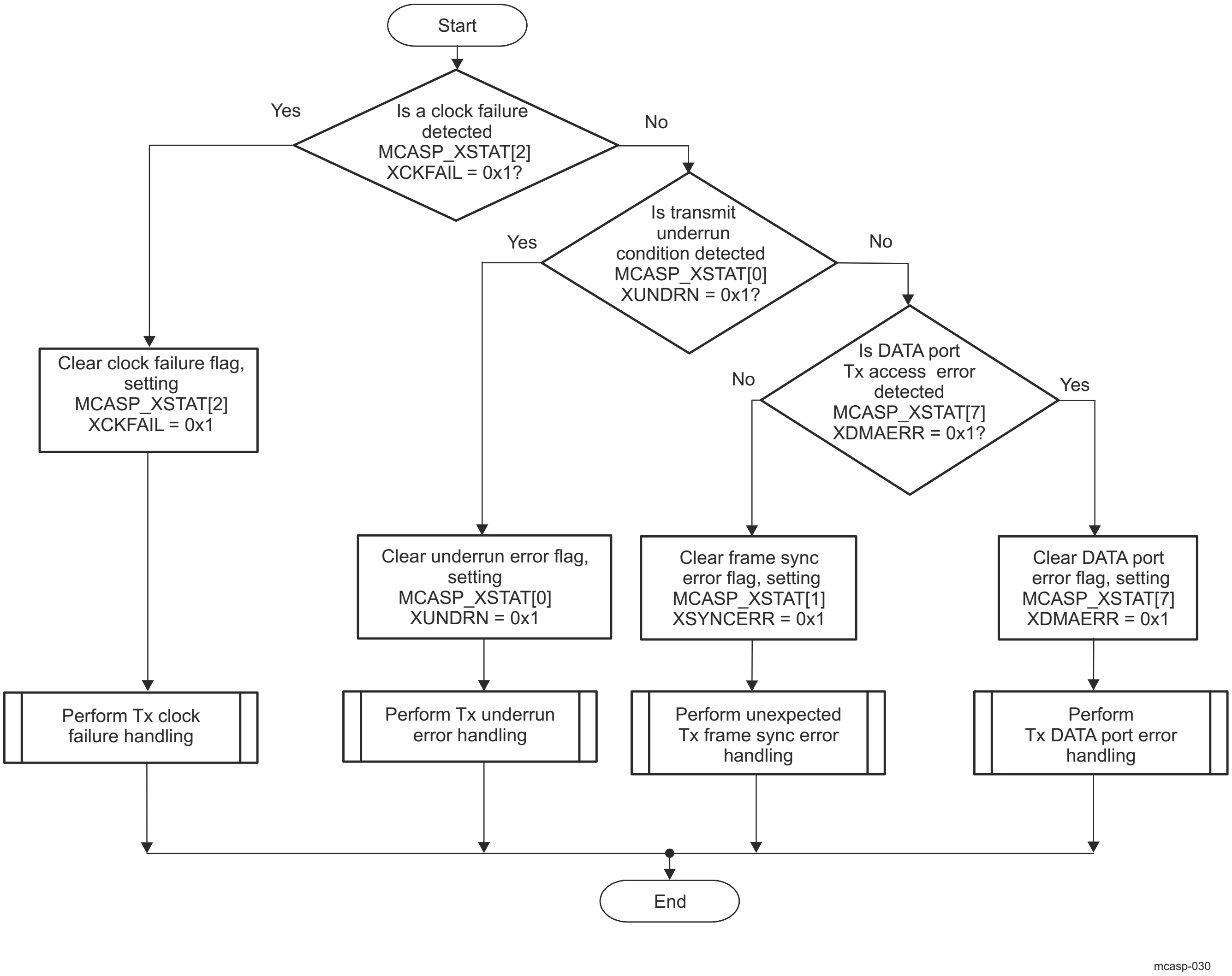

Figure 12-33. MCASP Transmit Error Handling

Note

- For more information about transmit clock failure handling, see Section 12.1.1.4.15.6.2 , *Transmit Clock Failure Check and Recovery*.
- For more information about transmit buffer underrun handling, see Section 12.1.1.4.15.1 , *Buffer Underrun Error -Transmitter*.
- For more information about DATA port Tx error handling, see Section 12.1.1.4.15.3 , *DATA Port Error - Transmitter*.
- For more information about unexpected Tx frame sync error handling, see Section 12.1.1.4.15.5 , *Unexpected Frame Sync Error*.

12.1.1.5.2.3.4 Subsequence – MCASP Receive Error Handling

Figure 12-34 shows the receive error handling schema for the MCASP, which can ONLY be implemented as part of the Rx polling sequence.

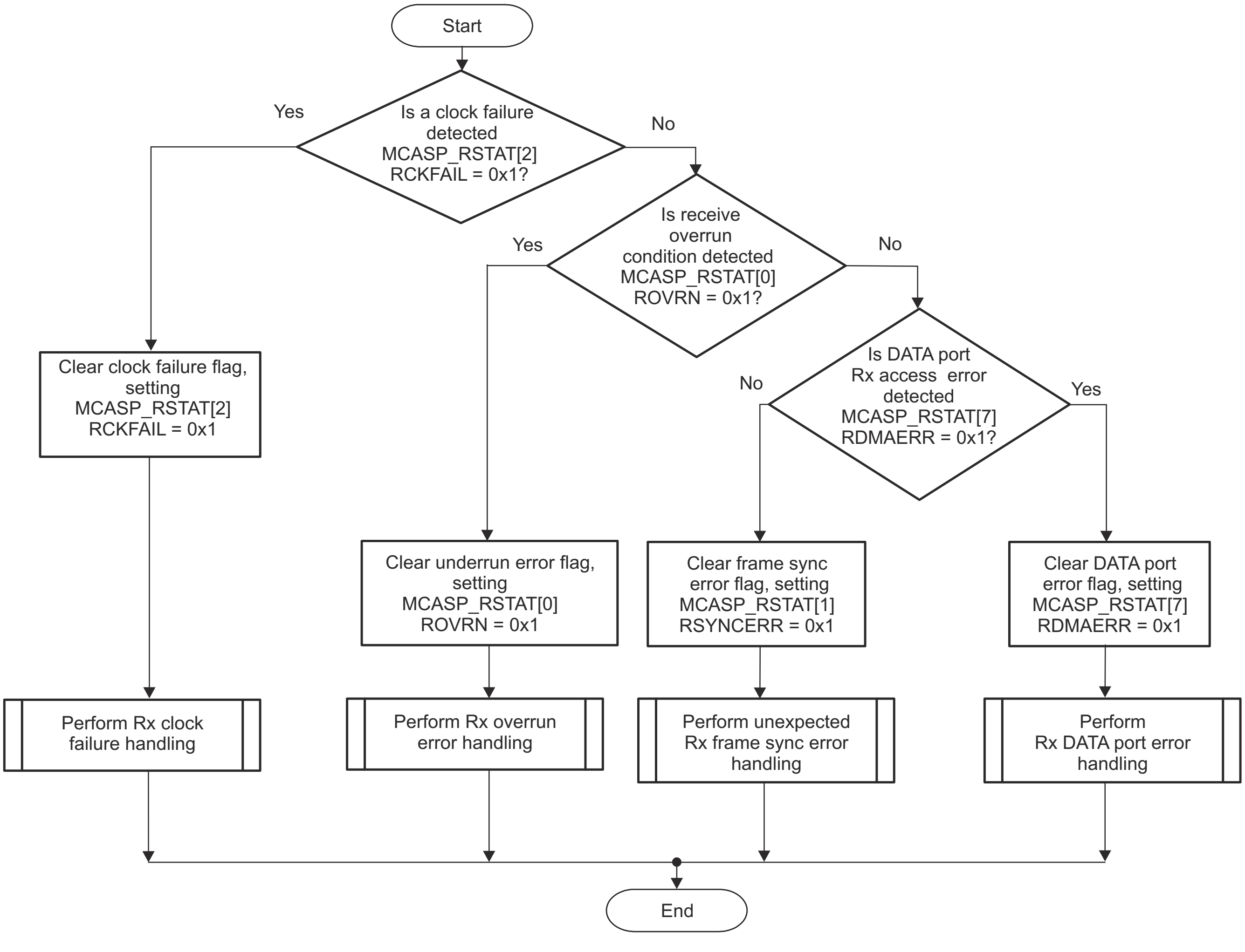

Figure 12-34. MCASP Receive Error Handling

This register is for MCASP receive error handling: MCASP_RSTAT.

Note

- For more information about receive clock failure handling, see Section 12.1.1.4.15.6.3 , *Receive Clock Failure Check and Recovery*.
- For more information about receive buffer overrun handling, see Section 12.1.1.4.15.2 , *Buffer Overrun Error - Receiver*.
- For more information about DATA port Rx error handling, see Section 12.1.1.4.15.4 , *DATA Port Error - Receiver*.
- For more information about unexpected Rx frame sync error handling, see Section 12.1.1.4.15.5 , *Unexpected Frame Sync Error*.

12.2 General Connectivity Peripherals

This section describes the general connectivity peripherals in the device.

12.2.1 General-Purpose Interface (GPIO)

This chapter describes the General-Purpose Input/Output (GPIO) for the device.

12.2.1.1 GPIO Overview

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

The device has one or more instances of GPIO modules. The GPIO pins are grouped into banks (16 pins per bank and 9 banks per module), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Not all GPIO pins are pinned out. See General Purpose Input/Output (GPIO) in the Module Integration section for more information.

Figure 12-35 presents the GPIO modules overview.

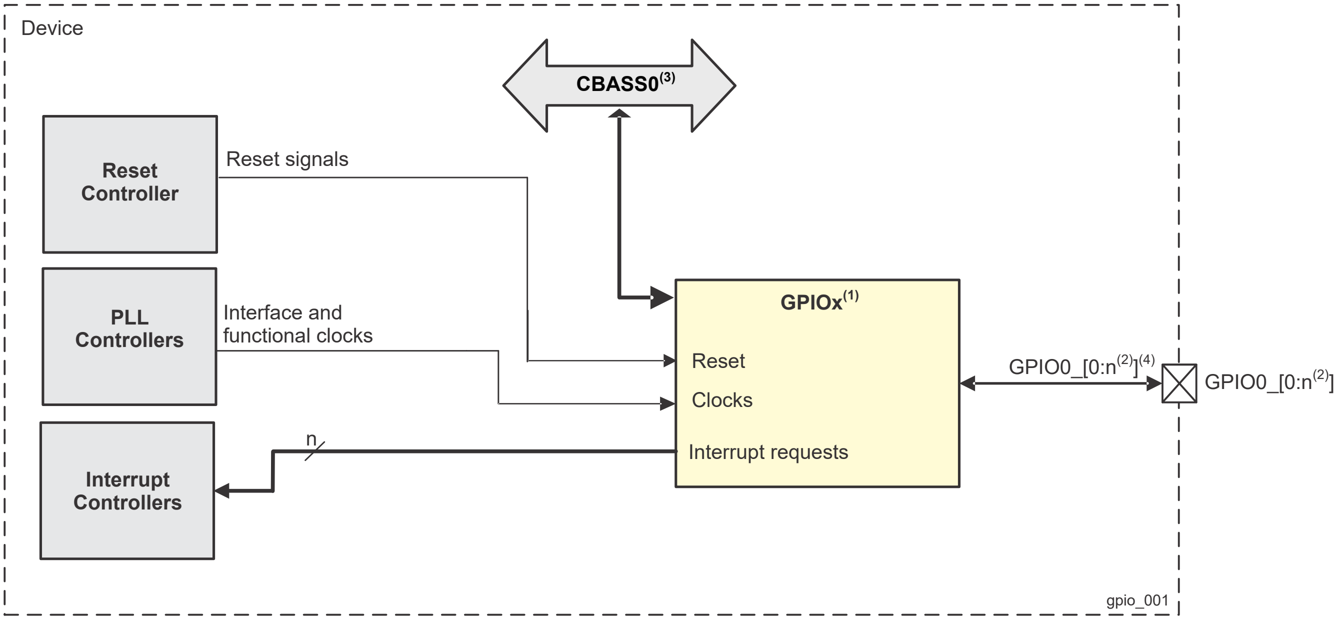

Figure 12-35. GPIO Modules Overview

Note

(1): x represents a valid instance of GPIO in a domain.

Note

(2): n represents the maximum number of GPIO signals -1.

Note

(3): CBASS0 represents the connectivity in the domain of the IP.

Note

(4): Some GPIO signals may be uni-directional. Consult the device datasheet for specifics.

12.2.1.1.1 GPIO Features

Each channel in the GPIO modules has the following features:

- Supports 9 banks of 16 GPIO signals
- Supports up to 9 banks of interrupt capable GPIOs
- Interrupts:
  - Can enable interrupts for each bank of 16 GPIO signals
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- Set/clear functionality:
  - Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate Input/Output registers:
  - If preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s) in addition to set/clear.
  - Output register, when read in, reflects output drive status. This, in addition to the input register reflecting pin status, allows wired logic be implemented.

12.2.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.2.1.2 GPIO Environment

This section describes the GPIO external connections (environment).

The general-purpose interface combines three GPIO modules for a flexible, user-programmable, general-purpose input/output (I/O) controller. The general-purpose interface implements functions that are not implemented with the dedicated controllers in the device and require simple input and/or output software-controlled signals. The GPIO allows a variety of custom connections and expands the I/O capabilities of the system to the real world.

The general-purpose interface can physically connect the device to a keyboard matrix and peripheral integrated circuits (ICs).

Figure 12-36 shows a typical application using the general-purpose interface.

12.2.1.2.1 GPIO Interface Signals

Figure 12-36 shows all of the GPIO interface signals.

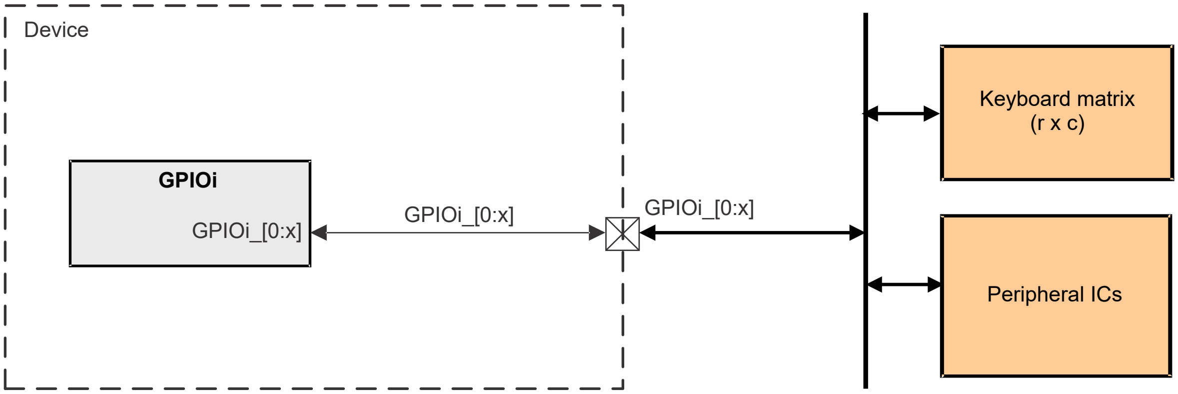

Note

i represents a GPIO instance. See the device datasheet for available domains and GPIO instances.

Note

See Module Integration section for signal specifics in GPIO.

Figure 12-36. GPIO Interface Signals and Typical Application

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.1.4 GPIO Functional Description

12.2.1.4.1 GPIO Block Diagram

Figure 12-37 shows the general-purpose interface block diagram.

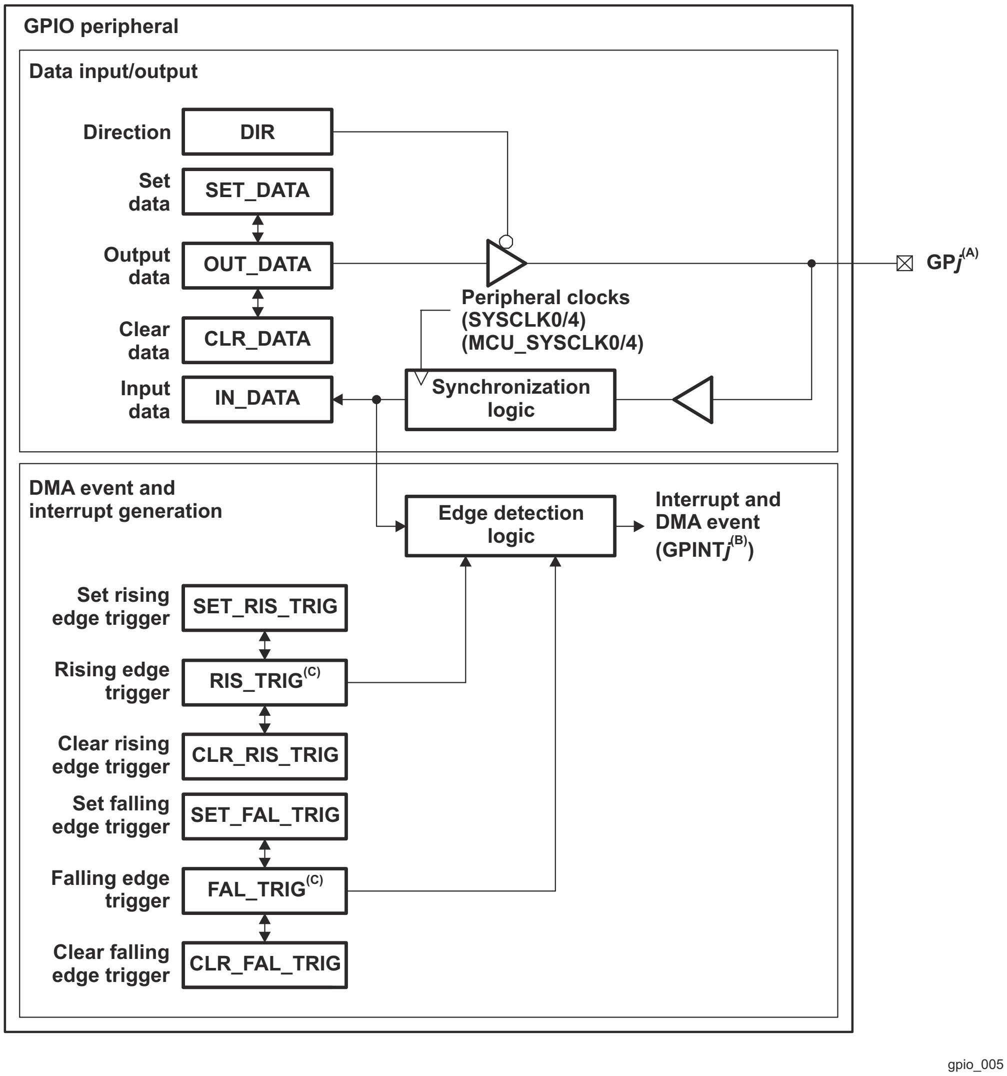

Note

Some of the GPj pins are muxed with other device signals. For details, see the device-specific Datasheet.

Note

All GPINTj can be used as host CPU interrupts and synchronization events to the DMA.

Note

The RIS_TRIG and FAL_TRIG registers are internal to the GPIO module and are not visible to the host CPU.

Figure 12-37. GPIO Block Diagram

12.2.1.4.2 GPIO Function

Each GPIO pin (GPj) can be independently configured as either an input or an output using the GPIO direction registers. The GPIO direction register (DIR) specifies the direction of each GPIO signal. Logic 0 indicates the GPIO pin is configured as output, and logic 1 indicates input.

When configured as output, writing a 0x1 to a bit in the set data register drives the corresponding GPj to a logic-high state. Writing a 0x1 to a bit in the clear data register drives the corresponding GPj to a logic-low state. The output state of each GPj can also be directly controlled by writing to the output data register.

For example, to set GP8 to a logic-high state, the software can perform one of the following:

- Write 100h to the GPIO0_SET_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.
- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x1, and write the new value back to GPIO_OUT_DATA01.

To set GP8 to a logic-low state, the software can perform one of the following:

- Write 100h to the GPIO_CLR_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.
- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x0, and write the new value back to GPIO_OUT_DATA01.

Note that writing a 0x0 to bits in the set data and clear data registers does not affect the GPIO pin state.

Also, for GPIO pins configured as input, writing to the set data, clear data, or output data registers does not affect the pin state.

For a GPIO pin configured as input, reading the input data register (IN_DATA) will return the pin state. Reading the SET_DATA register or the CLR_DATA data register will return the value in OUT_DATA, not the actual pin state. The pin state is available by reading the input data register. Note that when the direction is configured as input, the output state is determined by software's programming set/clear/output registers, and may not agree with the pin state, which is driven by an external device.

12.2.1.4.3 Interrupt and Event Generation

Each GPIO pin (GPj) can be configured to generate a host CPU interrupt (GPINTj) or a synchronization event to the DMA (GPINTj). Configuration is on per-bank basis. Each bit of the BINT_EN parameter dictates YES/NO option for each bank. Bit 0 controls bank 0, bit 1 controls bank 1, and so on.

The interrupt and DMA event can be generated on the rising-edge, falling-edge, or on both edges of the GPIO signal. The edge detection logic is synchronized to the GPIO peripheral clock.

The direction of the GPIO pin does not need to be input when using the pin to generate the interrupt or DMA event. When the GPIO pin is configured as input, transitions on the pin trigger interrupts or DMA events. When the GPIO pin is configured as output, software can toggle the GPIO output register to change the pin state and in turn trigger the interrupt or DMA event.

Note that the direction of the pin need not be input for interrupt generation to work. When the GPINT pin is configured as input, transitions on the pin trigger interrupts. When the GPINT pin is configured as output, firmware can toggle the GPIO output register to change the pin state, and in turn trigger interrupts.

Each interrupt output of GPINT signal are available at the module boundary. Each group of 16 GPINT signals also has their masked interrupt outputs ORed together to generate a per bank interrupt, available at the module boundary. The idea is to either connect individual interrupts or per bank interrupts to the system interrupt controller.

12.2.1.4.3.1 Interrupt Enable (per Bank)

The GPIO_BINTEN register provides interrupt enable/disable feature for each bank of 16 GPINT signals.

12.2.1.4.3.2 Trigger Configuration (per Bit)

Two internal registers, RIS_TRIG and FAL_TRIG, specify which edge of the GPj signal generates an interrupt or DMA event. Each bit in these two registers corresponds to a GPj pin. Table 12-35 describes the host CPU interrupt and DMA event generation of GPj pin based on the bit settings of the RIS_TRIG and FAL_TRIG registers.

Table 12-35. GPIO Interrupt and DMA Event Configuration Options

Clarifying configuration of GPIO interrupt generation RIS_TRIG Bit n	FAL_TRIG Bit n	Host CPU Interrupt and DMA Event Generation
0	0	GPINTj interrupt and DMA event is disabled
0	1	GPINTj interrupt and DMA event is triggered on falling edge of GPj signal
1	0	GPINTj interrupt and DMA event is triggered on rising edge of GPj signal
1	1	GPINTj interrupt and DMA event is triggered on both rising and falling edge of GPj signal

The RIS_TRIG and FAL_TRIG registers are not directly accessible or visible to the host CPU. These registers are accessed indirectly through four registers: SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, and CLR_FAL_TRIG. Writing 1 to a bit on the SET_RIS_TRIG register sets the corresponding bit on the RIS_TRIG register. Writing 1 to a bit of the CLR_RIS_TRIG register clears the corresponding bit on the RIS_TRIG register. Writing to the SET_FAL_TRIG and CLR_FAL_TRIG registers works the same way on the FAL_TRIG register.

Reading the SET_RIS_TRIG or CLR_RIS_TRIG register returns the value of the RIS_TRIG register. Reading from the SET_FAL_TRIG and CLR_FAL_TRIG register returns the value of the FAL_TRIG register.

To use the GPIO pins as sources for host CPU interrupts and DMA events, the associated bank interrupt enable register bit in GPIO_BINTEN must also be set to 1. For example, to enable GPIO0_19 (which is in bank 1), GPIO_BINTEN[1] = 1 should be set to enable interrupts for bank 1.

12.2.1.4.3.3 Interrupt Status and Clear (per Bit)

The INTSTAT registers provide interrupt status upon reading, and interrupt clear feature upon writing 1 to the corresponding bit position(s). Upon receiving an interrupt, the ISR can examine the interrupt status and clear the processed interrupts.

Note

The GPIO module generates an interrupt pulse on the individual GPINT interrupt in response to each occurrence of the specified edge condition. Therefore, for GPINT signals having their interrupts routed directly to the interrupt controller, it is not necessary to clear the status bits in this module. The interrupt status and clear register is a facility for the per-bank interrupt connection.

12.2.1.4.4 GPIO Interrupt Connectivity

Because this device muxes GPIO signals with other functional signals, the availability of any particular GPIO and hence the usability of its associated interrupt will change based on the use case pin muxing. The large number of possible GPIO interrupt sources makes it impractical to route all interrupt events to each processing element. Since most applications do not typically require a large number of GPIO interrupts, the interrupt uncertainty is resolved by mapping all GPIO interrupts to a series of event muxes implemented using Interrupt Router (IntRouter) modules. These muxes allow any one of the available GPIO interrupts to be selected and passed on as an event to the various processor interrupt controllers and DMA controllers. Event selection is controlled through associated registers within each IntRouter.

The GPIO bank interrupts already represent a consolidation of the 16 GPIO interrupts associated with each bank and are routed directly to various interrupt controllers rather than through the GPIO IntRouters.

One of the GPIO pins has a potential use case as an Arm reset input and should therefore be routed as highest priority interrupt in the GIC and mapped to nFIQ in software.

Figure 12-38 shows the GPIO Interrupt Routers connectivity. Refer to *Interrupt Routers*, for more details on the GPIO Interrupt Routers connectivity.

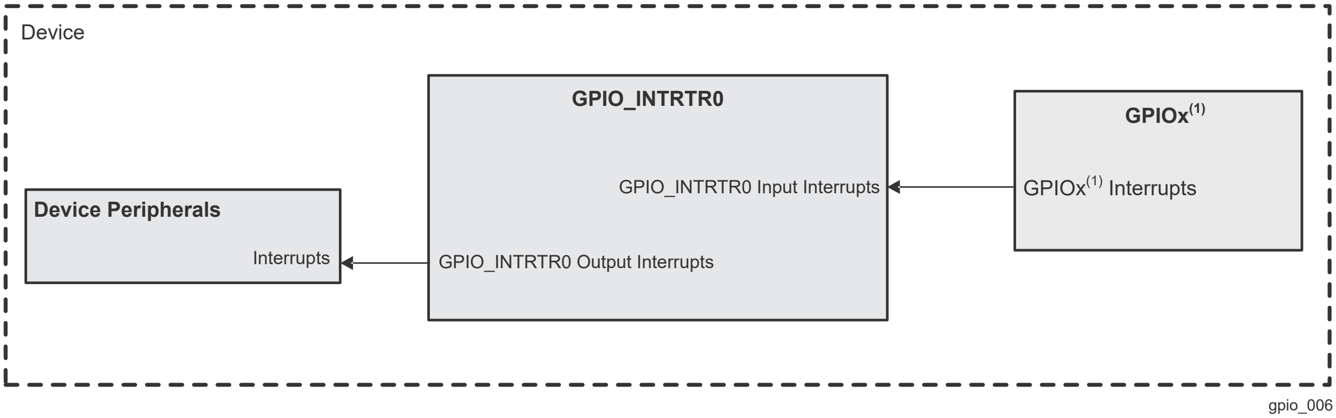

Note

(1): x represents a valid instance of GPIO in a domain.

Figure 12-38. GPIO Interrupt Router Connectivity

12.2.1.4.5 Emulation Halt Operation

The GPIO peripheral is not affected by emulation halts.

12.2.1.5 GPIO Programming Guide

12.2.1.5.1 GPIO Low-Level Programming Models

12.2.1.5.1.1 Global Initialization

12.2.1.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the general-purpose interface module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the general-purpose interface. For more information, see *GPIO Environment* and *Module Integration*.

Table 12-36. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC0	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*.
MCU_PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*.
GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
MCU_GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
Interconnects	For information about the MCU_CBASS0, and CBASS0 interconnects configuration, see *System Interconnect*.

12.2.1.5.1.1.2 GPIO Module Global Initialization

This procedure initializes the general-purpose Interface module after a power-on reset (POR) or software reset.

Table 12-37. GPIO Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure GPIO channels as input or output of the corresponding bank	DIR	-h
Interrupt requests configuration		
Configure detection events	SET_RIS_TRIG and/or SET_FAL_TRIG	-h
Clear interrupt status	INTSTAT	FFFFh
Enable interrupts for desired banks [0:8]	GPIO_BINTEN[8-0]	-h

12.2.1.5.1.2 GPIO Operational Modes Configuration

12.2.1.5.1.2.1 GPIO Read Input Register

Table 12-38. GPIO Read Input Register

Step	Register/Bit Field/Programming Model	Value
Read interrupt status of the corresponding bank	INTSTAT	-h
Read input register value	IN_DATA	-h
Clear interrupt status	INTSTAT	FFFF FFFFh

12.2.1.5.1.2.2 GPIO Set Bit Function

Table 12-39. GPIO Set Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to set desired bit(s) in SET_DATA register.	SET_DATA	-h

12.2.1.5.1.2.3 GPIO Clear Bit Function

Table 12-40. GPIO Clear Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to clear desired bit(s) in CLR_DATA register.	CLR_DATA	-h

12.2.2 Inter-Integrated Circuit (I2C) Interface

This section describes the Inter-Integrated Circuit (I2C) module in the device.

12.2.2.1 I2C Overview

The device contains multicontroller Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I^{2}C-bus-compatible device that connects via the I^{2}C serial bus. External components attached to the I^{2}C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^{2}C interface.

Each multicontroller I^{2}C module can be configured to act like a target or controller I^{2}C-compatible device.

I^{2}C instances may be implemented with dedicated, I^{2}C compliant, open-drain I/O buffers, or with standard LVCMOS I/O buffers. The I^{2}C instances associated with open-drain I/O buffers can support Hs-mode (up to 3.4 Mbps when the I/O buffers are operating at 1.8 V but limited to 400 kbps when the I/O buffers are operating at 3.3 V).

The I^{2}C instances associated with standard LVCMOS I/O buffers can support Fast-mode (up to 400 kbps). The LVCMOS I/O buffers being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.

Refer to the device specific datasheet for details on which instances support which buffer type.

For the specific I/O timing characteristics of the different I^{2}C instances, see the device-specific Datasheet.

I2C Modules Overview shows the I2C modules overview.

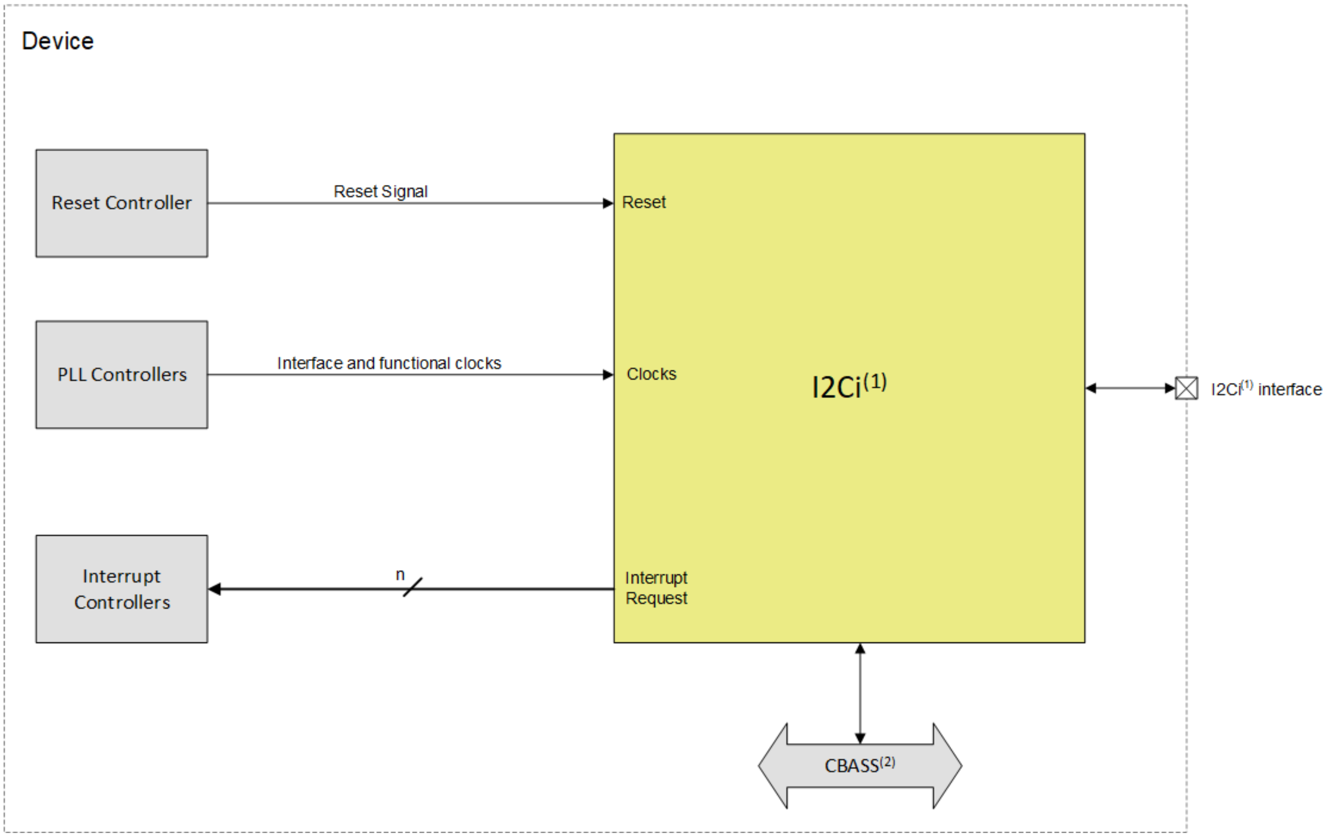

Figure 12-39. I2C Module Overview

Note

(1): i = 0 to (number of instances - 1) in the Domain

Note

(2): If MCU Domain is applicable, MCU_I2C instances are connected to MCU_CBASS

12.2.2.1.1 I2C Features

Each multicontroller I2C module has the following features:

- Compliant with Philips I^2C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Supports HS mode (up to 3.4 Mbps) only for instances with true open drain buffer and in 1.8 V mode
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multicontroller transmitter/target receiver mode
- Multicontroller receiver/target transmitter mode
- Combined controller transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read
- Module enable/disable capability
- Programmable multitarget channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

12.2.2.1.2 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.2.1.3 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.2.2.2 I2C Environment

This section describes the I2C external connections (environment).

12.2.2.2.1 I2C Typical Application

Figure 12-40 shows the multicontroller I2C and their related connections with I^{2}C-compliant devices.

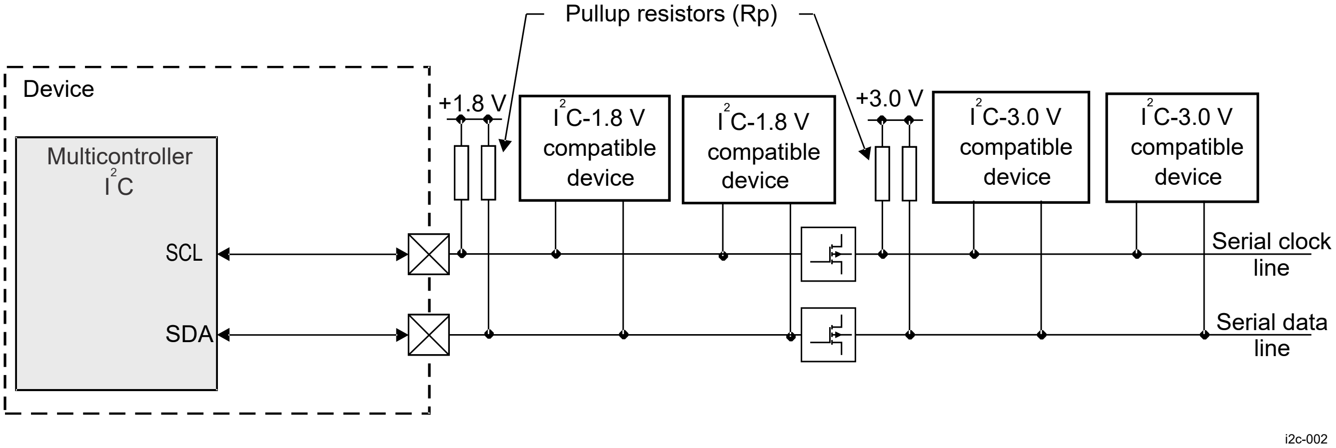

Figure 12-40. I2C and Typical Connections to I2C Devices

12.2.2.2.1.1 I2C Pins for Typical Connections in I2C Mode

Figure 12-41 shows the multicontroller I2C pins used for typical connections with I^{2}C devices.

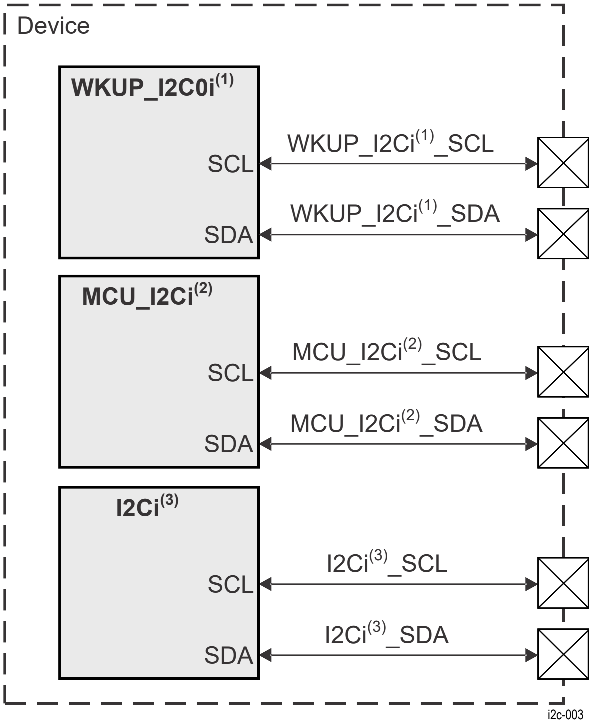

1. i = 0 to (number of devices - 1) in WKUP Domain, if applicable
2. i = 0 to (number of devices - 1) in MCU Domain, if applicable
3. i = 0 to (number of devices - 1) in MAIN Domain, if applicable

Figure 12-41. I2C Interface Signals

12.2.2.2.1.2 I2C Interface Typical Connections

Table 12-41 describes the I2C I/O signals.

Table 12-41. I2C I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value
			WKUP_I2Ci(2)	
SCL	WKUP_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	WKUP_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			MCU_I2Ci(2)	
SCL	MCU_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	MCU_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			I2Ci(2)	
SCL	I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	I2Ci(2)_SDA	I/O	I^2C serial data line.	1

(1) I = Input; O = Output; I/O = Bidirectional

(2) i represents an I2C instance. See the device datasheet for available domains and I2C instances.

12.2.2.2.1.3

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.2.2.2 I2C Typical Connection Protocol and Data Format

12.2.2.2.2.1 I2C Serial Data Format

The I2C controller operates in 8-bit word data format (byte write access supported for the last access). Each byte transmitted or received on the serial data line is 8 bits long. The number of bytes that can be transmitted or received is not restricted. The data is transferred with the most-significant bit (MSB) first. In receiver mode, each byte is followed by an acknowledge bit from the I2C module.

Figure 12-42 shows a typical I^2C communication format.

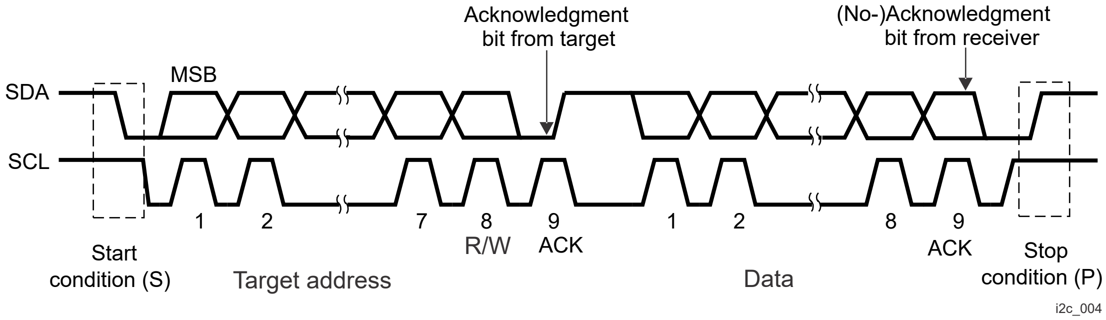

Figure 12-42. I2C Data Transfer

12.2.2.2.2.2 I2C Data Validity

The data on the serial data line (SDA) must be stable during the high period of the serial clock line. The high and low states of the data line can change only when the clock signal on the serial clock line (SCL) is low.

Figure 12-43 is an example of data validity requirements.

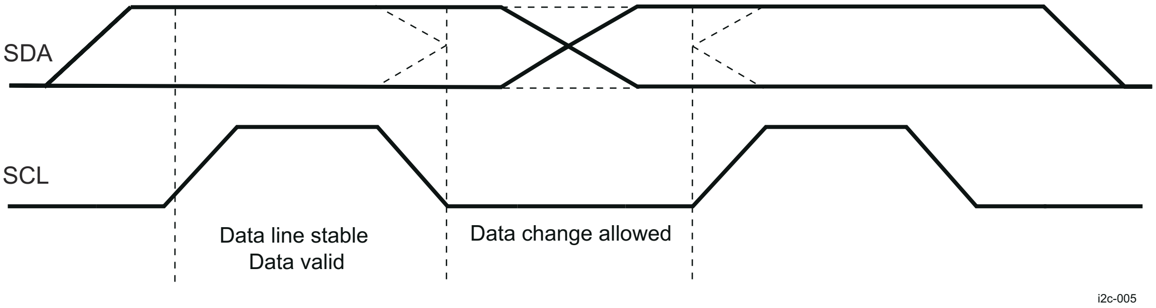

Figure 12-43. I2C Bit Transfer on the I2C Bus

12.2.2.2.2.3 I2C Start and Stop Conditions

The I2C module generates start (S) and stop (P) conditions when it is configured as a controller.

- An S condition is a high-to-low transition on the serial data line while serial clock line is high.
- A P condition is a low-to-high transition on the serial data line while serial clock line is high.

The bus is considered busy after the S condition (the I2C_IRQSTATUS_RAW [12] BB bit is 1 to indicate that the bus is busy) and free after the P condition (the I2C_IRQSTATUS_RAW [12] BB bit is 0 to indicate that the bus is free).

Figure 12-44 shows the waveforms that occur during an S and a P condition.

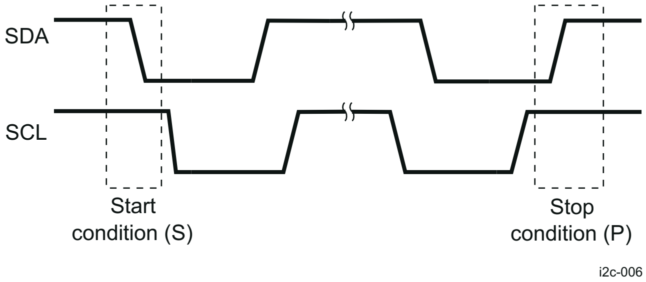

Figure 12-44. I2C S and P Condition Events

Note

I2C controller does not support messages non-compliant with I^{2}C standard. Void messages are non-standard I^{2}C messages and will lockup the controller. A void message is a START condition followed by a STOP condition, in other words, while the bus is free the SDA line is pulled low (START) and then released (STOP). This would result in a timeout (software) of the next controller transfer which would never complete. A soft reset of the controller is recommended for recovery.

12.2.2.2.2.4 I2C Addressing

The I2C module supports two data formats in fast/standard (F/S) and HS modes:

- 7-bit/10-bit addressing format
- 7-bit/10-bit addressing format with repeated start (Sr) condition

12.2.2.2.2.4.1 Data Transfer Formats in F/S Mode

Figure 12-45 shows the I2C data transfer formats in F/S mode.

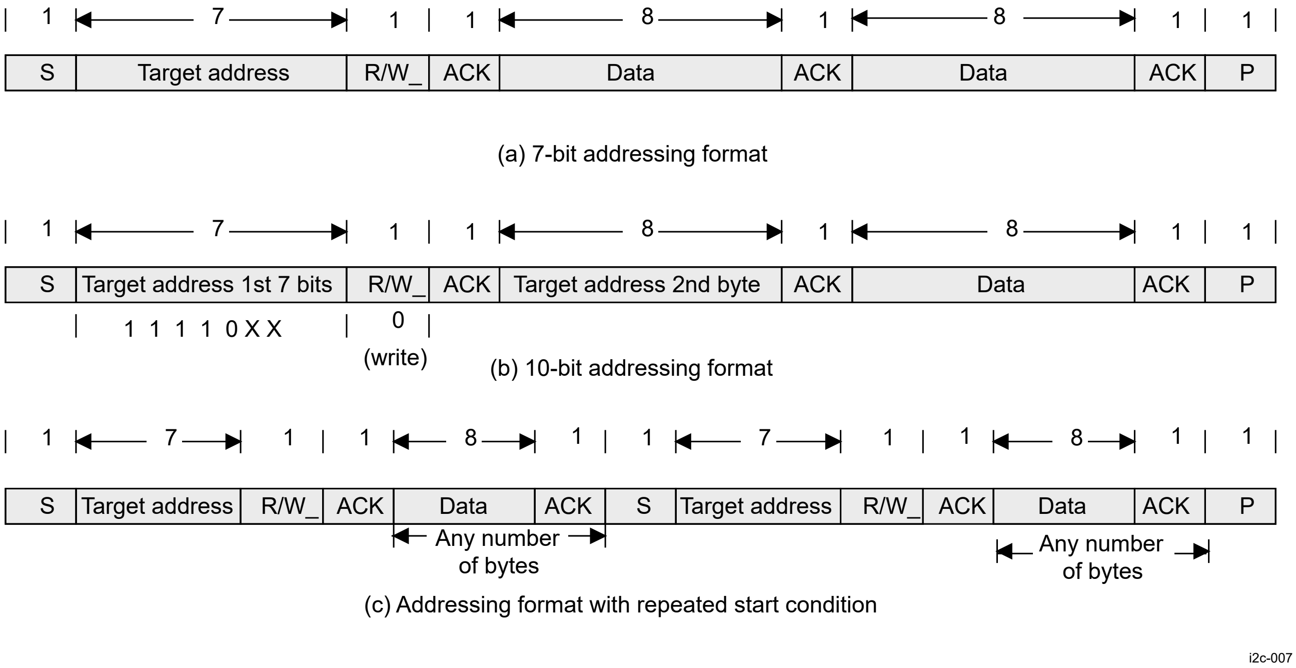

Figure 12-45. I2C Data Transfer Formats in F/S Mode

The first word after an S condition consists of 8 bits. In acknowledge mode, an extra dedicated acknowledgment bit is inserted after each byte.

In addressing formats with 7-bit addresses, the first byte is composed of 7 MSB target address bits and 1 least-significant bit (LSB) R/W_ bit.

The LSB R/W_ bit of the address byte indicates the transmission direction of the data bytes that follow it. If R/W_ is 0, the controller writes data to the selected target; if it is 1, the controller reads data from the target.

In addressing formats with 10-bit addresses, the structure of the first byte is 11110XXY, where XX is the two MSBs of the 10-bit addresses, and Y is the R/W_ bit. If the R/W_ bit is 0, the next byte contains the last 8 bits of the target address. If the R/W_ bit is 1, the next byte contains data transmitted from the target to the controller.

12.2.2.2.2.4.2 Data Transfer Format in HS Mode

Figure 12-46 shows the I2C data transfer format in HS mode.

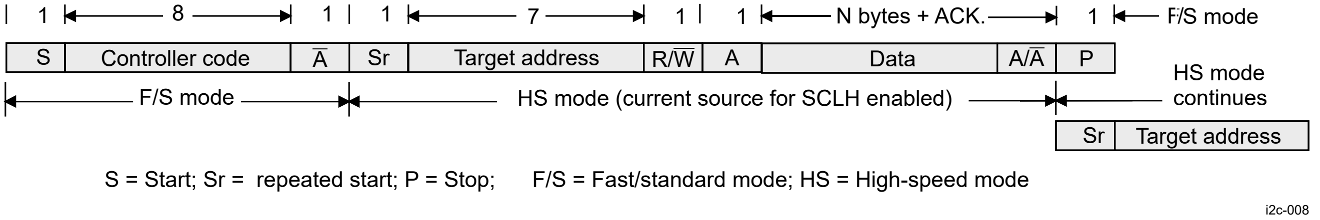

Figure 12-46. HS I2C Data Transfer in HS Mode

Each multicontroller I2C can also operate in HS mode. In this case, after the S condition, the module, which is in F/S mode, writes the controller code address (0x00001XXX, where XXX is the variable portion of the controller code) on the bus. No device connected on the same bus acknowledges this address. The module switches the clock to the HS clock and after an Sr condition, and sends the target address and the data, as shown in Figure 12-46.

12.2.2.2.2.5 I2C Controller Transmitter

In controller transmitter mode, data assembled in one of the previously described data formats is shifted out on the serial data line SDA in sync with the self-generated clock pulses on the serial clock line SCL. The clock pulses are inhibited and SCL is held low when the intervention of the processor is required (XUDF) after a byte is transmitted.

12.2.2.2.2.6 I2C Controller Receiver

Controller receiver mode can be entered only from controller transmitter mode. With any of the address formats (a), (b), or (c) (see Figure 12-45), if R/W_ is high, the module enters controller receiver mode after the target address byte and bit R/W_ are transmitted. Serial data bits received on bus line SDA are shifted in synchronization with the self-generated clock pulses on SCL.

12.2.2.2.2.7 I2C Target Transmitter

Target transmitter mode can be entered only from target receiver mode. With any of the address formats (a), (b), or (c) (see Figure 12-45), the target transmitter is entered if the target address byte is the same as its own address and bit R/W_ is transmitted, if R/W_ is high. The target transmitter shifts the serial data out on the data line SDA in sync with the clock pulses that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (XUDF).

12.2.2.2.2.8 I2C Target Receiver

In this mode, serial data bits received on the bus line SDA are shifted-in in sync with the clock pulses on SCL that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (ROVR) after a byte is received.

12.2.2.2.2.9 I2C Bus Arbitration

If two or more controller transmitters start a transmission on the same bus almost simultaneously, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial bus by the competing transmitters. When a transmitter senses that a high signal it has presented on the bus has been overruled by a low signal, it switches to the target receiver mode, sets the arbitration lost (I2C_IRQSTATUS_RAW[0] AL) flag, and generates the arbitration lost interrupt. I2C Arbitration Between Controller Transmitters shows the arbitration procedure between two devices. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. If two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

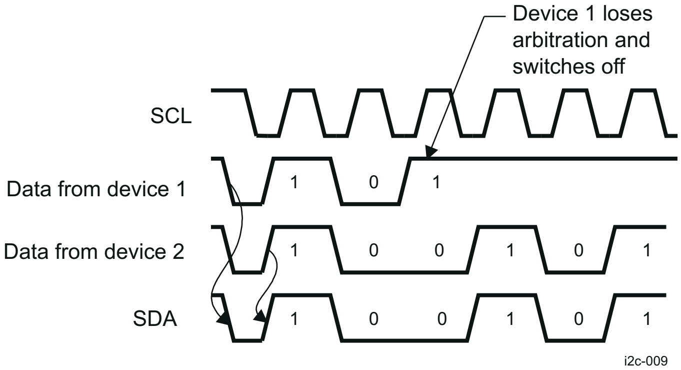

Figure 12-47. I2C Arbitration Between Controller Transmitters

12.2.2.2.2.10 I2C Clock Generation and Synchronization

Under normal conditions, only one controller device generates the clock signal - SCL. However, there are two or more controller devices during the arbitration procedure, and the clock must be synchronized so that the data output can be compared. The wired-AND property of the clock line means that a device that first generates a low period of the clock line overrules the other devices. At this high/low transition, the clock generators of the other devices are forced to start generation of their own low period. The clock line is then held low by the device with the longest low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their high periods. A synchronized signal on the clock line is thus obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period. If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the WAIT-state. In this way a target can slow down a fast controller and the slow device can create enough time to store a received byte or prepare a byte to be transmitted (clock stretching).

Note

In case the SCL or SDA lines are stuck low, a bus clearing operation is supported:

- If the clock line (SCL) is stuck low, the preferential procedure is to reset the bus using the hardware reset signal if the I^2C devices have hardware reset inputs. If the I^2C devices do not have hardware reset inputs, cycle power to the devices to activate the mandatory internal power-on reset (POR) circuit.
- If the data line (SDA) is stuck low, the controller should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks. If not, then use the hardware reset or cycle power to clear the bus.

Figure 12-48 shows clock synchronization.

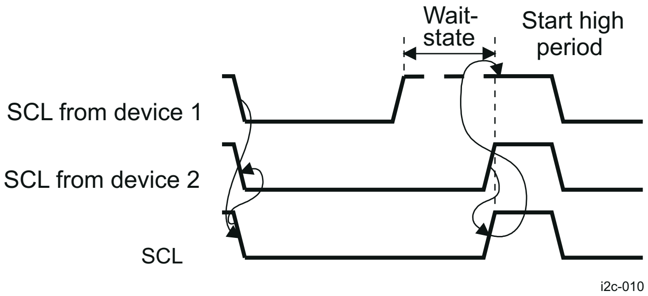

Figure 12-48. I2C Clock Generators Synchronization

12.2.2.3 I2C Functional Description

12.2.2.3.1 I2C Block Diagram

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

Figure 12-49 presents the multicontroller I2C block diagram.

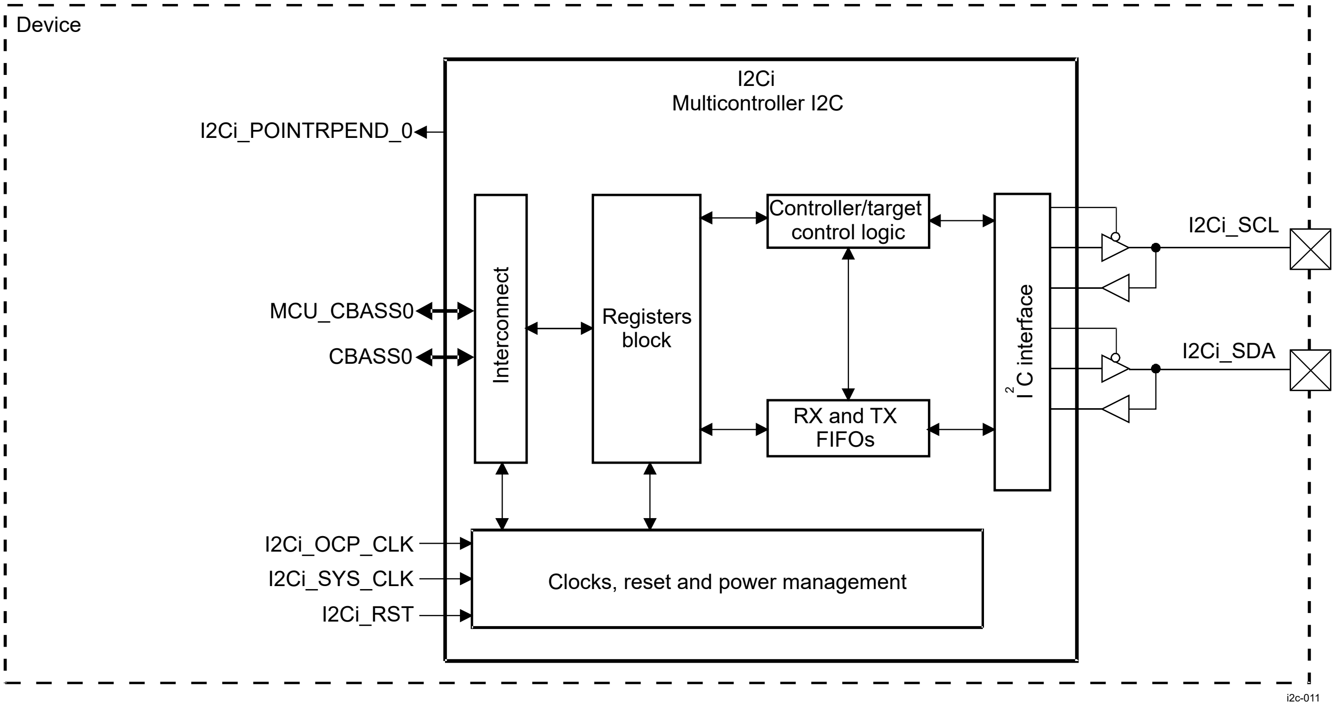

Note

i = 0 to number of devices in MCU domain -1, if applicable.

Note

i = 0 to number of devices in MAIN domain -1, if applicable.

Figure 12-49. I2C Block Diagram

The ten multicontroller I2C can be configured in F/S I^2C mode or HS I^2C mode. The operation mode is selected by configuring the I2C_CON[13-12] OPMODE bit field.

Table 12-42 lists the available operation modes.

Table 12-42. I^2C Operation Mode Selection

Operation Mode	Value of I2C_CON[13-12] OPMODE
F/S I^2C	0x0
HS I^2C	0x1
SCCB	0x2
Reserved (not used)	0x3

12.2.2.3.2 I2C Clocks

12.2.2.3.2.1 I2C Clocking

Each multicontroller I2C uses the SYS_CLK functional clock in the Device Configuration section. The internal sampling clock INTERNAL_CLK is generated by dividing the functional clock by the I2C_PSC[7-0] PSC bit field value + 1 in F/S mode, or in the first phase of HS mode; or by directly using the functional clock in the second phase of HS mode (prescaler is bypassed).

The low time of the SCLL signal is determined by the I2C_SCLL[7-0] SCLL bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLL[15-8] HSSCLL bit field in the second phase of HS mode.

The high time of the SCLH signal is determined by the I2C_SCLH[7-0] SCLH bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLH[15-8] HSSCLH bit field in the second phase of HS mode.

Table 12-43 lists the t_{LOW} and t_{high} values in controller mode only (in target mode, the I2C controller does not generate the I^2C clock).

Table 12-43. I^2C t_{LOW} and t_{high} Values of the I^2C Clock

Mode	Clock	t_{LOW}	t_{high}
F/S or HS first phase	INTERNAL_CLK = SYS_CLK / (I2C_PSC[7-0] PSC bit field + 1)	(I2C_SCLL[7-0] SCLL bit field value + 7) × INTERNAL_CLK period	(I2C_SCLH[7-0] SCLH bit field value + 5) × I2Ci_INTERNAL_CLK period
HS second phase	SYS_CLK	(I2C_SCLL[15-8] HSSCLL bit field value + 7) × SYS_CLK period	(I2C_SCLL[15-8] HSSCLH bit field value + 5) × I2Ci_SYS_CLK period

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Note

i = 0 to number of devices in MCU domain -1, if applicable.

Note

i = 0 to number of devices in MAIN domain -1, if applicable.

Note

For HS mode, the I2C_SCLL[15-8] HSSCLL and I2C_SCLL[7-0] SCLL bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

For HS mode, the I2C_SCLH[15-8] HSSCLH and I2C_SCLH[7-0] SCLH bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

Note

The equations in Table 12-43 give the SCLL timing values for SCLL/SCLH/HSSCLL/HSSCLH at I2C controller outputs. Actual t_{low} and thigh periods may vary depending on the board (the load capacitance on the SCLL signal). If necessary, any adjustments to the SCLL/SCLH/HSSCLL/HSSCLH values must be determined by measurements of actual SCL signal on the board.

CAUTION

During active mode (the I2C_CON[15] I2C_EN bit is set to 1), make no changes to the I2C_SCLL and I2C_SCLH registers. Changes may result in unpredictable behavior.

Table 12-44 lists the register values for obtaining the maximum I^{2}C bit rates and the maximum period of the filtered spikes in F/S mode and HS mode.

Table 12-44. I2C Register Values for Maximum I2C Bit Rates in I2C F/S, I2C HS Modes(1)

	I^{2}C Mode for			Description
	Standard Mode	**Fast Mode**	**High-Speed Mode(2)**	
SYS_CLK frequency (MHz)	96			
OCP_CLK frequency (MHz)	133			
I2C_PSC[7-0] PSC	**23**	**9**	**1**	Prescaler value for F/S and HS modes
INTERNAL_CLK frequency (MHz)	4	9.6	96	
I2C_SCLL[7-0] SCLL	**13**	**7**	**115**	Value for F/S mode and first phase of HS mode
I2C_SCLH[7-0] SCLH	**15**	**5**	**113**	Value for F/S mode and first phase of HS mode
Maximum bit rate (Mbps)	0.1	0.4	0.4	F/S mode and first phase in HS mode maximum bit rate
Maximum filter period (ns)	250	104.2	10	
I2C_SCLL[15-8] HSSCLL			**12**	Values for second phase of HS mode
I2C_SCLH[15-8] HSSCLH			**5**	Values for second phase of HS mode
HS mode maximum bit rate (Mbps)			3.31	HS mode maximum bit rate
Maximum filter period (ns)			10	

(1) Programmable fields are in bold.

(2) HS mode is not supported on this family of devices.

Note

This table presents informative values only for the configuration parameters and the I^{2}C bus performance obtained according to these values. The delays added by the analog pads are not considered in these figures.

Note

For MCU_I2C[0-1]

For I2C[0-3]

I2Ci_INTERNAL_CLK freq = I2Ci_SYS_CLK / (PSC +1)

F/S filter period = 1 / I2Ci_INTERNAL_CLK

HS filter period = 1 / I2Ci_SYS_CLK freq

HS bit rate = I2Ci_SYS_CLK freq / (HSSCLL+ 7 + HSSCLH + 5)

FS bit rate = I2Ci_INTERNAL_CLK / (SCLL+ 7 + SCLH + 5)

12.2.2.3.2.2 I2C Automatic Blocking of the I2C Clock Feature

This feature offers the possibility for the LH to command the blocking of the I^{2}C clock after the target addressing phase, when the I2C controller is addressed by an external controller device using a certain Own Address.

The release of the I^2C clock can be performed independently for each Own Address (I2C_OA, and I2C_OAx registers, where x = 1, 2, 3) by deasserting the corresponding bit in the I2C_SBLOCK register.

12.2.2.3.3 I2C Software Reset

Each multicontroller I2C supports the software reset by accessing the I2C_SYSC[1] SRST bit (1: reset; 0: normal mode).

The software reset status can be checked by accessing the I2C_SYSS[0] RDONE bit (1: reset is done; 0: reset is ongoing).

To do a software reset, the following steps must be done:
1. Ensure that the module is disabled (clear the I2C_CON[15] I2C_EN bit to 0).
2. Set the I2C_SYSC[1] SRST bit to 1.
3. Enable the module by setting I2C_CON[15] I2C_EN bit to 1.
4. Check the I2C_SYSS[0] RDONE bit until it is set to 1 to indicate the software reset is complete.

Note

The I2C_CON[15] I2C_EN bit can hold the functional clock domain of the multicontroller I2C in reset after the device reset has been released. When the system bus reset is removed, this bit remains cleared. The functional part of the I2C controller is held in reset state while this bit is 0, and all configuration registers can be accessed.

The I2C_CON[15] I2C_EN bit must be set to 1 to enable the functional part of the I2C controller.

The I2C_SYSS[0] RDONE bit is asserted only after the module is enabled by setting the I2C_CON[15] I2C_EN bit to 1.

12.2.2.3.4 I2C Power Management

Table 12-45 describes power-management features available for the multicontroller I2C.

Note

For information about source clock gating, see *Power* in the *Device Configuration*.

Note

Some of the I2C features described in this section may not be supported on this family of devices. See the *Module Integration* section for more information about unsupported features..

Table 12-45. I2C Local Power-Management Features

Feature	Registers	Description
Clock auto gating	I2C_SYSC[0] AUTOIDLE	This bit allows a local power optimization inside the module.
Target idle modes	I2C_SYSC[4-3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	I2C_SYSC[9-8] CLOCKACTIVITY	For configuration details, see Table 12-46.
Global wake-up enable	I2C_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.

Table 12-46. I2C Clock Activity Settings

I2C_SYSC[9-8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	OCP_CLK	SYS_CLK	
00	OFF	OFF	Both clocks are disabled.
10	OFF	ON	Interface clock is disabled; Functional clock is enabled
01	ON	OFF	Functional clock is disabled; Interface clock is enabled

Table 12-46. I2C Clock Activity Settings (continued)

I2C_SYSC[9-8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	OCP_CLK	SYS_CLK	
11	ON	ON	Both clocks are enabled.

12.2.2.3.5 I2C Interrupt Requests

The I2C controller must allocate a minimum of five registers for interrupts.

- Interrupt Raw Status (I2C_IRQSTATUS_RAW)
- Interrupt Enabled Status (I2C_IRQSTATUS)
- Interrupt Enable Set (I2C_IRQENABLE_SET)
- Interrupt enable Clear (I2C_IRQENABLE_CLR)
- End of interrupt (I2C_EOI)

End of Interrupt (I2C_EOI) is used by software to trigger an interrupt service completion.

Table 12-47 lists the event flags, and their mask, that can cause module interrupts.

Table 12-47. I2C Events

Event Flag	Event Unmask	Event Mask	Description
I2C_IRQSTATUS[0] AL	I2C_IRQENABLE_SET[0] AL_IE	I2C_IRQENABLE_CLR[0] AL_IE	Arbitration lost. This bit is automatically set by the hardware when it loses the arbitration in controller transmit mode, an interrupt is signaled to the host.
I2C_IRQSTATUS[1] NACK	I2C_IRQENABLE_SET[1] NACK_IE	I2C_IRQENABLE_CLR[1] NACK_IE	No acknowledgement. Bit is set when No Acknowledge is received, an interrupt is signaled to the host.
I2C_IRQSTATUS[2] ARDY	I2C_IRQENABLE_SET[2] ARDY_IE	I2C_IRQENABLE_CLR[2] ARDY_IE	Register access ready. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to the host.
I2C_IRQSTATUS[3] RRDY	I2C_IRQENABLE_SET[3] RRDY_IE	I2C_IRQENABLE_CLR[3] RRDY_IE	Receive data ready. Set to 1 by core when in receiver mode, a new data can be read. An interrupt is signaled to the host.
I2C_IRQSTATUS[4] XRDY	I2C_IRQENABLE_SET[4] XRDY_IE	I2C_IRQENABLE_CLR[4] XRDY_IE	Transmit data ready. Set to 1 by core when transmitter is ready for new data. An interrupt is signaled to the host.
I2C_IRQSTATUS[5] GC	I2C_IRQENABLE_SET[5] GC_IE	I2C_IRQENABLE_CLR[5] GC_IE	General call. Set to 1 by core when General Call address was detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[6] STC	I2C_IRQENABLE_SET[6] STC_IE	I2C_IRQENABLE_CLR[6] STC_IE	Start condition detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[7] AERR	I2C_IRQENABLE_SET[7] AERR_IE	I2C_IRQENABLE_CLR[7] AERR_IE	Bus Access Error. An interrupt is signaled to the host.
I2C_IRQSTATUS[8] BF	I2C_IRQENABLE_SET[8] BF_IE	I2C_IRQENABLE_CLR[8] BF_IE	Bus free. An interrupt is signaled to the host.
I2C_IRQSTATUS[9] AAS	I2C_IRQENABLE_SET[9] AAS_IE	I2C_IRQENABLE_CLR[9] AAS_IE	Address recognized as target. An interrupt is signaled to the host.
I2C_IRQSTATUS[10] XUDF	I2C_IRQENABLE_SET[10] XUDF_IE	I2C_IRQENABLE_CLR[10] XUDF_IE	Transmit underflow. An interrupt is signaled to the host.
I2C_IRQSTATUS[11] ROVR	I2C_IRQENABLE_SET[11] ROVR_IE	I2C_IRQENABLE_CLR[11] ROVR_IE	Receive overrun. An interrupt is signaled to the host.
I2C_IRQSTATUS[12] BB	N/A	N/A	Bus busy indicator
I2C_IRQSTATUS[13] RDR	I2C_IRQENABLE_SET[13] RDR_IE	I2C_IRQENABLE_CLR[13] RDR_IE	Receive draining. An interrupt is signaled to the host.

Table 12-47. I2C Events (continued)

Event Flag	Event Unmask	Event Mask	Description
I2C_IRQSTATUS[14] XDR	I2C_IRQENABLE_SET[14] XDR_IE	I2C_IRQENABLE_CLR[14] XDR_IE	Transmit draining. An interrupt is signaled to the host.

12.2.2.3.6 I2C Programmable Multitarget Channel Feature

This feature allows each multicontroller I2C to be addressed using four separate Own Addresses configured in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3). An additional register (I2C_ACTOA) is used to indicate to the LH which address is used by the external controller to communicate with the I2C controller.

Each Own Address can be independently configured in 7-bit or 10-bit mode by setting the corresponding bit (I2C_CON[7] XOA0, I2C_CON[6] XOA1, I2C_CON[5] XOA2, or I2C_CON[4] XOA3).

12.2.2.3.7 I2C FIFO Management

The depth of the RX and TX FIFOs can be checked by reading the I2C_BUFSTAT[15-14] FIFODEPTH bit field (0x0: 8 bytes, 0x1: 16 bytes, 0x2: 32 bytes, and 0x3: 64 bytes).

12.2.2.3.7.1 I2C FIFO Interrupt Mode

In FIFO interrupt mode (relevant interrupts enabled by the I2C_IRQENABLE_SET register), an interrupt signal informs the processor of the receiver and transmitter status. These interrupts are raised when the RX/TX FIFO thresholds (defined by the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX FIFO or the I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX FIFO) are reached; the interrupt signals instruct the LH to transfer data to the destination (from the I2C controller in receive mode and/or from any source to the I2C controller FIFO in transmit mode).

Figure 12-50 and Figure 12-51 show receive and transmit operations, respectively, from a FIFO management point of view.

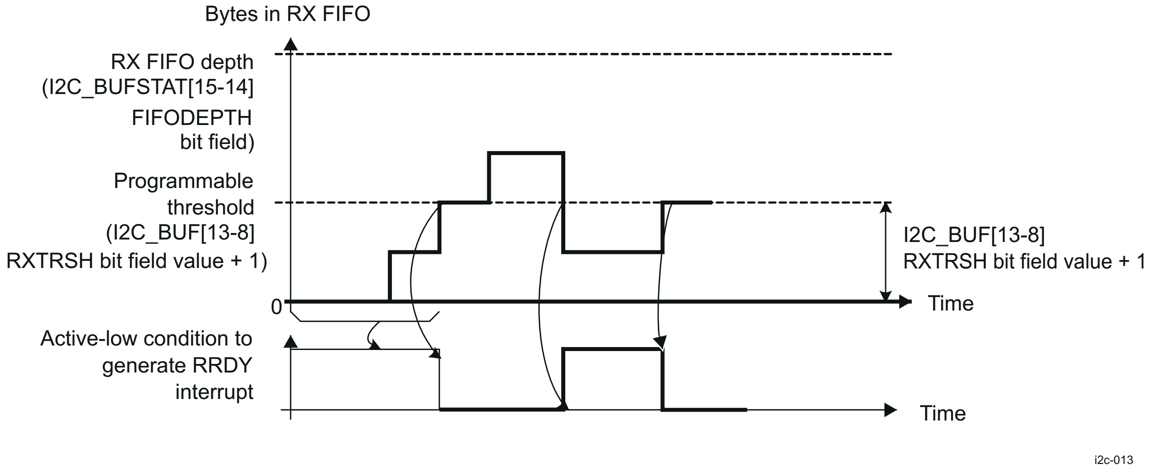

Figure 12-50. I2C Receive FIFO Interrupt Request Generation

In Figure 12-50 , the RRDY interrupt condition shows that the condition for generating an RRDY interrupt is achieved. The interrupt request is generated when this signal is active, and it can be cleared only by the LH by writing 1 in the corresponding bit. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In receive mode, an RRDY interrupt is generated as soon as the FIFO reaches its receive threshold (I2C_BUF[13-8] RXTRSH bit field value + 1). The interrupt can be deasserted only when the LH has handled enough bytes to make the number of bytes in the RX FIFO lower than the programmed threshold. For each interrupt, the LH can be configured to read a number of bytes equal to the value of the RX FIFO threshold.

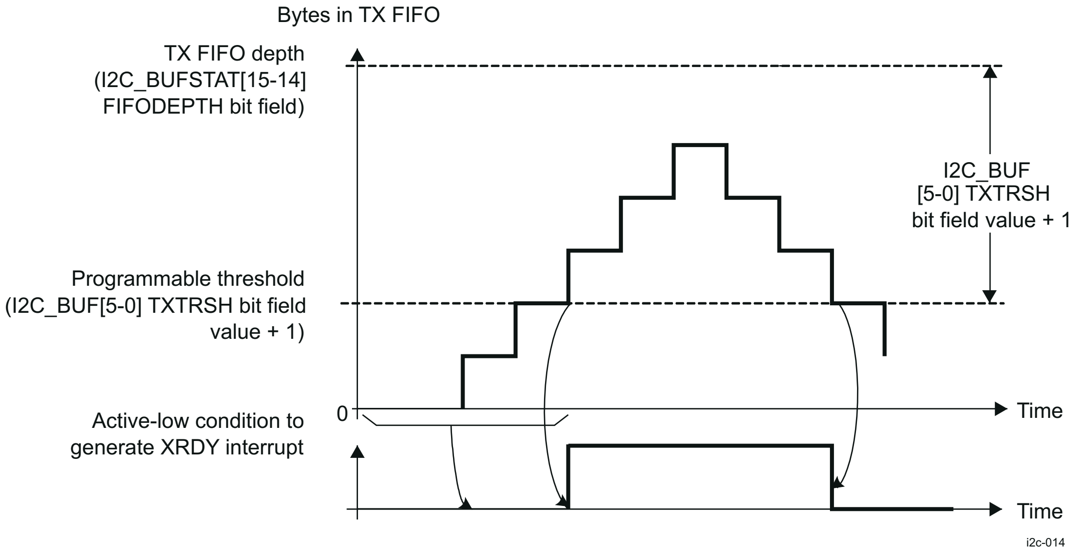

Figure 12-51. I2C Transmit FIFO Interrupt Request Generation

In Figure 12-51 , the XRDY interrupt condition shows that the condition for generating an XRDY interrupt is achieved. The interrupt request is generated when TX FIFO is empty or when the TX FIFO threshold is not reached, and the LH can clear the XRDY status bit by setting the I2C_IRQENABLE_CLR[4] XRDY_IE bit to 1 after transmitting the configured number of bytes. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In interrupt mode, the module offers two options for the LH application to handle the interrupts:

- When detecting an interrupt request (XRDY or RRDY type), the LH can write/read 1 data byte to/from the TX/RX FIFO and then clear the interrupt. The module reasserts the interrupt until the interrupt condition is not met.
- When detecting an interrupt request (XRDY or RRDY type), the LH can be programmed to write/read the amount of data bytes specified by the corresponding FIFO threshold (I2C_BUF[5-0] TXTRSH + 1 or I2C_BUF[5-0] RXTRSH + 1). In this case, the interrupt condition is cleared and the next interrupt is asserted again when the XRDY or RRDY condition is met again.

If the second-interrupt-serving approach is used, an additional mechanism (draining feature) is implemented for cases where the transfer length is not a multiple of the FIFO threshold value (see Section 12.2.2.3.7.3 , *Draining Feature [I2C Mode Only]*).

Note

In target transmit mode (the I2C_CON[10] MST bit is cleared and the I2C_CON[9] TRX bit is set to 1), the draining feature must not be used, because the transfer length is not known at configuration time, and the external controller can end the transfer at any point by not acknowledging 1 data byte. If the draining feature is used in target transmit mode, data can remain in the TX FIFO without being transmitted over the I^2C bus. In this case, the TX FIFO must be cleared by setting the I2C_BUF[6] TXFIFO_CLR bit.

12.2.2.3.7.2 I2C FIFO Polling Mode

In FIFO polling mode (the I2C_IRQENABLE_SET[4] XRDY_IE and I2C_IRQENABLE_SET[3] RRDY_IE bits are disabled), the status of the module (receiver or transmitter) can be checked by polling the I2C_IRQSTATUS_RAW[4] XRDY and the I2C_IRQSTATUS_RAW[3] RRDY bits (the I2C_IRQSTATUS_RAW[13] RDR and I2C_IRQSTATUS_RAW[14] XDR bits can also be polled if the draining feature is enabled). The I2C_IRQSTATUS_RAW[4] XRDY and I2C_IRQSTATUS_RAW[3] RRDY bits accurately reflect the interrupt conditions described in the discussion of FIFO interrupt mode.

12.2.2.3.7.3 I2C Draining Feature

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

The draining feature is implemented to handle the end of a transfer whose length is not a multiple of the FIFO threshold values (the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold and the I2C_BUF[5-0] TXTRSH field value + 1 for the TX threshold). It can also transfer the remaining number of bytes (because the threshold is not reached).

This feature prevents the LH or the DMA controller from trying more FIFO accesses than necessary (for example, to generate at the end of a transfer a DMA RX request having fewer bytes in the FIFO than the configured DMA transfer length). Otherwise, an AERR interrupt is generated by the I2C_IRQSTATUS_RAW[7] AERR bit.

The draining mechanism generates an interrupt using the I2C_IRQSTATUS_RAW[13] RDR or I2C_IRQSTATUS_RAW[14] XDR bit at the end of the transfer, informing the LH that it must check the amount of data left to be transferred (the I2C_BUFSTAT[13-8] RXSTAT or I2C_BUFSTAT[5-0] TXSTAT bit fields) and enable the draining feature of the DMA controller by reconfiguring the DMA transfer length according to this value (when the DMA mode is enabled) or perform only the required number of data accesses (when the DMA mode is disabled).

In receive mode (controller or target), if the RX FIFO threshold (the I2C_BUF[13-8] RXTRSH bit field value + 1) is not reached, but the transfer ends on the I^2C bus and data remains in the RX FIFO (less than the threshold), the receive draining interrupt (the I2C_IRQSTATUS_RAW[13] RDR bit) is asserted to inform the LH that it can read the amount of data in the RX FIFO (the I2C_BUFSTAT[13-8] RXSTAT bit field). The LH performs a number of data read accesses equal to the I2C_BUFSTAT[13-8] RXSTAT bit field (interrupt or polling mode), or reconfigures the DMA controller with the required value to drain the FIFO.

In controller transmit mode, if the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field value + 1) is not reached, but the amount of data remaining to be written in the TX FIFO is less than the threshold, the transmit draining interrupt (the I2C_IRQSTATUS_RAW[14] XDR bit) is asserted to inform the LH that it can read the amount of data remaining to be written in the TX FIFO (the I2C_BUFSTAT[5-0] TXSTAT bit field). The LH must write the required number of data bytes specified by the I2C_BUFSTAT[5-0] TXSTAT bit field value or reconfigure the DMA controller with the value required to transfer the last bytes to the FIFO.

In controller mode, the LH can alternately not check the values of the I2C_BUFSTAT[5-0] TXSTAT and I2C_BUFSTAT[13-8] RXSTAT bit fields, because it can obtain this information internally (by computing the I2C_CNT[15-0] DATACOUNT bit field value modulo I2C_BUF[13-8] RXTRSH or I2C_BUF[5-0] TXTRSH).

By default, the draining feature is disabled; it can be enabled using the I2C_IRQENABLE_SET[14] XDR_IE or I2C_IRQENABLE_SET[13] RDR_IE bits (default disabled) only for transfers with lengths not equal to the threshold values (I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX threshold or the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold).

12.2.2.3.8 I2C Noise Filter

The noise filter is used to suppress any noise that is 50 ns or less in case of F/S operation modes, and any noise that is 10 ns or less in case of HS mode operation. The noise filter is always one period of the INTERNAL_CLK clock. This way, for HS mode operation (prescaler bypassed), the filter suppresses spikes of less than 10.4 ns.

For standard mode (for example, the I2C_PSC[7-0] PSC bit field = 4), the maximum width of suppressed spikes is 46.1 ns.

To ensure correct filtering, the prescaler must be programmed accordingly by the I2C*i*.I2C_PSC[7-0] PSC bit field.

12.2.2.3.9 I2C System Test Mode

A system test mode is available for multicontroller I2C module testing. This mode is enabled by setting the I2C_SYSTEST[15] ST_EN bit to 1. When this bit is cleared to 0, the I2C controller is configured in normal operation mode.

In system test mode, the I2C_SYSTEST[13-12] TMODE bit field selects the type of test. Table 12-48 lists the tests available for the multicontroller HS I2C.

Table 12-48. I2C List of Tests

I2C_SYSTEST[13-12] TMODE	Test	Description
00	Functional mode	Normal operation mode
01	Reserved (not used)	
10	Test of SCL serial clock line	The SCL line is driven with a permanent clock as if controlled with the parameters set in the I2C_PSC, I2C_SCLL, and I2C_SCLH registers.
11	Loop-back mode + SCL/SDA I/O	In controll transmit mode only, data transmitted out of the I2C_DATA register (write action) is received in the same I2C_DATA register through an internal path through the FIFO buffers. The interrupt request is normally generated if it is enabled. Moreover, the SCL and SDA are controlled with the I2C_SYSTEST[3-0] bits.

Note

When the I2C_SYSTEST[13-12] TMODE bit field is set to 11, the I2C controller must be configured in I^{2}C F/S (I2C_CON[13-12] OPMODE set to 00) or I^{2}C HS mode (I2C_CON[13-12] OPMODE set to 01).

Note

In normal operation mode (the I2C_SYSTEST[15] ST_EN bit cleared to 0), the I2C_SYSTEST[3-0] bits that control the SCL, SDA lines in system test mode are read-only bits.

In system test mode (the I2C_SYSTEST[15] ST_EN bit set to 1), the I2C_IRQSTATUS_RAW[4] XRDY, I2C_IRQSTATUS_RAW[3] RRDY, I2C_IRQSTATUS_RAW[10] XUDF, I2C_IRQSTATUS_RAW[11] ROVR, I2C_IRQSTATUS_RAW[2] ARDY and I2C_IRQSTATUS_RAW[1] NACK status bits can be set to 1 when the I2C_SYSTEST[11] SSB bit is set to 1. Clearing the I2C_SYSTEST[11] SSB bit to 0 does not clear the I2C_IRQSTATUS_RAW bits to 0. The I2C_IRQSTATUS_RAW bit field can be cleared to 0 only by writing 1 in the corresponding bits.

12.2.2.4 I2C Programming Guide

12.2.2.4.1 I2C Low-Level Programming Models

12.2.2.4.1.1 I2C Programming Model

This section describes the programming model of the multicontroller I2C configured in I^{2}C mode.

12.2.2.4.1.1.1 Main Program

12.2.2.4.1.1.1.1 Configure the Module Before Enabling the I2C Controller

Before enabling the I2C controller, perform the following steps:

1. Enable the functional and interface clocks (see *Module Integration* for details).
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock by programming the corresponding value in the I2C_PSC[7-0] PSC bit field. This value depends on the frequency of the functional clock (SYS_CLK).
3. Program the I2C_SCLL[7-0] SCLL and I2C_SCLH[7-0] SCLH bit fields to obtain a bit rate of 100 kbps or 400 kbps. These values depend on the internal sampling clock frequency (see Table 12-43).
4. (Optional) Program the I2C_SCLL[15-8] HSSCLL and I2C_SCLH[15-8] HSSCLH bit fields to obtain a bit rate of 400 kbps or 3.4 Mbps (for the second phase of HS mode). These values depend on the internal sampling clock frequency (see Table 12-43).
5. Configure the Own Address of the I2C controller by storing it in the I2C_OA register. Up to four Own Addresses can be programmed in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3) for each I2C controller.

> **Note**
>
> For a 10-bit address, set the corresponding expand Own Address bit in the I2C_CON register.

6. Set the TX threshold (in transmitter mode) and the RX threshold (in receiver mode) by setting the I2C_BUF[5-0] TXTRSH bit field to (TX threshold – 1) and the I2C_BUF[13-8] RXTRSH bit field to (RX threshold – 1), where the TX and RX thresholds are greater than or equal to 1.
7. Take the I2C controller out of reset by setting the I2C_CON[15] I2C_EN bit to 1.

12.2.2.4.1.1.1.2 Initialize the I2C Controller

To initialize the I2C controller, perform the following steps:

1. Configure the I2C_CON register:
    - For controller or target mode, set the I2C_CON[10] MST bit (0: target; 1: controller).
    - For transmitter or receiver mode, set the I2C_CON[9] TRX bit (0: receiver; 1: transmitter).
2. If using an interrupt to transmit and receive data, set the corresponding bit in the I2C_IRQENABLE_SET register to 1 (the I2C_IRQENABLE_SET[4] XRDY_IE bit for the transmit interrupt, the I2C_IRQENABLE_SET[3] RRDY bit for the receive interrupt).

12.2.2.4.1.1.1.3 Configure Target Address and the Data Control Register

In controller mode, configure the target address register by programming the I2C_SA[9-0] SA bit field and the number of data bytes (I^{2}C data payload) associated with the transfer by programming the I2C_CNT[15-0] DCOUNT bit field.

> **Note**
>
> For a 10-bit address, set the I2C_CON[8] XSA bit to 1.

12.2.2.4.1.1.1.4 Initiate a Transfer

Poll the I2C_IRQSTATUS_RAW[12] BB bit. If it is cleared to 0 (bus not busy), configure the I2C_CON[0] STT and I2C_CON[1] STP bits. To initiate a transfer, the I2C_CON[0] STT bit must be set to 1, and it is not mandatory to set the I2C_CON[1] STP bit to 1.

12.2.2.4.1.1.1.5 Receive Data

Poll the I2C_IRQSTATUS_RAW[3] RRDY bit, or use the RRDY interrupt (the I2C_IRQENABLE_SET[3] RRDY_IE bit must be set to 1) to read the receive data in the I2C_DATA register.

If the transfer length does not equal the RX FIFO threshold (the I2C_BUF[13-8] RTRSH bit field + 1), use the draining feature (enable the RDR interrupt by setting the I2C_IRQENABLE_SET[13] RDR_IE bit to 1).

Note

In receive mode only, the I2C_IRQSTATUS_RAW[11] ROVR (receive overrun) bit indicates whether the receiver has experienced overrun. An overrun condition occurs when the shift register and the RX FIFO are full. An overrun condition does not result in data loss; the I2C controller simply holds SCL to low to prevent other bytes from being received.

The I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a read access is performed in the I2C_DATA register while the RX FIFO is empty. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET[7] AERR_IE bit to 1.

12.2.2.4.1.1.1.6 Transmit Data

Poll the I2C_IRQSTATUS_RAW[4] XRDY bit, or use the XRDY interrupt (the I2C_IRQENABLE_SET[4] XRDY_IE bit must be set to 1) to write data to the I2C_DATA register.

If the transfer length does not equal the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field + 1), use the draining feature (enable the XDR interrupt by setting the I2C_IRQENABLE_SET[14] XDR_IE bit to 1).

Note

In transmit mode only, the I2C_IRQSTATUS_RAW[10] XUDF bit indicates whether the transmitter has experienced underflow.

In controller transmit mode, underflow occurs when the shift register and the TX FIFO are empty and there are still some bytes to transmit (the value of the I2C_CNT[15-0] DCOUNT bit field is not 0).

In target transmit mode, underflow occurs when the shift register and the TX FIFO are empty and the external I^2C controller device still requests data bytes to be read.

The I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a write access is performed in the I2C_DATA register while the TX FIFO is full. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET[7] AERR_IE bit to 1.

12.2.2.4.1.1.2 Interrupt Subroutine Sequence

1. Test for arbitration lost (the I2C_IRQSTATUS_RAW[0] AL bit) and resolve accordingly.
2. Test for no acknowledgment (the I2C_IRQSTATUS_RAW[1] NACK bit) and resolve accordingly.
3. Test for register access ready (the I2C_IRQSTATUS_RAW[2] ARDY bit) and resolve accordingly.
4. Test for receive data ready (the I2C_IRQSTATUS_RAW[3] RRDY bit) and resolve accordingly.
5. Test for transmit data ready (the I2C_IRQSTATUS_RAW[4] XRDY bit) and resolve accordingly.
6. Test for general call (the I2C_IRQSTATUS_RAW[5] GC bit) and resolve accordingly.
7. Test for start (S) condition (the I2C_IRQSTATUS_RAW[6] STC bit) and resolve accordingly. For this test, the functional clock must be inactive.
8. Test for access error (the I2C_IRQSTATUS_RAW[7] AERR bit) and resolve accordingly.
9. Test for bus free (the I2C_IRQSTATUS_RAW[8] BF bit) and resolve accordingly.

12.2.2.4.1.1.3 Programming Flow-Diagrams

Figure 12-52 through Figure 12-58 are procedure flow charts for programming the F/S and HS I^2C modes.

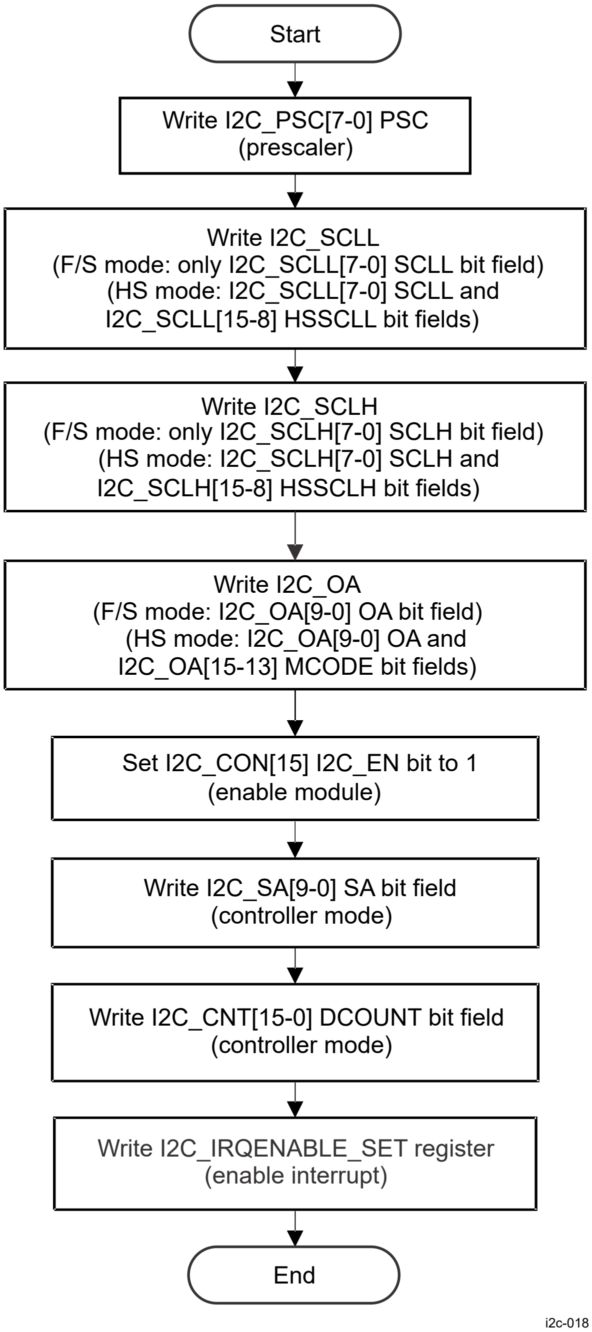

Figure 12-52. I2C Setup Procedure

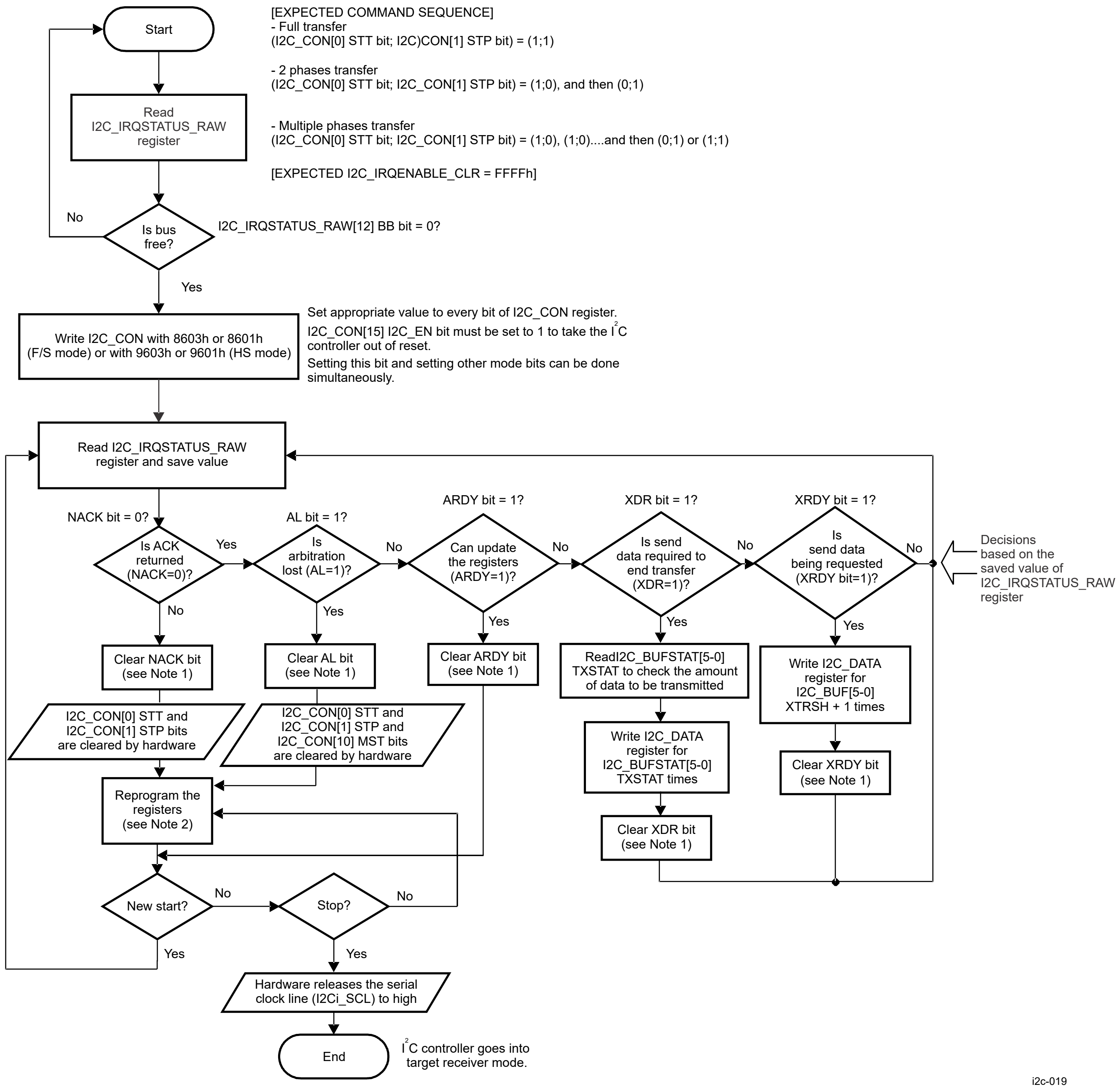

[EXPECTED COMMAND SEQUENCE]
- Full transfer
(I2C_CON[0] STT bit; I2C)CON[1] STP bit) = (1;1)

- 2 phases transfer
(I2C_CON[0] STT bit; I2C_CON[1] STP bit) = (1;0), and then (0;1)

- Multiple phases transfer
(I2C_CON[0] STT bit; I2C_CON[1] STP bit) = (1;0), (1;0)....and then (0;1) or (1;1)

[EXPECTED I2C_IRQENABLE_CLR = FFFFh]

Set appropriate value to every bit of I2C_CON register.
I2C_CON[15] I2C_EN bit must be set to 1 to take the I^2C controller out of reset.
Setting this bit and setting other mode bits can be done simultaneously.

I^2C controller goes into target receiver mode.

Note

The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram the registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-53. I2C Controller Transmitter Mode, Polling Method, in F/S and HS Modes

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Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.

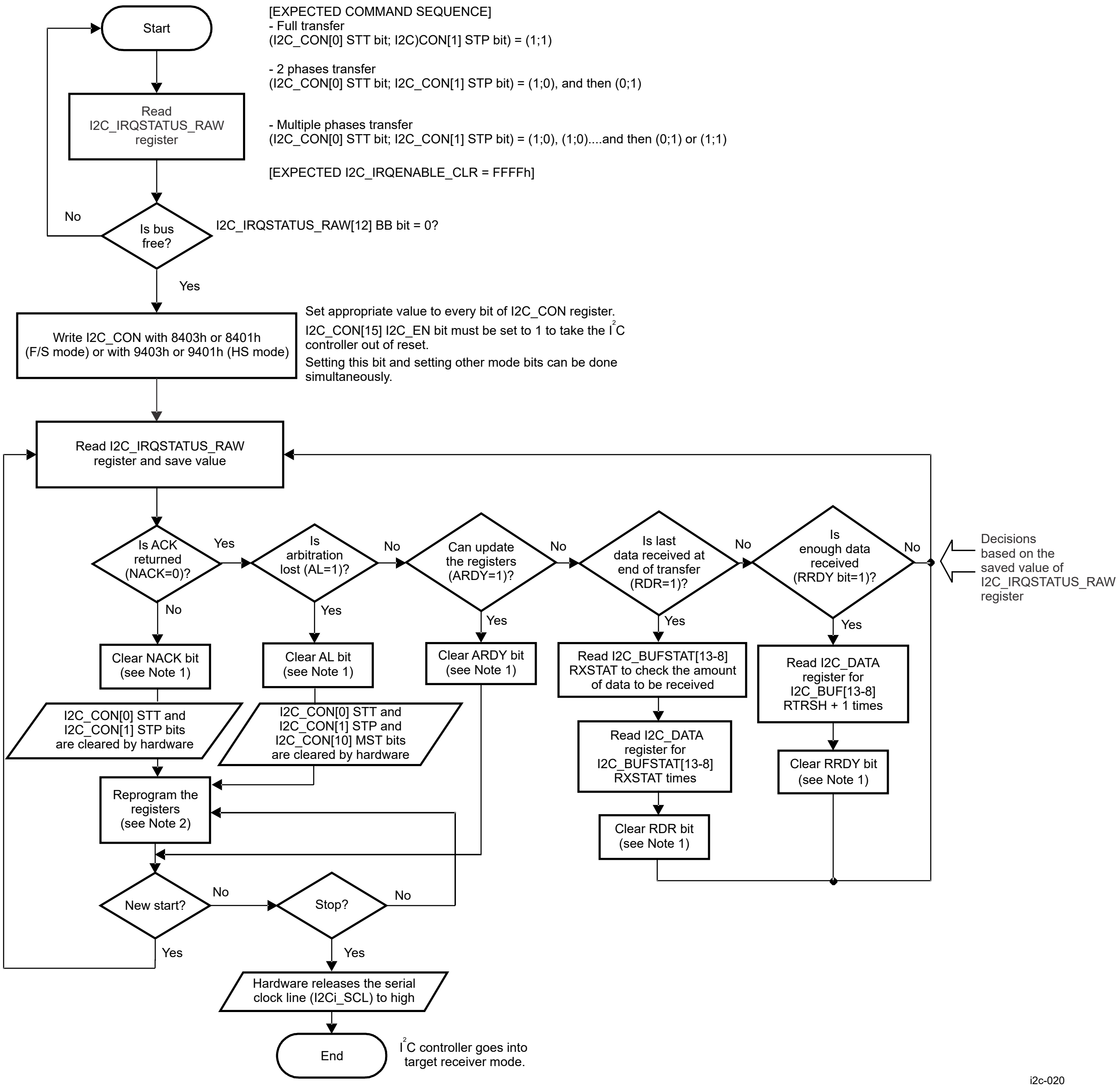

Note

The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-54. I2C Controller Receiver Mode, Polling Method, in F/S and HS Modes

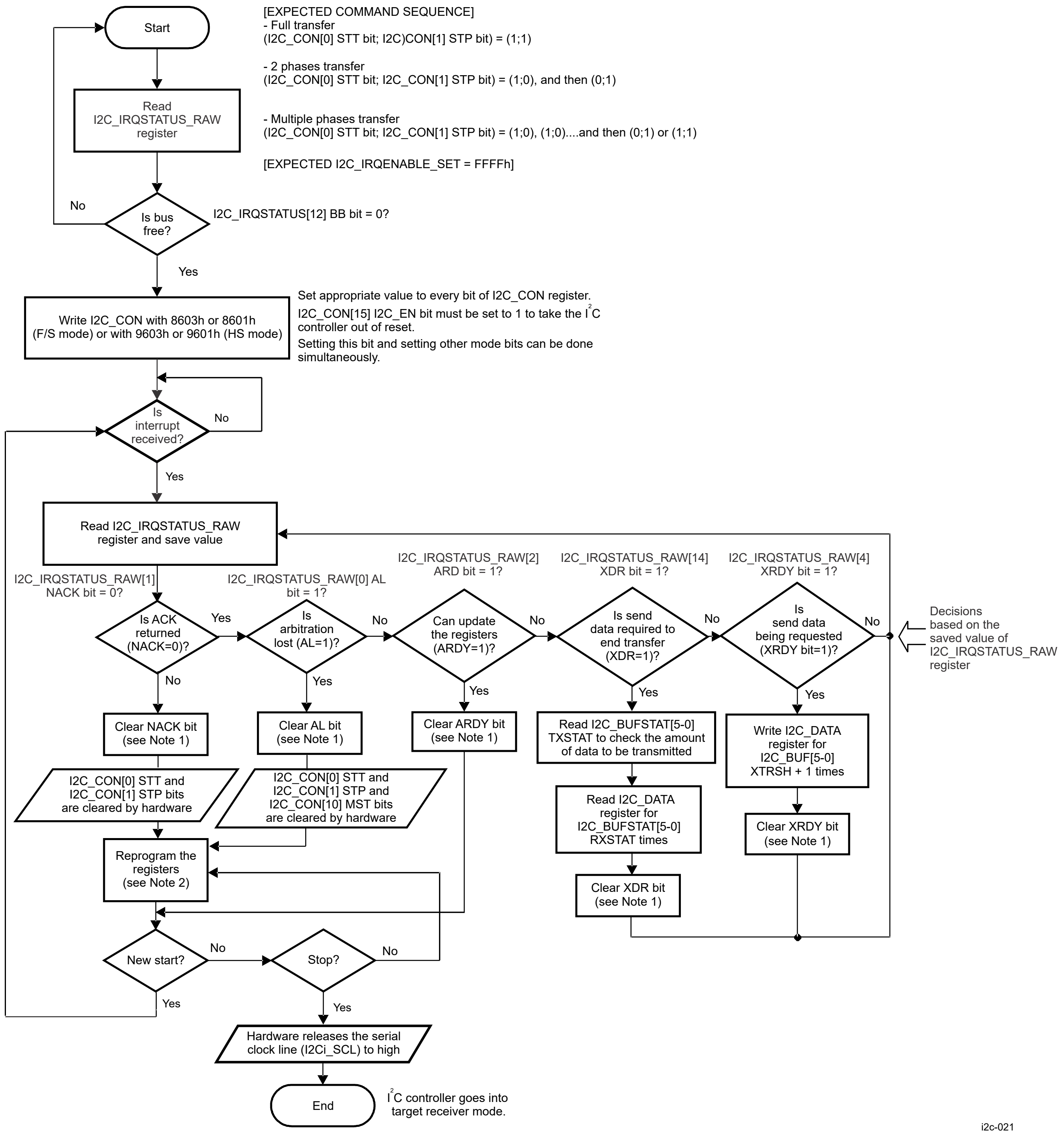

Note

The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-55. I2C Controller Transmitter Mode, Interrupt Method, in F/S and HS Modes

Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.

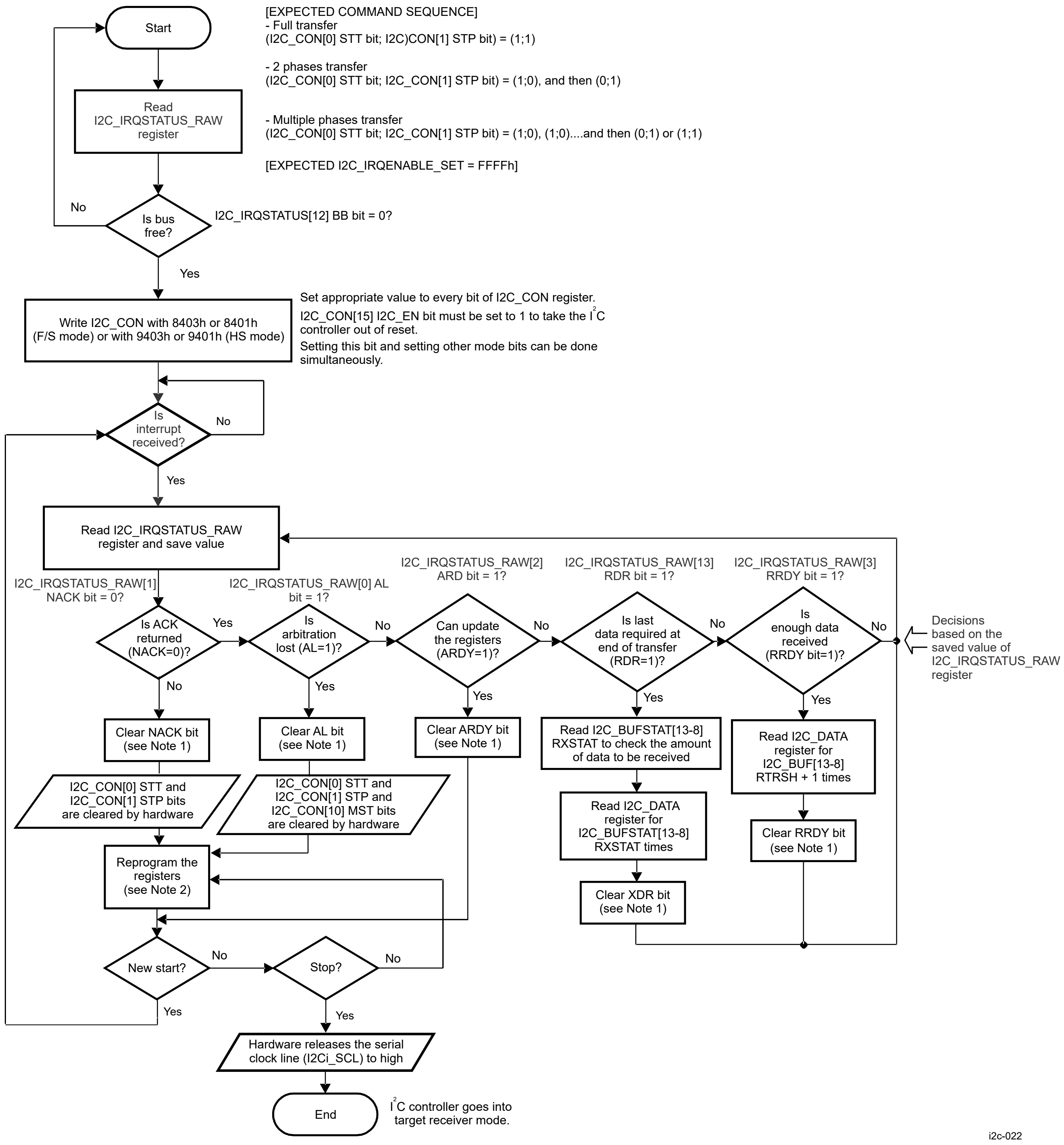

Note

The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-56. I2C Controller Receiver Mode, Interrupt Method, in F/S and HS Modes

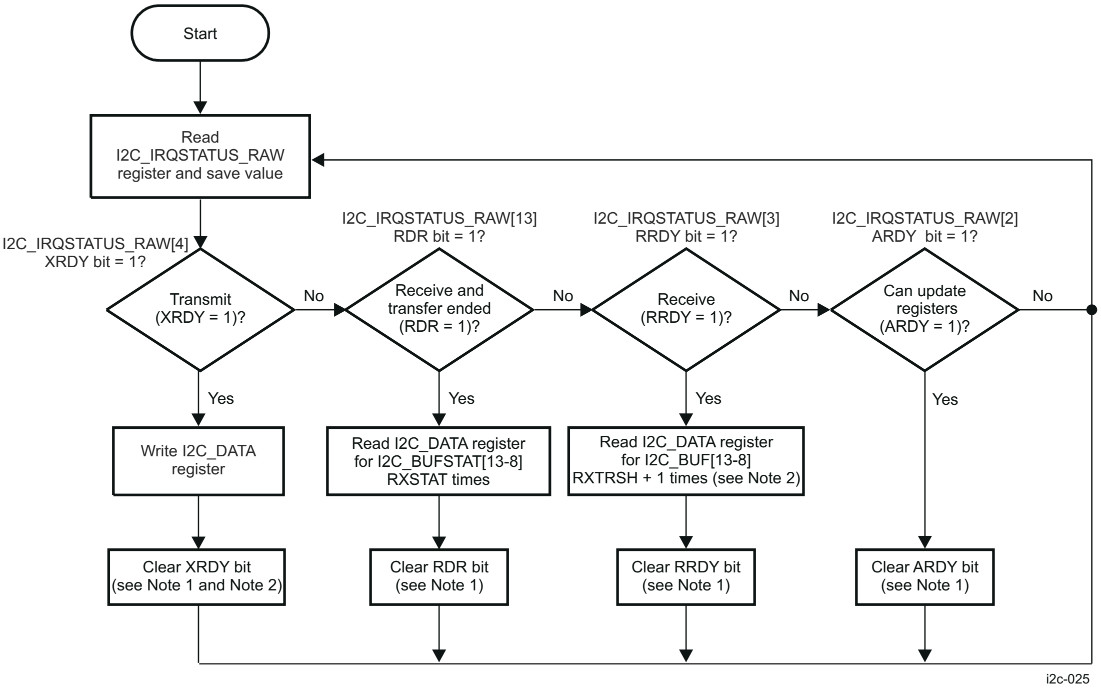

Note

The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

In target transmitter mode, the amount of data requested by the external controller I^{2}C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-57. I2C Target Transmitter/Receiver Mode, Polling

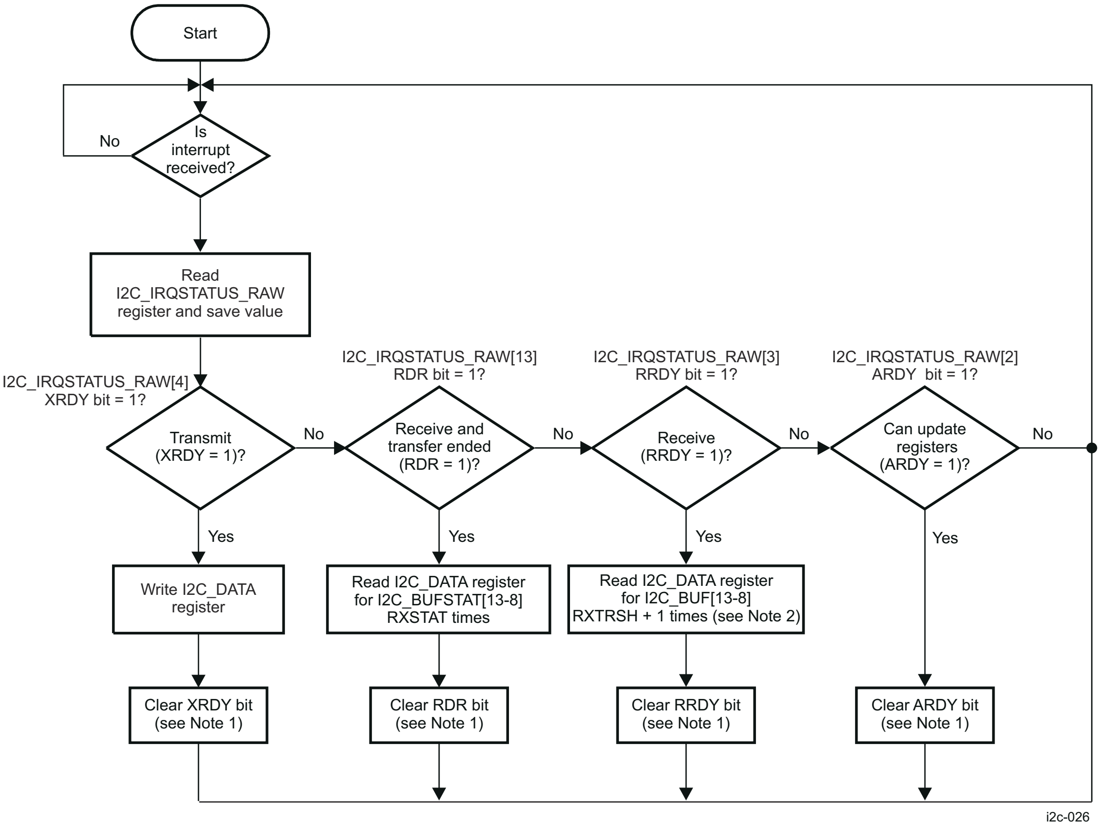

Note

The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

In target transmitter mode, the amount of data requested by the external controller I^2C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-58. I2C Target Transmitter/Receiver Mode, Interrupt

12.2.3 Multichannel Serial Peripheral Interface (MCSPI)

This section describes the Multichannel Serial Peripheral Interface (MCSPI) modules for the device.

12.2.3.1 MCSPI Overview

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

Figure 12-59 shows the MCSPI overview.

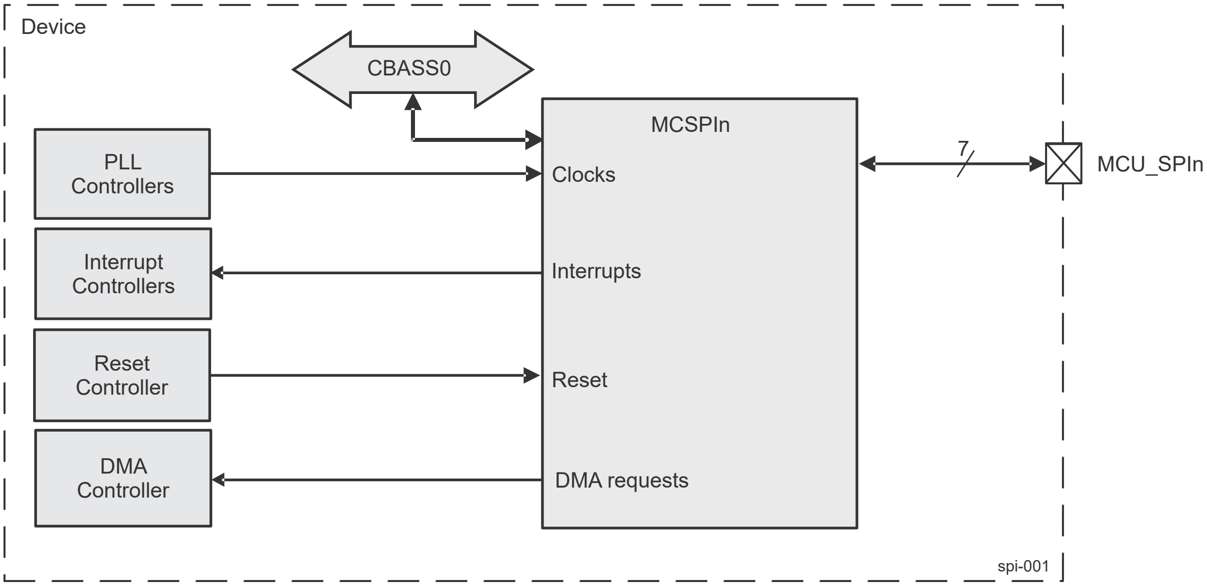

Figure 12-59. MCSPI Overview

n represents a valid instance of MCSPI in a domain.

12.2.3.1.1 MCSPI Features

The MCSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in peripheral mode
- Controller multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - MCSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.

12.2.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.2.3.2 MCSPI Environment

This section describes the MCSPI external connections (environment).

12.2.3.2.1 Basic MCSPI Pins for Controller Mode

Figure 12-60 shows all of the MCSPI interface signals in controller mode.

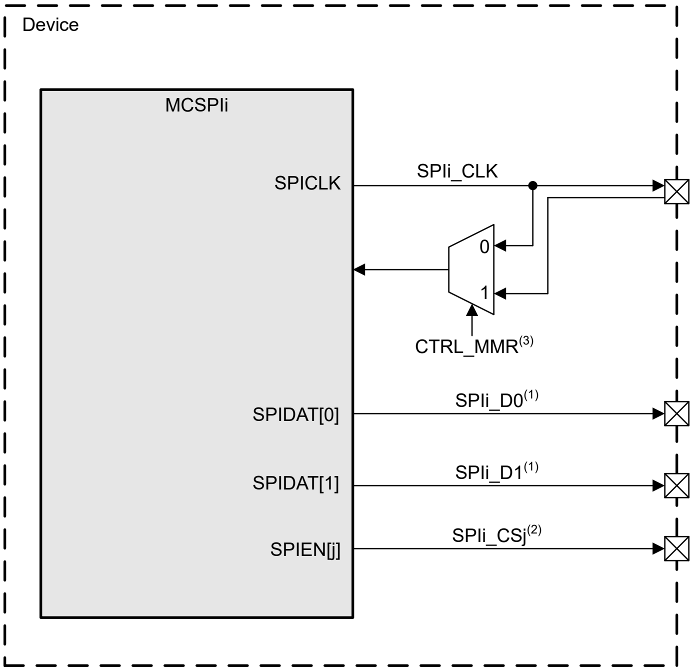

Note

Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

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Note

j = 0 to 3

Note

The source of the loopback clock is defined by MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL[16] MSTR_LB_CLKSEL bit (and the respective register for MCU_MCSPI1) and MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL[16] MSTR_LB_CLKSEL bit (and the respective for MCSPIi) in *Control Module (CTRL_MMR)*.

Note

i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Figure 12-60. MCSPI Interface Signals in Controller Mode

Table 12-49 describes the MCSPI I/O signals in controller mode.

Table 12-49. MCSPI I/O Signals (Controller Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
		MCU_MCSPIi(5)		
SPICLK	MCU_SPIi(5)_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	MCU_SPIi(5)_D0	O(3)	MCSPI Data I/O for controller mode.	HiZ

Table 12-49. MCSPI I/O Signals (Controller Mode) (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
SPIDAT[1]	MCU_SPIi[5]_D1	I[4]	MCSPI Data I/O for controller mode.	HiZ
SPIEN_[n]	MCU_SPIi[5]_CSi	O	MCSPI Chip-select i output for controller mode	HiZ
			MCSPIi[5]	
SPICLK	SPIi[5]_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	SPIi[5]_D0	O[3]	MCSPI Data I/O for controller mode.	HiZ
SPIDAT[1]	SPIi[5]_D1	I[4]	MCSPI Data I/O for controller mode.	HiZ
SPIEN_[n]	SPIi[5]_CSi	O	MCSPI Chip-select i output for controller mode	HiZ

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[16] DPE0.
(4) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[17] DPE1.
(5) i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Note

For SPIi[5]_CLK and MCU_SPIi[5]_CLK signals to work properly, the RXACTIVE bit of the appropriate MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIGx/ MAIN_CTRL_MMR_CFG0_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.3.2.2 Basic MCSPI Pins for Peripheral Mode

Figure 12-61 shows all of the MCSPI interface signals in peripheral mode.

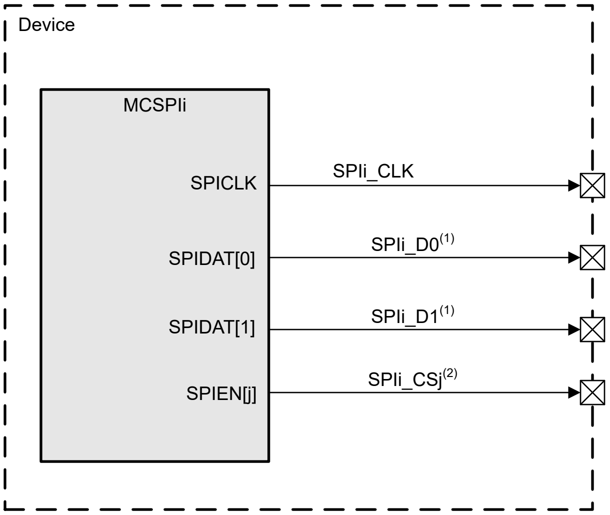

Note

Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Note

j = 0 to 3

Note

i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Figure 12-61. MCSPI Interface Signals in Peripheral Mode

Table 12-50 describes the MCSPI I/O signals in peripheral mode.

Table 12-50. MCSPI I/O Signals (Peripheral Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[1]
MCU_MCSPI[1-0]				
SPICLK	MCU_SPIi[5]_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ
SPIDAT[0]	MCU_SPIi[5]_D0	I[2]	MCSPI Data I/O for peripheral mode.	HiZ
SPIDAT[1]	MCU_SPIi[5]_D1	O[3]	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN_[n]	MCU_SPIi[5]_CSi	I[4]	MCSPI chip-select i input for peripheral mode.	HiZ
MCSPI[4-0]				
SPICLK	SPIi[5]_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ
SPIDAT[0]	SPIi[5]_D0	I[2]	MCSPI Data I/O for peripheral mode.	HiZ
SPIDAT[1]	SPIi[5]_D1	O[3]	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN_[n]	SPIi[5]_CSi	I[4]	MCSPI chip-select i input for peripheral mode.	HiZ

(1) HiZ = High Impedance

(2) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[16] DPE0.

(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[17] DPE1.

(4) The chip-select input in peripheral mode can be selected through the MCSPI_CH(i)CONF[22-21] SPIENSLV bit field.

(5) i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Note

For SPI[4-0]_CLK and MCU_SPI[1-0]_CLK signals to work properly, the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx/ CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.3.2.3 MCSPI Protocol and Data Format

The synchronous MCSPI protocol allows a controller device to initiate serial data transfers to a peripheral device. A peripheral select line (SPIEN_[n]) allows selection of an individual peripheral MCSPI device. Peripheral devices that are not selected do not interfere with MCSPI bus activities.

MCSPI offers the flexibility to modify the following parameters to adapt to the device features:

- Word length

  MCSPI supports any MCSPI word ranging from 4 bits to 32 bits long (the MCSPI_CH(i)CONF[11-7] WL bit field).

  MCSPI word length can be changed between transmissions to allow the controller device to communicate with peripheral devices that have different requirements.
- MCSPI enable (SPIEN_[n], for channel i)

  The polarity of the MCSPI enable signals is programmable (the MCSPI_CH(i)CONF[6] EPOL bit). SPIEN_[n] signals can be active high or low.

  Assertion of the SPIEN_[n] signals is programmable and can be done manually or automatically. The manual assertion mode is available in single controller mode only. SPIEN_[n] can be kept active between words with the MCSPI_CH(i)CONF[20] FORCE bit.

  Two consecutive words for two different peripheral devices can go along with active SPIEN_[n] signals with different polarity.
- Programmable start-bit

  In start-bit mode a start-bit is added before the MCSPI word length to indicate how the next MCSPI word must be handled. The start-bit is enabled by setting the MCSPI_CH(i)CONF[23] SBE bit to 1. The MCSPI_CH(i)CONF[24] SBPOL bit defines the polarity of the start-bit.
- Programmable MCSPI clock
  - Bit rate

    In controller mode, the baud rate of the MCSPI serial clock is programmable using the 50-MHz reference clock (from the device clock management module). Table 12-51 lists the SPICLK bit rates obtained for data transfer when programming the clock divider (the MCSPI_CH(i)CONF[5-2] CLKD bit field).

Table 12-51. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz
64	781.25 kHz
128	390.625 kHz
256	~195 kHz
512	~97.7 kHz
1024	~48.8 kHz
2048	~24.4 kHz

Table 12-51. MCSPI Controller Clock Rates (continued)

Divider	Clock Rate
4096	~12.2 kHz

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements and Switching Characteristics* chapter in the device-specific Datasheet.

– Polarity and phase

The polarity (the MCSPI_CH(i)CONF[1] POL bit) and the phase (the MCSPI_CH(i)CONF[0] PHA bit) of the MCSPI serial clock (SPICLK) are configurable to offer four combinations. Software selects the right combination, depending on the device. See Table 12-52 and Figure 12-62.

Data transfer is not required to update polarity, but it is configuration specific.

- In multi-controller mode POL/PHA is only updated to a channel's settings when a transaction is necessary on that channel.
- In single-controller mode POL/PHA is only updated on CS assertion (assuming channel already enabled), which is now SW-controlled using the FORCE bitfield.

Table 12-52. Phase and Polarity Combinations

Polarity (POL)	Phase (PHA)	MCSPI Mode	Description
0	0	Mode 0	SPICLK is inactive low and sampling occurs at the rising edge.
0	1	Mode 1	SPICLK is inactive low and sampling occurs at the falling edge.
1	0	Mode 2	SPICLK is inactive high and sampling occurs at the falling edge.
1	1	Mode 3	SPICLK is inactive high and sampling occurs at the rising edge.

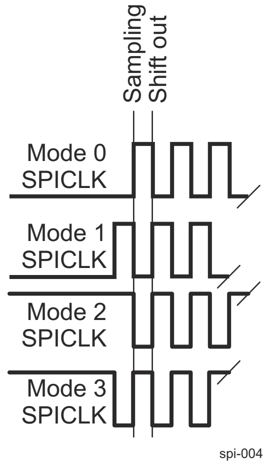

Figure 12-62. Phase and Polarity Combinations

12.2.3.2.3.1 Transfer Format

In controller and peripheral modes, the MCSPI drives the data lines when SPIEN_[n] is asserted.

Each word is transmitted starting with the most-significant bit (MSB).

This section explains the two cases of data transmission determined by the clock phase (PHA) and the type of data transmission using a start-bit (SBE) called the start-bit mode:

- Transmission in mode 0 and mode 2 (PHA = 0)

When PHA = 0, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid one-half cycle of SPICLK after the assertion of SPIEN_[n].

Therefore, the first edge of the SPICLK line is used by the controller to sample the first data bit sent by the peripheral. On the same edge, the first data bit sent by the controller is sampled by the peripheral.

On the next SPICLK edge, the received data bit is shifted into the receive shift register and a new data bit is transmitted on the serial data line.

This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on odd-numbered edges and shifted on even-numbered edges, see Figure 12-63.

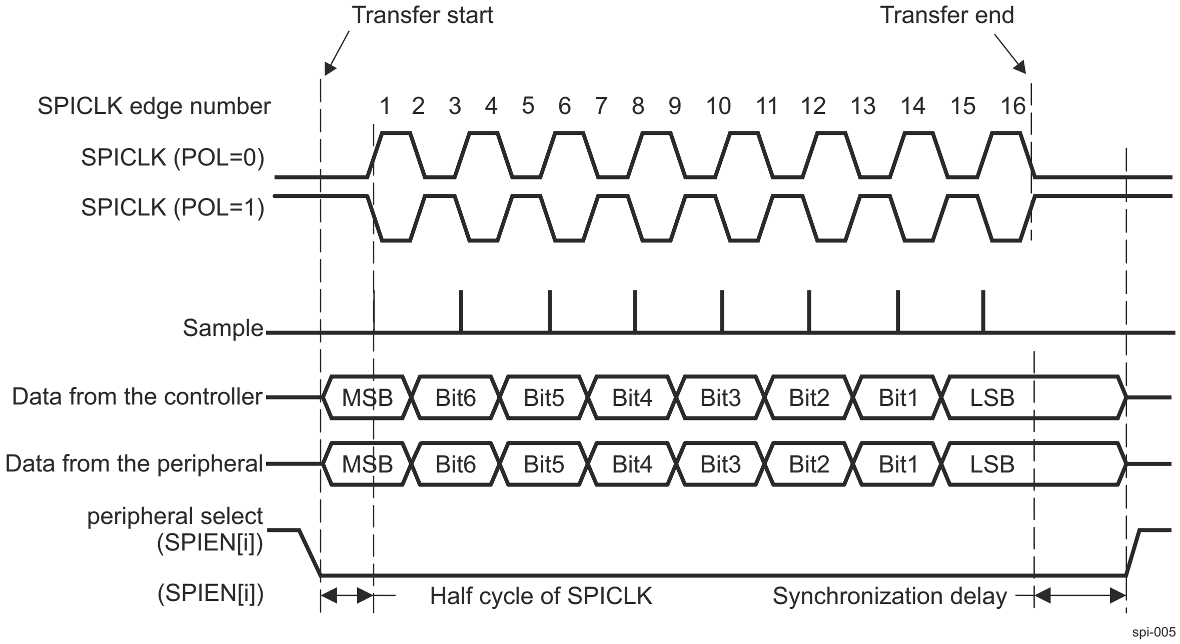

Figure 12-63. Full-Duplex Transfer Format With PHA = 0

- Transmission in mode 1 and mode 3 (PHA = 1)

  When PHA = 1, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid on the following SPICLK edge (one-half cycle later). This is the sampling edge for the controller and peripheral. A synchronization delay is added between the activation of SPIEN_[n] and the first SPICLK edge.

  The received data bit is shifted into the shift register on the third SPICLK edge.

  This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on even-numbered edges and shifted on odd-numbered edges.

Note

The minimum synchronization delay is one cycle of SPICLK, if the frequency of SPICLK equals the frequency of MCSPI_FCLK (MCSPI functional clock) in controller mode. The minimum synchronization delay is one-half cycle of SPICLK, if the frequency of SPICLK is lower than the frequency of MCSPI_FCLK in the controller and peripheral modes.

- Transmission with a start-bit (SBE = 1)

  When the MCSPI_CH(i)CONF[23] SBE bit is set to 1, a start-bit is added before the MSB to indicate whether the next MCSPI word must be handled as a command or as data.

  Figure 12-64 shows an example of a data transfer with an extra start-bit.

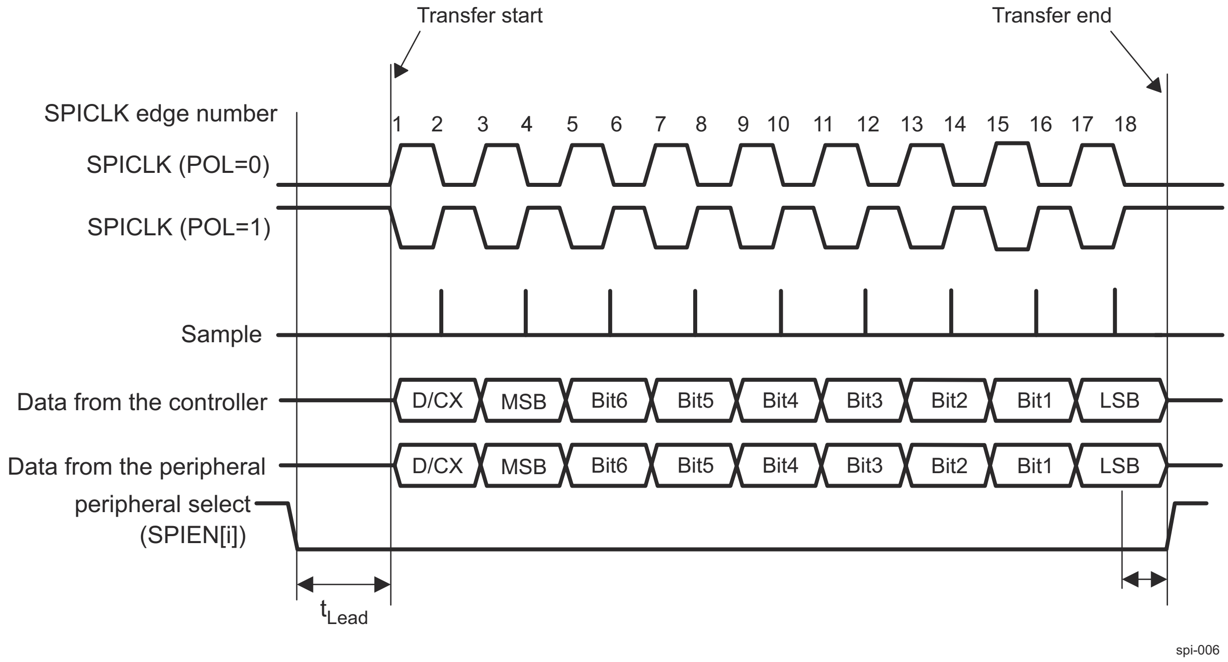

Figure 12-64. Extended MCSPI Transfer With a Start-Bit (SBE = 1)

12.2.3.2.4 MCSPI in Controller Mode

Figure 12-65 shows a case in controller mode (full-duplex) where the MCSPI module is connected with two peripheral devices.

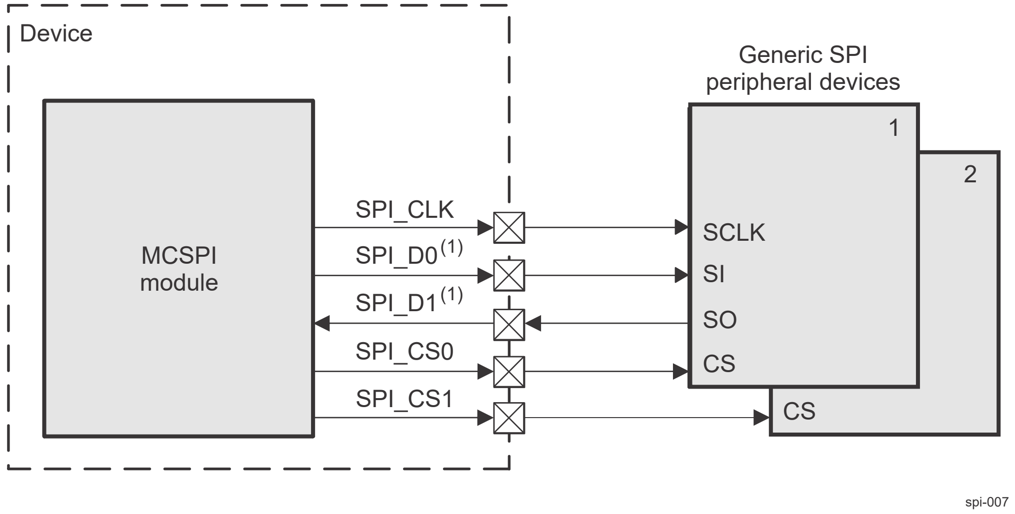

Note

Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-65. MCSPI Controller Mode (Full Duplex)

Figure 12-66 shows the controller single mode, which can also be configured in receive-only mode.

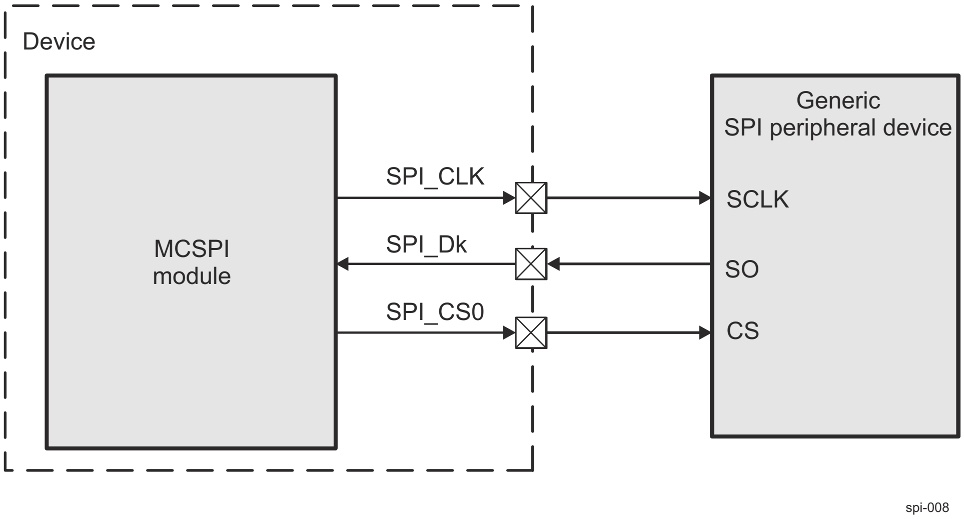

Note

k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

---

Figure 12-66. MCSPI Controller Single Mode (Receive Only)

12.2.3.2.5 MCSPI in Peripheral Mode

Figure 12-67 shows a case in peripheral mode (full-duplex).

Note

Only channel 0 can be configured as peripheral, but the chip-enable signal can be connected to any SPIEN_[n] pin and then rerouted internally to channel 0 (the MCSPI_CH0CONF[22-21] SPIENSLV bit field). For more information, see Section 12.2.3.4.4 , *MCSPI Peripheral Mode*.

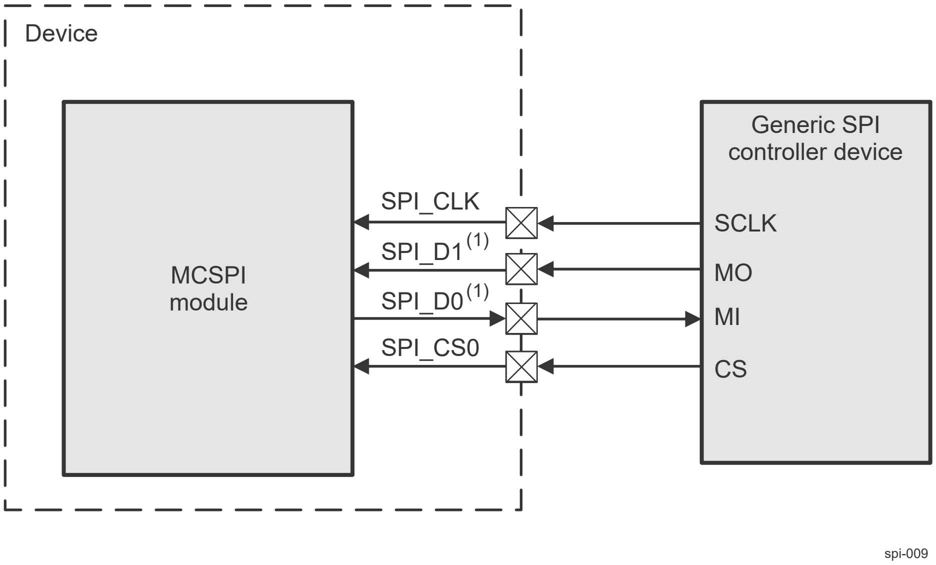

Note

Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-67. MCSPI Peripheral Mode (Full Duplex)

Figure 12-68 shows the peripheral single mode, which can also be configured in transmit-only mode.

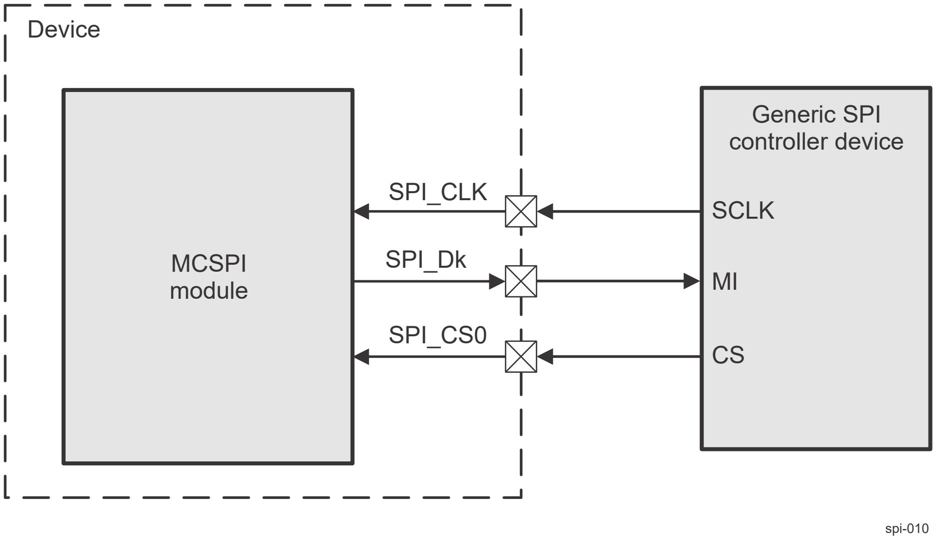

Note

k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-68. MCSPI Peripheral Single Mode (Transmit Only)

12.2.3.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.3.4 MCSPI Functional Description

12.2.3.4.1 MCSPI Block Diagram

Figure 12-69 shows the MCSPI module.

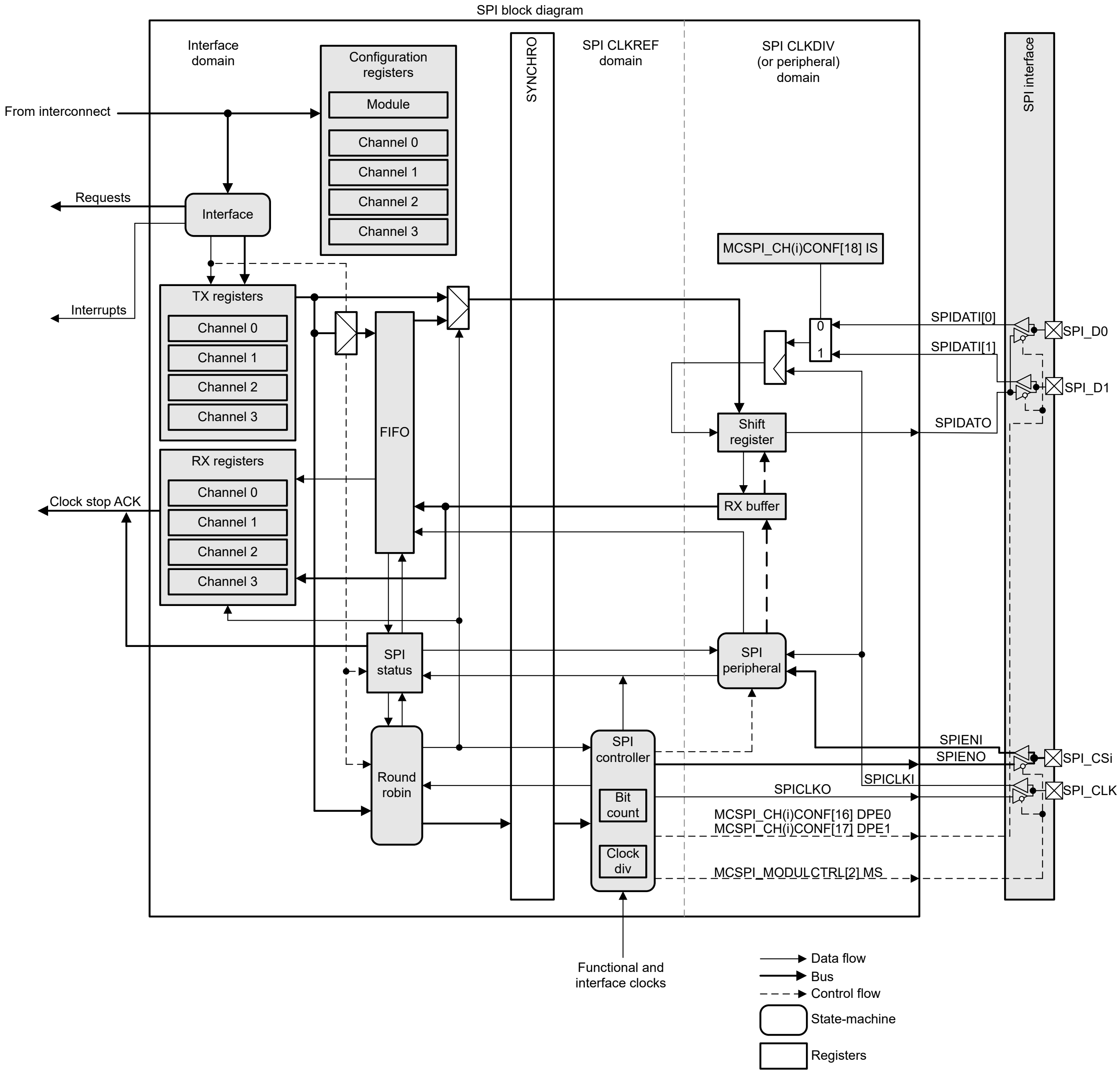

Figure 12-69. MCSPI Block Diagram

12.2.3.4.2 MCSPI Reset

The MCSPI module can be reset either by hardware or by software reset. All configuration registers and all state machines are reset by the hardware reset signal (MCSPI_RST). MCSPI can be reset by software through the MCSPI_SYSCONFIG[1] SOFTRESET bit. This bit has the same impact on the module as the hardware reset signal. The only exception is that the MCSPI_SYSCONFIG register is not affected by that software reset.

12.2.3.4.3 MCSPI Controller Mode

12.2.3.4.3.1 Controller Mode Features

The MCSPI controller mode supports multichannel communication with up to four independent MCSPI communication channel contexts. The MCSPI initiates a data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) and generates clock (SPICLK) and control (SPIEN_[n]) signals.

Connected to multiple external devices, the MCSPI exchanges data with one MCSPI device at a time through two main modes (available in peripheral mode):

- Two-data-pins interface mode (transmit-and-receive mode for full-duplex transmission)
- Single-data-pin interface mode (recommended for half-duplex transmission)

Note

There is a fixed chip select line allocation in multichannel controller mode. Channel i is mapped to SPIEN_[n].

Two DMA request events (read and write) allow synchronized accesses of the DMA controller with the activity of MCSPI.

Three interrupt events can be used for data transmission and reception in controller mode (for more information about interrupts, see Section 12.2.3.4.7.1 , *Interrupt Events in Controller Mode*).

12.2.3.4.3.2 Controller Transmit-and-Receive Mode (Full Duplex)

In full-duplex transmission, data is transmitted (shifted out serially on SPIDAT[0]) and received (shifted in serially on SPIDAT[1]) simultaneously on separate data lines.

The controller transmit-and-receive mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field).

Channel access to the shift registers for transmission/reception is based on the MCSPI_TXi transmitter register state, the MCSPI_RXi receiver register state, and round-robin arbitration.

Channels that meet the following rules are included in the round-robin list of active channels scheduled for transmission and/or reception. The arbiter skips channels that do not meet the rules and searches in the rotation for the next enabled channel.

- Rule 1: Only enabled channels (the MCSPI_CH(i)CTRL[0] EN bit) can be scheduled for transmission and/or reception.
- Rule 2: If its MCSPI_TXi transmitter register is not empty (the MCSPI_CH(i)STAT[1] TXS bit), an enabled channel can be scheduled when the shift register is assigned. If the MCSPI_TXi register is empty when the shift register is assigned, the TXx_UNDERFLOW event is activated, and the next enabled channel with new data to transmit is scheduled (see also transmit-only mode).
- Rule 3: An enabled channel can be scheduled if its receive register is not full (the MCSPI_CH(i)STAT[0] RXS bit) when the shift register is assigned (see also receive-only mode). Therefore, the MCSPI_RXi register cannot be overwritten. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set to this mode.

When MCSPI word transfer completes (the MCSPI_CH(i)STAT[2] EOT bit is set), the updated MCSPI_TXi register of the next scheduled channel is loaded into the shift register. The serialization (transmit-and-receive) starts depending on the channel communication configuration. When serialization completes, the received data transfers to the channel receive register.

The serial clock (SPICLK) synchronizes shifting and sampling of the information on the two serial data lines (SPIDAT[0] and SPIDAT[1]). Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral.

Figure 12-70 shows an example of a full-duplex system with a controller device on the left and a peripheral device on the right. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral. At the same time, WordB transfers from the peripheral to the controller.

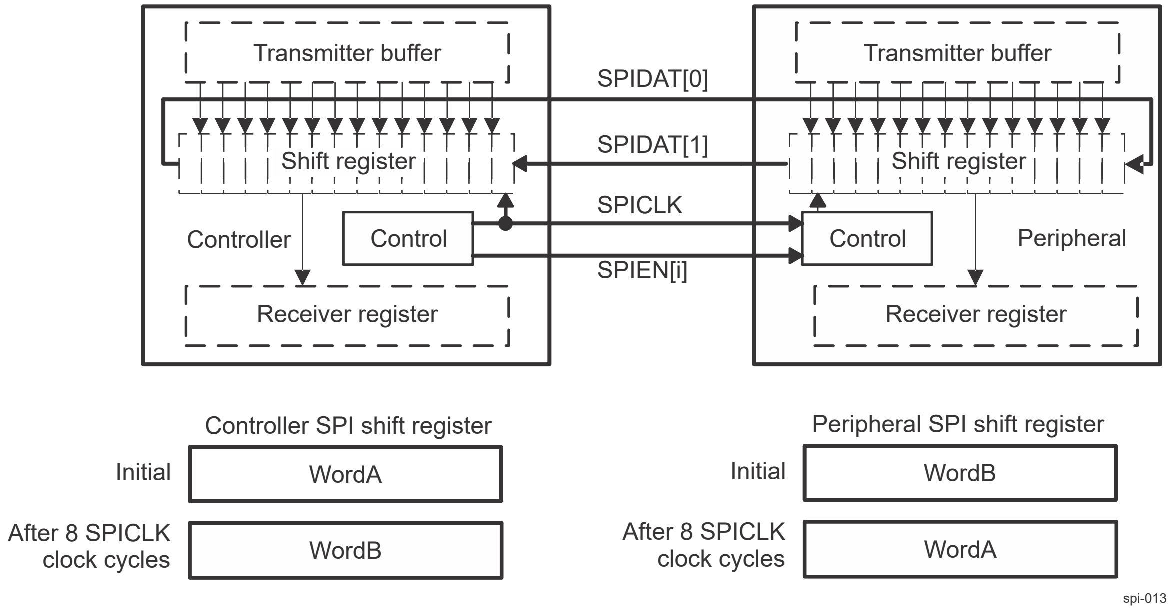

Figure 12-70. MCSPI Full-Duplex Transmission (Example)

12.2.3.4.3.3 Controller Transmit-Only Mode (Half Duplex)

The controller transmit-only mode prevents the processor from reading the MCSPI_RXi register (minimizing data movement) when only transmission is meaningful.

The controller transmit-only mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field). Transmission starts only after data is loaded into the MCSPI_TXi register.

Rule 1 and Rule 2, defined in Section 12.2.3.4.3.2 , apply in this mode.

Rule 3, defined in Section 12.2.3.4.3.2 , does not apply.

In controller transmit-only mode, the MCSPI_RXi register state FULL does not prevent transmission and the MCSPI_RXi register is always overwritten with the new MCSPI word. This event is not significant when only transmission is meaningful. Thus, the RX0_OVERFLOW bit in the MCSPI_IRQSTATUS register is never set in this mode.

The hardware automatically disables the RX_FULL interrupt and the DMA read requests.

The transfer status is given by the MCSPI_CH(i)STAT[2] EOT bit.

12.2.3.4.3.4 Controller Receive-Only Mode (Half Duplex)

The controller receive mode prevents the processor from refilling the MCSPI_TXi register (minimizing data movement) when only reception is meaningful.

The controller receive mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field).

The controller receive-only mode enables channel scheduling only on the empty state of the MCSPI_RXi register.

Rule 1 and Rule 3, defined in Section 12.2.3.4.3.2 , apply in this mode.

Rule 2, defined in Section 12.2.3.4.3.2 , does not apply.

In the controller receive-only mode, software must write dummy data to the MCSPI_TXi register. Only one dummy write is enough to receive any number of words from the peripheral. Software must ensure that the MCSPI_TXi register is always full (the TXi_EMPTY bits of MCSPI_IRQSTATUS) when receiving. The content of the MCSPI_TXi register is always loaded into the shift register when the shift register is assigned. After writing the dummy data to the MCSPI_TXi register, the TXi_EMPTY and TXi_UNDERFLOW bits in the MCSPI_IRQSTATUS register are never set in receive-only mode.

The MCSPI_CH(i)STAT[2] EOT bit gives the status of serialization. The RXi_FULL bits of the MCSPI_IRQSTATUS register are set when received data is loaded from the shift register to the corresponding MCSPI_RXi register. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.2.3.4.3.5 Single-Channel Controller Mode

When the MCSPI is configured as a controller device with a single enabled channel (MCSPI_MODULCTRL[2] MS = 0 and MCSPI_MODULCTRL[0] SINGLE = 1), the assertion of the SPIEN_[n] signal is optional depending on device connected to the controller. In 3-pin mode (MCSPI_MODULCTRL[1] PIN34 = 1) the controller starts transmitting data when a write to the MCSPI_TXi register or the FIFO is performed. In 4-pin mode (MCSPI_MODULCTRL[1] PIN34 = 0) the assertion and de-assertion of SPIEN_[n] is controlled by software using the MCSPI_CH(i)CONF[20] FORCE bit.

12.2.3.4.3.5.1 Programming Tips When Switching to Another Channel

When a single channel is enabled and data transfer is ongoing:

- Wait for the MCSPI word transfer to complete (wait until the MCSPI_CH(i)STAT[2] EOT bit is set to 1) before disabling the current channel and enabling a different channel.
- Disable the current channel, and then enable the other channel.

12.2.3.4.3.5.2 Force SPIEN_[n] Mode

Continuous transfers are allowed manually by keeping the SPIEN_[n] signal active for successive MCSPI words transfer. Several sequences (configuration/enable/disable of the channel) can be run without deactivating the SPIEN_[n] line. This mode is supported by all channels and any controller sequence can be used (transmit-receive, transmit-only, receive-only).

Keeping the SPIEN_[n] active mode is supported when:

- A single channel is used (with the MCSPI_MODULCTRL[0] SINGLE bit set to 1).
- Transfer parameters are loaded in the configuration register of the appropriate channel (MCSPI_CH(i)CONF).

  The state of the SPIEN_[n] signal is programmable:
  - Writing 1 to the MCSPI_CH(i)CONF[20] FORCE bit drives the SPIEN_[n] line high when the MCSPI_CH(i)CONF[6] EPOL bit is set to 0. SPIEN_[n] is driven low when the MCSPI_CH(i)CONF[6] EPOL bit is set to 1.
  - Writing 0 to the MCSPI_CH(i)CONF[20] FORCE bit drives the SPIEN_[n] line low when the MCSPI_CH(i)CONF[6] EPOL bit is set to 0. SPIEN_[n] is driven high when the MCSPI_CH(i)CONF[6] EPOL bit is set to 1.
- A single channel is enabled (the MCSPI_CH(i)CTRL[0] EN bit is set to 1). The first enabled channel activates the SPIEN_[n] line.

When the channel is enabled, the SPIEN_[n] signal activates with the programmed polarity. As in the multichannel controller mode, the transfer start depends on the status of the MCSPI_TXi register (the MCSPI_CH(i)STAT[1] TXS bit), the status of the MCSPI_RXi register (the MCSPI_CH(i)STAT[1] RXS bit), and the defined mode (the MCSPI_CH(i)CONF[13-12] TRM bit field) of the channel enabled.

The MCSPI_CH(i)STAT[2] EOT bit gives the transfer status of each MCSPI word. The RXx_FULL bit in the MCSPI_IRQSTATUS register is set when received data is loaded from the shift register to the MCSPI_RXi register.

A change in the configuration parameters is propagated directly on the MCSPI interface. If the SPIEN_[n] signal is activated, ensure that the configuration is changed only between MCSPI words to avoid corrupting the current transfer.

Note

To avoid data corruption, SPIEN_[n] polarity and SPICLK phase and SPICLK polarity must not be modified when the SPIEN_[n] signal is activated.

A delay between MCSPI words that requires the connected MCSPI peripheral device to switch from one configuration to another (for instance, from transmit-only to receive-only) must be handled by software.

At the end of the last MCSPI word, the channel must be deactivated (the MCSPI_CH(i)CTRL[0] EN bit set to 0) and SPIEN_[n] can be forced to its INACTIVE state using the MCSPI_CH(i)CONF[20] FORCE bit.

Figure 12-71 and Figure 12-72 show successive transfers with SPIEN_[n] maintained active low with a different configuration for each MCSPI word in single-data-pin and dual-data-pin interface modes, respectively.

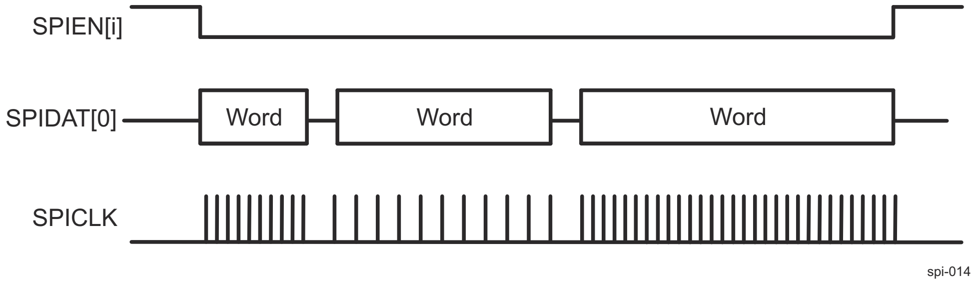

Figure 12-71. Continuous Transfers With SPIEN_[n] Maintained Active (Single-Data-Pin Interface Mode)

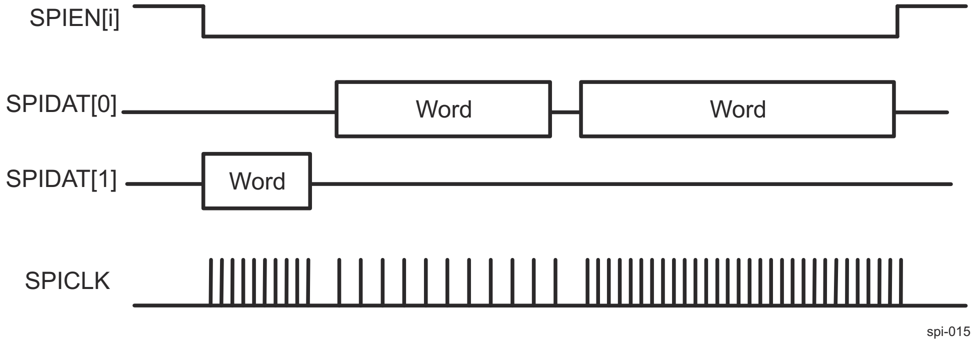

Figure 12-72. Continuous Transfers With SPIEN_[n] Maintained Active (Dual-Data-Pin Interface Mode)

Note

The SPIEN_[n] signal can be maintained active via software using the MCSPI_CH(i)CONF[20] FORCE bit only when the MCSPI_MODULCTRL[0] SINGLE bit is set to 0x1.

12.2.3.4.3.5.3 Turbo Mode

Turbo mode improves the throughput of the MCSPI interface when a single channel is enabled by allowing transfers until the shift register and the MCSPI_RXi register are full. Turbo mode is time saving when a transfer exceeds two words. This mode is programmable per channel (through the MCSPI_CH(i)CONF[9] TURBO bit).

When several channels are enabled, the TURBO bit has no effect and the channel access to the shift registers remains as previously described.

In turbo mode, Rule 1 and Rule 2 apply, but Rule 3 does not (see Section 12.2.3.4.3.2 , *Controller Transmit-and-Receive Mode (Full Duplex)*). An enabled channel can be scheduled if its receive register is full (the MCSPI_CH(i)STAT[0] RXS bit) when the shift-register is assigned until the shift register is full.

The MCSPI_RXi register cannot be overwritten in turbo mode. Consequently, the MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.2.3.4.3.6 Start-Bit Mode

In start-bit mode, an extended bit is added before the MCSPI word to indicate whether the next MCSPI word must be handled as a command or as data. This feature is available only in controller mode. Start-bit mode cannot be used at the same time as turbo mode and/or force SPIEN_[n] mode. In this case, only one channel can be used; round-robin arbitration is not possible.

This mode is programmable per channel by setting the MCSPI_CH(i)CONF[23] SBE bit to 1. The polarity of the extended bit is programmable per channel. When the MCSPI_CH(i)CONF[24] SBPOL bit is set to 0, the MCSPI word must be handled as a command. When the MCSPI_CH(i)CONF[24] SBPOL bit is set to 1, the MCSPI word must be handled as data. Moreover, start-bit polarity can be changed dynamically during start-bit transfer without disabling the channel for reconfiguration; in this case, users must configure the MCSPI_CH(i)CONF[24] SBPOL bit before writing the MCSPI word to be transmitted to the TX register.

12.2.3.4.3.7 Chip-Select Timing Control

The chip-select (CS) timing control is available only in controller mode with automatic CS generation (the MCSPI_MODULCTRL[0] SINGLE bit set to 0) to add a programmable delay between CS assertion and first clock edge, or CS removal and last clock edge. This option is available only in 4-pin mode when MCSPI_MODULCTRL[1] PIN34 set to 0.

This mode is programmable per channel through the MCSPI_CH(i)CONF[26-25] TCS0 bit field.

Figure 12-73 shows the CS SPIEN timing controls.

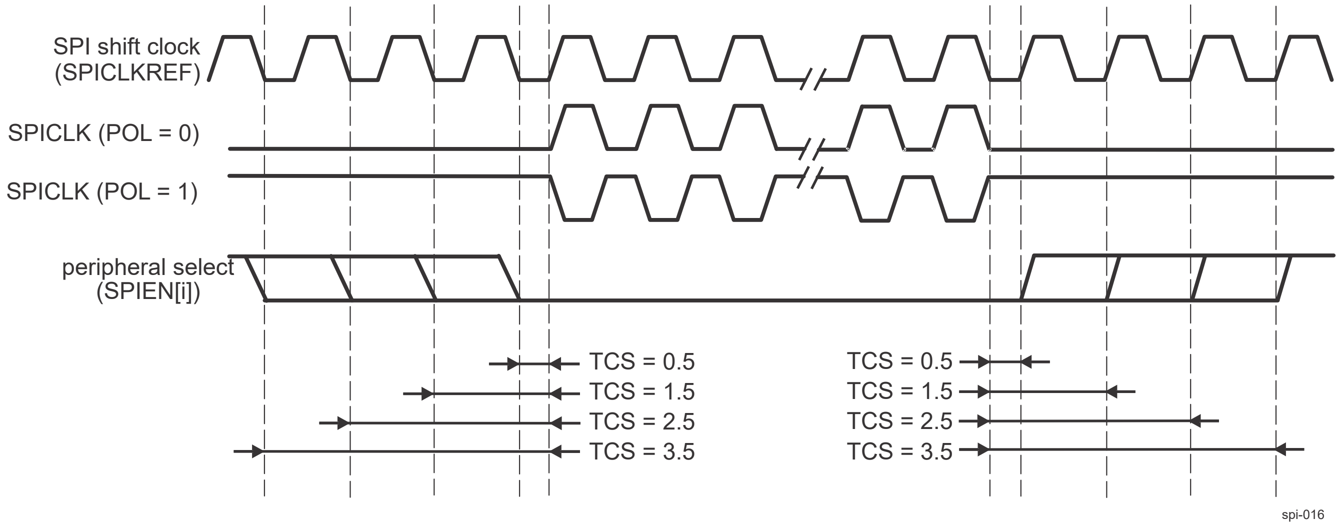

Figure 12-73. CS SPIEN Timing Controls

Note

Because of the design implementation for transfers using a clock divider ratio set to 1 (clock bypassed), a half cycle must be added to the value between CS assertion and the first clock edge with PHA = 1 or between CS removal and the last clock edge with PHA = 0.

12.2.3.4.3.8 Programmable MCSPI Clock (SPICLK)

In controller mode, the baud rate of the MCSPI serial clock is programmable.

An internal reference clock, SPICLKREF, is used as input of a programmable divider (the MCSPI_CH(i)CONF[5-2] CLKD bit field) to generate the bit rate of the serial output clock SPICLK. Table 12-53 summarizes the supported divisor values.

Table 12-53. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz
64	781.25 kHz
128	~390 kHz
256	~195 kHz
512	~97.7 kHz
1024	~48.8 kHz
2048	~24.4 kHz
4096	~12.2 kHz
8192 and higher: Division not supported	–

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements and Switching Characteristics* chapter in the device-specific Datasheet.

12.2.3.4.3.8.1 Clock Ratio Granularity

By default, the clock division ratio is defined by the MCSPI_CH(i)CONF[5-2] CLKD bit field with power-of-2 granularity leading to a clock division in the range 1 to 4096; in this case, the duty cycle is always 50 percent. With the MCSPI_CH(i)CONF[29] CLKG bit, clock division granularity can be changed to one clock cycle; in that case the MCSPI_CH(i)CTRL[15-8] EXTCLK bit field is concatenated with the MCSPI_CH(i)CONF[5-2] CLKD bit field to give a 12-bit-wide division ratio in the range 1 to 4096.

When granularity is one clock cycle (the CLKG bit set to 1), for the odd value of the clock ratio, the clock high level lasts one clock cycle more than the low level, depending on the MCSPI_CH(i)CONF[1] POL and MCSPI_CH(i)CONF[0] PHA bits (see Table 12-54).

Table 12-54. CLKSPIO High/Low Time Computation

Clock Ratio F_{RATIO}	CLKSPIO High Time	CLKSPIO Low Time
1	T_{HIGH_REF}	T_{LOW_REF}
Even >= 2	T_ref * (F_{RATIO}/2)	T_ref * (F_{RATIO}/2)
Odd >= (POL = PHA)	T_ref * (F_{RATIO}– 1)/2	T_ref * (F_{RATIO} + 1)/2
Odd >= (POL =! PHA)	T_ref * (F_{RATIO}+ 1)/2	T_ref * (F_{RATIO} – 1)/2

Note

F_{RATIO} = SPICLK frequency (F_{OUT}) division ratio
T_{HIGH} = SPICLK high time period
T_{LOW} = SPICLK low time period
T_ref = MCSPI_FCLK period
T_{HIGH_REF} = MCSPI_FCLK high time period
T_{LOW_REF} = MCSPI_FCLK low time period

If the CLKG bit is set to 1; F_{RATIO} = EXTCLK concatenated with CLKD + 1.

For odd ratio values, the duty cycle is calculated as follows:

Duty_cycle = $(1 – 1/F_{RATIO})/2$

Table 12-55 shows examples of clock granularity with a clock source frequency of 50 MHz.

Table 12-55. Clock Granularity Examples

EXTCLK	CLKD	CLKG	F_{RATIO}	PHA	POL	T_{HIGH} (ns)	T_{LOW} (ns)	T_{PERIOD} (ns)	Duty Cycle	F_{OUT} (MHz)
X	0	0	1	X	X	10.0	10.0	20.0	50–50	50
X	1	0	2	X	X	20.0	20.0	40.0	50–50	25
X	2	0	4	X	X	40.0	40.0	80.0	50–50	12.5
X	3	0	8	X	X	80.0	80.0	160.0	50–50	6.2
0	0	1	1	X	X	10.0	10.0	20.0	50–50	50
0	1	1	2	X	X	20.0	20.0	40.0	50–50	25
0	2	1	3	1	0	40.0	20.0	60.0	66–33	16.6
0	2	1	3	1	1	20.0	40.0	60.0	33–66	16.6
0	3	1	4	X	X	40.0	40.0	80.0	50–50	12.5
5	0	1	81	1	0	820.0	800.0	1620.0	50.6–49.4	0.617
5	7	1	88	X	X	880.0	880.0	1760.0	50–50	0.568

12.2.3.4.4 MCSPI Peripheral Mode

To select the MCSPI peripheral mode, set the MCSPI_MODULCTRL[2] MS bit.

A MCSPI peripheral device can be connected to up to four external MCSPI controller devices but handles transactions with one MCSPI controller device at a time.

In peripheral mode, the MCSPI initiates data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) when it is selected by an active control signal (SPIEN_[n]) and receives an MCSPI clock (SPICLK) from the external MCSPI controller device. Only channel 0 can be configured as a peripheral but through the MCSPI_CH0CONF_0[22-21] SPIENSLV bit field any of the SPIEN_[n] signals can be used to select the MCSPI module. In peripheral mode and when the MCSPI_MODULCTRL[1] PIN34 is set to 0x0 (default behaviour), the MCSPI uses the edge of SPIEN_[n] to detect word length. For this reason, SPIEN_[n] must become inactive between each word.

When the MCSPI_MODULCTRL[1] PIN34 is set to 0x0, the MCSPI does not support SPIEN_[n] active between MCSPI words. In this case, the MCSPI uses the edge to detect word length.

When the MCSPI_MODULCTRL[1] PIN34 is set to 0x1, a multiword transfer can be performed without needing the external MCSPI controller to deactivate SPIEN_[n] between each word as in this case the MCSPI module works in 3-pin peripheral mode and SPIEN_[n] is not needed.

12.2.3.4.4.1 Dedicated Resources

Only channel 0 can be enabled in peripheral mode.

Figure 12-74 shows an example of four peripherals wired on a single controller device.

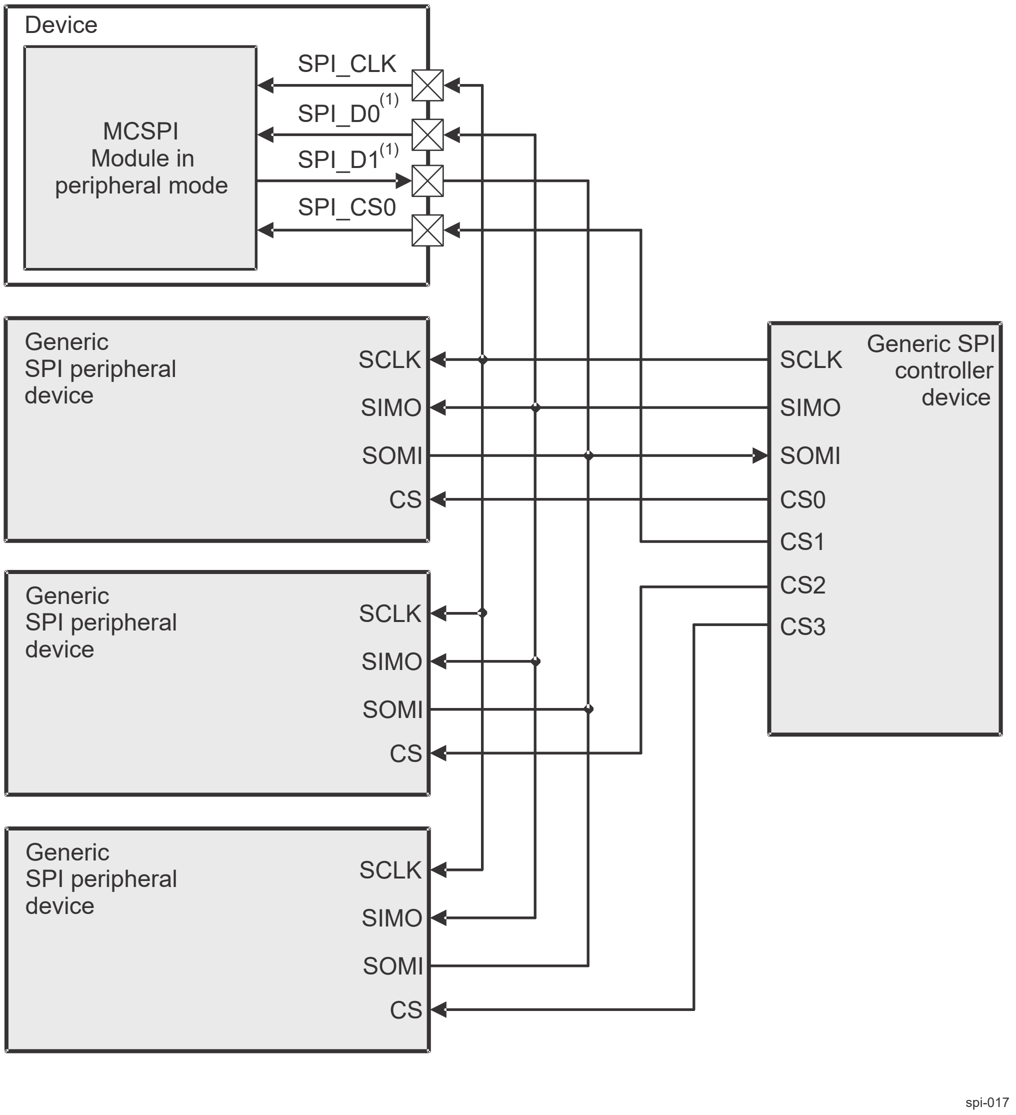

Note

Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-74. Example of MCSPI Peripheral With One Controller and Multiple Peripheral Devices on Channel 0

Channel 0 in peripheral mode has the following resources:

- Its own channel enable, programmable with the MCSPI_CH0CTRL[0] EN bit. This channel must be enabled before transmission and reception.
- For this mode, the peripheral-select signal can be detected on any of the SPIEN_[n] ports. This is programmable with the MCSPI_CH0CONF[22-21] SPIENSLV bit field.
- Its own transmitter register, MCSPI_TX0, on top of the common transmit shift register. If the MCSPI_TX0 register is empty, the MCSPI_CH0STAT[1] TXS bit is set. If MCSPI is selected by an external controller (the active signal on the SPIEN_[n] port assigned to channel 0), the MCSPI_TX0 register content of channel 0 is always loaded into the shift register, whether its content is updated or not. The MCSPI_TX0 register must be loaded before MCSPI is selected by a controller.

- Its own receiver register, MCSPI_RX0, on top of the common receive shift register. If the MCSPI_RX0 register is full, the MCSPI_CH0STAT[0] RXS bit is set.

Note

The MCSPI_TXi and MCSPI_RXi registers are not used. Reading from or writing to a channel register other than channel 0 has no effect.

- Its own communication configuration with the following parameters through the MCSPI_CH0CONF:
  - Transmit and receive modes, programmable with the TRM field
  - Interface mode (two data pins or single data pin) and data pins assignment, both programmable with the IS and DPE bits. (The MCSPI modules are in peripheral mode after reset and must be properly configured for the modules to act in controller mode.)
  - MCSPI word length, programmable with the WL bit
  - SPIEN_[n] polarity, programmable with the EPOL bit
  - SPICLK polarity, programmable with the POL bit
  - SPICLK phase, programmable with the PHA bit

  The SPICLK frequency of a transfer is controlled by the external MCSPI controller connected to the MCSPI peripheral device. The MCSPI_CH0CONF[5-2] CLKD bit field is not used in peripheral mode.

Note

The configuration of the channel can be loaded in the MCSPI_CH0CONF only when the channel is disabled.

- Two DMA request events, read and write, synchronize read/write accesses of the DMA controller with the activity of MCSPI. DMA requests are asserted using the MCSPI_CH0CONF[15] DMAR bit for reading and the MCSPI_CH0CONF[14] DMAW bit for writing.
- Four interrupt events (see Section 12.2.3.4.7.2 , *Interrupt Events in Peripheral Mode*).

12.2.3.4.4.2 Peripheral Transmit-and-Receive Mode

The peripheral receive mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x0).

In peripheral transmit-and-receive mode, the MCSPI_TX0 register must be loaded before MCSPI is selected by an external MCSPI controller device.

After a channel is enabled, transmission and reception proceed with interrupt and DMA request events.

The MCSPI_TX0 register content is always loaded in the shift register whether it is updated or not. The event TX0_UNDERFLOW is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CH0STAT[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX0 register (see Section 12.2.3.4.7.2 , *Interrupt Events in Peripheral Mode*).

12.2.3.4.4.3 Peripheral Transmit-Only Mode

The peripheral transmit-only mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x2) and avoids the requirement for the processor to read the MCSPI_RX0 register (minimizing data movement) only when transmission is meaningful.

To use the MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX0 register.

When the MCSPI word transfer completes, the MCSPI_CH0STAT[2] EOT bit is set.

Figure 12-75 shows a half-duplex system with a controller device on the left and a transmit-only peripheral device on the right. Each time a bit transfers out from the peripheral, 1 bit transfers in the controller. After eight cycles of the serial clock SPICLK, WordB transfers from the peripheral to the controller.

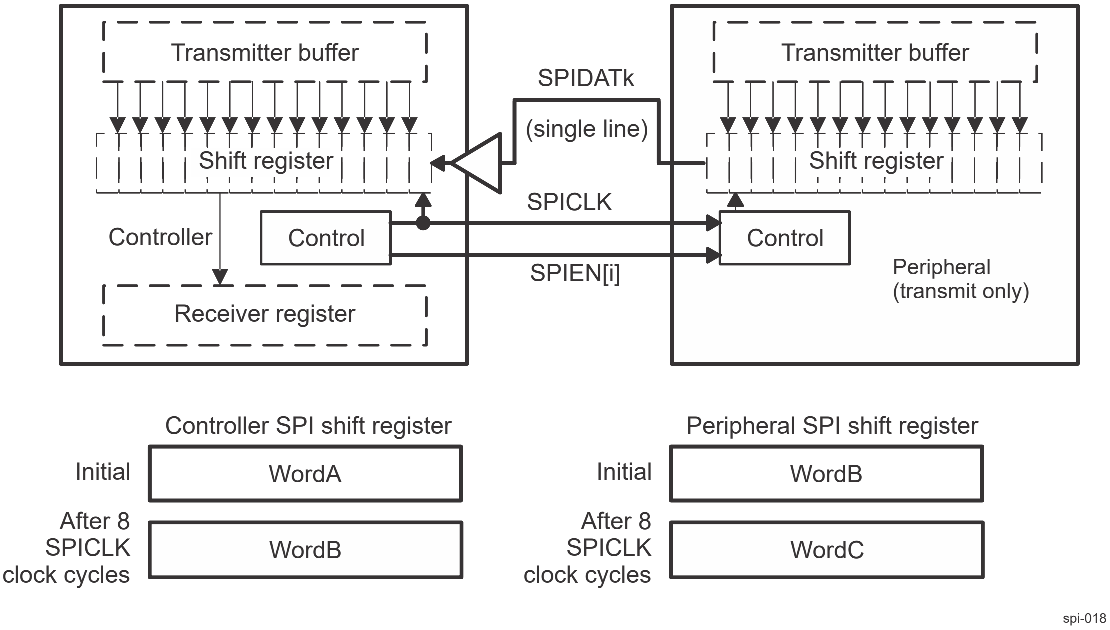

Note

k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-75. MCSPI Half-Duplex Transmission (Transmit-Only Peripheral)

12.2.3.4.4.4 Peripheral Receive-Only Mode

The peripheral receive mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x1).

In receive-only mode, the MCSPI_TX0 register must be loaded before the MCSPI is selected by an external MCSPI controller device. The MCSPI_TX0 register content is always loaded into the shift register whether it is updated or not. The TX0_UNDERFLOW event is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CH0STAT[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use the MCSPI as a peripheral receive-only device, the TX0_EMPTY and TX0_UNDERFLOW interrupts and the DMA write requests must be disabled due to the state of the MCSPI_TX0 register.

For a full-duplex transmission, the serial clock (SPICLK) synchronizes shifting and sampling of the information on the single serial data line. For full duplex, two data lines are required. If SPICLK synchronizes on a single serial data line, the data line should be half-duplex.

Figure 12-76 shows a half-duplex system with a controller device on the left and a receive-only peripheral device on the right. Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral.

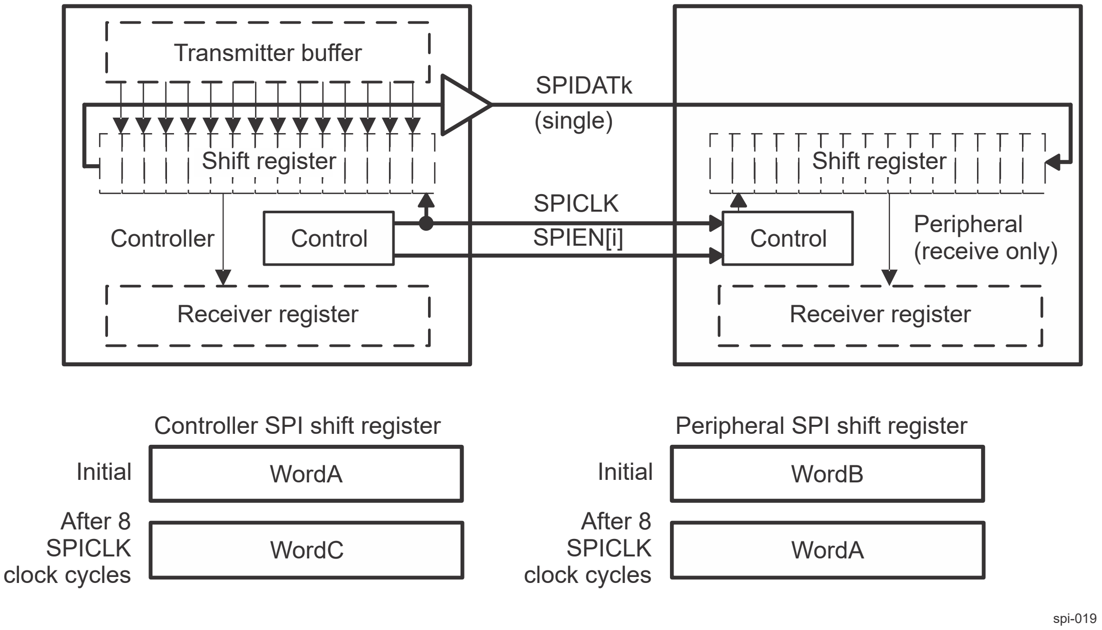

Note

k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-76. MCSPI Half-Duplex Transmission (Receive-Only Peripheral)

12.2.3.4.5 MCSPI 3-Pin or 4-Pin Mode

Depending on targeted application the MCSPI interface can be configured to use 3 or 4 pins through the MCSPI_MODULCTRL[1] PIN34 bit. If this bit is set to 0, MCSPI is in 4-pin mode using the SPICLK, SPIDAT[0], SPIDAT[1] and SPIEN_[n] signals. If PIN34 is set to 1 the controller is in 3-pin mode and SPIEN_[n] is not used. In this mode all options related to chip select management are useless (EPOL, FORCE and TCS0 bits of MCSPI_CH(i)CONF). 3-pin and 4-pin operation applies to both controller and peripheral modes.

12.2.3.4.6 MCSPI FIFO Buffer Management

The MCSPI controller has a built-in 64-byte buffer to unload the DMA or interrupt handler and improve data throughput.

This buffer can be used by only one channel at a time and is selected by setting the MCSPI_CH(i)CONF[28] FFER or MCSPI_CH(i)CONF[27] FFEW bit to 1. If several channels are selected and several FIFO enable bit fields are set to 1, the controller forces the buffer not to be used; the driver must set only one FIFO enable bit field.

The buffer can be used in the following modes:

- Controller or peripheral mode
- Transmit-only, receive-only, or transmit-and-receive mode
- Single channel or turbo mode, or normal round-robin mode. In round-robin mode the buffer is used by only one channel.

Every word length (MCSPI_CH(i)CONF[11-7] WL) is supported.

In transmit-and-receive mode, the buffer can be used in transmit (see Figure 12-77) or receive (see Figure 12-78) directions, or in both directions. If only one direction is chosen in transmit-and-receive mode, the full buffer is used for this direction. In both directions, the buffer is split into two halves, one for each direction (see Figure 12-79).

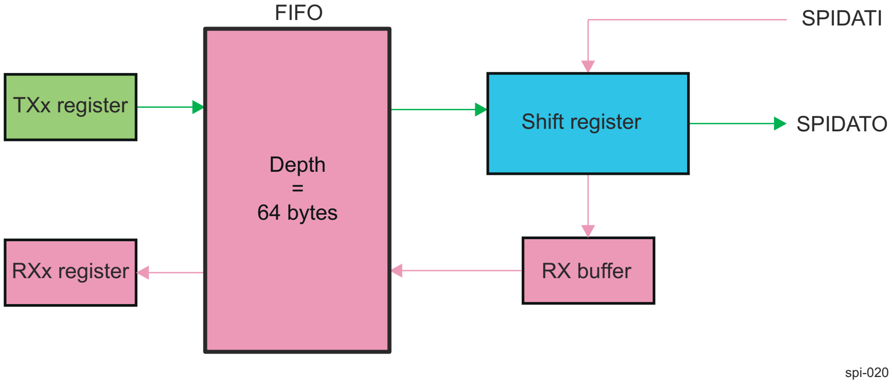

Figure 12-77. Buffer Used in Transmit Direction Only

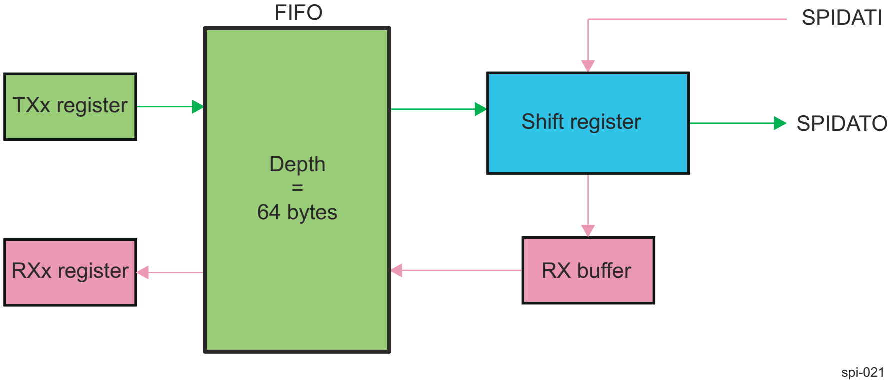

Figure 12-78. Buffer Used in Receive Direction Only

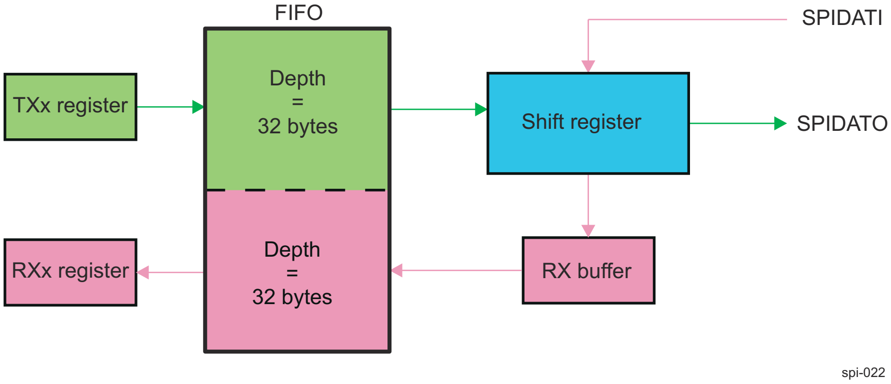

Figure 12-79. Buffer Used for Transmit and Receive Directions

Two levels (MCSPI_XFERLEVEL[5-0] AEL and MCSPI_XFERLEVEL[13-8] AFL) rule the buffer management. The granularity of these levels is 1 byte; it is not aligned with the MCSPI word length. The driver must set these values as a multiple of the MCSPI word length defined in WL. Table 12-56 lists the number of bytes written in the FIFO, depending on the word length.

Table 12-56. FIFO Writes, Word Length Relationship

	MCSPI Word Length (WL)		
	3 ≤ WL≤ 7	**8 ≤ WL ≤ 15**	**16 ≤ WL ≤ 31**
Number of bytes written in the FIFO	1 byte	2 bytes	4 bytes

The FIFO buffer pointers are reset when the corresponding channel is enabled or the FIFO configuration changes.

12.2.3.4.6.1 Buffer Almost Full

The MCSPI_XFERLEVEL[15-8] AFL bit field is needed when the buffer is used to receive an MCSPI word from a peripheral (the MCSPI_CH(i)CONF[28] FFER bit must be set to 1). It defines the almost-full buffer status. See Figure 12-80.

When the FIFO pointer reaches this level, an interrupt or a DMA request is sent to the processor to enable the system to read AFL + 1 bytes from the receive register.

Note

AFL + 1 must correspond to a multiple value of the MCSPI_CH(i)CONF[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first receive register read.

No new request is asserted again as long as the system has not performed the correct number of read accesses.

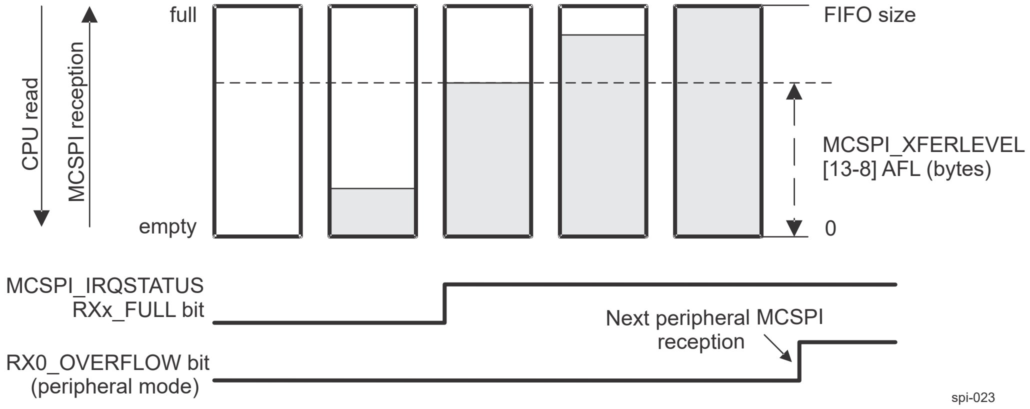

Figure 12-80. Buffer Almost Full Level (AFL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS RXi_FULL flag.

12.2.3.4.6.2 Buffer Almost Empty

The MCSPI_XFERLEVEL[7-0] AEL bit field is needed when the buffer is used to transmit an MCSPI word to a peripheral (the MCSPI_CH(i)CONF[27] FFEW bit must be set to 1). It defines the almost-empty buffer status. See Figure 12-81.

When the FIFO pointer does not reach this level, an interrupt or a DMA request is sent to the processor to enable the system to write AEL + 1 bytes to the transmit register.

Note

AEL + 1 must correspond to a multiple value of the MCSPI_CH(i)CONF[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first transmit register write.

No new request is asserted again as long as the system has not performed the correct number of write accesses.

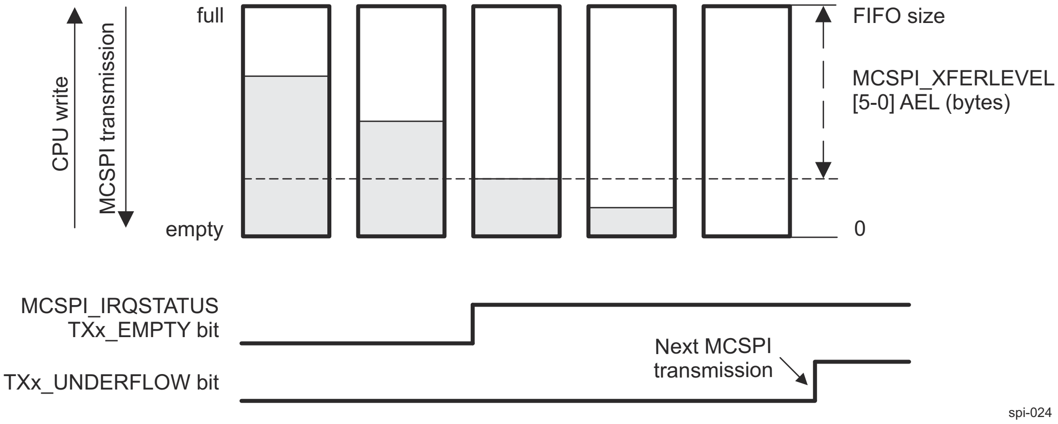

Figure 12-81. Buffer Almost Empty Level (AEL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS TXi_EMPTY flag.

12.2.3.4.6.3 End of Transfer Management

When the FIFO buffer is enabled for a channel, the user must previously configure in the MCSPI_XFERLEVEL register the AEL and AFL levels and especially the MCSPI_XFERLEVEL[31-16] WCNT bit field to define the number of MCSPI words to be transferred using the FIFO before enabling the channel.

This counter lets the controller stop the transfer correctly after a defined number of MCSPI word transfers. If WNCT is set to 0x0000, the counter is not used and the user must stop the transfer manually by disabling the channel; in this case, the user does not know how many MCSPI transfers have been done. For received words, software must poll the MCSPI_CH(i)STAT[5] RXFFE bit and read the MCSPI_RXi receive register to empty the FIFO buffer.

When the end-of-word count interrupt is generated (the MCSPI_IRQSTATUS[17] EOW bit is set), the user can disable the channel and poll the MCSPI_CH(i)STAT[5] RXFFE bit to know the last MCSPI words in the FIFO buffer and read them.

No new request is asserted as long as the system has not performed the correct number of write accesses.

12.2.3.4.6.4 Multiple MCSPI Word Access

The processor has the ability to perform multiple MCSPI word access to the receive or transmit registers within a single 32-bit interface access by setting the MCSPI_MODULCTRL[7] MOA to 1 under specific conditions:

- The channel selected has the FIFO enable.
- Only FIFO sense enabled support the kind of access.
- MCSPI_MODULCTRL[7] MOA is set to 1.
- Only 32-bit interface access and data width can be performed to receive or transmit registers, for other kind of access the processor must de-assert MCSPI_MODULCTRL[7] MOA bit.
- The level MCSPI_XFERLEVEL[7-0] AEL and MCSPI_XFERLEVEL[15-8] AFL must be 32-bit aligned, it means that AEL[0] = AEL[1] = 1 or AFL[0] = AFL[1] = 1.
- If MCSPI_XFERLEVEL[31-16] WCNT is used it must be configured according to MCSPI word length.
- The word length of MCSPI words allows to perform multiple MCSPI access, that means that MCSPI_CH(i)CONF[11-7] WL is <16.

The number of MCSPI word access depends on MCSPI word length:

- 3 ≤ WL ≤ 7, MCSPI word length smaller or equal to byte length, 4 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT), set the bit field to WCNT[0] = WCNT[1] = 0.
- 8 ≤ WL ≤ 15, MCSPI word length greater than byte or equal to 16-bit length, 2 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT]), set the bit field to WCNT[0] = 0.
- 16 ≤ WL Multiple MCSPI word access is not applicable.

12.2.3.4.6.5 First MCSPI Word Delay

Figure 12-82 shows the MCSPI controller ability to delay the first MCSPI word transfer to give time for system to complete some parallel processes or fill the FIFO in order to improve transfer bandwidth. This delay is applied only on first MCSPI word after MCSPI channel enabled and first write in transmit register. It is based on output clock frequency.

This option is meaningful in controller mode and single channel mode asserted through MCSPI_MODULCTRL[0] SINGLE.

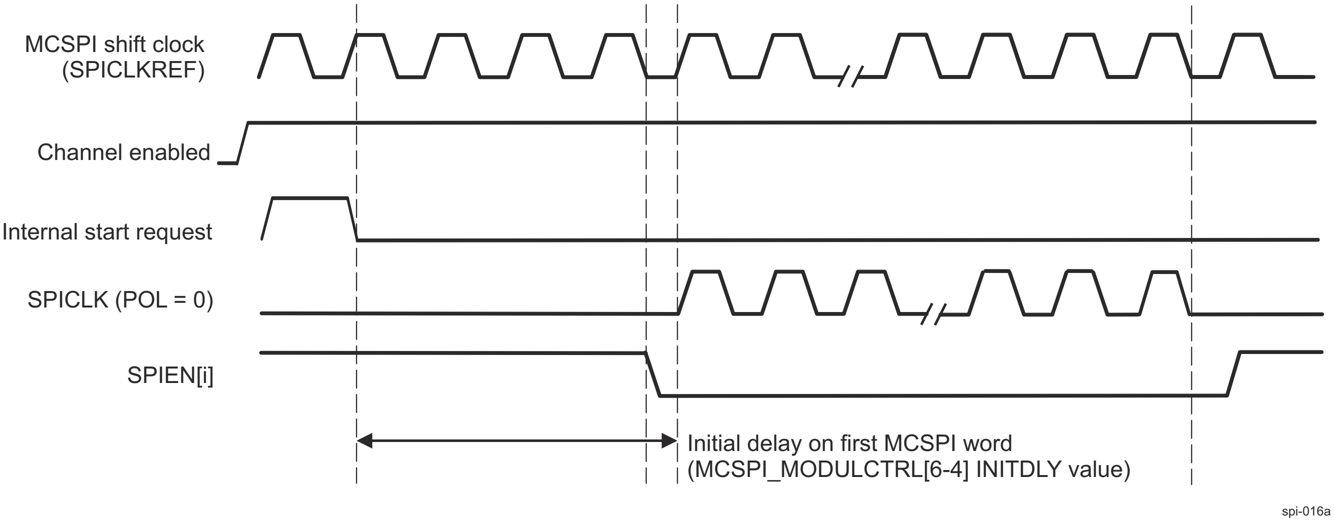

Figure 12-82. Controller Single Channel Initial Delay

Few delay values are available: No delay, 4/8/16/32 MCSPI cycles.

Its accuracy is half cycle in clock bypass mode and depends on clock polarity and phase.

12.2.3.4.7 MCSPI Interrupts

Each channel can issue interrupt events.

Each interrupt event has status bits in the MCSPI_IRQSTATUS register (RXi_FULL, TXi_UNDERFLOW, TXi_EMPTY, etc.) (where x = 0, 3) that indicate whether service is required. Each status bit has an interrupt enable bit (a mask) in the MCSPI_IRQENABLE register (RXi_FULL_ENABLE, TXi_UNDERFLOW_ENABLE, TXi_EMPTY_ENABLE, etc.).

When an interrupt occurs and a mask is later applied on it, the interrupt line is not asserted again, even if the interrupt source is not serviced.

The MCSPI supports interrupt-driven and polling operations.

12.2.3.4.7.1 Interrupt Events in Controller Mode

In controller mode, the interrupt events related to the state of the MCSPI_TXi register are TXi_EMPTY and TXi_UNDERFLOW. The interrupt event related to the state of the MCSPI_RXi register is RXi_FULL.

12.2.3.4.7.1.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXi register is empty (transient event). Enabling a channel automatically triggers this event, except in controller receive-only mode (see Section 12.2.3.4.3.4 , *Controller Receive-Only Mode*). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[27] FFEW bit is set to 1), the MCSPI_IRQSTATUS TXi_EMPTY bit is set as soon as there is enough space in the buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TXi register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXi_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXi_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TXi register defined by the MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.2.3.4.7.1.2 TXx_UNDERFLOW

The event TXx_UNDERFLOW is activated when the channel is enabled and if the MCSPI_TXi register or the FIFO is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

The TXi_UNDERFLOW is a harmless warning in controller mode.

To avoid having a TXi_UNDERFLOW event at the beginning of a transmission, the TXi_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXi register, because the channel is enabled. To avoid having a TXx_UNDERFLOW event, the MCSPI_TXi register must seldom be loaded.

The MCSPI_IRQSTATUS TXi_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.1.3 RXx_ FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXi register becomes filled (transient event). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[28] FFER bit is set to 1), RXi_ FULL is asserted as soon as the number of bytes held in the FIFO to be read reaches the MCSPI_XFERLEVEL[13-8] AFL threshold.

The MCSPI_RXi register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXi_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXi_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RXi. The processor must perform the correct number of reads.

12.2.3.4.7.1.4 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as MCSPI_XFERLEVEL[31-16] WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2 Interrupt Events in Peripheral Mode

In peripheral mode, the interrupt events related to the state of the MCSPI_TXi register are TX0_EMPTY and TX0_UNDERFLOW. The interrupt events related to the state of the MCSPI_RXi are RX0_FULL and RX0_OVERFLOW (channels 1, 2, and 3 do not have a receiver overflow status bit). See the MCSPI_IRQSTATUS register.

12.2.3.4.7.2.1 TXx_EMPTY

The TXi_EMPTY event is activated when a channel is enabled and its MCSPI_TXi register is empty. Enabling the channel automatically raises this event. If the FIFO buffer is enabled (the MCSPI_CH(i)CONF[27] FFEW bit is set to 1), the TXx_EMPTY event is asserted as soon as there is enough space in buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TXi register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXi_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXi_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TXi register defined by MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.2.3.4.7.2.2 TXx_UNDERFLOW

The TXx_UNDERFLOW event is activated when a channel is enabled and if the MCSPI_TXi register is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

When FIFO is enabled, the data emitted while the underflow event is raised is not the last data written in the FIFO but the next data in the FIFO (an old transmitted value or a dummy data in the FIFO has been reset).

TXx_UNDERFLOW indicates an error (data loss) in peripheral mode.

To avoid having a TXi_UNDERFLOW event at the beginning of a transmission, the TXi_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXi register because the channel is enabled.

The MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2.3 RXx_FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXi register is being filled (transient event). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[28] FFER bit is set to 1), RXi_FULL is asserted as soon as the number of bytes held in the buffer to read defined by the MCSPI_XFERLEVEL[13-8] AFL bit field.

The MCSPI_RXi register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXi_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXi_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RXi. The processor must perform the correct number of reads.

12.2.3.4.7.2.4 RX0_OVERFLOW

The RX0_OVERFLOW event is activated in peripheral mode in transmit-and-receive mode or receive-only mode when a channel is enabled and the MCSPI_RXi register or FIFO is full when a h MCSPI word is received. The MCSPI_RXi register is always overwritten with the new MCSPI word. If the FIFO is enabled, data within the FIFO are overwritten; it must be considered as corrupted. The RX0_OVERFLOW event should not appear in peripheral mode using the FIFO.

The RX0_OVERFLOW event indicates an error (data loss) in peripheral mode.

The MCSPI_IRQSTATUS[3] RX0_OVERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2.5 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.3 Interrupt-Driven Operation

An interrupt enable bit in the MCSPI_IRQENABLE register can be set to enable each event to generate interrupt requests when the corresponding event occurs. Status bits are automatically set by hardware logic conditions.

When an event occurs (the single interrupt line is asserted), the processor must:

1. Read the MCSPI_IRQSTATUS register to identify which event occurred.
2. Read the MCSPI_RXi register that corresponds to the event to remove the source of an RXi_FULL event or write into the MCSPI_TXi register that corresponds to the event to remove the source of a TXi_EMPTY event. No action is required to remove the source of the TXi_ UNDERFLOW and RX0_OVERFLOW events.
3. Set the corresponding bit of the MCSPI_IRQSTATUS register to 1 to clear an interrupt status and then release the interrupt line.

The interrupt status bit must always be reset after channel enabling and before events are enabled as interrupt sources.

12.2.3.4.7.4 Polling

When the interrupt capability of an event is disabled in the MCSPI_IRQENABLE register, the interrupt line is not asserted, but the status bits in the MCSPI_IRQSTATUS register can be polled by software to detect when the corresponding event occurs.

Once the expected event occurs:

- RXx_FULL: To remove the source of the event, the processor must read the corresponding MCSPI_RXi register.
- TXx_EMPTY: To remove the source of the event, the processor must write into the corresponding MCSPI_TXi register.
- TXx_UNDERFLOW and RX0_OVERFLOW: No action is required to remove the source of the event.

To clear an interrupt, set the corresponding status bit of the MCSPI_IRQSTATUS register to 1. This does not affect the interrupt line state.

12.2.3.4.8 MCSPI DMA Requests

Each MCSPI channel, if enabled, can issue DMA requests. There are two DMA request lines per MCSPI channel (one for read and one for write).

The DMA read request line is asserted when the MCSPI channel is enabled and new data is available in the receive register of the MCSPI channel. A DMA read request can be individually masked with the MCSPI_CH(i)CONF[15] DMAR bit. The DMA read request line is de-asserted when reading of the MCSPI_RXi register of the MCSPI channel completes.

The DMA write request line is asserted when the MCSPI channel is enabled and the MCSPI_TXi register of the MCSPI channel is empty. A DMA write request can be individually masked with the MCSPI_CH(i)CONF[14] DMAW bit. The DMA write request line is de-asserted when loading of the MCSPI_TXi register of the channel completes.

12.2.3.4.9 MCSPI Power Saving Management

Power consumption can be optimized by switching off internal clocks (interface and functional clock) when there is no activity.

12.2.3.4.9.1 Normal Mode

In normal mode, internal MCSPI module clocks are automatically switched off (autogated) when there is no activity in peripheral or controller mode.

Autogating of the module interface clock and functional clock occurs when the following conditions are met:

- The MCSPI_SYSCONFIG[0] AUTOIDLE bit is set.
- In controller mode, there is no data to transmit or receive in all channels.
- In peripheral mode, the MCSPI is not selected by the external controller and there are no register accesses.

Autogating of the module interface clock and functional clock stops when the following conditions are met:

- In controller mode, an internal access occurs.
- In peripheral mode, an internal access occurs or the MCSPI is selected by the external controller.

12.2.3.4.9.2 Idle Mode

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

At the power management level, when all conditions to shut off the MCSPI_FCLK or MCSPI_ICLK clocks are met, the corresponding LPSC asserts a clock stop request to the MCSPI. Although this procedure is completely hardware-oriented and out of software control, the method in which the MCSPI module acknowledges the clock stop request can be configured through the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field.

The settings of the SIDLEMODE bit field and the related acknowledgement modes are:

- Force-idle mode (the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0): The MCSPI module acknowledges unconditionally the clock stop request, regardless of its internal operations. This mode must be used carefully in this case because it does not prevent the loss of data when the clock is switched off.
- No-idle mode (the SIDLEMODE bit field is set to 0x1): The MCSPI never acknowledges the clock stop request and is safe from a module point of view because it ensures that the clocks remain active. However, it is not efficient to save power because it does not allow shut off of MCSPI_FCLK and MCSPI_ICLK.
- Smart-idle mode (the SIDLEMODE bit field is set to 0x2): The MCSPI acknowledges the clock stop request, depending on its internal activity. MCSPI acknowledges the shut off of MCSPI_FCLK and MCSPI_ICLK only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for efficient system power management.

When configured in smart-idle mode, the MCSPI also offers an additional feature to control gating of MCSPI_FCLK or MCSPI_ICLK. The MCSPI_SYSCONFIG[9-8] CLOCKACTIVITY bit field determines which clock shuts down (MCSPI_FCLK, MCSPI_ICLK, neither clock, or both clocks).

The setting of the CLOCKACTIVITY bit field is used internally to the MCSPI to determine on which part of the module the conditions to acknowledge the clock stop request are tested. For example, if MCSPI_FCLK is not shut off on clock stop request, the MCSPI considers only MCSPI_ICLK and the associated pending activities before acknowledging the request.

Some MCSPI features are associated with MCSPI_ICLK and others with MCSPI_FCLK. Using the CLOCKACTIVITY bit field with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if MCSPI acknowledges the clock stop request.

12.2.3.4.9.2.1 Force-Idle Mode

Force-idle mode is enabled and exited as follows:

- Force-idle mode is enabled when the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0.
    - In force-idle mode, the MCSPI responds unconditionally to the clock stop request by de-asserting unconditionally the interrupt and DMA request lines, if asserted.
    - The transition from normal mode to idle mode does not affect the interrupt event bits of the MCSPI_IRQSTATUS register.
    - In force-idle mode, because the module must be disabled, the interrupt and DMA request lines are likely de-asserted. The interface clock and MCSPI clock provided to the MCSPI can be switched off.
    - A clock stop request during an MCSPI data transfer can lead to an unexpected and unpredictable result. Software must avoid such a request.

12.2.3.5 MCSPI Programming Guide

This section describes the low-level hardware programming sequences for the configuration and use of the MCSPI module.

12.2.3.5.1 MCSPI Global Initialization

12.2.3.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCSPI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCSPI. For further information, see *MCSPI Integration* and *MCSPI Environment*.

Table 12-57 lists the information on the global initialization of the surrounding modules.

Table 12-57. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts and if this applicable, see *Interrupts*.
MCU_M4FSS0_CORE0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_M4FSS0_CORE0 interrupts and if this is applicable, see *Interrupts*.
R5FSS0/1_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0/1_CORE0/1 interrupts and if this is applicable, see *Interrupts*.
PRUSS	Device INTCs must be configured to enable the interrupt request generation. For information about enabling PRUSS interrupts and if this is applicable, see *Interrupts*.
PDMA0 and PDMA1	Device INTCs must be configured to enable the interrupt request generation.
MCU_PLLCTRL0 and PLLCTRL0	PLL controller's configuration must be done to enable the module clocks. For more information, see *Clocking*.

12.2.3.5.1.2 MCSPI Global Initialization

12.2.3.5.1.2.1 Main Sequence – MCSPI Global Initialization

The procedure in Table 12-58 can be used to initialize MCSPI when performing software reset.

Table 12-58. MCSPI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	MCSPI_SYSCONFIG[1] SOFTRESET	1
Wait until reset is finished?	MCSPI_SYSSTATUS[0] RESETDONE	=1
Configure static settings (such as SPI controller or peripheral) as required.	MCSPI_MODULCTRL[8-0]	0x-
Write MCSPI_SYSCONFIG	MCSPI_SYSCONFIG	0x-

12.2.3.5.2 MCSPI Operational Mode Configuration

12.2.3.5.2.1 MCSPI Operational Modes

The selection of the working mode is done with the MCSPI_CH(i)CONF register.

Table 12-59. MCSPI Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set receive mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x1
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-60. MCSPI Transmit Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x2

Table 12-60. MCSPI Transmit Mode Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-61. MCSPI Transmit-and-Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit and receive mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x0
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

12.2.3.5.2.1.1 Common Transfer Sequence

MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: Interrupts, DMA
- SPIEN_[n] lines assertion/deassertion: automatic, manual

For all these sequences, the host process contains the main process and the interrupt routines.

The interrupt routines are called on the interrupt signals or by an internal call if the module is used in polling mode.

Table 12-62 represents the main sequence which is common to all transfers.

In multi-channel controller mode, the sequences of different channels can be run simultaneously.

Table 12-62. Common Transfer Sequence (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	0x-
Write MCSPI_CH(i)CONF to configure the channel	MCSPI_CH(i)CONF	0x-
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait for the first write request (TX empty or DMA write)		
Write the transmitter register with data	MCSPI_TXi	0x-
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.2 End of Transfer Sequences

The end of transfer depends on the transfer mode. Table 12-63 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-63. End of Transfer Sequences

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	**DMA**	**INTERRUPT**	**DMA**	**INTERRUPT**	**DMA**
CONTROLLER Normal	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.5.1	See Section 12.2.3.5.2.1.5.2
	Minimum number of word	1	1	1	1	1	2
	DMA transfer size		N		N		N-1

Table 12-63. End of Transfer Sequences (continued)

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	DMA	INTERRUPT	DMA	INTERRUPT	DMA
CONTROLLER Turbo	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.6.1	See Section 12.2.3.5.2.1.6.2
	Minimum number of word	1	1	1	1	2	3
	DMA transfer size		N		N		N-2
PERIPHERAL	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.7	
	Minimum number of word	1	1	1	1	1	1
	DMA transfer size		N		N	N	N

The transfer to execute has a size of N words.

The different sequences can be merged in one process to manage transfers of several types. The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = 0
- read_count = 0
- channel_enable = FALSE
- last_transfer = FALSE
- last_request = FALSE

They are initialized before starting the channel.

12.2.3.5.2.1.3 Transmit-and-Receive (Controller and Peripheral)

If the requests are configured in DMA, write_count and read_count are assigned with 'N' when the DMA handlers have completed their 'N' CBASS0 accesses.

Table 12-64. Transmit-and-Receive (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait for write_count = N **AND** read_count = N		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-65. Transmit-and-Receive (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXi_EMPTY		
Write the transmitter register with data	MCSPI_TXi	0x-
Increment write_count +1		
IF: RXi_FULL		
Read the receiver register	MCSPI_RXi	
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.4 Transmit-Only (Controller and Peripheral)

12.2.3.5.2.1.4.1 Based on Interrupt Requests

Table 12-66. Transmit-Only With Interrupts (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until last transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-67. Transmit-Only With Interrupts (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXx_EMPTY **AND** write_count < N		
Write the transmitter register with data	MCSPI_TXi	0x-
Increment write_count +1		
ELSEIF: write_count ≥ N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.4.2 Based on DMA Write Requests

When the DMA handler has completed its ‘N’ CBASS0 accesses, write_count is assigned with ‘N’.

Table 12-68. Transmit-Only With DMA (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until write_count = N		
Disable DMA write request	MCSPI_CH(i)CONF[14] DMAW	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-69. Transmit-Only With DMA (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXi_EMPTY **AND** write_count = N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.5 Controller Normal Receive-Only

12.2.3.5.2.1.5.1 Based on Interrupt Requests

Table 12-70. Receive-Only With Interrupt (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until last_request = TRUE		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register	MCSPI_RXi	0x-

Table 12-70. Receive-Only With Interrupt (Controller Normal) (Main Process) (continued)

Step	Register/Bit Field/Programming Model	Value
Increment read_count +1		

Table 12-71. Receive-Only With Interrupt (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL **AND** read_count = N - 1		
last_request = TRUE		
ELSEIF: read_count ≠ N - 1		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.5.2 Based on DMA Read Requests

When the DMA handler has completed its ‘N-1’ CBASS0 accesses, read_count is assigned with ‘N-1’.

Table 12-72. Receive-Only With DMA (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until read_count = N - 1		
Disable DMA read request	MCSPI_CH(i)CONF[15] DMAR	0
Wait until last_transfer = TRUE		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		

Table 12-73. Receive-Only With DMA (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL **AND** read_count = N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.6 Controller Turbo Receive-Only

12.2.3.5.2.1.6.1 Based on Interrupt Requests

Table 12-74. Receive-Only With Interrupt (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until channel_enable = TRUE		
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Wait until channel_enable = FALSE		

Table 12-75. Receive-Only With Interrupt (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		
Wait until channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.2.3.5.2.1.6.2 Based on DMA Read Requests

When the DMA handler has completed its ‘N-2’ CBASS0 accesses read_count is assigned with ‘N-2‘.

Table 12-76. Receive-Only With DMA (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until channel_enable = TRUE		
Wait until read_count = TRUE		
Disable DMA read request	MCSPI_CH(i)CONF[15] DMAR	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Wait until channel_enable = FALSE		

Table 12-77. Receive-Only With DMA (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		
Wait until channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.2.3.5.2.1.7 Peripheral Receive-Only

If the requests are configured in DMA, read_count is assigned with ‘N’ when the DMA handler has completed its ‘N‘ CBASS0 accesses.

Table 12-78. Receive-Only (Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until read_count = N		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-79. Receive-Only (Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.8 Transfer Procedures With FIFO

These flows describe the transfer with FIFO.

The MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: IRQ, DMA

For all these flows, the host process contains the main process and the interrupt routine. This routine is called on the IRQ signals or by an internal call if the module is used in polling mode.

For more information, see Section 12.2.3.4.6 , *MCSPI FIFO Buffer Management*.

Table 12-80. FIFO Mode Common Sequence (Controller) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS	1
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	1
Write MCSPI_CH(i)CONF to configure the channel	MCSPI_CH(i)CONF	0x-
Write MCSPI_XFERLEVEL	MCSPI_XFERLEVEL	0x-
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
IF: Receive only		
Wait for the write request (TX empty or DMA write)		
Write for the transmitter register with data	MCSPI_TXi	0x-
ENDIF		
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.8.1 Common Transfer Sequence in FIFO Mode

This flow describes the host sequence for a transfer of any type defined in Section 12.2.3.5.2.1.8 , *Transfer Procedures With FIFO*.

In multi-channel, only one channel can use the FIFO.

Before enabling the FIFO for a channel (MCSPI_CH(i)CONF[28] FFER and MCSPI_CH(i)CONF[27] FFEW bits), the host must check that the FIFO is not enabled for another channel, even if these channels are not used.

In transmit-and-receive mode, the FIFO can be enabled for write or read request only, without FIFO for the other request.

In Peripheral mode, the channel 0 only can be activated. The correct SPIEN line is chosen in MCSPI_CH0CONF[22-21] SPIENSLV bits.

The MCSPI module can start the transfer only when the first write request has been released by writing the MCSPI_TXi register, even in receive-only mode (only one write request occurs in this case).

12.2.3.5.2.1.8.2 End of Transfer Sequences in FIFO Mode

Table 12-81 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-81. End of Transfer Sequences in FIFO Mode

Word count	TRANSMIT AND RECEIVE	TRANSMIT-ONLY	RECEIVE-ONLY
Yes	See Figure 12-83	See Figure 12-85	See Figure 12-86
No	See Figure 12-84	See Figure 12-85	See Figure 12-87

The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = N
- read_count = N
- last_request = FALSE

They are initialized before starting the channel.

12.2.3.5.2.1.8.3 Transmit-and-Receive With Word Count

Figure 12-83 shows the flow of a transfer in transmit-and-receive mode, with word count.

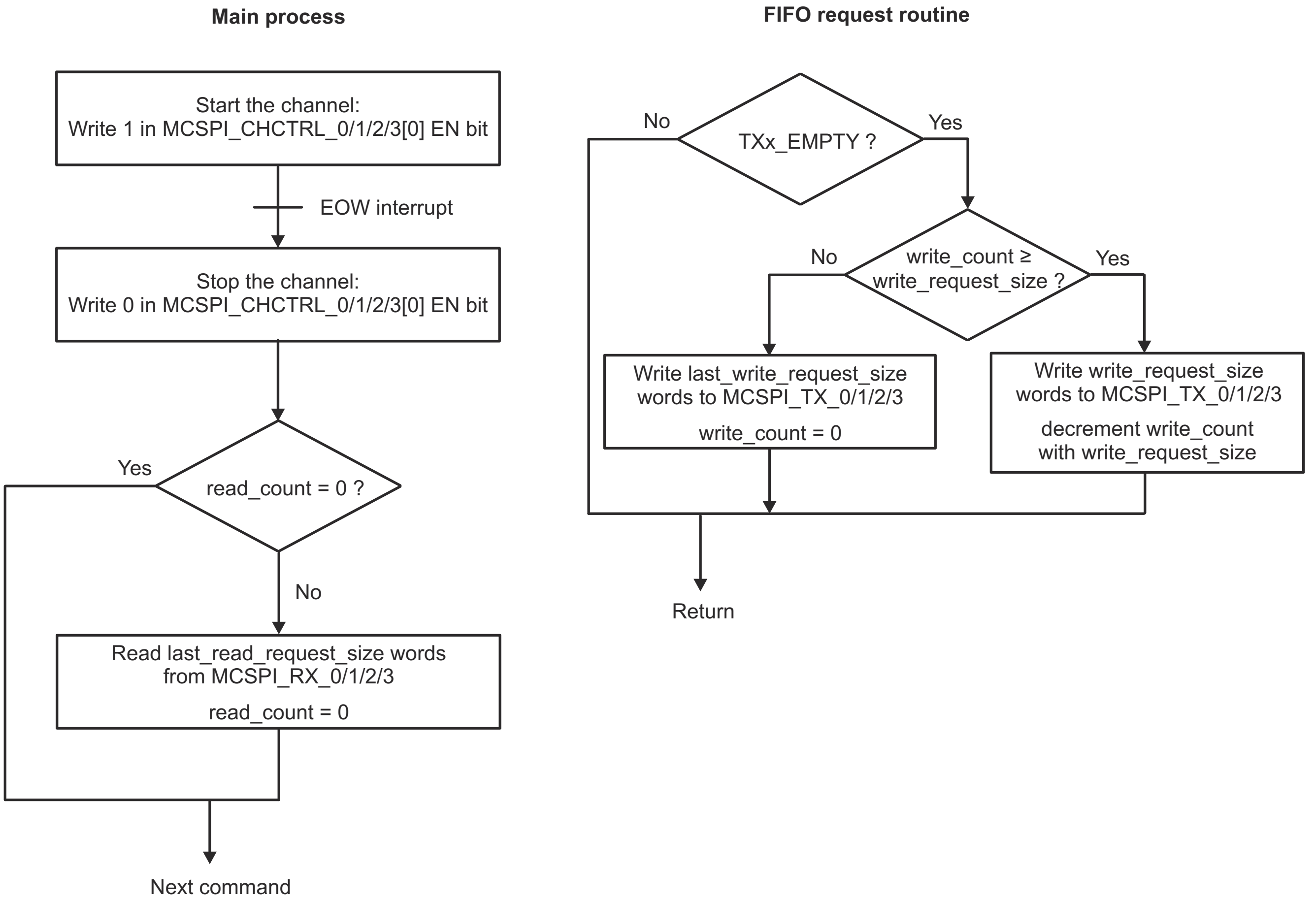

Figure 12-83. FIFO Mode Transmit-and-Receive With Word Count (Controller)

12.2.3.5.2.1.8.4 Transmit-and-Receive Without Word Count

Figure 12-84 shows the flow of a transfer in transmit-and-receive mode, without word count.

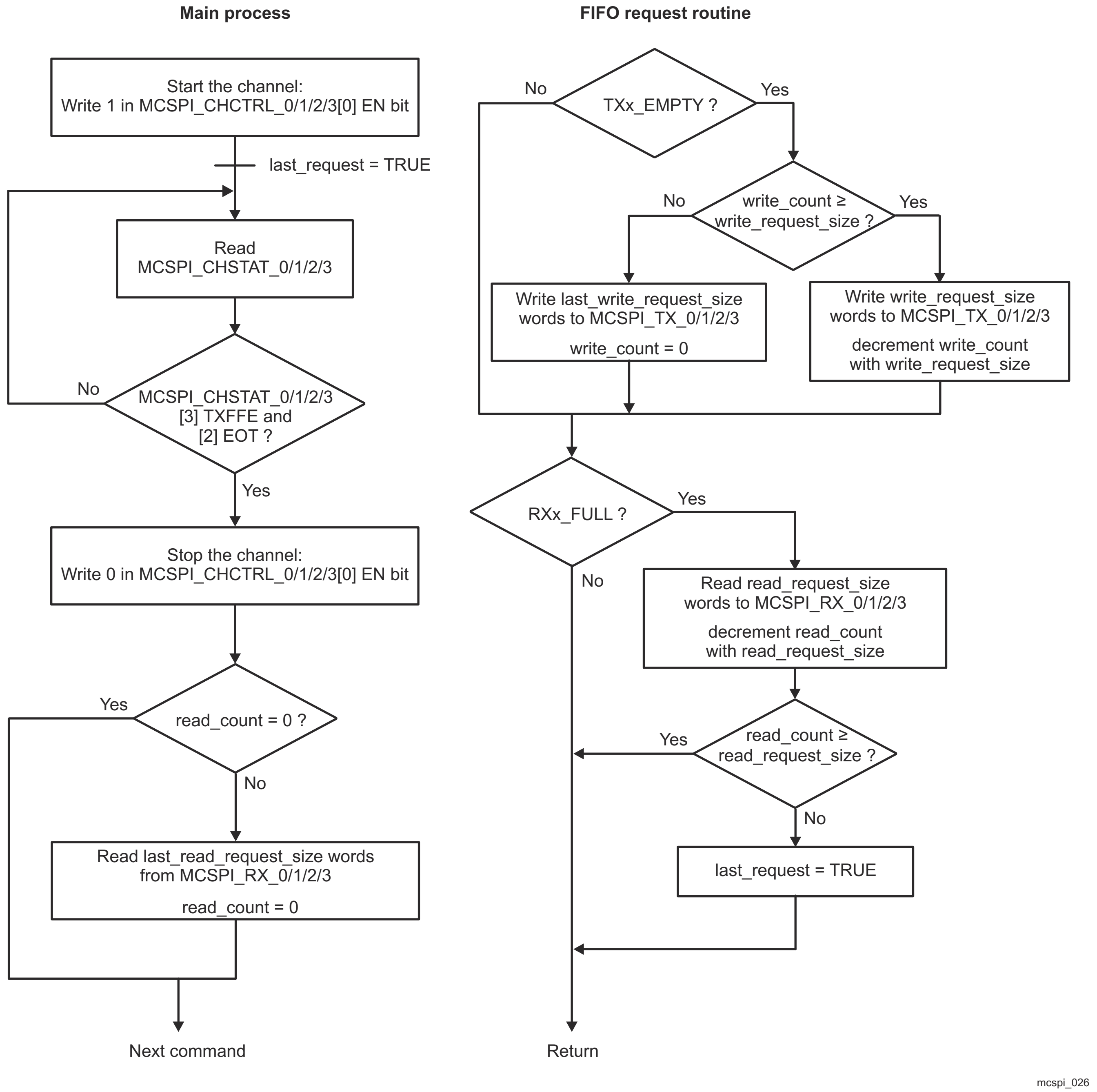

Figure 12-84. FIFO Mode Transmit-and-Receive Without Word Count (Controller)

12.2.3.5.2.1.8.5 Transmit-Only

Figure 12-85 shows the flow of a transfer in transmit-only mode, with or without word count. The difference between word count enabled or not is just on the condition after starting the channel:

- word count enable: wait for EOW interrupt
- word count disable: wait for write_count = 0

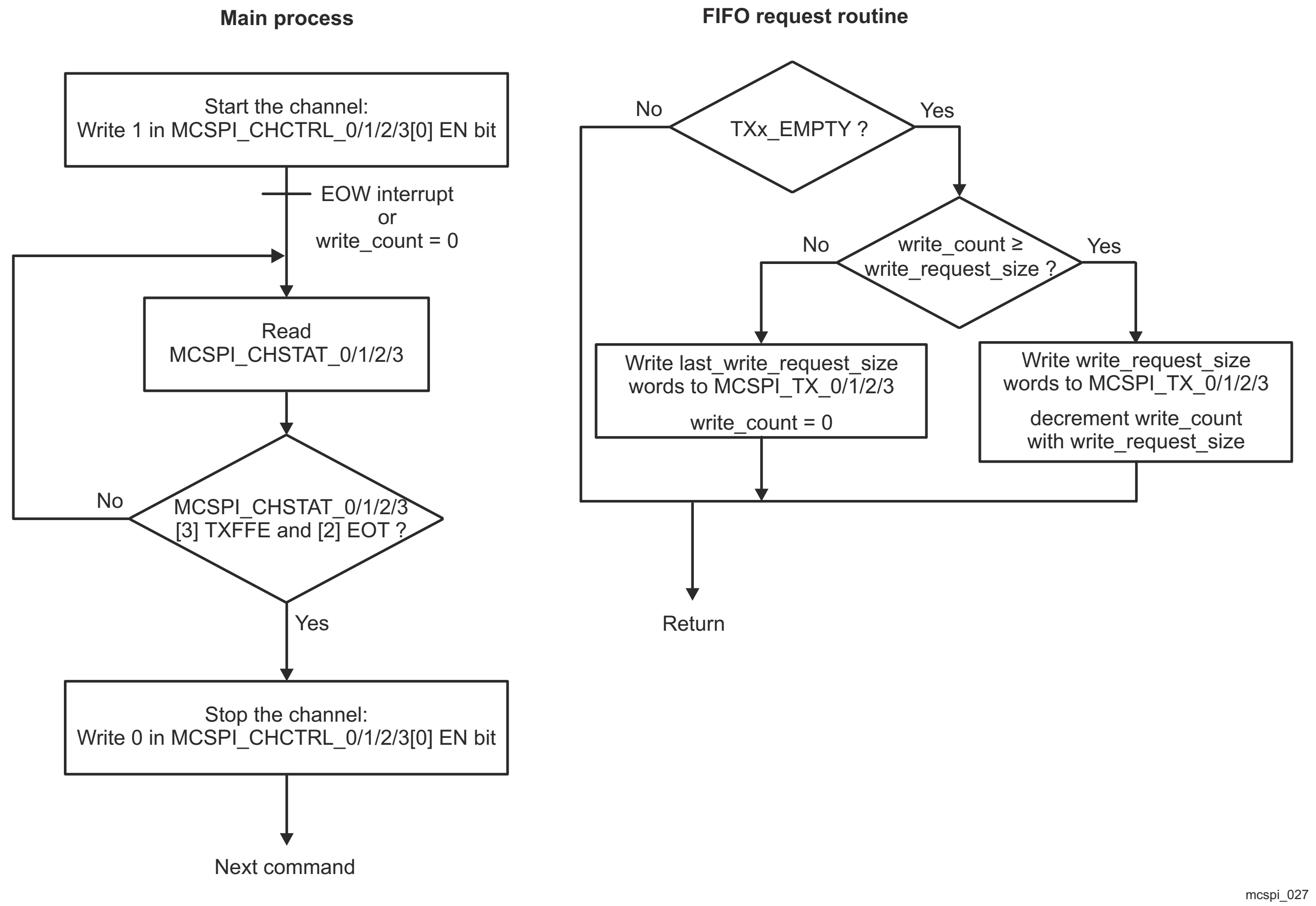

Figure 12-85. FIFO Mode Transmit-Only (Controller)

12.2.3.5.2.1.8.6 Receive-Only With Word Count

Figure 12-86 shows the flow of a transfer in receive-only mode, with word count.

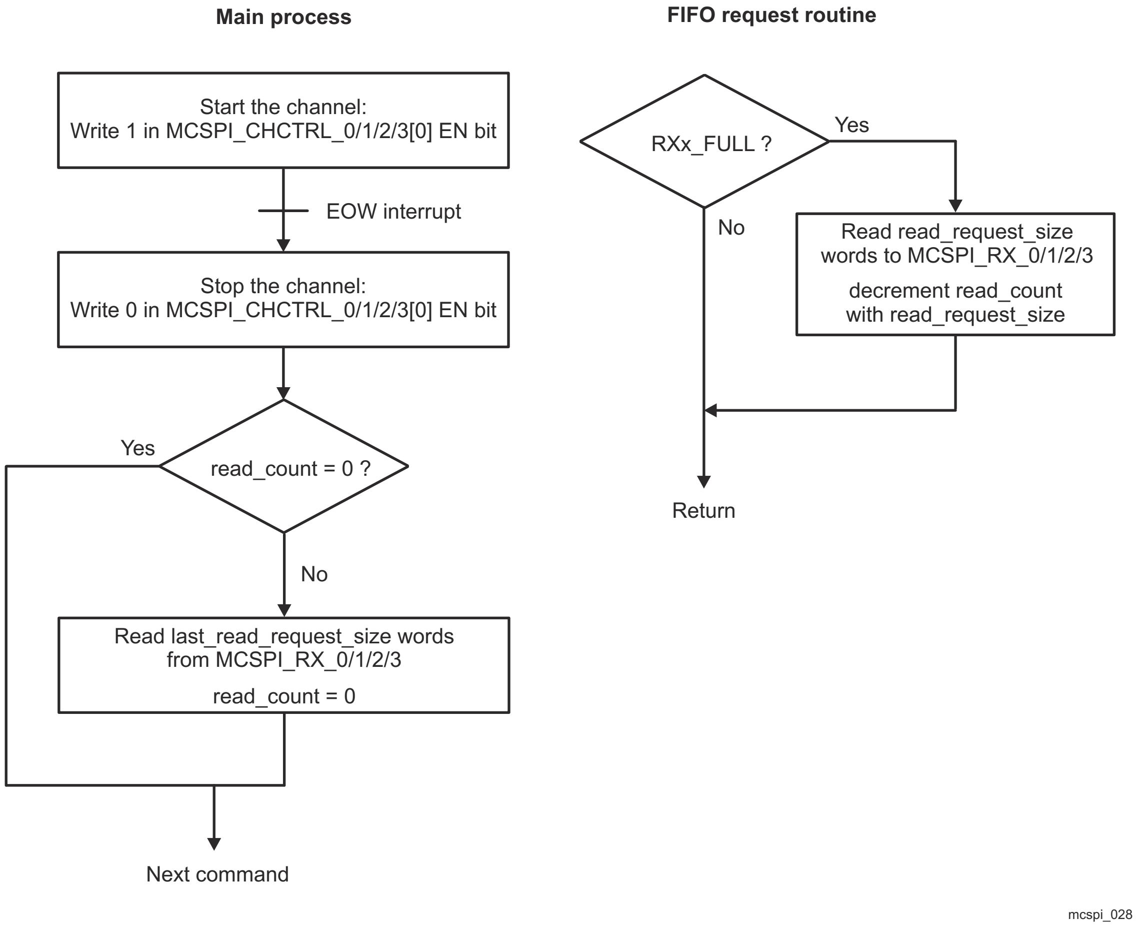

Figure 12-86. FIFO Mode Receive-Only With Word Count (Controller)

12.2.3.5.2.1.8.7 Receive-Only Without Word Count

Figure 12-87 shows the flow of a transfer in receive-only mode, with word count.

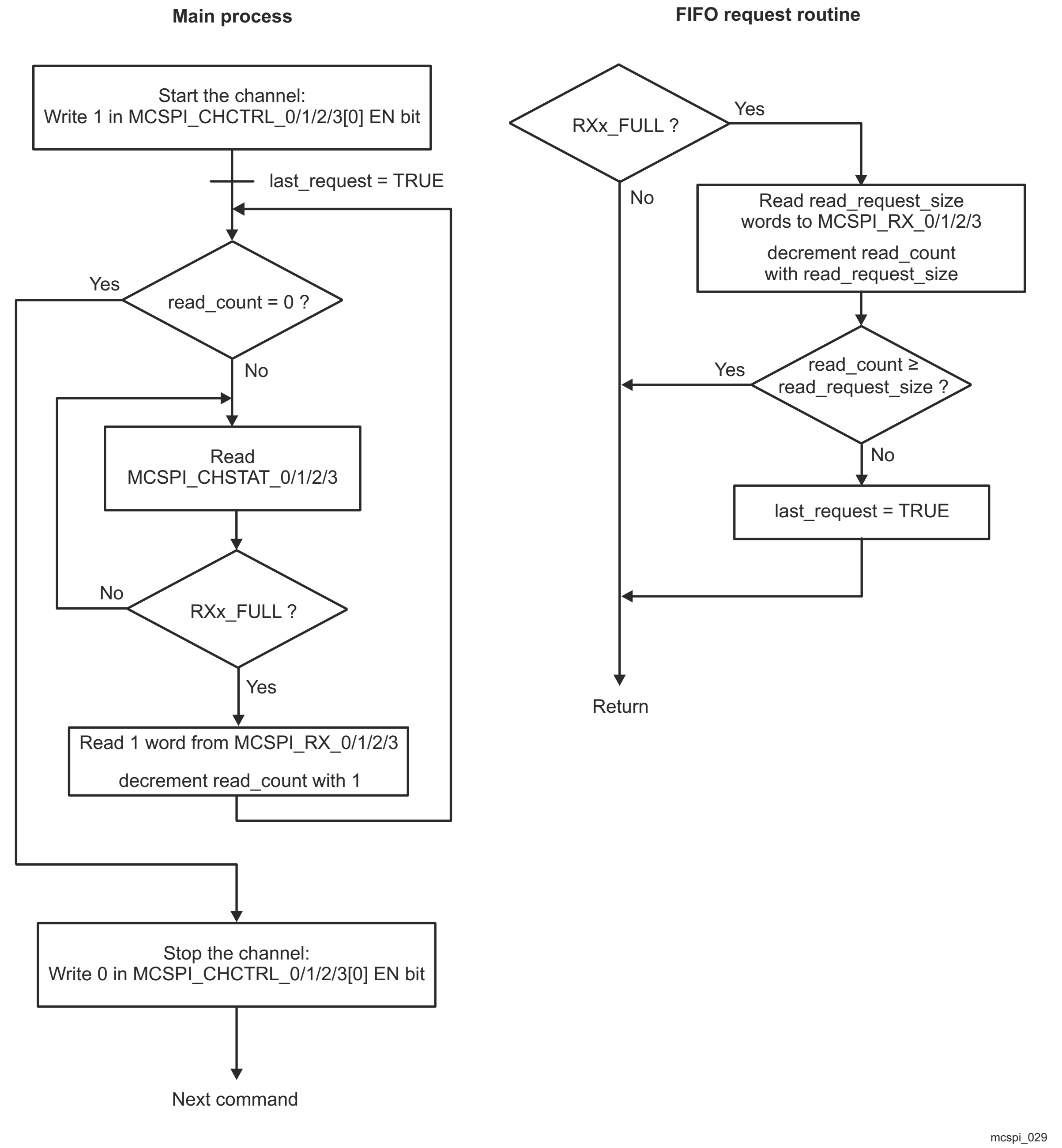

Figure 12-87. FIFO Mode Receive-Only Without Word Count (Controller)

12.2.3.5.2.1.9 Common Transfer Procedures Without FIFO – Polling Method

12.2.3.5.2.1.9.1 Receive-Only Procedure – Polling Method

Table 12-82 lists the receive-only procedure using the polling method.

Table 12-82. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-59.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Wait for end-of-transfer.	MCSPI_CH(i)STAT[2] EOT	=1
Read the receiver register.	MCSPI_RXi	0x-

Table 12-82. Receive-Only Procedure – Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.9.2 Receive-Only Procedure – Interrupt Method

Table 12-83 lists the receive-only procedure using the interrupt method.

Table 12-83. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-59.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Enable the interrupt for the receiver register.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	1
Wait for interrupt.		
Read the status register.	MCSPI_IRQSTATUS[2] RX_FULL	1
Disable the interrupt if no more data is expected.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.2.1.9.3 Transmit-Only Procedure – Polling Method

Table 12-84 lists the transmit-only procedure using the polling method.

Table 12-84. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-60.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until end of transfer?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.9.4 Transmit-and-Receive Procedure – Polling Method

Table 12-85 lists the transmit-and-receive procedure using the polling method.

Table 12-85. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-61.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until transmit/receive word?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.3 Common Transfer Procedures Without FIFO – Polling Method

12.2.3.5.3.1 Receive-Only Procedure – Polling Method

Table 12-86 lists the receive-only procedure using the polling method.

Table 12-86. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-59.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Wait for end-of-transfer.	MCSPI_CH(i)STAT[2] EOT	=1

Table 12-86. Receive-Only Procedure – Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
Read the receiver register.	MCSPI_RXi	0x-
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.3.2 Receive-Only Procedure – Interrupt Method

Table 12-87 lists the receive-only procedure using the interrupt method.

Table 12-87. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-59.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Enable the interrupt for the receiver register.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	1
Wait for interrupt.		
Read the status register.	MCSPI_IRQSTATUS[2] RX_FULL	1
Disable the interrupt if no more data is expected.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.3.3 Transmit-Only Procedure – Polling Method

Table 12-88 lists the transmit-only procedure using the polling method.

Table 12-88. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-60.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until end of transfer?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.3.4 Transmit-and-Receive Procedure – Polling Method

Table 12-89 lists the transmit-and-receive procedure using the polling method.

Table 12-89. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-61.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until transmit/receive word?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.4 Universal Asynchronous Receiver/Transmitter (UART)

This chapter describes the function, operation, and configuration of the Universal Asynchronous Receiver/Transmitter (UART)/RS-485/Infrared Data Association (IrDA)/Consumer Infrared (CIR) module in the device.

Note

UART and USART acronyms are used interchangeably in this section.

12.2.4.1 UART Overview

The UART is a peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

Figure 12-88 shows the UART modules overview.

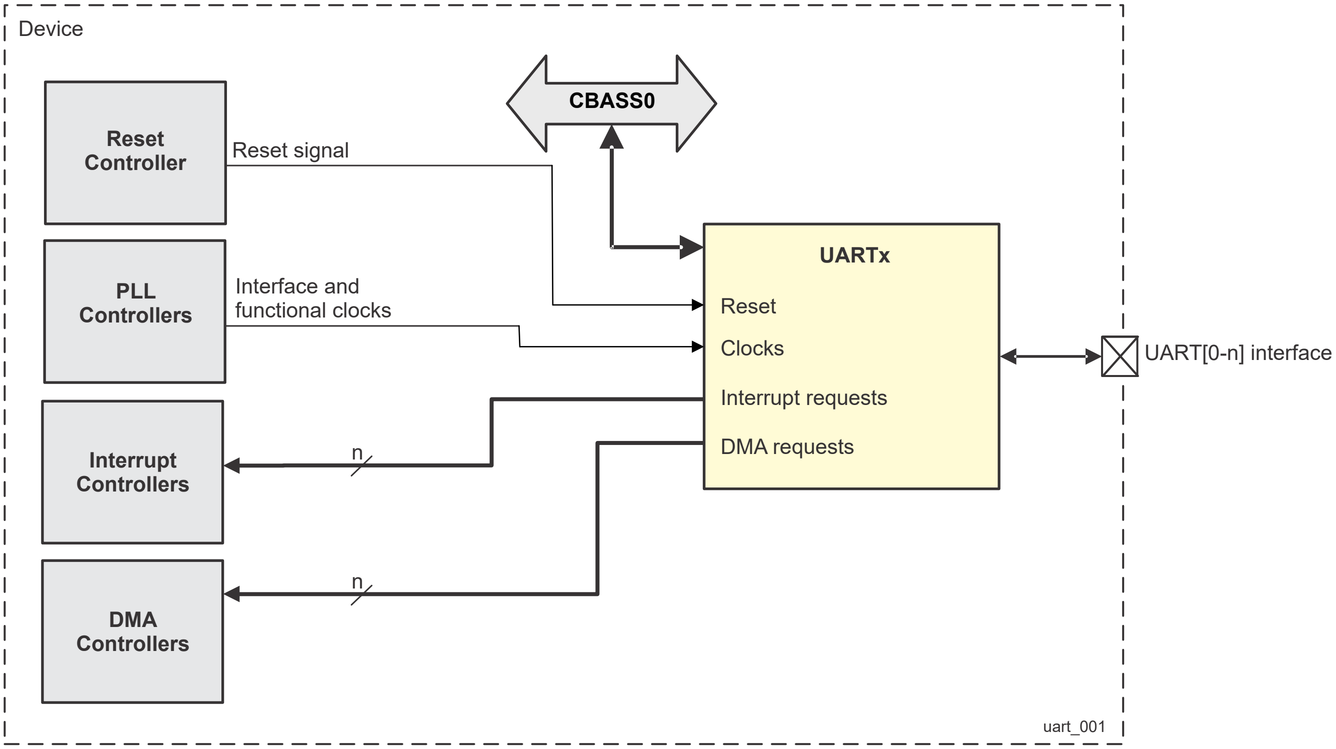

Note

x represents a valid instance of UART in a domain. See the device datasheet for specifics.

Note

n represents the maximum number of available UART signals -1.

Figure 12-88. UART Modules Overview

12.2.4.1.1 UART Features

The UART includes the following features:

- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter

- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature
- Configurable data format:
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS)
- UART0 module in MAIN domain has extended modem control signals (DCD, RI, DTR, DSR)

12.2.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.2.4.1.3 IrDA Features

The IrDA includes the following features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  - Slow infrared (SIR 115.2 KBAUD), medium infrared (MIR 0.576 MBAUD) and fast infrared (FIR 4.0 MBAUD) operations (very fast infrared (VFIR) is not supported)
  - Frame formatting: addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  - Uplink/downlink cyclic redundancy check (CRC) generation/detection
  - Asynchronous transparency (automatic insertion of break character)
  - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- IrDA mode when 48 MHz function clock is used

12.2.4.1.4 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR includes the following features to provide CIR support for remote-control applications:

- Transmit and receive mode
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle
- CIR mode when 48 MHz function clock is used

12.2.4.2 UART Environment

The , modules are hereinafter referred to as UART module.

This section describes the UART/RS-485/IrDA/CIR external connections (environment).

- The UART interface is described in Section 12.2.4.2.1 , *UART Functional Interfaces*.
- The RS-485 interface is described in Section 12.2.4.2.2 , *RS-485 Functional Interfaces*.
- The IrDA interface is described in Section 12.2.4.2.3 , *IrDA Functional Interfaces*.
- The CIR interface is described in Section 12.2.4.2.4 , *CIR Functional Interfaces*.

12.2.4.2.1 UART Functional Interfaces

12.2.4.2.1.1 System Using UART Communication With Hardware Handshake

Each UART instance can be easily connected to the UART port of an external IC (see Figure 12-89).

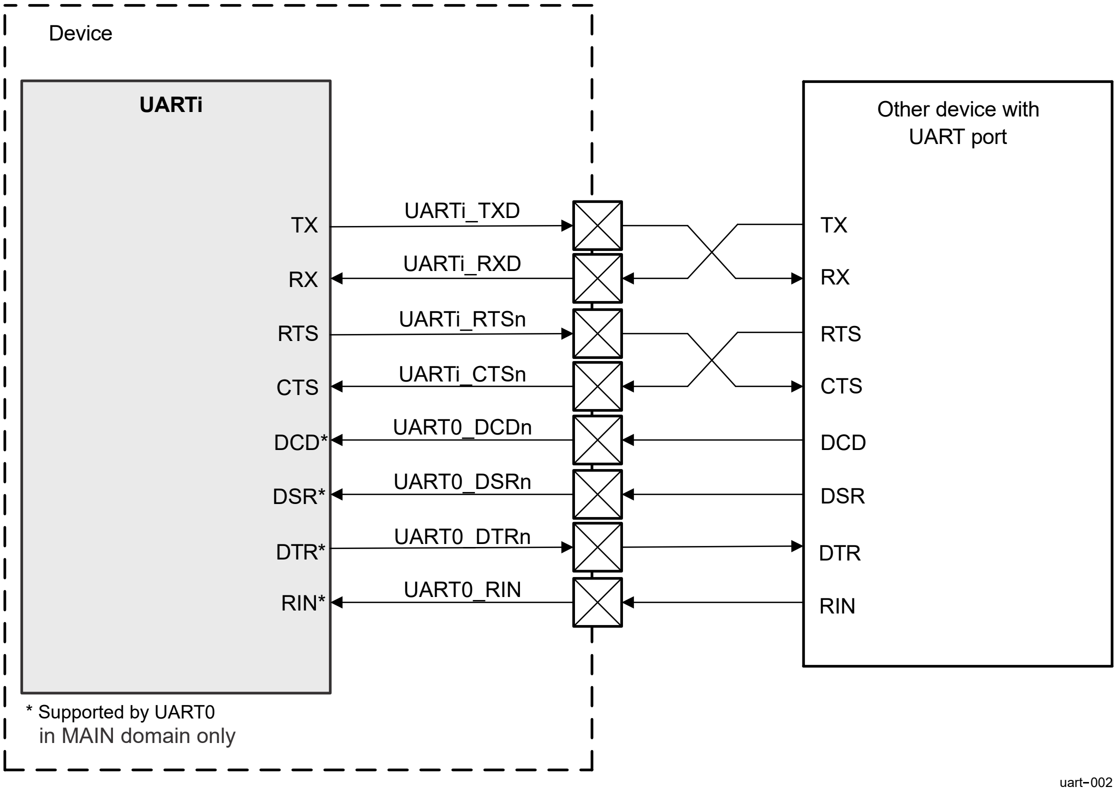

Note

i represents a valid instance of UART in a domain. See the device datasheet for valid domains and instances.

Figure 12-89. UART Mode Interface Signals

12.2.4.2.1.2 UART Interface Description

Table 12-90 lists the UART interface input/output (I/O) signals.

Table 12-90. UART I/O Signals

Module Pin Name	Device Level Signal Name	I/O(1)	Description	Module Pin Reset Value(2)
		WKUP_UARTi(10)		
RX	WKUP_UARTi(10)_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi(10)_TXD	O	Serial data output(3)	1
CTS	WKUP_UARTi(10)_CTSn	I	Clear to send(4)	HiZ
RTS	WKUP_UARTi(10)_RTSn	O	Request to send(5)	1
		MCU_UARTi(10)		
RX	MCU_UARTi(10)_RXD	I	Serial data input	HiZ
TX	MCU_UARTi(10)_TXD	O	Serial data output(3)	1
CTS	MCU_UARTi(10)_CTSn	I	Clear to send(4)	HiZ
RTS	MCU_UARTi(10)_RTSn	O	Request to send(5)	1
		UARTi(10) Modem Signals		
RX	UARTi(10)_RX	I	Serial data input	HiZ
TX	UARTi(10)_TX	O	Serial data output(3)	1
CTS	UARTi(10)_CTSn	I	Clear to send(4)	HiZ
RTS	UARTi(10)_RTSn	O	Request to send(5)	1
DCD	UARTi(10)_DCDn	I	Data Carrier Detect(6)	HiZ
DSR	UARTi(10)_DSRn	I	Data Set Ready(7)	HiZ
DTR	UARTi(10)_DTRn	O	Data Terminal Ready(8)	1
RIN	UARTi(10)_RIN	I	Ring Indicator(9)	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Because this pin is active high in IrDA mode and the output is muxed, this pin is set to low on reset (when the UART_MDR1[2-0] bit field is set to 0x7) and takes the defined inactive level of that signal corresponding to when and how the UART_MDR1 register is programmed; that is, the output is 1 (inactive for UART modem modes) and 0 (inactive for IrDA modes).

(4) Active-low modem status signal. Reading the UART_MSR[4] NCTS_STS bit checks the condition of CTS. Reading the UART_MSR[0] CTS_STS bit checks a change of state of CTS since the last read of the modem status register. The auto-CTS mode uses CTS to control the transmitter.

(5) When active (low), the module is ready to receive data. Setting the UART_MCR[1] RTS bit activates RTS signal, which becomes inactive as the result of a module reset, loopback mode, or clearing the UART_MCR[1] RTS bit. In auto-RTS mode, RTS signal becomes inactive as a result of the receiver threshold logic.

(6) Active-low modem status signal. The condition of DCD can be checked by reading the UART_MSR[7] NCD_STS bit. Any change in its state can be detected by reading the UART_MSR[3] DCD_STS bit.

(7) Active-low modem status signal. Reading the UART_MSR[5] NDSR_STS bit checks the condition of DSR. Reading the UART_MSR[1] DSR_STS bit checks a change of state of DSR since the last read of the UART_MSR register.

(8) When active (low), this signal informs the modem that the module is ready to communicate. It is activated by setting the UART_MCR[0] DTR bit.

(9) Active-low modem status signal. The condition of RIN can be checked by reading the UART_MSR[6] NRI_STS bit. Any change in its state can be detected by reading the UART_MSR[2] RI_STS bit.

(10) i represents a UART instance. See the device datasheet for available domains and UART instances.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.1.3 UART Protocol and Data Format

The UART device operates in three modes:

- UART 16× (<= 230.4 kbps)
- UART 16× with autobauding (>= 1200 bps and <= 115.2 kbps)
- UART 13× (>= 460.8 kbps)

CAUTION

To be used as a UART, the operating mode must be programmed appropriately in the UART_MDR1[2-0] MODE_SELECT bit field to select UART, IrDA, or CIR mode, and the UART_MDR3[4] DIR_EN bit field to select RS-485 mode.

The UART uses a wired interface for serial communication with a remote device.

The UART is functionally compatible with the TL16C750 UART and earlier designs such as the TL16C550.

Figure 12-90 shows the UART frame data format.

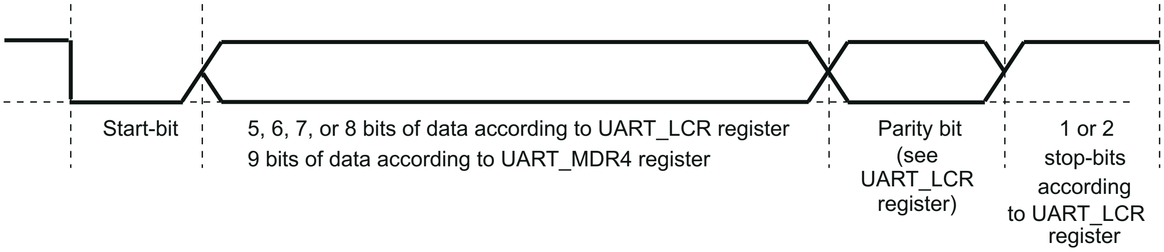

Figure 12-90. UART Frame Data Format

12.2.4.2.2 RS-485 Functional Interfaces

12.2.4.2.2.1 System Using RS-485 Communication

The RS-485 network physical layer consists of two-wire differential bus, usually twisted pair. External RS-485 transceiver IC is needed to access a RS-485 bus by the RS-485 mode. Figure 12-91 shows an example connection of an UART instance in RS-485 mode.

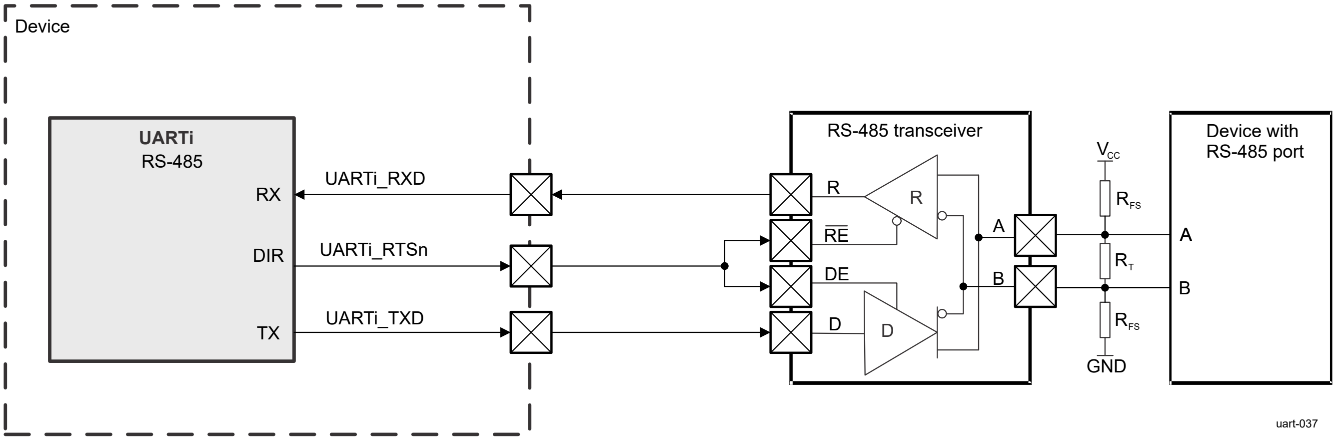

Note

i represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-91. RS-485 Mode Interface Signals

12.2.4.2.2.2 RS-485 Interface Description

Table 12-91 lists the RS-485 interface input/output (I/O) signals.

Table 12-91. UART I/O Signals (RS-485 Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			WKUP_UARTi(3)	
RX	WKUP_UARTi(3)_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi(3)_TXD	O	Serial data output	1
DIR	WKUP_UARTi(3)_RTSn	O	RS-485 Direction	1
			MCU_UARTi(3)	
RX	MCU_UARTi(3)_RXD	I	Serial data input	HiZ
TX	MCU_UARTi(3)_TXD	O	Serial data output	1
DIR	MCU_UARTi(3)_RTSn	O	RS-485 Direction	1
			UARTi(3)	
RX	UARTi(3)_RXD	I	Serial data input	HiZ
TX	UARTi(3)_TXD	O	Serial data output	1
DIR	UARTi(3)_RTSn	O	RS-485 Direction	1

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) i represents a valid UART instance. See the device datasheet for available domains and UART instances.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.3 IrDA Functional Interfaces

12.2.4.2.3.1 System Using IrDA Communication Protocol

Figure 12-92 shows an example connection of an UART instance to an external infrared transceiver in the IrDA modes (FIR, SIR, and MIR).

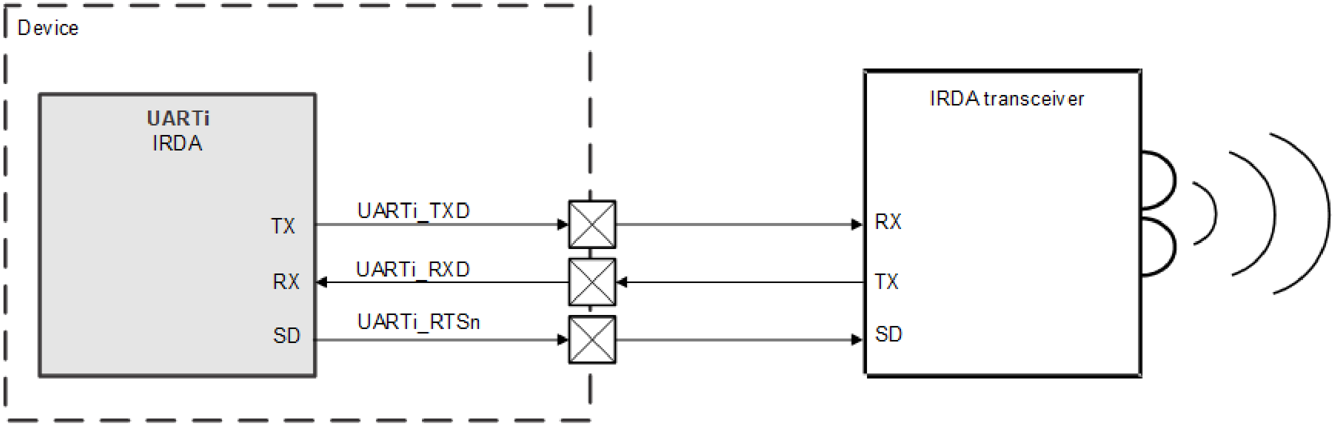

Note

i represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-92. IrDA Mode Interface Signals

12.2.4.2.3.2 IrDA Interface Description

Table 12-92 lists the IrDA interface I/O signals.

Table 12-92. UART I/O Signals (IrDA Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
RX		I	Serial data input	HiZ
TX		O	Serial data output in IrDA modes (SIR, MIR, and FIR).[3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1
RX		I	Serial data input	HiZ
TX		O	Serial data output in IrDA modes (SIR, MIR, and FIR).[3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout (see UART_ACREG[6] SD_MOD bit).

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.3.3 IrDA Protocol and Data Format

12.2.4.2.3.3.1 SIR Mode

In SIR mode, data is transferred between the Host CPU and peripheral devices at speeds of up to 115.2 baud. A SIR transmit frame begins with start flags (a single 0xC0, a multiple 0xC0, or a single 0xC0 preceded by a number of 0xFF flags), followed by frame data and a CRC-16, and ends with a stop flag (0xC1).

The bit format for a single word uses 1 start-bit, 8 data bits, and 1 stop-bit, and is unaffected by the use and settings of the UART_LCR register.

The UART_BLR[6] XBOF_TYPE bit selects whether the 0xC0 or 0xFF start patterns are used when multiple start flags are required.

The SIR transmit state-machine attaches start flags, CRC-16, and stop flags, and checks the outgoing data to establish whether data transparency is required.

The SIR transparency is carried out if the outgoing data between the start and stop flags contains 0xC0, 0xC1, or 0x7D. If one of these start flags is about to be transmitted, the SIR state-machine sends an escape character (0x7D), inverts the fifth bit of the real data to be sent, and then sends this data immediately after the 0x7D character.

The SIR receive state-machine recovers the receive clock, removes the start flags and any transparency from the incoming data, and determines the frame boundary with reception of the stop flag. The SIR state-machine also checks for errors such as a frame abort (0x7D character followed immediately by a 0xC1 stop flag without transparency), a CRC error, or a frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to find possible errors of the received frame.

Note

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. See the description of the UART_ACREG[5] DIS_IR_RX bit. This applies to all three modes: SIR, MIR, and FIR.

Infrared output in SIR mode can be 1.6-µs or 3/16 encoding, selected by the UART_ACREG[7] PULSE_TYPE bit. In 1.6-µs encoding, the infrared pulse width is 1.6 µs; and in 3/16th encoding, the infrared pulse width is 3/16th of a bit duration (1/baud rate).

For back-to-back frames, the transmitting device must send at least two start flags at the start of each frame.

Note

Reception supports variable-length stop-bits.

12.2.4.2.3.3.1.1 Frame Format

Figure 12-93 shows the IrDA SIR frame format.

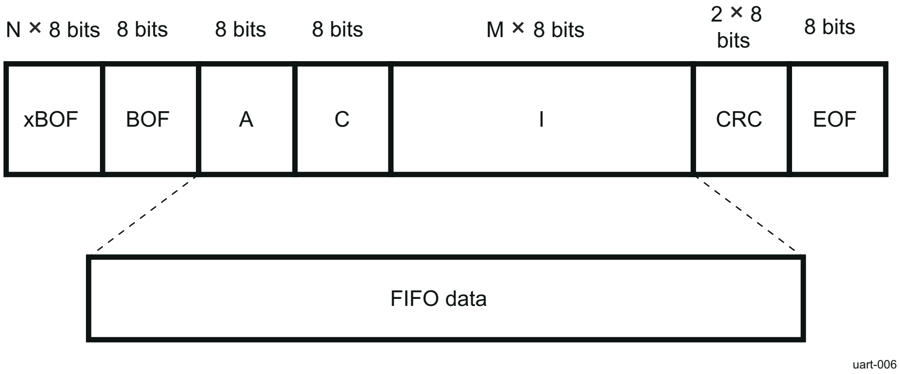

Figure 12-93. IrDA SIR Frame Format

The CRC is applied on the address (A), control (C), and information (I) bytes.

Note

The two words of CRC are written to the FIFO in reception.

12.2.4.2.3.3.1.2 Asynchronous Transparency

Before transmitting a byte, the UART IrDA controller examines each byte of the payload and the CRC field (between BOF and EOF). For each byte equal to 0xC0 (BOF), 0xC1 (EOF), or 0x7D (control escape), the controller performs certain tasks:

- In transmission:
  - Inserts a control escape (CE) byte preceding the byte
  - Complements bit 5 of the byte (that is, exclusive ORs the byte with 0x20)

  The byte sent for the CRC computation is the initial byte written in the TX FIFO (before the XOR with 0x20).
- In reception:

  For the A, C, I, and CRC fields:
  - Compares the byte with the CE byte; if they are not equal, sends the byte to the CRC detector and stores it in the RX FIFO.

- If the byte is equal to the CE byte, discards the CE byte
- Complements bit 5 of the byte following the CE
- Sends the complemented byte to the CRC detector and stores it in the RX FIFO

12.2.4.2.3.3.1.3 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

When a 0x7D character that is followed immediately by a 0xC1 character is received without transparency, the receiver treats the frame as an aborted frame.

12.2.4.2.3.3.1.4 Pulse Shaping

The SIR mode supports the 3/16 and the 1.6-µs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse-width method in transmit mode.

12.2.4.2.3.3.1.5 Encoder

Serial data from the transmit state-machine are encoded to transmit data to the optoelectronics. While the TX FIFO output is high, the TX line is always low, and the counter used to form a pulse on TX is cleared continuously.

After the TX FIFO output resets to 0, TX rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, TX falls, creating a 3-clock-wide pulse. While the TX FIFO output stays low, a pulse is transmitted during the seventh clock to the tenth clock of each 16-clock bit cycle.

Figure 12-94 shows the IrDA SIR encoding mechanism.

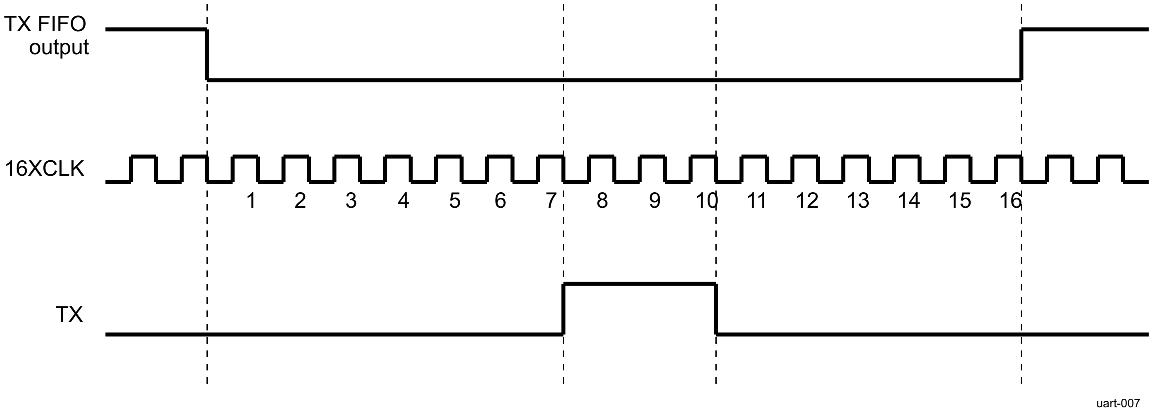

Figure 12-94. IrDA SIR Encoding Mechanism

12.2.4.2.3.3.1.6 Decoder

After reset, the RX FIFO input is high and the 4-bit counter is cleared. When a rising edge is detected on RX, the RX FIFO input falls on the next rising edge of 16XCLK with sufficient setup time. The RX FIFO input stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (rising edges) are detected on the RX, the RX FIFO input remains high.

Figure 12-95 shows the IrDA SIR decoding mechanism.

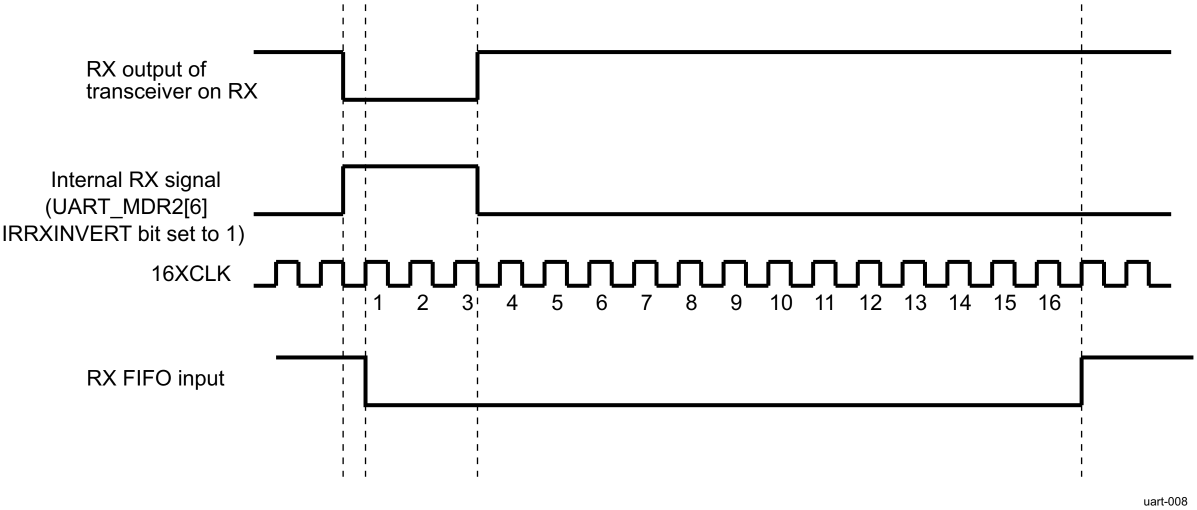

Figure 12-95. IrDA SIR Decoding Mechanism

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. The operation of the RX input can be disabled using the UART_ACREG[5] DIS_IR_RX bit. The UART_MDR2[6] IRRXINVERT bit can invert the signal from the transceiver (RX) pin to the IR RX logic in the UART. This inversion is performed by default.

12.2.4.2.3.3.1.7 IR Address Checking

In all IR modes, when address checking is enabled by setting the UART_EFR[1-0] bit field (see Table 12-93), only frames intended for the device are written to the RX FIFO. This is to avoid receiving frames not meant for this device in a multipoint infrared environment. To program two frame addresses that the UARTi receives in IrDA mode, use the UART_XON1_ADDR1[7-0] and UART_XON2_ADDR2[7-0] bit fields.

Table 12-93. UART_EFR[1-0] IR Address Checking Options

UART_EFR[1]	UART_EFR[0]	IR Address Checking
0	0	All address-checking operations disabled
0	1	Only address 1 checking enabled
1	0	Only address 2 checking enabled
1	1	All address-checking operations enabled

12.2.4.2.3.3.2 SIR Free-Format Mode

To allow complete software flexibility when transmitting and receiving infrared data packets, the SIR free-format (FF) mode is a subfunction of the existing SIR mode. In FF mode, all frames going to and from the FIFO buffers are untouched with respect to appending and removing control characters and CRC values.

The FF mode corresponds to a UART mode with a pulse modulation of 3/16 of baud rate pulse width.

For example, a normal SIR packet has BOF control and CRC error-checking data appended (transmitting) or removed (receiving) from the data going to and from the FIFOs.

Figure 12-96 shows SIR FF mode.

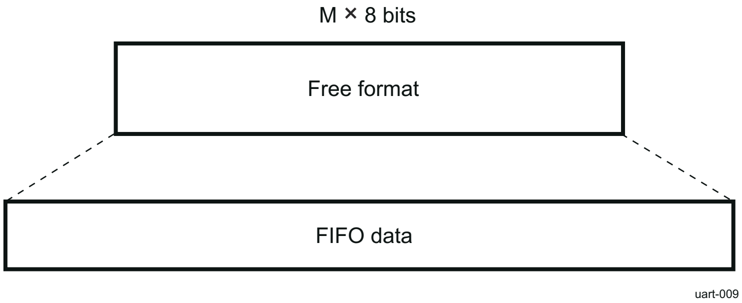

Figure 12-96. SIR FF Mode

In SIR FF mode, the Host CPU software must construct (that is, encode and decode) the entire FIFO data packet.

12.2.4.2.3.3.3 MIR Mode

In MIR mode, data is transferred between the Host CPU and the peripheral devices at 0.576 Mbps or 1.152 Mbps. A MIR transmit frame starts with at least two start flags, followed by a frame data and a CRC-16, and ends with a stop flag (see Figure 12-97).

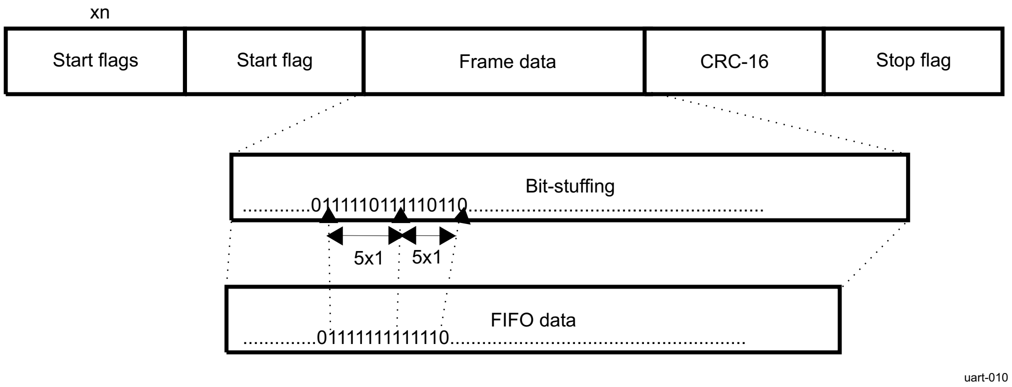

Figure 12-97. MIR Transmit Frame Format

On transmit, the MIR state-machine attaches start flags, a CRC-16, and stop flags, as in SIR mode. All fields are transmitted least-significant bit (LSB) of each byte first.

In MIR mode:

- The state-machine looks for consecutive 1s in the frame data and automatically inserts 0 after five consecutive 1s (this is called bit-stuffing).
- 0x7E is used for start and stop flags (unambiguously, not data, because of bit-stuffing).
- An abort sequence requires a minimum of seven consecutive 1s (unambiguously, not data, because of bit-stuffing).
- Back-to-back frames are allowed with three or more stop flags between them. If two consecutive frames are not back to back, the gap between the last stop flag of the first frame and the start flag of the second frame must be separated by at least seven bit durations.

On receive, the MIR receive state-machine recovers the receive clock, removes the start flags, destuffs the incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as frame abort, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.2.4.2.3.3.3.1 MIR Encoder/Decoder

To meet the MIR baud rate tolerance of 0.1 percent with a 48-MHz clock input, a 42-41-42 encoding/decoding adjustment is performed. The reference start point is the first start flag, and the 42-41-42 cyclic pattern is repeated until the stop flag is sent or detected.

The jitter created this way is within MIR tolerances. The pulse width is not exactly 1/4, but it is within the tolerances defined by IrDA specifications.

Figure 12-98 shows the MIR baud rate adjustment mechanism.

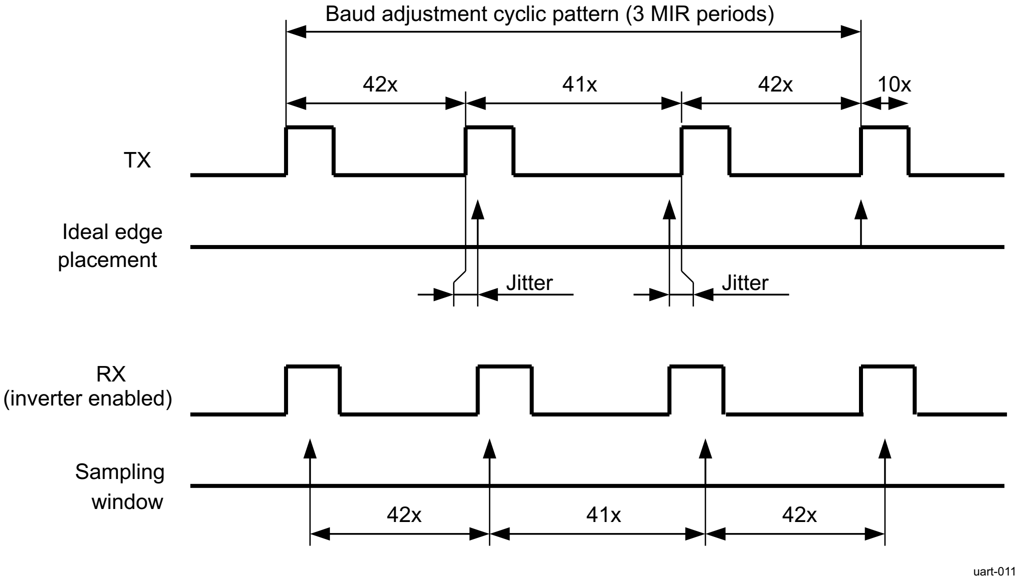

Figure 12-98. MIR Baud Rate Adjustment Mechanism

12.2.4.2.3.3.3.2 SIP Generation

In the MIR and FIR operation modes, the transmitter must send a serial infrared interaction pulse (SIP) at least once every 500 ms. The SIP informs slow devices (operating in SIR mode) that the medium is occupied.

Figure 12-99 shows the SIP.

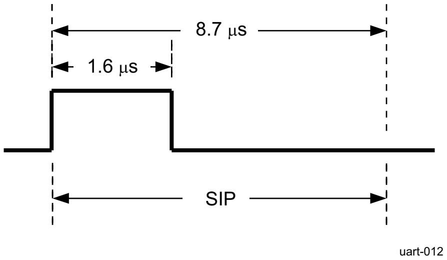

Figure 12-99. SIP

12.2.4.2.3.3.4 FIR Mode

In FIR mode, data is transferred between the Host CPU and the peripheral devices at 4 Mbps. A FIR transmit frame starts with a preamble that is followed by a start flag, frame data, CRC-32, and ends with a stop flag.

Figure 12-100 shows the FIR transmit frame format.

Figure 12-100. FIR Transmit Frame Format

Preamble (16x)	Start flag	Frame data	CRC-32	Stop flag

On transmit, the FIR transmit state-machine attaches the preamble, start flag, CRC-32, and stop flag. An abort sequence requires at least two transmissions of 0000. Back-to-back frames are allowed, but each frame must be complete.

The state-machine also encodes the transmit data into 4-PPM format (see Table 12-94) and generates the SIP (see Section 12.2.4.2.3.3.3.2 , *SIP Generation*).

Table 12-94. 4-PPM Format

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
00	1000
01	0100
10	0010
11	0001

The four symbols described in Table 12-94 are the legal, encoded data symbols. All other combinations are illegal for encoding data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag because they are unambiguously not data (see Table 12-95).

Table 12-95. FIR Preamble, Start Flag, and Stop Flag

Frame Part	Transmitted Frame (Bin)
Preamble	1000 0000 1010 1000 (16 repeated transmissions)
Start flag	0000 1100 0000 1100 0110 0000 0110 0000
Stop flag	0000 1100 0000 1100 0000 0110 0000 0110

All fields are transmitted LSBs of each byte first (see Table 12-96).

Table 12-96. FIR Data Byte Transmission Order Example

Data Byte (Hex)	Data Byte Pair (Bin)	4-PPM Data Symbol (Bin)	Transmission Order
0x0B	00	1000	4
	00	1000	3
	10	0010	2
	11	0001	1

On receive, the FIR receive state-machine recovers the receive clock, removes the preamble and the start flag, decodes the 4-PPM incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as illegal symbol, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.2.4.2.4 CIR Functional Interfaces

12.2.4.2.4.1 System Using CIR Communication Protocol With Remote Control

All UART modules can be connected to an external infrared transceiver in CIR mode. Figure 12-101 shows an example connection of a UART instance in CIR mode.

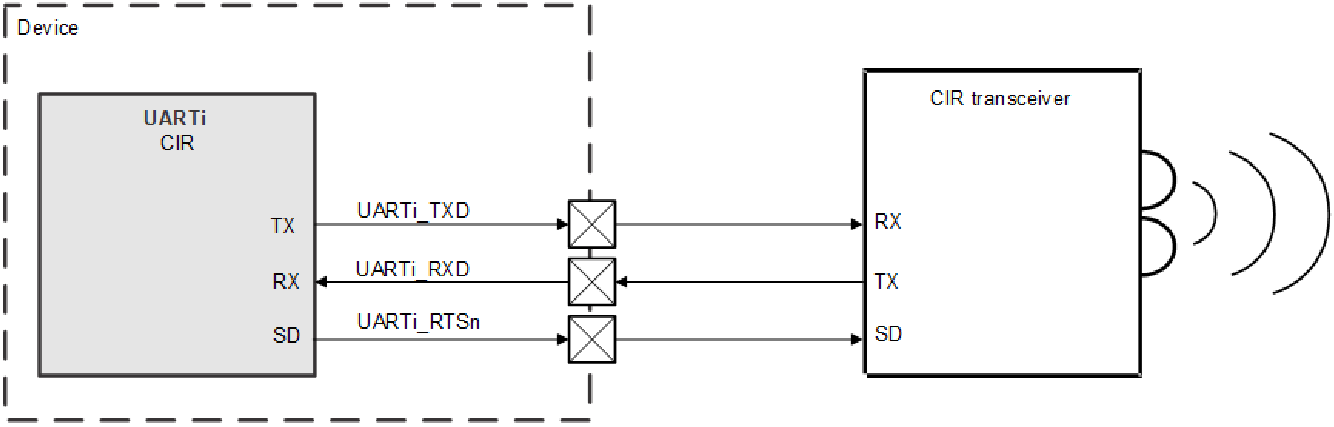

Note

i represents a valid instance of UART in a domain. See the device data sheet for valid domains.

Figure 12-101. CIR Mode Interface Signals

12.2.4.2.4.2 CIR Interface Description

Table 12-97 lists the CIR interface I/O signals.

Table 12-97. UART I/O Signals (CIR Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
RX		I	Serial data input	HiZ
TX		O	Serial data output in CIR mode. [3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1
			UART[0-9]	
RX		I	Serial data input	HiZ
TX		O	Serial data output in CIR mode. [3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout is an inverted value of the UART_ACREG[6] SD_MOD bit.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.4.3 CIR Protocol and Data Format

In CIR mode, the infrared operation functions as a programmable (universal) remote control.

The CIR mode uses a variable PWM technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on user-defined frame structure and packet content.

12.2.4.2.4.3.1 Carrier Modulation

Each modulated pulse that constitutes a digit is a train of on/off pulses (see Figure 12-102).

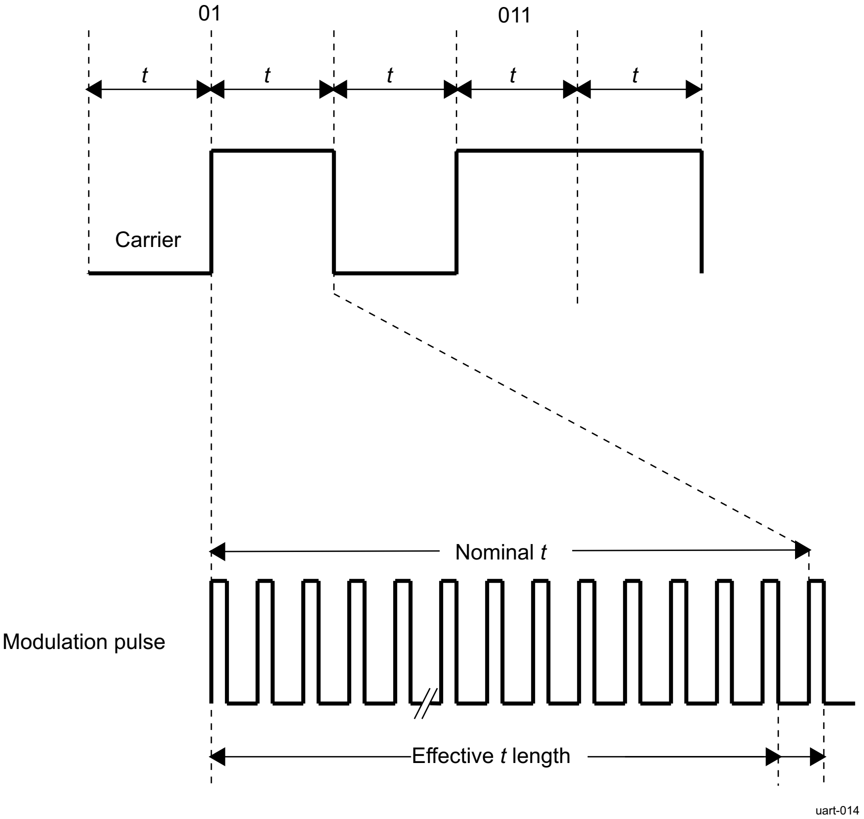

Figure 12-102. CIR Pulse Modulation

12.2.4.2.4.3.2 Pulse Duty Cycle

The programmer can choose one of four duty cycles for modulation pulses by setting the appropriate value in the UART_MDR2[5-4] CIR_PULSE_MODE bit field (1/4, 1/3, 5/12, or 1/2).

Figure 12-103 shows the CIR modulation duty cycles.

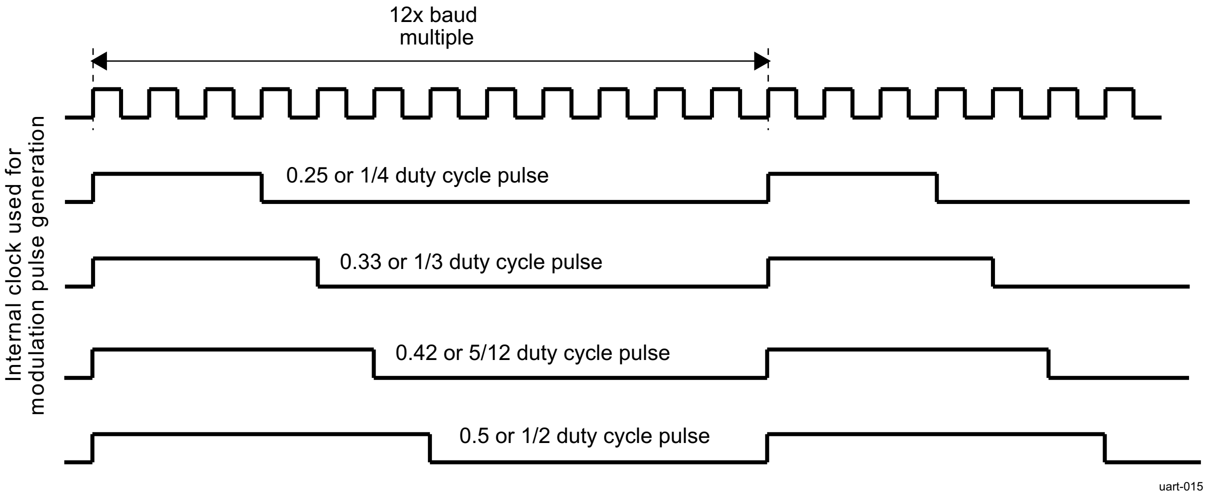

Figure 12-103. CIR Modulation Duty Cycle

The transmission logic ensures that all pulses are transmitted completely (no cutoff during transmission). While transmitting continuous bytes back-to-back, no delay is inserted between 2 transmitted bytes. Thus, software must handle the delay between consecutively transmitted bytes if the receiving end requires it.

12.2.4.2.4.3.3 Consumer IR Encoding/Decoding

There are two methods of encoding for remote-control applications:

- Pulse duration encoding (time-extended bit forms): A variable pulse distance, or duration, in which the difference between logic 1 and logic 0 is the length of the pulse width
- Biphase encoding: The encoding of logic 0 and logic 1 is in the change of signal level from 1 to 0 or 0 to 1, respectively.

Japanese manufacturers favor pulse duration encoding; European manufacturers favor biphase encoding.

CIR mode uses a completely flexible free-format encoding in which 1 is transmitted from the TX FIFO as a modulated pulse with duration *t*.

Similarly, 0 is transmitted as a blank duration T. The Host CPU constructs and deciphers the protocol of the data. For example, the RC-5 protocol using Manchester encoding can be emulated as using a 01 pair for 1 and a 10 pair for 0 (see Figure 12-104).

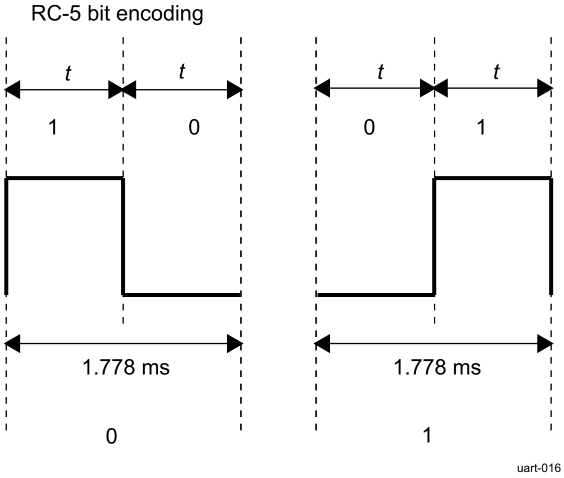

Figure 12-104. UART RC-5 Bit Encoding

Because CIR mode logic does not impose a fixed format for infrared packets of data, the Host CPU software can define the format using simple data structures that are then modulated into an industry standard, such as RC-5 or SIRC. To send a sequence of 0101 in RC-5, the Host CPU software must write an 8-bit binary character of 10011001 to the data FIFO of the UART.

For SIRC, the modulation length (multiples of *t*) is used to distinguish between 1 and 0. The subsequent SIRC digits show the difference in encoding between this and, for example, RC-5. The pulse width is extended for one digit.

Figure 12-105 shows SIRC bit encoding.

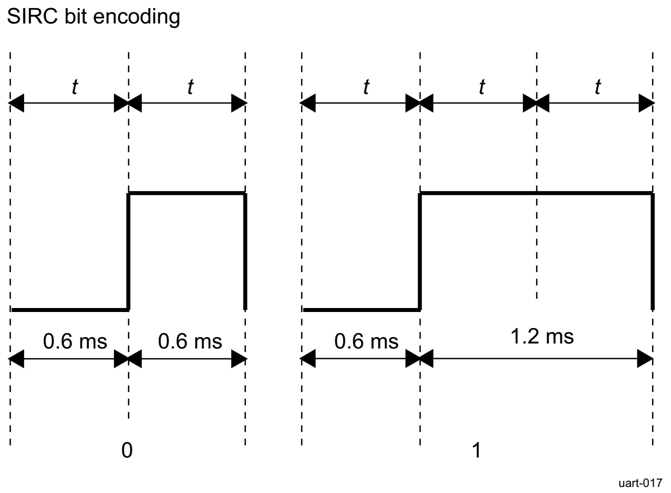

Figure 12-105. UART SIRC Bit Encoding

To construct comprehensive packets constituting remote-control commands, the Host CPU software must combine a number of 8-bit data characters in a sequence that follows one of the universally accepted formats.

Figure 12-106 shows a standard RC-5 frame as detected by UART in CIR mode (the SIRC format follows this). Each field in RC-5 can be considered as two *t* pulses (digital bits) from the TX FIFO.

S1	S2	T	A4	A3	A2	A1	A0	C5	C4	C3	C2	C1	C0

uart-018

Figure 12-106. UART RC-5 Standard Packet Format

Where:

S1, S2:	Start-bits (always 1)
T:	Toggle bit
A4..A0:	Address (or system) bits
C5..C0:	Command bits

The toggle bit T changes when a new command is transmitted to detect when the same key is pressed twice (effectively receiving the same data from the host consecutively). A brief delay in the transmission of the same command is detected by the use of the toggle bit because a code is sent while the Host CPU transmits characters to the UART for transmission. The address bits define the machine or device for which the infrared transmission is intended, and the command defines the operation.

To accommodate an extended RC-5 format, the S2 bit is replaced by an additional command bit (C6) that lets the command range increase to 7 bits. This format is known as the extended RC-5 format.

The SIRC encoding uses the duration of modulation for mark and space; therefore, the duration of data bits in the standard frame length varies.

Figure 12-107 shows the packet format and bit encoding. As Figure 12-108 shows, 1 start-bit of 2.4 ms and control codes are followed by data that constitute the entire frame.

S	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4

uart-019

Figure 12-107. UART SIRC Packet Format

Note

The encoding must take a standard duration, but the contents of the data can vary. This implies that the control software for sending and receiving data packets must exercise a scheme of interpacket delay, where successive packets can be sent only after a real-time delay expires.

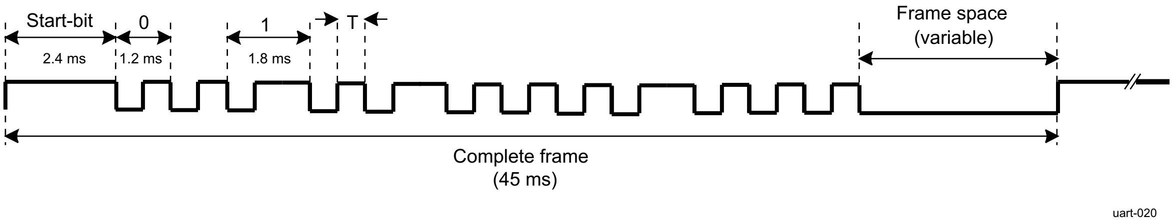

Figure 12-108. UART SIRC Bit Transmission Example

Note

This document does not describe all encoding methods and techniques; the previous information discusses the considerations required to employ different encoding methods for different industry-standard protocols. See industry-standard documentation for specific methods of encoding and protocol use.

12.2.4.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.4.4 UART Functional Description

12.2.4.4.1 UART Block Diagram

The UART module can be divided into three main blocks:

- FIFO management
- Mode selection
- Protocol formatting

FIFO management is common to all functions and enables the transmission and reception of data from the host processor point of view.

There are two modes:

- Function mode: Routes the data to the chosen function (UART, RS-485, IrDA, or CIR) and enables the mechanism corresponding to the chosen function.
- Register mode: Enables conditional access to registers.

For more information about mode configuration, see Section 12.2.4.4.7 , *Mode Selection*.

Protocol formatting has three subcategories:

- Clock generation: The 48-MHz input clock generates all necessary clocks.
- Data formatting: Each function uses its own state-machine that is responsible for the transition between FIFO data and frame data associated with it.
- Interrupt management: Different interrupt types are generated depending on the chosen function. In each mode, when an interrupt is generated, the UART_IIR_UART register indicates the interrupt type.
  - UART mode interrupts: Seven interrupts prioritized in six different levels
  - IrDA mode interrupts: Eight interrupts. The interrupt line is activated when any interrupt is generated (there is no priority).
  - CIR mode interrupts: A subset of existing IrDA mode interrupts is used.

In parallel with these functional blocks, a power-saving strategy exists for each function.

Figure 12-109 is the UART block diagram.

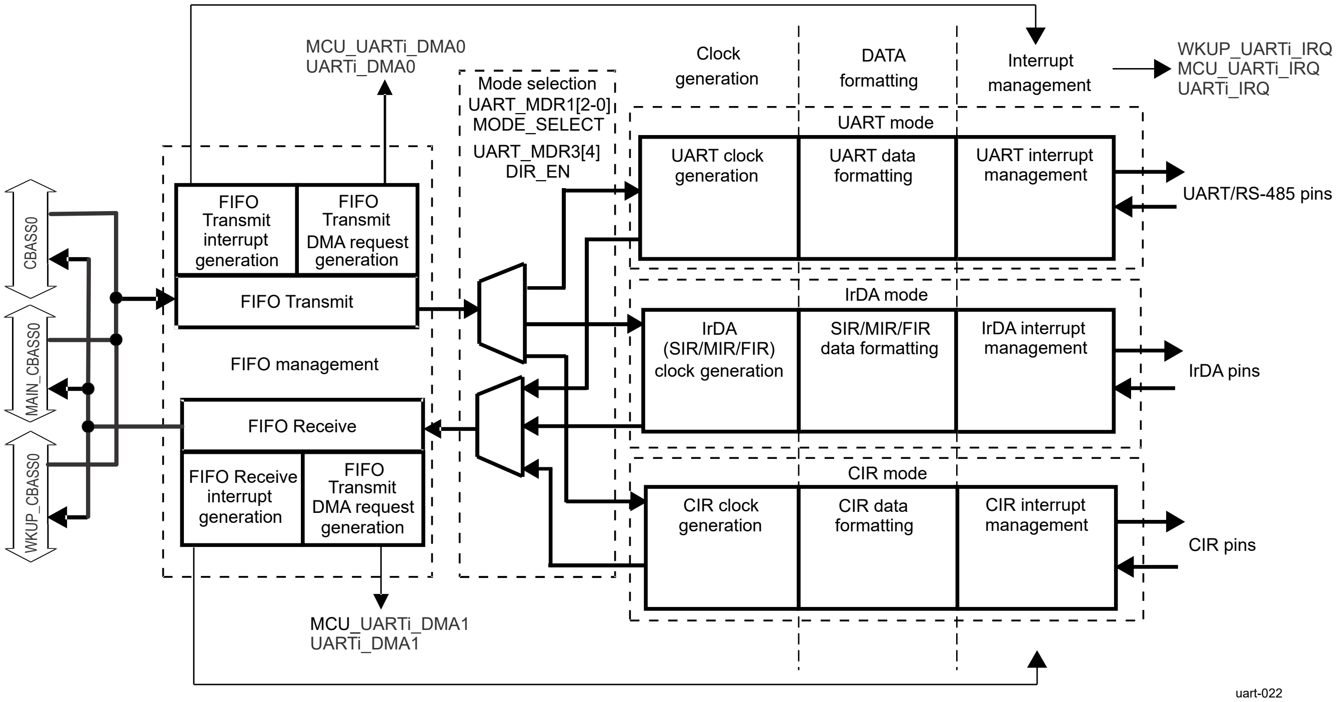

Note

i represents a valid instance of UART in a domain. See the device datasheet for valid domains and instances.

Figure 12-109. UART Functional Block Diagram

12.2.4.4.2 UART Clock Configuration

Each UART uses a 48-MHz functional clock for its logic and to generate external interface signals. Each UART uses an interface clock for register accesses.

12.2.4.4.3 UART Software Reset

The UART_SYSC[1] SOFTRESET bit controls the software reset; setting this bit to 1 triggers a software reset functionally equivalent to hardware reset.

12.2.4.4.3.1 Independent TX/RX

The receiver and transmitter are enabled by default after reset. Software can choose to disable, re-enable or to reset either the RX or the TX side independently of the other through the UART_ECR register.

12.2.4.4.4 UART Power Management

12.2.4.4.4.1 UART Mode Power Management

12.2.4.4.4.1.1 Module Power Saving

In UART modes, sleep mode is enabled by setting the UART_IER_UART[4] SLEEP_MODE bit to 1 (when the UART_EFR[4] ENHANCED_EN bit is set to 1).

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RX, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- The only pending interrupts are THR interrupts.

Sleep mode is a good way to lower UART power consumption, but this state can be achieved only when the UART is set to modem mode. Therefore, even if the UART has no key role functionally, it must be initialized in a functional mode to take advantage of sleep mode.

In sleep mode, the module clock and baud rate clock are stopped internally. Because most registers are clocked by these clocks, this greatly reduces power consumption. The module wakes up when a change is detected on the RX line, when data is written to the TX FIFO, and when there is a change in the state of the modem input pins.

An interrupt can be generated on a wake-up event by setting the UART_SCR[4] RX_CTS_WU_EN bit to 1. To understand how to manage the interrupt, see Section 12.2.4.4.5.1.2 , *Wake-Up Interrupt*.

Note

There must be no writing to the divisor latches, UART_DLL and UART_DLH, to set the baud clock (BCLK) while in sleep mode. It is advisable to disable sleep mode using the UART_IER_UART[4] SLEEP_MODE bit before writing to the UART_DLL or UART_DLH register.

12.2.4.4.4.1.2 System Power Saving

Sleep and auto-idle modes are embedded power-saving features. Power-reduction techniques can be applied at the system level by shutting down certain internal clock and power domains of the device.

The UART supports an idle req/idle ack handshaking protocol used at the system level to shut down the UART clocks in a clean and controlled manner and to switch the UART from interrupt-generation mode to wake-up generation mode for unmasked events (see the UART_SYSC[2] ENAWAKEUP bit and the UART_WER register).

For more information, see *Power* in the *Device Configuration*.

12.2.4.4.4.2 IrDA Mode Power Management

12.2.4.4.4.2.1 Module Power Saving

In IrDA modes, sleep mode is enabled by setting the UART_MDR1[3] IR_SLEEP bit to 1.

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RXD, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- No interrupts are pending except THR interrupts.

The module wakes up when a change is detected on the RXD line or when data is written to the TX FIFO.

12.2.4.4.4.2.2 System Power Saving

System power saving for the IrDA mode has the same function as for the UART mode (see Section 12.2.4.4.4.1.2 , *System Power Saving*).

12.2.4.4.4.3 CIR Mode Power Management

12.2.4.4.4.3.1 Module Power Saving

Module power saving for the CIR mode has the same function as for the IrDA mode (see Section 12.2.4.4.4.2.1 , *Module Power Saving*).

12.2.4.4.4.3.2 System Power Saving

System power saving for the CIR mode has the same function as for the UART mode (see Section 12.2.4.4.4.1.2 , *System Power Saving*).

12.2.4.4.4.4 Local Power Management

Table 12-98 describes power-management features available for the UART.

> **Note**
>
> For information about source clock gating and the sleep/wake-up transitions description, see *Power* in the *Device Configuration*.

Table 12-98. UART Local Power-Management Features

Feature	Registers	Description
Clock autogating	UART_SYSC[0] AUTOIDLE	This bit allows local power optimization in the module by gating the clock on interface activity or gating the UARTi_FCLK clock on internal activity.
Peripheral idle modes	UART_SYSC[4-3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	N/A	Feature not available
Controller standby modes	N/A	Feature not available
Global wake-up enable	UART_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.
Wake-Up sources enable	N/A	Feature not available

12.2.4.4.5 UART Interrupt Requests

12.2.4.4.5.1 UART Mode Interrupt Management

12.2.4.4.5.1.1 UART Interrupts

The UART mode includes seven possible interrupts prioritized to six levels.

When an interrupt is generated, the interrupt identification register (UART_IIR_UART) sets the UART_IIR_UART[0] IT_PENDING bit to 0 to indicate that an interrupt is pending, and indicates the type of interrupt through the UART_IIR_UART[5-1] bit field. Table 12-99 summarizes the interrupt control functions.

Table 12-99. UART Mode Interrupts

IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000001	N/A	No Interrupt	N/A	N/A
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO.	FE, PE, BI: Read the UART_RHR register. OE: Read the UART_LSR_UART register.
001100	2	RX time-out	Stale data in RX FIFO	Read the UART_RHR register.
000100	2	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears
000010	3	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears
000000	4	Modem status	See the UART_MSR register.	Read the MSR register
010000	5	XOFF interrupt/ special character interrupt	Receive XOFF characters/special character	Receive XON character(s), if XOFF interrupt/read of the UART_IIR_UART register, if special character interrupt
100000	6	CTS, RTS	RTS pin or CTS pin change state from active (low) to inactive (high)	Read the UART_IIR_UART register

For the receiver-line status interrupt, the UART_LSR_UART[7] RX_FIFO_STS bit generates the interrupt.

For the XOFF interrupt, if an XOFF flow character detection caused the interrupt, the interrupt is cleared by an XON flow character detection. If special character detection caused the interrupt, the interrupt is cleared by a read of the UART_IIR_UART register.

12.2.4.4.5.1.2 Wake-Up Interrupt

Wake-up interrupt is a special interrupt that works differently from other interrupts. This interrupt is enabled when the UART_SCR[4] RX_CTS_WU_EN bit is set to 1. The UART_IIR_UART register is not modified when this occurs; the UART_SSR[1] RX_CTS_WU_STS bit must be checked to detect a wake-up event.

When a wake-up interrupt occurs, it can be cleared only by resetting the UART_SCR[4] RX_CTS_WU_EN bit. This bit must be reenabled (set to 1) after the current wake-up interrupt event is processed to detect the next incoming wake-up event.

12.2.4.4.5.2 IrDA Mode Interrupt Management

12.2.4.4.5.2.1 IrDA Interrupts

The IrDA function generates interrupts. All interrupts can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_IRDA). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_IRDA).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_IRDA and UART_IIR_IRDA mappings, depending on the selected mode.

The IrDA modes have eight possible interrupts (see Table 12-100). The interrupt line is activated when any interrupt is generated (there is no priority).

Table 12-100. IrDA Mode Interrupts

IIR_IRDA Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears.
1	THR interrupt	TFE (UART_THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears.
2	Last byte in RX FIFO	Last byte of frame in RX FIFO is available to be read at the UART_RHR port.	Read the UART_RHR register.
3	RX overrun	Write to the UART_RHR register when the RX FIFO is full.	Read UART_RESUME register.
4	Status FIFO interrupt	Status FIFO triggers level reached.	Read STATUS FIFO.
5	TX status	UART_THR empty before EOF sent. Last bit of transmission of the IrDA frame occurred, but with an underrun error OR Transmission of the last bit of the IrDA frame completed successfully.	Read the UART_RESUME register OR Read the UART_IIR_IRDA register.
6	Receiver line status interrupt	CRC, ABORT, or frame-length error is written into the STATUS FIFO.	Read the STATUS FIFO (read until empty - maximum of eight reads required).
7	Received EOF	Received end-of-frame	Read the UART_IIR_IRDA register.

12.2.4.4.5.2.2 Wake-Up Interrupts

The wake-up interrupt for IrDA mode has the same function as that for UART mode (see Section 12.2.4.4.5.1.2 , *Wake-Up Interrupt*).

12.2.4.4.5.3 CIR Mode Interrupt Management

12.2.4.4.5.3.1 CIR Interrupts

The CIR function generates interrupts that can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_CIR). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_CIR).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_CIR and UART_IIR_CIR mappings, depending on the selected mode.

Table 12-101 lists the interrupt modes to be maintained. In CIR mode, the sole purpose of the UART_IIR_CIR[5] TX_STATUS_IT bit is to indicate that the last bit of infrared data was passed to the TX pin.

Table 12-101. CIR Mode Interrupts

IIR_CIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
1	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR register until the interrupt condition disappears
2	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
3	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
4	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
5	TX status	Transmission of the last bit of the frame is complete successfully	Read the UART_IIR_CIR register
6	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
7	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

12.2.4.4.5.3.2 Wake-Up Interrupts

The wake-up interrupt for CIR mode has the same function as that for UART mode (see Section 12.2.4.4.5.1.2 , *Wake-Up Interrupt*).

12.2.4.4.6 UART FIFO Management

The FIFO is accessed by reading and writing the UART_RHR and UART_THR registers. Parameters are controlled using the FIFO control register (UART_FCR) and supplementary control register (UART_SCR). Reading the UART_SSR[0] TX_FIFO_FULL bit at 1 means the FIFO is full.

The UART_TLR register controls the FIFO trigger level, which enables DMA and interrupt generation. After reset, transmit (TX) and receive (RX) FIFOs are disabled; thus, the trigger level is the default value of 1 byte. Figure 12-110 shows the FIFO management registers.

Note

Data in the UART_RHR register is not overwritten when an overflow occurs.

Note

The UART_SFLSR, UART_SFREGL, and UART_SFREGH status registers are used in IrDA mode only. For information about their use, see Section 12.2.4.4.8.3.3 , *IrDA Data Formatting*.

Note

Bits UART_FCR[2] TX_FIFO_CLEAR and UART_FCR[1] RX_FIFO_CLEAR are automatically cleared by hardware after 4 × + 5 × UARTi_FCLK clock cycles. This delay is needed to finish the resetting of the corresponding FIFO and DMA control registers.

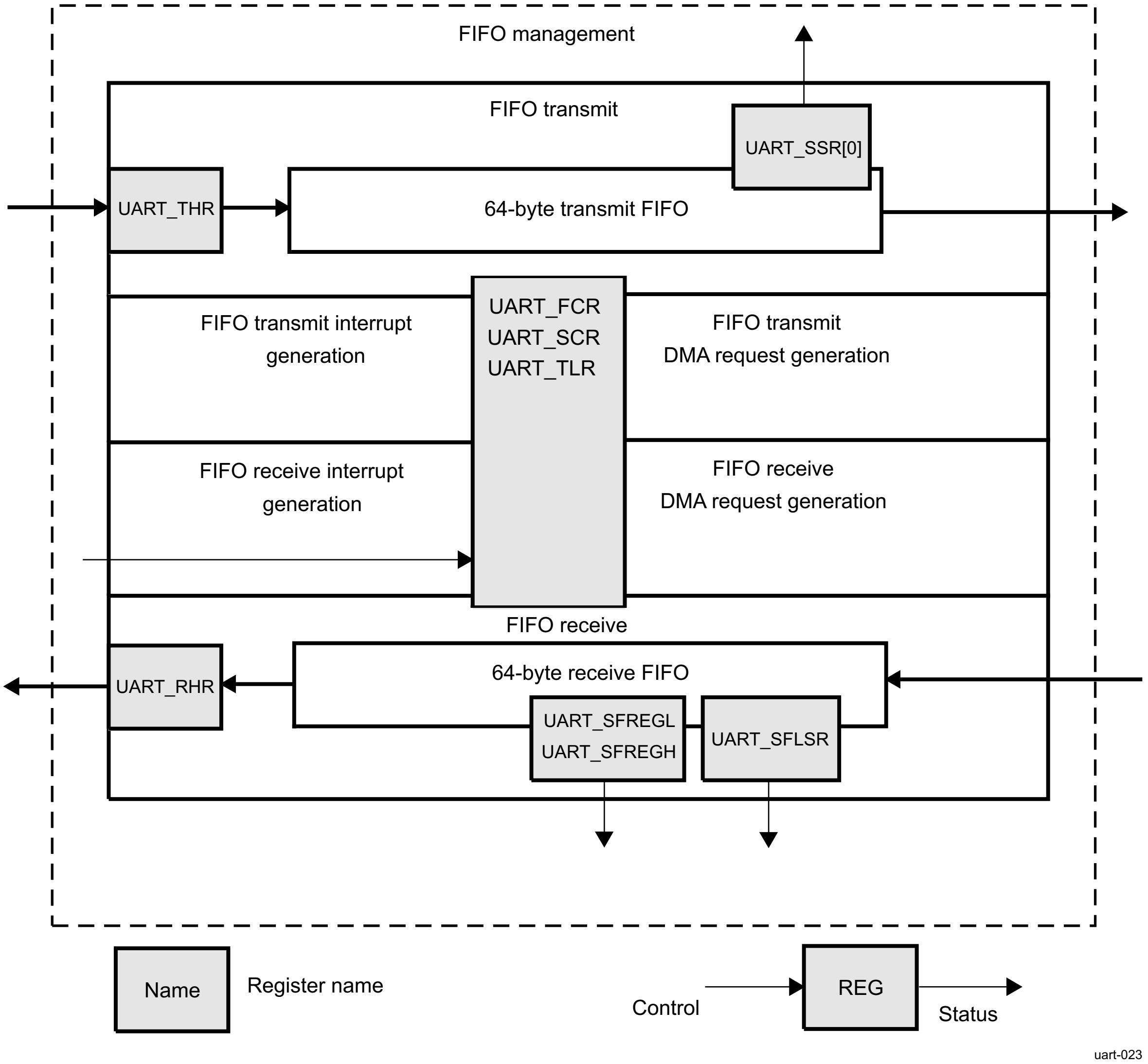

Figure 12-110. UART FIFO Management Registers

12.2.4.4.6.1 FIFO Trigger

12.2.4.4.6.1.1 Transmit FIFO Trigger

Table 12-102 lists the TX FIFO trigger level settings.

Table 12-102. UART TX FIFO Trigger Level Setting Summary

SCR[6]	TLR[3:0]	TX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[5-4] TX_FIFO_TRIG bit field (8,16, 32, or 56 spaces)
0	!= 0x0	Defined by the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field (from 4 to 60 spaces with a granularity of 4 spaces)
1	Value	Defined by the concatenated value of TX_FIFO_TRIG_DMA and TX_FIFO_TRIG (from 1 to 63 spaces with a granularity of 1 space) **Note:** The combination of TX_FIFO_TRIG_DMA = 0x0 and TX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 space required). All zeros result in unpredictable behavior.

12.2.4.4.6.1.2 Receive FIFO Trigger

Table 12-103 lists the RX FIFO trigger-level settings.

Table 12-103. UART RX FIFO Trigger-Level Setting Summary

SCR[7]	TLR[7:4]	RX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[7-6] RX_FIFO_TRIG bit field (8,16, 56, or 60 characters)
0	!= 0x0	Defined by the UART_TLR[7-4] RX_FIFO_TRIG_DMA bit field (from 4 to 60 characters with a granularity of 4 characters)
1	Value	Defined by the concatenated value of RX_FIFO_TRIG_DMA and RX_FIFO_TRIG (from 1 to 63 characters with a granularity of 1 character) **Note:** The combination of RX_FIFO_TRIG_DMA = 0x0 and RX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 character required). All zeros result in unpredictable behavior.

The receive threshold is programmed using the UART_TCR[7-4] RX_FIFO_TRIG_START and UART_TCR[3-0] RX_FIFO_TRIG_HALT bit fields:

- Trigger levels from 0 to 60 bytes are available with a granularity of 4 (trigger level = 4 × [4-bit register value]).
- To ensure correct device operation, ensure that RX_FIFO_TRIG_HALT > RX_FIFO_TRIG when auto-RTS is enabled.

  Delay = [4 + 16 × (1 + CHAR_LENGTH + Parity + Stop – 0.5)] × Baud_rate + 4 × FCLK

  Note

  The RTS signal is deasserted after the UART module receives the data over RX_FIFO_TRIG_HALT. Delay means how long the UART module takes to deassert the RTS signal after reaching RX_FIFO_TRIG_HALT.

- In FIFO interrupt mode with flow control, ensure that the trigger level to HALT transmission is greater than or equal to the RX FIFO trigger level (the UART_TCR[7-4] RX_FIFO_TRIG_START bit field or the UART_FCR[7-6] RX_FIFO_TRIG bit field); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist, because a DMA request is sent when a byte is received.

12.2.4.4.6.2 FIFO Interrupt Mode

In FIFO interrupt mode (the FIFO control register UART_FCR[0] FIFO_EN bit is set to 1 and relevant interrupts are enabled by the UART_IER_UART register), an interrupt signal informs the processor of the status of the receiver and transmitter. These interrupts are raised when the RX/TX FIFO threshold (the UART_TLR[7-4] RX_FIFO_TRIG_DMA and UART_TLR[3-0] TX_FIFO_TRIG_DMA bit fields or the UART_FCR[7-6] RX_FIFO_TRIG and UART_FCR[5-4] TX_FIFO_TRIG bit fields, respectively) is reached.

The interrupt signals instruct the Host CPU to transfer data to the destination (from the UART in receive mode and/or from any source to the UART FIFO in transmit mode).

When UART flow control is enabled with interrupt capabilities, the UART flow control FIFO threshold (the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field) must be greater than or equal to the RX FIFO threshold.

Figure 12-111 shows the generation of the RX FIFO interrupt request.

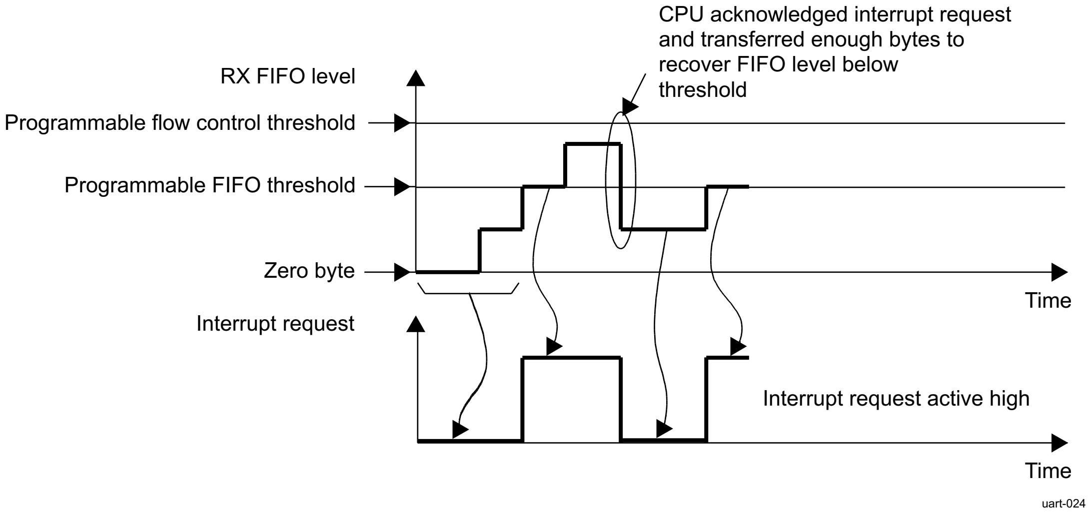

Figure 12-111. UART RX FIFO Interrupt Request Generation

In receive mode, no interrupt is generated until the RX FIFO reaches its threshold. Once low, the interrupt can be deasserted only when the Host CPU has handled enough bytes to put the FIFO level below threshold. The flow control threshold is set at a higher value than the FIFO threshold.

Figure 12-112 shows the generation of the TX FIFO interrupt request.

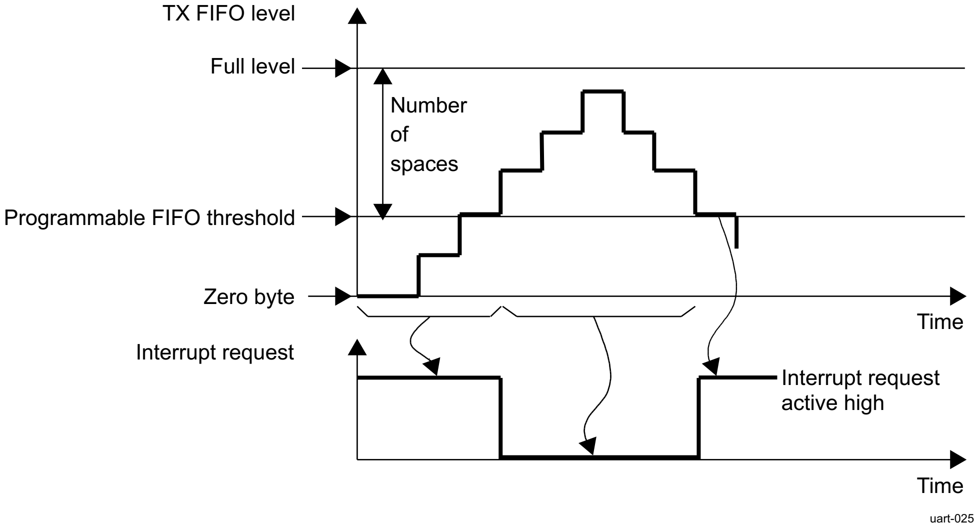

Figure 12-112. UART TX FIFO Interrupt Request Generation

In transmit mode, an interrupt request is automatically asserted when the TX FIFO is empty. This request is deasserted when the TX FIFO crosses the threshold level. The interrupt line is deasserted until a sufficient number of elements is transmitted to go below the TX FIFO threshold.

12.2.4.4.6.3 FIFO Polled Mode Operation

In FIFO polled mode (the UART_FCR[0] FIFO_EN bit is set to 0 and the relevant interrupts are disabled by the UART_IER_UART register), the status of the receiver and transmitter can be checked by polling the line status register (UART_LSR_UART).

This mode is an alternative to the FIFO interrupt mode of operation in which the status of the receiver and transmitter is automatically determined by sending interrupts to the Host CPU.

12.2.4.4.6.4 FIFO DMA Mode Operation

Although the DMA operation includes four modes (DMA modes 0 through 3), the information in *UART Hardware Requests*, assumes that mode 1 is used. (Mode 2 and mode 3 are legacy modes that use only one DMA request for each module.)

In mode 2, the remaining DMA request is used for RX. In mode 3, the remaining DMA request is used for TX.

DMA requests in mode 2 and mode 3 use the signals (where i = 0 to).

signals are not used by the module in mode 2 and mode 3:

The DMA mode and signals usage can be selected as follows:

- When the UART_SCR[0] DMA_MODE_CTL bit is set to 0, setting the UART_FCR[3] DMA_MODE bit to 0 enables DMA mode 0. Setting the UART_FCR[3] DMA_MODE bit to 1 enables DMA mode 1.
- When the UART_SCR[0] DMA_MODE_CTL bit is set to 1, the UART_SCR[2-1] DMA_MODE_2 bit field determines DMA mode 0 to mode 3 based on the supplementary control register (UART_SCR) description.

For example:

- If no DMA operation is desired, set the UART_SCR[0] DMA_MODE_CTL bit to 1 and the UART_SCR[2-1] DMA_MODE_2 bit field to 0x0. (The DMA_MODE bit is discarded.)
- If DMA mode 1 is desired, set the UART_SCR[0] DMA_MODE_CTL bit to 0 and the UART_FCR[3] DMA_MODE bit to 1, or set the UART_SCR[0] DMA_MODE_CTL bit to 1 and the UART_SCR[2-1] DMA_MODE_2 bit field to 01. (The UART_FCR[3] DMA_MODE bit is discarded.)

If the FIFOs are disabled (the UART_FCR[0] FIFO_EN bit is set to 0), the DMA occurs in single-character transfers.

When DMA mode 0 is programmed, the signals associated with DMA operation are not active.

Depending on UART_MDR3[2] SET_DMA_TX_THRESHOLD, the threshold can be programmed different ways:

- SET_TX_DMA_THRESHOLD = 1:

  The threshold value will be the value of the UART_TX_DMA_THRESHOLD register. If SET_TX_DMA_THRESHOLD + TX trigger spaces 64, then the default method of threshold is used: threshold value = TX FIFO size.
- SET_TX_DMA_THRESHOLD = 0:

  The threshold value = TX FIFO size TX trigger space. The TX DMA line is asserted if the TX FIFO level is lower then the threshold. It remains asserted until TX trigger spaces number of bytes are written into the FIFO. The DMA line is then deasserted and the FIFO level is compared with the threshold value.

12.2.4.4.6.4.1 DMA sequence to disable TX DMA

In order to disable TX DMA if it is not needed anymore (e.g. all transfers are done and UART idle mode is desired), the following sequence must be use

1. DMA mode 1 is set (both TX/RX DMA) by registers UART_SCR[0] DMA_MODE_CTL = 0 and UART_FCR[3] DMA_MODE = 1:
   a. Set the UART_SCR[2-1] DMA_MODE_2 bit fields to 01 (DMA mode 1)
   b. Set the UART_SCR[0] DMA_MODE_CTL bit to1 (this setting of UART_SCR[0] DMA_MODE-CTL will ignores UART_FCR[3] DMA_MODE_CTL bit)

   Note

   It is strongly suggested to do steps ‘a’ and ‘b’ in two separate write in order to avoid malfunction of the device.

   c. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

   ---

   Note

   There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   ---

   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   f. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   g. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

2. DMA mode 1 is set (both TX/RX DMA) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 01. It is almost the same as above, but steps ‘a’, and ‘b’ can be skipped:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

   ---

   Note

   There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   ---

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

3. DMA mode 3 is set (TX DMA only) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 11. It is the same as above:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

   ---

   Note

   There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   ---

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

12.2.4.4.6.4.2 DMA Transfers (DMA Mode 1, 2, or 3)

Figure 12-113 through Figure 12-116 show the supported DMA operations.

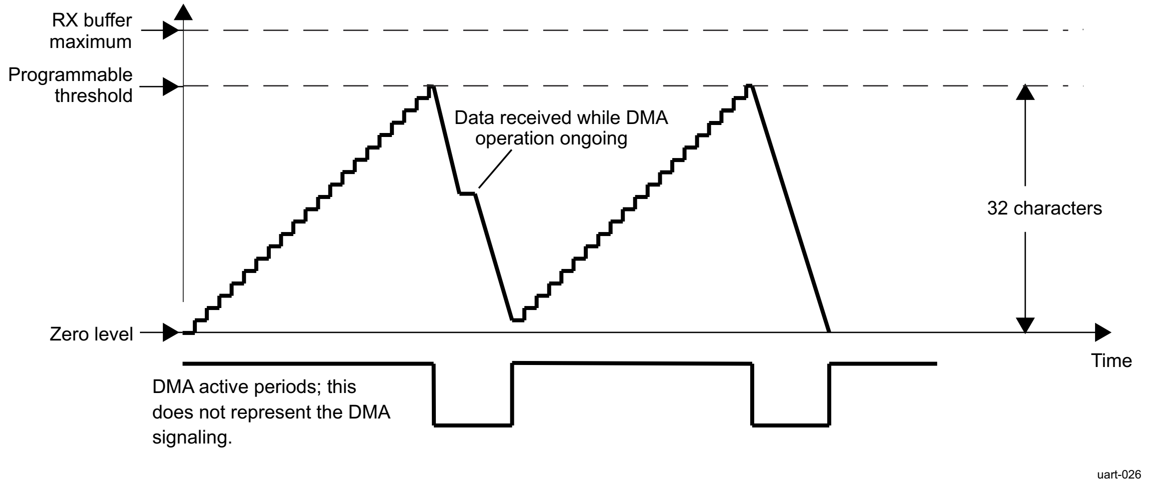

Figure 12-113. UART Receive FIFO DMA Request Generation (32 Characters)

In receive mode, a DMA request is generated when the RX FIFO reaches its threshold level defined in the trigger level register (UART_TLR). This request is deasserted when the number of bytes defined by the threshold level is read by the device DMA controllers.

In transmit mode, a DMA request is automatically asserted when the TX FIFO is empty. This request is deasserted when the number of bytes defined by the number of spaces in the UART_TLR register is written by the device DMA controllers. If an insufficient number of characters is written, the DMA request stays active.

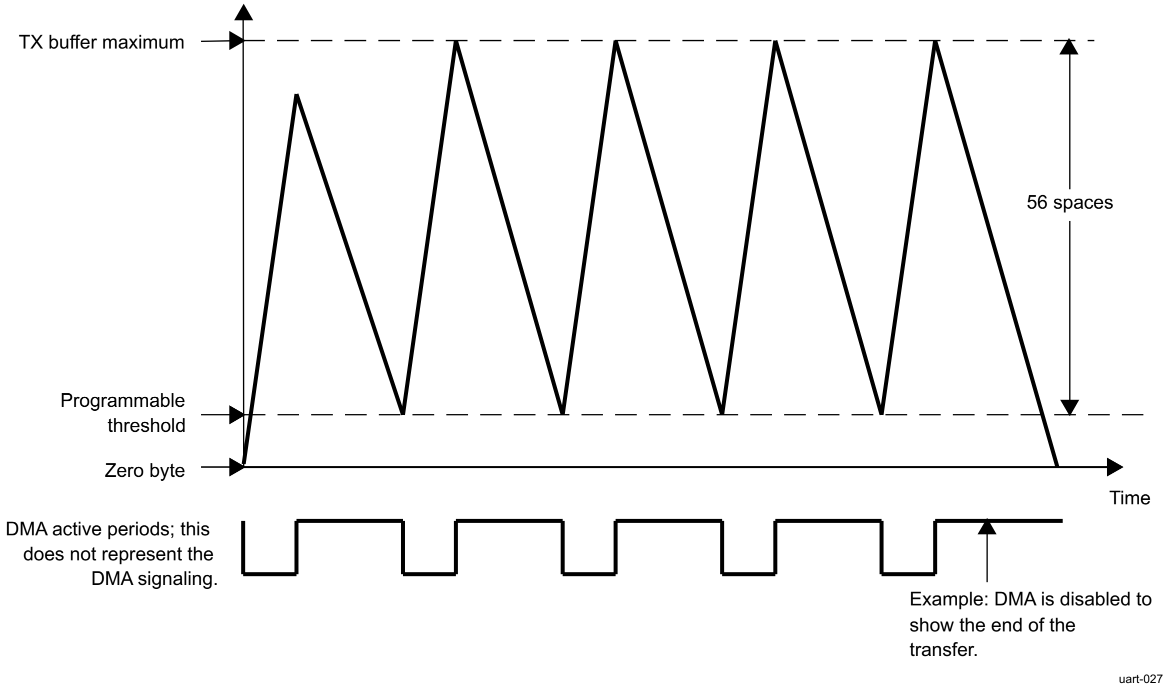

Figure 12-114. UART Transmit FIFO DMA Request Generation (56 Spaces)

The DMA request is again asserted if the FIFO can receive the number of bytes defined by the UART_TLR register.

The threshold can be programmed in a number of ways. Figure 12-114 shows a DMA transfer operating with a space setting of 56 that can arise from using the auto settings in the UART_FCR[5-4] TX_FIFO_TRIG bit field or the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field concatenated with the TX_FIFO_TRIG bit field.

The setting of 56 spaces in the UART module must correlate with the settings of the device DMA controllers, so that the buffer does not overflow (program the DMA request size of the LH controller to equal the number of spaces in the UART module).

Figure 12-115 shows an example with eight spaces to show the buffer level crossing the space threshold. The LH DMA controller settings must correspond to those of the UART module.

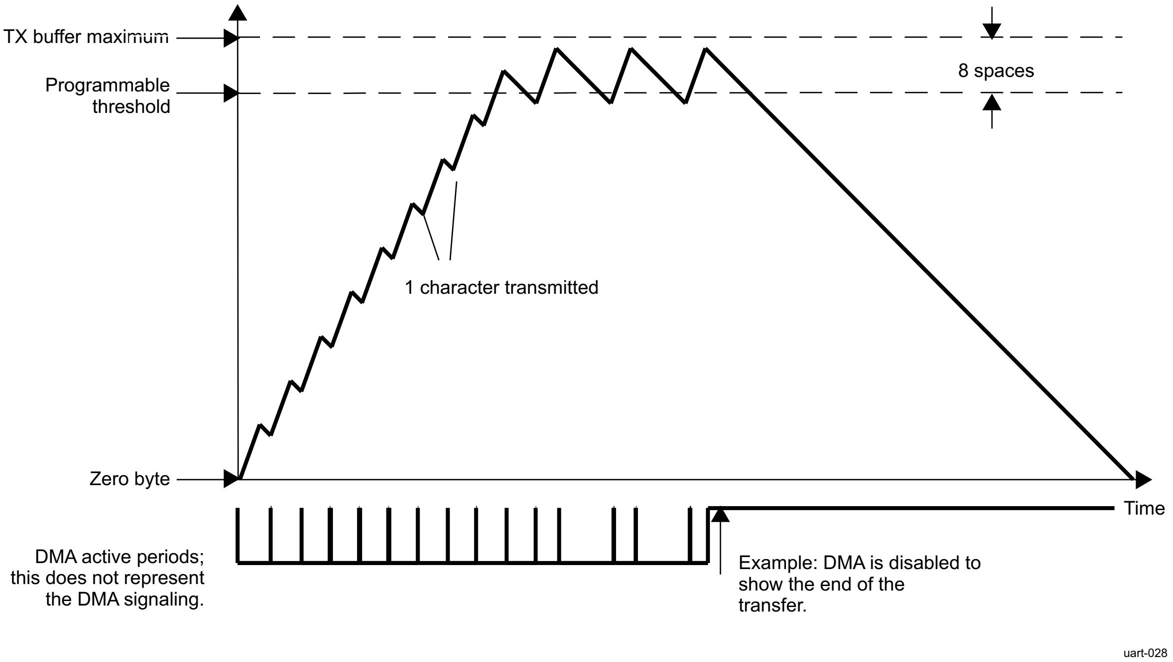

Figure 12-115. UART Transmit FIFO DMA Request Generation (8 Spaces)

The next example shows the setting of one space that uses the DMA for each transfer of one character to the transmit buffer (see Figure 12-116). The buffer is filled faster than the baud rate at which data is transmitted to the TX pin. Eventually, the buffer is completely full and the DMA operations stop transferring data to the transmit buffer.

On two occasions, the buffer holds the maximum amount of data words; shortly after this, the DMA is disabled to show the slower transmission of the data words to the TX pin. Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UART_DLL and UART_DLH registers.

The DMA settings must correspond to the system LH DMA controller settings to ensure correct operation of this logic.

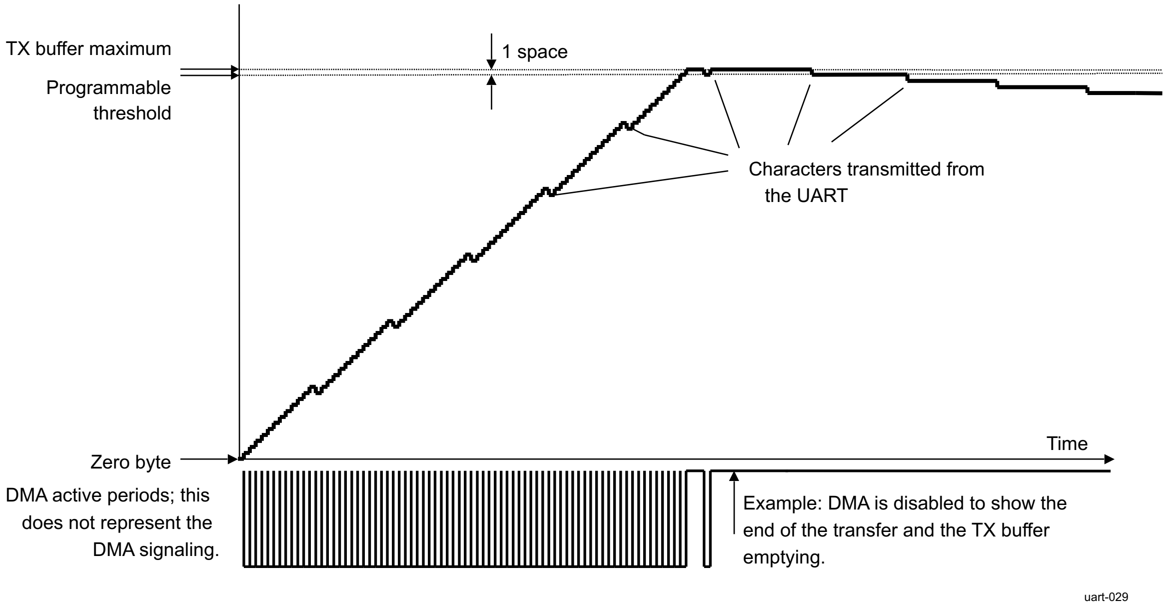

Figure 12-116. UART Transmit FIFO DMA Request Generation (1 Space)

The final example illustrates the setting of eight spaces but setting the TX DMA threshold directly by setting UART_MDR3[1] NONDEFAULT_FREQ bit and UART_TX_DMA_THRESHOLD register (see Figure 12-117). In the example, the UART_TX_DMA_THRESHOLD[5-0] TX_DMA_THRESHOLD = 3 and the trigger level is 8. The buffer is filled at a faster rate than the BAUD rate transmits data to the TX pin. The buffer is filled with 8 bytes and the DMA operations stop transferring data to the transmit buffer. When the buffer is emptied to the threshold level by transmission, the DMA operation activates again to fill the buffer with 8 bytes.

Eventually, the buffer will be emptied at the rate specified by the BAUD Rate settings of the UART_DLL and UART_DLH registers.

If the selected threshold level + trigger level exceeds max buffer size, then the original TX DMA threshold method is used to prevent TX overrun, regardless of the UART_MDR3[1] NONDEFAULT_FREQ value.

The DMA settings should correspond to the system Local Host DMA controller settings in order to ensure the correct operation of this logic.

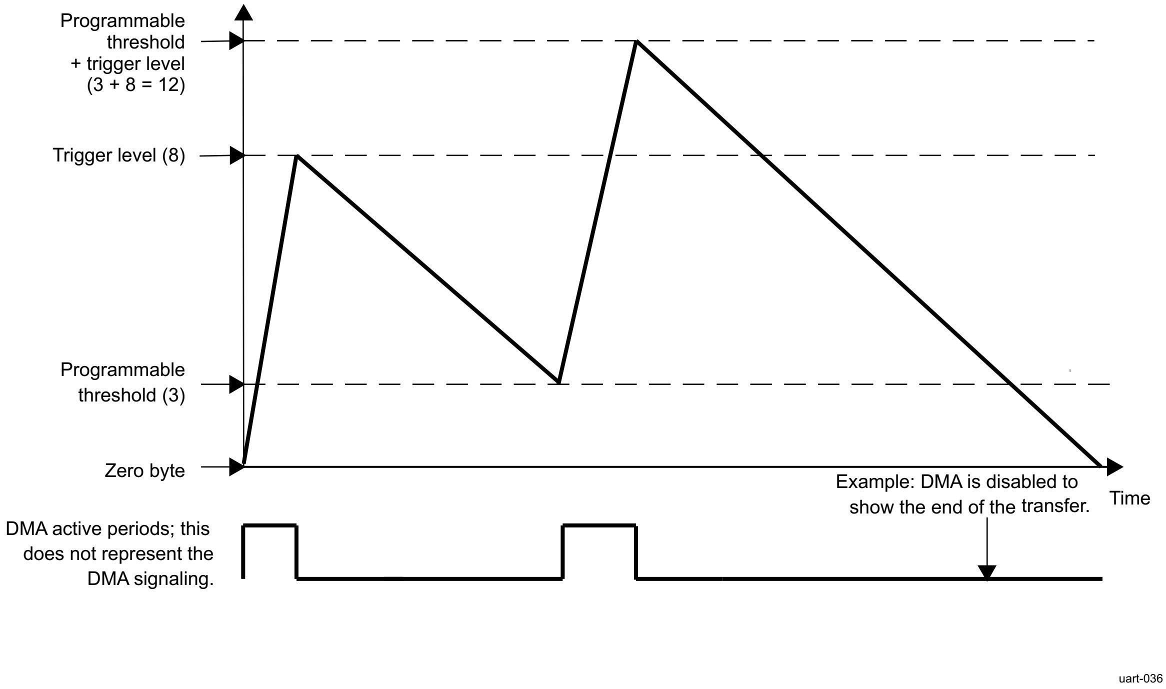

Figure 12-117. UART Transmit FIFO DMA Request Generation Using Direct TX DMA Threshold Programming. (Threshold = 3; Spaces = 8)

12.2.4.4.6.4.3 DMA Transmission

Figure 12-118 shows DMA transmission.

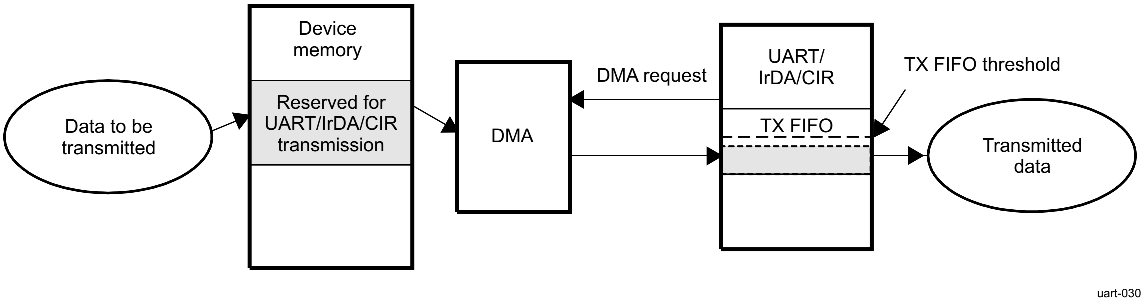

Figure 12-118. DMA Transmission

1. Data to be transmitted are put in the device memory reserved for UART transmission by the DMA:
   a. Until the TX FIFO trigger level is not reached, a DMA request is generated
   b. An element (1 byte) is transferred from the SDRAM to the TX FIFO at each DMA request (DMA element synchronization).
2. Data in the TX FIFO are automatically transmitted.
3. The end of the transmission is signaled by the UART_THR empty (TX FIFO empty).

Note

In IrDA mode, the transmission does not end immediately after the TX FIFO empties, at which point the last data byte, the CRC field, and the stop flag still must be transmitted; thus, the end of transmission occurs a few milliseconds after the UART_THR register empties.

12.2.4.4.6.4.4 DMA Reception

Figure 12-119 shows DMA reception.

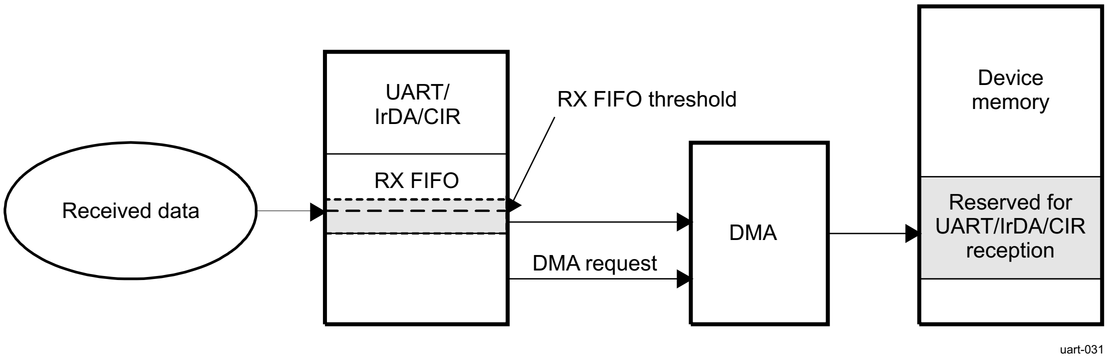

Figure 12-119. DMA Reception

1. Enable the reception.
2. Received data are put in the RX FIFO.
3. Data are transferred from the RX FIFO to the device memory by the DMA:
    a. At each received byte, the RX FIFO trigger level (one character) is reached and a DMA request is generated.
    b. An element (1 byte) is transferred from the RX FIFO to the SDRAM at each DMA request (DMA element synchronization).
4. The end of the reception is signaled by the EOF interrupt.

12.2.4.4.7 UART Mode Selection

12.2.4.4.7.1 Register Access Modes

12.2.4.4.7.1.1 Operational Mode and Configuration Modes

Register access depends on the register access mode, although register access modes are not correlated to functional mode selection. Three different modes are available:

- Operational mode
- Configuration mode A
- Configuration mode B

Operational mode is the selected mode when the function is active; serial data transfer can be performed in this mode.

Configuration mode A and configuration mode B are used during module initialization steps. These modes enable access to configuration registers, which are hidden in the operational mode. The modes are used when the module is inactive (no serial data transfer processed) and only for initialization or reconfiguration of the module.

The value of the UART_LCR register determines the register access mode (see Table 12-104).

Table 12-104. UART Register Access Mode Programming (Using UART_LCR)

Mode	Condition
Configuration mode A	UART_LCR[7] = 0x1 and UART_LCR[7-0] != 0xBF
Configuration mode B	UART_LCR[7] = 0x1 and UART_LCR[7-0] = 0xBF
Operational mode	UART_LCR[7] = 0x0

12.2.4.4.7.1.2 Register Access Submode

In each access register mode (operational mode or configuration mode A/B), some register accesses are conditional on the programming of a submode (MSR_SPR, TCR_TLR, and XOFF). These registers are identified in Table 12-127, *UART Load FIFO Triggers Defined by the Concatenated Value*.

Table 12-105 through Table 12-107 summarize the register access submodes.

Table 12-105. UART Subconfiguration Mode A Summary

Mode	Condition
MSR_SPR	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

Table 12-106. UART Subconfiguration Mode B Summary

Mode	Condition
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1
XOFF	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)

Table 12-107. UART Suboperational Mode Summary

Mode	Condition
MSR_SPR	UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

12.2.4.4.7.1.3 Registers Available for the Register Access Modes

Table 12-108 lists the names of the register bits in each access register mode. Gray shading indicates that the register does not depend on the register access mode (available in all modes).

Table 12-108. UART Register Access Mode Overview

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART	UART_IER_UART
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART	UART_FCR
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART	–
0x018	UART_MSR / UART_TCR	UART_TCR	UART_TCR / UART_XOFF1	UART_TCR / UART_XOFF1	UART_MSR / UART_TCR	UART_TCR
0x01C	UART_SPR / UART_TLR	UART_SPR / UART_TLR	UART_TLR / UART_XOFF2	UART_TLR / UART_XOFF2	UART_SPR / UART_TLR	UART_SPR / UART_TLR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	UART_UASR	–	UART_UASR	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR

Table 12-108. UART Register Access Mode Overview (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

12.2.4.4.7.2 UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection

To select a mode, set the UART_MDR1[2:0] MODE_SELECT bit field (see Table 12-109).

Table 12-109. UART Mode Selection

Value	Mode
0x0:	UART 16× mode
0x1:	SIR mode
0x2:	UART 16× auto-baud
0x3:	UART 13× mode
0x4:	MIR mode
0x5:	FIR mode
0x6:	CIR mode

MODE_SELECT is effective when the module is in operational mode (see Section 12.2.4.4.7.1 , *Register Access Modes*).

To select a RS-485 mode, set the UART_MDR3[4] DIR_EN bit field to 0x1.

12.2.4.4.7.2.1 Registers Available for the UART Function

Only the registers listed in Table 12-110 are used for the UART function.

Table 12-110. UART Mode Register Overview

Address Offset	Registers(1)(2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (UART)	UART_IER_UART (UART)
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (UART)	UART_FCR (UART)

Table 12-110. UART Mode Register Overview (continued)

Address Offset	Registers[1][2]					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	**Write**	**Read**	**Write**	**Read**	**Write**
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART (UART)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (UART)	–
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_XOFF1/ UART_TCR	UART_XOFF1/ UART_TCR	UART_MSR/ UART_TCR	UART_TCR
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR/ UART_XOFF2	UART_TLR/ UART_XOFF2	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	–	–	–	–	–	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	UART_UASR	–	UART_UASR	–	–	–
0x03C	–	–	–	–	–	–
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	–	–
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

12.2.4.4.7.2.2 Registers Available for the IrDA Function

Only the registers listed in Table 12-111 are used for the IrDA function.

Table 12-111. IrDA Mode Register Overview

Address Offset	Registers(1)(2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (IrDA)	UART_IER_UART (IrDA)
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (IrDA)	UART_FCR (IrDA)
0x00C	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	UART_XON1_ADDR1	UART_XON1_ADDR1	–	–
0x014	UART_LSR_UART (IrDA)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (IrDA)	–
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/ UART_TCR	UART_TCR
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR	UART_TLR	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	–	–	–	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(IrDA) notation indicates that the register exists for other functions (UART or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the IrDA function.

12.2.4.4.7.2.3 Registers Available for the CIR Function

Only the registers listed in Table 12-112 are used for the CIR function.

Table 12-112. CIR Mode Register Overview

Address Offset	**Registers**[1][2]					
	Configuration Mode A		**Configuration Mode B**		**Operational Mode**	
	Read	**Write**	**Read**	**Write**	**Read**	**Write**
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	–	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (CIR)	UART_IER_UART (CIR)
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART (CIR)	UART_FCR (CIR)
0x00C	UART_LCR	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	–	–	–	–
0x014	UART_LSR_UART (CIR)	–	–	–	UART_LSR_UART (CIR)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	UART_RESUME	–	UART_RESUME	–	UART_RESUME	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	–	–	–	–	–	–
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(CIR) notation indicates that the register exists for other functions (IrDA or UART), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the CIR function.

12.2.4.4.8 UART Protocol Formatting

12.2.4.4.8.1 UART Mode

12.2.4.4.8.1.1 UART Clock Generation: Baud Rate Generation

The UART function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-120 shows the baud rate generator and associated controls.

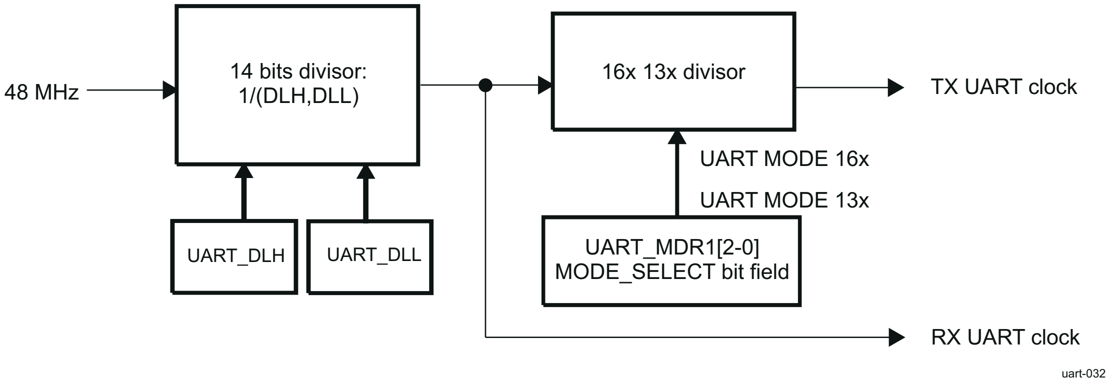

Figure 12-120. UART Baud Rate Generation

CAUTION

Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), UART_MDR1[2-0] MODE_SELECT = DISABLE must be set to 0x7. Failure to observe this rule can result in unpredictable module behavior.

12.2.4.4.8.1.2 Choosing the Appropriate Divisor Value

Two divisor values are:

- UART 16× mode: Divisor value = Operating frequency / (16× baud rate)
- UART 13× mode: Divisor value = Operating frequency / (13× baud rate)

Table 12-113 describes the UART baud rate settings.

Table 12-113. UART Baud Rate Settings (48MHz, 160MHz, 192MHz Clock)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
0.3kbps	16x	48	10000	0x27, 0x10	0.3kbps	0
0.6kbps	16x	48	5000	0x13, 0x88	0.6kbps	0
1.2kbps	16x	48	2500	0x09, 0xC4	1.2kbps	0
2.4kbps	16x	48	1250	0x04, 0xE2	2.4kbps	0
4.8kbps	16x	48	625	0x02, 0x71	4.8kbps	0
9.6kbps	16x	48	312	0x01, 0x38	9.615385kbps	-0.16
9.6kbps	16x	192	1250	0x04, 0xE2	9.6kbps	0
14.4kbps	16x	48	208	0x00, 0xD0	14.42308kbps	-0.16
19.2kbps	16x	192	625	0x02, 0x71	19.2kbps	0
28.8kbps	16x	48	104	0x00, 0x68	28.84615kbps	-0.16
38.4kbps	16x	48	78	0x00, 0x4E	38.46154kbps	-0.16
57.6kbps	16x	48	52	0x00, 0x34	57.69231kbps	-0.16
115.2kbps	16x	48	26	0x00, 0x1A	115.3846kbps	-0.16

Table 12-113. UART Baud Rate Settings (48MHz, 160MHz, 192MHz Clock) (continued)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
230.4kbps	16x	48	13	0x00, 0x0D	230.7692kbps	-0.16
460.8kbps	13x	48	8	0x00, 0x08	461.5385kbps	-0.16
921.6kbps	13x	48	4	0x00, 0x04	923.0769kbps	-0.16
1.843Mbps	13x	48	2	0x00, 0x02	1.846154Mbps	-0.17
2.5Mbps	16x	160	4	0x00, 0x04	2.5Mbps	0
3.0Mbps	16x	48	1	0x00, 0x01	3.0Mbps	0
3.6884Mbps	13x	48	1	0x00, 0x01	3.692308Mbps	-0.11
4Mbps	16x	192	3	0x00, 0x03	4Mbps	0
5Mbps	16x	160	2	0x00, 0x02	5Mbps	0
10Mbps	16x	160	1	0x00, 0x01	10Mbps	0
12Mbps	16x	192	1	0x00, 0x01	12Mbps	0

12.2.4.4.8.1.3 UART Data Formatting

The UART can use hardware flow control to manage transmission and reception. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS output and CTS input signals.

The UART is enhanced with the autobauding function. In control mode, autobauding lets the speed, the number of bits per character, and the parity selected be set automatically.

12.2.4.4.8.1.3.1 Frame Formatting

When autobauding is not used, frame format attributes must be defined in the UART_LCR register.

Character length is specified using the UART_LCR[1-0] CHAR_LENGTH bit field.

The number of stop-bits is specified using the UART_LCR[2] NB_STOP bit.

The parity bit is programmed using the UART_LCR[5-3] PARITY_EN, UART_LCR[5-3] PARITY_TYPE_1, and UART_LCR[5-3] PARITY_TYPE_2 bit fields (see Table 12-114).

Table 12-114. UART Parity Bit Encoding

PARITY_EN	PARITY_TYPE_1	PARITY_TYPE_2	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

12.2.4.4.8.1.3.2 Hardware Flow Control

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled and disabled independently by programming the UART_EFR[7] AUTO_CTS_EN and UART_EFR[6] AUTO_RTS_EN bit fields, respectively.

With auto-CTS, CTS signal must be active before the module can transmit data.

Auto-RTS activates the RTS output only when there is enough room in the RX FIFO to receive data. It deactivates the RTS output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the UART_TCR register determine the levels at which RTS is activated and deactivated.

If auto-CTS and auto-RTS are enabled, data transmission does not occur unless the RX FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If auto-CTS and auto-RTS are not enabled, overrun errors occur if the transmit data rate exceeds the RX FIFO latency.

- Auto-RTS:

  Auto-RTS data flow control originates in the receiver block. The RX FIFO trigger levels used in auto-RTS are stored in the UART_TCR register. RTS is active if the RX FIFO level is below the HALT trigger level in the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field. When the RX FIFO HALT trigger level is reached, RTS is deasserted. The sending device (for example, another UART) can send an additional byte after the trigger level is reached because it may not recognize the deassertion of RTS until it begins sending the additional byte.

  RTS is automatically reasserted when the RX FIFO reaches the RESUME trigger level programmed by the UART_TCR[7-4] RX_FIFO_TRIG_START bit field. This reassertion requests the sending device to resume transmission.

  In this case, RTS is an active-low signal.
- Auto-CTS:

  The transmitter circuitry checks CTS before sending the next data byte. When CTS is active, the transmitter sends the next byte. To stop the transmitter from sending the next byte, CTS must be deasserted before the middle of the last stop-bit currently sent.

  The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the CTS state changes do not have to trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO, and a receiver overrun error can result.

  In this case, CTS is an active-low signal.

12.2.4.4.8.1.3.3 Software Flow Control

Software flow control is enabled through the enhanced feature register (UART_EFR) and the modem control register (UART_MCR). Different combinations of software flow control can be enabled by setting different combinations of the UART_EFR[3-0] bit field (see Table 12-115).

Two other enhanced features relate to software flow control:

- XON-any function (UART_MCR[5] XON_EN): Operation resumes after receiving any character after the XOFF character is recognized. If special character detect is enabled and special character is received after XOFF1, it does not resume transmission. The special character is stored in the RX FIFO.

Note

The XON-any character is written into the RX FIFO even if it is a software flow character.

- Special character (UART_EFR[5] SPECIAL_CHAR_DETEC T): Incoming data is compared to XOFF2. When the special character is detected, the XOFF interrupt (UART_IIR_UART) is set, but it does not halt transmission. The XOFF interrupt is cleared by a read of UART_IIR_UART. The special character is transferred to the RX FIFO. Special character does not work with XON2, XOFF2, or sequential XOFFs.

Table 12-115. UART_EFR[3:0] Software Flow Control Options

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit XON1, XOFF1
0	1	X	X	Transmit XON2, XOFF2
1	1	X	X	Transmit XON1, XON2: XOFF1, XOFF2(1)
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares XON1, XOFF1
X	X	0	1	Receiver compares XON2, XOFF2

Table 12-115. UART_EFR[3:0] Software Flow Control Options (continued)

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
X	X	1	1	Receiver compares XON1, XON2: XOFF1, XOFF2(1)

(1) In these cases, the XON1 and XON2 characters or the XOFF1 and XOFF2 characters must be transmitted/received sequentially with XON1/XOFF1 followed by XON2/XOFF2.
XON1 is defined in the UART_XON1_ADDR1[7-0] XON_WORD1 bit field. XON2 is defined in the UART_XON2_ADDR2[7-0] XON_WORD2 bit field.
XOFF1 is defined in the UART_XOFF1[7-0] XOFF_WORD1 bit field. XOFF2 is defined in the UART_XOFF2[7-0] XOFF_WORD2 bit field.

12.2.4.4.8.1.3.3.1 Receive (RX)

When software flow control operation is enabled, the UART compares incoming data with XOFF1/2 programmed characters (in certain cases, XOFF1 and XOFF2 must be received sequentially). When the correct XOFF characters are received, transmission stops after transmission of the current character completes. Detection of XOFF also sets the UART_IIR_UART[4] bit (if enabled by UART_IER_UART[5]) and causes the interrupt line to go low.

To resume transmission, an XON1/2 character must be received (in certain cases, XON1 and XON2 must be received sequentially). When the correct XON characters are received, the UART_IIR_UART[4] bit is cleared and the XOFF interrupt disappears.

Note

When a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RX FIFO.

When XON-any and special character detect are disabled and software flow control is enabled, no valid XON or XOFF characters are written to the RX FIFO. For example, when UART_EFR[1-0] = 0x2, if XON1 and XOFF1 characters are received, they are not written to the RX FIFO.

When pairs of software flow characters are programmed to be received sequentially (UART_EFR[1-0] = 0x3), the software flow characters are not written to the RX FIFO if they are received sequentially. However, received XON1/XOFF1 characters must be written to the RX FIFO if the subsequent character is not XON2/XOFF2.

12.2.4.4.8.1.3.3.2 Transmit (TX)

Two XOFF1 characters are transmitted when the RX FIFO passes the trigger level programmed by UART_TCR[3-0] RX_FIFO_TRIG_HALT. As soon as the RX FIFO reaches the trigger level programmed by UART_TCR[7-4] RX_FIFO_TRIG_START, two XON1 characters are sent, so the data transfer recovers.

Note

If software flow control is disabled after an XOFF character is sent, the module transmits XON characters automatically to enable normal transmission.

The transmission of XOFF(s)/XON(s) follows the same protocol as transmission of an ordinary byte from the TX FIFO. This means that even if the word length is 5, 6, or 7 characters, the 5, 6, or 7 LSBs of XOFF1/2 and XON1/2 are transmitted. The 5, 6, or 7 bits of a character are seldom transmitted, but this function is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously.

12.2.4.4.8.1.3.4 Autobauding Modes

In autobauding mode, the UART can extract transfer characteristics (speed, length, and parity) from an "at" (AT) command (ASCII code). These characteristics are used to receive data after an AT and to send data.

The following AT commands are valid:

AT	DATA	<CR>
at	DATA	<CR>
A/		
a/		

A line break during the acquisition of the sequence AT is not recognized, and an echo function is not implemented in hardware.

A/ and a/ are not used to extract characteristics, but they must be recognized because of their special meaning. A/ or a/ is used to instruct the software to repeat the last received AT command; therefore, an a/ always follows an AT, and transfer characteristics are not expected to change between an AT and an a/.

When a valid AT is received, AT and all subsequent data, including the final <CR> (0x0D), are saved to the RX FIFO. The autobaud state-machine waits for the next valid AT command. If an a/ (A/) is received, the a/ (A/) is saved in the RX FIFO and the state-machine waits for the next valid AT command.

On the first successful detection of the baud rate, the UART activates an interrupt to signify that the AT (upper or lower case) sequence is detected. The UART_UASR register reflects the correct settings for the baud rate detected. Interrupt activity can continue in this fashion when a subsequent character is received. Therefore, it is recommended that the software enable the RHR interrupt when using the autobaud mode.

The following settings are detected in autobaud mode with a module clock of 48 MHz:

- Speed:
  - 115.2K baud
  - 57.6K baud
  - 38.4K baud
  - 28.8K baud
  - 19.2K baud
  - 14.4K baud
  - 9.6K baud
  - 4.8K baud
  - 2.4K baud
  - 1.2K baud
- Length: 7 or 8 bits
- Parity: Odd, even, or space

Note

The combination of 7-bit character plus space parity is not supported.

Autobauding mode is selected when the UART_MDR1[2-0] MODE_SELECT bit field is set to 0x2. In UART autobauding mode, UART_DLL, UART_DLH, and UART_LCR[5-0] bit field settings are not used; instead, the UART_UASR register is updated with the configuration detected by the autobauding logic.

UASR Autobauding Status Register Use

This register is used to set up transmission according to the characteristics of the previous reception instead of the UART_LCR, UART_DLL, and UART_DLH registers when the UART is in autobauding mode.

To reset the autobauding hardware (to start a new AT detection) or to set the UART in standard mode (no autobaud), the UART_MDR1[2-0] MODE_SELECT bit field must be set to reset state (0x7) and then to the UART in autobauding mode (0x2) or to the UART in standard mode (0x0).

Use limitation:

- Only 7- and 8-bit characters (5- and 6-bit not supported)

- 7-bit character with space parity not supported
- Baud rate between 1200 and 115.2 bps (10 possibilities)

12.2.4.4.8.1.3.5 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4:2] bit field reflects the error bits (BI: break condition, FE: framing error, PE: parity error) of the character at the top of the RX FIFO (the next character to be read). Therefore, reading the UART_LSR_UART register and then reading the UART_RHR register identifies errors in a character.

Reading the UART_RHR register updates the BI, FE, and PE bits (see Table 12-99 for the UART mode interrupts).

The UART_LSR_UART[7] RX_FIFO_STS bit is set when there is an error in the RX FIFO and is cleared only when no errors remain in the RX FIFO.

Note

Reading the UART_LSR_UART register does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the UART_RHR register.

Reading the UART_LSR_UART register clears the OE bit if it is set (see Table 12-99 for the UART mode interrupts).

12.2.4.4.8.1.3.6 Overrun During Receive

Overrun during receive occurs if the RX state-machine tries to write data into the RX FIFO when it is already full. When overrun occurs, the device interrupts the Host CPU with the UART_IIR_UART[5-1] IT_TYPE bit field set to 0x3 (receiver line status error) and discards the remaining portion of the frame.

Overrun also causes an internal flag to be set, which disables further reception. Before the next frame can be received, the Host CPU must:

- Reset the RX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

12.2.4.4.8.1.3.7 Time-Out and Break Conditions

12.2.4.4.8.1.3.7.1 Time-Out Counter

An RX idle condition is detected when the receiver line (RX) is high for a time that equals 4x the programmed word length + 12 bits or manually configured amount of baud clocks, if a value other zero is set in the timeout register. RX is sampled midway through each bit.

For sleep mode, the counter is reset when there is activity on RX.

There are two modes of operation:

- In default operation on the UART_EFR2[6] TIMEOUT_BEHAVE is set to 0. For the time-out interrupt, the counter counts only when there is data in the RX FIFO, and the count is reset when there is activity on RX or when the UART_RHR register is read.
- Optionally, for choose to enable the timeout counter even if no character has been received by setting UART_EFR2[6] TIMEOUT_BEHAVE bit. This will generate periodic interrupts if the RX line remains idle. In this mode the counter will auto-reset when a timeout has been reached. Reading the UART_IIR_UART will clear the interrupt, but not the counter.

12.2.4.4.8.1.3.7.2 Break Condition

When a break condition occurs, TX is pulled low. A break condition is activated by setting the UART_LCR[6] BREAK_EN bit. The break condition is not aligned on word stream (a break condition can occur in the middle of a character). The only way to send a break condition on a full character is:

1. Reset the TX FIFO (if enabled).
2. Wait for the transmit shift register to empty (the UART_LSR_UART[6] TX_SR_E bit is set to 1).

3. Take a guard time according to stop-bit definition.
4. Set the BREAK_EN bit to 1.

The break condition is asserted while the BREAK_EN bit is set to 1.

The time-out counter and break condition apply only to UART modem operation and not to IrDA/CIR mode operation.

12.2.4.4.8.2 RS-485 Mode

12.2.4.4.8.2.1 RS-485 External Transceiver Direction Control

The UART_MDR3[4] DIR_EN bit enables hardware control over an external transceiver to support RS-485. The direction signal comes across the DIR port. The direction polarity is controlled by the UART_MDR3[3] DIR_POL bit. The direction is determined by the hardware monitoring the TX FIFO and the TX shift register. When both are empty the transceiver is set to RX. There is a guard band delay counter of 3 bit clock cycles after the TX shift register is going empty to allow time for the stop bit to transition through the transceiver before a direction change to receive might be applied.

Figure 12-121 shows the direction control.

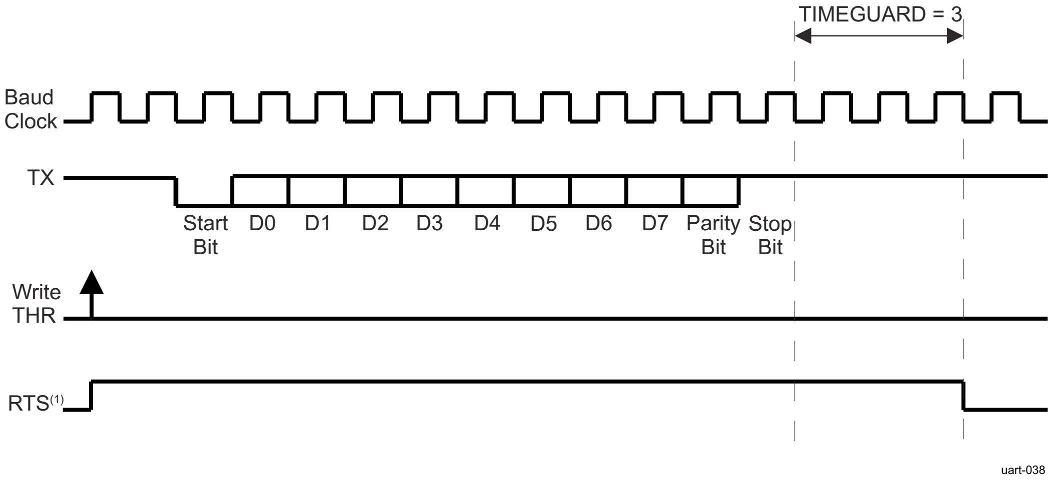

(1) Assumes DIR_POL = 1

Figure 12-121. RS-485 External Transceiver Direction Control

12.2.4.4.8.3 IrDA Mode

12.2.4.4.8.3.1 IrDA Clock Generation: Baud Generator

The IrDA function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-122 shows the baud rate generator and associated controls.

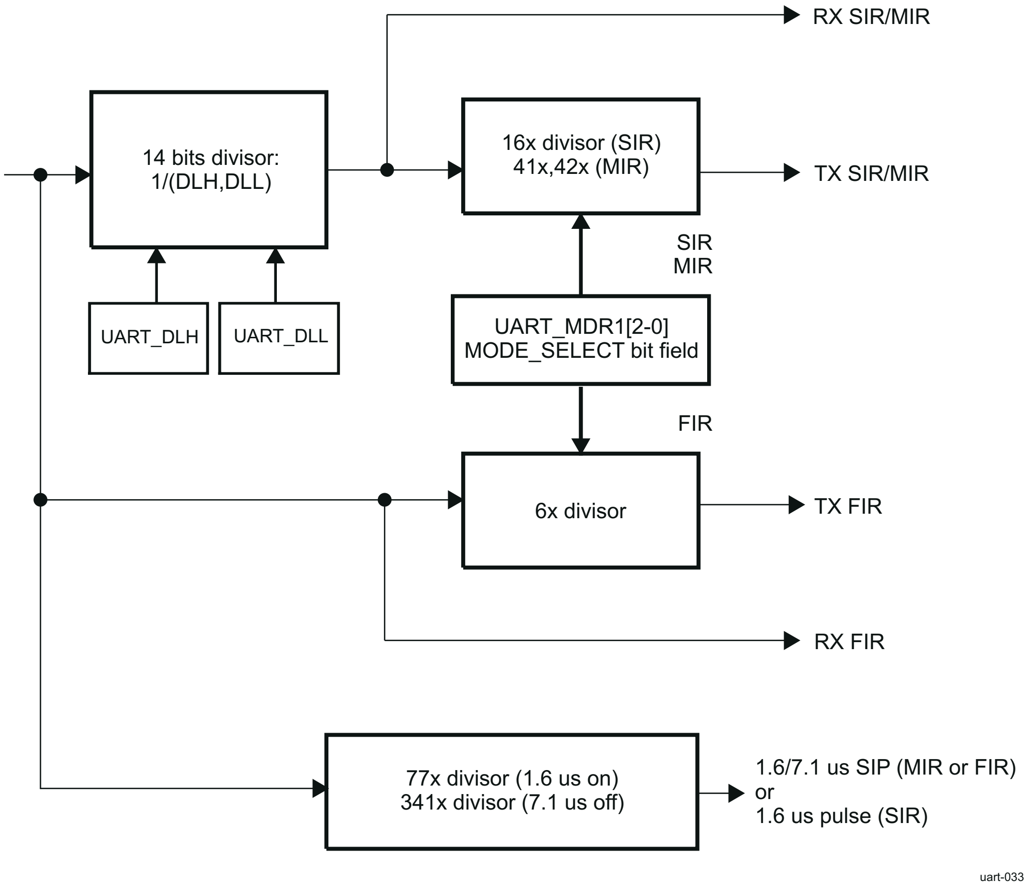

Figure 12-122. IrDA Baud Rate Generator

CAUTION

Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), MODE_SELECT=DISABLE (UART_MDR1[2-0] MODE_SELECT) must be set to 0x7). Failure to observe this rule can result in unpredictable module behavior.

12.2.4.4.8.3.2 Choosing the Appropriate Divisor Value

Three divisor values are:

- SIR mode: Divisor value = Operating frequency/(16× baud rate)
- MIR mode: Divisor value = Operating frequency/(41×/42× baud rate)
- FIR mode: Divisor value = None

Table 12-116 lists the IrDA baud rate settings.

Table 12-116. IrDA Baud Rate Settings

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
2.4 kbps	SIR	16x	3/16	1250	2.4 kbps	0	0	78.1 µs
9.6 kbps	SIR	16x	3/16	312	9.6153 kbps	+0.16	0	19.5 µs
19.2 kbps	SIR	16x	3/16	156	19.231 kbps	+0.16	0	9.75 µs
38.4 kbps	SIR	16x	3/16	78	38.462 kbps	+0.16	0	4.87 µs
57.6 kbps	SIR	16x	3/16	52	57.692 kbps	+0.16	0	3.25 µs
115.2 kbps	SIR	16x	3/16	26	115.38 kbps	+0.16	0	1.62 µs

Table 12-116. IrDA Baud Rate Settings (continued)

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
0.576 Mbps	MIR	41×/42×	1/4	2	0.5756 Mbps(1)	0	+1.63/-0.80	416 ns
1.152 Mbps	MIR	41×/42×	1/4	1	1.1511 Mbps(1)	0	+1.63/-0.80	208 ns
4 Mbps	FIR	6×	4 PPM	–	4 Mbps	0	0	125 ns

(1) Average value

Note

Baud rate error and source jitter table values do not include 48-MHz reference clock error and jitter.

12.2.4.4.8.3.3 IrDA Data Formatting

The methods described in this section apply to all IrDA modes (SIR, MIR, and FIR).

12.2.4.4.8.3.3.1 IR RX Polarity Control

The UART_MDR2[6] IRRXINVERT bit provides the flexibility to invert the RX pin in the UART to ensure that the protocol at the output of the transceiver has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.

12.2.4.4.8.3.3.2 IrDA Reception Control

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

Operation of the RX input can be disabled by the UART_ACREG[5] DIS_IR_RX bit.

12.2.4.4.8.3.3.3 IR Address Checking

In all IR modes, when address checking is enabled, only frames intended for the device are written to the RX FIFO. This restriction avoids receiving frames not meant for this device in a multipoint infrared environment. It is possible to program two frame addresses that the UART IrDA receives, with the UART_XON1_ADDR1[7-0] XON_WORD1 and UART_XON2_ADDR2[7-0] XON_WORD2 bit fields.

Setting the UART_EFR[0] bit to 1 selects address1 checking. Setting the UART_EFR[1] bit to 1 selects address2 checking. Setting the UART_EFR[1-0] bit field to 0 disables all address checking operations. If both bits are set, the incoming frame is checked for private and public addresses.

If address checking is disabled, all received frames write to the RX FIFO.

12.2.4.4.8.3.3.4 Frame Closing

A transmission frame can be terminated in two ways:

- Frame-length method: Set the UART_MDR1[7] FRAME_END_MODE bit to 0. The Host CPU writes the value of the frame length to the UART_TXFLH and UART_TXFLL registers. The device automatically attaches end flags to the frame when the number of bytes transmitted equals the value of the frame length.
- Set-EOT bit method: Set the UART_MDR1[7] FRAME_END_MODE bit to 1. The Host CPU writes 1 to the UART_ACREG[0] EOT bit just before it writes the last byte to the TX FIFO. When the Host CPU writes the last byte to the TX FIFO, the device internally sets the tag bit for that character in the TX FIFO. As the TX state-machine reads data from the TX FIFO, it uses this tag-bit information to attach end flags and correctly terminate the frame.

12.2.4.4.8.3.3.5 Store and Controlled Transmission

In store and controlled transmission (SCT) mode, the Host CPU starts writing data to the TX FIFO. Then, after writing a part of a frame (for a bigger frame) or an entire frame (a small frame; that is, a supervisory frame), the Host CPU writes 1 to the UART_ACREG[2] SCTX_EN bit (deferred TX start) to start transmission.

SCT mode is enabled by setting the UART_MDR1[5] SCT bit to 1. This transmission method differs from normal mode, in which data transmission starts immediately after data is written to the TX FIFO. SCT mode is useful for sending short frames without TX underrun.

12.2.4.4.8.3.3.6 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4-2] bit field reflects the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (the next frame status to be read).

The error is triggered by an interrupt (for IrDA mode interrupts, see Table 12-100). The STATUS FIFO must be read until empty (a maximum of eight reads is required).

12.2.4.4.8.3.3.7 Underrun During Transmission

Underrun during transmission occurs when the TX FIFO is empty before the end of the frame is transmitted. When underrun occurs, the device closes the frame with end flags but attaches an incorrect CRC value. The receiving device detects a CRC error and discards the frame; it can then ask for a retransmission.

Underrun also causes an internal flag to be set, which disables additional transmissions. Before the next frame can be transmitted, the Host CPU must:

- Reset the TX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

This function can be disabled by the UART_ACREG[4] DIS_TX_UNDERRUN bit, compensated by the extension of the stop-bit in transmission if the TX FIFO is empty.

12.2.4.4.8.3.3.8 Overrun During Receive

Overrun during receive for the IrDA mode has the same function as that for the UART mode (see Section 12.2.4.4.8.1.3.6 , *Overrun During Receive*).

12.2.4.4.8.3.3.9 Status FIFO

In IrDA modes, a status FIFO records the received frame status. When a complete frame is received, the length of the frame and the error bits associated with the frame are written to the status FIFO.

Reading the UART_SFREGH[3-0] MSB and UART_SFREGL[3-0] (LSB) bit fields obtains the frame length. The frame error status is read in the UART_SFLSR register. Reading the UART_SFLSR register increments the status FIFO read pointer. Because the status FIFO is eight entries deep, it can hold the status of eight frames.

The Host CPU uses the frame-length information to locate the frame boundary in the received frame data. The Host CPU can screen bad frames using the error status information and can later request the sender to resend only the bad frames.

This status FIFO can be used effectively in DMA mode because the Host CPU must be interrupted only when the programmed status FIFO trigger level is reached, not each time a frame is received.

12.2.4.4.8.3.3.10 Multi-drop Parity Mode with Address Match

Multi-drop mode is enabled in the UART_EFR2 register.

Address matching mode is only available with 8 bit character length setting. UART_LCR[1-0] CHAR_LENGTH bit fields should always be set to 0x11 (8 bits) prior to enabling the feature.

This mode allows the transmitter to send data on a line where multiple receivers are connected, when supported. In this mode, a set parity bit is used to mark an address, and a parity of 0 denotes data.

This setting affects how the parity is generated. Writing a 0x1 into the UART_ECR[0] A_MULTIDROP bit will set the parity bit for the next byte to be sent, which will then be considered an address, for sending a data frame, the UART_ECR[0] A_MULTIDROP bit has to be cleared.

On reception if the feature is enabled by setting the UART_EFR2[2] MULTIDROP bit to 0x1 incoming frames with parity set to 0x1 are treated as address frames and with parity set to 0x0 as data frames. The receiver will drop all data frames until a matching address frame was found.

The matching address is determined by the values set in UART_MAR, UART_MMR and UART_MBR registers and the value set in UART_EFR2[7] BROADCAST bit.

Table 12-117 summarizes the operation of address matching based on the mentioned values.

Table 12-117. Details of address matching

Received frame	Received parity	Frame type	UART_MAR	UART_MMR	UART_MBR	UART_EFR2[7] BROADCAST	Operation of receiver	Address matching
0xXX(2)	0	DATA	X(1)	X(1)	0xXX(2)	X(1)	Drops data until matching address found	N/A
0xXX(2)	1	ADDRESS	0xXX(2)	0x00	0xXX(2)	0	Matches any address	Yes
0xEF	1	ADDRESS	0xXX(2)	0xXX(2)	0xEF	1	Matches broadcast address	Yes
0x1A	1	ADDRESS	0x1A	0xFF	0xXX(2)	0	Single address match	Yes
0xF5	1	ADDRESS	0xF3	0xF9	0xXX(2)	0	Group address match	Yes

(1) X indicates a do not care bit value

(2) 0xXX indicates a do not care 8 bit hexadecimal value

The possible values for matching address can be calculated in the following way:

- Single and Group addresses can be formed by masking the UART_MAR registers value with the value set in the UART_MMR register, bits set to 0x0 in the UART_MMR register result in do not care values.
- Broadcast addresses can be set in the UART_MBR register if broadcast address is enabled in the UART_EFR2[7] BROADCAST bit, the module will match on received address frames containing the broadcast address.
- For more details, see example below:
  - UART_MAR: 0xF3, UART_MMR: 0xF9, UART_MBR: 0xFF
  - Single and Group addresses: 0xF1, 0xF3, 0xF5, 0xF7
  - Broadcast addresses: 0xFF

If an address match occurred the matching address value can be obtained from the UART_RHR register in the following way:

- If the FIFO is disabled or the threshold is set to 0x1, the matching address can be directly read from UART_RHR as the FIFO will not be overwritten.
- If the FIFO is enabled or the threshold is greater than 0x1, the matching address will be the latest frame in the FIFO with a parity error bit set.

For received data, the parity error bit in the UART_LSR_UART register is set when a bit with a parity of 0x1 is received indicating an address frame and the received address matches based on the values of UART_MAR, UART_MMR, UART_MBR and UART_EFR2[2] MULTIDROP bit.

In Multi-drop mode no parity is used, as the parity bit is used to differentiate address and data frames. The parity error bit is used for indicating an address match.

For enabling the interrupt generation for address matching UART_IER_UART[2] LINE_STS_IT bit has to be set to 0x1.

An interrupt for the matching address can be identified by reading the UART_IIR_UART[5-1] IT_TYPE bit fields, a value of 0x00011 indicates a receiver line status error. After the UART_LSR_UART[2] RX_PE bit has to be read, a value of 0x1 indicates that an address match occurred. The reception of a frame is indicated with a value of 0x1 in the UART_LSR_UART[0] RX_FIFO_E bit as the matching value is written into the FIFO regardless of the frame type (data or address). UART_LSR_UART[7] RX_FIFO_STS bit will also be set to 0x1 as the parity error bit is used to indicate a matching address.

Note that the operation of the UART_LSR_UART[2] RX_PE bit depends on the value set in UART_EFR2[2] MULTIDROP bit. If UART_EFR2[2] MULTIDROP bit is set to 0x0, UART_LSR_UART[2] RX_PE bit is used to indicate a received parity error. If UART_EFR2[2] MULTIDROP bit is set to 0x1, the receiver is in Multi-drop Address Match mode, thus the value in UART_LSR_UART[2] RX_PE bit is used to indicate an address match.

The interrupt is cleared the same way in both operation modes: reading the UART_LSR_UART register updates the values.

12.2.4.4.8.3.3.11 Time-guard

The time-guard feature enables the UART interface to operate with slow remote devices.

When set, it will insert a number of idle states between transmitting two characters, the length of which can be set in the UART_TIMEGUARD register. The value in the register defines the number of baud clocks of idle period to insert.

This idle state essentially acts like a long stop bit.

12.2.4.4.8.3.4 SIR Mode Data Formatting

This section provides specific instructions for SIR mode programming.

12.2.4.4.8.3.4.1 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

A transmission frame can be aborted by setting the UART_ACREG[1] ABORT_EN bit to 1. When this bit is set to 1, 0x7D and 0xC1 are transmitted and the frame is not terminated with CRC or stop flags.

When a 0x7D character followed immediately by a 0xC1 character is received without transparency, the receiver treats a frame as an aborted frame.

> **CAUTION**
>
> When the TX FIFO is not empty and the UART_MDR1[5] SCT bit is set to 1, the UART IrDA starts a new transfer with data of a previous frame when the aborted frame is sent. Therefore, the TX FIFO must be reset before sending an aborted frame.

12.2.4.4.8.3.4.2 Pulse Shaping

SIR mode supports the 3/16 or the 1.6-µs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse width method in the transmit mode.

12.2.4.4.8.3.4.3 SIR Free Format Programming

The SIR FF mode is selected by setting the module in the UART mode (UART_MDR1[2-0] MODE_SELECT = 0x0) and the UART_MDR2[3] PULSE bit to 1 to allow pulse shaping.

Because the bit format stays the same, some UART mode configuration registers must be set at specific values:

- UART_LCR[1-0] CHAR_LENGTH bit field = 0x3 (8 data bits)
- UART_LCR[2] NB_STOP bit = 0x0 (1 stop-bit)
- UART_LCR[3] PARITY_EN bit = 0x0 (no parity)

The UART mode interrupts are used for the SIR FF mode, but many are not relevant (XOFF, RTS, CTS, modem status register, etc.).

12.2.4.4.8.3.5 MIR and FIR Mode Data Formatting

This section describes common instructions for FIR and MIR mode programming.

At the end of a frame reception, the CPU reads the line status register (UART_LSR_UART) to detect errors in the received frame.

When the UART_MDR1[6] SIP_MODE bit is set to 1, the TX state-machine always sends one SIP at the end of a transmission frame. However, when the SIP_MODE bit is set to 0, SIP transmission depends on the UART_ACREG[3] SEND_SIP bit.

The CPU can set the SEND_SIP bit at least once every 500 ms. The advantage of this approach over the default approach is that the TX state-machine does not have to send the SIP at the end of each frame, thus reducing the overhead required.

12.2.4.4.8.4 CIR Mode

12.2.4.4.8.4.1 CIR Mode Clock Generation

Depending on the encoding method (variable pulse distance/biphase), the Host CPU must develop a data structure that combines 1 and 0 with a *t* period to encode the complete frame to transmit. This can then be transmitted to the infrared output with a modulation method, as shown in Figure 12-123.

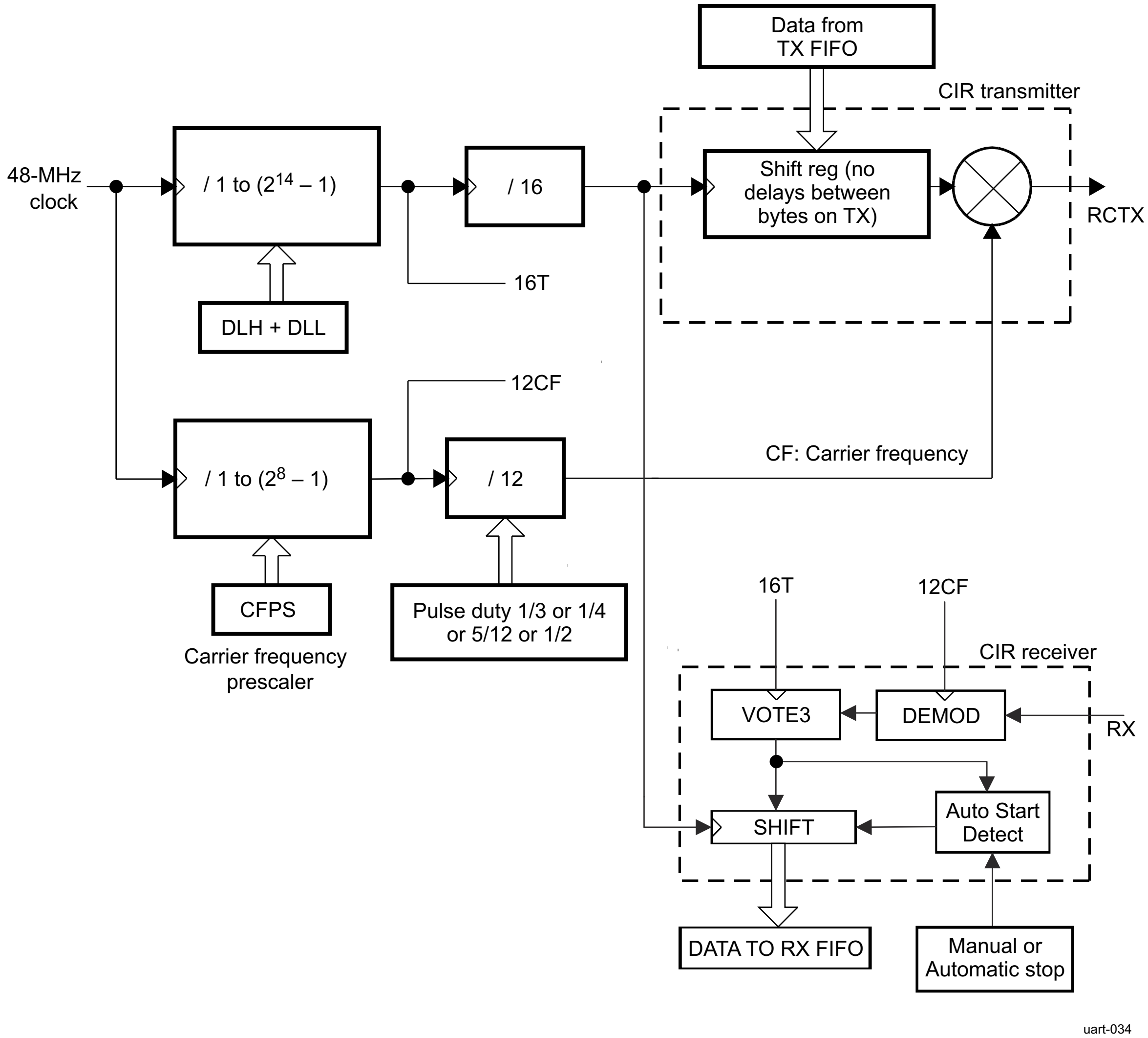

Figure 12-123. CIR Mode Block Components

Based on the requested modulation frequency, the UART_CFPS register must be set with the correct dividing value to provide an accurate pulse frequency:

Dividing value = (FCLK / 12) / MODfreq

Where:

FCLK = System clock frequency (48 MHz)

12 = Real value of baud multiple

MODfreq = Effective frequency of the modulation (MHz)

Example: For a targeted modulation frequency of 36 kHz, the value of CFPS must be set to 0x7 (decimal), which provides a modulation frequency of 36.04 kHz.

Note

The UART_CFPS register starts with a reset value of 105 (decimal), which translates to a frequency of 38.1 kHz.

The duty cycle of these pulses is user-defined by the pulse duty register bits in the UART_MDR2 register. Table 12-118 shows the duty cycle.

Table 12-118. CIR Duty Cycle

UART_MDR2[5-4] CIR_PULSE_MODE	Duty Cycle (High-Level)
00	1/4
01	1/3
10	5/12
11	1/2

12.2.4.4.8.4.2 CIR Data Formatting

The methods described in this section apply to all CIR modes.

12.2.4.4.8.4.2.1 IR RX Polarity Control

The IR RX polarity control for CIR mode has the same function as that for IrDA mode (see Section 12.2.4.4.8.3.3.1 , *IR RX Polarity Control*).

12.2.4.4.8.4.2.2 CIR Transmission

In transmission, the Host CPU software must exercise an element of real-time control to transmit data packets, each of which must be emitted at a constant delay from the start-bits of each individual packet. Thus, when sending a series of packets, the packet-to-packet delay must respect a specific delay. Two methods can be used to control this delay:

- Filling the TX FIFO with a number of zero bits that are transmitted with a *t* period
- Using an external system timer to control the delay between each start-of-frame or between the end of a frame and the start of the next one. This can be performed by:
  - Controlling the start of the frame using the UART_MDR1[5] SCT bit and the UART_ACREG[2] SCTX_EN bit, depending on the timer status
  - Using the UART_IIR_UART[5] TX_STATUS_IT interrupt bit to preload the next frame in the TX FIFO and to control the start of the timer (in case of control delay between the end of a frame and the start of the next frame)

12.2.4.4.8.4.2.3 CIR Reception

In reception, there are 2 ways to stop it

- The Host CPU can disable the reception by setting the UART_ACREG[5] DIS_IR_RX bit to 1. When it considers that the reception is finished because a large number of 0 has been received. To receive a new frame, the UART_ACREG[5] DIS_IR_RX bit must be set to 0.
- Using a specific mechanism, depending on the value set in the BOF length register (UART_EBLR), allows stopping automatically the reception. If the value set in the UART_EBLR register is different than 0, this features is enabled and count a number of bit received at 0. When the counter achieved the value defined in the UART_EBLR register, the reception is automatically stop and UART_IIR_CIR[2] RX_STOP_IT bit is set. When a 1 is detected on the RX pin, the reception is automatically enabled.

There is a limitation when receiving data in UART CIR mode. The IrDA transceivers on the market have a common characteristic that shrinks the hold time of the received modulation pulse. The UART filtering schema on receiving is based on the same encoding mechanism used in transmission.

For the following scenario:

- shift register period: 0.9us
- modulation frequency: 36kHz
- duty cycle: 1/4 of a modulation frequency period

So the data sent in those conditions would look like 7us pulses within 28us period. The UART expects to receive similar incoming data on receive, but available transceiver timing characteristics typically send 2us modulated pulses. Those will be filtered out and RX FIFO will not receive any data.

This does not affect UART CIR mode in transmission.

Note

The CIR RX demodulation can be bypassed by setting the UART_MDR3[0] DISABLE_CIR_RX_DEMOD bit.

12.2.4.5 UART Programming Guide

This section describes the procedure for operating the UART with FIFO and DMA or interrupts. This three-part procedure ensures the quick start of the UART. It does not cover every UART feature.

The first programming model covers software reset of the UART. The second programming model describes FIFO and DMA configuration. The last programming model describes protocol, baud rate, and interrupt configuration.

Note

Each programming model can be used independently of the other two; for instance, reconfiguring the FIFOs and DMA settings only.

Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 12.2.4.4.7.1 , *Register Access Modes*.

12.2.4.5.1 UART Global Initialization

12.2.4.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the UART module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the UART.

For more information, see , *UART Integration*.

12.2.4.5.1.2 UART Module Global Initialization

The procedure in Table 12-119 can be used to initialize UART when performing software reset.

Table 12-119. UART Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	UART_SYSC[1] SOFTRESET	1
Wait until reset is finished.	UART_SYSS[0] RESETDONE	=1

12.2.4.5.2 UART Mode selection

Table 12-120 describes how to set different register access mode.

Table 12-120. UART Configure Register Access Mode

Step	Register/Bit Field/Programming Model	Value
Set the register access mode A	UART_LCR[7] DIV_EN	1
	UART_LCR[7-0]	≠0xBF
Set the register access mode B	UART_LCR[7-0]	0xBF
Set the operational mode	UART_LCR[7] DIV_EN	0

12.2.4.5.3 UART Submode selection

This section describes how to set different register access submode.

Table 12-121. UART Configure Register Access Submode TCR_TLR

Step	Register/Bit Field/Programming Model	Value
Configure the submode TCR_TLR		
Configure mode B	see Table 12-120	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Configure mode A	see Table 12-120	0x1

Table 12-121. UART Configure Register Access Submode TCR_TLR (continued)

Step	Register/Bit Field/Programming Model	Value
Set the submode TCR_TLR	UART_MCR[6] TCR_TLR	1

Table 12-122. UART Configure Register Access Submode MSR_SPR

Step	Register/Bit Field/Programming Model	Value
First option: configure the submode MSR_SPR		
Configure mode B	see Table 12-120	
Set the submode MSR_SPR	UART_EFR[4] ENHANCED_EN	0
Second option: configure the submode MSR_SPR		
Configure mode B	see Table 12-120	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Set the submode MSR_SPR	UART_MCR[6] TCR_TLR	0

Table 12-123. UART Configure Register Access Submode XOFF

Step	Register/Bit Field/Programming Model	Value
Configure of the XOFF		
Configure B	see Table 12-120	
Set the submode XOFF	UART_EFR[4] ENHANCED_EN	0

12.2.4.5.4 UART Load FIFO trigger and DMA mode settings

12.2.4.5.4.1 DMA mode Settings

To enable and configure program the DMA mode, perform the following steps:

Table 12-124. DMA Mode Settings

Step	Register/Bit Field/Programming Model	Value
Set the option of DMA mode configuration	UART_SCR[0] DMA_MODE_CTL	-
IF Configure DMA mode 0 and 1	UART_SCR[0] DMA_MODE_CTL	=0
Select the DMA mode, for more information see Section 12.2.4.4.6.4	UART_FCR[3] DMA_MODE	-
IF Configure DMA mode from 0 to 3	UART_SCR[0] DMA_MODE_CTL	=1
Select the DMA mode, for more information see Section 12.2.4.4.6.4	UART_SCR[2-1] DMA_MODE_2	-

12.2.4.5.4.2 FIFO Trigger Settings

In this section is described configuration and settings of FIFO trigger level, which enable DMA and interrupt generation.

Table 12-125. Load FIFO Triggers Defined by the FCR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-121	0x-
Set the desire RX FIFO trigger level	UART_FCR[5-4] TX_FIFO_TRIG	0x-
Set the desire TX FIFO trigger level	UART_FCR[7-6] RX_FIFO_TRIG	0x-

Table 12-126. Load FIFO Triggers Defined by the TLR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-121	0x-
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA	0x-
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA	0x-

Table 12-127. Load FIFO Triggers Defined by the Concatenated Value

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-121	0x-
Set the register bit	UART_SCR[7] RX_TRIG_GRANU1	1
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA UART_FCR[7-6] RX_FIFO_TRIG	0x-
Set the register bit	UART_SCR[6] TX_TRIG_GRANU1	1
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA UART_FCR[5-4] TX_FIFO_TRIG	0x-

12.2.4.5.5 UART Protocol, Baud rate and interrupt settings

12.2.4.5.5.1 Baud rate settings

Table 12-128. UART Baud Rate Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Switch to register configuration mode B	see Table 12-120	
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-120	
Disable sleep mode	UART_IER_UART[4] SLEEP_MODE	0
Switch to register configuration mode A or B	see Table 12-120	
Set the appropriate divisor value	UART_DLL[7-0] CLOCK_LSB UART_DLH[5-0] CLOCK_MSB	0x-

12.2.4.5.5.2 Interrupt settings

Table 12-129. UART Interrupt Settings

Step	Register/Bit Field/Programming Model	Value
Switch to register configuration mode B	see Table 12-120	0x7
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-120	
Set the desired interrupt configuration (0: Disable the interrupt; 1: Enable the interrupt)	UART_IER_UART[7] CTS_IT UART_IER_UART[6] RTS_IT UART_IER_UART[5] XOFF_IT UART_IER_UART[4] SLEEP_MODE UART_IER_UART[3] MODEM_STS_IT UART_IER_UART[2] LINE_STS_IT UART_IER_UART[1] THR_IT UART_IER_UART[0] RHR_IT	0x-

12.2.4.5.5.3 Protocol settings

Load the desired protocol formatting (parity, stop-bit, character length) and switch to register operational mode.

Table 12-130. UART Protocol Settings

Step	Register/Bit Field/Programming Model	Value
Load desired protocol formatting, see Section 12.2.4.4.8.1.3.1 , *Frame Formatting*	UART_LCR[5] PARITY_TYPE_2 UART_LCR[4] PARITY_TYPE_1 UART_LCR[3] PARITY_EN UART_LCR[2] NB_STOP UART_LCR[1-0] PARITY_LENGTH	0x-

Table 12-130. UART Protocol Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Switch to register operational mode	UART_LCR[7] DIV_EN UART_LCR[6] BREAK_EN	0

12.2.4.5.5.4 UART/RS-485/IrDA(SIR/MIR/FIR)/CIR

Table 12-131. UART Mode Selection

Step	Register/Bit Field/Programming Model	Value
Load the desired UART/IrDA (SIR, MIR, FIR)/CIR modes, see Section 12.2.4.4.7.2 , *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR1[2-0] MODE_SELECT	0x-
Load the desire RS-485 mode, see Section 12.2.4.4.7.2 , *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR3[4] DIR_EN	0x1

12.2.4.5.5.5 UART Multi-drop Parity Address Match Mode Configuration

Table 12-132. UART Multi-drop Parity Address Match Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Disable receive mode	UART_ECR[3] RX_EN	0
Enable Multi-drop parity Address match mode	UART_EFR2[2] MULTIDROP	1
Set the matching device address	UART_MAR[7-0] ADDRESS	0x-
Set the address match masking	UART_MMR[7-0] MASK	0x-
Set the broadcast address match	UART_MBR[7-0] BROADCAST_ADDRESS	0x-
Enable broadcast address matching if needed	UART_EFR2[7] BROADCAST	1
Enable receive mode	UART_ECR[3] RX_EN	1

12.2.4.5.6 UART Hardware and Software Flow Control Configuration

This section describes the programming steps to enable and configure hardware and software flow control. Hardware and software flow control cannot be used at the same time.

12.2.4.5.6.1 Hardware Flow Control Configuration

Table 12-133. UART Hardware Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-121	0x7
Load the start and halt trigger value.	UART_TCR[7-4] AUTO_RTS_START UART_TCR[3-0] AUTO_RTS_HALT	0x-
Enable or disable receive and transmit hardware flow control mode.	UART_EFR[7] AUTO_CTS_EN UART_EFR[6] AUTO_RTS_EN	0x-

12.2.4.5.6.2 Software Flow Control Configuration

Table 12-134. UART Software Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Set the register access submode XOFF	see Table 12-123	
Load the software control characters	UART_XON1_ADDR1[7-0] XON_WORD1 UART_XON2_ADDR2[7-0] XON_WORD2 UART_XOFF1[7-0] XOFF_WORD1 UART_XOFF2[7-0] XOFF_WORD2	0x-
Set the register access submode TCR_TLR	see Table 12-121	
Enable or disable XON any function (0: Disable; 1: Enable).	UART_MCR[5] XON_EN	--

Table 12-134. UART Software Flow Control Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Load start and halt trigger value for software flow control	UART_TCR[7-4] AUTO_RTS_START	0x-
	UART_TCR[3-0] AUTO_RTS_HALT	
Enable or disable special character function (0: Disable; 1: Enable)	UART_EFR[5] SPEC_CHAR	0x-
Set the software flow control mode	UART_EFR[3-0] SW_FLOW_CONTROL	0x-

12.2.4.5.7 IrDA Programming Model

12.2.4.5.7.1 SIR mode

12.2.4.5.7.1.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with parity forced to 1, baud rate = 115.2 kbps, FIFOs disabled, 2 stop-bits, and 8-bit word length:

Table 12-135. SIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate(115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.1.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 6-byte frame with no parity, baud rate = 115.2 kbps, FIFOs disabled, 3/16 encoding, 2 stop-bits, and 7-bit word length:

Table 12-136. SIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 6 bytes	UART_TXFLL[7-0] TXFLL	0x06
Set the seven starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
Set SIR pulse width to be 1.6 μs	UART_ACREG[7] PULSE_TYPE	1

12.2.4.5.7.2 MIR mode

12.2.4.5.7.2.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-137. MIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (1.152 bps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set MIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force outputs DTR and RTS to active	UART_MCR[1-0]	0x3
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.2.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 60-byte frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-138. MIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 kbps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 60 bytes	UART_TXFLL[7-0] TXFLL	0x3C
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.2.4.5.7.3 FIR mode

12.2.4.5.7.3.1 Receive

The following programming model explains how to program the module to receive the IrDA frame with no parity, baud rate = 4 Mbps, FIFOs enabled, 8-bit word length.

Table 12-139. FIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB	0x0
	UART_DLH[7-0] CLOCK_MSB	
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.2.4.5.4 , *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x5
Set frame length	UART_RXFLL[7-0] RXFLL	0xA
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00

Table 12-139. FIR Mode Receive Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.3.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 4-byte frame with no parity, baud rate = 4 Mbps, FIFOs enabled, and 8-bit word length.

Table 12-140. FIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB UART_DLH[5-0] CLOCK_MSB	0x0
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.2.4.5.4 , *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Set FIR mode and enable auto-SIP mode	UART_MDR1[7-0]	0x45
Set frame length	UART_TXFLL[7-0] TXFLL	0x4
	UART_TXFLH[7-0] TXFLH	0x0
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	1
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.3 High-speed Serial Interfaces

This section describes the high-speed serial interfaces in the device.

12.3.1 Gigabit Ethernet Switch (CPSW3G)

This chapter describes the Gigabit Ethernet Switch (CPSW3G) subsystem in the device.

12.3.1.1 CPSW0 Overview

The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

Figure 12-124 shows the CPSW0 module overview.

Figure 12-124. CPSW0 Overview

12.3.1.1.1 CPSW0 Features

The 3-port CPSW0 subsystem provides the following features:

- Two Ethernet ports (port 1 and 2) with selectable RGMII and RMII interfaces and an internal Communications Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Cut through switch support
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
  - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
  - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
  - IEEE P802.3br Interspersing Express Traffic
  - IEEE 802.1Qbv Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE)
  - 512 ALE table entries
  - Configurable number of addresses plus VLANs
  - Wire rate lookup
  - Host controlled time-based aging and/or auto-aging
  - Spanning tree support
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive-based or destination-based Multicast and Broadcast rate limits
  - MAC address blocking
  - Source port locking
  - OUI (Vendor ID) host accept/deny feature
  - Configurable number of classifier/policers (32)
  - VLAN support
    - 802.1Q compliant
      - Auto add port VLAN for untagged frames on ingress
      - Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes

- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECDED)

12.3.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.3.1.1.3 CPSW Terminology

Terminology:

AVB	Audio Video Bridging
AVBTP	Audio Video Bridging Trasport Protocol
BCCA	Best Controller Clock Algorithm
CFI	Canonical Format Indicator
CPPI	Communications Port Programming Interface
CPSW	Common Platform Switch
DLR	Device Level Ring
DSCP	Differentiated Services Code Point
EEE	Energy Efficient Ethernet
EMAC	Ethernet Media Access Control
EOP	End of Packet
EOQ	End of Queue
IPG	Inter-Packet Gap
LPI	Low Power Indicator
MDIO	Management Data Input/Output
MOF	Middle of Frame
OUI	Organizationally Unique Identifier
PFC	Priority based Flow Control
PTP	Precision Time Protocol
RMON	Remote Monitoring
RTCP	RTP Control Protocol
RTP	Real-time Transport Protocol
SCR	Switched Central Resource
SRP	Stream Reservation Protocol
TOS	Type of Service
VLAN	Virtual Local Area Network

12.3.1.2 CPSW0 Environment

This section describes the CPSW0 external connections (environment).

12.3.1.2.1 CPSW0 RMII Interface

Figure 12-125 shows a device with integrated EMAC and MDIO interfaced via a RMII connection in a typical system. The individual CPSW0 and MDIO signals for the RMII interface are summarized in Table 12-141.

The CPSW0 module integrated in the device supports internal and external clock sources in RMII mode. Figure 12-125 shows the internal clock source for RMII_MHZ_50_CLK clock. It is 50 MHz clock source that is provided on the CLKOUT0 device pin. This clock has to be routed on the PCB to the RMII_REF_CLK device pin and the external PHY, RMII clock input.

For more information, refer to either the IEEE 802.3 standard or ISO/IEC 8802-3:2000(E).

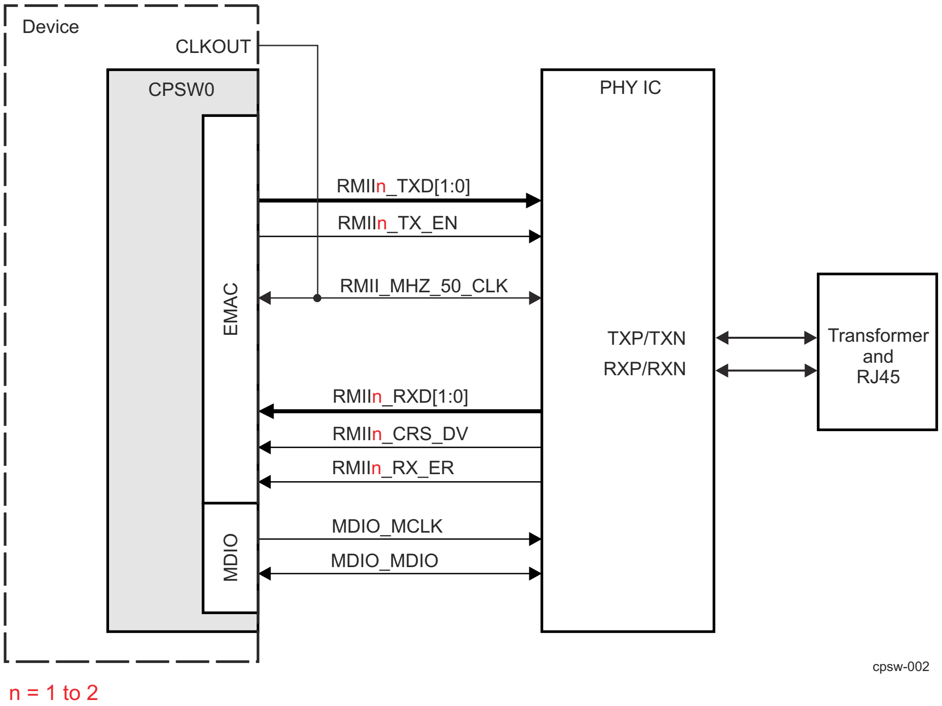

Figure 12-125. RMII Interface Typical Application (Internal Clock Source)

Figure 12-126 shows the external clock source for RMII_MHZ_50_CLK clock. In this case a 50 MHz clock is available on the PCB and it can be sourced from an oscillator or from the Ethernet PHY. This externally generated clock should be routed to both RMII_REF_CLK device pin and the external PHY, RMII clock input.

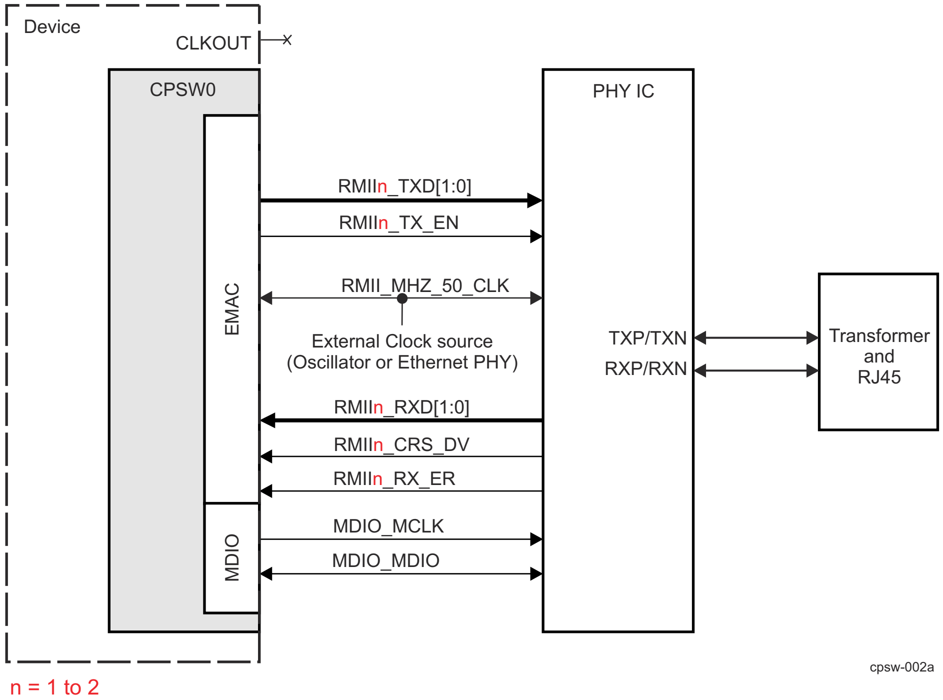

Figure 12-126. RMII Interface Typical Application (External Clock Source)

Table 12-141. RMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RMIIn_TXD[1:0]	RMIIn_TXD[1:0]	O	Transmit data. The transmit data pins are a collection of 2 bits of data. TXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_TX_EN is asserted.
RMIIn_TX_EN	RMIIn_TX_EN	O	RMII transmit enable. The transmit enable signal indicates that the RMIIn_TXD[1:0] pins are generating data for use by the PHY. RMIIn_TX_EN is synchronous to RMII_MHZ_50_CLK.
RMII_MHZ_50_CLK	RMII_REF_CLK	I	RMII 50MHz reference clock. The reference clock is used to synchronize all RMII signals. RMII_MHZ_50_CLK must be continuous and fixed at 50 MHz.
RMIIn_RXD[1:0]	RMIIn_RXD[1:0]	I	Receive data. The receive data pins are a collection of 2 bits of data. RXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_CRS_DV is asserted and RMIIn_RX_ER is de-asserted.
RMIIn_CRS_DV	RMIIn_CRS_DV	I	Carrier sense/receive data valid. Multiplexed signal between carrier sense and receive data valid.
RMIIn_RX_ER	RMIIn_RX_ER	I	Receive error. The receive error signal is asserted to indicate that an error was detected in the received frame.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO data pin.
MDIO_MDIO	MDIO0_MDIO	I/O	MDIO data pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output

(2) n 1 to 2

12.3.1.2.2 CPSW0 RGMII Interface

Figure 12-127 shows a device with integrated EMAC and MDIO interfaced via a RGMII connection in a typical system. The individual CPSW0 and MDIO signals for the RGMII interface are summarized in Table 12-142.

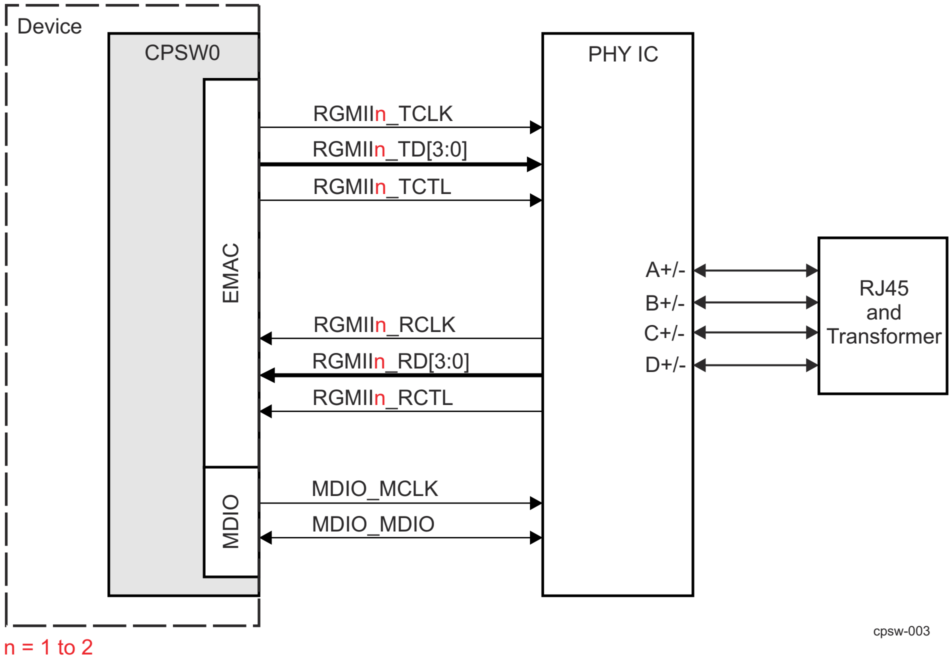

Figure 12-127. RGMII Interface Typical Application

Table 12-142. RGMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RGMIIn_TD[3:0]	RGMIIn_TD[3:0]	O	The transmit data pins are a collection of 4 bits of data. TD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_TCTL is asserted.
RGMIIn_TCTL	RGMIIn_TX_CTL	O	Transmit Control/enable. The transmit enable signal indicates that the TD pins are generating data for use by the PHY.
RGMIIn_TCLK	RGMIIn_TXC	O	The transmit reference clock. The clock is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, and 125 MHz at 1000 Mbps of operation.
RGMIIn_RD[3:0]	RGMIIn_RD[3:0]	I	The receive data pins are a collection of 4 bits of data. RD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_RX_CTL is asserted
RGMIIn_RCTL	RGMIIn_RX_CTL	I	The receive data valid/control signal indicates that the RD pins are nibble data for use by the EMAC.
RGMIIn_RCLK	RGMIIn_RXC	I	The receive clock is a continuous clock that provides the timing reference for receive operations. The clock is generated by the PHY and is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, 125 MHz at 1000 Mbps of operation.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO pin.
MDIO_MDIO	MDIO0_MDIO	I/O	The MDIO0_MDIO pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output

(2) n 1 to 2

Note

The Control Module registers assign the specific function to the device pads. For more information on Control Module settings, see *Pad Configuration Registers* in *Control Module (CTRL_MMR)* and the device-specific Datasheet.

12.3.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.3.1.4 CPSW0 Functional Description

The three-port switch Ethernet subsystem module (CPSW) is compliant to the IEEE Std 802.3 Specification. CPSW top level functional block diagram is shown in *CPSW Top Level Block Diagram*.

12.3.1.4.1 Functional Block Diagram

The three-port Ethernet subsystem consists of:

- CPSW_3G
- One RGMIIn (where n = 1 to 2) interface module
- One RMIIn (where n = 1 to 2) interface module
- One Host Port 0 CPPI Packet Streaming Interface
- CPSW subsystem control registers (REG)
- One MDIO interface module
- One Interrupt Controller module

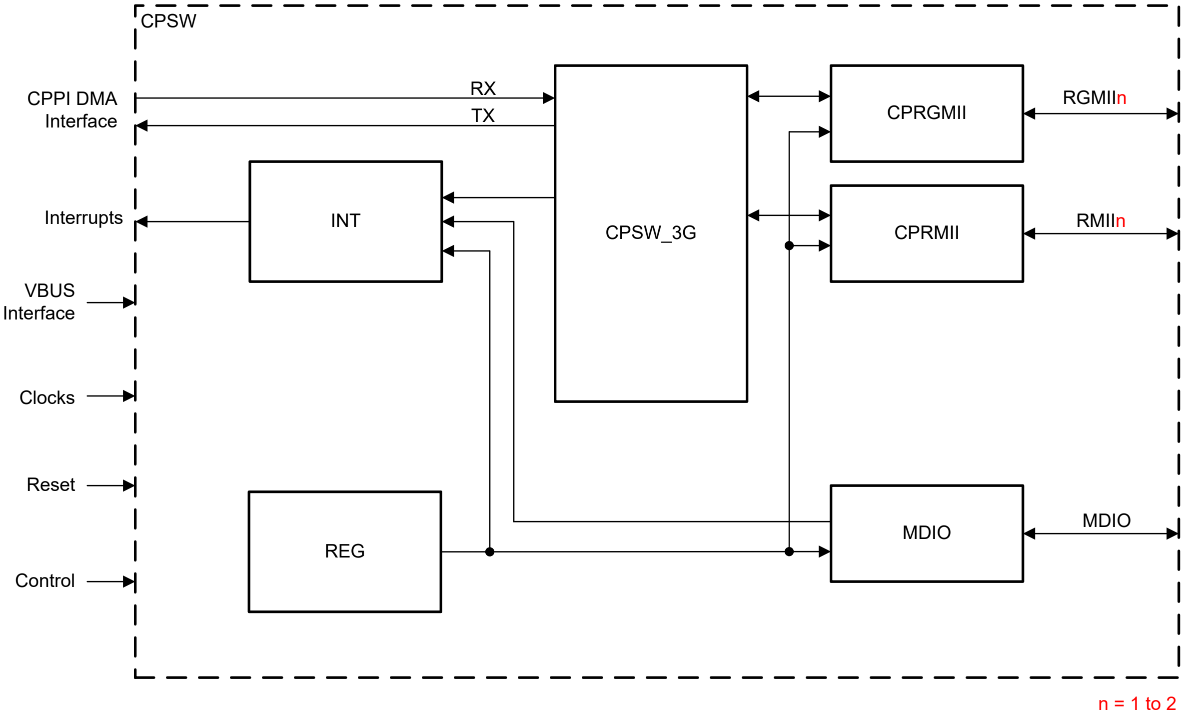

Figure 12-128. CPSW Top Level Block Diagram

12.3.1.4.2 CPSW Ports

The Ethernet Subsystem has three ports. Port 0 is the Host port (internal to the Subsystem). Port 1 and 2 are the external ports connected to RGMII and RMII interfaces as per the interface selected.

Naming conventions followed in this chapter:

- Port0 is referred to the CPPI Host Port
- Port1 and 2 are referred to the interfaces RGMII/RMII

12.3.1.4.2.1 Interface Mode Selection

The three-port switch (CPSW) Ethernet Subsystem has one 10/100/1000 Ethernet port with selectable RMII and RGMII interfaces.

The interface modes for all 2 Ethernet ports are selected by configuring the Ethernet interface mode selection bitfield (PORT_MODE_SEL) in the ENET1_CTRL and ENET2_CTRL registers.

See the device-specific Datasheet for configuring the pin mux mode as per the interface selected.

12.3.1.4.3 Clocking

12.3.1.4.3.1 Subsystem Clocking

CPSW clocking summary is shown in *CPSW Integration*.

12.3.1.4.3.2 Interface Clocking

Data is transmitted and received with respect to the reference clocks of the interface pins.

12.3.1.4.3.2.1 RGMII Interface Clocking

RGMII_RXC, RGMII_TXC frequencies are:

- 2.5 MHz at 10 Mbps
- 25 MHz at 100 Mbps
- 125 MHz at 1000 Mbps

12.3.1.4.3.2.2 RMII Interface Clocking

RMII interface clock RMII_50MHZ_CLK frequency is:

- 50 MHz at 10 Mbps
- 50 MHz at 100 Mbps

For more details on RMII clocking, please see *CPSW0 Integration*

CLKOUT_CTRL bits are used to enable and select the clock source for CLKOUT device pin.

12.3.1.4.3.2.3 MDIO Clocking

The MDIO clock is based on a divide-down of the interface (CPPI_ICLK) clock. The application software or driver must control the divide-down value.

See the CPSW3_MDIO_CONTROL_REG register for configuring the Clock Divider ([15-0]CLKDIV) value.

12.3.1.4.4 Software IDLE

The submodule software idle register bits enable CPSW operation to be completely or partially suspended by software control. There are two CPSW submodules that contain software idle register bits. Each of the two submodules may be individually commanded to enter the idle state. The idle state is entered at packet boundaries, and no further packet operations will occur on an idled submodule until the idle command is removed. The CPSW module enters the idle state when all two submodules are commanded to enter and have entered the idle state. Idle status is determined by reading or polling the two submodule idle bits. The CPSW_3G is in the idle state when all two submodules are in the idle state. The CPSW3_CPSW_NU_SOFT_IDLE_REG[0] SOFT_IDLE bit may be set if desired after the submodules are in the idle state. The SOFT_IDLE bit causes packets to not be transferred from one FIFO to another FIFO internal to the switch.

12.3.1.4.5 Interrupt Functionality

CPSW Ethernet Subsystem has six interrupt outputs:

- Cn_FH_PEND_INTR - FHost (from host to Ethernet) level interrupt
- Cn_TH_PEND_INTR - THost (from Ethernet to host) level interrupt
- Cn_TH_THRESH_PEND_INTR - THost (from Ethernet to host) non-paced level interrupt
- Cn_MISC_PEND_INTR - Miscellaneous non-paced pending interrupt
- ECC_SEC_PEND_INTR: ECC SEC pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately if desired.
- ECC_DED_PEND_INTR: ECC DED pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately.

Note

n = 0 to $num_cores-1

12.3.1.4.5.1 EVNT_PEND Interrupt

See Section 12.3.1.4.7 , *Common Platform Time Sync (CPTS)* for more details on this interrupt.

12.3.1.4.5.2 Statistics Interrupt (STAT_PEND0)

The statistics level interrupt (STAT_PEND0) will be asserted, if enabled when any statistics value is greater than or equal to 8000 0000h. The statistics interrupt is cleared by writing to decrement any statistics values greater than 8000 0000h (such that their new values are less than 8000 0000h). The statistics are mapped into internal memory space and are 32-bits wide. The raw and masked statistics interrupt status may be read by reading the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG and CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG registers, respectively.

The statistics interrupt is enabled by setting to 1h the TS_PEND_EN bit in the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.

12.3.1.4.5.3 ECC DED Level Interrupt (ECC_DED_INT)

Level interrupt (ECC_DED_INT) indicating an ECC double error has been detected.

12.3.1.4.5.4 ECC SEC Level Interrupt (ECC_SEC_INT)

Level interrupt (ECC_SEC_INT) indicating an ECC single error has been detected and corrected.

12.3.1.4.5.5 MDIO Interrupts

Normal Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 0h)

MDIO_LINKINT event is set if there is a change in the link state of the PHY corresponding to the address in the PHYADR_MON field of the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register and the corresponding LINKINT_ENABLE bit is set. The MDIO_LINKINT event is also captured in the MDIO CPSW3_MDIO_LINK_INT_MASKED_REG register. When the GO bit in the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register transitions from 1 to 0, indicating the completion of a user access, and the corresponding USERINTMASKSET bit in the CPSW3_MDIO_USER_INT_MASK_SET_REG register is set, the MDIO_USERINT signal is asserted. The MDIO_USERINT event is also captured in the CPSW3_MDIO_USER_INT_MASKED_REG register.

State Change Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 1h)

In State Change Mode, the MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO CPSW3_MDIO_ALIVE_REG or CPSW3_MDIO_LINK_REG registers changes due to MDIO operations. The MDIO_LINKINT event is also captured in the CPSW3_MDIO_LINK_INT_MASKED_REG register. MDIO_LINKINT[1] output is unused in State Change Mode. The CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k registers are unused in state change mode.

Manual Mode: (CPSW3_MDIO_POLL_REG[31] MANUALMODE = 1h)

Manual Mode allows software to directly control the MDIO serial clock output (CPSW3_MDIO_MANUAL_IF_REG[2] MDIO_MDCLK_O) and the MDIO serial data output enable (CPSW3_MDIO_MANUAL_IF_REG[1] MDIO_OE). Manual Interface Mode is enabled when the MANUALMODE bit is set in the CPSW3_MDIO_POLL_REG register. Manual Mode is intended to be used by software for slow speed general purpose IO operations and not for MDIO PHY operations.

12.3.1.4.6 CPSW_3G

The CPSW_3G RMII/ RGMII interface is compliant to the IEEE Std 802.3 Specification.

The CPSW_3G contains two Ethernet port interfaces (Ethernet port 1 and 2), one CPPI packet streaming interface host port (port 0), Common Platform Time Sync (CPTS), ALE Engine and Statistics (STATS). A top-level block diagram of the CPSW_3G is shown in Figure 12-129.

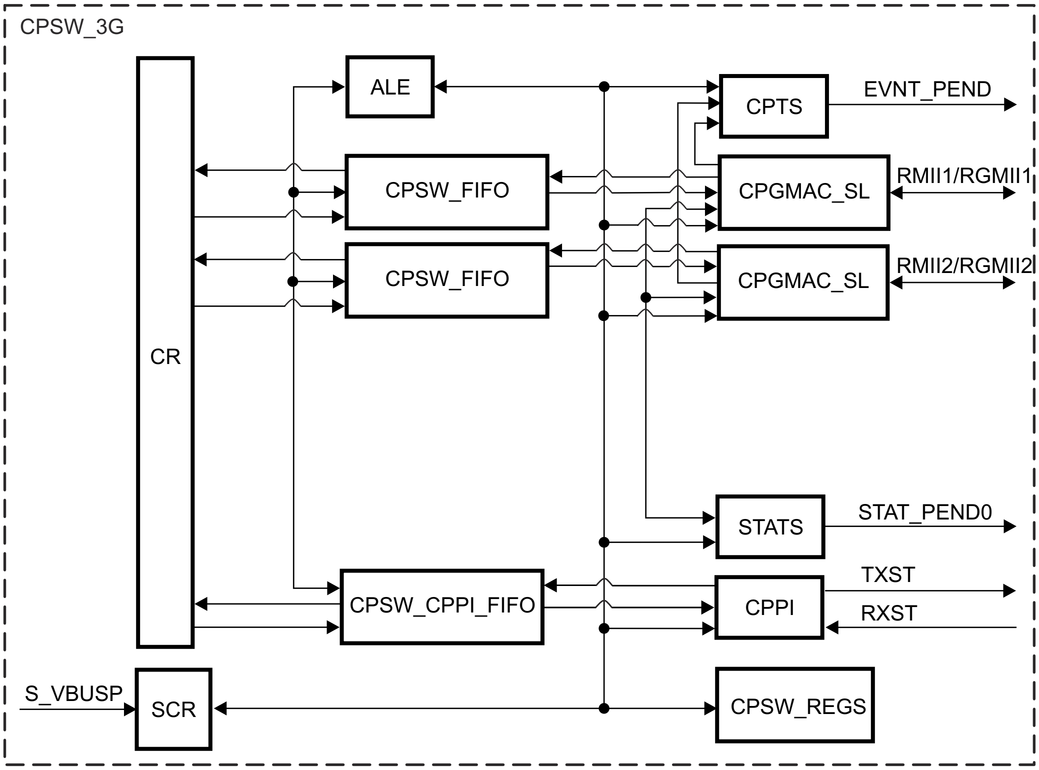

Figure 12-129. CPSW_3G Block Diagram

12.3.1.4.6.1 Address Lookup Engine (ALE)

The Address Lookup Engine (ALE) is a sub-block of the CPSW Switch and it processes all received packets and determines to which port(s) the packet should be forwarded. The ALE uses the incoming packet received port number, destination address, source address, length/type, and VLAN information to determine how the packet should be forwarded. The ALE outputs the port mask to the switch fabric that indicates the port(s) the packet should be forwarded to. The ALE is enabled when the ENABLE_ALE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register is set. All packets are dropped when the ENABLE bit is cleared to 0.

12.3.1.4.6.1.1 Error Handling

In normal operation, the Ethernet port modules are configured to issue an abort, instead of an end of packet, at the end of a packet that contains an error (runt, frag, oversize, jabber, crc, alignment, code etc.) or at the end of a MAC control packet. However, when the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG configuration bit(s) RX_CEF_EN, RX_CSF_EN, or RX_CMF_EN are set, error frames, short frames or MAC control frames have a normal end of packet instead of an abort at the end of the packet. When the ALE receives a packet that contains errors (due to a set header error bit), or a MAC control frame and does not receive an abort, the packet will be forwarded only to the host port (port 0). Packets with errors that are forwarded to the host have no VLAN untagging or drop due to rate limiting. No ALE learning occurs on packets with errors or mac control frames. Learning is based on source address and lookup is based on destination address. Directed packets from the host are not learned, updated, or touched.

12.3.1.4.6.1.2 Bypass Operations

The ALE may be configured to operate in bypass mode by setting the ENABLE_BYPASS bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register. When in bypass mode, all Ethernet port received packets are forwarded only to the host port (port 0). In bypass mode, the ALE processes host port transmit packets the same as in normal mode. In general, packets would be directed by the host in bypass mode.

12.3.1.4.6.1.3 OUI Deny or Accept

The ALE may be configured to operate in OUI deny mode by setting the ENABLE_OUI_DENY bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register. When in OUI deny mode, a packet with a non-matching OUI source address will be dropped unless the destination address matches a multicast table entry with the SUPER bit set. When ENABLE_OUI_DENY bit is cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory address table entry. Broadcast packets will be dropped unless the broadcast address is entered into the table with the SUPER bit set. Unicast packets will be dropped unless the unicast address is in the table with BLOCK and SECURE both set (supervisory unicast packet).

12.3.1.4.6.1.4 Statistics Counting

ALE sends many statistics along with the frame routing so the CPSW can count them on a per port basis. There are many reasons to drop frames the below drop events are individually counted in CPSW per port statistics counters.

Table 12-143. Learned Address Control Bits

Abbreviation	Description
vddc	Dual VLAN or Double VLAN drop counter.
frdc	IPv4 fragmented drop counter.
nldc	IPv4 Protocol or IPv6 Next Header drops due to next header limit drop counter.
etdc	Ether Type field is <= 1500 and the frame size is too small drop counter.
smdc	The Source Address has bit 40 set drop counter.
badc	The Source or Destination Address blocked drop counter.
svdc	The Source Address is locked to a different port drop counter.
des	The Source and Destination are equal and the Source Address is not in the table drop counter.
adc	The Source Address is not in the table in authentication mode drop counter.
vicdc	The VLAN ingress check failed drop counter.
rldc	Rate Limit Drop Counter.
over	Lookup Overflow, the rate of the ALE clock is not sufficient to handle the incoming frame rate (Should never happen).
drop	Packet is dropped and not forwarded.

12.3.1.4.6.1.5 Automotive Security Features

The ALE has many automotive security features that most enterprise switches do not require.

- VLANs can be configured to not allow fragmented IPv4 frames. That is a VLAN can be configured to not allow fragmented IPv4 traffic.
- VLANs can be configured to only allow up to four different IPv4 Protocols or IPv6. Next Header values, for example a VLAN can be configured to only allow TCP traffic in both IPv4 and IPv6 packets.
- Drop invalid Source Addresses, that is drop Source Addresses with bit 40 set (Multicast/Broadcast indicator on Destination Addresses)
- IEEE802.3 Length Check, drop frames that the IEEE802.3 Length is not contained within the frame. (Ether Types 0-1500)
- Any Source Address can be secured to a port dropping any attempts from other ports to masquerade as a service.

- Any source or destination address can be blocked.
- Per Port or Per VLAN ingress checking, dropping traffic from non-member ports.
- Classification, Policing on L2 and L3 information.

12.3.1.4.6.1.6 CPSW Switching Solutions

The host port can operate in many different modes as well depending on the functionality of the host. It is important to understand the modes and configure them properly.

The ALE Table is designed to maximize the modes without compromise of the system functionality as well.

12.3.1.4.6.1.6.1 Basics of 3-port Switch Type

The 3-port switch has a host port, and that port can operate in two fundamental modes. Bridge mode allows the host to extent the switched domain to another network like Wi-Fi or another multi-port switch. In this case the host must be able to see unknown unicast addresses so they can be broadcast to the other network. In Port mode the host need not see any unknown unicast traffic. The CPSW3_CPSW_NU_ALE_ALE_CONTROL[8] EN_HOST_UNI_FLOOD bit determines the host mode for unknown unicast traffic. This bit should only be set if the user is bridging two or more networks together.

The 3-port switch can operate like a two-port switch using the ALE table just for the host info, the only adder is now other VLANs need to be supported for transit traffic between the external ports. This can easily be done using the default VLAN rules so no ALE table entries are used.

The 3-port switch can also operate in a fully authenticated environment where all network nodes are registered via the 802.1x based protocols. In this case the ALE table is filled with network node addresses that have been authenticated

12.3.1.4.6.1.7 VLAN Routing and OAM Operations

12.3.1.4.6.1.7.1 InterVLAN Routing

The CPSW module supports wire rate InterVLAN routing for a small number of routes, that is the host will setup an ALE classifier with and associated egress operation that will cause the CPSW to perform particular egress operations. The ALE can optionally check time to live validity as well.

The ALE uses the classifier along with an egress opcode, destination port mask and TTL check field to tell the CPSW to manipulate the packet on the egress. The CPSW will use the opcode along with a per port operation table to process the packet. By setting up the CPSW egress operation table you can replace the DA, SA and VLAN along with optionally updating the time to live IP header field. This allows the CPSW to perform the routing function for a small set of routes without getting the local host/CPU involved.

The Egress opcode will only be use for a classifier match and the packet would normally be sent only to the host. That is the host would have routed the packet but the CPSW has been configured to do the work instead. In the event that the time-to-live check feature is enabled and the time-to-live is either 0 or 1, the packet will not get the egress opcode and instead be sent to the host as if the route is not setup. This allows the host to deal with invalid TTL fields.

12.3.1.4.6.1.7.2 OAM Operations

The ALE supports OAM loopback on ports so that a remote link can be tested. That is a port placed in OAM loopback will echo packets received on a port back to the port with an egress op of 0xFF which will swap the SA and DA on egress in the CPSW.

Any supervisory packet will not be affected, so the spanning tree and other bridging functions are not affected.

Packets will only be echoed if the port is in OAM loopback mode, the received packet in not a supervisor packet. The port is in a forwarding state and the packet received DA!=SA and there are no errors in the packet.

When a port is in OAM loopback the port will not egress traffic from other ports, no address for loop backed traffic will be learned if enabled. Any packet received on the OAM loopback port with an error will be process as if the port is not in OAM. That is if the host has enabled copy errored frames the errored frames will be sent to the host instead.

12.3.1.4.6.1.8 Supervisory packets

Multicast supervisory packets are designated by the SUPER bit in the table entry. Unicast supervisory packets are indicated when BLOCK and SECURE are both set. Supervisory packets are not dropped due to rate limiting, OUI, or VLAN processing. The purpose of supervisory packets is to allow packets that would be otherwise blocked to be forwaded for special purposes.

12.3.1.4.6.1.9 Address Table Entry

The ALE table contains multiple table entry types. Each table entry represents a free entry, an address, a VLAN, an address/VLAN pair, or an OUI address. Software should ensure that there are not double address entries in the table. The double entry used would be indeterminate. Reserved table bits must be written with zeroes.

Source Address learning occurs for packets with a unicast, multicast or broadcast destination address and a unicast or multicast (including broadcast) source address. Multicast source addresses have the group bit (bit 40) cleared before ALE processing begins, changing the multicast source address to a unicast source address. A multicast address of all ones is the broadcast address which may be added to the table. A learned unicast source address is added to the table with the following control bits:

Table 12-144. Learned Address Control Bits

Bit(s)	Value
Ageable	1
Touch	1
BLOCK	0
SECURE	0

If a received packet has a source address that is equal to the destination address then the following occurs:

- The address is learned if the address is not found in the table.
- The address is updated if the address is found.
- The packet is dropped.

Table Entry Type

00 - Free Entry

01 - Address Entry : unicast or multicast determined by destination **address bit 40.**

10 - VLAN entry

11 - VLAN Address Entry : unicast or multicast determined by **address bit 40.**

12.3.1.4.6.1.9.1 Multicast Address Table Entry

Table 12-145. Multicast Address Table Entry Bit Values

70:68	67:66	65	64	63:62	61:60	59:48	47:0
Reserved	PORT_MASK	SUPER	Reserved	MCAST_FWD_STATE	ENTRY_TYPE (01)	Reserved	MULTICAST_ADDRESS

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Port Mask(1:0) (PORT_MASK)

This 2-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Multicast Forward State (MCAST_FWD_STATE)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state in order to forward the packet. If the transmit PORT_MASK has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

00 - Forwarding

01 - Blocking/Forwarding/Learning

10 - Forwarding/Learning

11 - Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.2 OUI Unicast Address Table Entry

Table 12-146. OUI Unicast Address Table Entry Bit Values

70:64	63:62	61:60	59:48	47:24	23:0
Reserved	UNICAST_TYPE (10)	ENTRY_TYPE (01)	Reserved	UNICAST_OUI	Reserved

Unicast Type (UNICAST_TYPE)

This field indicates the type of unicast address the table entry contains.

00 - Unicast address that is not ageable.

01 - Ageable unicast address that has not been touched.

10 - OUI address - lower 24-bits are don't cares (not ageable).

11 - Ageable unicast address that has been touched.

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_OUI)

For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup.

12.3.1.4.6.1.9.3 Unicast Address Table Entry (Bit 40 == 0)

Table 12-147. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	RESERVED	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk numbe

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/ Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE it a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.3.1.4.6.1.9.4 Multicast Address Table Entry (Bit 40==1)

Table 12-148. Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0

Table 12-148. Multicast Address Table Entry Bit Values (continued)

RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (1h)	RESERVED	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.5 VLAN/Unicast Address Table Entry (Bit 40 == 0)

Table 12-149. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	VLAN_ID	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk number

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE is a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

3h: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.3.1.4.6.1.9.6 VLAN/Multicast Address Table Entry (Bit 40==1)

Table 12-150. VLAN/Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0
RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (11)	VLAN_ID	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

11: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.7 Inner VLAN Table Entry

Table 12-151. Inner VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	0h	ENTRY_TYPE (1h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

This field indicates which port(s) are the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW3_CPSW_NU_ALE_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.3.1.4.6.1.9.8 Outer VLAN Table Entry

Table 12-152. Outer VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	2h	ENTRY_TYPE (2h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

Index into CPSW_ALE_MSK_MUX0 to CPSW_Ix_ALE_MSK_MUXx register array that is used to create the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW3_CPSW_NU_ALE_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.3.1.4.6.1.9.9 EtherType Table Entry

Table 12-153. EtherType Table Entry

70:65	64:62	61:60	59:16	15:0
RESERVED	4h	ENTRY_TYPE (2h)	RESERVED	ETHERTYPE

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

Ether Type (ETHERTYPE)

16-bits Ether Type field.

12.3.1.4.6.1.9.10 IPv4 Table Entry

Table 12-154. IPv4 Table Entry

70	69:65	64:62	61:60	59:32	31:0
RESERVED	IGNMBITS	6h	ENTRY_TYPE (2h)	RESERVED	IPV4ADR

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv4 Address (IPV4ADR)

32-bit IPv4 Address. Any ignored bits must be zero value in the table entry.

12.3.1.4.6.1.9.11 IPv6 Table Entry High

Table 12-155. IPv6 Table Entry High

70:64	63	62	61:60	59:0
IGNMBITS	RESERVED	(1h)	ENTRY_TYPE (2h)	IPV6ADR[127:68]

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 64 bits (IPV6ADR[127:68])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

12.3.1.4.6.1.9.12 IPv6 Table Entry Low

Table 12-156. IPv6 Table Entry Low

70:63	62	61:60	59:0
IPV6ADR[67:60]	1h	ENTRY_TYPE (2h)	IPV6ADR[59:0]

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 8 bits (IPV6ADR[67:60])

IPv6 Address - upper 60 bits (IPV6ADR[59:0])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

Note: IPV6 table address entries operate differently than all other table entry types. IPV6 table entries have a high entry concatenated with a low entry. The high entry must have an entry_pointer value of the low entry_pointer plus 0x40. Bit six of the entry_pointer must be set for the high entry and must be zero for the low entry.

12.3.1.4.6.1.10 Multicast Address

Multicast addresses are addresses with bit 40 set. Only destination addresses can be Multicast addresses. The group bit (bit 40) of the source address is reserved in the IEEE tandard.

A multicast address of all ones is the broadcast address which can be added to the lookup table if forwading of broadcast packets need be modified.

12.3.1.4.6.1.10.1 Multicast Ranges

Added IgnMbits to indicate at least one bit of the multicast address is ignored. Up to 10 bits of the multicast address can be ignored to provide the ability to create multiple multicast address ranges.

if ((IgnMbits)&(MultiCastAddress[0] ==0x000)) { MultiCastAddress[0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[1:0]==0x001)) { MultiCastAddress[1:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[2:0]==0x003)) { MultiCastAddress[2:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[3:0]==0x007)) { MultiCastAddress[3:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[4:0]==0x00F)) { MultiCastAddress[4:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[5:0]==0x01F)) { MultiCastAddress[5:0] is ignored in compare} if ((IgnMbits)&(MultiCastAddress[6:0]==0x03F)) { MultiCastAddress[6:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[7:0]==0x07F)) { MultiCastAddress[7:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[8:0]==0x0FF)) { MultiCastAddress[8:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[9:0]==0x1FF)) { MultiCastAddress[9:0] is ignored in compare}

Below is 'C' code to modify ALE MultiCastAddress and IgnMbits when iNumOfBitsToIgnore is greater than zero. Where fGenMask(iOffset,iBitsToMask) creates a Mask for the value provided. For example fGenMast(0,5) will return 0x1F.

```
if(iNumOfBitsToIgnore)
{
int iIgnClrMsk,iIgnSetMsk;
iIgnClrMsk=fGenMask(0, iNumOfBitsToIgnore);
iIgnSetMsk=fGenMask(0, iNumOfBitsToIgnore -1);
MultiCastAddress &= ~iIgnClrMsk;
MultiCastAddress |= iIgnSetMsk;
IgnMbits = 1;
}
else
{
IgnMbits = 0;
}
```

Multicast Addresses or Ranges can overlap, in the event of an overlap; the higher ALE index will be used.

12.3.1.4.6.1.11 Aging and Auto Aging

The ALE supports software control or automatic aging of agable addresses.

Any time an agable address is seen as a source address entering from a port the source address entry will be marked as touched.

If the aging timer expires or the software sets the [29] AGE_OUT_NOW bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL, the aging process will be started.

The aging process will read each ALE entry and for all entries that are an address with or without VLAN that is also agable, the touch check process will be done.

The touch check process will test the TOUCH bit and if clear, the entry will be marked as free, else the TOUCH bit will be cleared.

What this means is that if the aging interval was programmed as one second, any unused entry could stay in the ALE table for 1.000001 to 1.999999 seconds

12.3.1.4.6.1.12 ALE Policing and Classification

The ALE has a number of configurable classifier engines (policers) that can be used for classification. Classification is a subset of the policing function and uses a policer without the color marking or rate limiting functions. A policer is a hardware engine that is used for policing. The POLCNTDIV8 field in the CPSW3_CPSW_NU_ALE_ALE_STATUS register indicates the number of policers available to be used for classification. Each policer can be enabled to match on one or more of any of the below packet fields for classification. All but Port and Priority are index references to the ALE table entries.

- Port Number
- Priority extracted from VLAN, mapped from DSCP if enabled, or Default Port Priority
- Organization Network Unique identifier - ONU
- Destination Address - DA
- Source Address - SA
- Outer VLANID -S-VLANID
- Inner VLANID -C-VLANID
- Ether Type
- IP Source Address - IPSA with full CIDR masking for IPv4 and IPv6
- IP Destination Address - IPSA with full CIDR masking for IPv4 and IPv6
- Support Host Thread/Flow ID mapping based on any packet classification above

12.3.1.4.6.1.12.1 ALE Policing

The policing function on each policer engine is implemented as dual-counter three-color marking engine as described in the IETF RFC2698. The first counter is the Committed Information Rate (CIR) counter and the second counter is the Peak Information Rate (PIR) counter. The policing function can use either or both counters. Based on the counter values the packet color is determined. The color is used to determine whether the packet is dropped or forwarded. The ALE has a local feature that can drop packets regardless of queue state.

The policing rates are determined by the below equations:

CIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW3_CPSW_NU_ALE_POLICECFG7[31-0] CIR_IDLE_INC_VAL) / 32768

PIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW3_CPSW_NU_ALE_POLICECFG6[31-0] PIR_IDLE_INC_VAL) / 32768

Each policer has 10 different match operations (see Section 12.3.1.4.6.1.12). Since multiple policing entries can be hit on a single packet this provides the ability to create precise traffic stream control.

Packets are colored at ALE lookup time. Packets can be colored RED, YELLOW, or GREEN. If multiple policers are configured for a packet stream then the packet color is merged from all matching (hit) policers. If any policer is RED then the packet is marked RED. Else if any policer is YELLOW then the packet is marked YELLOW. Otherwise the packet is marked GREEN.

The Policing engine supports several modes such that packets that don't hit a policing/classifier match can be treated as RED, YELLOW, GREEN or policer 0 color. Using policer 0 allows for a system to regulate unregulated traffic.

12.3.1.4.6.1.12.2 Classifier to Host Thread Mapping

The ALE module allows Host Thread mapping based on any packet classification. That is the ALE can generate a thread ID used by the host based on ALE classifier matches.

When enabled the highest classifier match can map to a particular thread ID value.

The ALE also supports an optional default Thread ID value in the event that no classifier match.

Each Thread ID, including the default thread ID, has an enable functionality such that, if no classifier matches occur the default value is used, if the default is not enabled, the switch will use the {port,priority} value instead. If multiple classifier matches occur, the highest matching entry with a thread enable bit set will be used.

Three registers are used for ALE classification thread mapping configuration (CPSW3_CPSW_NU_ALE_THREADMAPDEF, CPSW3_CPSW_NU_ALE_THREADMAPCTL and CPSW3_CPSW_NU_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW3_CPSW_NU_ALE_THREADMAPCTL register allows the CPSW3_CPSW_NU_ALE_THREADMAPVAL register contents to be written to the selected classifier. There is a CPSW3_CPSW_NU_ALE_THREADMAPDEF register that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.3.1.4.6.1.12.3 ALE Classification

When the policers are configured as classifiers, the color marking and policing functions of the policing/classifier engines are not used. One or multiple classifiers can be configured to match on a single packet. For example, a classifier can be enabled to match on priority while another classifier could match IP address.

12.3.1.4.6.1.12.3.1 Classifier to CPPI Transmit Flow ID Mapping

The ALE can generate a 6-bit transmit CPPI Flow ID based on classifier matches that can be used instead of the switch default transmit Flow ID mapping. The switch default flow ID is the remapped received packet priority (0 to 7). Thread and flow ID are used interchangeably for this since there is a single hardware thread (TXST_THREAD_MREADY) but there are 6-bits of FLOW_ID in the transmit CPPI INFO word 0. When enabled, the highest classifier match can map to a particular 6-bit flow ID value that is associated with the classifier. The ALE also supports an optional ALE default thread/flow ID value in the event that no classifiers match. Each thread/flow ID, including the ALE default thread/flow ID, has an enable such that the ALE default thread/Flow ID is used if enabled and if no matches occur (instead of the remapped received packet priority). If the ALE default is not enabled and no matches occur then the switch default value will be used. If multiple classifier matches occur, the highest match with a thread enable bit set will be used. The resultant flow ID has the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG register value added to it to determine the actual value in the INFO 0 Flow ID field.

Three registers are used for ALE classification thread/flow ID mapping configuration (CPSW3_CPSW_NU_ALE_THREADMAPDEF, CPSW3_CPSW_NU_ALE_THREADMAPCTL and CPSW3_CPSW_NU_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW3_CPSW_NU_ALE_THREADMAPCTL register allows the CPSW3_CPSW_NU_ALE_THREADMAPVAL register contents to be written to the selected classifier. There is a single CPSW3_CPSW_NU_ALE_THREADMAPDEF that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.3.1.4.6.1.13 Mirroring

The ALE supports three mirroring modes: destination port, source port and or table entry.

Destination port mirroring allows packets from any ingress port or trunk which ends up switching to a particular egress destination port or trunk to be mirrored to yet another egress destination port or trunk. For example any traffic from any port that is switched to port 'A' can be also mirrored to port 'B'. (MIRROR_DP=A, MIRROR_DEN=1h, MIRROR_TOP=B in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register).

Source port mirroring allows packets received on any enabled ingress source port or trunk to be switched to the mirror egress port as well as the actual egress destination ports. For example traffic received on ingress port 'A' can be switched to egress port 'B' as well as the intended egress destination port.(Iy_REG_Py_MIRROR_SP=1h in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register, MIRROR_SEN=1h, MIRROR_TOP=B in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register).

Table entry mirroring allows for any MAC Address, MAC Address with VLAN, ONU Address or VLAN entry that matches on ingress to be switched to the egress destination as well as the actual egress destination. For example all traffic for VLAN ID of 35 can be mirrored to port 'B'. That is any traffic switched on VLAN ID of 35 will be mirrored. ({VLAN ID of 35 in ALE Table entry index=C}, MIRROR_MIDX=C, MIRROR_MEN=1h, MIRROR_TOP=B)

In the event that mirrored packets are mirrored to or from a port that is also the mirror port the packet will not be duplicated or marked as a mirror packet since the packet has already been on the port as ingress or egress. The packet sent to the mirror port may have modified VLAN info based on the port and VLAN lookup table entries. The mirror port need not be a member of the VLAN ID it is mirroring, the ALE will forward traffic to the mirror port after ingress and egress filters are applied.

The switch may decide to drop any mirror traffic based on switch buffer thresholds as to prevent required traffic from becoming congested.

Port mirroring is controlled by register fields in CPSW3_CPSW_NU_ALE_ALE_CONTROL, CPSW3_CPSW_NU_ALE_ALE_CTRL2 and the port control registers.

- MIRROR_DP - The destination port that will have its traffic mirrored (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_TOP - The port to which mirrored traffic is sent (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_MEN - The enable for mirroring traffic that matches a supported lookup table entry (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_DEN - The Enable for destination port mirroring (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_SEN - The Enable for source port mirroring (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_MIDX - The index of a lookup table entry that will be mirrored CPSW3_CPSW_NU_ALE_ALE_CTRL2 register).
- Iy_REG_Py_MIRROR_SP - The enable for the Source port to be mirrored. Although multiple source ports can be mirrored concurrently, a mirror traffic bandwidth issue may occur on the mirror egress port (CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register).

12.3.1.4.6.1.14 Trunking

The ALE supports port trunking of any port in any of four trunk groups. That is, four trunk groups can be supported with up to eight ports in each trunk group. There are no port adjacency rules for trunk groups. When ports are a member of a trunk group, addresses added and used in the lookup table will refer to the trunk group rather than port as indicated in the lookup table entries. If ports are removed from a trunk group, the ALE will redistribute the traffic based on the crc polynomial of enabled fields and the remaining ports within the trunk group. A trunk group may contain only one port. Packet priority, DA, SA, C-VLAN ID, IPv4SA, IPv4DA, IPv6SA, and/or IPv6DA can be used in the hash to generate destination port within the trunk group. If all hash enables are disabled, the packet can be directed to a particular port within the trunk group which allows for testing paths etc. A host directed frame is directed to the directed port regardless of trunk group settings.

Trunking is controlled through fields in the CPSW3_CPSW_NU_ALE_ALE_CTRL2 register and in each ALE CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register:

- TRK_EN_DST - Enable destination address hashing for trunk port calculation.
- TRK_EN_SRC - Enable source address hashing for trunk port calculation.
- TRK_EN_PRI - Enable priority hashing for trunk port calculation.
- TRK_EN_IVLAN - Enable inner C-VLAN ID hashing for trunk port calculation.
- TRK_EN_SIP - Enable source IP address hashing for trunk port calculation.
- TRK_EN_DIP - Enable destination IP address hashing for trunk port calculation.
- TRK_BASE - Hashing formula starting value and test port offset.
- Iy_REG_Py_TRUNKEN - Enable this port as a trunk group
- Iy_REG_Py_TRUNKNUM - Trunk group number defines this port as a member of a particular trunk group.

12.3.1.4.6.1.15 DSCP

The ALE can map DSCP field to priority prior to classification matching. When enabled the DSCP is mapped via 64 priority entries such that any DSCP value can be mapped to any of the eight priorities. When a packet is received without a VLAN priority this remapped priority can be used instead of the default Port VLAN priority field. See CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_y and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_DSCP_MAP_REG registers in the Register Manual section for DSCP mapping.

12.3.1.4.6.1.16 Packet Forwarding Processes

There are four processes that an incoming received packet may go through to determine packet forwarding. The processes are *Ingress Filtering*, *VLAN_Aware Lookup*, and *Egress.*

Packet processing begins in the Ingress Filtering process. Each port has an associated packet forwarding state that can be one of four values (Disabled, Blocked, Learning, or Forwarding). The default state for all ports is Disabled. The host sets the packet forwarding state for each port.

In the packet ingress process (receive packet process), there is a forward state test for unicast destination addresses and a forward state test for multicast addresses. The multicast forward state test indicates the port states required for the receiving port in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state for the packet to be forwarded for transmission. The MCAST_FWD_STATE indicates the required port state for the receiving port as indicated in the preceding table. The unicast forward state test indicates the port state required for the receiving port in order to forward the unicast packet. The transmit port must be in the Forwarding state in order to forward the packet. The BLOCK and SECURE bits determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state. The transmit port must be in the Forwarding state regardless. The forward state test used in the ingress process is determined by the destination address packet type (multicast/unicast).

In general, packets received with errors are dropped by the address lookup engine without learning, updating, or touching the address. The error condition and the abort are indicated by the Ethernet port to the ALE. Packets with errors may be passed to the host (not aborted) by a Ethernet port port, if the port has the RX_CMF_EN, RX_CEF_EN, or RX_CSF_EN bit(s) set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG registers. Error packets that are passed to the host by the Ethernet port are considered to be bypass packets by the ALE and are sent only to the host. Error packets do not learn, update, or touch addresses regardless of whether they are aborted or sent to the host. Packets with long or short errors received by the host are dropped. Packets with errors received by the host are forwarded as normal.

The following control bits are in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG registers:

- [22] RX_CEF_EN - enables frames that are fragments, long, jabber, CRC, code, and alignment errors to be forwarded
- [23] RX_CSF_EN - enables short frames to be forwarded
- [24] RX_CMF_EN - enables MAC control frames to be forwarded.

12.3.1.4.6.1.16.1 Ingress Filtering Process

Condition and action
If ((ALE BYPASS) and (host port is not the receive port)) then use host portmask and go to Egress process
if (directed packet) then use directed port number and go to Egress process
If (Rx ly_REG_Py_PORTSTATE is Disabled) then discard the packet
if ((ALE BYPASS or error packet) and (host port is not the receive port)) then use host portmask and go to Egress process
if (((BLOCK) and (unicast source address found)) or ((BLOCK) and (unicast destination address found))) then discard the packet

if ((ENABLE_RATE_LIMIT) and (rate limit exceeded) and (not BCAST_MCAST_CTL) then if (((Multicast/Broadcast destination address found) and (not SUPER)) or (Multicast/Broadcast destination address not found)) then discard the packet
if ((not forward state test valid) and (destination address found)) then discard the packet to any port not meeting the requirements • Unicast destination addresses use the unicast forward state test and multicast destination addresses use the multicast forward state test.
if ((destination address not found) and ((not transmit port forwarding) or (not receive port forwarding))) then discard the packet to any ports not meeting the above requirements
if (source address found) and (secure) and (not block) and (receive port number != port_number)) then discard the packet
if ((not super) and (drop_untagged) and ((non-tagged packet) or ((priority tagged) and not(en_vid0_mode)) then discard the packet

If (VLAN_Unaware)
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = “000000”
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = “111111”
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = “111111”
UVLAN_MEMBER_LIST = “111111”
else if (VLAN not found)
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER = CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER
else
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
UVLAN_MEMBER_LIST = found UVLAN_MEMBER_LIST

if ((not SUPER) and (Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member)) then discard the packet
if ((ENABLE_AUTH_MODE) and (source address not found) and not(destination address found and (SUPER))) then discard the packet
if (destination address equals source address) then discard the packet
if (VLAN_AWARE) goto VLAN_Aware_Lookup process else goto VLAN_Unaware_Lookup process

12.3.1.4.6.1.16.2 VLAN_Aware Lookup Process

Condition and action
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER) then portmask is the logical "AND" of the PORT_NUMBER and UVLAN_MEMBER_LIST less the host port and goto Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical “AND” of the PORT_NUMBER and the UVLAN_MEMBER_LIST and goto Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_NUMBER and goto Egress process
if (Unicast packet) # destination address not found then portmask is VLAN member LIST less host port and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical “AND” of CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST and found destination address/VLAN portmask (PORT_MASK) and UVLAN_MEMBER_LIST and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_MASK and goto Egress process
if (Multicast packet) # destination address not found then portmask is the logical “AND” of CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST and UVLAN_MEMBER_LIST then goto Egress process
if (Broadcast packet) then use found UVLAN_MEMBER_LIST and goto Egress process

Note

The UVLAN_MEMBER_LIST, UVLAN_UNREG_MCAST_FLOOD_MASK, UVLAN_REG_MCAST_FLOOD_MASK and UVLAN_FORCE_UNTAGGED_EGRESS are set in the Section 12.3.1.4.6.1.16.1 *Ingress Filtering Process*, based on VLAN_Unaware, Unknown_VLAN rules and VLAN table entries.

12.3.1.4.6.1.16.3 Egress Process

Condition and action
Clear Rx port from portmask (don’t send packet to Rx port).
Clear disabled ports from portmask.
if ((ENABLE_OUI_DENY) and (OUI source address not found) and (not ALE BYPASS) and (not error packet) and ((not mcast destination address) and (SUPER))) then Clear host port from portmask

if ((not ENABLE_OUI_DENY) and (OUI source address found) and (not ALE BYPASS) and (not error packet) and not ((mcast destination address) and (SUPER))) then Clear host port from portmask
if ((ENABLE_RATE_LIMIT) and (BCAST_MCAST_CTL)) then if (not SUPER) and (rate limit exceeded on any tx port) then clear rate limited tx port from portmask If address not found then SUPER cannot be set.
If portmask is zero then discard packet
Send packet to portmask ports.

12.3.1.4.6.1.16.4 Learning/Updating/Touching Processes

The learning, updating, and touching processes are applied to each receive packet that is not aborted. The processes are concurrent with the packet forwarding process. In addition to the following, a packet must be received without error in order to learn/update/touch an address.

12.3.1.4.6.1.16.4.1 Learning Process

The learning process is applied to each receive packet that is not aborted. The learning process is a concurrent process with the packet forwarding process.

Condition and action
If (directed) then do not learn, update, or set touched else continue
If (not (Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (Iy_REG_Py_NO_LEARN)) then do not learn address
if ((Non-tagged packet) and (Iy_REG_Py_DROP_UN_TAGGED)) then do not learn address
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”)) then do not learn address
if ((Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found)) then do not learn address
if ((source address found) and (receive port_number != PORT_NUMBER) and (SECURE or BLOCK)) then do not update address else continue
if ((source address found) and (receive port number != PORT_NUMBER)) then update address else continue
if ((source address not found) and (VLAN_AWARE) and not (LEARN_NO_VLANID)) then learn address with VLAN
if ((source address not found) and ((not VLAN_AWARE) or (VLAN_AWARE and LEARN_NO_VLANID))) then learn address without VLAN

12.3.1.4.6.1.16.4.2 Updating Process

Condition and action

if (dlr_unicast) then do not update address
If (not(Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (ly_REG_Py_NO_SA_UPDATE)) then do not update address
if ((Non-tagged packet) and (ly_REG_Py_DROP_UN_TAGGED)) then do not update address
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”)) then do not update address
if ((ly_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found)) then do not update address
if ((source address found) and (receive port number != PORT_NUMBER) and (SECURE or BLOCK)) then do not update address
if ((source address found) and (receive port number != PORT_NUMBER)) then update address

12.3.1.4.6.1.16.4.3 Touching Process

if ((source address found) and (ageable) and (not touched)) then set touched

12.3.1.4.6.1.17 VLAN Aware Mode

The CPSW is in VLAN aware mode when the VLAN_AWARE bit is set in the CPSW3_CONTROL_REG register.

In VLAN aware mode, transmitted packet data is changed depending on the packet type (PKT_TYPE), packet priority (PKT_PRI), and VLAN information.

The VLAN_LTYPE_SEL value is selected by the S_CN_SWITCH bit in the CPSW3_CONTROL_REG register and is either the VLAN_LTYPE_INNER (8100h default) or VLAN_LTYPE_OUTER (88A8h default) value.

12.3.1.4.6.1.18 VLAN Unaware Mode

An egress port is operating in the VLAN unaware mode when the VLAN_AWARE bit in the CPSW3_CONTROL_REG register is cleared to 0h. In VLAN unaware mode, transmit (egress) packets are not modified on egress.

12.3.1.4.6.2 Packet Priority Handling

Packets are received on three ports, two Ethernet port and one CPPI host port. Received packets have a received packet priority (0 to 7, with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port’s DSCP priority mapping registers (IPv4 packet).

3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority.

The received packet priority is mapped through the receive ports associated packet-priority-to-header-packet-priority-mapping register (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG) to obtain the header packet priority. The header packet priority is the hardware switch priority. The header packet priority is also used as the actual transmit packet priority if the VLAN information is to be sent on egress.

The header packet priority is mapped at each destination FIFO through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG register (header priority to switch priority mapping register) to obtain the hardware switch priority (hardware queue 0 through 7).

12.3.1.4.6.2.1 Priority Mapping and Transmit VLAN Priority

There are three priorities that are used inside the Gigabit Ethernet Switch: **packet priority**, **header packet priority**, and **switch priority**. The **header packet priority** is used as the outgoing VLAN priority if the packet is egressing from the switch with a VLAN tag. The **switch priority** determines which of the 8 FIFO priority queues the packet uses during egress.

Figure 12-130 below, as well as the corresponding explanation that follows, explains each of the priorities, how they are determined, and how they are used. A number in parentheses in the figure indicates a process (Ethernet port ingress, host port egress, etc.). Each bullet in the text following the diagram explains one of the 5 processes pointed out in the figure.

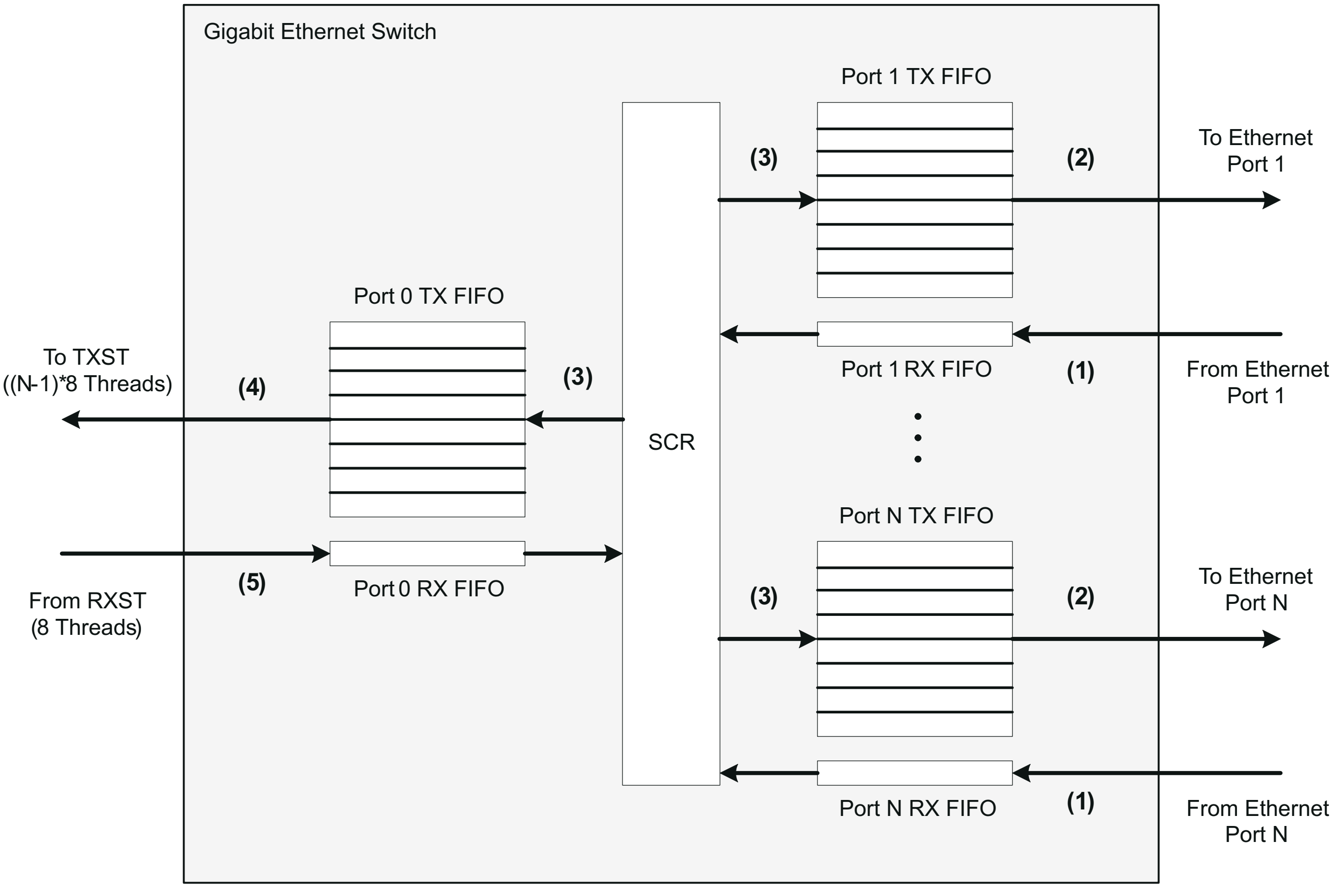

Figure 12-130. Gigabit Ethernet Switch Priority Mapping and Transmit VLAN Processing

From Figure 12-130 above:

- (1) is the ingress process that occurs at the external Ethernet ports
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the ingress port's priority. This **packet priority** is then mapped to a **header packet priority** using the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register where N is the port where the packet entered the switch. This process is explained in further detail in Section 12.3.1.4.6.2 .
- (2) is the egress process that occurs at the external Ethernet ports
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1) or (5). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.3.1.4.6.4.1 .
- (3) is the process by which it is decided which priority TX queue to place the packet on in the Port N TX FIFO during egress
  - Each Port's TX FIFO has 8 queues that each correspond to a priority that is used when determining which packet will egress from the switch next at that port. The **header packet priority** (Ethernet port ingress, process (1)) or the receive packet thread (host port 0 ingress, process (5)) gets mapped through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the egress port number) to determine the **switch priority** of the packet. The **switch priority** determines which TX FIFO queue to place the packet in. The FIFO architecture is described in Section 12.3.1.4.6.10.5 . The header packet priority to switch priority mapping is discussed in Section 12.3.1.4.6.2 .
- (4) is the egress process that occurs at Host Port 0 toward the transmit streaming interface (TXST)
  - The TXST has 8 egress threads for each external Ethernet port (32 threads in a 5-port switch and 64 threads in a 9-port switch). The TX thread that is selected for a packet is determined by the Ethernet port of ingress and the **switch priority** of the packet that was determined in process (3).
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.3.1.4.6.4.1 .
- (5) is the ingress process that occurs at Host Port 0
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the host port's priority. This packet priority is then mapped to a **header packet priority** using the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register.
  - Host port 0 also has a received packet thread. The receive packet thread is based on either the packet's VLAN priority, IPv4 or IPv6 DSCP value, or the streaming interface (RXST) thread that the packet entered host port 0 on.

12.3.1.4.6.3 CPPI Port Ingress

Packets received on the CPPI host port have a received packet priority (0 to 7 with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG register, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port's DSCP priority mapping registers (IPv4 packet).
3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG register, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority

The CPPI Port (port 0) also has a received packet thread. The received packet thread is determined exactly as the received packet priority except for untagged packets. For untagged packets, the received packet thread is the packet streaming interface thread that the packet was received on (instead of the port VLAN priority or DSCP priority). The received packet thread is the hardware switch priority. The received packet thread only determines which hardware switch priority the packet should be sent to, the egress VLAN rules are identical to packets that were received on Ethernet ports (as determined by the header packet priority).

For CPPI ingress packets, the destination port hardware switch priority is the below selected value remapped through CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG:

1. If the ingress packet is priority tagged or vlan tagged:
   - If RX_REMAP_VLAN in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_VLAN in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the the destination hardware switch priority is the packet priority value. Port transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
2. Else if the ingress packet has the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V4 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V4 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit TOS field in byte 15 (upper 6-bits) mapped through the port's DSCP priority mapping registers (IPV4 packet). Port 1 transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
3. Else if the ingress packet has the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V6 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V6 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPV6 packet). Port 1 transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
4. Else the ingress packet is non-tagged and the destination hardware switch priority is the CPPI receive thread number.

12.3.1.4.6.4 Packet CRC Handling

The P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register determines if host port egress packets have CRC included or not. If P0_TX_CRC_REMOVE is set to 1h then all packets that are transmitted from port 0 do not contain CRC. If P0_TX_CRC_REMOVE bit is cleared to 0h then all packets that are transmitted from port 0 contain CRC. The CRC type, if present, is determined by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. If the CRC_TYPE bit is cleared to 0h then the CRC present in each packet after host port egress is Ethernet CRC. If the CRC_TYPE bit is set to 1h then the CRC present in each packet after host port egress is Castagnoli CRC.

Note

The CRC type present in the packet after host port egress is determined solely by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register regardless of the CRC type present in the packet during Ethernet port ingress.

12.3.1.4.6.4.1 Transmit VLAN Processing

Transmit packets are NOT modified during switch egress when the VLAN_AWARE bit in the CPSW3_CONTROL_REG register is cleared to 0h. This means that the switch is not in VLAN-aware mode.

The next three sections cover transmit processing when the switch is in VLAN-aware mode for different packet types. The Gigagibit Ethernet switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW3_CONTROL_REG register. While in VLAN-aware mode, VLAN is added, removed, or replaced according to the type of packet as well as the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header as explained below.

12.3.1.4.6.4.1.1 Untagged Packets (No VLAN or Priority Tag Header)

Untagged packets are all packets that are not a VLAN packet or a priority tagged packet. According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header the packet may exit the switch with a VLAN tag inserted or the packet may leave the switch unchanged. The two cases are discussed below.

- Insert VLAN Case:

  Untagged input packets have the header packet VLAN inserted when the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the transmit packet header is de-asserted. For untagged packets, the VLAN EtherType = 0x8100 is inserted after the source address followed by the two byte header packet VLAN. The header packet VLAN is composed of the header packet priority along with the PORT_CFI and and PORT_VID values from the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PORT_VLAN_REG register (where N is the port that the untagged packet entered the switch) through. The packet length/type field is output four bytes later than it is input and is not removed or replaced. If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a hardware generated CRC.

- No Change Case:

  Untagged input packets are output unchanged when the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS transmit packet header bit is asserted.

12.3.1.4.6.4.1.2 Priority Tagged Packets (VLAN VID == 0 && EN_VID0_MODE ==0h)

Priority tagged packets are packets that contain a VLAN header with VID = 0. According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, priority tagged packets may exit the switch with their VLAN ID and priority replaced or they may have their priority tag completely removed. The two cases are discussed below.

Note

In order for a priority tagged packet to fall into this category the ENABLE_VID0_MODE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register must also be set to 0h. If the ENABLE_VID0_MODE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register is set to 1h, then packets with a VLAN VID of 0 will fall into the VLAN Tagged Packets category in Section 12.3.1.4.6.4.1.3 below.

- Replace Priority and VLAN ID Case:

  Priority tagged input packets have the packet VLAN ID and the packet priority replaced with the header packet VLAN ID and the header packet priority when the transmit packet header CPSW_FORCE_UNTAGGED_EGRESS_REG[1-0] MASK bit is de-asserted. The header packet VLAN ID comes from the PORT_VID bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PORT_VLAN_REG register (where N is the port where the packet entered the switch). The header packet priority is based on the packet priority to header packet priority mapping in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch).

- Remove VLAN Header Case:

  Priority tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority-tagged packets use all four input CRC bytes as pad, input 65-byte priority-tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority-tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.3.1.4.6.4.1.3 VLAN Tagged Packets (VLAN VID != 0 || (EN_VID0_MODE ==1h && VLAN VID ==0))

VLAN tagged packets are packets that contain a VLAN header specifying the VLAN the packet belongs to (VID), the packet priority (PRI), and the drop eligibility indicator (CFI). According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, VLAN tagged packets may exit the switch with their VLAN priority replaced or they may have their VLAN header completely removed. The two cases are discussed below.

- Replace Priority Case:

  VLAN tagged input packets are output with the packet priority replaced with the header packet priority when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is deasserted. The header packet priority is based on the packet priority to header packet priority mapping in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch). If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a generated CRC.

- Remove VLAN Header Case:

  VLAN tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority tagged packets use all four input CRC bytes as pad, input 65-byte priority tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.3.1.4.6.4.2 Ethernet Port Ingress Packet CRC

All Ethernet ports check the ingress packet CRC in all modes/speeds. The receive port can check either Ethernet CRC or Castagnoli CRC as determined by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register.

12.3.1.4.6.4.3 Ethernet Port Egress Packet CRC

Ethernet ports transmit each egress packet with the CRC selected by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register, regardless of the type of CRC that the packet had on ingress to the switch. At the egress port after passing through the switch, the packet CRC is checked for correctness and if the CRC is correct then the packet is output with the generated selected output CRC. If the packet CRC is incorrect, due either to a bit flip in a memory or an error CRC passed in on host ingress, then the generated egress CRC type is used with at least a single byte of the CRC inverted to indicate the error. If the packet length including CRC is divisible by 4 then all 4 CRC bytes will be inverted on error. If there are three bytes remainder after dividing the packet length by 4 then three bytes will be inverted (and so on down to one byte remainder).

12.3.1.4.6.4.4 CPPI Port Ingress Packet CRC

CPPI port ingress packets can be passed in with or without a CRC. The host port is Ethernet CRC only. CPPI ingress packets are not checked for CRC correctness on CPPI ingress, however they are checked for correctness on Ethernet egress and are output with a CRC error if they came in with a CRC error. If a CPPI ingress packet does not have the INFO0 PASSED_CRC bit set then a CRC will be generated for the packet on CPPI ingress. If the PASSED_CRC bit is set then the packet is received and forwarded unchanged. The CRC type is input in the INFO0 word CRC_TYPE bit and must be Ethernet CRC.

12.3.1.4.6.4.5 CPPI Port Egress Packet CRC

The P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register determines if CPPI egress packet have an Ethernet CRC included or not.

12.3.1.4.6.5 FIFO Memory Control

Each of the two CPSW_3G ports has an identical associated FIFO. Each FIFO contains a single logical receive queue and eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each FIFO memory contains 20,480 bytes (20k) total organized as 2560 by 64-bit words contained in a single memory instance. The FIFO memory is used for the associated port transmit and receive queues. The TX_MAX_BLKS field in the FIFOs associated CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG register determines the maximum number of 1k FIFO memory blocks to be allocated to the eight logical transmit queues (transmit total). The RX_MAX_BLKS field in the FIFO's associated CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG register determines the maximum number of 1k memory blocks to be allocated to the logical receive queue. The TX_MAX_BLKS value plus the RX_MAX_BLKS value must sum to 20 (the total number of blocks in the FIFO). If the sum were less than 20, then some memory blocks would be unused. The default is 17 (decimal) transmit blocks and three receive blocks. The FIFOs follow the naming convention of the Ethernet ports. Host Port is Port0 and External Ports is Port1.

Each transmit FIFO contains a configurable number of blocks (20 max) that are either 1k or 4k byte blocks that can be allocated to any priority.

12.3.1.4.6.6 FIFO Transmit Queue Control

There are eight transmit queues in the Ethernet port transmit FIFO. Software has some flexibility in determining how packets are loaded into the queues and on how packet priorities are selected for transmission (how packets are removed and transmitted from queues).

12.3.1.4.6.6.1 CPPI Port Receive Rate Limiting

Port 0 receive operations can be configured to rate limit the host ingress data for each receive thread (priority). CPPI Receive has 8 threads for QOS. There is a committed information rate (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each thread (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a thread when the committed information rate for the thread is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. No bulk thread will be enabled to send unless there are CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PRI_CTL_REG[15-12] TX_HOST_BLKS_REM number of unused blocks remaining in each of the Ethernet port transmit FIFOs. The “blocks remaining check” ensures that bulk traffic from the host will not block rate-limited traffic from the host. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then threads 7 and 6 should be configured for committed information (and excess information if desired). When any channels are configured to be rate-limited, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting is configured for any thread. The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to receive is controlled by the below equation. If the configured excess information rate is zero, then only the committed information rate is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

For example, 10Mbps on priority 7 would give the below:

10Mbps = ~ ((350 * 936) / 32768), at 350Mhz and CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y[27-0] PRI_CIR value = 936 (no excess information rate)

12.3.1.4.6.6.2 Ethernet Port Transmit Rate Limiting

Ethernet port transmit operations can be configured to rate limit egress data for each egress priority. There is a committed information rate (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each priority (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a priority when the committed information rate for the priority is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then priorities 7 and 6 should be configured for committed information (and excess information if desired). The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to send is controlled by the below equation. If the excess information rate is disabled then the committed information rate only is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

12.3.1.4.6.7 Interspersed Express Traffic (IET – P802.3br/D2.0)

When IET is enabled through CPSW3_CONTROL_REG[17] IET_ENABLE = 1h and configured, IET allows premptable traffic on selected transmit priorities to be prempted by express traffic on selected express priorities. Received traffic is separated onto express and prempt receive queues. When IET is disabled (IET_ENABLE = 0h), all Ethernet traffic is express traffic and switch operation is as if IET does not exist. Traffic is only intended to be moved to the prempt queue after premption is verified and enabled.

12.3.1.4.6.7.1 IET Configuration

1. Using the prempt receive queue requires more blocks to be allocate to the ports receive FIFO. Write a value of decimal 7 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG [15-8] TX_MAX_BLKS register for every port to be enabled for IET.
2. Write the [23-0]MAC_VERIFY_CNT bit field in the Ethernet port CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_VERIFY_REG register to set the verify/response timeout count. The default is 10ms for Gigabit mode. For other time values or link speeds the verify

count should be updated. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[2] MAC_DISABLEVERIFY bit is to be set (this is forced mode) then this step is unneeded.

3. The receive FIFO block allocation is insufficient if CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP[31-0] COUNT is nonzero, indicating that receive packets are being dropped due to FIFO block allocation.
4. Write the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register in the Ethernet port as below:
   - Set the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG[16] IET_PORT_EN bit. The port will not actually be enabled until bit IET_ENABLE is set in the CSL_CPSW3_CONTROL_REG.
   - The CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[0] MAC_PENABLE bit can be set as desired. No effect will occur until IET_ENABLE is set. This bit enables premptable packets to be prempted by express traffic but does not preclude packets from being sent to the prempt queue.
   - If verify/response is desired then CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[3] MAC_LINKFAIL should be cleared by software to enable verify and response packets. Otherwise, MAC_DISABLEVERIFY bit should be set for forced mode. Verification and response will occur immediately after clearing this bit.
   - Configure the remaining CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register bits as desired.
5. Set the IET_ENABLE bit in the CSL_CPSW3_CONTROL_REG register to enable IET operations.
6. After preemption has been verified, the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[23-16] MAC_PREMPT field is written to configure the FIFO priorities to be sent to the prempt queue (the other priorities with cleared bits go to the express queue). The hardware switch for each queue from express to prempt happens only when there are no packets queued on the priority.

12.3.1.4.6.8 Enhanced Scheduled Traffic (EST – P802.1Qbv/D2.2)

12.3.1.4.6.8.1 Enhanced Scheduled Traffic Overview

- When enabled and configured, EST allows express queue traffic to be scheduled (placed) on the wire at specific repeatable time intervals.
- EST operates on a repeating time interval generated by the CPTS EST function generator. For example, a 125us repeating time interval can be configured.
- Each Ethernet port has 128 EST fetch commands maximum in the global EST fetch RAM.
- Each 22-bit fetch command consists of a 14-bit fetch count (14 MSB’s) and an 8-bit priority fetch allow (8 LSB’s) that will be applied for the fetch count time in wireside clocks.
- The configured port fetch commands are executed in sequence, beginning at port address zero each time through the time interval beginning at cycle start.
- EST allows non-scheduled express and prempt queue traffic to be cleared from the wire to ensure that the scheduled traffic is transmitted at the proper time (zero allow).
- EST can be used with or without premption. The CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[23-16] MAC_PREMPT value determines whether the priority is enabled on the express or prempt queue. Whether a priority is on the express or prempt queue only effects the wire clear time from an EST operation perspective.
- Software should not move priorities to the prempt queue unless preemption is configured, enabled, and verified allowing preemption to occur.
- Express packet time stamp events can be enabled to assist software in configuring and timing EST operations.

12.3.1.4.6.8.2 Enhanced Scheduled Traffic Fetch RAM

- The EST fetch RAM is read/writable in the CPSW configuration address space.
- The Ethernet transmit port has 128 locations in the global EST fetch RAM.
  - Ethernet port 1 has EST fetch RAM addresses 0x000-0x07F.

- **One buffer operation:** When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF is set to 1h, the 128 port locations operate as one buffer. The EST_BUFACT bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_FIFO_STATUS_REG register is the upper address bit of the port's fetch RAM address indicating whether operation is currently in the upper or lower 64 locations of the port's fetch RAM.
- **Two buffer operation:** When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared there are two 64-location buffers with CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[1] EST_BUFSEL selecting the buffer to be used. When the buffer is switched by changing the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[1] EST_BUFSEL value, the actual switch occurs on cycle start. The actual buffer being used is indicated by the EST_BUFACT bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_FIFO_STATUS_REG. Software should avoid writing the switched out buffer fetch RAM locations until it detects that the actual switch has occurred.
- The first address location in the port's fetch RAM space (location zero) is read at the beginning of each EST time interval (cycle start). Addresses are then read in ascending order for the duration of the interval. The port address zero is then read again at the beginning of the next cycle repeating the time interval packet operations.

12.3.1.4.6.8.3 Enhanced Scheduled Traffic Time Interval

- Each Ethernet port has an Enhanced Scheduled Traffic Function (ESTF) generator in the CPTS submodule.
- The EST function generator generates the EST time interval as a configured number of CPTS reference clocks (CPTS_RFT_CLK).
- The EST function generator rising edge is the cycle start time and the cycle repeats (cycle start occurs) after every time interval.
- The first fetch allowed value is at the port base address zero in the EST fetch RAM and is actually applied 16 wireside clocks after cycle start. The 16 clock cycle delay allows the first fetch value time to be fetched from the EST fetch RAM (prefetch time at cycle start).
- Each successive fetch allow is applied for the associated fetch count thereafter. The minimum non-zero fetch count is 16. The minimum value of 16 guarantees that the next fetch value has time to be fetched before the current fetch count is over. There are 64 maximum fetch values when CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF = 0h, and 128 maximum fetch values when CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF = 1h.
- The next cycle start then causes the fetch to once again start at the port address zero.

12.3.1.4.6.8.4 Enhanced Scheduled Traffic Fetch Values

- The 22-bit fetch value is made up of the 14-bit fetch count and the 8-bit fetch allow.
- The fetch time indicates the number of wireside clocks that the fetch allow will be active.
- The fetch count is in Ethernet wireside clocks which is bytes in Gigabit mode (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[7] GIG = 1h) and nibbles in 10/100Mbps mode.
- When a fetch allow bit is set, the corresponding priority is enabled to begin packet transmission on an allowed priority subject to rate limiting. The actual packet transmission on the wire may carry over into the next fetch count and is the reason for the wire clear time in the fetch zero allow.
- When a fetch allow bit is cleared, the corresponding priority is not enabled to transmit for the fetch count time.
- A non-zero fetch allow value with a non-zero fetch count causes the fetch allow value to be applied for the fetch count number of wireside clocks.
- A zero fetch count causes the associated fetch allow to be held for the duration of the cycle (until the next cycle start).
- A zero fetch allow with a non-zero fetch count is intended to clear the wire for a scheduled (timed) express packet in the next fetch. A zero fetch allow indicates that no packet can be started for transmission for the associated fetch count. The associated fetch count must be sufficient to guarantee that the wire is cleared given that a packet on an allowed priority in the previous fetch could have been started on the previous clock

and that there is hardware latency in the clear time. The timed packet should be sent on a priority that is enabled in the next fetch but disabled in the current zero allow fetch. The fetch allow previous to a zero allow should have only prempt priorities enabled or only express priorities enabled but not both.

- The number of clocks required to clear the wire varies depending Ethernet wire speed and on whether express or prempt priorities were allowed in the previous fetch command.

12.3.1.4.6.8.5 Enhanced Scheduled Traffic Packet Fill

Packet fill can (should) be configured and enabled to occur in the fetch count time associated with a fetched zero allow that preceeds a timed express packet. The intention with fill is that a smaller packet on a non-timed priority might be able to be inserted on the wire during the wire clear time which would increase wire utilization. Fill must be configured to ensure that any fill packet does not conflict with the timed express packet allowed in the next fetch. Incorrect configuration might push out in time any express timed packet which indicates that the fill margin needs to be increased.

Fill Comfiguration:

- The **pn_est_fill_margin** value in **Enet_Pn_EST_Control** should be written with a 0x100 value.
- The **pn_est_prempt_comp** value in **Enet_Pn_EST_Control** should be written with a 0x12 value (if IET is to be configured and enabled). This value times eight is the number of wireside clocks required to clear prempt packets off the wire at the end of a zero allow.
- The **pn_est_fill_en** bit in **Enet_Pn_EST_Control** should be set.

12.3.1.4.6.8.6 Enhanced Scheduled Traffic Time Stamp

The EST can be configured to generate CPTS timestamp events for selected express traffic. The EST timestamp events use the CPTS host event type (CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] EVENT_TYPE = 7 decimal. The EST timestamps will not override host sent timestamps for packets that were sent from the host with an enabled host timestamp.

- EST Events (host events) contain the below information:
  - Time Stamp of the selected express packet.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[28-24] PORT_NUMBER indicates the transmit port number.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] EVENT_TYPE is decimal 7 (host event).
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] MESSAGE_TYPE indicates the packet transmit hardware switch priority.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID upper nibble indicates the packet receive port number.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID lower byte indicates the sequence number of the express packet in numerical order. The first event is event one, the second is event two and so on. The sequence ID rolls over to zero after 0xFF (8-bits).
  - The event domain is the value from the CPSW3_CPSW_NU_EST_TS_DOMAIN_REG[7-0] EST_TS_DOMAIN register.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[2] EST_TS_EN is set, timestamp events will be generated on selected express traffic.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[3] EST_TS_FIRST is also set, events will be generated only on the first express packet in each time interval. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is also set then the event will only be on the first CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet in the time interval. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then the event will be generated on the first express packet in the time interval on any priority.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[3] EST_TS_FIRST is clear, events will be generated on every express packet. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI

is set then the event will be generated on every CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then event will be generated on every express packet on any priority.

12.3.1.4.6.8.7 Enhanced Scheduled Traffic Packets Per Priority

The number of packets allowed in a transmit FIFO priority can be selected by writing a non-zero value to CPSW_P0_RX_PKTS_PRI_REG register (packet priority 0 to 7). Then port 0 receive gap should then be enabled by setting the corresponding priority through CPSW_P0_RX_GAP_REG[7-0] RX_GAP_EN bit field. The receive gap allows a packet to land in the transmit FIFO before another packet is allowed in which guarantees that only the selected number (max) of packets is allowed in on the specified priority. If the receive gap is not enabled, then there might be one or two more packets allowed in on the priority/thread than the packets per priority value has selected (through CPSW_P0_RX_PKTS_PRI_REG register).

12.3.1.4.6.9 Audio Video Bridging

Audio Video Bridging is an ongoing project of IEEE 802.1 concerned with enabling low-latency streaming of time-sensitive audiovisual data over networks. Devices are designated as talkers (transmitters), bridges, or listeners (receivers). It is suggested that the maximum latency could be 2 ms over 7 hops for Class A devices and 20 ms over 7 hops for Class B devices. A hop is essentially a single local area network stage in the journey of a packet. Every time a bridge is encountered between one network section and another a hop is involved. One of the performance goals is that AVB streams will not use more than 75 percent of a link's bandwidth, leaving the remaining capacity for non-AVB streams.

The goal of developing AVB is simply--extend Ethernet's data-networking capabilities to the realm of reliable real-time audio/video networking.

An "Audio Video Bridging" network is one that implements a set of protocols being developed by the IEEE 802.1 Audio/Video Bridging Task Group. There are four primary differences between the proposed Audio Video Bridging architecture and existing 802 architectures (from now on the term "AVB" will be used instead of "Audio Video Bridging"):

1. Precise synchronization - IEEE 802.1AS: "*Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.* "a.k.a Precision Time Protocol (PTP).
2. Traffic shaping for media streams - IEEE 802.1Qav: "*Virtual Bridged Local Area Networks:* Forwarding and Queuing for Time-Sensitive Streams."
3. Admission controls - IEEE 802.1Qat: "*Virtual Bridged Local Area Networks - Amendment 9:* Stream Reservation Protocol (SRP)."
4. Identification of non-participating devices - IEEE 802.1BA: "Audio/Video Bridging (AVB) Systems"

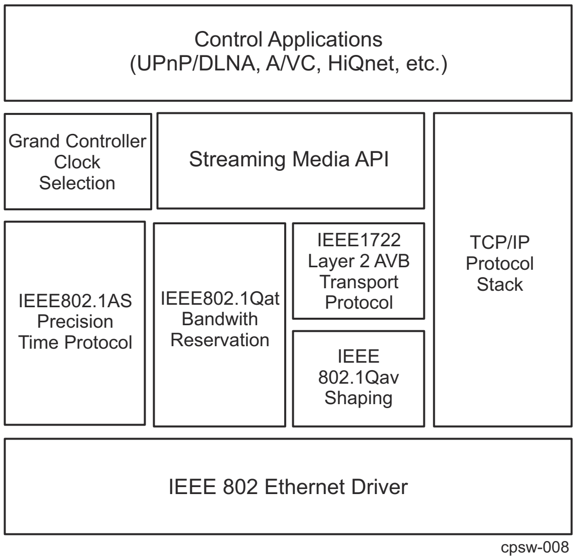

Figure 12-131. The Network Static with AVB

The following sections describe the media transport protocols that work within the AVB framework.

12.3.1.4.6.9.1 IEEE 802.1AS: Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks (Precision Time Protocol (PTP))

The protocol defined by 802.1AS automatically selects a device to be the controller clock, and then distributes this clock throughout the bridged LAN / IP subnet to all other network devices using link-specific transmit/receive time-stamping. However, we only use a two-step solution only on transmit. That is, we do not modify a packet with the timestamp on the way out. The timestamp packet is sent out and then a separate message with the timestamp is sent by the host afterward. Receive can be one or two step.

Note

The 802.1AS-distributed clock is not used as a media clock. Rather, the shared 802.1AS clock reference is used to regenerate the media clock at the listener/renderer. Such a reference removes the need to force the latency of the network to be constant, or compute long running averages in order to estimate the actual media rate of the transmitter in the presence of substantial network jitter. IEEE 802.1AS is based on the ratified IEEE 1588 standard.

Based on IEEE 1588:2002,A PTP devices exchange standard Ethernet messages that synchronize network nodes to a common time reference by defining clock controller selection and negotiation algorithms, link delay measurement and compensation, and clock rate matching and adjustment mechanisms.

Designed as a simplified profile of IEEE 1588, a primary difference between 1588 and IEEE 802.1AS is that PTP is a layer 2-in other words, a non-IP routable protocol. Like IEEE 1588, PTP defines an automatic method for negotiating the network clock controller, the Best Controller Clock Algorithm (BCCA). PTP nodes can be assigned one of eight priority levels, presumably based on clock quality. BCCA defines the underlying negotiation and signaling mechanism whose purpose is to identify the AVB LAN Grandcontroller. Once a Grandcontroller has been selected, synchronization automatically begins.

At the core of 802.1AS synchronization is time-stamping. In short, during PTP message ingress/egress from the 802.1AS-capable MAC, the PTP Ether type triggers the sampling of the value of a local real-time counter (RTC). Target nodes compare the value of their RTC against the PTP Grandcontroller and, by use of link delay measurement and compensation techniques, match their RTC value to the time of the AVB LAN PTP domain. After network time throughout the AVB LAN has converged, periodic SYNC and FOLLOW_UP messages provide the information that enables the PTP rate matching adjustment algorithms. The result is all PTP nodes are then synchronized to the same "Wall Clock" time. PTP assures 1-μs accuracy over seven network hops.

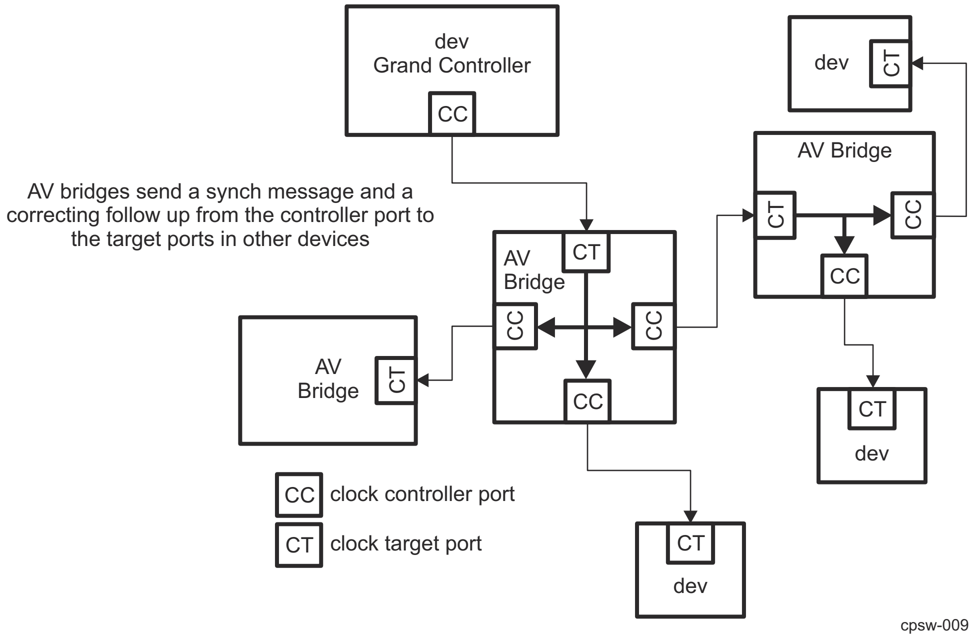

Figure 12-132. AVB Network & PTP Clock Entities

The media transport protocols that work within the AVB framework are:

12.3.1.4.6.9.1.1 IEEE 1722: "Layer 2 Transport Protocol for Time-Sensitive Streams"

AVBTP or 1722 sits above the IEEE 802.1 AVB plumbing and below the application layer. It acts as the conduit between an Ethernet MAC and a streaming application. AVBTP abstracts the underlying network transmission channel to enable the virtual connection of distributed audio and video CODECs over reliable Ethernet networks. A complete AVBTP Ethernet packet is shown in Figure 12-133 and illustrates how IEC 61883-6 AM824 uncompressed audio samples are encapsulated in an Ethernet frame.

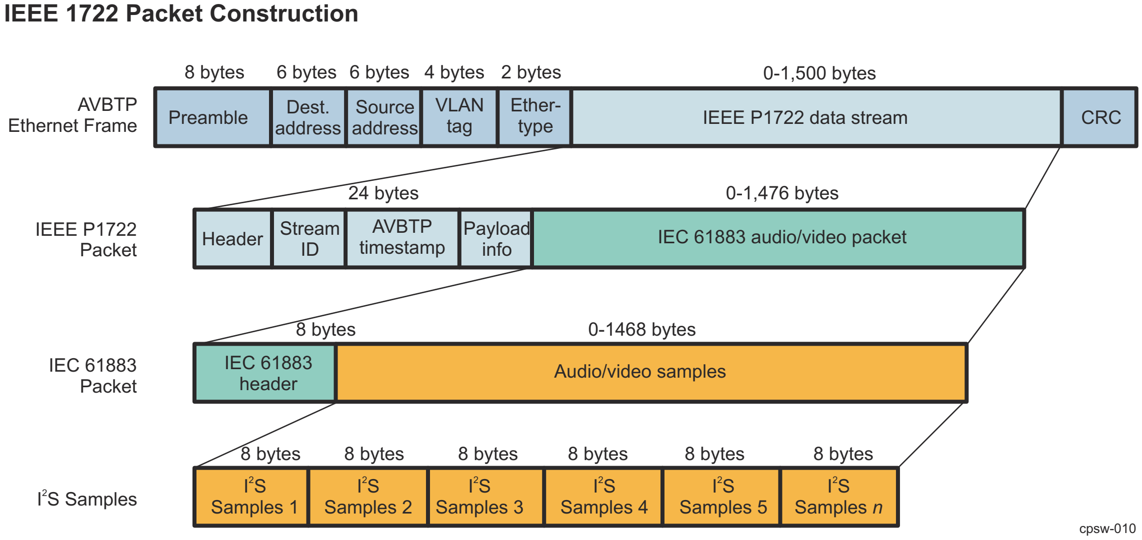

Figure 12-133. IEEE 1722 Packets

1722 or AVBTP Presentation Time and Synchronization:

Synchronization in an AVB network starts with the Precision Time Protocol but ends with synchronized media clocks. PTP is responsible for synchronizing all nodes in an AVB network to identical wall clock time; not for synchronizing media clocks. In other words, PTP does not actually transport synchronized media clocks but instead provides a low-level building block crucial for managing a distributed media synchronization system.

A crucial benefit of this approach is coexistence of multiple, independent media clock domains on an AVB network. Unrelated audio and video streams can simultaneously exist in the same LAN.

12.3.1.4.6.9.1.1.1 Cross-timestamping and Presentation Timestamps

AVBTP assumes that AVB node media clocks are clocked by free-running oscillators. It is also assumed that the node's internal concept of wall clock time has been synchronized to the PTP Grandcontroller. AVBTP media clock sources embed "AVBTP Presentation Timestamps" in AVBTP streaming packets. Figure 12-134 illustrates the relationship between PTP network time and AVBTP Presentation Timestamps.

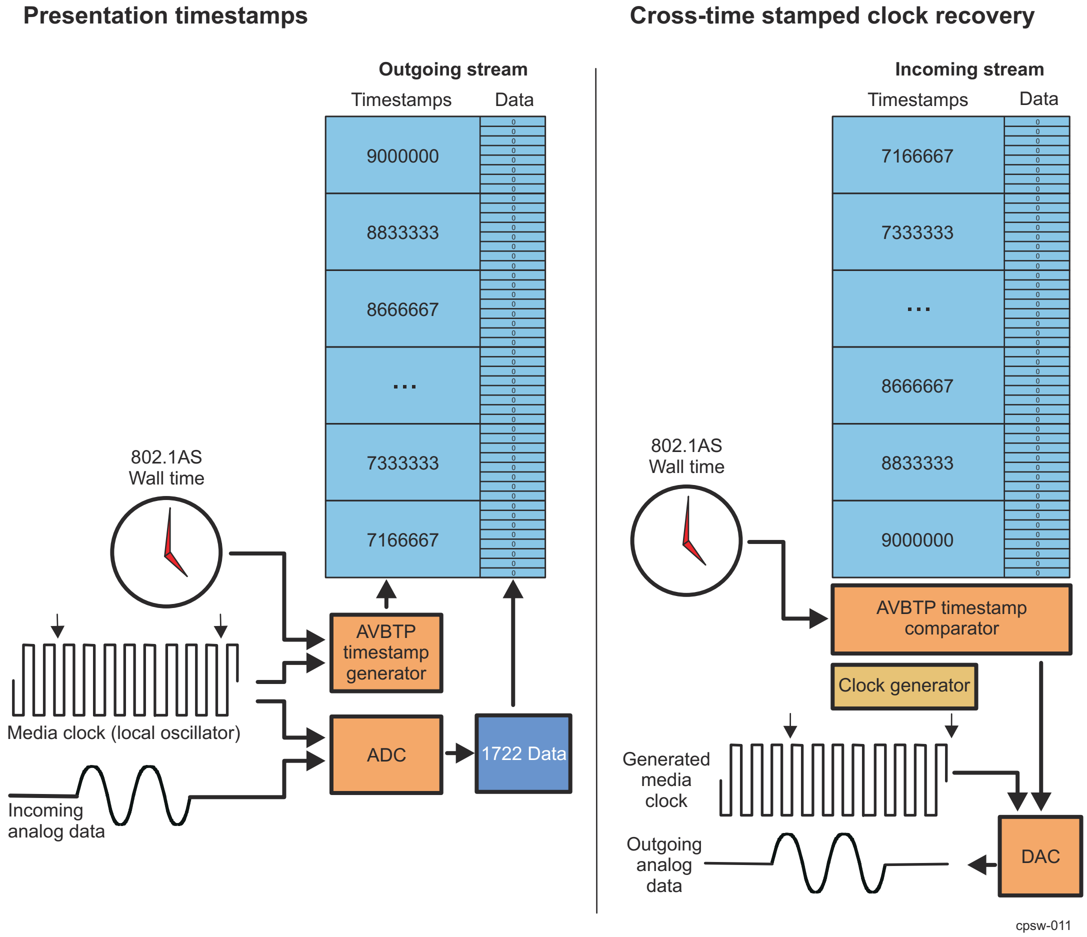

Figure 12-134. Cross Time Stamping and Presentation Timestamps

12.3.1.4.6.9.1.2 IEEE 1733: Extends RTCP for RTP Streaming over AVB-supported Networks

This standard specifies the protocol, data encapsulations, connection management and presentation time procedures used to ensure interoperability between audio and video based end stations that use standard networking services provided by all IEEE 802 networks meeting QoS requirements for time-sensitive applications by leveraging the Real-time Transport Protocol (RTP) family of protocols and IEEE 802.1 Audio/Video Bridging (AVB) protocols.

12.3.1.4.6.9.2 IEEE 802.1Qav: "Virtual Bridged Local Area Networks: Forwarding and Queuing for Time-Sensitive Streams"

This standard allows bridges to provide guarantees for time-sensitive (that is, bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data transmission (AV traffic). It specifies per priority ingress metering, priority regeneration, and timing-aware queue draining algorithms. This standard uses the timing derived from IEEE 802.1AS. Virtual Local Area Network (VLAN) tag encoded priority values are allocated, in aggregate, to segregate frames among controlled and non-controlled queues, allowing simultaneous support of both AV traffic and other bridged traffic over and between wired and wireless Local Area Networks (LANs).

Such a guarantee in bandwidth is provided by two functional entities:

- A registration protocol, which registers the service and its maximum network utilization with a device or switch (IEEE 802.1Qat: "Virtual Bridged Local Area Networks - Amendment 9: Stream Reservation Protocol (SRP)")
- A hardware bandwidth management service.
  - Receive policing
  - Transmit rate control.

End Station Behavior

In order for an end station to successfully participate in the transmission and reception of time-sensitive streams, it is necessary for their behavior to be compatible with the operation of the forwarding and queuing mechanisms employed in bridges.

The requirements for end stations that participate as "talkers" i.e., sources of time-sensitive streams are different from the requirements that apply to "listeners", the destination station(s) for the streams.

Talker Behavior

In order for Talker-originated data streams to make use of the credit-based shaper behavior in Bridges, it is a requirement for a Talker to use the priorities that the Bridges in the network recognize as being associated with SR classes exclusively for transmitting stream data.

It is also necessary for the Talker and the Bridges in the path to the Listener(s), to have a common view of the bandwidth required in order to transmit the Talker's streams, and for that bandwidth to be reserved along the path to the Listener(s). This latter requirement can be met by means of stream reservation mechanisms, such as defined in SRP, or by other management means.

End stations that are Talkers shall exhibit transmission behavior for frames that are part of "time-sensitive streams" that is consistent with the operation of the credit-based shaper algorithm, both in terms of the way they transmit frames that are part of an individual data stream, and in terms of the way they transmit stream data frames from a Port.

In effect, the queuing model for a Talker Port (and a Listener port), and for given priorities, can be considered to look like Figure 12-135.

Listener Behavior

The primary requirement for a listener station is that it is capable of buffering the amount of data that could be transmitted for a stream during a time period equivalent to the accumulated maximum jitter that could be experienced by stream data frames in transmission between Talker and Listener.

From the point of view of the specification of the forwarding and queuing requirements for time-sensitive streams, it is assumed that the listener will assess the buffering required for a stream as part of the stream bandwidth reservation mechanisms employed by the implementation.

The credit-based shaper's operation details are beyond the scope of this document.

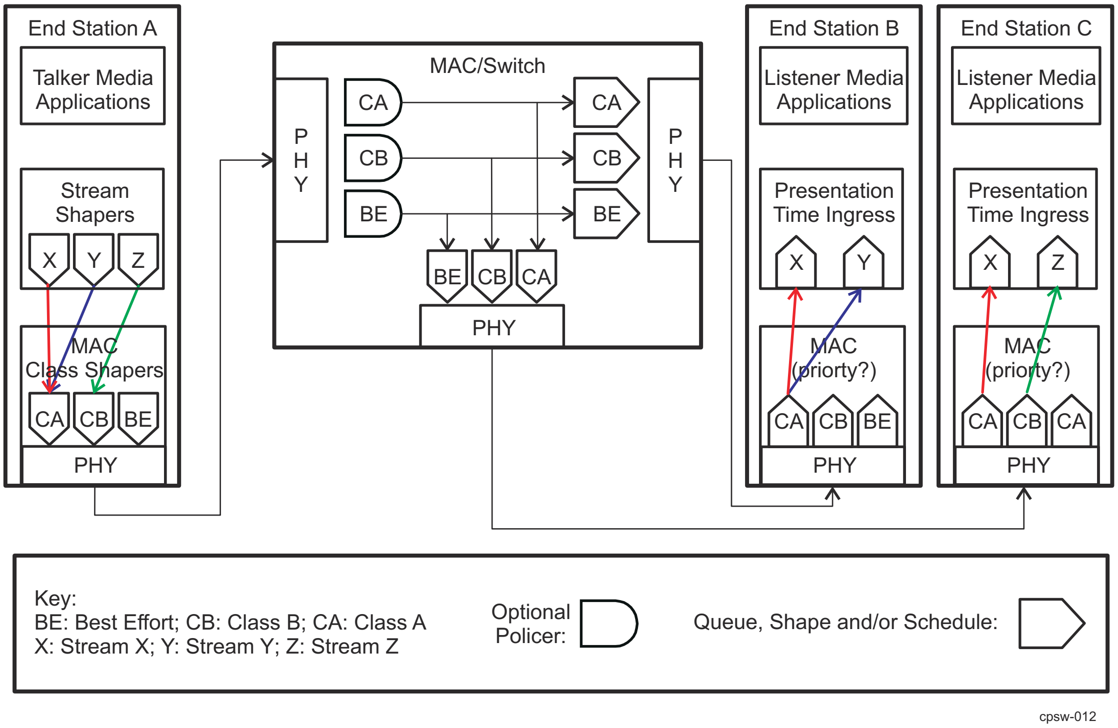

Figure 12-135. AV Stream Queuing/Policing

12.3.1.4.6.9.2.1 Configuring the Device for 802.1Qav Operation

There is no dedicated register-set to be configured for the time-sensitive stream handling. The list of functional features of CPSW_3G that will have to be configured are:

- DESCRIPTORS and CHANNEL CONFIGURATIONS:
  - CPPI TX and RX descriptors
  - VLAN and Priority tags

Table 12-157. Example of TX Configuration

TX DMA CHANNEL	Packet Priority	Switch Queue Priority
7	7	3
6	5	2
5	3	1
4	1	0

Table 12-158. Example of RX Configuration

RX DMA CHANNEL	Packet Priority	Switch Queue Priority
0	7	0
0	5	0
0	3	0
0	1	0

- ALE Configuration:
  - ALE in VLAN-ware mode, Non-ALE in bypass mode.

12.3.1.4.6.10 Ethernet MAC Sliver

The Ethernet port peripheral is compliant to the IEEE Std 802.3 Specification. Half-duplex mode is supported in 10/100 Mbps mode, but not in 1000 Mbps (gigabit) mode.

Features:

- Synchronous 10/100/1000 Mbit operation
- RMII/RGMII Interface
- Hardware Error handling including CRC
- Full-Duplex Gigabit operation (half-duplex gigabit is not supported)
- EtherStats and 802.3Stats RMON statistics gathering support for external statistics collection module
- Transmit CRC generation selectable on a per channel basis
- Emulation Support
- VLAN Aware Mode Support
- Hardware flow control
- Programmable Inter Packet Gap (IPG).

12.3.1.4.6.10.1 Ethernet MAC Sliver Overview

12.3.1.4.6.10.1.1 CRC Insertion

The MAC generates and appends a 32-bit Ethernet CRC onto the transmitted data, if the transmit packet header PASS_CRC bit is 0h. For the Ethernet port generated CRC case, a CRC at the end of the input packet data is not allowed.

If the header word PASS_CRC bit is set, then the last four bytes of the TX data are transmitted as the frame CRC. The four CRC data bytes should be the last four bytes of the frame and should be included in the packet byte count value. The MAC performs no error checking on the outgoing CRC when the PASS_CRC bit is set.

12.3.1.4.6.10.1.2 MTXER

The MTXER signal is only used for EEE. If an underflow condition occurs on a transmitted frame, the frame CRC will be inverted to indicate the error to the network. Underflow is a hardware error.

12.3.1.4.6.10.1.3 Adaptive Performance Optimization (APO)

The Ethernet MAC port incorporates Adaptive Performance Optimization (APO) logic that may be enabled by setting the TX_PACE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. Transmission pacing to enhance performance is enabled when set. Adaptive performance pacing introduces delays into the normal transmission of frames, delaying transmission attempts between stations, reducing the probability of collisions occurring during heavy traffic (as indicated by frame deferrals and collisions) thereby increasing the chance of successful transmission.

When a frame is deferred, suffers a single collision, multiple collisions or excessive collisions, the pacing counter is loaded with an initial value of 31. When a frame is transmitted successfully (without experiencing a deferral, single collision, multiple collision or excessive collision) the pacing counter is decremented by one, down to zero.

With pacing enabled, a new frame is permitted to immediately (after one IPG) attempt transmission only if the pacing counter is zero. If the pacing counter is non zero, the frame is delayed by the pacing delay, a delay of approximately four inter-packet gap delays. APO only affects the IPG preceding the first attempt at transmitting a frame. It does not affect the back-off algorithm for re-transmitted frames.

12.3.1.4.6.10.1.4 Inter-Packet-Gap Enforcement

The measurement reference for the IPG of 96-bit times is changed depending on frame traffic conditions. If a frame is successfully transmitted without collision, and MCRS is de-asserted within approximately 48-bit times of MTXEN being de-asserted, then 96-bit times is measured from MTXEN. If the frame suffered a collision, or if MCRS is not de-asserted until more than approximately 48-bit times after MTXEN is de-asserted, then 96-bit times (approximately, but not less) is measured from MCRS.

The Ethernet port transmit inter-packet gap (IPG) may be shortened by eight bit times when short gap is enabled and triggered. Setting the [10] TX_SHORT_GAP_ENABLE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register enables the gap to be shortened when triggered. The condition is triggered when the ports associated transmit packet FIFO has a user defined number of FIFO blocks used. The associated transmit FIFO blocks used value determines if the gap is shortened, and so on. The CPSW3_CPSW_NU_GAP_THRESH_REG register value determines the short gap threshold. If the FIFO blocks used is greater than or equal to the GAP_THRESH value then short gap is triggered.

12.3.1.4.6.10.1.5 Back Off

The Gigabit Ethernet Mac Sliver implements the 802.3 binary exponential back-off algorithm.

12.3.1.4.6.10.1.6 Programmable Transmit Inter-Packet Gap

The transmit inter-packet gap (IPG) is programmable through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. The default value is decimal 12. The transmit IPG may be increased to the maximum value of 1FFh. Increasing the IPG is not compatible with transmit pacing. The short gap feature will override the increased gap value, so the short gap feature may not be compatible with an increased IPG.

12.3.1.4.6.10.1.7 Speed, Duplex and Pause Frame Support Negotiation

The Ethernet port can operate in half duplex or full duplex in 10/100 Mbit modes, and can operate in full duplex only in 1000 Mbit mode. Pause frame support is included in 10/100/1000 Mbit modes as configured by the host.

12.3.1.4.6.10.2 RMII Interface

The CPRMII peripheral is compliant to the RMII specification document.

12.3.1.4.6.10.2.1 Features

- Source Synchronous 10/100 Mbit operation
- Full and Half Duplex support

12.3.1.4.6.10.2.2 RMII Receive (RX)

The CPRMII receive (RX) interface converts the input data from the external RMII PHY (or switch) into the required MII (CPGMAC) signals. The carrier sense and collision signals are determined from the RMII input data stream and transmit inputs as defined in the RMII specification.

An asserted RMII_RXER on any di-bit in the received packet will cause an MII_RXER assertion to the CPGMAC during the packet. In 10Mbps mode, the error is not required to be duplicated on 10 successive clocks. Any di-bit which has an asserted RMII_RXER during any of the 10 replications of the data will cause the error to be propagated.

Any received packet that ends with an improper nibble boundary aligned RMII_CRS_DV toggle will issue an MII_RXER during the packet to the CPGMAC. Also, a change in speed or duplex mode during packet operations will cause packet corruption.

The CPRMII can accept receive packets with shortened preambles, but 0x55 followed by a 0x5D is the shortest preamble that will be recognized (1 preamble byte with the start of frame byte). At least one byte of preamble with the start of frame indicator is required to begin a packet. An asserted RMII_CRS_DV without at least a single correct preamble byte followed by the start of frame indicator will be ignored.

12.3.1.4.6.10.2.3 RMII Transmit (TX)

The CPRMII transmit (TX) interface converts the CPGMAC MII input data into the RMII transmit format. The data is then output to the external RMII PHY.

The CPGMAC does not source the transmit error (MII_TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be de-asserted at all times and is not an input into the CPRMII module. Zeroes are output on RMII_TXD[1:0] for each clock that RMII_TXEN is de-asserted.

12.3.1.4.6.10.3 RGMII Interface

The CPRGMII peripheral is compliant to the RGMII specification document.

12.3.1.4.6.10.3.1 Features

- Supports 1000/100/10 Mbps speed
- Full and Half Duplex support (CPGMAC supports only Full duplex in Gigabit mode).
- MII mode support
- Energy Efficient Ethernet Support

12.3.1.4.6.10.3.2 RGMII Receive (RX)

The CPRGMII receive (RX) interface converts the source synchronous DDR input data from the external RGMII PHY into the required G/MII (CPGMAC) signals.

12.3.1.4.6.10.3.3 In-Band Mode of Operation

The CPRGMII is operating in the in-band mode of operation when the RGMII_RX_INBAND input is asserted. RGMII_RX_INPUT is asserted by configuring the CTL_EN bit to 1h of the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. The link status, duplexity, and speed are determined from the RGMII input data stream RXD[3:0] when RX_CTL is deasserted, as defined in the RGMII specification. The PHY might need to be configured beforehand to output in-band data. The in-band data is indicated as shown in Table 12-159.

Table 12-159. In-Band Data

RXD3	RXD[2:1]		RXD0
Duplex status:	Link Speed:	RXC_CLK Speed:	Link Status:
0h: half-duplex	0h: 10-Mbps mode	2.5 MHz	0h: Link is down
1h: full-duplex	1h: 100-Mbps mode	25 MHz	1h: Link is up
	2h: 1000-Mbps mode	125 MHz	
	3h: Reserved	Reserved	

12.3.1.4.6.10.3.4 Forced Mode of Operation

The CPRGMII is operating in the forced mode of operation when the RGMII_RX_INBAND input is deasserted by setting to 0h bit CTL_EN of the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. In the forced mode of operation, the in-band data is ignored if present.
The link status is forced high, and the duplexity and speed are determined from the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[0] FULLDUPLEX and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[7] GIG bits. If bit [7] GIG = 1h, then CPRGMII is operating in Gigabit mode. If bit [7] GIG is cleared (0h), then CPRGMII is operating in 100 Mbps mode.

12.3.1.4.6.10.3.5 RGMII Transmit (TX)

The CPRGMII transmit (TX) interface converts the CPGMAC G/MII input data into the DDR RGMII format. The DDR data is then output to the external PHY.

The CPGMAC does not source the transmit error (TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be deasserted at all times and is not an input into the CPRGMII module.

In 10/100 Mbps mode, the TXD[7:0] data bus uses only the lower nibble. The CPRGMII will output the lower nibble twice in 10/100 Mbps mode to avoid unnecessary signal switching.

Packets will be precluded from transmission through the CPRGMII module for 4096 transmit clocks after the rising edge of RGMII_LINK. Packet transmission will begin on the first TX_CTL rising edge after the 4096 transmit clock count has expired.

12.3.1.4.6.10.4 Frame Classification

Received frames are proper (good) frames if they are between 64 and CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN in length (inclusive) and contain no errors (code/align/CRC).

Received frames are long frames if their frame count exceeds the value in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG/ CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG register. The register reset (default) value is 1518 (decimal). Long received frames are either oversized or jabber frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment errors are jabber frames.

Received frames are short frames if their frame count is less than 64 bytes. Short frames that contain no errors are undersized frames. Short frames with CRC, code, or alignment errors are fragment frames. If RX_CSF_EN bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG is set to 1h, undersized frames from 33 to 63 bytes will be forwarded only to the host on a best effort basis (meaning that the ALE may or may not be able to keep up with the packet rate and the short packet may be dropped due to bandwidth limitations). If RX_CSF_EN and RX_CEF_EN in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG are set, fragment frames from 33 to 63 bytes will also be forwarded only to the host on a best effort basis. Ethernet port received frames shorter than 33 bytes are dropped in all cases.

A received long packet will always contain RX_MAXLEN number of bytes transferred to memory (if CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[22]RX_CEF_EN = 1h). An example with RX_MAXLEN = 1518 is:

- If the frame length is 1518, then the packet is not a long packet and there will be 1518 bytes transferred to memory.
- If the frame length is 1519, there will be 1518 bytes transferred to memory. The last three bytes will be the first three CRC bytes.
- If the frame length is 1520, there will be 1518 bytes transferred to memory. The last two bytes will be the first two CRC bytes.
- If the frame length is 1521, there will be 1518 bytes transferred to memory. The last byte will be the first CRC byte.

If the frame length is 1522, there will be 1518 bytes transferred to memory. The last byte will be the last data byte.

12.3.1.4.6.10.5 Receive FIFO Architecture

This section describes the architecture of the Ethernet port's receive FIFOs. Internal to the Gigabit Ethernet switch, all Ethernet ports have an identical associated packet FIFO. Each transmit packet FIFO contains eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each transmit FIFO memory contains 81,920 bytes total organized as 2560 by 256-bit words. Each FIFO also contains a single memory for the receive queue. Each receive FIFO memory contains a total of 32768 bytes total organized as 1024 by 256-bit words.

12.3.1.4.6.11 Embedded Memories

Table 12-160. Embedded Memories

Memory Type Description	Number of Instances	
Single-port 3072-word × 64 RAM	1	(Combined FIFO RAM)
Single-port 128-word × 28-bit RAM	1	1 (EST)

12.3.1.4.6.12 Memory Error Detection and Correction

The CPSW_3G error detection and correction logic uses the ECC Aggregator Module.

The CPSW3_ECC_ECC_VECTOR register is used to select which ECC RAM's status and control registers are currently being read or written as shown in Table 12-161. The CPSW FIFO RAMs implement ECC only on packet headers. The packet data is protected by Ethernet CRC. The ALE and EST RAMs have complete ECC as normal.

Table 12-161. ECC RAM to CPSW RAM Mapping

ECC RAM Number	CPSW RAM
0	ALE RAM
1	Port 0 FIFO RAM

12.3.1.4.6.12.1 Packet Header ECC

Only packet headers bits are protected by ECC in the FIFO RAMs. The ECC_ERR_CTRL1[31-0] ECC_ROW bit is used to activate a row address where force single-bit error or force double-bit error needs to be applied. ECC_ERR_CTRL2 [15-0] ECC_BIT1 is implemented to determine which bit of the header is flipped for an SEC error when the ECC_CRC_MODE bit is cleared in the CPSW3_CONTROL_REG register. The ECC status registers return the RAM row address where the single or double-bit error has occured (ECC_ERR_STAT2[31-0] ECC_ROW) along with the bit position in the RAM data that is in error (ECC_ERR_STAT1[31-16] ECC_BIT1 value). Forcing double-bit errors in testing can cause indeterminate operation if multiple used packet header bits are flipped given that only single-bit errors are fixed by the ECC logic. Header bits 207 down to 200 are not currently used in the CPSW and may be used to test double bit errors without the possibility of requiring a reset for the switch to recover from the double bit error. No header bits are flipped when ECC_CRC_MODE is set to 1h. Either the RX_ECC_ERR_EN (enable receive ECC error operations) or the TX_ECC_ERR_EN (enable transmit ECC error operations) bits must be set in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register to test ECC header errors.

The header ECC code is stored in bits 255 down to 208. If any bit is flipped in the ECC code, the flipped bit will be corrected, but the index of the flipped bit will be reported as bit zero. This implies that when the aggregator reports that there is a SEC on bit 0, it can mean two things: either SEC on data bit 0 or SEC somewhere inside the ECC code. Any packet header with ECC error issues a pulse interrupt (ECC_PULSE_INTR) as does an ALE RAM ECC error.

12.3.1.4.6.12.2 Packet Protect CRC

Each packet received without error is passed through the CPSW_3G memories with a generated Ethernet protect CRC. The protect CRC is checked on egress for correctness and removed. If the CRC is correct (no RAM bit errors), then the packet is output with the selected port CRC type. If a protect CRC error is detected on host egress then the TXST_DROP signal will be asserted so that the packet is dropped to the host. If a protect CRC error is detected on Ethernet egress then the egress CRC will be generated on the packet and at least one byte of the CRC will be inverted on output. CRC memory protect errors do not assert the ECC_PULSE_INTR signal. CRC memory protect errors are counted in the associated port statistics registers and issue an interrupt on STAT_PEND_INTR if any CRC memory protect error occurs (and the statistics for that port are enabled). When the ECC_CRC_MODE bit in the CSL_CPSW3_CONTROL_REG register is set, the ECC_ERR_CTRL2 [15-0] ECC_BIT1 bit field will flip the associated column bit in any FIFO memory read operation, inducing a CRC protect error when the protect CRC is checked. No header bits are flipped when ECC_CRC_MODE is set. Either the RX_ECC_ERR_EN or the TX_ECC_ERR_EN bits must be set in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register to test packet CRC errors.

12.3.1.4.6.12.3 Aggregator RAM Control

The ECC logic for each FIFO RAM (receive and transmit) is divided into eight separate ECC encoders/decoders that encode/decode 26-bits of data each. Each of the 8 encoders (0 to 7) generates 6-bits of ECC code (48 code bits total), and each of the eight decoders (0 to 7) checks 6-bits of ECC code across the 26-bits of data (208 data bits total). The 48-bits of ECC code are passed through the RAM in the upper 48 unused bits in the header word.

The header data bits and ECC code bits are shown in Table 12-162. The [15-0] ECC_BIT1 value returned on error is a 16-bit value that is the concatenation of 5 bits of zero, 3 bits of the encoder/decoder number (0 to 7), 3 bits of zero, and 5 bits of index into the indicated 26-bit encoder/decoder.

For example, an ECC_BIT1 value of 0x0308 is bit 8 of encoder/decoder 3, which is header bit 86 (that is, (26×3) + 8).

Table 12-162. ECC Submodule Header Data Bit to Encoder/Decoder Mapping

Header Data Bits	Encoder/Decoder
25:0	Encoder/Decoder 0 Data
51:26	Encoder/Decoder 1 Data
77:52	Encoder/Decoder 2 Data
103:52	Encoder/Decoder 3 Data
129:104	Encoder/Decoder 4 Data
155:130	Encoder/Decoder 5 Data
181:156	Encoder/Decoder 6 Data
207:182	Encoder/Decoder 7 Data
213:208	Encoder/Decoder 0 ECC
219:214	Encoder/Decoder 1 ECC
225:220	Encoder/Decoder 2 ECC
231:226	Encoder/Decoder 3 ECC
237:232	Encoder/Decoder 4 ECC
243:238	Encoder/Decoder 5 ECC
249:244	Encoder/Decoder 6 ECC
255:250	Encoder/Decoder 7 ECC

12.3.1.4.6.13 Ethernet Port Flow Control

The Ethernet port have flow control available for transmit and receive. Transmit flow control stops the Ethernet port from transmitting packets to the wire (switch egress) in response to a received pause frame. Transmit flow control does not depend on FIFO usage.

The Ethernet port have flow control available for receive operations (packet ingress). Ethernet port receive flow control is initiated when enabled and triggered. Packets received on an Ethernet port can be sent to the CPPI port. The destination port can trigger the receive Ethernet port flow control. An Ethernet destination port triggers another Ethernet receive flow control when the destination port is full.

When a packet is received on an Ethernet port interface with enabled flow control the below occurs:

- The packet will be sent to all ports that currently have room to take the entire packet.
- The packet will be retried until successful to all ports that indicate they don't have room for the packet.

The flow control trigger to the Ethernet port will be asserted until the packet has been sent, and there is room in the logical receive FIFO for packet runout from another flow control trigger (RX_BLK_CNT = 0h). Ethernet port receive flow control is disabled by default on reset. Ethernet port receive flow control requires that the RX_FLOW_EN bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG be set to 1h. When receive flow control is enabled on a port, the port's associated FIFO block allocation must be adjusted. The port RX allocation must increase from the default three blocks to accommodate the flow control runout. A corresponding decrease in the TX block allocation is required. If a sending port ignores a pause frame then packets may overrun on receive (and be dropped) but will not be dropped on transmit.

12.3.1.4.6.13.1 Ethernet Receive Flow Control

For every Ethernet port to be configured for fullduplex receive flow control, write a value of decimal 7 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[15-8] TX_MAX_BLKS register. This re-allocation allows for flow control runout on the receive FIFO at the expense of FIFO memory on the Ethernet transmit side. 10/100Mbps half-duplex collision based receive flow control does not need this re-allocation. Receive flow control is enabled by the RX_FLOW_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register.

12.3.1.4.6.13.1.1 Collision Based Receive Buffer Flow Control

Collision-based receive buffer flow control provides a means of preventing frame reception when the port is operating in half-duplex mode (FULLDUPLEX is cleared in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG). When receive flow control is enabled and triggered, the port will generate collisions for received frames. The jam sequence transmitted will be the twelve byte sequence C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3 (hex). The jam sequence will begin no later than approximately as the source address starts to be received. Note that these forced collisions will not be limited to a maximum of 16 consecutive collisions, and are independent of the normal back-off algorithm. Receive flow control does not depend on the value of the incoming frame destination address. A collision will be generated for any incoming packet, regardless of the destination address.

12.3.1.4.6.13.1.2 IEEE 802.3X Based Receive Flow Control

IEEE 802.3x based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (FULLDUPLEX bit is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register). When receive flow control is enabled and triggered, the port will transmit a pause frame to request that the sending station stop transmitting for the period indicated within the transmitted pause frame.

The Ethernet port will transmit a pause frame to the reserved multicast address at the first available opportunity (immediately if currently idle, or following the completion of the frame currently being transmitted). The pause frame will contain the maximum possible value for the pause time (FFFFh). The MAC will count the receive pause frame time (decrements FF00h down to 0) and retransmit an outgoing pause frame if the count reaches zero. When the flow control request is removed, the MAC will transmit a pause frame with a zero pause time to cancel the pause request.

Note that transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval will be received normally (provided the RX FIFO is not full at which time the receive FIFO will overrun and CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP[31-0] COUNT value will increment).

Pause frames will be transmitted if enabled and triggered regardless of whether or not the port is observing the pause time period from an incoming pause frame.

The Ethernet port will transmit pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01.
- The 48-bit source address - from SL_SA[47-0] input.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause time value FF.FF. A pause-quantum is 512 bit-times. Pause frames sent to cancel a pause request will have a pause time value of 00.00.
- Zero padding to 64-byte data length (The Ethernet port will transmit only 64 byte pause frames).
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[3] RX_FLOW_EN is cleared to 0h while the pause time is nonzero, then the pause time will be cleared to 0h and a 0 count pause frame will be sent.

12.3.1.4.6.13.2 Flow Control Trigger

Receive flow control is triggered (when enabled), when the number of words in the receive FIFO is greater than or equal to the value writen in the CPSW_PN_RX_FLOW_THRESH_REG[8-0] COUNT bit field. The flow control packet runout is then contained in the remainder of the receive FIFO.

12.3.1.4.6.13.3 Ethernet Transmit Flow Control

Incoming pause frames are acted upon, when enabled, to prevent the Ethernet port from transmitting any further frames. Incoming pause frames are only acted upon when the [0] FULLDUPLEX and [4] TX_FLOW_EN bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register are set. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames will be transferred to memory if the [24] RX_CMF_EN (RX Copy MAC Control Frames Enable) bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register is set. The [4] TX_FLOW_EN and [0] FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

Pause frames are a subset of MAC Control Frames with an opcode field = 0001h. Incoming pause frames will only be acted upon by the port if:

- [4] TX_FLOW_EN is set in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register, and
- the RX maximum frame length is 64 bytes inclusive (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN), and
- the frame contains no CRC error or align/code errors.

The pause time value from valid frames will be extracted from the two bytes following the opcode. The pause time will be loaded into the port's transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame then:

- if the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- if the new pause time value is zero then the transmit pause timer will immediately expire, else the port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded).

If [4] TX_FLOW_EN in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register is cleared, then the pause-timer will immediately expire.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming pause frames consist of the below:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or the Ethernet port SL_SA [47:0] input.
- The 48-bit source address of the transmitting device.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_TX_PAUSETIMER_REG[15-0] TX_PAUSETIMER. A pause-quantum is 512 bit-times.
- Padding to 64-byte data length.
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 Bytes. The standard allows pause frames longer than 64 Bytes to be discarded or interpreted as valid pause frames. The Ethernet port will recognize any pause frame between 64 Bytes and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes in length.

12.3.1.4.6.14 Energy Efficient Ethernet Support (802.3az)

Energy Efficient Ethernet (EEE) allows the LPSC to turn off the module clock during inactive periods as determined by network and host traffic. The module can then be awakened by host queued transmit packet(s) or by a port's external Ethernet PHY. The module EEE clock stop interface is used by the external controller to control module EEE operations. EEE operations are configured as shown below:

1. The 12-bit EEE clock pre-scale value is written to the CPSW3_CPSW_NU_EEE_PRESCALE_REG register. The pre-scaler is used to clock all EEE-related counters
2. The port Idle to LPI count values (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IDLE2LPI_REG[23-0] COUNT) are written with the desired values
3. The port LPI to Wake count values (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_LPI2WAKE_REG[23-0] COUNT) are written with the desired values
4. The [0] EEE_EN bit is set in the switch CSL_CPSW3_CPSW_NU_CONTROL_REG register

EEE operation can begin after configuration. The host allows (through LPSC) the CPSW to enter a low power state by asserting the EEE_CLKSTOP_REQ signal. There are no requirements on host queues or traffic in order for the host to assert or de-assert EEE_CLKSTOP_REQ to the CPSW.

Each Ethernet port has a transmit and a receive LPI (low power indicate) state. The PHY indicates LPI by asserting MRXER with a MRXD[7:0] value of 0x01 while MRXDV is deasserted (inter-packet gap). The Ethernet transmit port indicates LPI after the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IDLE2LPI_REG value has been counted (the transmit port has gone idle for the configured amount of time). If another packet is received for transmit during the count then the count is restarted. When the transmit port has been idle for the Idle to LPI time, the transmit port enters the LPI state and indicates LPI to the associated PHY. The LPI is indicated to the external PHY by an asserted MTXER with a MTXD[7:0] while MTXEN is deasserted (inter-packet gap). The CPPI (port 0) LPI state includes transmit and receive. The CPPI LPI state is entered when the CPPI transmit and receive have both been idle for the Idle to LPI time (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG). The Idle to LPI time value for all ports must be large relative to the switch latency to ensure that the count is not able to complete between successive packets.

Note

External PHY signaling has the following conditions:

- RGMII is a DDR interface. TXEN and TXER are the sampled values of TX_CTL at the rising and the falling TXC edges, respectively. RXDV and RXER are the sampled values of RX_CTL at the rising and the falling RXC clock edges, respectively
- In RMII mode, EEE is not supported.

When all transmit and receive ports are in the LPI state (CPSW LPI state), the EEE_CLKSTOP_ACK signal is asserted, and the LPSC is allowed to stop the module clock. When EEE_CLKSTOP_ACK is asserted, the clock may be turned on and off as desired by the host. The host is allowed to restart the clock, perform target read/write operations to the CPSW memory address space, and then turn off the clock again while EEE_CLKSTOP_ACK is asserted.

The software can remove and disable from re-entering the CPSW LPI state by restarting the module clock and then de-asserting EEE_CLKSTOP_REQ. There must be at least one rising edge of the clock before EEE_CLKSTOP_REQ is de-asserted. The module EEE_CLKSTOP_ACK output signal will be deasserted on the clock after the de-assertion of EEE_CLKSTOP_REQ. The host may queue CPPI receive packets at any time without regard to the CPSW module LPI state. The Host must deassert EEE_CLKSTOP_REQ on wakeup for a minimum of two clock periods. If EEE_CLKSTOP_REQ is deasserted for less than 5 clock periods for a wakeup event from the host to a particular Ethernet port (or visa versa), then the wakeup event will not cause the other Ethernet port port to awaken.

The external Ethernet PHY’s can also wakeup the LPSC by removing the Ethernet receive LPI indication. If the CPSW module is in Idle state with EEE_CLKSTOP_ACK asserted and the receive LPI indication is removed, the EEE_CLKSTOP_WAKEUP signal will be asynchronously asserted. On wakeup, the LPSC restarts the clock and de-assert the EEE_CLKSTOP_REQ signal. The EEE_CLKSTOP_WAKEUP signal will be synchronously deasserted with EEE_CLKSTOP_ACK. Upon the deassertion of EEE_CLKSTOP_REQ, the Ethernet ports will count the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_LPI2WAKE_REG time for each port at which time the port is available for transmit.

12.3.1.4.6.15 Ethernet Switch Latency

When CPSW is configured as a store and forward switch, the switch latency is defined as the amount of time between the end of packet reception of the received packet to the start of the output packet transmit.

The store and forward latency is shown in Table 12-163:

Table 12-163. Switch Latency

Mode	Latency
Gig (1000)	880 ns
100	1.3 μs
10	6.5 μs

12.3.1.4.6.16 MAC Emulation Control

The emulation control input (EMUSUSP) and submodule emulation control registers allow CPSW operation to be completely or partially suspended. Each Ethernet port has associated emulation control registers (CPSW3_CPSW_NU_EM_CONTROL_REG and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_EMCONTROL_REG). The submodule emulation control registers must be accessed to facilitate CPSW emulation control. The CPSW module enters the emulation suspend state if all three submodules are configured for emulation suspend and the emulation suspend input is asserted. A partial emulation suspend state is entered if one or two submodules is configured for emulation suspend and the emulation suspend input is asserted. Emulation suspend occurs at packet boundaries. The emulation control feature is implemented for compatibility with other peripherals.

Ethernet port Emulation Control

The emulation control input (TBEMUSUP) and register bits (SOFT and FREE bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_EMCONTROL_REG register) allow Ethernet port operation to be suspended. When the emulation suspend state is entered, the Ethernet port will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For receive, frames that are detected by the Ethernet port after the suspend state is entered are ignored.

Table 12-164 shows the operations of the emulation control input and register bits.

Table 12-164. Emulation Control Input

EMUSUSP	SOFT	FREE	Description
0	X	X	Normal Operation
1	0	0	Normal Operation
1	1	0	Emulation Suspend
1	X	1	Normal Operation

12.3.1.4.6.17 MAC Command IDLE

The CMD_IDLE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register allows MAC operation to be suspended. When the idle state is commanded, the MAC will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For transmission, any complete or partial frame in the TX cell FIFO will be transmitted. For receive, frames that are detected by the MAC after the suspend state is entered are ignored. No statistics will be kept for ignored frames. Commanded idle is similar in operation to emulation control and clock stop.

12.3.1.4.6.18 CPSW Network Statistics

The CPSW has a set of statistics that record events associated with frame traffic on selected switch ports. The statistics values are cleared to zero 38 clocks after the rising edge of CPSW0_RST. When one ore more port enable (Pn_STAT_EN) bits in the CPSW3_CPSW_NU_STAT_PORT_EN_REG register are set, all statistics registers are write to decrement. The value written will be subtracted from the register value with the result being stored in the register. If a value greater than the statistics value is written, then zero will be written to the register (writing 0xFFFF FFFF clears a statistics location). When all port enable bits are cleared to zero, all statistics registers are read/write (normal write direct, so writing 0x0000 0000 clears a statistics location). All write accesses must be 32-bit accesses.

The statistics interrupt (STAT_PEND0) will be issued if enabled when any statistics value is greater than or equal to 0x8000 0000. The statistics interrupt is removed by writing to decrement any statistics value greater than 0x8000 0000. The statistics are mapped into internal memory space and are 32-bits wide. All statistics rollover from 0xFFFF FFFF to 0x0000 0000.

Table 12-165 and Table 12-166 summarize network statistics.

12.3.1.4.6.18.1 Rx-only Statistics Descriptions

12.3.1.4.6.18.1.1 Good Rx Frames (Offset = 3A000h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.2 Broadcast Rx Frames (Offset = 3A004h)

All ports

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for address FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.3 Multicast Rx Frames (Offset = 3A008h)

All ports

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.4 Pause Rx Frames (Offset = 3A00Ch)

Ethernet port N where N = 1 to 2

The total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled on the port (TX_FLOW_EN = 1h).

The port could have been in either half or full-duplex mode.

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.5 Rx CRC Errors (Offset = 3A010h)

All ports

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no code/align error
- Had a CRC error

Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles, and
- Failing the Frame Check Sequence test.

12.3.1.4.6.18.1.6 Rx Align/Code Errors (Offset = 3A014h)

Ethernet port N where N = 1 to 2

The total number of frames received on the port that experienced an alignment error or code error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had either an alignment error, or a code error.

Overruns have no effect upon this statistic.

An alignment error is defined to be:

- A frame containing an odd number of nibbles

- Failing the Frame Check Sequence test if the final nibble is ignored

A code error is defined to be a frame which has been discarded because the port's MRXER pin driven with a one for at least one bit-time's duration at any point during the frame's reception.

Note

RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing Rx Align/Code Errors and Rx CRC errors.

12.3.1.4.6.18.1.7 Oversize Rx Frames (Offset = 3A018h)

All ports

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error, or code error.

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.8 Rx Jabbers (Offset = 3A01Ch)

All ports

The total number of jabber frames received on the port. A jabber frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.9 Undersize (Short) Rx Frames (Offset = 3A020h)

All ports

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 bytes
- Had no CRC error, alignment error, or code error

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.10 Rx Fragments (Offset = 3A024h)

Ethernet port N where N = 1 to 2

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long

- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half-duplex, collision-based flow control

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.11 RX IPG Error (Offset = 3A05Ch)

The total number of 10G frames received on a port that had a correct preamble but did not have at least five bytes of IDLE preceding the frame. This does not indicate if the frame with the IPG error was kept or ignored.

12.3.1.4.6.18.1.12 ALE Drop (Offset = 3A028h)

All ports

The total number of frames received on a port such that the destination address was not equal to the source address and the packet was not destined to the port it was received on, but the frame was not forwarded to any port (the PORT_MASK was zero).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was not equal to the source address
- the packet was not destined for the port it was receive on
- had a zero PORT_MASK

12.3.1.4.6.18.1.13 ALE Overrun Drop (Offset = 3A02Ch)

All ports (non cut-thru mode)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to exceeding the maximum ALE lookup rate (Port 0 should not have ALE Overrun Drops because the ingress rate is controlled to prevent it). This statistic should be zero and when non-zero indicates a system clock issue or indicates that short packets were sent with RX_CSF_EN at a rate that exceeded the maximum lookup rate.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- The port has no receive priorities enabled for cut-thru, and
- the maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.

Ethernet Ports (cut-thru mode)

The total number of received frames on a port that were dropped due to packet errors. This statistic does not count error frames that are sent to the host with a set CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[22] RX_CEF_EN or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[24] RX_CMF_EN.

- was any data or MAC control frame, and
- the port has at least one receive priority enabled for cut thru, and
- the received packet was long, mac_control, code, align, crc error, and
- was dropped on receive (not transferred to the host due to error enable bits).

12.3.1.4.6.18.1.14 Rx Octets (Offset = 3A030h)

All ports

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode

- Of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.15 Rx Bottom of FIFO Drop (Offset = 3A084h)

Ethernet port N where N = 1 to 2

The total number of frames received on a port that overran the port's receive FIFO and were dropped (bottom of receive FIFO). Port 0 (CPPI receive port) should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. An overrun frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- Was dropped on port 0 due to a lack of memory space in the receive FIFO.

Note

This statistic should be zero if proper flow control is being followed.

Host port 0

This statistic also counts frames dropped on port 0 that were 17 to 63 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 simply gives an indication that a packet was dropped. No other statistics are counted for frames shorter than 33 bytes.

12.3.1.4.6.18.1.16 Portmask Drop (Offset = 3A088h)

All ports

The total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). Port mask drop frame is defined to be:

- Any data or MAC control frame
- Any length greater than 32 bytes
- Was dropped by the ALE due to PORT_MASK=0 (was not sent to any destination port)
- Was not a long or error packet with the port in cut-thru mode
- The frame could have been dropped due to error or other counted reason, so it could be counted elsewhere also.

Note

This statistic does not count in the overall total as it includes every packet received greater than 32 bytes that had a zero PORT_MASK.

12.3.1.4.6.18.1.17 Rx Top of FIFO Drop (Offset = 3A08Ch)

All ports

The total number of frames received on a port that had a start-of-frame (SOF) overrun on any destination port egress (when attempting to load the packet from the top of the ingress port receive FIFO into any other port's transmit FIFO). If a multicast/broadcast packet is dropped by multiple destination ports then this statistic will increment by the number of ports that dropped the packet. Rx Top Of FIFO Drop is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error or code error
- had a SOF of frame overrun on another port egress.

12.3.1.4.6.18.1.18 ALE Rate Limit Drop (Offset = 3A090h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to receive rate limiting on this port or due to transmit rate limiting on any destination port (not sent to all expected destination ports if transmit rate limiting).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the receive rate was exceeded and the packet was dropped, or the transmit rate was exceeded to any destination port and the packet was dropped to one or more expected destination ports (indicates that the destinations were reduced due to rate limiting).

12.3.1.4.6.18.1.19 ALE VLAN Ingress Check Drop (Offset = 3A094h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to VLAN ingress check failure.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the VLAN ID ingress check failed (the receive port was not in the group)
- The address lookup did not return a match with the SUPER bit set.

12.3.1.4.6.18.1.19.1 ALE DA=SA Drop (Offset = 3A098h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to destination address equal to source address.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was equal to the source address
- the source address was not an entry in the table.

12.3.1.4.6.18.1.19.2 Block Address Drop (Offset = 3A09Ch)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to the destination or source address being blocked.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- the source or destination address matched a table entry with the block bit set.

12.3.1.4.6.18.1.19.3 ALE Secure Drop (Offset = 3A0A0h)

The total number of frames received on a port that were dropped (zero port_mask) due to a secure violation (the source address is owned by a different receive port).

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- the source address is an entry in the table with the SECURE bit set and a port number for a different receive port.

12.3.1.4.6.18.1.19.4 ALE Authentication Drop (Offset = 3A0A4h)

The total number of frames received on a port that were dropped (zero port_mask) due to authentication failure.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- CPSW3_CPSW_NU_ALE_ALE_CONTROL[1] ENABLE_AUTH_MODE is set to 1h, and
- the source address is not equal to the destination address, and
- the source address is not a table entry, and
- the destination address is not a table entry with the SUPER bit set.

12.3.1.4.6.18.1.19.5 ALE Unknown Unicast (Offset = 3A0A8h)

All ports

The total number of frames received on a port that had a unicast destination address with an unknown source address.

- was any data frame with a unicast destination address
- the source address was not a table entry
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

Note: The ALE Unknown Unicast Bytecount statistic is the number of bytes contained in the ALE Unknown Unicast frames.

12.3.1.4.6.18.1.19.6 ALE Unknown Unicast Bytecount (Offset = 3A0ACh)

The total number of bytes received on a port that had a unicast destination address with an unknown source address.

12.3.1.4.6.18.1.19.7 ALE Unknown Multicast (Offset = 3A0B0h)

The total number of frames received on a port that had a multicast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Multicast Bytecount statistic is the number of bytes contained in the ALE Unknown Multicast frames.

12.3.1.4.6.18.1.19.8 ALE Unknown Multicast Bytecount (Offset = 3A0B4h)

The total number of bytes received on a port that had a multicast destination address with an unknown source address.

12.3.1.4.6.18.1.19.9 ALE Unknown Broadcast (Offset = 3A0B8h)

The total number of frames received on a port that had a broadcast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Broadcast Bytecount statististic is the number of bytes contained in the ALE Unknown Broadcast frames.

12.3.1.4.6.18.1.19.10 ALE Unknown Broadcast Bytecount (Offset = 3A0BCh)

The total number of bytes received on a port that had a broadcast destination address with an unknown source address.

12.3.1.4.6.18.1.19.11 ALE Policer/Classifier Match (Offset = 3A0C0h)

All ports

The total number of frames received on a port that matched a policer. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.2 ALE Policer Match Red (Offset = 3A0C4h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.3 ALE Policer Match Yellow (Offset = 3A0C8h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.4 IET Receive Assembly Error (Offset = 3A140h)

The total number of premptable received frames with IET assembly errors.

- any frame received
- was any size, and
- was a non-initial fragment that mismatched the frame count or fragment count (went to the assembly error state in the IET receive state machine)

12.3.1.4.6.18.5 IET Receive Assembly OK (Offset = 3A144h)

The total number of correctly received and re-assembled premptable frames.

- any premptable frame received
- was any size, and
- was correctly received and re-assembled without error

12.3.1.4.6.18.6 IET Receive SMD Error (Offset = 3A148h)

The total number of received frames rejected due to an unknown SMD value or received frames rejected with an SMD-C when no frame is in progress.

- any frame received
- was any size, and
- was rejected because of an unknown SMD value or SMD-C with no frame in progress.

Note: If IET_ENABLE is not set, this statistic counts any received frame with any non express SMD.

12.3.1.4.6.18.7 IET Receive Merge Fragment Count (Offset = 3A14Ch)

The total number of received non-initial fragments that did not have an assembly error. The IET stat CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_k is derived by adding the Receive Assembly Error count to this value.

- any frame received
- was any size, and
- was a non-initial fragment that did not contain an assembly error

12.3.1.4.6.18.8 Rx Cut Thru with No Delay

The total number of frames received on the port and subsequently sent cut-thru to all internal destination port FIFOs with no delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports without delay.

12.3.1.4.6.18.9 Rx Cut Thru with Delay

The total number of frames received on the port and subsequently sent cut-thru to all destination ports with some amount of delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports with some amount of delay.

12.3.1.4.6.18.10 Rx Cut Thru Store-and-Forward

The total number of frames received on the port were attempted to be sent cut-thru to all destination ports but were held off due to configuration or traffic conditions. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was attempted to be sent cut-thru by the receive port to all destination ports but was sent store-and-forward.

12.3.1.4.6.18.11 Tx-only Statistics Descriptions

The maximum and minimum transmit frame size is software controllable.

12.3.1.4.6.18.11.1 Good Tx Frames (Offset = 3A034h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

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Note

A nonzero CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_k value should be subtracted from this value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.3.1.4.6.18.11.2 Broadcast Tx Frames (Offset = 3A038h)

All ports

The total number of good broadcast frames transmitted on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.3.1.4.6.18.11.3 Multicast Tx Frames (Offset = 3A03Ch)

All ports

The total number of good multicast frames transmitted on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.3.1.4.6.18.11.4 Pause Tx Frames (Offset = 3A040h)

Ethernet port N where N = 1 to 2

This statistic indicates the number of IEEE 802.3X pause frames transmitted by the port.

Pause frames cannot contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect upon the statistic. Pause frames sent by software will not be included in this count.

Since pause frames are only transmitted in full duplex, carrier loss and collisions have no effect upon this statistic.

Transmitted pause frames are always 64-byte multicast frames so will appear in the *Tx Multicast Frames* and *64octet Frames* statistics.

12.3.1.4.6.18.11.5 Deferred Tx Frames (Offset = 3A044h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that first experienced deferment. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.6 Collisions (Offset = 3A048h)

Ethernet port N where N = 1 to 2

This statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances.

1. When a transmit data or MAC control frame:
    - Was destined for any unicast, broadcast or multicast address
    - Was any size
    - Had no carrier loss and no underrun

  - Experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions)

    CRC errors have no effect upon this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.

12.3.1.4.6.18.11.7 Single Collision Tx Frames (Offset = 3A04Ch)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced exactly one collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.8 Multiple Collision Tx Frames (Offset = 3A050h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced multiple collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.9 Excessive Collisions (Offset = 3A054h)

Ethernet port N where N = 1 to 2

The total number of frames for which transmission was abandoned due to excessive collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.10 Late Collisions (Offset = 3A058h)

Ethernet port N where N = 1 to 2

The total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted. The *Late Collisions* statistic dominates over the single-, multiple- , and excessive- collision statistics. If a late collision occurs, the frame will not be counted in any of these other three statistics.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.11 Carrier Sense Errors (Offset = 3A060h)

Ethernet port N where N = 1 to 2

The total number of frames on the port that experienced carrier loss. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don't care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.12 Tx Octets (Offset = 3A064h)

All ports

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

12.3.1.4.6.18.11.13 Transmit Priority 0-7 (Offset = 3A180h to 3A1A8h)

The total number of frames transmitted on the port from transmit FIFO priority 0-7. Collision retries do not affect this statistic. Pause frames do not affect this statistic.

- Any frame transmitted from priority 0-7, and
- Was less than or equal to CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG
- Collision retries are not counted in this statistic.
- Pause frames are not counted in this statistic.
- Carrier sense errors do not affect this statistic.

Note: The Transmit Priority 0-7 Bytecount statistic is the number of bytes contained in the frames of the Transmit Priority 0-7 statistic.

12.3.1.4.6.18.11.14 Transmit Priority 0-7 Drop (Offset = 3A1C0h to 3A1E8)

The total number of transmit frames on the port that overran the transmit FIFO priority 0-7 and were dropped. This count includes frames dropped due to CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG.

- Any frame destined to be transmitted from priority 0-7, and
- Was any size, and
- Was dropped due to priority 0-7 FIFO overrun (Start of packet overrun).
- Was dropped due to frame size larger than CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG.

Note: The Transmit Priority 0-7 Drop Bytecount statististic is the number of bytes contained in the frames of the Transmit Priority 0-7 Drop statistic.

12.3.1.4.6.18.11.15 Tx Memory Protect Errors (Offset = 3A17Ch)

All ports

The total number of transmit frames on the port that had a memory protect CRC error on egress:

- Any frame destined to be transmitted,
- Was any size
- Had a memory protect CRC error on egress.

Note

1. Frames to the host with memory protect errors are dropped via TXST_DROP. Ethernet frames will have at least one byte of the generated port type CRC inverted on egress.
2. This statistic is 8-bits wide only and will not rollover but will limit at 0xFF.
3. A non-zero value in this statistic will issue a STAT_PEND0 interrupt for the associated port.

12.3.1.4.6.18.11.16 IET Transmit Merge Hold Count (Offset = 3A150h)

The total number of premptable frames that were prempted and reassembled by the assertion of MAC_HOLD in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register or were prempted by Enhanced Scheduled Traffic (EST). The IET statistic can be derived and maintained by software.

- Any frame destined to be transmitted on the premptable port, and
- was any size, and
- was prempted by the assertion of MAC_HOLD.
- was prempted by Enhanced Scheduled Traffic (EST).

12.3.1.4.6.18.11.17 IET Transmit Merge Fragment Count (Offset = 3A14Ch)

The total number of non-initial premptable transmit fragments on premptable transmit.

- Any frame destined to be transmitted on the premptable port, and
- Was any size, and
- was a non-initial fragment.

12.3.1.4.6.18.11.18 Tx CRC Errors

The total number of frames transmitted on the port with a CRC error. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size, and
- was sent cut-thru by the receive port and was received with a CRC error, or
- was a transmitted frame that also had a memory protect error (counted also in CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_k).

Note

For port0 this statistics location (CPSW_STAT0_TXDROP) counts the number of drops to the host due to a memory protect error, or due to a cut-thru packet having an error on reception but was forwarded with the error. The Ethernet port receive error could be long, CRC, jabber, or code. For Ethernet ports, the receive error could be the same but the packet is transmitted with at least one byte of the actual outgoing packet CRC inverted to indicate the error.

Note

A nonzero CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_k value should be subtracted from the CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_k value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.3.1.4.6.18.11.19 Tx Cut Thru

The total number of cut-thru frames transmitted on the port with or without delay. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted cut-thru with or without delay.

12.3.1.4.6.18.11.20 Tx Cut Thru Store-and-Forward

The total number of cut-thru frames transmitted store and forward. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted store-and-forward due to traffic congestion.

12.3.1.4.6.18.12 Rx- and Tx (Shared) Statistics Descriptions

12.3.1.4.6.18.12.1 Rx + Tx 64 Octet Frames (Offset = 3A068h)

All ports

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.2 Rx + Tx 65–127 Octet Frames (Offset = 3A06Ch)

All ports

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.3 Rx + Tx 128–255 Octet Frames (Offset = 3A070h)

All ports

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.4 Rx + Tx 256–511 Octet Frames (Offset = 3A074h)

All ports

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.5 Rx + Tx 512–1023 Octet Frames (Offset = 3A078h)

All ports

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.6 Rx + Tx 1024_Up Octet Frames (Offset = 3A07Ch)

All ports

The total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 1024 to RX_MAXLEN bytes long on receive, or any size on transmit

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.7 Net Octets (Offset = 3A080h)

All ports

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier-loss was experienced
- Every byte transmitted before each collision was experienced, (that is, multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic.

The objective of this statistic is to give a reasonable indication of Ethernet utilization.

12.3.1.4.6.18.13

Table 12-165. Rx Statistics Summary

<table>
<tr><th rowspan="3">Rx Statistic</th><th rowspan="3">Frame/Oct</th><th rowspan="3">Rx/Rx+Tx</th><th colspan="5">Frame Type</th><th colspan="8">Frame Size (bytes)</th><th colspan="5">Event</th></tr>
<tr><th colspan="2">MAC control</th><th colspan="3">Data(5)</th><th rowspan="2"><64</th><th rowspan="2">64</th><th rowspan="2">65-127</th><th rowspan="2">128-255</th><th rowspan="2">256-511</th><th rowspan="2">512-1023</th><th rowspan="2">1024-rx_max len</th><th rowspan="2">>rx_max len</th><th rowspan="2">Flow Coll.(8)</th><th rowspan="2">CRC Error</th><th rowspan="2">Align/Code</th><th rowspan="2">Overrun</th><th rowspan="2">Addr. Disc.</th></tr>
<tr><th>Pause frame</th><th>Non-pause(4)</th><th>Multicast</th><th>Broadcast</th><th>Unicast</th></tr>
<tr><td>Good Rx Frames</td><td>F</td><td>Rx</td><td>(y|(1)</td><td>y|</td><td>y|</td><td>y|</td><td>y)</td><td>n</td><td>(y|</td><td>y|</td><td>y|</td><td>y|</td><td>y|</td><td>y)</td><td>n</td><td>-(2)</td><td>n</td><td>n</td><td>-</td><td>n</td></tr>
<tr><td>Broadcast Rx Frames</td><td>F</td><td>Rx</td><td>(%|(6)</td><td>%|</td><td>n</td><td>y)</td><td>n</td><td>n</td><td>(y|</td><td>y|</td><td>y|</td><td>y|</td><td>y|</td><td>y)</td><td>n</td><td>-</td><td>n</td><td>n</td><td>-</td><td>n</td></tr>
<tr><td>Multicast Rx Frames</td><td>F</td><td>Rx</td><td>(%|</td><td>%|</td><td>y)</td><td>n</td><td>n</td><td>n</td><td>(y|</td><td>y|</td><td>y|</td><td>y|</td><td>y|</td><td>y)</td><td>n</td><td>-</td><td>n</td><td>n</td><td>-</td><td>n</td></tr>
<tr><td>Pause Rx Frames</td><td>F</td><td>Rx</td><td>y</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>(y|</td><td>y|</td><td>y|</td><td>y|</td><td>y|</td><td>y)</td><td>n</td><td>-</td><td>n</td><td>n</td><td>-</td><td>-</td></tr>
</table>

Table 12-165. Rx Statistics Summary (continued)

Rx Statistic	Frame/ Oct	Rx/ Rx+ Tx	Frame Type					Frame Size (bytes)								Event				
			MAC control		Data(5)															
			Pause frame	Non-pause(4)	Multicast	Broadcast	Unicast	<64	64	65-127	128-255	256-511	512-1023	1024-rx_max len	>rx_max len	Flow Coll.(8)	CRC Error	Align/ Code	Overrun	Addr. Disc.
Rx CRC Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	y	n	-	n
Rx Align/Code Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	-	y	-	n
Oversized Rx Frames	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	n	n	-	n
Rx Jabbers	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	(y|	y)	-	n
Undersized Rx Frames	F	Rx	n	n	(y|	y|	y)	y	n	n	n	n	n	n	n	-	n	n	-	n
Rx Fragments	F	Rx	n	n	(y|	y|	y)	y^(7)	n	n	n	n	n	n	n	-	(y|	y)	-	-
Rx Overruns(9)	F	Rx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	y	n
64octet Frames	F	Rx+ Tx(3)	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	n	-	-	-	-	n
65-127octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	n	-	-	-	-	n
128-255octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	n	-	-	-	-	n
256-511octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	n	-	-	-	-	n
512-1023octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	n	n	-	-	-	-	n
1024-UPoctet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	y	n	-	-	-	-	n
Rx Octets	O	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Net Octets	O	Rx+ Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning "OR" is indicated. Parentheses are significant.

(2) "-" indicates conditions which are ignored in the formations of the statistic.

(3) Statistics marked "Rx+Tx" are formed by summing the Rx and Tx statistics, each of which is formed independently.

(4) The non-pause column refers to all MAC control frames (for example, frames with length/type=88.08) with opcodes other than 0x0001. The pauseframe column refers to MAC frames with the opcode=0x0001.

(5) The multicast, broadcast and unicast columns in the table refer to non-MAC Control/non-pause frames (i.e. data frames).

(6) "%" If either a MAC control frame or pause frame has a multicast or broadcast destination address then the appropriate statistics will be updated.

(7) "y^" Frame fragments are not counted if less than 8 bytes.

(8) Flow coll. are half-duplex collisions forced by the MAC to achieve flow-control. A collision will be forced during the first 8 bytes so should not show in frame fragments. Some of the '-'s in this column might in reality be 'n's.

(9) The rx_overruns stat is for RX_MOF_OVERRUNS and RX_SOF_OVERRUNS added together.

Table 12-166. Tx Statistics Summary

Tx Statistic(9)	Frame/Oct	Tx/Rx+Tx	Frame Type					Frame Size (bytes)							Event									
			MAC control(4)		Data			64	65-127	128-255	256-511	512-1023	1024-1535	>1535	CRC Error	Collision Type					No Carrier	Queued	Deferred	Underrun
			Pause-MAC	Any-CPU	Multicast	Broadcast	Unicast									Flow(8)	1	2-15	16	Late				
Good Tx Frames	F	Tx	(y|(1)	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-(2)	-	-	-	n	n	n	-	-	n
Broadcast Tx Frames	F	Tx	n	(%|(5)	n	y)	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Multicast Tx Frames	F	Tx	(y|	%|	y)	n	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Pause Tx Frames	F	Tx	y	n	n	n	n	y	n	n	n	n	n	n	-	-	-	-	-	-	-	-	-	-
Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	(+(6)	+	+	+	+)	n	-	-	-
Single Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	y	n	n	n	n	-	-	-
Multiple Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	y	n	n	n	-	-	-
Excessive Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	y	n	n	-	-	-
Late Collisions	F	Tx	n	(y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	-	-	-	-	-	y	-	-	-	-
Deferred Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	n	n	n	-	y	n
Carrier Sense Errors	F	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	-	-	y	-	-	-
64octet Frames	F	Rx+Tx(3)	(y|	y|	y|	y|	y)	y	n	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
65-127octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
128-255octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	-	-	-	-	n	n	n	-	-	-
256-511octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	-	-	-	-	n	n	n	-	-	-
512-1023octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	-	-	-	-	n	n	n	-	-	-
1024-UPoctet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	y	-	-	-	-	n	n	n	-	-	-
Tx Octets	O	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Net Octets	O	Rx+Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	$(7)	$	$	$	$	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning “OR” is indicated. Parentheses are significant.

(2) “-“ indicates conditions which are ignored in the formations of the statistic.

(3) Statistics marked “Rx+Tx” are formed by summing the Rx and Tx statistics, each of which is formed independently.

(4) Pause (MAC) frames are issued in the MAC as perfect (no CRC error) 64 byte frames in full duplex only, so they cannot collide.
(5) “%” If a CPU sourced MAC control frame has a multicast or broadcast destination address then the appropriate statistics will be updated.
(6) “+” indicates collisions which are “summed” (i.e. every collision is counted in the Collisions statistic). Jam sequences used for halfduplex flow control are also counted.
(7) “$” Every byte written on the wire during each retry attempt is also counted in addition to frames which experience no collisions or carrier loss.
(8) The flow collision type is for half-duplex collisions forced by the MAC to achieve flow control. Some of the ‘-‘s in this column might in reality be ‘n’s. To prevent double-counting, Net Octets are unaffected by the jam sequence – the ‘received’ bytes, however, are counted. (See Table 12-165.)
(9) When the transmit Tx FIFO is drained due to the MAC being disabled or link being lost, then the frames being purged will not appear in the Tx statistics.

12.3.1.4.7 Common Platform Time Sync (CPTS)

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations. It enables compliance with the IEEE 1588-2008 standard for a precision clock synchronization protocol.

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports up to 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports a configurable number of timestamp Generator bit outputs (CPTS_GENFn).
- Supports Ethernet Enhanced Scheduled Traffic Operations (CPTS_ESTFn).
- 32-bit and 64-bit timestamp modes with PPM and nudge adjustment.

12.3.1.4.7.1 CPSW0 CPTS Integration

This section describes CPTS module integration in the CPSW0 module, including information about clocks, resets, and hardware requests.

Figure 12-136 shows CPTS integration in the device CPSW0 module.

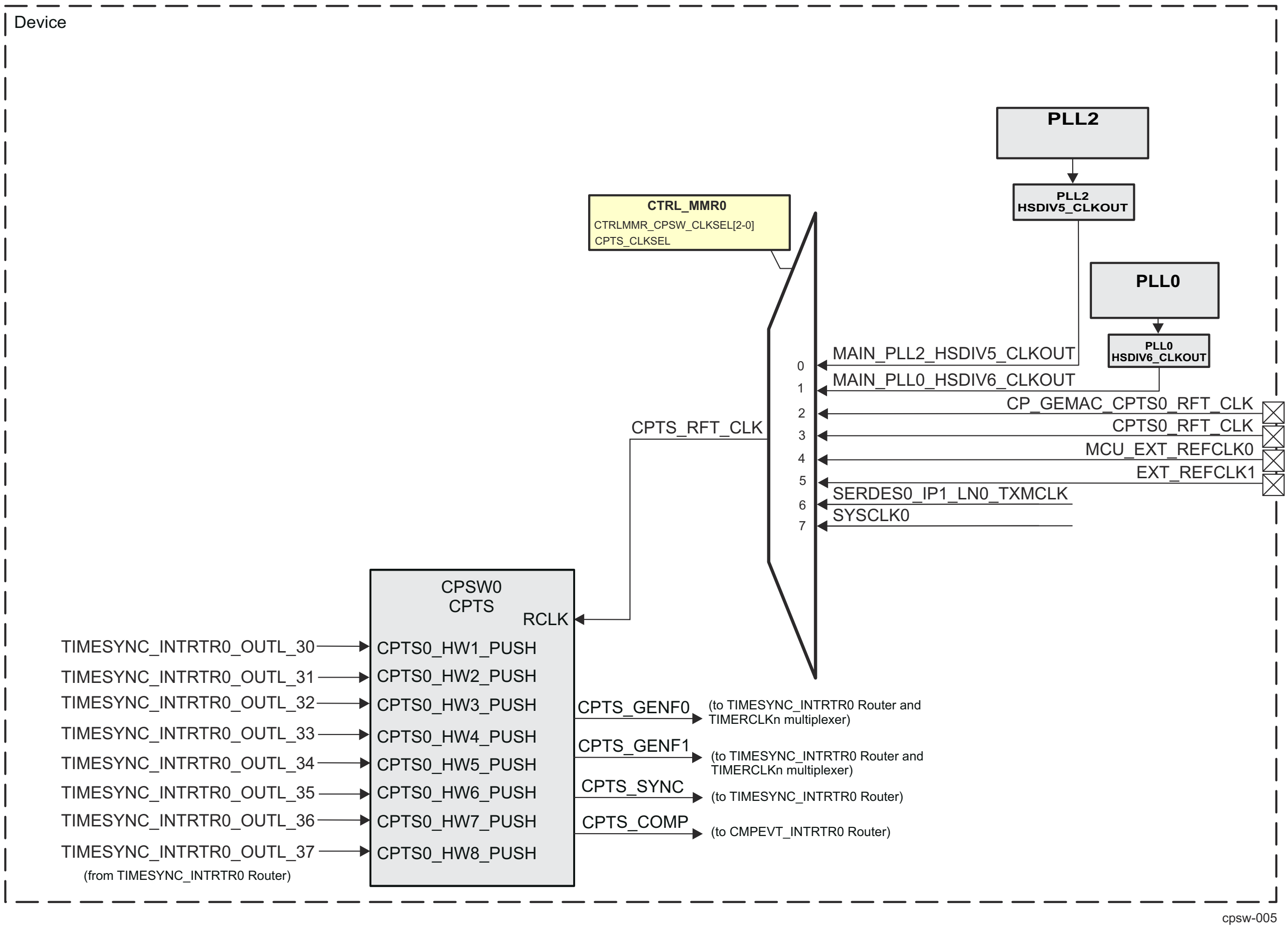

Figure 12-136. CPSW0 CPTS Integration

CPTS IEEE 1588 clock (RCLK) is selected through the CPTS_CLKSEL bit.

Note

For more information about CPTS clocks and resets, see *CPWS0 Clocks* in *CPSW0 Integration*.

12.3.1.4.7.2 CPTS Architecture

Figure 12-137 shows the architecture of the CPTS module inside the CPSW Ethernet Subsystem. Time stamp values for every packet transmitted or received on external port of the CPSW are recorded. At the same time, each packet is decoded to determine if it is a valid time sync event. If so, an event is loaded into the Event FIFO for processing containing the recorded time stamp value when the packet was transmitted or received.

In addition, both hardware (HWn_TS_PUSH) and software (TS_PUSH) can be used to read the current time stamp value though the Event FIFO. The reference clock used for the time stamp (CPTS_RFT_CLK) can be derived from several sources.

Figure 12-137. CPTS Block Diagram

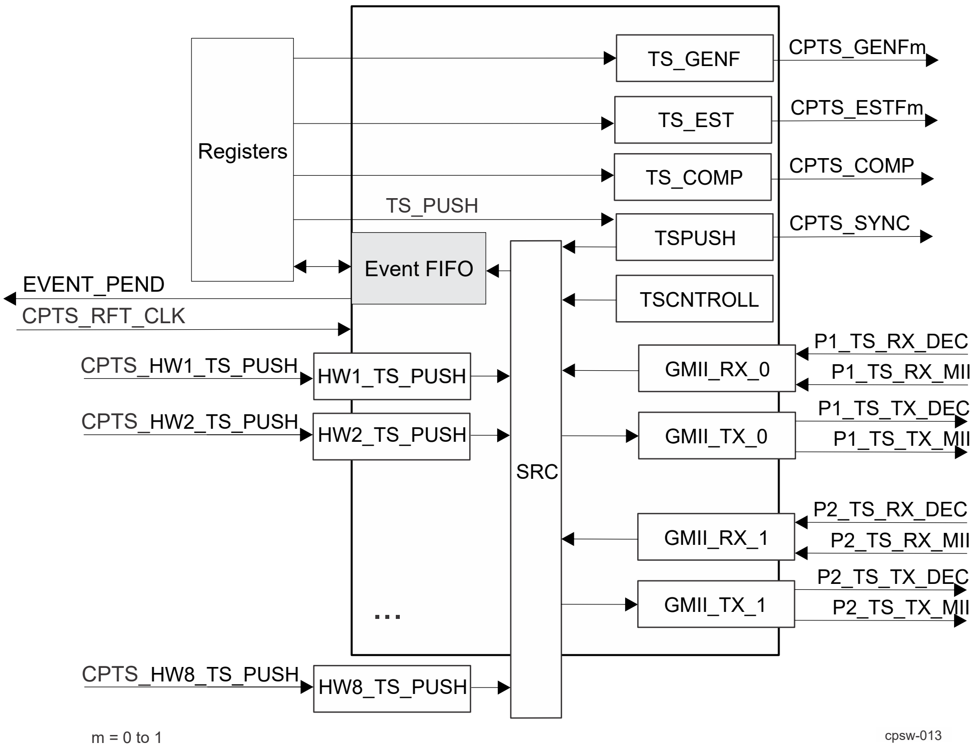

Note

See Section 12.3.1.4.7.1 , *CPSW0 CPTS Integration* for CPTS integration in the device CPSW0 module.

12.3.1.4.7.3 CPTS Initialization

The CPTS module should be configured as follows:

1. Reset the CPTS module.
2. Write the CPTS_CLKSEL value with the desired reference clock selection. This value is allowed to be written only when the CPTS_EN bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register is cleared to zero.
3. Set the CPTS_EN bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register.
4. If using interrupts and not polling, enable the interrupt by setting the TS_PEND_EN bit in the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.

12.3.1.4.7.4 32-bit Time Stamp Value

The time stamp value is a 32-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

If more than 32-bits of time stamp are required by the application, the host software must maintain the necessary number of upper bits. The upper time stamp value should be incremented by the host when the rollover event is detected.

For test purposes, the time stamp can be written via the time stamp load function (CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG / CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG and CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG registers).

12.3.1.4.7.5 64-bit Time Stamp Value

The time stamp value is a 64-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

64-bit mode is selected when CPSW3_CPSW_NU_CPTS_CONTROL_REG[5] MODE bit set to 1h.

For test purposes, the time stamp value can be written via the time stamp load function (CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG, CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG, and CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG registers). The CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG feature is included to allow 1ns timestamp operations with an CPTS_RFT_CLK rate less than 1Ghz. Table 12-167 shows the CPTS_RFT_CLK and CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG values for 1ns operations.

Table 12-167. ADD_VAL feature

CPTS_RFT_CLK (MHz)	CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL
1 GHz	0
500 MHz	1
333.33 MHz	2
250 MHz	3
200 MHz	4
166.66 MHz	5
142.85714 MHz	6
125 MHz	7

12.3.1.4.7.6 64-Bit Timestamp Nudge

The 64-bit TIME_STAMP value can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL bit field value which is a two's complement value. A value of FFh will subtract 1 clock cycle from the next incremented 64-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW3_CPSW_NU_CPTS_EVENT_3_REG[31-0] TIME_STAMP value). A nudge value of 1h will add 1 clock cycle to the next incremented TIME_STAMP[63-0] value. For example, if the current TIME_STAMP value is F06h, and CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL = 3h, the next incremented timestamp value would be F0Ah without a nudge and F0Ah +/- [7-0] TS_NUDGE_VAL with a nudge. The [7-0] TS_NUDGE_VAL value is cleared to zero when the nudge has occurred.

12.3.1.4.7.7 64-bit Timestamp PPM

The 64-bit TIME_STAMP can be adjusted by parts per million or by parts per hour. Writing a non-zero value to the CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL (Time stamp PPM Low value) and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL (Time stamp PPM High value) enables PPM operations. The adjustment is up or down depending on the [7] TS_PPM_DIR bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register. The TIME_STAMP value is increased by the PPM value when [7] TS_PPM_DIR bit is cleared. The TIME_STAMP value is decreased by the PPM value when [7] TS_PPM_DIR bit is set.

Parts Per Million example:
To adjust for 100 parts per million the configured value for TS_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured value for TS_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.3.1.4.7.8 Event FIFO

All time sync events are pushed onto the Event FIFO. There are 32 locations in the event FIFO with no overrun indication supported. Software must service the event FIFO in a timely manner to prevent FIFO overrun.

12.3.1.4.7.9 Timestamp Compare Output

CPTS features one Time Stamp Compare (CPTS_COMP) output. The CPTS_COMP function is a software oriented feature that is intended to be replaced going forward by the hardware oriented GENF function. CPTS_COMP is not compatible with timepstamp PPM or a non-zero CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value.

12.3.1.4.7.9.1 Non-Toggle Mode: 32-bit

The CPTS_COMP output is asserted for CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH periods when the CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP value (lowe 32-bits) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and the length value is non-zero. The CPTS_COMP rising edge occurs three CPTS_RFT_CLK clock periods after the values compare. A timestamp compare event is pushed into the event FIFO when CPTS_COMP is asserted. The polarity of the CPTS_COMP output is determined by the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit. The output is asserted low when the polarity bit is 0h.

12.3.1.4.7.9.2 Non-Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIME_STAMP are used (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) are used.

12.3.1.4.7.9.3 Toggle Mode: 32-bit

The CPTS_COMP output is asserted (CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH) for CPTS_RFT_CLK clock periods when the TIME_STAMP[31:0] value compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG and the length value is non-zero. The CPTS_COMP toggles thereafter on CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH for CPTS_RFT_CLK periods. The length high or low can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE bit field value which is a two's complement value. A value of FFh will subtract one CPTS_RFT_CLK period from the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH value. A value of 0x01h will add one CPTS_RFT_CLK period to the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value. Only a single high or low time is adjusted (nudged) and the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred. The CPTS_COMP output is asserted low when the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is 0h. No compare events and no CPTS_EVNT interrupts are generated in toggle mode. The CPSW3_CPSW_NU_CPTS_CONTROL_REG[6] TS_COMP_TOG bit must be set for toggle mode (value 1h). Note this bit must be set before writing a non-zero value to CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register.

12.3.1.4.7.9.4 Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIMESTAMP are used (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) are used.

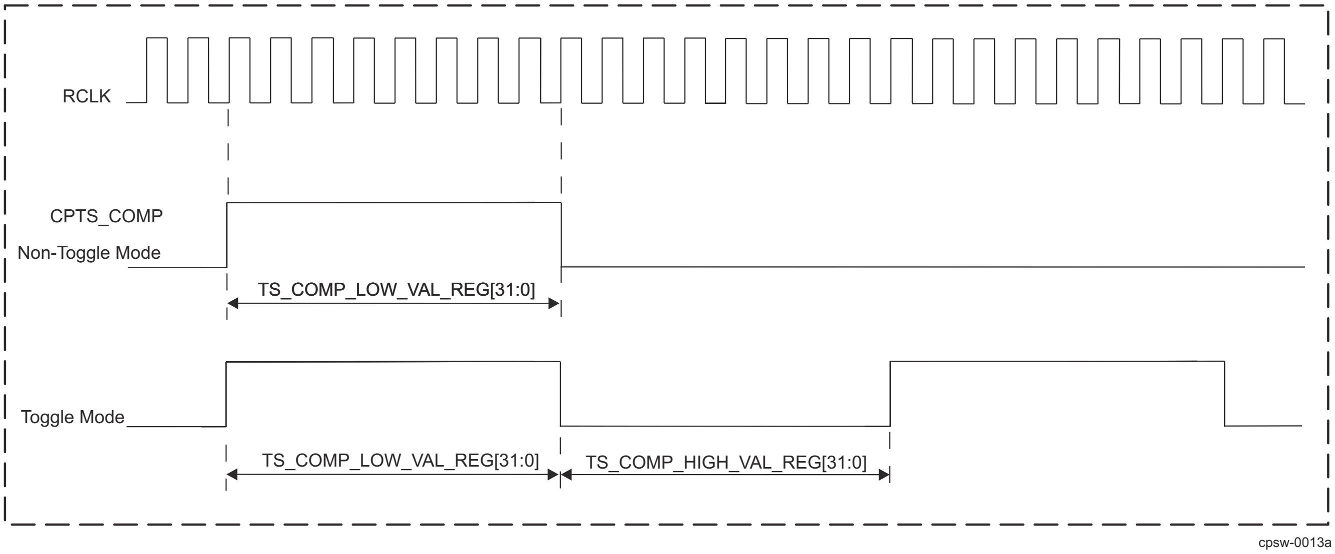

Figure 12-138. CPTS_COMP Output in Toggle and Non-Toggle Mode

12.3.1.4.7.10 Timestamp Sync Output

The CPTS_SYNC output is a selected bit of the [31-0]TIME_STAMP counter value. One of bits 17-31 can be selected in CPSW3_CPSW_NU_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL. The CPTS_SYNC output is disabled when CPSW3_CPSW_NU_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL is zero.

If the selected counter bit is 1 at the time when TS_SYNC_SEL value is written then a rising edge will not occur on the CPTS_SYNC output. A rising edge will occur on the CPTS_SYNC output upon the next transition to 1 of the selected counter bit. The TS_SYNC_SEL value must be written to zero before changing to a different non-zero value. No events are generated due to the CPTS_SYNC operation. The CPTS_SYNC output is two CPTS_RFT_CLK periods after the actual count value.

12.3.1.4.7.11 Timestamp GENFn Output

The CPTS_GENFn outputs have a programmable cycle (frequency) with a PPM feature and software nudge feature. The CPTS_GENFn output cycle is CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods (which is different than CPTS_COMP operation). Figure 12-139 represents the CPTS_GENFn output signal.

The CPTS_GENFn output cycle is CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods beginning when the 64-bit TIME_STAMP value compares with the 64-bit GENFn_COMP value (CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_L and CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_L registers) and the length value is non-zero. The CPTS_GENFn output cycle repeats thereafter every CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods. The upper 32-bit word should be written first for 64-bit values. The length should be zero while the comparison value and other configuration parameters are being configured. The length should be written non-zero to enable operations last. The first cycle after comparison is active high when the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is low. No compare events and no CPTS_EVNT interrupts are generated.

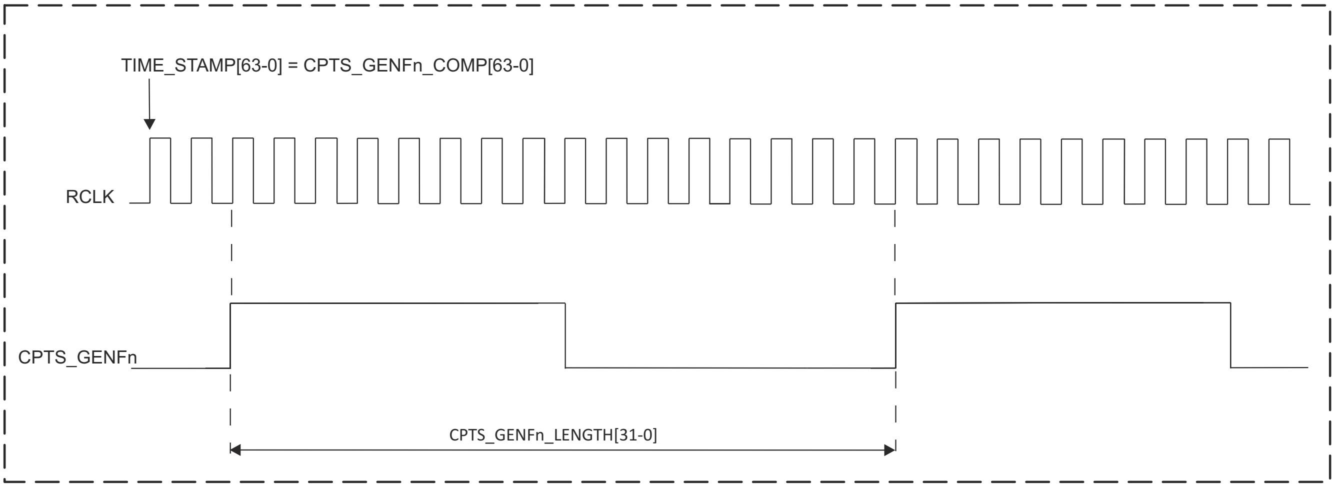

Figure 12-139. CPTS_GENFn Output Signal Diagram

12.3.1.4.7.11.1 GENFn Nudge

The cycle length can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE register value which is a two's complement value. A value of FFh will subtract 1 CPTS_RFT_CLK from theCPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] value. A value of 1h will add 1 CPTS_RFT_CLK to theCPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] value. The CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred.

12.3.1.4.7.11.2 GENFn PPM

The CPTS_GENFn output cycle can be adjusted by parts per million or by parts per hour. Writing a non-zero value to CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L/ CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L enables PPM operations. The PPM counter continually loads and decrements to zero and then loads again. A single CPTS_RFT_CLK adjustment is made when the PPM counter decrements to zero. The adjustment is up or down depending on the CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG[0] PPM_DIR bit. When PPM_DIR bit is set a single CPTS_RFT_CLK time is subtracted from the generate function counter which has the effect of increasing the generate function frequency by the PPM amount. When PPM_DIR bit is cleared a single CPTS_RFT_CLK time is added to the generate function counter which has the effect of decreasing the generate function frequency by the PPM amount.

Parts Per Million example:
To adjust for 100 parts per million the configured value for
GENF_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L and
CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured
value for GENF_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L and
CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.3.1.4.7.12 Timestamp ESTFn

Each Ethernet port has a dedicated ESTFn generator which operates identically to the GENFn function.

12.3.1.4.7.13 Time Sync Events

Time Sync events are 96-bit values that are pushed onto the event FIFO and read by software in 32-bit reads. Four 32-bit registers, CPSW3_CPSW_NU_CPTS_EVENT_0_REG through CPSW3_CPSW_NU_CPTS_EVENT_3_REG hold the data of a time sync event. There are eight types of sync events:

- Time Stamp Push Event
- Time Stamp Counter Rollover Event (32-bit mode only)
- Time Stamp Counter Half-rollover Event (32-bit mode only)
- Hardware Time Stamp Push Event
- Ethernet Receive Event
- Ethernet Transmit Event
- Time Stamp Compare Event
- Host Transmit Event

12.3.1.4.7.13.1 Time Stamp Push Event

Software can obtain the current time stamp value (at the time of the write) by initiating a time stamp push event. The push event is initiated by setting the [0]TS_PUSH bit of the CPSW3_CPSW_NU_CPTS_TS_PUSH_REG register. The time stamp value is returned in the event, along with a time stamp push event code. The upper 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_3_REG register) of the timestamp are zero in 32-bit mode.

12.3.1.4.7.13.2 Time Stamp Counter Rollover Event (32-bit mode only)

The CPTS module contains a 32-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG). The counter upper bits are maintained by host software. The rollover event indicates to software that the time stamp counter has rolled over from 0xFFFF FFFF to 0x0000 0000 and the software-maintained upper count value should be incremented. This event occurs only in 32-bit mode.

12.3.1.4.7.13.3 Time Stamp Counter Half-rollover Event (32-bit mode only)

The CPTS includes a time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP) has incremented from 0x7FFF FFFF to 0x8000 0000. The half-rollover event is included to enable software to correct a misaligned event condition. This event occurs only in 32-bit mode.

The half-rollover event is included to enable software to determine the correct time for each event that contains a valid time stamp value, such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), the rollover event could possibly be loaded into the event FIFO before the Ethernet event, even though the Ethernet event time was actually taken before the rollover. Figure 12-140 shows a misalignment condition. This misaligned event condition arises because an Ethernet event time stamp occurs at the beginning of a packet and time passes before the packet is determined to be a valid synchronization packet. The misaligned event condition occurs if the rollover occurs in the middle, after the packet time stamp has been taken, but before the packet has been determined to be a valid time sync packet.

Host software must detect and correct for misaligned event conditions. For every event time stamp after a rollover and before a half-rollover, software must examine the time stamp most significant bit. If bit 31 of the time stamp value is low (0x0000 0000 through 0x7FFF FFFF), then the event time stamp was taken after the rollover and no correction is required. If the value is high (0x8000 0000 through 0xFFFF FFFF), the time stamp value was taken before the rollover and a misalignment is detected. The misaligned case indicates to software that it must subtract one from the upper count value stored in software to calculate the correct time for the misaligned event. The misaligned event occurs only on the rollover boundary and not on the half-rollover boundary. Software only needs to check for misalignment from a rollover event to a half-rollover event.

When a rollover occurs, software increments the software time stamp upper value. The misaligned case indicates to software that the misaligned event time stamp has a valid upper value that is pre-increment, so one must be subtracted from the upper value to allow software to calculate the correct time for the misaligned event.

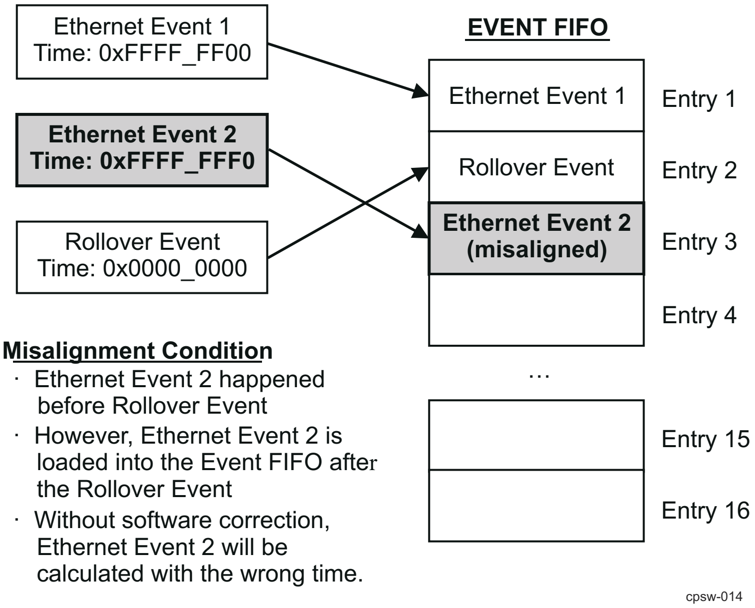

Figure 12-140. Event FIFO Misalignment Condition

12.3.1.4.7.13.4 Hardware Time Stamp Push Event

There are four hardware time stamp inputs (CPTS_HW[1:4]_TS_PUSH events) that can cause hardware time stamp push events to be loaded into the Event FIFO. Each time stamp input is mapped in the device as shown in *CPTS Integration*. The event is loaded into the event FIFO on the rising edge of the timer, and the PORT_NUMBER field in the CPSW3_CPSW_NU_CPTS_EVENT_1_REG register indicates the hardware push input that caused the event (encoded).

The hardware time stamp inputs are asynchronous and are low frequency signals. The CPTS logic synchronizes and performs a rising edge detect on the incoming asynchronous input.

Each hardware time stamp input must be asserted for at least 10 periods of the selected CPTS_RFT_CLK clock. Each input can be enabled or disabled by setting the respective bits in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register.

Hardware time stamps are intended to be an extremely low frequency signals, such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that there is no overrun, or events will be lost.

12.3.1.4.7.13.5 Ethernet Port Events

Packets transmitted or received on each Ethernet port can generate Ethernet Transmit Events or Ethernet Receive Events, respectively. The CPTS hardware will decode each packet to determine if it is a valid CPTS time sync event.

According to the IEEE 802.3 Ethernet standard, each Ethernet frame contains a 2-octet EtherType field to indicate which protocol is encapsulated in the PayLoad field, as shown in Figure 12-141. For standard time sync packets, this will contain the EtherType for the Precision Time Protocol (IEEE 1588), which is defined as 0x88F7. The CPTS hardware will compare this field to the TS_LTYPE1 field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG or the TS_LTYPE2 field in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register (depending on which enable bit was set) , which should also be programmed to 88F7h.

When a virtual LAN is used, an additional 4-octet 802.1Q tag is inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-141. To indicate to the CPTS hardware that a virtual LAN is in use, the TS_TX_VLAN_LTYPE1_EN (or TS_TX_VLAN_LTYPE2_EN) enable bit must be set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register. The EtherType for the 802.1Q tag is defined as 0x8100, and the CPTS hardware will compare this value to the TS_VLAN_LTYPE1 (or TS_VLAN_LTYPE2 depending on which enable bit was set) field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register, which should also be programmed to 0x8100.

When two stacked VLANs are used, two additional 4-octet 801.Q tags are inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-141. In this case, both TS_VLAN_LTYPE1 and TS_VLAN_LTYPE2 must be enabled. The outer tag must match the value of the TS_VLAN_LTYPE1 field, and the inner tag must match the value of the TS_VLAN_LTYPE2 field.

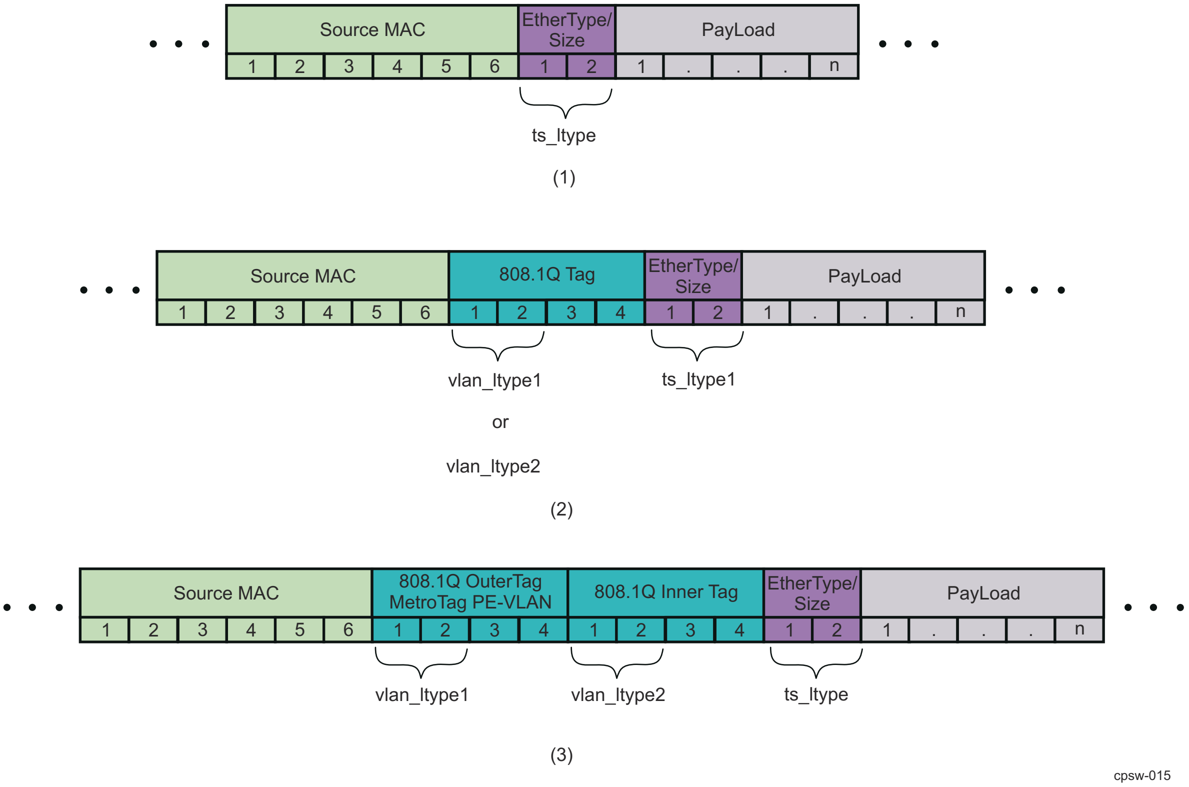

Figure 12-141. Partial Ethernet-II Frames Showing Register Mapping of EtherTypes for a Simple Frame (1), a Single 1Q Tag Added (2), and Two 1Q Tags Added (3)

12.3.1.4.7.13.5.1 Ethernet Port Receive Event

This section describes Ethernet port receive events. Ethernet port generates time synchronization events for valid received time sync packets. For every packet received on the Ethernet port, a timestamp will be captured by the receive module inside the CPTS for the corresponding port. The time stamp will be captured by the receive module regardless of whether or not the packet is a time synchronization packet to make sure that the time stamp is captured as soon as possible. The packet is sampled on both the rising and falling edges of the CPTS_RFT_CLK, and the time stamp will be captured once the start of frame delimiter for the receive packet is detected.

After the time stamp has been captured, the receive interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPSW decoder determines if the packet is a valid Ethernet receive time synchronization event. The receive interface for the port will use the following criteria to determine if the packet is a valid Annex D, Annex E, or Annex F time synchronization Ethernet receive event:

Annex D (IPv4)

1. Receive annex D time sync is enabled (TS_RX_ANNEX_D_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x0800
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800
3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

   -OR-

   The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:

  a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set -OR-
  b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.

9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
11. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex E (IPv6)

1. Receive annex E time sync is enabled (TS_RX_ANNEX_E_EN bit is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field.
6. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

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Note

All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.

-OR-

The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.

7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
    a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register is set, or
    b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.
10. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex F (IEEE 802.3)

1. Receive Annex F time sync is enabled (TS_RX_ANNEX_F_EN is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true:
    a. The first packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG/ CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
    b. The first packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
    c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register
    d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
    e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
    f. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.

    g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
    h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register

3. The PTP message begins in the byte after the LTYPE.
4. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
5. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

If all of the criteria described above are met for either Annex D, Annex E, or Annex F, and the packet is determined to be a valid time synchronization packet, then the RX interface will push an Ethernet receive event into the event FIFO.

12.3.1.4.7.13.5.2 Ethernet Port Transmit Event

This section describes Ethernet port transmit events. For every packet transmitted on the Ethernet ports, the port transmit interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPTS transmit interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet transmit event. The CPSW decoder determines if the packet is a valid ethernet receive time synchronization event. To be a valid Ethernet transmit time synchronization event, the conditions listed below must be true for either Annex D, Annex E, or Annex F:

Annex D (IPv4)

1. Transmit time sync is enabled (TS_TX_ANNEX_D_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
    a. The first packet LTYPE matches 0x0800
    b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800

   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800

3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

> The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if TS_TTL_NONZERO is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   f. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
11. The packet was sent by host port 0.

Annex E (IPv6)

1. Transmit annex E time sync is enabled (TS_TX_ANNEX_E_EN bit is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).

2. One of the sequences below is true.
    a. The first packet LTYPE matches 0x86dd.
    b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
    c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
    d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field..
6. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
    a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

    Note

    All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.

    -OR-

    The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
    a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.

8. The PTP message begins in byte 62.
9. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
10. The packet was sent by host port 0.

Annex F (IEEE 802.3)

1. Transmit time sync is enabled (TS_TX_ANNEX_F_EN is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   d. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG

register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register

3. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
4. The packet was sent by host port 0.

If all of the criteria described above are met, and the packet is determined to be a valid time synchronization packet, then the time stamp for the transmit event will not be generated until the start of frame delimiter of the packet is actually transmitted. The start of frame delimiter will be sampled on every rising and falling edge of the CPTS_RFT_CLK. Once the packet is transmitted, then the TX interface will push an Ethernet transmit event into the event FIFO.

12.3.1.4.7.13.5.3 Time Sync Message Types

Table 12-168. Values of Message Type Field

Message Type	Value (hex)
Sync	0
Delay_Req	1
Pdelay_Req	2
Pdelay_Resp	3
Reserved	4:7
Follow_Up	8
Delay_Resp	9
Pdelay_Resp_Follow_Up	A
Announce	B
Signaling	C
Management	D
Reserved	E:F

Once a transmitted or received packet is determined to be a valid time sync packet, the Ethernet Transmit Event or Ethernet Receive Event is loaded onto the Event FIFO.

The CPSW3_CPSW_NU_CPTS_EVENT_1_REG register contains the Message Type and Sequence ID values from the original time sync packet. The CPSW3_CPSW_NU_CPTS_EVENT_0_REG (and CPSW3_CPSW_NU_CPTS_EVENT_3_REG) register contains the time stamp value when the packet arrived at the corresponding port.

12.3.1.4.7.14 Timestamp Compare Event

Note

Timestamp compare events are generated for non-toggle mode only.

The CPTS can generate an event for a time stamp comparison in 32-bit or 64-bit mode.

12.3.1.4.7.14.1 32-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 32-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register and the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.3.1.4.7.14.2 64-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 64-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG and CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG registers and the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.3.1.4.7.15 Host Transmit Event

The host can send a packet to be transmitted on an Ethernet port that will generate a time synchronization event. The host sets the TSTAMP_EN bit and sends the DOMAIN, MESSAGE_TYPE, and SEQUENCE_ID in the additional control information that resides in the protocol specific section of the descriptor that is transmitted to the CPSW_3G. An event is then generated and placed on the event FIFO once the packet is transmitted. Host events allow the user to timestamp exactly when a software generated packet exits the device.

12.3.1.4.7.16 CPTS Interrupt Handling

When an event is push onto the Event FIFO, an interrupt can be generated to indicate to software that a time sync event occurred. The following steps should be taken to process time sync events using interrupts:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.
2. Upon interrupt, read the CPSW3_CPSW_NU_CPTS_EVENT_0_REG through CPSW3_CPSW_NU_CPTS_EVENT_3_REG registers values.
3. Set the CPSW3_CPSW_NU_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
4. Process the interrupt as required by the application software.

Software has the option of processing more than a single event from the event FIFO in the interrupt service routine in the following way:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG
2. Upon interrupt, enter the CPTS service routine.
3. Read the CPSW3_CPSW_NU_CPTS_EVENT_0_REG through CPSW3_CPSW_NU_CPTS_EVENT_3_REG registers values.
4. Set the CPSW3_CPSW_NU_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
5. Wait for an amount of time greater than four CPTS_RFT_CLK periods plus four CPPI_ICLK periods.
6. Read the TS_PEND_RAW bit in the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG register to determine if another valid event is in the event FIFO. If bit TS_PEND_RAW is asserted, go to step 3. If bit TS_PEND_RAW is not asserted proceed with step 7.
7. Process the interrupt(s) as required by the application software.

Software also has the option of disabling the interrupt and polling the TS_PEND_RAW bit of the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG register to determine if a valid event is on the event FIFO.

12.3.1.4.8 CPPI Streaming Packet Interface

The receive streaming interface on port 0 of the CPSW is responsible for receiving packet for Ethernet egress data from the packet streaming switch in the . The CPPI receive port is equivalent to an Ethernet port with the difference being that the data is provided to the CPSW in the 128-bit streaming interface data format instead RGMII data format.

In addition to the packet data, the receive streaming interface also can provide additional control information that resides in the information words of the descriptor that was transmitted to the CPSW.

The tables below show the information that may be passed along with which descriptor information word to put it in.

12.3.1.4.8.1 Port 0 CPPI Transmit Packet Streaming Interface (CPSW_3G Egress)

The CPSW_3G has a single transmit packet streaming interface. All Ethernet packet data destined for the host (Port 0) is transferred on the transmit packet streaming interface. The transmit packet streaming interface is equivalent to an Ethernet MAC output with the difference being that 128-bit streaming interface data is output. Egress packet data is packed on the 128-bit data bus with all words having 16-bytes except possibly the last packet data word which is the word previous to the EOP word. INFO Word 0–3 is transferred on SOP. The EOP word contains the packet status 0–3 (data type 24) which includes the timestamp and checksum data. Packets are not dropped on the transmit streaming interface due to pushback, but packets may be dropped in the associated priority FIFO.

INFO Word 0–3 and Status Data Word 0–3 (on EOP) are the only non-payload data word types that are transferred. Long packets are truncated at the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN byte value of the ingress port (only the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG_k number of bytes are kept if long packets are transferred due to CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k register copy error frames set - RX_CEF_EN). MAC control frames are only transferred if the receiving Ethernet port has the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN bit set.

The error encoding on the TXST_PKT_ERR[3:0] output is shown in Table 12-169:

Table 12-169. Error Encoding on the TXST_PKT_ERR[3:0] Output

TXST_PKT_ERR[3:0]	Description
0000	No Error
0001	CRC Error
0010	Code or alignment error
0011	Short (no code/align/crc error)
0100	FragCRC (short with crc error)
0101	Frag Code/Align (short with code/align error)
0110	Long
0111	Jabber CRC (long with crc error)
1000	Jabber Code/Align (long with code/align error)
1001	Mac ontrol packet (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN set on ingress Ethernet port)
1010	Mac control CRC
1011	Mac control Code/Align
1100	Mac control short/frag (short MAC control frame with CRC/Code/Align)
1101	Mac control long/jabber (long MAC control frame with CRC/Code/Align)
1110	Reserved

Table 12-169. Error Encoding on the TXST_PKT_ERR[3:0] Output (continued)

TXST_PKT_ERR[3:0]	Description
1111	Reserved

The CPPI Port 0 transmit packet streaming interface has a single output thread. If a packet transmission has begun then the entire packet will be transmitted before the next packet is sent (packet data from multiple packets are not interleaved on the transmit streaming interface). The default egress flow is the port number minus 1, concatenated with the 3-bit Port 0 transmit FIFO hardware switch priority. For example, a packet that was received on port 4 with a Port 0 transmit FIFO hardware switch priority of 5 would be sent on flow 29 (decimal) or flow 0b0011101 (binary). Priority remapping on ingress and Port 0 transmit egress effects the output flow.

INFO Words are a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Figure 12-142. TX INFO Word 0 Format

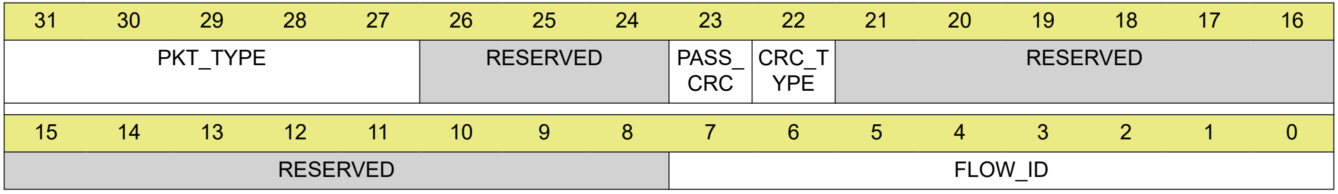

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PKT_TYPE					RESERVED			PASS_CRC	CRC_TYPE	RESERVED					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED								FLOW_ID							

Bit	Field	Description
31-27	PKT_TYPE	Always set to 0b00111. Host PD (Packet Descriptor) Word 2. Packet Type: bits[31-27].
26-24	RESERVED	Reserved.
23	PASS_CRC	This bit is cleared to zero (no CRC passed) when the P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register is set (and the egress packet has no errors). When the remove bit is cleared to zero then this bit is cleared and no CRC is passed with the output packet. The packet length includes the CRC if it is present.
22	CRC_TYPE	The packet CRC type. The type of CRC passed is determined by CRC_TYPE field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k register (not by the type of CRC the packet had on Ethernet port ingress). Host PD Word 1. Protocol Specific Flags: bits[27-24]. 0h: Ethernet CRC 1h: Castagnoli CRC
21-8	RESERVED	Reserved.
7-0	FLOW_ID	This is the packet output transmit streaming interface flow. The default flow ID can be overridden by ALE classification (Thread mapping). The switch default flow is the 3-bit “From Port” value concatenated with the 3-bit “Switch Priority” {From_Port[2:0], Switch_Priority[2:0]} as shown below: Host PD (Packet Descriptor) Word 1. Flow ID: bits[13-0]. 0h: The packet was received on Ethernet port 1 Switch Priority – The actual hardware switch priority that the packet was stored in on the CPPI transmit FIFO.

Figure 12-143. TX INFO Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x4 (fixed_ps_size)												0			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		PKT_LENGTH													

Bit	Field	Description
31-20	FIXED_PS_SIZE	Fixed packet size: 0x4
19-14	RESERVED	Reserved.
13-0 (Host PD (Packet Descriptor) Word 1. Packet Length: bits[21-0])	PKT_LENGTH	Specifies the number of bytes in the entire packet. Offset bytes are not included. Valid only on SOP. The packet length must be greater than zero. The packet data will be truncated to the packet length if the packet length is shorter than the sum of the packet buffer descriptor buffer lengths. A host error occurs if the packet length is greater than the sum of the packet buffer descriptor buffer lengths.

Figure 12-144. TX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xFFFF															

Figure 12-145. TX INFO Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SRC_ID							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Bit	Field	Description
31-24	RESERVED	Reserved.
23-16	SRC_ID	The packet SRC_ID value comes from the PORT1/PORT2 field in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG register. (src_tag) PD (Packet Descriptor) Word 3. Source Tag Low bits[23-16] if RFLOW[a]_RFC.rx_src_tag_lo_sel = 0x4 or (src_tag) PD (Packet Descriptor) Word 3. Source Tag High bits[31-24] if RFLOW[a]_RFC.rx_src_tag_hi_sel = 0x4
15-0	RESERVED	Reserved.

Note

TX Status Data Word [0..3] are mapped to Host Packet Descriptor Protocol Specific Words if RFLOW[a]_RFA.rx_psinfo_present = 1 and RFLOW[a]_RFA.rx_ps_location = 0

Figure 12-146. TX Status Data Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Figure 12-146. TX Status Data Word 0 Format (continued)

TIMESTAMP[31:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[31:0]															

Bit	Field	Description
31-0	TIMESTAMP[31:0]	Contains the lower 32-bits of the time stamp value.

Figure 12-147. TX Status Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP[63:32]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[63:32]															

Bit	Field	Description
31-0	TIMESTAMP[63:32]	Contains the upper 32-bits of the time stamp value.

Figure 12-148. TX Status Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											IPV4_VALID	IPV6_VALID	TCP_UDP_N	FRAGMENT	CHECKSUM_ERROR
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM_ADD															

Bit	Field	Description
31-21	RESERVED	Reserved.
20	IPV4_VALID	An IPV4 TCP or UDP Packet was detected.
19	IPV6_VALID	An IPV6 TCP or UDP Packet was detected.
18	TCP_UDP_N	Valid only when either the IPV4_VALID or IPV6_VALID bits are set. 0h: Indicates UDP packet was detected. 1h: Indicates TCP packet was detected.
17	FRAGMENT	Indicates that an IP fragment was detected. Valid only when when either the IPV4_VALID or IPV6_VALID bits are set.
16	CHECKSUM_ERROR	Valid only when either the IPV4_VALID or IPV6_VALID bits are set.
15-0	CHECKSUM_ADD	This is the value that was summed during the checksum computation. This value is FFFFh for IPV4/6 UDP/TCP packets with no checksum error.

Figure 12-149. TX Status Data Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 12-149. TX Status Data Word 3 Format (continued)

0

Bit	Field	Description
31-0	RESERVED	Reserved.

12.3.1.4.8.2 Port 0 CPPI Receive Packet Streaming Interface (CPSW_3G Ingress)

Info Word 0/1/2/3 (INFO1 and INFO3 are ignored) are transferred on SOP. If a timestamp word (Extended Packet Info Word 0/1/2/3) is to be transferred it must be after SOP and before any packet data is transferred. Any following non-data type words will be dropped. The EOP word must be payload data.

Input receive packets cannot be aborted by the host. The INFO Word bit descriptions and Extended Packet INFO Word bit descriptions are shown below. The PASS_CRC bit indicates that the CRC is passed with the packet data. Packets that have a passed CRC that is an error CRC will be output on the Ethernet port with at least one CRC byte inverted to indicate the error if P0_RX_PASS_CRC_ERR bit is set, otherwise they are dropped. The packet is a directed packet when any of the TO_PORT bits are nonzero. A packet may be directed only to a single port. The packet will be sent to the port number indicated. For directed packets the lookup process is skipped to determine the destination. However, in vlan aware mode (when VLAN_AWARE bit in the CPSW3_CONTROL_REG register is set to 1h) the lookup is performed to determine untagged egress. Packets longer then the value in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bit field are dropped. Packets shorter than 60-Bytes are padded to 64-Bytes (after adding pad and CRC) if P0_RX_PAD bit in the CPSW3_CONTROL_REG register is set and if PASS_CRC is clear, otherwise they are dropped. This means that packets shorter than 64-Bytes are dropped if the PASS_CRC info bit is set regardless of P0_RX_PAD bit (packets are padded only if they are short and do not have CRC).

A RX INFO word is a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Note

RX Control Data Words [0..2] are mapped to Host Packet Descriptor Protocol Specific Words if (TCHAN[a]_TCFG.tx_filt_pswords = 0) and (Host PD Word 1.Protocol Specific Region Location.bit[28] = 0h) and (Host PD Word 1.Protocol Specific Valid Word Count.bits[22-27] = 4h)

Figure 12-150. RX INFO Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PASS_CRC	CRC_TYPE	RESERVED					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED															

Bit	Field	Description
31-24	RESERVED	Reserved.
23	PASS_CRC	The PASS_CRC bit indicates that the CRC is passed with the packet data. 0h: CRC is not passed with packet (CRC_TYPE is don't care) 1h: CRC of type CRC_TYPE is passed with the packet.

Bit	Field	Description
22 (Host PD (Packet Descriptor) Word 1. Protocol Specific Flags: bits[27-24])	CRC_TYPE	CRC Type 0h: Ethernet CRC 1h: Castagnoli CRC
21-0	RESERVED	Reserved.

Figure 12-151. RX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											TO_PORT				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED															

Bit	Field	Description
31-21	RESERVED	Reserved.
20-16 (Host PD (Packet Descriptor) Word 3. Dest Tag Low bits[8-0])	TO_PORT	Port number to send the directed packet to. This field is set by the host. This field is valid on SOP. Directed packets go to the directed port, but an ALE lookup is performed to determine untagged egress in VLAN_AWARE mode. 0h: Not directed 1h: Send the packet to port 1. 2h: Send the packet to port 2.
15-0	RESERVED	Reserved.

Figure 12-152. RX Control Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP_EN	RESERVED			DOMAIN								MSG_TYPE			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEQUENCE_ID															

Bit	Field	Description
31	TIMESTAMP_EN	When set, this bit indicates that the packet will generate a timesync event on Ethernet egress (if the CPTS is configured properly) with the associated DOMAIN, MSG_TYPE, and SEQUENCE_ID.
30-28	RESERVED	Reserved.
27-20	DOMAIN	Timesync domain.
19-16	MSG_TYPE	Timesync message type.
15-0	SEQUENCE_ID	Timesync sequence ID.

Figure 12-153. RX Control Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHECKSUM_RESULT								CHECKSUM_START_BYTE							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM_INV	RESERVED	CHECKSUM_BYTECOUNT													

Bit	Field	Description
31-24	CHECKSUM_RESULT	This is the packet byte number where the checksum result will be placed in the egress packet. The first packet byte which is the first byte of the destination address is Byte 1 (not byte zero).
23-16	CHECKSUM_START_BYTE	This is the packet byte number to start the checksum calculation on. The first packet byte is Byte 1.
15	CHECKSUM_INV	When set, a zero checksum value will be inverted and sent as FFFFh.
14	RESERVED	Reserved.
13-0	CHECKSUM_BYTECOUNT	This is the number of bytes to calculate the checksum on. The outgoing Ethernet packet will have a checksum inserted when this value is non-zero.

Other INFO words are not taken into account.

12.3.1.4.8.3 Cut-Thru

An Ethernet port received packet can be sent cut-thru to all destination ports when the following is true:

- The CPSW3_CONTROL_REG[19] CUT_THRU_ENABLE bit is set, and
- The receive port is full duplex, and
- The Ethernet receive port speed is non-zero, and
- The packet was received on an express priority, and
- The Ethernet receive port has the remapped received packet priority enabled via the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CUT_THRU_REG[15-8] RX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports have the remapped packet priority enabled via the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CUT_THRU_REG[7-0] TX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports are full duplex, and
- All Ethernet destination ports are express priorities, and
- All Ethernet destination ports have a non-zero CPSW_PN_SPEED_REG_k[3-0] SPEED, and
- All Ethernet destination ports are equal to or slower in speed than the Ethernet receive port, and
- The host port is not in the destination port list unless the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit is set.

Whether or not a packet actually egresses cut-thru (with or without delay) on an Ethernet destination port depends on traffic congestion on that port. Cut-thru is compatible with Intersperced Express Traffic (IET) and Enhanced Scheduled Traffic (EST).

12.3.1.4.8.3.1 Host Port Cut-Thru Operations

Packets received (CPSW ingress) on the host port are sent store-and-forward to all Ethernet destination ports. Setting the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit enables Ethernet received packets to be sent cut-thru to a destination port mask that includes the host port. The packet can egress cut-thru on Ethernet ports, but the packet will not actually egress cut-thru on the host port. Setting CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH can cause head of line blocking on the host priority if multiple Ethernet ports are sending to the same host port priority. The head of line blocking issue is worsened if there are differing Ethernet port speeds. Clearing the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit causes packets with the host port in the destination mask to egress store-and-forward on all egress ports.

12.3.1.4.8.3.2 Cut-Thru Error Packets

Any received packets with errors sent cut-thru from an Ethernet receive port to any Ethernet transmit port(s) will egress with at least one byte of the generated outgoing packet CRC inverted to indicate the error. This is due to the fact that cut-thru operations begin before the end of packet when the receive port determines that the packet had an error (long/code/align/CRC).

Any packet also sent cut-thru with the host included in the destination port mask will be dropped to the host (TXST_PKT_DROP) with the packet error indicated on TXST_PKT_ERR[3:0].

Any long/Jabber/Code/Align/CRC errored Ethernet received packet that is not actually sent cut-thru by the receive port will dropped unless CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is set (which if set will cause the packet to be sent to the host port with the error indicated on TXST_PKT_ERR[3:0]. If a long/Jabber/Code/Align/CRC errored Ethernet received packet is sent cut-thru by the received port then a set CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN will not cause the errored packet to be sent to the host port since the packet has already been transferred to the destination ports.

The following cut-thru notes are valid:

- Any Ethernet received packet and that is sent cut-thru to any destination port will not be dropped at any destination port due to priority maximum lengths (CPSW3_CPSW_NU_TX_PRIx_MAXLEN_REG).
- Any Ethernet received packet that is decoded as a timesync packet will be sent store-and-forward to all destination ports.
- Cut-Thru is full duplex only.
- Cut-Thru is not compatible with any form of flow control.
- Cut-Thru should not be enabled for any receive port that is in ALE bypass mode.

12.3.1.4.8.4 Port Speed

Cut-thru operations require that the Ethernet port speeds be known. Port speed can be set manually by software or be automatically determined by the hardware. A zero port speed causes the port to be disabled for cut-thru operations, but does not disable the port. The port speed values are as follows:

- 0000 – Port speed operations disabled (not a port disable)
- 0001 – 10Mpbs
- 0010 – 100Mbps
- 0011 – 1G
- 0100 – 2.5G
- 0101 – 5G
- 0110 – 10G
- 0111 through 1111 Reserved

When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is cleared, the port speed is written by software. When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is set, the port speed is automatically detected by the hardware.

12.3.1.4.8.5 CPPI Checksum Offload

The CPPI host port can be enabled to perform checksum offload on host port packet ingress and egress. UDP (User Datagram Protocol) and TCP (Transmission Control Protocol) over IPV4 and IPV6 are supported. For the purposes of checksum description, the first packet byte (the first byte of the destination address) is byte 1 (not byte 0). That is, a 64 byte packet goes from byte 1 to byte 64. For all packet types, the S_CN_SWITCH bit in the CPSW3_CONTROL_REG register must be set for the Outer VLAN L type to be supported.

12.3.1.4.8.5.1 CPPI Transmit Checksum Offload

IPV4 and IPV6 UDP and TCP packets that are received on any Ethernet port and destined for port 0 egress are checked for correct checksum as described below. The byte counts below are shown for packets with no VLAN’s. The byte counts vary with one or two packet VLAN's. Packets received on an Ethernet port with errors are not checked for a correct checksum if they are passed to the host.

12.3.1.4.8.5.1.1 IPV4 UDP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).
- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no UDP header).
- Byte 24 = 0x11 for UDP protocol.
- Received packet UDP checksum of zero means that there is no IPV4 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.3.1.4.8.5.1.2 IPV4 TCP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).
- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no TCP header).
- Byte 24 = 0x06 for TCP protocol.

12.3.1.4.8.5.1.3 IPV6 UDP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x11 for UDP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x11). Middle and last fragments have a fragment extension header followed by data only (no UDP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.
- Received packet UDP checksum of zero means that there is no IPV6 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.3.1.4.8.5.1.4 IPV6 TCP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x06 for TCP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x06). Middle and last fragments have a fragment extension header followed by data only (no TCP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset.

Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.

12.3.1.4.8.6 CPPI Receive Checksum Offload

Packets sent from host port 0 (switch ingress) to any Ethernet port can have a checksum calculated and inserted into the Ethernet egress packet. The RX_CHECKSUM_EN bit in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register must be set for receive checksum operation to be enabled. When bit RX_CHECKSUM_EN is enabled, Control Data Word 2 input on CPPI receive PSI interface determines how the checksum is calculated. The CHECKSUM_RESULT field in Control Data Word 2 determines where the checksum is inserted. The checksum result location is adjusted by the egress port if a VLAN is to be inserted or removed on Ethernet port egress.

12.3.1.4.8.7 Egress Packet Operations

Each CPSW egress port (Ethernet and Host) is capable of performing egress packet processing operations (CPSW3_CPSW_NU_ALE_EGRESSOP). IntraVLAN processing either adds, removes, or replaces VLAN information or does nothing. InterVLAN routing allows hardware routing between a limited number of VLANs - thereby allowing high-bandwidth or other routing operations to be offloaded from software to the CPSW (hardware). IntraVLAN processing and InterVLAN routing operations are mutually exclusive. In addition, the packet source and destination addresses can be swapped on egress to facilitate OAM or generic testing operations.

12.3.1.4.9 MII Management Interface (MDIO)

The MII Management interface module implements the 802.3 serial management interface to interrogate and control external Ethernet PHY using a two-wire bus.

12.3.1.4.9.1 MDIO Frame Formats

Table 12-170 shows the address, Table 12-171 shows the read format and Table 12-172 shows the write format of the supported Clause 45 MII Management interface frames. Post-increment accesses are not supported.

Table 12-182. MDIO Clause 45 Address Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	00	AAAAA	RRRRR	10	AAAA.AAAA.AAAA.AAAA

Table 12-183. MDIO Clause 45 Read Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	11	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD

Table 12-184. MDIO Clause 45 Write Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic 1. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic 1 bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction. The MDIO CPSW3_MDIO_USER_ADDR0_REG register must be written before a read or write operation is performed to set the address used in the operation. Each read or write operation has a preceeding address frame.

Preamble

The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a 1. This sequence provides the PHY a pattern to use to establish synchronization. The preamble is required in clause 45 operation.

Start Delimiter

The preamble is followed by the start delimiter which is indicated by a 00 pattern.

Operation Code

The operation code for an address transaction is 00. The operation code for a read is 11, while the operation code for a write is a 01.

PHY Address

The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

MMD Number

The MMD number is the 5 bits allowing 32 unique values. The first bit transmitted is the MSB.

Turnaround

An idle bit time during which no device actively drives the MDIO signal shall be inserted between the register address field and the data field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Address

The address field is 16 bits on address operations. The first bit transmitted is the MSB of the address word. Each read/write operation initiated has an automatic address operation initiated first that uses the MDIO CPSW3_MDIO_USER_ADDR0_REG/ CPSW3_MDIO_USER_ADDR1_REG register values as the 16-bit address.

Data

The Data field is 16 bits on read and write operations. The first bit transmitted and received is the MSB of the data word.

12.3.1.4.9.2 MDIO Functional Description

The MII Management I/F will remain idle until enabled by setting the ENABLE bit in the CPSW3_MDIO_CONTROL_REG register. The MII Management I/F will then continuously poll the link status from within the Generic Status Register of all possible 32 PHY addresses in turn recording the results in the MDIO CPSW3_MDIO_LINK_REG register. Individual PHY's can be enabled or disabled for polling the associated bit in the CPSW3_MDIO_POLL_EN_REG register. The CPSW3_MDIO_LINK_REG and CPSW3_MDIO_ALIVE_REG register bit values are updated on the poll of each PHY. The LINKSEL bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit in the MDIO CPSW3_MDIO_LINK_INT_RAW_REG register and the MDIO CPSW3_MDIO_LINK_INT_MASKED_REG register, if enabled by the LINKINT_ENABLE bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register.

The MDIO CPSW3_MDIO_ALIVE_REG register is updated by the MII Management I/F module if the PHY acknowledged the read of the generic status register. In addition, any PHY register read transactions initiated by the host also cause the MDIO CPSW3_MDIO_ALIVE_REG register to be updated.

At any time, the host can define a transaction for the MII Management interface module to undertake using the DATA, PHYADR, REGADR, and WRITE fields in a CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register. When the host sets the GO bit in this register, the MII Management interface module will begin the transaction without any further intervention from the host. Upon completion, the MII Management interface will clear the GO bit and set the USERINTRAW field in the CPSW3_MDIO_USER_INT_RAW_REG register corresponding to the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register being used. The corresponding bit in the CPSW3_MDIO_USER_INT_MASKED_REG register may also be set depending on the mask setting in the MDIO CPSW3_MDIO_USER_INT_MASK_SET_REG and CPSW3_MDIO_USER_INT_MASK_CLEAR_REG registers. A round-robin arbitration scheme is used to schedule transactions that may be queued by the host in different CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k registers. The host should check the status of the GO bit in the MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the ACK bit in the MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register to determine the status of a read transaction.

It is necessary for software to use the MII Management interface module to setup the auto-negotiation parameters of each PHY attached to a MAC port, retrieve the negotiation results, and setup the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register in the corresponding MAC.

12.3.1.5 CPSW0 Programming Guide

12.3.1.5.1 Initialization and Configuration of CPSW Subsystem

To configure the CPSW Ethernet Subsystem for operation, the host must perform the following:

1. Select the Interface (RMII, or RGMII) Mode. See the ENET1_CTRL and ENET2_CTRL[2-0] PORT_MODE_SEL fields.

2. Configure pads (pin muxing), as per the interface selected. Refer to *Pad Configuration Registers* and the device-specific data sheet.
3. Enable the CPSW Ethernet Subsystem clocks. See *CPSW Integration*
4. Ensure that at least 2000 CPPI_ICLK periods are run after reset is de-asserted.
5. Configure the CPSW3_CONTROL_REG register
6. Configure the Ethernet Port Source Address registers (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_SA_L_REG_k and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_SA_H_REG_k)
7. Configure the CPSW statistic port enable register CPSW3_CPSW_NU_STAT_PORT_EN_REG
8. Configure the ALE (Section 12.3.1.4.6.1 , *Address Lookup Engine*)
9. Configure the MDIO (Section 12.3.1.5.3.1 , *Initializing the MDIO Module*)
10. Configure Ethernet port, as per the desired mode of operations

12.3.1.5.2 CPSW Reset

To reset the Ethernet port, the host must perform the following:

1. Set CMD_IDLE bit to 1h in the Ethernet port control register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG.
2. Wait for IDLE bit to be set to 1h, which is indicated in the Ethernet port status register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_STATUS_REG.
3. Set SOFT_RESET bit to 1h in the Ethernet port software reset register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG.
4. Wait for SOFT_RESET bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG registers to be cleared to confirm reset completion.
5. Configure the Ethernet ports.
6. Re-configure registers reset to default value by CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG.

12.3.1.5.3 MDIO Software Interface

12.3.1.5.3.1 Initializing the MDIO Module

The following steps are performed by the application software or device driver to initialize the MDIO device:

1. Configure the PREAMBLE and CLKDIV bits in the MDIO Control register (CPSW3_MDIO_CONTROL_REG).
2. Enable the MDIO module by setting the ENABLE bit in CPSW3_MDIO_CONTROL_REG.
3. The MDIO PHY alive status register (MDIO CPSW3_MDIO_ALIVE_REG) can be read in polling fashion until a PHY connected to the system responded, and the MDIO PHY link status register (MDIO CPSW3_MDIO_LINK_REG) can determine whether this PHY already has a link.
4. Set the appropriate PHY addresses in the MDIO user PHY select register (CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k, where k = 0 or 1), and set the LINKINT_ENABLE bit to enable a link change event interrupt if desirable.
5. Set the appropriate LINKSEL bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register (where k = 0 or 1).
6. Set the appropriate USERINTMASKSET bit field in the CPSW3_MDIO_USER_INT_MASK_SET_REG register.
7. If an interrupt on general MDIO register access is desired, set the corresponding bit in the MDIO user command complete interrupt mask set register (MDIO CPSW3_MDIO_USER_INT_MASK_SET_REG) to use the MDIO user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1).

12.3.1.5.3.2 Writing Data To a PHY Register

The MDIO module includes a user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device.To write a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k) is cleared.
2. Write to the GO, WRITE, REGADR, PHYADR, and DATA bits in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k corresponding to the PHY and PHY register SW wants to write.
3. The write operation to the PHY is scheduled and completed by the MDIO module. Completion of the write operation can be determined by polling the GO bit in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k for a 0.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW3_MDIO_USER_INT_MASK_SET_REG), then the bit is also set in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.3.1.5.3.3 Reading Data From a PHY Register

The MDIO module includes a user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device. To read a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) is cleared.
2. Write to the GO, REGADR, and PHYADR bits in the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register corresponding to the PHY and PHY register SW wants to read.
3. The read data value is available in the DATA bit field in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register after the module completes the read operation on the serial bus. Completion of the read operation can be determined by polling the GO and ACK bits in CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register. After the GO bit has cleared, the ACK bit is set on a successful read.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW3_MDIO_USER_INT_MASK_SET_REG), then the bit is also set in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.3.2 Universal Serial Bus Subsystem (USBSS)

This section describes the Universal Serial Bus Subsystem (USBSS) in the device.

12.3.2.1 USB Overview

USB (Universal Serial Bus) provides a low-cost connectivity solution for numerous consumer portable devices by implementing a mechanism for data transfer between USB devices.

The device instantiates two independent instances of a third-party USB subsystem (USB2SS) operating at up to USB2.0 speeds (480Mb/s), either of which can be independently configured to act as a USB Host or a USB Device. SuperSpeed (5.0 Gb/s) operation is not supported in either operational mode.

12.3.2.1.1 USB Features

The USB 2.0 subsystem supports the following USB Features:

- Operational modes:
  - Supports USB 2.0 Host mode at High-Speed (HS, 480 Mbps), Full-Speed (FS, 12 Mbps), and Low-Speed (LS, 1.5 Mbps)
  - Supports USB 2.0 Device mode at High-Speed (HS, 480 Mbps), and Full-Speed (FS, 12 Mbps). Low-Speed is not supported in Device mode.
  - Supports all modes of transfers - Control, Bulk, Interrupt, and Isochronous.
- A DRD (Dual-Role-Device - Host or Device) USB controller with the following features:
  - Compatible to the xHCI 1.0 specification in Host mode
  - Compatible with the USB 2.0 specification in Device mode
  - Supports 15 IN (Receive), 15 OUT (Transmit) endpoints (EPs), and one EP0 endpoint which is bidirectional
  - Internal DMA controller
  - Descriptor caching and data pre-fetching ensures high performance
  - Dynamic FIFO memory allocation for all endpoints
- Operation flexibility
  - Same programming model for HS, FS, and LS operation
  - Each controller instance can provide either USB Host or USB Device functionality

12.3.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

12.3.2.2 USB Environment

12.3.2.2.1 USB Pin List

The names of the pins used by the USB2SS with descriptions are shown in Table 12-173 and Table 12-174.

Table 12-185. USB Signal Pins Description

Pin Name	I/O[1]	Description
USBn_DP	I/O	USB 2.0 and 1.1 Specification-compliant signal pins. They are HS/FS/LS bidirectional differential data pins.
USBn_DM	I/O	

(1) I = Input, O = Output, A = Analog

Table 12-186. USB Control, Configuration, and Monitor Signal Pins

Pin Name	I/O[1]	Description
USBn_DRVVBUS	O	An active-high digital output signal for VBUS power supply. Used to enable an external charge pump to supply +5V power to the VBUS receptable when operating in USB Host mode.
USBn_VBUS[2]	A/I	An analog input for monitoring the voltage on VBUS.

Table 12-186. USB Control, Configuration, and Monitor Signal Pins (continued)

Pin Name	I/O[1]	Description
USBn_ID	I	USB operational mode identifier. This functionality is supported via GPIO.

(1) I = Input, O = Output, A = Analog

(2) This pin is not 5V tolerant. Refer to the device-specific datasheet for implementation requirements.

12.3.2.2.2 Typical Pin Connections of Device

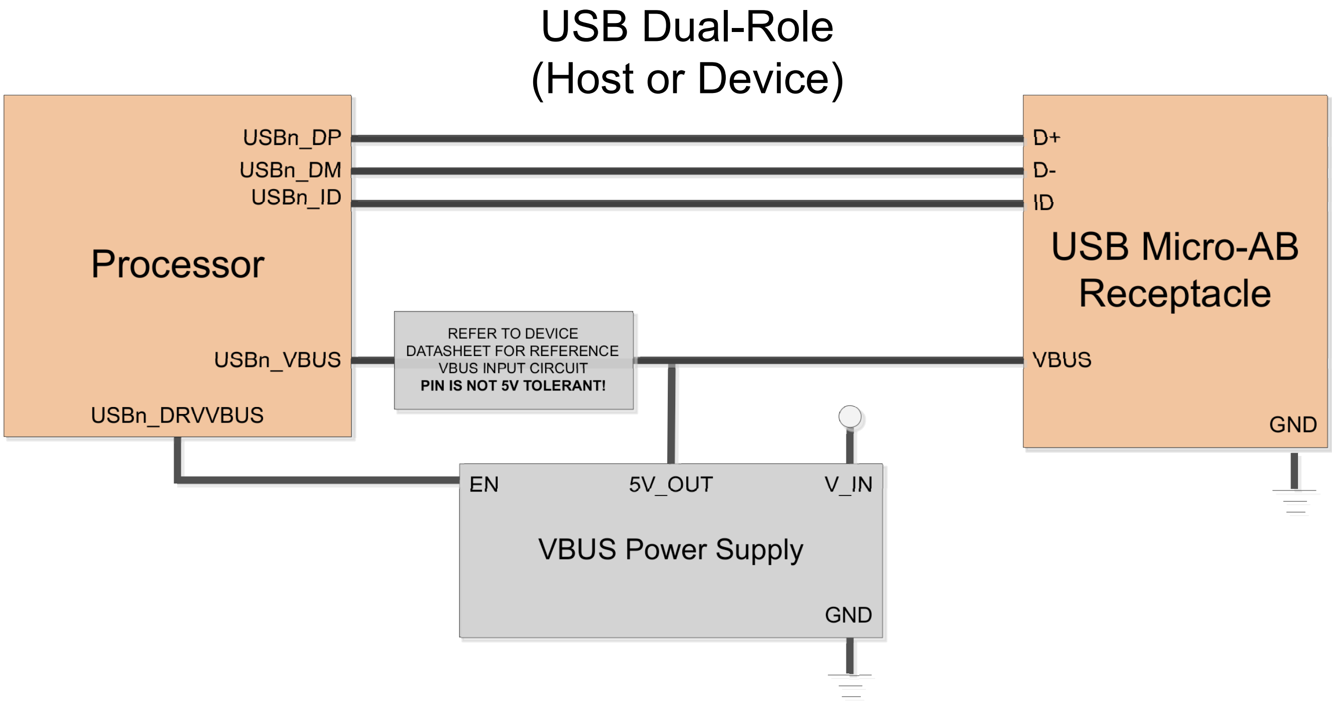

Figure 12-154. USB Dual-Role Connections

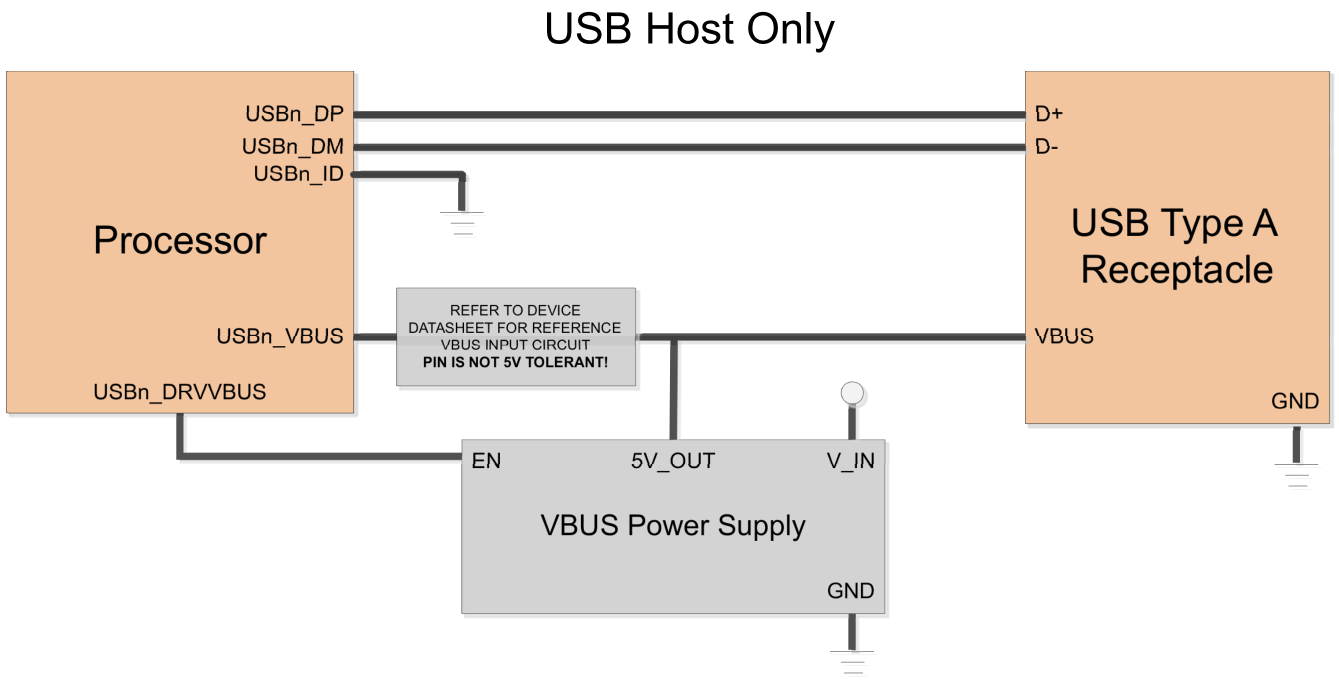

Figure 12-155. USB Host-Only Connections

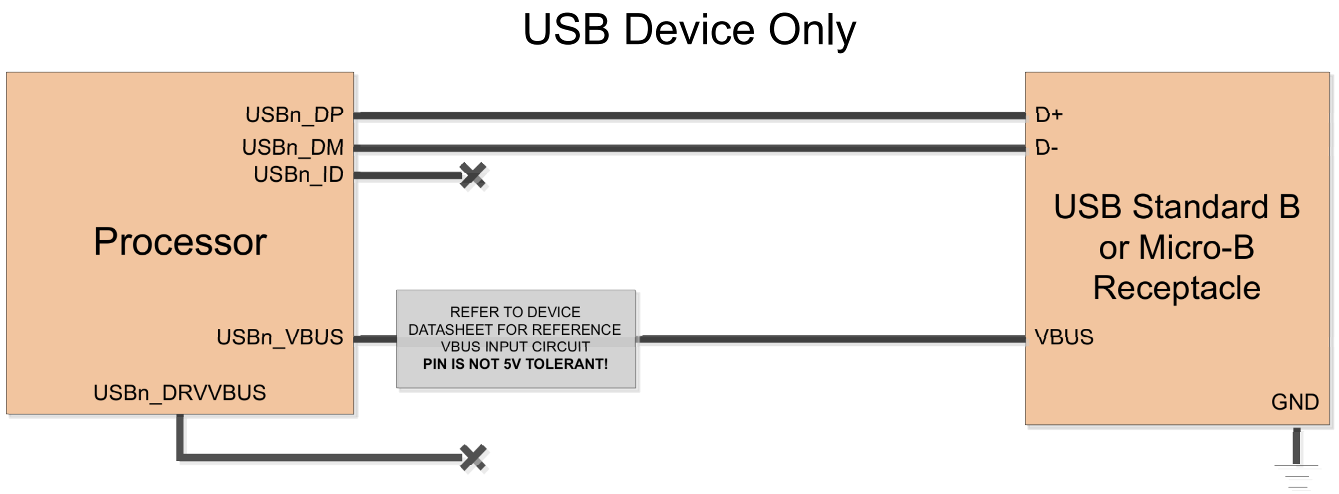

Figure 12-156. USB Device-Only Connections

12.3.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.3.2.4 Use Cases

This is a standard USB 2.0 module, and is optimized for following applications and systems:

- Portable electronic devices
- High-bandwidth applications

It supports all typical USB connections, and Table 12-175 shows some examples.

Table 12-187. Typical Use Cases In Terms of Connections

Connectors (Receptacle)	Signals to Use	SS	HS/FS	LS (Host only)	Comments
USB 2.0 Micro-AB	DP, DM, VBUS, ID	N	Y	Y	Support Host or Device operation, depending on state of the ID pin.
USB 2.0 Type-A	DP, DM, VBUS	N	Y	Y	Support HS/FS/LS Host
USB 2.0 Type-B	DP, DM, VBUS	N	Y	Y	Only used for USB2.0 Device (no LS)

12.3.2.4.1 USB Operational Mode Determination

USB[n]_ID Pin	USB[n]_VBUS Pin(1)	USB Role
FLOAT	FLOAT or GROUND	INDETERMINATE
GROUND	UNUSED	HOST
FLOAT	RAIL VOLTAGE	DEVICE

(1) PHY VBUS pin voltage is dependent on the divider circuit used on the board. Refer to the device datasheet for VBUS implementation requirements.

12.3.2.4.2 VBUS Voltage Sourcing Control

When either of the USB controllers assumes the role of a host, the controller is required to supply 5V to an attached device through its VBUS line. In order to achieve this task, the USB controller requires the use of external power logic (or a charge pump) capable of sourcing 5V power. The USB_DRVVBUS pin is used as a control signal to enable/disable this external power logic to either source or disable power on the VBUS line. The control on the USB_DRVVBUS is handled by the controller based on host software programming. The control should be transparent to the user so long as the proper hardware connection and software initialization are in place. The USB controller drives the USB_DRVVBUS signal high when it assumes the role of a host while the controller is in session. When assuming the role of a device, the controller drives the USB_DRVVBUS signal low disabling the external charge pump/power logic; hence, no power is driven on the VBUS line (in this case, power is expected to be provided by the external host).

Note that both USB controllers are self-powered and the device does not rely on the voltage on the VBUS line sourced by an external host for controller operation when assuming the role of a device. The voltage present on the VBUS line is used to identify the presence of a Host. The USB PHY continually monitors the voltage on the VBUS and reports the status to USB controller.

12.3.2.4.3 VBUS Detection

VBUS detection is supported by the USB2SS via the USB_VBUS pin, but **it is important that this pin not be connected directly to the connector 5V or any other 5V source.** Instead, an external circuit must be used to ensure that the recommended operating conditions of the pin are not exceeded. Refer to the device datasheet for requirements and example VBUS-sense circuitry.

The PHY includes session valid and VBUS valid comparators and provides corresponding status signals.

The Controller uses the session valid output from the PHY in device mode. One of the reasons is because the USB specification requires that the DP pull-up (implemented inside the PHY) must be be enabled only after VBUS is turned on by host. This PHY output also in general indicates that a connection is active from host and it can also be used to detect disconnects.

The USB2SS wrapper also includes logic to detect a change on session valid and VBUS valid outputs from PHY.

12.3.2.4.4 Pull-up/Pull-down Resistors

As the USB controllers are dual role controllers, capable of assuming a role of a host or device, the required pull-up/pull-down resistors cannot exist external to the device. These pull-up/pulldown resistors exist internal to the device, within the PHY to be more specific, and are enabled or disabled based on the role the controller assumes allowing for dynamic hardware configuration. When assuming the role of a host, the data lines are pulled low by the PHY enabling the internal 15KΩ resistors. When assuming the role of a device the required 1.5KΩ pull-up resistor on the D+ line is enabled automatically to signify the USB capability to the external host as a FS device (HS operation is negotiated during reset bus condition). Low-Speed Device functionality is not supported.

12.4 Memory Interfaces

This section describes the memory interfaces in the device.

12.4.1 Flash Subsystem (FSS)

This section describes the Flash Subsystem (FSS) in the device.

12.4.1.1 FSS Overview

The Flash Subsystem (FSS) provides access to external Flash devices via Octal Serial Peripheral Interface (OSPI).

The FSS includes one OSPI. For more information, see *Octal Serial Peripheral Interface (OSPI)*.

Figure 12-157 shows the FSS overview.

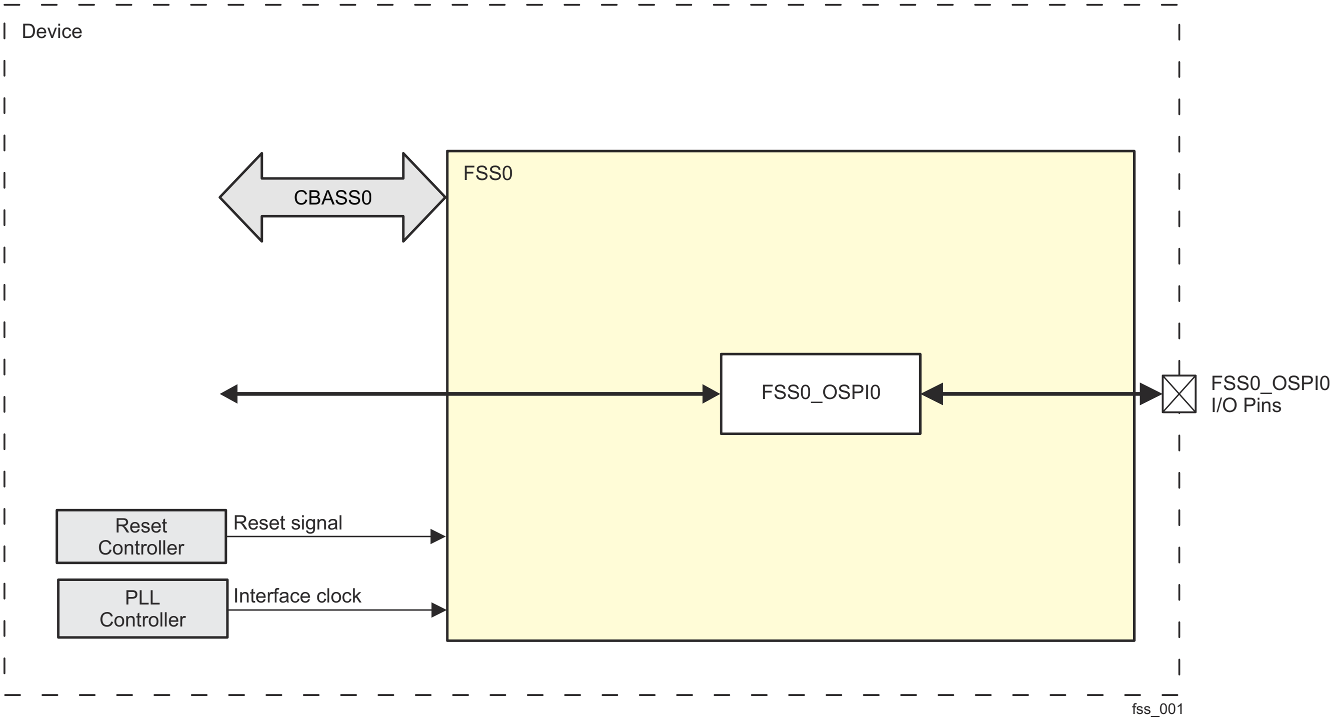

Figure 12-157. FSS Overview

12.4.1.1.1 FSS Features

For more information, see Section 12.4.2.1.1 , *OSPI Features*.

12.4.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.4.1.2 FSS Environment

The FSS is hereinafter also referred to as FSS0.

12.4.1.2.1 FSS Typical Application

Figure 12-158 shows typical FSS application.

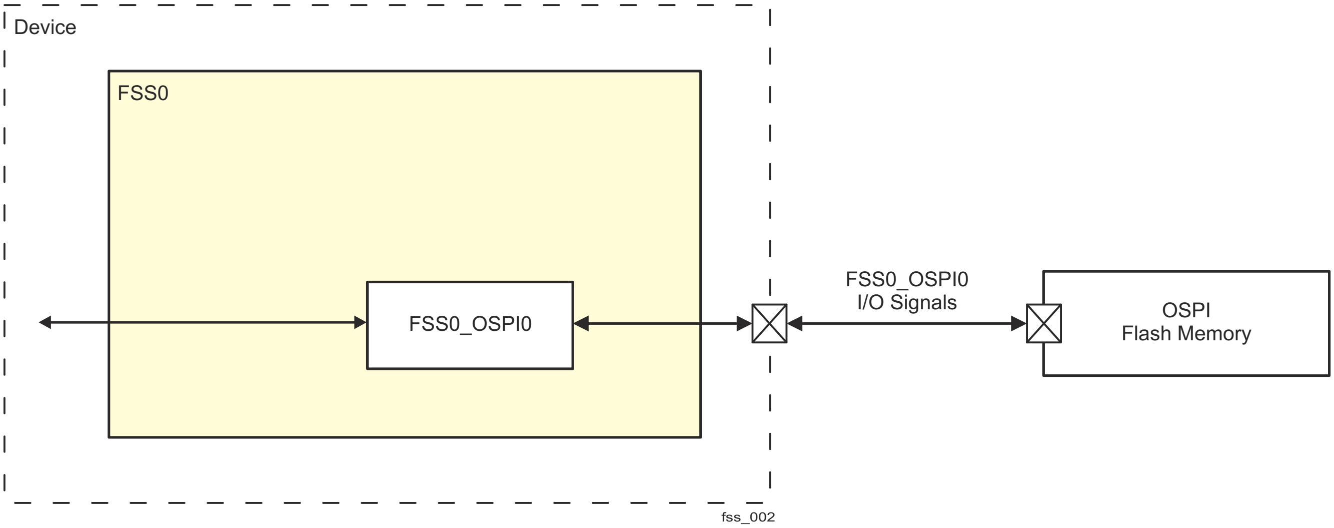

Figure 12-158. FSS Typical Application

Table 12-176 describes the FSS I/O signals.

Table 12-188. FSS I/O Signals

FSS0 Interface	I/O Signals
FSS0_OSPI0	For more information about OSPI I/O signals, see *OSPI I/O Signals*.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.1.4 FSS Functional Description

12.4.1.4.1 FSS Block Diagram

Figure 12-159 shows the FSS block diagram.

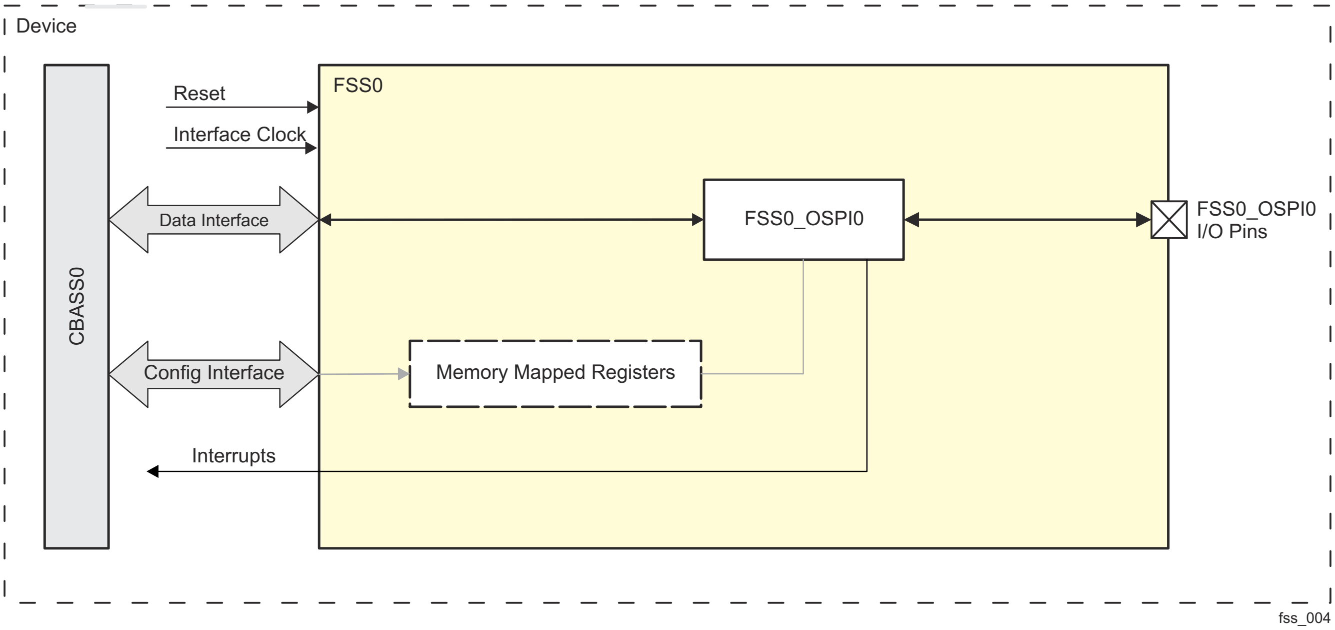

Figure 12-159. FSS Block Diagram

FSS Blocks:

- CBASS0: The CBASS0 interconnect allows FSS to communicate with the device modules and subsystems.
- Data Interface: It is 64-bit data/32-bit address multi issue data interface with coherent in-band bypass. It provides accessibility to the FSS0_OSPI0.
- Config Interface: It is used for configuration of the memory mapped registers within the FSS.
- Interface Clock and Reset:
  - For more information, see *FSS0 Clocks and Resets*.
  - For more information, see *FSS0_OSPI Clocks and Resets*.
- Interrupts: For more information, see *FSS0_OSPI Hardware Requests*.
- Memory Mapped Registers: This block includes the FSS registers. The configuration of these registers defines which FSS features are used. For more information, see *FSS Registers*.
- FSS0_OSPI0: For more information about OSPI, please see *Octal Serial Peripheral Interface (OSPI)*.
- FSS0_OSPI0 I/O Pins: For more information, see *OSPI I/O Signals*.

12.4.1.4.2 FSS Regions

12.4.1.4.2.1 FSS Regions Boot Size Configuration

The boot size for FSS defaults to 64 MB but can be configured to be 128 MB. Selection of boot block which will be used is also configurable. For more information see CTRLMMR_FSS_CTRL register in *Control Module (CTRL_MMR)*.

12.4.1.4.3 FSS Memory Regions

Table 12-177 shows the FSS memory regions.

Table 12-189. FSS Memory Regions

Address Range	Size	Description
0x400000000 - 0x4FFFFFFFF	4 GB	External Memory Space (Region 0)
0x060000000 - 0x067FFFFFF	128 MB	Boot Space (Region 1)
0x500000000 - 0x5FFFFFFFF	4 GB	External Memory Space (Region 3)

12.4.1.5 FSS Programming Guide

12.4.1.5.1 FSS Initialization Sequence

Initialization steps:

- Configure the main boot parameters for FSS (see Section 12.4.1.4.2.1):
  - Select the boot block to be used.
  - Select the size of the boot block to be used.
- Enable FSS in PSC.
- Configure the FSS0_OSPI0.
- Enable the FSS0_OSPI0 in PSC. For more information about OSPI configuration, please see *Octal Serial Peripheral Interface (OSPI)*.

12.4.1.5.2 FSS Power Up/Down Sequence

There are two PSC controls for the FSS: for FSS0 itself and for FSS0_OSPI0. The CPU enables the FSS0_OSPI0 before using the FSS. Software should ensure the FSS0_OSPI0 is enabled prior to FSS transactions.

Normal Power Down Sequence:

- Block any new transaction.
- Power down the FSS0_OSPI0.
- In the event when the FSS0_OSPI0 is powered down, the FSS can then be powered down.

12.4.2 Octal Serial Peripheral Interface (OSPI)

This section describes the Octal Serial Peripheral Interface (OSPI) module for the device.

12.4.2.1 OSPI Overview

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

shows the OSPI allocation across device domains.

Figure 12-160 shows the OSPI module overview.

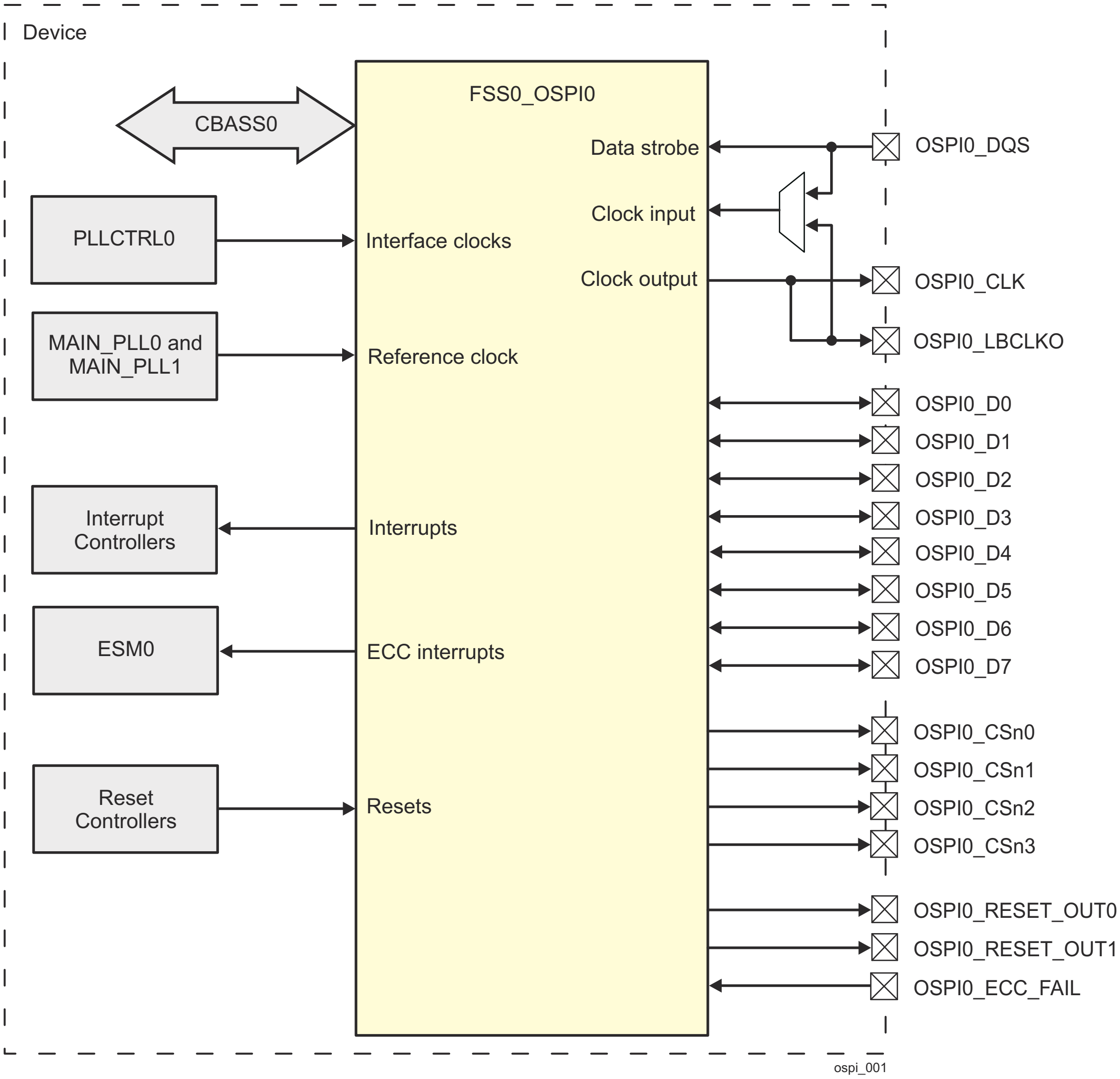

Figure 12-160. OSPI Overview

12.4.2.1.1 OSPI Features

The OSPI module has the following features:

- Support for single, dual, quad (QSPI mode) or octal I/O bus widths.
- Memory mapped ‘direct’ mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Support for DDR Mode and DTR protocol (including Octal DDR protocol with DQS for Octal-SPI devices)
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Supports BOOT mode.
- Bidirectional CRC on Multiple-SPI interface.
- Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.
- Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash.

12.4.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.4.2.2 OSPI Environment

The FSS0_OSPI0 module is hereinafter referred to as OSPI module.

This section describes the OSPI external connections (environment).

The OSPI module is primarily intended for fast booting from Octal- and Quad-SPI flash memories. Figure 12-161 shows a typical connection of the OSPI module to an external Octal-SPI flash memory.

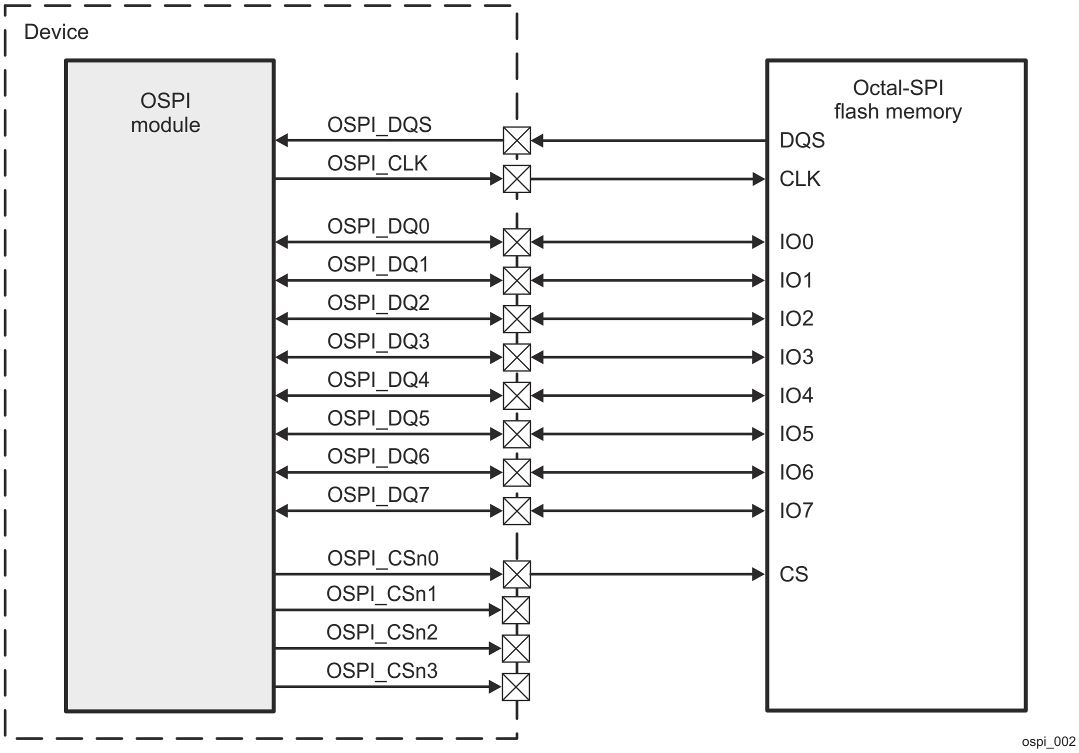

Figure 12-161. OSPI Connected to an External Octal-SPI Flash Memory

Table 12-178 lists and describes the FSS0_OSPI I/O signals.

Table 12-190. OSPI I/O Signals

Module Pin	Device Level Signal	I/O[(1)]	Description	Module Pin Reset Value[(2)]
			FSS0_OSPIi[(4)]	
DQ0	OSPIi[(4)]_D0	IO	FSS0_OSPIi[(4)] data input/output 0	HiZ
DQ1	OSPIi[(4)]_D1	IO	FSS0_OSPIi[(4)] data input/output 1	HiZ
DQ2	OSPIi[(4)]_D2	IO	FSS0_OSPIi[(4)] data input/output 2	HiZ
DQ3	OSPIi[(4)]_D3	IO	FSS0_OSPIi[(4)] data input/output 3	HiZ
DQ4	OSPIi[(4)]_D4	IO	FSS0_OSPIi[(4)] data input/output 4	HiZ
DQ5	OSPIi[(4)]_D5	IO	FSS0_OSPIi[(4)] data input/output 5	HiZ
DQ6	OSPIi[(4)]_D6	IO	FSS0_OSPIi[(4)] data input/output 6	HiZ
DQ7	OSPIi[(4)]_D7	IO	FSS0_OSPIi[(4)] data input/output 7	HiZ
N_SS_OUT0	OSPIi[(4)]_CSn0	O	FSS0_OSPIi[(4)] external flash device chip select 0	0x1
N_SS_OUT1	OSPIi[(4)]_CSn1	O	FSS0_OSPIi[(4)] external flash device chip select 1	0x1
N_SS_OUT2	OSPIi[(4)]_CSn2	O	FSS0_OSPIi[(4)] external flash device chip select 2	0x1
N_SS_OUT3	OSPIi[(4)]_CSn3	O	FSS0_OSPIi[(4)] external flash device chip select 3	0x1
OCLK	OSPIi[(4)]_CLK	O	FSS0_OSPIi[(4)] clock output for the external flash device	0x0
	OSPI0_LBCLKO	O	FSS0_OSPIi[(4)] external loopback output	0x0

Table 12-190. OSPI I/O Signals (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
DQS	OSPIi[4]_DQS	I[3]	FSS0_OSPIi[4] data strobe / external loopback input	Don't care
RESET_OUT0	OSPIi[4]_RESET_OUT0	O	FSS0_OSPIi[4] reset output 0 for the external flash device	0x1
RESET_OUT1	OSPIi[4]_RESET_OUT1	O	FSS0_OSPIi[4] reset output 1 for the external flash device	0x1
ECC_FAIL	OSPIi[4]_ECC_FAIL	I	FSS0_OSPIi[4] ECC status from the external flash device	0x1

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the loopback clock is defined by CTRLMMR_MCU_OSPIn_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.

(4) i represents an OSPI instance. See the device datasheet for available domains and OSPI instances.

Table 12-179 describes the OSPI I/O connectivity to external SPI devices.

Table 12-191. OSPI I/O Connectivity to External SPI Devices

Module Pin	I/O[1]	Description			
		4-pin[1] SPI - Single Read/Write (SIO) (DATA_XFER_TYPE_EXT_MODE_FLD=0x0)	4-pin[1] SPI - Dual Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x1)	6-pin[1] SPI - Quad Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x2)	11-pin[1] SPI - Octal Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x3)
DQ0	IO	Used as SPI data output	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0
DQ1	IO	Used as SPI data input	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1
DQ2	IO	Not used	Not used	Used as SPI data input 2 Used as SPI data output 2	Used as SPI data input 2 Used as SPI data output 2
DQ3	IO	Not used	Not used	Used as SPI data input 3 Used as SPI data output 3	Used as SPI data input 3 Used as SPI data output 3
DQ4	IO	Not used	Not used	Not used	Used as SPI data input 4 Used as SPI data output 4
DQ5	IO	Not used	Not used	Not used	Used as SPI data input 5 Used as SPI data output 5
DQ6	IO	Not used	Not used	Not used	Used as SPI data input 6 Used as SPI data output 6
DQ7	IO	Not used	Not used	Not used	Used as SPI data input 7 Used as SPI data output 7
DQS	I[2]	Not used	Not used	Not used	Data strobe or loopback clock input
OCLK	O	Output clock or loopback clock output. For more information, see Table 12-178.			
N_SS_OUT0	O	External SPI device chip-select 0			
N_SS_OUT1	O	External SPI device chip-select 1			
N_SS_OUT2	O	External SPI device chip-select 2			
N_SS_OUT3	O	External SPI device chip-select 3			
RESET_OUT0	O	External SPI device reset 0			
RESET_OUT1	O	External SPI device reset 1			
ECC_FAIL	I	External SPI device ECC failure indication			

(1) This is the pin count at the external SPI flash memory side.

(2) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the loopback clock is defined by CTRLMMR_MCU_OSPIn_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.

Note

For OSPI0_CLK, OSPI0_LBCLKO, and OSPI0_DQS signals to work properly, the RXACTIVE bit of the appropriate registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.2.4 OSPI Functional Description

12.4.2.4.1 OSPI Block Diagram

Figure 12-162 shows the OSPI module block diagram.

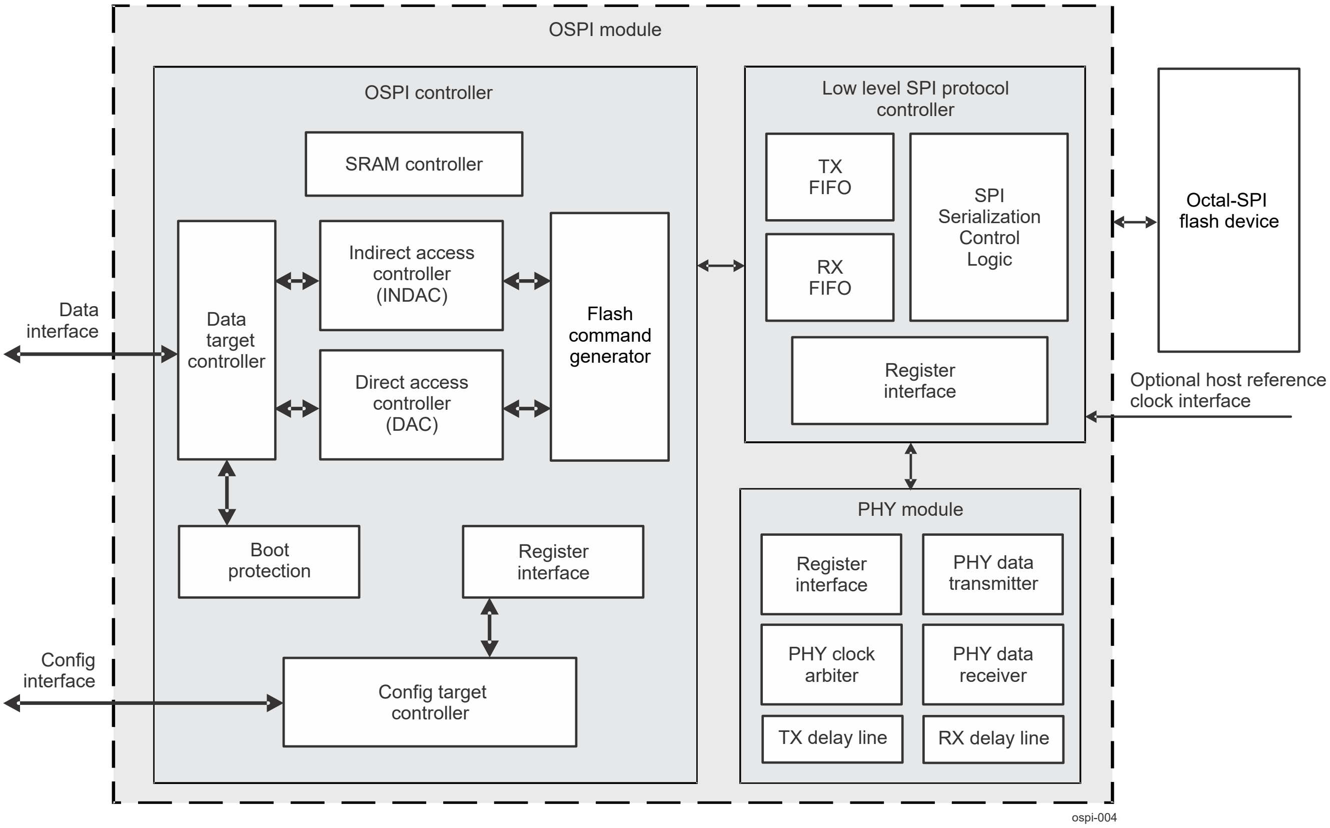

Figure 12-162. OSPI Block Diagram

The OSPI module is composed of three main blocks. The first one is the OSPI controller, the second one is the low level SPI protocol controller, and the third one is the integrated PHY.

The OSPI module has the following two target interfaces:

- Data target interface intended for data transfer.
- Configuration target interface intended for accessing the programmable set of registers.

12.4.2.4.1.1 Data Target Interface

The data interface is used for data transfer to external flash devices in direct and indirect mode of operation. The data target controller validates incoming data accesses, responds to invalid requests, performs any required byte and halfword reordering, blocks writes that violate the programmed write protection rules (only for direct access) and forwards the transfer request to either the direct access controller (DAC) or the indirect access controller (INDAC).

The data interface bus is 32-bits wide. Therefore only byte, halfword and word accesses are permitted. When the controller is configured to work in SPI Octal DDR Mode or Octal DDR Protocol (where 2 bytes are collected within single SPI clock cycle what exceeds the size of 1 byte transfer request), 8 bit transfer size is not allowed.

Note

Cache line wrap accesses over the data target port should be word aligned.

Data target port doesn't support cache line wrap bursts of 128 bytes.

12.4.2.4.1.2 Configuration Target Interface

The configuration interface is used to configure the OSPI module and perform software controlled flash accesses using the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register (for more information refer to Section 12.4.2.4.11 , *OSPI Software Triggered Instruction Generator (STIG)*). Depending on the address it routes the incoming interconnect transfer to the Low level SPI protocol controller or to the ECC aggregator. The configuration port is also used to interact with the OSPI configuration and SRAM ECC registers.

Note

The configuration interface supports only 32-bit accesses. For single byte or halfword manipulations software should perform read-modify-write operations.

12.4.2.4.1.3 OSPI Clock Domains

The OSPI module has two main clock sources for the Octal-SPI controller.

- For interface clocks
- For reference clock

The source for the interface clocks corresponds to the configuration and data buses. The data bus clock (OSPI_HCLK) is the main system clock used to transfer data over the data bus between a controller on the system interconnect and the OSPI module. The data bus clock also drives the internal OSPI SRAM. The configuration bus clock (OSPI_PCLK) is used to access the OSPI configuration register and perform basic configuration and for interrupt handling. The OSPI reference clock (OSPI_RCLK) drives the SPI transmit and receive logic in the OSPI module. It is also used to generate the output SPI protocol clock (OSPI_OCLK) and for oversampling of the input data. Using the reference clock (OSPI_RCLK) allows the OSPI module to decouple the frequency of the SPI flash device from the device system clocks, thereby providing more flexible clocking solution.

Note

There is no particular clock ratio requirement between configuration (OSPI_PCLK) and data bus (OSPI_HCLK) clocks.

12.4.2.4.2 OSPI Modes

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

The OSPI module supports four SPI modes. These modes are defined through the OSPI_FLASH_CFG_CONFIG_REG[1] SEL_CLK_POL_FLD and OSPI_FLASH_CFG_CONFIG_REG[2] SEL_CLK_PHASE_FLD bits. The SEL_CLK_POL_FLD bit defines the clock polarity and the SEL_CLK_PHASE_FLD bit defines the data launch and data capture relation to the OSPI clock edges. Table 12-180 gives a brief description of these modes.

Table 12-192. OSPI Modes

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
0	0	0	Clock inactive state: low

Table 12-192. OSPI Modes (continued)

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
			Data launch edge: clock falling edge
			Data capture edge: clock rising edge
1	0	1	Clock inactive state: low
			Data launch edge: clock rising edge
			Data capture edge: clock falling edge
2	1	0	Clock inactive state: high
			Data launch edge: clock rising edge
			Data capture edge: clock falling edge
3	1	1	Clock inactive state: high
			Data launch edge: clock falling edge
			Data capture edge: clock rising edge

Octal flash devices provide DQS signal which allows source synchronous capture, but for Quad flash devices the OSPI module has a loopback mode. In this loopback mode the clock, looped back at board level, is used for registering the input data, and the edge used is same as the launch edge, thus giving a full cycle path (for more information, see Section 12.4.2.4.2.1 , *Read Data Capture*).

12.4.2.4.2.1 Read Data Capture

Figure 12-163 shows the Read Data Capture Logic in the OSPI module.

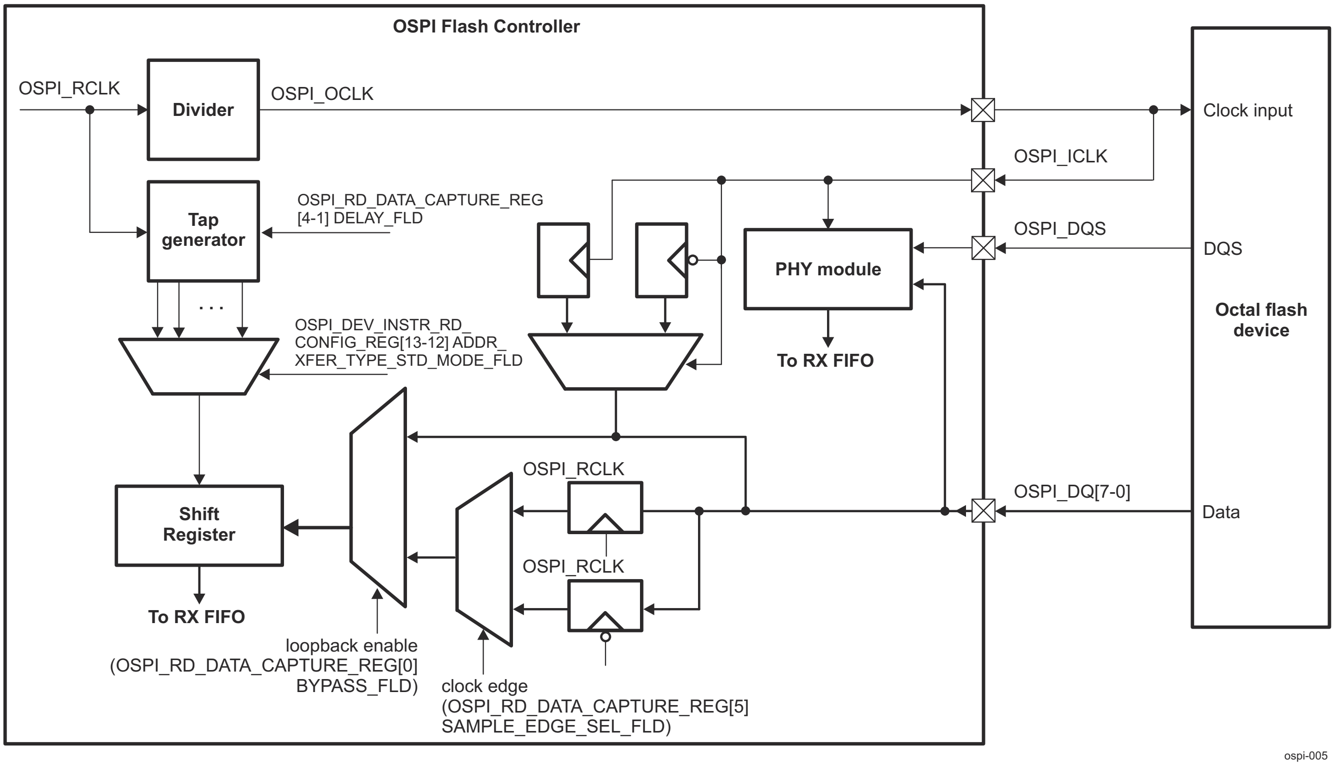

Figure 12-163. Read Data Capture Logic

The PHY module includes a DLL which allows adjustment of the sampling edge with respect to the incoming data to achieve maximum frequency. There are three sources for the sampling signal:

- The reference clock

- Output SPI clock external loopback
- The DQS (only available in Octal Flash devices)

The loopback mode (only for Quad flash devices) can work in two cases. The first one is when OSPI_FLASH_CFG_CONFIG_REG[2] SEL_CLK_PHASE_FLD=0. When SEL_CLK_PHASE_FLD=1 there aren't enough clock falling edges for the register pipeline to catch the last data driven, thus causing a functional failure. Additionally, since the capture edge is falling edge, it gives a full cycle input path only in SPI mode 0, that is when SEL_CLK_POL_FLD=0 and SEL_CLK_PHASE_FLD=0. Thus SPI mode 0 is the first of two modes that support high MHz operation (greater than 50 MHz). The second mode is when SEL_CLK_PHASE_FLD=1 and SEL_CLK_PHASE_FLD=1 (SPI mode 3). In this case the missing clock falling edge is compensated inside the OSPI controller when using the incorporated PHY module by inverting the loopback clock.

The loopback mode is enabled by writing 0x0 to OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[0] BYPASS_FLD. The taps are selected by programming OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD field. The taps delay the read data capturing logic by the programmed number of OSPI_RCLK cycles.

12.4.2.4.2.1.1 Mechanisms of Data Capturing

There are two mechanisms of data capturing in the OSPI module. They can be combined in some parts to ensure reliable sampling solution independent on the system requirements and the controller configuration. The mechanisms are as follows:

- Data capturing mechanism using taps
- Data capturing mechanism using PHY module.

12.4.2.4.2.1.2 Data Capturing Mechanism Using Taps

This section describes the data capturing mechanism where sampling point is adjusted for one of the reference clock edges inside divided OSPI clock.

After POR, the adapted loopback clock circuit and the OSPI_RCLK delay register line both wake in a disabled state. The OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG register provides the control for the mechanism using taps.

OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[5] SAMPLE_EDGE_SEL_FLD bit selects the edge of the reference clock, on which data outputs from flash memory are sampled.

OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD bit field controls the additional number of read data capture cycles (this is the fast reference clock, running at least x4 of the device clock) that should be applied to the internal read data capture circuit. The large clock-to-out delay of the flash memory together with trace delays as well as other device delays may impose a maximum flash clock frequency which is less than the flash memory device itself can operate at. To compensate, software shall set this register to a value that guarantees robust data captures.

12.4.2.4.2.1.3 Data Capturing Mechanism Using PHY Module

PHY module is responsible for data capturing. More detailed description of all internal PHY sampling mechanisms is included in *Read Data Capturing by the PHY Module*.

12.4.2.4.2.1.4 External Pull Down on DQS

Per the OSPI protocol, the FLASH device drives DQS while CS is asserted. When CS is not asserted the FLASH device presents HiZ on DQS. When configured to use DQS, the controller uses the DQS as a clock, which samples the incoming data into a FIFO. Noise on the DQS when it is HiZ can cause spurious false triggering of the FIFO and filling it with invalid data. There is no way to clear this data except to reset the OSPI module.

To avoid this issue, it is recommended to add a pull down on the DQS line.

During device wakeup, before the IO ring is configured properly, the CS to the FLASH device is HiZ. Depending on the actual level of the CS line the FLASH device might drive the DQS High, Low or HiZ. A pull down on DQS forces the DQS input to Low, but the DQS might still be High or in the presence of noise there might be transitions between Low and High. This again can cause the same issue of capturing garbage data in the Controller FIFO.

To avoid this issue it is recommended to release the OSPI from reset only after the IO ring is configured properly.

12.4.2.4.3 OSPI Power Management

Note

The OSPI module does not provide any hardware signal for busy or idle status. Software need to ensure that the OSPI module is idle before clocks can be shut off by reading the OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit.

OSPI_PCLK and OSPI_HCLK share the same clock stop request/acknowledge and clock enable/acknowledge interface.

12.4.2.4.4 Auto HW Polling

The OSPI controller is capable of automatically testing the Flash device busy bit to guarantee no reads or writes are ignored by the flash when it is busy burning in programmed data.

At the end of a programming transaction, the Flash device goes into a burn-in state and becomes busy.

When Auto HW Polling is enabled, the OSPI controller keeps track of programming transactions and will initiate a Flash status read polling transactions automatically, until Flash indicates it is not busy, before any additional data read or programming operations are sent to the flash device. See OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG register and the associated registers.

The OSPI controller requires that the OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[23-16] POLL_COUNT_FLD field should always be set with values greater or equal to 3 (>=3).

12.4.2.4.5 Flash Reset

OSPI provides Flash reset out ports. These ports are active low and controlled thru OSPI_FLASH_CFG_CONFIG_REG register.

12.4.2.4.6 OSPI Memory Regions

Note

For more information about the memory space, see *FSS Memory Regions*.

12.4.2.4.7 OSPI Interrupt Requests

The OSPI module generates three interrupts. The ECC interrupts (FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_0 and FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_0) are generated by the OSPI ECC aggregator.

The other interrupt (FSS0_OSPI_0_OSPI_LVL_INTR_0) is generated by the OSPI module.

Table 12-181 lists the event flags and the corresponding mask bits of the sources which can cause interrupts.

Table 12-193. OSPI Events

Event Flag	Event Mask	Description
OSPI_FLASH_CFG_IRQ_STATUS_REG[0] MODE_M_FAIL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[0] MODE_M_FAIL_MASK_FLD	Event Flag and Event Mask for the OSPI Interrupts.
OSPI_FLASH_CFG_IRQ_STATUS_REG[1] UNDERFLOW_DET_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[1] UNDERFLOW_DET_MASK_FLD	

Table 12-193. OSPI Events (continued)

Event Flag	Event Mask	Description
OSPI_FLASH_CFG_IRQ_STATUS_REG[2] INDIRECT_OP_DONE_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[2] INDIRECT_OP_DONE_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[3] INDIRECT_READ_REJECT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[3] INDIRECT_READ_REJECT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[4] PROT_WR_ATTEMPT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[4] PROT_WR_ATTEMPT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[5] ILLEGAL_ACCESS_DET_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[5] ILLEGAL_ACCESS_DET_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[6] INDIRECT_XFER_LEVEL_BREACH_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[6] INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[7] RECV_OVERFLOW_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[7] RECV_OVERFLOW_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[8] TX_FIFO_NOT_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[8] TX_FIFO_NOT_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[9] TX_FIFO_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[9] TX_FIFO_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[10] RX_FIFO_NOT_EMPTY_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[10] RX_FIFO_NOT_EMPTY_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[11] RX_FIFO_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[11] RX_FIFO_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[12] INDRD_SRAM_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[12] INDRD_SRAM_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[13] POLL_EXP_INT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[13] POLL_EXP_INT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[14] STIG_REQ_INT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[14] STIG_REQ_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[16] RX_CRC_DATA_ERR_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[16] RX_CRC_DATA_ERR_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[17] RX_CRC_DATA_VAL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[17] RX_CRC_DATA_VAL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[18] TX_CRC_CHUNK_BRK_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[18] TX_CRC_CHUNK_BRK_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[19] ECC_FAIL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[19] ECC_FAIL_MASK_FLD	

Table 12-193. OSPI Events (continued)

Event Flag	Event Mask	Description
OSPI_ECC_SEC_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_SEC_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_SEC_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	Event Flag and Event Mask for the ECC Interrupts.
OSPI_ECC_DED_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_DED_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_DED_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	
OSPI_ECC_AGGR_STATUS_SET[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_SET[0] PARITY	
OSPI_ECC_AGGR_STATUS_SET[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_SET[1] TIMEOUT	
OSPI_ECC_AGGR_STATUS_CLR[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_CLR[0] PARITY	
OSPI_ECC_AGGR_STATUS_CLR[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_CLR[1] TIMEOUT	

12.4.2.4.8 OSPI Data Interface

12.4.2.4.8.1 Data Interface Address Remapping

The incoming data interface address, by default, maps directly to the address sent serially to the FLASH device. If the FLASH device has a 24-bit address, then the 24 LSB's of the data address is forwarded. A remap feature is available to remap all incoming data addresses to ADDRESS + N, where N is the value stored in the OSPI_FLASH_CFG_REMAP_ADDR_REG[31-0] VALUE_FLD bit field. It is enabled via the OSPI_FLASH_CFG_CONFIG_REG[16] ENB_AHB_ADDR_REMAP_FLD bit. This feature could be used when software needs to move boot code to another FLASH region.

12.4.2.4.8.2 Write Protection

In order to protect the FLASH device, a software controlled write protection feature is supported. Any data write detected (by using DAC), pointing to an area of the FLASH that is protected, is not permitted.

A programmable region of the FLASH device, defined as a number of FLASH 'blocks' starting from a particular block number can be protected. Three programmable registers are provided. The first OSPI_FLASH_CFG_LOWER_WR_PROT_REG register defines the FLASH block that is located at the bottom of the region to be protected. The second OSPI_FLASH_CFG_UPPER_WR_PROT_REG register defines the FLASH block that is located at the top of the region to be protected. The third OSPI_FLASH_CFG_WR_PROT_CTRL_REG register is a control register consisting of 2 bits. The OSPI_FLASH_CFG_WR_PROT_CTRL_REG[0] INV_FLD bit allows software to invert the region that is being protected, causing the programmed region to become the only areas of FLASH memory that is not protected from writes. The OSPI_FLASH_CFG_WR_PROT_CTRL_REG[1] ENB_FLD bit is the write protection enable bit. When this bit is set to 0, the FLASH device is unprotected.

For implementation, the data interface must map the incoming address into its associated FLASH block. A block can be between 1 and 65 KB, programmed via the OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG register.

12.4.2.4.8.3 Access Forwarding

For legal accesses, the data interface will forward all accesses to one of two access controllers - the direct access and the indirect access controllers. Assuming DAC has been enabled via the

OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTRL_FLD bit, then by default all accesses will be forwarded to this controller. Before any accesses can be forwarded to INDAC, it must first be configured by software. This process is fully explained in Section 12.4.2.4.10 , *OSPI Indirect Controller (INDAC)*. If DAC is disabled, any incoming access that cannot be forwarded to INDAC will be completed immediately with an error. If DAC is enabled, the same access will be forwarded and serviced by DAC.

12.4.2.4.9 OSPI Direct Access Controller (DAC)

Direct access refers to the operation where data interface accesses directly trigger a read or write to FLASH memory. It is memory mapped and can be used to both access and directly execute code from external FLASH memory. Any incoming access that is not recognized as being within the programmable indirect trigger region is assumed to be a direct access and will be serviced by the DAC. Note that accesses that use DAC do not use the embedded SRAM. The data transfer stops when read or write burst is carried out. The amount of wait states applied will be dependent on the latency through the controller. Latency is kept to a minimum when the use of XIP read instructions are enabled (see OSPI_FLASH_CFG_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD and OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD bits).

12.4.2.4.10 OSPI Indirect Access Controller (INDAC)

12.4.2.4.10.1 Indirect Read Controller

The aim of the indirect mode of operation is to read significant numbers of bytes from FLASH memory without requiring a data interface access to trigger it. Instead indirect operations are controlled and triggered by software via specific control/configuration Indirect Read Transfer registers (OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG, OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG, OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG, and OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG). This block will communicate with an embedded low level SPI protocol state machine module to perform an efficient and optimized FLASH read burst, placing the read data into the local SRAM module ready for fast and low latency delivery to any external controller.

By default, the Indirect Read controller is disabled. Before enabling it, software must configure how much data is required and the start address. The start address and total number of bytes to be fetched is defined in OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG and OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. For more information refer to Section 12.4.2.4.10.3 , *Indirect Access Queuing*.

The total number of bytes to read in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the size of requests. In the case of SRAM overrun, the controller will back pressure FLASH reads until space becomes available in the SRAM. Back pressuring the reads on the SPI interface is handled by completing any current read burst, waiting until space in the SRAM becomes available and then issuing a new read burst at the address where the previous terminated burst ended.

An external controller will be able to fetch the data that the controller has read from external FLASH memory by issuing data interface reads to the OSPI module. The address of the incoming read access must be in the range of indirect trigger address programmed via the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register to indirect trigger address + 2**(indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the indirect range to grant SRAM as source. Each valid Indirect Read will cause the internal SRAM to be popped, thereby decoupling the incoming read access address from the FLASH address – that is not direct mapped. Therefore the indirect trigger address does not have any relationship with the FLASH address. It is just to indicate that data should take the SRAM as source instead of the FLASH memory array after triggering of any valid Indirect Read. The FLASH address for

Indirect Read is taken from the OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG register. Assuming the requested data is present in the SRAM at the point the data interface access is received by the OSPI module, then the data will be fetched from the SRAM and the response to the read burst will be achieved with minimum latency. Once the data has been read from the SRAM, the OSPI module will free up the associated resource in the SRAM.

If a read access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a read access is received whose address is within the range described above but the requested data is not immediately present in the SRAM then wait states will be applied until the data has been read from FLASH and pushed to the SRAM.

If a read burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface reads until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final read, the external controller may issue a 16-bit (Halfword) or byte access to complete the transfer. It is also permitted for the external controller to always issue a 32-bit Word read on the last indirect access. The controller will pad the upper bits of the response with zero. The current expectation is that the SRAM will be kept fairly full while the read operation is carried out. The fill level of the SRAM is directly readable by software reading the OSPI_FLASH_CFG_SRAM_FILL_REG register.

An indirect operation may be cancelled at any time by setting 1 to OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via configuration registers and then decide for itself when the data should be fetched from the local SRAM. The fill level watermark register (see OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG register) is provided. When the SRAM fill level passes this watermark, an interrupt is generated. If the watermark value is > 0, the watermark interrupt is also generated when the final byte of data has been read by the OSPI module and placed in the SRAM, even if the actual SRAM fill level has not risen above the watermark. This last feature is useful to avoid software tracking how much data has been read and resetting the watermark value for the last few bytes of an indirect read transfer.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an Indirect Read operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit starts an indirect read operation. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[2] RD_STATUS_FLD bit is available to check the status.

12.4.2.4.10.1.1 Indirect Read Transfer Process

The following sequence can be followed:

1. Setup OSPI_FLASH_CFG_CONFIG_REG register.
2. Setup the indirect transfer's FLASH start address in the OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer's trigger address in the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register.

5. Setup the indirect transfer's trigger address range in the OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG register.
6. If the watermark interrupt feature is to be used, set the OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level increases beyond the watermark level. Setting the watermark can be useful indication to software when to read the next part of the indirect read transfer. Note that if the watermark is set to a value other than zero, the watermark interrupt will always trigger once the final byte of indirect transfer has been fetched and placed in the embedded SRAM, even if the watermark value is higher than the actual completed fill level.
7. Trigger Indirect Read access by setting the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit to 1.
8. If the watermark interrupt feature is to be used, wait for watermark interrupt. Else poll the SRAM fill level via the OSPI_FLASH_CFG_SRAM_FILL_REG register to decide when sufficient data is in the SRAM to trigger data fetches.
9. Read the expected amount of data from SRAM. If there is still more data to fetch in order to complete the indirect read transfer, then loop back to step 8. Otherwise continue to step 10.
10. The completion status of the Indirect Read operation can be polled via the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD bit.
11. An Indirect Complete interrupt will be generated when the Indirect read operation has completed.

12.4.2.4.10.2 Indirect Write Controller

The aim of the indirect mode of operation is to perform bulk transfer of data from the processor into a FLASH memory in the most efficient manner. The fewest possible write cycles inside the FLASH device will be carried out for the indirect transfer, thus maximizing the life of the device. Indirect write operation can be thought of from a software perspective as the inverse of the indirect read. It is controlled and triggered by software via specific control/configuration Indirect Write Transfer registers (for more information see the following registers: OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG, OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG, OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG, and OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG). This block will await delivery of the write data via the external data interface controller, placing it in the local SRAM before communicating with the existing legacy SPI core to perform an efficient and optimized FLASH write burst.

By default, the indirect write controller is disabled. Before enabling it, the software must configure how much data is required and the start address. The start address and total number of bytes to be written is defined in OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG and OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. The Indirect write queuing is very similar to indirect read queuing. For more information refer to Section 12.4.2.4.10.3 , *Indirect Access Queuing*.

The total number of bytes to write in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the amount of data that can be accepted from the external controller. In the case of an SRAM overrun, the controller will back pressure the data interface with wait states. Note the fill level of the SRAM is readable via programmable OSPI_FLASH_CFG_SRAM_FILL_REG register and this can be used to avoid this situation.

An external controller will provide the write data and will transfer this to the OSPI module by issuing data interface writes. The address of the incoming write access must be in the range of Indirect trigger address programmed via the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register to Indirect trigger address + 2**(Indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the Indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the Indirect Range to grant SRAM as source. Each write will cause the internal SRAM to be pushed, thereby decoupling the incoming write access address from the FLASH address – that is not direct mapped. Therefore Indirect trigger address does not have any relationship with FLASH address. It is just to indicate that data should take SRAM as source instead of FLASH Memory array after triggering of any valid Indirect Write. The FLASH address for Indirect Write is taken from the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register. Assuming the SRAM is not full at the point the data interface access is received by the OSPI module, then the data will be pushed to the SRAM with minimum latency.

If a write access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a write access is received whose address is within the range described above but the SRAM is full then wait states will be applied until some or all of the data has been pushed from the SRAM to the FLASH.

If a write burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller, and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface writes until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final write, the external controller may issue a 32-bit word, 16-bit (halfword) or a byte access to complete the transfer. If the number of bytes to write is less than 4 on the last transfer, the controller is still permitted to issue a 32-bit transfer. In these cases, the extra bytes are discarded by the controller.

When the SRAM holds a number of bytes equal to or greater than the size of a FLASH page (which itself is programmed into the OSPI module, with a default of 256 bytes) or when the SRAM holds all remaining bytes of the currently executing indirect transfer, the OSPI module will initiate a write burst to the flash command generator.

An indirect operation may be cancelled at any time by setting 1 to the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via the configuration registers and then decide for itself when the data should be written to the local SRAM. The fill level watermark register (see OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG register) is provided. When the SRAM fill level falls below this watermark, an interrupt is generated.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an indirect write operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit starts an indirect write operation. The OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[2] WR_STATUS_FLD bit is available to check the status.

12.4.2.4.10.2.1 Indirect Write Transfer Process

The following sequence can be followed:

1. Setup OSPI_FLASH_CFG_CONFIG_REG register.
2. Setup the indirect transfer’s FLASH start address in the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer’s trigger address in the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register.
5. Setup the indirect transfer's trigger address range in the OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG register.

6. It is functionally valid for software to simply write all the data to the SRAM in one block transfer. However, if the total number of bytes to write is greater than the size of the partitioned SRAM, then it is quite likely the SRAM will become full causing the OSPI to back-pressure the system data bus for a considerable time. This time is based on the FLASH data-rate and the page-write time of the device. To avoid sending all the write data in one block transfer, software can make use of the watermark interrupt to identify a convenient time to send data a page at a time to the SRAM module. Alternatively, software can poll the SRAM fill level register directly to identify how empty the SRAM is at any one time in order to make a judgment as to when the most practical time to send the next part of the transfer.
7. If the watermark interrupt feature is to be used, set the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level falls below the watermark. The watermark should be set to a number between zero and a page size. That is if the page size is 256 bytes, then setting the watermark to a value between 10 and 250 is reasonable and will cause the interrupt to trigger when the fill level drops below the programmed number. Setting the watermark can be useful to provide an indication to software when to write the next page of data to the SRAM.
8. Trigger Indirect Write access by setting OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit.
9. If the remaining number of bytes still to be transferred into the SRAM for the current indirect transfer is greater than a FLASH page, then write 1 FLASH page worth of data to the SRAM. Otherwise send the remaining data from the indirect transfer to SRAM.
10. If all the data in the indirect transfer has now been sent to the SRAM, then go to 12 and await indirect complete status. Otherwise if there is more data still to be transferred then either:
    - If the watermark interrupt feature is being used, then wait for watermark interrupt.
    - Alternatively the SRAM fill level can be interrogated to identify a convenient time to send more data.
11. Loop back to 9.
12. Optional: The completion status of the Indirect write operation can be polled via OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD.
13. An Indirect Complete interrupt will be generated when the Indirect write operation has completed.

12.4.2.4.10.3 Indirect Access Queuing

Software is permitted to queue up to two indirect transfers for both the indirect write controller and the indirect read controller. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. Any attempt to queue more than two operations will cause an interrupt to be generated. To take advantage of this feature, software should attempt to keep both indirect programming slots full at all times.

From the software perspective, indirect access queuing is achieved by triggering bit 0 of the indirect transfer control register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit) twice in short succession. The indirect number of bytes register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG register) and the indirect FLASH start address register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register) must be setup with the relevant transfer data before START_FLD bit can be triggered for each transfer. Since these registers will change regularly, the hardware must keep sampled versions of these registers for the duration of the indirect transfer.

The internal register block will only issue an indirect start trigger to the key underlying datapath blocks one at a time. There are 2 independent datapath blocks in the indirect access controller that will receive and independently sample this information. The first is the datapath block on the data bus side of the SRAM. For indirect reads, this is a read interface, for indirect writes, it is a write interface. The second is the datapath block on the FLASH side of the SRAM. For indirect reads, this is a write interface, for indirect writes, it is a read interface. Both blocks will process the indirect transfers at different times. For example, for an indirect read operation, the datapath block on the FLASH side of the SRAM will be able to start processing the second queued transfer as soon as the last byte of the first transfer has been written to the SRAM. Before commencing the second transfer, this block must resample the OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG and OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG registers. Similarly, the datapath block on the bus side will resample the same registers locally when it has forwarded all the FLASH data associated with the first indirect transfer from the SRAM onto the data bus.

12.4.2.4.10.4 Consecutive Writes and Reads Using Indirect Transfers

It is permitted for software to trigger an indirect read operation while an indirect write operation is in progress. Similarly it is permitted to trigger an indirect write while an indirect read operation is in progress. Indirect write operations will take overall precedence.

12.4.2.4.10.5 Accessing the SRAM

The SRAM depth is separated in two segmets. The lower segment is reserved for indirect read use. The upper segment is for indirect write use only. The size of each segment is programmable via the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG register. This feature allows to allocate how many bits of the SRAM address bus are allocated to indirect read. By default, this is set so that exactly half of the SRAM is portioned for use by the indirect read controller. To ensure the read data bus is not directly fed by the SRAM read data through combinatorial logic, an extra bank of holding registers is included in the indirect read data path. These registers act as an extra location to be added to the allocated number of SRAM locations for indirect read.

To illustrate how the SRAM (and the extra bank of holding registers) can be allocated between indirect read and write, the following example is provided. The depth of the SRAM in this example is configured to be 8 bits. This is equal to 256 locations.

- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x00, then 256 locations are allocated to indirect writes and 1 location to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x01, then 255 locations are allocated to indirect writes and 2 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x02, then 254 locations are allocated to indirect writes and 3 locations to indirect reads.
- And so on until.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFD, then 3 locations are allocated to indirect writes and 254 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFE, then 2 locations are allocated to indirect writes and 255 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFF, then 1 location is allocated to indirect writes and 256 locations to indirect reads.

Note

A value of 0xFF or 0x00 in the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG register should be avoided by software, as only the bottom 8 bits of the SRAM fill level are accessible through software (up to 255 limit) via the OSPI_FLASH_CFG_SRAM_FILL_REG register. If the fill level reaches 256 on either the indirect read or write side, it will appear when reading the Fill Level to be 0.

There are four SRAM sources that are arbitrated and muxed onto the single SRAM port. Up to three sources can access this port at any one time. The sources are described as follows:

- Indirect Write, Write source. This is located on the data bus side of the SRAM.
- Indirect Write, Read source. This is located on the FLASH side of the SRAM.
- Indirect Read, Write source. This is located on the FLASH side of the SRAM.
- Indirect Read, Read source. This is located on the data bus side of the SRAM.

A fixed priority arbitration scheme is implemented. Table 12-182 shows priority allocated to these sources.

Table 12-194. SRAM Access Priority

SRAM Access Priority		
Indirect Write	Write to SRAM (from System Data Bus)	3rd (exclusive with Data Bus Read Request)
	Read from SRAM (from OSPI Module)	2nd
Indirect Read	Write to SRAM (from OSPI Module)	1st
	Read from SRAM (from System Data Bus)	3rd (exclusive with Data Bus Write Request)

Note

With the exception of the write port during an Indirect Read operation (on the FLASH side of the SRAM), the logic driving all four sources must not assume single cycle completion. Writes to the SRAM during an indirect read must be allowed to complete immediately to avoid data loss. Therefore this port is given maximum priority.

12.4.2.4.11 OSPI Software-Triggered Instruction Generator (STIG)

The DAC and INDAC are used to transfer data. In order to access the volatile and non-volatile configuration registers, the legacy SPI Status register, other status/protection registers as well as to perform ERASE functions, a separate software controller is required. The software triggered instruction generator (STIG) is controlled using the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register by setting up the command to issue to the FLASH device. This is a generic controller and can be used to perform any instruction that the FLASH device supports from the extended SPI protocol. Configuring of instructions which are not compliant with the specification of the FLASH devices could cause unpredicted behavior of the controller. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bits should be set different than OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit is used to trigger the command. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit is used by software to poll the status of the command execution. For reads, when the command has been serviced (OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit toggles from '1' to '0'), up to 8 bytes of read data will be placed in the OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG registers. For writes, the write data should be placed in the OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG registers.

The completion of the STIG request could be also checked by the corresponding interrupt. The occurrence of the interrupt indicates that the controller is ready for accepting a new STIG request. It is important to notice that completion of the STIG request is not equivalent to completion it on SPI side. For example, if STIG is configured to the command composed of data to transmit only, the data is taken from the corresponding STIG register fields and put into TX FIFO. Since all bytes to write are known, another STIG can be queued before serialization of the current one is completed.

There are some commands which require more data to read than 8 bytes (for example READ ID command). The additional STIG Memory Bank is implemented in order to accommodate these data if needed. The STIG Memory Bank (internal component of the controller) is controlled by the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit. If enabled, the number of bytes to read in the STIG is extended to 16 as defined in OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field. It should be noticed that there are very few commands (excluding Read Array ones which are not intended to handle effectively in STIG Mode but in Direct/Indirect Modes) which return more than 8 bytes to the controller. If the maximum number of bytes to Read using STIG in target application is less than 16, the depth of the STIG Memory Bank can be set smaller what will result in saving noticeable part of the area.

If number of bytes to Read in the STIG as defined in OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field exceeds the Memory Bank Depth, remaining data will overwrite the STIG Memory Bank locations starting from its first address. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG keep the last 8 bytes read from the Flash Device by STIG when Memory Bank is enabled. Therefore, for example if the user wants to get just a single byte from the last eight bytes from long continuous read SPI data chain, there is no need to access the STIG Memory Bank since data can be taken from suitable Flash Command Read Data register. In order to access more data, STIG Memory Bank data request should be triggered. It is controlled by the OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG and works analogously for triggering STIG from the functional standpoint.

OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[0] TRIGGER_MEM_BANK_REQ_FLD bit is used to trigger the command, bit OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[1] MEM_BANK_REQ_IN_PROGRESS_FLD is used by software to poll the status of the command execution. When MEM_BANK_REQ_IN_PROGRESS_FLD bit toggles from "1" to "0", the byte of data (OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[15-8] MEM_BANK_READ_DATA_FLD) from corresponding address (OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[28-20] MEM_BANK_ADDR_FLD bit field) is valid. The address should be set before triggering the STIG Memory Bank access. Each consecutive STIG access overwrites the previous one so that the data in the Bank always fit into byte index fetched by the last STIG access configured to use the Memory Bank (first incoming byte equals first address of the Memory Bank, second one equals the second address and so on).

12.4.2.4.11.1 Servicing a STIG Request

A STIG request will cause the OSPI Flash controller to interrogate the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register to determine what and how many bytes it should send to the FLASH device. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD field of this register indicate the instruction to be sent and is always pushed first. If there is an address to send, then the address (the size of which is also programmed in the same register) is sent next. The address itself is stored in the OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG register. If Mode bits are enabled by OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD bit. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field are being sent right after address. If OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD and OSPI_FLASH_CFG_CONFIG_REG[29] CRC_ENABLE_FLD are both enabled, STIG will replace XIP Mode bits (not applicable for CRC aware SPI interface) for automatically calculated address CRC byte. Therefore, to execute CRC aware STIGs (meaning the commands requiring sending address CRC byte), ENB_MODE_BIT_FLD bit should always be set. If there are any dummy cycles to send (the size of which is also programmed in OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register) then those are sent next. If there is data to write or read (the size of which is also programmed in OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register) then for the case of writes, up to 8 bytes can be sent (as stored in the Flash Command Write Data registers, OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG registers) next. In the read case, when the read data has been collected from the FLASH device, the OSPI Flash Controller stores that in the Flash Command Read Data Registers (OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG registers). Up to 8 bytes can be get if OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit is disabled or up to 512 when enabled. When the OSPI Flash controller starts to service a STIG request, it sets the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit to indicate a command execution is in progress. When the OSPI Flash controller is in the auto-polling state, servicing a STIG request is slightly different. Most of devices are largely inaccessible after a program operation until the device has completed that write. Some group of them has a possibility to suspend programming page. It can be controlled by the OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG[8] DEVICE_STATUS_VALID_FLD bit, which indicate active auto-polling phase. After requesting a STIG, the OSPI Flash Controller immediately issues appropriate OPCODE to Memory. During servicing a STIG (in auto-polling phase) the status bit of command execution remains steady and other parts of transfer such as ADDRESS or DUMMY BITS, and so forth, are disabled (to issued Program Suspend Command is needed OPCODE only).

There is a programmable option to add delay between every repetitive poll operation (delay is defined by OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field). This feature is implemented to free up SPI bandwidth if needed.

12.4.2.4.12 OSPI Arbitration Between Direct / Indirect Access Controller and STIG

When multiple controllers are active simultaneously, a simple fixed-priority arbitration scheme is used to arbitrate between each interface and access the external FLASH. The fixed priority is defined as follows, highest priority first.

- The Indirect Access Write
- The Direct Access Write
- The STIG
- The Direct Access Read
- The Indirect Access Read

12.4.2.4.13 OSPI Command Translation

Requests issued by the direct access controller, the indirect access controller or the STIG will be translated into a sequence of byte transfers to send downstream (before serialization to the FLASH device). These sequences depend on the requested transfer but an example of a typical 1-byte non sequential READ is shown below:

INSTRUCTION OPCODE -> ADDRESS -> Mode Byte -> Dummy Bytes -> 1 byte of don't care

For sequential accesses, an extra byte of data per read is pushed to the FLASH device on the back of the above sequence assuming it can be done so with no gap between each transferred byte.

When PHY mode is enabled and consequently no clock divider is configured, latency caused by multi domain synchronization may make an extra byte insufficient to avoid the transfer gap. To ensure the sequential access non-interrupted and keep the maximum performance of the controller, PHY Pipeline Mode is implemented. When enabled, number of don't care bytes is calculated based on the configuration.

The actual sequence sent to the FLASH device depends on the requested transfers, whether the transfer is non-sequential or sequential, whether the device has been configured in XIP mode and the state of the main Device Instruction Type programmable registers (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG).

For writes, the write enable latch (or WEL) within the FLASH device itself must be high before a write sequence can be issued. The OSPI Flash Controller will automatically issue the write enable latch command before triggering a write command via the direct or indirect access controllers (DAC/INDAC) – that is the user does not need to perform this operation. For increasing flexibility and performance user can turn off this feature by setting the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[8] WEL_DIS_FLD bit. The opcode for WREN is typically 0x06 and is common between devices.

When write requests from the direct or indirect access controllers are no longer being received and all outstanding requests have been sent, the FLASH device will automatically start the page program write cycle. Any incoming request at this time will be held in wait states until the cycle has completed. The OSPI Flash Controller will automatically poll the FLASH device legacy SPI status register to identify when the write cycle has completed. This is achieved by sending the RDSR opcode to the FLASH device and waiting until the device itself has indicated the write cycle has completed (until the Write in Progress bit has cleared to zero and the write enable latch bit has also cleared to zero or device is ready bit has set to one). The WREN and the RDSR device instructions are the only ones that are sent by the controller under the hood. For any other specific instruction that the user determines should be sent to the device (for example if the device needs to be unprotected before a write command is issued), these should be handled separately by issuing FLASH commands via the STIG.

There is an option to trigger HOLD or RESET feature on I/Os of the Flash Device. The HOLD one is generally common across the devices and takes an alternative function of DQ3 pin (applicable when device operates neither in Quad SPI mode nor DDR). The transfer can be hold and then resumed by dedicated software trigger field (OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD). The devices which have the HOLD feature on DQ3 usually need another dedicated pin for hardware reset and ones without HOLD feature usually have alternative reset on DQ3 what makes the additional reset pin being redundant. The controller supports both variants and reset selection register field (OSPI_FLASH_CFG_CONFIG_REG[6] RESET_CFG_FLD) allows the user to configure which hardware reset solution is implemented in the device under usage.

After configuration is done, it is possible to trigger HOLD or RESET features using I/Os (OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD or OSPI_FLASH_CFG_CONFIG_REG[5] RESET_PIN_FLD bits). After HOLD activation the controller is introduced into waiting state and any other operations should not be requested before de-asserting of HOLD configuration bit. The HOLD feature is useful when any SPI transaction needs to be prolonged in order to adjust it into specific point in time. Note that any HOLD trigger issued during active SPI transaction may be synchronized into reference clock domain at the time the SPI transfer turns to be finished. In this case, there is nothing to hold so the low level SPI logic will not activate HOLD on DQ3. To check if HOLD request suspended the transfer OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit can be polled for. If SPI is not in the IDLE state, the transfer was successfully suspended. It is important for the software to take care of resetting OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD bit before newly triggered SPI transaction. In case HOLD request is set before the beginning of the transfer it will be HOLD right after it starts what may not always be a goal. The hardware RESET needs to be activated when CS is high (no valid transaction is present on SPI bus). It can be checked by polling of OSPI_FLASH_CFG_CONFIG_REG[31]. If the controller is in the IDLE state and no other transfer requests are queued to perform, the hardware RESET can be triggered. The RESET feature is useful when any write, program or erase operation needs to be cancelled. No transfer request is permitted before driving the reset back to being inactive. Triggering HOLD or RESET on DQ3 at the time the device is configured to work in Quad SPI mode or DDR will overwrite transfer data on DQ3 with '0'. This behavior is considered as a software error so it is advisable for the system to make sure that the flash device was introduced to suitable SPI mode (that is by polling its configuration register) before triggering alternative DQ3 function. There are four independent reset outputs implemented to separate between multiple devices connected to the controller (up to 4 are supported). The decision which reset output is to be activated after triggering OSPI_FLASH_CFG_CONFIG_REG[5] RESET_PIN_FLD bit is made based on OSPI_FLASH_CFG_CONFIG_REG[9] PERIPH_SEL_DEC_FLD and OSPI_FLASH_CFG_CONFIG_REG[13-10] PERIPH_CS_LINES_FLD bits. Reset output OSPI_ECC_VECTOR is to be directly driven into corresponding dedicated RESET pins of the devices with separated RESET pin and alternatively, Reset output OSPI_ECC_VECTOR is to be control OSPI_ECC_VECTOR of the DQ3 RESET devices enabling separating of DQ3 Controller Outputs on SoC integration level.

The controller supports all combinations of CPHA and CPOL for Serial Clock. It allows the controller to support any SPI target devices not limited to Flash Memories. Multiple-SPI flash devices use just a subset of these combinations depending on the Transfer Mode as defined in Table 12-183.

Table 12-195. Flash SPI Modes

(SEL_CLK_POL_FLD, SEL_CLK_PHASE_FLD)	Edge Mode	Support
0x00 (SPI MODE 0)	SDR	Yes
0x01 (SPI MODE 1)	SDR	No
0x10 (SPI MODE 2)	SDR	No
0x11 (SPI MODE 3)	SDR	No
0x00 (SPI MODE 0)	DDR	Yes
0x01 (SPI MODE 1)	DDR	No
0x10 (SPI MODE 2)	DDR	No
0x11 (SPI MODE 3)	DDR	No

12.4.2.4.14 Selecting the Flash Instruction Type

In order to send the correct READ and WRITE opcodes, software should initialize the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers. These registers include fields to setup the required instruction opcodes that is intended to be used to access the FLASH (default is basic READ and basic page program) as well as the instruction type, edge mode (DDR or SDR) and whether the instruction uses single, dual, quad or octal pins for address and data transfer. Providing this level of control to the user provides a future proofed generic solution. To ensure the controller can operate from a reset state, the registers will be reset to an opcode compatible with SIO devices what can be modified using BOOT feature.

Despite being applicable for both READs and WRITEs, the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD field only appears once – it is not included in the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG register. If software sets this to anything other than '0', then the address transfer type and the data transfer type bits of both OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers become don't care. It is made available to allow software to support the less common FLASH instructions where the opcode, address and data are sent on 2 or 4 lanes (the opcode from most instructions are sent serially to the FLASH device, even for dual/quad instructions).

There are devices capable to handling Read Operations in Dual Data Rate Mode (DDR) (it is also called Dual Transfer Rate Mode (DTR)). That means they can issue and capture the data on both rising and falling edges during working with dedicated command type. This enables the controller to maintain throughput at twice lower frequency of OSPI clock. The Device Read Instruction Register has DDR enable bit which informs Octal-SPI Flash Controller that opcode written into Read Opcode field is capable with DDR command type. The other field defined in OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[19-16] DDR_READ_DELAY_FLD which enables the controller to shift the transmitted data in DDR mode. By default, data are shifted by 1 clock cycle to ensure hold timing greater than 0 during DDR transactions. It may not be sufficient for high reference clock frequency in accordance with the high dividers.

Table 12-184 shows how software should configure the OSPI module for selected specific READ and WRITE instruction supported by the abovementioned device.

Table 12-196. READ and WRITE Instruction Configuration

READ							
OPCODE	OPCODE sent over how many lanes / edge mode?	ADDRESS / DUMMY / MODE sent over how many lanes / edge mode?	DATA bytes sent over how many lanes / edge mode?	Instruction Type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	DDR bit enable (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD)
READ	1/SDR	1/SDR	1/SDR	0	0	0	0
FAST_READ	1/SDR	1/SDR	1/SDR	0	0	0	0
DTR_FAST_READ	1/SDR	1/DDR	1/DDR	0	0	0	1
DOFR (Dual O/p Fast Read)	1/SDR	1/SDR	2/SDR	0	0	1	0
DIOFR (Dual I/O Fast Read)	1/SDR	2/SDR	2/SDR	0	1	1	0
DDIOFR (DTR Dual I/ O Fast Read)	1/SDR	2/DDR	2/DDR	0	1	1	1
QOFR (Quad O/p Fast Read)	1/SDR	1/SDR	4/SDR	0	0	2	0
QIOFR (Quad I/O Fast Read)	1/SDR	4/SRD	4/SDR	0	2	2	0
DQIOFR (DTR Quad I/ O Fast Read)	1/SDR	4/DDR	4/DDR	0	2	2	1
OOFR (Octal O/p Fast Read)	1/SDR	1/SDR	8/SDR	0	0	3	0

Table 12-196. READ and WRITE Instruction Configuration (continued)

OIOFR (Octal I/O Fast Read)	1/SDR	8/SDR	8/SDR	0	3	3	0
DOIOFR (DTR Octal O/p Fast Read)	1/SDR	1/DDR	8/DDR	0	0	3	1
4DOIOFR (4-byte DTR Octal I/O Fast Read)	1/SDR	8/DDR	8/DDR	0	3	3	1
DCFR (Dual Command Fast Read)	2/SDR	2/SDR	2/SDR	1	Don't care	Don't care	0
DDCFR (DTR Dual Command Fast Read)	2/SDR	2/DDR	2/DDR	1	Don't care	Don't care	1
QCFR (Quad Command Fast Read)	4/SDR	4/SRD	4/SDR	2	Don't care	Don't care	0
DQCFR (DTR Quad Command Fast Read)	4/SDR	4/DDR	4/DDR	2	Don't care	Don't care	1
OCFR (Octal Command Fast Read)	8/SDR	8/SDR	8/SDR	3	Don't care	Don't care	0
4DOCFR (4-byte DTR Octal Command Fast Read)	8/SDR	8/DDR	8/DDR	3	Don't care	Don't care	1
WRITE							
OPCODE	OPCODE sent over how many lanes?	ADDRESS / DUMMY / MODE sent over how many lanes?	DATA bytes sent over how many lanes?	Instruction Type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	
PP	1	1	1	0	0	0	
DIFP (Dual Input Fast Program)	1	1	2	0	0	1	
DIEFP (Dual Input Extended Fast Program)	1	2	2	0	1	1	
QIFP (Quad Input Fast Program)	1	1	4	0	0	2	
QIEFP (Quad Input Extended Fast Program)	1	4	4	0	2	2	
OIFP (Octal Input Fast Program)	1	1	8	0	0	3	
OIEFP (Octal Input Extended Fast Program)	1	8	8	0	3	3	
DCPP (Dual Command Fast Program)	2	2	2	1	Don't care	Don't care	

Table 12-196. READ and WRITE Instruction Configuration (continued)

QCPP (Quad Command Fast Program)	4	4	4	2	Don't care	Don't care
OCPP (Octal Command Fast Program)	8	8	8	3	Don't care	Don't care

Note

This data are applicable for both 3-byte or 4-byte address variants of the commands if did not indicate otherwise.

Note

In DTR protocol all transfer phases (including opcode) take DDR edge mode independently on the command under execution. DTR protocol is to be enabled by OSPI_FLASH_CFG_CONFIG_REG[24] ENABLE_DTR_PROTOCOL_FLD bit. It has higher priority than DDR Mode enable bit from OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD.

12.4.2.4.15 OSPI Data Interface

12.4.2.4.16 OSPI PHY Module

OSPI module fully integrates PHY module dedicated to more flexible and power efficient transfers.

The PHY module communicates with the OSPI Flash controller via the aforementioned PHY Interface and handles data transfer on low-level stage of design hierarchy. However, when the OSPI_RCLK is configured to be equal to the SPI clock instead of alternative approach using clock divider, there is just one OSPI_RCLK cycle (not 4 or more) within single SPI period or half period for DDR Mode (SPI Control Module works on reference clock). Given that OSPI_RCLK is the input clock for RX FIFO and the output one for TX FIFO, the PHY solution incurs more restrictive requirement for value of system clock in order to synchronize data without SPI transfer interruption. For example, when the controller operates in DDR 1× octal Mode, 2 bytes of data (equivalent to one RX FIFO location) is gathered within just single OSPI_RCLK cycle. The controller cannot predict next data access while operating in the Direct Mode (meaning its size or whether it is sequential to the previous one or not). As a result, if the OSPI_HCLK is not significantly greater than OSPI_RCLK, the SPI transfer has to be suspended until the Flash Command Generator forwards new data to TX FIFO.

An optional PHY Pipeline Mode is implemented to avoid the necessity of stable clocking of the system clock for the Direct Mode when the PHY mode is enabled and to keep maximum performance while ensuring correct operation of the OSPI controller with the PHY using low frequencies from all its domains. This mode is a trade-off between large software overhead when operating in the Indirect Mode and the described limitations present in the Direct Mode. For more information about PHY Pipeline Mode, see Section 12.4.2.4.16.1 , *PHY Pipeline Mode*.

When DDR 2× Mode is granted based on configuration – SPI transfer is automatically performed using the PHY module even if the OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD is de-asserted. SDR 2× commands are handled with PHY module paths being bypassed. Nevertheless, dividers of 2, 4 or 6 for DDR and divider of 2 for SDR should not be configured based on controller requirements and these configurations are perceived as a software error.

Note

Please refer to the OSPI Controller PHY Tuning Algorithm Application Note for additional details related to the OSPI PHY Module and Tuning Algorithm,

12.4.2.4.16.1 PHY Pipeline Mode

This mode is used for Direct Read Mode of operation. If any other operations are intended to be executed, it is recommended to disable PHY Pipeline Mode and re-enable for subsequent Direct Reads in PHY mode. Since there is comprehensive software mechanism controlling Read data transfers in Indirect Mode, pipeline of data interface accesses is not effective for this mode. Enable PHY Pipeline feature when at least four 4-byte-sized data words are predicted to be read in sequentially. The Flash Command Generator pipelines and puts them into TX FIFO which causes CS to remain active because low level SPI protocol controller controls TX FIFO fill level. In order to correctly trigger Direct Read in Pipeline Mode TX FIFO must be empty. Therefore first polling of OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit needs to be done. The sequential data transfer will be interrupted when the data target select signal of the data interface is asserted to low. This information is also detected by Data Target Module which informs the Flash Command Generator that the next access is invalid and a TX FIFO locations can be flushed transparently for the system.

In PHY Pipeline Mode it is recommended for Data Controller not to introduce wait states in between consecutive occurrences of the data interface signal that indicates transfer has finished. It will ensure regular transfer rate on data side. Introducing wait states gradually slows data transfer rate down and may finally cause SPI transfer interruption because of TX FIFO data starvation. The system, however, may need to introduce some number of wait states after completion of sequential transfer (composed of 4-byte sized data words) for progressing the data. The dedicated buffer is implemented in Data Target Controller which collects all incoming data during wait states injection. In order to keep SPI transfer uninterrupted, number of wait states should be as little as possible. The higher the OSPI_HCLK/ OSPI_RCLK ratio the more wait states can be introduced without SPI transfer interruption. In case the system is able to launch a new transfer before wait states overflow, buffered data transfer to the host will continue. It compensates slowed down transfer by introducing wait states. In case the system is not able to launch a new transfer before wait states overflow, next incoming transfer is considered non-sequential and is executed after all pipelined data is flushed.

This mode can be enabled when following conditions are met:

- OSPI_HCLK > OSPI_RCLK (Comparing the slow data clock with the fast reference one makes Pipeline Mode ineffective – Suspend of SPI Transfer would be possible. Consequently, this condition has to be met to operate in this mode.)
- Only 4-byte sized Data Words are permitted (This ensures more data clock cycles for synchronization of FIFOs between consecutive pulses of the signal indicating transfer has finished.)
- The transfer with introduced wait states or non-sequential transfers can only be triggered in between at least four 4-byte sized Data Bursts sequential accesses (16 Bytes) to be sure that Data Controller can trust buffered incoming data during wait states injection.
- Do not use Pipeline Mode along with Continuous Mode (XIP). Benefit of XIP is limited for bulk data transfers intended to execute in Pipeline Mode.

12.4.2.4.16.2 Read Data Capturing by the PHY Module

Read Data Capturing by the PHY module is useful, as the user is not responsible for the design dedicated DLL being compatible with the Octal-SPI Flash Controller. Another benefit is an option to adjust both SPI clock and sampling clock in a very wide range to fit them into individual requirements of any system. If loopback clock (OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[0] BYPASS_FLD) and PHY mode (OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the loopback clock is driven into RX DLL instead of gated reference clock. Because of the architecture of DLL, loopback clock needs to be provided in SPI Mode 0. If DQS (OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[8] DQS_ENABLE_FLD) and PHY mode (OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the DQS is driven into RX DLL instead of gated reference clock.

12.4.2.5 OSPI Programming Guide

12.4.2.5.1 Configuring the OSPI Controller for Use After Reset

The OSPI controller has been designed to wake up in a state that is suitable for performing basic reads and writes using the direct access controller. The BASIC read (opcode 0x03) and BASIC write (opcode 0x02) instructions are operations supported by all target devices. The controller also wakes up with a baud rate divider setting of divide-by-32. Assuming the reference clock is operating at 400 MHz after reset, then this means the effective SPI clock is just 12.5 MHz. This should be slow enough to meet all timing requirements of all target devices without any further device programming.

If the target device does not use 3 address bytes, the device size configuration register must be modified to the appropriate size.

If software plans to write to the device, and the number of bytes per device page is not equal to 256, then the device size configuration register must also be modified.

While not a requirement, it is prudent for software to enable the write protect feature prior to enabling the OSPI controller. This will block any data writes from taking effect. To do so, the protection registers (OSPI_FLASH_CFG_LOWER_WR_PROT_REG, OSPI_FLASH_CFG_UPPER_WR_PROT_REG and OSPI_FLASH_CFG_WR_PROT_CTRL_REG) should be setup and the number of bytes per device block in the device size configuration register should also be setup.

After Power-on Reset (POR), software can read from and write to the FLASH device (albeit slowly). Enabling/Disabling the controller and DAC is achieved with just one write to corresponding fields of the OSPI_FLASH_CFG_CONFIG_REG register. User shall take note to maintain the default values of the baud rate divisor and the default state of SEL_CLK_POL_FLD/ SEL_CLK_PHASE_FLD bits of this register. A write data value of 0x00780081 is recommended.

12.4.2.5.2 Configuring the OSPI Controller for Optimal Use

Note

When using the OSPI Controller, the opcodes in OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD, OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD and OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[7-0] OPCODE_FLD bit fields shall not match the opcode in the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bit field.

For high speed transfers PHY mode can be enabled and for optimal configuration PHY Pipeline mode is recommended. For more information, see *PHY Pipeline Mode*.

To access the flash optimally, software must configure the controller accurately:

1. Wait until any pending STIG or INDAC operation has completed or poll OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit.
2. Disable the DAC through OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD bit. It is permitted, but not necessary to also disable the OSPI controller completely via OSPI_FLASH_CFG_CONFIG_REG[0] ENB_SPI_FLD bit.
3. Update the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers for the instruction type you wish to use for indirect and direct writes and reads.
4. Update the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field if mode bits have been enabled in the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[20] MODE_BIT_ENABLE_FLD bit.
5. Update the OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG if the contents are incorrect. Note parts or all of this register may have been updated after initialization. The number of address bytes is a key configuration setting required for performing reads and writes. The number of bytes per page is required for performing

any write. The number of bytes per device block is only required if the write protect feature is used. If the default values are correct for the target device, or if some of the values (not including the number address bytes) were incorrect but device writes were not permitted.

6. Update the OSPI_FLASH_CFG_DEV_DELAY_REG. This register allows the user to tweak how the chip select is driven after each FLASH access. This is required as each device may have different timing requirements. As the serial clock frequency is increased, these timing requirements become more important. Note the numbers programmed in this register are based on the period of reference clock. Example: A device needs 50ns minimum time before CS can be re-asserted after it has been de-asserted. By default, the controller will only provide a minimum of 1 SCLK period. When the device is operating at 100 MHz, the SCLK period is only 10ns, so 40ns extra is required. Since the register defines the number of reference clock cycles to add, and reference clock is running at 400 MHz (2.5ns period), then the user should program a value of at least 16 to the OSPI_FLASH_CFG_DEV_DELAY_REG[31-24] D_NSS_FLD. This delay can be extended during auto-polling phase. There is possibility to define the polling repetition delay in the OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field.
7. Update the OSPI_FLASH_CFG_REMAP_ADDR_REG register, if required. Affects DAC path only.
8. Setup and enable write protection registers (OSPI_FLASH_CFG_LOWER_WR_PROT_REG, OSPI_FLASH_CFG_UPPER_WR_PROT_REG and OSPI_FLASH_CFG_WR_PROT_CTRL_REG) if they are required and if they have not already been setup from post initialization.
9. Enable required interrupts via the OSPI_FLASH_CFG_IRQ_MASK_REG register.
10. Setup the baud rate divisor in the OSPI_FLASH_CFG_CONFIG_REG[22-19] MSTR_BAUD_DIV_FLD to define the required clock frequency of the target device.
11. Update the OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG register. This register will delay when the read data is captured and can help when the read data path from the device to the controller is long and the device clock frequency is high. An update to this register may not be necessary.
12. Enable the OSPI controller and the DAC via the OSPI_FLASH_CFG_CONFIG_REG.

12.4.2.5.3 Using the Flash Command Control Register (STIG Operation)

The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register provides software means to access the FLASH device in a flexible and programmable manner. This is known as a STIG operation (Software Triggered Instruction Generator). The instruction opcode, number of address bytes (if any), the address itself, number of dummy cycles (if any), number of write data bytes (if any), the write data itself and the number of read data bytes (if any) can be programmed. Once these have been programmed, software can trigger the command via OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit and wait for its acceptance by polling OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit. When CMD_EXEC_STATUS_FLD bit turns de-asserted, another STIG can be triggered. This method of accessing the FLASH is the typical mechanism that software would use to access the FLASH device's registers, as well as for performing ERASE operations. It can also be used to access the FLASH array itself, although the maximum of 8 data bytes may be read or written at any one time, defined in the Flash Command Write and Read Data registers (OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG, OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG, OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG). This number of bytes can be extended for Read Data commands using additional STIG Memory Bank controlled by OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD and OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG.

Commands issued using this interface have a higher priority than all other READ accesses coming from data interface, and will therefore interrupt any READ commands being requested by the indirect or direct controllers.

12.4.2.5.4 Using SPI Legacy Mode

SPI legacy mode allows software to access the internal TX-FIFO and RX-FIFO directly, thus bypassing the direct, indirect and STIG controllers.

Legacy mode allows the user to issue any FLASH instruction to the device, but does place a heavy software overhead in order to manage the fill levels of the FIFO's effectively. This is because the legacy SPI core is bi-directional in nature, with data continuously being transferred in either direction while the chip select is enabled. Even if the driver only wishes to read data from the FLASH device, dummy data must be written out to ensure the chip select stays active, and vice versa for write transactions.

Since the TX-FIFO and RX-FIFO are of limited depth, software has a responsibility to maintain the FIFO levels to ensure the TX-FIFO does not become exhausted during the instruction execution and the RX-FIFO doesn't overflow. This can place a lot of overhead on software. Interrupts are provided to indicate when the fill levels pass programmable watermarks, which are themselves programmable registers OSPI_FLASH_CFG_TX_THRESH_REG and OSPI_FLASH_CFG_RX_THRESH_REG.

The limited depth may impose the limitation over execution of some specific SPI commands in legacy mode. Note that the controller interprets all transmitted bytes as valid. For example, if the Flash Device was configured to return valid data after many dummy cycles, the TX FIFO could become full before the controller sends all of dummy data.

12.4.2.5.5 Entering XIP Mode from POR

XIP is a mode that can be entered in a non-volatile way if the device has XIP enabled as a non-volatile configuration setting. Software will not be able to discover the state of XIP from POR via FLASH status register reads as the only operation a FLASH device will recognize when XIP mode is enabled is an XIP read operation.

If it is already known that the device will enter XIP from POR, then the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD and OSPI_FLASH_CFG_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD bits should be set in initial boot.

If it is not already known that the device will enter XIP from POR, and XIP from POR may be supported by the attached FLASH device, then software can attempt to exit XIP mode by issuing an XIP exit command using a STIG command (via the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register). To do this, software must be aware of the mode bit requirements of that device, as XIP entry and exit changes per device.

12.4.2.5.6 Entering XIP Mode Otherwise

XIP mode is supported in most FLASH devices. Some of them use signature bits that are sent to the device immediately following the address bytes, other use signature bits and also require a FLASH device configuration register write to enable XIP. For the FLASH devices that must be compliant to the OSPI controller, the following steps can be taken by software to enter XIP mode:

1. Disable the DAC and INDAC (OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD) to ensure no new data read accesses will be sent to the FLASH device.
2. (Optional)Configure the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG to issue a VCR write to FLASH memory, because XIP mode must first be enabled for some devices.
3. Configure the XIP mode bits in the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field.
4. Enable the local controllers XIP mode by setting OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD bit.
5. Re-enable the DAC and, if required, the INDAC.

12.4.2.5.7 Exiting XIP Mode

To exit XIP mode, software should first disable the DAC and INDAC to ensure no new data read accesses will be sent to the FLASH device. It should then set mode bits to other than the established in the corresponding Flash Device specifications. These are dependent on the FLASH device and manufacturer. Software should then reset OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD.

Note the FLASH device must see a READ instruction before it can disable its internal XIP mode state, so this means XIP mode will internally stay active until the next READ instruction is serviced. User must take care to ensure that XIP mode is disabled before the end of any READ sequence.

12.4.3 General-Purpose Memory Controller (GPMC)

This section describes the General-Purpose Memory Controller (GPMC) for the device.

12.4.3.1 GPMC Overview

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

Figure 12-164 shows the GPMC0 module overview.

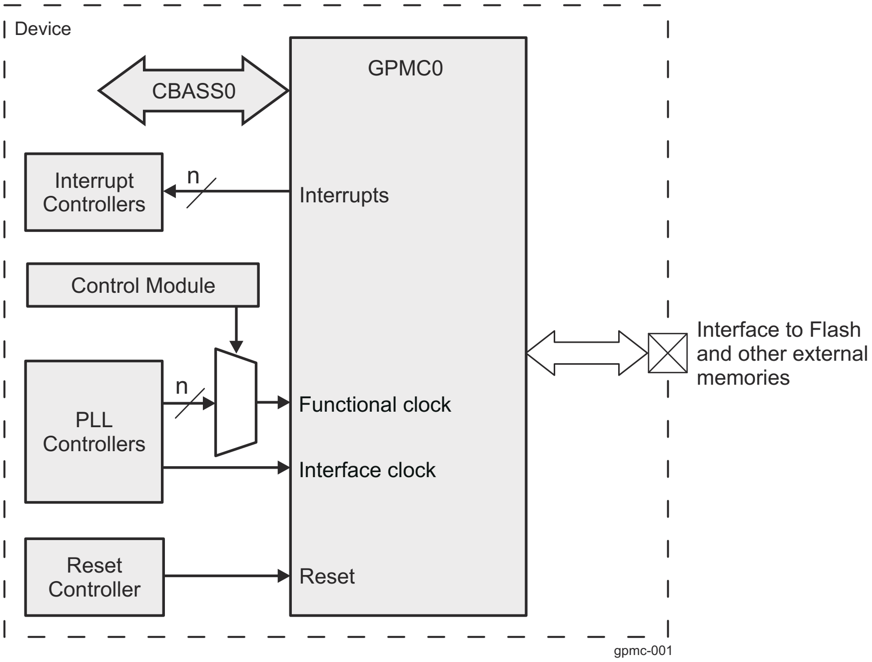

Figure 12-164. GPMC0 Overview

12.4.3.1.1 GPMC Features

The main features of the GPMC are:

- 8-, 16- or 32-bit-wide data path to external memory device
- Supports up to 4 chip select regions of programmable size and programmable base addresses in a total address space of 1GB
- Supports on-the-fly error code detection using the Bose-Chaudhurl-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth usage
- The clock to the external memory is provided from GPMC_FCLK divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters with a timing granularity of one GPMC_FCLK clock cycle.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pin monitoring

- Support bus keeping
- Support bus turnaround
- Prefetch and write-posting engine associated with DMA controller at system level to achieve full performance from the NAND device with minimum effect on NOR/SRAM concurrent access
- 32-bit interconnect target interface which supports non-wrapping and wrapping burst of up to 16x32 bits.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4-8-16-32 Word16, 4-8-16 Word32)
- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
- Synchronous read/write burst access with wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little-endian access only

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External asynchronous or synchronous 32-bit wide memory or device
- External 16-bit non-multiplexed NOR flash device
- External 16- and 32-bit address and data multiplexed NOR Flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit and 32-bit pseudo-SRAM (pSRAM) device

Note

Page mode is available only in non-multiplexed mode.

12.4.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.4.3.2 GPMC Environment

The GPMC0 module is hereinafter referred to as GPMC.

This section describes the GPMC0 external connections (environment).

12.4.3.2.1 GPMC Modes

This section shows four GPMC0 external connection options:

- Figure 12-165 shows a connection between the GPMC0 and a 32-bit synchronous address/data-multiplexed external memory device.
- Figure 12-166 shows a connection between the GPMC0 and a 16-bit synchronous address/data-multiplexed (or AAD-multiplexed but this protocol uses fewer address pins) external memory device.
- Figure 12-167 shows a connection between the GPMC0 and a 16-bit synchronous non-multiplexed external memory device.
- Figure 12-168 shows a connection between the GPMC0 and an 8-bit synchronous non-multiplexed external memory device.
- Figure 12-169 shows a connection between the GPMC0 and an 8-bit NAND device.

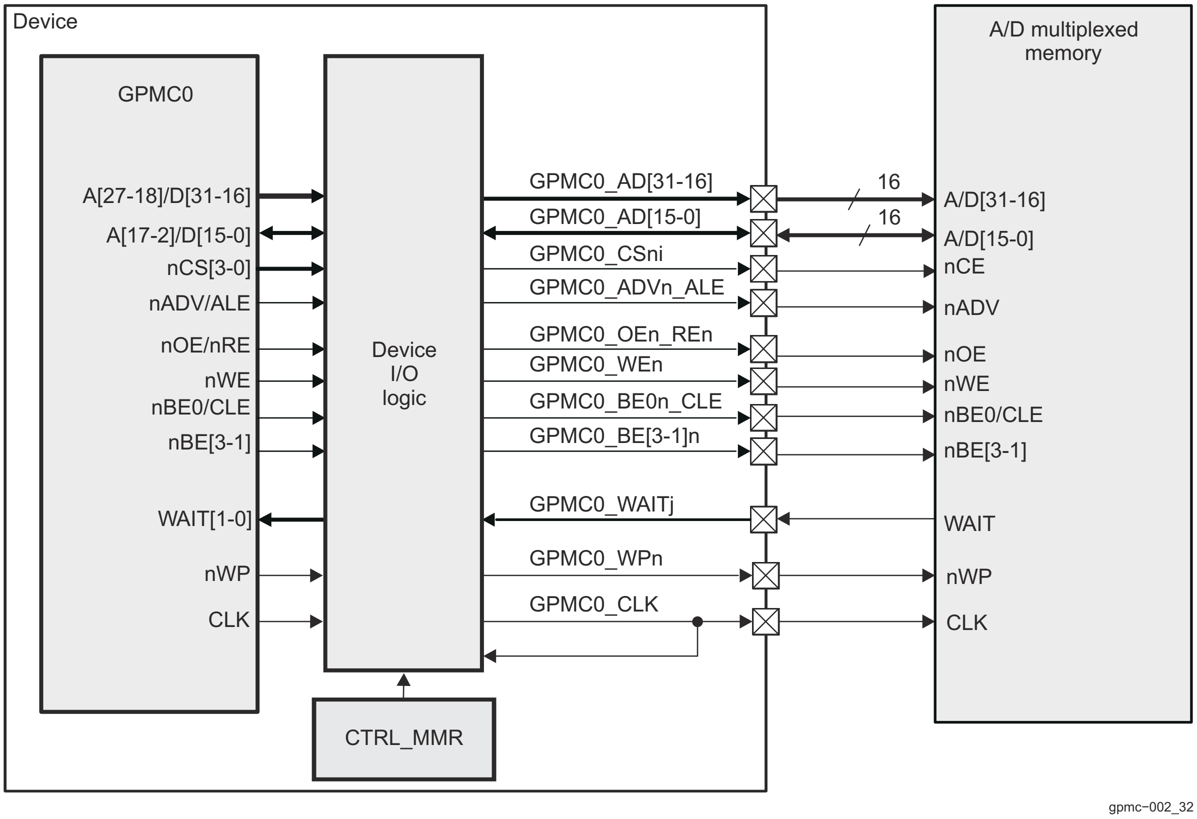

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-165. GPMC to 32-Bit Address/Data-Multiplexed Memory

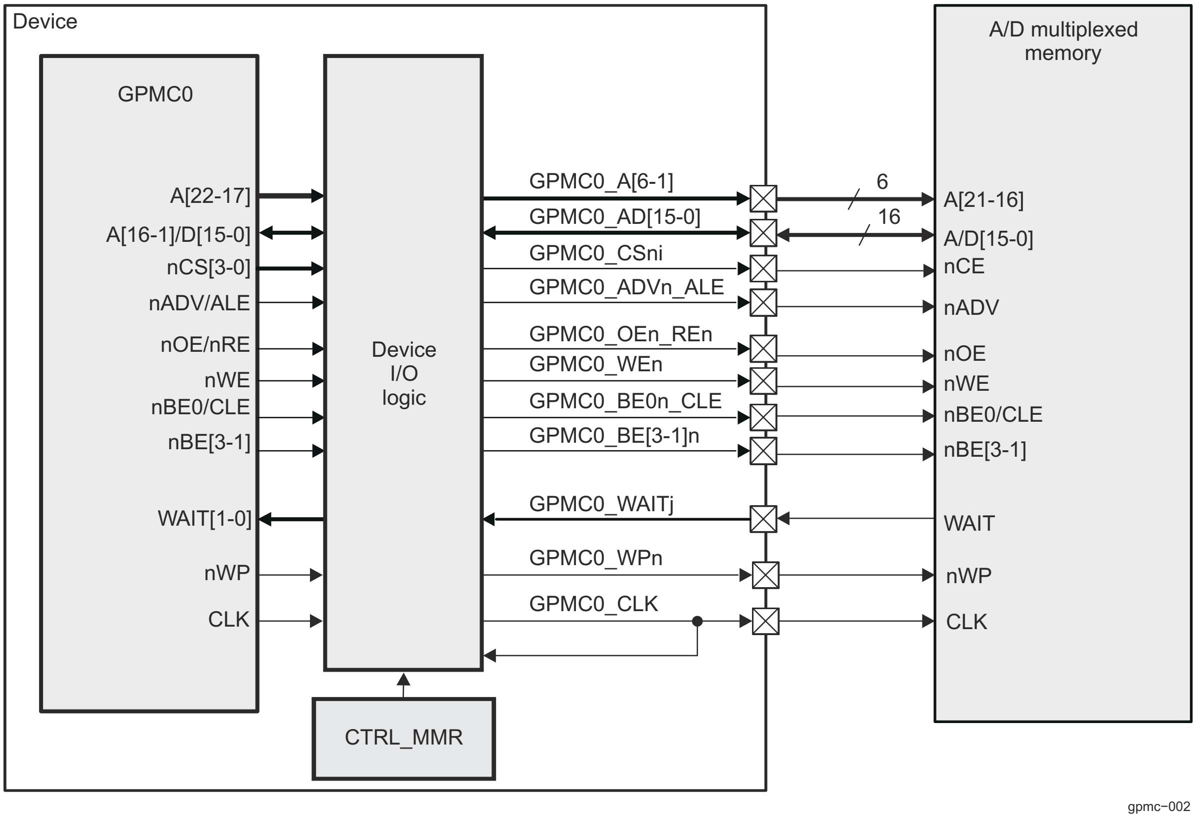

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-166. GPMC to 16-Bit Address/Data-Multiplexed Memory

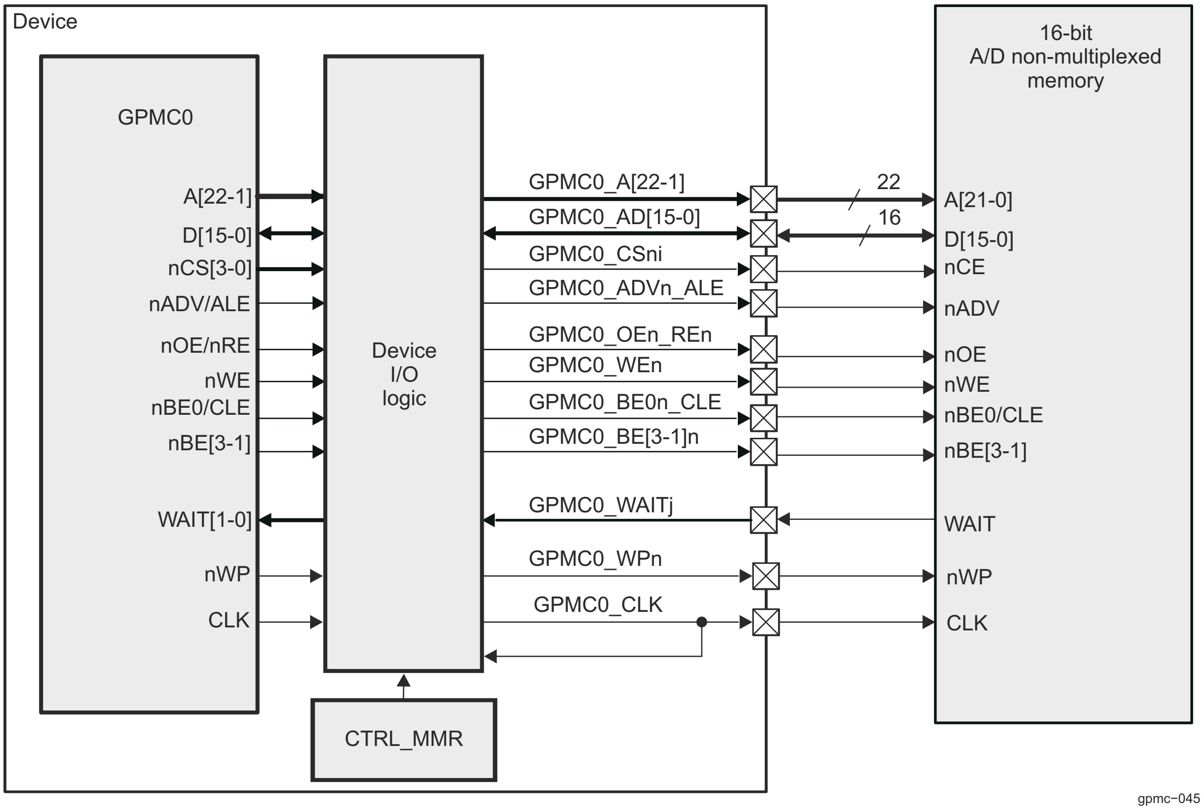

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-167. GPMC to 16-Bit Non-Multiplexed Memory

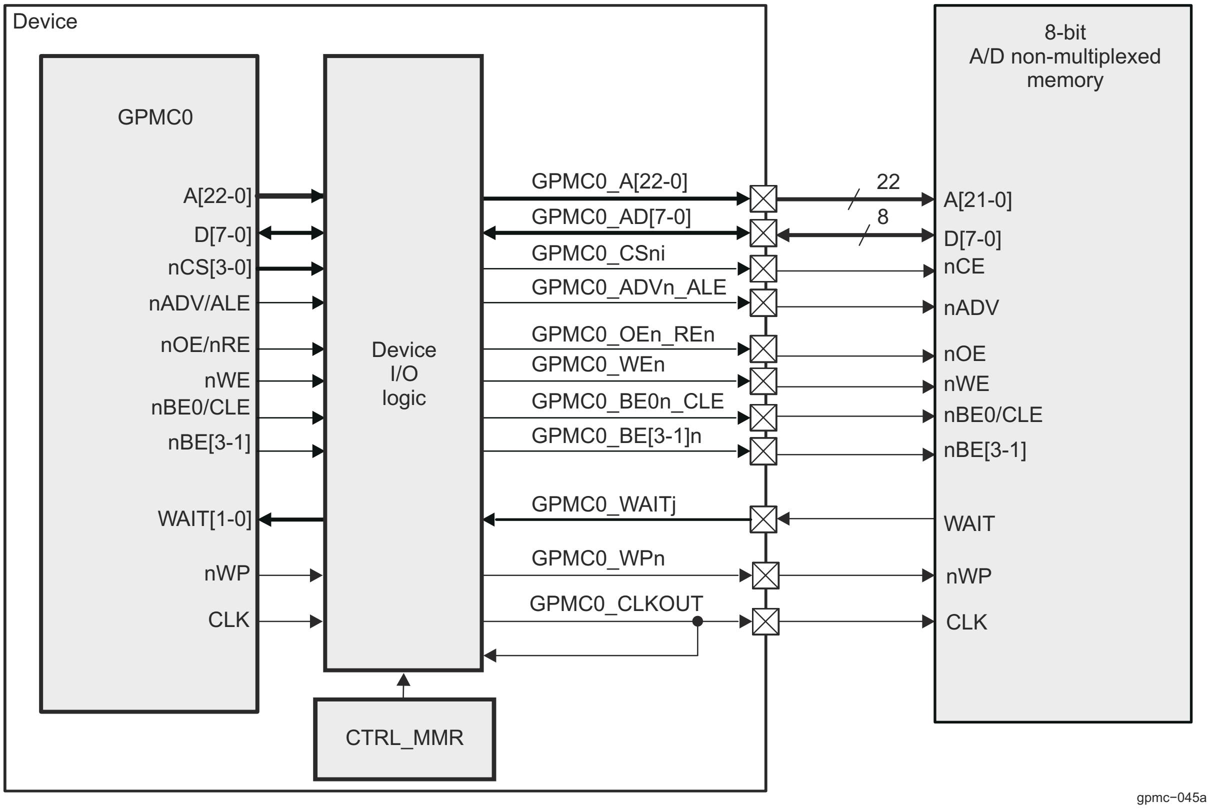

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-168. GPMC to 8-Bit Non-Multiplexed Memory

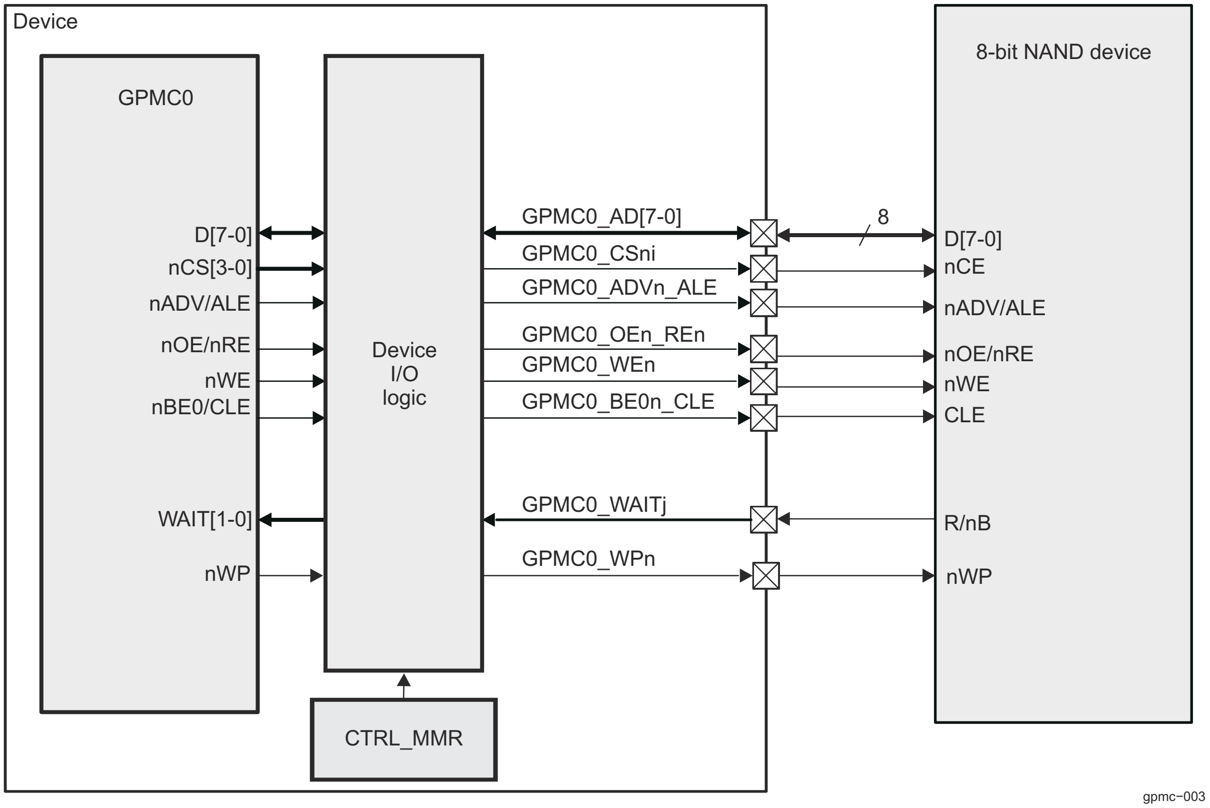

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-169. GPMC to 8-Bit NAND Device

12.4.3.2.2 GPMC I/O Signals

Table 12-185 lists the GPMC subsystem input/output (I/O) pins.

Table 12-197. GPMC I/O Signals (Controller Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			GPMC0	
A[22-0]	GPMC0_A[22-0]	O	23-bit output address bus	-
A[27-2]/D[31-0]	GPMC0_AD[31-0]	I/O	Multiplexed address/data	-
nCS[3-0]	GPMC0_CSn[3-0]	O	Chip-selects (active low)	-
CLK CLKLB	GPMC0_CLK	O	Clock generated for the external memory or device. For more information, see *GPMC0 Integration*.	-
N/A	GPMC0_FCLK_MUX	O	Free running clock. GPMC functional clock (GPMC0_FCLK) propagated on a device pad. For more information on the GPMC0_FCLK_MUX integration, see *GPMC0 Integration*.	-
nADV/ALE	GPMC0_ADVn_ALE	O	Address valid (active low). Also used as address latch enable (active high) for NAND protocol memories.	-
nOE/nRE	GPMC0_OEn_REn	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.	-

Table 12-197. GPMC I/O Signals (Controller Mode) (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
nWE	GPMC0_WEn	O	Write enable (active low)	-
nBE0/CLE	GPMC0_BE0n_CLE	O	Lower-byte enable (active low). Also used as command latch enable for NAND protocol memories.	-
nBE[3-1]	GPMC0_BE[3-1]n	O	Upper-byte enable (active low)	-
WAIT[1-0]	GPMC0_WAIT[1-0]	I	External wait signal for NOR and NAND protocol memories. Can be mapped on any of the chip-selects.	-
nWP	GPMC0_WPn	O	Write protect (active low)	-
DIR	GPMC0_DIR	O	This signal can be used to control an external buffer direction. Also controls the signal direction of D[15-0]. Low during transmit (for write access: data OUT from GPMC0 to memory). High during receive (for read access: data IN from memory to GPMC0).	-

(1) I = Input; O = Output; I/O - Bidirectional

(2) HiZ = High Impedance

Note

For GPMC output clock signal (CLK) to work properly, the RXACTIVE bit of the appropriate CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

Table 12-186 shows the use of address and data GPMC pins based on the type of external device.

Table 12-198. GPMC Pin Multiplexing Options

GPMC Pin	Multiplexed Address Data 32-Bit Device	Multiplexed Address Data 16-Bit Device	non-multiplexed Address Data 16-Bit Device (incomplete 28-bit address range)	non-multiplexed Address Data 8-Bit Device (incomplete 28-bit address range)	16-Bit NAND Device	8-Bit NAND Device
GPMC0_A[22]	Not used	Not used	A22	A22	Not used	Not used
GPMC0_A[21]	Not used	Not used	A21	A21	Not used	Not used
GPMC0_A[20]	Not used	Not used	A20	A20	Not used	Not used
GPMC0_A[19]	Not used	Not used	A19	A19	Not used	Not used
GPMC0_A[18]	Not used	Not used	A18	A18	Not used	Not used
GPMC0_A[17]	Not used	Not used	A17	A17	Not used	Not used
GPMC0_A[16]	Not used	Not used	A16	A16	Not used	Not used
GPMC0_A[15]	Not used	Not used	A15	A15	Not used	Not used
GPMC0_A[14]	Not used	Not used	A14	A14	Not used	Not used
GPMC0_A[13]	Not used	Not used	A13	A13	Not used	Not used
GPMC0_A[12]	Not used	Not used	A12	A12	Not used	Not used
GPMC0_A[11]	Not used	Not used	A11	A11	Not used	Not used
GPMC0_A[10]	Not used	A26	A10	A10	Not used	Not used
GPMC0_A[9]	Not used	A25	A9	A9	Not used	Not used
GPMC0_A[8]	Not used	A24	A8	A8	Not used	Not used

Table 12-198. GPMC Pin Multiplexing Options (continued)

GPMC Pin	Multiplexed Address Data 32-Bit Device	Multiplexed Address Data 16-Bit Device	non-multiplexed Address Data 16-Bit Device (incomplete 28-bit address range)	non-multiplexed Address Data 8-Bit Device (incomplete 28-bit address range)	16-Bit NAND Device	8-Bit NAND Device
GPMC0_A[7]	Not used	A23	A7	A7	Not used	Not used
GPMC0_A[6]	Not used	A22	A6	A6	Not used	Not used
GPMC0_A[5]	Not used	A21	A5	A5	Not used	Not used
GPMC0_A[4]	Not used	A20	A4	A4	Not used	Not used
GPMC0_A[3]	Not used	A19	A3	A3	Not used	Not used
GPMC0_A[2]	Not used	A18	A2	A2	Not used	Not used
GPMC0_A[1]	Not used	A17	A1	A1	Not used	Not used
GPMC0_A[0](1)	Not used	A0 - Not used	Not used	A0	Not used	Not used
GPMC0_AD[31]	D31	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[30]	D30	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[29]	D29	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[28]	D28	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[27]	D27	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[26]	D26	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[25]	A27/D25	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[24]	A26/D24	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[23]	A25/D23	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[22]	A24/D22	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[21]	A23/D21	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[20]	A22/D20	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[19]	A21/D19	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[18]	A20/D18	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[17]	A19/D17	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[16]	A18/D16	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[15]	A17/D15	A16/D15	D15	Not used	D15	Not used
GPMC0_AD[14]	A16/D14	A15/D14	D14	Not used	D14	Not used
GPMC0_AD[13]	A15/D13	A14/D13	D13	Not used	D13	Not used
GPMC0_AD[12]	A14/D12	A13/D12	D12	Not used	D12	Not used
GPMC0_AD[11]	A13/D11	A12/D11	D11	Not used	D11	Not used
GPMC0_AD[10]	A12/D10	A11/D10	D10	Not used	D10	Not used
GPMC0_AD[9]	A11/D9	A10/D9	D9	Not used	D9	Not used
GPMC0_AD[8]	A10/D8	A9/D8	D8	Not used	D8	Not used
GPMC0_AD[7]	A9/D7	A8/D7	D7	D7	D7	D7
GPMC0_AD[6]	A8/D6	A7/D6	D6	D6	D6	D6
GPMC0_AD[5]	A7/D5	A6/D5	D5	D5	D5	D5
GPMC0_AD[4]	A6/D4	A5/D4	D4	D4	D4	D4
GPMC0_AD[3]	A5/D3	A4/D3	D3	D3	D3	D3
GPMC0_AD[2]	A4/D2	A3/D2	D2	D2	D2	D2
GPMC0_AD[1]	A3/D1	A2/D1	D1	D1	D1	D1
GPMC0_AD[0]	A2/D0	A1/D0	D0	D0	D0	D0

(1) Used to effectively address 8-bit (only) non-multiplexed memories

With all device types, the GPMC does not drive unnecessary address lines. They stay at their reset value of 0x0.

Address mapping supports address/data-multiplexed 16- or 32-bit-wide devices:

- The NOR flash memory controller still supports non-multiplexed address and data memory devices.
- Multiplexing mode can be selected through the GPMC_CONFIG1_i[9-8] MUXADDDATA bit field (where i = 0 to 3).

12.4.3.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.3.4 GPMC Functional Description

The GPMC basic programming model offers maximum flexibility to support various access protocols for each of the four configurable chip-selects. Use optimal chip-select settings, based on the characteristics of the external device:

- Different protocols can be selected to support generic asynchronous or synchronous random-access devices (NOR flash, SRAM) or to support specific NAND devices.
- The address and data bus can be multiplexed on the same external bus.
- Read and write access can be independently defined as asynchronous or synchronous.
- System requests (byte, 16-bit word, burst) are performed through single or multiple accesses. External access profiles (single, multiple with optimized burst length, native- or emulated-wrap) are based on external device characteristics (supported protocol, bus width, data buffer size, native-wrap support).
- System burst read or write requests are synchronous-burst (multiple-read or multiple-write). When neither burst nor page mode is supported by external memory or ASIC devices, system burst read or write requests are translated to successive single synchronous or asynchronous accesses (single reads or single writes). 8-bit wide devices are supported only in single synchronous or single asynchronous read or write mode.
- To simulate a programmable internal-wait-state, an external WAIT pin can be monitored to dynamically control external access at the beginning (initial access time) of and during a burst access.

Each control signal is controlled independently for each chip-select. The internal functional clock of the GPMC (GPMC_FCLK) is used as a time reference to specify the following:

- Read- and write-access duration
- Most GPMC external interface control-signal assertion and deassertion times
- Data-capture time during read access
- External wait-pin monitoring time
- Duration of idle time between accesses, when required

12.4.3.4.1 GPMC Block Diagram

Figure 12-170 shows the GPMC functional block diagram. The GPMC consists of six blocks:

- Interconnect port interface
- Address decoder, GPMC configuration, and chip-select configuration register file
- Access engine
- Prefetch and write-posting engine
- Error correction code engine (ECC)
- External device/memory port interface

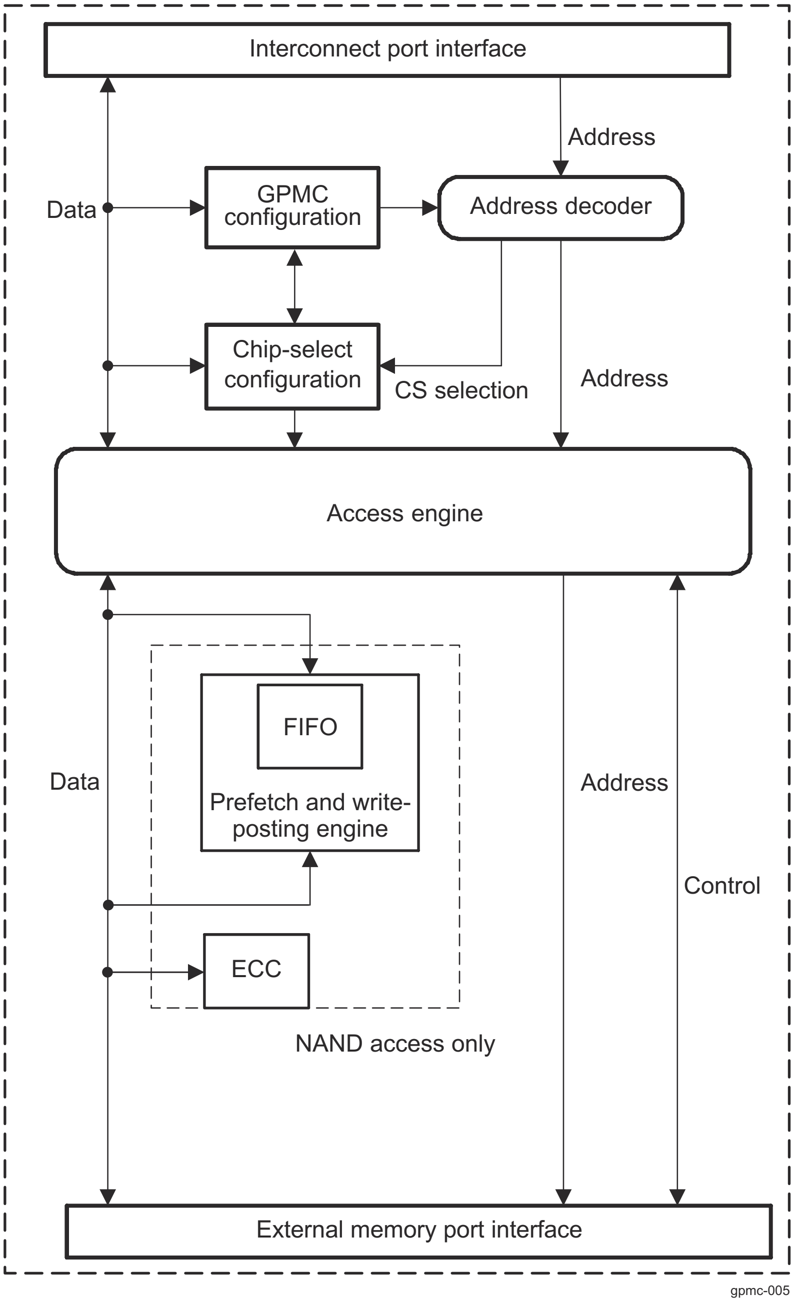

Figure 12-170. GPMC Block Diagram

The GPMC can access various external devices. The flexible programming model allows a wide range of attached device types and access schemes.

Based on the programmed configuration bit fields stored in the GPMC registers, the GPMC can generate the timing of all control signals depending on the attached device and access type.

Given the chip-select decoding and its associated configuration registers, the GPMC selects the appropriate control signal timing for the device type.

12.4.3.4.2 GPMC Clock Configuration

Table 12-187 describes the GPMC clocks.

Table 12-199. GPMC Clocks

Signal	I/O[1]	Description
GPMC_FCLK	I	Functional clock
GPMC_ICLK	I	Interface clock
CLK (GPMC_CLKOUT pin)	O	External clock provided to synchronous external memory devices and to DCC5 in the device.

(1) I = Input; O = Output; I/O - Bidirectional

The GPMC output clock (CLK) is generated by the GPMC from the internal GPMC_FCLK clock. The source of the GPMC_FCLK is described in *GPMC0 Clocks*. The GPMC output clock is configured using the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field (where i = 0 to 3), as shown in Table 12-188.

Table 12-200. GPMC Output Clock Configuration

Source Clock	GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER	GPMC Output Clock Provided to External Memory Device
GPMC_FCLK	00	GPMC_FCLK
	01	GPMC_FCLK/2
	10	GPMC_FCLK/3
	11	GPMC_FCLK/4

When using synchronous interface protocols, the GPMC output clock (CLK), toggles only during the read or write access cycle. In some applications, it may be desirable to have a continuous clock running at the GPMC interface clock frequency for clocking attached devices. This option is enabled by an optional clock path from the GPMC functional clock input (GPMC_FCLK) to the GPMC_FCLK_MUX pin. This output clock, to GPMC_FCLK_MUX pin, can be selected through the standard MUXMODE selection of the GPMC_FCLK_MUX pin PADCONFIG control register.

Note that when using such synchronous interface protocols with the continuous clock option, user should ensure that the GPMC outputs are timed to the same frequency (GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0).

12.4.3.4.3 GPMC Power Management

Table 12-189 describes the local power-management features available for the GPMC module.

Table 12-201. GPMC Local Power-Management Features

Feature	Registers	Description
Clock autogating	*GPMC_SYSCONFIG*[0] AUTOIDLE	This bit allows a local power optimization inside the module, by gating the GPMC_ICLK clock upon the internal activity.
Target idle modes	*GPMC_SYSCONFIG*[4-3] SIDLEMODE	Force-idle, no-idle and smart-idle modes are available.

12.4.3.4.4 GPMC Interrupt Requests

The GPMC generates one interrupt request (see *GPMC0 Hardware Requests*).

Table 12-190 lists the event flags, and their mask, that can cause module interrupts.

Table 12-202. GPMC Interrupt Events

Event Flag	Event Mask	Sensitivity	Description
GPMC_IRQSTATUS[9] WAIT1EDGE DETECTIONSTATUS	GPMC_IRQENABLE[9] WAIT1EDGE DETECTIONENABLE	Edge	Wait1 edge detection interrupt: Triggered if a rising or falling edge is detected on the GPMC_WAIT1 signal. The rising or falling edge detection of Wait1 is selected through the GPMC_CONFIG[9] WAIT1PINPOLARITY bit.

Table 12-202. GPMC Interrupt Events (continued)

Event Flag	Event Mask	Sensitivity	Description
GPMC_IRQSTATUS[8] WAIT0EDGE DETECTIONSTATUS	GPMC_IRQENABLE[8] WAIT0EDGE DETECTIONENABLE	Edge	Wait0 edge detection interrupt: Triggered if a rising or falling edge is detected on the GPMC_WAIT0 signal. The rising or falling edge detection of Wait0 is selected through the GPMC_CONFIG[8] WAIT0PINPOLARITY bit.
GPMC_IRQSTATUS[1] TERMINAL COUNTSTATUS	GPMC_IRQENABLE[1] TERMINAL COUNTENABLE	Level	Terminal count event: Triggered on prefetch process completion; that is, when the number of currently remaining data to be requested reaches 0.
GPMC_IRQSTATUS[0] FIFOEVENTSTATUS	GPMC_IRQENABLE[0] FIFOEVENTENABLE	Level	FIFO event interrupt: Indicates available FIFO levels for write-posting mode and prefetch mode. GPMC_PREFETCH_CONFIG1[2] DMAMODE must be set to 0.

12.4.3.4.5 GPMC Interconnect Port Interface

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The GPMC interconnect interface is a pipelined interface including a 16 × 32-bit word write buffer.

Any system host can issue external access requests through the GPMC.

The device system can issue the following requests through this interface:

- One 8-, 16-, or 32-bit interconnect access (read/write)
- Two incrementing 32-bit interconnect accesses (read/write)
- Two wrapped 32-bit interconnect accesses (read/write)
- Four incrementing 32-bit interconnect accesses (read/write)
- Four wrapped 32-bit interconnect accesses (read/write)
- Eight incrementing 32-bit interconnect accesses (read/write)
- Eight wrapped 32-bit interconnect accesses (read/write)

Only linear burst transactions are supported; interleaved burst transactions are not supported. Only power-of-two-length precise bursts 2 × 32, 4 × 32, 8 × 32, and 16 × 32, with the burst base address aligned on the total burst size, are supported (this limitation applies to incrementing bursts only).

This interface also provides one interrupt and one DMA request line for specific event control.

It is recommended to program the *GPMC_CONFIG1_i*[24-23] ATTACHEDDEVICEPAGELENGTH bit field according to the page length of the effective attached device and to enable the *GPMC_CONFIG1_i*[31] WRAPBURST bit if the attached device supports wrapping burst.

It is possible, however, to emulate wrapping burst on a nonwrapping memory by providing relevant addresses within the page or by splitting transactions. Bursts larger than the memory page length are chopped into multiple burst transactions. Because of the alignment requirements, a page boundary is never crossed.

12.4.3.4.6 GPMC Address and Data Bus

The current application supports GPMC connection to NAND devices and to address/data-multiplexed memories or devices. Connection to address/data-non-multiplexed memories or devices is supported with an address range of 256MB.

Depending on the GPMC configuration of each chip-select, address and data bus lines that are not required for a particular access protocol are not updated (changed from current value) and are not sampled when input (input data bus).

- For address/data-multiplexed and AAD-multiplexed NOR devices, the address is multiplexed on the data bus.

- 8-bit-wide NOR devices do not use GPMC I/O: GPMC_AD[15-8] for data (they are used for address if needed).
- 16-bit-wide NAND devices do not use GPMC I/O: GPMC_A[22-0].
- 8-bit-wide NAND devices do not use GPMC I/O: GPMC_A[22-0] and GPMC I/O: GPMC_AD[15-8].

12.4.3.4.6.1 GPMC I/O Configuration Setting

Note

In this section and the following sections, the i in GPMC_CONFIGx_i stands for the GPMC chip-select i, where i = 0 to 3.

To select a NAND device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b10
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b00

To select an address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b10

To select an address/address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b01

To select an address/data-non-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b00

12.4.3.4.7 GPMC Address Decoder and Chip-Select Configuration

Addresses are decoded accordingly with the address request of the chip-select and the content of the chip-select base address register file, which includes a set of global GPMC configuration registers and four sets of chip-select configuration registers.

The GPMC configuration register file is memory-mapped and can be read or written with byte, 16-bit word, or 32-bit word accesses. The register file must be configured as a noncacheable, nonbufferable region to prevent any desynchronization between host execution (write request) and the completion of register configuration (write completed with register updated).

After the chip-select is configured, the access engine accesses the external device, drives the external interface control signals, and applies the interface protocol based on user-defined timing parameters and settings.

12.4.3.4.7.1 Chip-Select Base Address and Region Size

Any external memory or ASIC device attached to the GPMC external interface can be accessed by any device system host within the GPMC 128MB address space. For more information, see *Memory Map*.

Note

Even though GPMC supports total address space of 1GB, only 128MB are physically available in this device.

The GPMC 128MB address space can be divided into a maximum of four chip-select regions with programmable base address and programmable chip-select size. The chip-select size is programmable from 16MB to 256MB (must be a power-of-two) and is defined by the mask field. Attached memory smaller than the programmed chip-select region size is accessed through the entire chip-select region (aliasing).

Each chip-select has a 6-bit base address encoding and 4-bit decoding mask, which must be programmed according to the following rules:

- The programmed chip-select region base address must be aligned on the chip-select region size address boundary and is limited to a power-of-two address value. During access decoding, the value of the register base address is used to compare the address with the address bit line mapping, as shown in Figure 12-171 (with A0 as the device system byte-address line). The base address is programmed through the GPMC_CONFIG7_i[5-0] BASEADDRESS bit field.
- The register mask is used to exclude some address lines from the decoding. A register mask bit field set to 0 suppresses the associated address line from the address comparison (incoming address bit line is don't care). The value of the register mask must be limited to the subsequent value, based on the desired chip-select region size. Any other value has an undefined result. When multiple chip-select regions with overlapping addresses are enabled concurrently, access to these chip-select regions is cancelled and a GPMC access error is posted. The mask field is programmed through the GPMC_CONFIG7_i[11-8] MASKADDRESS bit field.

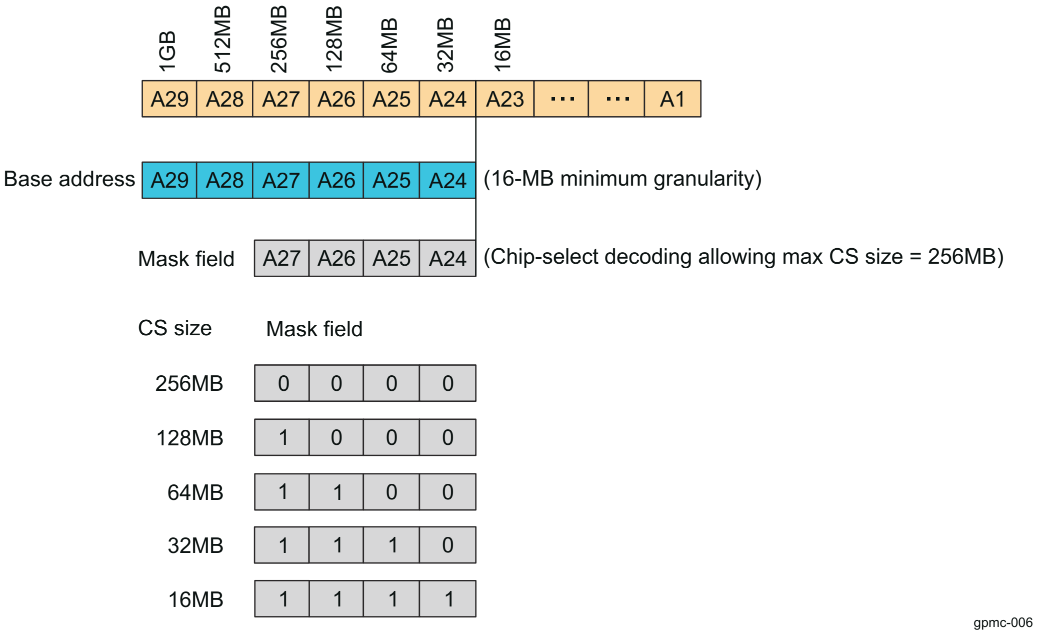

Figure 12-171. Chip-Select Address Mapping and Decoding Mask

For example, to map the 128MB address space (from 2000 0000h to 27FF FFFFh), the GPMC_CONFIG7_i[5-0] BASEADDRESS bit field should be set to 20h.

Chip-select configuration (base and mask address or any protocol and timing settings) must be performed while the associated chip-select is disabled through the GPMC_CONFIG7_i[6] CSVALID bit (where i stands for the GPMC chip-select i, where i = 0 to 3). In addition, a chip-select configuration can be disabled only if there is no ongoing access to that chip-select. This requires monitoring the activity of the prefetch or write-posting engine if the engine is active on the chip-select. Also, the write buffer state must be monitored to wait for any posted write completion to the chip-select.

Any access attempted to a nonvalid GPMC address region (CSVALID disabled or address decoding outside a valid chip-select region) is not propagated to the external interface and a GPMC access error is posted. In case of overlapping chip-selects, an error is generated and no access occurs on either chip-select.

CS0 is the only chip-select region enabled after a power up or GPMC reset.

CAUTION

Although the GPMC interface can drive up to four chip-selects, the frequency specified for this interface is for a specific load. If this load is exceeded, the maximum frequency cannot be reached. One solution is to implement a board with buffers to allow the slowest device to maintain the total load on the lines at the value specified in the device-specific Datasheet.

12.4.3.4.7.2 Access Protocol

12.4.3.4.7.2.1 Supported Devices

The access protocol of each chip-select can be independently specified through the *GPMC_CONFIG1_i*[11-10] DEVICETYPE parameter (where i = 0 to 3) for:

- Random-access synchronous or asynchronous memory, such as NOR flash and SRAM
- NAND flash asynchronous devices

Note

For more information about the NAND flash GPMC basic programming model and NAND support, see Section 12.4.3.4.11 , *GPMC NAND Device Basic Programming Model*, and Section 12.4.3.4.11.1 , *NAND Memory Device in Byte or Word16 Stream Mode*.

12.4.3.4.7.2.2 Access Size Adaptation and Device Width

Each chip-select can be independently configured through the *GPMC_CONFIG1_i*[13-12] DEVICESIZE bit field (where i = 0 to 3) to interface with a 16- or 8-bit-wide device. System requests with data width greater than the external device data bus width are split into successive accesses according to the external device data-bus width and little-endian data organization.

12.4.3.4.7.2.3 Address/Data-Multiplexing Interface

For random synchronous or asynchronous memory interfacing (DEVICETYPE = 0b00), an address- and data-multiplexing protocol can be selected through the *GPMC_CONFIG1_i*[9-8] MUXADDDATA bit field (where i = 0 to 3). The nADV signal must be used as the external device address latch control signal. For the associated chip-select configuration, nADV assertion and deassertion time and nOE assertion time must be set to the appropriate value to meet the address latch setup/hold time requirements of the external device. See *Module Integration*.

Note

This address/data-multiplexing interface is not applicable to NAND device interfacing. NAND devices require a specific address, command, and data-multiplexing protocol. See Section 12.4.3.4.11 , *NAND Device Basic Programming Model*.

12.4.3.4.7.3 External Signals

12.4.3.4.7.3.1 WAIT Pin Monitoring Control

GPMC access time can be dynamically controlled using an external GPMC_WAIT pin when the external device access time is not deterministic and cannot be defined and controlled using only the GPMC internal RDACCESSTIME, WRACCESSTIME, and PAGEBURSTACCESSTIME wait-state generator.

The GPMC features two input WAIT pins: GPMC_WAIT1, and GPMC_WAIT0. These pins allow control of external devices with different WAIT pin polarity. They also allow the overlap of WAIT pin assertion from different devices without affecting access to devices for which the WAIT pin is not asserted.

- The GPMC_CONFIG1_i[17-16] WAITPINSELECT bit field (where i = 0 to 3) selects which input GPMC_WAIT pin is used for the device attached to the corresponding chip-select.

- The polarity of the WAIT pin is defined through the WAITxPINPOLARITY bit of the GPMC_CONFIG register. A WAIT pin configured to be active low means that low level on the WAIT signal indicates that the data is not ready and that the data bus is invalid. When a WAIT pin is inactive, data is valid.

The GPMC access engine can be configured per chip-select to monitor or not the WAIT pin of the external memory device, based on the access type: read or write.

- The GPMC_CONFIG1_i[22] WAITREADMONITORING bit defines whether or not the WAIT pin must be monitored during read accesses.
- The GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit defines whether or not the WAIT pin must be monitored during write accesses.

The GPMC access engine can be configured to monitor the WAIT pin of the external memory device asynchronously or synchronously with the GPMC output clock, depending on the access type: synchronous or asynchronous (the GPMC_CONFIG1_i[29] READTYPE and GPMC_CONFIG1_i[27] WRITETYPE bits).

12.4.3.4.7.3.1.1 Wait Monitoring During Asynchronous Read Access

When WAIT pin monitoring is enabled for read accesses (WAITREADMONITORING), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state.

During asynchronous read accesses with WAIT pin monitoring enabled, the WAIT pin must be at a valid level (asserted or deasserted) for at least two GPMC clock cycles before RDACCESSTIME completes, to ensure correct dynamic access-time control through WAIT pin monitoring. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

In this context, RDACCESSTIME is used as a wait invalid timing window and is set to such a value that the WAIT pin is at a valid state two GPMC clock cycles before RDACCESSTIME completes.

Similarly, during a multiple-access cycle (for example, asynchronous read page mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the wait-deasserted state. Wait monitoring pipelining is also applicable to multiple accesses (access within a page).

- Wait monitored as active freezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as asserted extends the current access time in the page. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive completes the current access time and starts the next access phase in the page. The data bus is considered valid, and data are captured during this clock cycle. In case of a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their related control timing value and according to the CYCLETIME counter status.

When a delay larger than two GPMC clocks must be observed between wait-pin deactivation time and data valid time (including the required GPMC and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data-capture time and the effective unlock of the CYCLETIME counter. This extra delay can be programmed in the *GPMC_CONFIG1_i*[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3).

Note

- The WAITMONITORINGTIME parameter does not delay the WAIT pin active or inactive detection, nor does it modify the two GPMC clocks pipelined detection delay.
- This extra delay is expressed as a number of GPMC output clock cycles, even though the access is defined as asynchronous, and no GPMC output clock is provided to the external device. Still, because *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

Figure 12-172 shows wait behavior during an asynchronous single read access.

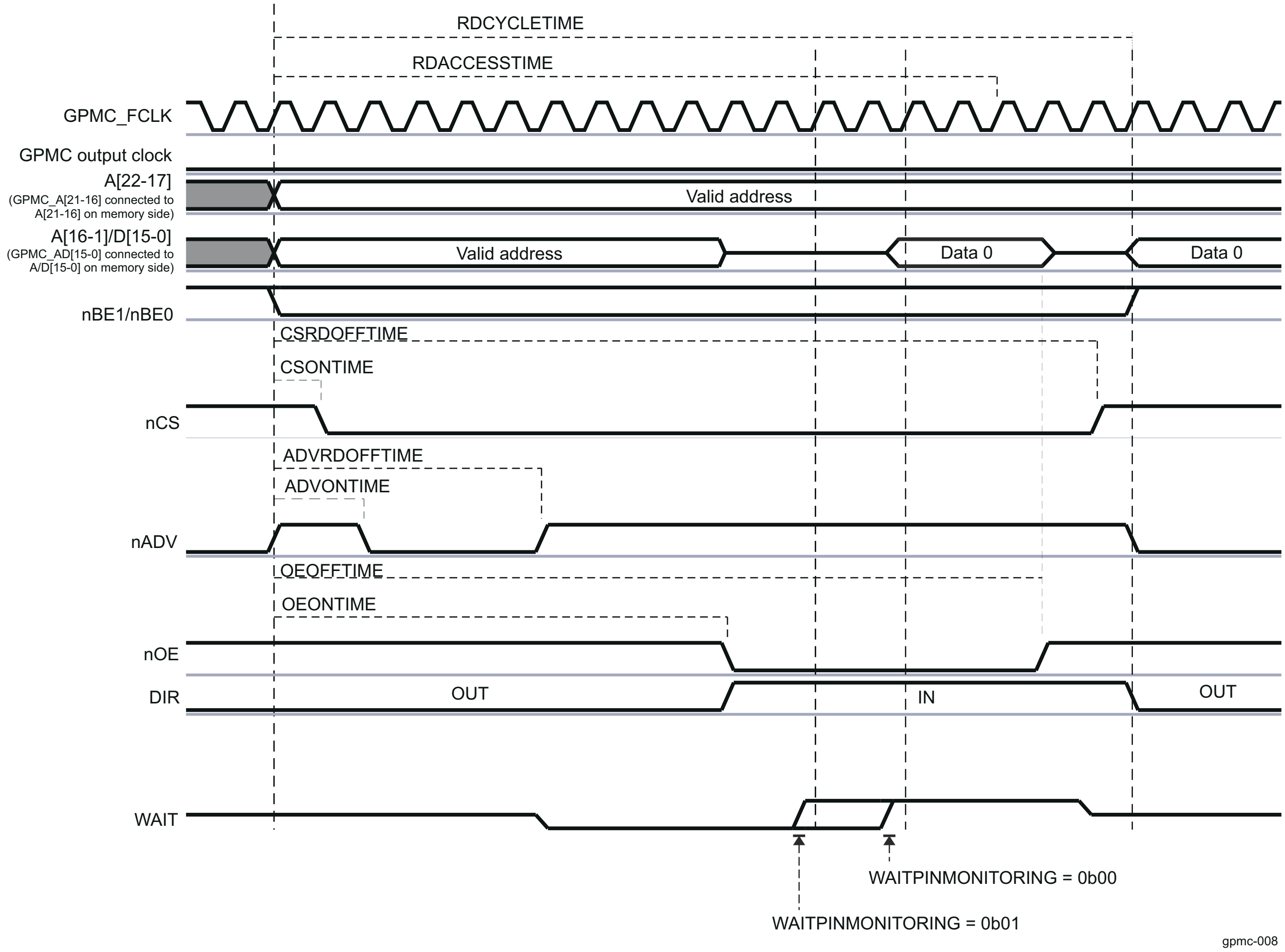

Figure 12-172. Wait Behavior During an Asynchronous Single Read Access (GPMCFCLKDivider = 1)

Note

The WAIT signal is active low. *GPMC_CONFIG1_i*[19-18] WAITMONITORINGTIME = 0b00, or 0b01.

12.4.3.4.7.3.1.2 Wait Monitoring During Asynchronous Write Access

When WAIT pin monitoring is enabled for write accesses (*GPMC_CONFIG1_i*[21] WAITWRITEMONITORING bit = 0x1), the wait invalid timing window is defined by the WRACCESSTIME field. WRACCESSTIME must be set so that the WAIT pin is at a valid state two GPMC clock cycles before WRACCESSTIME completes. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

- Wait monitored as active freezes the CYCLETIME counter. This informs the GPMC that the data bus is not captured by the external device. The control signals are kept in their current state. The data bus still drives the data.
- Wait monitored as inactive unfreezes the CYCLETIME counter. This informs that the data bus is correctly captured by the external device. All signals, including the data bus, are controlled according to their related control timing value and to the CYCLETIME counter status.

When a delay larger than two GPMC clock cycles must be observed between wait-pin deassertion time and the effective data write into the external device (including the required GPMC data setup time and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data write time into the external device and the effective unfreezing of the CYCLETIME counter. This extra delay can be programmed in the *GPMC_CONFIG1_i*[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3).

Note

- The WAITMONITORINGTIME parameter does not delay the WAIT pin assertion or deassertion detection, nor does it modify the two GPMC clock cycles pipelined detection delay.
- This extra delay is expressed as a number of GPMC output clock cycles, even though the access is defined as asynchronous, and even though no clock is provided to the external device. Still, because the *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER bit field is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

12.4.3.4.7.3.1.3 Wait Monitoring During Synchronous Read Access

During synchronous accesses with WAIT pin monitoring enabled, the WAIT pin is captured synchronously with GPMC output clock, using the rising edge of this clock.

The WAIT signal can be programmed to apply to the same clock cycle in which it is captured. Alternatively, it can be sampled one or two GPMC output clock cycles ahead of the clock cycle to which it applies. This pipelining is applicable to the entire burst access and to all data phases in the burst access. This wait pipelining depth is programmed in the GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3), and is expressed as a number of GPMC output clock cycles.

In synchronous mode, when WAIT pin monitoring is enabled (the GPMC_CONFIG1_i[22] WAITREADMONITORING bit), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state detection.

Depending on the programmed value of WAITMONITORINGTIME, the WAIT pin must be at a valid level, either asserted or deasserted:

- In the same clock cycle the data is valid if WAITMONITORINGTIME = 0 (at RDACCESSTIME completion)
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK clock cycles before RDACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Similarly, during a multiple-access cycle (burst mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the WAIT-INACTIVE state. The wait pipelining-depth programming applies to the whole burst access.

- Wait monitored as active freezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in a lock state), wait monitored as active extends the current access time in the burst. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in lock state), wait monitored as inactive completes the current access time and starts the next access phase in the burst. The data bus is considered valid, and data are captured during this clock cycle. In a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their relative control timing value and the CYCLETIME counter status.

Figure 12-173 shows wait behavior during a synchronous read burst access.

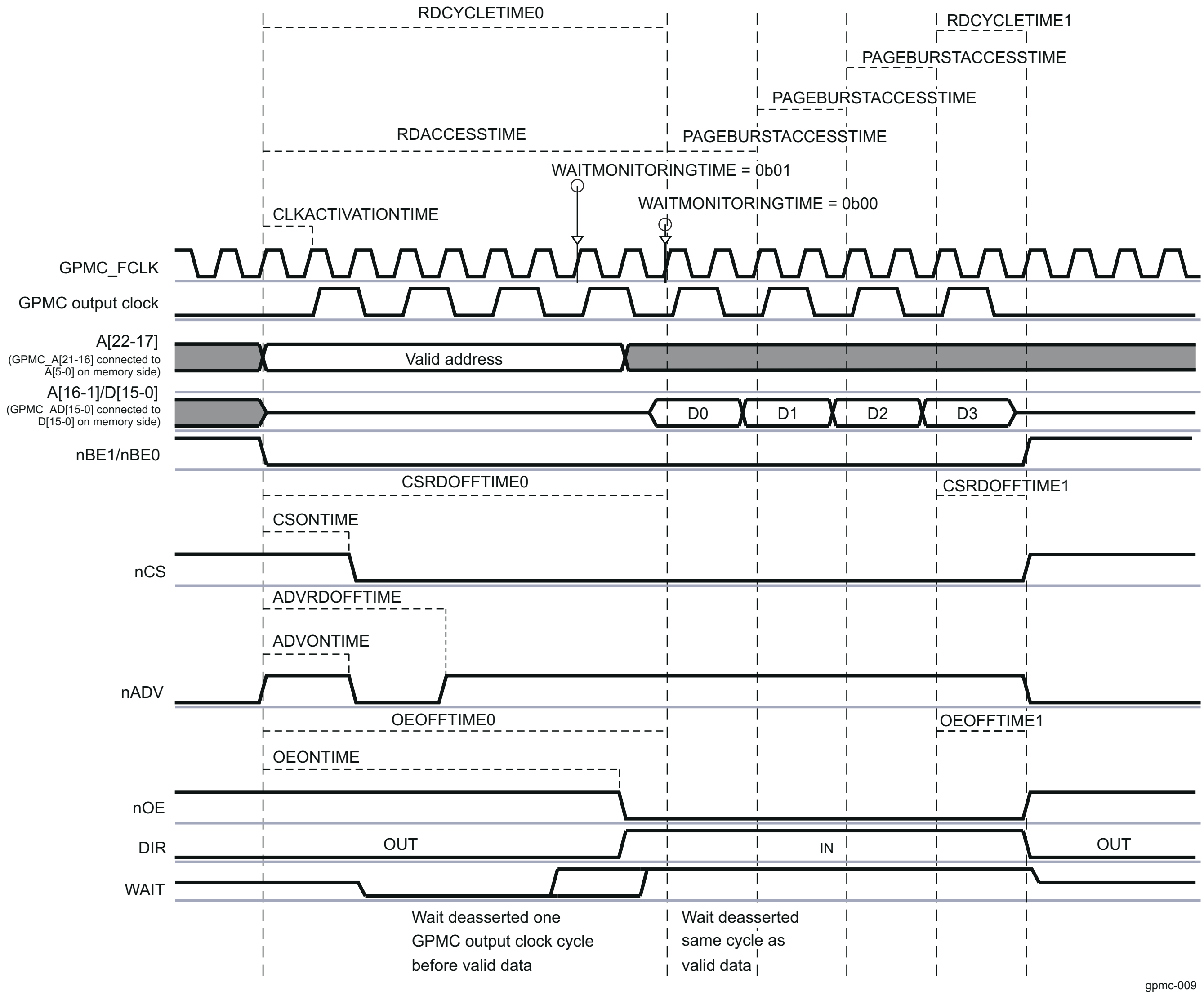

Figure 12-173. Wait Behavior During a Synchronous Read Burst Access

Note

The WAIT signal is active low. WAITMONITORINGTIME = 0b00, 0b01.

12.4.3.4.7.3.1.4 Wait Monitoring During Synchronous Write Access

During synchronous accesses with WAIT pin monitoring enabled (the *GPMC_CONFIG1_i*[21] WAITWRITEMONITORING bit), the WAIT pin is captured synchronously with GPMC output clock, using the rising edge of this clock.

If enabled, external WAIT pin monitoring can be used in combination with WRACCESSTIME to delay the GPMC output clock capture edge of the effective memory device.

WAIT-monitoring pipelining depth is similar to synchronous read access:

- At WRACCESSTIME completion if WAITMONITORINGTIME = 0
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK cycles before WRACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Wait-monitoring pipelining definition applies to whole burst accesses:

- Wait monitored as active freezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as active indicates that the data bus is not being captured by the external device. Control signals are kept in their current state. The data bus is kept in its current state.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive indicates the effective data capture of the bus by the external device and starts the next access of the burst. In case of a single access or if this was the last access in a multiple access cycle, all signals, including the data bus, are controlled according to their related control timing value and the CYCLETIME counter status.

Note

WAIT monitoring is supported for all configurations except *GPMC_CONFIG1_i*[19-18] WAITMONITORINGTIME = 0x0 (where i = 0 to 3) for write bursts with a clock divider of 1 or 2 (the *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER bit field is equal to 0x0 or 0x1, respectively).

12.4.3.4.7.3.1.5 Wait With NAND Device

For information about the use of the WAIT pin for communication with a NAND flash external device, see Section 12.4.3.4.11.2 , *NAND Device-Ready Pin*.

12.4.3.4.7.3.1.6 Idle Cycle Control Between Successive Accesses

12.4.3.4.7.3.1.6.1 Bus Turnaround (BUSTURNAROUND)

To prevent data-bus contention, an access that follows a read access to a slow memory/device must be delayed (in other words, control the nCS/nOE deassertion to data bus in high-impedance delay).

The bus turnaround is a time-out counter starting after nCS or nOE deassertion time, whichever occurs first, and delays the next access start-cycle time. The counter is programmed through the *GPMC_CONFIG6_i*[3-0] BUSTURNAROUND bit field (where i = 0 to 3).

After a read access to a chip-select with a nonzero BUSTURNAROUND, the next access is delayed until the BUSTURNAROUND delay completes, if the next access is one of the following:

- A write access to any chip-select (the same or different chip-select from which the data was read)
- A read access to a different chip-select than the chip-select from which the data was read access
- A read or write access to a chip-select associated with an address/data-multiplexed device

Note

Bus keeping starts after bus turnaround completion so that DIR changes from IN to OUT after bus turnaround. The bus does not have enough time to go into high-impedance even though it can be driven with the same value before bus turnaround timing.

BUSTURNAROUND delay runs in parallel with *GPMC_CONFIG6_i*[3-0] CYCLE2CYCLEDELAY bit field delays. BUSTURNAROUND is a timing parameter for the ending chip-select access, while CYCLE2CYCLEDELAY is a timing parameter for the following chip-select access. The effective minimum delay between successive accesses is driven by these delay timing parameters and by the access type of the following access (see Figure 12-174 through Figure 12-176).

Another way to prevent bus contention is to define an earlier nCS or nOE deassertion time for slow devices or to extend the value of RDCYCLETIME. Doing this prevents bus contention, but it also affects all accesses of this specific chip-select.

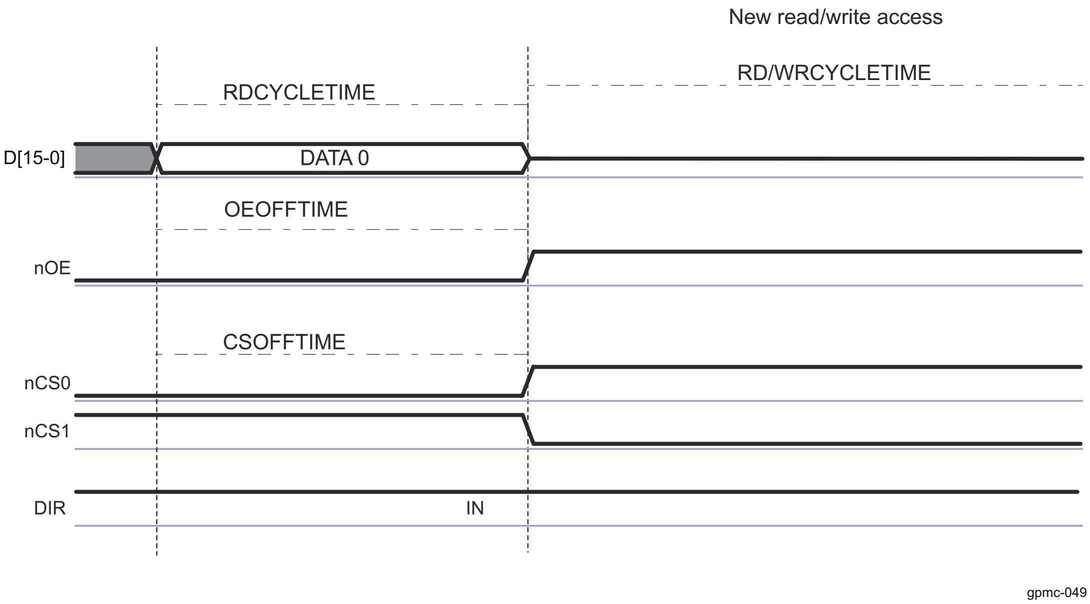

Figure 12-174. Read-to-Read for an Address-Data Multiplexed Device, on Different Chip-Select, Without Bus Turnaround (nCS Attached to a Fast Device)

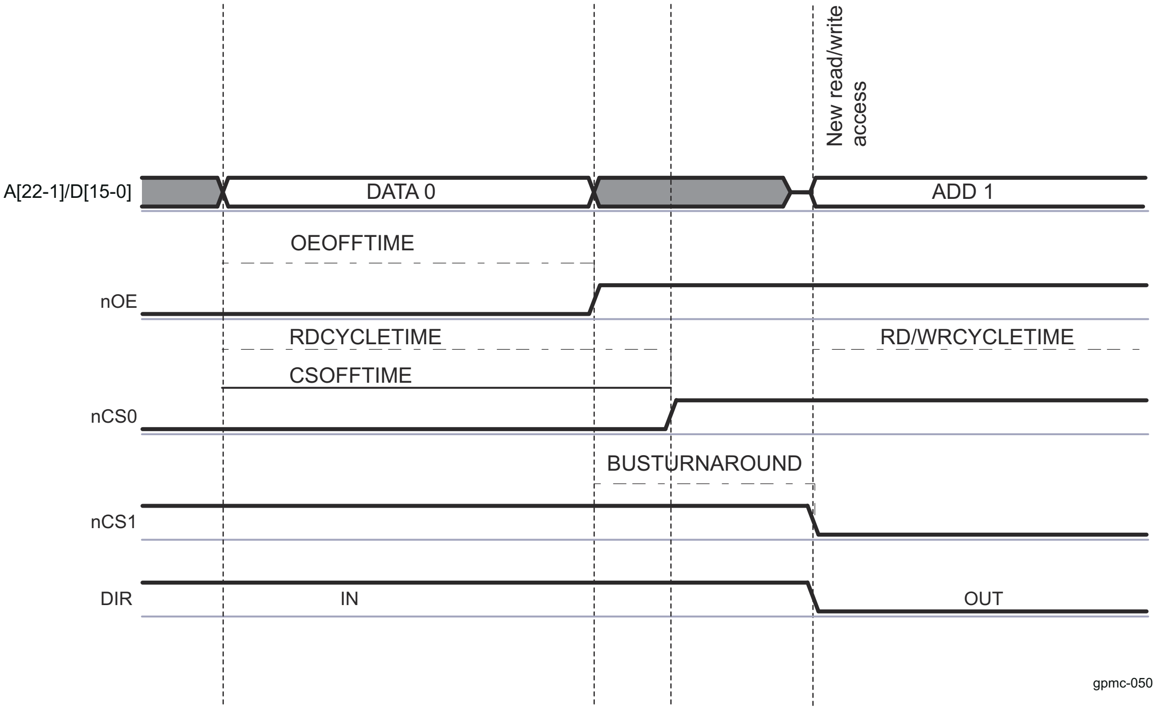

Figure 12-175. Read- to-Read/Write for an Address-Data Multiplexed Device, on Different Chip-Select, With Bus Turnaround

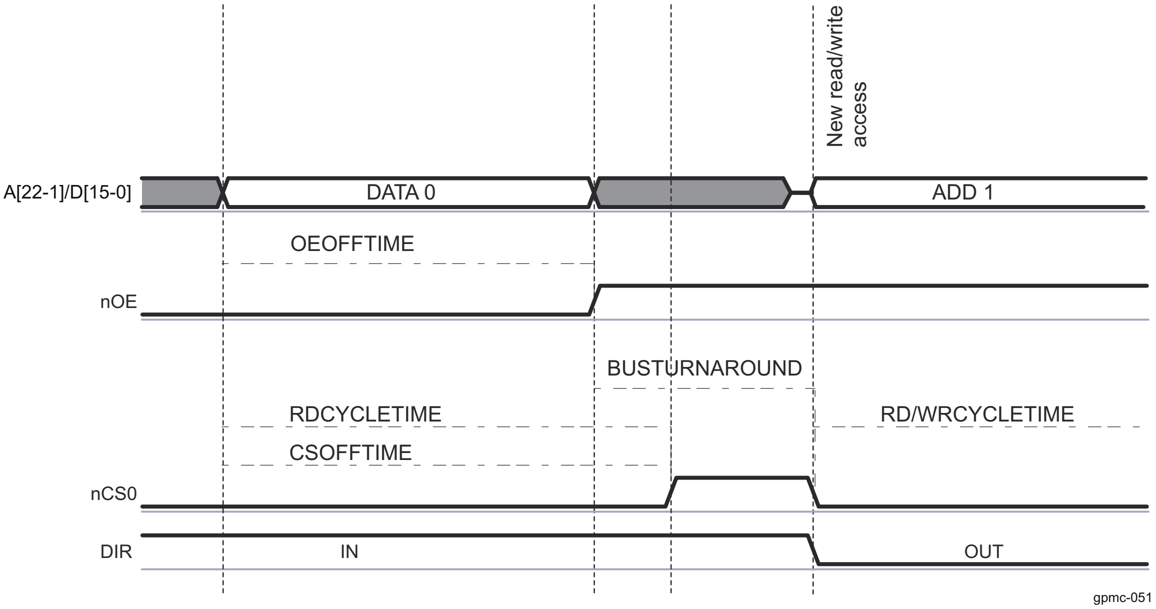

Figure 12-176. Read-to-Read/Write for a Address-Data or AAD-Multiplexed Device, on Same Chip-Select, With Bus Turnaround

12.4.3.4.7.3.1.6.2 Idle Cycles Between Accesses to Same Chip-Select (CYCLE2CYCLESAMECSEN, CYCLE2CYCLEDELAY)

Some devices require a minimum chip-select signal inactive time between accesses. The *GPMC_CONFIG6_i*[7] CYCLE2CYCLESAMECSEN bit (where i = 0 to 3) enables insertion of a minimum number of GPMC_FCLK cycles, defined by the *GPMC_CONFIG6_i*[11-8] CYCLE2CYCLEDELAY bit field, between successive accesses of any type (read or write) to the same chip-select.

If CYCLE2CYCLESAMECSEN is enabled, any subsequent access to the same chip-select is delayed until its CYCLE2CYCLEDELAY completes. The CYCLE2CYCLEDELAY counter starts when CSRDOFFTIME/ CSWROFFTIME completes.

The same applies to successive accesses occurring during 32-bit word or burst accesses split into successive single accesses when the single-access mode is used (*GPMC_CONFIG1_i*[30] READMULTIPLE = 0 or *GPMC_CONFIG1_i*[28] WRITEMULTIPLE = 0).

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC output clock (CLK)) are kept inactive (ADV#/ ALE, BE0#/CLE, and GPMC output clock at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC_FCLK cycles. This prevents back-to-back accesses to the same chip-select without idle cycles between accesses.

12.4.3.4.7.3.1.6.3 Idle Cycles Between Accesses to Different Chip-Select (CYCLE2CYCLEDIFFCSEN, CYCLE2CYCLEDELAY)

Because of the pipelined behavior of the system, successive accesses to different chip-selects can occur back-to-back with no idle cycles between accesses. Depending on the control signals (nCS, nADV/ALE, nBE0/ CLE, nOE/RE, nWE) assertion and deassertion timing parameters and on the device timing parameters, the assertion times of some control signals may overlap between the successive accesses to a different chip-select. Similarly, some control signals (WE, OE/RE) may not respect required transition times.

To work around overlapping and to observe the required control-signal transitions, a minimum of CYCLE2CYCLEDELAY inactive cycles is inserted between the access being initiated to this chip-select and the previous access ending for a different chip-select. This applies to any type of access (read or write).

If the *GPMC_CONFIG6_i*[6] CYCLE2CYCLEDIFFCSEN bit is enabled, the chip-select access is delayed until CYCLE2CYCLEDELAY cycles have expired since the end of a previous access to a different chip-select.

CYCLE2CYCLEDELAY count starts at CSRDOFFTIME/CSWROFFTIME completion. All control signals are kept inactive during the idle GPMC_FCLK cycles.

Note

CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDIFFCSEN must be set in the *GPMC_CONFIG6_i* registers to get idle cycles inserted between accesses on this chip-select and after accesses to a different chip-select, respectively.

The CYCLE2CYCLEDELAY delay runs in parallel with the BUSTURNAROUND delay. The BUSTURNAROUND is a timing parameter defined for the ending chip-select access, whereas CYCLE2CYCLEDELAY is a timing parameter defined for the starting chip-select access. The effective minimum delay between successive accesses is based on the larger delay timing parameter and on access type combination, because bus turnaround does not apply to all access types. For more information about bus turnaround, see Section 12.4.3.4.7.3.1.6.1 , *Bus Turnaround (BUSTURNAROUND)*.

Table 12-191 describes the configuration required for idle cycle insertion.

Table 12-203. Idle Cycle Insertion Configuration

1st Access Type	BUSTURNAROUND Timing Parameter	Second Access Type	Chip-Select	Add/Data Multiplexed	CYCLE2CYCLESAMECSEN Parameter	CYCLE2CYCLEDIFFCSEN Parameter	Idle Cycle Insertion Between the Two Accesses
R/W	= 0	R/W	Any	Any	0	x	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Same	Nonmuxed	x	0	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Different	Nonmuxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	R/W	Any	Muxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	W	Any	Any	0	0	BUSTURNAROUND cycles are inserted.
W	> 0	R/W	Any	Any	0	0	No idle cycles are inserted if the two accesses are well pipelined.
R/W	= 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted.
R/W	= 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted.
R/W	> 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is max (BUSTURNAROUND, CYCLE2CYCLEDELAY).
R/W	> 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is maximum (BUSTURNAROUND, CYCLE2CYCLEDELAY).

12.4.3.4.7.3.1.7 Slow Device Support (TIMEPARAGRANULARITY Parameter)

All access-timing parameters can be multiplied by 2 by setting the *GPMC_CONFIG1_i*[4] TIMEPARAGRANULARITY bit (where i stands for the GPMC chip-select i, where i = 0 to 3). Increasing all access timing parameters allows support of slow devices.

12.4.3.4.7.3.2 DIR Pin

The DIR pin is used to control I/O direction on the GPMC data bus GPMC_D[15-0]. Depending on pad multiplexing, this signal can be output and used externally to the device, if required. The DIR pin is low during transmit (OUT) and high during receive (IN).

For write accesses, the DIR pin stays OUT from start-cycle time to end-cycle time.

For read accesses, the DIR pin goes from OUT to IN at nOE assertion time and stays IN until:

- BUSTURNAROUND is enabled
  - The DIR pin goes from IN to OUT at end-cycle time plus programmable bus turnaround time.
- BUSTURNAROUND is disabled
  - After an asynchronous read access, the DIR pin goes from IN to OUT at RDACCESSTIME + 1 GPMC_FCLK cycle or when RDCYCLETIME completes, whichever occurs last.
  - After a synchronous read access, the DIR pin goes from IN to OUT at RDACCESSTIME + 2 GPMC_FCLK cycles or when RDCYCLETIME completes, whichever occurs last.

Because of the bus-keeping feature of the GPMC, after a read or write access and with no other accesses pending, the default value of the DIR pin is OUT (see Section 12.4.3.4.8.10 , *Bus Keeping Support*). In non-multiplexed devices, the DIR pin stays IN between two successive read accesses to prevent unnecessary toggling.

12.4.3.4.7.3.3 Reset

No reset signal is sent to the external memory device by the GPMC.

GPMC_RST is the reset signal for the GPMC module. It is connected and controlled by LPSC8 in VD_CORE. That reset signal initializes the internal state-machine and the internal configuration registers.

12.4.3.4.7.3.4 Write Protect Signal (nWP)

When connected to the attached memory device, the write protect signal can enable or disable the lockdown function of the attached memory. The nWP output pin value is controlled through the GPMC_CONFIG[4] WRITEPROTECT bit which is common for all chip selects.

12.4.3.4.7.3.5 Byte Enable (nBE1/nBE0)

Byte enable signals (nBE1/nBE0) are:

- Valid (asserted or nonasserted according to the incoming system request) from access start to access completion for asynchronous and synchronous single accesses
- Asserted low from access start to access completion for asynchronous and synchronous multiple read accesses
- Valid (asserted or nonasserted, according to the incoming system request) synchronously to each written data for synchronous multiple write accesses.

12.4.3.4.7.4 Error Handling

When an error occurs in the GPMC, the error information is stored in the GPMC_ERR_TYPE register and the address of the illegal access is stored in the GPMC_ERR_ADDRESS register. The GPMC keeps only the first error abort information until the GPMC_ERR_TYPE register is reset. Subsequent accesses that cause errors are not logged until the error is cleared by hardware with the GPMC_ERR_TYPE[0] ERRORVALID bit.

- ERRORNOTSUPPADD occurs when an incoming system request address decoding does not match any valid chip-select region, or if two chip-select regions are defined as overlapped, or if a register file access is tried outside the valid address range of 1KB.

- ERRORNOTSUPPMCMD occurs when an unsupported command request is decoded at the interconnect interface.
- ERRORTIMEOUT: A time-out mechanism prevents the system from hanging. The start value of the 9-bit time-out counter is defined in the GPMC_TIMEOUT_CONTROL register and enabled with the GPMC_TIMEOUT_CONTROL[0] TIMEOUTENABLE bit. When enabled, the counter starts at start-cycle time until it reaches 0 and data is not responded to from memory, and then a time-out error occurs. When data are sent from memory, this counter is reset to its start value. With multiple accesses (asynchronous page mode or synchronous burst mode), the counter is reset to its start value for each data access within the burst.

The GPMC does not generate interrupts on these errors. An interrupt generation is handled at interconnect level.

12.4.3.4.8 GPMC Timing Setting

The GPMC offers maximum flexibility to support various access protocols. Most of the timing parameters of the protocol access used by the GPMC to communicate with attached memories or devices are programmable on a chip-select basis. Assertion and deassertion times of control signals are defined to match the attached memory or device timing specifications and to get maximum performance during accesses. For more information about GPMC_CLKOUT and GPMC_FCLK, see Section 12.4.3.4.8.6 , *GPMC_CLKOUT*.

Note

In the following sections, the start access time refers to the time at which the access begins.

12.4.3.4.8.1 Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME)

The GPMC_CONFIG5_i[4-0] RDCYCLETIME and GPMC_CONFIG5_i[12-8] WRCYCLETIME bit fields (where i = 0 to 3) define the address bus and byte-enable valid times for read and write accesses. To ensure a correct duty cycle of GPMC output clock between accesses, RDCYCLETIME and WRCYCLETIME are expressed in GPMC_FCLK cycles and must be multiples of the GPMC output clock cycle. The RDCYCLETIME and WRCYCLETIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

When RDCYCLETIME or WRCYCLETIME completes, if they are not already deasserted, all control signals (nCS, nADV/ALE, nOE/RE, nWE, and BE0/CLE) are deasserted to their reset values, regardless of their deassertion time parameters.

An exception to this forced deassertion occurs when a pipelined request to the same chip-select or to a different chip-select is pending. In such a case, it is not necessary to deassert a control signal with deassertion time parameters equal to the cycle-time parameter. This exception to forced deassertion prevents any unnecessary glitches. This requirement also applies to BE signals, thus avoiding an unnecessary BE glitch transition when pipelining requests.

Note

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC output clock) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC output clock at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC_FCLK cycles.

If no inactive cycles are required between successive accesses to the same chip-select or a different chip-select (GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN = 0 or GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN = 0, where i = 0 to 3), and if assertion-time parameters associated with the pipelined access are equal to 0, asserted control signals (nCS, nADV/ALE, nBE0/CLE, nWE, and nOE/RE) are kept asserted. This applies to any read/write to read/write access combination.

If inactive cycles are inserted between successive accesses (that is, CYCLE2CYCLESAMECSEN = 1 or CYCLE2CYCLEDIFFCSEN = 1), the control signals are forced to their respective default reset values for the number of GPMC_FCLK cycles defined in CYCLE2CYCLEDELAY.

12.4.3.4.8.2 nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY)

The GPMC_CONFIG2_i[3-0] CSONTIME bit field (where i = 0 to 3) defines the nCS signal-assertion time relative to the start access time. It is common for read and write accesses.

The GPMC_CONFIG2_i[12-8] CSRDOFFTIME (read access) and GPMC_CONFIG2_i[20-16] CSWROFFTIME (write access) bit fields define the nCS signal deassertion time relative to start access time.

The CSONTIME, CSRDOFFTIME, and CSWROFFTIME parameters apply to synchronous and asynchronous modes. CSONTIME can be used to control an address and byte-enable setup time before chip-select assertion. CSRDOFFTIME and CSWROFFTIME can be used to control an address and byte-enable hold time after chip-select deassertion.

nCS signal transitions, as controlled through CSONTIME, CSRDOFFTIME, and CSWROFFTIME, can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG2_i[7] CSEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nCS assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. CSEXTRADELAY is especially useful in configurations where GPMC output clock and GPMC_FCLK have the same frequency, but it can also be used for all GPMC configurations. If enabled, CSEXTRADELAY applies to all parameters that control nCS transitions.

The CSEXTRADELAY bit must be used carefully to avoid control signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than the nCS signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

12.4.3.4.8.3 nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME)

The *GPMC_CONFIG3_i*[3-0] ADVONTIME field (where i = 0 to 3) defines the nADV/ALE signal-assertion time relative to start access time. It is common to read and write accesses.

The *GPMC_CONFIG3_i*[12-8] ADVRDOFFTIME (read access) and *GPMC_CONFIG3_i*[20-16] ADVWROFFTIME (write access) bit fields define the nADV/ALE signal-deassertion time relative to start access time.

ADVONTIME can be used to control an address and byte-enable valid setup time control before nADV/ALE assertion. ADVRDOFFTIME and ADVWROFFTIME can be used to control an address and byte-enable valid hold time control after nADV/ALE deassertion. ADVRDOFFTIME and ADVWROFFTIME apply to synchronous and asynchronous modes.

The nADV/ALE signal transitions as controlled through ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME can be delayed by a half-GPMC_FCLK period by enabling the *GPMC_CONFIG3_i*[7] ADVEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nADV/ALE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. The ADVEXTRADELAY configuration parameter is especially useful in configurations where GPMC output clock and GPMC_FCLK have the same frequency, but can be used for all GPMC configurations. If enabled, ADVEXTRADELAY applies to all parameters controlling nADV/ALE transitions.

ADVEXTRADELAY must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than nADV/ALE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME, *GPMC_CONFIG3_i*[26-24] ADVAADMUXRDOFFTIME, and *GPMC_CONFIG3_i*[30-28] ADVAADMUXWROFFTIME parameters have the same functions as ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME, but apply to the first address phase in the AAD-multiplexed protocol. The user must ensure that ADVAADMUXxxOFFTIME is programmed to a value less than or equal to ADVxxOFFTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. ADVAADMUXxxOFFTIME can be programmed to the same value as ADVONTIME if no high nADV pulse is needed between the two AAD-multiplexed address phases, which is the typical case in synchronous mode. In this configuration, nADV is kept low until it reaches the correct ADVxxOFFTIME.

For more information about the use of ADVONTIME, ADVRDOFFTIME, ADVWROFFTIME, and ADVAADMUXRDOFFTIME and ADVAADMUXWROFFTIME for command latch enable (CLE) and address latch enable (ALE) use for a NAND flash interface, see Section 12.4.3.4.11 , *GPMC NAND Access Description*.

12.4.3.4.8.4 nOE/nRE: Output Enable/Read Enable Signal Control Assertion/Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME)

The GPMC_CONFIG4_i[3-0] OEONTIME bit field (where i = 0 to 3) defines the nOE/nRE signal assertion time relative to start access time. It applies only to read accesses.

The GPMC_CONFIG4_i[12-8] OEOFFTIME bit field defines the nOE/nRE signal deassertion time relative to start access time. It applies only to read accesses. nOE/nRE is not asserted during a write cycle.

The OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME parameters apply to synchronous and asynchronous modes. OEONTIME can be used to control an address and byte enable valid setup time control before nOE/nRE assertion. OEOFFTIME can be used to control an address and byte-enable valid hold time control after nOE/nRE assertion.

The OEAADMUXONTIME and OEAADMUXOFFTIME parameters have the same functions as OEONTIME and OEOFFTIME, but apply to the first OE assertion in the AAD-multiplexed protocol for a read phase, or to the only OE assertion for a write phase. The user mut ensure that OEAADMUXOFFTIME is programmed to a value less than OEONTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. OEAADMUXOFFTIME must never be equal to OEONTIME because the AAD-multiplexed protocol requires a second address phase with the nOE signal deasserted before nOE can be asserted again to define a read command.

The nOE/RE signal transitions as controlled through OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[7] OEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nOE/RE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. If enabled, OEEXTRADELAY applies to all parameters controlling nOE/nRE transitions.

OEEXTRADELAY must be used carefully, to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program RDCYCLETIME and WRCYCLETIME to be greater than the nOE/RE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

Note

When the GPMC generates a read access to an address-/data-multiplexed device, it drives the address bus until nOE assertion time.

12.4.3.4.8.5 nWE: Write Enable Signal Control Assertion/Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY)

The GPMC_CONFIG4_i[19-16] WEONTIME bit field (where i = 0 to 3) defines the nWE signal-assertion time relative to start access time. The GPMC_CONFIG4_i[28-24] WEOFFTIME bit field defines the nWE signal-deassertion time relative to start access time. These bit fields apply only to write accesses. nWE is not asserted during a read cycle.

WEONTIME can be used to control an address and byte-enable valid setup time control before nWE assertion. WEOFFTIME can be used to control an address and byte-enable valid hold time control after nWE assertion.

nWE signal transitions as controlled through WEONTIME, and WEOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[23] WEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nWE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. If enabled, WEEXTRADELAY applies to all parameters controlling nWE transitions.

The WEEXTRADELAY bit must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the WRCYCLETIME bit field to be greater than the nWE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

12.4.3.4.8.6 GPMC_CLKOUT

The GPMC output clock generated for external synchronous memory or device is GPMC_CLKOUT.

- The GPMC_CLKOUT clock frequency is the GPMC_FCLK functional clock frequency divided by 1, 2, 3, or 4, depending on the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field (where i = 0 to 3), with a guaranteed 50-percent duty cycle. For information about the duty cycle error, see the device-specific Datasheet.
- The GPMC_CLKOUT clock is activated only when the access in progress is defined as synchronous (read or write access).
- The GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME bit field (where i = 0 to 3) defines the number of GPMC_FCLK cycles from start access time to GPMC_CLKOUT activation.
- The GPMC_CLKOUT clock is stopped when cycle time completes and is asserted low between accesses.
- The GPMC_CLKOUT clock is kept low when access is defined as asynchronous.

CAUTION

When the cycle time completes, the GPMC_CLKOUT may be high because of the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field. To ensure correct stoppage of the GPMC_CLKOUT clock within the required 50-percent duty cycle, the user must extend the RDCYCLETIME or WRCYCLETIME value.

Note

To ensure a correct external clock cycle, the following rules must be applied:

- (RDCYCLETIME CLKACTIVATIONTIME) must be a multiple of (GPMCFCLKDIVIDER + 1).
- The PAGEBURSTACCESSTIME value must be a multiple of (GPMCFCLKDIVIDER + 1).

12.4.3.4.8.7 GPMC Output Clock and Control Signals Setup and Hold

Control-signal transition (assertion and deassertion) setup and hold values with respect to the GPMC output clock edge can be controlled in the following ways:

- For the GPMC output clock signal, the GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME bit field (where i = 0 to 3) allows setup and hold control of control-signal assertion time.
- The use of a divided GPMC output clock allows setup and hold control of the control-signal assertion and deassertion times.
- When the GPMC output clock runs at the GPMC_FCLK frequency so that GPMC output clock edge and control-signal transitions refer to the same GPMC_FCLK edge, the control-signal transitions can be delayed by a half-GPMC_FCLK period to provide minimum setup and hold times. This half-GPMC_FCLK delay is enabled with the CSEXTRADELAY, ADVEXTRADELAY, OEEXTRADELAY, or WEEXTRADELAY parameter. This delay must be used carefully to prevent control-signal overlap between successive accesses to different chip-selects. This implies that the RDCYCLETIME and WRCYCLETIME are greater than the last control-signal deassertion time, including the extra half-GPMC_FCLK cycle.

12.4.3.4.8.8 Access Time (RDACCESSTIME / WRACCESSTIME)

The read/write access time durations can be programmed independently through the GPMC_CONFIG5_i[20-16] RDACCESSTIME and GPMC_CONFIG6_i[28-24] WRACCESSTIME bit fields (where i = 0 to 3). This allows nOE and GPMC data-capture timing parameters to be independent of nWE and memory device data capture timing parameters. The RDACCESSTIME and WRACCESSTIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

12.4.3.4.8.8.1 Access Time on Read Access

In asynchronous read mode, for single and paged accesses, the GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field (where i = 0 to 3) defines the number of GPMC_FCLK cycles from start access time to the GPMC_FCLK rising edge used for the first data capture. RDACCESSTIME must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached memory device.

In synchronous read mode, for single or burst accesses, RDACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC_FCLK rising edge corresponding to the GPMC output clock rising edge used for the first data capture.

GPMC output clock, which is sent to the memory device for synchronization with the GPMC controller, is internally retimed to correctly latch the returned data. The GPMC_CONFIG5_i[4-0] RDCYCLETIME bit field must be greater than RDACCESSTIME to let the GPMC latch the last return data using the internally retimed GPMC output clock.

The external WAIT signal can be used in conjunction with RDACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access in asynchronous and synchronous modes. For more information about wait monitoring, see Section 12.4.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.4.3.4.8.8.2 Access Time on Write Access

In asynchronous write mode, the GPMC_CONFIG6_i[28-24] WRACCESSTIME timing parameter is not used to define the effective write access time. Instead, it is used as a wait invalid timing window and must be set to a correct value so that the GPMC_WAIT pin is at a valid state two GPMC output clock cycles before WRACCESSTIME completes. For more information about wait monitoring, see Section 12.4.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

In synchronous write mode, for single or burst accesses, WRACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC output clock rising edge used by the memory device for the first data capture.

The external WAIT signal can be used in conjunction with WRACCESSTIME to control the effective memory device data-capture GPMC output clock edge for a synchronous write access. For more information about wait monitoring, see Section 12.4.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.4.3.4.8.9 Page Burst Access Time (PAGEBURSTACCESSTIME)

The *GPMC_CONFIG5_i*[27-24] PAGEBURSTACCESSTIME bit field (where i = 0 to 3) can be set with a granularity of 1 or 2 through the *GPMC_CONFIG1_i*[4] TIMEPARAGRANULARITY bit.

12.4.3.4.8.9.1 Page Burst Access Time on Read Access

In asynchronous page read mode, the delay between successive word captures in a page is controlled through the PAGEBURSTACCESSTIME bit field. The PAGEBURSTACCESSTIME parameter must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached device.

In synchronous burst read mode, the delay between successive word captures in a burst is controlled through the PAGEBURSTACCESSTIME bit field.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access. For more information about wait monitoring, see Section 12.4.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.4.3.4.8.9.2 Page Burst Access Time on Write Access

Asynchronous page write mode is not supported. PAGEBURSTACCESSTIME is irrelevant in this case.

In synchronous burst write mode, PAGEBURSTACCESSTIME controls the delay between successive memory device word captures in a burst.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective memory device data capture GPMC output clock edge in synchronous write mode. For more information about wait monitoring, see Section 12.4.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.4.3.4.8.10 Bus Keeping Support

At the end cycle time of a read access, if no other access is pending, the GPMC drives the bus with the last data read after RDCYCLETIME completes to prevent bus floating and reduce power consumption.

After a write access, if no other access is pending, the GPMC keeps driving the data bus after WRCYCLETIME completes with the same data to prevent bus floating and power consumption.

12.4.3.4.9 GPMC NOR Access Description

For each chip-select configuration, the read access can be specified as asynchronous or synchronous access through the GPMC_CONFIG1_i[29] READTYPE bit (where i = 0 to 3). For each chip-select configuration, the write access can be specified as synchronous or asynchronous access through the GPMC_CONFIG1_i[27] WRITETYPE bit where (i = 0 to 3).

Asynchronous and synchronous read and write access time and related control signals are controlled through timing parameters that refer to GPMC_FCLK. The primary difference of synchronous mode is the availability of a configurable clock interface to control the external device. Synchronous mode also affects data-capture and wait-pin monitoring schemes in read access.

For more information about asynchronous and synchronous access, see the descriptions of GPMC output clock (CLK), RdAccessTime, WrAccessTime, and WAIT pin monitoring.

For more information about timing-parameter settings, see the sample timing diagrams in this chapter.

Note

The address bus and nBE[1-0] are fixed for the duration of a synchronous burst read access, but they are updated for each beat of an asynchronous page-read access.

12.4.3.4.9.1 Asynchronous Access Description

This section describes:

- Asynchronous single-read operation on an address/data multiplexed device
- Asynchronous single write operation on an address/data-multiplexed device
- Asynchronous single read operation on an AAD-multiplexed device
- Asynchronous single write operation on an AAD-multiplexed device
- Asynchronous multiple (page) read operation on a non-multiplexed device

In asynchronous operations GPMC output clock is not provided outside the GPMC and is kept low.

12.4.3.4.9.1.1 Access on Address/Data Multiplexed Devices

12.4.3.4.9.1.1.1 Asynchronous Single-Read Operation on an Address/Data Multiplexed Device

Figure 12-177 shows an asynchronous single read operation on an address/data-multiplexed device.

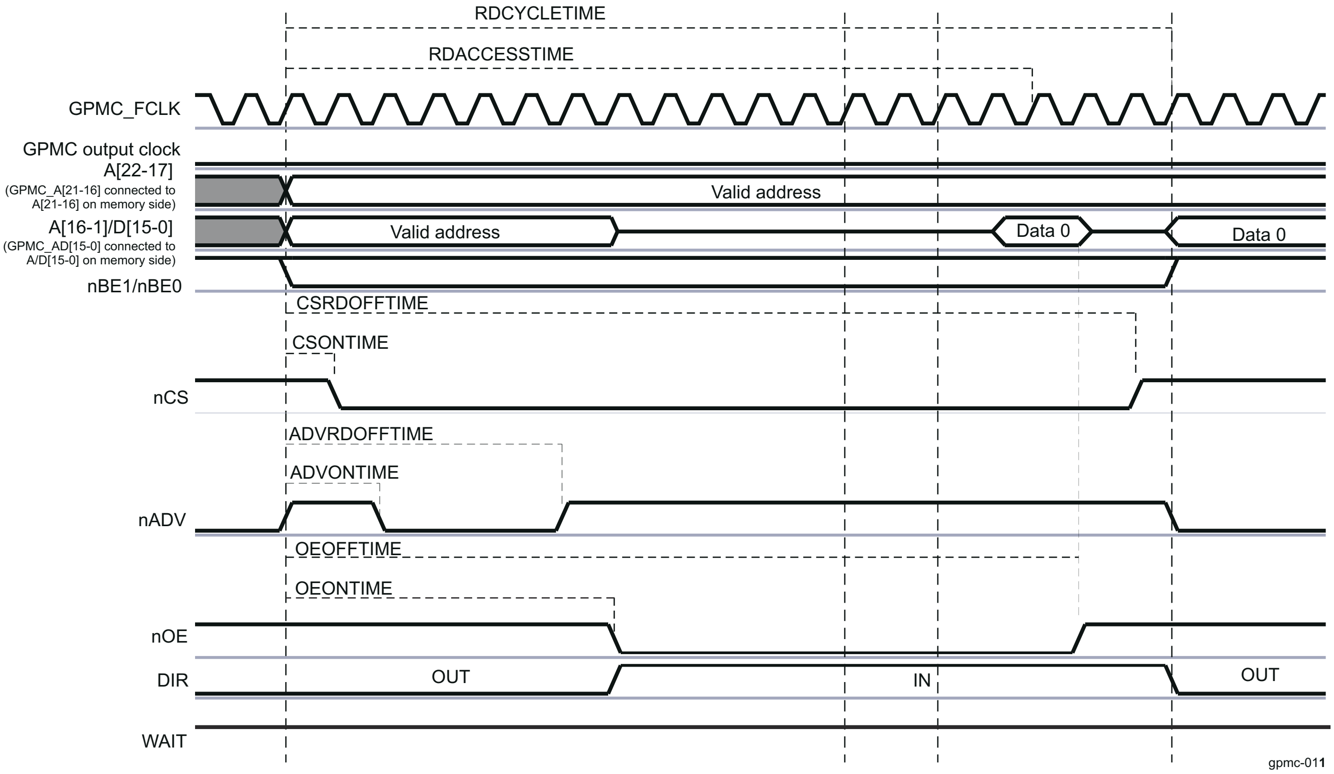

Figure 12-177. Asynchronous Single Read on an Address/Data-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.4.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-231 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.4.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

Address bits (A[16-1] from a GPMC perspective, A[15-0] from an external device perspective) are placed on the address/data bus, and the remaining address bits GPMC_A[22-16] are placed on the address bus. The address phase ends at nOE assertion, when the DIR signal goes from OUT to IN.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the *GPMC_CONFIG2_i*[3-0] CSONTIME bit field. It controls the address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12-8] CSRDOFFTIME bit field. It controls the address hold time from nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the *GPMC_CONFIG3_i*[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the *GPMC_CONFIG3_i*[12-8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the *GPMC_CONFIG4_i*[3-0] OEONTIME bit field.
  - nOE deassertion time is controlled by the *GPMC_CONFIG4_i*[12-8] OEOFFTIME bit field.
- Read data is latched when RDACCESSTIME completes. Access time is defined in the *GPMC_CONFIG5_i*[20-16] RDACCESSTIME bit field.
- Direction signal DIR: DIR goes from OUT to IN at the same time that nOE is asserted.
- The end of the access is defined by the
- GPMC_CONFIG5_i[4-0] RDCYCLETIME parameter.

In the GPMC, when a 16-bit wide device is attached to the controller, a 32-bit word write access is split into two 16-bit word write accesses. For more information about GPMC access size and type adaptation, see Section 12.4.3.4.9.5 , *System Burst Versus External Device Burst Support*.

Between two successive accesses, if an nCS pulse is needed:

- The *GPMC_CONFIG6_i*[11-8] CYCLE2CYCLEDELAY bit field can be programmed with the *GPMC_CONFIG6_i*[7] CYCLE2CYCLESAMECSEN bit enabled.
- The CSWROFFTIME and CSONTIME parameters also allow a chip-select pulse, but this affects all other types of access.

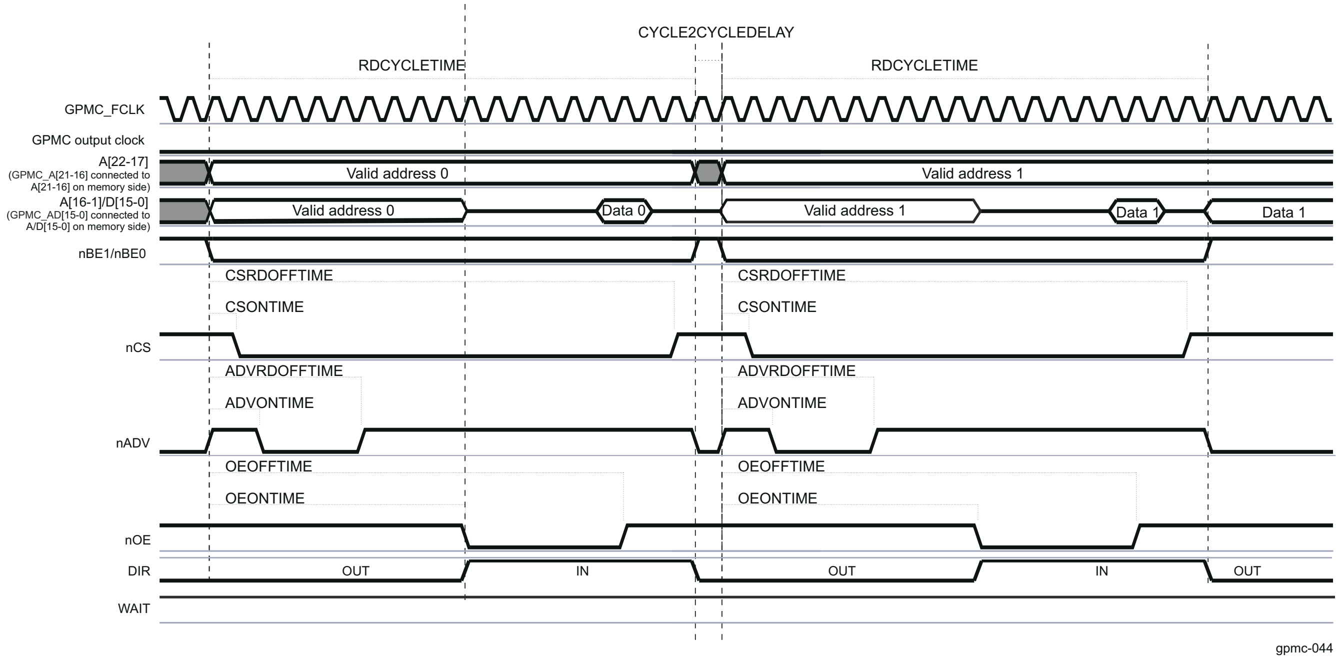

Figure 12-178. Two Asynchronous Single-Read Accesses on an Address/Data-Multiplexed Device (32-Bit Read Split Into 2 x 16-Bit Read)

12.4.3.4.9.1.1.2 Asynchronous Single-Write Operation on an Address/Data-Multiplexed Device

Figure 12-179 shows an asynchronous single-write operation on an address/data-multiplexed device.

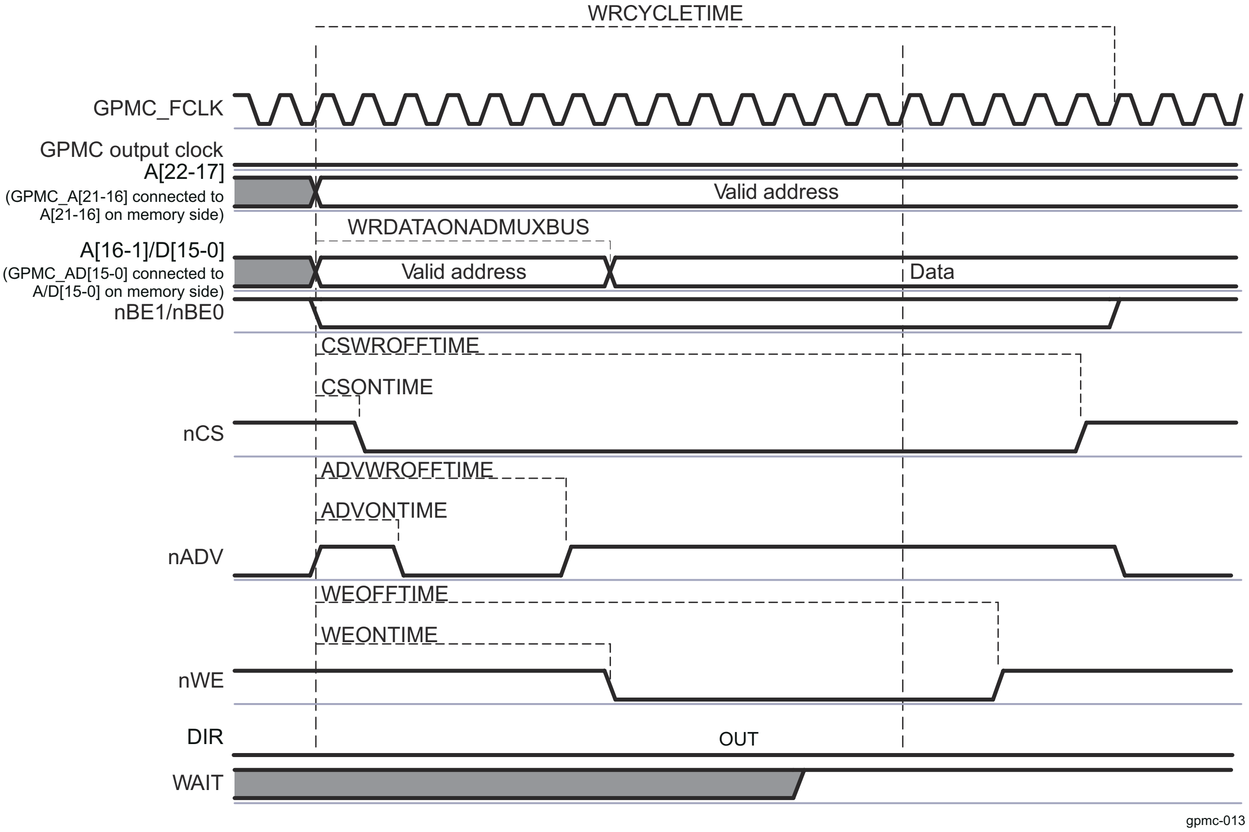

Figure 12-179. Asynchronous Single-Write on an Address/Data-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.4.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-231 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an address/data-multiplexed device, it drives the address bus until nWE assertion time. For more information, see Section 12.4.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

The nCS and nADV signals are controlled in the same way as for a asynchronous single-read operation on an address/data-multiplexed device.

- Write enable signal nWE:
  - nWE assertion indicates a write cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19-16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28-24] WEOFFTIME bit field.
- Direction signal DIR: DIR signal is OUT during the entire access.
- The end of the access is defined by the GPMC_CONFIG5_i[12-8] WRCYCLETIME parameter.

Address bits A[16-1] (GPMC point of view) are placed on the address/data bus at the start of cycle time, and the remaining address bits A[22-17] are placed on the address bus.

Data is driven on the address/data bus at a GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS time.

Note

Multiple write access in asynchronous mode is not supported. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

After a write operation, if no other access (read or write) is pending, the data bus keeps its previous value. See Section 12.4.3.4.8.10 , *Bus Keeping Support*.

12.4.3.4.9.1.1.3 Asynchronous Multiple (Page) Write Operation on an Address/Data-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for address/data-multiplexed devices.

If the *GPMC_CONFIG1_i*[28] WRITEMULTIPLE bit is enabled (0x1) with the *GPMC_CONFIG1_i*[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices, see Section 12.4.3.4.9.3 , *Asynchronous and Synchronous Accesses in non-multiplexed Mode*.

12.4.3.4.9.1.2 Access on Address/Address/Data-Multiplexed Devices

12.4.3.4.9.1.2.1 Asynchronous Single Read Operation on an AAD-Multiplexed Device

Figure 12-180 shows an asynchronous single-read operation on an AAD-multiplexed device.

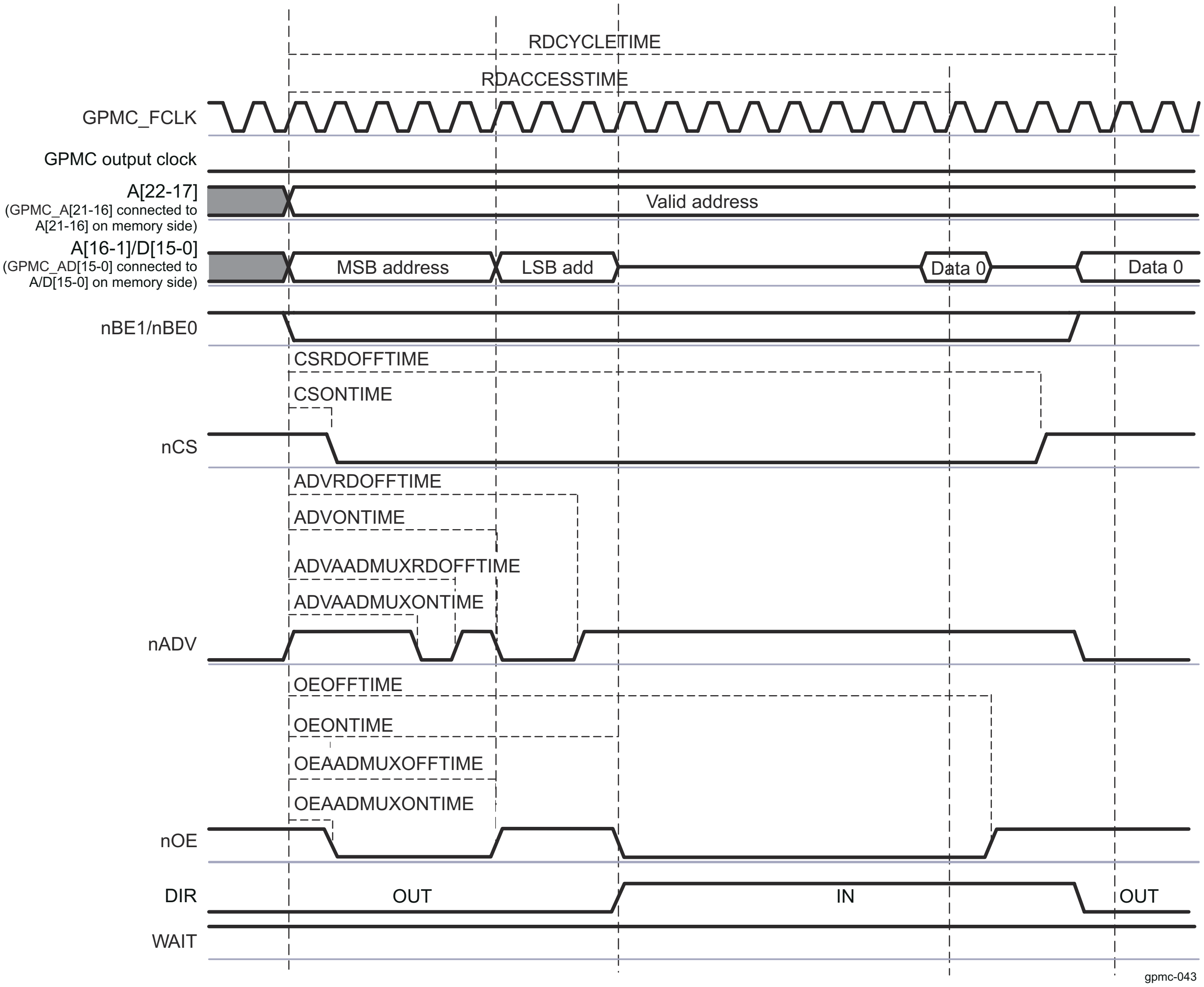

Figure 12-180. Asynchronous Single Read on an AAD-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.4.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-231 lists the timing bit fields to set up to configure the GPMC in asynchronous single write mode.

When the GPMC generates a read access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The first address phase ends at the first nOE deassertion time. The second phase for LSB address is qualified with nOE driven high. The second address phase ends at the second nOE assertion time, when the DIR signal goes from OUT to IN.

The nCS and DIR signals are controlled in the same way as for an asynchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV. nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the *GPMC_CONFIG3_i*[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the *GPMC_CONFIG3_i*[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the *GPMC_CONFIG3_i*[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the *GPMC_CONFIG3_i*[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE. nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the *GPMC_CONFIG4_i*[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the *GPMC_CONFIG3_i*[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the *GPMC_CONFIG4_i*[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the *GPMC_CONFIG4_i*[12-8] OEOFFTIME bit field.

12.4.3.4.9.1.2.2 Asynchronous Single-Write Operation on an AAD-Multiplexed Device

Figure 12-181 shows an asynchronous single-write operation on an AAD-multiplexed device.

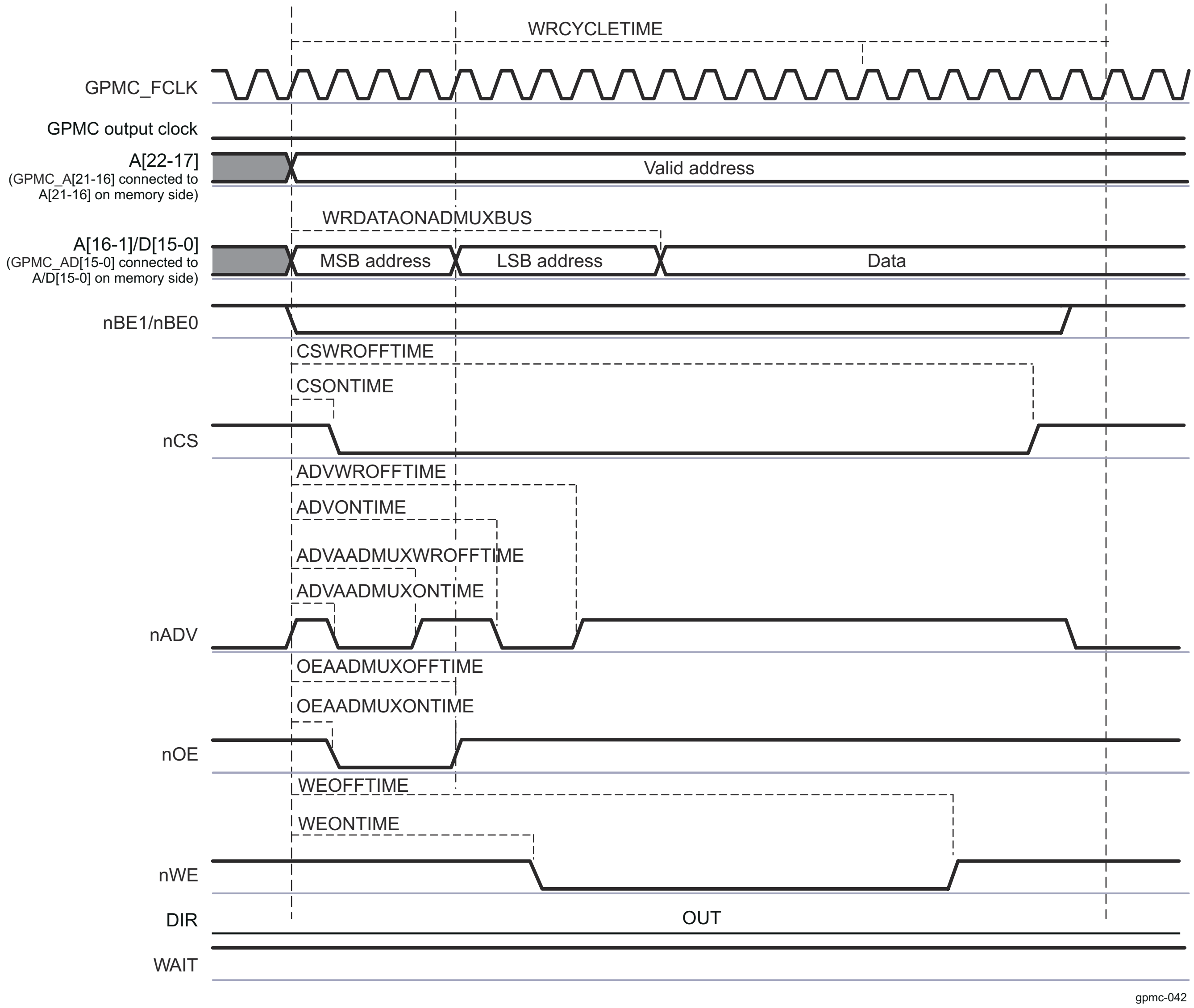

Figure 12-181. Asynchronous Single Write on an AAD-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.4.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-231 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, nWE, and DIR signals are controlled in the same way as for an asynchronous single-write operation on an address/data-multiplexed device. See Table 12-222, *NAND Memory Type*.

- Address valid signal nADV is asserted and deasserted twice during a write transaction:
  - nADV first assertion time is controlled by the *GPMC_CONFIG3_i*[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the *GPMC_CONFIG3_i*[30-28] ADVAADMUXWROFFTIME bit field.
  - nADV second assertion time is controlled by the *GPMC_CONFIG3_i*[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the *GPMC_CONFIG3_i*[20-16] ADVWROFFTIME bit field.
- Output enable signal nOE is asserted during the address phase of a write transaction:

  - nOE assertion time is controlled by the *GPMC_CONFIG4_i*[6-4] OEAADMUXONTIME bit field.
  - nOE deassertion time is controlled by the *GPMC_CONFIG3_i*[15-13] OEAADMUXOFFTIME bit field.

The address bits for the first address phase are driven onto the data bus until nOE deassertion. Data is driven onto the address/data bus at the clock edge defined by the *GPMC_CONFIG6_i*[19-16] WRDATAONADMUXBUS parameter.

12.4.3.4.9.1.2.3 Asynchronous Multiple (Page) Read Operation on an AAD-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for AAD-multiplexed devices.

If the GPMC_CONFIG1_i[28] WRITEMULTIPLE bit is enabled (0x1) with the GPMC_CONFIG1_i[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices, see Section 12.4.3.4.9.3 , *Asynchronous and Synchronous Accessed in non-multiplexed Mode*.

12.4.3.4.9.2 Synchronous Access Description

This section describes read and write synchronous accesses on address/data-multiplexed devices. All information in this section can be applied to any type of memory (non-multiplexed, address and data-multiplexed, or AAD-multiplexed) with the difference limited to the address phase. For accesses on non-multiplexed devices, see Section 12.4.3.4.9.3 , *Asynchronous and Synchronous Accessed in non-multiplexed Mode*.

In synchronous operations:

- The GPMC_CLKOUT clock is provided outside the GPMC when accessing the memory device.
- The GPMC_CLKOUT clock is derived from the GPMC_FCLK clock using the *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER bit field. In the following section i stands for the chip-select number, i = 0 to 3.
- The *GPMC_CONFIG1_i*[26-25] CLKACTIVATIONTIME bit field specifies that the GPMC_CLKOUT is provided outside the GPMC for 0 to 2 GPMC_FCLK cycles after start access time until RDCYCLETIME or WRCYCLETIME completes.

12.4.3.4.9.2.1 Synchronous Single Read

Figure 12-182 and Figure 12-183 show a synchronous single-read operation with GPMCFCLKDIVIDER equal to 0 and 1, respectively.

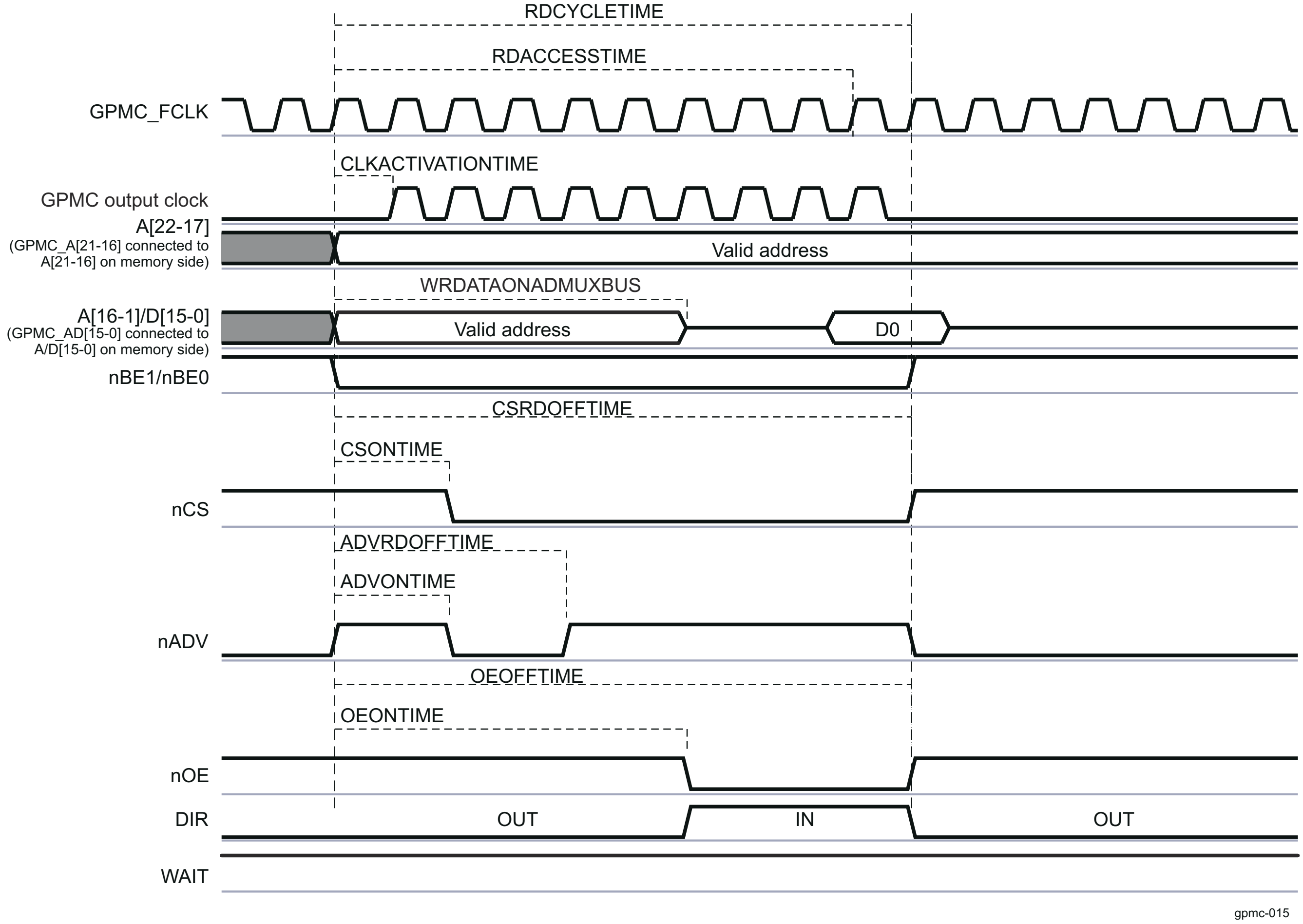

Figure 12-182. Synchronous Single Read (GPMCFCLKDIVIDER = 0)

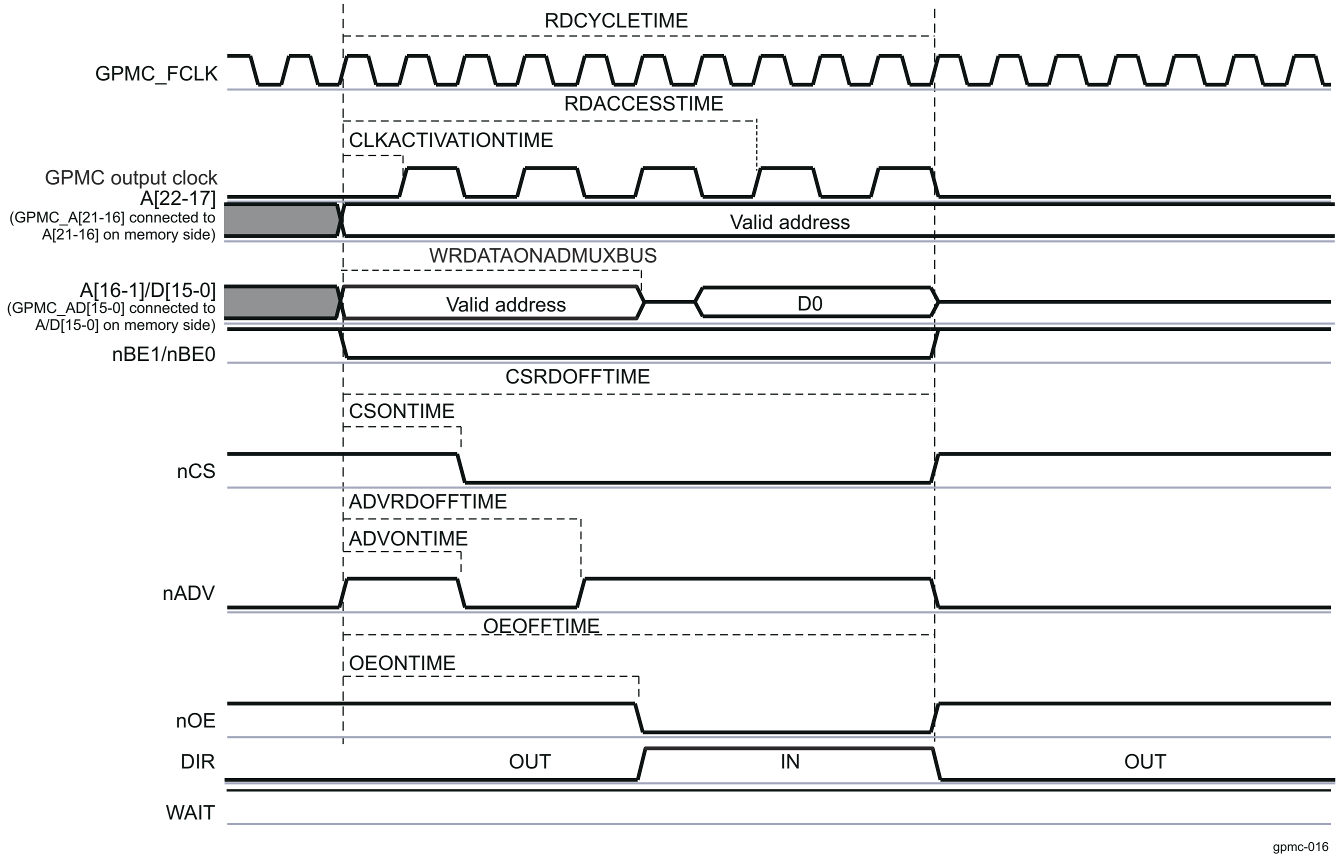

Figure 12-183. Synchronous Single Read (GPMCFCLKDIVIDER = 1)

For formulas to calculate timing parameters, see Section 12.4.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-231 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.4.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3-0] CSONTIME bit field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12-8] CSRDOFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.
- Initial latency for the first read data is controlled by GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field or by monitoring the WAIT signal.
- Total access time (the GPMC_CONFIG5_i[4-0] RDCYCLETIME bit field) corresponds to RDACCESSTIME plus the address hold time from nCS deassertion, plus time from RDACCESSTIME to CSRDOFFTIME.
- Direction signal DIR: DIR goes from OUT to IN at the same time as nOE assertion.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS and DIR signals are controlled in the same way as for a synchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 12.4.3.4.8.10 , *Bus Keeping Support*.

12.4.3.4.9.2.2 Synchronous Multiple (Burst) Read (4-, 8-, 16-Word16 Burst With Wraparound Capability)

Figure 12-184 and Figure 12-185 show a synchronous multiple-read operation with GPMCFCLKDivider equal to 0 and 1, respectively.

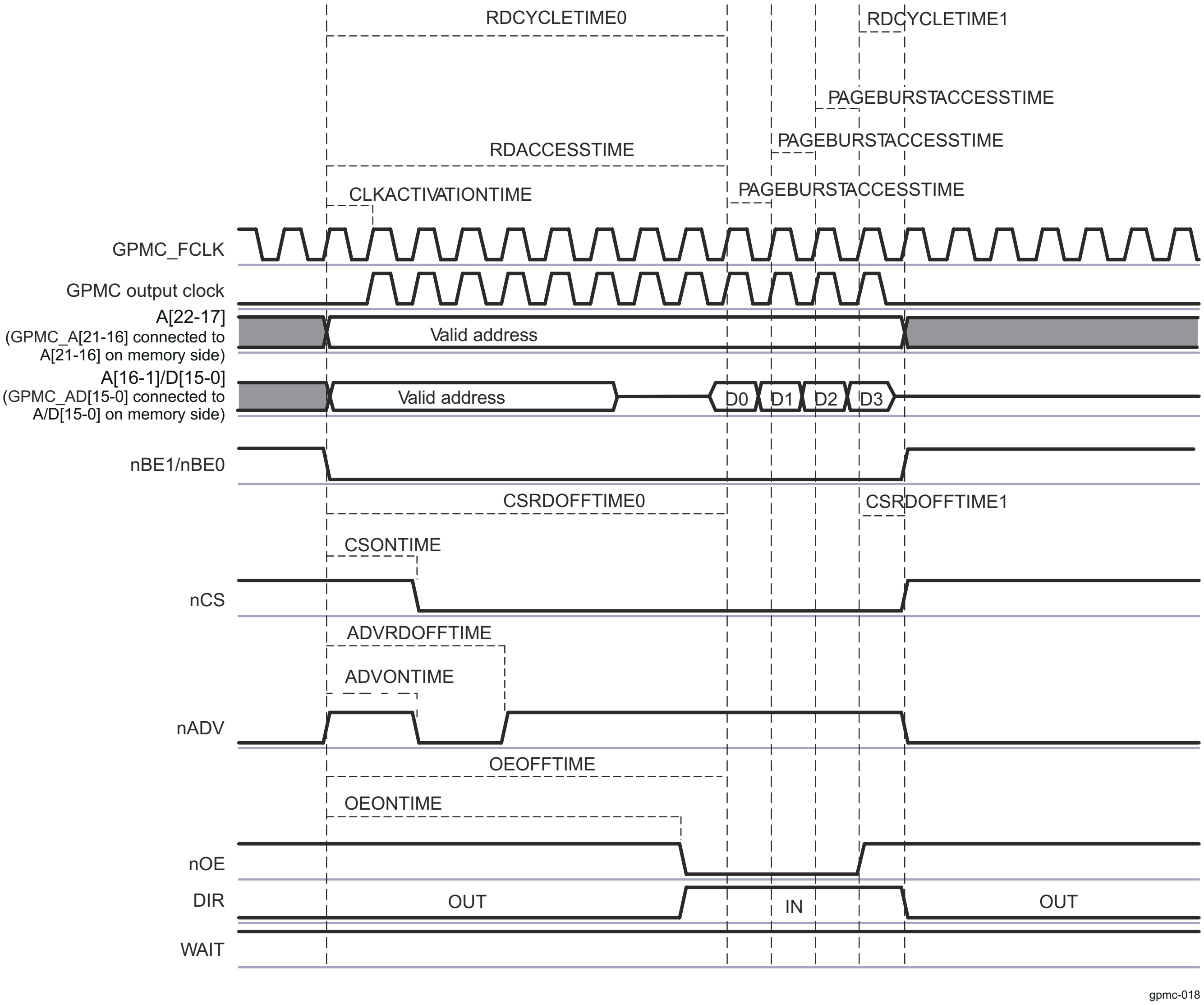

Figure 12-184. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 0)

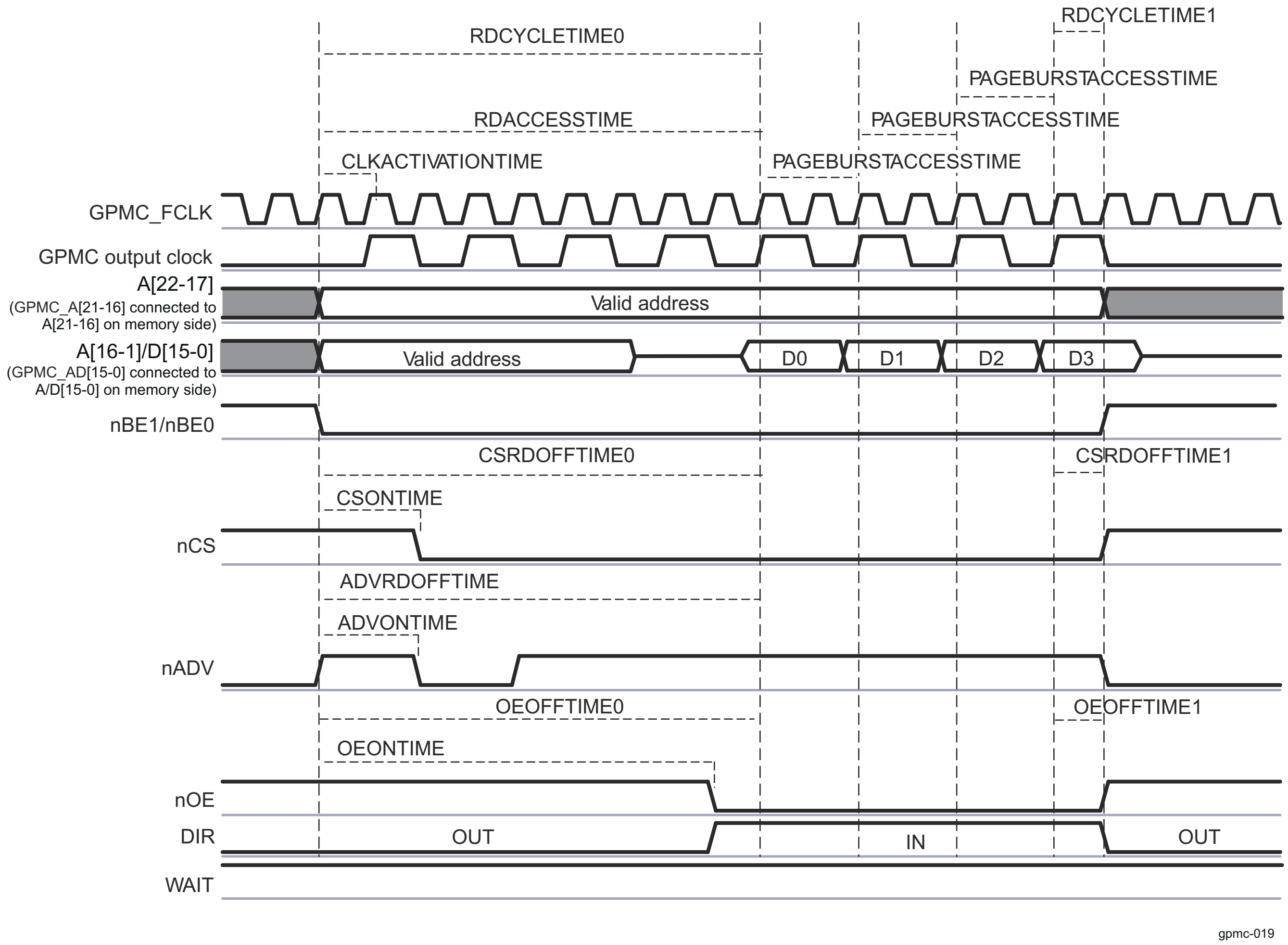

Figure 12-185. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 1)

When the GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as for a synchronous single-read operation. See Table 12-217, *NOR Memory Type*.

Initial latency for the first read data is controlled by RDACCESSTIME or by monitoring the WAIT signal. Successive read data are provided by the memory device every one or two GPMC_CLKOUT cycles. The PAGEBURSTACCESSTIME parameter must be set accordingly with the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field and the memory-device internal configuration. Depending on the device page length, the GPMC checks the device page crossing during a new burst request and purposely inserts initial latency (of RDACCESSTIME) when required.

Total access time GPMC_CONFIG5_i[4-0] RDCYCLETIME corresponds to RDACCESSTIME plus the address hold time from nCS deassertion. In Figure 12-185, the programmed value of RDCYCLETIME equals RDCYCLETIME0 + RDCYCLETIME1.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 12.4.3.4.8.10 , *Bus Keeping Support*.

Burst wraparound is enabled through the GPMC_CONFIG1_i[31] WRAPBURST bit and allows a 4-, 8-, or 16-Word16 linear burst access to wrap within its burst-length boundary through the GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH bit field.

12.4.3.4.9.2.3 Synchronous Single Write

Burst write mode is used for synchronous single or burst accesses.

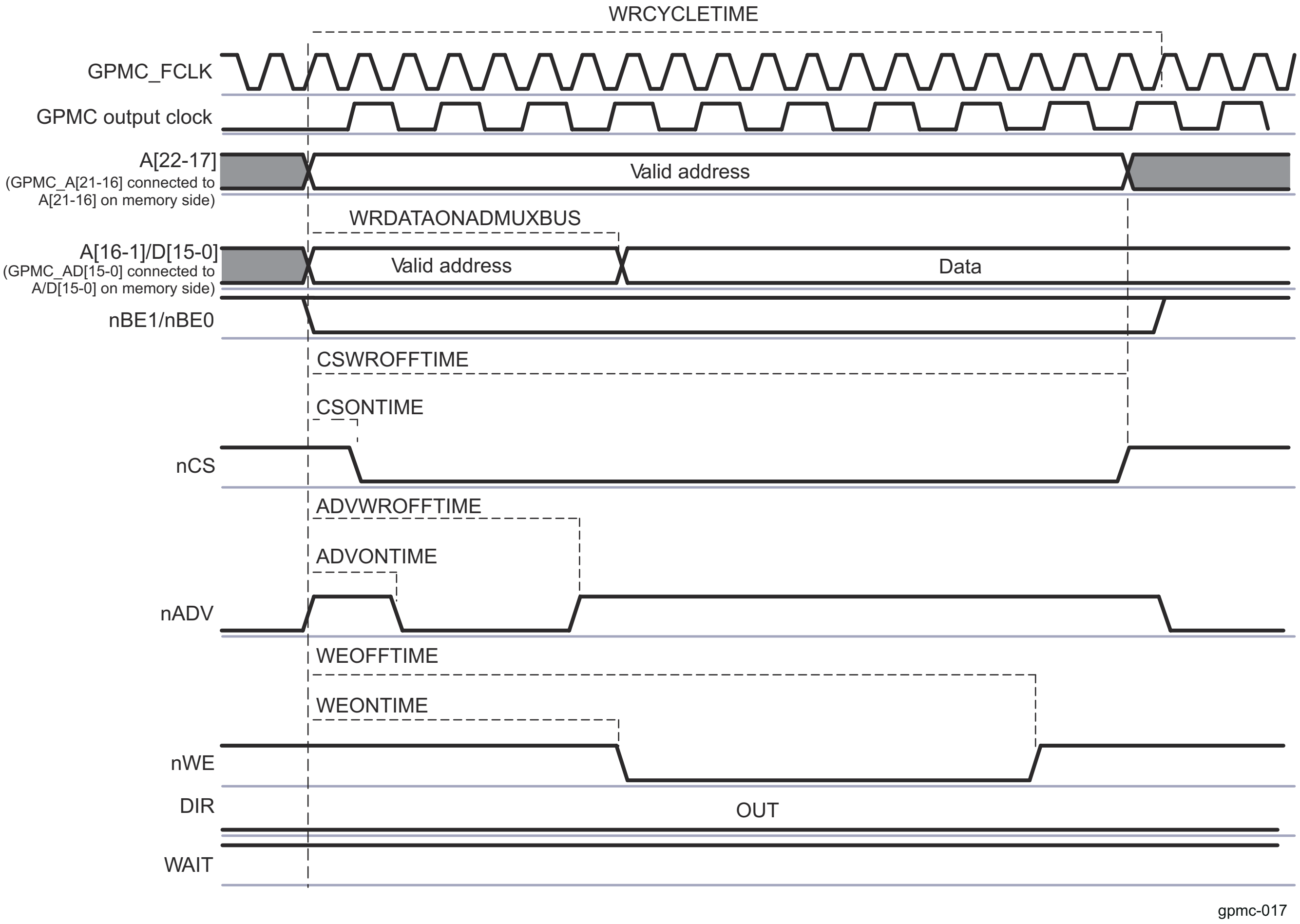

Figure 12-186. Synchronous Single Write on an Address/Data-Multiplexed Device

When the GPMC generates a write access to an address/data-multiplexed device, it drives the data bus (with address bits A[16-1]) until the GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS bit field time. The first data of the burst is driven on the address/data bus at WRDATAONADMUXBUS time.

12.4.3.4.9.2.4 Synchronous Multiple (Burst) Write

Synchronous burst write mode provides synchronous single or consecutive accesses.

Figure 12-187 shows a synchronous burst write access when the chip-select is configured in address/data-multiplexed mode.

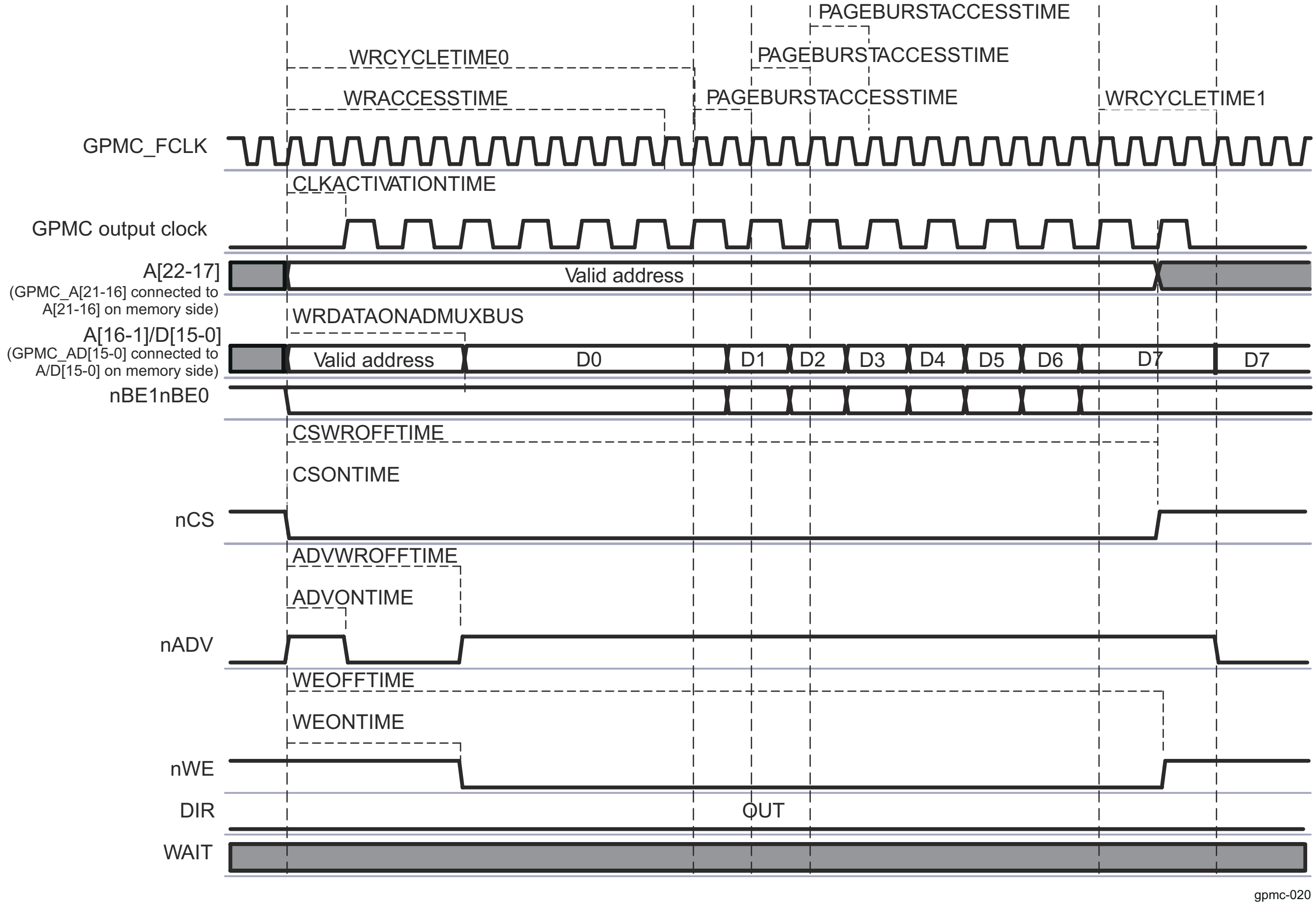

Figure 12-187. Synchronous Multiple Write (Burst Write) in Address/Data-Multiplexed Mode

Figure 12-188 shows the same synchronous burst write access when the chip-select is configured in address/address/data-multiplexed (AAD-multiplexed) mode.

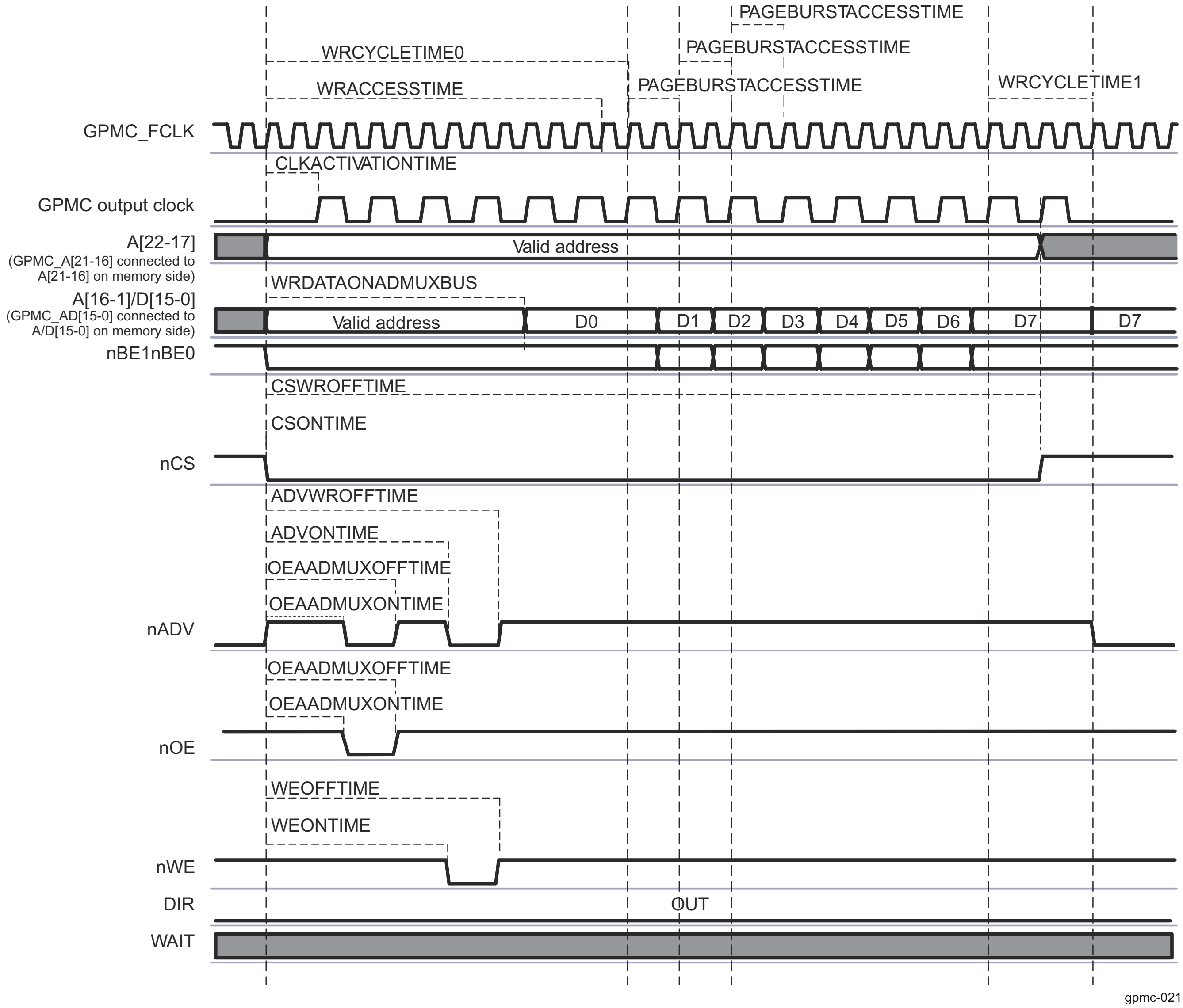

Figure 12-188. Synchronous Multiple Write (Burst Write) in Address/Address/Data-Multiplexed Mode

The first data of the burst is driven on the A/D bus at the GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS bit field.

When WRACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.4.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3-0] CSONTIME bit field (where i = 0 to 3) and ensures address setup time to nCS assertion.
  - nCS deassertion time controlled by the GPMC_CONFIG2_i[20-16] CSWROFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[20-16] ADVWROFFTIME bit field.

- Write enable signal nWE:
  - nWE assertion indicates a read cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19-16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28-24] WEOFFTIME bit field.

Note

The nWE falling edge must not be used to control the time when the burst first data is driven in the address/data bus, because some new devices require the nWE signal to be low during the address phase.

- Direction signal DIR is OUT during the entire access.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, and DIR signals are controlled as previously described.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG4_i[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.

First write data is driven by the GPMC at GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS, when in address/data-multiplexed configuration. The next write data of the burst is driven on the bus at WRACCESSTIME + 1 during GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME GPMC_FCLK cycles. The last data of the synchronous burst write is driven until GPMC_CONFIG5_i[12-8] WRCYCLETIME completes.

- WRACCESSTIME is defined in the GPMC_CONFIG6_i[28-24] bit field.
- The PAGEBURSTACCESSTIME parameter must be set accordingly with GPMCFCLKDIVIDER and the memory-device internal configuration.

Total access time GPMC_CONFIG5_i[12-8] WRCYCLETIME corresponds to WRACCESSTIME plus the address hold time from nCS deassertion. In Figure 12-187, the programmed value of WRCYCLETIME equals WRCYCLETIME0 + WRCYCLETIME1. WRCYCLETIME0 and WRCYCLETIME1 delays are not actual parameters and are only a graphical representation of the full WRCYCLETIME value.

After a write operation, if no other access (read or write) is pending, the data bus keeps the previous value. See Section 12.4.3.4.8.10 , *Bus Keeping Support*.

12.4.3.4.9.3 Asynchronous and Synchronous Accesses in non-multiplexed Mode

Page mode is available only in non-multiplexed mode.

- Asynchronous single-read operation on a non-multiplexed device
- Asynchronous single-write operation on a non-multiplexed device
- Asynchronous multiple- (page mode) read operation on a non-multiplexed device
- Synchronous operations on a non-multiplexed device

12.4.3.4.9.3.1 Asynchronous Single-Read Operation on non-multiplexed Device

Figure 12-189 shows an asynchronous single-read operation on a non-multiplexed device.

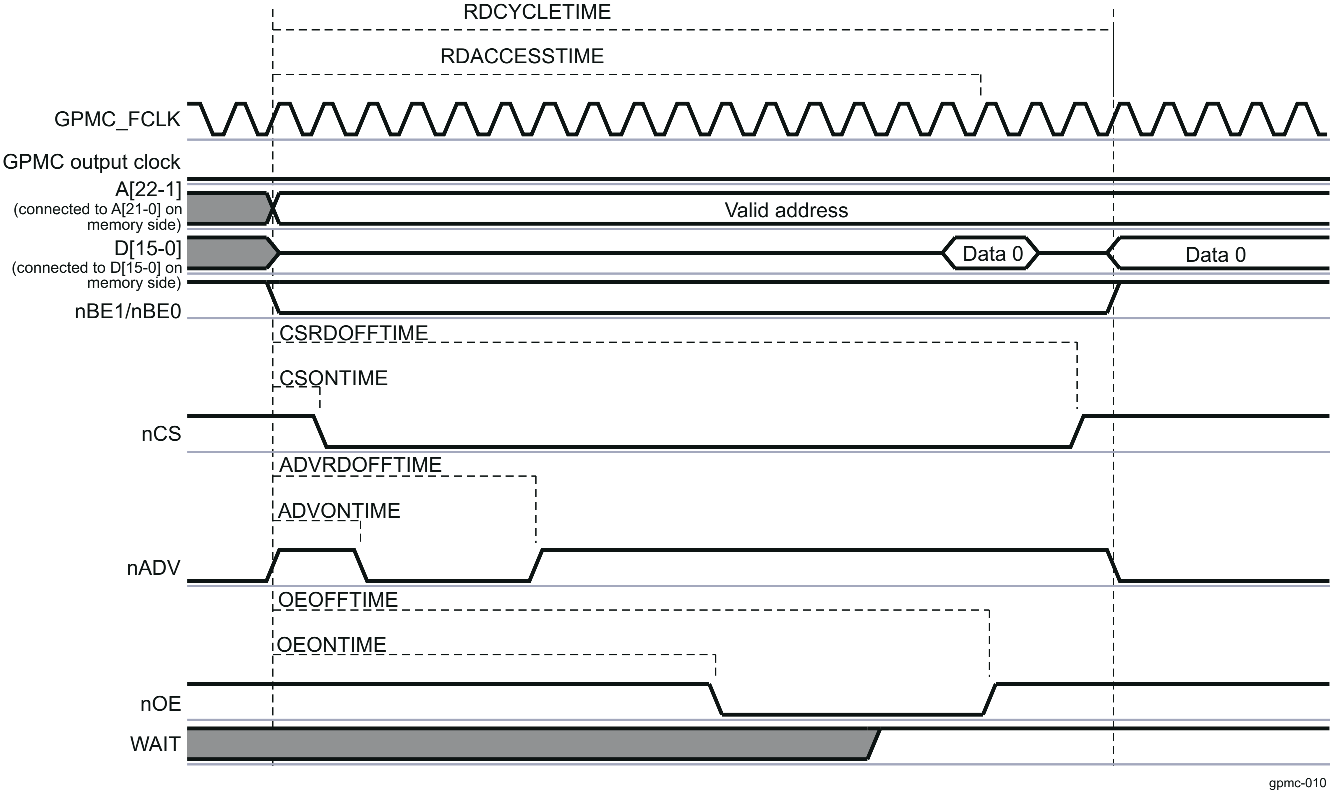

Figure 12-189. Asynchronous Single Read on an Address/Data-non-multiplexed Device

The 22-bit address (For a 16-bit data memory device, hence GPMC A[0] is not necessary to be output) is driven onto the address bus A[22-1] and the 16-bit data is driven onto the data bus D[15-0].

Read data is latched at GPMC_CONFIG1_5[20-16] RDACCESSTIME completion time. The end of the access is defined by the GPMC_CONFIG1_5[4-0] RDCYCLETIME parameter.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-222, *NAND Memory Type*).

12.4.3.4.9.3.2 Asynchronous Single-Write Operation on non-multiplexed Device

Figure 12-190 shows an asynchronous single-write operation on a non-multiplexed device.

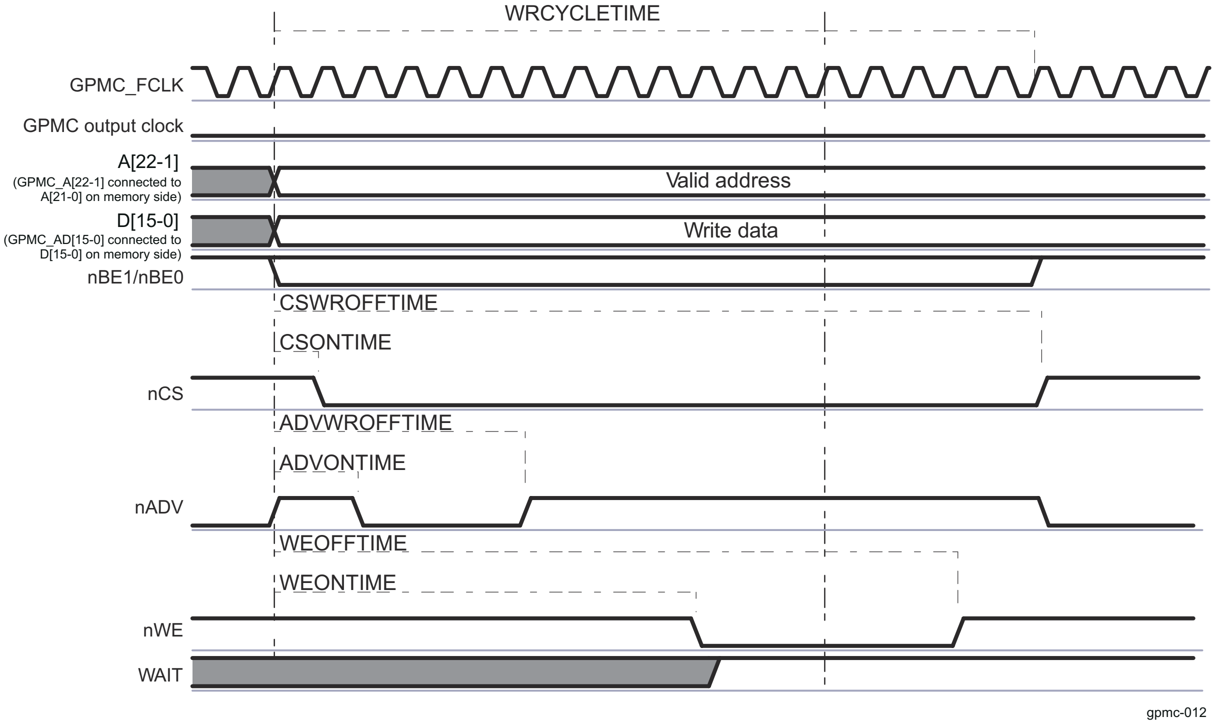

Figure 12-190. Asynchronous Single Write on an Address/Data-non-multiplexed Device

The nCS, nADV, nWE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-222).

12.4.3.4.9.3.3 Asynchronous Multiple (Page Mode) Read Operation on non-multiplexed Device

Figure 12-191 shows an asynchronous multiple-read operation on a non-multiplexed device in which two word32 host read accesses to the GPMC are split into one multiple- (page mode of 4 word16) read access to the attached device.

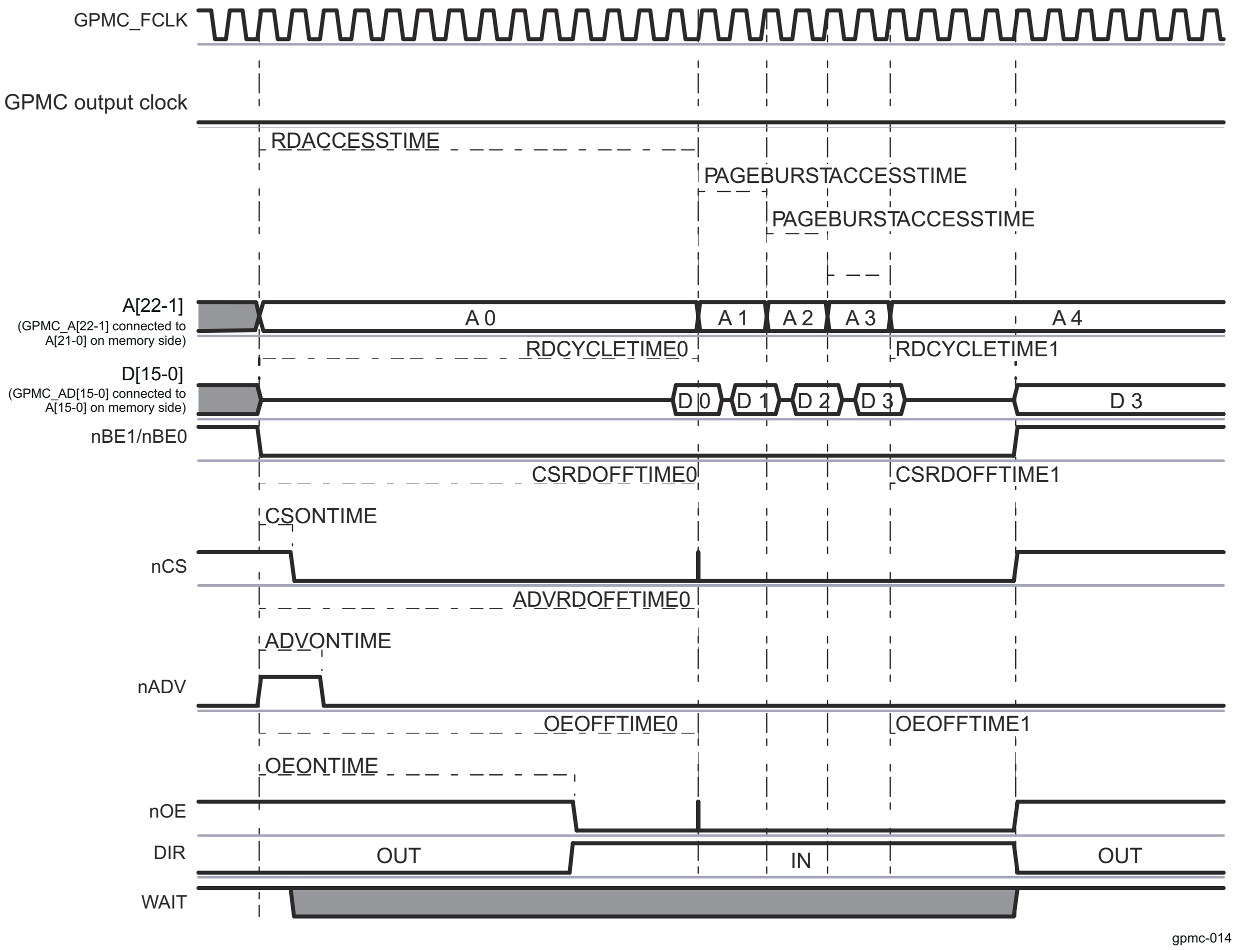

Figure 12-191. Asynchronous Multiple (Page Mode) Read

Note

The WAIT signal is active low.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-222).

When RDACCESSTIME completes, control signal timings are frozen during the multiple data transactions, corresponding to PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

Read data is latched at *GPMC_CONFIG5_i*[20-16] RDACCESSTIME completion time (where i = 0 to 3). The end of the access is defined by the *GPMC_CONFIG5_i*[4-0] RDCYCLETIME parameter.

During consecutive accesses, the GPMC increments the address after each data read completes.

Delay between successive read data in the page is controlled by the *GPMC_CONFIG5_i*[27-24] PAGEBURSTACCESSTIME parameter. Depending on the device page length, the GPMC can control device page crossing during a burst request and insert initial RDACCESSTIME latency. Page crossing is possible only with a new burst access, meaning a new initial access phase is initiated.

Total access time RDCYCLETIME corresponds to RDACCESSTIME, plus the address hold time, starting from the nCS deassertion.

- The read cycle time is defined in the *GPMC_CONFIG5_i*[4-0] RDCYCLETIME bit field.

- In Figure 12-191, the programmed value of RDCYCLETIME equals RDCYCLETIME0 (before paged accesses) + RDCYCLETIME1 (after paged accesses).

12.4.3.4.9.3.4 Synchronous Operations on a non-multiplexed Device

All information for this section is equivalent to similar operations for address/data-multiplexed or AAD-multiplexed accesses. The only difference resides in the address phase. See Section 12.4.3.5.3 , *GPMC Configuration in NOR Mode*.

12.4.3.4.9.4 Page and Burst Support

Each chip-select can be configured to process system single or burst requests into successive single accesses or asynchronous page/synchronous burst accesses, with appropriate access size adaptation.

Depending on the external device page or burst capability, read and write accesses can be independently configured through the GPMC. The GPMC_CONFIG1_i[30] READMULTIPLE and GPMC_CONFIG1_i[28] WRITMULTIPLE bits (where i = 0 to 3) are associated with the READTYPE and WRITETYPE parameters.

Note

- Asynchronous write page mode is not supported.
- 8-bit-wide device support is limited to nonburstable devices (READMULTIPLE and WRITEMULTIPLE are ignored).
- Not applicable to NAND device interfacing.

12.4.3.4.9.5 System Burst vs External Device Burst Support

The device system can issue the following requests to the GPMC:

- Byte, 16-bit word, 32-bit word requests (byte-enable-controlled). This is always a single request from the interconnect point of view.
- Incrementing fixed-length bursts of two, four, and eight words
- Wrapped (critical word access first) fixed-length burst of two, four, or eight words

To process a system request with the optimal protocol, the READMULTIPLE (and READTYPE) and WRITEMULTIPLE (and WRITETYPE) parameters must be set according to the burstable capability (synchronous or asynchronous) of the attached device.

The GPMC access engine issues only fixed-length bursts. The maximum length that can be issued is defined per chip-select by the *GPMC_CONFIG1_i*[24-23] ATTACHEDDEVICEPAGELENGTH bit field (where i = 0 to 3). When the value of ATTACHEDDEVICEPAGELENGTH is less than the length of the system burst request (including the appropriate access size adaptation according to the device width), the GPMC splits the system burst request into multiple bursts. Within the specified 4-, 8-, or 16-word value, the value of the ATTACHEDDEVICEPAGELENGTH bit field must correspond to the maximum length burst supported by the memory device configured in fixed-length burst mode (as opposed to continuous burst mode).

To get optimal performance from memory devices that natively support 16 Word16-length-wrapping burst capability (critical word access first), the ATTACHEDDEVICEPAGELENGTH parameter must be set to 16 words and the *GPMC_CONFIG1_i*[31] WRAPBURST bit (where i = 0 to 3) must be set to 1. Similarly DEVICEPAGELENGTH is set to 4 and 8 for memories supporting 4 and 8 Word16-length-wrapping burst, respectively.

When the memory device does not offer (or is not configured to offer) native 16 Word16-length-wrapping burst, the WRAPBURST parameter must be cleared, and the GPMC access engine emulates the wrapping burst by issuing the appropriate burst sequences according to the value of ATTACHEDDEVICEPAGELENGTH.

When the memory device does not support native-wrapping burst, there is usually no difference in behavior between a fixed-burst length mode and a continuous-burst mode configuration (except for a potential power increase from a memory-speculative data prefetch in a continuous burst read). However, even though continuous burst mode is compatible with GPMC behavior, because the GPMC access engine issues only fixed-length burst and does not benefit from continuous burst mode, it is best to configure the memory device in fixed-length burst mode.

The memory device maximum-length burst (configured in fixed-length burst wrap or nonwrap mode) usually corresponds to the memory device data buffer size. Memory devices with a minimum of 16 half-word buffers are the most appropriate (especially with wrap support), but memory devices with smaller buffer size (4 or 8) are also supported, assuming that the *GPMC_CONFIG1_i*[24-23] ATTACHEDDEVICEPAGELENGTH bit field is set accordingly to 4 or 8 words.

The device system issues only requests with addresses or starting addresses for nonwrapping burst requests; that is, the request size boundary is aligned. In case of an eight-word-wrapping burst, the wrapping address always occurs on the eight-word boundary. As a consequence, all words requested must be available from the memory data buffer when the buffer size is equal to or greater than the value of ATTACHEDDEVICEPAGELENGTH. This usually means that data can be read from or written to the buffer at a constant rate (number of cycles between data) without wait-states between data accesses. If the memory does not behave this way (nonzero wait-state burstable memory), WAIT pin monitoring must be enabled to dynamically control data access completion within the burst.

Note

When the system burst request length is less than the value of ATTACHEDDEVICEPAGELENGTH, the GPMC proceeds with the required accesses.

12.4.3.4.10 GPMC pSRAM Access Specificities

pSRAM devices are SRAM-pin-compatible low-power memories that contain a self-refreshed DRAM memory array. The GPMC_CONFIG1_i[11-10] DEVICETYPE bit field (where i = 0 to 3) must be set to 0b00.

The pSRAM device uses the NOR protocol. It supports the following operations:

- Asynchronous single read
- Asynchronous page read
- Asynchronous single write
- Synchronous single read and write
- Synchronous burst read
- Synchronous burst write (not supported by NOR flash memory)

pSRAM devices must be powered up and initialized in a predefined manner according to the specifications of the attached device.

pSRAM devices can be programmed to use either mode: fixed or variable latency. pSRAM devices can automatically schedule autorefresh operations, which force the GPMC to use its WAIT signal capability when read or write operations occur during an internal self-refresh operation, or they can automatically include the autorefresh operation in the access time. These devices do not require additional WAIT signal capability or a minimum nCS high pulse width between consecutive accesses to ensure that the correct internal refresh operation is scheduled.

12.4.3.4.11 GPMC NAND Access Description

NAND (8-bit and 16-bit) memory devices using a standard NAND asynchronous address/data-multiplexing scheme can be supported on any chip-select with the appropriate asynchronous configuration settings.

As for any other type of memory compatible with the GPMC interface, accesses to a chip-select allocated to a NAND device can be interleaved with accesses to chip-selects allocated to other external devices. This interleaved capability limits the system to *chip enable don't care* NAND devices, because the chip-select allocated to the NAND device must be deasserted if accesses to other chip-selects are requested.

12.4.3.4.11.1 NAND Memory Device in Byte or 16-bit Word Stream Mode

NAND devices require correct command and address programming before data array read or write accesses. The GPMC does not include specific hardware to translate a random address system request into a NAND-specific multiphase access. In that sense, GPMC NAND support, as opposed to random memory-map device support, is data stream-oriented (byte or 16-bit word).

The GPMC NAND programming model depends on a software driver for address and command formatting with the correct data address pointer value according to the block and page structure. Because of NAND structure and protocol interface diversity, the GPMC does not support automatic command and address phase programming, and software drivers must access the NAND device ID to ensure that correct command and address formatting are used for the identified device.

NAND device data read and write accesses are achieved through an asynchronous read or write access. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Any chip-select region can be qualified as a NAND region to constrain the nADV/ALE signal as ALE (ALE active high, default state value at low) during address program access, and the nBE0/CLE signal as CLE (CLE active high, default state value at low) during command program access. GPMC address lines are not used (the previous value is not changed) during NAND access.

12.4.3.4.11.1.1 Chip-Select Configuration for NAND Interfacing in Byte or Word Stream Mode

The GPMC_CONFIG7_i register (where i = 0 to 3) associated with a NAND device region interfaced in byte or word stream mode can be initialized with a minimum size of 16MB, because any address location in the chip-select memory region can be used to access a NAND data array. The NAND flash protocol specifies an address sequence where address bits are passed through the data bus in a series of write accesses with the ALE pin asserted. After this address phase, all operations are streamed and the system requests address is irrelevant.

CAUTION

To allow correct command, address, and data-access controls, the GPMC_CONFIG1_i register associated with a NAND device region must be initialized in asynchronous read and write modes with the parameters listed in Table 12-192. Failure to comply with these settings corrupts the NAND interface protocol.

Table 12-204. Chip-Select Configuration for NAND Interfacing

Bit Field	Register	Value	Comments
WRAPBURST	GPMC_CONFIG1_i[31] (1)	0	No wrap
READMULTIPLE	GPMC_CONFIG1_i[30]	0	Single access
READTYPE	GPMC_CONFIG1_i[29]	0	Asynchronous mode
WRITEMULTIPLE	GPMC_CONFIG1_i[28]	0	Single access
WRITETYPE	GPMC_CONFIG1_i[27]	0	Asynchronous mode
CLKACTIVATIONTIME	GPMC_CONFIG1_i[26-25]	0b00	
ATTACHEDDEVICEPAGELENGTH	GPMC_CONFIG1_i[24-23]	Don't care	Single-access mode
WAITREADMONITORING	GPMC_CONFIG1_i[22]	0	Wait not monitored by GPMC access engine
WAITWRITEMONITORING	GPMC_CONFIG1_i[21]	0	Wait not monitored by GPMC access engine
WAITMONITORINGTIME	GPMC_CONFIG1_i[19-18]	Don't care	Wait not monitored by GPMC access engine
WAITPINSELECT	GPMC_CONFIG1_i[17-16]		Select which wait is monitored by edge detectors
DEVICESIZE	GPMC_CONFIG1_i[13-12]	0b00 or 0b01	8- or 16-bit interface

Table 12-204. Chip-Select Configuration for NAND Interfacing (continued)

Bit Field	Register	Value	Comments
DEVICETYPE	GPMC_CONFIG1_i[11-10]	0b10	NAND device in stream mode
MUXADDDATA	GPMC_CONFIG1_i[9-8]	0b00	non-multiplexed mode
TIMEPARAGRANULARITY	GPMC_CONFIG1_i[4]	0	Timing achieved with best GPMC clock granularity
GPMCFCLKDIVIDER	GPMC_CONFIG1_i[1-0]	Don't care	Asynchronous mode

(1) i = 0 to 3

The GPMC_CONFIG1_i to GPMC_CONFIG4_i registers (where i = 0 to 3) associated with a NAND device region must be initialized with the correct control-signal timing value according to the NAND device timing parameters.

12.4.3.4.11.1.2 NAND Device Command and Address Phase Control

NAND devices require multiple address programming phases. The software driver must issue the correct number of command and address program accesses, according to the device command set and the device address-mapping scheme.

NAND device-command and address-phase programming is achieved through write requests to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations (where i = 0 to 3) with the correct command and address values. These locations are mapped in the associated chip-select register region. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Command and address values are not latched during the access and cannot be read back at the register location.

- Only write accesses must be issued to these locations, but the GPMC does not discard any read access. Accessing a NAND device with nOE and CLE or ALE asserted (read access) can produce undefined results.
- Write accesses to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations must be posted for faster operations (where i = 0 to 3). The GPMC_CONFIG[0] NANDFORCEPOSTEDWRITE bit enables write accesses to these locations as posted, even if they are defined as nonposted.

A write buffer is used to store write transaction information before the external device is accessed:

- Up to eight consecutive posted write accesses can be accepted and stored in the write buffer.
- For nonposted write, the pipeline is one deep.
- An GPMC_STATUS[0] EMPTYWRITEBUFFERSTATUS bit stores the empty status of the write buffer.

The GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers (where i = 0 to 3) are 32-bit word locations, which means any 32-or 16-bit word access is split into 4- or 2-byte accesses if an 8-bit-wide NAND device is attached. For multiple-command phase or multiple-address phase, the software driver can use 32- or 16-bit word access to these registers, but it must consider the splitting and little-endian ordering scheme. When only one byte command or address phase is required, only byte write access to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers can be used, and any of the four byte locations of the registers is valid.

The same applies to a GPMC_NAND_COMMAND_i and a GPMC_NAND_ADDRESS_i (where i = 0 to 3) 32-bit word write access to a 16-bit-wide NAND device (split into two 16-bit word accesses). In the case of a 16-bit word write access, the MSByte of the 16-bit word value must be set according to the NAND device requirement (usually 0). Either 16-bit word location or any one of the four byte locations of the registers is valid.

12.4.3.4.11.1.3 Command Latch Cycle

Writing data at the GPMC_NAND_COMMAND_i location (where i = 0 to 3) places the data as the NAND command value on the bus, using a regular asynchronous write access.

- nCE is controlled by the CSONTIME and CSWROFFTIME timing parameters.

- CLE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE and nRE (nOE) are maintained inactive.

Figure 12-192 shows the NAND command latch cycle.

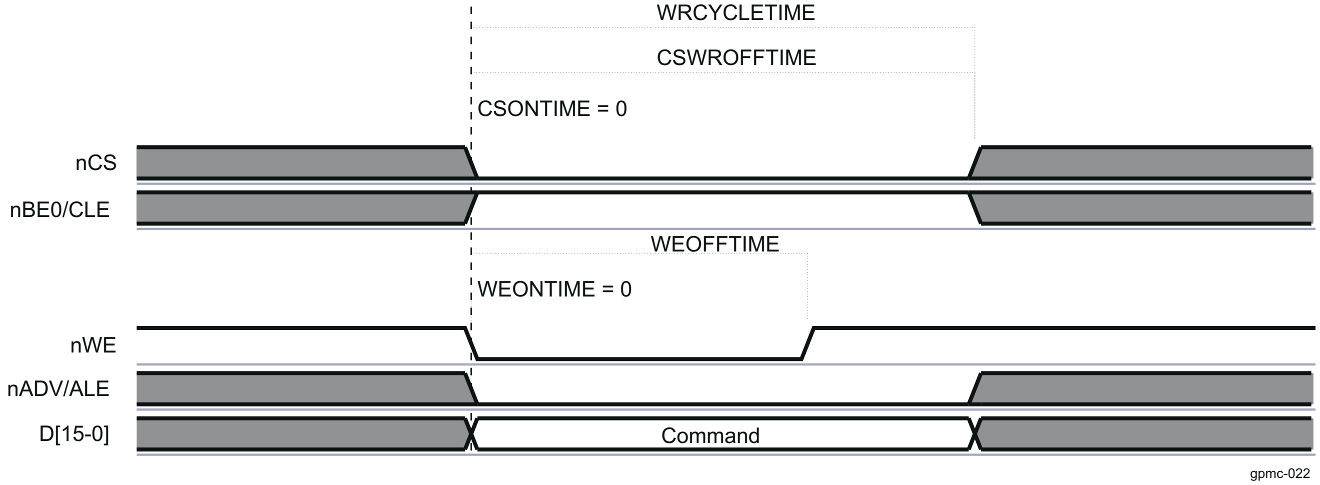

Figure 12-192. NAND Command Latch Cycle

Note

CLE is shared with the nBE0 output signal and has an inverted polarity from BE0. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, nBE0 (also nBE1) must not toggle, because it is shared with CLE.

NAND flash memories do not use byte-enable signals.

12.4.3.4.11.1.4 Address Latch Cycle

Writing data at the *GPMC_NAND_ADDRESS_i* location (where i = 0 to 3) places the data as the NAND partial address value on the bus, using a regular asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- ALE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- CLE and nRE (nOE) are maintained inactive.

Figure 12-193 shows the NAND address latch cycle.

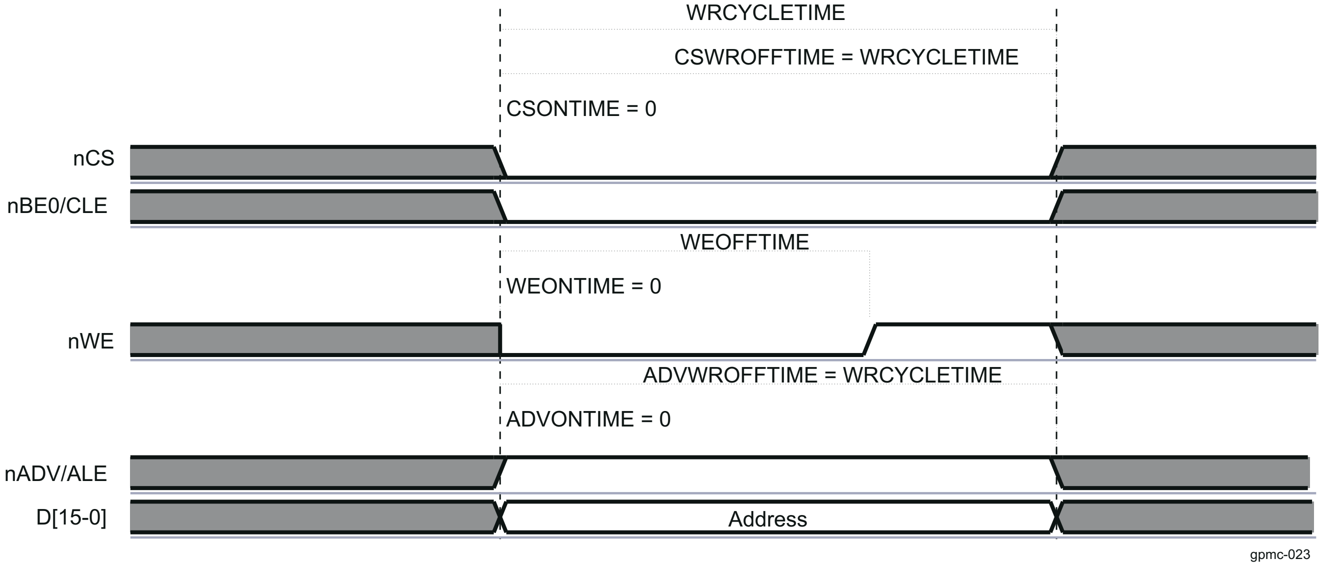

Figure 12-193. NAND Address Latch Cycle

Note

ALE is shared with the nADV output signal and has an inverted polarity from ADV. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, ALE is kept stable.

12.4.3.4.11.1.5 NAND Device Data Read and Write Phase Control in Stream Mode

NAND device data read and write accesses are achieved through a read or write request to the chip-select-associated memory region at any address location in the region or through a read or write request to the GPMC_NAND_DATA_i location (where i = 0 to 3) mapped in the chip-select-associated control register region. GPMC_NAND_DATA_i is not a true register, but an address location to enable nRE or nWE signal control. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.

- nCS is controlled by the CSONTIME and CSRDOFFTIME timing parameters.
- nRE is controlled by the OEONTIME and OEOFFTIME timing parameters.
- To take advantage of nRE high-to-data invalid minimum timing value, RDACCESSTIME can be set so that data are effectively captured after nRE deassertion. This allows optimization of NAND read access cycle time completion. For optimal timing parameter settings, see the NAND device and the device timing parameters.

ALE, CLE, and nWE are maintained inactive.

Figure 12-194 shows the NAND data read cycle.

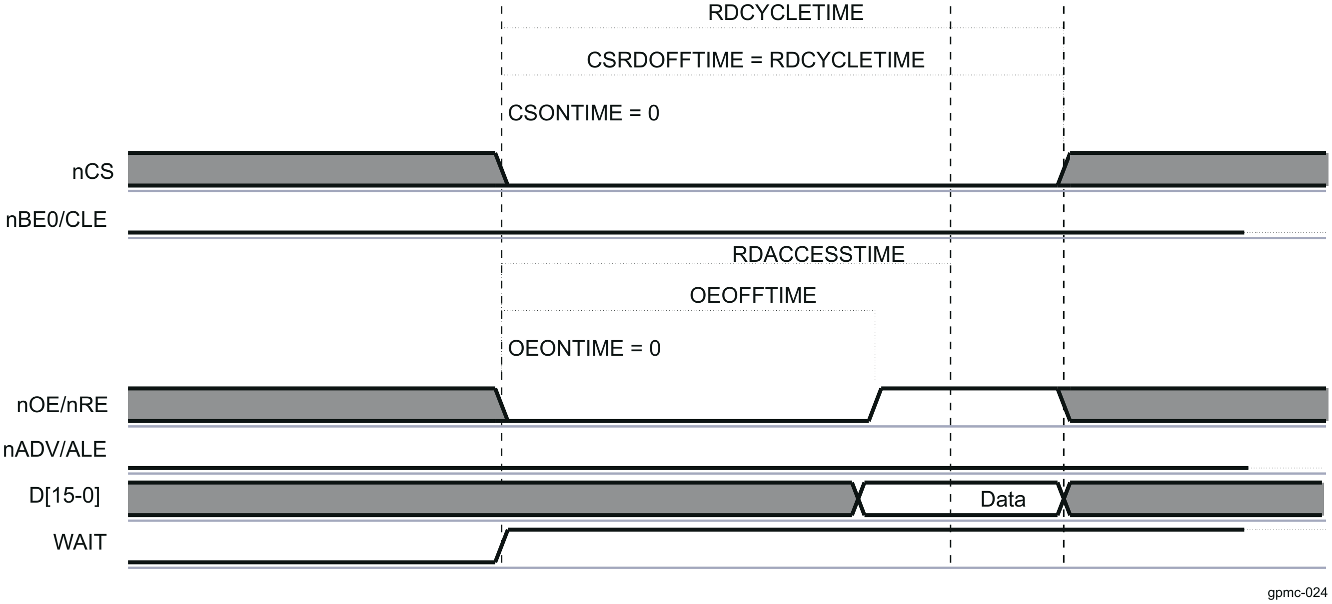

Figure 12-194. NAND Data Read Cycle

Writing data to the GPMC_NAND_DATA_i location or to any location in the associated chip-select memory region activates an asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE, CLE, and nRE (nOE) are maintained inactive.

Figure 12-195 shows the NAND data write cycle.

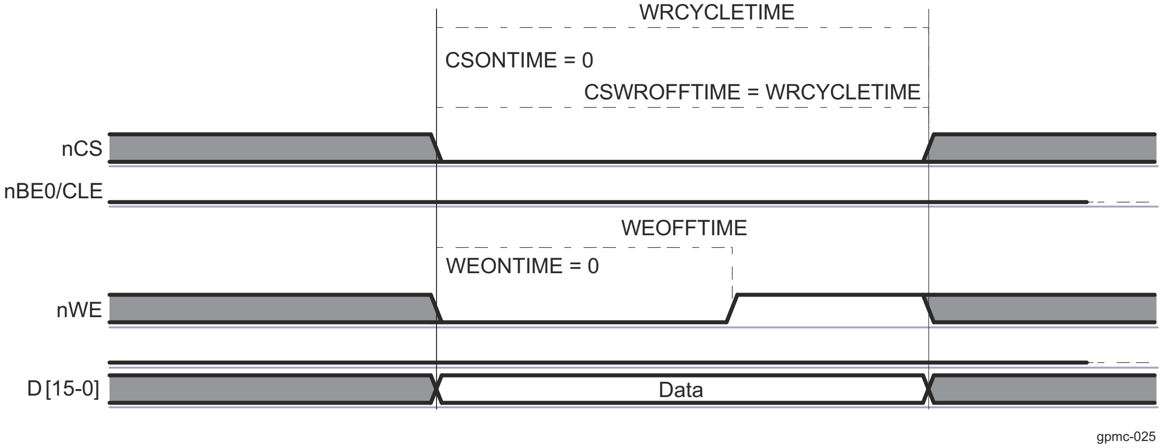

Figure 12-195. NAND Data Write Cycle

12.4.3.4.11.1.6 NAND Device General Chip-Select Timing Control Requirement

For most NAND devices, read data access time is dominated by nCS-to-data-valid timing and has faster nRE-to-data-valid timing. Successive accesses with nCS deassertions between accesses are affected by this timing constraint. Because accesses to a NAND device can be interleaved with other chip-select accesses, there is no certainty that nCS always stays low between two accesses to the same chip-select. Moreover, an nCS deassertion time between the same chip-select NAND accesses is likely to be required as follows: the nCS deassertion requires programming CYCLETIME and RDACCESSTIME according to the nCS-to-data-valid critical timing.

To get full performance from NAND read and write accesses, the prefetch engine can dynamically reduce the following on back-to-back NAND accesses (to the same memory) and suppress the minimum nCS high pulse width between accesses:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSRDOFFTIME
- CSWROFFTIME
- ADVRDOFFTIME
- ADVWROFFTIME
- OEOFFTIME
- WEOFFTIME

For more information about optimal prefetch engine access, see Section 12.4.3.4.11.4 , *Prefetch and Write-Posting Engine*.

Some NAND devices require minimum write-to-read idle time, especially for device-status read accesses following status-read command programming (write access). If such write-to-read transactions are used, a minimum nCS high pulse width must be set. For this, CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDELAY must be set according to the appropriate timing requirement to prevent any timing violation.

NAND devices usually have an important nRE high-to-data bus in three-state mode. This requires a bus turnaround setting (BUSTURNAROUND = 1) so that the next access to a different chip-select is delayed until the BUSTURNAROUND delay completes. Back-to-back NAND read accesses to the same NAND flash are not affected by the programmed bus turnaround delay.

12.4.3.4.11.1.7 Read and Write Access Size Adaptation

12.4.3.4.11.1.7.1 8-Bit-Wide NAND Device

Host 16- and 32-bit word read and write access requests to a chip-select associated with an 8-bit-wide NAND device are split into successive read and write byte accesses to the NAND memory device. Byte access is ordered according to little-endian organization. A NAND 8-bit-wide device must be interfaced on the D0D7 interface bus lane. GPMC data accesses are justified on this bus lane when the cs is associated with an 8-bit-wide NAND device.

12.4.3.4.11.1.7.2 16-Bit-Wide NAND Device

Host 32-bit word read and write access requests to a chip-select associated with a 16-bit-wide NAND device are split into successive read and write 16-bit word accesses to the NAND memory device. 16-bit word access is ordered according to little-endian organization.

Host byte read and write access requests to a 16-bit-wide NAND device are completed as 16-bit accesses on the device itself, because there is no byte-addressing capability on 16-bit-wide NAND devices. This means that the NAND device address pointer is incremented on a 16-bit word basis and not on a byte basis. For a read access, only the requested byte is given back to the host, but the remaining byte is not stored or saved by the GPMC, and the next byte or 16-bit word read access gets the next 16-bit word NAND location. For a write access, the invalid byte part of the 16-bit word is driven to FF, and the next byte or 16-bit word write access programs the next 16-bit word NAND location.

Generally, byte access to a 16-bit-wide NAND device must be avoided, especially when ECC calculation is enabled. 8- or 16-bit ECC-based computations are corrupted by a byte read to a 16-bit-wide NAND device, because the nonrequested byte is considered invalid on a read access (not captured on the external data bus; FF is fed to the ECC engine) and is set to FF on a write access.

Host requests (read/write) issued in the chip-select memory region are translated in successive single or split accesses (read/write) to the attached device. Therefore, incrementing 32-bit burst requests are translated in multiple 32-bit sequential accesses following the access adaptation of the 32-bit to 8- or 16-bit device.

12.4.3.4.11.2 NAND Device-Ready Pin

The NAND memory device provides a ready pin to indicate data availability after a block/page opening and to indicate that data programming is complete. The ready pin can be connected to one of the wait GPMC input pins; data read accesses must not be tried when the ready pin is sampled inactive (device is not ready) even if the associated chip-select WAITREADMONITORING bit field is set. The duration of the NAND device busy state after the block/page opening is so long (up to 50 micro second) that accesses occurring when the ready pin is sampled inactive can stall GPMC access and eventually cause a system time-out.

Note

If a read access to a NAND flash is done using WAIT monitoring mode, the device is blocked during a page opening, and so is the GPMC. If the correct settings are used, other chip-selects can be used while the memory processes the page opening command.

To avoid a time-out caused by a block/page opening delay in NAND flash, disable the WAIT pin monitoring for read and write accesses (that is, set the *GPMC_CONFIG1_i*[21] WAITWRITEMONITORING and *GPMC_CONFIG1_i*[22] WAITREADMONITORING bits to 0, where i = 0 to 3), and use one of the following methods instead:

- Use software to poll the WAITxSTATUS bit (where x = 0 to 1) of the *GPMC_STATUS*.
- Configure an interrupt that is generated on the WAIT signal change (through the *GPMC_IRQENABLE* register bits[11-8]).

Even if the READWAITMONITORING bit is not set, the external memory nR/B pin status is captured in the programmed wait bit in the *GPMC_STATUS* register.

The READWAITMONITORING bit method must be used for other memories than NAND flash, if they require the use of a WAIT signal.

12.4.3.4.11.2.1 Ready Pin Monitored by Software Polling

The ready signal state can be monitored through the GPMC_STATUS[9-8] WAITxSTATUS bit (where x = 0 to 1). Software must monitor the ready pin only when the signal is declared valid. Refer to the NAND device timing parameters to set the correct software temporization to monitor ready only after the invalid window is complete from the last read command written to the NAND device.

12.4.3.4.11.2.2 Ready Pin Monitored by Hardware Interrupt

Each GPMC_WAIT input pin can generate an interrupt when a wait-to-no-wait transition is detected. Depending on whether the GPMC_CONFIG[9-8] WAITxPINPOLARITY bits (where x = 0 to 1) is active low or active high, the wait-to-no-wait transition is a low-to-high external WAIT signal transition or a high-to-low external WAIT signal transition, respectively.

The wait transition pin detector must be cleared before any transition detection. This is done by writing 1 to the WAITxEDGEDETECTIONSTATUS bit (where x = 0 to 1) of the GPMC_IRQSTATUS register according to the GPMC_WAIT pin used for the NAND device-ready signal monitoring. To detect a wait-to-no-wait transition, the transition detector requires a wait active time detection of a minimum of two GPMC_FCLK cycles. Software must incorporate precautions to clear the wait transition pin detector before wait (busy) time completes.

A wait-to-no-wait transition detection can issue a GPMC interrupt if the WAITxEDGEDETECTIONENABLE bit in the GPMC_IRQENABLE register is set and if the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register is set.

The WAITMONITORINGTIME bit field does not affect wait-to-no-wait transition time detection.

It is also possible to poll the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register according to the GPMC_WAIT pin used for NAND device ready signal monitoring.

12.4.3.4.11.3 ECC Calculator

The GPMC includes an error code correction (ECC) calculator circuitry that enables ECC calculation on the fly during data read or data program (that is, write) operations. The page size supported by the ECC calculator in one calculation/context is 512 bytes.

The user can choose from two different algorithms with different error correction capabilities through the *GPMC_ECC_CONFIG*[16] ECCALGORITHM bit:

1. Hamming code for 1-bit error code correction on 8- or 16-bit NAND flash organized with page size greater than 512 bytes
2. Bose-Chaudhurl-Hocquenghem (BCH) code for 4- to 16-bit error correction

The GPMC does not handle the error code correction directly. During writes, the GPMC computes parity bits. During reads, the GPMC provides enough information for the processor to correct errors without reading the data buffer all over again.

The Hamming code ECC is based on a 2-dimensional (2D) (row and column) bit parity accumulation. This parity accumulation is accomplished on the programmed number of bytes or 16-bit words read from the memory device, or is written to the memory device in stream mode.

Because the ECC engine includes only one accumulation context, it can be allocated to only one chip-select at a time through the *GPMC_ECC_CONFIG*[3-1] ECCCS bit field. Even if two chip-selects use different ECC algorithms, one the Hamming code and the other a BCH code, they must define separate ECC contexts because some of the ECC registers are common to all types of algorithms.

12.4.3.4.11.3.1 Hamming Code

All references to ECC in this subsection refer to the 1-bit error correction Hamming code.

The ECC is based on a 2D (row and column) bit parity accumulation known as the Hamming code. The parity accumulation is done for a programmed number of bytes or 16-bit word read from the memory device or written to the memory device in stream mode.

There is no automatic error detection or correction, and the software NAND driver must read the multiple ECC calculation results, compare them to the expected code value, and take the appropriate corrective actions according to the error handling strategy (ECC storage in spare byte, error correction on read, block invalidation).

The ECC engine includes a single accumulation context. It can be allocated to a single designated chip-select at a time, and parallel computations on different chip-selects are not possible. Because it is allocated to a single chip-select, the ECC computation is not affected by interleaved GPMC accesses to other chip-selects and devices. The ECC accumulation is sequentially processed in the order of data read from or written to the memory on the designated chip-select. The ECC engine does not differentiate read accesses from write accesses and does not differentiate data from command or status information. Software must ensure that only relevant data are passed to the NAND flash memory while the ECC computation engine is active.

The starting NAND page location must be programmed first, followed by an ECC accumulation context reset with an ECC enabling, if required. The NAND device accesses discussed in the following sections must be limited to data read or write until the specified number of ECC calculations is complete.

12.4.3.4.11.3.1.1 ECC Result Register and ECC Computation Accumulation Size

The GPMC includes up to nine ECC result registers (*GPMC_ECCj_RESULT*, where j = 1 to 9) to store ECC computation results when the specified number of bytes or 16-bit words has been computed.

The ECC result registers are used sequentially: one ECC result is stored in one ECC result register on the list, the next ECC result is stored in the next ECC result register on the list, and so forth, until the last ECC computation. The value of the *GPMC_ECCj_RESULT* register is valid only when the programmed number of bytes or 16-bit words has been accumulated, which means that the same number of bytes or 16-bit words has been read from or written to the NAND device in sequence.

The *GPMC_ECC_CONTROL*[3-0] ECCPOINTER bit field must be set to the correct value to select the ECC result register to be used first in the list for the incoming ECC computation process. The ECCPointer can be read to determine which ECC register is used in the next ECC result storage for the ongoing ECC computation. The value of the *GPMC_ECCj_RESULT* register (where j = 1 to 9) can be considered valid when ECCPOINTER equals j + 1. When the *GPMC_ECCj_RESULT* register (where j = 9) is updated, ECCPOINTER is frozen at 10, and ECC computing is stopped (ECCENABLE = 0).

The ECC accumulator must be reset before any ECC computation accumulation process. The *GPMC_ECC_CONTROL*[8] ECCCLEAR bit must be set to 1 (nonpersistent bit) to clear the accumulator and all ECC result registers.

For each ECC result (each *GPMC_ECCj_RESULT* register, where j = 1 to 9), the number of bytes or 16-bit words used for ECC computing accumulation can be selected from between two programmable values.

The ECCjRESULTSIZE bits (where j = 1 to 9) in the *GPMC_ECC_SIZE_CONFIG* register select which programmable size value (ECCSIZE0 or ECCSIZE1) must be used for this ECC result (stored in the *GPMC_ECCj_RESULT* register).

The ECCSIZE0 and ECCSIZE1 bit fields allow selection of the number of bytes or 16-bit words used for ECC computation accumulation. Any even values from 2 to 512 are allowed.

Flexibility in the number of ECCs computed and the number of bytes or 16-bit words used in the successive ECC computations enables different NAND page error-correction strategies. Usually based on 256 or 512 bytes and on 128 or 256 16-bit word, the number of ECC results required is a function of the NAND device page size. Specific ECC accumulation size can be used when computing the ECC on the NAND spare byte.

For example, with a 2-KB data page, 8-bit-wide NAND device, eight ECCs accumulated on 256 bytes can be computed and added to one extra ECC computed on the 24 spare bytes area where the eight ECC results used for comparison and correction with the computed data page ECC are stored. The GPMC then provides nine *GPMC_ECCj_RESULT* registers (j = 1 to 9) to store the results. In this case, ECCSIZE0 is set to 256, and ECCSIZE1 is set to 24; the ECC[1-8]RESULTSIZE bits are set to 0, and the ECC9RESULTSIZE bit is set to 1.

12.4.3.4.11.3.1.2 ECC Enabling

The *GPMC_ECC_CONFIG*[3-1] ECCCS bit field selects the allocated chip-select. The *GPMC_ECC_CONFIG*[0] ECCENABLE bit enables ECC computation on the next detected read or write access to the selected chip-select.

The following fields must not be changed or cleared while an ECC computation is in progress:

- CCPOINTER
- ECCCLEAR
- ECCSIZE
- ECCjRESULTSIZE (where j = 1 to 9)
- ECC16B
- ECCCS

The ECC accumulator and ECC result register must not be changed or cleared while an ECC computation is in progress.

Table 12-193 describes the ECC enable settings.

Table 12-205. ECC Enable Settings

Bit Field	Register	Value	Comments
ECCCS	*GPMC_ECC_CONFIG*	0–3	Selects the chip-select where ECC is computed
ECC16B	*GPMC_ECC_CONFIG*	0/1	Selects column number for ECC calculation
ECCCLEAR	*GPMC_ECC_CONTROL*	0–7	Clears all ECC result registers
ECCPOINTER	*GPMC_ECC_CONTROL*	0–7	A write to this bit field selects the ECC result register where the first ECC computation is stored. Set to 1 by default.

Table 12-205. ECC Enable Settings (continued)

Bit Field	Register	Value	Comments
ECCSIZE1	*GPMC_ECC_SIZE_CONFIG*	0x00–0xFF	Defines ECCSIZE1
ECCSIZE0	*GPMC_ECC_SIZE_CONFIG*	0x00–0xFF	Defines ECCSIZE0
ECCjRESULTSIZE (j from 1 to 9)	*GPMC_ECC_SIZE_CONFIG*	0/1	Selects the size of ECCn result register
ECCENABLE	*GPMC_ECC_CONFIG*	1	Enables the ECC computation

12.4.3.4.11.3.1.3 ECC Computation

The ECC algorithm is a multiple parity bit accumulation computed on the odd and even bit streams extracted from the byte or Word16 streams. The parity accumulation is split into row and column accumulations, as shown in Figure 12-196 and Figure 12-197. The intermediate row and column parities are used to compute the upper level row and column parities. Only the final computation of each parity bit is used for ECC comparison and correction.

P1o = bit7 XOR bit5 XOR bit3 XOR bit1 on each byte of the data stream
P1e = bit6 XOR bit4 XOR bit2 XOR bit0 on each byte of the data stream

P2o = bit7 XOR bit6 XOR bit3 XOR bit2 on each byte of the data stream
P2e = bit5 XOR bit4 XOR bit1 XOR bit0 on each byte of the data stream

P4o = bit7 XOR bit6 XOR bit5 XOR bit4 on each byte of the data stream
P4e = bit3 XOR bit2 XOR bit1 XOR bit0 on each byte of the data stream

Each column parity bit is XORed with the previous accumulated value.

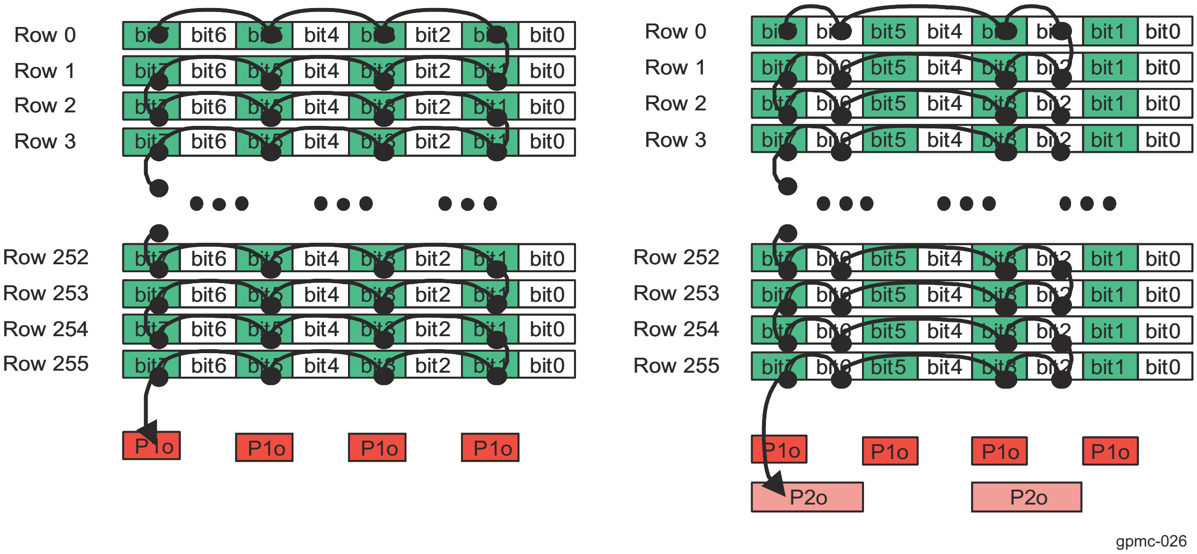

Figure 12-196. Hamming Code Accumulation Algorithm (1/2)

For line parities, the bits of each new data are XORed together, and line parity bits are computed as described below:

P8e = row0 XOR row2 XOR row4 XOR ... XOR row254
P8o = row1 XOR row3 XOR row5 XOR ... XOR row255

P16e = row0 XOR row1 XOR row4 XOR row5 XOR ... XOR row252 XOR row 253
P16o = row2 XOR row3 XOR row6 XOR row7 XOR ... XOR row254 XOR row 255

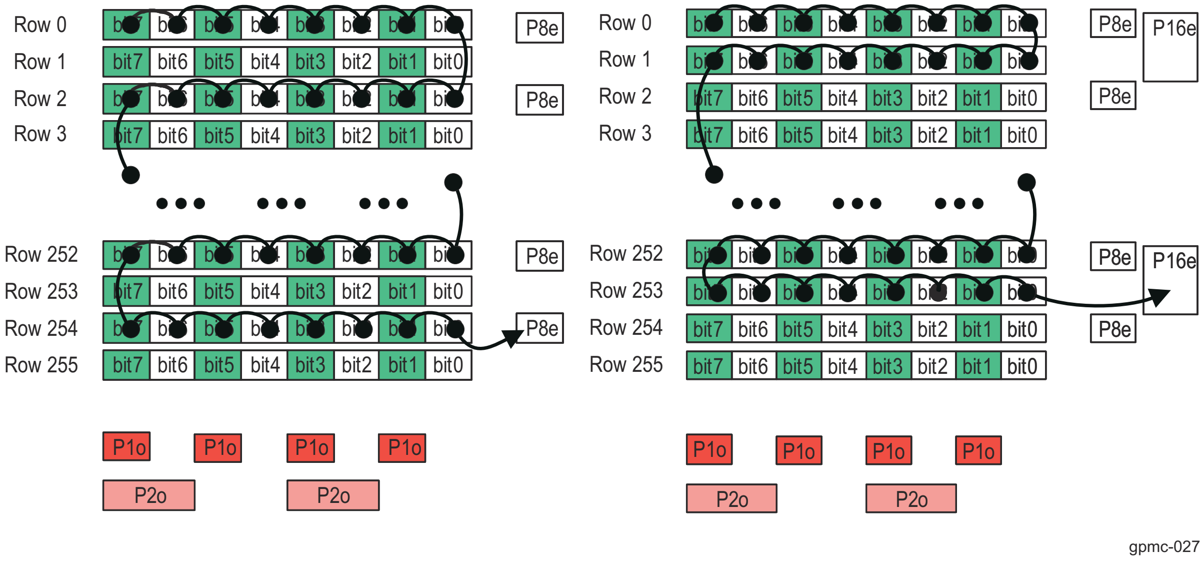

Figure 12-197. Hamming Code Accumulation Algorithm (2/2)

Unused parity bits in the result registers are set to 0.

Figure 12-198 shows ECC computation for a 256-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and sixteen row parity bits (P8o-P16o-P32o--P1024o for odd parities, and P8e-P16e-P32e--P1024e for even parities).

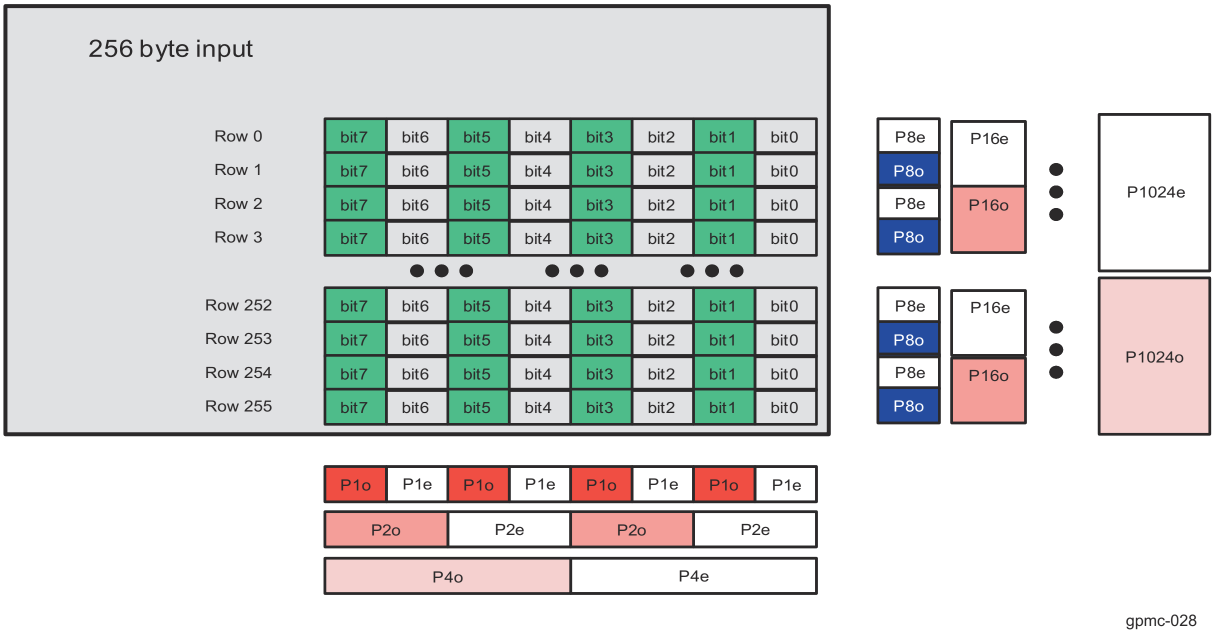

Figure 12-198. ECC Computation for a 256-Byte Data Stream (Read or Write)

Figure 12-199 shows ECC computation for a 512-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and eighteen row parity bits (P8o-P16o-P32o--P1024o- - P2048o for odd parities, and P8e-P16e-P32e--P1024e- P2048e for even parities).

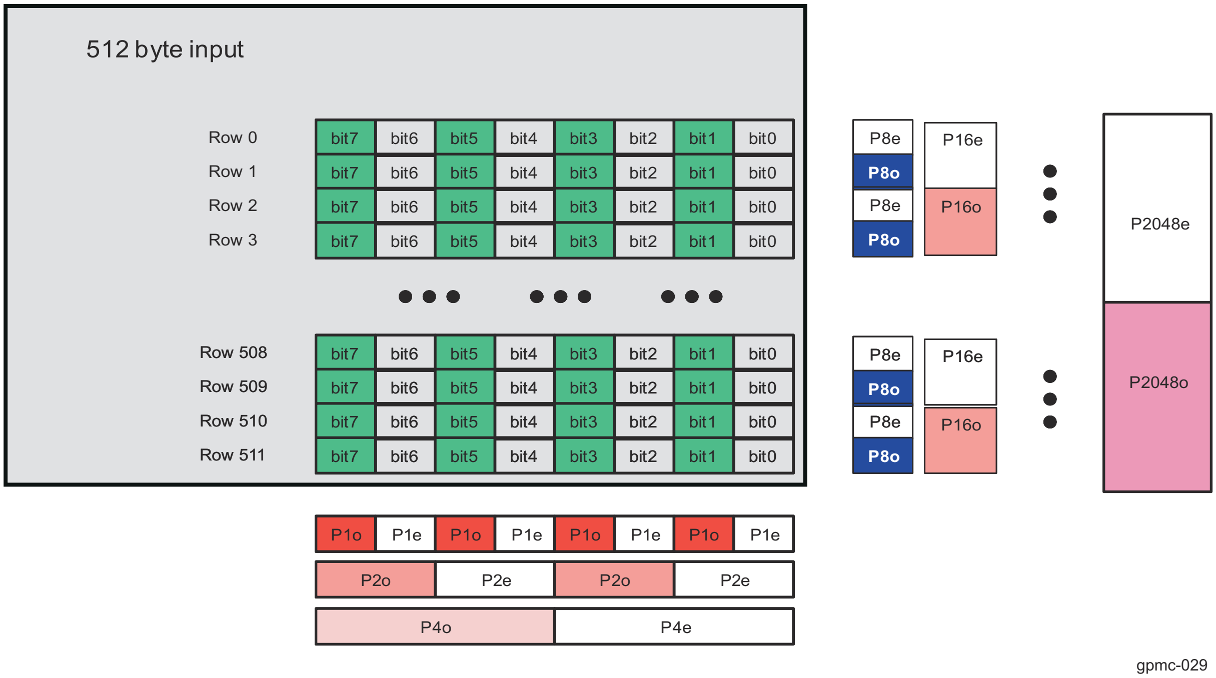

Figure 12-199. ECC Computation for a 512-Byte Data Stream (Read or Write)

For a 2-KB page, four 512 bytes ECC calculations plus 1 for the spare area are required. Results are stored in the *GPMC_ECCj_RESULT* registers (where j = 1 to 9).

12.4.3.4.11.3.1.4 ECC Comparison and Correction

To detect an error, the computed ECC result must be XORed with the parity value stored in the spare area of the accessed page.

- If the result of this logical XOR is all 0s, no error is detected and the read data is correct.
- If every second bit in the parity result is a 1, 1 bit is corrupted and is located at bit address (P2048o, P1024o, P512o, P256o, P128o, P64o, P32o, P16o, P8o, P4o, P2o, P1o). Software must correct the corresponding bit.
- If only 1 bit in the parity result is 1, it is an ECC error and the read data is correct.

12.4.3.4.11.3.1.5 ECC Calculation Based on 8-Bit Word

The 8-bit-based ECC computation is used for 8-bit-wide NAND device interfacing.

The 8-bit-based ECC computation can be used for 16-bit-wide NAND device interfacing to get backward compatibility on the error-handling strategy used with 8-bit-wide NAND devices. In this case, the 16-bit-wide data read from or written to the NAND device is fragmented into 2 bytes. According to little-endian access, the LSB of the 16-bit-wide data is ordered first in the byte stream used for 8-bit-based ECC computation.

12.4.3.4.11.3.1.6 ECC Calculation Based on 16-Bit Word

ECC computation based on an 16-bit word is used for 16-bit-wide NAND device interfacing. This ECC computation is not supported when interfacing an 8-bit-wide NAND device, and the GPMC_ECC_CONFIG[7] ECC16B bit must be set to 0 when interfacing an 8-bit-wide NAND device.

The parity computation based on 16-bit words affects the row and column parity mapping. The main difference is that the odd and even parity bits P8o and P8e are computed on rows for an 8-bit-based ECC and on columns for a 16-bit based ECC. Figure 12-200 and Figure 12-201 show a 128 Word16 ECC computation scheme and a 256 16-bit word ECC computation scheme.

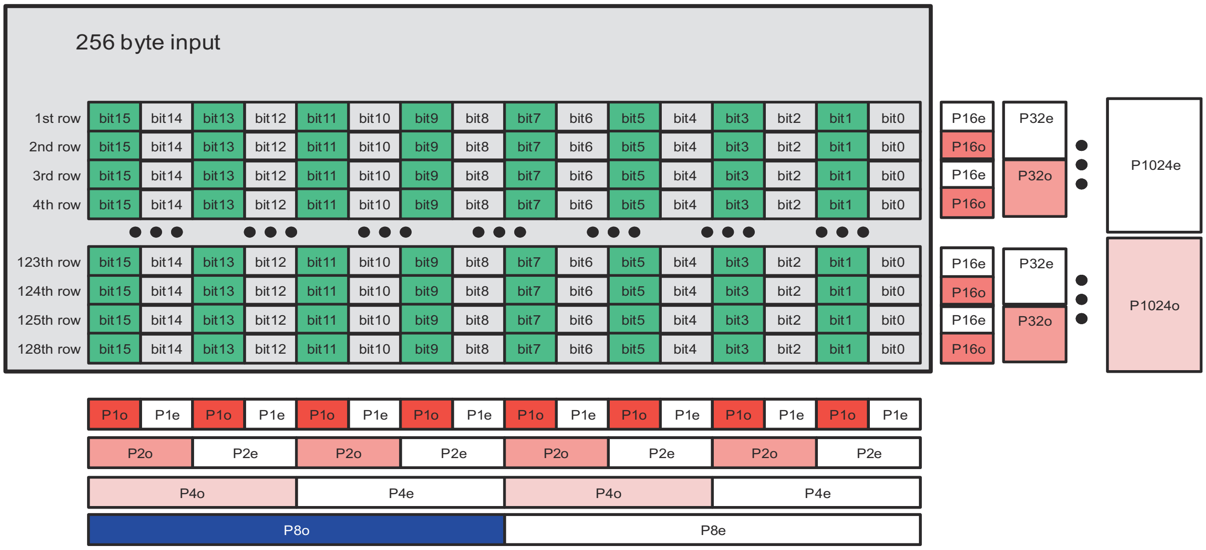

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Figure 12-200. 128 Word16 ECC Computation

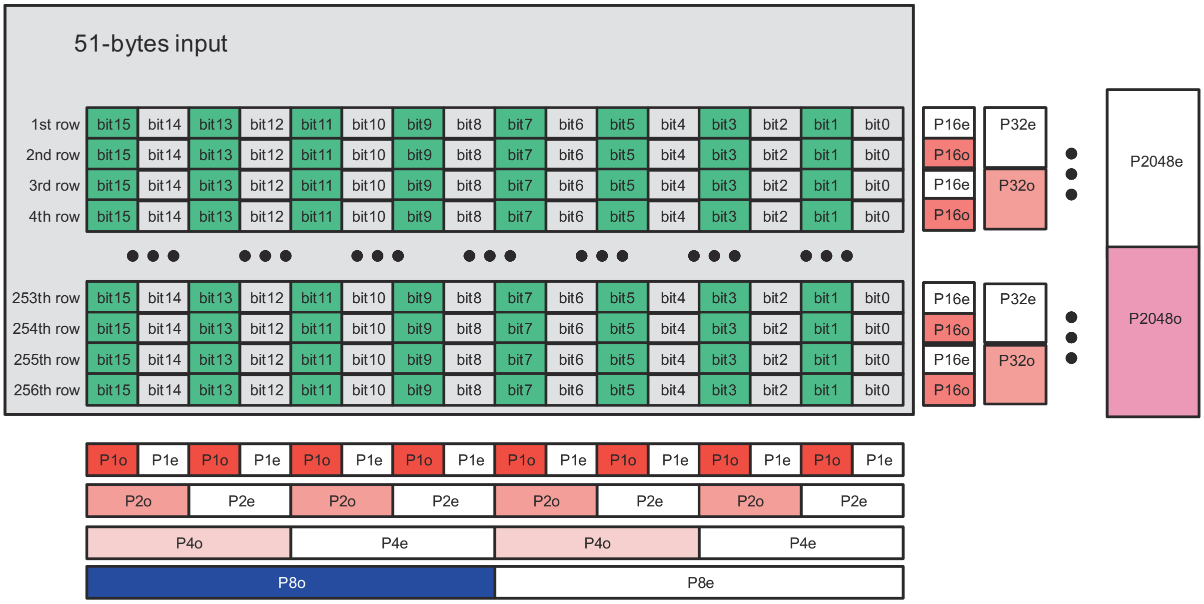

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Figure 12-201. 256 Word16 ECC Computation

12.4.3.4.11.3.2 BCH Code

All references to ECC in this subsection refer to the 4- to 16-bit error correction BCH code.

12.4.3.4.11.3.2.1 Requirements

1. Read and write accesses to a NAND flash take place by whole pages, in a predetermined sequence: first the data byte page itself, and then some spare bytes, including the BCH ECC (and other information). The NAND device can cache a full page, including spares, for read and write accesses.
    - Typical page write sequence:
        - Sequential write to NAND cache of main data plus spare data, for a page. ECC is calculated on the fly. Calculated ECC can be inserted on the fly in the spares or replaced by dummy accesses.

  - When the calculated ECC is replaced by dummy accesses, it must be written to the cache in a second, separate phase. The ECC module is disabled during that time.
  - NAND writes its cache line (page) to the array.
- Typical page read sequence:
  - Sequential read of a page. ECC is calculated on the fly.
  - The status of the ECC module buffers determines the presence of errors.

2. Accesses to several memories can be interleaved by the GPMC, but only one of those memories at a time can be a NAND using the BCH engine; in other words, only one BCH calculation (for example, for a single page) can be ongoing at any time. The sequential nature of NAND accesses ensures that the data is always written or read out in the same order. BCH-relevant accesses are selected by the chip-selects of the GPMC.
3. Each page can hold up to 4KB of data, spare bytes not included. This means up to 8 × 512-byte BCH messages. Because all the data is written or read out first, followed by the BCH ECC, the BCH engine must be able to hold eight 104-bit remainders or syndromes (or smaller, 52-bit ones) at the same time.

   The BCH module can store all remainders internally. After the page start, an internal counter is used to detect the 512-byte sector boundaries. On those boundaries, the current remainder is stored and the divider reset for the next calculation. At the end of the page, the BCH module contains all remainders.
4. NAND access cycles hold 8 or 16 bits of data each (1 or 2 bytes); Each NAND cycle takes at least four cycles of the GPMC internal clock. This means the NAND flash timing parameters must define a RDCYCLETIME and a WRCYCLETIME of at least four clock cycles after optimization when using the BCH calculator.
5. The spare area is assumed to be large enough to hold the BCH ECC; that is, to have a message of at least 13 bytes available per 512-byte sector of data. The zone of unused spare area by the ECC may or may not be protected by the same ECC scheme, by extending the BCH message beyond 512 bytes (the maximum codeword is 1023 bytes long, ECC included, which leaves much space to cover spare bytes).

12.4.3.4.11.3.2.2 Memory Mapping of BCH Codeword

BCH encoding considers a block of data to protect as a polynomial message M(x). In a standard case, 512 bytes of data (that is, 2^{12} bits = 4096 bits) are seen as a polynomial of degree $2^{12} - 1 = 4095$, with parameters ranging from M0 to M4095. For 512 bytes of data, 52 bits are required for 4-bit error correction, 104 bits are required for 8-bit error correction, and 207 bits are required for 16-bit error correction. The ECC is a remainder polynomial R(x) of degree 103 (or 51, depending on the selected mode). The complete codeword C(x) is the concatenation of M(x) and R(x), as described in Table 12-194.

Table 12-206. Flattened BCH Codeword Mapping (512 Bytes + 104 Bits)

	Message M(x)			ECC R(x)		
Bit Number	M4095	...	M0	R103	...	R0

If the message is extended by the addition of spare bytes to be protected by the same ECC, the principle is still valid. For example, a 3-byte extension of the message gives a polynomial message M(x) of degree $((512 + 3) \times 8) - 1 = 4119$, for a total of 3 + 13 = 16 spare bytes of spare, all protected as part of the same codeword.

The message and the ECC bits are manipulated and mapped in the GPMC byte-oriented system. The ECC bits are stored in the following registers (where i = 0 to 3):

- GPMC_BCH_RESULT_0_i
- GPMC_BCH_RESULT_1_i
- GPMC_BCH_RESULT_2_i
- GPMC_BCH_RESULT_3_i

12.4.3.4.11.3.2.2.1 Memory Mapping of Data Message

The data message mapping must follow the following rules:

- Bit endianness within a byte is little-endian; that is, the bytes LSB is also the lowest-degree polynomial parameter: a byte b7-b0 (with b0 the LSB) represents a segment of polynomial $b7 * x^{(7+i)} + b6 * x^{(6+i)} + ... + b0 * x^i$

- The message is mapped in the NAND starting with the highest-order parameters, that is, in the lowest addresses of a NAND page.
- Byte endianness within the 16-bit words in the NAND is big-endian (that is, the same message mapped in 8- and 16-bit memories has the same content at the same byte address).

Note

The BCH module has no visibility over actual addresses. The most important point is the sequence of data words the BCH sees. However, the NAND page is always scanned incrementally in read and write accesses, which produces the mapping patterns described in the following.

Table 12-195 and Table 12-196 describe the mapping of the same 512-byte vector (typically, a BCH message) in the NAND memory space. The byte address is only an offset module 512 (0x200), because the same page may contain several contiguous 512-byte sectors (BCH blocks). The LSB and MSB are, respectively, the bits M0 and M(2^{12}–1) of the codeword mapping discussed previously. In both cases the data vectors are aligned; that is, their boundaries coincide with the RAM data word boundaries.

Table 12-207. Aligned Message Byte Mapping in 8-Bit NAND

Byte Offset	8-Bit Word
0x000	(MSB) Byte 511 (0x1FF)
0x001	Byte 510 (0x1FE)
...	...
0x1FF	Byte 0 (0x0) (LSB)

Table 12-208. Aligned Message Byte Mapping in 16-Bit NAND

Byte Offset	16-Bit Word MSB	16-Bit Word LSB
0x000	Byte 510 (0x1FE)	(MSB) Byte 511 (0x1FF)
0x002	Byte 508 (0x1FC)	Byte 509 (0x1FD)
...	...	...
0x1FE	Byte 0 (0x0)	(LSB) Byte 1 (0x1)

Table 12-197 through Table 12-202 list the mapping in memory of arbitrarily-sized messages, starting on access (byte or 16-bit word) boundaries for more clarity. Note that message may actually start and stop on arbitrary nibbles. A nibble is a 4-bit entity. The unused nibbles are not discarded, and they can still be used by the BCH module, but as part of the next message section (for example, on the ECC of another sector).

Table 12-209. Aligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	**4-Bit Least Significant Nibble**
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
S/2 – 2	Nibble 3	Nibble 2
S/2 – 1	Nibble 1	Nibble 0 (LSB)

Table 12-210. Misaligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	**4-Bit Least Significant Nibble**
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
(S + 1) / 2 – 2	Nibble 2	Nibble 1

Table 12-210. Misaligned Nibble Mapping of Message in 8-Bit NAND (continued)

Byte Offset	8-Bit Word	
(S + 1) / 2 – 1	Nibble 0 (LSB)	

Table 12-211. Aligned Nibble Mapping of Message in 16-Bit NAND

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
S/2 – 4	Nibble 5	Nibble 4	Nibble 7	Nibble 6
S/2 – 2	Nibble 1	Nibble 0 (LSB)	Nibble 3	Nibble 2

Table 12-212. Misaligned Nibble Mapping of Message in 16-Bit NAND (1 Unused Nibble)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 1) / 2 – 4	Nibble 4	Nibble 3	Nibble 6	Nibble 5
(S + 1) / 2 – 2	Nibble 0 (LSB)		Nibble 2	Nibble 1

Table 12-213. Misaligned Nibble Mapping of Message in 16-Bit NAND (2 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 2) / 2 – 4	Nibble 3	Nibble 2	Nibble 5	Nibble 4
(S + 2) / 2 – 2			Nibble 1	Nibble 0 (LSB)

Table 12-214. Misaligned Nibble Mapping of Message in 16-Bit NAND (3 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 3) / 2 – 4	Nibble 2	Nibble 1	Nibble 4	Nibble 3
(S + 3) / 2 – 2			Nibble 0 (LSB)	

Many other cases exist than those given in the previous tables; for example, where the message does not start on a word boundary.

12.4.3.4.11.3.2.2.2 Memory-Mapping of the ECC

The ECC (or remainder) is presented by the BCH module as a single 104-bit (or 52-bit), little-endian vector. Software must fetch those 13 bytes (or 6 bytes) from the module interface and then store them to the spare area (page write) in the NAND or to an intermediate buffer for comparison with the stored ECC (page read). There are no constraints on the ECC mapping inside the spare area: it is software-controlled.

It is advised, however, to maintain a coherence in the respective formats of the message or the ECC remainder once they have been read out of the NAND. The error correction algorithm works from the complete codeword (concatenated message and remainder) once an error is detected. The creation of this codeword must be made as straightforward as possible.

There are cases in which the same NAND access contains both data and the ECC protecting that data. This is the case when the data/ECC boundary (which can be on any nibble) does not coincide with an access boundary. The ECC is calculated on the fly following the write. In that case, the write must also contain part of the ECC because it is impossible to insert the ECC on the fly. Instead:

- During the initial page write (BCH encoding), the ECC is replaced by dummy bits. The BCH encoder is by definition turned OFF during the ECC section, so the BCH result is unmodified.
- During a second phase, the ECC is written to the correct location, next to the actual data.
- The completed line buffer is then written to the NAND array.

12.4.3.4.11.3.2.2.3 Wrapping Modes

For a given wrapping mode, the module automatically goes through a specific number of sections as data is being fed into the module. For each section, the BCH core can be enabled (in which case the data is fed to the BCH divider) or not (in which case the BCH simply counts to the end of the section). When enabled, the data is added to the ongoing calculation for a given sector number (for example, number 0).

Wrapping modes are described as follows. To better understand and see the real-life read and write sequences implemented with each mode, see Section 12.4.3.4.11.3.2.3 , *Supported NAND Page Mappings and ECC Schemes*.

For each mode:

- A sequence describes the mode in pseudo language, with, for each section, the size and the buffer used for ECC processing (if ON). The programmable lengths are size, size0, and size1.
- A checksum condition is given. If the checksum condition is not respected for a given mode, the module behavior is unpredictable. S is the number of sectors in the page; size0 and size1 are the section sizes programmed for the mode, in nibbles.

Wrapping modes 8 through 11 insert a 1-nibble padding where the BCH processing is OFF. This is intended for t = 4 ECC, where ECC is 6 bytes long and the ECC area is expected to include (at least) 1 unused nibble to remain byte-aligned.

12.4.3.4.11.3.2.2.3.1 Manual Mode (0x0)

This mode is intended for short sequences, added manually to a given buffer through the software data port input. A complete page may be built out of several such sequences.

To process an arbitrary sequence of 4-bit nibbles, accesses to the software data port, containing the appropriate data, must be made. If the sequence end does not coincide with an access boundary (for example, to process 5 nibbles = 20 bits in 16-bit access mode) and those nibbles must be skipped, a number of unused nibbles must be programmed in GPMC_ECC_SIZE_CONFIG[31-22] ECCSIZE1 In the same example, 5 nibbles to process + 3 to discard = 8 nibbles = 2 × 16-bit accesses. Software must set:

- GPMC_ECC_SIZE_CONFIG[21-12] ECCSIZE0 = 0x5
- GPMC_ECC_SIZE_CONFIG[31-22] ECCSIZE1 = 0x3

Note

In the following figures, size and size0 are the same parameter.

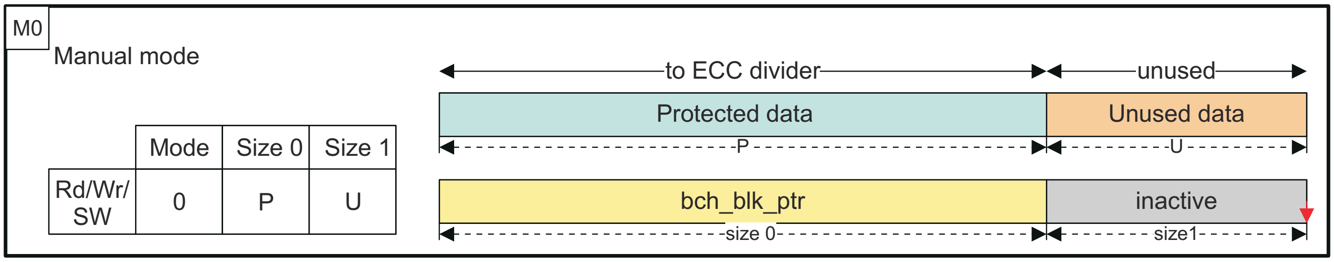

Figure 12-202. Manual Mode Sequence and Mapping

Section processing sequence:

- One time with buffer
  - size0 nibbles of data, processing ON
  - size1 nibbles of unused data, processing OFF

Checksum: size0 + size1 nibbles must fit in a whole number of accesses.

In the following sections, S is the number of sectors in the page.

12.4.3.4.11.3.2.2.3.2 Mode 0x1

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.4.3.4.11.3.2.2.3.3 Mode 0xA (10)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - 1 nibble pad spare, processing OFF
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

12.4.3.4.11.3.2.2.3.4 Mode 0x2

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.4.3.4.11.3.2.2.3.5 Mode 0x3

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.4.3.4.11.3.2.2.3.6 Mode 0x7

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.4.3.4.11.3.2.2.3.7 Mode 0x8

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

12.4.3.4.11.3.2.2.3.8 Mode 0x4

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.4.3.4.11.3.2.2.3.9 Mode 0x9

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

12.4.3.4.11.3.2.2.3.10 Mode 0x5

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.4.3.4.11.3.2.2.3.11 Mode 0xB (11)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

12.4.3.4.11.3.2.2.3.12 Mode 0x6

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.4.3.4.11.3.2.3 Supported NAND Page Mappings and ECC Schemes

The following rules apply to the entire mapping description:

- Main data area (sectors) size is hardcoded to 512 bytes.
- Spare area size is programmable.
- All page sections (of main area data bytes, protected spare bytes, unprotected spare bytes, and ECC) are defined as explained in Section 12.4.3.4.11.3.2.2.1 , *Memory Mapping of Data Message*.

Each of the following sections gives a NAND page mapping example (per-sector spare mappings, pooled spare mapping, per-sector spare mapping, with ECC separated at the end of the page).

In the mapping diagrams, sections that belong to the same BCH codeword have the same color (blue or green); unprotected sections are not covered (orange) by the BCH scheme.

Below each mapping diagram, a write (encoding) and read (decoding: syndrome generation) sequence is given, with the number of the active buffers at each point in time (yellow). In the inactive zones (grey), no computing is taking place but the data counter is still active.

In Figure 12-203 through Figure 12-205, the tables on the left summarize the mode, size0, and size1 parameters to program for, respectively, write and read processing of a page, with the given mapping, where:

- P is the size of spare byte section Protected by the ECC (in nibbles)
- U is the size of spare byte section Unprotected by the ECC (in nibbles)
- E is the size of the ECC (in nibbles)
- S is the number of Sectors per page (two in the current diagrams)

Each time the processing of a BCH block is complete (ECC calculation for write/encoding, syndrome generation for read/decoding, indicated by red arrows), the update pointer is pulsed. The processing for block 0 can be the first or the last to complete, depending on the NAND page mapping and operation (read or write). All examples show a page size of 1 KB + spares; that is, S = 2 sectors of 512 bytes. The same principles can be extended to larger pages by adding more sectors.

The actual BCH codeword size is used during the error location work to restrict the search range: by definition, errors can happen only in the codeword that was actually written to the NAND, not in the mathematical codeword of $n = 2^{13} – 1 = 8191$ bits; that codeword (higher-order bits) is all-zero and implicit during computations.

The actual BCH codeword size depends on the mode, the programmed sizes, and the sector number (all sizes in nibbles):

- Spares mapped and protected per sector (below: see M1-M2-M3-M9-M10):
  - All sectors: (512) + P + E
- Spares pooled and protected by sector 0 (below: see M5-M6):
  - Sector 0 codeword: (512) + P + E
  - Other sectors: (512) + E
- Unprotected spares (below: see M4-M7-M8-M11-M12):
  - All codewords (512) + E

12.4.3.4.11.3.2.3.1 Per-Sector Spare Mappings

In these schemes, each 512-byte sector of the main area has its own dedicated section of the spare area. The spare area of each sector is composed of:

- ECC, which must be located after the data it protects
- Other data, which may or may not be protected by the ECC for its sector.

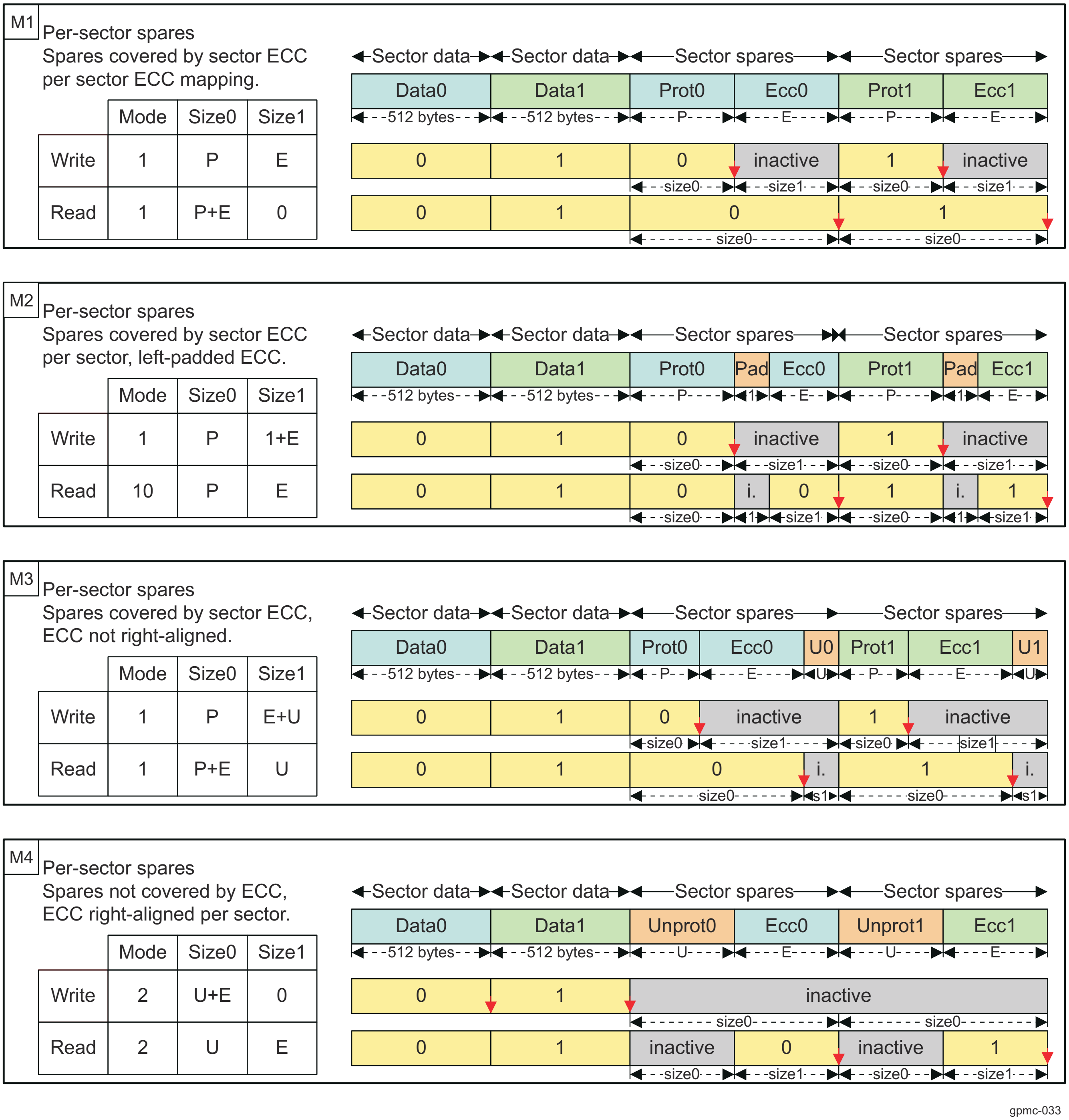

M1 Per-sector spares
Spares covered by sector ECC
per sector ECC mapping.

	Mode	Size0	Size1
Write	1	P	E
Read	1	P+E	0

M2 Per-sector spares
Spares covered by sector ECC
per sector, left-padded ECC.

	Mode	Size0	Size1
Write	1	P	1+E
Read	10	P	E

M3 Per-sector spares
Spares covered by sector ECC,
ECC not right-aligned.

	Mode	Size0	Size1
Write	1	P	E+U
Read	1	P+E	U

M4 Per-sector spares
Spares not covered by ECC,
ECC right-aligned per sector.

	Mode	Size0	Size1
Write	2	U+E	0
Read	2	U	E

Figure 12-203. NAND Page Mapping and ECC: Per-Sector Schemes

12.4.3.4.11.3.2.3.2 Pooled Spare Mapping

In the following schemes, the spare area is pooled for the page.

- The ECC of each sector is aligned at the end of the spare area.
- The non-ECC spare data may or may not be covered by the ECC of sector 0.

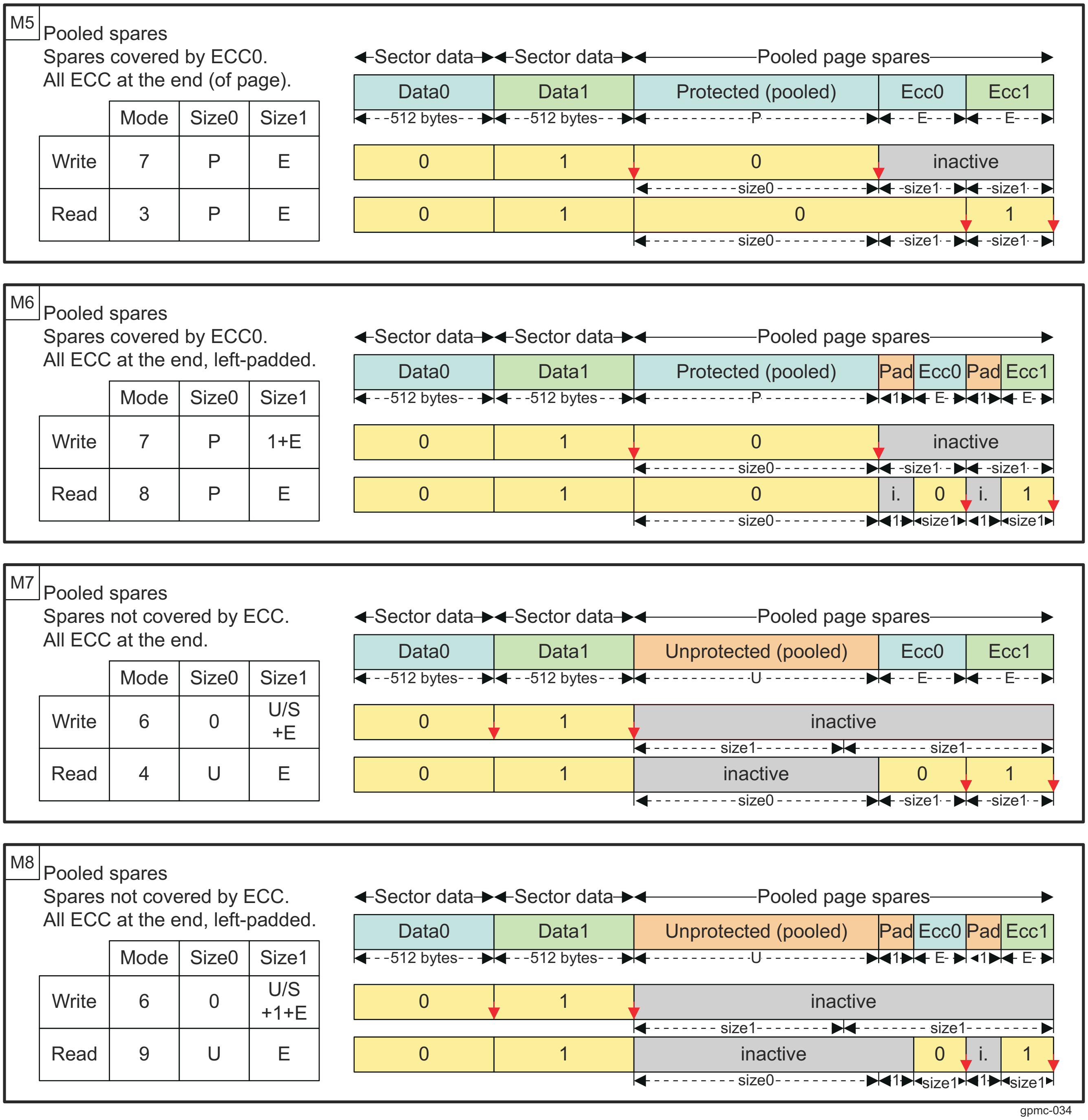

M5

	Mode	Size0	Size1
Write	7	P	E
Read	3	P	E

M6

	Mode	Size0	Size1
Write	7	P	1+E
Read	8	P	E

M7

	Mode	Size0	Size1
Write	6	0	U/S +E
Read	4	U	E

M8

	Mode	Size0	Size1
Write	6	0	U/S +1+E
Read	9	U	E

Figure 12-204. NAND Page Mapping and ECC: Pooled Spare Schemes

12.4.3.4.11.3.2.3.3 Per-Sector Spare Mapping, with ECC Separated at the End of the Page

In these schemes, each 512-byte sector of the main area is associated with two sections of the spare area.

- ECC section, all aligned at the end of the page
- Other data section, aligned before the ECCs, each of which may or may not be protected by the ECC for its sector.

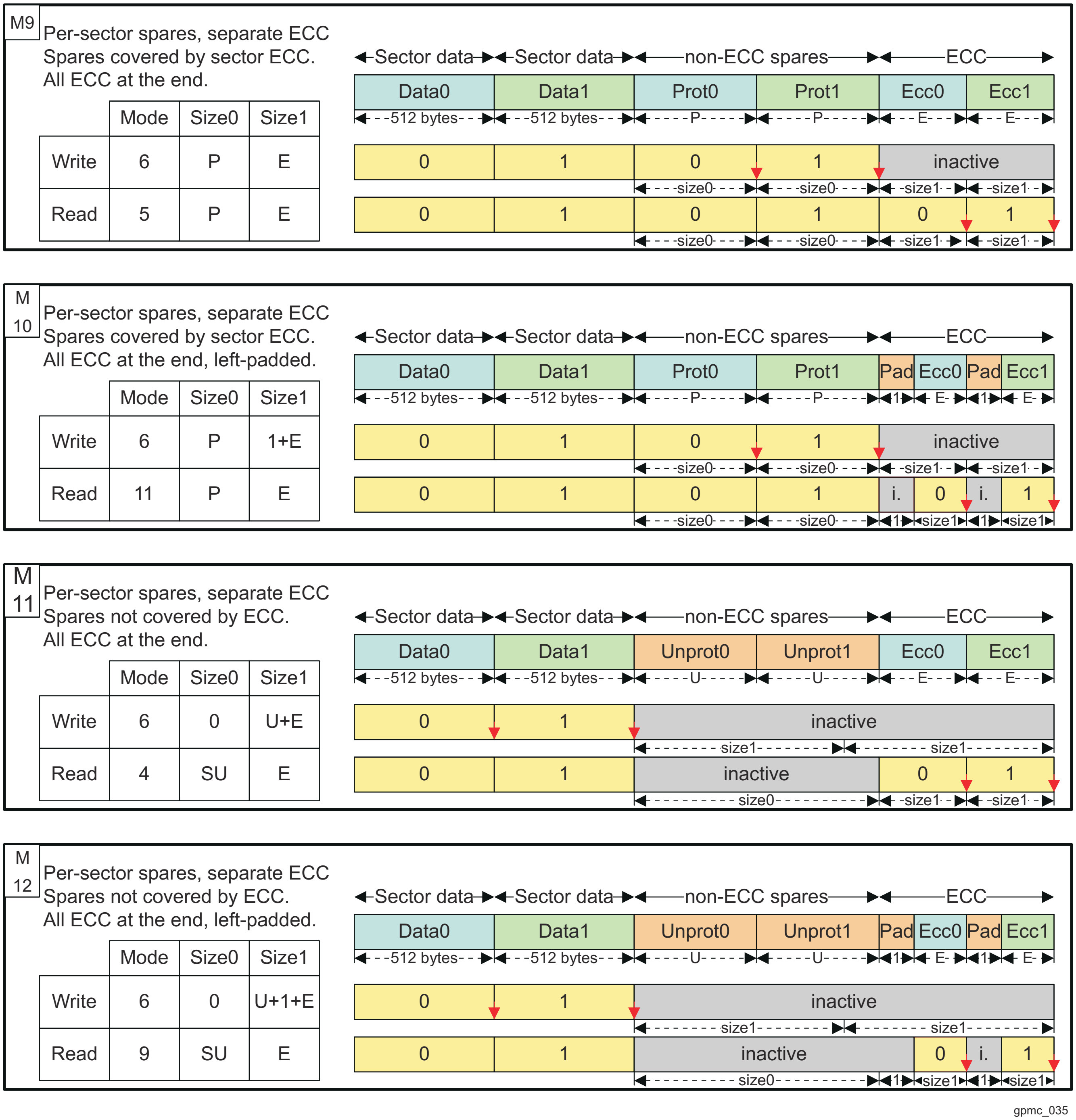

M9

	Mode	Size0	Size1
Write	6	P	E
Read	5	P	E

M 10

	Mode	Size0	Size1
Write	6	P	1+E
Read	11	P	E

M 11

	Mode	Size0	Size1
Write	6	0	U+E
Read	4	SU	E

M 12

	Mode	Size0	Size1
Write	6	0	U+1+E
Read	9	SU	E

Figure 12-205. NAND Page Mapping and ECC: Per-Sector Schemes, With Separate ECC

12.4.3.4.11.4 Prefetch and Write-Posting Engine

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

NAND device data access cycles are usually much slower than the CPU system frequency; such NAND read or write accesses issued by the processor affect the overall system performance, especially considering long read or write sequences required for NAND page loading or programming. To minimize this effect on system performance, the GPMC includes a prefetch and write-posting engine, which can be used to read from or write to any chip-select location in a buffered manner.

The prefetch and write-posting engine is a simplified embedded-access requester that presents requests to the access engine on a user-defined chip-select target. The access engine interleaves these requests with any request coming from the interconnect interface; as a default, the prefetch and write-posting engine has the lowest priority.

The prefetch and write-posting engine is dedicated to data-stream access (as opposed to random data access); thus, it is primarily dedicated to NAND support. The engine does not include an address generator; the request is limited to chip-select target identification. It includes a 64-byte FIFO associated with a DMA request synchronization line, for optimal DMA-based use.

The prefetch and write-posting engine uses an embedded 64-byte (32 16-bit word) FIFO to prefetch data from the NAND device in read mode (prefetch mode) or to store host data to be programmed into the NAND device in write mode (write-posting mode). The FIFO draining and filling (read and write) can be controlled by a device host processor through interrupt synchronization (an interrupt is triggered whenever a programmable threshold is reached) or by a device DMA module through DMA request synchronization, with a programmable request byte size in prefetch or posting mode.

The prefetch and write-posting engine includes a single memory pool. Therefore, only one mode, read or write, can be used at any given time. In other words, the prefetch and write-posting engine is a single-context engine that can be allocated to only one chip-select at a time for a read prefetch or a write-posting process.

The engine does not support atomic command and address phase programming and is limited to linear memory read or write access. As a consequence, it is limited to NAND data-stream access. The engine depends on the NAND software driver to control block and page opening with the correct data address pointer initialization, before the engine can read from or write to the NAND memory device.

Once started, engine data read and write sequencing is based solely on FIFO location availability and until the total programmed number of bytes is read or written.

Any host-concurrent accesses to a different chip-select are correctly interleaved with ongoing engine accesses. The engine has the lowest priority access so that host accesses to a different chip-select do not suffer a large latency.

A round-robin arbitration scheme can be enabled to ensure minimum bandwidth to the prefetch and write-posting engine in the case of back-to-back direct memory requests to a different chip-select. If the *GPMC_PREFETCH_CONFIG1*[23] PFPWENROUNDROBIN bit is enabled, the arbitration grants the prefetch and write-posting engine access to the GPMC bus for a number of requests programmed in the *GPMC_PREFETCH_CONFIG1*[19-16] PFPWWEIGHTEDPRIO bit field.

The prefetch/write-posting engine read or write request is routed to the access engine with the chip-select destination ID. After the required arbitration phase, the access engine processes the request as a single access with the data access size equal to the device size specified in the corresponding chip-select configuration.

Note

The destination chip-select configuration must be set to the NAND protocol-compatible configuration for which address lines are not used (the address bus is not changed from its current value). Selecting a different chip-select configuration can produce undefined behavior.

12.4.3.4.11.4.1 General Facts About the Engine Configuration

The engine can be configured only if the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is deasserted.

The engine must be correctly configured in prefetch or write-posting mode and must be linked to a NAND chip-select before it can be started. The chip-select is linked using the GPMC_PREFETCH_CONFIG1[26-24] ENGINECSSELECTOR bit field.

In prefetch and write-posting modes, the engine uses byte or 16-bit word access requests, respectively, for an 8- or 16-bit-wide NAND device attached to the linked chip-select. The FIFOTHRESHOLD and TRANSFERCOUNT bit fields must be programmed accordingly as a number of bytes.

When the GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE bit is set, the FIFO entry on the interconnect port side is accessible at any address in the associated chip-select memory region. When the ENABLEENGINE bit is set, any host access to this chip-select is rerouted to the FIFO input. Directly accessing the NAND device linked to this chip-select from the host is still possible through the following registers (where i = 0 to 3):

- GPMC_NAND_COMMAND_i
- GPMC_NAND_ADDRESS_i
- GPMC_NAND_DATA_i

The FIFO entry on the interconnect port can be accessed with byte, 16-bit word, or 32-bit word access size, according to little-endian format, even though the FIFO input is 32 bits wide.

The FIFO control is made easier through the use of interrupts or DMA requests associated with the FIFOTHRESHOLD bit field. The GPMC_PREFETCH_STATUS[30-24] FIFOPOINTER bit field monitors the number of available bytes to be read in prefetch mode or the number of free empty slots that can be written in write-posting mode. The GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field monitors the number of remaining bytes to be read or written by the engine according to the value of the TRANSFERCOUNT bit field. The FIFOPOINTER and COUNTVALUE bit fields are always expressed as a number of bytes even if a 16-bit-wide NAND device is attached to the linked chip-select.

In prefetch mode, when the FIFOPOINTER equals 0 (that is, the FIFO is empty), a host read access receives the byte last read from the FIFO as its response. In case of 32-bit word or 16-bit word read accesses, the last byte read from the FIFO is copied the required number of times to fit the requested word size. In write-posting mode, when the FIFOPOINTER equals 0 (that is, the FIFO is full), a host write overwrites the last FIFO byte location. There is no underflow or overflow error reporting in the GPMC.

12.4.3.4.11.4.2 Prefetch Mode

The prefetch mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is cleared.

The NAND software driver must issue the block and page opening (READ) command with the correct data address pointer initialization before the engine can be started to read from the NAND memory device. The engine is started by asserting the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit. The STARTENGINE bit automatically clears when the prefetch process completes.

If required, the ECC calculator engine must be initialized (that is, reset, configured, and enabled) before the prefetch engine is started so that the ECC is computed correctly on all data read by the prefetch engine.

When the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit is cleared, the prefetch engine starts requesting data as soon as the STARTENGINE bit is set. If using this configuration, the host must monitor the NAND device-ready pin so that it sets the STARTENGINE bit only when the NAND device is in a ready state (that is, data is valid for prefetching).

When the SYNCHROMODE bit is set, the prefetch engine starts requesting data when an active-to-inactive WAIT signal transition is detected. The transition detector must be cleared before any transition detection (see Section 12.4.3.4.11.2.2 , *Ready Pin Monitored by Hardware Interrupt*). The GPMC_PREFETCH_CONFIG1[5-4] WAITPINSELECTOR bit field selects which GPMC_WAIT pin edge detector triggers the prefetch engine in this synchronized mode.

If the STARTENGINE bit is set after the NAND address phase (page opening command), the engine is effectively started only after the actual NAND address phase completion. To prevent GPMC stall during this NAND address phase, set the STARTENGINE bit before NAND address phase completion when in synchronized mode. The prefetch engine starts when an active-to-inactive WAIT signal transition is detected. The STARTENGINE bit is automatically cleared on prefetch process completion.

The prefetch engine issues a read request to fill the FIFO with the amount of data specified by the GPMC_PREFETCH_CONFIG2[13-0] TRANSFERCOUNT bit field.

Table 12-203 describes the prefetch mode configuration.

Table 12-215. Prefetch Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Prefetch engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26-24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active.
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	0	Selects prefetch mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14-8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13-0]		Selects the number of bytes to be read or written by the engine to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0/1	Selects when the engine starts the access to the chip-select
WAITPINSELECT	GPMC_PREFETCH_CONFIG1[17-16]	0 to 1	Selects WAIT pin edge detector (if GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE = 0x1)
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 12.4.3.4.11.4.6 , *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30-28]		Number of clock cycle removed to timing parameters
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

12.4.3.4.11.4.3 FIFO Control in Prefetch Mode

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The FIFO can be drained directly by a device host processor or a DMA module channel.

In draining mode, the FIFO status can be monitored through the GPMC_PREFETCH_STATUS[30-24] FIFOPOINTER bit field or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. The FIFOPOINTER indicates the current number of available data to be read; FIFOTHRESHOLDSTATUS set to 1 indicates that at least FIFOTHRESHOLD bytes are available from the FIFO.

An interrupt can be triggered by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. The FIFO interrupt event is logged, and the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, all the available bytes must be read, or at least enough bytes to get below the programmed FIFO threshold, and the FIFOEVENTSTATUS bit must be cleared to enable further interrupt events. The FIFOEVENTSTATUS bit must always be reset before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt generation must be enabled after enabling the STARTENGINE bit.

Prefetch completion can be monitored through the GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field. COUNTVALUE indicates the number of currently remaining data to be requested according to the TRANSFERCOUNT value. An interrupt can be triggered by the GPMC when the prefetch process is complete (that is, COUNTVALUE equals 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set.

At prefetch completion, the TERMINALCOUNT interrupt event is also logged, and the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the TERMINALCOUNTSTATUS bit must be cleared. The TERMINALCOUNTSTATUS bit must always be cleared prior to asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

Note

The COUNTVALUE value is valid only when the prefetch engine is active (started), and an interrupt is only triggered when COUNTVALUE reaches 0, that is, when the prefetch engine automatically goes from an active to an inactive state.

The number of bytes to be prefetched (programmed in TRANSFERCOUNT) must be a multiple of the programmed FIFOTHRESHOLD to trigger the correct number of interrupts allowing a deterministic and transparent FIFO control. If this guideline is respected, the number of ISR accesses is always required and the FIFO is always empty after the last interrupt is triggered. In other cases, the TERMINALCOUNT interrupt must be used to read the remaining bytes in the FIFO (the number of remaining bytes being lower than the FIFOTHRESHOLD value).

In DMA draining mode, the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes are ready to be read from the FIFO. The DMA channel that owns this DMA request must be programmed so that the number of bytes programmed in FIFOTHRESHOLD is read from the FIFO during the DMA request process. The DMA request is kept active until this number of bytes has effectively been read from the FIFO, and no other DMA request can be issued until the ongoing active request is complete.

In prefetch mode, the TERMINALCOUNT event is also a source of DMA requests if the number of bytes to be prefetched is not a multiple of FIFOTHRESHOLD, the remaining bytes in the FIFO can be read by the DMA channel using the last DMA request. This assumes that the number of remaining bytes to be read is known and controlled through the DMA channel programming model.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (the STARTENGINE bit is set to 1). The associated DMA channel must always be enabled after setting the STARTENGINE bit so that the out-of-date active DMA request does not trigger spurious DMA transfers.

12.4.3.4.11.4.4 Write-Posting Mode

The write-posting mode is selected when the *GPMC_PREFETCH_CONFIG1*[0] ACCESSMODE bit is set.

The NAND software driver must issue the correct address pointer initialization command (page program) before the engine can start writing data into the NAND memory device. The engine starts when the *GPMC_PREFETCH_CONTROL*[0] STARTENGINE bit is set to 1. The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the NAND software driver must issue the second cycle program command and monitor the status for programming process completion (adding ECC handling, if required).

If used, the ECC calculator engine must be started (configured, reset, and enabled) before the posting engine is started so that the ECC parities are calculated properly on all data written by the prefetch engine to the associated chip-select.

In write-posting mode, the *GPMC_PREFETCH_CONFIG1*[3] SYNCHROMODE bit must be cleared so that posting starts as soon as the STARTENGINE bit is set and the FIFO is not empty.

If the STARTENGINE bit is set after the NAND address phase (page program command), the STARTENGINE setting is effective only after the actual NAND command completion. To prevent GPMC stall during this NAND command phase, set the STARTENGINE bit field before the NAND address completion and ensure that the associated DMA channel is enabled after the NAND address phase.

The posting engine issues a write request when valid data are available from the FIFO and until the programmed *GPMC_PREFETCH_CONFIG2*[13-0] TRANSFERCOUNT accesses are complete.

The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the NAND software driver must issue the second cycle program command and monitor the status for programming process completion. The closing program command phase must be issued only when the full NAND page has been written into the NAND flash write buffer, including the spare area data and the ECC parities, if used.

Table 12-204 describes the write-posting configuration.

Table 12-216. Write-Posting Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	*GPMC_PREFETCH_CONTROL*[0]	0	Write-posting engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	*GPMC_PREFETCH_CONFIG1*[26-24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active
ACCESSMODE	*GPMC_PREFETCH_CONFIG1*[0]	1	Selects write-posting mode
FIFOTHRESHOLD	*GPMC_PREFETCH_CONFIG1*[14-8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	*GPMC_PREFETCH_CONFIG2*[13-0]		Selects the number of bytes to be read or written by the engine from/to the selected chip-select
SYNCHROMODE	*GPMC_PREFETCH_CONFIG1*[3]	0	Engine starts the access to chip-select as soon as STARTENGINE is set.
ENABLEOPTIMIZEDACCESS	*GPMC_PREFETCH_CONFIG1*[27]	0/1	See Section 12.4.3.4.11.4.6 , *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	*GPMC_PREFETCH_CONFIG1*[30-28]		
ENABLEENGINE	*GPMC_PREFETCH_CONFIG1*[7]	1	Engine enabled
STARTENGINE	*GPMC_PREFETCH_CONTROL*[0]	1	Starts the prefetch engine

12.4.3.4.11.4.5 FIFO Control in Write-Posting Mode

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The FIFO can be filled directly by a device host processor or a DMA module channel.

In filling mode, the FIFO status can be monitored through the FIFOPOINTER or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. FIFOPOINTER indicates the current number of available free byte places in the FIFO, and the FIFOTHRESHOLDSTATUS bit, when set, indicates that at least FIFOTHRESHOLD free byte places are available in the FIFO.

An interrupt can be issued by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, enough bytes must be written to fill the FIFO or to get below the programmed threshold, and the FIFOEVENTSTATUS bit must be cleared to get further interrupt events. The FIFOEVENTSTATUS bit must always be cleared before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt must be enabled after enabling the STARTENGINE bit.

The posting completion can be monitored through the GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field. COUNTVALUE indicates the current number of remaining data to be written based on the value of the TRANSFERCOUNT bit field. An interrupt is issued by the GPMC when the write-posting process completes (that is, COUNTVALUE equal to 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the

TERMINALCOUNTSTATUS bit must be cleared. The TERMINALCOUNTSTATUS bit must always be cleared before asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

Note

The value of the COUNTVALUE bit field is valid only if the write-posting engine is active and started, and an interrupt is issued only when COUNTVALUE reaches 0; that is, when the posting engine automatically goes from active to inactive.

In DMA filling mode, the DMAMode bit field in the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes-free places are available in the FIFO. The DMA channel that owns this DMA request must be programmed so that a number of bytes equal to the value programmed in the FIFOTHRESHOLD bit field are written into the FIFO during the DMA access. The DMA request remains active until the associated number of bytes has effectively been written into the FIFO, and no other DMA request can be issued until the ongoing active request completes.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (STARTENGINE set to 1). The associated DMA channel must always be enabled after setting the STARTENGINE bit so that an out-of-date active DMA request does not trigger spurious DMA transfers.

In write-posting mode, DMA or CPU fills the FIFO with no consideration for the associated byte enables. Any byte stored in the FIFO is written into the memory device.

12.4.3.4.11.4.6 Optimizing NAND Access Using the Prefetch and Write-Posting Engine

Access time to a NAND memory device can be optimized for back-to-back accesses if the associated nCS signal is not deasserted between accesses. The GPMC access engine can track prefetch engine accesses to optimize the access timing parameter programmed for the allocated chip-select, if no accesses to other chip-selects (that is, interleaved accesses) occur. Similarly, the access engine also eliminates CYCLE2CYCLEDELAY even if CYCLE2CYCLESAMECSEN is set. This capability is limited to the prefetch and write-posting engine accesses, and accesses to a NAND memory device (through the defined chip-select memory region or through the GPMC_NAND_DATA_i location, where i = 0 to 3) are never optimized.

The GPMC_PREFETCH_CONFIG1[27] ENABLEOPTIMIZEDACCESS bit must be set to enable optimized accesses. To optimize access time, the GPMC_PREFETCH_CONFIG1[30-28] CYCLEOPTIMIZATION bit field defines the number of GPMC_FCLK cycles to be suppressed from the following timing parameters:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSOFFTIME
- ADVOFFTIME
- OEOFFTIME
- WEOFFTIME

Figure 12-206 shows that in the case of back-to-back accesses to the NAND flash through the prefetch engine, CYCLE2CYCLESAMECSEN is forced to 0 when using optimized accesses. The first access uses the regular timing settings for this chip-select. All accesses after this one use settings reduced by x clock cycles, x being defined by the GPMC_PREFETCH_CONFIG1[30-28] CYCLEOPTIMIZATION bit field.

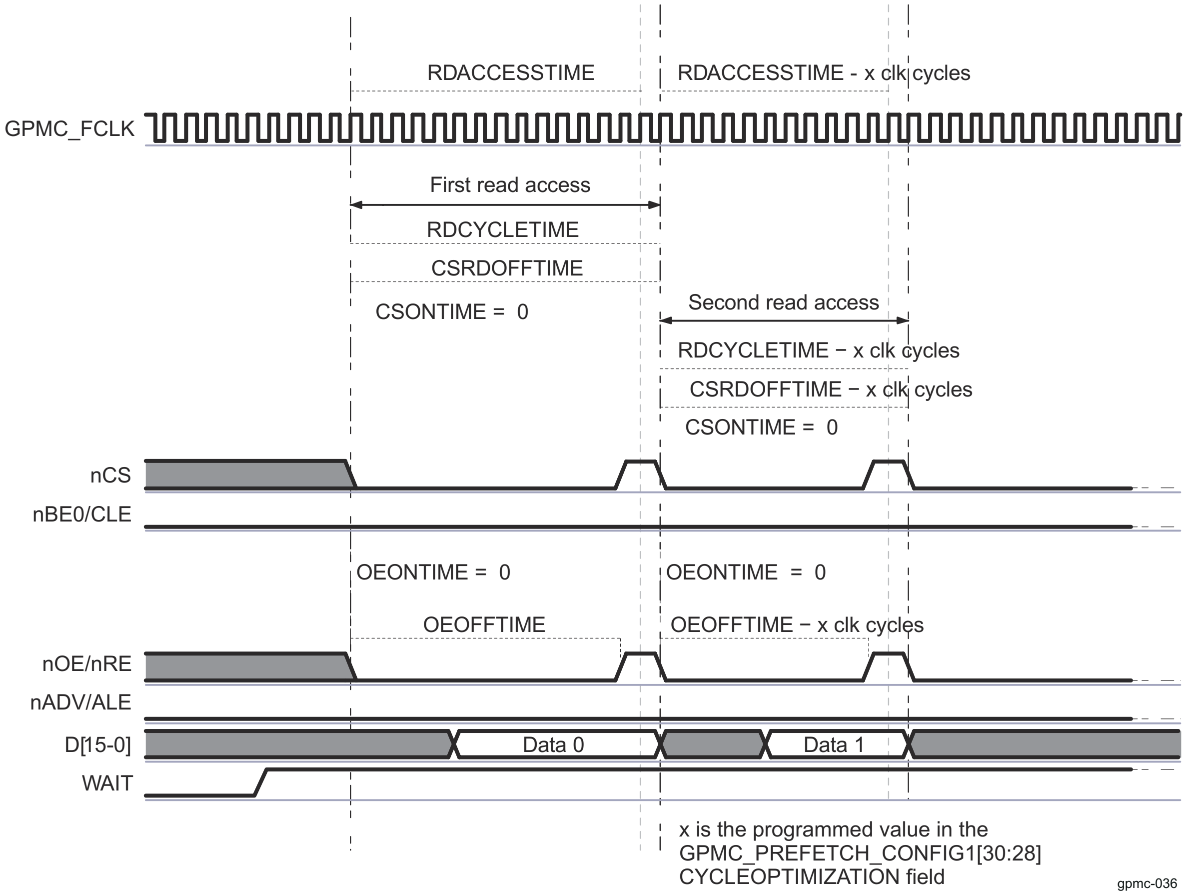

Figure 12-206. NAND Read Cycle Optimization Timing Description

12.4.3.4.11.4.7 Interleaved Accesses Between Prefetch and Write-Posting Engine and Other Chip-Selects

Any on-going read or write access from the prefetch and write-posting engine is completed before an access to any other chip-select can be initiated. As a default, the arbiter uses a fixed-priority algorithm, and the prefetch and write-posting engine has the lowest priority. The maximum latency added to access starting time in this case equals the RDCYCLETIME or WRCYCLETIME (optimized or not) plus the requested BUSTURNAROUND delay for bus turnaround completion programmed for the chip-select to which the NAND device is connected.

Alternatively, a round-robin arbitration can be used to prioritize accesses to the external bus. This arbitration scheme is enabled by setting the *GPMC_PREFETCH_CONFIG1*[23] PFPWENROUNDROBIN bit. When a request to another chip-select is received while the prefetch and write-posting engine is active, priority is given to the new request. The request processed thereafter is the prefetch and write-posting engine request, even if another interconnect request is passed in the mean time. The engine keeps control of the bus for an additional number of requests programmed in the *GPMC_PREFETCH_CONFIG1*[19-16] PFPWWEIGHTEDPRIO bit field. Control is then passed to the direct interconnect request.

As an example, the round-robin arbitration scheme is selected with PFPWWEIGHTEDPRIO set to 0x2. Considering that the prefetch and write-posting engine and the interconnect interface are always requesting access to the external interface, the GPMC grants priority to the direct interconnect access for one request. The GPMC then grants priority to the engine for three requests, and finally back to the direct interconnect access, until the arbiter is reset when one of the two initiators stops initiating requests.

12.4.3.4.12 GPMC Use Cases and Tips

12.4.3.4.12.1 How to Set GPMC Timing Parameters for Typical Accesses

12.4.3.4.12.1.1 External Memory Attached to the GPMC Module

As discussed in the introduction to this chapter, the GPMC module supports the following external memory types:

- Asynchronous or synchronous, 8- or 16-bit-wide memory or device
- 16-bit address/data-multiplexed or non-multiplexed NOR flash device
- 8- or 16-bit NAND flash device

The following examples describe how to calculate GPMC timing parameters by showing a typical parameter setup for the access to be performed.

The example is based on a 512-Mb multiplexed NOR flash memory with the following characteristics:

- Type: NOR flash (address/data-multiplexed mode)
- Size: 512M bits
- Data Bus: 16 bits wide
- Speed: 104-MHz clock frequency
- Read access time: 80 ns

12.4.3.4.12.1.2 Typical GPMC Setup

Table 12-205 lists some of the I/Os of the GPMC module.

Table 12-217. Typical GPMC Setup Signals

Module Pin	I/O(1)	Description
GPMC0_FCLK	Internal	Functional clock. Acts as the time reference.
GPMC0_ICLK	Internal	Interface clock. Acts as the time reference.
GPMC0_CLKOUT	O	External clock provided to the external device for synchronous operations
GPMC0_A[21-16]	O	Address
GPMC0_AD[15-0]	I/O	Data-multiplexed with addresses A[16-1] on memory side
GPMC0_CSn[3-0]	O	Chip-selects
GPMC0_ADVn_ALE	O	Address valid enable
GPMC0_OEn_REn	O	Output enable (read access only)
GPMC0_WEn	O	Write enable (write access only)
GPMC0_WAIT[1-0]	I	Ready signal from memory device. Indicates when valid burst data is ready to be read

(1) I = Input; O = Output

Figure 12-207 shows the typical connection between the GPMC module and an attached NOR Flash memory.

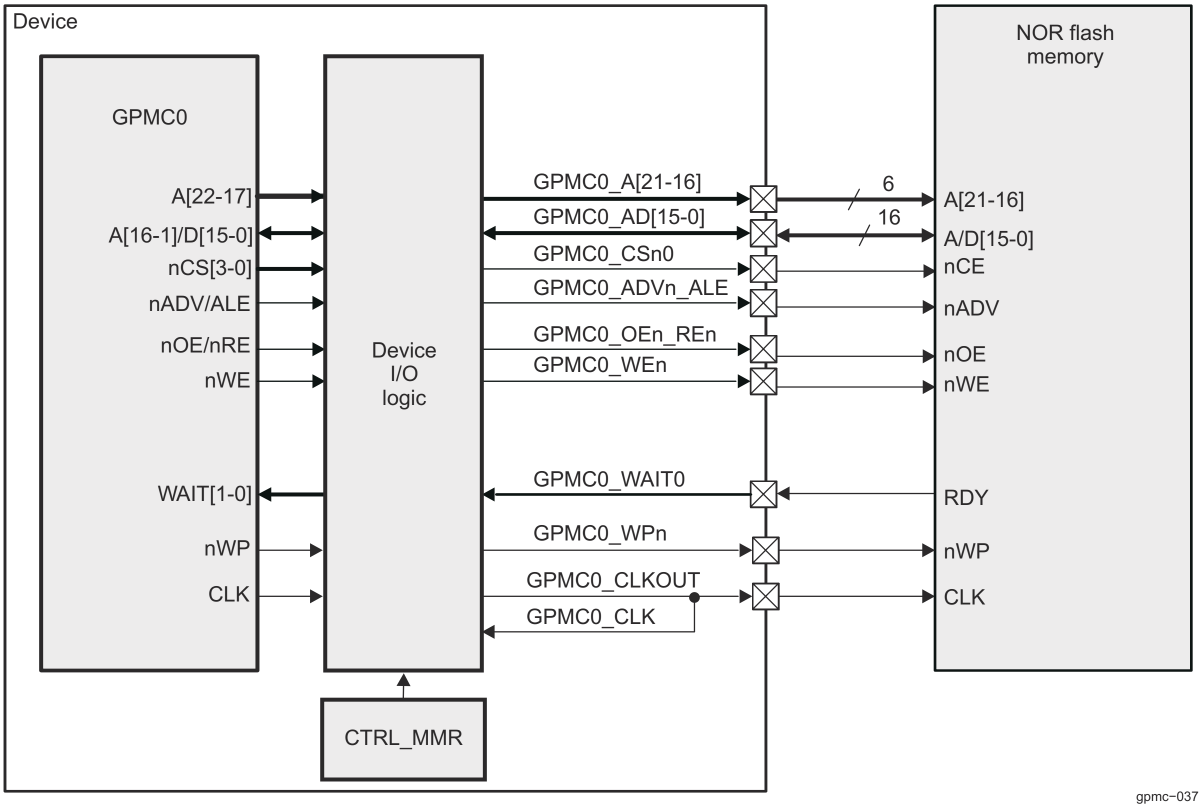

Figure 12-207. GPMC Connection to an External NOR Flash Memory

The following sections demonstrate how to calculate GPMC parameters for three access types:

- Synchronous burst read
- Asynchronous read
- Asynchronous single write

12.4.3.4.12.1.2.1 GPMC Configuration for Synchronous Burst Read Access

Note

The examples in Section 12.4.3.4.12.1.2.1 through Section 12.4.3.4.12.1.2.3 are based on a clock rate of 104 MHz. See the device-specific Datasheet for the maximum frequency appropriate for this device and the memory datasheet for the maximum frequency for the particular memory device.

The clock runs at 104 MHz (f = 104 MHz; T = 9.615 ns).

Table 12-206 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 12-207 shows how to calculate timings for the GPMC using the memory parameters.

Figure 12-208 shows the synchronous burst read access.

Table 12-218. Useful Timing Parameters on the Memory Side

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCES	nCS setup time to clock	0
tACS	Address setup time to clock	3
tIACC	Synchronous access time	80
tBACC	Burst access time valid clock to output delay	5.2

Table 12-218. Useful Timing Parameters on the Memory Side (continued)

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCEZ	Chip-select to High-Z	7
tOEZ	Output enable to High-Z	7
tAVC	nADV setup time	6
tAVD	nAVD pulse	6
tACH	Address hold time from clock	3

The following terms, which describe the timing interface between the controller and its attached device, are used to calculate the timing parameters on the GPMC side:

- Read access time (GPMC side): Time required to activate the clock + read access time requested on the memory side + data setup time required for optimal capture of a burst of data
- Data setup time (GPMC side): Ensures a good capture of a burst of data (as opposed to taking a burst of data out). One word of data is processed in one clock cycle (T = 9.615 ns). The read access time between two bursts of data is tBACC = 5.2 ns. Therefore, data setup time is a clock period – tBACC = 4.415 ns of data setup.
- Access completion (GPMC side): (Different from page burst access time) Time required between the last burst access and access completion: nCS/nOE hold time (nCS and nOE must be released at the end of an access. These signals are held to allow the access to complete).
- Read cycle time (GPMC side): Read access time + access completion
- Write cycle time for burst access: Not supported for NOR flash memory

Table 12-219. Calculating GPMC Timing Parameters

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
GPMC FCLK Divider	–	–	–	GPMCFCLKDIVIDER = 0x0
ClkActivation Time	min (tCES, tACS)	3	1	CLKACTIVATIONTIME = 0x1
RdAccessTime	roundmax (ClkActivationTime + tIACC + DataSetupTime)	94.03: (9.615 + 80 + 4.415)	10: roundmax (94.03 / 9.615)	RDACCESSTIME = 0xA
PageBurst RdAccessTime	roundmax (tBACC)	roundmax (5.2)	1	PAGEBURSTACCESSTIME = 0x1
RdCycleTime	RdAccess time + max (tCEZ, tOEZ)	101.03: (94.03 + 7)	11	RDCYCLETIME = 0xB
CsOnTime	tCES	0	0	CSONTIME = 0x0
CsReadOffTime	RdCycleTime	-	11	CSRDOFFTIME = 0xB
AdvOnTime	tAVC (1)	0	0	ADVONTIME = 0x0
AdvRdOffTime	tAVD + tAVC (2)	12	2	ADVRDOFFTIME = 0x2
OeOnTime (3)	(ClkActivationTime + tACH) < OeOnTime (ClkActivationTime + tIACC)	–	3, for instance	OEONTIME = 0x3
OeOffTime	RdCycleTime	–	11	OEOFFTIME = 0xB

(1) The external clock provided to the NOR flash is not yet available.
(2) AdvRdOffTime – AdvOnTime = tAVD; thus, AdvRdOffTime = tAVD + AdvOnTime = tAVD + tAVC.
(3) OeOnTime must ensure that addresses are available. It must not exceed the availability of the first burst of data.

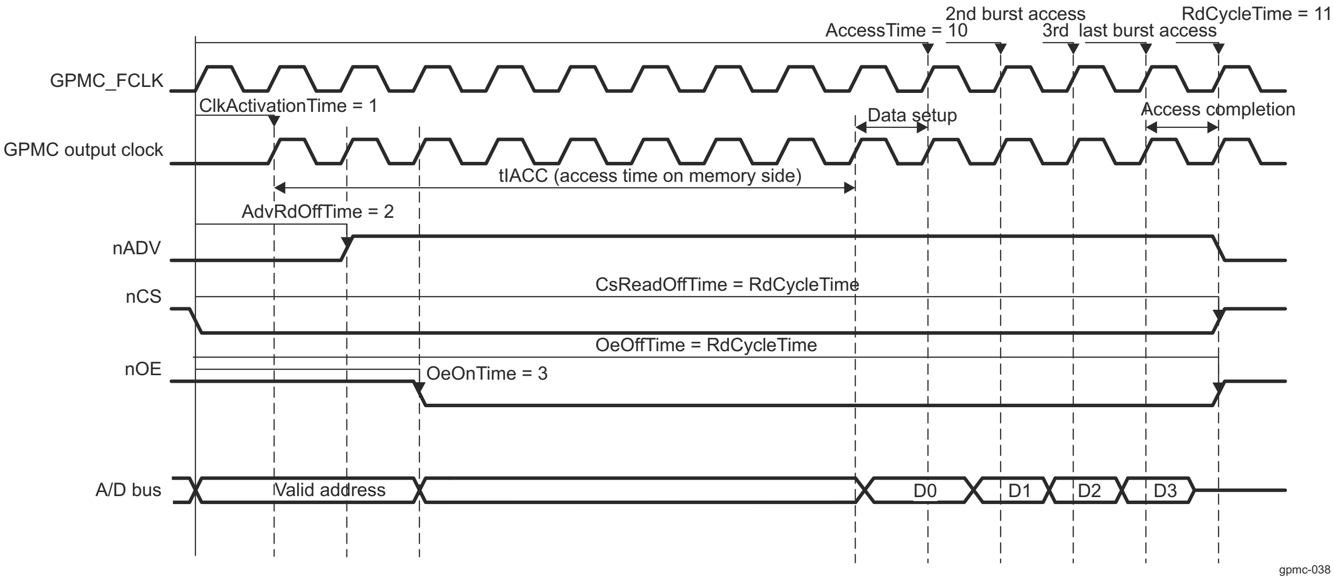

Figure 12-208. Synchronous Burst Read Access (Timing Parameters in Clock Cycles)

12.4.3.4.12.1.2.2 GPMC Configuration for Asynchronous Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9.615 ns).

Table 12-208 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 12-209 shows how to calculate timings for the GPMC using the memory parameters.

Figure 12-209 shows the asynchronous read access.

Table 12-220. AC Characteristics for Asynchronous Read Access

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCE	Read Access time from nCS low	80
tAAVDS	Address setup time to rising edge of nADV	3
tAVDP	nADV low time	6
tCAS	nCS setup time to nADV	0
tOE	Output enable to output valid	6
tOEZ	Output enable to High-Z	7

Use the following formula to calculate the RdCycleTime parameter for this typical access:

RdCycleTime = RdAccessTime + AccessCompletion = RdAccessTime + 1 clock cycle + tOEZ:

1. On the memory side, the external memory makes the data available to the output bus. This is the memory-side read access time defined in Table 12-208: the number of clock cycles between the address capture (nADV rising edge) and the data valid on the output bus.

   The GPMC requires some hold time to allow the data to be captured correctly and the access to be finished.
2. To read the data correctly, the GPMC must be configured to meet the data setup time requirement of the memory; the GPMC module captures the data on the next rising edge. This is access time on the GPMC side.
3. There must also be a data hold time for correctly reading the data (checking that there is no nOE/nCS deassertion while reading the data). This data hold time is one clock cycle (that is, RdAccessTime + 1).
4. To complete the access, nOE/nCS signals are driven to High-Z. RdAccessTime + 1 + tOEZ is the read cycle time.

5. Addresses can now be relatched and a new read cycle begun.

Table 12-221. GPMC Timing Parameters for Asynchronous Read Access

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
ClkActivationTime	n/a (asynchronous mode)			
RdAccessTime	round max (tCE)	80	10	RDACCESSTIME = 0xA
PageBurstAccessTime	N/A (single access)			
RdCycleTime	RdAccessTime + 1cycle + tOEZ	96.615	12	RDCYCLETIME = 0xC
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsReadOffTime	RdAccessTime + 1 cycle	89.615	11	CSRDOFFTIME = 0xB
AdvOnTime	tAAVDS	3	1	ADVONTIME = 0x1
AdvRdOffTime	tAAVDS + tAVDP	9	1	ADVRDOFFTIME = 0x1
OeOnTime	OeOnTime >= AdvRdOffTime (multiplexed mode)	-	3, for instance	OEONTIME = 0x3
OeOffTime	RdAccessTime + 1cycle	89.615	11	OEOFFTIME = 0xB

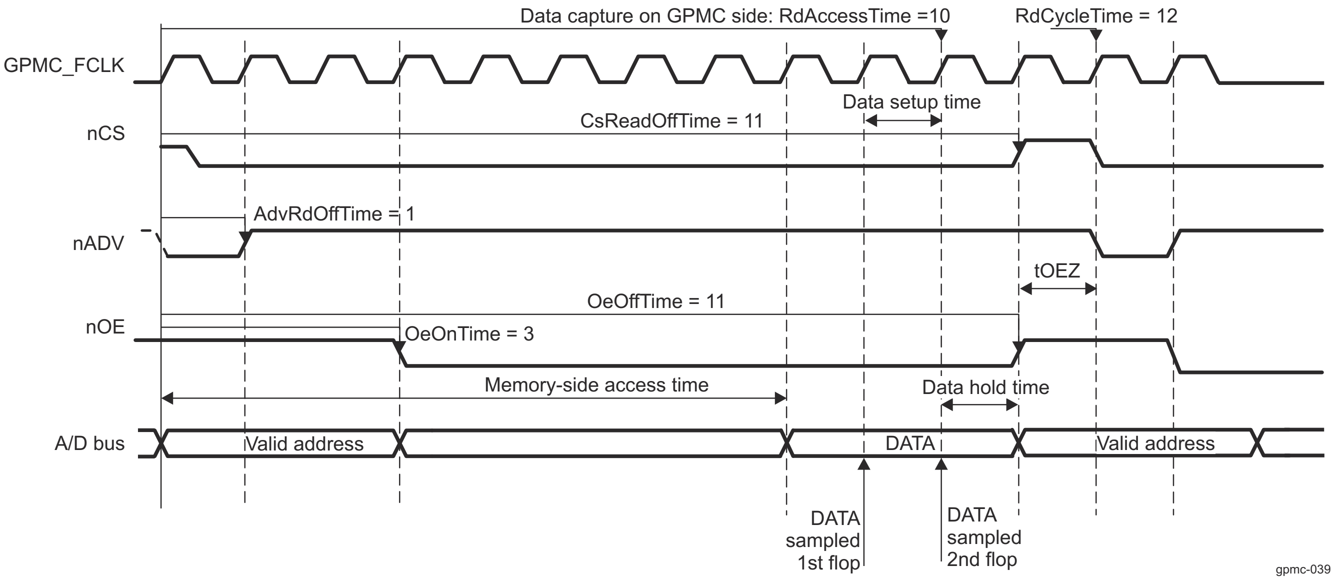

Figure 12-209. Asynchronous Single Read Access (Timing Parameters in Clock Cycles)

12.4.3.4.12.1.2.3 GPMC Configuration for Asynchronous Single Write Access

The clock runs at 104 MHz: (f = 104 MHz; T = 9.615 ns).

Table 12-211 shows how to calculate timings for the GPMC using the memory parameters.

Table 12-210 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Figure 12-210 shows the synchronous burst write access.

Table 12-222. AC Characteristics for Asynchronous Single Write (Memory Side)

AC Characteristics on the Memory Side	Description	Duration (ns)
tWC	Write cycle time	60
tAVDP	nADV low time	6
tWP	Write pulse width	25

Table 12-222. AC Characteristics for Asynchronous Single Write (Memory Side) (continued)

AC Characteristics on the Memory Side	Description	Duration (ns)
tWPH	Write pulse width high	20
tCS	nCS setup time to nWE	3
tCAS	nCS setup time to nADV	0
tAVSC	nADV setup time	3

For asynchronous single write access, write cycle time is WrCycleTime = WeOffTime + AccessCompletion = WeOffTime + 1. For the AccesCompletion, the GPMC requires one cycle of data hold time (nCS deassertion). For more information, see the device-specific Datasheet.

Table 12-223. GPMC Timing Parameters for Asynchronous Single Write

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Registers Configuration
ClkActivationTime	N/A (asynchronous mode)			
WdAccessTime	Applicable only to WAITMONITORING (the value is the same as for read access)			
PageBurstAccessTime	N/A (single access)			
WrCycleTime	WeOffTime + AccessCompletion	57.615	6	WRCYCLETIME = 0x6
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsWrOffTime	WeOffTime + 1	57.615	6	CSWROFFTIME = 0x6
AdvOnTime	tAVSC	3	1	ADVONTIME = 0x1
AdvWrOffTime	tAVSC + tAVDP	9	1	ADVWROFFTIME = 0x1
WeOnTime	tCS	3	1	WEONTIME = 0x1
WeOffTime	tCS + tWP + tWPH	48	5	WEOFFTIME = 0x5

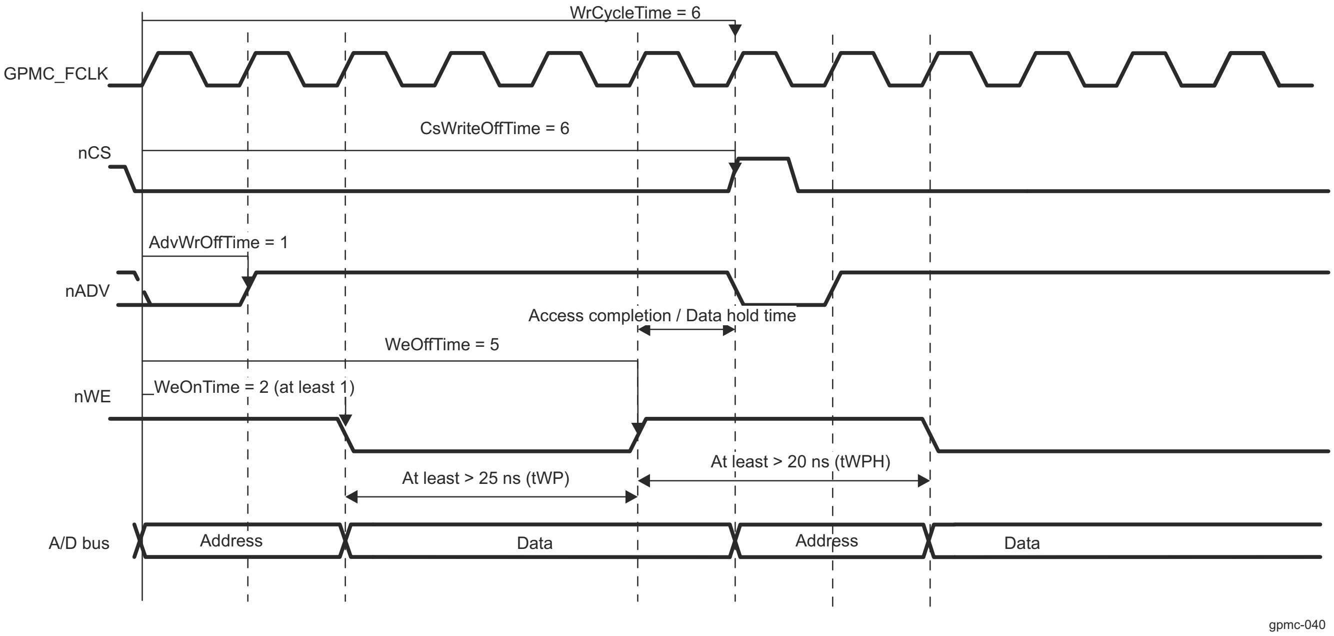

Figure 12-210. Asynchronous Single Write Access (Timing Parameters in Clock Cycles)

12.4.3.4.12.2 How to Choose a Suitable Memory to Use With the GPMC

This section is intended to help the user select a suitable memory device to interface with the GPMC controller.

12.4.3.4.12.2.1 Supported Memories or Devices

NAND flash and NOR flash architectures are the two flash technologies. The GPMC supports various types of external memory or devices, basically any one that supports NAND or NOR protocols:

- 8- and 16-bit-wide asynchronous or synchronous memory or device (only 8-bit: nonburst device)
- 16-bit address and data-multiplexed NOR flash devices (pSRAM, and so on)
- 8- and 16-bit NAND flash devices

12.4.3.4.12.2.1.1 Memory Pin Multiplexing

This section describes the interfacing differences of the GPMC supported memories.

Table 12-224. Supported Memory Interfaces

<table>
<tr><th>Function</th><th>16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash (1)</th><th>16-Bit NAND</th><th>8-Bit NAND</th></tr>
<tr><td>GPMC_A[22]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[21]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[20]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[19]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[18]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[17]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[16]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[15]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[14]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[13]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[12]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[11]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[10]</td><td>A26</td><td></td><td></td></tr>
<tr><td>GPMC_A[9]</td><td>A25</td><td></td><td></td></tr>
<tr><td>GPMC_A[8]</td><td>A24</td><td></td><td></td></tr>
<tr><td>GPMC_A[7]</td><td>A23</td><td></td><td></td></tr>
<tr><td>GPMC_A[6]</td><td>A22</td><td></td><td></td></tr>
<tr><td>GPMC_A[5]</td><td>A21</td><td></td><td></td></tr>
<tr><td>GPMC_A[4]</td><td>A20</td><td></td><td></td></tr>
<tr><td>GPMC_A[3]</td><td>A19</td><td></td><td></td></tr>
<tr><td>GPMC_A[2]</td><td>A18</td><td></td><td></td></tr>
<tr><td>GPMC_A[1]</td><td>A17</td><td></td><td></td></tr>
<tr><td>GPMC_A[0]</td><td>A16</td><td></td><td></td></tr>
<tr><td>GPMC_AD[15]</td><td>D15 or A16</td><td>IO15</td><td></td></tr>
<tr><td>GPMC_AD[14]</td><td>D14 or A15</td><td>IO14</td><td></td></tr>
<tr><td>GPMC_AD[13]</td><td>D13 or A14</td><td>IO13</td><td></td></tr>
<tr><td>GPMC_AD[12]</td><td>D12 or A13</td><td>IO12</td><td></td></tr>
<tr><td>GPMC_AD[11]</td><td>D11 or A12</td><td>IO11</td><td></td></tr>
<tr><td>GPMC_AD[10]</td><td>D10 or A11</td><td>IO10</td><td></td></tr>
<tr><td>GPMC_AD[9]</td><td>D9 or A10</td><td>IO9</td><td></td></tr>
<tr><td>GPMC_AD[8]</td><td>D8 or A9</td><td>IO8</td><td></td></tr>
<tr><td>GPMC_AD[7]</td><td>D7 or A8</td><td colspan="2">IO7</td></tr>
<tr><td>GPMC_AD[6]</td><td>D6 or A7</td><td colspan="2">IO6</td></tr>
<tr><td>GPMC_AD[5]</td><td>D5 or A6</td><td colspan="2">IO5</td></tr>
<tr><td>GPMC_AD[4]</td><td>D4 or A5</td><td colspan="2">IO4</td></tr>
</table>

Table 12-224. Supported Memory Interfaces (continued)

Function	16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash (1)	16-Bit NAND	8-Bit NAND
GPMC_AD[3]	D3 or A4	IO3	
GPMC_AD[2]	D2 or A3	IO2	
GPMC_AD[1]	D1 or A2	IO1	
GPMC_AD[0]	D0 or A1	IO0	
GPMC_CLKOUT	CLK		
GPMC_CSn0	nCS0 (chip-select)	nCE0 (chip-enable)	
GPMC_CSn1	nCS1	nCE1	
GPMC_CSn2	nCS2	nCE2	
GPMC_CSn3	nCS3	nCE3	
GPMC_ADVn_ALE	nADV (address valid)	ALE (address latch enable)	
GPMC_OEn_REn	nOE (output enable)	nRE (read enable)	
GPMC_WEn	nWE (Write enable)	nWE (write enable)	
GPMC_BE0n_CLE	nBE0 (byte enable)	CLE (command latch enable)	
GPMC_BE1n	nBE1		
GPMC_WAIT0	WAIT0	R/nB0 (ready/busy)	
GPMC_WAIT1	WAIT1	R/nB1	
GPMC_WPn	nWP (Write Protect)	nWP (Write Protect)	

(1) Addresses seen from the device side. When interfacing to the external device, A1 is connected to the memory A0, A2 to the memory A1, and so on.

12.4.3.4.12.2.1.2 NAND Interface Protocol

NAND flash architecture, introduced in 1989, is a flash technology. NAND is a page-oriented memory device; that is, read and write accesses are done by pages. NAND achieves great density by sharing common areas of the storage transistor, which creates strings of serially connected transistors (in NOR devices, each transistor stands alone). Because of its high density NAND is best suited to devices that require high capacity data storage, such as pictures, music, and data files. NAND nonvolatility makes of it a good storage solution for many applications where mobility, low power, and speed are key factors. Low pin count and simple interface are other advantages of NAND.

Table 12-213 summarizes the NAND interface signals level applied to external device or memories.

Table 12-225. NAND Interface Bus Operations Summary

Bus Operation	CLE	ALE	nCE	nWE (1)	nRE (1)	nWP
Read (cmd input)	H	L	L	RE	H	x
Read (add input)	L	H	L	RE	H	x
Write (cmd input)	H	L	L	RE	H	H
Write (add input)	L	H	L	RE	H	H
Data input	L	L	L	RE	H	H
Data output	L	L	L	H	FE	x
Busy (during read)	x	x	H (2)	H (2)	H (2)	x
Busy (during program)	x	x	x	x	x	H
Busy (during erase)	x	x	x	x	x	H
Write protect	x	x	x	x	x	L

Table 12-225. NAND Interface Bus Operations Summary (continued)

Bus Operation	CLE	ALE	nCE	nWE [(1)]	nRE [(1)]	nWP
Standby	x	x	H	x	x	H/L

---

(1) RE stands for rising edge; FE stands for falling edge

(2) Can be nCE high, or WE and nRE high.

12.4.3.4.12.2.1.3 NOR Interface Protocol

NOR flash architecture, introduced in 1988, is a flash technology. Unlike NAND, which is a sequential access device, NOR is directly addressable; that is, it is designed to be a random access device. NOR is best suited to devices used to store and run code or firmware, usually in small capacities. While NOR has fast read capabilities, it also has slow write and erase functions when compared to the NAND architecture.

Table 12-214 summarizes the level of the NOR interface signals applied to external devices or memories.

Table 12-226. NOR Interface Bus Operations Summary

Bus Operation	CLK	nADV	nCS	nOE	nWE	WAIT	DQ[15-0]
Read (asynchronous)	x	L	L	L	H	Asserted	Output
Read (synchronous)	Running	L	L	L	H	Driven	Output
Read (burst suspend)	Halted	x	L	H	H	Active	Output
Write	x	L	L	H	L	Asserted	Input
Output disable	x	x	L	H	H	Asserted	High-Z
Standby	x	x	H	x	x	High-Z	High-Z

12.4.3.4.12.2.1.4 Other Technologies

Other supported device types interact with the GPMC through the NOR interface protocol.

FPGA (Field-Programmable Gate Array) is a low-power integrated circuit based on an array of programmable logic blocks.

pSRAM (pseudo-static random access memory) is a low-power memory device. pSRAM is based on the DRAM cell with internal refresh and address control features, and interfaces as a synchronous NOR flash. It has synchronous write capability.

12.4.3.5 GPMC Basic Programming Model

12.4.3.5.1 GPMC High-Level Programming Model Overview

The goal of the basic high-level programming model is to introduce a top-down approach to users that need to configure the GPMC module.

Figure 12-211 and Table 12-215 through Table 12-216 show a programming model top-level diagram for the GPMC, and a description of each step. Each block of the diagram is described in one of the following sections through a set of registers to configure.

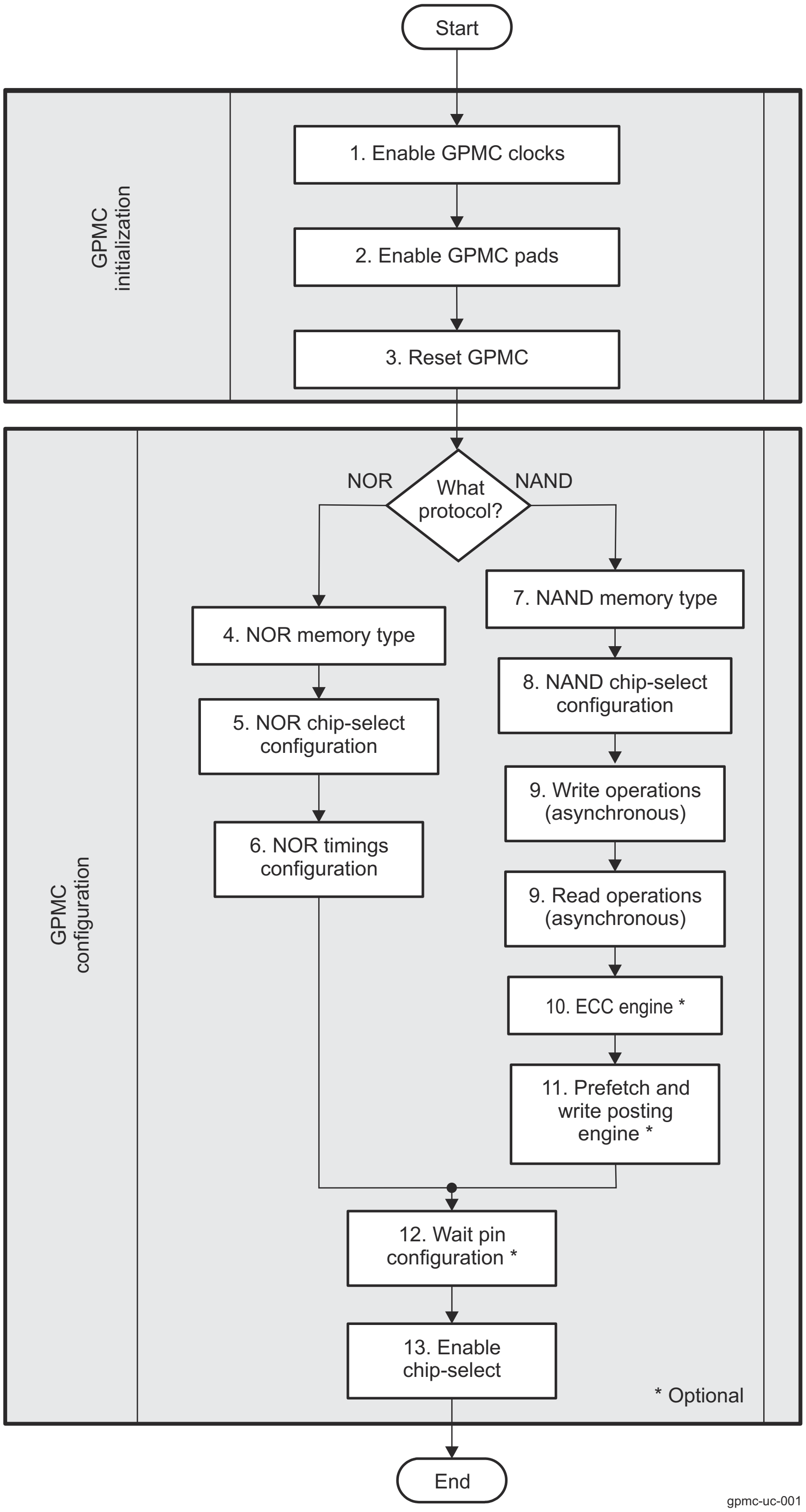

Figure 12-211. Programming Model Top-Level Diagram

Table 12-227. GPMC Configuration in NOR Mode

Step	Description
NOR Memory Type	See Table 12-217.

Table 12-227. GPMC Configuration in NOR Mode (continued)

Step	Description
NOR Chip-Select Configuration	See Table 12-218.
NOR Timings Configuration	See Table 12-219.
WAIT Pin Configuration	See Table 12-227.
Enable Chip-Select	See Table 12-228.

Table 12-228. GPMC Configuration in NAND Mode

Step	Description
NAND Memory Type	See Table 12-222.
NAND Chip-Select Configuration	See Table 12-223.
Write Operations (Asynchronous)	See Table 12-224.
Read Operations (Asynchronous)	See Table 12-224.
ECC Engine	See Table 12-225.
Prefetch and Write-Posting Engine	See Table 12-226.
WAIT Pin Configuration	See Table 12-227.
Enable Chip-Select	See Table 12-228.

12.4.3.5.2 GPMC Initialization

GPMC can be reset via software bit in LPSC. For more information, see *Reset*.

12.4.3.5.3 GPMC Configuration in NOR Mode

This section gives a generic configuration for parameters related to the NOR memory connected to the GPMC.

Table 12-229. NOR Memory Type

Subprocess Name	Register / Bit Field	Value
Set the NOR protocol.	GPMC_CONFIG1_i[11-10] DEVICETYPE	0x0
Set a device size.	GPMC_CONFIG1_i[13-12] DEVICESIZE	x
Select an address and data multiplexing protocol.	GPMC_CONFIG1_i[9] MUXADDDATA	x
Set the attached device page length.	GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH	x
Set the wrapping burst capabilities.	GPMC_CONFIG1_i[31] WRAPBURST	x
Select a timing signals latencies factor.	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Select an output clock frequency (1).	GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER	x
Choose an output clock activation time (1).	GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME	x
Set a single or multiple access for read operations (1).	GPMC_CONFIG1_i[30] READMULTIPLE	x
Set a synchronous or asynchronous mode for read operations.	GPMC_CONFIG1_i[29] READTYPE	x
Set a single or multiple access for write operations.	GPMC_CONFIG1_i[28] WRITEMULTIPLE	x
Set a synchronous or asynchronous mode for write operations.	GPMC_CONFIG1_i[27] WRITETYPE	x

(1) Applies only to synchronous configurations (or non-multiplexed asynchronous for multiple access one)

Table 12-230. NOR Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	GPMC_CONFIG7_i[5-0] BASEADDRESS	x
Select the chip-select mask address.	GPMC_CONFIG7_i[11-8] MASKADDRESS	x

Table 12-231. NOR Timings Configuration

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in various memory modes.	See *GPMC Timing Parameters*	

Table 12-232. WAIT Pin Configuration

Subprocess Name	Register/Bit Field	Value
Enable or disable WAIT pin monitoring for read operations.	GPMC_CONFIG1_i[22] WAITREADMONITORING	x
Enable or disable WAIT pin monitoring for write operations.	GPMC_CONFIG1_i[21] WAITWRITEMONITORING	x
Select a WAIT pin monitoring time.	GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME	x
Choose the input WAIT pin for the chip-select.	GPMC_CONFIG1_i[17-16] WAITPINSELECT	x

Table 12-233. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	GPMC_CONFIG7_i[6] CSVALID	x

12.4.3.5.4 GPMC Configuration in NAND Mode

This section gives a generic configuration for parameters related to the NAND memory connected to the GPMC.

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

Table 12-234. NAND Memory Type

Subprocess Name	Register/Bit Field	Value
Set the NAND protocol.	*GPMC_CONFIG1_i*[11-10] DEVICETYPE	0x2
Set a device size.	*GPMC_CONFIG1_i*[13-12] DEVICESIZE	x
Set the address and data multiplexing protocol to non-multiplexed attached device.	*GPMC_CONFIG1_i*[9] MUXADDDATA	0x0
Select a timing signals latencies factor.	*GPMC_CONFIG1_i*[4] TIMEPARAGRANULARITY	x
Set a synchronous or asynchronous mode and a single or multiple access for read and write operations.	See Section 12.4.3.5.5 , *Set Memory Access*.	x

Table 12-235. NAND Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	*GPMC_CONFIG7_i*[5-0] BASEADDRESS	x
Select the chip-select minimum granularity (16MB).	*GPMC_CONFIG7_i*[11-8] MASKADDRESS	x

Table 12-236. Asynchronous Read and Write Operations

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in asynchronous modes	See Section 12.4.3.5.6 , *GPMC Timing Parameters*.	

Table 12-237. ECC Engine

Subprocess Name	Register/Bit Field	Value
Select the ECC result register where the first ECC computation is stored (applies only to Hamming).	*GPMC_ECC_CONTROL*[3-0] ECCPOINTER	x (2)
Clear all ECC result registers.	*GPMC_ECC_CONTROL*[8] ECCCLEAR	Write 1 to clear.
Define ECCSIZE0 and ECCSIZE1.	*GPMC_ECC_SIZE_CONFIG*[21-12] ECCSIZE0 and [31-22] ECCSIZE1	x (1)

Table 12-237. ECC Engine (continued)

Subprocess Name	Register/Bit Field	Value
Select the size of each of the 9 result registers (size specified by ECCSIZE0 or ECCSIZE1).	*GPMC_ECC_SIZE_CONFIG*[j-1] ECCjRESULTSIZE where j = 1 to 9	x
Select the chip-select where ECC is computed.	*GPMC_ECC_CONTROL*[3-1] ECCCS	x
Select the Hamming code or BCH code ECC algorithm in use.	*GPMC_ECC_CONTROL*[16] ECCALGORITHM	x
Select word size for ECC calculation.	*GPMC_ECC_CONTROL*[7] ECC16B	x
If the BCH code is used, Set an error correction capability and Select a number of sectors to process.	*GPMC_ECC_CONTROL*[13-12] ECCBCHTSEL and *GPMC_ECC_CONTROL*[6-4] ECCTOPSECTOR	x
Enable the ECC computation.	*GPMC_ECC_CONTROL*[0] ECCENABLE	0x1

(1) Depends on the size of each sector in the NAND page

(2) This parameter depends on the numbers of sectors in a page.

Table 12-238. Prefetch and Write-Posting Engine

Subprocess Name	Register/Bit Field	Value
Disable the engine before configuration.	*GPMC_PREFETCH_CONTROL*[0] STARTENGINE	0x0
Select the chip-select associated with a NAND device where the prefetch engine is active.	*GPMC_PREFETCH_CONFIG1*[26-24] ENGINECSSELECTOR	x
Select access direction through prefetch engine, read or write.	*GPMC_PREFETCH_CONFIG1*[0] ACCESSMODE	x
Select the threshold used to issue an interrupt request.	*GPMC_PREFETCH_CONFIG1*[14-8] FIFOTHRESHOLD	x
Select interrupt synchronization mode.	*GPMC_PREFETCH_CONFIG1*[2] DMAMODE	x
Select if the engine immediately starts accessing the memory upon STARTENGINE assertion or if hardware synchronization based on a WAIT signal is used.	*GPMC_PREFETCH_CONFIG1*[3] SYNCHROMODE	x
Select which WAIT pin edge detector should start the engine in synchronized mode.	*GPMC_PREFETCH_CONFIG1*[5-4] WAITPINSELECTOR	x
Enter a number of clock cycles removed to timing parameters (for all back-to-back accesses to the NAND flash except the first one).	*GPMC_PREFETCH_CONFIG1*[30-28] CYCLEOPTIMIZATION	x
Enable the prefetch postwrite engine.	*GPMC_PREFETCH_CONFIG1*[7] ENABLEENGINE	0x1
Select the number of bytes to be read or written by the engine to the selected chip-select.	*GPMC_PREFETCH_CONFIG2*[13-0] TRANSFERCOUNT	x
Start the prefetch engine.	*GPMC_PREFETCH_CONTROL*[0] STARTENGINE	0x1

Table 12-239. WAIT Pin Configuration

Subprocess Name	Register/Bit Field	Value
Selects when the engine starts the access to chip-select.	*GPMC_PREFETCH_CONFIG1*[3] SYNCHROMODE	x
Select which WAIT pin edge detector should start the engine in synchronized mode.	*GPMC_PREFETCH_CONFIG1*[5-4] WAITPINSELECTOR	x

Table 12-240. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	*GPMC_CONFIG7_i*[6] CSVALID	x

12.4.3.5.5 Set Memory Access

Note

Some of the GMPC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

This section describes the bit field to configure to set the GPMC in various memory modes. Table 12-229 and Table 12-230 provide check lists for mode parameters and access type parameters, respectively.

Table 12-241. Mode Parameters Check List

Register	Bit	Name	Asynchronous				Synchronous			
			Single Read Access	Single Write Access	Multiple Read (Page) Access	Multiple Write (Page) Access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access
GPMC_CONFIG1_i	30	READMULTIPLE	0x0	Don't care	0x1 (1)	Not Supported	0x0	Don't care	0x1	Don't care
GPMC_CONFIG1_i	29	READTYPE	0x0	Don't care	0x0 (1)	Not Supported	0x1	Don't care	0x1	Don't care
GPMC_CONFIG1_i	28	WRITEMULTIPLE	Don't care	0x0	- (1)	Not Supported	Don't care	0x0	Don't care	0x1
GPMC_CONFIG1_i	27	WRITETYPE	Don't care	0x0	- (1)	Not Supported	Don't care	0x1	Don't care	0x1

(1) Multiple read is not supported in address/data-multiplexed and AAD-multiplexed modes. Multiple read is supported in non-multiplexed mode.

Table 12-242. Access Type Parameters Check List

Register	Bit	Name	Access Type		
			non-multiplexed	Address/ Data-Multiplexed	AAD-Multiplexed
GPMC_CONFIG1_i	9-8	MUXADDDATA	0x0	0x2	0x1

12.4.3.5.6 GPMC Timing Parameters

Figure 12-212 shows a programming model diagram for the NOR interfacing timing parameters.

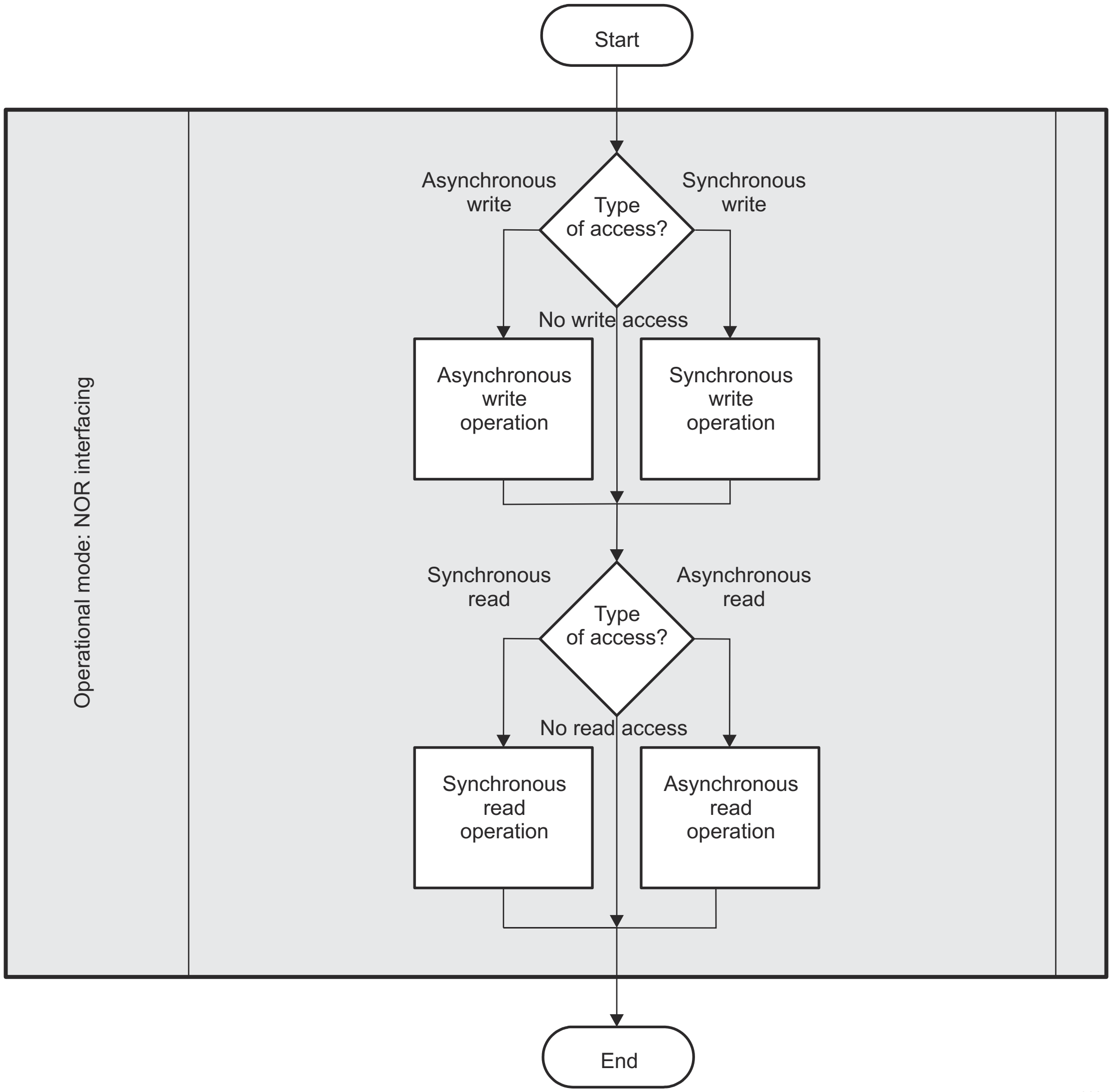

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Figure 12-212. NOR Interfacing Timing Parameters Diagram

Table 12-231 lists the bit fields to configure adequate timing parameters in various memory modes.

Table 12-243. Timing Parameters

			Asynchronous			Synchronous				Access Type		
Register	**Bit**	**Name**	**Single Read Access**	**Single Write Access**	**Multiple Read (Page) access**	**Single Read Access**	**Single Write Access**	**Multiple Read (Burst) Access**	**Multiple Write (Burst) Access**	**Non-multiplexed**	**Address/ Data-Multiplexed**	**AAD Multiplexed**
GPMC_CONFIG1_i	9	MUXADDDATA	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	29	READTYPE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	30	READMULTIPLE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	27	WRITETYPE		y			y		y	y	y	y
GPMC_CONFIG1_i	28	WRITEMULTIPLE		y			y		y	y	y	y
GPMC_CONFIG1_i	31	WRAPBURST						y	y	y	y	y

Table 12-243. Timing Parameters (continued)

			Asynchronous			Synchronous				Access Type		
GPMC_CONFIG1_i	26-25	CLKACTIVATIONTIME				y	y	y	y	y	y	y
GPMC_CONFIG1_i	19-18	WAITMONITORINGTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	4	TIMEPARAGRANULARITY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	20-16	CSWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG2_i	12-8	CSRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG2_i	7	CSEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	3-0	CSONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	30-28	ADVAADMUXWROFFTIME		y			y		y			y
GPMC_CONFIG3_i	30-29	ADVAADMUXRDOFFTIME	y		y	y		y				y
GPMC_CONFIG3_i	6-4	ADVAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG3_i	20-16	ADVWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG3_i	12-8	ADVRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG3_i	7	ADVEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	3-0	ADVONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG4_i	15-13	OEAADMUXOFFTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	6-4	OEAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	28-24	WEOFFTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	23	WEEXTRADELAY		y			y		y	y	y	y
GPMC_CONFIG4_i	19-16	WEONTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	12-8	OEOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG4_i	7	OEEXTRADELAY	y		y	y		y		y	y	y
GPMC_CONFIG4_i	3-0	OEONTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	27-24	PAGEBURSTACCESSTIME			y			y	y	y	y	y
GPMC_CONFIG5_i	20-16	RDACCESSTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	12-8	WRCYCLETIME		y			y		y	y	y	y
GPMC_CONFIG5_i	4-0	RDCYCLETIME	y		y	y		y		y	y	y
GPMC_CONFIG6_i	28-24	WRACCESSTIME		y			y		y	y	y	y
GPMC_CONFIG6_i	19-16	WRDATAONADMUXBUS		y			y		y		y	y
GPMC_CONFIG6_i	11-8	CYCLE2CYCLEDELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	7	CYCLE2CYCLESAMECSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	6	CYCLE2CYCLEDIFFCSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	3-0	BUSTURNAROUND	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG7_i	6	CSVALID	y	y	y	y	y	y	y	y	y	y

12.4.3.5.6.1 GPMC Timing Parameters Formulas

This section is intended to help the user calculate the GPMC timing bit field values. Formulas are not listed exhaustively.

The section describes:

- NAND flash interface timing parameters formulas
- Synchronous NOR flash timing parameters formulas
- Asynchronous NOR flash timing parameters formulas

For complete information, such as OPP and board effects on timings, see the device-specific Datasheet.

12.4.3.5.6.1.1 NAND Flash Interface Timing Parameters Formulas

This section lists formulas to calculate NAND timing parameters. This is the case when GPMC_CONFIG1_i[11-10] DEVICETYPE = 0x2. Table 12-232 describes the NAND timing parameters.

Table 12-244. NAND Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – GPMC_WEn valid time
B	ns	Delay time – GPMC_CS valid to GPMC_WEn valid
C	ns	Delay time – GPMC_BE0n_CLE/GPMC_ADVn_ALE high to GPMC_WEn valid
D	ns	Delay time – GPMC_AD[15-0] valid to GPMC_WEn valid
E	ns	Delay time – GPMC_WEn invalid to GPMC_AD[15-0] invalid
F	ns	Delay time – GPMC_WEn invalid to GPMC_BE0n_CLE/GPMC_ADVn_ALE invalid
G	ns	Delay time – GPMC_WEn invalid to GPMC_CS invalid
H	ns	Cycle time – Write cycle time
I	ns	Delay time – GPMC_CS valid to GPMC_OEn_REn valid
J	ns	Setup time – GPMC_AD[15-0] valid to GPMC_OEn_REn invalid
K	ns	Pulse duration – GPMC_OEn_REn valid time
L	ns	Cycle time – Read cycle time
M	ns	Delay time – GPMC_OEn_REn invalid to GPMC_CS invalid

The configuration parameters are calculated through the following formulas. For more information, see the device-specific Datasheet.

A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period

B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK period

D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK period

E = (WrCycleTime – WEOffTime * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK period

F = (ADVWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay) * GPMC_FCLK period

G = (CSWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay) * GPMC_FCLK period

H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

J = ((RdAccessTime – OEOffTime) * (TimeParaGranularity + 1) – 0.5 * OEExtraDelay)) * GPMC_FCLK period

K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK period

L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

M = (CSRdOffTime – OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay) * GPMC_FCLK period

Figure 12-213 shows a simplified example of command latch cycle timing where formulas are associated with signal waves.

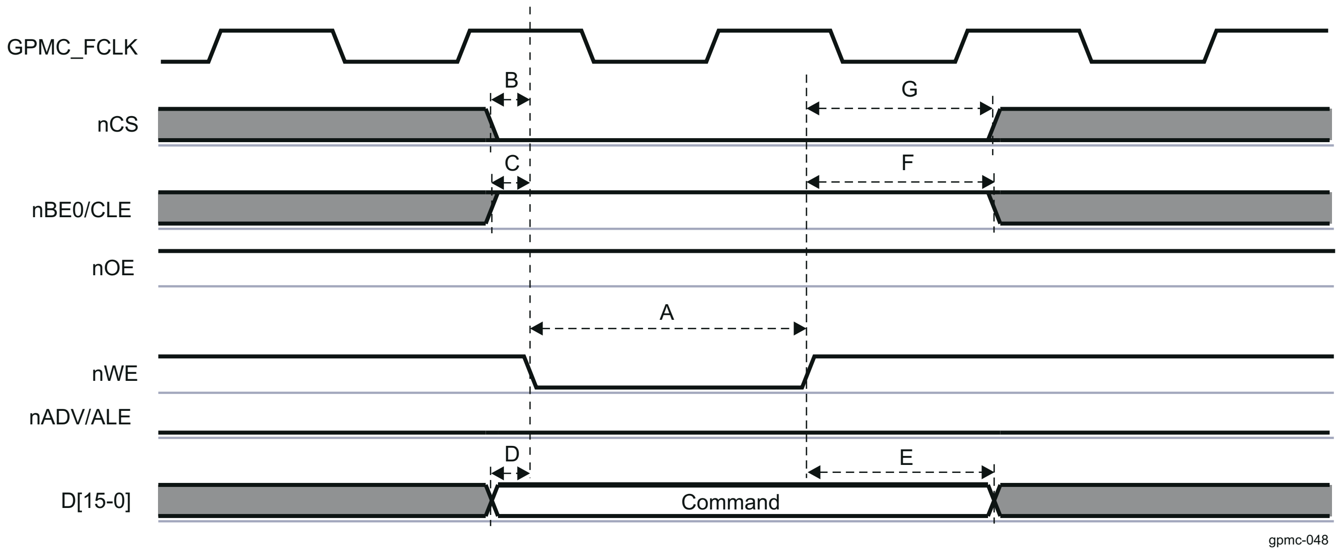

Figure 12-213. NAND Command Latch Cycle Timing Simplified Example

12.4.3.5.6.1.2 Synchronous NOR Flash Timing Parameters Formulas

This section lists all formulas to calculate synchronous NOR timing parameters. This is the case when *GPMC_CONFIG1_i*[11-10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to synchronous mode. Table 12-233 describes the synchronous NOR formulas.

Table 12-245. Synchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – nCS low
B	ns	Delay time – address bus valid to CLK first edge Delay time – nBE0 / nBE1 valid to CLK first edge
C	ns	Pulse duration – nBE0 / nBE1 low
D	ns	Delay time – CLK rising edge to nBE0 / nBE1 invalid Delay time – CLK rising edge to nADV/ALE invalid
E	ns	Delay time – CLK rising edge to nCS invalid Delay time – CLK rising edge to nOE/nRE invalid
F	ns	Delay time – CLK rising edge to nCS transition
G	ns	Delay time – CLK rising edge to nADV/ALE transition
H	ns	Delay time – CLK rising edge to nOE/nRE transition
I	ns	Delay time – CLK rising edge to nWE transition
J	ns	Delay time – CLK rising edge to A[16-1/]D[15-0] data bus transition Delay time – CLK rising edge to nBE0 / nBE1 transition
K	ns	Pulse duration – nADV/ALE low
L	ns	Delay time – WAIT invalid to first data latching CLK edge

The configuration parameters are calculated through the following formulas. For more information, see the device-specific Datasheet.

1. For single read accesses:
   A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – RDACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME – RDACCESSTIME) * GPMC_FCLK period

2. For burst read accesses (where n is the page burst access number):
   A = (CSRDOFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (RDCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
   E = (CSRDOFFTIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
3. For burst write accesses (where n is the page burst access number):
   A = (CSWROFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (WRCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (WRCYCLETIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
   E = (CSWROFFTIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
4. For all accesses:
   For nCS falling edge (chip-select activated):
   - Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSONTIME are odd) or (CLKACTIVATIONTIME and CSONTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in reading mode:
   - Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSRDOFFTIME are odd) or (CLKACTIVATIONTIME and CSRDOFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in writing mode:
   - Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSWROFFTIME are odd) or (CLKACTIVATIONTIME and CSWROFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3

F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV falling edge (nADV activated):

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVONTIME are odd) or (CLKACTIVATIONTIME and ADVONTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in reading mode:

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVRDOFFTIME are odd) or (CLKACTIVATIONTIME and ADVRDOFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in writing mode:

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVWROFFTIME are odd) or (CLKACTIVATIONTIME and ADVWROFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE falling edge (nOE activated):

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEONTIME are odd) or (CLKACTIVATIONTIME and OEONTIME are even)

  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE rising edge (nOE deactivated):

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEOFFTIME are odd) or (CLKACTIVATIONTIME and OEOFFTIME are even)
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE falling edge (nWE activated):

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEONTIME are odd) or (CLKACTIVATIONTIME and WEONTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE rising edge (nWE deactivated):

- Case where *GPMC_CONFIG1_i*[1-0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEOFFTIME are odd) or (CLKACTIVATIONTIME and WEOFFTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV low pulse duration:

- Read operation:

K = (ADVRDOFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

- Write operation:
  K = (ADVWROFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

For WAIT invalid to first data latching GPMC output clock edge:

- L = WAITMONITORINGTIME * (GPMCFCLKDIVIDER + 1) * GPMC_FCLK period + GPMC output clock period

Figure 12-214 shows a simplified example of a synchronous NOR single read where formulas are associated with signal waves.

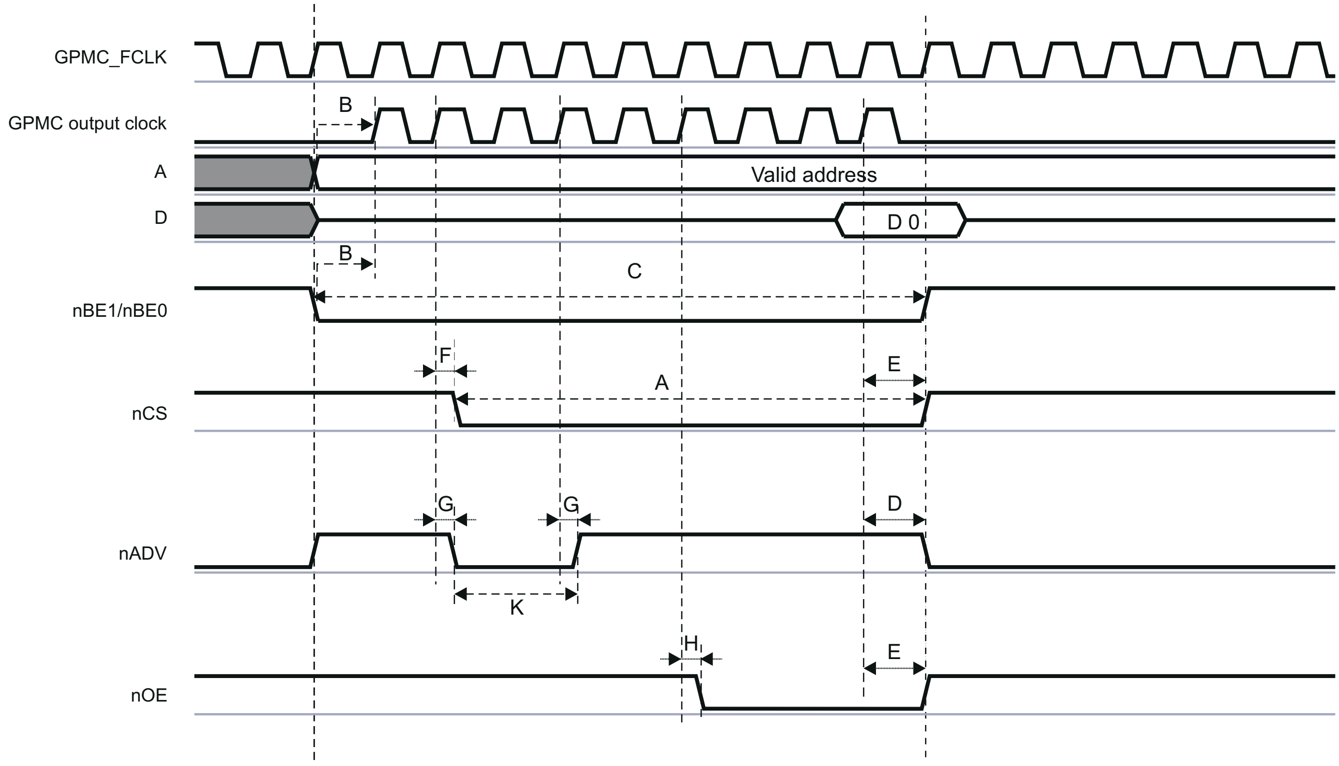

Figure 12-214. Synchronous NOR Single Read Simplified Example

12.4.3.5.6.1.3 Asynchronous NOR Flash Timing Parameters Formulas

This section lists all the formulas to calculate asynchronous NOR timing parameters. This is the case when *GPMC_CONFIG1_i*[11-10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to asynchronous mode. Table 12-234 describes the asynchronous NOR formulas.

Table 12-246. Asynchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – nCS low
B	ns	Delay time – nCS valid to nADV/ALE invalid
C	ns	Delay time – nCS valid to nOE/nRE invalid (single read)
D	ns	Pulse duration – address bus valid - 2nd, 3rd and 4th accesses
E	ns	Delay time – nCS valid to nWE valid
F	ns	Delay time – nCS valid to nWE invalid
G	ns	Address invalid duration between two successive R/W accesses
H	ns	Setup time – read data valid before nOE/nRE high

Table 12-246. Asynchronous NOR Formulas Description (continued)

Configuration Parameter	Unit	Description
I	ns	Delay time – nCS valid to nOE/nRE invalid (burst read)
J	ns	Delay time – address bus valid to nCS valid
		Delay time – data bus valid to nCS valid
		Delay time – nBE0 / nBE1 valid to nCS valid
K	ns	Delay time – nCS valid to nADV/ALE valid
L	ns	Delay time – nCS valid to nOE/nRE valid
M	ns	Delay time – nCS valid to first data latching edge
N	ns	Pulse duration – nBE0 / nBE1 valid time
O	ns	Delay time – nCS valid to nADV/ALE valid

The configuration parameters are calculated through the following formulas. These formulas are not exhaustive. For more information, see the device-specific Datasheet.

- nCS low pulse:
  For single read: A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: A = (CSRDOFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For single write: A = (CSWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst write: A = (CSWROFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
- nCS valid to nADV/ALE invalid delay:
  For reading: B = ((ADVRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
  For writing: B = ((ADVWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- C = ((OEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- D = PAGEBURSTACCESSTIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- E = ((WEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- F = ((WEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- G = CYCLE2CYCLEDELAY * GPMC_FCLK period
- H = ((OEOFFTIME – RDACCESSTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * OEEXTRADELAY) * GPMC_FCLK period
- I = ((OEOFFTIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period, where N = page burst access number
- J = (CSONTIME * (TIMEPARAGRANULARITY + 1) + 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- K = ((ADVONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- L = ((OEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- M = ((RDACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) – 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- nBE0 /nBE1 pulse:
  For single read: N = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

For burst read: N = (RDCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
For burst write: N = (WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number

- O = ((WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period

Figure 12-215 shows a simplified example of an asynchronous NOR single write where formulas are associated with signal waves.

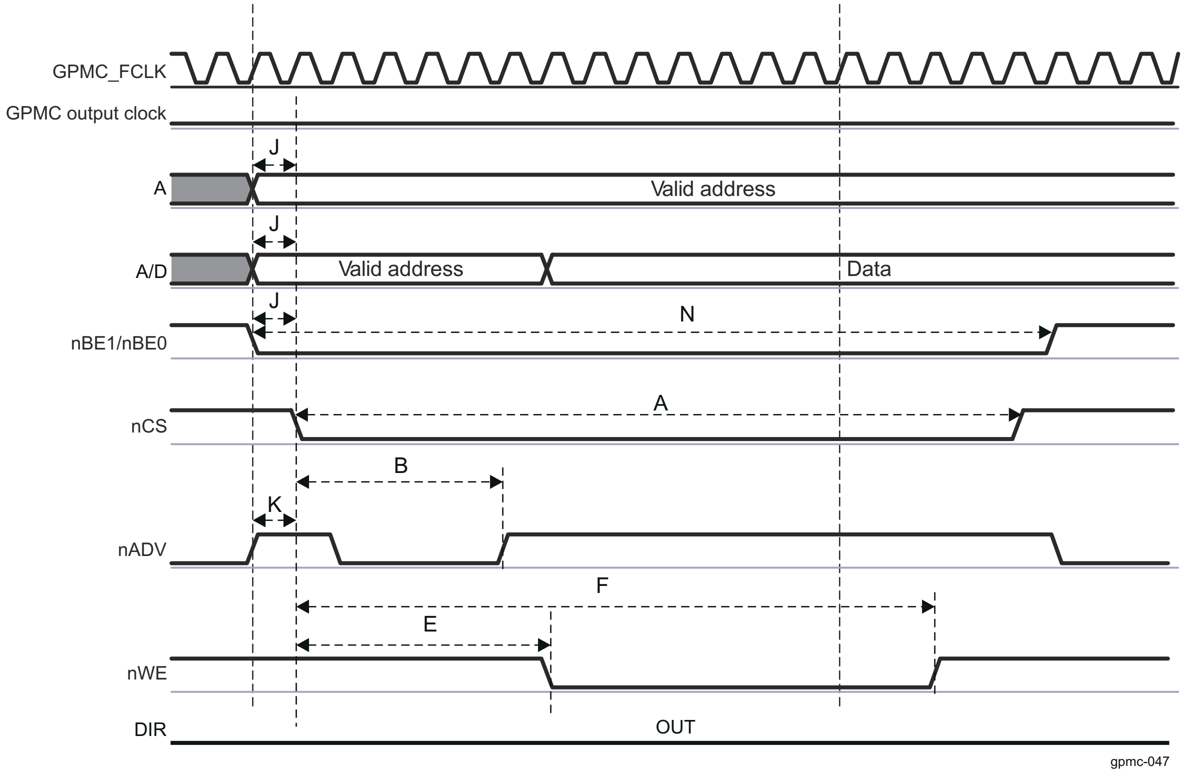

Figure 12-215. Asynchronous NOR Single Write Simplified Example

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Note

Write multiple access is not supported in asynchronous mode. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

12.4.4 Error Location Module (ELM)

This section describes the Error Location Module (ELM) for the device.

12.4.4.1 ELM Overview

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

The maximum acceptable number of errors that can be corrected depends on a programmable configuration parameter. 4-, 8-, and 16-bit error-correction levels are supported. The ELM depends on a static and fixed definition of the generator polynomial for each error-correction level that corresponds to the generator polynomials defined in the GPMC (there are three fixed polynomial for the three correction error levels). A larger number of errors than the programmed error-correction level may be detected, but the ELM cannot correct them all. The offending block is then tagged as *uncorrectable* in the associated computation exit status register. If the computation is successful, that is, if the number of errors detected does not exceed the maximum value authorized for the chosen correction capability, the exit status register contains the information on the number of detected errors.

When the error-location process completes, an interrupt is triggered to inform the software that its status can be checked. The number of detected errors and their locations in the NAND block can be retrieved from the module through register accesses.

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Figure 12-216 shows the ELM0 module overview.

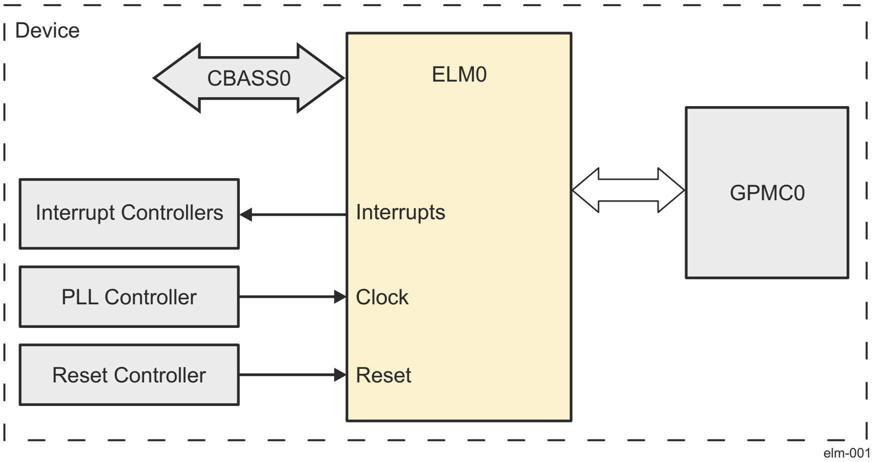

Figure 12-216. ELM0 Overview

12.4.4.1.1 ELM Features

The ELM has the following features:

- 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error-location process completion:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode.

12.4.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.4.4.2 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.4.3 ELM Functional Description

The ELM0 module is hereinafter referred to as ELM.

The ELM is designed around the error-location engine, which handles the computation based on the input syndrome polynomials.

The ELM maps the error-location engine to a standard interconnect interface by using a set of registers to control inputs and outputs.

12.4.4.3.1 ELM Software Reset

To perform a software reset, set the ELM_SYSCONFIG[1] SOFTRESET bit to 1. The ELM_SYSSTS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the ELM_SYSCONFIG[1] SOFTRESET bit is automatically reset.

12.4.4.3.2 ELM Power Management

Note

Some of the ELM features described in this section may not be supported on this family of devices. See the *Module Integration* section for more information about Unsupported Features.

Table 12-235 describes the power-management features available to the ELM.

Table 12-247. Local Power-Management Features

Feature	Registers	Description
Clock autogating	ELM_SYSCONFIG[0] AUTOGATING	This bit allows a local power optimization inside the module by gating the ELM_FICLK clock upon the interface activity.
Idle modes	ELM_SYSCONFIG[4-3] SIDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	ELM_SYSCONFIG[8] CLOCKACTIVITY	The clock can be switched off or maintained.

12.4.4.3.3 ELM Interrupt Requests

Table 12-236 lists the event flags, and their masks, that can cause module interrupts asserting the signal.

Table 12-248. ELM Events

Event Flag	Event Mask	Description
ELM_IRQSTS[8] PAGE_VALID	ELM_IRQEN[8] PAGE_MASK	Page interrupt
ELM_IRQSTS[7] LOC_VALID_7	ELM_IRQEN[7] LOCATION_MASK_7	Error-location interrupt for syndrome polynomial 7
ELM_IRQSTS[6] LOC_VALID_6	ELM_IRQEN[6] LOCATION_MASK_6	Error-location interrupt for syndrome polynomial 6
ELM_IRQSTS[5] LOC_VALID_5	ELM_IRQEN[5] LOCATION_MASK_5	Error-location interrupt for syndrome polynomial 5
ELM_IRQSTS[4] LOC_VALID_4	ELM_IRQEN[4] LOCATION_MASK_4	Error-location interrupt for syndrome polynomial 4
ELM_IRQSTS[3] LOC_VALID_3	ELM_IRQEN[3] LOCATION_MASK_3	Error-location interrupt for syndrome polynomial 3
ELM_IRQSTS[2] LOC_VALID_2	ELM_IRQEN[2] LOCATION_MASK_2	Error-location interrupt for syndrome polynomial 2
ELM_IRQSTS[1] LOC_VALID_1	ELM_IRQEN[1] LOCATION_MASK_1	Error-location interrupt for syndrome polynomial 1
ELM_IRQSTS[0] LOC_VALID_0	ELM_IRQEN[0] LOCATION_MASK_0	Error-location interrupt for syndrome polynomial 0

12.4.4.3.4 ELM Processing Initialization

ELM_LOCATION_CONFIG global setting parameters must be set before using the error-location engine. The ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL bit field defines the error-correction level used (4-, 8-, or 16-bit error correction). The ELM_LOCATION_CONFIG[26-16] ECC_SIZE bit field defines the maximum buffer length beyond which the engine processing no longer looks for errors.

Software can choose to use the ELM in continuous mode or page mode. If all ELM_PAGE_CTRL[i] SECTOR_i bits (i is the syndrome polynomial number, where i = 0 to 7) are reset, continuous mode is used. In any other case, page mode is implicitly selected.

- Continuous mode: Each syndrome polynomial is processed independently. Results for a syndrome can be retrieved and acknowledged at any time, regardless of the status of the other seven processing contexts.
- Page mode: Syndrome polynomials are grouped into atomic entities: only one page can be processed at any given time, even if all eight contexts are not used for this page. Unused contexts are lost and cannot be affected to any other processing. The full page must be acknowledged and cleared before moving to the next page.

For completion interrupts to be generated correctly, all ELM_IRQEN[i] LOCATION_MASK_i bits (where i = 0 to 7) must be forced to 0 when in page mode, and set to 1 in continuous mode. Additionally, the ELM_IRQEN[8] PAGE_MASK bit must be set to 1 when in page mode.

Software initiates error-location processing by writing a syndrome polynomial into one of the eight possible register sets. Each of these register sets includes seven registers: ELM_SYNDROME_FRAGMENT_0_i to ELM_SYNDROME_FRAGMENT_6_i. The first six registers can be written in any order, but ELM_SYNDROME_FRAGMENT_6_i must be written last because it includes the validity bit, which instructs the ELM that this syndrome polynomial must be processed (the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit).

As soon as one validity bit is asserted (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x1, where i = 0 to 7), error-location processing can start for the corresponding syndrome polynomial. The associated ELM_LOCATION_STS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i registers (where i = 0 to 7) are not reset. Software must not consider them until the corresponding ELM_IRQSTS[i] LOC_VALID_i bit is set.

12.4.4.3.5 ELM Processing Sequence

While the error-location engine is busy processing one syndrome polynomial, further syndrome polynomials can be written. They are processed when the current processing completes.

The engine completes early when:

- No error is detected; that is, when the ELM_LOCATION_STS_i[8] ECC_CORRECTABLE bit is set to 1 and the ELM_LOCATION_STS_i[4-0] ECC_NB_ERRORS bit field is set to 0x0.
- Too many errors are detected; that is, when the ELM_LOCATION_STS_i[8] ECC_CORRECTABLE bit is set to 0 while the ELM_LOCATION_STS_i[4-0] ECC_NB_ERRORS bit field is set with the value output by the error-location engine. The reported number of errors is not ensured if ECC_CORRECTABLE is 0.

If the engine completes early, the associated error-location registers ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i (where i = 0 to 7) are not updated.

In all other cases, the engine goes through the entire error-location process. Each time an error location is found, it is logged in the associated ECC_ERROR_LOCATION bit field. The first error detected is logged in the ELM_ERROR_LOCATION_0_i[12-0] ECC_ERROR_LOCATION bit field; the second is logged in the ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION bit field, and so on.

Table 12-237 describes the ELM_LOCATION_STS_i value decoding.

Table 12-249. ELM_LOCATION_STS_i Value Decoding

ECC_CORRECTABLE Value	ECC_NB_ERRORS Value	Status	Number of Errors Detected	Action Required

Table 12-249. ELM_LOCATION_STS_i Value Decoding (continued)

1	0	OK	0	None
1	≠ 0	OK	ECC_NB_ERRORS	Correct the data buffer read based on the ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i results.
0	Any	Failed	Unknown	Software-dependent

12.4.4.3.6 ELM Processing Completion

When the processing for a given syndrome polynomial completes, its ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit is reset. It must not be set again until the exit status registers, ELM_LOCATION_STS_i (where i = 0 to 7) for this processing are checked. Failure to comply with this rule leads to potential loss of the first polynomial process data output.

The error-location engine signals the process completion to the ELM. When this event is detected, the corresponding ELM_IRQSTS[i] LOC_VALID_i bit (where i = 0 to 7) is set. The processing exit status is available from the associated ELM_LOCATION_STS_i register, and error locations are stored in order in the ECC_ERROR_LOCATION bit fields. Software must read only valid error-location registers based on the number of errors detected and located.

Immediately after the error-location engine completes, a new syndrome polynomial can be processed, if any is available, as reported by the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit, depending on the configured error-correction level. If several syndrome polynomials are available, a round-robin arbitration is used to select one for processing.

In continuous mode (that is, all bits in ELM_PAGE_CTRL are reset), an interrupt is triggered whenever a ELM_IRQSTS[i] LOC_VALID_i bit is asserted. Software must read the ELM_IRQSTS register to determine which polynomial is processed and retrieve the exit status and error locations (ELM_LOCATION_STS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i). When done, software must clear the corresponding ELM_IRQSTS[i] LOC_VALID_i bit by setting it to 1. Other status bits must be set to 0 so that other interrupts are not unintentionally cleared. When using this mode, the ELM_IRQSTS[8] PAGE_VALID interrupt is never triggered.

In page mode, the module does not trigger interrupts for the processing completion of each polynomial because the ELM_IRQEN[i] LOCATION_MASK_i bits are cleared. A page is defined using the ELM_PAGE_CTRL register. Each SECTOR_i bit set means the corresponding polynomial i is part of the page processing. A page is fully processed when all tagged polynomials have been processed, as logged in the ELM_IRQSTS[i] LOC_VALID_i bits. The module triggers an ELM_IRQSTS[8] PAGE_VALID interrupt whenever it detects that the full page has been processed. To make sure the next page can be correctly processed, all status bits in the ELM_IRQSTS register must be cleared by using a single atomic-write access.

Note

Do not modify page setting parameters in the ELM_PAGE_CTRL register unless the engine is idle, no polynomial input is valid, and all interrupts have been cleared.

Because no polynomial-level interrupt is triggered in page mode, polynomials cleared in the ELM_PAGE_CTRL[i] SECTOR_i bits (where i = 0 to 7) are processed as usual, but are essentially ignored. Software must manually poll the ELM_IRQSTS bits to check for their status.

12.4.4.4 ELM Basic Programming Model

12.4.4.4.1 ELM Low-Level Programming Model

12.4.4.4.1.1 Processing Initialization

Table 12-250. ELM Processing Initialization

Step	Register/Bit Field/Programming Model	Value
Resets the module.	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTS[0] RESETDONE	0x1
Configure the target interface power management.	ELM_SYSCONFIG[4-3] SIDLEMODE	Set value
Defines the error-correction level used.	ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL	Set value
Defines the maximum buffer length.	ELM_LOCATION_CONFIG[26-16] ECC_SIZE	Set value
Sets the ELM in continuous mode or page mode.	ELM_PAGE_CTRL	Set value
IF continuous mode is used:	All ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x0
Enable interrupt for syndrome polynomial i.	ELM_IRQEN[i] LOCATION_MASK_i	0x1
ELSE (page mode is used):	One syndrome polynomial i is set ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	All ELM_IRQEN[i] LOCATION_MASK_i = 0x0 and ELM_IRQEN[8] PAGE_MASK = 0x1	Set value
ENDIF		Set value
Set the input syndrome polynomial i.	ELM_SYNDROME_FRAGMENT_0_i	Set value
	ELM_SYNDROME_FRAGMENT_1_i	Set value
	ELM_SYNDROME_FRAGMENT_5_i	Set value
	ELM_SYNDROME_FRAGMENT_6_i	Set value
Initiates the computation process.	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID	0x1

12.4.4.4.1.2 Read Results

The engine goes through the entire error-location process and results can be read. Table 12-239 and Table 12-240 describe the processing completion for continuous and page modes, respectively.

Table 12-251. ELM Processing Completion for Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the interrupt is generated, or poll the status register.		
Read for which i the error-location process is complete.	*ELM_IRQSTS*[i] LOC_VALID_i	0x1
IF the process fails (too many errors):	*ELM_LOCATION_STS_i*[8] ECC_CORRECTABLE	0x0
It is software dependant.		
ELSE (process successful, the engine completes):	*ELM_LOCATION_STS_i*[8] ECC_CORRECTABLE	0x1
Read the number of errors.	*ELM_LOCATION_STS_i*[4-0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers. Software must correct errors in the data buffer.	*ELM_ERROR_LOCATION_0_i*[12-0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12-0] ECC_ERROR_LOCATION	
ENDIF		
Clear the corresponding i interrupt.	*ELM_IRQSTS*[i] LOC_VALID_i	0x1

A new syndrome polynomial can be processed after the end of processing (

ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x0) and after the exit status register check (*ELM_LOCATION_STS_i*

Table 12-252. ELM Processing Completion for Page Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the interrupt is generated, or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	*ELM_IRQSTS*[8] PAGE_VALID	0x1
Repeat the following actions the necessary number of times. That is, once for each valid defined block in the page.		
Read the process exit status.	*ELM_LOCATION_STS_i*[8] ECC_CORRECTABLE	
IF the process fails (too many errors):	*ELM_LOCATION_STS_i*[8] ECC_CORRECTABLE	0x0
It is software dependent.		
ELSE (process successful, the engine completes):	*ELM_LOCATION_STS_i*[8] ECC_CORRECTABLE	0x1
Read the number of errors.	*ELM_LOCATION_STS_i*[4-0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers.	*ELM_ERROR_LOCATION_0_i*[12-0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12-0] ECC_ERROR_LOCATION	
ENDIF		
End Repeat		
Clear the *ELM_IRQSTS* register.	*ELM_IRQSTS*	0x1FF

12.4.4.4.1.3

Next page can be correctly processed after a page is fully processed, when all tagged polynomials have been processed (*ELM_IRQSTS*[i] LOC_VALID_i = 0x1 for all syndrome polynomials i used in the page).

12.4.4.4.2 Use Case: ELM Used in Continuous Mode

In this example, the ELM is programmed for an 8-bit error-correction capability in continuous mode (see Table 12-241). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, a nonzero polynomial syndrome is reported from the GPMC (polynomial syndrome 0 is used in the ELM):

- P = 0x0A16ABE115E44F767BFB0D0980.

Table 12-253. Use Case: Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Reset the module.	*ELM_SYSCONFIG*[1] SOFTRESET	0x1
Wait until reset is done.	*ELM_SYSSTS*[0] RESETDONE	0x1
Configure the target interface power management: Smart idle is used.	*ELM_SYSCONFIG*[4-3] SIDLEMODE	0x2
Define the error-correction level used: 8 bits.	*ELM_LOCATION_CONFIG*[1-0] ECC_BCH_LEVEL	0x1
Define the maximum buffer length: 528 bytes (2 × 528 = 1056).	*ELM_LOCATION_CONFIG*[26-16] ECC_SIZE	0x420
Set the ELM in continuous mode.	*ELM_PAGE_CTRL*	0
Enable interrupt for syndrome polynomial 0.	*ELM_IRQEN*[0] LOCATION_MASK_0	0x1
Set the input syndrome polynomial 0.	*ELM_SYNDROME_FRAGMENT_0_i* (where i = 0)	0xFB0D0980
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xE44F767B
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x16ABE115
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0x0000000A

Table 12-253. Use Case: Continuous Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Initiate the computation process.	*ELM_SYNDROME_FRAGMENT_6_i*[16] SYNDROME_VALID (where i = 0)	0x1
Wait until process is complete for syndrome polynomial 0: is generated or poll the status register.		
Read that error-location process is complete for syndrome polynomial 0.	*ELM_IRQSTS*[0] LOC_VALID_0	0x1
Read the process exit status: All errors were successfully located.	*ELM_LOCATION_STS*[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the number of errors: Four errors detected.	*ELM_LOCATION_STS*[4-0] ECC_NB_ERRORS (where i = 0)	0x4
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers: Errors are located in the data buffer at decimal addresses 431, 1062, 1909, 3452.	*ELM_ERROR_LOCATION_0_i* (where i = 0)	0x1AF
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x426
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x775
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xD7C
Clear the corresponding interrupt for polynomial 0.	*ELM_IRQSTS*[0] LOC_VALID_0	0x1

The NAND flash data in the sector are seen as a polynomial of degree 4223 (number of bits in a 528 byte buffer minus 1), with each data bit being a coefficient in the polynomial. When reading from a NAND flash using the GPMC module, computation of the polynomial syndrome assumes that the first NAND word read at address 0x0 contains the highest-order coefficient in the message. Furthermore, in the 16-bit NAND word, bits are ordered from bit 7 to bit 0, and then from bit 15 to bit 8. Based on this convention, an address table of the data buffer can be built. NAND memory addresses in Table 12-242 are given in decimal format.

Table 12-254. 16-Bit NAND Sector Buffer Address Map

NAND Memory Address	Message Bit Addresses in Memory Word															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4215	4214	4213	4212	4211	4210	4209	4208	4223	4222	4221	4220	4219	4218	4217	4216
1	4175	4174	4173	4172	4171	4170	4169	4168	4183	4182	4181	4180	4179	4178	4177	4176
...																
47	3463	3462	3461	3460	3459	3458	3457	3456	3471	3470	3469	3468	3467	3466	3465	3464
48	3447	3446	3445	3444	3443	3442	3441	3440	3455	3454	3453	3452	3451	3450	3449	3448
49	3431	3430	3429	3428	3427	3426	3425	3424	3439	3438	3437	3436	3435	3434	3433	3432
50	3415	3414	3413	3412	3411	3410	3409	3408	3423	3422	3421	3420	3419	3418	3417	3416
...																
255	135	134	133	132	131	130	129	128	143	142	141	140	139	138	137	136
256	119	118	117	116	115	114	113	112	127	126	125	124	123	122	121	120
257	103	102	101	100	99	98	97	96	111	110	109	108	107	106	105	104
258	87	86	85	84	83	82	81	80	95	94	93	92	91	90	89	88
259	71	70	69	68	67	66	65	64	79	78	77	76	75	74	73	72
260	55	54	53	52	51	50	49	48	63	62	61	60	59	58	57	56
261	39	38	37	36	35	34	33	32	47	46	45	44	43	42	41	40
262	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24
263	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

The table can now be used to determine which bits in the buffer were incorrect and must be flipped. In this example, the first bit to be flipped is bit 4 from the 49th byte read from memory. It is up to the processor to correctly map this word to the copied buffer and flip this bit. The same process must be repeated for all detected errors.

12.4.4.4.3 Use Case: ELM Used in Page Mode

In this example, the ELM module is programmed for a 16-bit error-correction capability in page mode (see Table 12-243). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, four non-zero polynomial syndromes are reported from the GPMC (polynomial syndrome 0, 1, 2, and 3 are used in the ELM):

- P0 = 0xE8B0 12ADDB5A318E05BE B0693DB28330B5CC A329AA05E0B718EF
- P1 = 0xBAD0 49A0D932C22E6669 0948DF08BE093336 79C6BA10E5F935EB
- P2 = 0x69D9 B86ABCD5EC3697FA A6498FEE54556EA0 1579EF7D60BA3189
- P3 = 0x0

Table 12-255. Use Case: Page Mode

Step	Register/Bit Field/Programming Model	Value
Reset the module	*ELM_SYSCONFIG*[1] SOFTRESET	0x1
Wait until reset is done.	*ELM_SYSCONFIG*[0] RESETDONE	0x1
Configure the target interface power management: Smart idle is used.	*ELM_SYSCONFIG*[4-3] SIDLEMODE	0x2
Define the error-correction level used: 16 bits	*ELM_LOCATION_CONFIG*[1-0] ECC_BCH_LEVEL	0x2
Define the maximum buffer length: 528 bytes	*ELM_LOCATION_CONFIG*[26-16] ECC_SIZE	0x420
Set the ELM in page mode (four blocks in a page)	*ELM_PAGE_CTRL*[0] SECTOR_0	0x1
	ELM_PAGE_CTRL[1] SECTOR_1	0x1
	ELM_PAGE_CTRL[2] SECTOR_2	0x1
	ELM_PAGE_CTRL[3] SECTOR_3	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	*ELM_IRQEN*	0x100
Set the input syndrome polynomial 0.	*ELM_SYNDROME_FRAGMENT_0_i* (where i = 0)	0xE0B718EF
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xA329AA05
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x8330B5CC
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0xB0693DB2
	ELM_SYNDROME_FRAGMENT_4_i (where i = 0)	0x318E05BE
	ELM_SYNDROME_FRAGMENT_5_i (where i = 0)	0x12ADDB5A
	ELM_SYNDROME_FRAGMENT_6_i (where i = 0)	0xE8B0
Set the input syndrome polynomial 1.	*ELM_SYNDROME_FRAGMENT_0_i* (where i = 1)	0xE5F935EB
	ELM_SYNDROME_FRAGMENT_1_i (where i = 1)	0x79C6BA10
	ELM_SYNDROME_FRAGMENT_2_i ((where i = 1)	0xBE093336
	ELM_SYNDROME_FRAGMENT_3_i (where i = 1)	0x0948DF08
	ELM_SYNDROME_FRAGMENT_4_i (where i = 1)	0xC22E6669
	ELM_SYNDROME_FRAGMENT_5_i (where i = 1)	0x49A0D932
	ELM_SYNDROME_FRAGMENT_6_i (where i = 1)	0xBAD0
Set the input syndrome polynomial 2.	*ELM_SYNDROME_FRAGMENT_0_i* (where i = 2)	0x60BA3189
	ELM_SYNDROME_FRAGMENT_1_i (where i = 2)	0x1579EF7D
	ELM_SYNDROME_FRAGMENT_2_i (where i = 2)	0x54556EA0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 2)	0xA6498FEE
	ELM_SYNDROME_FRAGMENT_4_i (where i = 2)	0xEC3697FA
	ELM_SYNDROME_FRAGMENT_5_i (where i = 2)	0xB86ABCD5
	ELM_SYNDROME_FRAGMENT_6_i (where i = 2)	0x69D9
Set the input syndrome polynomial 3.	*ELM_SYNDROME_FRAGMENT_0_i* (where i = 3)	0x0

Table 12-255. Use Case: Page Mode (continued)

Step	Register/Bit Field/Programming Model	Value
	ELM_SYNDROME_FRAGMENT_1_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_2_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_4_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_5_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_6_i (where i = 3)	0x0
Initiate the computation process for syndrome polynomial 0	*ELM_SYNDROME_FRAGMENT_6_i*[16] SYNDROME_VALID (where i = 0)	0x1
Initiate the computation process for syndrome polynomial 1	*ELM_SYNDROME_FRAGMENT_6_i*[16] SYNDROME_VALID (where i = 1)	0x1
Initiate the computation process for syndrome polynomial 2	*ELM_SYNDROME_FRAGMENT_6_i*[16] SYNDROME_VALID (where i = 2)	0x1
Initiate the computation process for syndrome polynomial 3	*ELM_SYNDROME_FRAGMENT_6_i*[16] SYNDROME_VALID (where i = 3)	0x1
Wait until process is complete for syndrome polynomial 0, 1, 2, and 3: Wait until the interrupt is generated or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	*ELM_IRQSTS*[8] PAGE_VALID	0x1
Read the process exit status for syndrome polynomial 0: All errors were successfully located.	*ELM_LOCATION_STS*[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the process exit status for syndrome polynomial 1: All errors were successfully located.	*ELM_LOCATION_STS*[8] ECC_CORRECTABLE (where i = 1)	0x1
Read the process exit status for syndrome polynomial 2: All errors were successfully located.	*ELM_LOCATION_STS*[8] ECC_CORRECTABLE (where i = 2)	0x1
Read the process exit status for syndrome polynomial 3: All errors were successfully located.	*ELM_LOCATION_STS*[8] ECC_CORRECTABLE (where i = 3)	0x1
Read the number of errors for syndrome polynomial 0: four errors detected.	*ELM_LOCATION_STS*[4-0] ECC_NB_ERRORS (where i = 0)	0x4
Read the number of errors for syndrome polynomial 1: two errors detected.	*ELM_LOCATION_STS*[4-0] ECC_NB_ERRORS (where i = 1)	0x2
Read the number of errors for syndrome polynomial 2: one error detected.	*ELM_LOCATION_STS*[4-0] ECC_NB_ERRORS (where i = 2)	0x1
Read the number of errors for syndrome polynomial 3: no errors detected.	*ELM_LOCATION_STS*[4-0] ECC_NB_ERRORS (where i = 3)	0x0
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers:	*ELM_ERROR_LOCATION_0_i* (where i = 0)	0x1FE
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x617
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x650
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xA83
Read the error-location bit addresses for syndrome polynomial 1 of the first two registers:	*ELM_ERROR_LOCATION_0_i* (where i = 1)	0x4
	ELM_ERROR_LOCATION_1_i (where i = 1)	0x1036
Read the errors location bit addresses for syndrome polynomial 2 of the first registers:	*ELM_ERROR_LOCATION_0_i* (where i = 1)	0x3E8
Clear the *ELM_IRQSTS* register.	*ELM_IRQSTS*	0x1FF

12.4.5 Multi-Media Card Secure Digital (MMCSD) Interface

This section describes the MMCSD modules in the device.

12.4.5.1 MMCSD Overview

This device contains one or more MMCSD module instances. Each MMCSD instance includes one MMCSD Host Controller.

An instance supports either an 8-bit or 4-bit wide data bus.

A host controller can support eMMC and/or SD/SDIO. See the device specific datasheet for interfaces supported by the controller.

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded Multi-Media Card), SD 4.10 (Secure Digital), and SDIO 3.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

The MMCSD Host Controller provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method. In programmed IO method, the device CPU transfers data using the Buffer Data Port register (MMCSDi_DATA_PORT). In DMA data transfer method, the MMCSD Host Controller can read or write memory without device CPU intervention.

Figure 12-217 shows the MMCSDi module overview (where i represents a valid instance of MMCSD in a domain. Consult the device specific datasheet for available domains and instances).

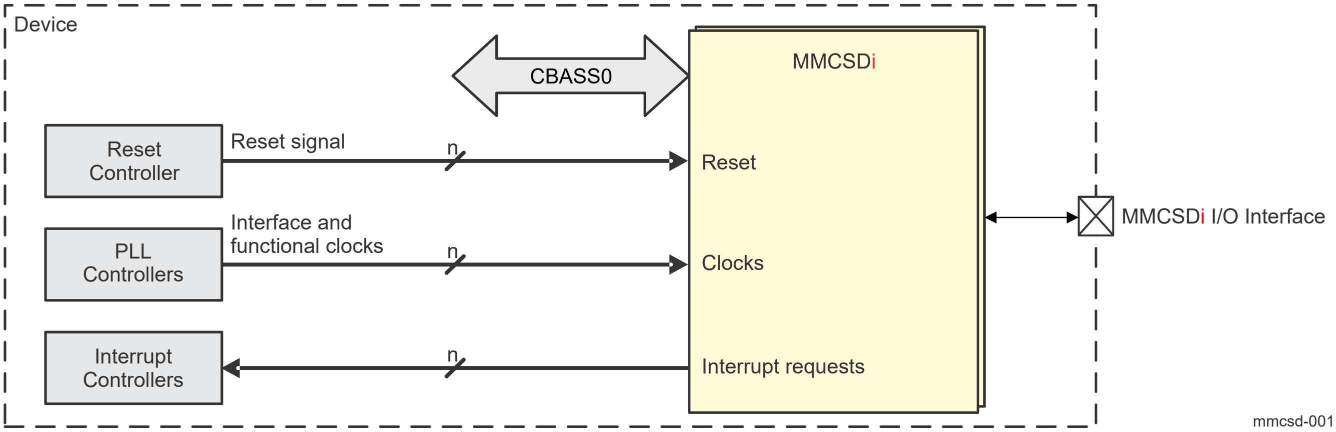

Note

i represents a valid instance of MMCSD in a domain.

Figure 12-217. MMCSDi Module Overview

12.4.5.1.1 MMCSD Features

Table 12-256. MMCSD Features

Feature		MMCSD0 (8-bit)	MMCSD1/2 (4-bit)
Muxing of other LVCMOS interfaces onto the MMCSD interface at the SoC level (See the device specific data sheet for supported interfaces, if applicable)		✓	✓
Controller			
Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3 (for more information about ADMA support, see Section 12.4.5.4.4 , *Advanced DMA*)		✓	✓
System Bus Interface			
64-bit data width (host interface)		✓	✓
64-bit address		✓	✓
Clock asynchronous to eMMC/SD clock (MMCi_CLK)		✓	✓
Little endian only		✓	✓
Configuration Bus Interface			
32-bit data width (target interface)		✓	✓
Linear incrementing addressing mode		✓	✓
32-bit aligned accesses only		✓	✓
Little endian only		✓	✓
Multi-Media Card Support			
eMMC Electrical Standard 5.1 (JESD84-B51)		✓	✓
Backward compatible with earlier eMMC standards		✓	✓
Legacy MMC SDR	8-bit bus width, 0-25 MHz, 25 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-25 MHz, 12.5 MBps		3.3/1.8v
	1-bit bus width, 0-25 MHz, 3.125 MBps		
High Speed SDR	8-bit bus width, 0-50 MHz, 50 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-50 MHz, 25 MBps		3.3/1.8v
	1-bit bus width, 0-50 MHz, 6.25 MBps		
High Speed DDR	8-bit bus width, 0-50 MHz, 100 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-50 MHz, 50 MBps		3.3/1.8v
HS200 SDR	0-200 MHz, 8-bit bus width, 200 MBps	1.8v	N/A
	0-200 MHz, 4-bit bus width, 100 MBps		1.8v
Secure Digital Card Support			
SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01		✓	✓
SDIO Specification v3.00		✓	✓
Backward compatible with earlier SD card specifications		✓	✓
Default Speed mode	3.3 V signaling, frequency up to 25 MHz, up to 12.5 MBps	✓	✓
High Speed mode	3.3 V signaling, frequency up to 50 MHz, up to 25 MBps	✓	✓
SDR12	UHS-I 1.8 V signaling, frequency up to 25 MHz, up to 12.5 MBps	✓	✓
SDR25	UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 25 MBps	✓	✓
SDR50	UHS-I 1.8 V signaling, frequency up to 100 MHz, up to 50 MBps		✓
DDR50	UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 50 MBps		✓
SDR104	UHS-I 1.8 V signaling, frequency up to 200 MHz, up to 100 MBps		✓

12.4.5.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.4.5.2 MMCSD Environment

The MMCSD instance is hereinafter referred to as MMCSDi module.

This section describes the MMCSDi external connections (environment).

The MMCSD (see the device specific datasheet for supported instances) can be used for connection to 1, 4, or 8-bit devices (dedicated for connection to eMMC devices). The MMCSD (see the device specific datasheet for supported instances) can be used for connection to 1 or 4-bit devices (dedicated for connection to SD or SDIO devices). For each MMCSD an integrated UHS-I PHY provides interface to external device.

Figure 12-218 shows the MMCSDi (where i represents a valid instance of MMCSD in a domain. See the device specific datasheet for available domains and MMCSD instances) connected to MMC, SD, or SDIO device.

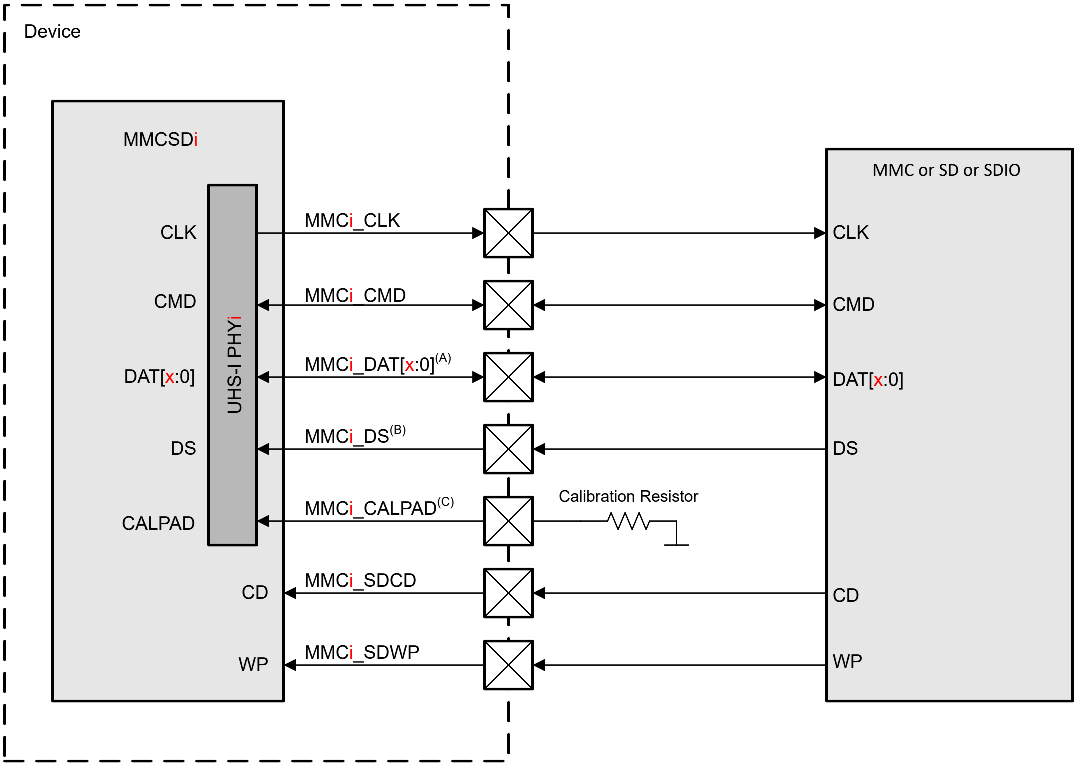

Note

x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

Note

Used for HS400 mode (See the device specific datasheet for valid instances)

Note

Used for PHY Calibration Resistor (See the device specific datasheet for valid instances)

Figure 12-218. MMCSDi Connected to MMC, SD, or SDIO Device

Table 12-245 describes the MMCSDi I/O signals.

Table 12-257. MMCSDi I/O Signals

Module Pin(4)	Device Level Signal	I/O(1)	Description
		MMCSDi(3)	
CLK	MMCi(3)_CLK	O	External Clock
CMD	MMCi(3)_CMD	I/O	Command Line
DAT[x:0](5)	MMCi(3)_DAT[x:0]	I/O	Data Signals
DS	MMCi(3)_DS	I	Data Strobe
CALPAD	MMCi(3)_CALPAD(2)	A	PHY Calibration Resistor
WP	MMCi(3)_SDWP	I	SD Card Write Protect
CD	MMCi(3)_SDCD	I	SD Card Detect

(1) I = Input; O = Output; HiZ = High Impedance; A = Analog
(2) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(3) i represents an MMC instance. See the device datasheet for available domains and MMC instances.
(4) Some pins may not be pinned out or relevant to this device. See the device datasheet for specifics.
(5) x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), refer to the device-specific Datasheet.

12.4.5.2.1 MMCSD IO Multiplexer

Figure 12-219 describes the IOMUX_ENABLE multilplexer, which is controlled by the MMC_SSCFG_PHY_CTRL_1_REG[31] IOMUX_ENABLE bit.

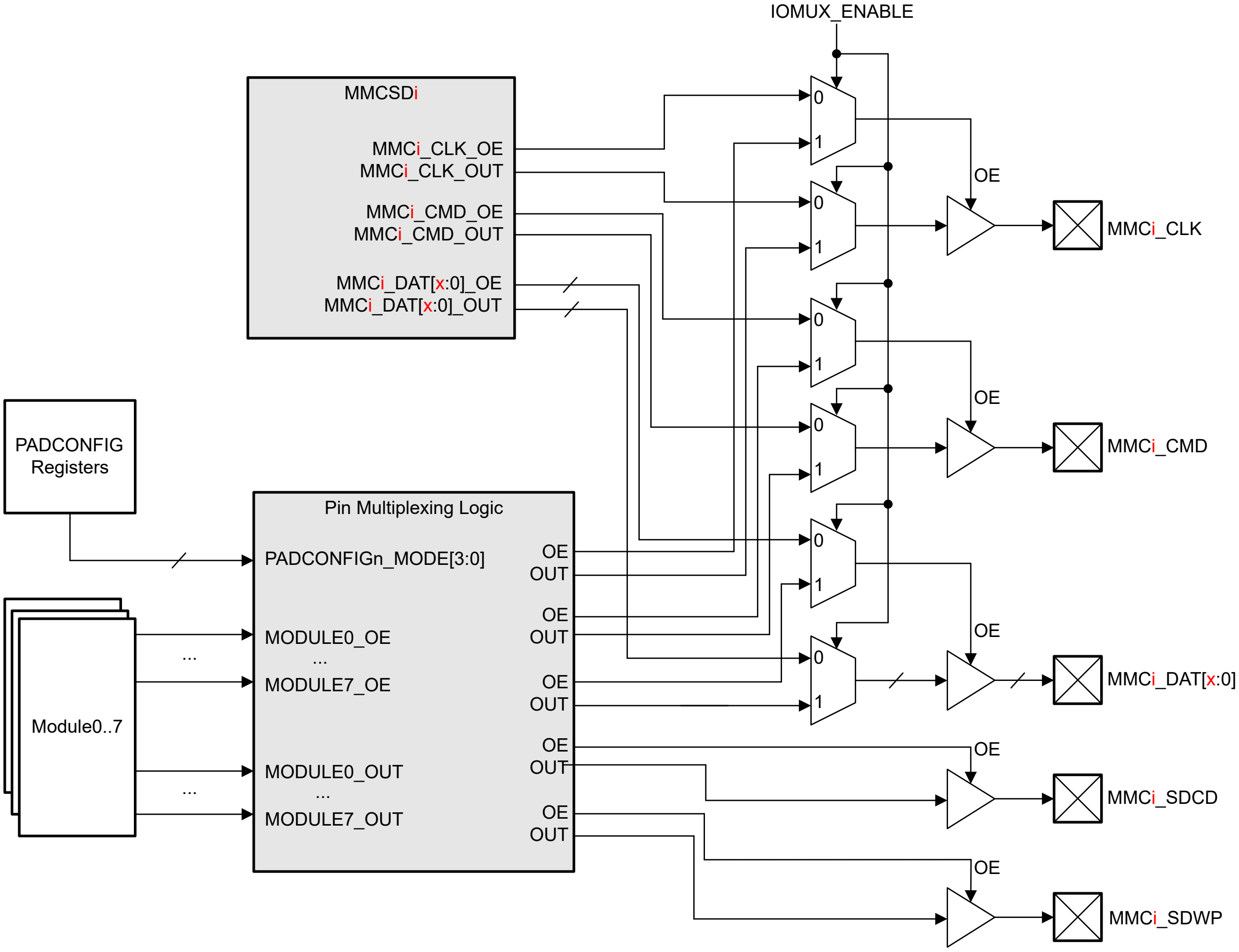

Note

i represents a valid instance of MMCSD. See the device data sheet for specifics.

Note

x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

Note

Only MMCi_CLK, MMCi_CMD and MMCi_DAT[n:0] are routed through the IOMUX_ENABLE multiplexer. MMCi_SDCD and MMCi_SDWP are not routed through the IOMUX_ENABLE multiplexer.

Note

The IOMUX_ENABLE multiplexer does not affect the signal functions selected from the respective PADCONFIG register for the MMCi_SDCD or MMCi_SDWP pins.

Figure 12-219. MMCSD IOMUX_ENABLE Multiplexer

12.4.5.2.2 Protocol and Data Format

The bus protocol between the MMCSD Host Controller and the card is message-based. Each message is represented by one of the following parts:

- Command: A command starts an operation. The command is transferred serially from the MMCSD Host Controller to the card on the CMD line.
- Response: A response is an answer to a command. The response is sent from the card to the MMCSD Host Controller. It is transferred serially on the CMD line.
- Data: Data are transferred from the MMCSD Host Controller to the card or from the card to the MMCSD Host Controller using the data lines.
- Busy: The DAT[0] signal is maintained low by the card as far as it is programming the data received.
- CRC status: The CRC result is sent by the card through the DAT[0] line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on DAT[0]. In the case of successful transmission, over all active data lines, the card sends a positive CRC status on DAT[0] and starts the data programming procedure.

12.4.5.2.2.1 Protocol

There are two types of data transfer:

- Sequential operation
- Block-oriented operation

There are specific commands for each type of operation (sequential or block-oriented).

For information about commands and programming sequences supported by the MMC, SD, and SDIO devices, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

Figure 12-220 and Figure 12-221 show how sequential operations are defined. Sequential operation is only for 1-bit transfer and initiates a continuous data stream. The transfer terminates when a stop command follows on the CMD line.

Note

Stream commands are supported only by MMCs.

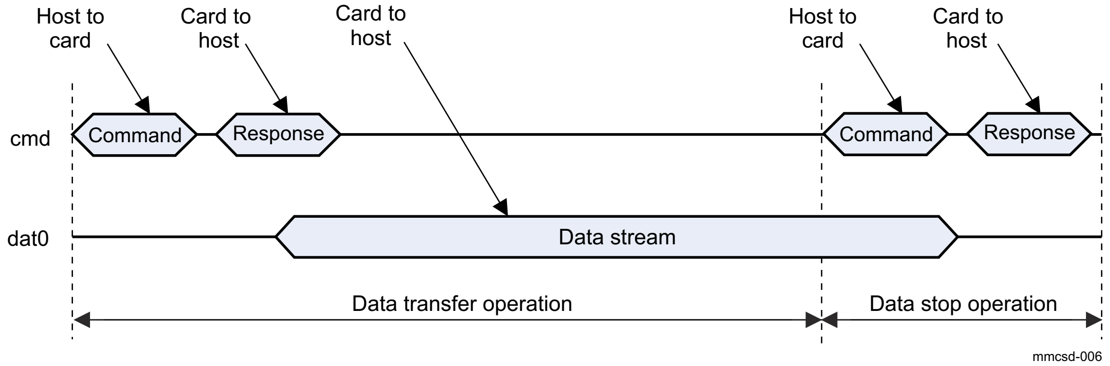

Figure 12-220. Sequential Read Operation (MMCs Only)

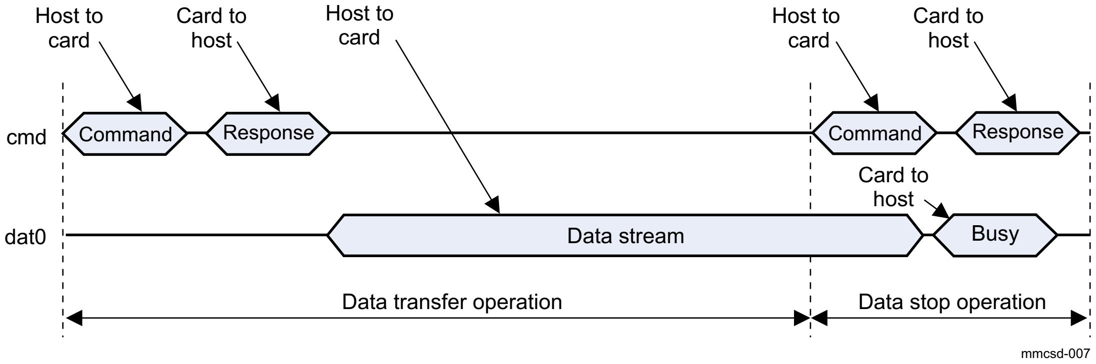

Figure 12-221. Sequential Write Operation (MMCs Only)

Figure 12-222 and Figure 12-223 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the CMD line. These operations are available for all kinds of devices (MMC, SD, SDIO).

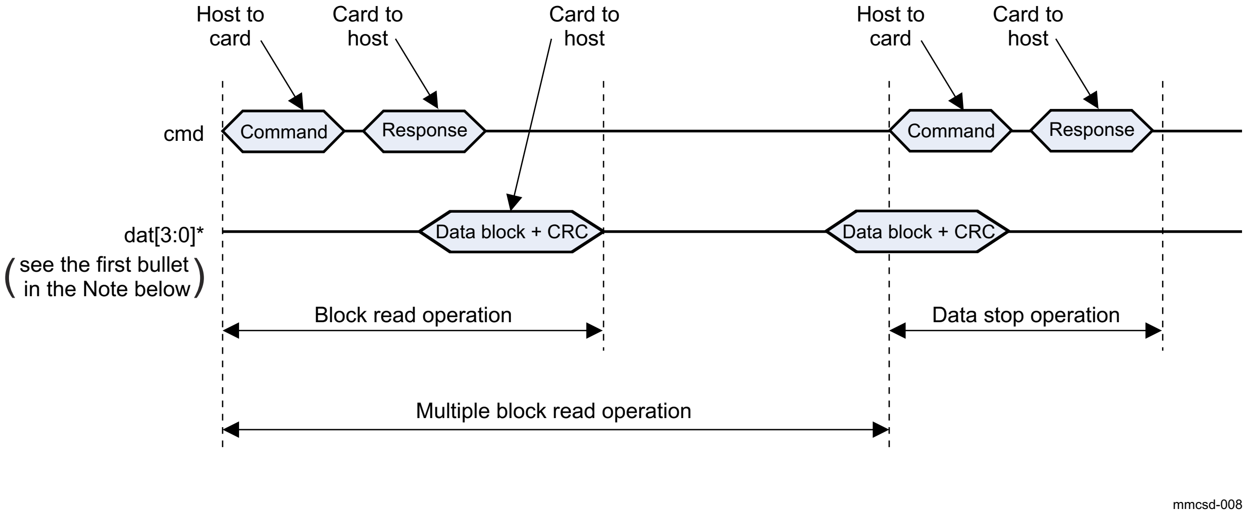

Figure 12-222. Multiple Block Read Operation

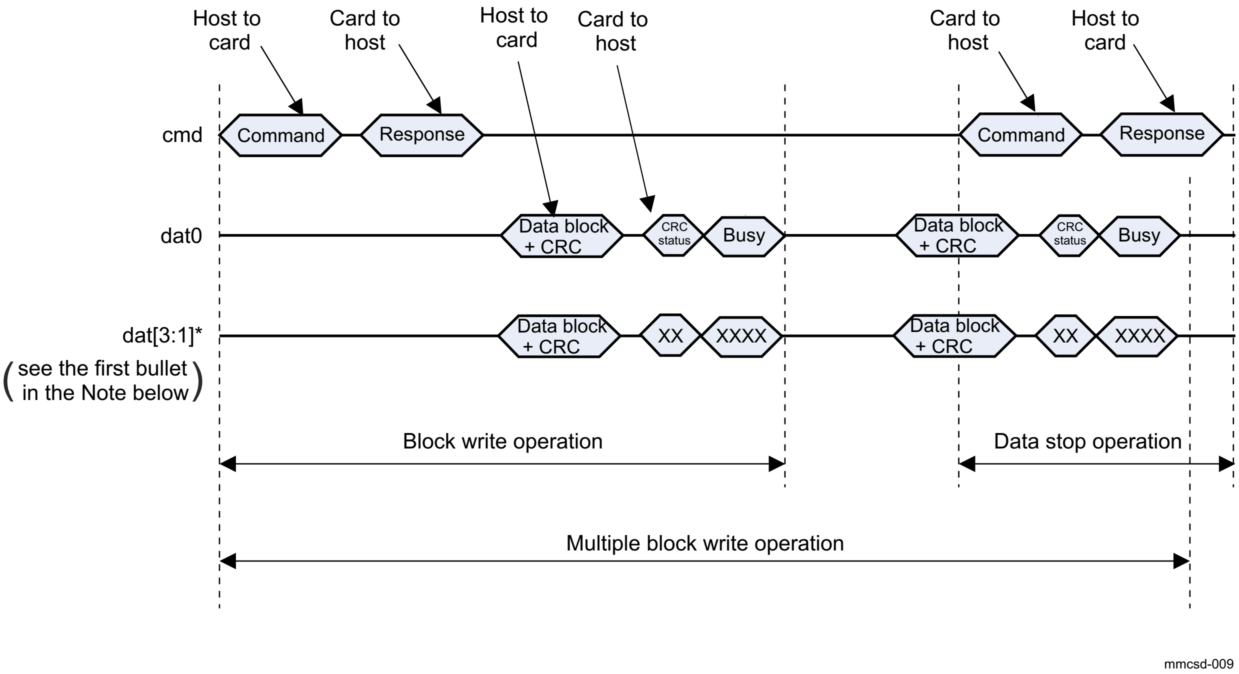

Figure 12-223. Multiple Block Write Operation With Card Busy Signal

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Note

- The card busy signal is not always generated by the card. Refer to Figure 12-222 and Figure 12-223, that show a particular case.
- Software must perform a software reset (see MMCSD0_SOFTWARE_RESET / MMCSD1_SOFTWARE_RESET register) after a data time-out to ensure that MMCi_CLK is stopped.
- For multiblock transfer, and especially for MMC devices, a transfer can be aborted without using a stop command. If a CMD23 is used before data transfer to define the number of blocks that will be transferred, then the transfer stops automatically after the last block (if the MMCs supports this feature).

12.4.5.2.2.2 Data Format

12.4.5.2.2.2.1 Coding Scheme for Command Token

Command tokens always start with 0 and end with 1. The second bit is a transmitter bit: 1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 12-224).

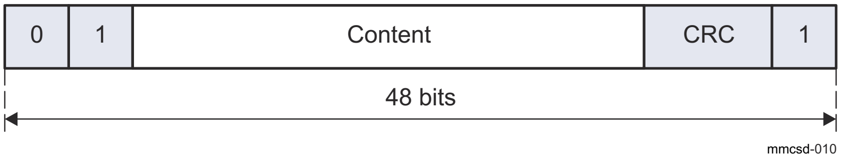

Figure 12-224. Command Token Format

12.4.5.2.2.2.2 Coding Scheme for Response Token

Response tokens always start with 0 and end with 1. The second bit is a transmitter bit: 0 for a card response. The content is different for each type of response (R1, R2, R3, R4, and R5, R6, R7 [for SD]) and the content is protected by 7-bit CRC checksum (see Figure 12-225 and Figure 12-226). Depending on the type of commands sent to the card, the MMCSD0_COMMAND / MMCSD1_COMMAND register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 12-246). For more information about response types, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

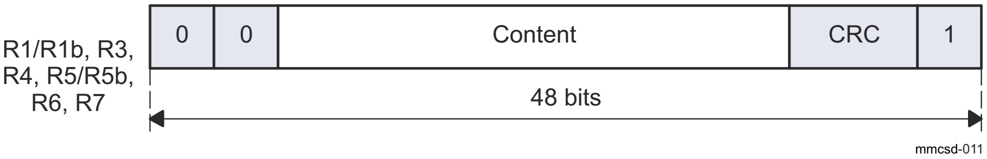

Figure 12-225. Response Token Format (R1/R1b, R3, R4, R5/R5b, R6, R7)

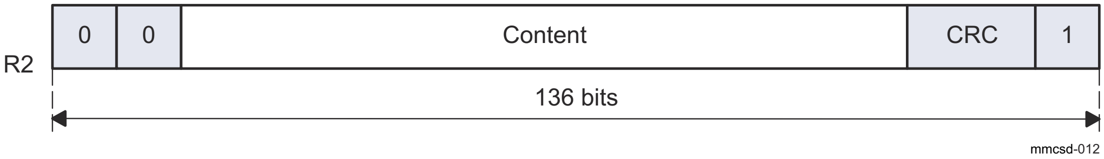

Figure 12-226. Response Token Format (R2)

Table 12-258. Relationship Between Configuration and Name of Response Type

Response Type MMCSD0_COMMAND[1-0] RESP_TYPE_SEL / MMCSD1_COMMAND[1-0] RESP_TYPE_SEL	Index Check Enable MMCSD0_COMMAND[4] CMD_INDEX_CHK_ENA / MMCSD1_COMMAND[4] CMD_INDEX_CHK_ENA	CRC Check Enable MMCSD0_COMMAND[3] CMD_CRC_CHK_ENA / MMCSD1_COMMAND[3] CMD_CRC_CHK_ENA	Name of Response Type
00	0	0	No response
01	0	1	R2
10	0	0	R3 (R4 for SD cards)
10	1	1	R1, R6, R5, (R7 for SD cards)
11	1	1	R1b, R5b

12.4.5.2.2.2.3 Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 12-227 through Figure 12-229).

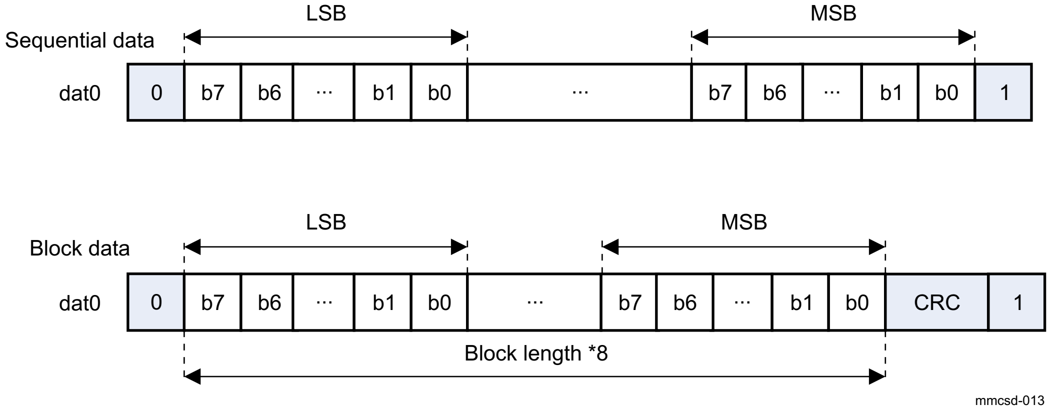

Figure 12-227. Data Token Format for 1-Bit Transfers

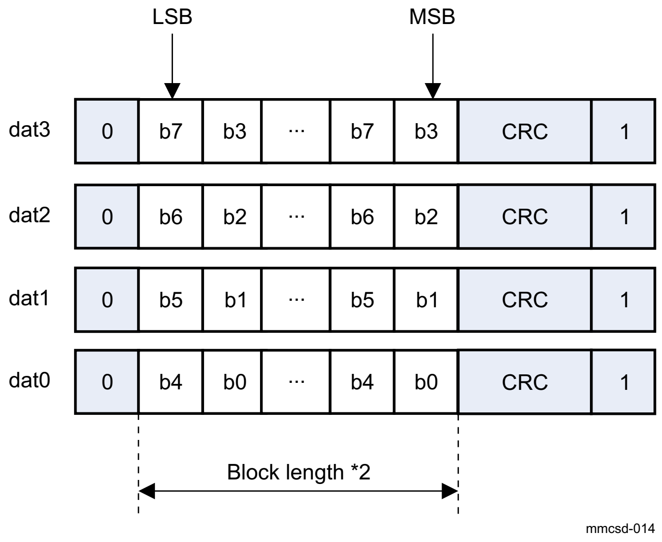

Figure 12-228. Data Token Format for 4-Bit Transfers

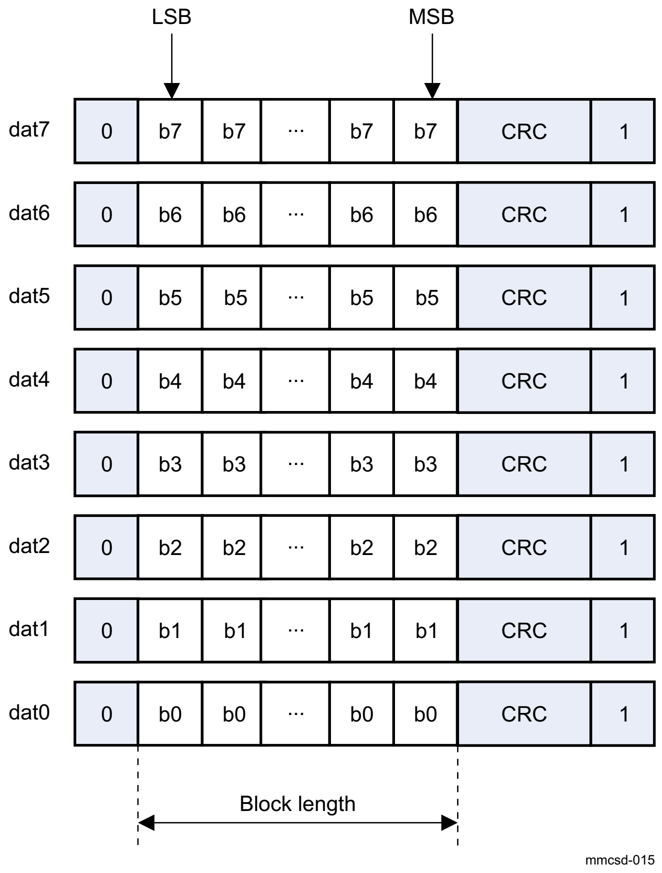

Figure 12-229. Data Token Format for 8-Bit Transfers

12.4.5.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.5.4 MMCSD Functional Description

12.4.5.4.1 Block Diagram

Figure 12-230 shows the MMCSDi module block diagram (where i represents a valid instance of MMCSD in a domain).

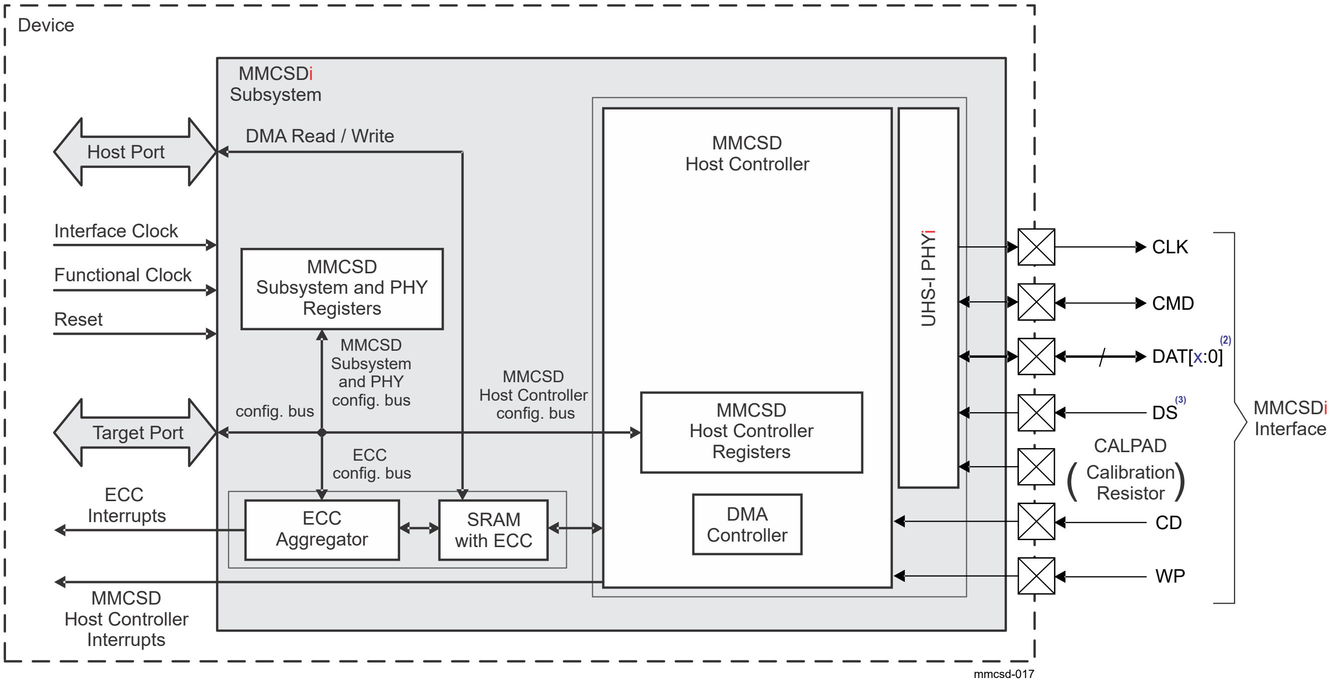

Note

(1) i represents a valid instance of MMCSD in a domain. Consult the device specific datasheet for available domains and MMCSD instances.

Note

(2) x = the maximum number of available DAT signals for an instance of MMCSD in a domain.

Note

(3) Used for HS200 mode (Consult the datasheet for supported devices).

Figure 12-230. MMCSDi Module Block Diagram

Basic Blocks:

- MMCSD Host Controller: The MMCSD Host Controller is situated in the MMCSD Subsystem and provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method.
- UHS-I PHY: The integrated UHS-I PHY provides an interface between the MMCSD Host Controller and external MMC/SD/SDIO devices.
- MMCSDi Interface: The MMCSDi Interface includes all used interface pins (for more information, see Table 12-245).
- Host Port: Provides a 64-bit wide read/write interface between the device and the MMCSD Subsystem internal SRAM.
- Target Port: Provides a 32-bit wide interface between the device and the MMCSD Subsystem and MMCSD Host Controller parts.
- MMCSD Host Controller Registers: This block includes set of all MMCSD Host Controller registers.

- MMCSD Subsystem and PHY Registers: This block implements memory-mapped registers at the MMCSD Subsystem level and memory-mapped registers to control and program the MMCSD PHY.
- ECC Aggregator: The ECC Aggregator block facilitates aggregating and reporting internal SRAM ECC errors (for more information, see *ECC Support*).
- Internal SRAM with ECC: The internal SRAM block is used for data storage during read/write transactions.
- DMA Controller: Manages the data transfer between the device memory and the MMCSD Subsystem internal SRAM.
- System Clocks: There are asynchronous relationship between the interface (system) clock and functional clock (for more information, see *MMCSD Clocks*).
- System Reset: The reset to the MMCSD Subsystem provides reset to the all MMCSD Subsystem parts (for more information, see *MMCSD Clocks*).
- Interrupts: The MMCSD Subsystem sources one MMCSD Host Controller interrupt and four ECC Aggregator interrupts (for more information, see *MMCSD Hardware Requests* and *Interrupt Requests*).

For more information about all MMCSD registers, see *MMCSD Registers*.

The MMCSD Host Controller can use a Programmed IO method (PIO) or DMA data transfer method to access external MMC/SD/SDIO devices.

The target port is used for device CPU access to the MMCSD Host Controller register set. The MMCSD Host Controller register set provides the communication between the device CPU and the MMCSD Host Controller. In PIO method the device CPU transfers data using the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the target port, the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register in the MMCSD Host Controller, and the PHY.

The host port is used for connection to the DMA controller (for more information about ADMA support, see *Advanced DMA* and MMCSD0_CAPABILITIES / MMCSD1_CAPABILITIES register). In DMA data transfer method the DMA controller uses the host port to transfer data between the device memory and the MMCSD Subsystem internal SRAM. The other side of the internal SRAM is connected to the MMCSD Host Controller. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the host port, internal SRAM, MMCSD Host Controller, and the PHY. The DMA controller manages the read/write operations from/to the internal SRAM without device CPU intervention.

12.4.5.4.2 Interrupt Requests

Each MMCSD instance sources one active high level MMCSD Host Controller interrupt and four active high level ECC Aggregator interrupts (see *Module Integration*). The MMCSD Host Controller interrupt is generated based on the bit values in the MMCSD0_NORMAL_INTR_STS / MMCSD1_NORMAL_INTR_STS and MMCSD0_NORMAL_INTR_STS_ENA / MMCSD1_NORMAL_INTR_STS_ENA registers. The ECC Aggregator interrupts are generated based on the ECC errors - single and double bit errors (for more information about ECC Aggregator interrupts, see *ECC Support*).

12.4.5.4.3 ECC Support

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED).

There are two SRAM memories (transmit SRAM and receive SRAM) within each MMCSD instance. These two memories are ECC protected.

The SEC logic detects and corrects a single bit error (single bit error per ECC word or per ECC data segment). The DED logic only detects (does not correct) double errors (double bit errors per ECC word or per ECC data segment).

12.4.5.4.3.1 ECC Aggregator

There are two SRAMs (each with size 4 KB - 512 words × 64-bit) in each MMCSD Subsystem. One SRAM dedicated for transmit and one SRAM dedicated for receive operations.

Figure 12-231 shows the ECC Aggregator block diagram.

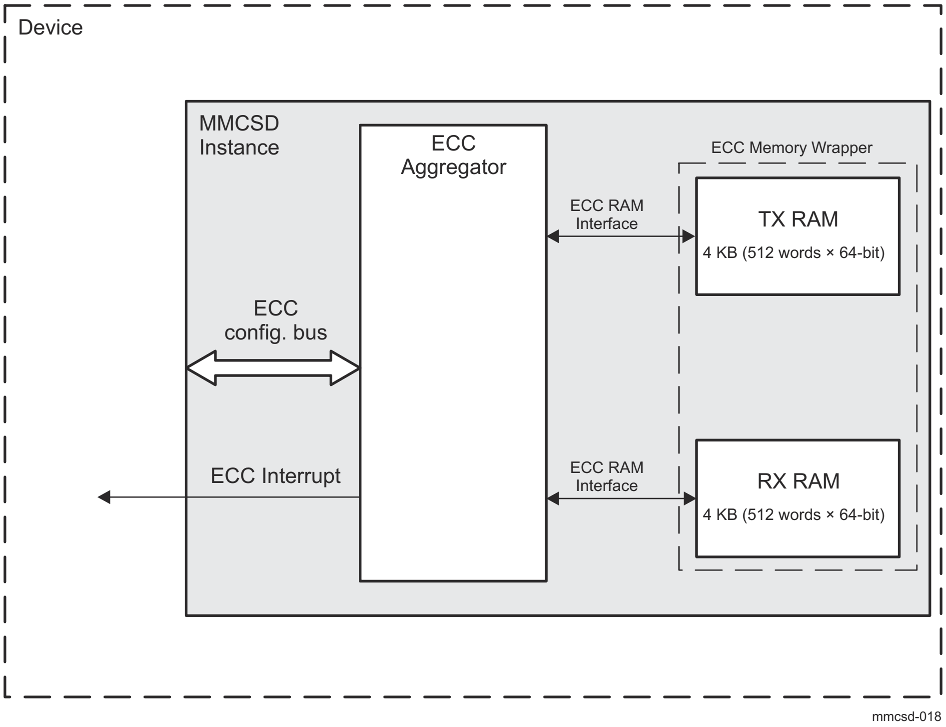

Figure 12-231. ECC Aggregator Block Diagram

Note

For more information about ECC Aggregator Registers, refer to *MMCSD Registers*.

12.4.5.4.4 Advanced DMA

The MMCSD modules support SD Advanced DMA – ADMA2 and ADMA3.

Note

For more information, refer to the SD Association specification titled *"SD Host Controller Simplified Specification, Part A2, Version 4.10"*.

12.4.5.5 MMCSD Programming Guide

12.4.5.5.1 Sequences

This section defines basic sequence flow chart divided into several sub sequences.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

"Wait for interrupts" is used in the flow chart. This means the Host Driver waits until specified interrupts are asserted. If already asserted, then fall through that step in the flow chart. Timeout checking shall be always required to detect no interrupt generated but this is not described in the flow chart.

This specification uses the double box like Figure 12-232, (the step (1) in Figure 12-236), it means that the other flows, which already are shown, shall be performed. Therefore, the interrupt may be included in the other flows.

mmcsd-019

Figure 12-232. Double Box Notation

12.4.5.5.1.1 SD Card Detection

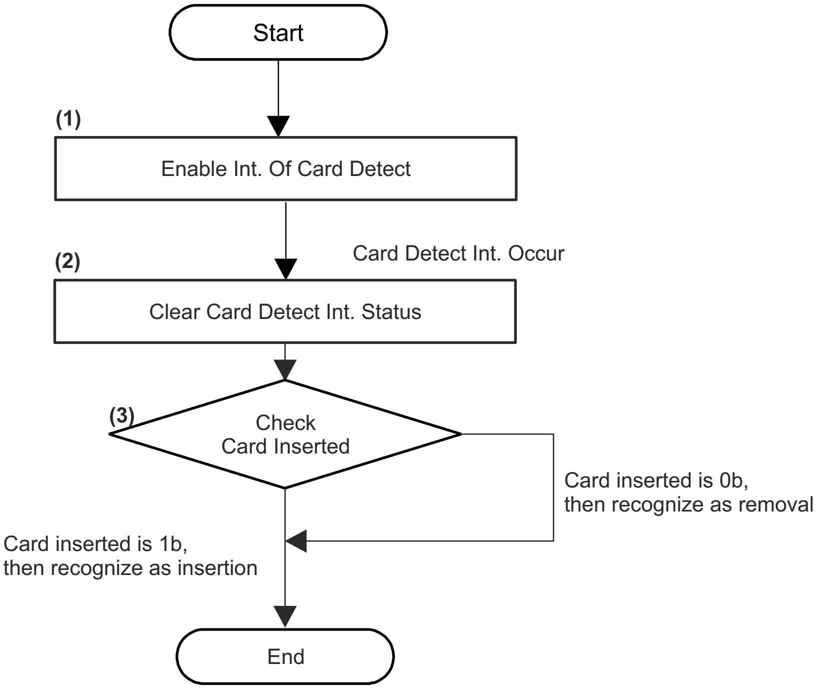

mmcsd-020

Figure 12-233. SD Card Detect Sequence

The flow chart for detecting a SD card is shown in Figure 12-233.

Each step is executed as follows:

To enable interrupt for card detection, write 1 to the following bits:

- MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION
- MMCSD0_NORMAL_INTR_SIG_ENA[6] CARD_INSERTION

- MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL
- MMCSD0_NORMAL_INTR_SIG_ENA[7] CARD_REMOVAL

(1) When the Host Driver detects the card insertion or removal, clear its interrupt statuses. If Card Insertion interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION bit. If Card Removal interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL bit.

(2) Check MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 1, the Host Driver can supply the power and the clock to the SD card. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 0, the other executing processes of the Host Driver shall be immediately closed.

If miniSD adaptor is used for standard SD slot and miniSD card is inserted or extracted from the adaptor, card detect interrupt may not be generated. When host does not receive response to any commands, miniSD card is extracted or in idle state, the host should try to re-initialize the card. In this case, all card information shall be re-loaded.

12.4.5.5.1.2 SD Clock Control

12.4.5.5.1.2.1 Internal Clock Setup Sequence

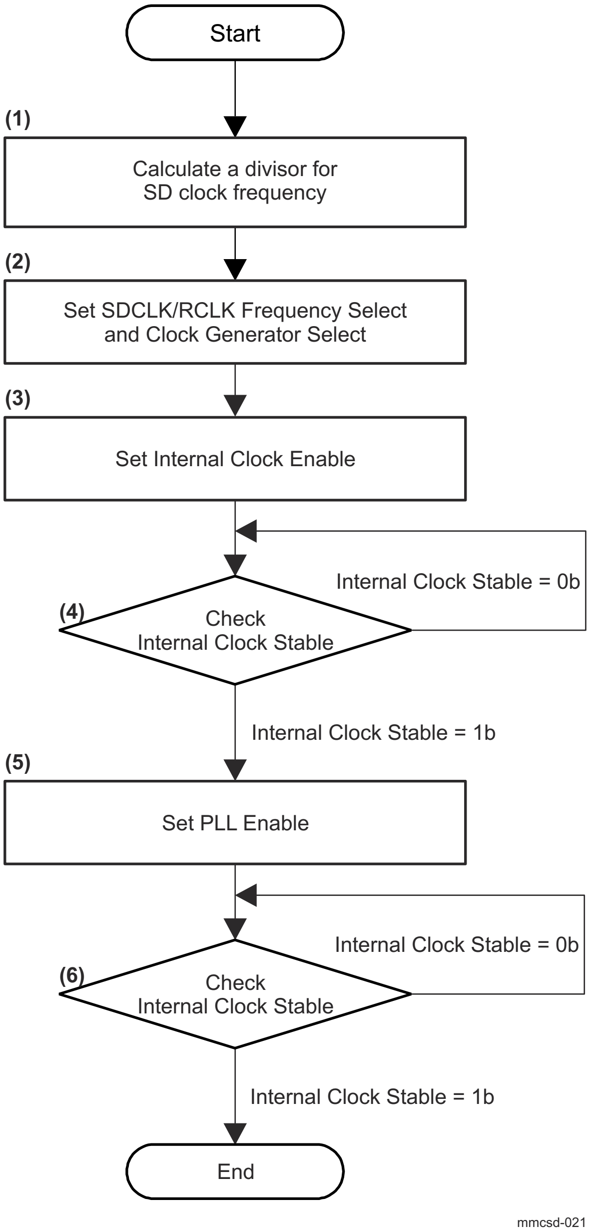

Figure 12-234. Internal Clock Setup Sequence

The sequence for supplying SD Clock to a SD card is described in Figure 12-234. From Version 4.10, MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is added. This sequence is also applicable to prior versions which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(1) Calculate a divisor to determine SD Clock frequency for legacy IF or RCLK frequency for UHS-II IF by reading MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ and MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit fields. If non-zero value is set to MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field, Programmable Clock Mode can be used (for more information, see MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit). If MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field and MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit in accordance with the calculated result of step (1).

If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set, these bits are set by Host Controller automatically as specified in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).

(3) Set MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit.

(4) Check MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit. Repeat this step until this status is 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

(5) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit. This step does not affect Host Controllers which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(6) If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is supported, PLL locked may be checked by this status (if MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this status is supposed to indicate 1 by step (3)). Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

12.4.5.5.1.2.2 SD Clock Supply and Stop Sequence

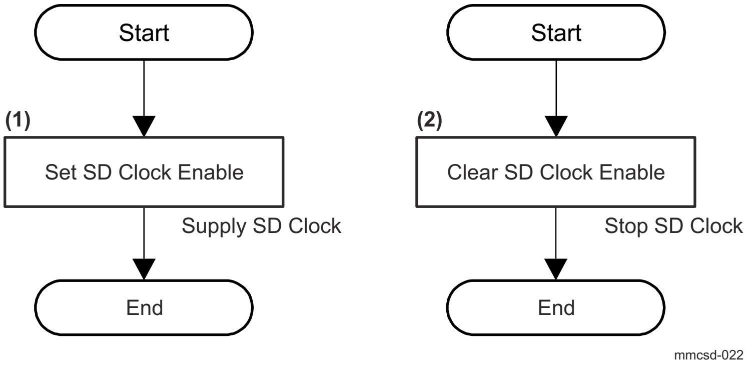

Figure 12-235. SD Clock Supply and Stop Sequence

The flow chart for stopping the SD Clock is shown in Figure 12-235. The Host Driver shall not stop the SD Clock when a SD transaction is occurring on the SD Bus -- namely, when either MMCSD0_PRESENTSTATE[1] INHIBIT_DAT or MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1.

(1) Setup Internal Clock (see Figure 12-234). Then set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 1. Then, the Host Controller starts supplying the SD Clock.

(2) Set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 0. Then, the Host Controller stops supplying the SD Clock. Internal Clock is still oscillating.

12.4.5.5.1.2.3 SD Clock Frequency Change Sequence

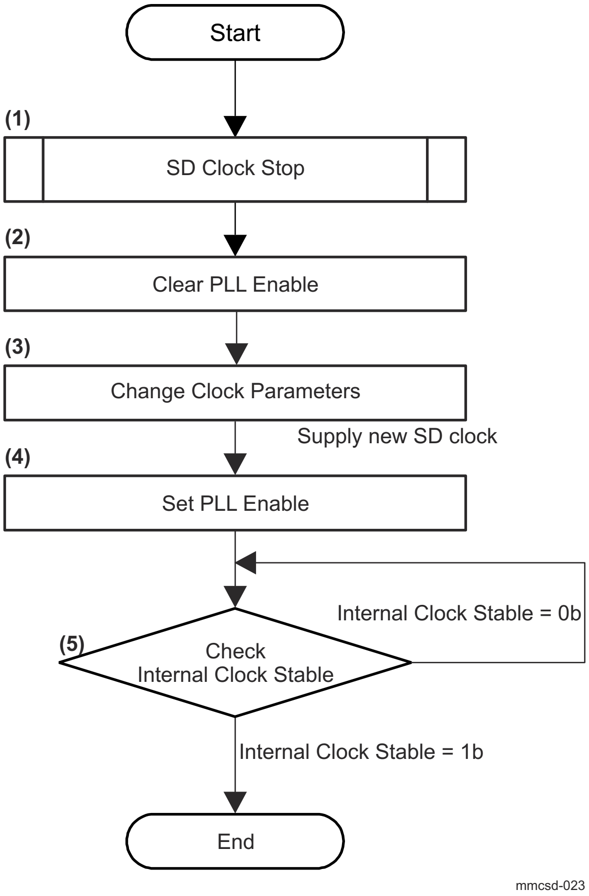

Figure 12-236. SD Clock Change Sequence

The sequence for changing SD Clock frequency is shown in Figure 12-236.

(1) Execute the SD Clock Stop Sequence (see Figure 12-235). If SD Clock supply to card is already stopped, skip this step.

(2) Clear MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 0. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step has no effect and may be skipped.

(3) When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 0, change clock parameters in the MMCSD0_CLOCK_CONTROL register. When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1, select Bus Speed Mode as described.

(4) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 1. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step this step has no effect and may be skipped.

(5) Wait until MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit is set to 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms. SD Clock Supply Sequence is required to provide clock to device (see Figure 12-235).

12.4.5.5.1.3 SD Bus Power Control

The sequence for controlling the SD Bus Power is described in Figure 12-237.

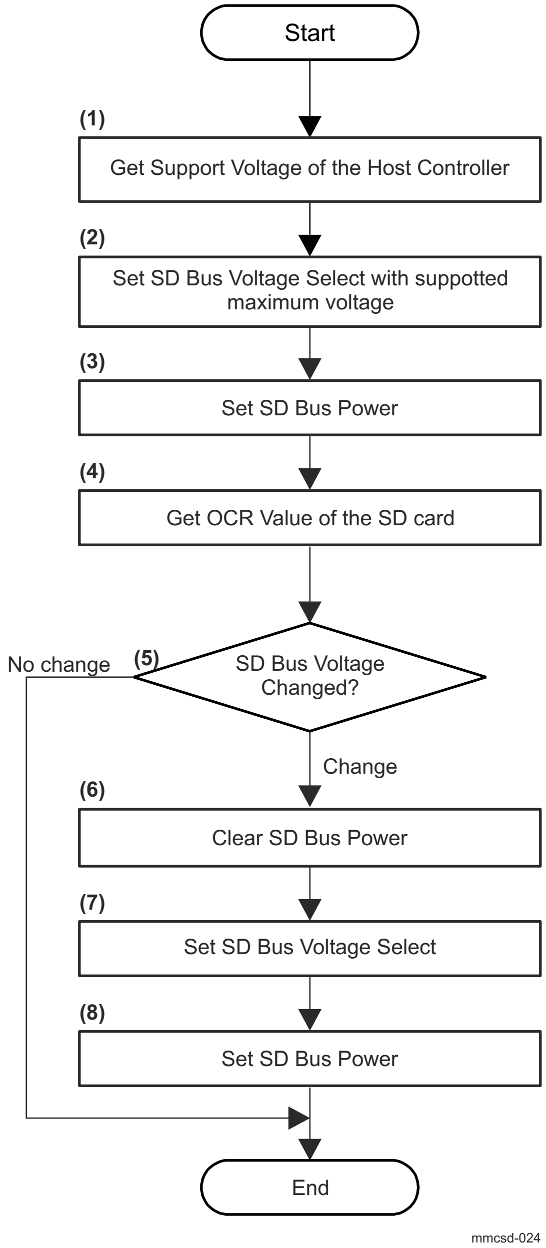

Figure 12-237. SD Bus Power Control Sequence

(1) By reading the MMCSD0_CAPABILITIES register, get the support voltage of the Host Controller.

(2) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field with maximum voltage that the Host Controller supports.

(3) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 1.

(4) Get the OCR value of all function internal of SD card.

(5) Judge whether SD Bus voltage needs to be changed or not. In case where SD Bus voltage needs to be changed, go to step (6). In case where SD Bus voltage does not need to be changed, go to "End".

(6) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 0 for clearing this bit. The card requires voltage rising from 0 volt to detect it correctly. The Host Driver shall

clear MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit before changing voltage by setting MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(7) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(8) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER to 1.

Note: Step (2) and step (3) can be executed at same time. And also, step (7) and step (8) can be executed at same time.

12.4.5.5.1.4 Changing Bus Width

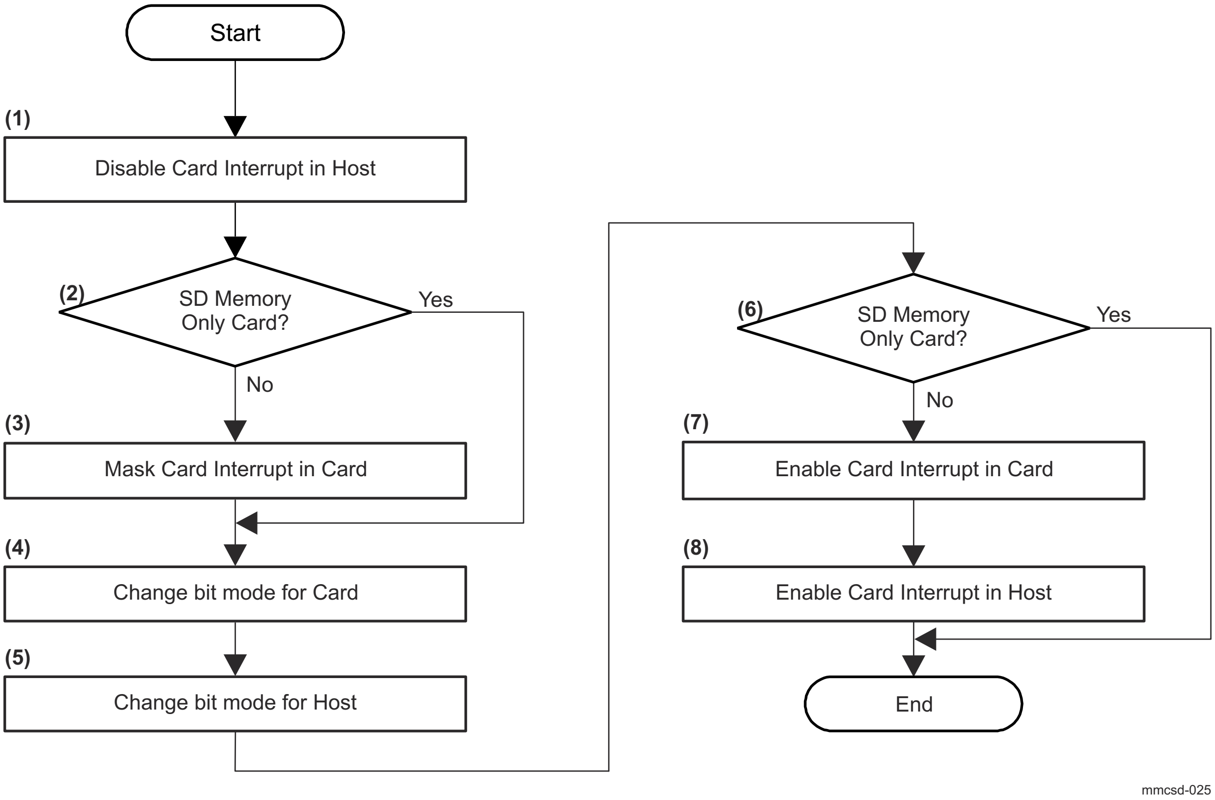

Figure 12-238. Change Bus Width Sequence

The sequence for changing bit mode on SD Bus is shown in Figure 12-238.

(1) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0 for masking incorrect interrupts that may occur while changing the bus width.

(2) In case of SD memory only card, go to step (4). In case of other card, go to step (3).

(3) Set "IENM" of the CCCR in a SDIO or SD combo card to 0 by CMD52.

(4) Change the bus width mode for a SD card. SD Memory Card bus width is changed by ACMD6 and SDIO card bus width is changed by setting Bus Width of Bus Interface Control register in CCCR.

(5) In case of changing to 4-bit mode, set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 1. In another case (1-bit mode), set this bit to 0.

(6) In case of SD memory only card, go to the "End". In case of other card, go to step (7).

(7) Set "IENM" of the CCCR in a SDIO or SD combo card to 1 by CMD52.

(8) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1.

Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

12.4.5.5.1.5 Timeout Setting on DAT Line

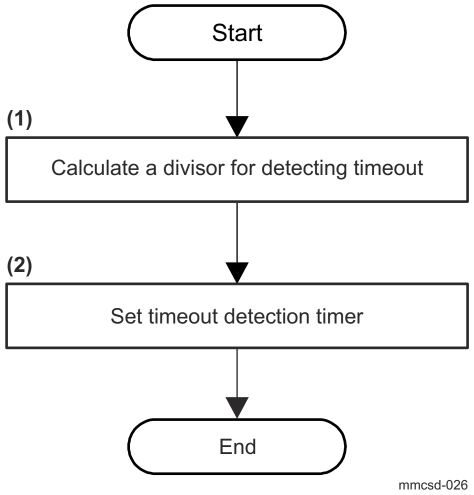

Figure 12-239. Timeout Setting Sequence

In order to detect timeout errors on DAT line, the Host Driver shall execute the following two steps before any SD transaction. For more information regarding SD transactions:

(1) Calculate a divisor to detect timeout errors by reading MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field and MMCSD0_CAPABILITIES[7] TIMEOUT_CLK_UNIT bit. If MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit field in accordance with the value from step (1) above.

12.4.5.5.1.6 Card Initialization and Identification (for SD I/F)

Figure 12-240 and Figure 12-241 shows initialization and card identification sequence for the Standard Capacity SD Memory Card (SDSC), the High Capacity SD Memory Card (SDHC) and the Extended Capacity SD Memory Card (SDXC) that was based on the Physical Layer Version 3.01. Refer to the latest sequence.

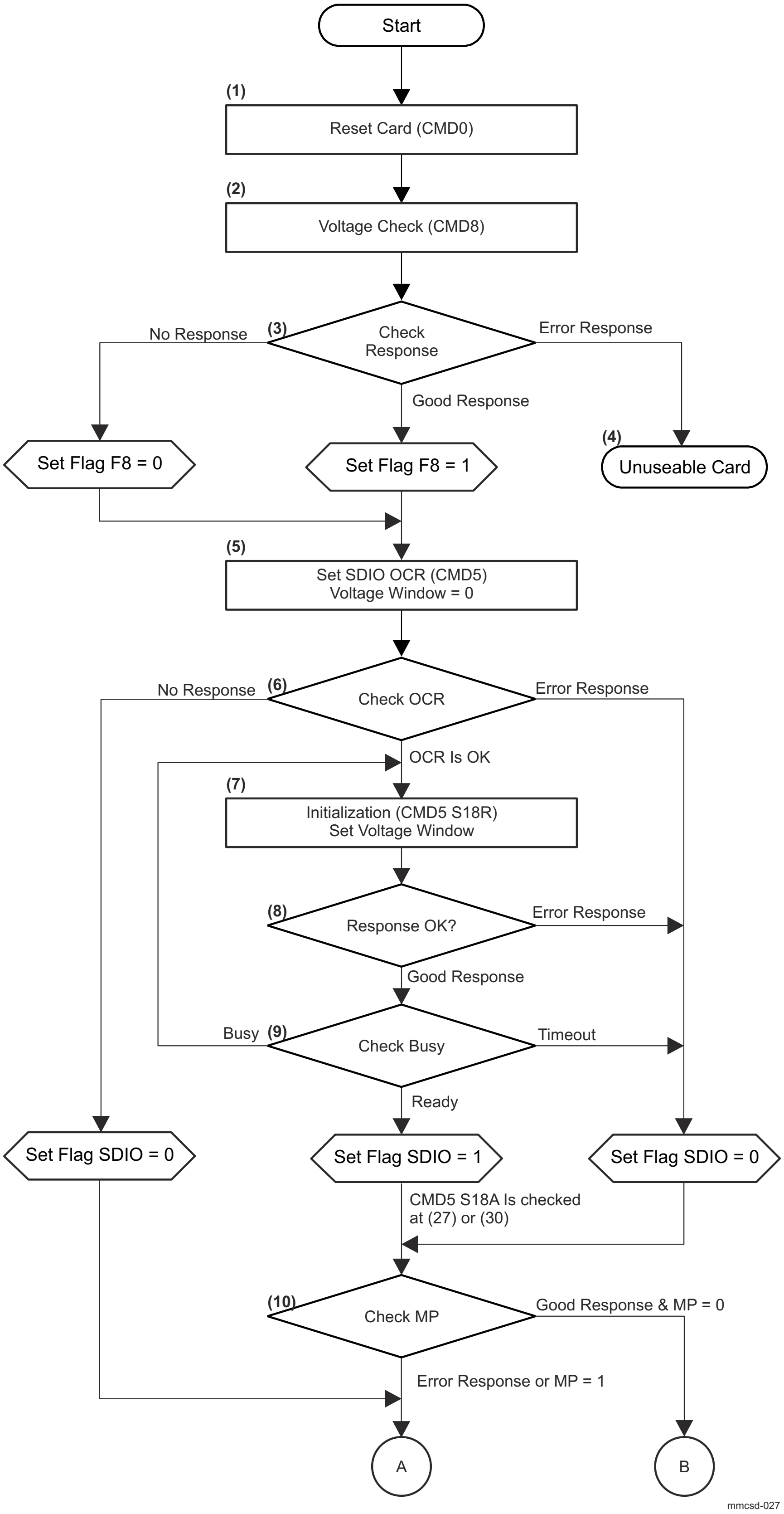

Figure 12-240. Card Initialization and Identification (1)

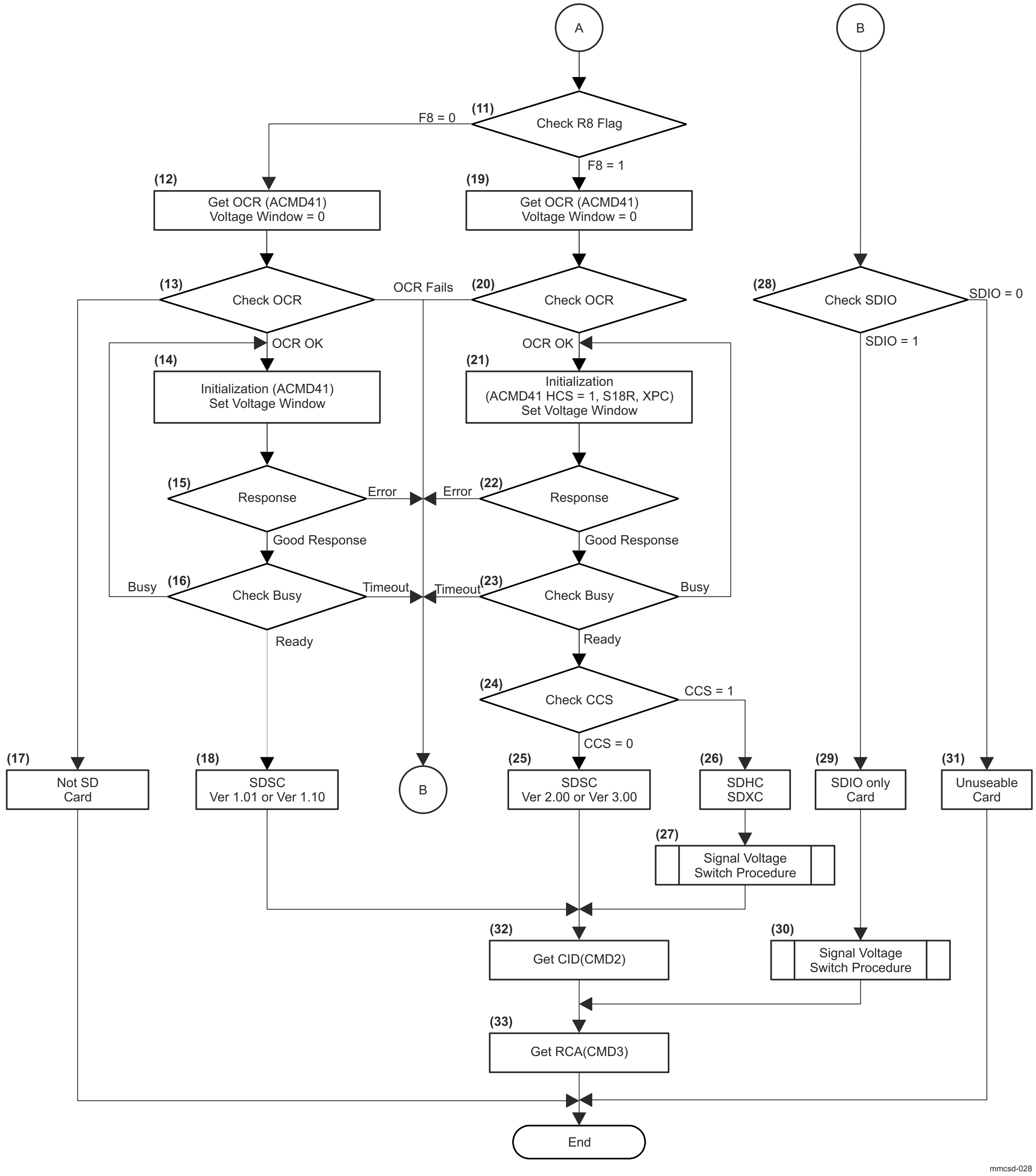

Figure 12-241. Card Initialization and Identification (2)

(1) SD Bus mode is selected by CMD0 (Keep Pin 1 to high during CMD0 execution).

(2) New CMD8 shall be issued after CMD0 to support High Capacity SD Memory Card.

(3) Voltage check command enables the Hosts to support future low voltage specification. However, at this time, only one voltage is defined. Legacy cards and Not SD cards do not respond to CMD8. In this case, set F8 to 0 (F8 is CMD8 valid flag used in step (11)) and go to Step (5). Only Version 2.00 or higher cards can respond to CMD8. The host needs to check whether CRC of the response is valid and whether VHS and check pattern in the argument are equal to VCA and check pattern in the response. Passing all these checks results in CMD8 response OK. In this case, set F8 to 1 and go to step (5). If one of the checks is failed, go to step (4).

(4) Initialization is stopped by CMD8 fails. The Host Driver should retry step (1) to (3) one more time (this is not described in the figure).

(5) SDIO OCR is available by issuing CMD5 with setting voltage window (bit 23 to 0) in the argument to 0. SDIO initialization is not started.

(6) No response means the card does not have SDIO function. Set SDIO flag to 0 and go to step (11). If the card responds to CMD5 and the response is OK, go to step (7). If the response is error, set SDIO flag to 0 and go to step (10). SDIO flag indicates whether SDIO functions are initialized or not.

(7) The SDIO portion starts initialization by CMD5 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to 1. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(8) If no response or error response is receive, set SDIO flag to 0 and go to step (10). If good response is received, go to step (9).

(9) Check busy status in the response. If busy is released, set SDIO flag to 1 and go to step (10). Repeat from step (7) while busy is indicated. Detecting timeout of 1 second exits the loop. In this case, set SDIO flag to 0 and go to step (10).

(10) Good response in this step means that all responses received at (6) and (8) are valid. When response is good, MP (memory present) flag in the response can be checked. If the response valid and MP = 0, go to step (28). Otherwise, go to step (11).

(11) Check F8 flag set in step (3). If CMD8 is executed correctly (F8 = 1), go to step (19). Otherwise, go to step (12).

(12) OCR is available by issuing ACMD41 with the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. The response of CMD55 (ACMD41) may indicate illegal command error due to some SD cards do not recognized CMD8. The Host Driver should ignore this error or issue CMD0 before ACMD41 to clear this error status.

(13) If response of CMD55 is not received, the card is not SD cards and goes to (17). If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (14). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(14) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(15) If no response or error response is received, go to step (28). If good response is received, go to step (16).

(16) Check busy status in the response. If busy is released, go to step (18). Repeat from step (14) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(17) The host recognizes that the card is not SD memory card and quits SD card initialization.

(18) The host recognizes that the card is Version 1.xx Standard Capacity SD Memory Card. Go to Step (30).

(19) OCR is available by issuing ACMD41 with setting the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. Setting of HCS does not affect this operation.

(20) If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (21). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(21) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to1. If the host can supply more than 150mA, XPC is set to 1. HCS in the argument is set to 1, which indicates supporting High Capacity Memory Card. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(22) If no response or error response is received, go to step (28). If good response is received, go to step (23).

(23) Check busy status in the response. If busy is released, go to step (24). Repeat from step (21) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(24) CCS in the response is valid after busy is released. If CCS = 0, it indicates the Standard Capacity SD Memory Card and go to step (25). If CCS = 1, it indicates the High Capacity SD Memory Card or Extended Capacity Memory Card and go to Step (26).

(25) The host recognizes that the card is Ver2.00 or Ver3.00 Standard Capacity SD Memory Card. Optimal functions defined in Version 2.00 or higher are available. Go to Step (32).

(26) The host recognizes that the card is the High Capacity SD Memory Card or Extended Capacity Memory Card.

(27) Perform the signal voltage switch procedure and go to step (32).

(28) Check SDIO flag. If SDIO = 1, go to step (28). Otherwise, go to step (31).

(29) The host recognizes that the card is SDIO only card and go to step (30).

(30) Perform the signal voltage switch procedure and go to step (33).

(31) The host recognizes that the card is unusable.

(32) In case of memory card, CMD2 is issued to get CID and Go to Step (31).

(33) CMD3 is issued to get RCA. If the RCA number is 0, the Host should issue CMD3 again.

12.4.5.5.1.6.1 Signal Voltage Switch Procedure (for UHS-I)

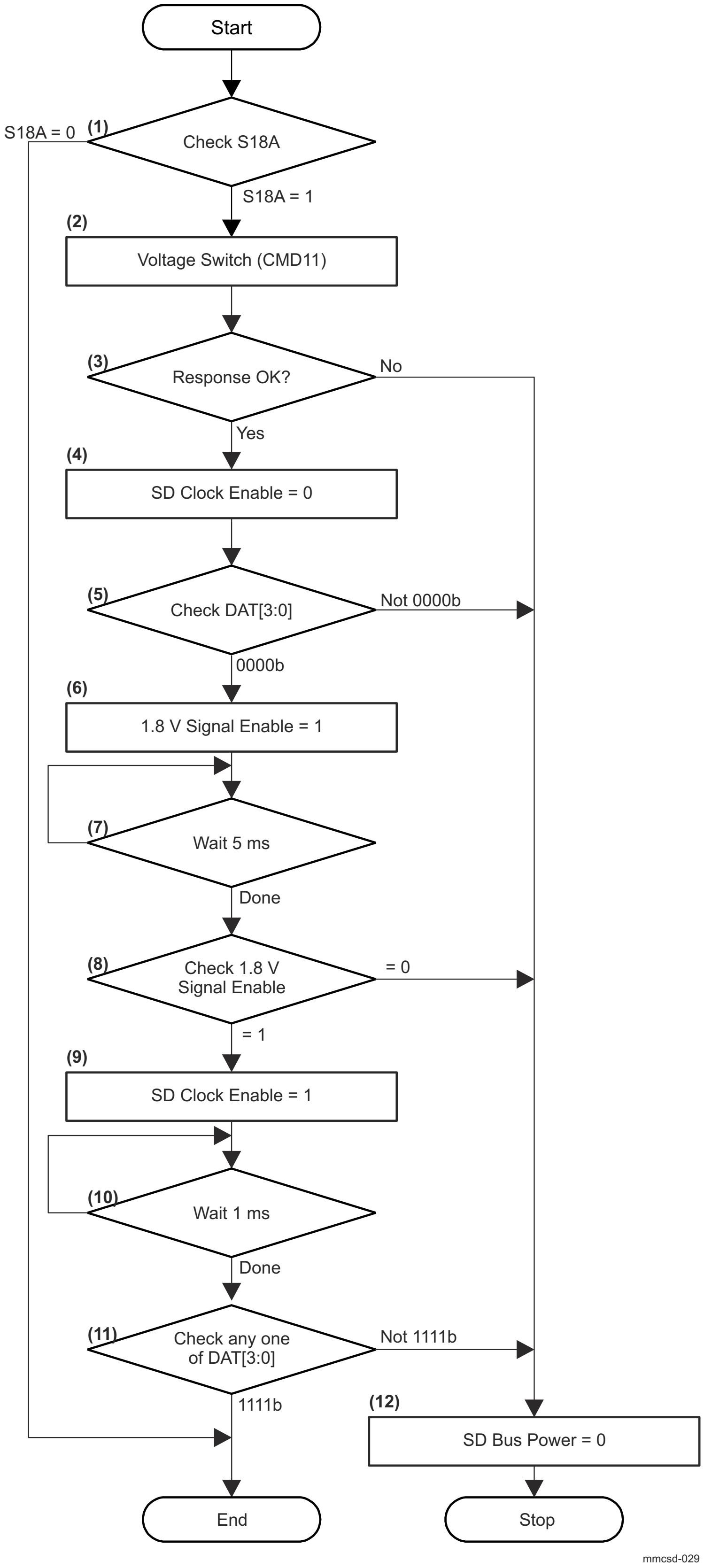

Figure 12-242. Signal Voltage Switch Procedure

(1) If S18A of CMD5 or S18A of ACMD41 is set to 1, signal voltage switch is performed according to the following steps. Otherwise, exits from this procedure.

(2) Issue CMD11.

(3) Check response and if an error is detected, go to step (12).

(4) Stop providing SD clock to the card.

(5) Check DAT[3:0] level. If the level is 0000b, the card is ready to start voltage switch sequence. Otherwise, go to (12) to quit the sequence.

(6) Set MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit.

(7) Wait 5 ms. 1.8 V voltage regulator shall be stable within this period.

(8) If MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is cleared by Host Controller, go to step (12).

(9) Provide SD Clock to the card again.

(10) Wait 1 ms.

(11) Check DAT[3:0] level. If the level is 1111b, switch to 1.8 V signal level is completed successfully. Otherwise, go to (12).

(12) If an error occurs during voltage switch procedure, stop providing the power to the card. In this case, Host Driver should retry initialization procedure by setting S18R to 0 at step (7) and (21) in Figure 12-240 and Figure 12-241.

12.4.5.5.1.7 SD Transaction Generation

This section describes the sequences how to generate and control various kinds of SD transactions. SD transactions are classified into three cases:

(1) Transactions that do not use the DAT line.

(2) Transactions that use the DAT line only for the busy signal.

(3) Transactions that use the DAT line for transferring data.

In this specification the first and the second case's transactions are classified as "Transaction Control without Data Transfer using DAT Line", the third case's transaction is classified as "Transaction Control with Data Transfer using DAT Line". Refer to the latest SD Physical Layer Specification and SDIO Specification for more detail about SD commands specification.

12.4.5.5.1.7.1 Transaction Control without Data Transfer Using DAT Line

In this section, the sequence for how to issue SD Command and how to complete SD Command is explained. Figure 12-243 shows the sequence to issue a SD Command and Figure 12-244 shows the sequence to finalize a SD Command.

12.4.5.5.1.7.1.1 The Sequence to Issue a SD Command

The sequence to issue the SD Command is detailed in Figure 12-243.

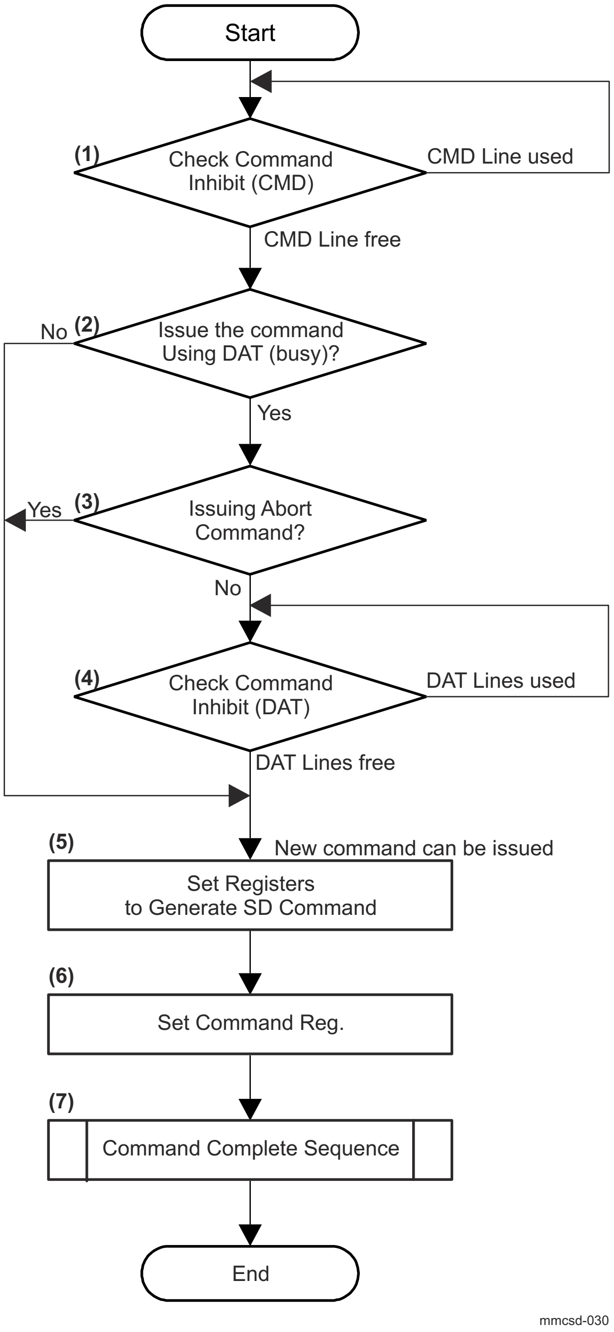

Figure 12-243. SD Command Issue Sequence

(1) Check MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 0. That is, when MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 1, the Host Driver shall not issue a SD Command.

(2) If the Host Driver issues a SD Command using DAT lines including busy signal, go to step (3). If without using DAT lines including busy signal, go to step (5).

(3) If the Host Driver is issuing an abort command, go to step (5). In the case of nonabort command, go to step (4).

(4) Check MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit. Repeat this step until MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit is set to 0.

(5) Set registers except the MMCSD0_COMMAND register.

(6) Set the MMCSD0_COMMAND register.

Note: Writing the upper byte [3] in the MMCSD0_COMMAND register causes the Host Controller to issue a SD command to the SD card.

(7) Perform Command Completion Sequence in accordance.

12.4.5.5.1.7.1.2 The Sequence to Finalize a Command

Figure 12-244 shows the sequence to finalize a SD Command when response check is disabled. There is a possibility that some errors (Command Index/End bit/CRC/Timeout Error) occur during this sequence. If response check is enabled, error is indicated by Response Error Interrupt.

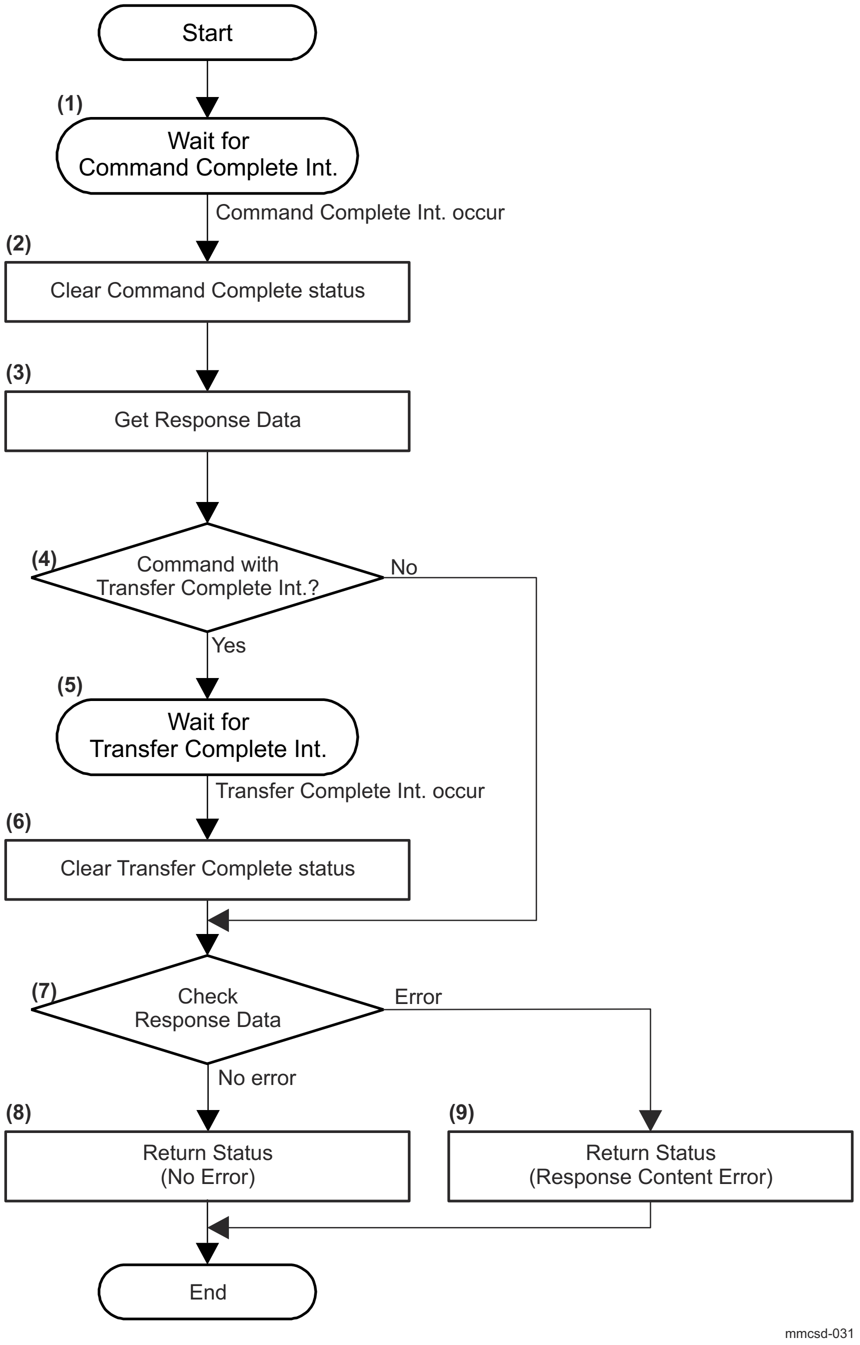

Figure 12-244. Command Complete Sequence

12.4.5.5.1.7.1.3

(1) If MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1 (response check is enabled), go to stop (4) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE). If the Command Complete Interrupt has occurred, go to step (2).

(2) Write 1 to MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(3) Read the Response register (see MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(4) Judge whether the command uses the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) or not. If it uses Transfer Complete, go to step (5). If not, go to step (7).

(5) Wait for the Transfer Complete Interrupt. If the Transfer Complete Interrupt has occurred, go to step (6).

(6) Write 1 to MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(7) Check for errors in Response Data (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If there is no error, go to step (8). If there is an error, go to step (9).

(8) Return Status of "No Error".

(9) Return Status of "Response Contents Error".

Note1: While waiting for the Transfer Complete interrupt, the Host Driver shall only issue commands that do not use the busy signal.

Note2: The Host Driver shall judge the Auto CMD12 complete by monitoring Transfer Complete.

Note3: When the last block of un-protected area is read using memory multiple block read command (CMD18), OUT_OF_RANGE error may occur even if the sequence is correct. The Host Driver should ignore it. This error will appear in the response of Auto CMD12 or in the response of the next memory command.

12.4.5.5.1.7.2 Transaction Control with Data Transfer Using DAT Line

Depending on whether DMA (optional) is used or not, there are two execution methods.

In addition, the sequences for SD transfers are classified into following three kinds according to how the number of blocks is specified:

(1) Single Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified is always one.

(2) Multiple Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified shall be one or more.

(3) Infinite Block Transfer: The number of blocks is not specified to the Host Controller before the transfer. This transfer is continued until an abort transaction is executed. This abort transaction is performed by CMD12 in the case of a SD memory card and by CMD52 in the case of a SDIO card.

12.4.5.5.1.7.2.1 Not using DMA

The sequence for not using DMA is shown in Figure 12-245.

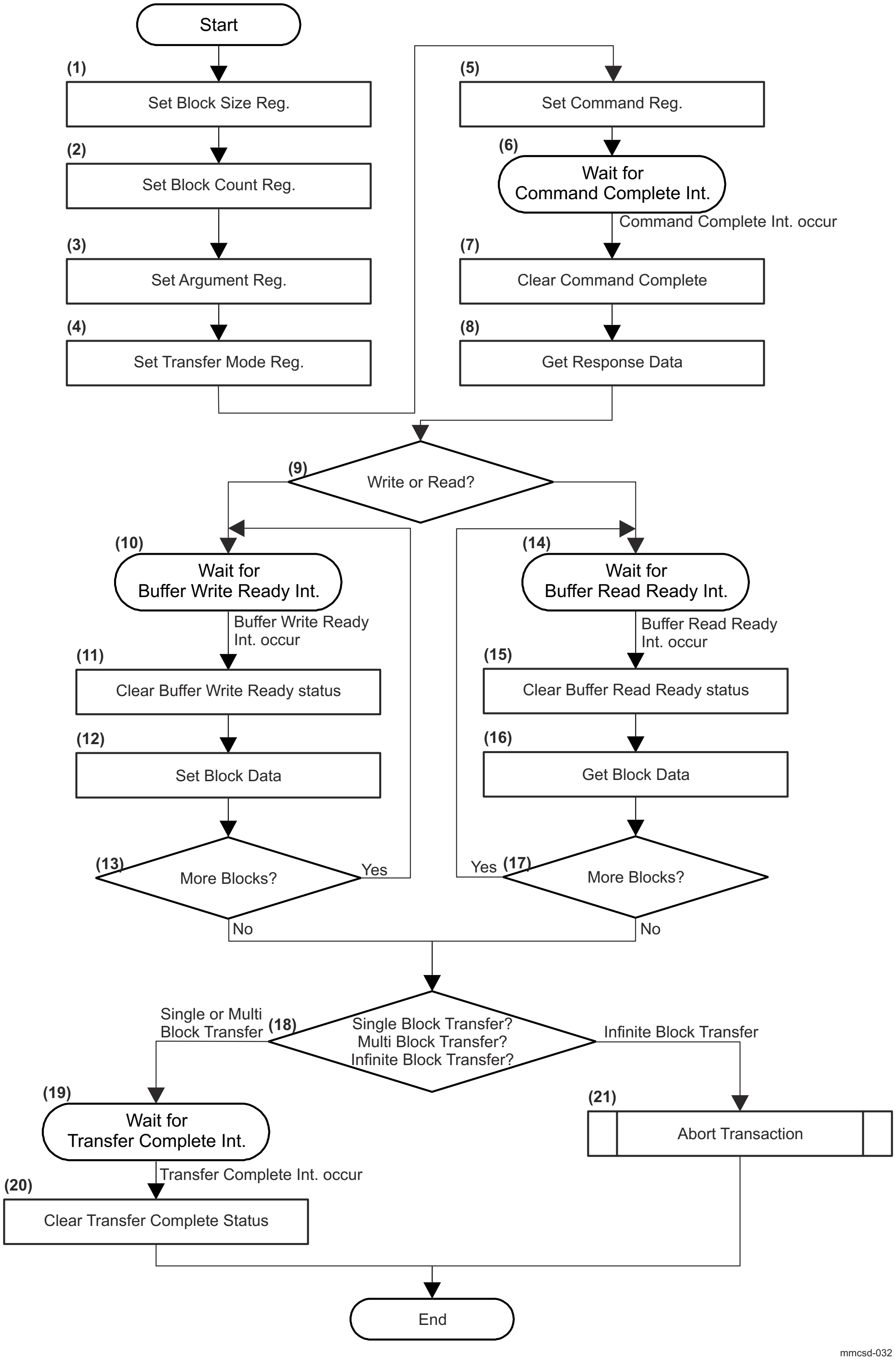

Figure 12-245. Transaction Control with Data Transfer Using DAT Line Sequence (Not using DMA)

(1) Set the value corresponding to the executed data byte length of one block to the MMCSD0_BLOCK_SIZE register.

(2) Set the value corresponding to the executed data block count to the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(3) Set the argument value to Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(4) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*.

If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(5) Set the value to MMCSD0_COMMAND register.

Note: When writing the upper byte [3] of MMCSD0_COMMAND register, SD command is issued.

(6) If response check is enabled, go to stop (9) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(7) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit for clearing this bit.

(8) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(9) In the case where this sequence is for write to a card, go to step (10). In case of read from a card, go to step (14).

(10) Then wait for Buffer Write Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY).

(11) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY bit for clearing this bit.

(12) Write block data (in according to the number of bytes specified at the step (1)) to MMCSD0_DATA_PORT register.

(13) Repeat until all blocks are sent and then go to step (18).

(14) Then wait for the Buffer Read Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY).

(15) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY bit for clearing this bit.

(16) Read block data (in according to the number of bytes specified at the step (1)) from the MMCSD0_DATA_PORT register.

(17) Repeat until all blocks are received and then go to step (18).

(18) If this sequence is for Single or Multiple Block Transfer, go to step (19). In case of Infinite Block Transfer, go to step (21).

(19) Wait for Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(20) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit for clearing this bit.

(21) Perform the sequence for Abort Transaction in accordance with Section 12.4.5.5.1.8 , *Abort Transaction*.

Note: Step (1) and Step (2) can be executed at same time. Step (4) and Step (5) can be executed at same time.

12.4.5.5.1.7.2.2 Using SDMA

The sequence for using SDMA is shown in Figure 12-246.

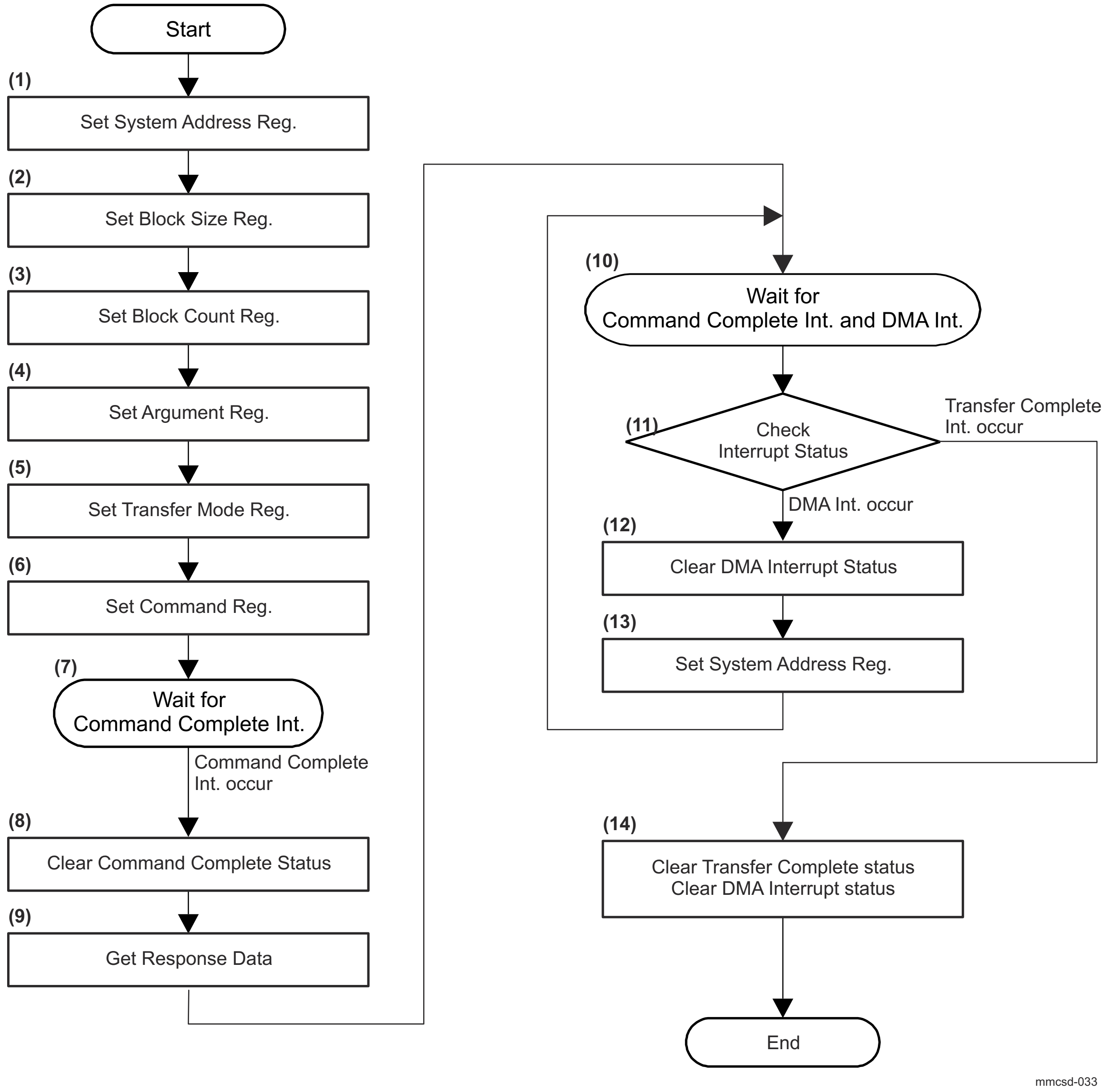

Figure 12-246. Transaction Control with Data Transfer Using DAT Line Sequence (Using SDMA)

(1) Data location of system memory is set to the SDMA System Address register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0 or set to the MMCSD0_ADMA_SYS_ADDRESS register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1.

(2) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(3) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(4) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(5) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the

MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5.

(6) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and SDMA is started.

(7) If response check is enabled, go to stop (10) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(8) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(9) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(10) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and DMA Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT).

(11) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step
(14) else if MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit is set to 1, go to Step
(12). The MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is higher priority than the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit.

(12) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

(13) Set the next system address of the next data position to the System Address register (MMCSD0_ADMA_SYS_ADDRESS) and go to Step (10).

(14) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit and MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

Note: Step (2) and Step (3) can be executed simultaneously. Step (5) and Step (6) can also be executed simultaneously.

12.4.5.5.1.7.2.3 Using ADMA

The sequence for using ADMA is shown in Figure 12-247.

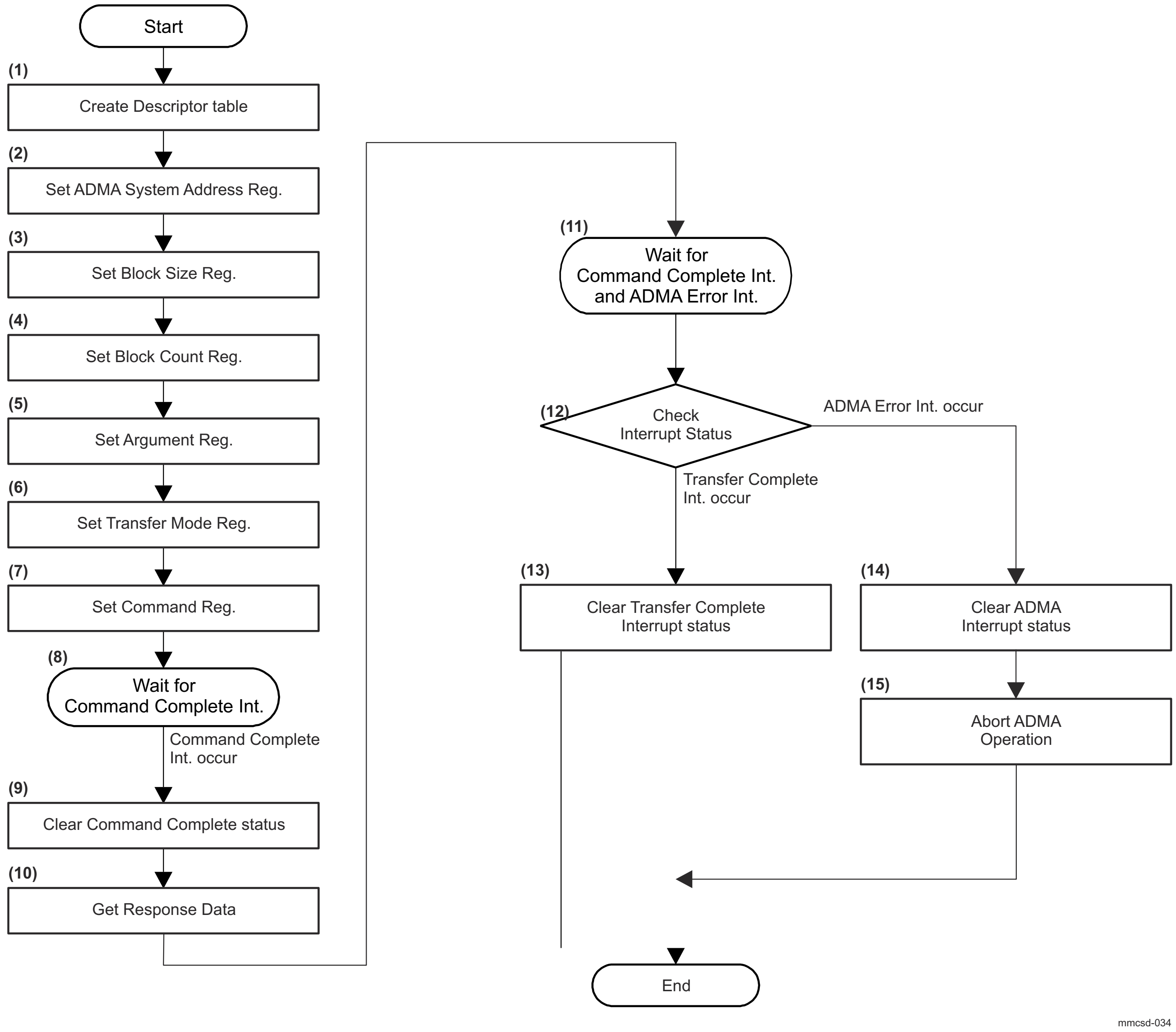

Figure 12-247. Transaction Control with Data Transfer Using DAT Line Sequence (Using ADMA)

(1) Create Descriptor table for ADMA in the system memory.

(2) Set the Descriptor address for ADMA in the MMCSD0_ADMA_SYS_ADDRESS register.

(3) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(4) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(5) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(6) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7]

RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(7) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and DMA is started.

(8) If response check is enabled, go to stop (11) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(9) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(10) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(11) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and ADMA Error Interrupt (MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE).

(12) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step (13) else if MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field is set to 1, go to Step (14).

(13) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(14) Write 1 to the MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field to clear this bit.

(15) Abort ADMA operation. SD card operation should be stopped by issuing abort command. If necessary, the Host Driver checks MMCSD0_ADMA_ERR_STATUS register to detect why ADMA error is generated.

Note: Step (3) and Step (4) can be executed simultaneously. Step (6) and Step (7) can also be executed simultaneously.

12.4.5.5.1.8 Abort Transaction

An abort transaction is performed by issuing CMD12 for a SD memory card and by issuing CMD52 for a SDIO card. There are two cases where the Host Driver needs to do an Abort Transaction. The first case is when the Host Driver stops Infinite Block Transfers. The second case is when the Host Driver stops transfers while a Multiple Block Transfer is executing.

There are two ways to issue an Abort Command. The first is an asynchronous abort. The second is a synchronous abort. In an asynchronous abort sequence, the Host Driver can issue an Abort Command at any time unless MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1. In a synchronous abort, the Host Driver shall issue an Abort Command after the data transfer stopped by using MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

12.4.5.5.1.8.1 Asynchronous Abort

The sequence for Asynchronous Abort is shown in Figure 12-248.

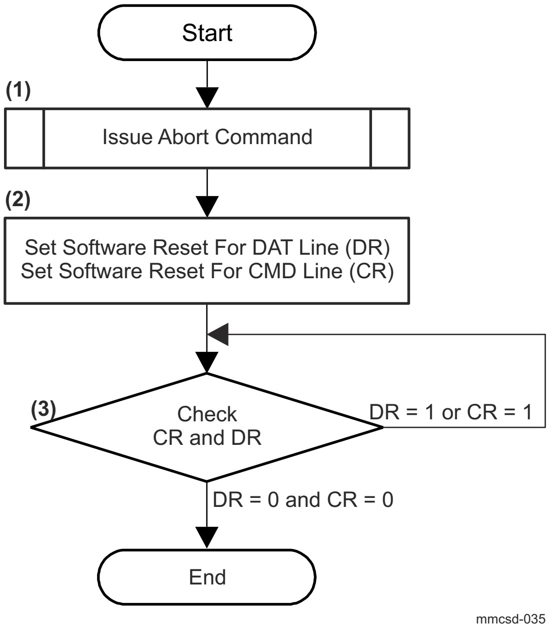

Figure 12-248. Asynchronous Abort Sequence

(1) Issue Abort Command in accordance.

(2) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(3) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (3).

12.4.5.5.1.8.2 Synchronous Abort

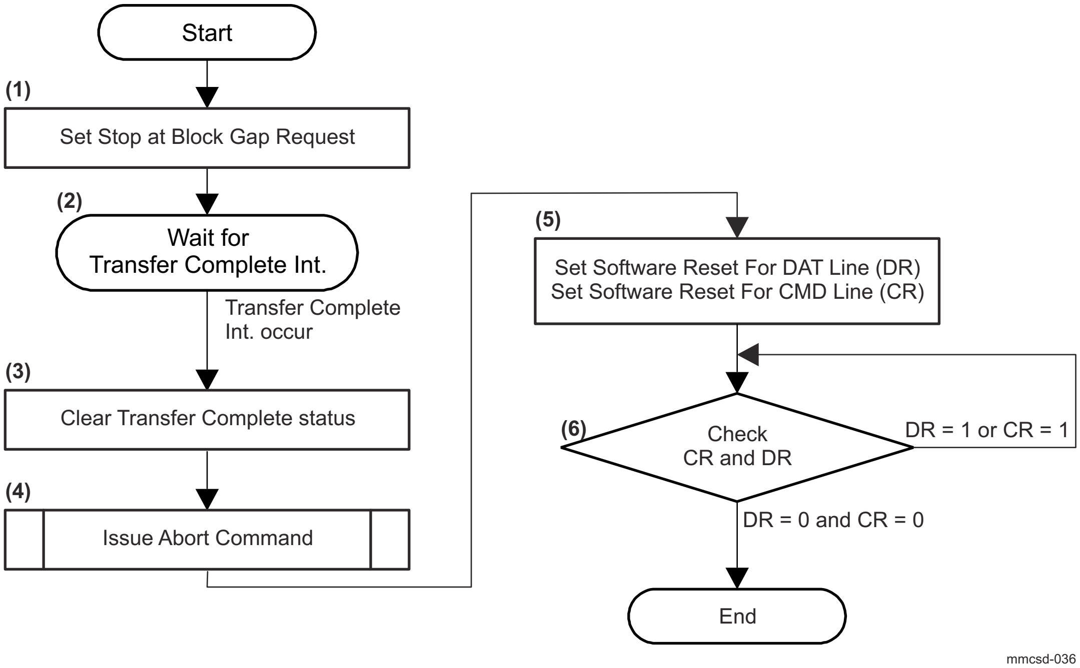

Figure 12-249. Synchronous Abort Sequence

(1) Set the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop SD transactions.

(2) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(3) Set the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to 1 to clear this bit.

(4) Issue the Abort Command

(5) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(6) Check both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (6).

12.4.5.5.1.9 Changing Bus Speed Mode

This section describes the sequence for switching the bus speed mode: Default Speed, High Speed mode and UHS-I mode. The switch command (CMD6) is used to change memory card bus speed mode. The EHS bit (SDIO Version 2.00) or BSS[2-0] bits (SDIO Version 3.00) in the CCCR register is used to change the bus speed mode for SDIO card. In case of Combo card, either of the switch method changes both memory and IO bus speed mode. This means the first switch is effective. Refer to the Physical Layer Specification Version 3.0x and the SDIO Specification Version 3.00 for more information about switching bus speed. Figure 12-250 shows the sequence for switching bus speed mode for Combo Card. Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

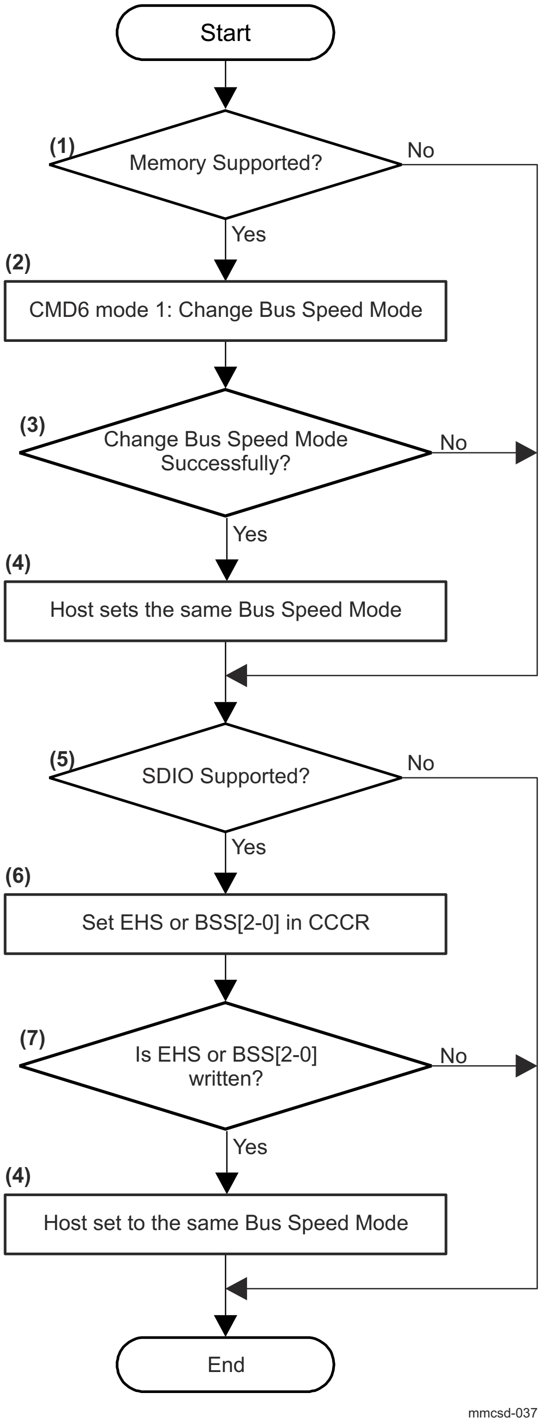

Figure 12-250. Changing Bus Speed Mode

(1) The Host Driver checks if the card supports memory. If not supported, go to (5).

(2) Issue CMD6 with mode 1 to change bus speed mode (Default, High Speed mode or UHS-I mode).

(3) Check the response of CMD6. If the card does not supports CMD6 (no response) or bus speed is not changed successfully, go to step (5). In this case, the card is in Default Speed mode.

(4) The Host Driver changes the Host Controller bus speed mode to the same mode.

(5) The Host Driver checks if the card supports SDIO. If not supported, go to the end.

(6) Issue CMD52 to write EHS bit or BSS[2-0] bits in CCCR to change bus speed mode (the same bus speed mode of (2) shall be set).

(7) If EHS or BSS[2-0] are not changed successfully, go to the end.

(8) The Host Driver changes the Host Controller bus speed to the same mode. In case of Combo card, bus speed is already changed at step (4) and this step does not affect changing bus speed.

12.4.5.5.1.10 Error Recovery

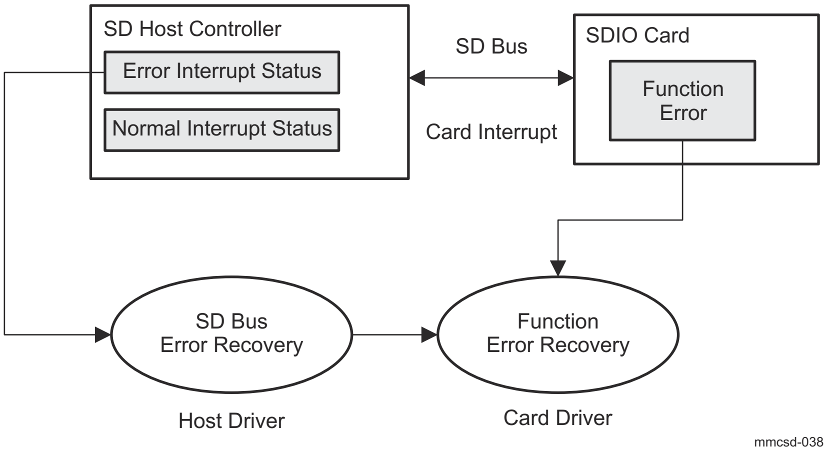

Figure 12-251. Error Report and Recovery

Figure 12-251 shows concept of error report and its recovery. The Host Controller has 2 interrupt status registers. If an error occurs in the SD Bus transaction, one of the bits is set in the MMCSD0_ERROR_INTR_STS register. If the function errors occur in the SDIO card, the card interrupt informs these function errors and the Card interrupt is set in the MMCSD0_NORMAL_INTR_STS_ENA register (the Card Interrupt is used to inform not only error statuses but also normal information. For example, to inform function ready). The Card Driver shall do function error recovery because the Host Driver does not know how to control the function. In the case that function error occurs due to SD Bus error, SD Bus error recovery is required before function error recovery. Abort command is used to recover SD Bus, and then the Host Driver should save error statuses related to SD Bus errors before issuing abort command and transfer these statuses to the Card Driver. These statuses may be used to recover function error. Following explanations are related to SD Bus error recovery. This specification does not specify the function error recovery.

When an error occurs during data transfer in 2L-HD UHS-II mode, there will be the case that Host Controller cannot drive D0 lane in input mode due to DIR LSS for retrieving lane direction is not detected. In this case, Host Driver cannot issue abort command for recovery. Then if DIR LSS is not detected, Host Controller sets MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit. Host Driver should execute power cycle if MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit is detected to recover from this error. Furthermore, if this type of error is detected several times in 2L-HD, Host Driver should use FD mode rather than using 2L-HD.

Implementation Note:

If the Card Driver cannot recover the function errors, the Host Driver should try following methods.

(9) Using IOEx for SDIO card

IOEx may be used as the reset per function basis. Sequence is as follows:

Clear IOEx = 0 and wait until IORx = 0 and then set IOEx = 1 again. SDIO may be recovered when IORx = 1.

(10) Using reset command for memory and SDIO card Re-initialization sequence is required.

(11) Off and on power supply for the SD Bus.

The card may be recovered by the power on reset. Re-initialization sequence is required.

The two cases where the Host Driver needs the "Error Recovery" sequence are classified as follows:

(1) Error Interrupt Recovery:

If error interrupt is indicated by the MMCSD0_ERROR_INTR_STS register, the Host Driver shall apply this sequence.

(2) Auto CMD12 Error Recovery:

If there are errors in Auto CMD12, the Host Driver shall apply this sequence. In terms of Return Status, Auto CMD12 Error Recovery is classified into 4 cases. It is shown in Figure 12-252. If error occurs during memory write transfer, strongly recommend using ACMD22 and then in the following recovery sequence, retry to send remaining blocks not written.

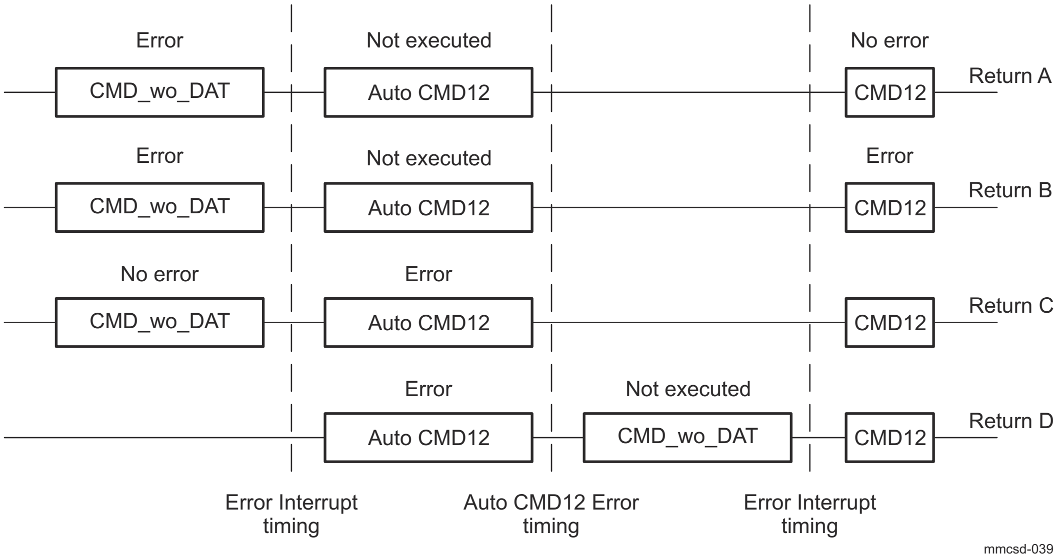

Figure 12-252. Return Status of Auto CMD12 Error Recovery

Implementation Note:

Abort command is used to recover from SD Bus error. SDIO transaction abort using CMD52 returns response but in the case of memory transaction abort using CMD12, response returns depending on the memory card state. If no response returns after issue CMD12, the Host Driver should check card state using CMD13. If the state is "tran" in the CURRENT_STATE, consider CMD12 is successful.

Implementation Note:

The following sequence is one possible error recovery flow. There may be another methods, sometimes using interrupts or polling. It can be possible to use another flows, based on Host System requirements.

In these error recovery sequences, return statuses for the next sequence. When the Host Controller cannot issue the next command due to SD Bus error, the error recovery sequences return "Non-recoverable" status. In this case, the Host System may cut off power to the SD Bus and then power on SD Bus and initialize both the Host Controller and the SD card again.

12.4.5.5.1.10.1 Error Interrupt Recovery

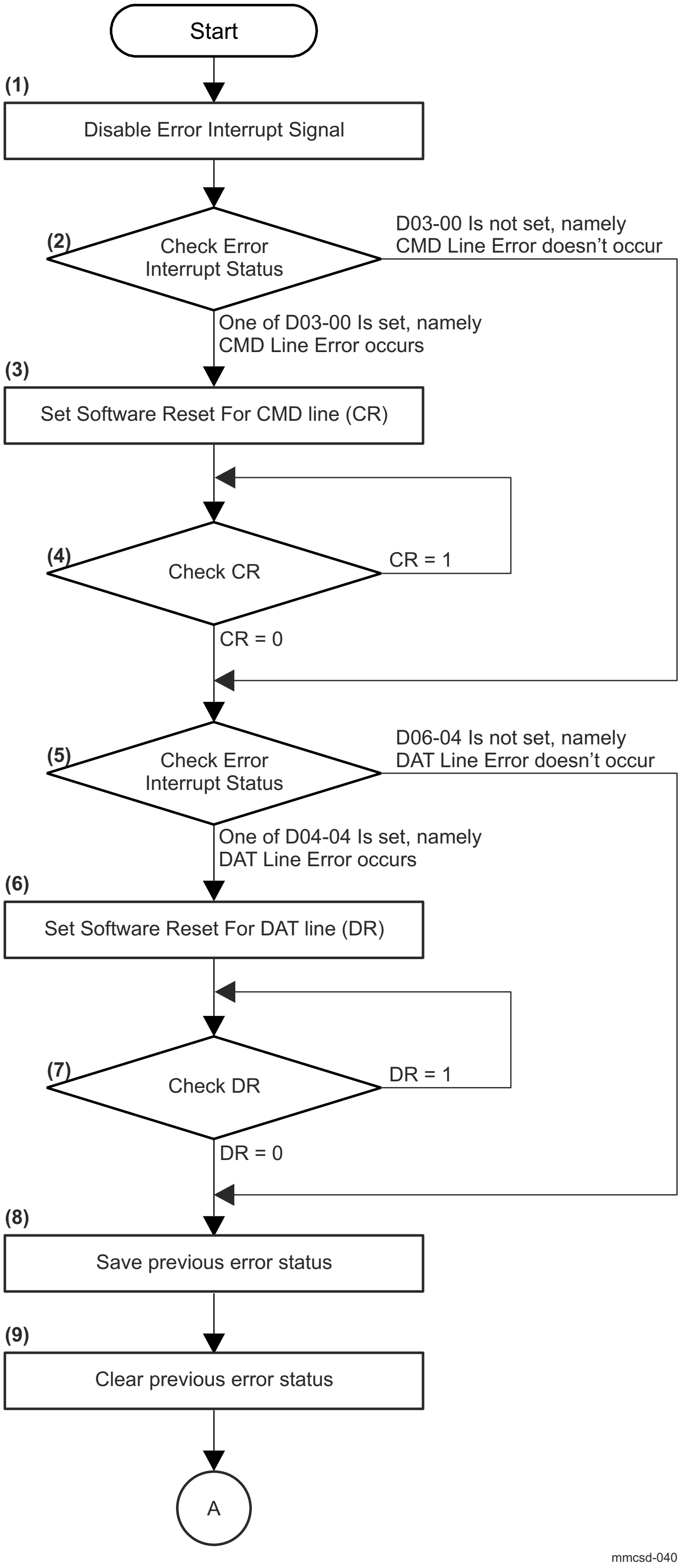

Figure 12-253. Error Interrupt Recovery Sequence (1)

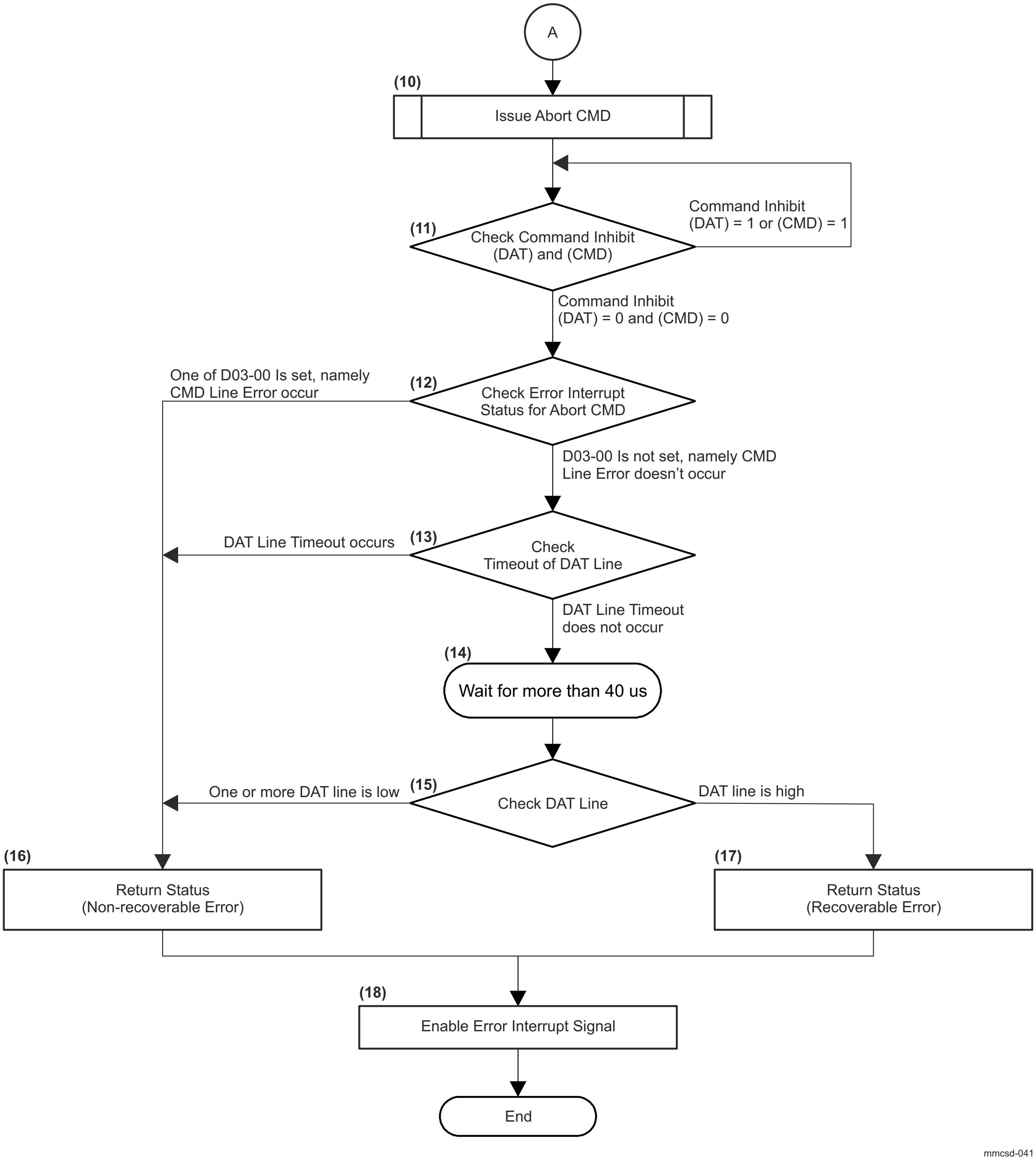

Figure 12-254. Error Interrupt Recovery Sequence (2)

(1) Disable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

(2) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D03-00) is set to 1, go to step (3). If none are set to 1 (all are 0), go to step (5).

(3) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1.

(4) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (5). If it is 1, go to step (4).

(5) Check bits D06-04 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D06-04) is set to 1, go to step (6). If none are set to 1 (all are 0), go to step (8).

(6) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(7) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (8). If it is 1, go to step (7).

(8) Save previous error status.

(9) Clear previous error status with setting them to 1.

(10) Issue Abort Command.

(11) MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until both MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit are set to 0.

(12) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register for Abort Command. If one of these bits is set to 1, go to step (16). If none of these bits are set to 1 (all are 0), go to step (13).

(13) Check MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If this bit is set to 1, go to step (16). If it is 0, go to step (14).

(14) Wait for more than 40 us.

(15) By monitoring the DAT [3:0] Line Signal Level in the MMCSD0_PRESENTSTATE register, judge whether the level of the DAT line is low or not. If one or more DAT lines are low, go to step (16). If the DAT lines are high, go to step (17).

(16) Return Status of "Non-recoverable Error".

(17) Return Status of "Recoverable Error".

(18) Enable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

12.4.5.5.1.10.2 Auto CMD12 Error Recovery

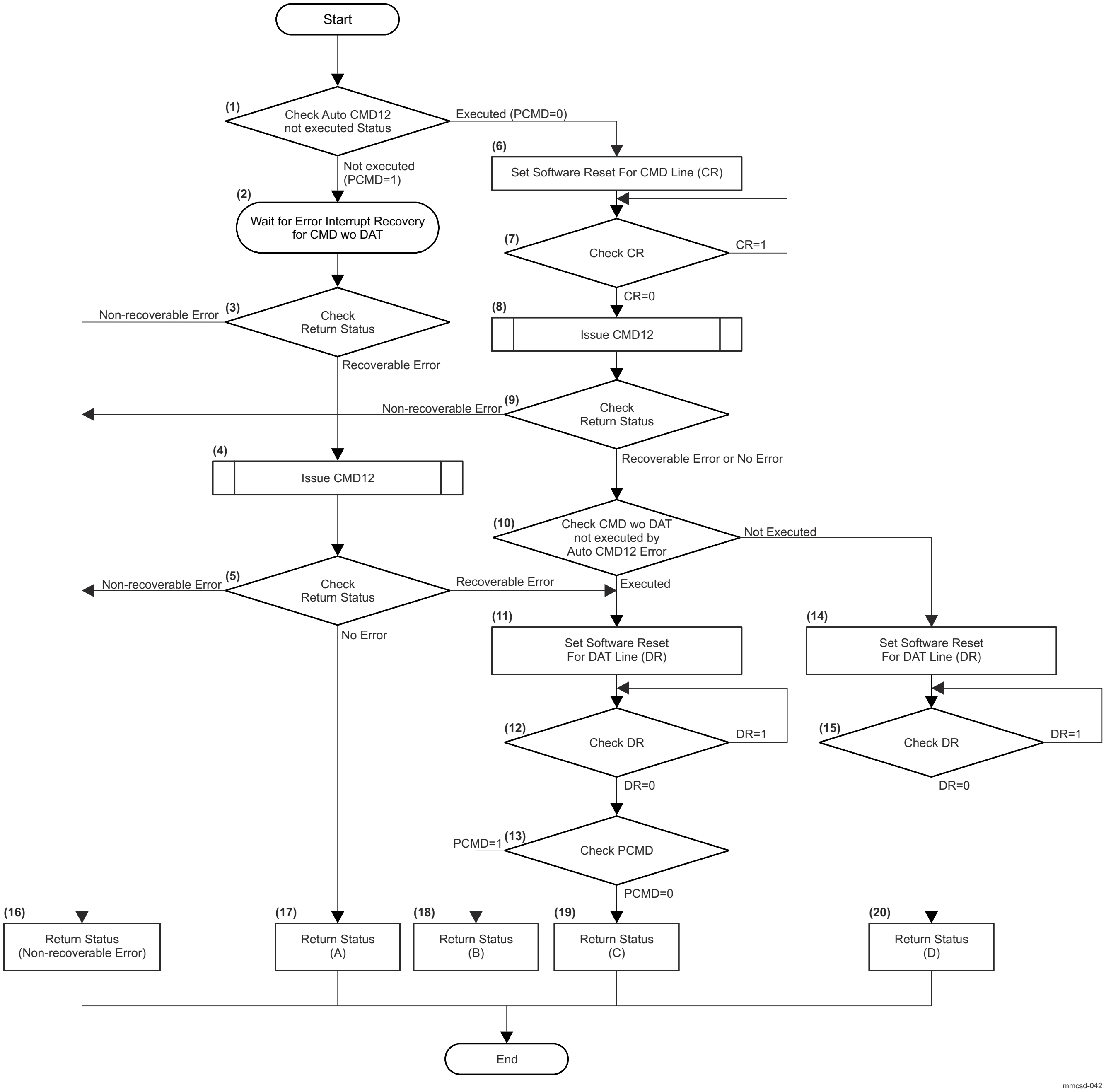

Figure 12-255. Auto CMD12 Error Recovery

The sequence for Auto CMD12 Error Recovery is shown in Figure 12-255. Following four cases A-D shall be covered.

A: An error occurred in CMD_wo_DAT, but not in the SD memory transfer.

B: An error occurred in CMD_wo_DAT, and also occurred in the SD memory transfer.

C: An error did not occur in CMD_wo_DAT, but an error occurred in the SD memory transfer.

D: CMD_wo_DAT was not issued, and an error occurred in the SD memory transfer.

(1) Check MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is set to 1, go to step (2). If this bit is set to 0, go to step (6). In addition, the Host Driver shall define PCMD flag, which changes to 1 if MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit is set to 1.

(2) Wait for Error Interrupt Recovery for CMD_wo_DAT.

(3) Check "Return Status". In the case of "Non-recoverable Error", go to step (16). In the case of "Recoverable Error", go to step (4).

(4) Issue CMD12 .

(5) If the CMD line errors occur for the CMD12 (one of D03-00 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Non-recoverable Error" and go to step (16). If not CMD line error and busy timeout error occur (D04 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Recoverable Error" and go to step (11). Otherwise, "Return Status" is "No error" and go to step (17).

(6) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 for software reset of the CMD line.

(7) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (8). If it is 1, go to step (7).

(8) Issue CMD12 . Acceptance of CMD12 depends on the state of the card. CMD12 may make the card to return to tran state. If the card is already in tran state, the card does not response to CMD12.

(9) Check "Return Status" for CMD12. If "Return Status" returns "Non-recoverable Error", go to step (16). In the case of "Recoverable Error" or "No error", go to step (10).

(10) Check the MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is 0, go to step (11). If it is 1, go to step (14).

(11) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(12) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (13). If it is 1, go to step (12).

(13) Check the PCMD flag. If PCMD is 1, go to step (18). If it is 0, go to step (19).

(14) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(15) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (20). If it is 1, go to step (15).

(16) Return Status of "Non-recoverable Error".

(17) Return Status that an error has occurred in CMD_wo_DAT, but not in the SD memory transfer.

(18) Return Status that an error has occurred in both CMD_wo_DAT, and the SD memory transfer.

(19) Return Status that an error has not occurred in CMD_wo_DAT, but has occurred in the SD memory transfer.

(20) Return Status that CMD_wo_DAT has not been issued, and an error has occurred in the SD memory transfer.

12.4.5.5.1.11 Wakeup Control (Optional)

After the Host System goes into standby mode, the Host System can resume from standby via a wakeup event initiated by one of the following three events:

(1) Interrupt from a SD card: If an SD card interrupt occurs, the Host System can resume from standby mode. If the Host System uses this wakeup factor, SD Bus power shall be kept on.

(2) Insertion of SD card: If a SD card is inserted, the Host System can resume from standby mode.

(3) Removal of SD card: If a SD card is removed, the Host System can resume from standby mode.

The sequence for preparing wakeup before the Host System goes into standby mode is shown in Figure 12-256.

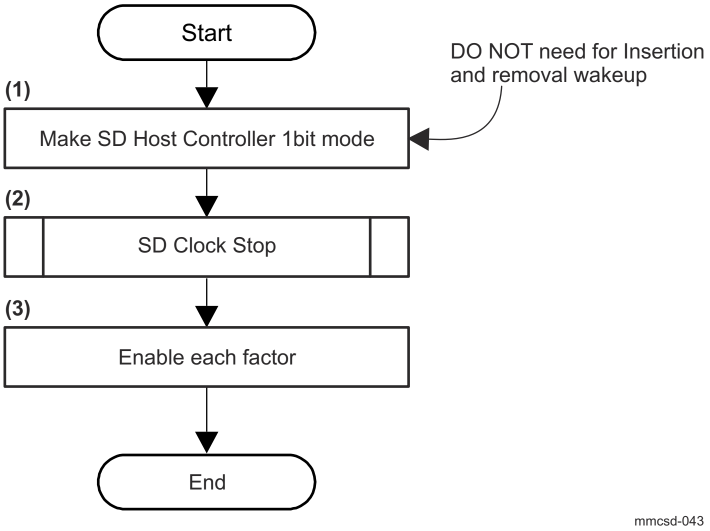

Figure 12-256. Wakeup Control before Standby Mode

(1) Set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 0.

(2) Execute SD Clock Stop Sequence as described in Section 12.4.5.5.1.2.2 , *SD Clock Supply and Stop Sequence*.

(3) Clear the MMCSD0_NORMAL_INTR_STS register and the MMCSD0_NORMAL_INTR_SIG_ENA register, and then set the enable bits of each wakeup event factor to 1 in the MMCSD0_WAKEUP_CONTROL register and set the bits of MMCSD0_ERROR_INTR_STS_ENA register to use wakeup.

The sequence for wakeup once in standby mode is shown in Figure 12-257.

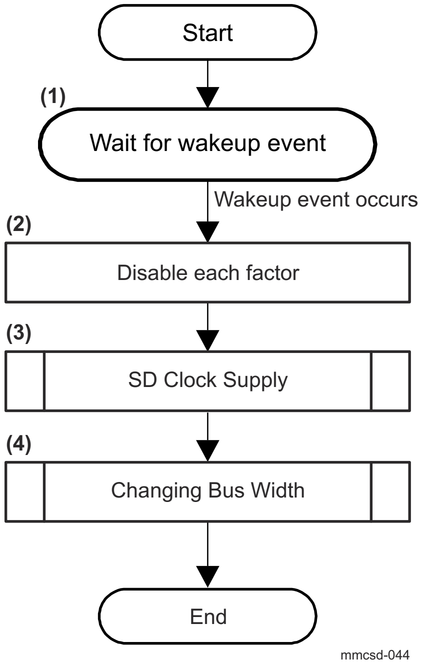

Figure 12-257. Wakeup from Standby

(1) Wait for wakeup event.

(2) Set the enable bits of each wakeup event factor to 0 in the MMCSD0_WAKEUP_CONTROL register and then clear event statuses in the MMCSD0_NORMAL_INTR_STS register. If necessary, set the MMCSD0_NORMAL_INTR_SIG_ENA register.

(3) Execute SD Clock Supply Sequence (see Section 12.4.5.5.1.2.2 , *SD Clock Supply and Stop Sequence*).

(4) Set the SD Bus width (see Section 12.4.5.5.1.4 , *Changing Bus Width*).

12.4.5.5.1.12 Suspend/Resume (Optional, Not Supported from Version 4.00)

If a SD card supports suspend and resume functionality, then the Host Controller can initiate suspend and resume. It is necessary for both the Host Controller and the SD card to support the function of "Read Wait". ADMA operation does not support this function.

12.4.5.5.1.12.1 Suspend Sequence

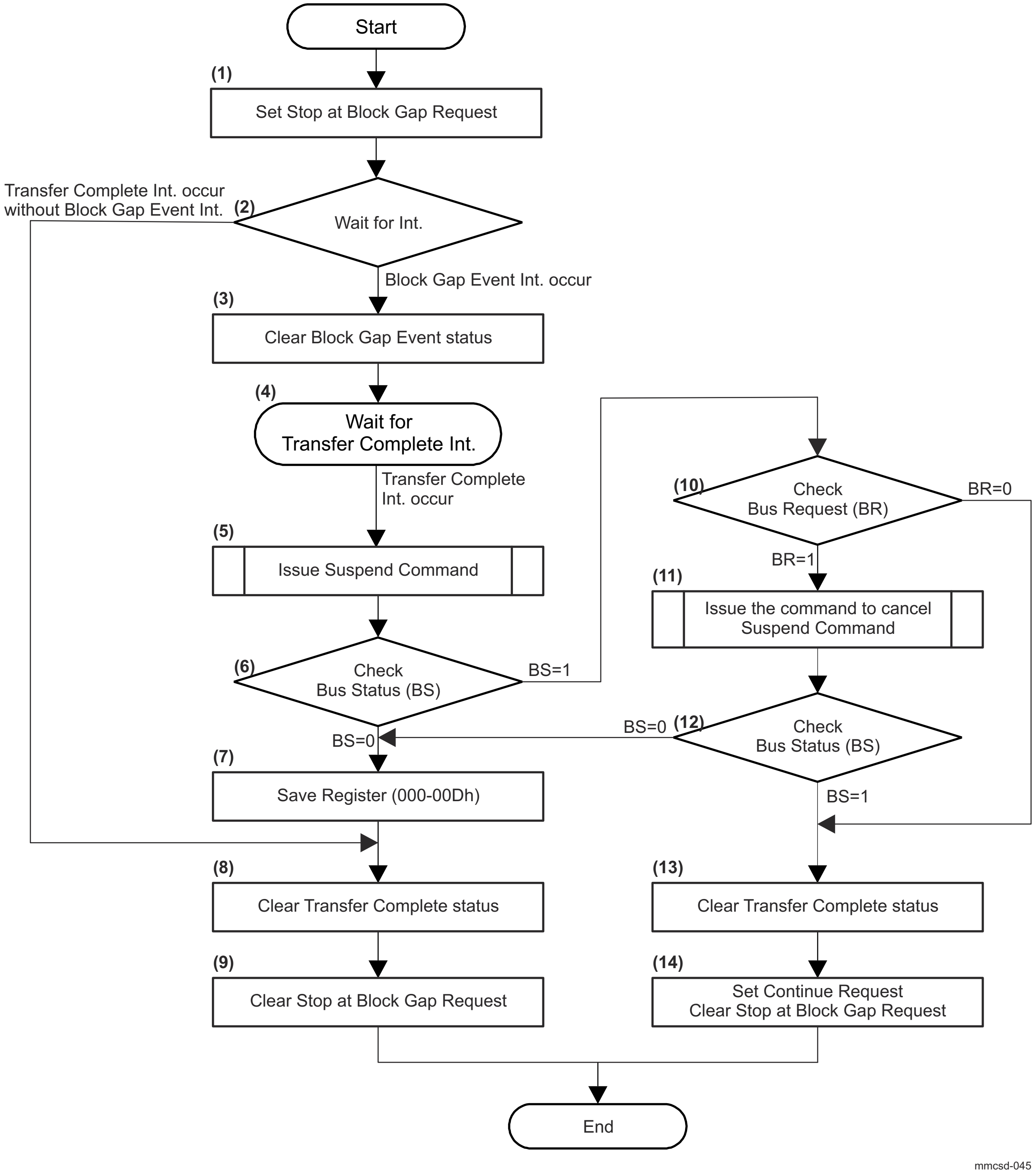

Figure 12-258. The Sequence for Suspend

(1) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop the SD transaction.

(2) Wait for an Interrupt. If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 0 and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1, go to step (8). If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 1, go to step (3).

(3) Set MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit to 1 to clear this bit.

(4) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(5) Issue the Suspend Command in accordance with Section 12.4.5.5.1.7.1 , *Transaction Control without Data Transfer Using DAT Line*.

(6) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (10).

(7) Save the register .

(8) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(9) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 0 to clear this bit.

(10) Check the BR value of the response data. If BR is 1, go to step (11). If BR is 0, go to step (13).

(11) Issues the command to cancel the previous suspend command in accordance with Section 12.4.5.5.1.7.1 , *Transaction Control without Data Transfer Using DAT Line*.

(12) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (13).

(13) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(14) Set MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 to continue the transaction. At the same time, write 0 to MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to clear this bit.

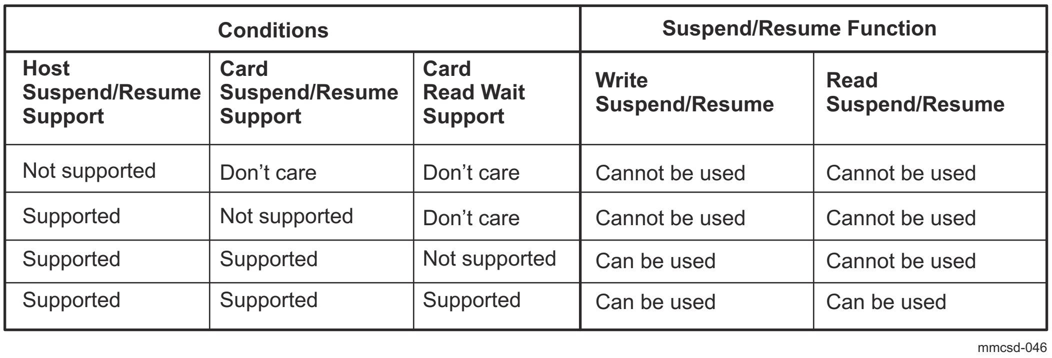

Conditions			Suspend/Resume Function	
Host Suspend/Resume Support	**Card Suspend/Resume Support**	**Card Read Wait Support**	**Write Suspend/Resume**	**Read Suspend/Resume**
Not supported	Don't care	Don't care	Cannot be used	Cannot be used
Supported	Not supported	Don't care	Cannot be used	Cannot be used
Supported	Supported	Not supported	Can be used	Cannot be used
Supported	Supported	Supported	Can be used	Can be used

Figure 12-259. Suspend/Resume Condition

12.4.5.5.1.12.2 Resume Sequence

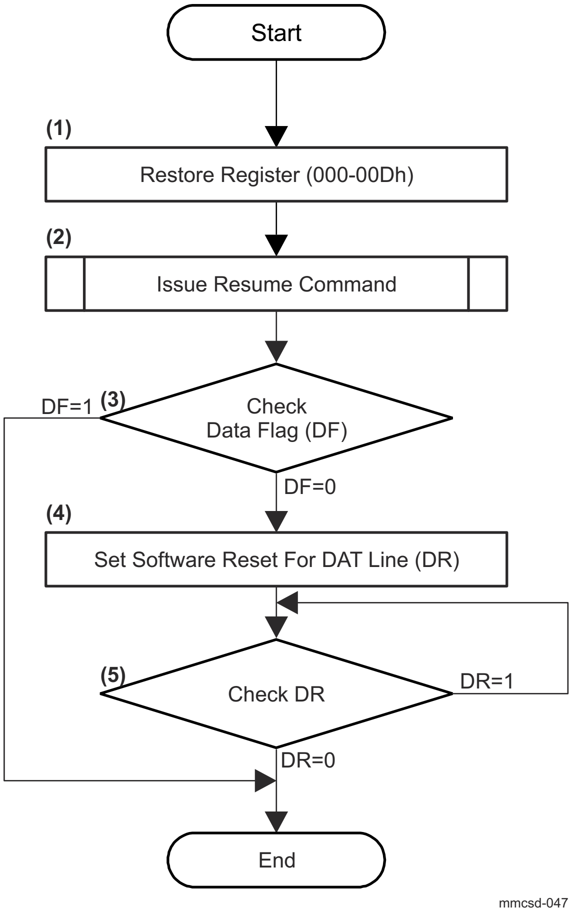

Figure 12-260. The Sequence for Resume

(1) Restore the register .

(2) Issue the Resume Command .

(3) Check the DF value of the response data. If DF is 0, go to step (4). If DF is 1, go to "End".

(4) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(5) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to "End". If it is 1, go to step (5).

12.4.5.5.1.12.3 Stop At Block Gap/Continue Timing for Read Transaction

The timing of Stop At Block Gap Request and Continue Request. The Transfer Complete interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is always generated by setting MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit where data transfer is stopped. However, generation of the Block Gap Event interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is dependent on whether the last data block is sent or not. Block Gap Event is not generated If all data blocks are transferred (the last block is transferred). It is not necessary to enable Block Gap Event interrupt. The status can be checked when transfer complete interrupt is detected. It is not necessary to use Continue Request (MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE) if Block Gap Event status is not set because there is no further data to be transferred. If Read Wait is not supported, Host Controller stops SD Clock at the block gap.

Implementation Note:

The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL, MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE, MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bits shall be set and cleared by the Host Controller.

The MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set and cleared by the Host Driver. The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit shall be set by the Host Driver and be cleared by the Host Controller. The MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit shall be set by the Host Controller and be cleared by the Host Driver.

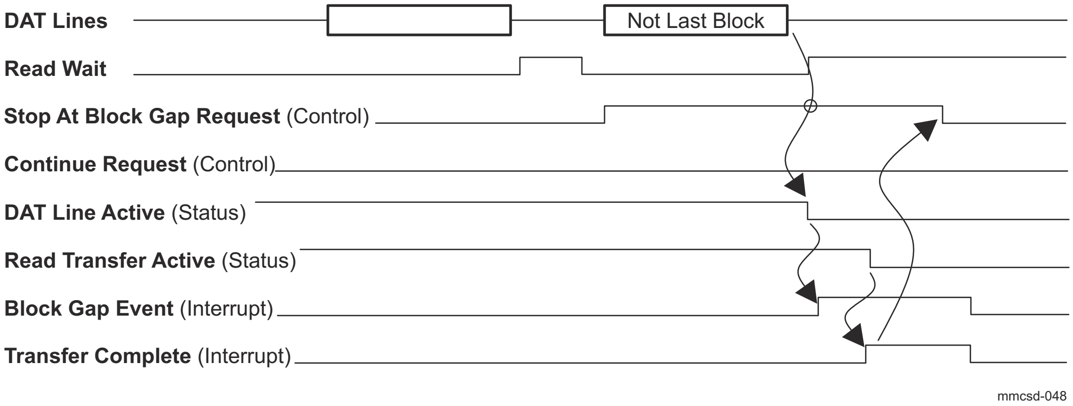

Figure 12-261. Wait Read Transfer by Stop At Block Gap Request

The Host Controller can accept a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP) when all the following conditions are met.

(1) It is at the block gap.

(2) The Host Controller can assert read wait or it is already asserted.

(3) The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is set to 1.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit:

(1) Clear MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE).

(3) After accepting MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit, clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

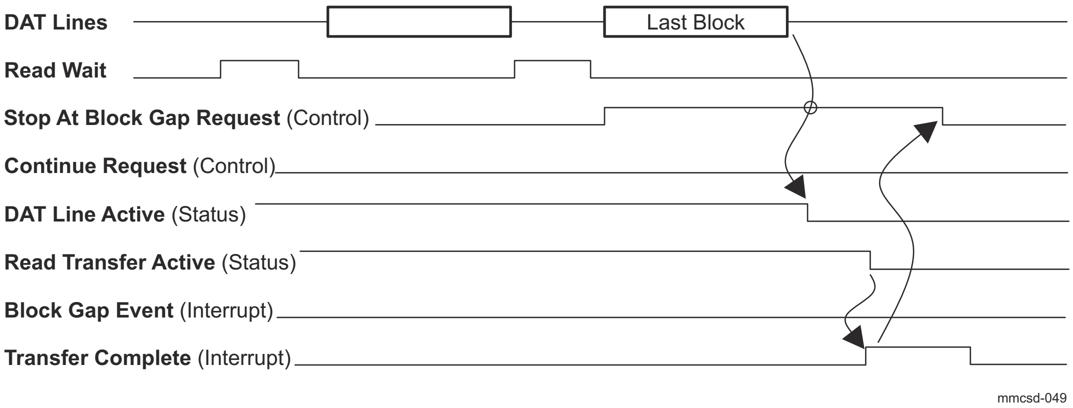

Figure 12-262. Stop At Block Gap Request is Not Accepted at the Last Block of the Read Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and stops the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit status is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

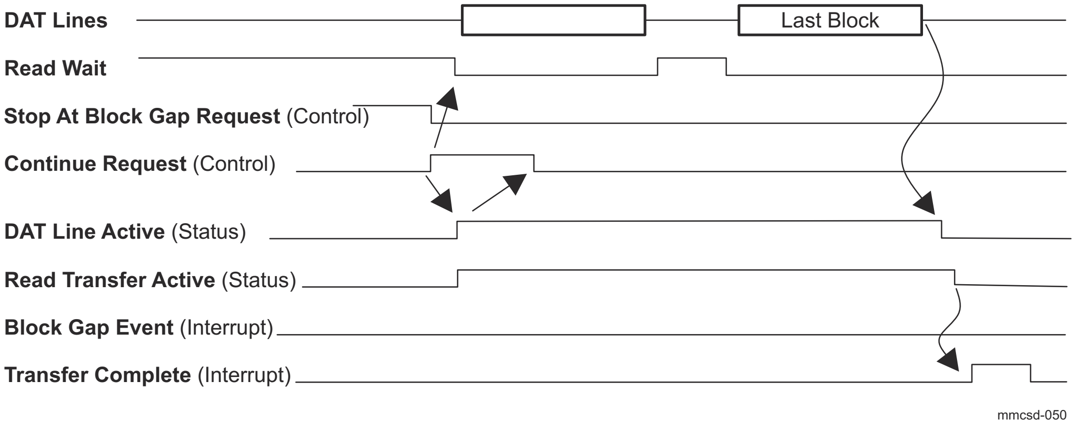

Figure 12-263. Continue Read Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Release MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit (if the data block can accept the next data).

(2) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit.

(3) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (2).

The end of the read transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and do not generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.4.5.5.1.12.4 Stop At Block Gap/Continue Timing for Write Transaction

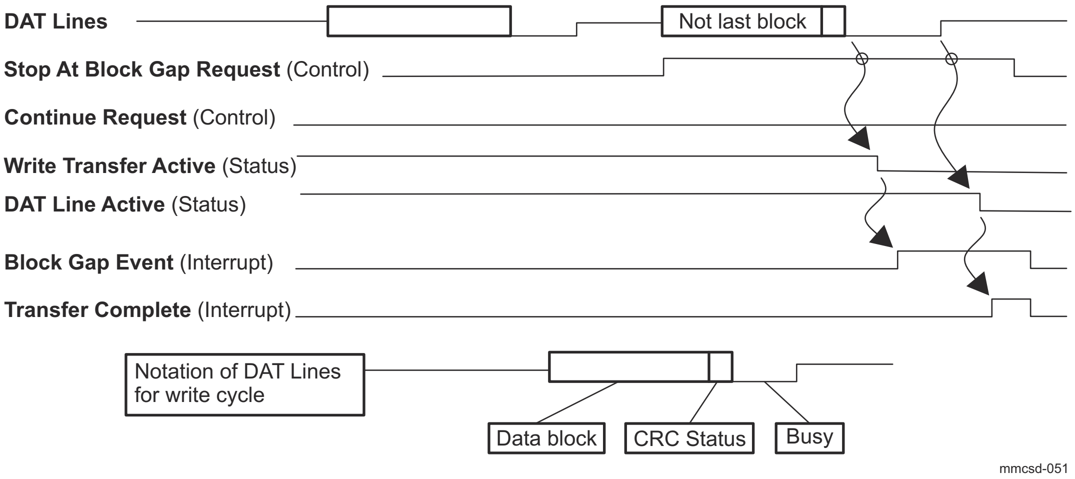

Figure 12-264. Wait Write Transfer by Stop At Block Gap Request

The Host Controller can accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit when matches all following conditions:

(1) It is at the block gap.

(2) No valid write data remains in the Host Controller.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

(3) After accepting the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit), clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

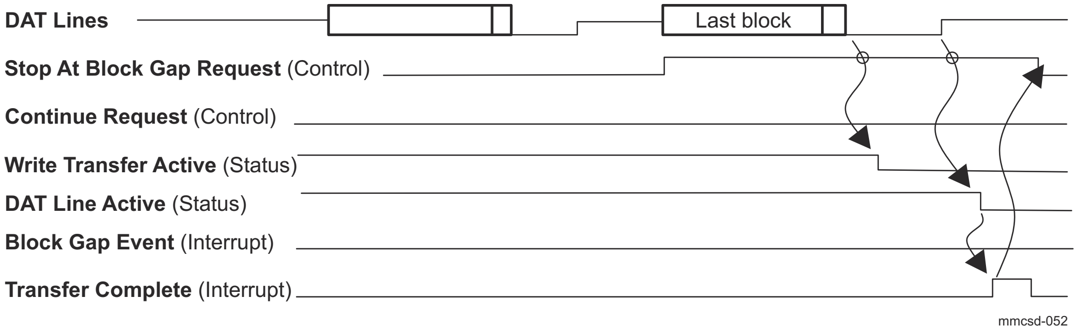

Figure 12-265. Stop At Block Gap Request is Not Accepted at the Last Block of the Write Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and terminates the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer

Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN bit is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

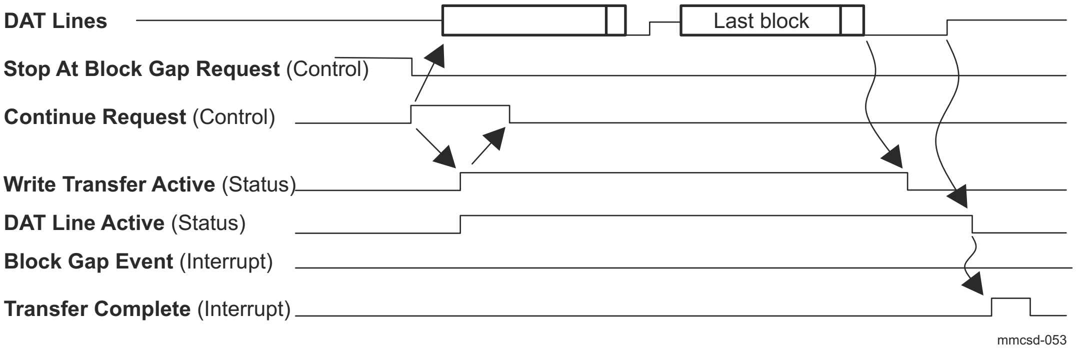

Figure 12-266. Continue Write Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit.

(2) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (1).

The end of transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit, and do not generate the (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generates the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.4.5.5.2 Driver Flow Sequence

Note

UHSII is not supported. For more information, see *Not Supported Features*.

12.4.5.5.2.1 Host Controller Setup and Card Detection

12.4.5.5.2.1.1 Host Controller Setup Sequence

Figure 12-267 and Table 12-247 show a Host Controller setup sequence.

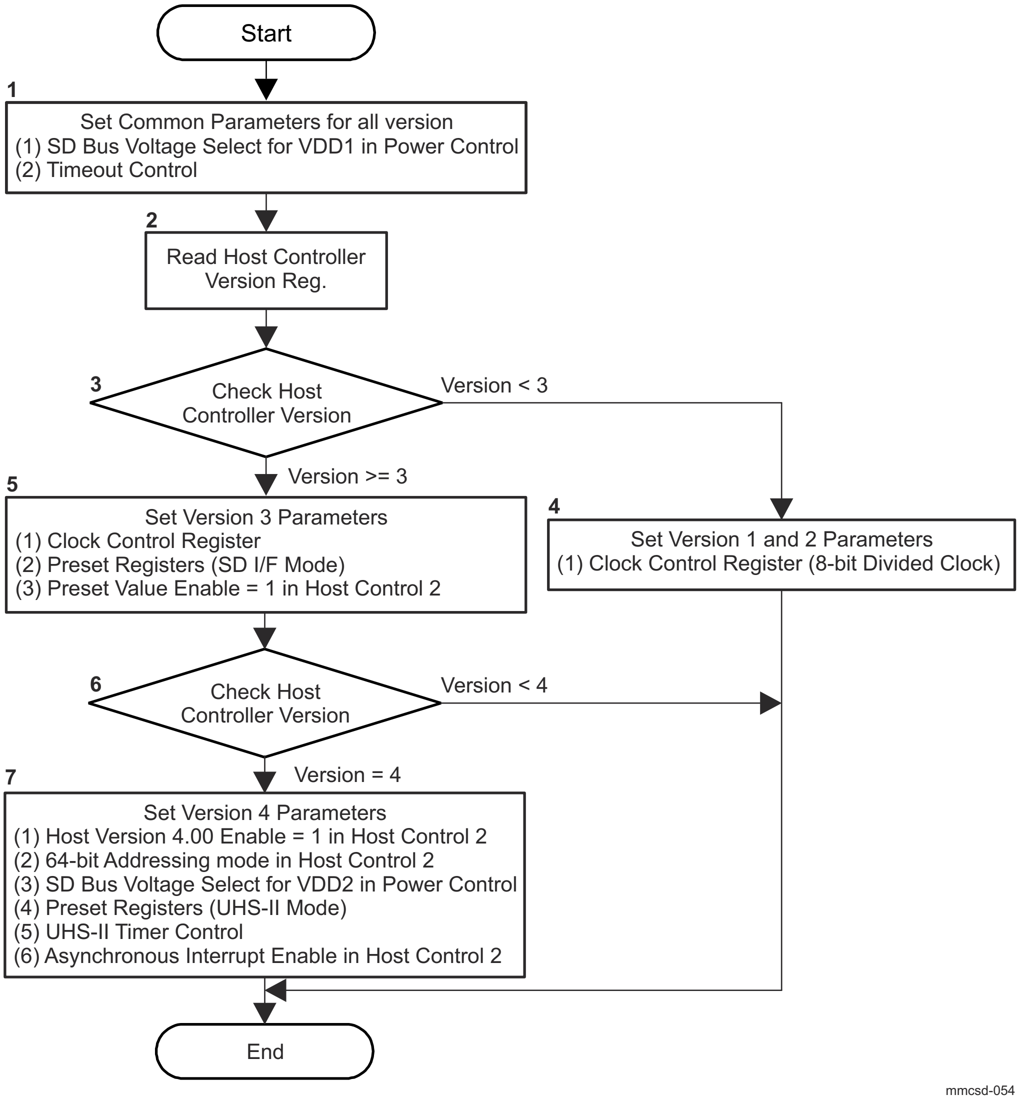

Figure 12-267. Host Controller Setup Sequence

Table 12-259. Host Controller Setup Sequence

Step	Description
1	Set parameters for all Host Controller version. Set the MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE and MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit fields.
2	Read the MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM bit field.
3	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is less than version 3, go to step (4), if it is version 3 or later go to step (5).

Table 12-259. Host Controller Setup Sequence (continued)

Step	Description
4	Set the MMCSD0_CLOCK_CONTROL register using 8-bit Divided Clock mode.
5	Set Version 3 parameters. The MMCSD0_CLOCK_CONTROL register is sets in 10-bit Divided Clock Mode or Programmable Clock Mode. If Clock Multiplier in the MMCSD0_CAPABILITIES register is not zero, Programmable Clock Mode should be used. If Preset Value is used, set Preset Values of SD I/F Modes in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit to 1.
6	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is version 4, go to step (7), if it is less than version 4, exits.
7	Set Version 4 parameters. Set the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit to 1. If the MMCSD0_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit is set to 1, set the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit to 1. If UHS-II Support is set to 1 and 1.8 V VDD2 Support is set to 1 in the MMCSD0_CAPABILITIES register, set SD Bus Voltage Select for VDD2 to 1.8 V mode in the MMCSD0_POWER_CONTROL register, set preset value for UHS-II Mode to Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set Timeout Counter Value for CMD_RES and Timeout Counter Value for Deadlock in the MMCSD0_UHS2_TIMER_CONTROL register based on Timeout Clock Frequency and Timeout Clock Unit in the MMCSD0_CAPABILITIES register. If Asynchronous Interrupt Support in the MMCSD0_CAPABILITIES register is set to 1, set Asynchronous Interrupt Enable to 1 in the MMCSD0_HOST_CONTROL2 register.

12.4.5.5.2.1.2 Card Interface Detection Sequence

This procedure is invoked by the Card Insertion interrupt. Figure 12-268 and Table 12-248 show a card interface detection sequence.

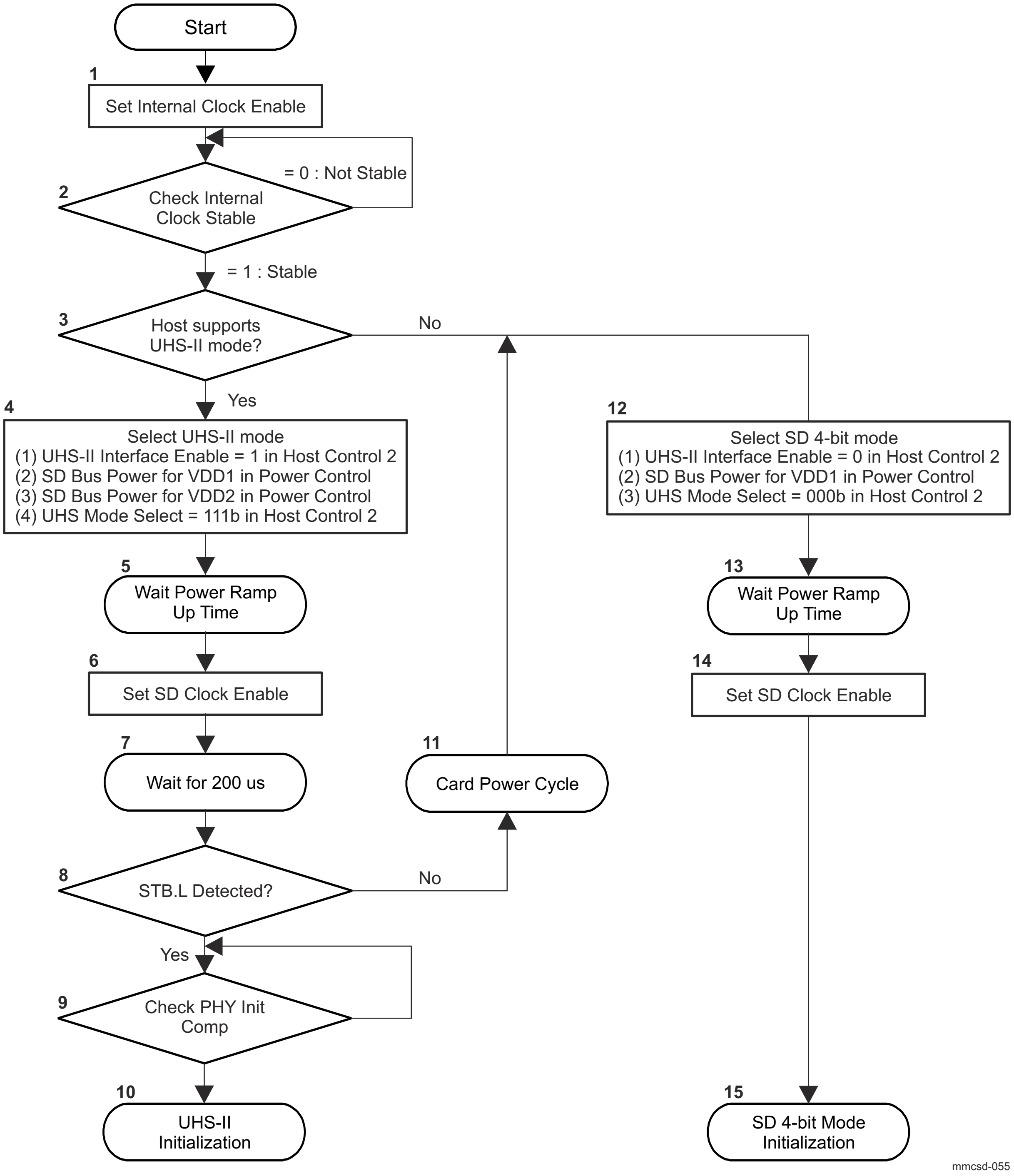

Figure 12-268. Card Interface Detection Sequence

Table 12-260. Card Interface Detection Sequence

Step	Description
1	Set Internal Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
2	Wait until Internal Clock Stable is set to 1 in the MMCSD0_CLOCK_CONTROL register.
3	If Host Supports UHS-II, go to step (4) else go to step (12).
4	Try to initialize a card to UHS-II mode. Set UHS-II Interface Enable to 1 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 and SD Bus Power for VDD2 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 111b in the MMCSD0_HOST_CONTROL2 register.

Table 12-260. Card Interface Detection Sequence (continued)

Step	Description
5	Wait power ramp up time. It is dependent on a Host System.
6	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
7	Wait 200 µs to check a card supports UHS-II mode.
8	Check STB.L Detection in the MMCSD0_PRESENTSTATE register. If UHS-II IF is detected, go to step (9). If UHS-II IF is not detected, go to step (11).
9	Wait until Lane Synchronization in the MMCSD0_PRESENTSTATE register is set to 1 (PHY Initialization is completed).
10	Perform UHS-II initialization.
11	Perform card power cycle.
12	Try to initialize a card to SD 4-bit mode. Set UHS-II Interface Enable to 0 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 000b in the MMCSD0_HOST_CONTROL2 register.
13	Wait power ramp up time. It is dependent on a Host System.
14	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
15	Perform SD 4-bit mode initialization. Refer to Section 12.4.5.5.1.6 , *Card Initialization and Identification (for SD I/F)*.

12.4.5.5.2.2 Boot Operation

The boot operation sequence is shown in Figure 12-269.

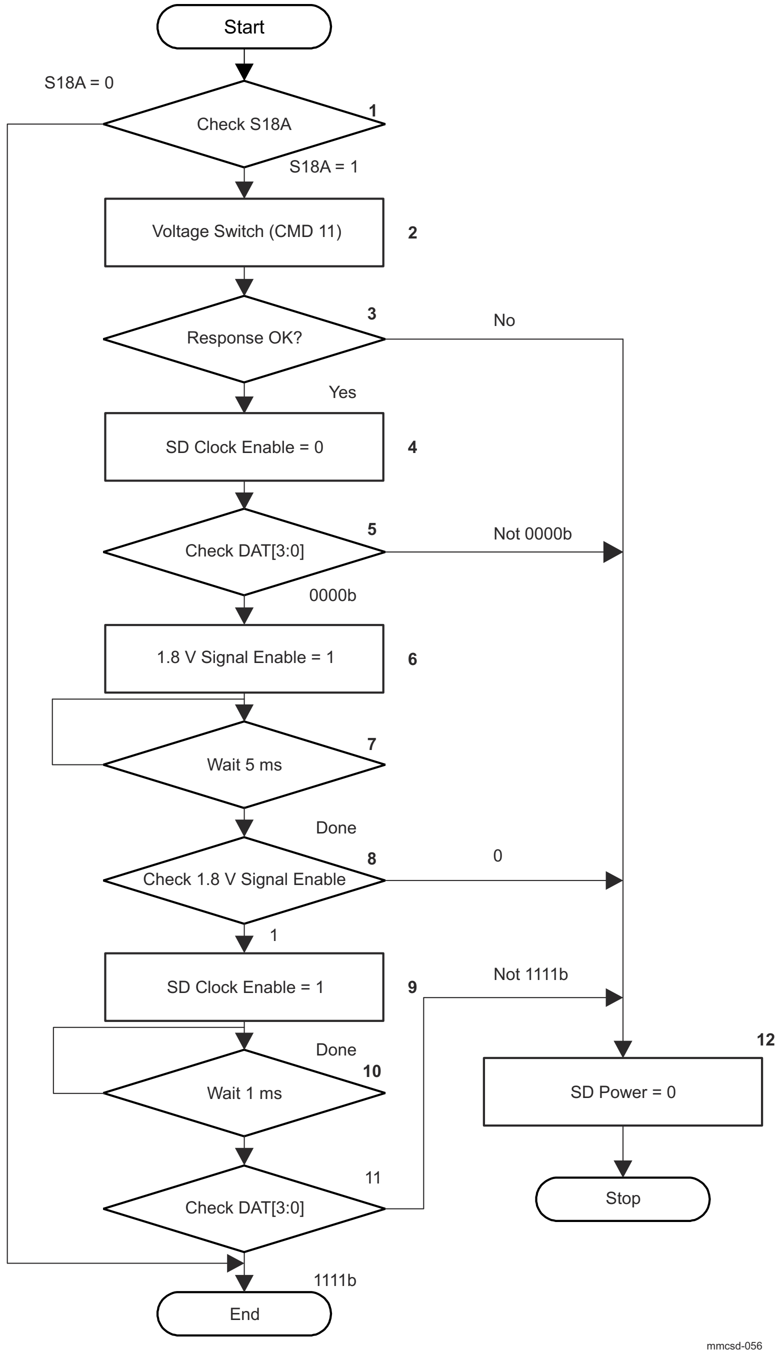

Figure 12-269. Boot Operation Sequence

12.4.5.5.2.2.1 Normal Boot Operation: (For Legacy eMMC 5.0)

The Host driver writes the boot timeout value into MMCSD0_BOOT_TIMEOUT_CONTROL register as per the eMMC4.3+ spec.

When the Host driver sets the "BOOT_ENABLE" to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit to "1" in MMCSD0_TRANSFER_MODE register, the Host controller drives the CMD line to "0" for boot operation.

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver

(MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK). If the Host controller doesn't receive the boot acknowledgement from the device within the timeout value, the Host controller will assert the data timeout error interrupt (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

After servicing the boot acknowledge interrupt or data timeout error interrupt, the driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The Host controller terminates the boot operation when the programmed number of blocks is transferred to the System. The Driver can writes "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can also be terminated in between the boot transfer (the Driver can set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, the Host controller asserts soft reset for CMD line and DATA line internally once the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE), to reset all the state machines to idle state.

There is no need to perform error recovery sequence in case data timeout interrupt occurs during boot operation (ignore sending abort command, soft reset and just clear the timeout interrupt and proceed with the boot flow).

If the device sends wrong acknowledgement to the Host, the Host controller will assert Data CRC Error interrupt (MMCSD0_ERROR_INTR_STS[5] DATA_CRC) on the Driver. In this case, the Host driver has to stop the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller will assert Data End Bit Error interrupt (MMCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver.

The Host driver stops the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation. If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.4.5.5.2.2.2 Alternate Boot Operation (For Legacy eMMC 5.0):

The Host driver writes the boot timeout value as per the eMMC4.3+ spec into MMCSD0_BOOT_TIMEOUT_CONTROL register.

If the "ALT_BOOT_MODE" and "BOOT_ENABLE" is set to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit is set to 1 in MMCSD0_TRANSFER_MODE register, the host controller drives the CMD0 (0xFFFFFFFA) on the CMD line.

The system shall wait for command complete interrupt before "RCV_BOOT_ACK" interrupt (MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK).

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The System needs to send CMD0 to inform the device about the boot operation complete. The system shall program MMCSD0_COMMAND register with argument "00000000h" for the CMD0 and waits for command complete.

The Host controller terminates the boot operation when the programmed number of blocks are transferred to the System and the Driver shall send CMD0 to eMMC card and then program "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can be terminated at any time (the Driver can send CMD0 and set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, all state machines in the Host controller need to move to IDLE state. The Host controller asserts the soft reset for CMD and data line internally when the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE) and all the state machine goes to the idle state.

If the Host controller doesn't receive the acknowledgement from the device with in timeout value the Host controller will assert the data timeout error interrupt (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

The driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

There is no need to perform error recovery sequence in case of data timeout interrupt as mentioned above. If the device sends wrong acknowledgement to the Host, then Host controller will assert Data CRC Error interrupt to the Driver (MMCSD0_ERROR_INTR_STS[5] DATA_CRC). The Host driver has to stop the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller asserts Data End Bit Error interrupt (MMCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver. The Host driver stops the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation . If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.4.5.5.2.2.3 Boot Code Chunk Read Operation (For Legacy eMMC 5.0):

The following figure explains the boot code read done as chunks of data (the Driver can read the boot data as 2K, 4K, 1K and 8K etc. instead of 128K at a time

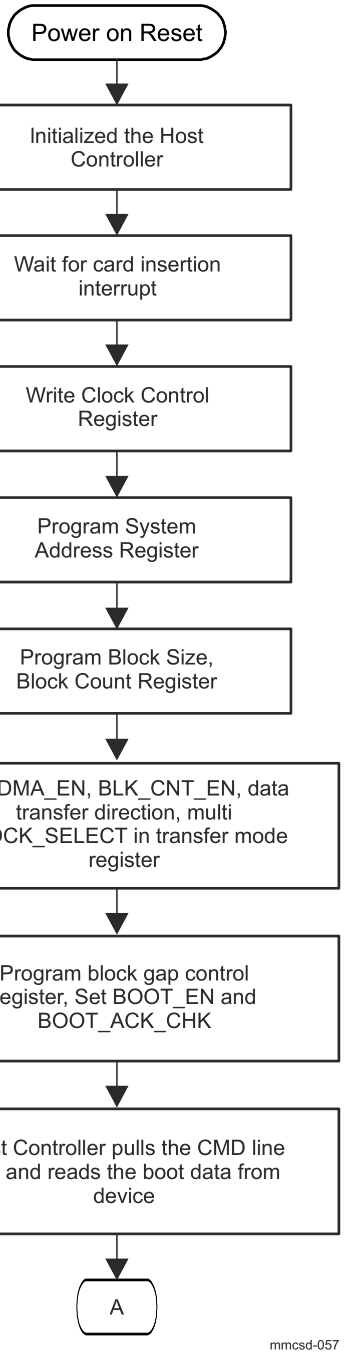

Figure 12-270. Boot Code Access Flow Diagram (1)

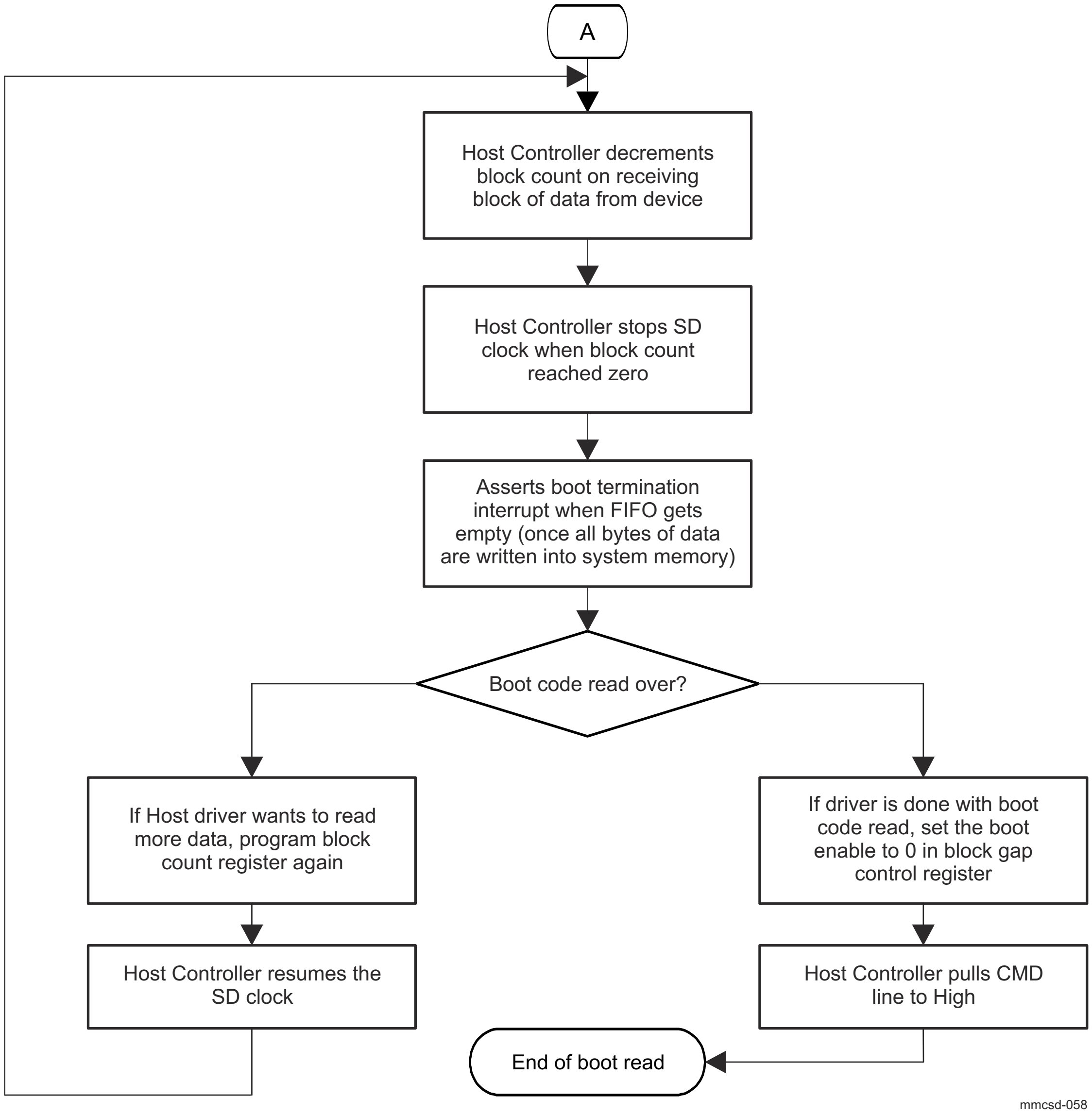

Figure 12-271. Boot Code Access Flow Diagram (2)

12.4.5.5.2.3 Retuning procedure (For Legacy Interface)

12.4.5.5.2.3.1 Sampling Clock Tuning

The SD bus can be operating in high clock frequency mode and then the data window from the card on CMD and DAT[3:0] lines gets smaller. The position of the data window will vary depending on the card and host system implementation. Therefore, the Host Controller shall support a tuning circuit when SDR104 or SDR50.

The Host Controller shall support a tuning circuit when SDR104 or SDR50 (if Use Tuning for SDR50 is set to 1 in the MMCSD0_CAPABILITIES register) is supported by executing the tuning procedure and adjusting the sampling clock. Execute Tuning and Sampling Clock Select in the MMCSD0_HOST_CONTROL2 register are used to control the tuning circuit.

See MMC SW Tuning Algorithm for more information.

12.4.5.5.2.3.2 Tuning Sequence

The Figure 12-272 defines sampling clock tuning procedure supported by Host Controller. In default, for lower frequency operation, fixed sampling clock is used to receive signals on CMD and DAT[3:0]. Before using

SDR104, sampling clock tuning is required. Start of sampling clock tuning is requested by setting Execute Tuning to 1 and Sampling Clock Select to 0.

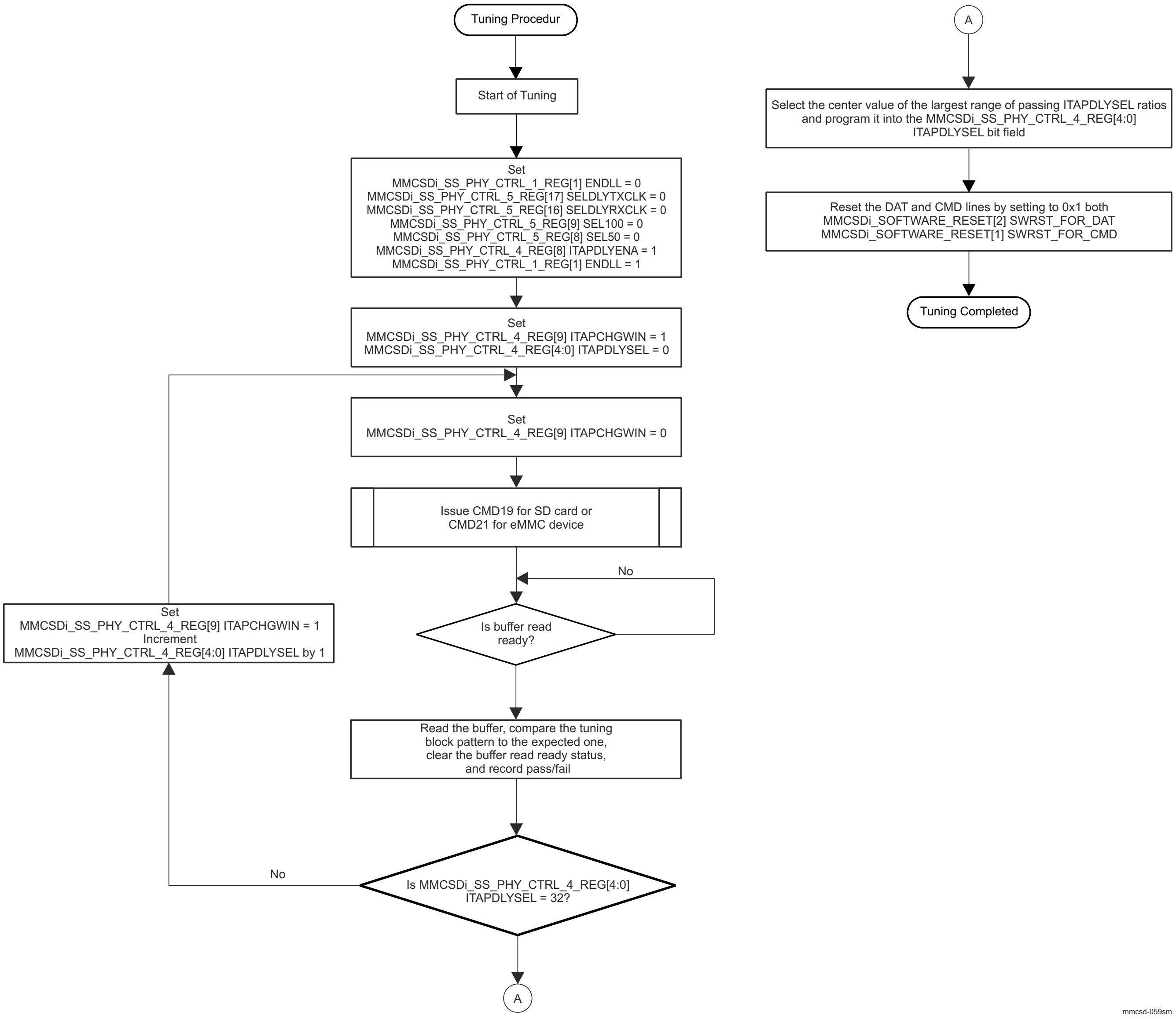

Figure 12-272. MMCSD Clock Tuning

Host driver issue CMD19 repeatedly until the host controller resets Execute Tuning to 0. Host Controller resets Execute Tuning to 0 when tuning is completed or tuning is not completed within 40 times. Host Driver can abort this loop by 40 times CMD19 issue or 150 ms time-out.

If tuning is completed successfully, Host Controller set Sampling Clock Select to 1 and this means the Host Controller start to use tuned sampling clock. If tuning is failed, Host Controller keeps Sampling Clock Select to 0. By writing Sampling Clock Select to 0, sampling clock is switched from tuned sampling clock to fixed sampling clock. Re-tuning time would be smaller than the first tuning time. CMD19 response errors are not indicated while tuning is performed.

The clock tuning tap delay values are selected using Variable sampling point detection. Fixed tap delay value is used for fixed tuning clock method.

12.4.5.5.2.3.3 Re-Tuning Modes

The re-tuning timing is specified by two methods: Re-Tuning Request generated by Host Controller and expiration of a re-tuning timer prepared by Host Driver.

(1) Re-Tuning Mode 1 The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4 MB.

(2) Re-Tuning Mode 2 The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4 MB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled.

12.4.5.5.2.4 Command Queuing Driver Flow Sequence

12.4.5.5.2.4.1 Command Queuing Initialization Sequence

Figure 12-273 and Table 12-249 show a Command Queuing initialization sequence.

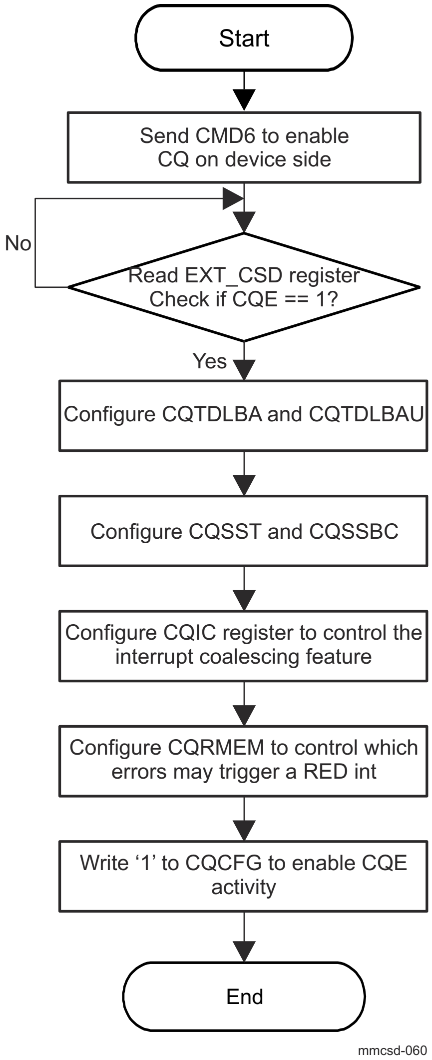

Figure 12-273. Command Queuing Initialization Sequence

Table 12-261. Command Queuing Initialization Sequence

Step	Description
1	Initialize and enable Command Queueing in the device.
2	Configure Task Descriptor size in MMCSD0_CQ_CONFIG register.
3	Configure MMCSD0_CQ_TDL_BASE_ADDR and MMCSD0_CQ_TDL_BASE_ADDR_UPBITS registers to point to the memory location allocated to the TDL in host memory.
4	Configure CQSST and CQSSBC to control when SEND_QUEUE_STATUS commands are sent to the device by CQE.
5	Configure MMCSD0_CQ_INTR_COALESCING register to control the interrupt coalescing feature: enable/disable, set interrupt count and timer protection.
6	Configure MMCSD0_CQ_RESP_ERR_MASK register to control which errors may trigger a RED interrupt (if different from reset values).
7	Write '1' to MMCSD0_CQ_CONFIG register to enable CQE activity.

12.4.5.5.2.4.2 Task Issuance Sequence

Figure 12-274 and Table 12-250 show a task issuance sequence.

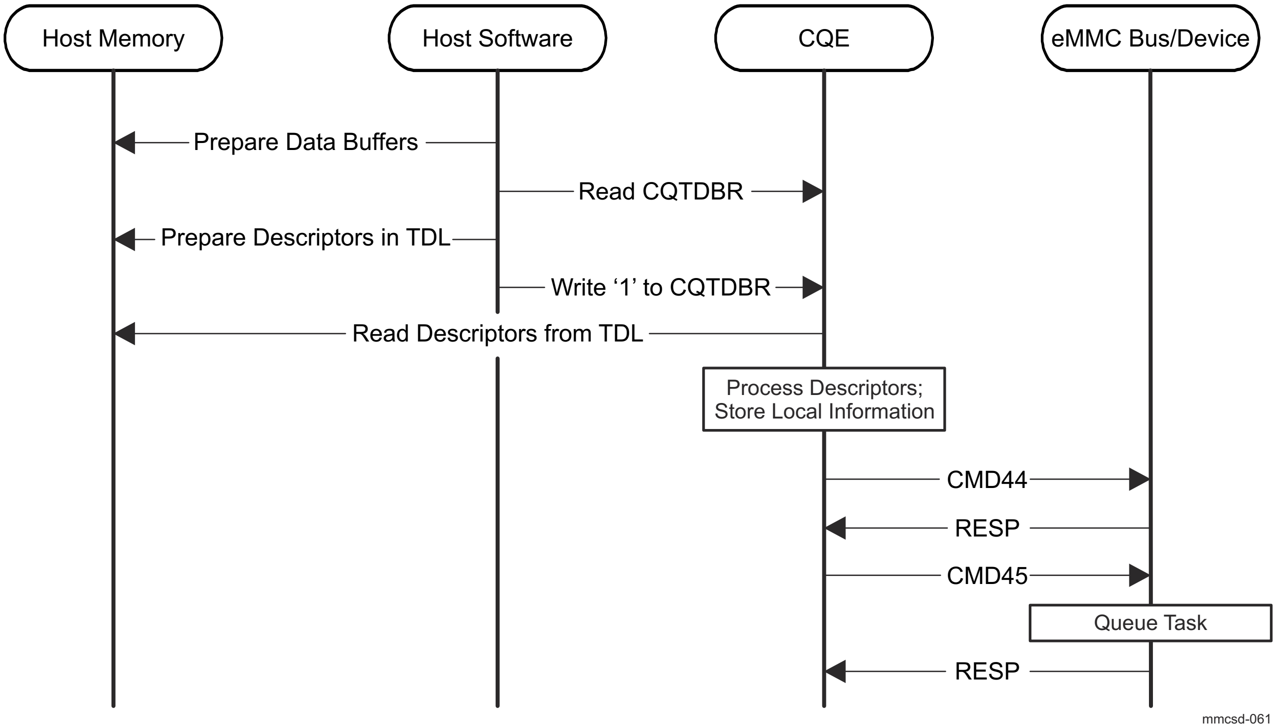

Figure 12-274. Task Issuance Sequence

Table 12-262. Task Issuance Sequence

Step	Description
1	Find an empty transfer request slot by reading the MMCSD0_CQ_TASK_DOOR_BELL register. An empty transfer request slot has its respective bit cleared to '0' in the MMCSD0_CQ_TASK_DOOR_BELL register.

Table 12-262. Task Issuance Sequence (continued)

Step	Description
2	Build a Task Descriptor at the 1st entry of the empty slot. Task Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, as required for Task Descriptors. • 3. Int = 1, if an interrupt on completion is required. Otherwise, Int = 0. • 4. Act = b101, to indicate a Task Descriptor . • 5. Data Direction = 1 for read commands, and 0 for write commands. • 6. Priority = 1 for high priority, and 0 for simple requests. • 7. QBR = 1 if Queue Barrier functionality is required. 0 otherwise. • 8. Forced Programming, Context ID, Tag Request, Reliable Write, Block Count, and Block Address programmed according to application requirements.
3	Build a Transfer Descriptor at the 2nd entry of the empty slot. Transfer Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, if a TRAN descriptor is used, to indicate the task only has one data buffer. End = 0 if LINK descriptor is used. • 3. Int = 0. Ignore in Command queueing. • 4. Act = b100, for TRAN descriptors, pointing directly to the task's single data buffer. Act = 401 b110, for LINK descriptors, point to a scatter/gather list (indirect). • 5. Address and Length programmed according to the data buffer supplied by the application.
4	If more than one transfer is requested, repeat step 1-3 for all needed transfers.
5	Set MMCSD0_CQ_TASK_DOOR_BELL register to indicate to the CQE that one or more transfer requests are ready to be sent to the attached device. Host software shall only write a '1' to the bit position that corresponds to new tasks; all other bit positions within MMCSD0_CQ_TASK_DOOR_BELL register should be written with a '0', which indicates no change to their current values.

12.4.5.5.2.4.3 Task Execution and Completion Sequence

The CQE is responsible for task execution, communication with the device and moving the data to the buffers in the host memory.

Figure 12-275 and Table 12-251 show a task execution and completion sequence.

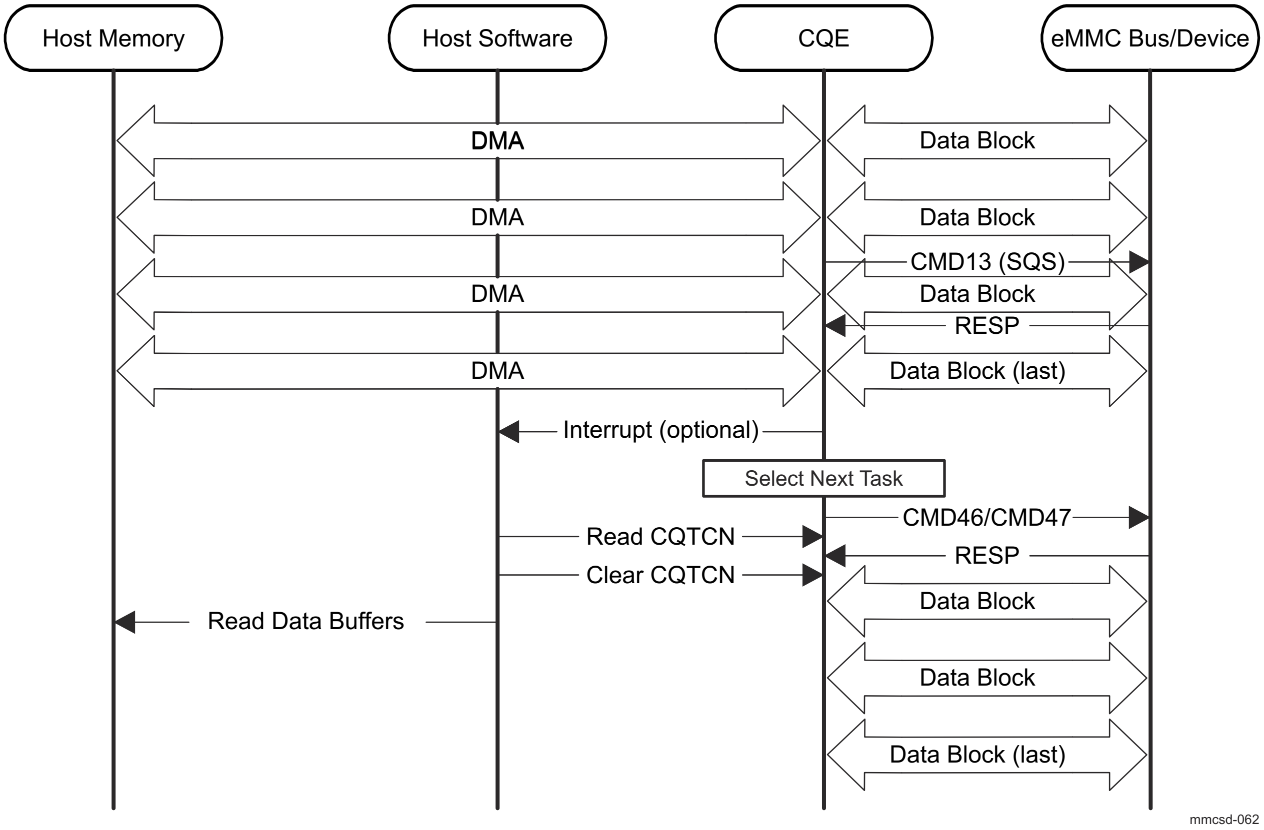

Figure 12-275. Task Execution and Completion Sequence

Table 12-263. Task Execution and Completion Sequence

Step	Description
1	Once the tasks are queued on the device side CQE sends CMD13 to determine the queue status. The queue status lets the CQE know which tasks are ready for execution.
2	The response to CMD13 may indicate no task is ready in which case the CQE is required to send CMD13 again at a later time as controlled CQSST register.
3	If a task is ready for execution then the host sends EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) to the device with the task id ordering it to execute a task.
4	When the task execution is completed, an interrupt may be generated, if requested, or as determined by Interrupt Coalescing mechanism.
5	The host software reads MMCSD0_CQ_TASK_COMP_NOTIF register to determine which task(s) has(have) been completed. Each bit set in MMCSD0_CQ_TASK_COMP_NOTIF register represents by index which task has completed but hasn't yet been served by software.
6	For every task completed clear the appropriate MMCSD0_CQ_TASK_COMP_NOTIF register bit.
7	Repeat steps 1-6 for the pending tasks.

12.4.5.5.2.4.4 Task Discard and Clear Sequence

Figure 12-276 and Table 12-252 show a task discard and clear sequence.

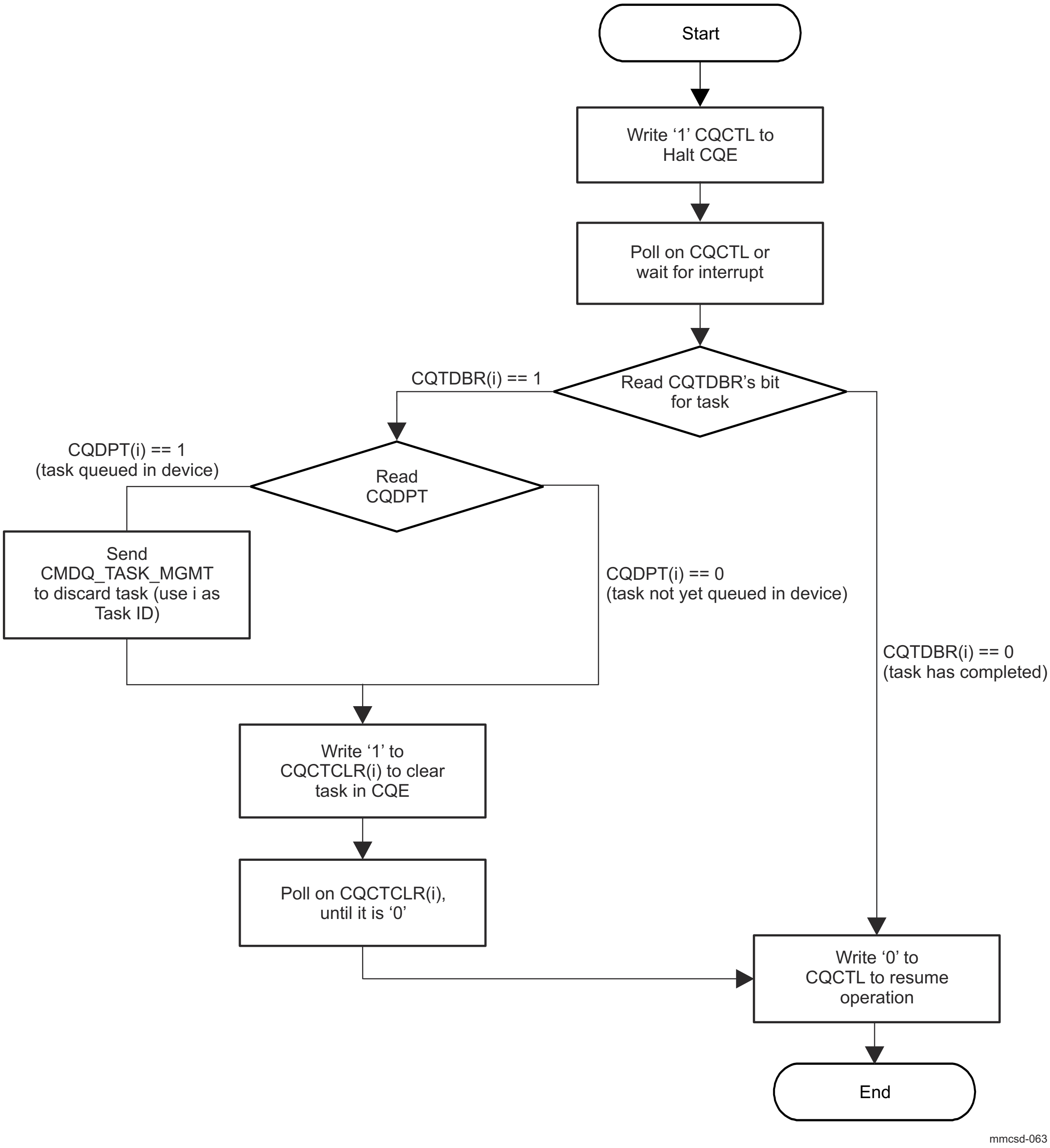

Figure 12-276. Task Discard and Clear Sequence

Table 12-264. Task Discard and Clear Sequence

Step	Description
1	While CQE is enabled write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
2	Poll on MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit.
3	Read MMCSD0_CQ_TASK_DOOR_BELL register to determine if the task to be dicarded is set to 1.
4	Read MMCSD0_CQ_DEV_PENDING_TASKS register to check if the task is queued in the device.
5	Send CMDQ_TASK_MGMT(CMD48) to discard task using the task id as the argument.
6	Write '1' to CQCTCLR[i] to clear task in CQE.

Table 12-264. Task Discard and Clear Sequence (continued)

Step	Description
7	Poll on CQCTCLR[i] until it is '0'.
8	Write '0' to MMCSD0_CQ_CONTROL register to resume CQE.

12.4.5.5.2.4.5 Error Detect and Recovery when CQ is enabled

Figure 12-277 and Table 12-253 show an error detect and recovery sequence.

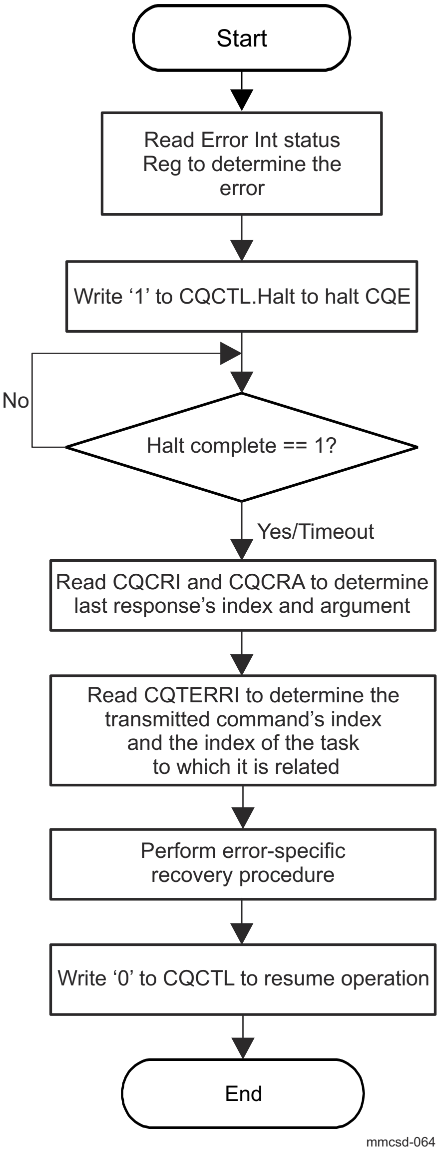

Figure 12-277. Error Detect and Recovery Sequence

Table 12-265. Error Detect and Recovery Sequence

Step	Description
1	Read eMMC host controller MMCSD0_ERROR_INTR_STS register and determine error is related to CQE.
2	Write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
3	Wait for MMCSD0_CQ_CONTROL[0] HALT_BIT bit to read '1'. In some error cases, this may not happen, so software should proceed to the next step after a sufficient time-out.

Table 12-265. Error Detect and Recovery Sequence (continued)

Step	Description
4	Read MMCSD0_CQ_CMD_RESP_INDEX and MMCSD0_CQ_CMD_RESP_ARG registers to determine last response's index and argument.
5	Read MMCSD0_CQ_TASK_ERR_INFO register to determine the transmitted command's index and the index of the task to which it is related.
6	Perform error-specific recovery procedure.
7	Write '0' to MMCSD0_CQ_CONTROL register to resume operation.

12.5 Industrial and Control Interfaces

This section describes the industrial and control interfaces in the device.

12.5.1 Modular Controller Area Network (MCAN)

This section describes the Modular Controller Area Network (MCAN) modules in the device.

12.5.1.1 MCAN Overview

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

They connect to the physical layer of the CAN network through external (for the device) transceivers. Each MCAN module supports flexible bit rates greater than 1 Mbps and is compliant to ISO 11898-1:2015.

Figure 12-278 shows the MCAN modules overview.

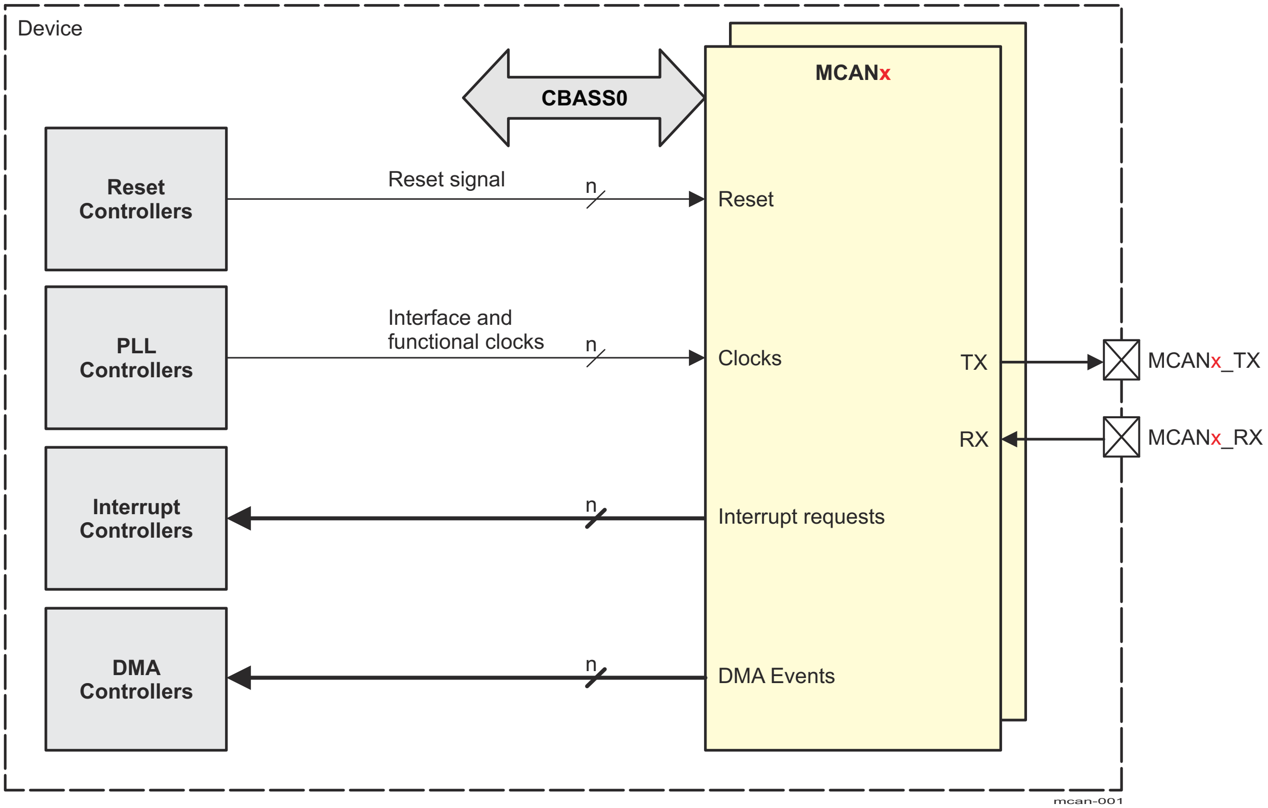

Note

x = 0 to number of MCAN in a domain -1

Figure 12-278. MCAN Modules Overview

12.5.1.1.1 MCAN Features

Each MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- SAE J1939 support
- AUTOSAR support

- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

12.5.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.5.1.2 MCAN Environment

This section describes the MCAN external connections (environment).

CAN network physical layer consists of two-wire differential bus, usually twisted pair, and provides high level of interference immunity. External CAN transceiver IC is needed to access a CAN bus by the MCAN.

Figure 12-279 shows the MCAN typical application.

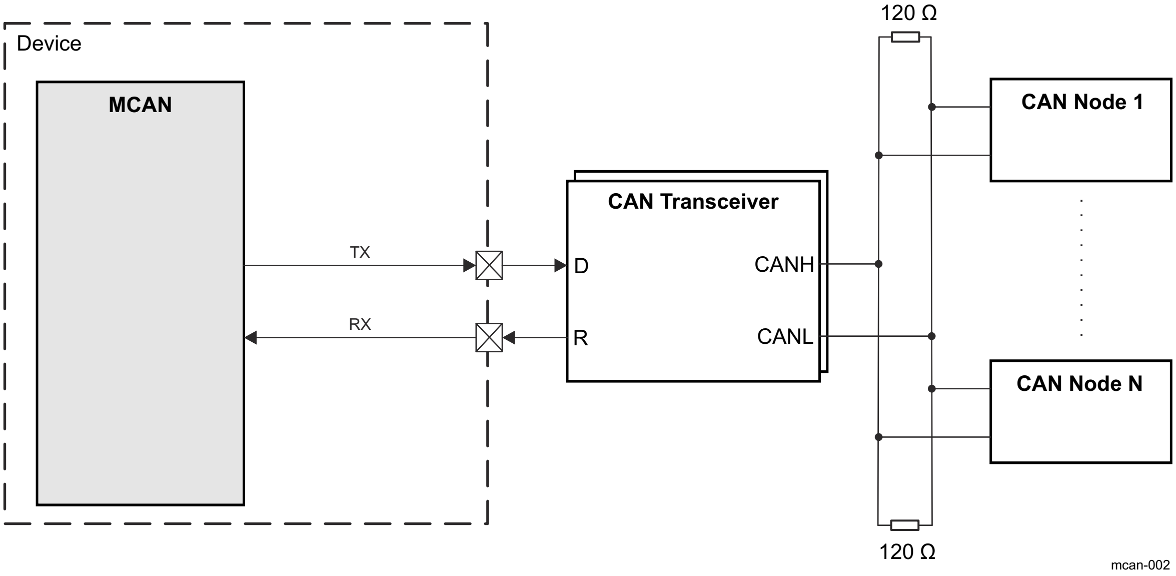

Figure 12-279. MCAN Typical Application

Table 12-254 describes the MCAN I/O signals.

Table 12-266. MCAN I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(1)
		MCANi(2)		
RX	MCANi(2)_RX	I	Serial data input from external CAN transceiver	HiZ
TX	MCANi(2)_TX	O	Serial data output to external CAN transceiver	1

(1) I = Input; O = Output; HiZ = High Impedance

(2) i represents an MCAN instance. See the device datasheet for available domains and MCAN instances.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.5.1.2.1 CAN Network Basics

- CAN bus is a 2-wire differential bus using Non-Return-to-Zero (NRZ) encoding and has two states:
  - Recessive state (logical 1)
  - Dominant state (logical 0)
- The network is multicontroller. When two or more nodes (ECUs) attempt to transmit at the same time, a non-destructive arbitration technique guarantees messages are sent in order of priority and no messages are lost.
- The message transmission is multicast. Data messages transmitted are identifier based, not address based.
- Content of message is labeled by the identifier that is unique throughout the network (for example: rpm, temperature, position, pressure, and so forth).
- All nodes on network receive the message and each performs an acceptance test on the identifier. If message is relevant, it is processed, otherwise it is ignored.
- The unique identifier also determines the priority of the message (the lower the numerical value of the identifier, the higher the priority is).
- Data is transmitted and received using message frames, consisting of the following basic fields:
  - Arbitration field
  - Control field
  - Data field (up to 8 bytes for Classical CAN and up to 64 bytes for CAN FD)
  - CRC field
  - ACK field

For more information, see *ISO 11898-1:2015: CAN data link layer and physical signaling*.

12.5.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.1.4 MCAN Functional Description

The MCAN module performs CAN protocol communication according to ISO 11898-1:2015. The bit rate can be programmed to values greater than 1 Mbps. Additional transceiver hardware is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message frames can be configured. The message frames and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler.

The register set of the MCAN module can be accessed directly via the module interface. These registers are used to control and configure the CAN core and the Message Handler, and to access the Message RAM.

Figure 12-280 shows the MCAN module block diagram.

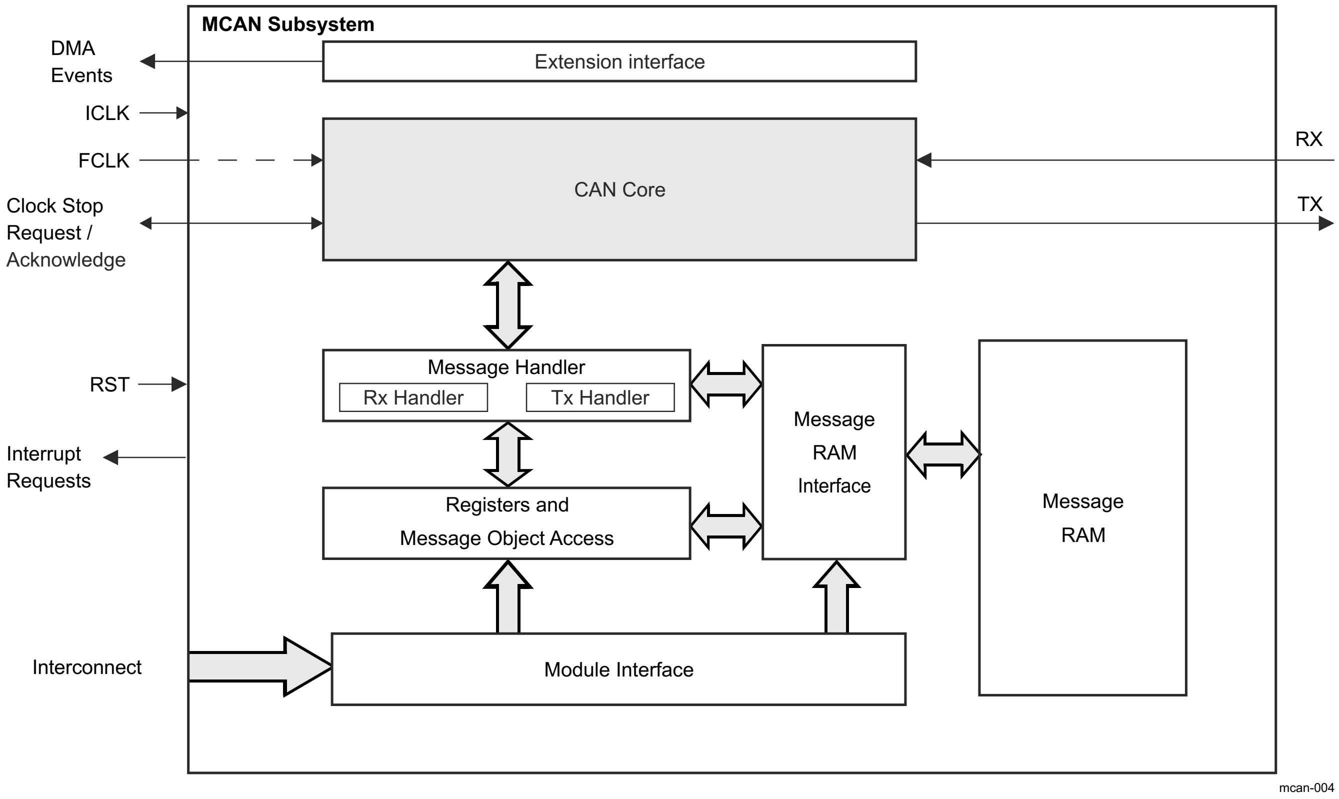

Figure 12-280. MCAN Block Diagram

The MCAN module blocks description:

- **CAN Core**: the CAN core consists of the CAN protocol controller and the Rx/Tx shift register. It handles all ISO 11898-1:2015 protocol functions and supports 11-bit and 29-bit identifiers.
- **Message Handler**: the Message Handler (Rx Handler and Tx Handler) is a state machine that controls the data transfer between the single-ported Message RAM and the CAN core's Rx/Tx shift register. It also handles the acceptance filtering and the Interrupt/DMA request generation as programmed in the control registers.
- **Message RAM**: the main purpose of the Message RAM is to store Rx/Tx messages, Tx Event elements, and Message ID Filter elements (for more information, see Section 12.5.1.4.10 , *Message RAM*).
- **Message RAM Interface**: enables connection between the Message RAM and the other blocks in the MCAN module.
- **Registers and Message Object Access**: data consistency is ensured by indirect accesses to the message objects. The interface registers have the same word-length as the Message RAM.

- **Module Interface**: provides connection to the Registers and Message Object Access block and Message RAM Interface block
- **Clocking**: two clocks are provided to the MCAN module: the peripheral synchronous clock (interface clock ICLK) and the peripheral asynchronous clock (functional clock - FCLK). For more information, see *Module Integration*.
- **Extension Interface**: this interface is used for DMA requests signaling (see Section 12.5.1.4.2.2).

12.5.1.4.1 Module Clocking Requirements

Two clocks are provided to the MCAN module:

- the peripheral synchronous clock (ICLK) as the general module clock source
- and the peripheral asynchronous clock (FCLK) provided to the CAN core for generating the CAN bit timing.

Within the MCAN module there is a synchronization mechanism implemented to ensure safe data transfer between the two clock domains. There is synchronization between the signals from the Host clock domain to the CAN clock domain and vice versa and between the reset signal to the Host clock domain and to the CAN clock domain.

Note

ICLK must always be higher or equal to FCLK, in order to achieve a stable functionality of the MCAN module. Here, also the frequency shift of the modulated ICLK has to be considered:

$f_{0,\mathrm{ICLK}} \pm \Delta f_{\mathrm{FM,ICLK}} \geq f_{\mathrm{FCLK}}$

For more information on how to configure the relevant clock source registers, see *Clocking* and the device-specific Datasheet.

12.5.1.4.2 Interrupt and DMA Requests

The MCAN module provides interrupt and DMA requests. They are configured via the Host CPU. The Suspend Mode is requesting or forcing (based on MCANSS_CTRL[3] DBGSUSP_FREE bit) the MCAN module to go into initialization mode (see MCAN_CCCR[0] INIT bit) in which new interrupts and DMA requests will not be issued, that is to prevents the interrupt and DMA requests from propagating to the Host CPU (for more information, see Section 12.5.1.4.3.8.2 , *Suspend Mode*).

12.5.1.4.2.1 Interrupt Requests

The MCAN module has two interrupt lines. There are 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts.

The MCAN core provides two interrupt requests (for Line 0 and Line 1).

For more information, see the following registers:

- Interrupt Register (MCAN_IR)
- Interrupt Enable (MCAN_IE)
- Interrupt Line Select (MCAN_ILS)
- Interrupt Line Enable (MCAN_ILE)

The MCAN module is capable of issuing ECC interrupts. After clearing the ECC interrupt source, the application software must also write 1 to EOI register (MCANSS_ECC_SEC_EOI_REG/MCANSS_ECC_DED_EOI_REG). For more information, see *ECC Aggregator*.

The MCAN module supports External Timestamp Counter. When the External Timestamp Counter rolls over it produces an interrupt (see Section 12.5.1.4.4.1 , *External Timestamp Counter*).

For more information, see the following registers:

- Interrupt Clear Shadow Register (MCANSS_ICS)
- Interrupt Raw Status Register (MCANSS_IRS)
- Interrupt Enable Clear Shadow Register (MCANSS_IECS)

- Interrupt Enable Register (MCANSS_IE)
- Interrupt Enable Status Register (MCANSS_IES)
- End Of Interrupt Register (MCANSS_EOI)
- External Timestamp Prescaler Register (MCANSS_EXT_TS_PRESCALER)
- External Timestamp Unserviced Interrupts Counter Register (MCANSS_EXT_TS_UNSERVICED_INTR_CNTR)

For more information about available Interrupt Requests, see *MCAN Hardware Requests*.

12.5.1.4.2.2 DMA Requests

Functional transmit and Filter DMA requests are generated by the MCAN module based on the signaling in the Extension Interface. The DMA signaling uses a simple DMA request active high pulse.

The active high pulse indicates a pending message is transmitted (see MCAN_TXBRP). This pulse can be used to transfer another message to the Tx Buffer, which would need to be followed by writing 1 to the corresponding MCAN_TXBAR[0] AR bit to mark a new Tx message pending transmission.

The Parity on Tx DMA Events is available using an EDC Controller which can be accessed through the ECC Aggregator.

Standard and Extended message filters can be set to issue a pulse when a filter match occurs. These 'Filter Events' can be used to DMA messages from the Rx FIFO. The events are high level single clock cycle pulses (ICLK).

12.5.1.4.3 Operating Modes

12.5.1.4.3.1 Software Initialization

Setting the MCAN_CCCR[0] INIT bit to 1 starts a software initialization. This is done either by software or by a hardware reset, when an uncorrected bit error was detected in the Message RAM, or by going Bus_Off state. While the MCAN_CCCR[0] INIT bit is set, the message transfer is stopped and the status of the output TX pin is recessive (high). The counters of the Error Management Logic (EML) are unchanged. Setting the MCAN_CCCR[0] INIT bit does not change any configuration register. Resetting the MCAN_CCCR[0] INIT bit finishes the software initialization. After waiting for the occurrence of a sequence of 11 consecutive recessive bits (indication for Bus_Idle state) the message transfer starts.

Access to the MCAN configuration registers is only enabled when both MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are set (write protection).

The MCAN_CCCR[1] CCE bit can only be set/reset while the MCAN_CCCR[0] INIT = 1. The MCAN_CCCR[1] CCE bit is automatically reset when the MCAN_CCCR[0] INIT bit is reset.

The following registers are reset when the MCAN_CCCR[1] CCE bit is set:

- MCAN_HPMS - High Priority Message Status
- MCAN_RXF0S - Rx FIFO 0 Status
- MCAN_RXF1S - Rx FIFO 1 Status
- MCAN_TXFQS - Tx FIFO/Queue Status
- MCAN_TXBRP - Tx Buffer Request Pending
- MCAN_TXBTO - Tx Buffer Transmission Occurred
- MCAN_TXBCF - Tx Buffer Cancellation Finished
- MCAN_TXEFS - Tx Event FIFO Status

The Timeout Counter value MCAN_TOCV[15-0] TOC field is preset to the value configured by the MCAN_TOCC[31-16] TOP field when the MCAN_CCCR[1] CCE bit is set.

In addition the Tx Handler and Rx Handler are held in idle state while MCAN_CCCR[1] CCE = 1.

The following registers are only writeable while MCAN_CCCR[1] CCE = 0

- MCAN_TXBAR - Tx Buffer Add Request
- MCAN_TXBCR - Tx Buffer Cancellation Request

MCAN_CCCR[7] TEST and MCAN_CCCR[5] MON bits can only be set by the Host CPU while MCAN_CCCR[0] INIT = 1 and MCAN_CCCR[1] CCE = 1. Both bits may be reset at any time. The MCAN_CCCR[6] DAR bit can only be set/reset while MCAN_CCCR[0] INIT = 1
and MCAN_CCCR[1] CCE = 1.

Table 12-255 shows the steps to configure the MCAN module.

Table 12-267. Steps to Configure MCAN Module

Step	Operation	Description	Pseudo Code
1	Initialize MCAN_CCCR	Set MCAN_CCCR[0] INIT bit and check that it has been set	INIT = 1; If INIT ≠ 1, wait until it is
2	Unlock protected registers	Set MCAN_CCCR[1] CCE bit	CCE = 1;
3	Configure CAN mode	Set MCAN_CCCR[8] FDOE bit to CAN FD	FDOE = 1 for CAN FD FDOE = 0 for CAN
4	Configure Bit Rate Switching	Set MCAN_CCCR[9] BRSE bit	BRSE = 1 with bit rate switching BRSE = 0 without bit rate switching
5	Set bit timing	Set MCAN_NBTP register	
6	Lock protected registers	Clear MCAN_CCCR[1] CCE bit	CCE = 0;
7	Return MCAN module to normal operation	Clear MCAN_CCCR[0] INIT bit and check it has been cleared	INIT = 0; If INIT ≠ 0, wait until it is

12.5.1.4.3.2 Normal Operation

Once the MCAN module is initialized and the MCAN_CCCR[0] INIT bit is reset to zero, the MCAN module synchronizes itself to the CAN bus and is ready for communication. After passing the acceptance filtering, received messages including Message Identifier (ID) and Data Length Code (DLC) are stored into a dedicated Rx Buffer or into Rx FIFO 0/Rx FIFO 1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated.

Note

Automated transmission on reception of remote frames is not supported.

12.5.1.4.3.3 CAN FD Operation

The CAN FD standard allows extended frames to be sent, up to 64 data bytes in a single frame at a higher bit rate for the data phase of a frame, up to 8 Mbps. The CAN FD standard introduces the ability to switch from one bit rate to another. Extended Data Length (EDL), as shown in Figure 12-281, sets a data length of up to 8 or up to 64 data bytes. Bit Rate Switching (BRS) indicates whether two bit rates (the data phase is transmitted at a different bit rate to the arbitration phase) are enabled.

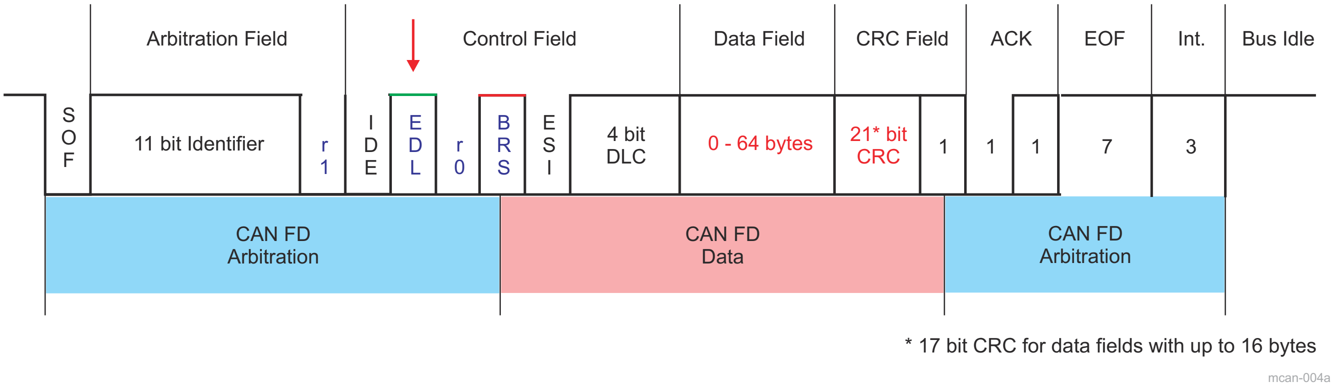

Figure 12-281. CAN FD Frame

Note

Figure 12-281 presents CAN FD frame according to the Non-ISO CAN FD (legacy) protocol. In the new ISO CAN FD protocol the CRC Field includes additional 5 bits (three stuff bit counter (SBC) bits and two parity bits). With these additional bits, a weakness identified in the error detection scheme chosen by the original protocol is removed. By setting MCAN_CCCR[15] NISO bit, the ISO or Non-ISO CAN FD format can be chosen. In CAN network ISO CAN FD and non-ISO CAN FD devices should never mix.

There are two variants of CAN FD frame transmission:

- CAN FD frame transmission without bit rate switching
- CAN FD frame transmission where control field, data field, and CRC field are transmitted with a higher bit rate than the beginning and the end of the frame

In the CAN frames FDF = recessive (logical 1) signifies a CAN FD frame, FDF = dominant (logical 0) signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF - res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by res = dominant and BRS = recessive. Note that the coding of res = recessive is reserved for future expansion of the protocol. In case the MCAN module receives a frame with FDF = recessive and res = recessive, it will signal a Protocol Exception Event by setting the MCAN_PSR[14] EXE bit. When Protocol Exception Handling is enabled (MCAN_CCCR[12] PXHD = 0), this causes the operation state to change from Receiver (MCAN_PSR[4-3] ACT = 10) to Integrating (MCAN_PSR[4-3] ACT = 00) at the next sample point. In case Protocol Exception Handling is disabled (MCAN_CCCR[12] PXHD = 1), the MCAN will treat a recessive res bit as an form error and will respond with an error frame.

CAN FD operation is enabled by programming the MCAN_CCCR[8] FDOE bit. In case MCAN_CCCR[8] FDOE = 1, transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via the FDF bit in the respective Tx Buffer element.

With MCAN_CCCR[8] FDOE = 0, received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if the FDF bit of a Tx Buffer element is set. The MCAN_CCCR[8] FDOE and MCAN_CCCR[9] BRSE bits can only be changed while the MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are both set. With MCAN_CCCR[8] FDOE = 0, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format.

With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 0, only FDF bit of a Tx Buffer element is evaluated. With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 1, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significant higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.
- During system startup all nodes are transmitting Classic CAN messages until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wakeup messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in Silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

In the CAN FD format, the DLC coding differs from the standard CAN format (see Table 12-256).

Table 12-268. DLC Coding

DLC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Number of Data Bytes in Standard CAN	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8
Number of Data Bytes in CAN FD	0	1	2	3	4	5	6	7	8	12	16	20	24	32	48	64

For CAN FD frames, the bit timing will be switched inside the frame after the BRS (Bit Rate Switch) bit in case this bit is recessive. In the CAN FD arbitration phase, before the BRS bit, the nominal CAN bit timing (see Figure 12-282) is used as configured by the Nominal Bit Timing and Prescaler Register MCAN_NBTP. In the following CAN FD data phase, the data phase bit timing is used as configured by the Data Bit Timing and Prescaler Register MCAN_DBTP. The bit timing is switched back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

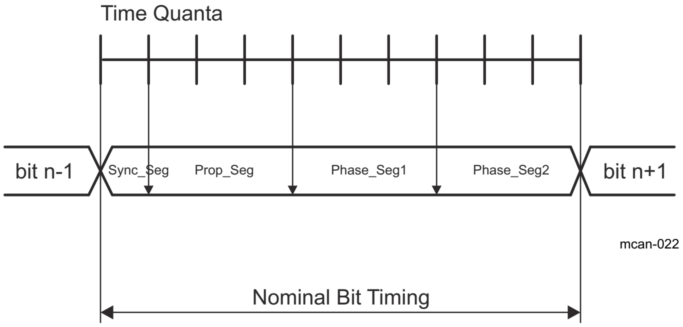

Figure 12-282. CAN Bit Timing

The maximum configurable data phase bit timing depends on the CAN clock frequency (FCLK). Example: with FCLK = 20 MHz and the shortest configurable bit time of 4 t_q (time quanta), the bit rate in the data phase is 5 Mbps.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the ESI (Error Status Indicator) bit depends on transmitter's error state (see MCAN_PSR[11] RESI bit) monitored at the start of the transmission. If the transmitter has error passive flag the ESI bit is transmitted recessive, else it is transmitted dominant.

12.5.1.4.3.4 Transmitter Delay Compensation

12.5.1.4.3.4.1 Description

When only one CAN FD node is transmitting and all others are receivers the length of the bus line has no impact. When transmitting via the TX pin the MCAN module receives the transmitted data from its local CAN transceiver via the RX pin. The received data is delayed. If the transmitter delay is greater than TSEG1 (time segment before sample point), a bit error is detected.

The MCAN module provides a delay compensation mechanism to compensate the transmitter delay. The compensation mechanism enables transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver. Without transmitter delay compensation the bit rate in the data phase is limited by the transmitter delay.

The mechanism enables configurations where the data bit time is shorter than the transmitter delay (it is described in detail in ISO 11898-1:2015). The transmitter delay compensation is enabled by setting the MCAN_DBTP[23] TDC bit to 1.

The delayed transmit data is compared against the received data at the Secondary Sample Point (SSP) in order to check for bit errors during the data phase of transmitting nodes. If a bit error is detected, the transmitter will react on this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the MCAN's transmit output TX pin through the transceiver to the receive input RX pin plus the transmitter delay compensation offset configured by the MCAN_TDCR[14-8] TDCO field (see Figure 12-283). The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (example: half of the bit time in the data phase). The position of the SSP is rounded down to the next integer number of mtq.

The actual transmitter delay compensation value can be checked by reading the MCAN_PSR[22-16] TDCV field. This field is cleared when the MCAN_CCCR[0] INIT bit is set and is updated at each transmission of CAN FD frame while the MCAN_DBTP[23] TDC bit is set.

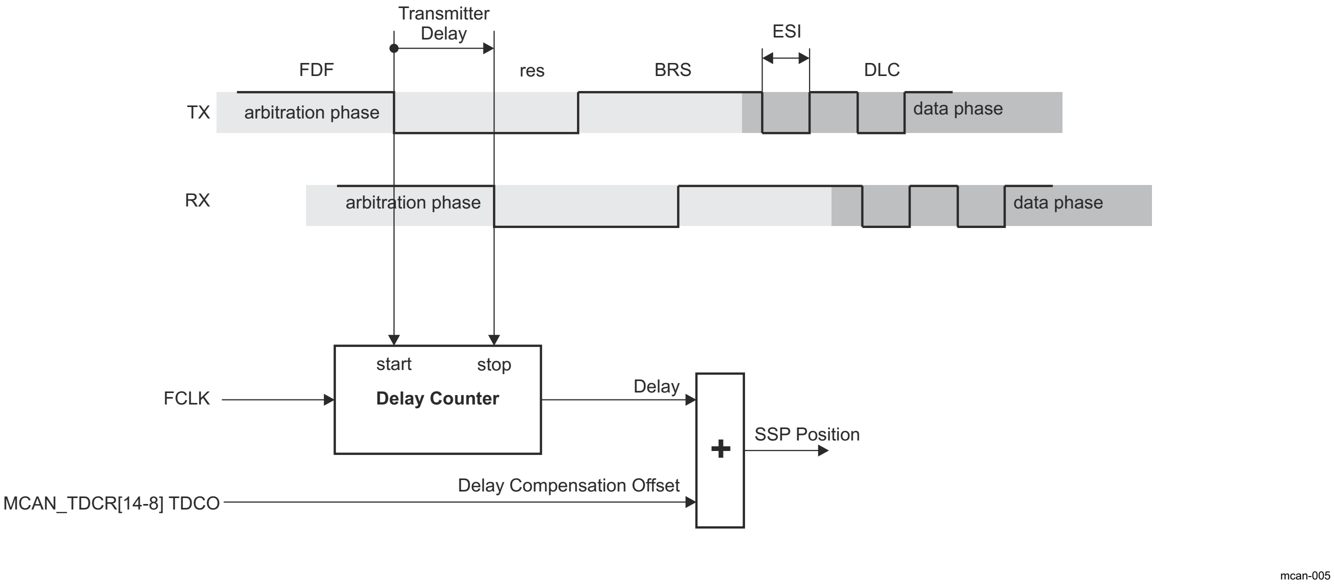

Figure 12-283. Transmitter Delay Measurement

12.5.1.4.3.4.2 Transmitter Delay Compensation Measurement

When transmitter delay compensation is enabled (by programming MCAN_DBTP[23] TDC = 1), the measurement is started within each transmitted CAN FD frame at the falling edge of FDF bit to bit res. The measurement is stopped when this edge is seen at the receive input RX pin of the transmitter. The resolution of this measurement is one mtq (see Figure 12-283). The mtq (minimum time quantum) dimension is equal to the CAN clock period (FCLK).

The use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR[6-0] TDCF field. This filter feature defines a minimum value for the SSP position to avoid the case in which a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in an early taken SSP position. Dominant edges on the RX pin, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR[6-0] TDCF field and the RX pin is low.

The following boundary conditions have to be considered:

- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO field) has to be less than 6 bit times in the data phase.
- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO) field has to be less or equal 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transmitter delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.

12.5.1.4.3.5 Restricted Operation Mode

In Restricted Operation Mode the CAN node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The recieve and transmit error counters (MCAN_ECR[14-8] REC and MCAN_ECR[7-0] TEC) are frozen while CAN error logging (MCAN_ECR[23-16] CEL) is active. The Host CPU can set the MCAN module into Restricted Operation Mode by setting MCAN_CCCR[2] ASM bit. The bit can only be set by the Host CPU at any time when both MCAN_CCCR[2] CCE and MCAN_CCCR[0] INIT bits are set to 1.

The Restricted Operation Mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation Mode, the Host CPU has to reset MCAN_CCCR[2] ASM bit. This mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

Note

The Restricted Operation Mode must not be combined with the Internal Loopback Mode .

12.5.1.4.3.6 Bus Monitoring Mode

Entering Bus Monitoring Mode is done by setting the MCAN_CCCR[5] MON bit to 1. In this mode (see ISO 11898-1:2015, *Bus Monitoring* section), the MCAN module is able to receive valid data and remote frames, but cannot start a transmission. The MCAN module sends only recessive bits on the CAN bus. If the MCAN module is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN module monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring Mode the MCAN_TXBRP register is held in reset state. The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. Figure 12-284 shows the connection of the TX and RX signals to the MCAN module in Bus Monitoring Mode.

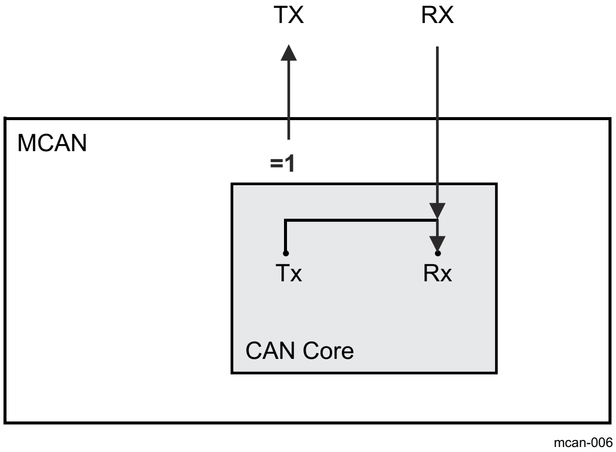

Figure 12-284. Connection of Signals in Bus Monitoring Mode

12.5.1.4.3.7 Disabled Automatic Retransmission (DAR) Mode

According to the CAN Specification (see ISO11898-1:2015, *Recovery Management* section), the MCAN module provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled (see the MCAN_CCCR[6] DAR bit).

12.5.1.4.3.7.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending MCAN_TXBRP[xx] TRPx bit is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

Successful transmission:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is not set

Successful transmission in spite of cancellation:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

Arbitration lost or frame transmission disturbed:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is not set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = 10 (transmission in spite of cancellation).

12.5.1.4.3.8 Power Down (Sleep Mode)

The entering in Power Down mode is controlled via two sources:

- PSC (via clock stop request signal)
- Software (by writing to the MCAN_CCCR[4] CSR bit)

As long as the clock stop request signal is active, the MCAN_CCCR[4] CSR bit is read as 1.

When all pending transmission requests have completed, the MCAN module waits until bus idle state is detected. Then the MCAN module sets the MCAN_CCCR[0] INIT bit to 1 to prevent any further CAN transfers.

The MCAN module acknowledges that it is ready for power down:

- By asserting clock stop acknowledge signal to the PSC (in case of PSC source).
- By setting the MCAN_CCCR[3] CSA flag bit to 1 (in case of Software source).

In this state, before the clocks are switched off, further register accesses can be made. Now the module clock inputs ICLK and FCLK may be switched off.

To leave power down mode, the application has to turn on the module clocks before resetting the input clock stop request signal respectively the MCAN_CCCR[4] CSR flag bit. The MCAN will acknowledge this by resetting the output clock stop acknowledge signal respectively the MCAN_CCCR[3] CSA flag bit. Afterwards, the application can restart CAN communication by resetting the MCAN_CCCR[0] INIT bit.

Restoring the clocks from clock stop mode, needs to be done according to how the clock stop was initiated:

- If Software asserts the MCAN_CCCR[3] CSA flag bit, once the MCAN module goes idle, the MCAN_CCCR[0] INIT bit is set. To get it started again, Software needs to write 0 to the MCAN_CCCR[0] INIT bit.
- If PSC is issuing a clock stop request, than there are two options for waking up:
  - After removing clock stop request signal, Software would need to write 0 to the MCAN_CCCR[0] INIT bit, or
  - If the MCANSS_CTRL[5] AUTOWAKEUP bit is set, than after removing clock stop request signal, an FSM inside the MCAN module will reset the MCAN_CCCR[0] INIT bit (without Software).

12.5.1.4.3.8.1 External Clock Stop Mode

The MCAN module supports two external clock stop modes:

- Immediate
- Graceful

In a graceful clock stop mode, when the clock stop request is asserted, the MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. The MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.5.1.4.3.8.3 , *Wakeup request*). When external clock stop request is removed and no suspend request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

12.5.1.4.3.8.2 Suspend Mode

The MCAN module supports two suspend modes:

- Immediate
- Graceful

In a graceful suspend mode (see the MCANSS_CTRL[3] DBGSUSP_FREE bit), when the suspend request is asserted, a clock stop request to the MCAN core is performed. The MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. At that point the MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle. The suspend state can be verified by reading MCAN_CCCR[0] INIT bit.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.5.1.4.3.8.3 , *Wakeup request*). When suspend request is removed, if no external clock stop request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:

- MCAN_ECR[23-16] CEL
- MCAN_PSR[2-0] LEC
- MCAN_PSR[10-8] DLEC
- MCAN_PSR[11] RESI
- MCAN_PSR[12] RBRS
- MCAN_PSR[13] RFDF
- MCAN_PSR[14] PXE

12.5.1.4.3.8.3 Wakeup request

Issuing a clock stop request puts the MCAN module into Power Down mode (Sleep Mode). During transition from IDLE to ACTIVE, if the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits are enabled, after the MCAN Core respond to the removal of the clock stop request with removing the clock stop acknowledge, a read-modify-write will be issued to clear the MCAN_CCCR[0] INIT bit and the MCAN core will resume operation.

If the MCANSS_CTRL[4] WAKEUPREQEN bit is set, the MCAN module provides a wakeup request on the following wakeup event:

- The receive RX pin is dominant (logical 0)

The wakeup request is de-asserted when any of the following conditions occur:

- Clock stop request is removed and clock stop acknowledge is de-asserted
- A reset is applied to the MCAN module

12.5.1.4.3.9 Test Modes

The MCAN_TEST register write access is enabled by setting the test mode enable MCAN_CCCR[7] TEST bit to 1. The MCAN_TEST register allows the configuration of the test modes and test functions.

The CAN transmit TX pin has four output functions. One of those functions can be selected by programming the MCAN_TEST[6-5] TX field. Additionally to its default function (the serial data output) it can drive the CAN Sample Point signal to monitor the MCAN's bit timing and it can drive constant dominant or recessive values.

The actual value of the CAN receive RX pin can be monitored from MCAN_TEST[7] RX bit. Both functions can be used to check the CAN bus physical layer. Due to the synchronization mechanism between CAN clock (FCLK) and Host clock (ICLK) domain, there may be a delay of several Host clock periods between writing to the MCAN_TEST[6-5] TX field until the new configuration is visible at the output TX pin. This applies also when reading input RX pin via the MCAN_TEST[7] RX bit.

Note

Test modes should be used for self test only. The software control for TX pin interferes with all CAN protocol functions. It is not recommended to use test modes for application.

12.5.1.4.3.9.1 Internal Loopback Mode

The MCAN module can be set into Internal Loopback Mode by programming MCAN_TEST[4] LBCK and MCAN_CCCR[5] MON bits to 1. The Internal Loopback Mode is used for a 'Hot Selftest'. The 'Hot Selftest' allows the MCAN module to be tested without affecting a running CAN system connected to the TX and RX pins. In this mode RX pin is disconnected from the MCAN module and TX pin is held recessive. Figure 12-285 shows the connection of the TX and RX pins to the MCAN module in case of Internal Loopback Mode.

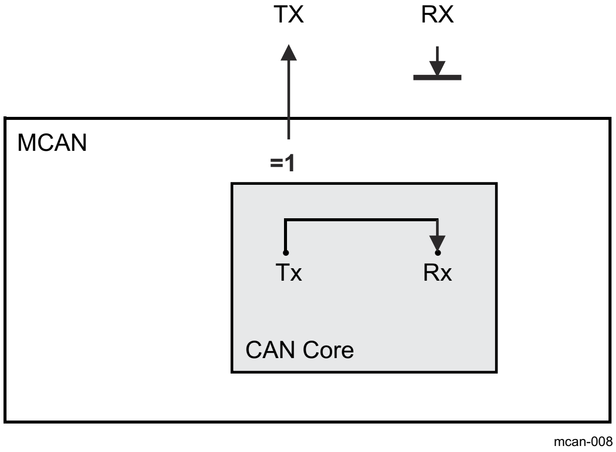

Figure 12-285. Internal Loopback Mode

12.5.1.4.4 Timestamp Generation

The MCAN module has integrated a 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler MCAN_TSCC[19-16] TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable via the MCAN_TSCV[15-0] TSC field. A write access to the MCAN_TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt MCAN_IR[16] TSW flag is set. On start of a frame reception/transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15-0]) or Tx Event FIFO (TXTS[15-0]) element. For more information, see Section 12.5.1.4.10 , *Message RAM*.

12.5.1.4.4.1 External Timestamp Counter

For CAN FD operation mode the MCAN core requires an External Timestamp Counter. An externally generated 16-bit vector may substitute the integrated 16-bit CAN bit time counter (internal timestamp counter) for receive and transmit timestamp generation. An external 16-bit timestamp counter can be used by programming the MCAN_TSCC[1-0] TSS field.

The External Timestamp Counter uses the interface clock (ICLK) as a reference clock. The MCAN Core accepts a 16-bit timestamp. A 24-bit prescaler provides a programmable resolution for the timestamp (see MCANSS_EXT_TS_PRESCALER[23-0] PRESCALER bit field). The External Timestamp Counter counter can be enabled or disabled through the MCANSS_CTRL[6] EXT_TS_CNTR_EN bit. When disabled the counter is reset back to zero. While enabled the counter keeps incrementing. When the timestamp rolls over the MCAN timestamp interrupt is generated.

When the timestamp rolls over the MCANSS_IRS register is set (see Figure 12-286). The MCANSS_IE register can be affected by writing to the *MCANSS_IESS* register to set or to the MCANSS_IECS register to clear. The *MCANSS_IESS* register is a shadow register mapped to the same address as the MCANSS_IE register. The level interrupt is a reflection of both MCANSS_IRS and MCANSS_IE being set. The MCANSS_IES register reflects the level interrupt. When an rollover event occurs the interrupt counter is incremented. Writing to the MCANSS_ICS register to clear the MCANSS_IRS register will also decrement the interrupt counter. Writing to the MCANSS_EOI register will issue another pulse if the interrupt counter is not zero.

The rollover event can be artificially simulated by software through writing to the Interrupt Set Shadow register (*MCANSS_ISS*). The *MCANSS_ISS* register is a shadow register mapped to the same address as the MCANSS_IRS register.

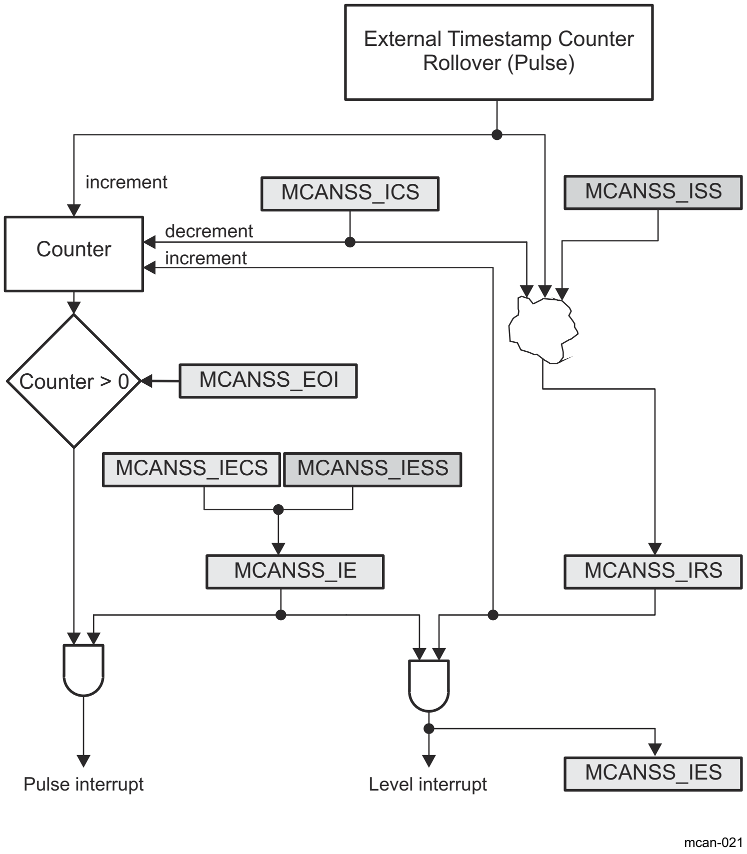

Figure 12-286. External Timestamp Counter Interrupt

12.5.1.4.5 Timeout Counter

The MCAN module has integrated a 16-bit Timeout Counter. It is used to signal timeout conditions for the Rx FIFO 0, Rx FIFO 1, and Tx Event FIFO Message RAM elements. The Timeout Counter is configured via the MCAN_TOCC register. It is enabled via the MCAN_TOCC[0] ETOC bit. The Timeout Counter operates as down-counter and uses the same prescaler programmed by the MCAN_TSCC[19-16] TCP field as the Timestamp Counter. The actual counter value can be monitored from the MCAN_TOCV[15-0] TOC field. The Timeout Counter can be started only when MCAN_CCCR[0] INIT = 0 and stopped when MCAN_CCCR[0] INIT = 1 (example: when the MCAN enters Bus_Off state). The operation mode is selected by the MCAN_TOCC[2-1] TOS field. When Continuous Mode is selected, the counter starts when MCAN_CCCR[0] INIT = 0, a write to the MCAN_TOCV register presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting.

In case the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored. Writing to the MCAN_TOCV register has no effect. When the counter reaches zero, the interrupt MCAN_IR[18] TOO flag is set.

In Continuous Mode, the counter is immediately restarted at the value configured by the MCAN_TOCC[31-16] TOP field.

12.5.1.4.6 ECC Support

The Message Memory is wrapped in an ECC wrapper providing SECDED parity functionality. The ECC wrapper is controlled by an ECC Aggregator.

12.5.1.4.6.1 ECC Wrapper

The ECC wrapper provides Single Error Correction (SEC) and Double Error Detection (DED) parity to the Message Memory content. It has side band signals for error notification. The ECC Wrapper implements an error injection test mode.

The error correction is done using a lazy write back. When an error is detected, it is noted in a FIFO Queue which waits for an access gap to write the data back and refresh the memory. If a transaction writes new data to the compromised entry before the lazy write back completes, the write back is discarded.

12.5.1.4.6.2 ECC Aggregator

Note

For more information about ECC Aggregator, refer to *ECC Aggregator*.

12.5.1.4.7 Rx Handling

The Rx Handler controls the following operations:

- Acceptance filtering
- The transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1)
- Rx FIFO Put and Get Index operations

12.5.1.4.7.1 Acceptance Filtering

The MCAN module is capable to configure two sets of acceptance filters - one set for standard and one set for extended identifiers. These filters can be assigned to an Rx Buffer or to one of the two Rx FIFOs.

The main features of the filter elements are:

- Each filter element can be configured as:
  - Range Filter (from - to)
  - Filter for specific IDs (for one or two dedicated IDs)
  - Classic Bit Mask Filter
- Each filter element can be enabled/disabled individually
- Each filter element can be configured for acceptance or rejection filtering
- Filters are checked sequentially and execution (acceptance filtering procedure) stops at the first matching filter element or when the end of the filter list is reached

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register
- Extended ID AND Mask (MCAN_XIDAM) register

Depending on the configuration of the filter element (see SFEC/EFEC in Section 12.5.1.4.10 , *Message RAM*) if filter matches, one of the following actions is performed:

- Received frame is stored in FIFO 0 or FIFO 1
- Received frame is stored in Rx Buffer
- Received frame is stored in Rx Buffer and generation of pulse at filter event pin is performed. This is high level single ICLK pulse. For more information, see Section 12.5.1.4.2.1 , *DMA Requests*.
- Received frame is rejected
- Set High Priority Message interrupt flag MCAN_IR[8] HPM
- Set High Priority Message interrupt flag MCAN_IR[8] HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering starts when complete Message ID is received. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If a filter element matches - the Rx Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If an error condition occurs (for example: CRC error), this message is rejected with the following impact on the affected Rx Buffer or Rx FIFO:

- Rx Buffer:
  New Data flag (MCAN_NDAT1/MCAN_NDAT2) of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields).
- Rx FIFO:
  Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields). If matching Rx FIFO is configured to operate in overwrite mode, the boundary conditions described in Section 12.5.1.4.7.2.2 have to be considered.

12.5.1.4.7.1.1 Range Filter

Each filter element can be configured to operate as Range Filter (Standard Filter Type SFT = 00/Extended Filter Type EFT = 00). The filter matches for all received message frames with IDs in the range from SFID1 to SFID2 (SFID2 ≥ SFID1) respectively in the range from EFID1 to EFID2 (EFID2 ≥ EFID1). For more information see Section 12.5.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.5.1.4.10.6 , *Extended Message ID Filter Element*.

There are two options for range filtering of extended frames:

- Extended Filter Type EFT = 00: The Extended ID AND Mask (MCAN_XIDAM) is used for Range Filtering. The Message ID of received frames is ANDed with the Extended ID AND Mask (MCAN_XIDAM) before the range filter is applied.
- Extended Filter Type EFT = 11: The Extended ID AND Mask (MCAN_XIDAM) is not used for Range Filtering.

12.5.1.4.7.1.2 Filter for specific IDs

Each filter element can be configured to filter one or two dedicated Message IDs (Standard Filter Type SFT =01/ Extended Filter Type EFT =01). To filter only one specific Message ID, the filter element has to be configured with SFID1 = SFID2 respectively EFID1 = EFID2. For more information see Section 12.5.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.5.1.4.10.6 , *Extended Message ID Filter Element*.

12.5.1.4.7.1.3 Classic Bit Mask Filter

Classic bit mask filtering can filter groups of Message IDs (Standard Filter Type SFT =10/Extended Filter Type EFT =10). This is done by masking single bits of a received Message ID. In this case SFID1/EFID1 element is used as Message ID filter, while SFID2/EFID2 element is used as filter mask.

A 0 bit at the filter mask (SFID2/EFID2) will mask out the corresponding bit position of the configured Message ID filter (SFID1/EFID1) and the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are 1 are relevant for acceptance filtering.

There are two interesting cases:

- All mask bits are 1: a match occurs only when the received Message ID and the configured Message ID filter are identical.
- All mask bits are 0: all Message IDs match.

12.5.1.4.7.1.4 Standard Message ID Filtering

The standard Message ID (11-bit ID) filtering flow is shown in Figure 12-287. Section 12.5.1.4.10.5 , *Standard Message ID Filter Element* describes the standard Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register

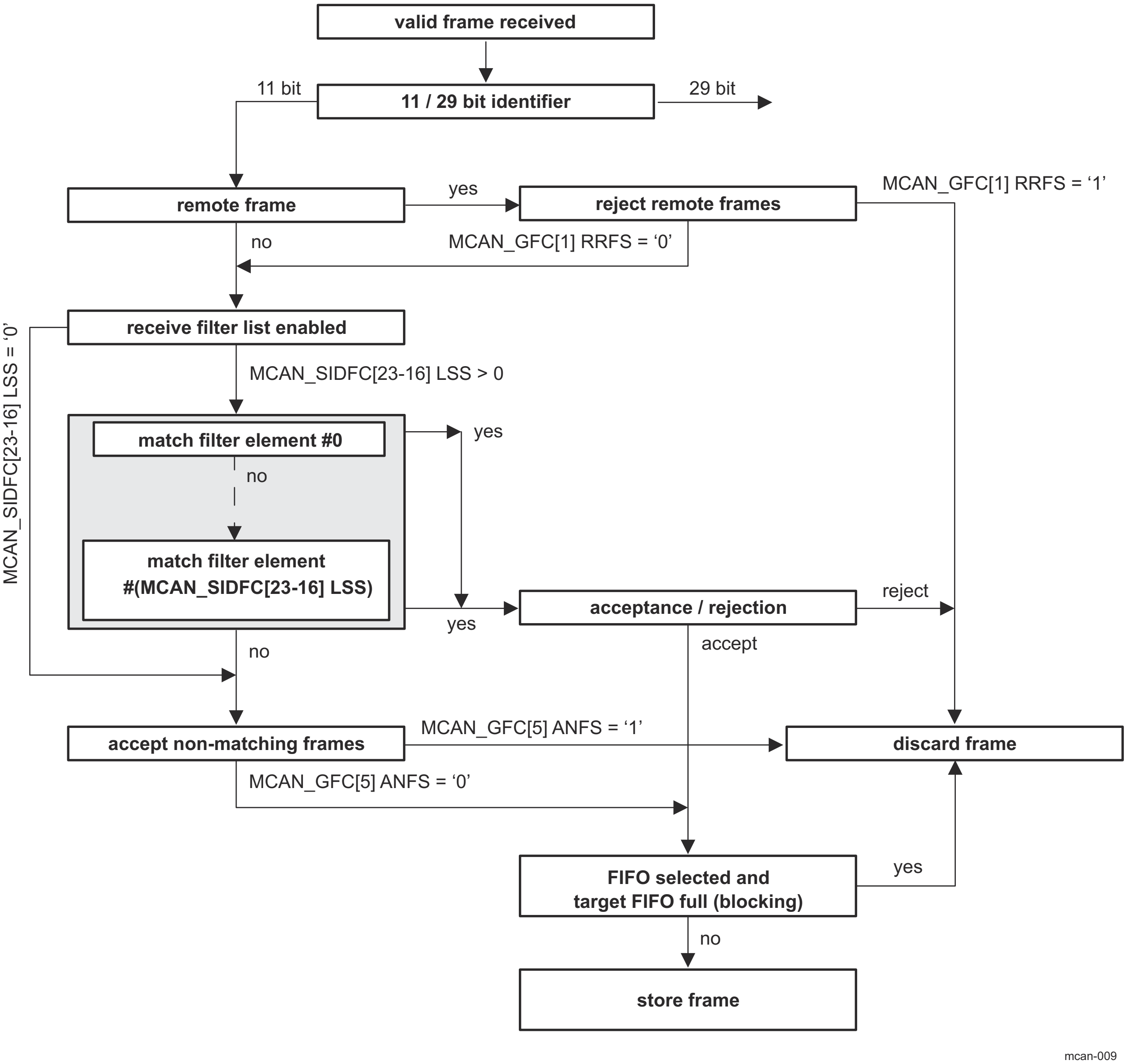

Figure 12-287. Standard Message ID Filter Path

12.5.1.4.7.1.5 Extended Message ID Filtering

The extended Message ID (29-bit ID) filtering flow is shown in Figure 12-288. Section 12.5.1.4.10.6 , *Extended Message ID Filter Element* describes the extended Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register

Note that before the filter list is executed the received identifier is ANDed with the Extended ID AND Mask (MCAN_XIDAM).

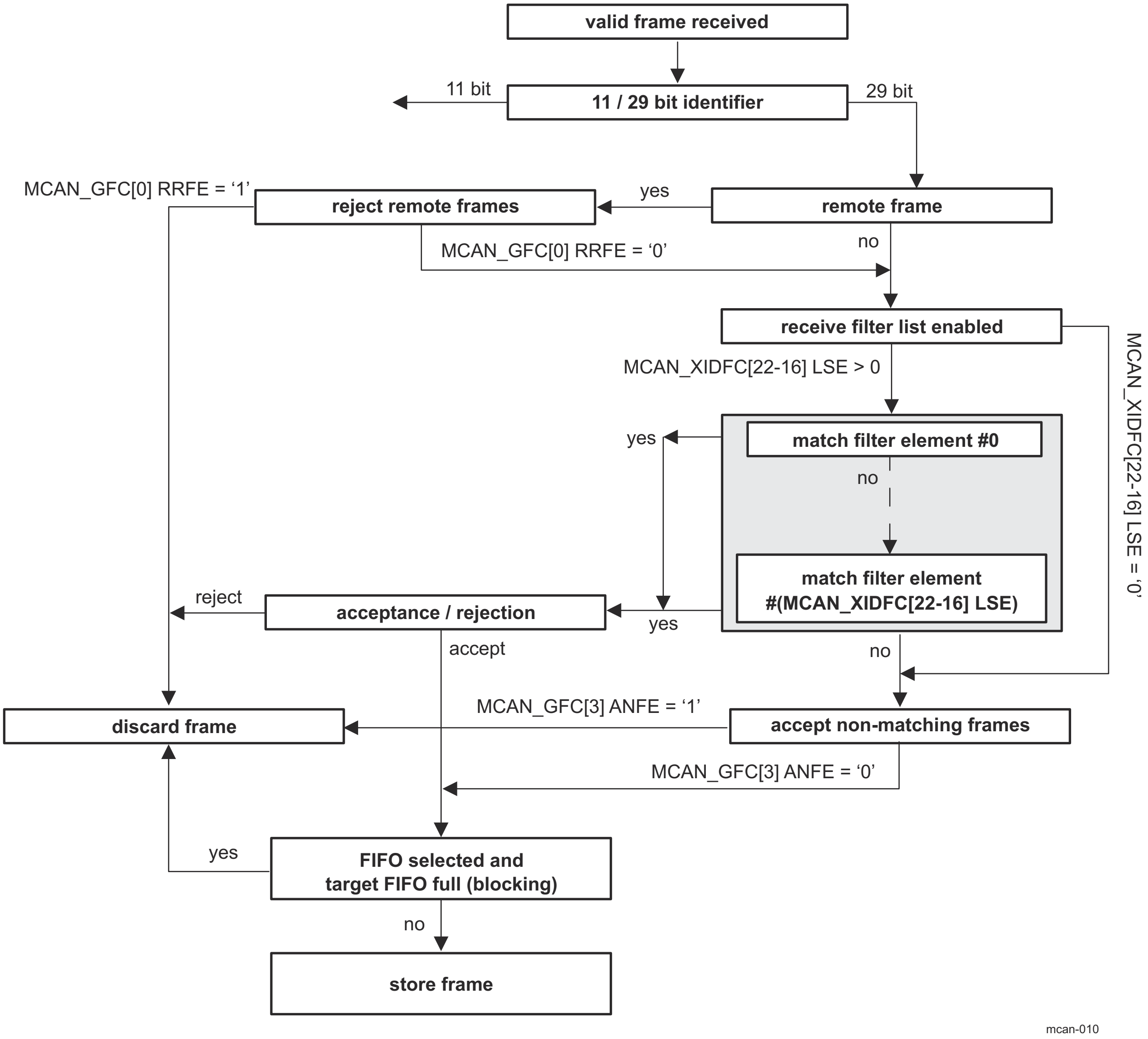

Figure 12-288. Extended Message ID Filter Path

12.5.1.4.7.2 Rx FIFOs

The configuration of the Rx FIFOs (Rx FIFO 0 and Rx FIFO 1) can be done via the MCAN_RXF0C and MCAN_RXF1C registers. Each Rx FIFO can be configured to store up to 64 received messages.

After acceptance filtering the received messages that passed are transferred to the Rx FIFO. The filter mechanisms available for the Rx FIFO 0 and Rx FIFO 1 is described in Section 12.5.1.4.7.1 , *Acceptance Filtering*. Section 12.5.1.4.10.2 , *Rx Buffer and FIFO Element* describes the Rx FIFO element.

The Rx FIFO watermark can be used to prevent an Rx FIFO overflow. If the Rx FIFO fill level reaches the Rx FIFO watermark configured by the MCAN_RXFnC[30-24] FnWM field (where: n = 0 or 1) an interrupt flag MCAN_IR[1] RF0W/MCAN_IR[5] RF1W is set.

When the Rx FIFO Put Index reaches the Rx FIFO Get Index (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) an Rx FIFO Full condition is signalled by the MCAN_RXFnS[24] FnF status bit and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set. Figure 12-289 shows Rx FIFO Status. The FIFOs fill level is presented in the MCAN_RXFnS[6-0] FnFL field (the number of elements stored in Rx FIFO).

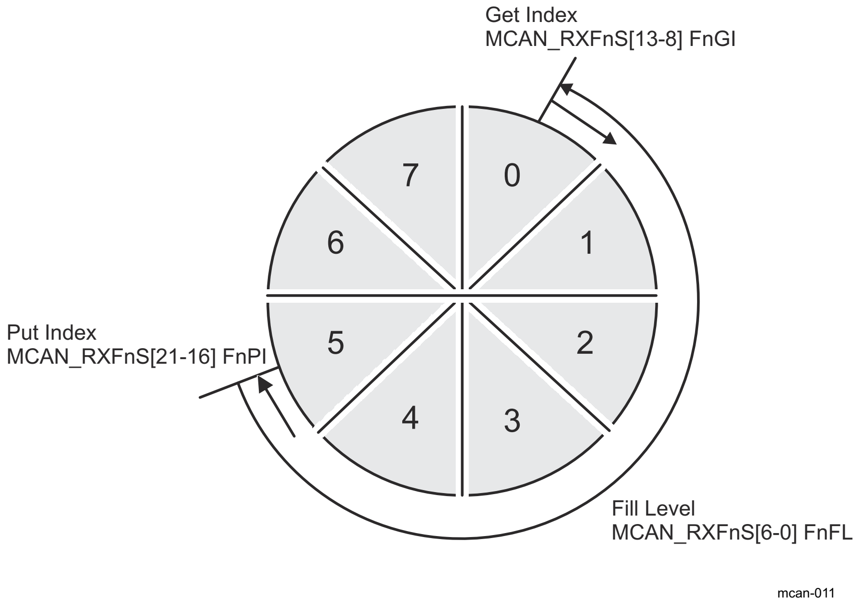

Figure 12-289. Rx FIFO Status

Rx FIFOs start address in the Message RAM (MCAN_RXFnC[15-2] FnSA field) have to be configured when reading from an Rx FIFO (Rx FIFO Get Index - MCAN_RXFnS[13-8] FnGI). Table 12-257 presents Rx Buffer/Rx FIFO Element Size for different Rx Buffer/Rx FIFO Data Field Size which is configured via the MCAN_RXESC register.

Table 12-269. Rx Buffer/Rx FIFO Element Size

MCAN_RXESC[10-8] RBDS MCAN_RXESC[2-0] F0DS/ MCAN_RXESC[6-4] F1DS	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.5.1.4.7.2.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is the default operation mode for the Rx FIFOs. It is configured by the MCAN_RXFnC[31] FnOM = 0.

If an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by the MCAN_RXFnS[24] FnF = 1 and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set.

In case a message is received while the corresponding Rx FIFO is full, this message is rejected and the message lost condition is signalled by MCAN_RXFnS[25] RFnL = 1 and interrupt flag MCAN_IR[3] RFnL/ MCAN_IR[25] RFnL is set.

12.5.1.4.7.2.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by the MCAN_RXFnC[31] FnOM = 1. When an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) signalled by MCAN_RXFnS[24] FnF = 1, the next accepted message for the FIFO will overwrite the oldest FIFO message. Put index/Get index are both incremented by one.

In overwrite mode if an Rx FIFO full condition is signalled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might happen, that a received message is written to the Message RAM (Put index) while the Host CPU is reading from the Message RAM (Get index). In this case inconsistent data may be read from the respective Rx FIFO element. The problem is solved by adding an offset to the Get index when reading from the Rx FIFO. The offset depends on how fast the Host CPU accesses the Rx FIFO. Figure 12-290 shows an offset of two with respect to the Get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

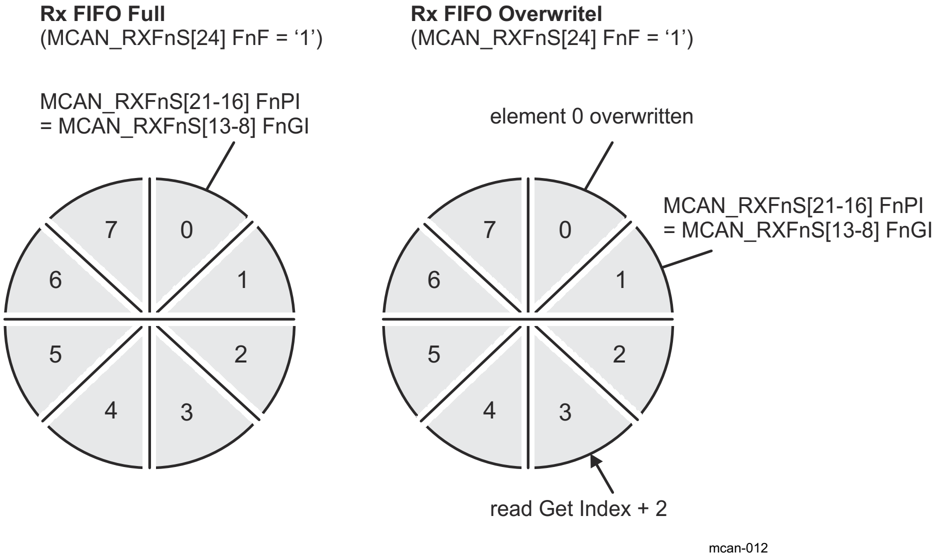

Figure 12-290. Rx FIFO Overflow Handling

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index MCAN_RXFnA[5-0] FnAI. This increments the get index to that element number. In case the Put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (MCAN_RXFnS[24] FnF = 0).

12.5.1.4.7.3 Dedicated Rx Buffers

The MCAN supports up to 64 dedicated Rx Buffers. The start address of the Rx Buffers section in the Message RAM is configured via MCAN_RXBC[15-2] RBSA field. To store in an Rx Buffer a Standard or Extended Message ID Filter Element with SFEC/EFEC = 111 and SFID2/EFID2[10-9] = 00 has to be configured (see Section 12.5.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.5.1.4.10.6 , *Extended Message ID Filter Element*).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element (the format is the same as for an Rx FIFO element). In addition the flag MCAN_IR[19] DRX (Message stored in Dedicated Rx Buffer) is set.

Table 12-258 shows Example Filter Configuration for Rx Buffers.

Table 12-270. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10-0] EFID1[28-0]	SFID2[10-9] EFID2[10-9]	SFID2[5-0] EFID2[5-0]
0	ID message 1	00	00 0000

Table 12-270. Example Filter Configuration for Rx Buffers (continued)

Filter Element	SFID1[10-0] EFID1[28-0]	SFID2[10-9] EFID2[10-9]	SFID2[5-0] EFID2[5-0]
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register MCAN_NDAT1/MCAN_NDAT2 is set. As long as the New Data flag is set, the respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host CPU by writing a 1 to the respective bit position.

While an Rx Buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

12.5.1.4.7.3.1 Rx Buffer Handling

Rx Buffer Handling include the following steps:

- Reset interrupt flag MCAN_IR[19] DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

12.5.1.4.7.4 Debug on CAN Support

Debug DMA is not supported feature. Debug messages can be traced through the RX FIFO (see Section 12.5.1.4.7.2).

12.5.1.4.8 Tx Handling

The Tx Handler is used to handle the Tx requests. It controls the transfer of transmit messages from the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue to the CAN Core, the Tx Event FIFO, and the Put and Get Index operations. The MCAN module supports up to 32 Tx Buffers. These Tx Buffers can be configured as dedicated Tx Buffers, Tx FIFO, or Tx Queue and as combination of dedicated Tx Buffers/Tx FIFO or dedicated Tx Buffers/Tx Queue. For each Tx Buffer element Classical CAN or CAN FD transmission mode can be configured. Section 12.5.1.4.10.3 describes the Tx Buffer Element. Table 12-259 shows the possible configurations for message transmission.

Table 12-271. Possible Configurations for Message Transmission

MCAN_CCCR		Tx Buffer Element		Frame Transmission
MCAN_CCCR[9] BRSE	MCAN_CCCR[8] FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	CAN FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	CAN FD without bit rate switching
1	1	1	1	CAN FD with bit rate switching

When the Tx Buffer Request Pending MCAN_TXBRP register is updated, or when a transmission has been started the Tx Handler starts scanning to check for the highest priority pending Tx request. The Tx Buffer with lowest Message ID has highest priority.

Note

AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation.

12.5.1.4.8.1 Transmit Pause

The transmit pause feature is intended for use in CAN networks where the CAN Message IDs are specific and cannot easily be changed. These Message IDs may have a higher priority than other defined Message IDs, while in a specific application their relative priority should be inverse. This allows for a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed (paused).

The transmit pause feature is enabled by the MCAN_CCCR[14] TXP bit. By default this bit is disabled (MCAN_CCCR[14] TXP = 0). Each time after successfully transmitted message, a pause for two CAN bit times occurs before the start of the next transmission. This allows the other CAN nodes in the network to transmit messages even if their Message IDs have lower priority.

12.5.1.4.8.2 Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the Host CPU.

There are two options:

- Each dedicated Tx Buffer is configured with a specific Message ID.
- Two or more dedicated Tx Buffers are configured with the same Message ID. In this case the Tx Buffer with the lowest buffer number is transmitted first.

After the data section has been updated, a transmission is requested by an Add Request. This is done via the MCAN_TXBAR[x]ARn bit (where x = 0 - 31). The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

Table 12-260 shows Tx Buffer/Tx FIFO/Tx Queue Element Size. A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM. The start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index from 0 to 31 (MCAN_TXFQS[20-16] TFQPI) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

Table 12-272. Tx Buffer/Tx FIFO/Tx Queue Element Size

MCAN_TXESC[2-0] TBDS	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.5.1.4.8.3 Tx FIFO

Tx FIFO mode is configured by setting bit MCAN_TXBC[30] TFQM = 0. The stored in the Tx FIFO messages are transmitted starting with the message referenced by the Get Index MCAN_TXFQS[12-8] TFGI field. After each transmission the Get Index is incremented until the Tx FIFO is empty. The Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field indicates the number of the available free Tx FIFO elements. The Tx FIFO allows transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. After each Add Request (MCAN_TXBAR[x] ARn = 1) the

Put Index is incemented to the next free Tx FIFO element. When the Put Index reaches the Get Index (MCAN_TXFQS[20-16] TFQPI = MCAN_TXFQS[12-8] TFGI), Tx FIFO Full condition is signalled by bit MCAN_TXFQS[21] TFQF = 1. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field.

In case a transmission request for the Tx Buffer referenced by the Get Index is cancelled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field is recalculated. In case transmission cancellation is applied to any other Tx Buffer - the Get Index and the FIFO Free Level remain unchanged.

A Tx FIFO element allocates Element Size 32-bit words in the Message RAM (see Table 12-260). The start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.5.1.4.8.4 Tx Queue

Tx Queue mode is configured by setting bit MCAN_TXBC[30] TFQM = 1. The stored in the Tx Queue messages are transmitted starting with the highest priority message (lowest Message ID). In case two or more Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. Each Add Request cyclically increments the Put Index to the next free Tx Buffer. In case of Tx Queue Full condition (MCAN_TXFQS[21] TFQF = 1), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

The application may use the MCAN_TXBRP register instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see Table 12-260). The start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.5.1.4.8.5 Mixed Dedicated Tx Buffers/Tx FIFO

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx FIFO: the number of Tx Buffers assigned to the Tx FIFO is configured by the MCAN_TXBC[29-24] TFQS field

If the MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by the MCAN_TXFQS[12-8] TFGI field)
- Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-291 shows Mixed Dedicated Tx Buffers/Tx FIFO example.

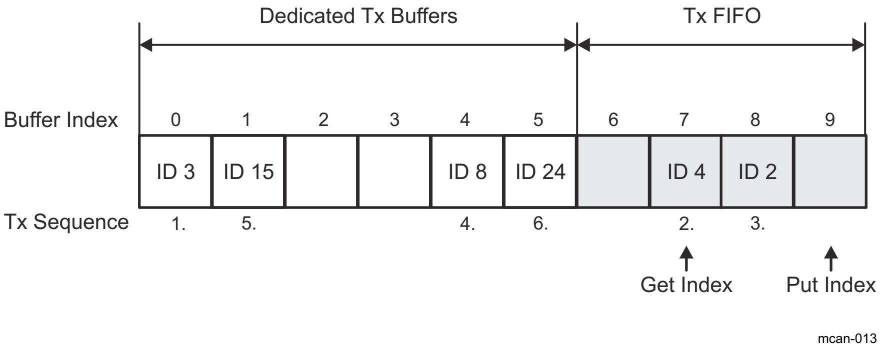

Figure 12-291. Mixed Dedicated Tx Buffers/Tx FIFO (example)

12.5.1.4.8.6 Mixed Dedicated Tx Buffers/Tx Queue

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx Queue: the number of Tx Buffers assigned to the Tx Queue is configured by the MCAN_TXBC[29-24] TFQS field

If MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan all Tx Buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-292 shows Mixed Dedicated Tx Buffers/Tx Queue example.

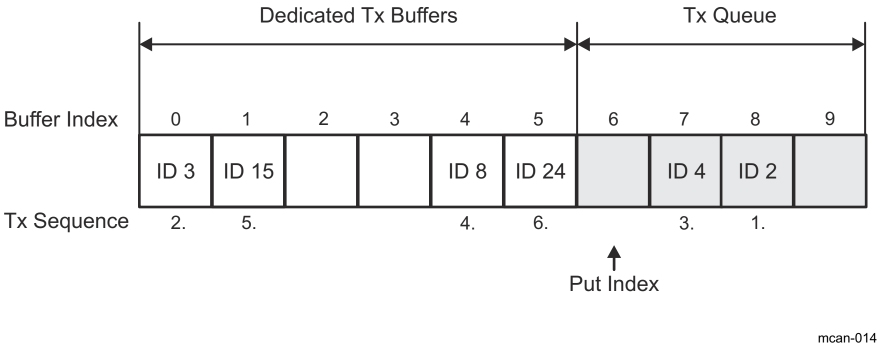

Figure 12-292. Mixed Dedicated Tx Buffers/Tx Queue (example)

12.5.1.4.8.7 Transmit Cancellation

This feature is especially intended for gateway and AUTOSAR based applications. The Host CPU can cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer by setting bit MCAN_TXBCR[n] CRn = 1 (where n = 0 - 31). The corresponding bit position n is equivalent to the number of the Tx Buffer.

Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signalled by setting the corresponding bit of the MCAN_TXBCF register (MCAN_TXBCF[n] CFn = 1).

If transmission from a Tx Buffer is already ongoing and a transmit cancellation is requested, the corresponding MCAN_TXBRP[n] TRPn bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding MCAN_TXBTO[n] TOn and MCAN_TXBCF[n] CFn bits are set. If the transmission was not successful, only the corresponding bit MCAN_TXBCF[n] CFn = 1.

Note

If pending transmission is cancelled immediately before this transmission could have been started, a short time window occurs where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

12.5.1.4.8.8 Tx Event Handling

To support Tx Event Handling the Message RAM has implemented a Tx Event FIFO section. Up to 32 Tx Event FIFO elements can be configured. Section 12.5.1.4.10.4 describes the Tx Event FIFO element. After message transmission on the CAN bus, Message ID and Timestamp are stored in a Tx Event FIFO element. To link a Tx Event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

A Tx Event FIFO full condition is signalled by the MCAN_IR[14] TEFF bit. In this case no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented (MCAN_TXEFS[12-8] EFGI). In case a Tx Event occurs while the Tx Event FIFO is full, this event is rejected and interrupt flag MCAN_IR[15] TEFL bit is set.

The Tx Event FIFO watermark can be configured to avoid a Tx Event FIFO overflow. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by the MCAN_TXEFC[29-24] EFWM field, interrupt flag MCAN_IR[13] TEFW is set. When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field has to be added to the Tx Event FIFO start address MCAN_TXEFC[15-2] EFSA field.

12.5.1.4.9 FIFO Acknowledge Handling

The Get Indices of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1) and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see MCAN_RXF0A, MCAN_RXF1A, and MCAN_TXEFA). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level.

There are two use cases:

- A single element has been read from the FIFO: the Get Index value is written to the FIFO Acknowledge Index.
- A sequence of elements has been read from the FIFO: the Get Index value (Index of the last element read) is written to the FIFO Acknowledge Index at the end of that read sequence.

The Host CPU has free access to the Message RAM. The special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This can be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also changes the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The MCAN module does not check for erroneous values.

12.5.1.4.10 Message RAM

The MCAN module has implemented Message RAM. The main purpose of the Message RAM is to store:

- Receive Messages
- Transmit Messages
- Tx Event Elements
- Message ID Filter Elements

12.5.1.4.10.1 Message RAM Configuration

The MCAN module is configured to allocate 4352 words in the Message RAM. The Message RAM has a width of 32 bits.

The Message RAM is capable to include each of the sections listed in Figure 12-293. It is not necessary to configure each of the sections (a section in the Message RAM may be 0) and there is not restriction with respect to the sequence of the sections. For parity checking or ECC a respective number of bits has to be added to each word.

When the MCAN module addresses the Message RAM it addresses 32-bit words. The start addresses are configurable and they are 32-bit word addresses.

The element size can be configured for:

- Rx FIFO 0 via the MCAN_RXESC[2-0] F0DS field
- Rx FIFO 1 via the MCAN_RXESC[6-4] F1DS field
- Rx Buffers via the MCAN_RXESC[10-8] RBDS field
- Tx Buffers via the MCAN_TXESC[2-0] TBDS field

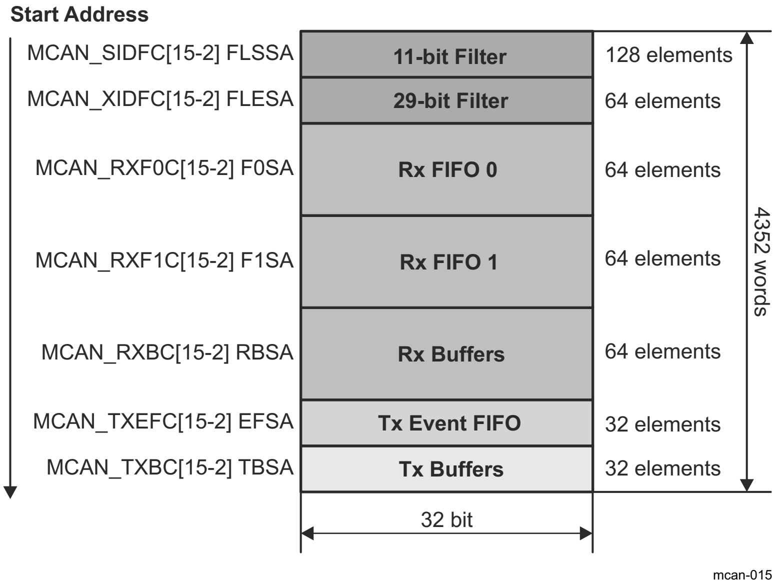

Figure 12-293. Message RAM Configuration

The Host CPU configures the following information in the Message RAM:

- Start addresses of the memory sections
- Number of elements in each section
- The size of the elements in some sections

Note

The MCAN module does not check for errors in the Message RAM configuration. The configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully. This will prevent falsification or loss of data.

12.5.1.4.10.2 Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_RXESC register.

Figure 12-294 shows Rx Buffer/Rx FIFO element structure.

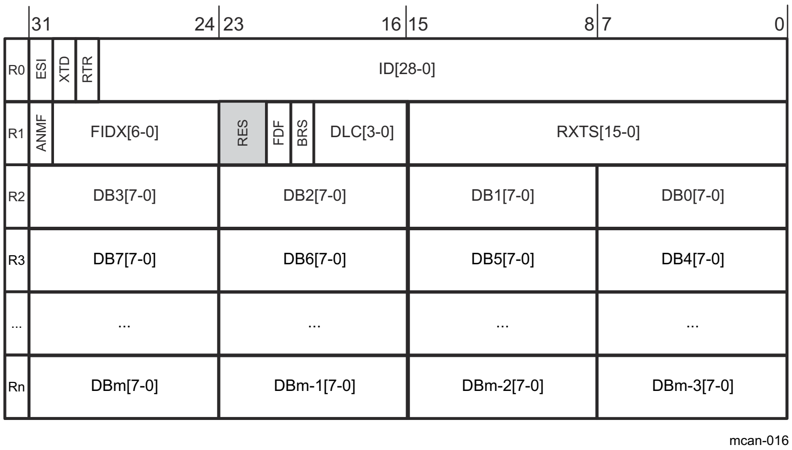

Figure 12-294. Rx Buffer/Rx FIFO Element Structure

Table 12-261 shows Rx Buffer/Rx FIFO element field descriptions.

Table 12-273. Rx Buffer/Rx FIFO Element Field Descriptions

Word	Bits	Field Name	Description
R0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive
	30	XTD	Extended Identifier Signals to the Host CPU whether the received frame has a standard or extended identifier. • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request Signals to the Host CPU whether the received frame is a data frame or a remote frame. • 0h = Received frame is a data frame • 1h = Received frame is a remote frame **Note:** There are no remote frames in CAN FD format. In case a CAN FD frame was received (FDF = 1), RTR bit reflects the state of the reserved r1 bit (RES[23]).

Table 12-273. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier is stored into ID[28-18].
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames may be enabled via the MCAN_GFC[5-4] ANFS and MCAN_GFC[3-2] ANFE fields. • 0h = Received frame matching filter index FIDX field • 1h = Received frame did not match any Rx filter element
	30-24	FIDX[6-0]	Filter Index 0h-7Fh (0-127): Index of matching Rx acceptance filter element (invalid if ANMF = 1). Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1.
	23-22	RES	Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame received without bit rate switching • 1h = Frame received with bit rate switching
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: received frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: received frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: received frame has 12/16/20/24/32/48/64 data bytes
	15-0	RXTS[15-0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP.
R2	31-24	DB3[7-0]	Data Byte 3
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
R3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6

Table 12-273. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Rn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3-17) are used for storage of a CAN message's data field.

12.5.1.4.10.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO/Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO/Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler makes difference between dedicated Tx Buffers and Tx FIFO/Tx Queue via the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_TXESC register.

Figure 12-295 shows Tx Buffer element structure.

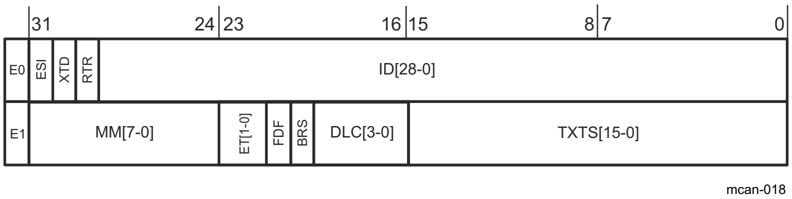

Figure 12-295. Tx Buffer Element Structure

Table 12-262 shows Tx Buffer element field descriptions.

Table 12-274. Tx Buffer Element Field Descriptions

Word	Bits	Field Name	Description
T0	31	ESI	Error State Indicator • 0h = ESI bit in CAN FD format depends only on error passive flag • 1h = ESI bit in CAN FD format transmitted recessive **Note:** The ESI bit of the transmit buffer is or'ed with the error passive flag to decide the value of the ESI bit in the transmitted CAN FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive.

Table 12-274. Tx Buffer Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Transmit data frame • 1h = Transmit remote frame **Note:** When RTR = 1, the MCAN module transmits a remote frame according to ISO11898-1:2015, even if the MCAN_CCCR[8] FDOE bit enables the transmission in CAN FD format.
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].
T1	31-24	MM[7-0]	Message Marker Written by Host CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-263).
	23	EFC	Event FIFO Control • 0h = Don't store Tx events • 1h = Store Tx events
	22	RES	Reserved
	21	FDF	FD Format • 0h = Frame transmitted in Classic CAN format • 1h = Frame transmitted in CAN FD format
	20	BRS	Bit Rate Switch • 0h = CAN FD frames transmitted without bit rate switching • 1h = CAN FD frames transmitted with bit rate switching **Note:** ESI, FDF, and BRS bits are only evaluated when CAN FD operation is enabled vie the MCAN_CCCR[8] FDOE bit. BRS bit is only evaluated when in addition the MCAN_CCCR[9] BRSE = 1.
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: transmit frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: transmit frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: transmit frame has 12/16/20/24/32/48/64 data bytes
	15-0	RES	Reserved

Table 12-274. Tx Buffer Element Field Descriptions (continued)

Word	Bits	Field Name	Description
T2	31-24	DB3[7-0]	Data Byte 3
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
T3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Tn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_TXESC), between two and sixteen 32-bit words (Tn = 3-17) are used for storage of a CAN message's data field.

12.5.1.4.10.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from the MCAN_TXEFS register.

Figure 12-296 shows Tx Event FIFO element structure.

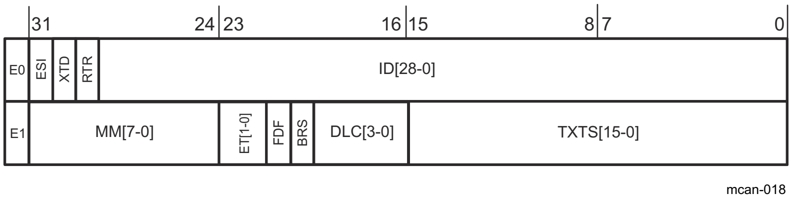

Figure 12-296. Tx Event FIFO Element Structure

Table 12-263 shows Tx Event FIFO element field descriptions.

Table 12-275. Tx Event FIFO Element Field Descriptions

Word	Bits	Field Name	Description
E0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive

Table 12-275. Tx Event FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Data frame transmitted • 1h = Remote frame transmitted
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].
E1	31-24	MM[7-0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-262).
	23-22	ET[1-0]	Event Type • 0h = Reserved • 1h = Tx event • 2h = Transmission in spite of cancellation (always set for transmissions in DAR mode) • 3h = Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame transmitted without bit rate switching • 1h = Frame transmitted with bit rate switching
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: frame with 0-8 data bytes transmitted • 9h-Fh (9-15) = CAN: frame with 8 data bytes transmitted • 9h-Fh (9-15) = CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted
	15-0	TXTS[15-0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP field.

12.5.1.4.10.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address MCAN_SIDFC[15-2] FLSSA field plus the index of the filter element (0-127).

Figure 12-297 shows Standard Message ID Filter element structure.

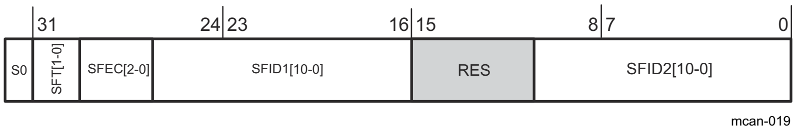

Figure 12-297. Standard Message ID Filter Element Structure

Table 12-264 shows Standard Message ID Filter element field descriptions.

Table 12-276. Standard Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
S0	31-30	SFT[1-0]	Standard Filter Type • 0h = Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) • 1h = Dual ID filter for SFID1 or SFID2 • 2h = Classic filter: SFID1 = filter; SFID2 = mask • 3h = Filter element disabled **Note:** With SFT = 11 the filter element is disabled and the acceptance filtering continues (same behaviour as with SFEC = 000)
	29-27	SFEC[2-0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer , configuration of SFT[1-0] ignored
	26-16	SFID1[10-0]	Standard Filter ID 1 When filtering for Rx Buffers this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used.
	15-11	RES	Reserved
	10-0	SFID2[10-0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: • 1) SFEC = 001 - 110 Second ID of standard ID filter element • 2) SFEC = 111 Filter for Rx Buffers

Table 12-276. Standard Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
		SFID2[10-9]	This field is decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		SFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.
		SFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.5.1.4.10.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address MCAN_XIDFC[15-2] FLESA field plus two times the index of the filter element (0-63).

Figure 12-298 shows Extended Message ID Filter element structure.

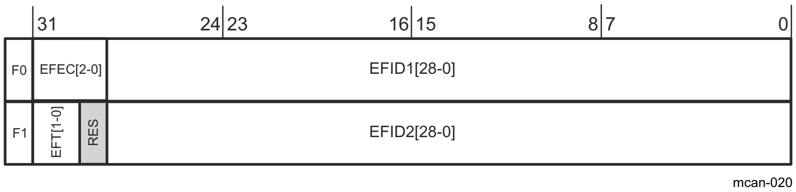

Figure 12-298. Extended Message ID Filter Element Structure

Table 12-265 shows Extended Message ID Filter element field descriptions.

Table 12-277. Extended Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
F0	31-29	EFEC[2-0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer or as debug message, configuration of EFT[1-0] ignored
	28-0	EFID1[28-0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx Buffers this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Section 12.5.1.4.7.1.5 , *Extended Message ID Filtering*) is used.
F1	31-30	EFT[1-0]	Extended Filter Type • 0h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) • 1h = Dual ID filter for EFID1 or EFID2 • 2h = Classic filter: EFID1 = filter, EFID2 = mask • 3h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	29	RES	Reserved
	28-0	EFID2[28-0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: • 1) EFEC = 001 - 110 Second ID of extended ID filter element • 2) EFEC = 111 Filter for Rx Buffers

Table 12-277. Extended Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
		EFID2[10-9]	This field decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		EFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.
		EFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.5.2 Enhanced Capture (ECAP) Module

This section describes the Enhanced Capture (ECAP) module in the device.

12.5.2.1 ECAP Overview

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

Figure 12-299 shows the ECAP modules overview.

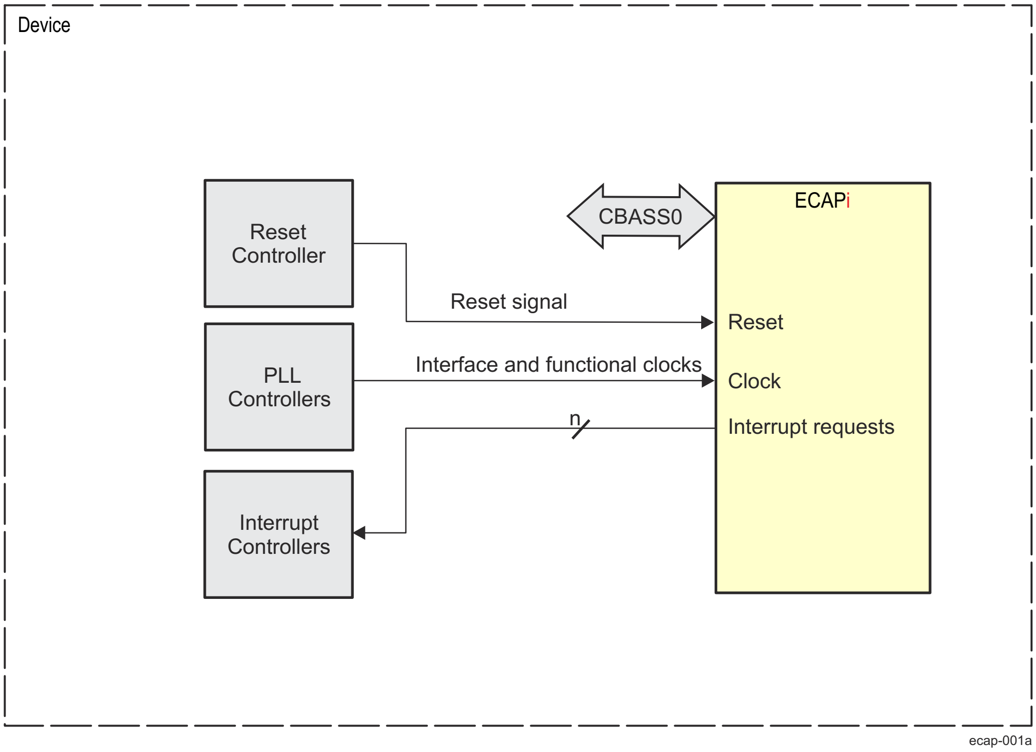

Note

i = 0 to number of instances - 1.

Figure 12-299. ECAP Overview

12.5.2.1.1 ECAP Features

The ECAP module includes the following features:

- 32-bit time base counter
- 4 × 32 bits event time-stamp capture registers (ECAP0_CAP1 through ECAP0_CAP4)
- 4-stage sequencer (Mod4 counter), synchronized to external events (ECAPx pin edges)
- Independent edge polarity (rising / falling edge) selection for all 4 sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Interrupt capabilities on any of the 4 capture events
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

12.5.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.5.2.2 ECAP Environment

12.5.2.2.1 ECAP I/O Interface

This section describes the ECAP external connections (environment).

Figure 12-300 shows the ECAP interface signals.

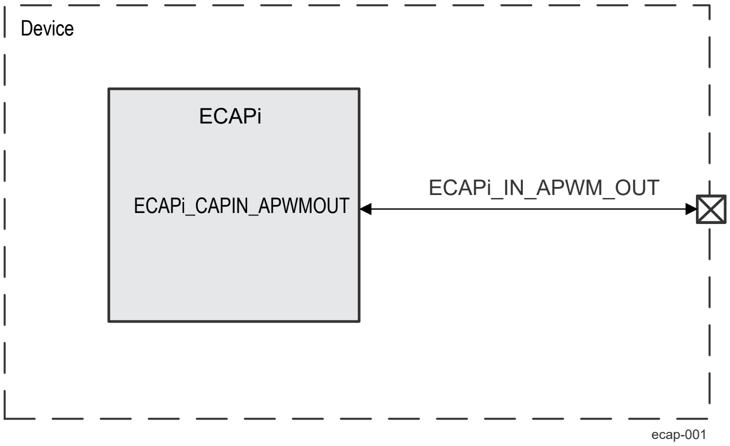

Note

i represents an ECAP instance. See the device datasheet for available domains and ECAP instances

Figure 12-300. ECAP External Interface I/Os

Table 12-266 describes the ECAP I/O signals.

Table 12-278. ECAP I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
		ECAPi(3)		
ECAPi(3)_CAPIN_APWMOUT	ECAPi(3)_IN_APWM_OUT	I/O	ECAPi(3) Capture input / PWM output	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) i represents an ECAP instance. See the device datasheet for available domains and ECAP instances

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.5.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.2.4 ECAP Functional Description

The ECAP module represents one complete capture channel, which has the following independent key resources:

- Dedicated input capture pin
- 32 events selection mapping capability to the input capture pin
- 32-bit time base counter
- 4 × 32-bit time-stamp capture registers (ECAP0_CAP1 through ECAP0_CAP4)
- 4-stage sequencer (Mod4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Input capture signal prescaling (from 2-62)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Control for continuous time-stamp captures using a 4-deep circular buffer (ECAP0_CAP1 through ECAP0_CAP4) scheme
- Interrupt capabilities on any of the 4 capture events

Multiple identical ECAP modules can be contained in a system as shown in Figure 12-301. For actual number of the ECAP modules integrated in the device, refer to *ECAP Integration*. The letter x within a signal or module name is used to indicate a generic ECAP instance on a device. For example, output interrupt request, ECAP1INT belongs to ECAP1, ECAP2INT belongs to ECAP2, and so forth.

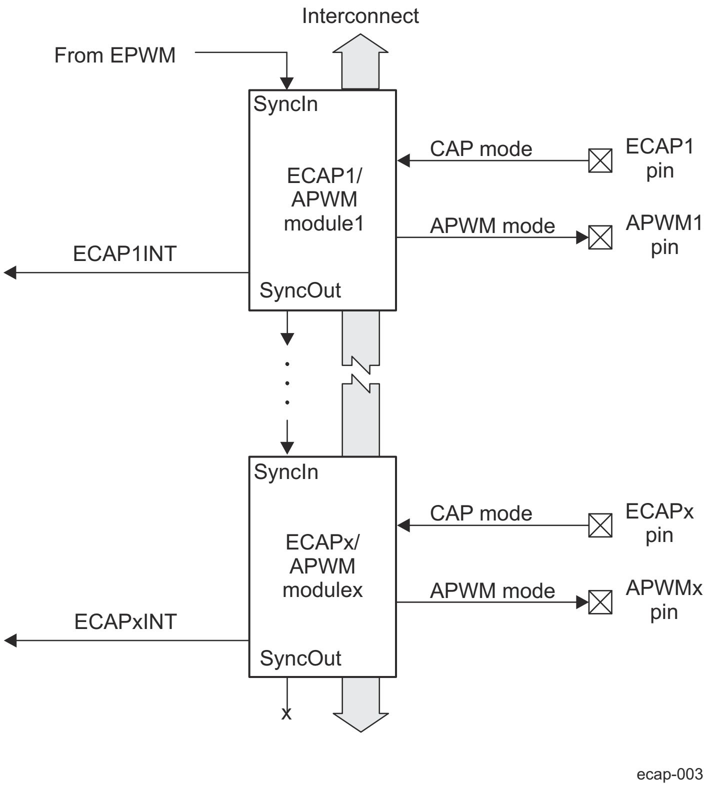

Figure 12-301. Multiple ECAP Modules

12.5.2.4.1 Capture and APWM Operating Modes

The ECAP module resources can be used to implement a single-channel PWM generator (with 32-bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The ECAP0_CAP1 and ECAP0_CAP2 registers become the active period and compare registers, respectively, while the ECAP0_CAP3 and ECAP0_CAP4 registers become the period and capture shadow registers, respectively. Figure 12-302 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

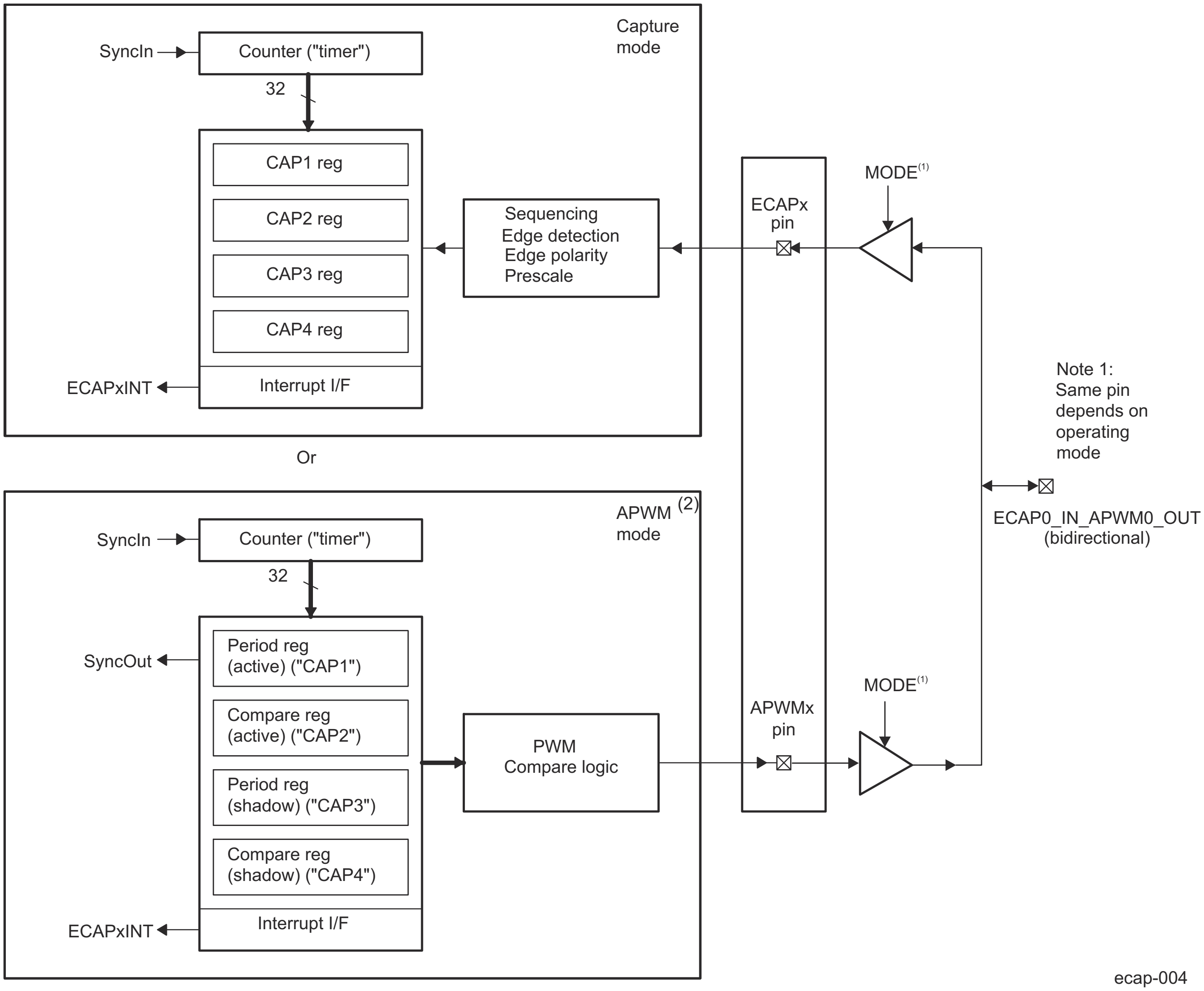

Note

A single pin is shared between CAP and APWM functions. In capture mode, it is an input. In APWM mode, it is an output.

Note

In APWM mode, writing any value to the ECAP0_CAP1/ECAP0_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) invokes the shadow mode.

Figure 12-302. Capture and APWM Modes of Operation

12.5.2.4.1.1 ECAP Capture Mode Description

Figure 12-303 shows the various components that implement the capture function.

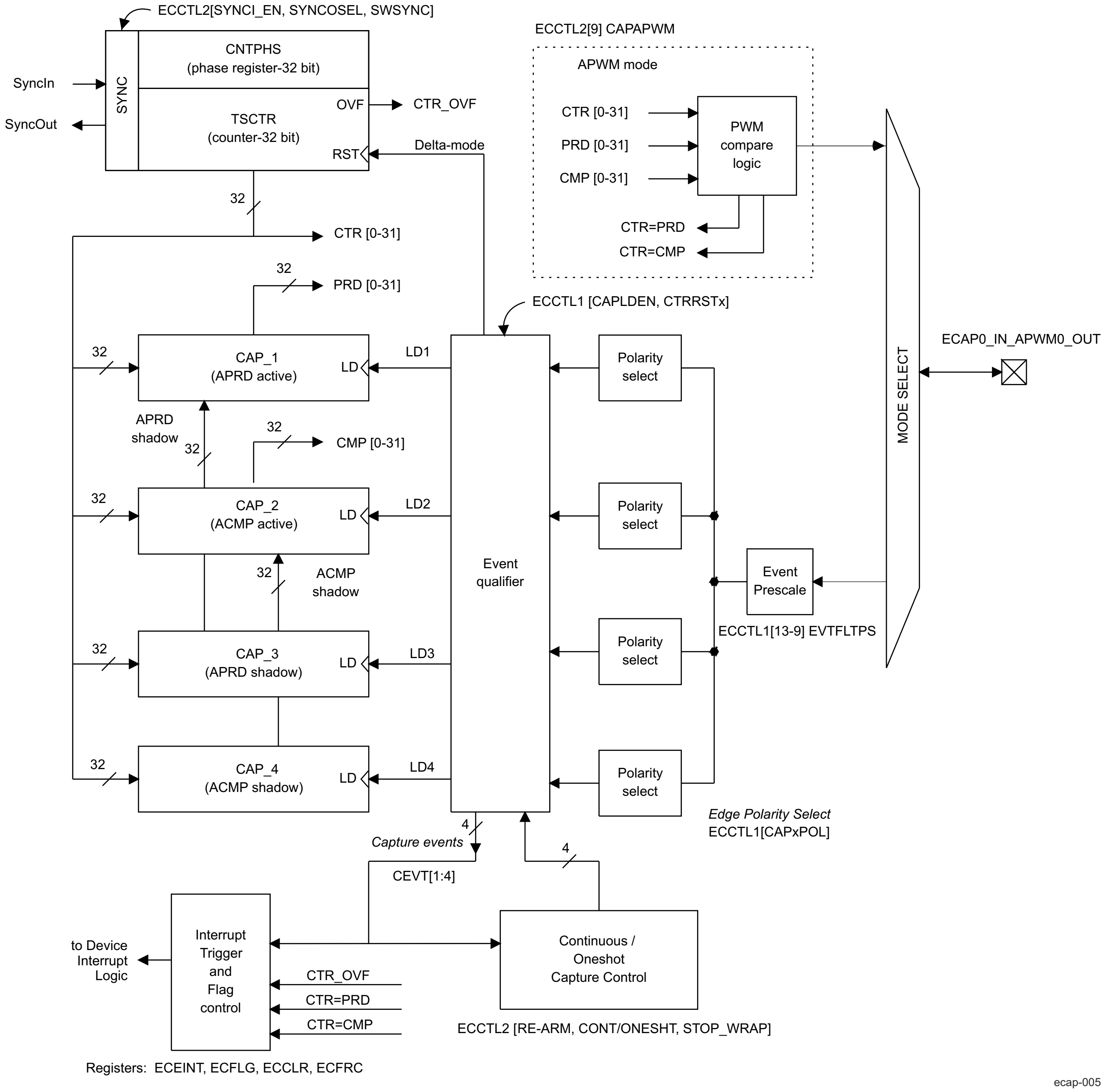

Figure 12-303. Capture Function Diagram

12.5.2.4.1.1.1 ECAP Event Prescaler

An input capture signal (pulse train) can be prescaled by N = 2-62 (in multiples of 2) or can bypass the prescaler. This is useful when very high frequency signals are used as inputs. Figure 12-304 shows a functional diagram and Figure 12-305 shows the operation of the prescale function.

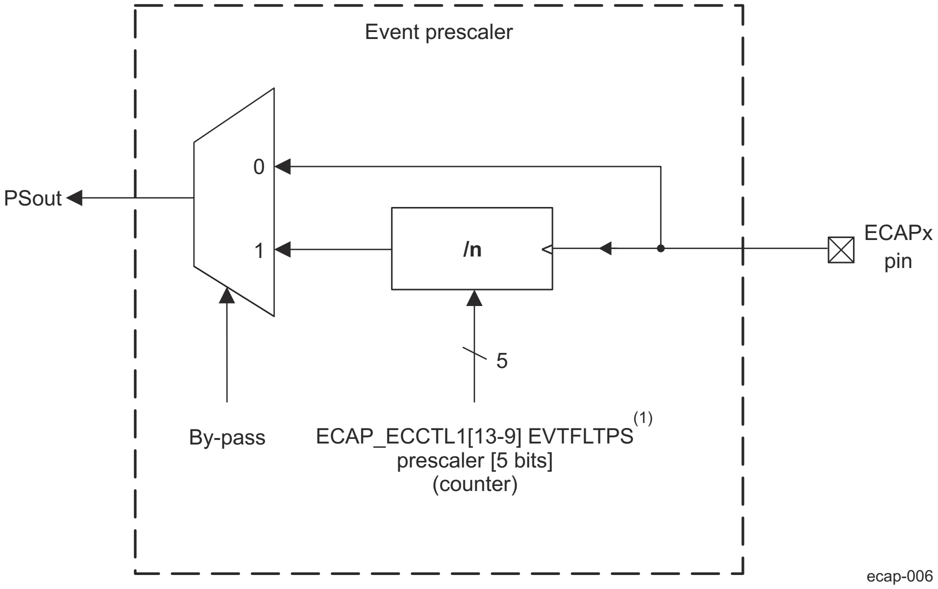

Note

When a prescale value of 1 is chosen (ECAP0_ECCTL[13-9] EVTFLTPS = 0b0000) the input capture signal by-passes the prescale logic completely.

Figure 12-304. Event Prescale Control

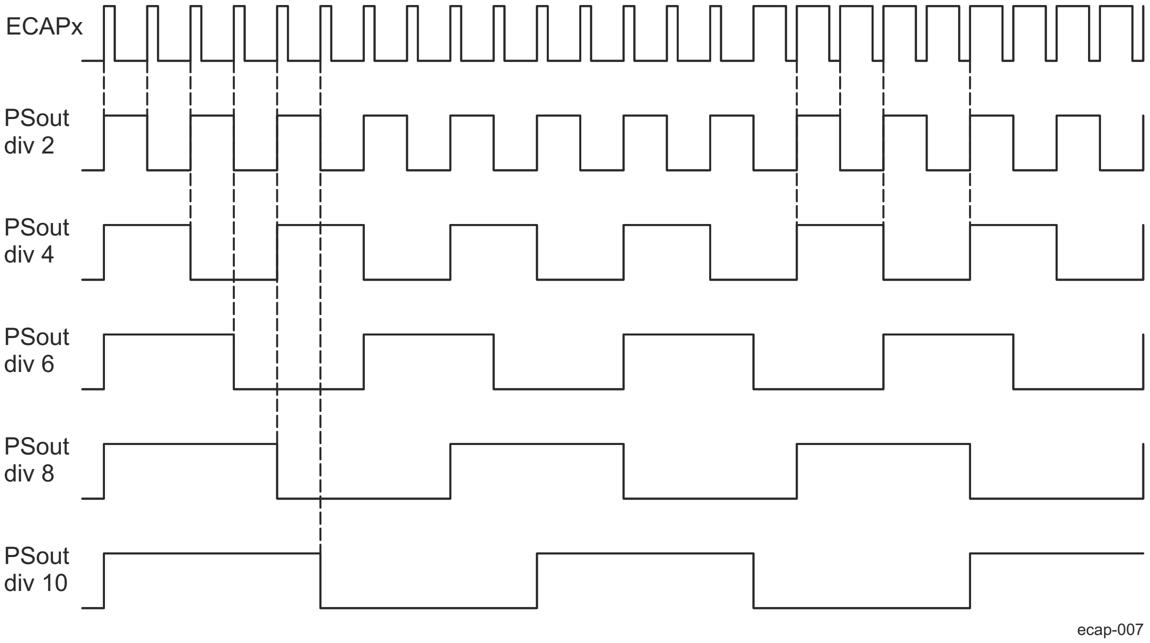

Figure 12-305. Prescale Function Waveforms

12.5.2.4.1.1.2 ECAP Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection multiplexers are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Mod4 sequencer.
- The edge event is gated to its respective CAP*n* register by the Mod4 counter. The CAP*n* register is loaded on the falling edge.

12.5.2.4.1.1.3 ECAP Continuous/One-Shot Control

- The Mod4 (2-bit) counter is incremented via edge qualified events CEVT1 through CEVT4 (see the ECAP0_ECINT_EN_FLG register).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output; when equal the Mod4 counter stops and inhibits further loads of the ECAP0_CAP1 through ECAP0_CAP4 registers. This occurs during one-shot operation.

The continuous/one-shot block (Figure 12-306) controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the ECAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of the ECAP0_CAP1 through ECAP0_CAP4 registers (time-stamps).

Re-arming prepares the ECAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of the ECAP0_CAP1 through ECAP0_CAP4 registers again, providing the ECAP0_ECCTL[8] CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0), the one-shot action is ignored, and capture values continue to be written to the ECAP0_CAP1 through ECAP0_CAP4 registers in a circular buffer sequence.

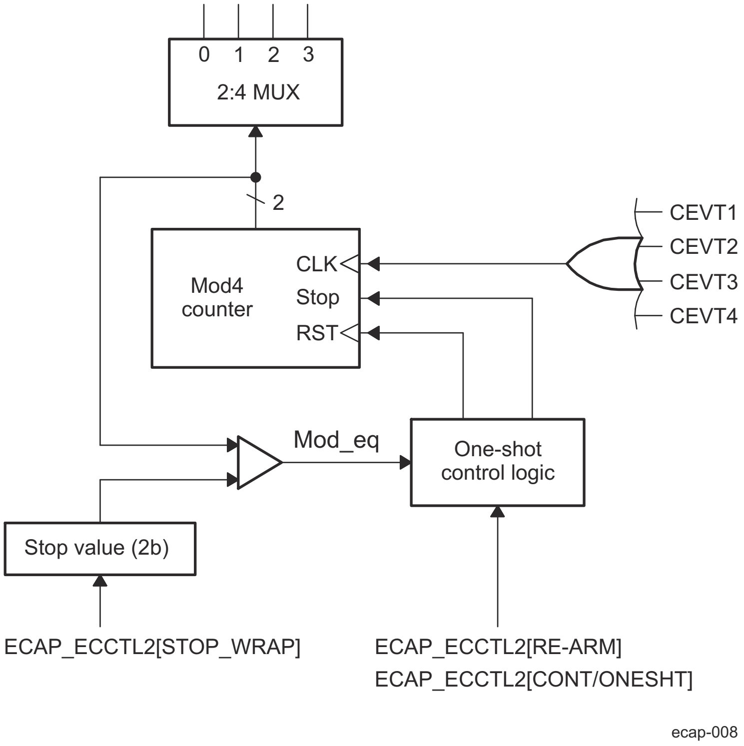

Figure 12-306. ECAP Continuous/One-shot Block Diagram

12.5.2.4.1.1.4 ECAP 32-Bit Counter and Phase Control

This counter (Figure 12-307) provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1 through LD4 signals.

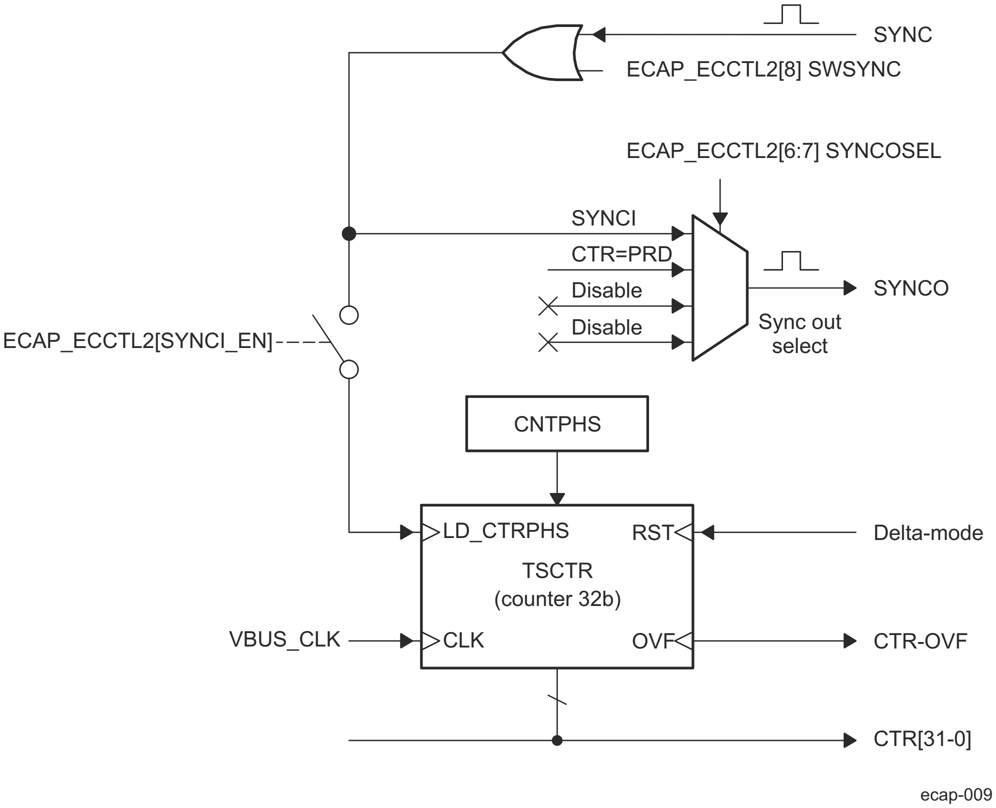

Figure 12-307. ECAP Counter and Synchronization Block Diagram

12.5.2.4.1.1.5 CAP1-CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0-31] and are loaded (capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via the control ECAP0_ECCTL[8] CAPLDEN bit. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

The ECAP0_CAP1 and ECAP0_CAP2 registers become the active period and compare registers, respectively, in APWM mode.

The ECAP0_CAP3 and ECAP0_CAP4 registers become the respective shadow registers (APRD and ACMP) for the ECAP0_CAP1 and ECAP0_CAP2 registers during APWM operation.

12.5.2.4.1.1.6 ECAP Interrupt Control

An interrupt can be generated on capture events CEVT1 through CEVT4, CNTOVF (see the ECAP0_ECINT_EN_FLG[21] CNTOVF_FLG bit) or APWM events (TSCNT = PRD, TSCNT = CMP). See Figure 12-308.

A counter overflow event (FFFF FFFFh->0000 0000h) is also provided as an interrupt source (CNTOVF).

The capture events are edge and sequencer qualified (that is, ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the ECAP*n* module) going to the interrupt controller.

Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CNTOVF, TSCNT = PRD, TSCNT = CMP) can be generated. The interrupt enable register (ECAP0_ECINT_EN_FLG) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECAP0_ECINT_EN_FLG) indicates if any interrupt event has been latched and contains the global interrupt flag ECAP0_ECINT_EN_FLG[16] INT_FLG bit. An interrupt pulse is generated to the interrupt controller only if any of the interrupt events are enabled, the flag bit is 1h, and the INT_FLG flag bit is 0h. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (ECAP0_ECINT_CLR_FRC) before any other interrupt pulses are generated. The interrupt force register (ECAP0_ECINT_CLR_FRC) can force an interrupt event. This is useful for test purposes.

12.5.2.4.1.1.7 ECAP Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of the ECAP0_CAP1 or ECAP0_CAP2 registers from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate - APRD or ACMP are transferred to the ECAP0_CAP1 or ECAP0_CAP2 register immediately upon writing a new value.
- On period equal, CTR[31-0] = PRD[31-0]

Note

The CEVT1_FLG, CEVT2_FLG, CEVT3_FLG, CEVT4_FLG flags are only active in capture mode (ECAP0_ECCTL[25] CAP_APWM == 0h). The TSCNT = PRD, TSCNT = CMP flags are only valid in APWM mode (ECAP0_ECCTL[25] CAP_APWM == 1h). CNTOVF_FLG flag is valid in both modes.

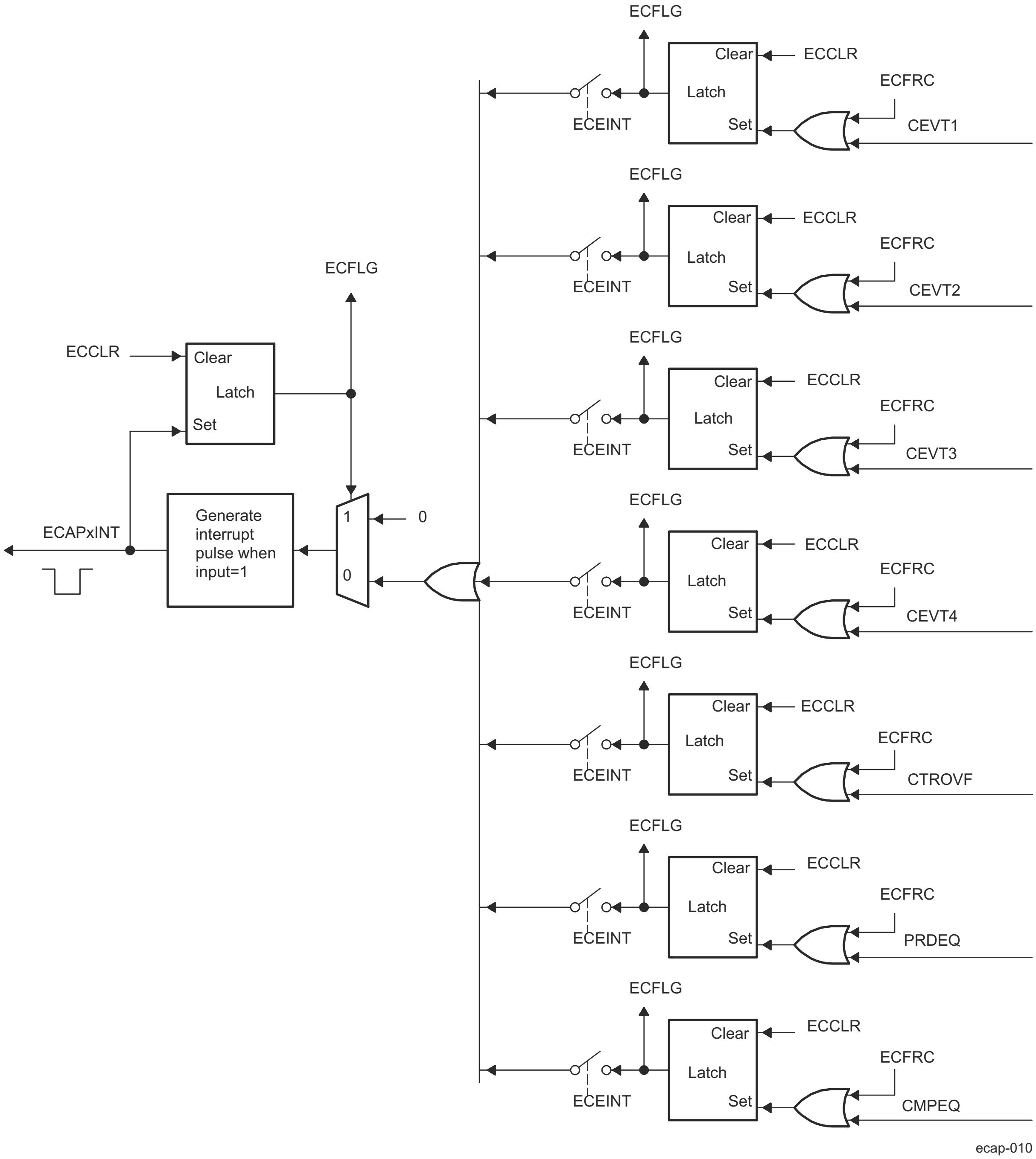

Figure 12-308. Interrupts in ECAP Module

12.5.2.4.1.2 ECAP APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When the ECAP0_CAP1/ECAP0_CAP2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via the shadow registers - APRD and ACMP (ECAP0_CAP3/ECAP0_CAP4). The shadow register contents are transferred over to ECAP0_CAP1/ECAP0_CAP2 registers either immediately upon a write, or on a TSCNT = PRD trigger.
- In APWM mode, writing to the ECAP0_CAP1/ECAP0_CAP2 active registers will also write the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) will invoke the shadow mode.
- During initialization, software must write the PRD and CMP values to the active registers. This automatically copies the initial values into the shadow values. For subsequent compare updates, during run-time, software should use only shadow registers.

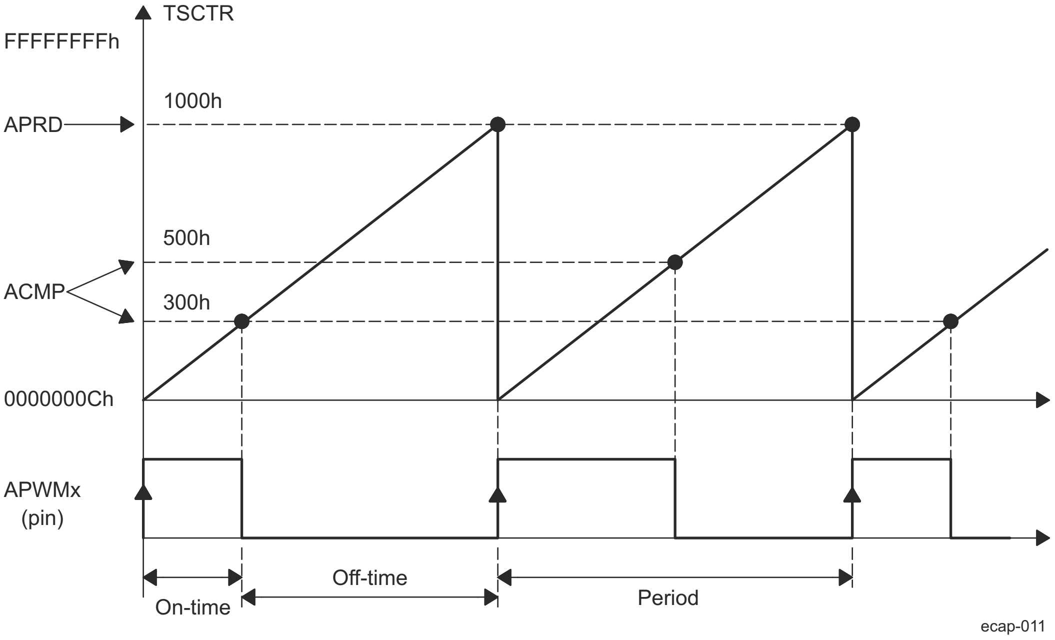

Figure 12-309. PWM Waveform Details of ECAP APWM Mode Operation

The behavior of APWM active-high mode (APWMPOL == 0) is:

```
CMP = 0x00000000, output low for duration of period (0% duty)
```

```
CMP = 0x00000001, output high 1 cycle
```

```
CMP = 0x00000002, output high 2 cycles
```

```
CMP = PERIOD, output high except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output high for complete period (100% duty)
```

```
CMP > PERIOD+1, output high for complete period
```

The behavior of APWM active-low mode (APWMPOL == 1) is:

```
CMP = 0x00000000, output high for duration of period (0% duty)
```

```
CMP = 0x00000001, output low 1 cycle
```

```
CMP = 0x00000002, output low 2 cycles
```

```
CMP = PERIOD, output low except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output low for complete period (100% duty)
```

```
CMP > PERIOD+1, output low for complete period
```

12.5.2.4.2 Summary of ECAP Functional Registers

Table 12-267 shows the ECAP module control and status register set. All 32-bit registers are aligned on even address boundaries and are organized in little-endian mode.

Note

In APWM mode, writing to the ECAP0_CAP1/ECAP0_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) invokes the shadow mode.

Table 12-279. ECAP Control and Status Functional Registers

Offset	Register Name	Description	Size (×16)
0h	ECAP0_TSCNT	Time-Stamp Counter Register	2
4h	ECAP0_CNTPHS	Counter Phase Offset Value Register	2
8h	ECAP0_CAP1	Capture 1 Register	2
Ch	ECAP0_CAP2	Capture 2 Register	2
10h	ECAP0_CAP3	Capture 3 Register	2
14h	ECAP0_CAP4	Capture 4 Register	2
28h	ECAP0_ECCTL	Capture Control Register	2
2Ch	ECAP0_ECINT_EN_FLG	Capture Interrupt Enable and Flag Register	2
30h	ECAP0_ECINT_CLR_FRC	Capture Interrupt Clear and Forcing Register	2
5Ch	ECAP0_PID	Revision ID Register	2

Note

For more information on the ECAP registers, see *ECAP Registers.*

12.5.2.5 ECAP Use Cases

The following sections will provide applications examples and code snippets to show how to configure and operate the ECAP module. For clarity and ease of use, below are useful #defines which will help in the understanding of the examples.

```
// ECCTL1 ( ECAP Control Reg 1)
//==========================
// CAPxPOL bits
#defineEC_RISING      0x0
#defineEC_FALLING     0x1
// CTRRSTx bits
#defineEC_ABS_MODE    0x0
#defineEC_DELTA_MODE      0x1
// PRESCALE bits
#defineEC_BYPASS      0x0
#defineEC_DIV1        0x0
#defineEC_DIV2        0x1
#defineEC_DIV4        0x2
#defineEC_DIV6        0x3
#defineEC_DIV8        0x4
#defineEC_DIV10       0x5
// ECCTL2 ( ECAP Control Reg 2)
//==========================
// CONT/ONESHOT bit
#defineEC_CONTINUOUS      0x0
#defineEC_ONESHOT     0x1
// STOPVALUE bit
#defineEC_EVENT1      0x0
#defineEC_EVENT2      0x1
#defineEC_EVENT3      0x2
#defineEC_EVENT4      0x3
// RE-ARM bit
#defineEC_ARM         0x1
// TSCTRSTOP bit
#defineEC_FREEZE      0x0
#defineEC_RUN         0x1
// SYNCO_SEL bit
#defineEC_SYNCIN      0x0
#defineEC_CTR_PRD     0x1
#defineEC_SYNCO_DIS       0x2
// CAP/APWM mode bit
#defineEC_CAP_MODE    0x0
#defineEC_APWM_MODE       0x1
// APWMPOL bit
#defineEC_ACTV_HI     0x0
#defineEC_ACTV_LO     0x1
// Generic
#defineEC_DISABLE     0x0
#defineEC_ENABLE      0x1
#defineEC_FORCE       0x1
```

12.5.2.5.1 Absolute Time-Stamp Operation Rising Edge Trigger Example

Figure 12-310 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFF FFFFh (maximum value), it wraps around to 0000 0000h (not shown in Figure 12-310), if this occurs, the CNTOVF_FLG (counter overflow) flag is set, and an interrupt (if enabled) occurs. Captured time-stamps are valid at the point indicated by the diagram, after the 4-th event, hence event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAP*n* registers.

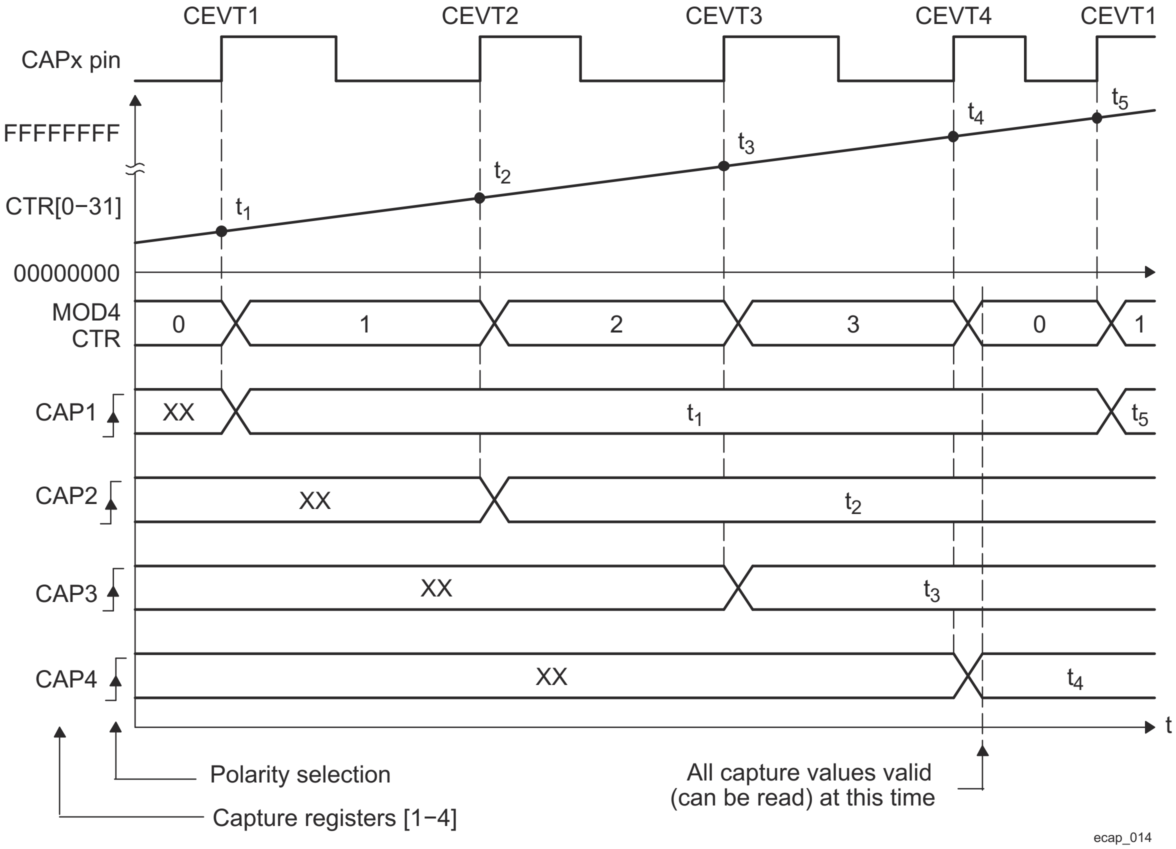

Figure 12-310. Capture Sequence for Absolute Time-Stamp, Rising Edge Detect

Table 12-280. ECAP Initialization for CAP Mode Absolute Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Absolute Time, Rising Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt2-TSt1;// Calculate 1st period
Period2 = TSt3-TSt2;// Calculate 2nd period
Period3 = TSt4-TSt3;// Calculate 3rd period
```

12.5.2.5.2 Absolute Time-Stamp Operation Rising and Falling Edge Trigger Example

In Figure 12-311 the ECAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, …etc. Duty Cycle1 (on-time %) = $(t_2 - t_1)$ / Period1 x 100%, etc. Duty Cycle1 (off-time %) = $(t_3 - t_2)$ / Period1 x 100%, etc.

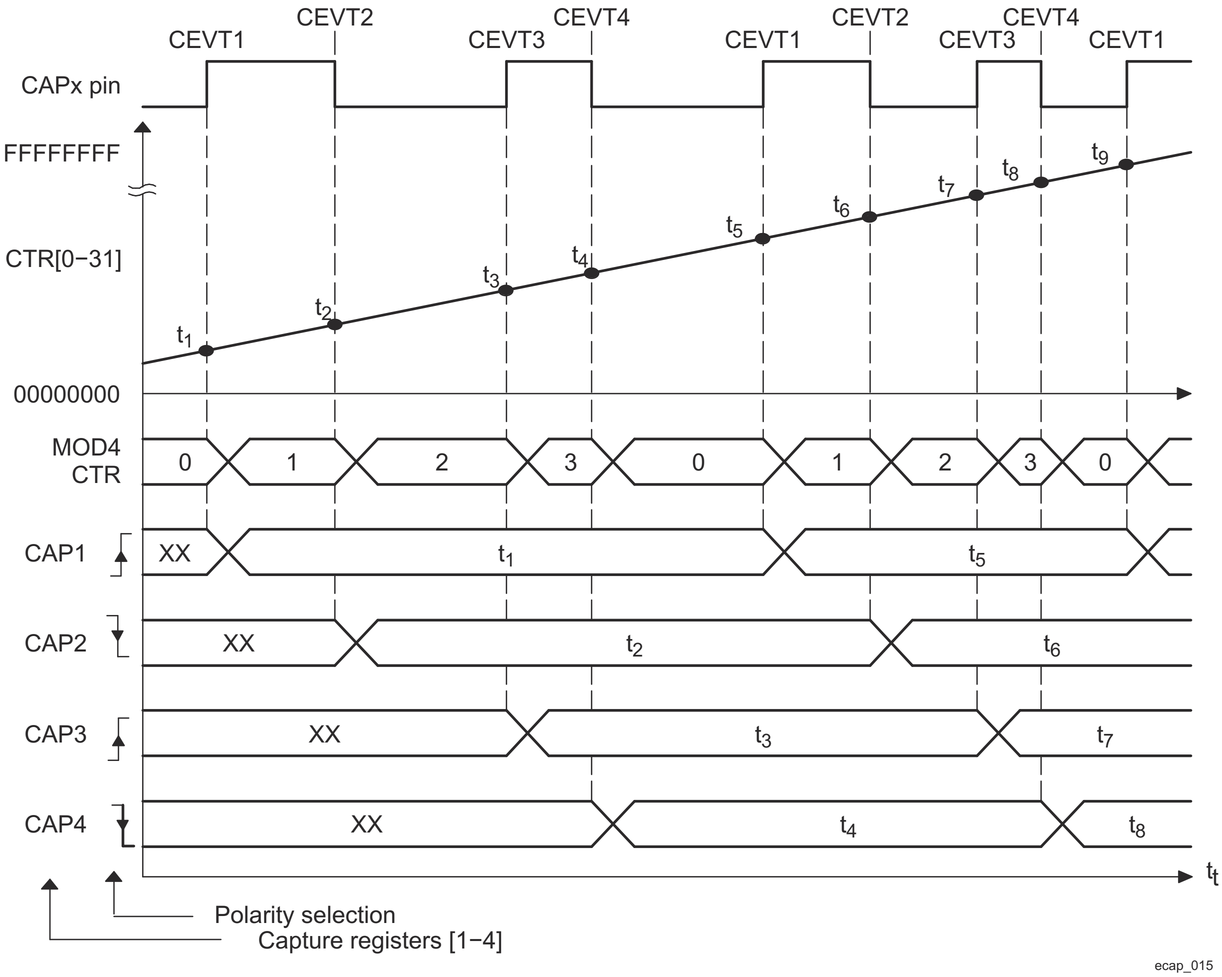

Figure 12-311. Capture Sequence for Absolute Time-Stamp, Rising and Falling Edge Detect

Table 12-281. ECAP Initialization for CAP Mode Absolute Time, Rising and Falling Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Absolute Time, Rising and Falling Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising & Falling edge triggers
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt3-TSt1;// Calculate 1st period
DutyOnTime1 = TSt2-TSt1;// Calculate On time
DutyOffTime1 = TSt3-TSt2;// Calculate Off time
```

12.5.2.5.3 Time Difference (Delta) Operation Rising Edge Trigger Example

Figure 12-312 shows how the ECAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is Reset back to Zero on every valid event. Here Capture events are qualified as Rising edge only. On an event, TSCTR contents (time-stamp) is captured first, and then TSCTR is reset to Zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFF FFFFh (maximum value), before the next event, it wraps around to 0000 0000h and continues, a CNTOVF_FLG (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAP*n* contents directly give timing data without the need for CPU calculations: Period1 = T_1, Period2 = T_2,…etc. As shown in Figure 12-312, the CEVT1 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

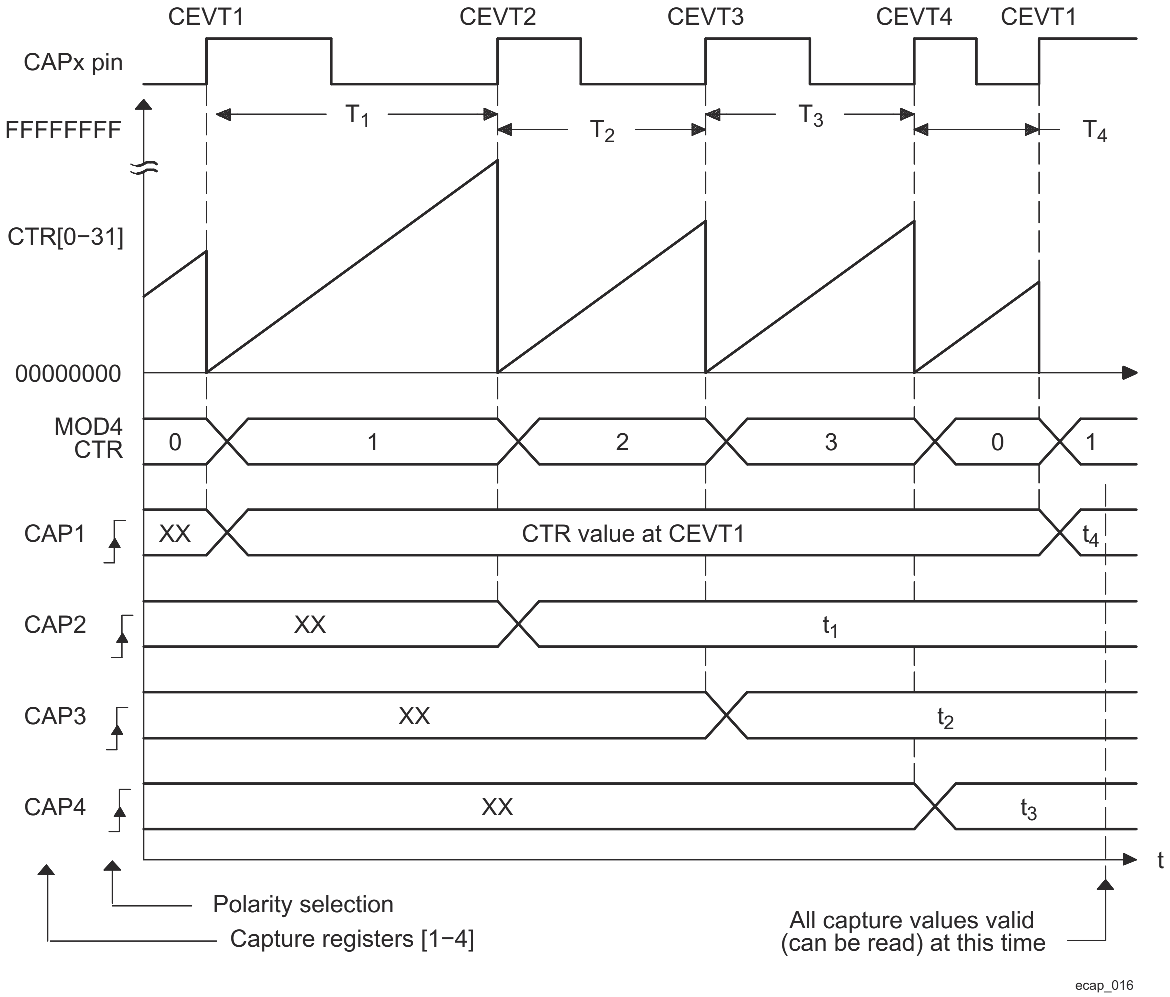

Figure 12-312. Capture Sequence for Delta Mode Time-Stamp, Rising Edge Detect

Table 12-282. ECAP Initialization for CAP Mode Delta Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Delta Time, Rising Edge Trigger

```
// Code snippet for CAP mode Delta Time, Rising edge trigger
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Period value.
Period4 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
Period2 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
Period3 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
```

12.5.2.5.4 Time Difference (Delta) Operation Rising and Falling Edge Trigger Example

In Figure 12-313 the ECAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information: Period1 = T_1 + T_2, Period2 = T_3 + T_4, …etc Duty Cycle1 (on-time %) = T_1 / Period1 × 100%, etc Duty Cycle1 (off-time %) = T_2 / Period1 × 100%, etc.

During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, that is, during run-time, only the shadow registers must be used.

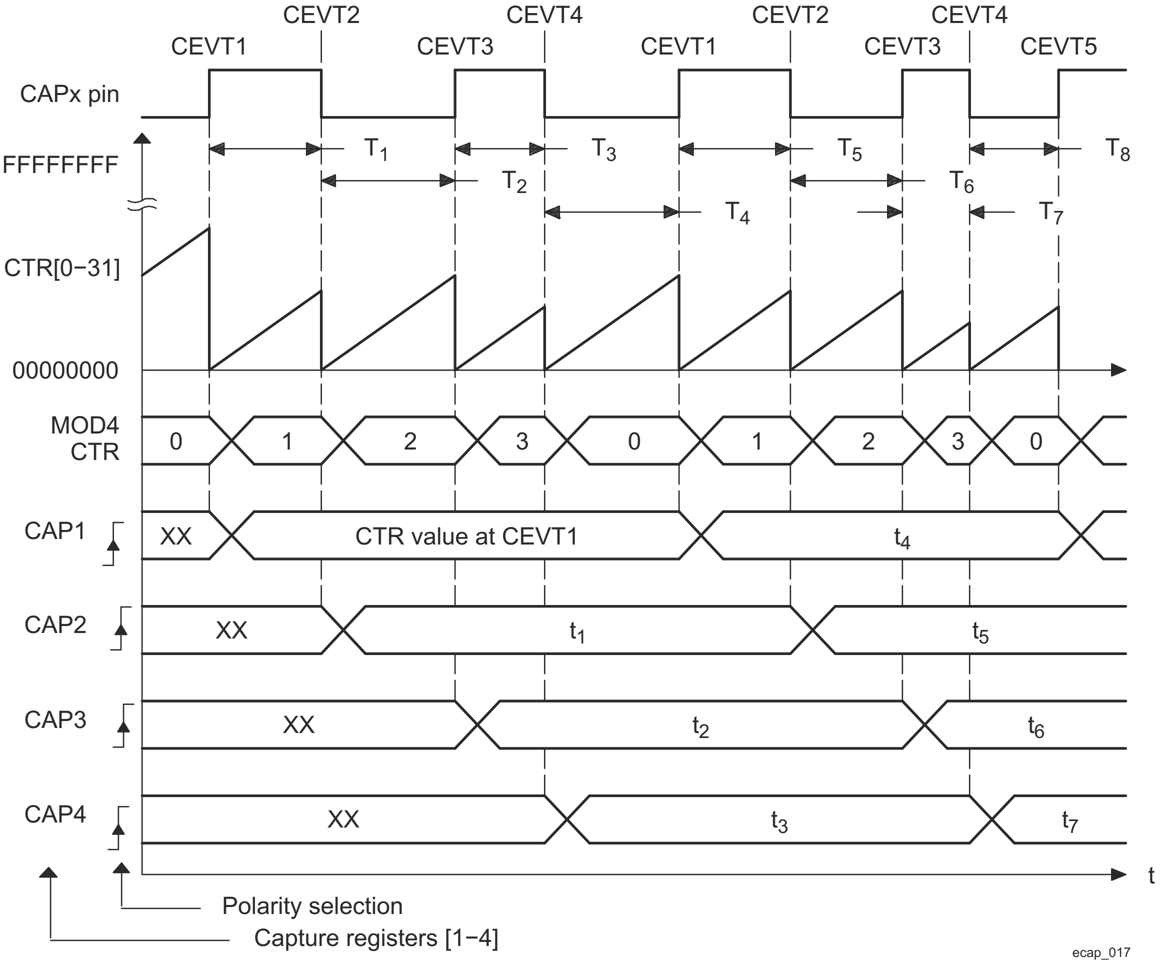

Figure 12-313. Capture Sequence for Delta Mode Time-Stamp, Rising and Falling Edge Detect

Table 12-283. ECAP Initialization for CAP Mode Delta Time, Rising and Falling Edge Triggers

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Delta Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Delta Time, Rising and Falling edge triggers
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Duty cycle values.
DutyOnTime1 =  ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
DutyOffTime1 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
DutyOnTime2 =  ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
DutyOffTime2 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = DutyOnTime1 + DutyOffTime1;
Period2 = DutyOnTime2 + DutyOffTime2;
```

12.5.2.5.5 Application of the APWM Mode

12.5.2.5.5.1 Simple PWM Generation (Independent Channel/s) Example

In this example, the ECAP module is configured to operate as a PWM generator. Here a very simple single channel PWM waveform is generated from output pin APWM*n*. The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time.

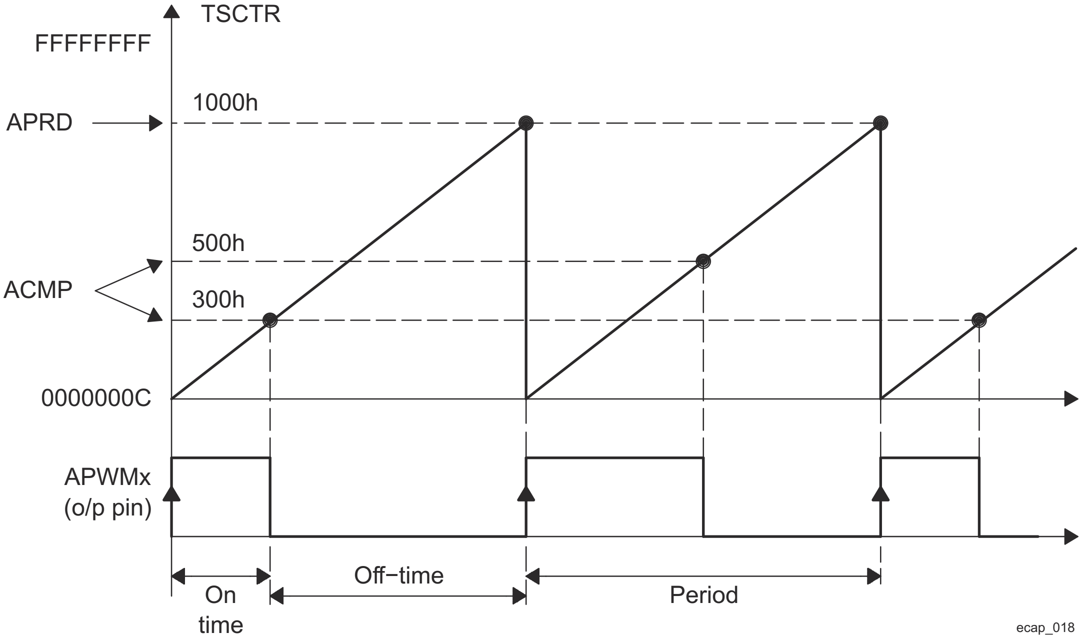

Figure 12-314. PWM Waveform Details of APWM Mode Operation

Table 12-284. ECAP Initialization for APWM Mode

Register	Bit	Value
CAP1	CAP1	0x1000
CTRPHS	CTRPHS	0x0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for APWM Mode

```
// Code snippet for APWM mode Example 1
// Run Time (Instant 1, e.g. ISR call)
//======================
   ECAPxRegs.CAP2 = 0x300;      // Set Duty cycle i.e. compare value
// Run Time (Instant 2, e.g. another ISR call)
//======================
   ECAPxRegs.CAP2 = 0x500;      // Set Duty cycle i.e. compare value
```

12.5.2.5.5.2 Multichannel PWM Generation with Synchronization Example

Figure 12-315 takes advantage of the synchronization feature between the ECAP modules. Here 4 independent PWM channels are required with different frequencies, but at integer multiples of each other to avoid "beat" frequencies. Hence one ECAP module is configured as the Controller and the remaining 3 are Targets all receiving their synch pulse (CTR = PRD) from the controller. Note the Controller is chosen to have the lower frequency (F1 = 1/20,000) requirement. Here Target2 Freq = 2 × F1, Target3 Freq = 4 × F1 and Target4 Freq = 5 × F1. Note here values are in decimal notation. Also, only the APWM1 output waveform is shown.

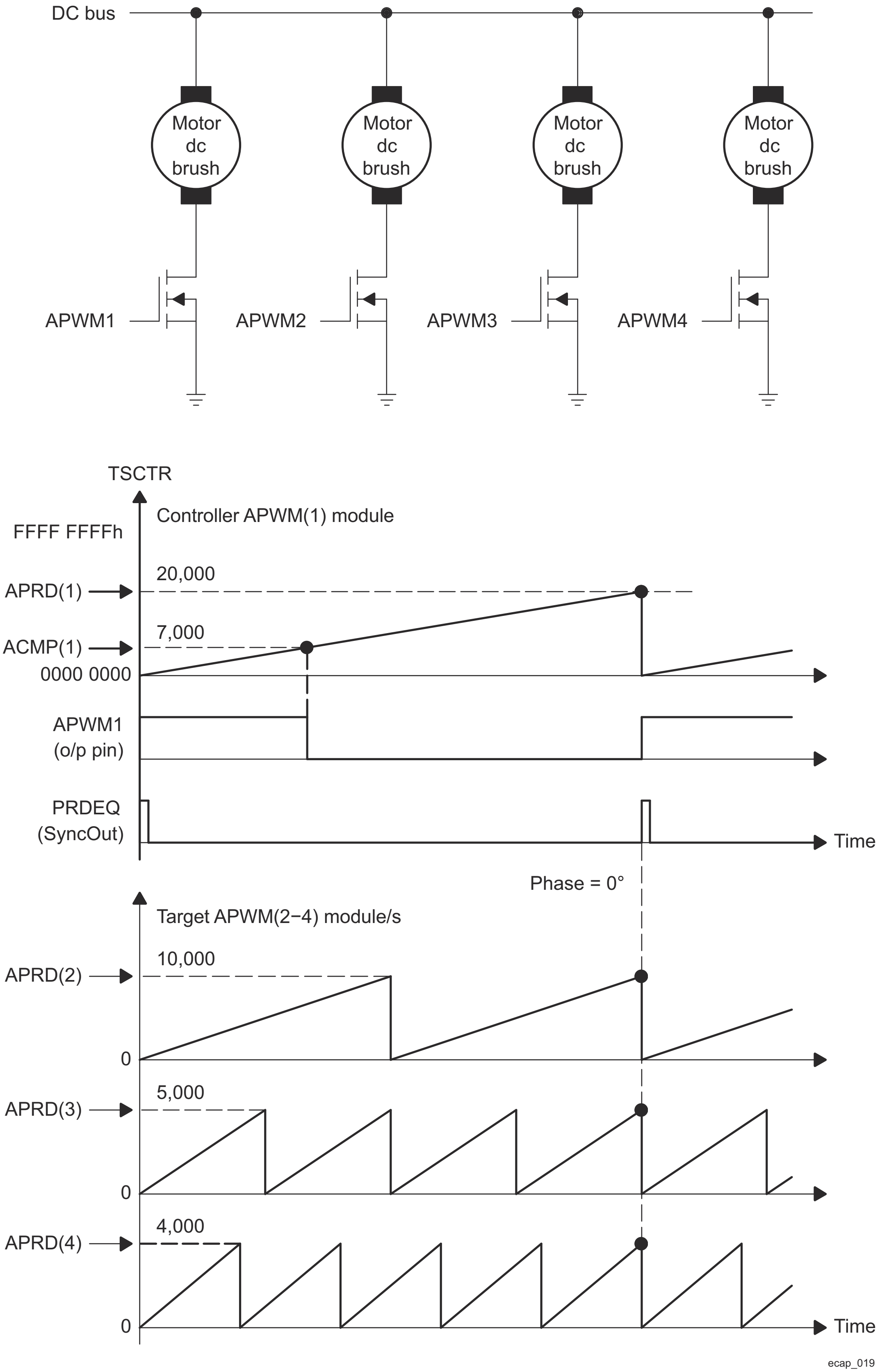

Figure 12-315. Multichannel PWM Example Using 4 ECAP Modules

Table 12-285. ECAP1 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	20000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-286. ECAP2 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	10000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-287. ECAP3 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	5000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-288. ECAP4 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	4000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for Multichannel PWM Generation with Synchronization

```
// Code snippet for APWM mode Example 2
// Run Time (Note: Example execution of one run-time instant)
//============================================================
   ECAP1Regs.CAP2 = 7000;    // Set Duty cycle i.e., compare value = 7000
   ECAP2Regs.CAP2 = 2000;    // Set Duty cycle i.e., compare value = 2000
   ECAP3Regs.CAP2 = 550;     // Set Duty cycle i.e., compare value = 550
   ECAP4Regs.CAP2 = 6500;    // Set Duty cycle i.e., compare value = 6500
```

12.5.2.5.5.3 Multichannel PWM Generation with Phase Control Example

In Figure 12-316, the Phase control feature of the APWM mode is used to control a 3 phase Interleaved DC/DC converter topology. This topology requires each phase to be off-set by 120° from each other. Hence if "Leg" 1 (controlled by APWM1) is the reference Leg (or phase), that is, 0°, then Leg 2 need 120° off-set and Leg 3 needs 240° off-set. The waveforms in Figure 12-316 show the timing relationship between each of the phases (Legs). Note ECAP1 module is the Controller and issues a SyncOut pulse to the targets (modules 2, 3) whenever TSCTR = Period value.

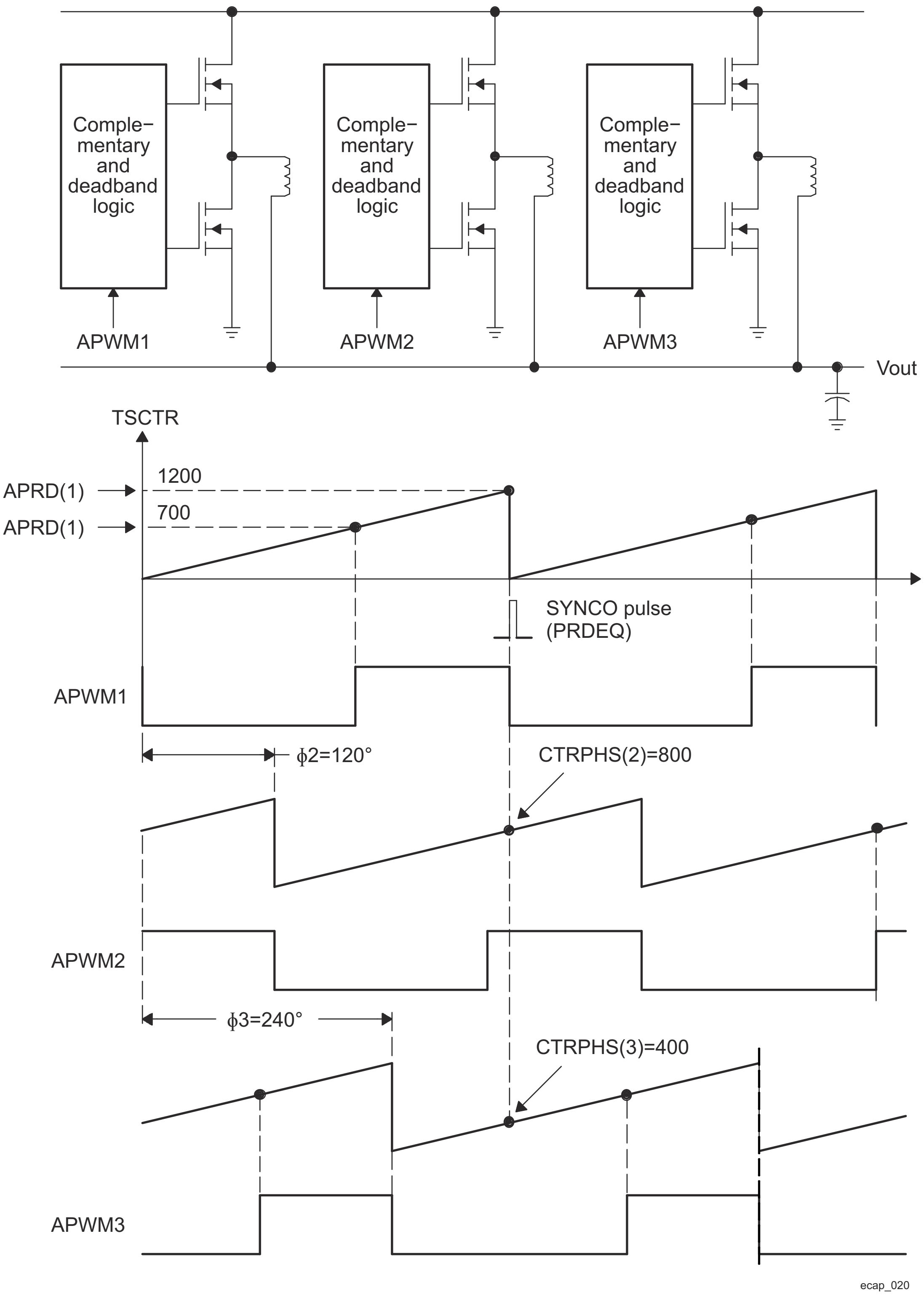

Figure 12-316. Multiphase (channel) Interleaved PWM Example Using 3 ECAP Modules

Table 12-289. ECAP1 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-290. ECAP2 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	800
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-291. ECAP3 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	400
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for Multichannel PWM Generation with Phase Control

```
// Code snippet for APWM mode Example 3
// Run Time (Note: Example execution of one run-time instant)
//=========================================================
// All phases are set to the same duty cycle
  ECAP1Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP2Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP3Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
```

12.5.3 Enhanced Pulse Width Modulation (EPWM) Module

This chapter describes the Enhanced Pulse Width Modulation (EPWM) module in the device.

12.5.3.1 EPWM Overview

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross-coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single-channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description, the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWMx instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

The EPWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB.

As also described in *Daisy-Chain Connectivity between EPWM Modules*, the EPWM modules are chained together via a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the Enhanced Capture (ECAP) peripheral module. The EPWM modules can also operate stand-alone.

Figure 12-317 shows the EPWM module overview.

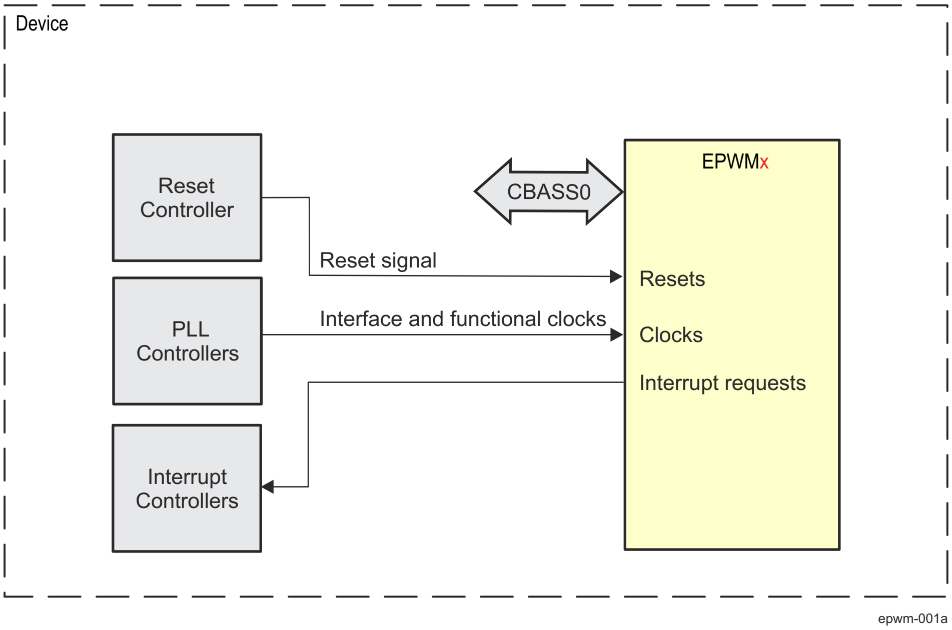

Note

x = 0 to number of instances

Figure 12-317. EPWM Overview

12.5.3.1.1 EPWM Features

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by a high-frequency carrier signal, useful for pulse transformer gate drives

12.5.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.5.3.1.3 Multiple EPWM Module Details

Each EPWM module is connected to the input/output signals shown in Figure 12-318.

The order in which the EPWM modules are connected may differ from what is shown in Figure 12-318. See *Daisy-Chain Connectivity between EPWM Modules* for the actual synchronization scheme implemented in the device. Each EPWM module consists of seven submodules and is connected within a system via the signals shown in Figure 12-319.

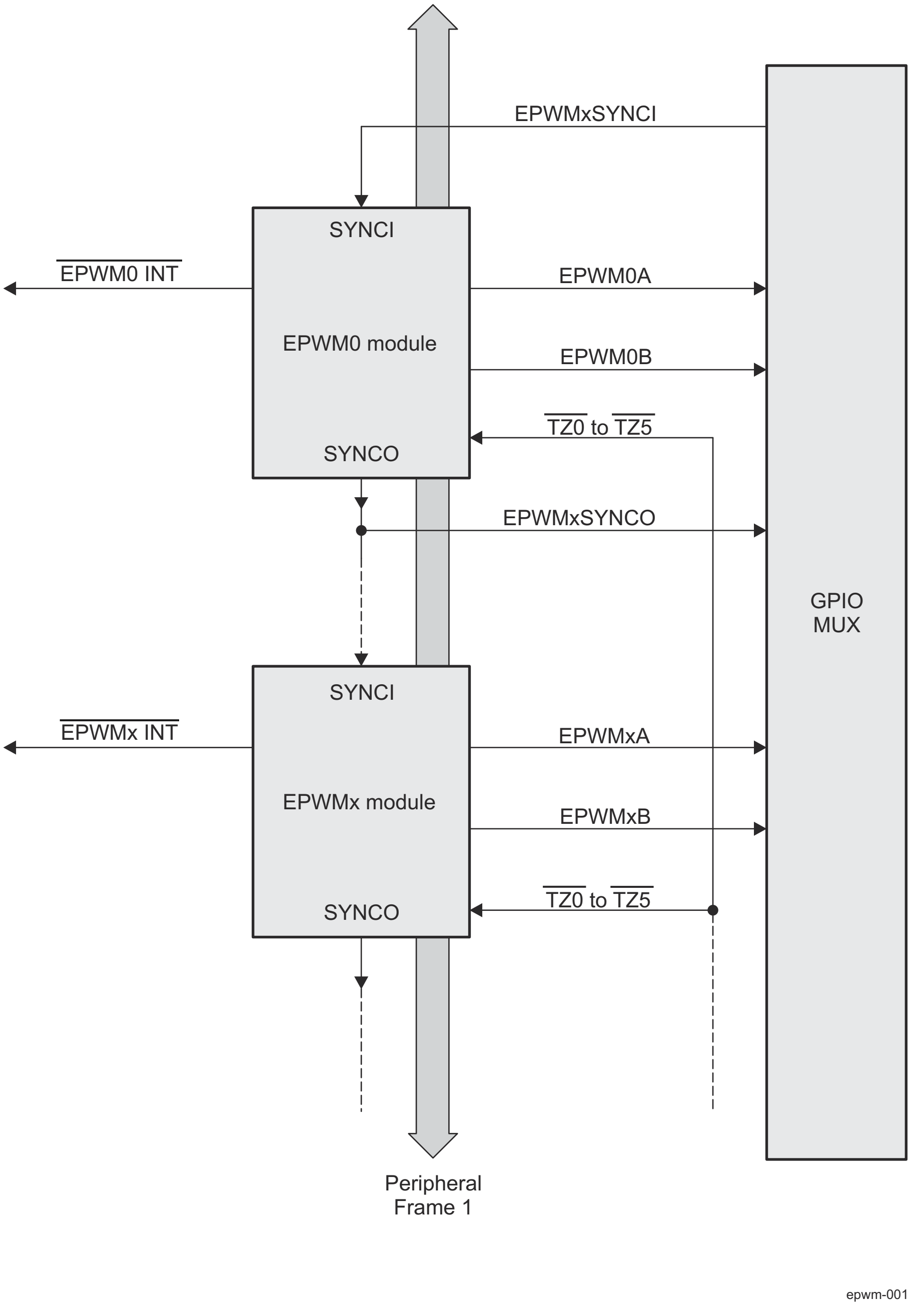

Note

x = 0 to number of instances

Figure 12-318. Multiple EPWM Modules

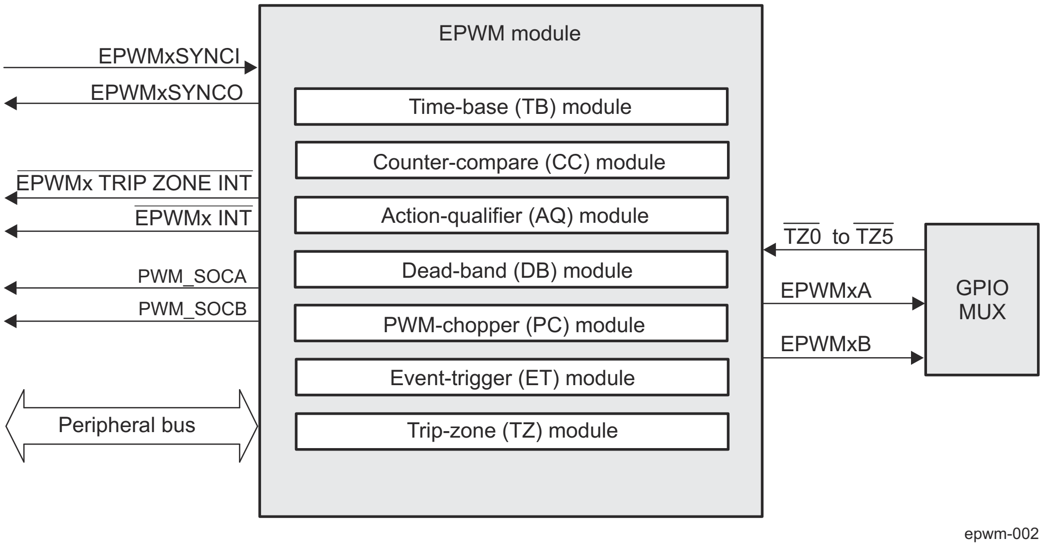

Note

x = 0 to number of instances

Figure 12-319. Submodules and Signal Connections for an EPWM Module

Figure 12-320 shows more internal details of a single EPWM module.

The main signals used by the EPWM module are:

- **PWM output signals (EPWMxA and EPWMxB)**
  The PWM output signals are available external to the device through the GPIO peripheral.
- **Trip-zone signals ($\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$)**
  These input signals alert the EPWM module of an external fault condition. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The trip-zone signal can be configured as an asynchronous input through the GPIO peripheral.
- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals**
  The synchronization signals daisy chain the EPWM modules together. Each module can be configured to either use or ignore its synchronization input. For more information see *Daisy-Chain Connectivity between EPWM Modules*.
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB)**
  Each EPWM module has two ADC start of conversion signals (one for each sequencer). Any EPWM module can trigger a start of conversion for either sequencer. Which event triggers the start of conversion is configured in the Event-Trigger submodule of the EPWM module.
- **Peripheral Bus**
  The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the EPWM registers.

Figure 12-320 also shows the key internal submodule interconnect signals. Each submodule is described in *EPWM Functional Description*.

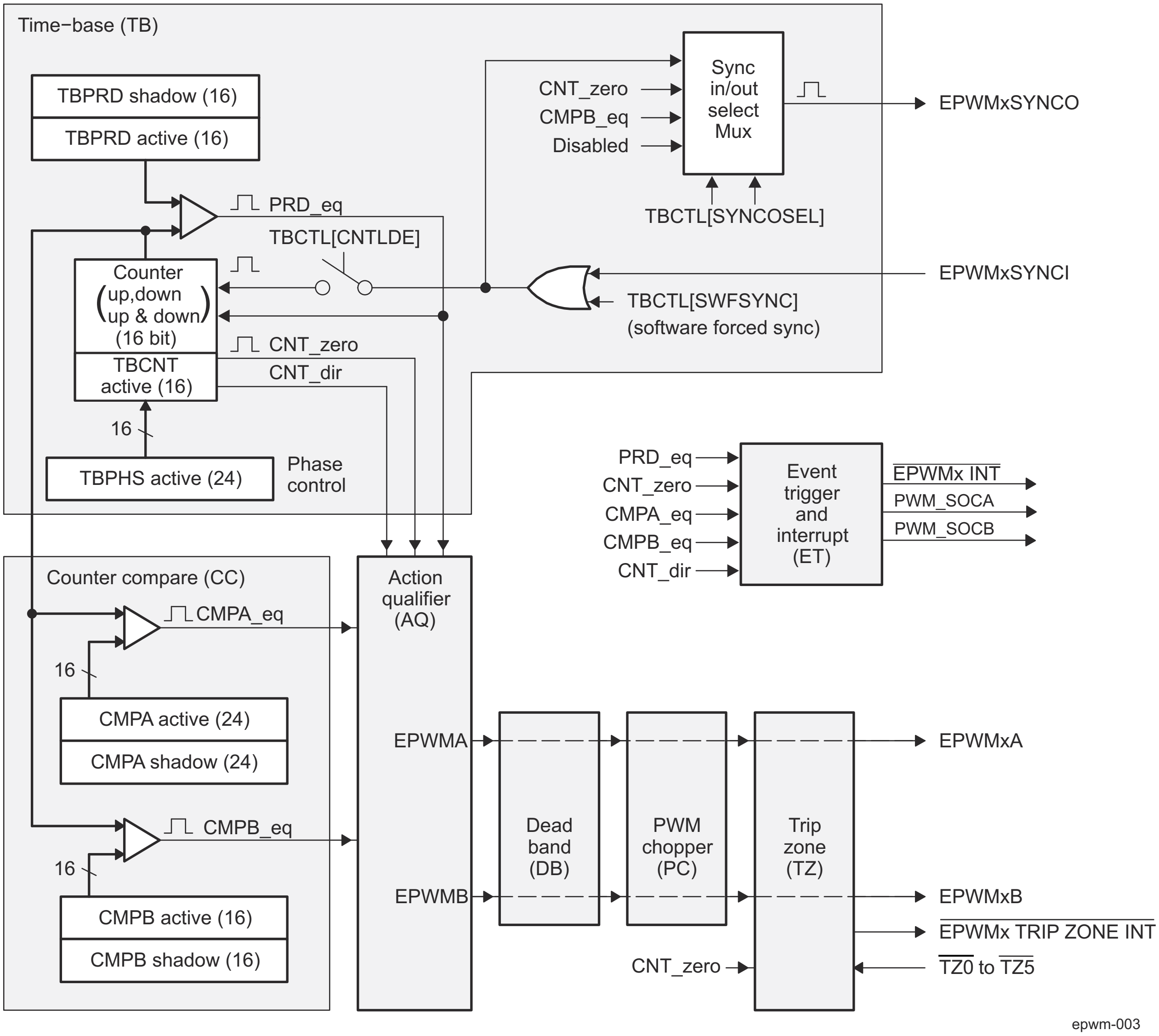

Figure 12-320. EPWM Submodule Interconnect Signals

12.5.3.2 EPWM Environment

The EPWMx (where x = 0 to number of instances) module is hereinafter referred to as EPWM module.

This section describes the EPWM external connections (environment).

Figure 12-321 shows the EPWM I/O interface signals.

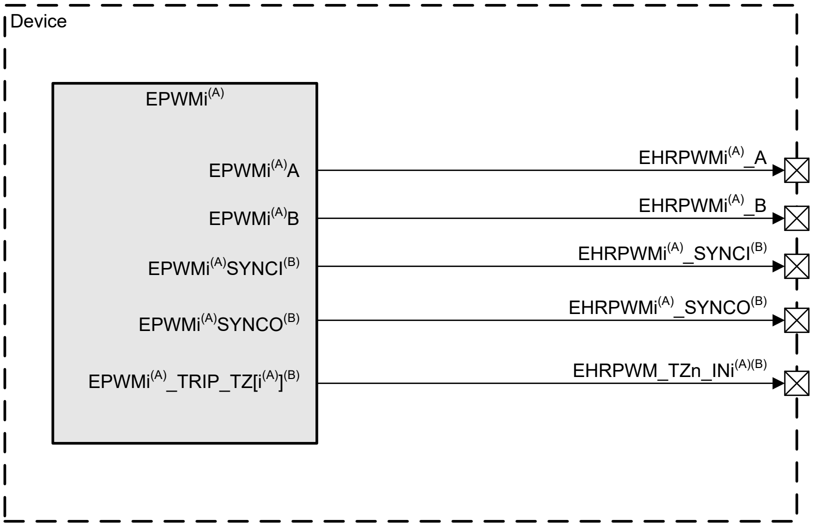

Figure 12-321. EPWM I/O Interface Signals

Note

i represents a valid instance of EPWM in a domain. See the device datasheet for specifics.

Note

Pin only available on specific instances. See the device datasheet for specifics.

Table 12-280 describes the EPWM I/O signals.

Table 12-292. EPWM I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
		EPWMi(3)		
EPWMi(3)A	EHRPWMi(3)_A	O	EPWMi(3) output A	0x0
EPWMi(3)B	EHRPWMi(3)_B	O	EPWMi(3) output B	0x0
EPWMi(3)SYNCI(4)	EHRPWMi(3)_SYNCI	I	EPWMi(3) Sync input	HiZ
EPWMi(3)SYNCO(4)	EHRPWMi(3)_SYNCO	O	EPWMi(3) Sync output	0x0
EPWMi(3)_TRIP_TZ[0](4)	EHRPWM_TZn_INi(3)	I	EPWMi(3) TripZone input	HiZ
		EPWM Start of Conversion		
PWM_SOCA	EHRPWM_SOCA	O	EPWM start of conversion output A	HiZ
PWM_SOCB	EHRPWM_SOCB	O	EPWM start of conversion output B	HiZ

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) i represents a valid instance of EPWM in a domain. See the device datasheet for specifics.
(4) Pin only available on specific instances. See the device datasheet for specifics.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.5.3.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.3.4 EPWM Functional Description

Seven submodules are included in each EPWM peripheral. Each of these submodules performs specific tasks that can be configured by software.

12.5.3.4.1 EPWM Submodule Features

Table 12-281 lists the seven key submodules together with a list of their main configuration parameters.

Table 12-293. Submodule Configuration Parameters

Submodule	Configuration Parameter or Option
Time-base (TB)	• Scale the time-base clock (TBCLK) relative to the system clock (FICLK). • Configure the PWM time-base counter (TBCNT) frequency or period. • Time-base counter mode selection: – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another EPWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Configure how the time-base counter will behave when the device is halted by an emulator. • Specify the source for the synchronization output of the EPWM module: – Synchronization input signal – Time-base counter equal to zero – Time-base counter equal to counter-compare B (CMPB) – No output synchronization signal generated
Counter-compare (CC)	• Specify the PWM duty cycle for output EPWMxA and/or output EPWMxB • Specify the time at which switching events occur on the EPWMxA or EPWMxB output
Action-qualifier (AQ)	• Specify the type of action taken when a time-base or counter-compare submodule event occurs: – No action taken – Output EPWMxA and/or EPWMxB switched high – Output EPWMxA and/or EPWMxB switched low – Output EPWMxA and/or EPWMxB toggled • Force the PWM output state through software control • Configure and control the PWM dead-band through software
Dead-band (DB)	• Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value • Bypass the dead-band module entirely. In this case the PWM waveform is passed through without modification
PWM-chopper (PC)	• Create a chopping (carrier) frequency • Pulse width of the first pulse in the chopped pulse train • Duty cycle of the second and subsequent pulses • Bypass the PWM-chopper module entirely. In this case the PWM waveform is passed through without modification.

Table 12-293. Submodule Configuration Parameters (continued)

Submodule	Configuration Parameter or Option
Trip-zone (TZ)	• Configure the EPWM module to react to one, all, or none of the trip-zone pins • Specify the tripping action taken when a fault occurs: – Force EPWMxA and/or EPWMxB high – Force EPWMxA and/or EPWMxB low – Force EPWMxA and/or EPWMxB to a high-impedance state – Configure EPWMxA and/or EPWMxB to ignore any trip condition • Configure how often the EPWM will react to the trip-zone pin: – One-shot – Cycle-by-cycle • Enable the trip-zone to initiate an interrupt • Bypass the trip-zone module entirely
Event-trigger (ET)	• Enable the EPWM events that will trigger an interrupt. • Specify the rate at which events cause triggers (every occurrence or every second or third occurrence) • Poll, set, or clear event flags

Some examples on various EPWM module configurations are shown below. These examples use the constant definitions shown in Section 12.5.3.4.1.1 .

Constant Definitions Used in the EPWM Code Examples

```
// TBCTL (Time-Base Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// TBCNT MODE bits
#define         TB_COUNT_UP        0x0
#define         TB_COUNT_DOWN      0x1
#define         TB_COUNT_UPDOWN    0x2
#define         TB_FREEZE          0x3
// PHSEN bit
#define         TB_DISABLE         0x0
#define         TB_ENABLE          0x1
// PRDLD bit
#define         TB_SHADOW          0x0
#define         TB_IMMEDIATE       0x1
// SYNCOSEL bits
#define         TB_SYNC_IN         0x0
#define         TB_CTR_ZERO        0x1
#define         TB_CTR_CMPB        0x2
#define         TB_SYNC_DISABLE    0x3
// HSPCLKDIV and CLKDIV bits
#define         TB_DIV1            0x0
#define         TB_DIV2            0x1
#define         TB_DIV4            0x2
// PHSDIR bit
#define         TB_DOWN            0x0
#define         TB_UP              0x1
```

```
// CMPCTL (Compare Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// LOADAMODE and LOADBMODE bits
#define         CC_CTR_ZERO        0x0
#define         CC_CTR_PRD         0x1
#define         CC_CTR_ZERO_PRD    0x2
#define         CC_LD_DISABLE      0x3
// SHDWAMODE and SHDWBMODE bits
#define         CC_SHADOW          0x0
#define         CC_IMMEDIATE       0x1
// AQCTLA and AQCTLB (Action-qualifier Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// ZRO, PRD, CAU, CAD, CBU, CBD bits
#define         AQ_NO_ACTION       0x0
#define         AQ_CLEAR           0x1
#define         AQ_SET             0x2
```

```
#define         AQ_TOGGLE         0x3
// DBCTL (Dead-Band Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// MODE bits
#define         DB_DISABLE        0x0
#define         DBA_ENABLE        0x1
#define         DBB_ENABLE        0x2
#define DB_FULL_ENABLE 0x3
// POLSEL bits
#define         DB_ACTV_HI        0x0
#define         DB_ACTV_LOC       0x1
#define         DB_ACTV_HIC       0x2
#define         DB_ACTV_LO        0x3
// PCCTL (chopper control)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// CHPEN bit
#define         CHP_ENABLE        0x0
#define CHP_DISABLE 0x1
// CHPFREQ bits
#define         CHP_DIV1          0x0
#define         CHP_DIV2          0x1
#define         CHP_DIV3          0x2
#define         CHP_DIV4          0x3
#define         CHP_DIV5          0x4
#define         CHP_DIV6          0x5
#define         CHP_DIV7          0x6
#define         CHP_DIV8          0x7
// CHPDUTY bits
#define         CHP1_8TH          0x0
#define         CHP2_8TH          0x1
#define         CHP3_8TH          0x2
#define         CHP4_8TH          0x3
#define         CHP5_8TH          0x4
#define         CHP6_8TH          0x5
#define         CHP7_8TH          0x6
// TZSEL (Trip-zone Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// CBCn and OSHTn bits
#define         TZ_ENABLE         0x0
#define         TZ_DISABLE        0x1
// TZCTL (Trip-zone Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// TZA and TZB bits
#define         TZ_HIZ            0x0
#define         TZ_FORCE_HI       0x1
#define         TZ_FORCE_LO       0x2
#define         TZ_DISABLE        0x3
// ETSEL (Event-trigger Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTSEL, SOCASEL, SOCBSEL bits
#define         ET_CTR_ZERO       0x1
#define         ET_CTR_PRD        0x2
#define         ET_CTRU_CMPA      0x4
#define         ET_CTRD_CMPA      0x5
#define         ET_CTRU_CMPB      0x6
#define         ET_CTRD_CMPB      0x7
// ETPS (Event-trigger Prescale)
// = = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTPRD, SOCAPRD, SOCBPRD bits
#define         ET_DISABLE        0x0
#define         ET_1ST            0x1
#define         ET_2ND            0x2
#define         ET_3RD            0x3
```

12.5.3.4.2 EPWM Time-Base (TB) Submodule

This section describes the Time-Base (TB) submodule in the PWM module.

12.5.3.4.2.1 Overview

Each EPWM module has its own time-base submodule that determines all of the timing events. Built-in synchronization logic allows the time-base of multiple EPWM modules (EPWMx) to work together as a single system. Figure 12-322 illustrates the time-base module's place within the EPWM.

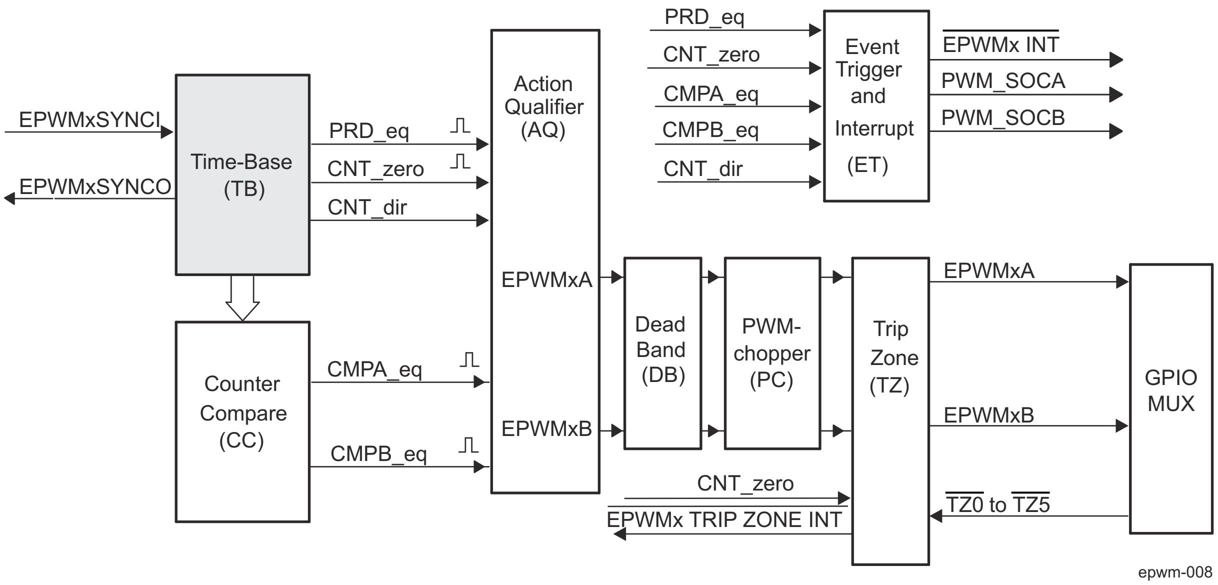

Figure 12-322. EPWM Time-Base Submodule

12.5.3.4.2.2 Controlling and Monitoring the EPWM Time-Base Submodule

Table 12-282 lists the registers used to control and monitor the time-base submodule.

Table 12-294. EPWM Time-Base Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TBCTL	Time-Base Control Register	0h	No
EPWM_TBSTS	Time-Base Status Register	2h	No
EPWM_TBPHS	Time-Base Phase Register	6h	No
EPWM_TBCNT	Time-Base Counter Register	8h	No
EPWM_TBPRD	Time-Base Period Register	Ah	Yes

Figure 12-323 shows the critical signals and registers of the time-base submodule. Table 12-283 provides descriptions of the key signals associated with the time-base submodule.

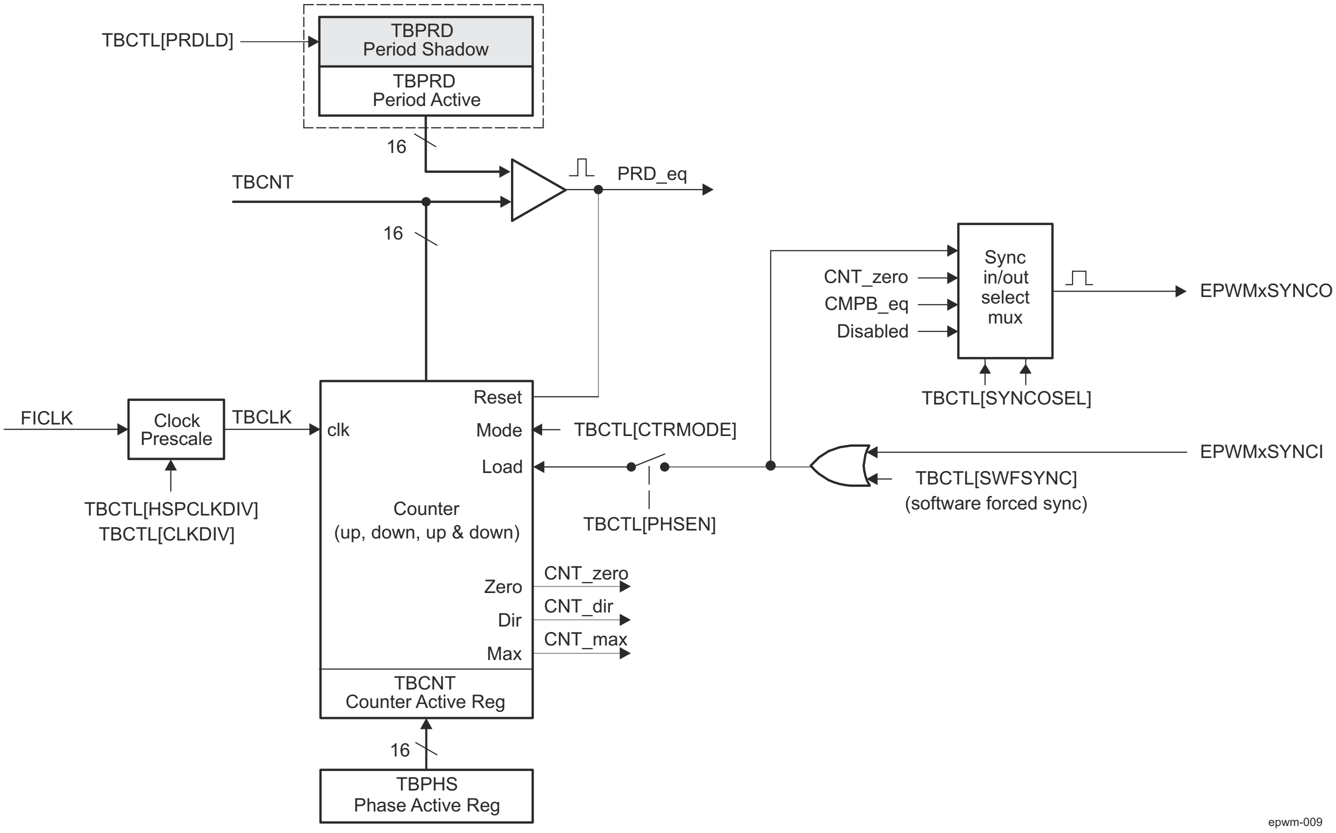

Figure 12-323. EPWM Time-Base Submodule Signals and Registers

Table 12-295. EPWM Time-Base Submodule Key Signals

Signal	Description
EPWMxSYNCI	Time-base synchronization input. Input pulse used to synchronize the time-base counter with the counter of another EPWM module earlier in the synchronization chain. An EPWM peripheral can be configured to use or ignore this signal. For the first EPWM module (EPWM0) this signal comes from a device pin. For subsequent EPWM modules this signal is passed from another EPWM peripheral. For example, EPWM2SYNCI is generated by the EPWM1 peripheral and the EPWM3SYNCI is generated (optional through internal multiplexer) by EPWM2 or from a device pin. See Section 12.5.3.4.2.3.2 for information on the synchronization order of a particular device.
EPWMxSYNCO	Time-base synchronization output. This output pulse is used to synchronize the counter of an EPWM module later in the synchronization chain. The EPWM module generates this signal from one of three event sources: 1. EPWMxSYNCI (Synchronization input pulse) 2. TBCNT = 0: The time-base counter (EPWM_TBCNT register) equal to zero (TBCNT = 0000h). 3. TBCNT = CMPB: The time-base counter (EPWM_TBCNT register) equal to the counter-compare B register — EPWM_CMPB (that is bitfield TBCNT = bitfield CMPB).
PRD_eq	Time-base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCNT = TBPRD.
CNT_zero	Time-base counter equal to zero. This signal is generated whenever the counter value is zero. That is when TBCNT equals 0000h.
CMPB_eq	Time-base counter equal to active counter-compare B register (TBCNT = CMPB). This event is generated by the counter-compare submodule and used by the synchronization out logic.
CNT_dir	Time-base counter direction.

Table 12-295. EPWM Time-Base Submodule Key Signals (continued)

Signal	Description
	Indicates the current direction of the EPWM's time-base counter. This signal is high when the counter is increasing and low when it is decreasing.
CNT_max	Time-base counter equal max value (TBCNT = FFFFh). Generated event when the EPWM_TBCNT register value reaches its maximum value. This signal is only used only as a status bit.
TBCLK	Time-base clock. This is a prescaled version of the system clock — FICLK and is used by all submodules within the EPWMn. This clock determines the rate at which time-base counter increments or decrements.

12.5.3.4.2.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period register (EPWM_TBPRD) and the mode of the time-base counter. Figure 12-324 shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (EPWM_TBPRD[15-0] TBPRD = 0x4). The time increment for each step is defined by the time-base clock (TBCLK) which is a prescaled version of the system clock (FICLK).

The time-base counter has three modes of operation selected by the time-base control register (EPWM_TBCTL):

- **Up-Down-Count Mode:** In up-down-count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until it reaches zero. At this point the counter repeats the pattern and begins to increment.
- **Up-Count Mode:** In this mode, the time-base counter starts from zero and increments until it reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.
- **Down-Count Mode:** In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until it reaches zero. When it reaches zero, the time-base counter is reset back to the period value and it repeats this pattern.

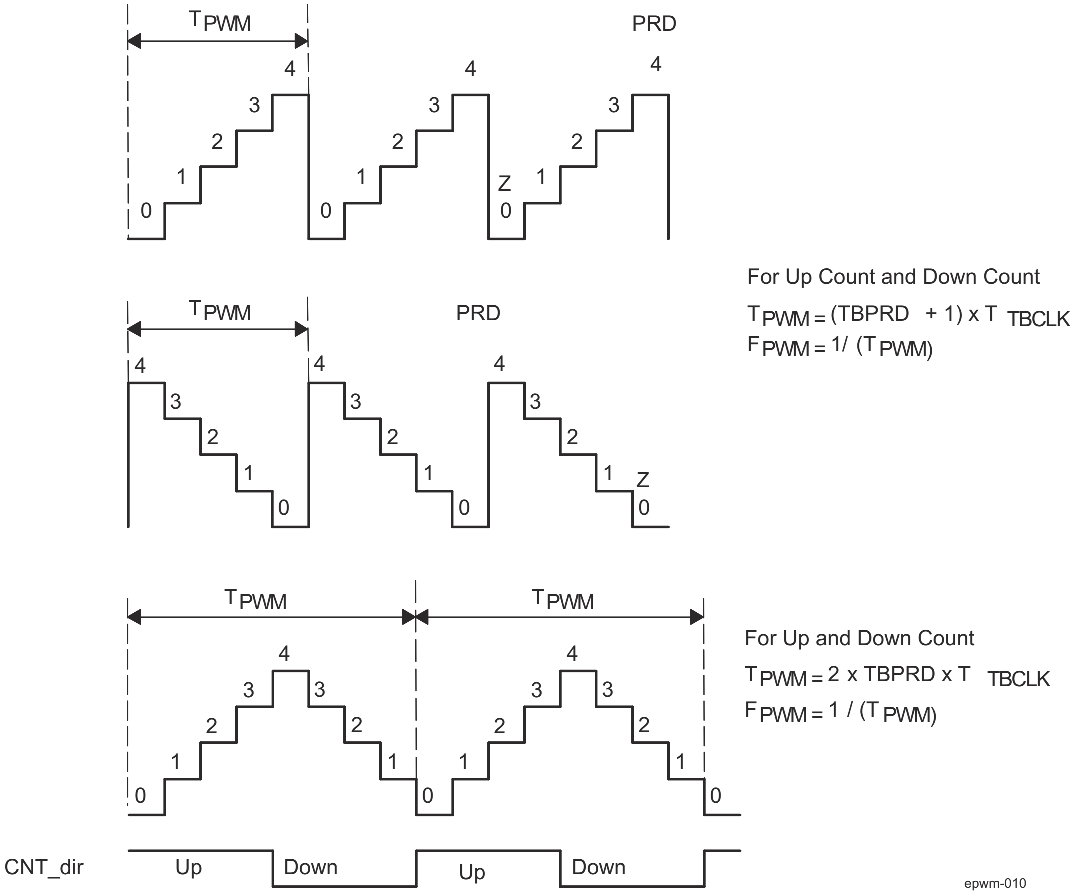

Figure 12-324. EPWM Time-Base Frequency and Period

12.5.3.4.2.3.1 EPWM Time-Base Period Shadow Register

The time-base period register (EPWM_TBPRD) has a shadow register. Shadowing allows the register update to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the EPWM module:

- **Active Register:** The active register controls the hardware and is responsible for actions that the hardware causes or invokes.
- **Shadow Register:** The shadow register buffers or provides a temporary holding location for the active register. It has no direct effect on any control hardware. At a strategic point in time the shadow register's content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

The memory address of the shadow period register is the same as the active register. Which register is written to or read from is determined by the EPWM_TBCTL[3] PRDLD bit. This bit enables and disables the EPWM_TBPRD shadow register as follows:

- **Time-Base Period Shadow Mode:** The EPWM_TBPRD shadow register is enabled when EPWM_TBCTL[3] PRDLD = 0h. Reads from and writes to the EPWM_TBPRD register memory address go to the shadow register. The shadow register contents are transferred to the active register (EPWM_TBPRD (Active) ← EPWM_TBPRD (shadow)) when the time-base counter register (EPWM_TBCNT) equals zero (TBCNT = 0000h). By default the EPWM_TBPRD shadow register is enabled.
- **Time-Base Period Immediate Load Mode:** If immediate load mode is selected (EPWM_TBCTL[3] PRDLD = 1h), then a read from or a write to the TBPRD memory address goes directly to the active register.

12.5.3.4.2.3.2 EPWM Time-Base Counter Synchronization

A time-base synchronization scheme connects all of the EPWM modules on a device. Each EPWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (EPWM0) comes from an external pin. For the device EPWM environment sync pin details refer to the Section 12.5.3.2 . The possible synchronization connections for the remaining EPWM modules is shown in Figure 12-325.

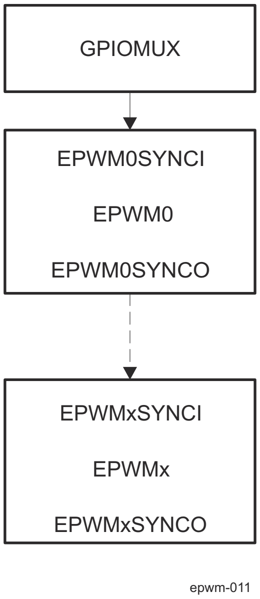

Figure 12-325. EPWM Time-Base Counter Synchronization Scheme 1

Each EPWM module can be configured to use or ignore the synchronization input. If the EPWM_TBCTL[2] PHSEN bit is set, then the time-base counter (TBCNT) of the EPWM module (EPWM_TBCNT register) will be automatically loaded with the phase register (EPWM_TBPHS) contents when one of the following conditions occur:

- **EPWMxSYNCI: Synchronization Input Pulse:** The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (EPWM_TBPHS → EPWM_TBCNT). This operation occurs on the next valid time-base clock (TBCLK) edge.
- **Software Forced Synchronization Pulse:** Writing a 1h to the EPWM_TBCTL[6] SWFSYNC control bit invokes a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on EPWMxSYNCI.

This feature enables the EPWM module to be automatically synchronized to the time base of another EPWM module. Lead or lag phase control can be added to the waveforms generated by different EPWM modules to synchronize them. In up-down-count mode, the EPWM_TBCTL[13] PHSDIR bit configures the direction of the time-base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The TBPHS bit is ignored in count-up or count-down modes. See Figure 12-326 through Figure 12-329 for examples.

Clearing the EPWM_TBCTL[2] PHSEN bit configures the EPWM to ignore the synchronization input pulse. The synchronization pulse can still be allowed to flow-through to the EPWMxSYNCO and be used to synchronize other EPWM modules. In this way, a controller time-base (for example: EPWM1) and downstream modules (EPWM2–EPWMx) can be set and they may select to run in synchronization with the controller.

12.5.3.4.2.4 Phase Locking the Time-Base Clocks of Multiple EPWM Modules

As already described in the *EPWM Modules Time-Base Clock Gating*, TB_CLKEN bit in the EPWMn_CTRL (where n = 0 to number of instances on the device) register of the device CTRL_MMR can be used to individually control or globally synchronize the time-base clocks of all enabled EPWM modules on a device.

When all TB_CLKEN bits are set to 0h, the time-base clocks of all EPWMx (where x = 0 to 8) modules are stopped (default). When all TB_CLKEN bits are simultaneously set in software to 1h, all EPWMx modules time-base clocks are started with the rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescaler bits in the EPWM_TBCTL register of each EPWM module must be set identically. The proper procedure for enabling the EPWM clocks is as follows:

1. Enable the EPWM module clocks.
2. Set TB_CLKEN = 0. This will stop the time-base clock within any enabled EPWMx module.
3. Configure the prescaler values and desired EPWM modes per each involved EPWMx.
4. Simultaneously set TB_CLKEN bits to 1h.

12.5.3.4.2.5 EPWM Time-Base Counter Modes and Timing Waveforms

The time-base counter operates in one of four modes:

- Up-count mode which is asymmetrical.
- Down-count mode which is asymmetrical.
- Up-down-count which is symmetrical.
- Frozen where the time-base counter is held constant at the current value.

To illustrate the operation of the first three modes, Figure 12-326 to Figure 12-329 show when events are generated and how the time-base responds to an EPWMxSYNCI signal.

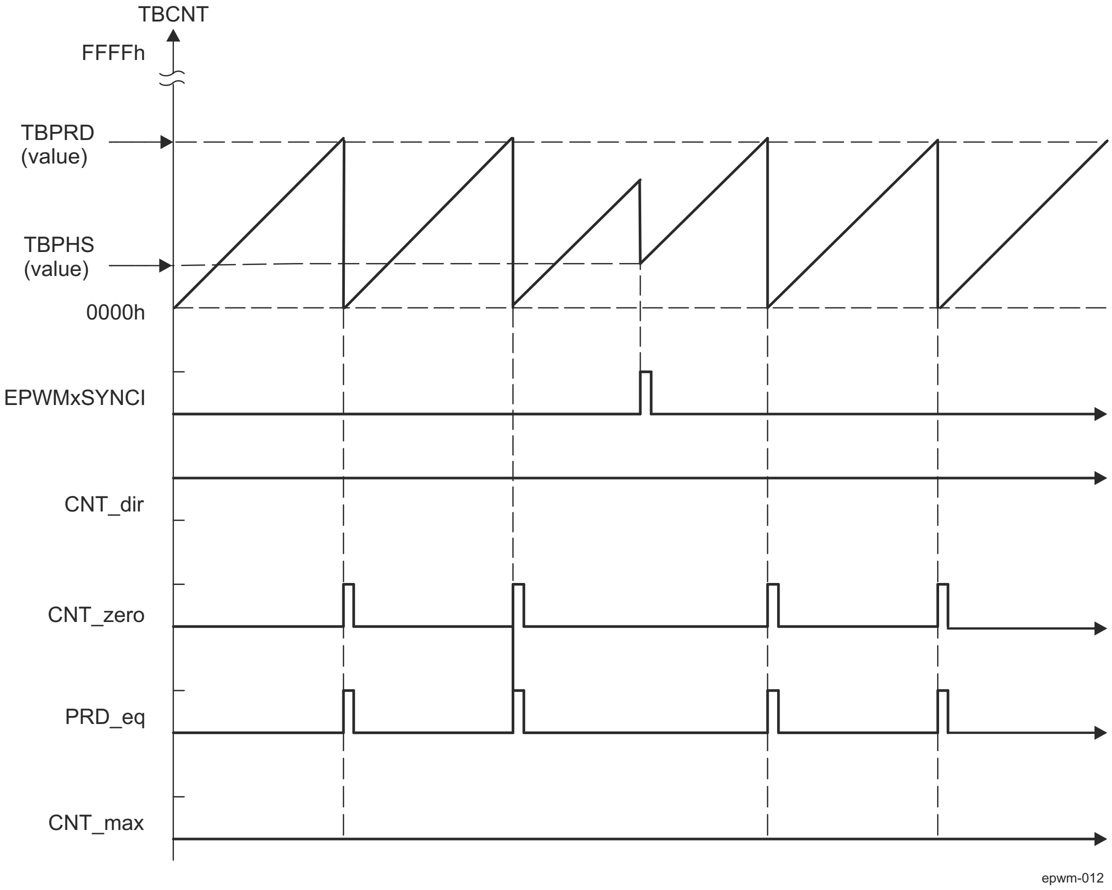

Figure 12-326. EPWM Time-Base Up-Count Mode Waveforms

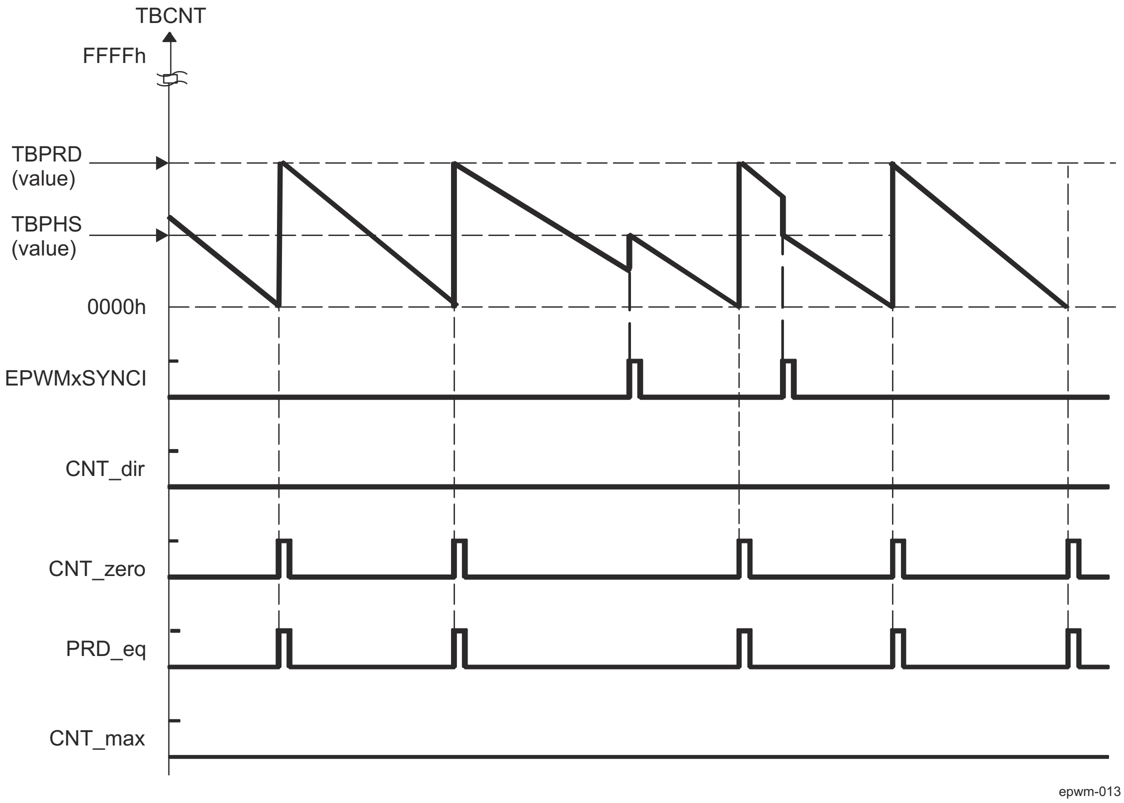

Figure 12-327. EPWM Time-Base Down-Count Mode Waveforms

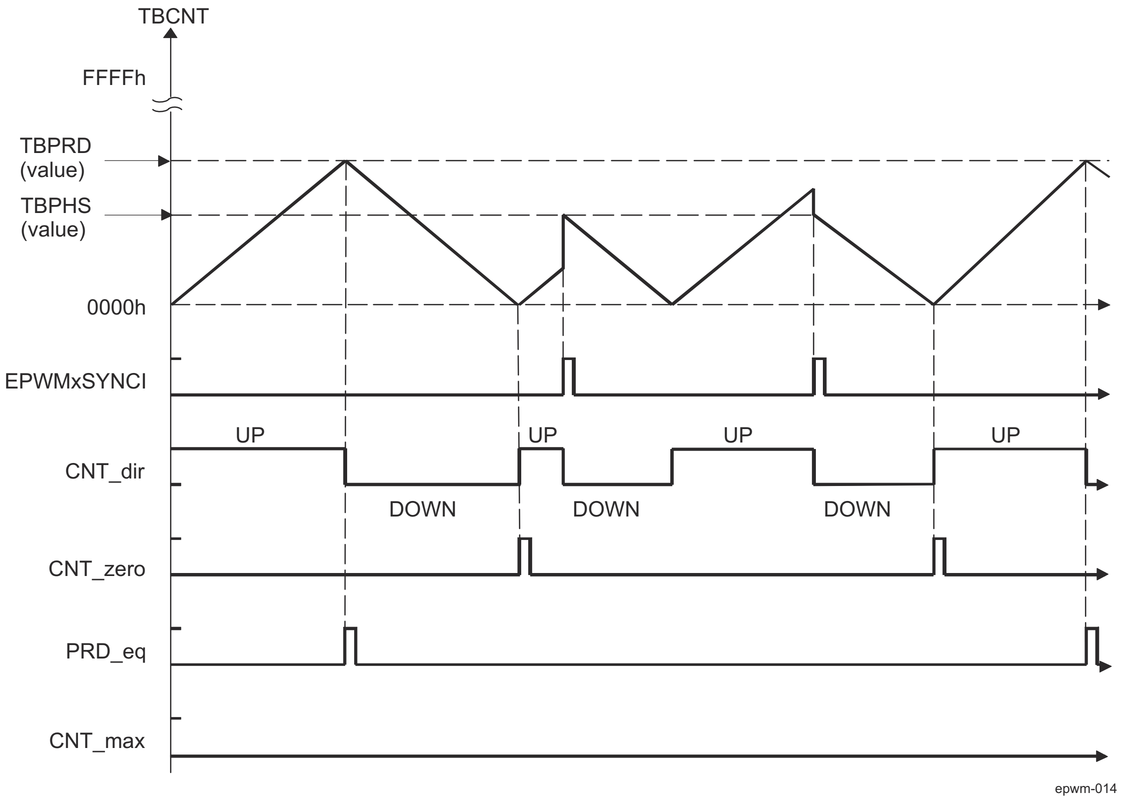

Figure 12-328. EPWM Time-Base Up-Down-Count Waveforms, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

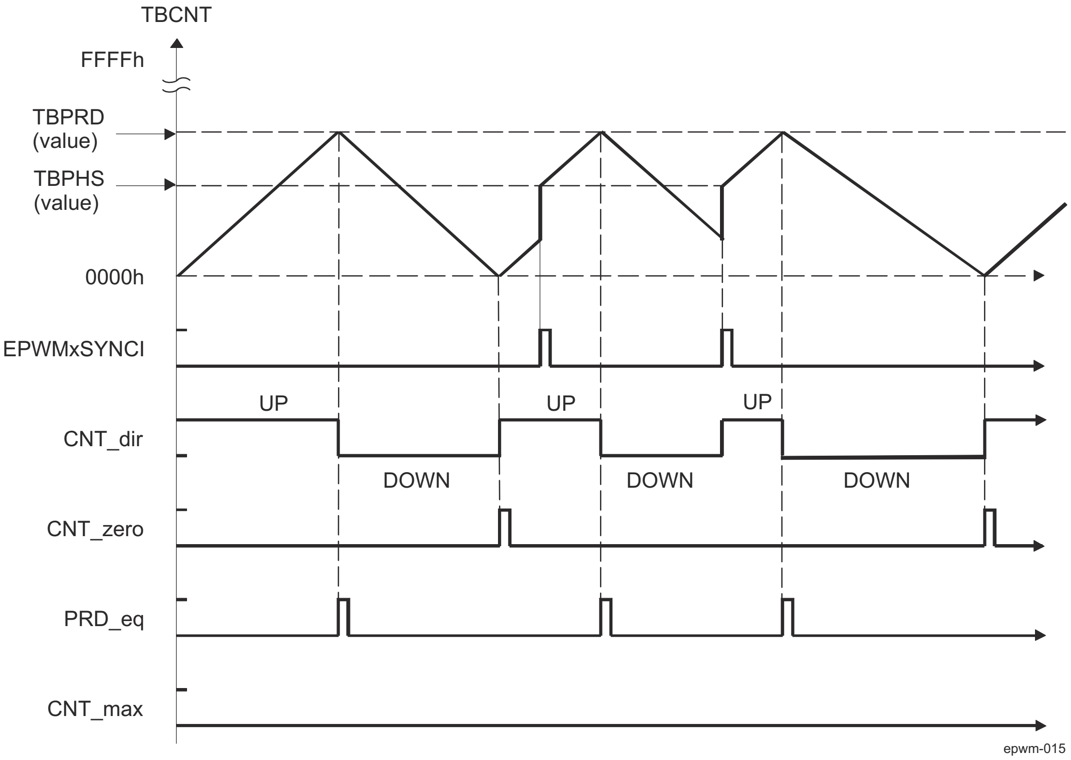

Figure 12-329. EPWM Time-Base Up-Down Count Waveforms, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.5.3.4.3 EPWM Counter-Compare (CC) Submodule

This section describes the Counter-Compare (CC) submodule in the PWM module.

12.5.3.4.3.1 Overview

Figure 12-330 illustrates the counter-compare submodule within the EPWM. Figure 12-331 shows the basic structure of the counter-compare submodule.

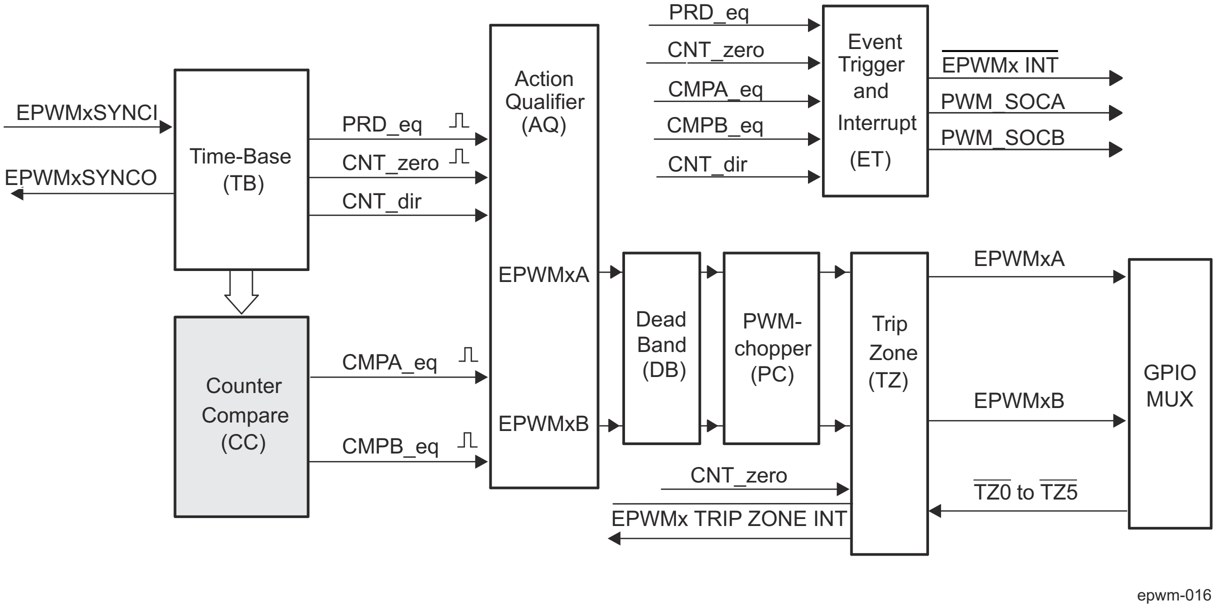

Figure 12-330. EPWM Counter-Compare Submodule

CC module features:

- Generates events based on programmable time stamps using the EPWM_CMPA and EPWM_CMPB registers
  - CMPA_eq (Time-base counter equals counter-compare A register (TBCNT = CMPA)).
  - CMPB_eq (Time-base counter equals counter-compare B register (TBCNT = CMPB)).
- Controls the PWM duty cycle if the action-qualifier submodule is configured appropriately
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle.

The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (EPWM_CMPA) and counter-compare B (EPWM_CMPB) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event.

12.5.3.4.3.2 Controlling and Monitoring the EPWM Counter-Compare Submodule

Table 12-284 lists the registers used to control and monitor the counter-compare submodule. Table 12-285 lists the key signals associated with the counter-compare submodule.

Table 12-296. EPWM Counter-Compare Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_CMPCTL	Counter-Compare Control Register.	Eh	No
EPWM_CMPA	Counter-Compare A Register	12h	Yes
EPWM_CMPB	Counter-Compare B Register	14h	Yes

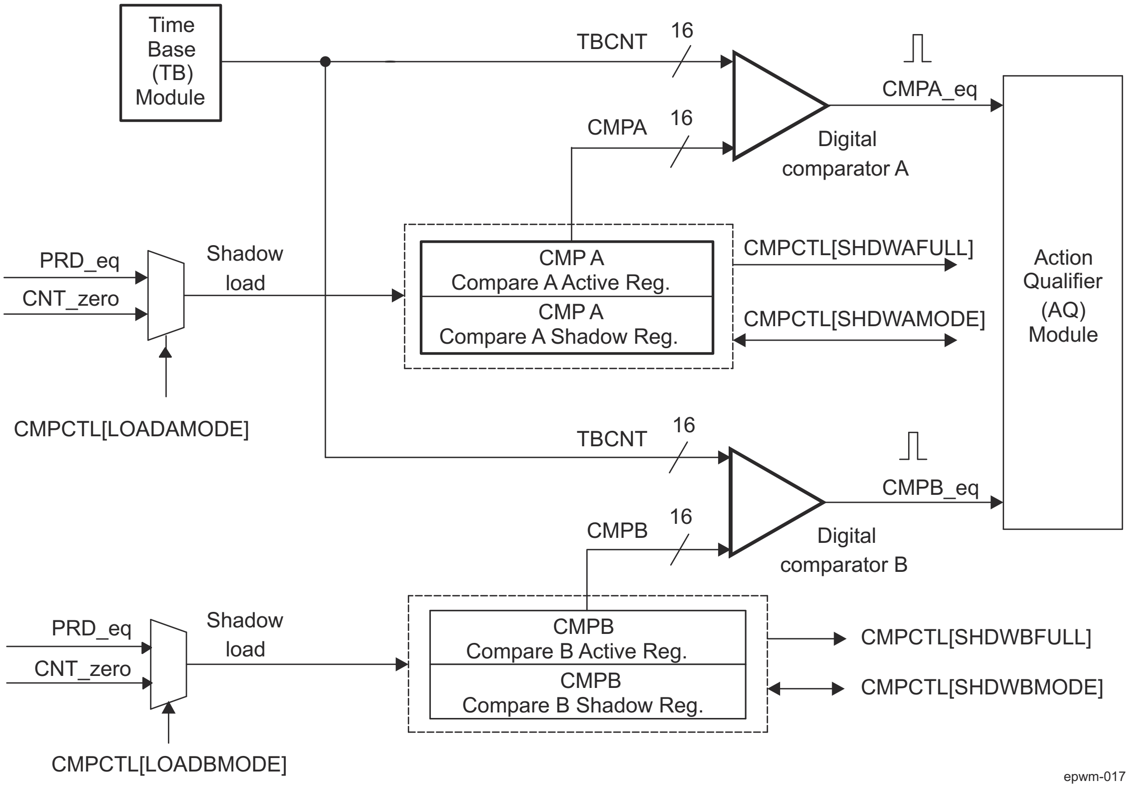

Figure 12-331. EPWM Counter-Compare Submodule Signals and Registers

Table 12-297. EPWM Counter-Compare Submodule Key Signals

Signal	Description of Event	Register Bitfields Compared
CMPA_eq	Time-base counter equal to the active counter-compare A value	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the active counter-compare B value	TBCNT = CMPB
PRD_eq	Time-base counter equal to the active period. Used to load active counter-compare A and B registers from the shadow register	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero. Used to load active counter-compare A and B registers from the shadow register	TBCNT = 0000h

12.5.3.4.3.3 Operational Highlights for the EPWM Counter-Compare Submodule

The counter-compare submodule is responsible for generating two independent compare events based on two compare registers:

1. CMPA: Time-base counter equal to counter-compare A register (EPWM_TBCNT = EPWM_CMPA).
2. CMPB: Time-base counter equal to counter-compare B register (EPWM_TBCNT = EPWM_CMPB).

For up-count or down-count mode, each event occurs only once per cycle. For up-down-count mode each event occurs twice per cycle, if the compare value is between 0000h and TBPRD; and occurs once per cycle, if the compare value is equal to 0000h or equal to TBPRD. These events are fed into the action-qualifier submodule where they are qualified by the counter direction and converted into actions if enabled. Refer to Section 12.5.3.4.4 for more details.

The counter-compare EPWM_CMPA and EPWM_CMPB registers each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occurs at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. The memory address of the active register and the shadow register is identical. Which register is written to or read from is determined by the EPWM_CMPCTL[4] SHDWAMODE and EPWM_CMPCTL[6] SHDWBMODE bits. These bits enable and disable the EPWM_CMPA shadow register and EPWM_CMPB shadow register respectively. The behavior of the two load modes is described below:

- **Shadow Load Mode:**
  The shadow mode for the EPWM_CMPA register is enabled by clearing the EPWM_CMPCTL[4] SHDWAMODE bit and the shadow register for EPWM_CMPB register is enabled by clearing the EPWM_CMPCTL[6] SHDWBMODE bit. Shadow mode is enabled by default for both EPWM_CMPA and EPWM_CMPB register.

  If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD).
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - Both PRD_eq and CNT_zero events occurrence

  Which of these three events will drive the counter compare module is specified by the EPWM_CMPCTL[1-0] LOADAMODE and EPWM_CMPCTL[3-2] LOADBMODE register bit fields. Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.
- **Immediate Load Mode:**
  If immediate load mode is selected (EPWM_CMPCTL[4] SHDWAMODE = 1h or EPWM_CMPCTL[6] SHDWBMODE = 1h), then a read from or a write to the register will go directly to the active register.

Figure 12-332 and Figure 12-333 show Compare A and B Dual Shadow registers.

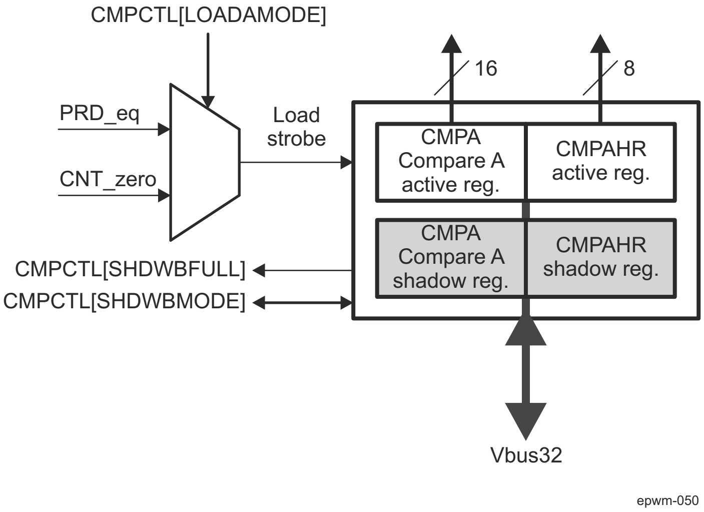

Figure 12-332. Compare A Dual Shadow register

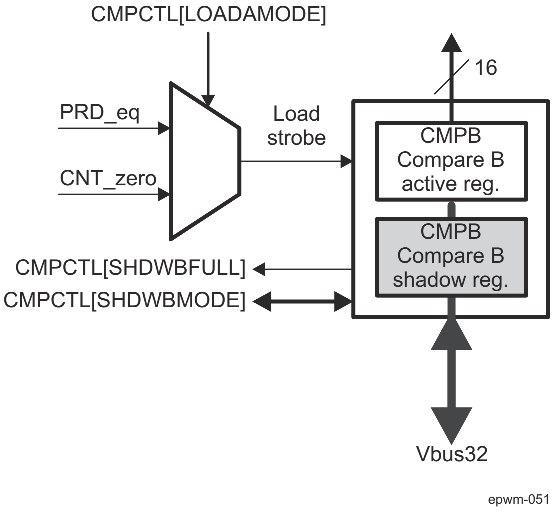

Figure 12-333. Compare B Dual Shadow register

12.5.3.4.3.4 EPWM Counter-Compare Submodule Timing Waveforms

As described in Section 12.5.3.4.2 , the Time Base (TB) module can be configured to operate in 3 distinct count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Down-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

The timing diagrams in Figure 12-334 to Figure 12-337 show how CMPA and CMPB events are generated in each of the 3 count modes and how the EPWMxSYNCI signal interacts.

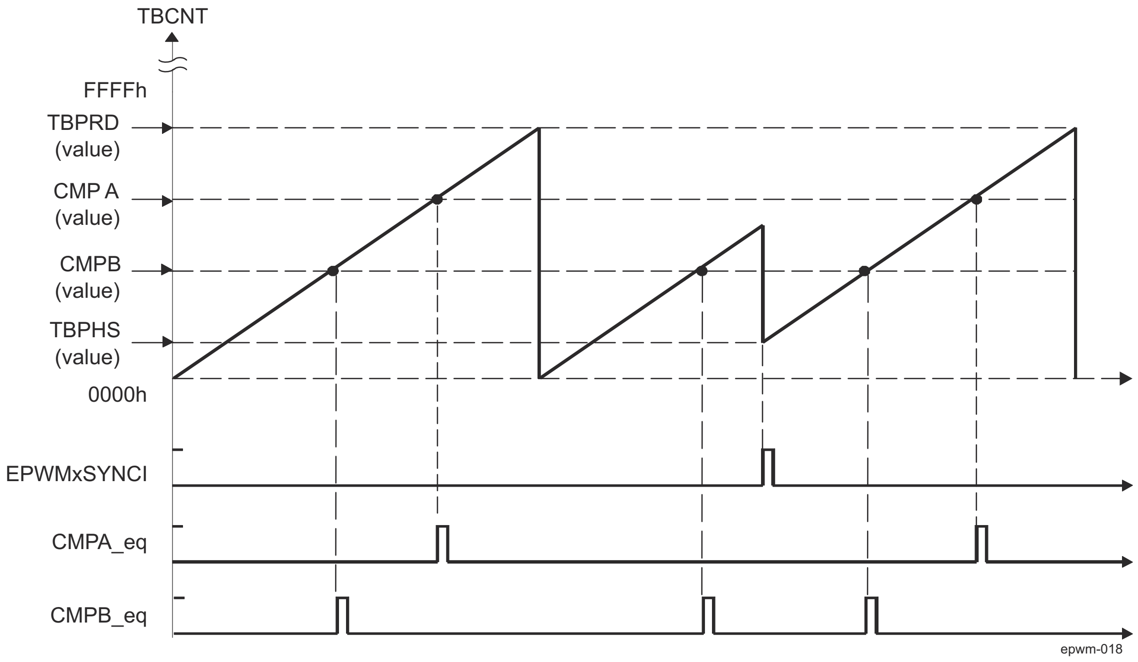

Note

An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCNT count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

Figure 12-334. EPWM Counter-Compare Event Waveforms in Up-Count Mode

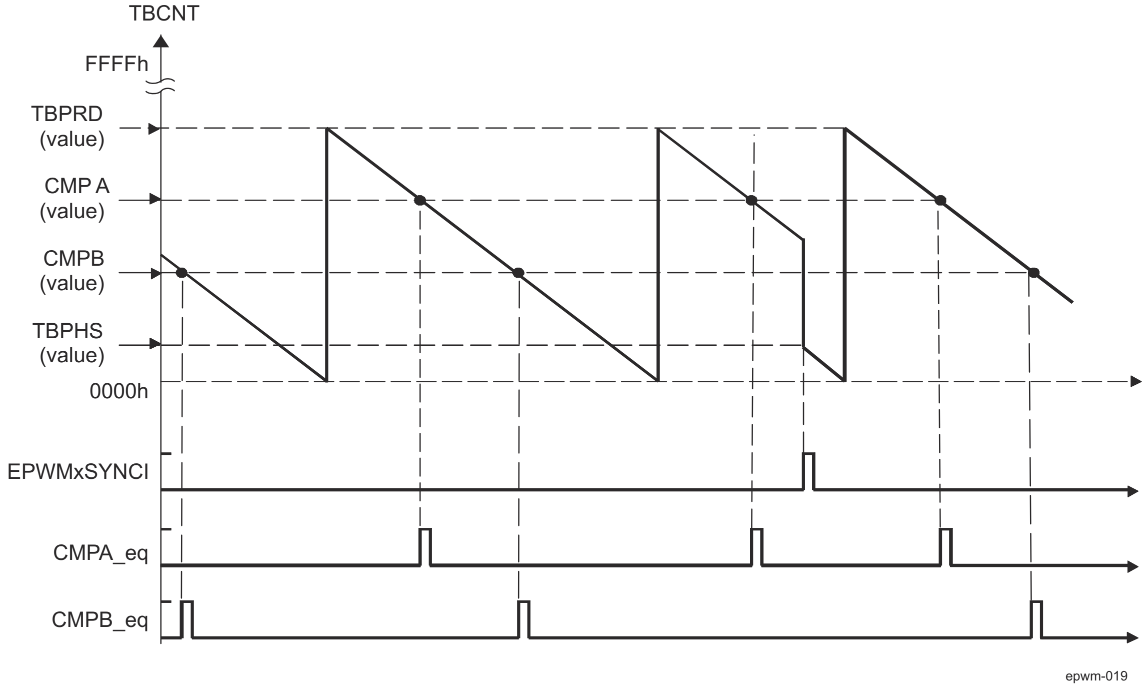

Figure 12-335. EPWM Counter-Compare Events in Down-Count Mode

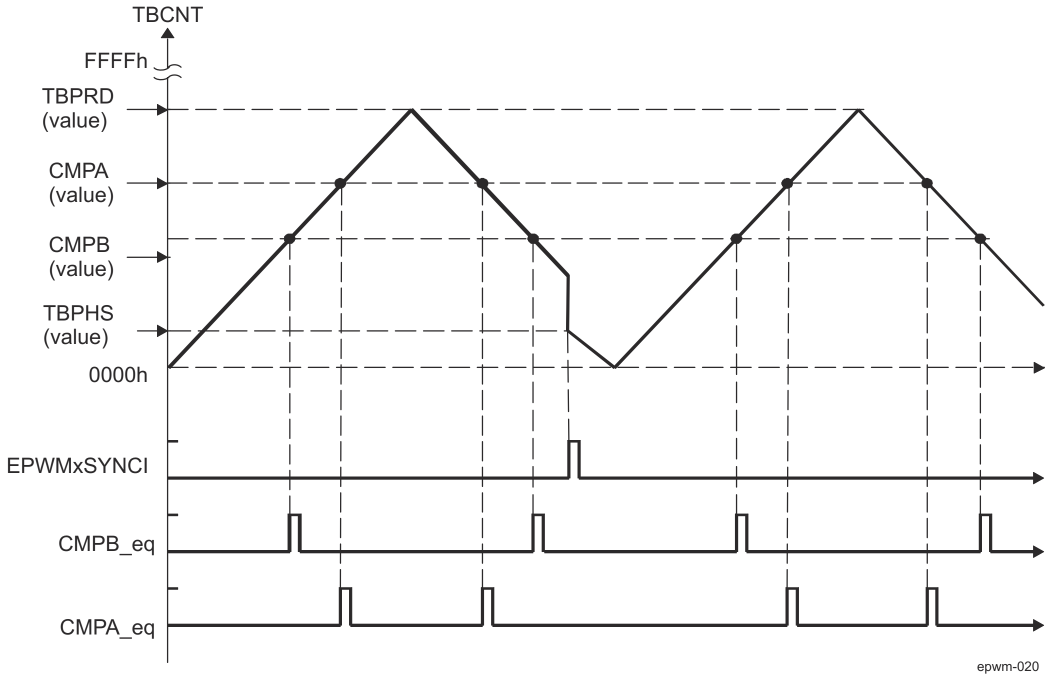

Figure 12-336. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

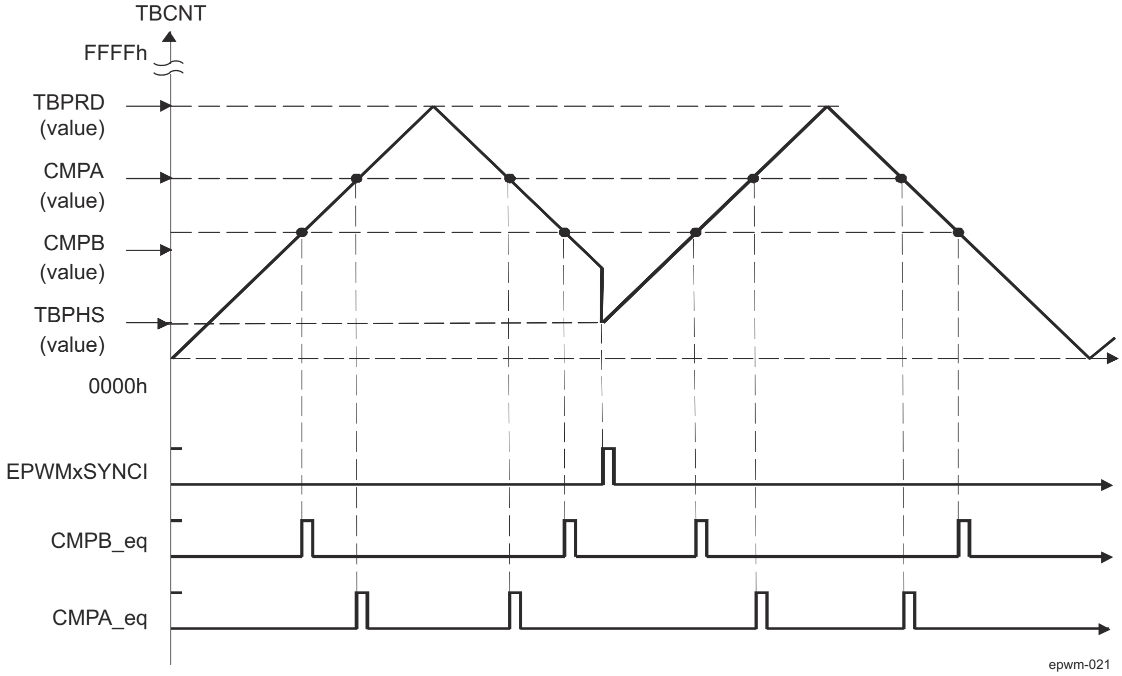

Figure 12-337. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.5.3.4.4 EPWM Action-Qualifier (AQ) Submodule

This section describes the Action-Qualifier (AQ) submodule in the PWM module.

12.5.3.4.4.1 Overview

Figure 12-338 shows the action-qualifier (AQ) submodule in the EPWM system. This submodule has the most important role in waveform construction and PWM generation. It decides which events are converted into various action types, thereby producing the required switched waveforms at the EPWMxA and EPWMxB outputs.

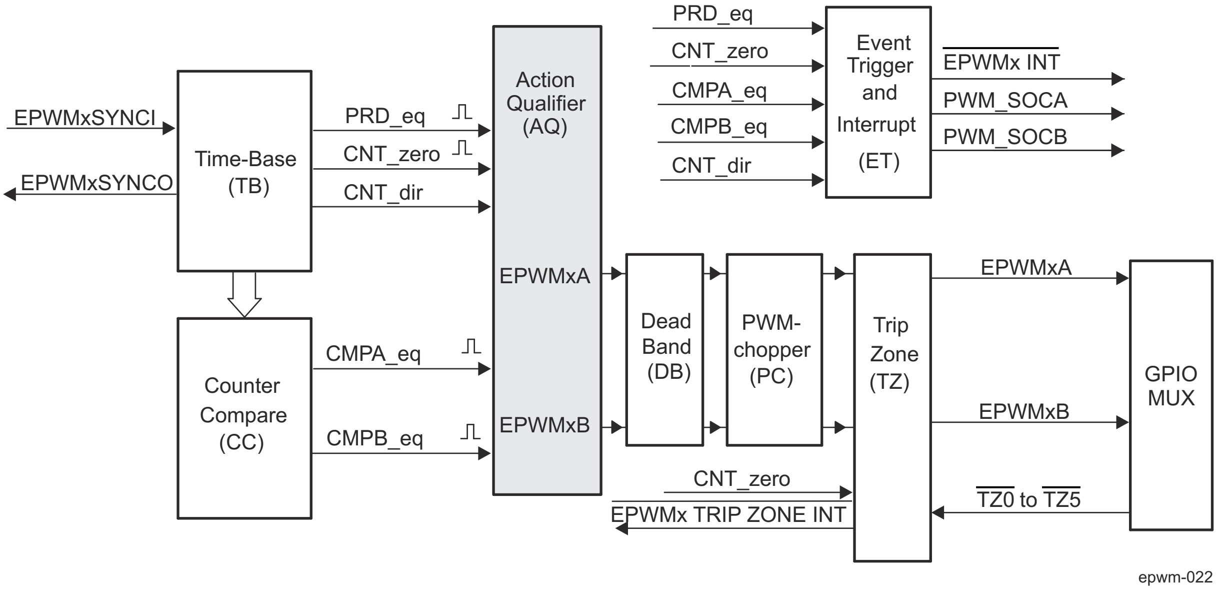

Figure 12-338. EPWM Action-Qualifier Submodule

AQ module features:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD)
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - CMPA_eq: Time-base counter equal to the counter-compare A register (TBCNT = CMPA)
  - CMPB_eq: Time-base counter equal to the counter-compare B register (TBCNT = CMPB)
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when it is decreasing

12.5.3.4.4.2 Controlling and Monitoring the EPWM Action-Qualifier Submodule

Table 12-286 lists the registers used to control and monitor the action-qualifier submodule.

Table 12-298. EPWM Action-Qualifier Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_AQCTLA	Action-Qualifier Control Register For Output A (EPWMxA)	16h	No
EPWM_AQCTLB	Action-Qualifier Control Register For Output B (EPWMxB)	18h	No
EPWM_AQSFRC	Action-Qualifier Software Force Register	1Ah	No
EPWM_AQCSFRC	Action-Qualifier Continuous Software Force	1Ch	Yes

The action-qualifier submodule is based on event-driven logic. It can be thought of as a programmable cross switch with events at the input and actions at the output, all of which are software controlled via the set of registers as shown in Figure 12-339. The possible input events are summarized again in Table 12-287.

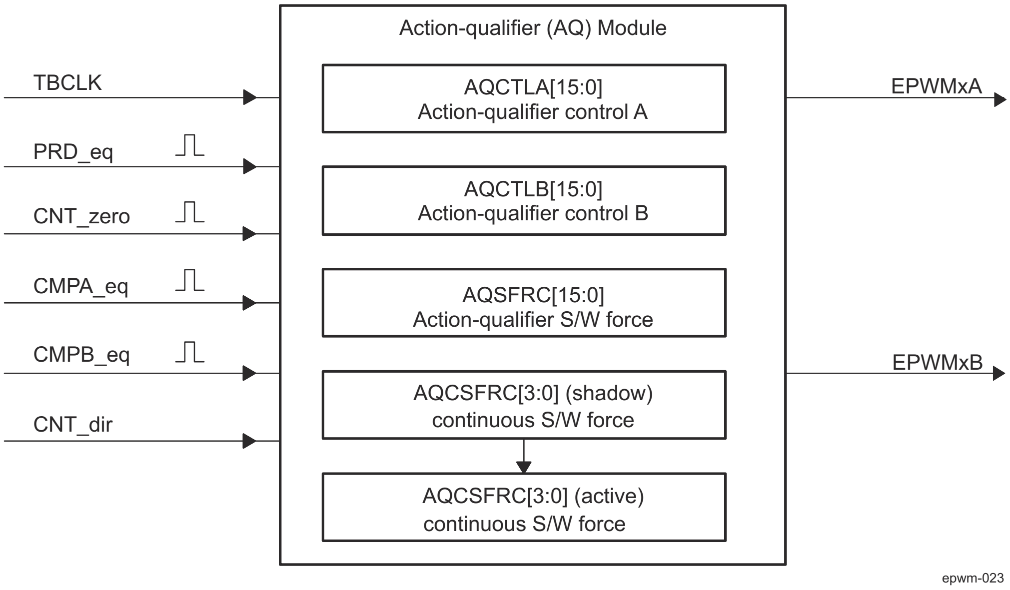

Figure 12-339. EPWM Action-Qualifier Submodule Inputs and Outputs

Table 12-299. EPWM Action-Qualifier Submodule Possible Input Events

Signal	Description	Register Bitfield Compared
PRD_eq	Time-base counter equal to the period value	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero	TBCNT = 0000h
CMPA_eq	Time-base counter equal to the counter-compare A	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the counter-compare B	TBCNT = CMPB
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by EPWM_AQSFRC and EPWM_AQCSFRC registers.

The action-qualifier submodule controls how the two outputs EPWMxA and EPWMxB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs EPWMxA and EPWMxB are:

- **Set High:** Set output EPWMxA or EPWMxB to a high level.
- **Clear Low:** Set output EPWMxA or EPWMxB to a low level.
- **Toggle:** If EPWMxA or EPWMxB is currently pulled high, then pull the output low. If EPWMxA or EPWMxB is currently pulled low, then pull the output high.
- **Do Nothing:** Keep outputs EPWMxA and EPWMxB at same level as currently set. Although the "Do Nothing" option prevents an event from causing an action on the EPWMxA and EPWMxB outputs, this event can still trigger interrupts. See the Event_Trigger (ET) submodule description in Section 12.5.3.4.8 for details.

Actions are specified independently for either output (EPWMxA or EPWMxB). Any or all events can be configured to generate actions on a given output. All qualifier actions are configured via the control registers found at the end of this section.

For clarity, the drawings in this chapter use a set of symbolic actions. These symbols are summarized in Figure 12-340. Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and their time positions are programmed via the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"; it is the default at reset.

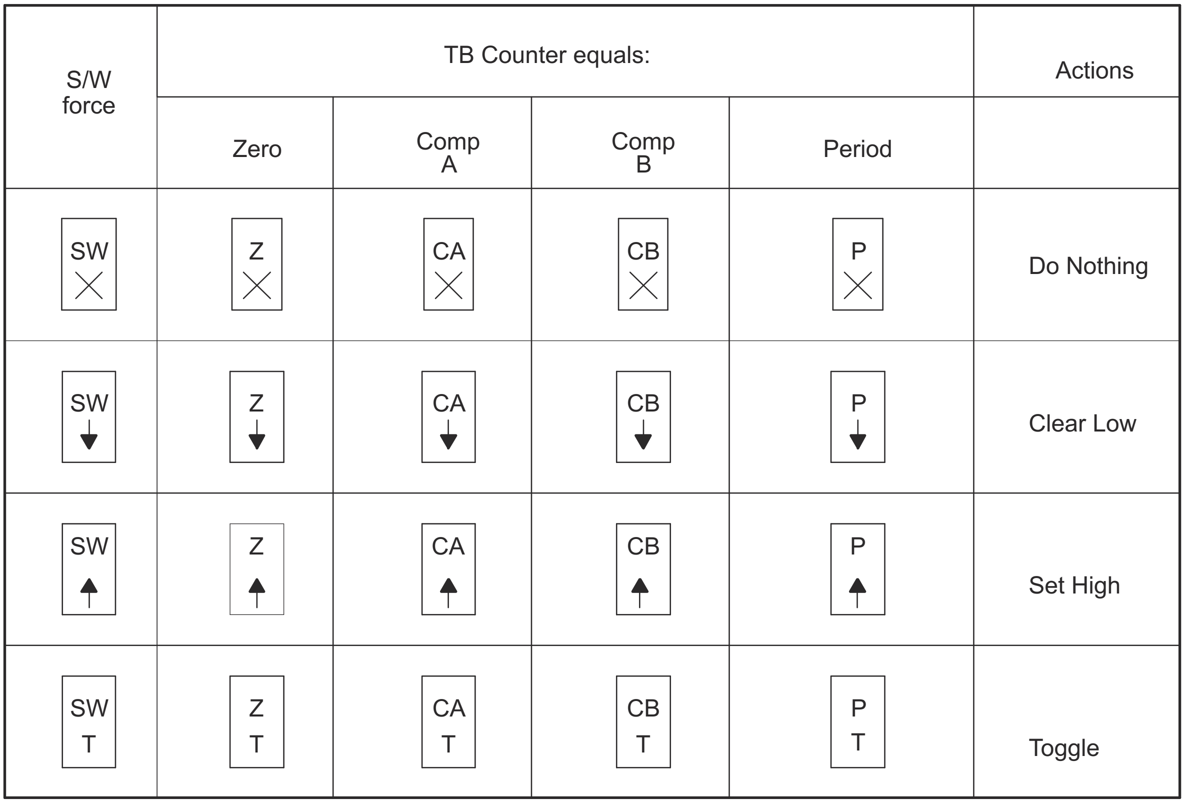

S/W force	TB Counter equals:				Actions
	Zero	Comp A	Comp B	Period	
SW ×	Z ×	CA ×	CB ×	P ×	Do Nothing
SW ↓	Z ↓	CA ↓	CB ↓	P ↓	Clear Low
SW ↑	Z ↑	CA ↑	CB ↑	P ↑	Set High
SW T	Z T	CA T	CB T	P T	Toggle

epwm-024

Figure 12-340. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

12.5.3.4.4.3 EPWM Action-Qualifier Event Priority

It is possible for the EPWM action qualifier to receive more than one event at the same time. In this case events are assigned a priority by the hardware. The general rule is: events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down-count mode are shown in Table 12-288. A priority level 1 is the highest priority and level 7 is the lowest. The priority changes slightly depending on the direction of TBCNT.

Table 12-300. EPWM Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event if TBCNT is Incrementing TBCNT = 0 up to TBCNT = TBPRD	Event if TBCNT is Decrementing TBCNT = TBPRD down to TBCNT = 1
1 (Highest)	Software forced event	Software forced event
2	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
3	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
4	Counter equals zero	Counter equals period (TBPRD in EPWM_TBPRD active register)
5	Counter equals CMPB on down-count (CBD) (1)	Counter equals CMPB on up-count (CBU) (1)
6 (Lowest)	Counter equals CMPA on down-count (CAD) (1)	Counter equals CMPA on up-count (CBU) (1)

(1) To maintain symmetry for up-down-count mode, both up-events (CAU/CBU) and down-events (CAD/CBD) can be generated for TBPRD. Otherwise, up-events can occur only when the counter is incrementing and down-events can occur only when the counter is decrementing.

Table 12-289 shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up and thus down-count events will never be taken.

Table 12-301. EPWM Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	Counter equal to CMPB on up-count (CBU)
4	Counter equal to CMPA on up-count (CAU)
5 (Lowest)	Counter equal to Zero

Table 12-290 shows the action-qualifier priority for down-count mode. In this case, the counter direction is always defined as down and thus up-count events will never be taken.

Table 12-302. EPWM Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

It is possible to set the compare value greater than the period. In this case the action will take place as shown in Table 12-291.

Table 12-303. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAU/CBU	Compare on Down-Count Event CAU/CBU
Up-Count Mode	If CMPA/CMPB ≤ TBPRD period, then the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB > TBPRD, then the event will not occur.	Never occurs.
Down-Count Mode	Never occurs.	If CMPA/CMPB < TBPRD, the event will occur on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).
Up-Down-Count Mode	If CMPA/CMPB < TBPRD and the counter is incrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB is ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).	If CMPA/CMPB < TBPRD and the counter is decrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCNT = TBPRD).

12.5.3.4.4.4 Waveforms for Common EPWM Configurations

Note

The waveforms in this chapter show the EPWMs behavior for a static compare register value. In a running system, the active compare registers (EPWM_CMPA and EPWM_CMPB) are typically updated from their respective shadow registers once every period. The user specifies when the update will take place — either when the time-base counter reaches zero or when the time-base counter reaches period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down-count mode to generate a symmetric PWM:

- If EPWM_CMPA / EPWM_CMPB is loaded on zero, then use EPWM_CMPA / EPWM_CMPB values greater than or equal to 1.
- If EPWM_CMPA / EPWM_CMPB is loaded on period, then use EPWM_CMPA / EPWM_CMPB values less than or equal to TBPRD - 1.

  This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down-count mode to generate an asymmetric PWM:

- To achieve 50-0% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on TBPRD. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

Figure 12-341 shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCNT. In this mode 0-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing the CMPA match will pull the PWM output high. Likewise, when the counter is decrementing the compare match will pull the PWM signal low. When CMPA = 0, the PWM signal is low for the entire period giving the 0% duty waveform. When EPWM_CMPA = EPWM_TBPRD, the PWM signal is high achieving 100% duty.

When using this configuration in practice, if CMPA/CMPB is loaded on zero, then use CMPA/CMPB values greater than or equal to 1. If CMPA/CMPB is loaded on period, then use CMPA/CMPB values less than or equal to TBPRD - 1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

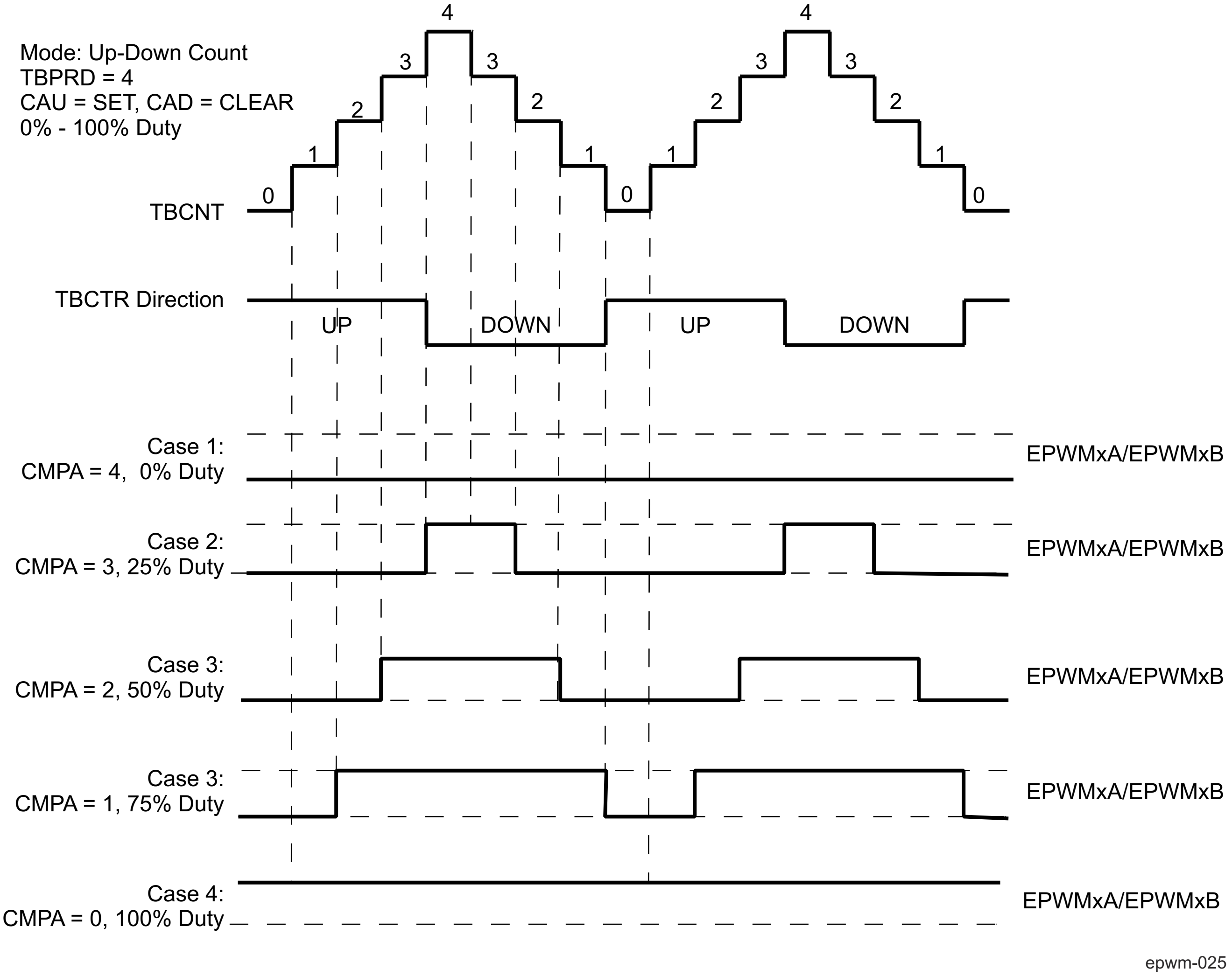

Figure 12-341. EPWM Up-Down-Count Mode Symmetrical Waveform

The PWM waveforms in Figure 12-342 through Figure 12-347 show some common action-qualifier configurations. Some conventions used in the figures are as follows:

- TBPRD, CMPA, and CMPB refer to the value written in their respective registers (EPWM_TBPRD, EPWM_CMPA, and EPWM_CMPB). The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either CMPA or CMPB.
- EPWMxA and EPWMxB refer to the output signals from EPWMx
- Up-Down means Count-up-and-down mode, Up means up-count mode and Dwn means down-count mode
- Sym = Symmetric, Asym = Asymmetric

Table 12-292 and Table 12-293 contain initialization and runtime register configurations for the waveforms in Figure 12-342.

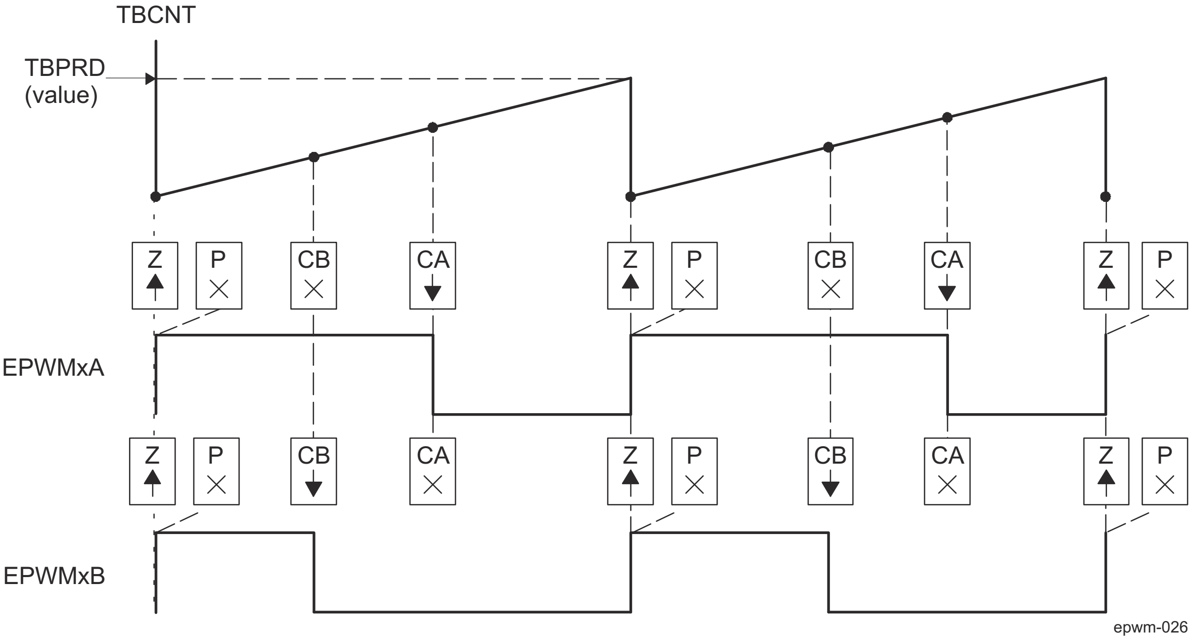

Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active high (that is, high time duty proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active high (that is, high time duty proportional to CMPB).

Note

The "Do Nothing" actions (X) are shown for completeness, but will not be shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-342. Up, Single Edge Asymmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active High

Table 12-304. EPWMx Initialization for Figure 12-342

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	ZRO	AQ_SET	
	CAU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_SET	
	CBU	AQ_CLEAR	

Table 12-305. EPWMx Run Time Changes for Figure 12-342

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-294 and Table 12-295 contain initialization and runtime register configurations for the waveforms in Figure 12-343.

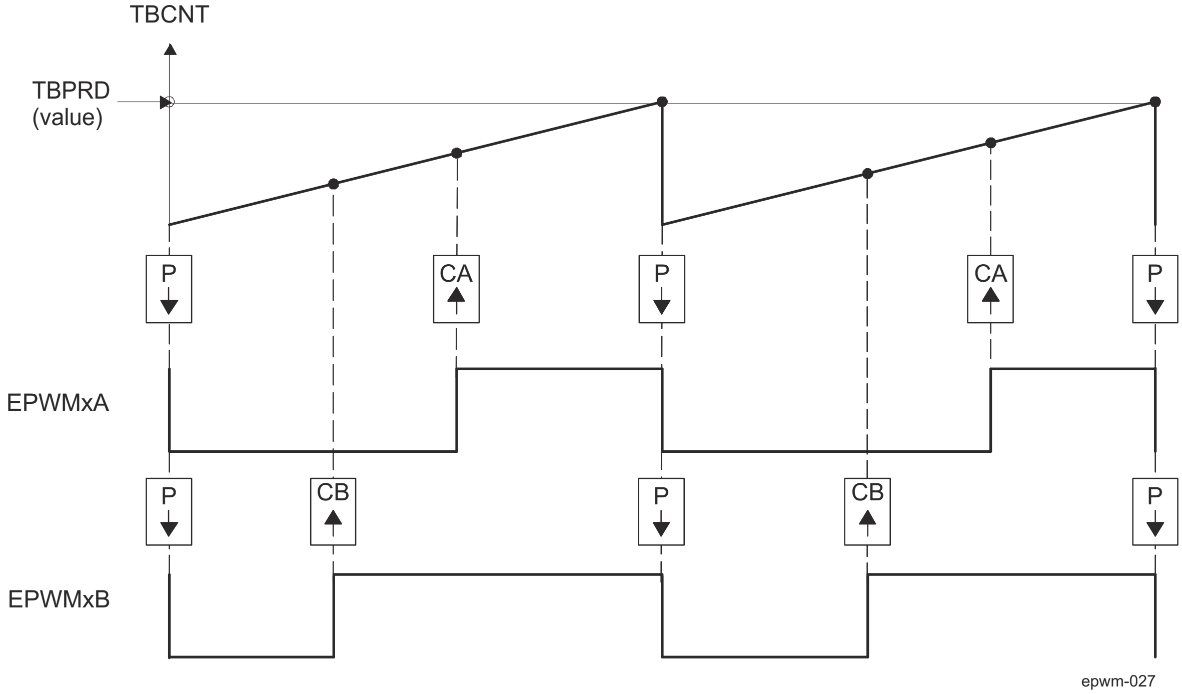

Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

The Do Nothing actions (X) are shown for completeness here, but will not be shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-343. Up, Single Edge Asymmetric Waveform With Independent Modulation on EPWMxA and EPWMxB — Active Low

Table 12-306. EPWMx Initialization for Figure 12-343

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	PRD	AQ_CLEAR	
	CAU	AQ_SET	
EPWM_AQCTLB	PRD	AQ_CLEAR	
	CBU	AQ_SET	

Table 12-307. EPWMx Run Time Changes for Figure 12-343

Register	Bit	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-296 and Table 12-297 contain initialization and runtime register configurations for the waveforms Figure 12-344. Use the code in Section 12.5.3.4.1.1 to define the headers.

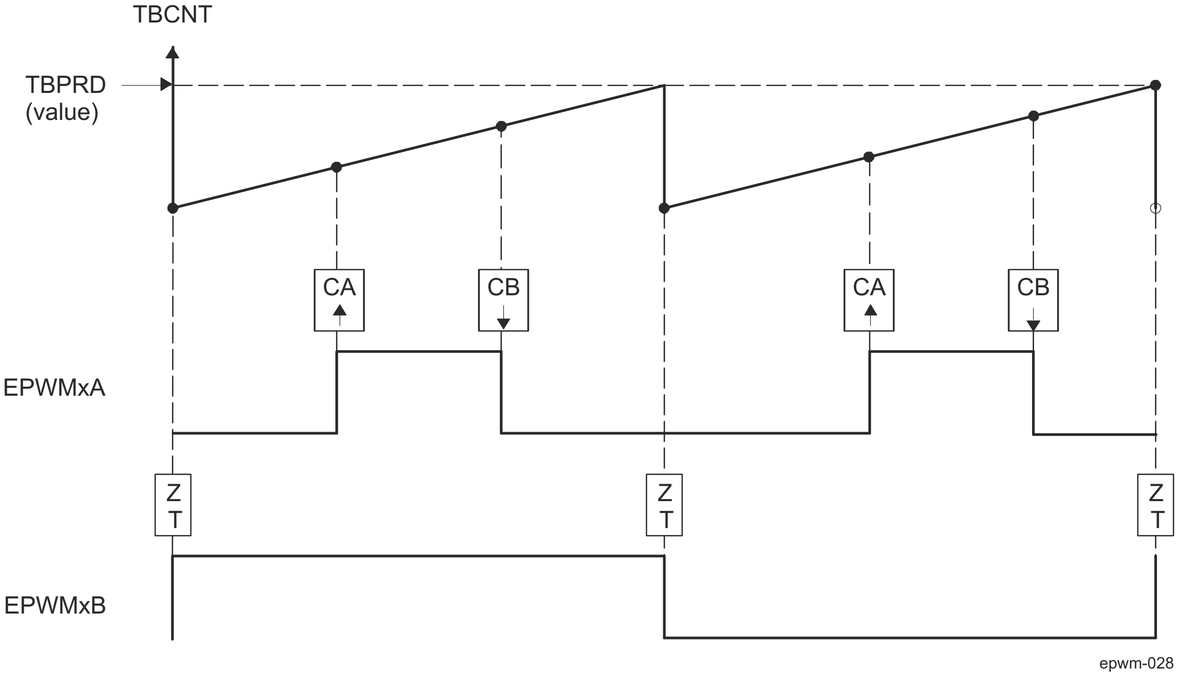

Note

PWM frequency = 1/((TBPRD + 1) × T_{TBCLK})

Note

Pulse can be placed anywhere within the PWM cycle (0000h - TBPRD)

Note

High time duty proportional to (CMPB - CMPA)

Note

EPWMxB can be used to generate a 50% duty square wave with frequency = 1/2 × ((TBPRD + 1) × TBCLK)

Figure 12-344. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA

Table 12-308. EPWMx Initialization for Figure 12-344

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	200 (C8h)	Compare A = 200 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_TOGGLE	

Table 12-309. EPWMx Run Time Changes for Figure 12-344

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	

Table 12-298 and Table 12-299 contain initialization and runtime register configurations for the waveforms in Figure 12-345. Use the code in Section 12.5.3.4.1.1 to define the headers.

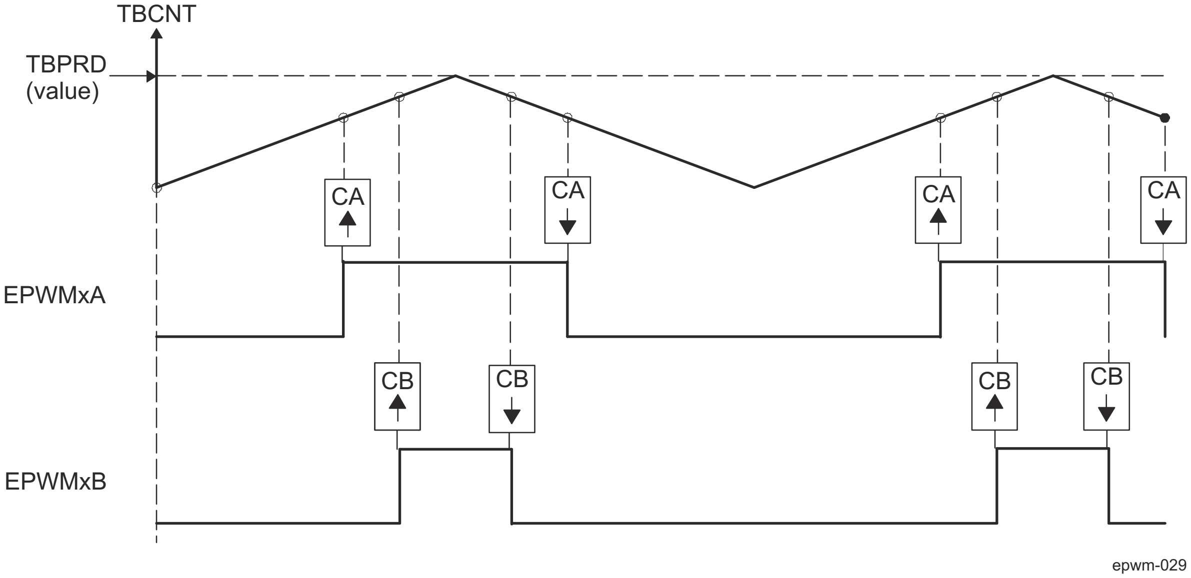

Note

PWM period = 2 x TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

Outputs EPWMxA and EPWMxB can drive independent power switches.

Figure 12-345. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active Low

Table 12-310. EPWMx Initialization for Figure 12-345

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	400 (190h)	Compare A = 400 TBCLK counts
EPWM_CMPB	CMPB	500 (1F4h)	Compare B = 500 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_SET	
	CBD	AQ_CLEAR	

Table 12-311. EPWMx Run Time Changes for Figure 12-345

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-300 and Table 12-301 contain initialization and runtime register configurations for the waveforms in Figure 12-346. Use the code in Section 12.5.3.4.1.1 to define the headers.

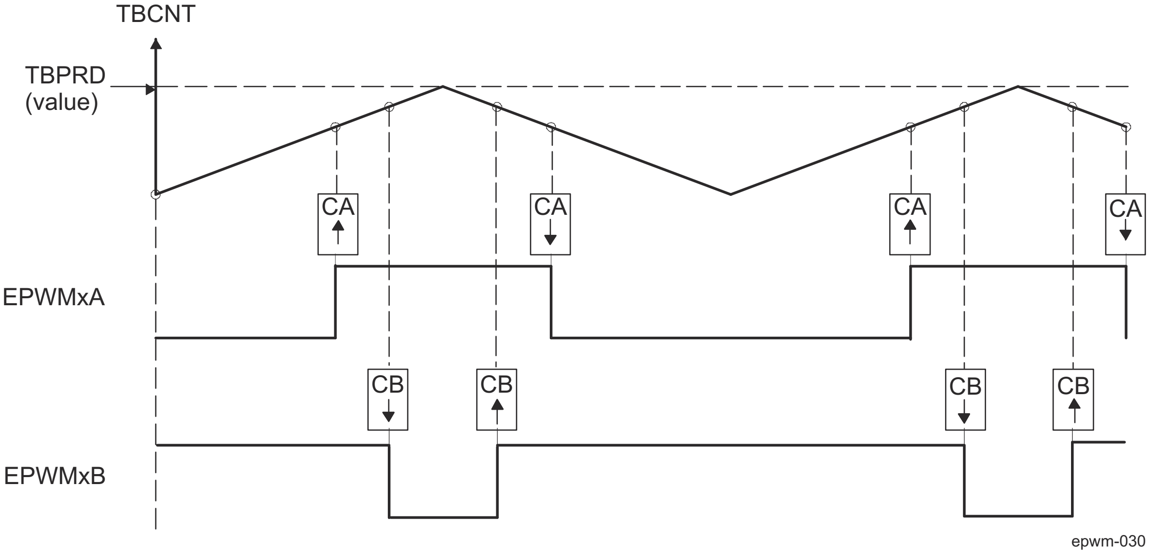

Note

PWM period = 2 × TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low, that is, low time duty proportional to CMPA.

Note

Duty modulation for EPWMxB is set by CMPB and is active high, that is, high time duty proportional to CMPB.

Note

Outputs EPWMx can drive upper/lower (complementary) power switches.

Note

Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 12-346. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Complementary

Table 12-312. EPWMx Initialization for Figure 12-346

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_CLEAR	
	CBD	AQ_SET	

Table 12-313. EPWMx Run Time Changes for Figure 12-346

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-302 and Table 12-303 contain initialization and runtime register configurations for the waveforms in Figure 12-347. Use the code in Section 12.5.3.4.1.1 to define the headers.

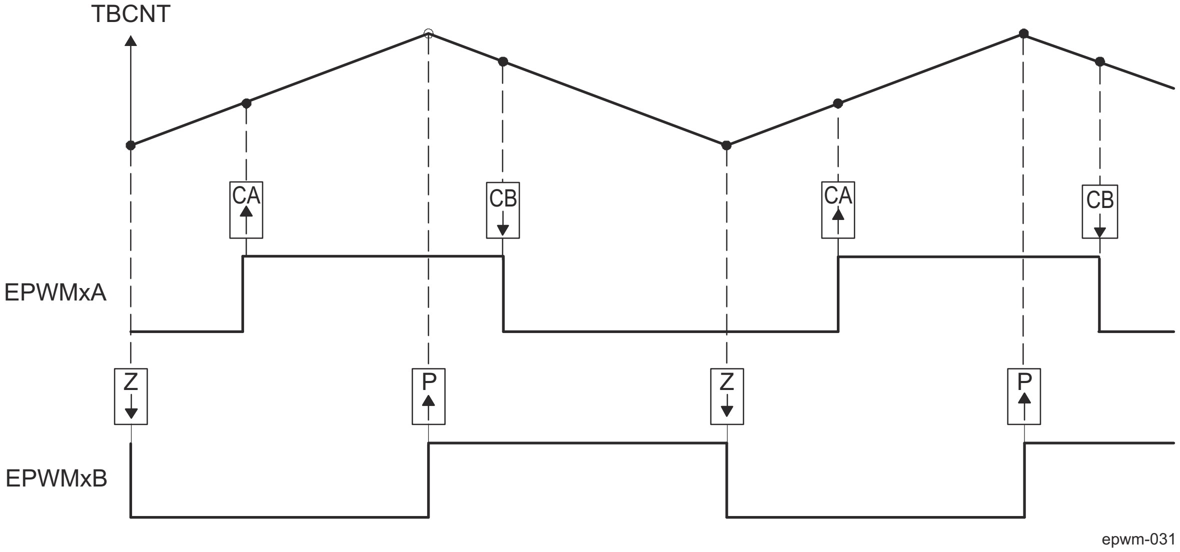

Note

PWM period = 2 × TBPRD × TBCLK

Note

Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.

Note

Duty modulation for EPWMxA is set by CMPA and CMPB.

Note

Low time duty for EPWMxA is proportional to (CMPA + CMPB).

Note

To change this example to active high, CMPA and CMPB actions need to be inverted (that is, Set ! Clear and Clear Set).

Note

Duty modulation for EPWMxB is fixed at 50% (utilizes spare action resources for EPWMxB).

Figure 12-347. Up-Down-Count, Dual Edge Asymmetric Waveform, With Independent Modulation on EPWMxA — Active Low

Table 12-314. EPWMx Initialization for Figure 12-347

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	250 (FAh)	Compare A = 250 TBCLK counts
EPWM_CMPB	CMPB	450 (1C2h)	Compare B = 450 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBD	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_CLEAR	
	PRD	AQ_SET	

Table 12-315. EPWMx Run Time Changes for Figure 12-347

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	Adjust duty for output EPWM1B

12.5.3.4.5 EPWM Dead-Band Generator (DB) Submodule

This section describes the Dead-Band Generator (DB) submodule in the PWM module.

12.5.3.4.5.1 Overview

Figure 12-348 illustrates the dead-band generator submodule within the EPWM module.

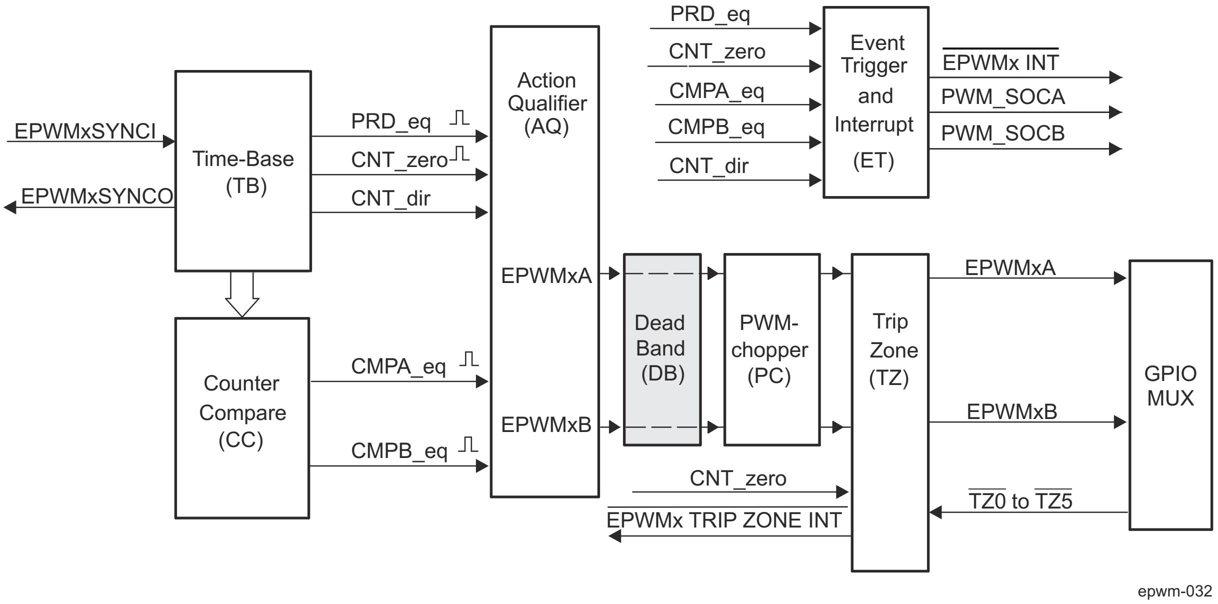

Figure 12-348. Dead-Band Generator Submodule

The "Action-qualifier (AQ) Module" section discussed how it is possible to generate the required dead-band by having full control over edge placement using both the CMPA and CMPB resources of the EPWM module. However, if the more classical edge delay-based dead-band with polarity control is required, then the dead-band generator submodule should be used.

The key functions of the dead-band generator submodule are:

- Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input
- Programming signal pairs for:
  - Active high (AH)
  - Active low (AL)
  - Active high complementary (AHC)
  - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in Figure 12-348)

12.5.3.4.5.2 Controlling and Monitoring the EPWM Dead-Band Submodule

The dead-band generator submodule operation is controlled and monitored via the following registers:

Table 12-316. Dead-Band Generator Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_DBCTL	Dead-Band Control Register	1Eh	No
EPWM_DBRED	Dead-Band Rising Edge Delay Count Register	20h	No
EPWM_DBFED	Dead-Band Falling Edge Delay Count Register	22h	No

12.5.3.4.5.3 Operational Highlights for the EPWM Dead-Band Generator Submodule

The dead-band submodule has two groups of independent selection options as shown in Figure 12-349.

- **Input Source Selection:** The input signals to the dead-band module are the EPWMxA and EPWMxB output signals from the action-qualifier. In this section they will be referred to as EPWMxA In and EPWMxB In. Using the EPWM_DBCTL[5-4] IN_MODE control bits, the signal source for each delay, falling-edge or rising-edge, can be selected:
  - EPWMxA In is the source for both falling-edge and rising-edge delay. This is the default mode.
  - EPWMxA In is the source for falling-edge delay, EPWMxB In is the source for rising-edge delay.
  - EPWMxA In is the source for rising edge delay, EPWMxB In is the source for falling-edge delay.
  - EPWMxB In is the source for both falling-edge and rising-edge delay.
- **Output Mode Control:** The output mode is configured by way of the EPWM_DBCTL[1-0] OUT_MODE bit fields. These bits determine if the falling-edge delay, rising-edge delay, neither, or both are applied to the input signals.
- **Polarity Control:** The polarity control (EPWM_DBCTL[3-2] POLSEL) allows to be specified whether the rising-edge delayed signal and/or the falling-edge delayed signal is to be inverted before being sent out of the dead-band submodule.

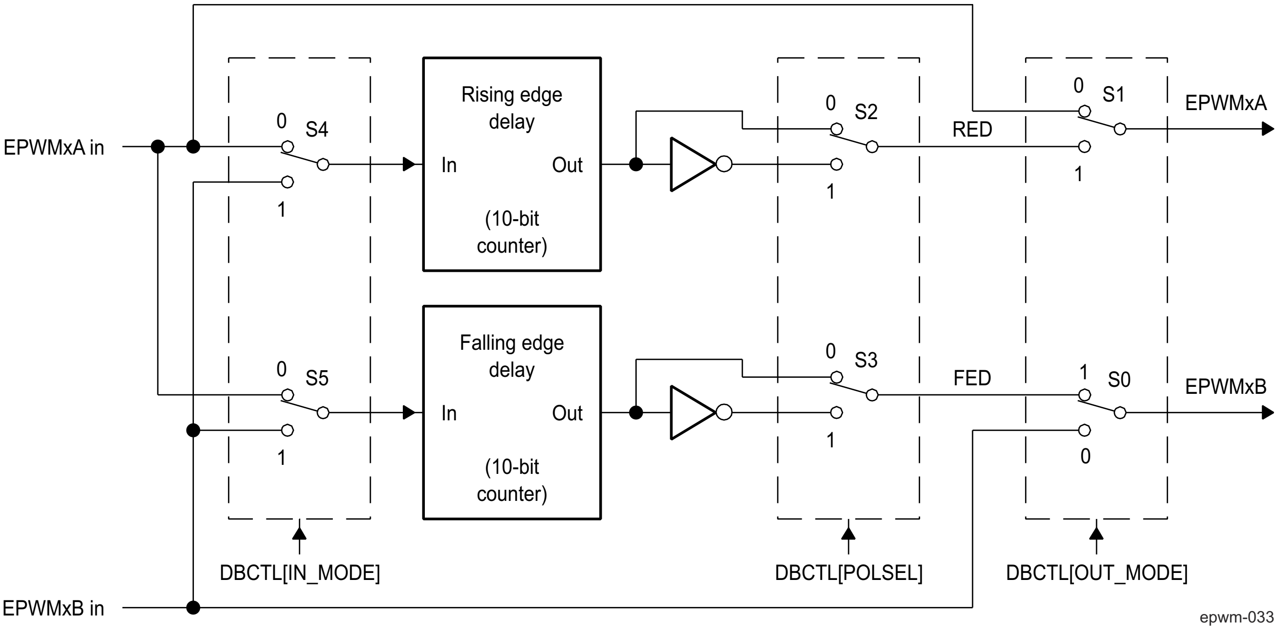

Figure 12-349. Configuration Options for the EPWM Dead-Band Generator Submodule

Although all combinations are supported, not all are typical usage modes. Table 12-305 lists some classical dead-band configurations. These modes assume that the EPWM_DBCTL[5-4] IN_MODE is configured such that EPWMxA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in Table 12-305 fall into the following categories:

- **Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED)** Allows to be fully disabled the dead-band submodule from the PWM signal path.
- **Mode 2-5: Classical Dead-Band Polarity Settings** These represent typical polarity configurations that should address all the active high/low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in Figure 12-350. Note that to generate equivalent waveforms to Figure 12-350, configure the action-qualifier submodule to generate the signal as shown for EPWMxA.
- **Mode 6: Bypass rising-edge-delay andMode 7: Bypass falling-edge-delay** Finally the last two entries in Table 12-305 show combinations where either the falling-edge-delay (FED) or rising-edge-delay (RED) blocks are bypassed.

Table 12-317. Classical Dead-Band Operating Modes

		EPWM_DBCTL[3-2] POLSEL		EPWM_DBCTL[1-0] OUT_MODE	
Mode	Mode Description [1]	S3	S2	S1	S0
1	EPWMxA and EPWMxB Passed Through (No Delay)	x	x	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay) EPWMxB Out = EPWMxA In with Falling Edge Delay	0 or 1	0 or 1	0	1
7	EPWMxA Out = EPWMxA In with Rising Edge Delay EPWMxB Out = EPWMxB In with No Delay	0 or 1	0 or 1	1	0

(1) These are classical dead-band modes and assume that EPWM_DBCTL[5-4] IN_MODE = 0h0. That is, EPWMxA in is the source for both the falling-edge and rising-edge delays. Enhanced, non-traditional modes can be achieved by changing the IN_MODE configuration.

Figure 12-350 shows waveforms for typical cases where 0% < duty < 100%.

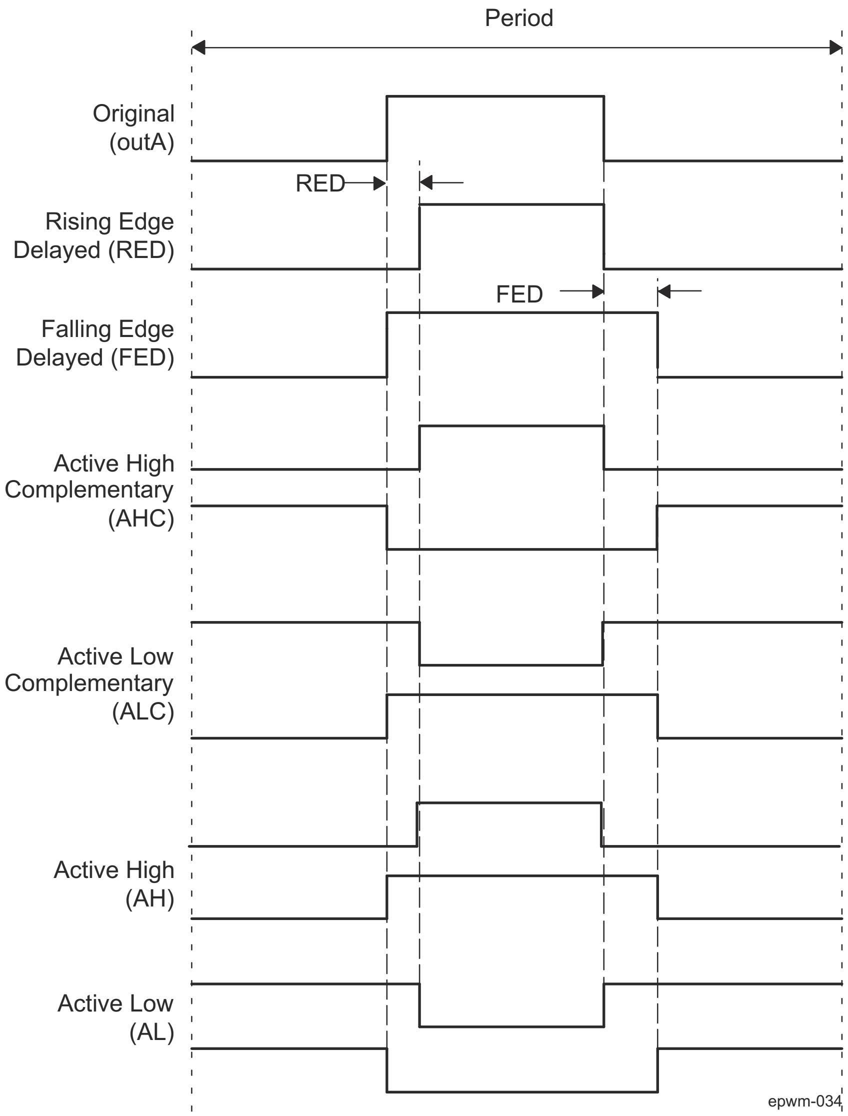

Figure 12-350. Dead-Band Waveforms for Typical Cases (0% < Duty < 100%)

The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the EPWM_DBRED and EPWM_DBFED registers. These are 10-bit registers and their value represents the number of time-base clock, TBCLK, periods a signal edge is delayed by. For example, the formulas to calculate falling-edge-delay and rising-edge-delay are:

$FED = EPWM\_DBFED \times T_{TBCLK}$

$RED = EPWM\_DBRED \times T_{TBCLK}$

Where T_{TBCLK} is the period of TBCLK, the prescaled version of FICLK.

12.5.3.4.6 EPWM-Chopper (PC) Submodule

This section describes the PWM-Chopper (PC) submodule in the PWM module.

12.5.3.4.6.1 Overview

Figure 12-351 illustrates the PWM-chopper (PC) submodule within the EPWM module. The PWM-chopper submodule allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band submodules. This capability is important if a pulse transformer-based gate drivers to control the power switching elements is needed.

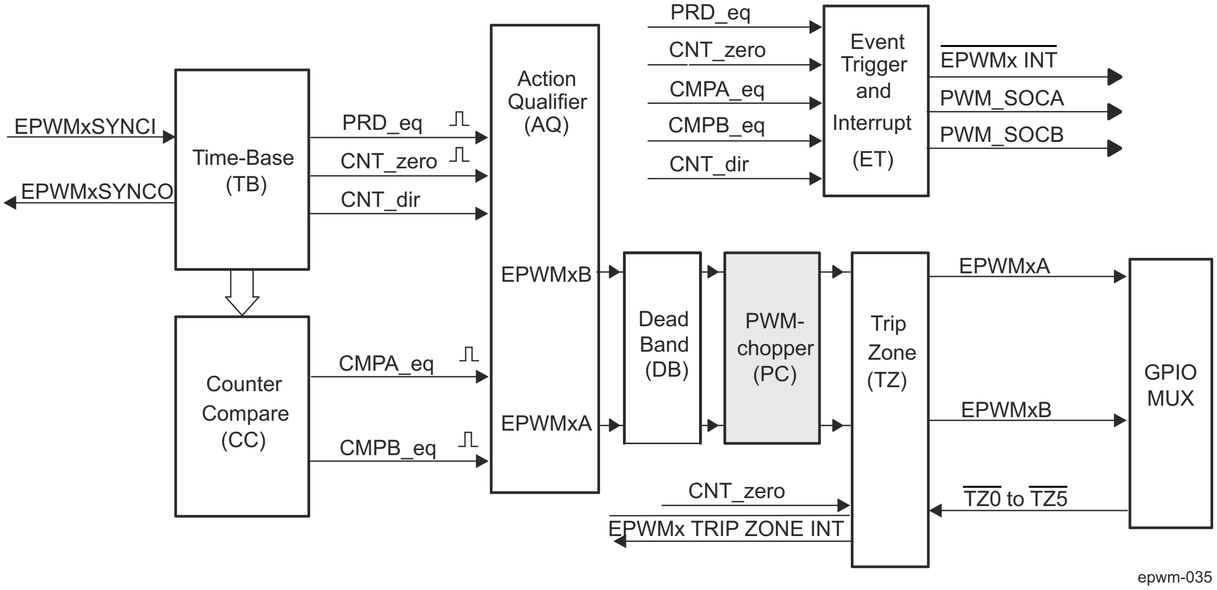

Figure 12-351. PWM-Chopper Submodule

12.5.3.4.6.2

PC module key features:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

12.5.3.4.6.3 Controlling the EPWM-Chopper Submodule

The EPWM-chopper submodule operation is controlled via the register in Table 12-306.

Table 12-318. EPWM-Chopper Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_PCCTL	PWM-chopper Control Register	3Ch	No

12.5.3.4.6.4 Operational Highlights for the EPWM-Chopper Submodule

Figure 12-352 shows the operational details of the EPWM-chopper submodule. The carrier clock is derived from FICLK. Its frequency and duty cycle are controlled via the CHPFREQ and CHPDUTY bits in the EPWM_PCCTL register. The one-shot block is a feature that provides a high energy first pulse to ensure hard and fast power switch turn on, while the subsequent pulses sustain pulses, ensuring the power switch remains on. The one-shot width is programmed via the OSHTWTH bits. The PWM-chopper submodule can be fully disabled (bypassed) via the CHPEN bit.

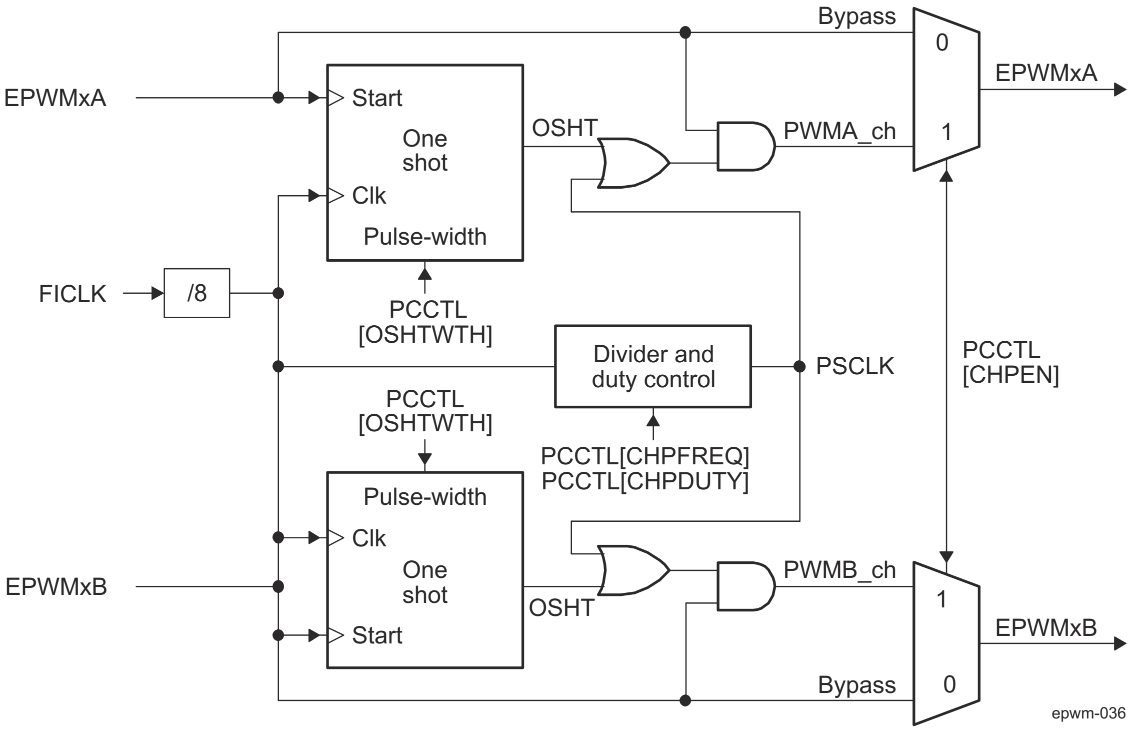

Figure 12-352. PWM-Chopper Submodule Signals and Registers

12.5.3.4.6.5 EPWM-Chopper Waveforms

Figure 12-353 shows simplified waveforms of the chopping action only; one-shot and duty-cycle control are not shown. Details of the one-shot and duty-cycle control are discussed in the following sections.

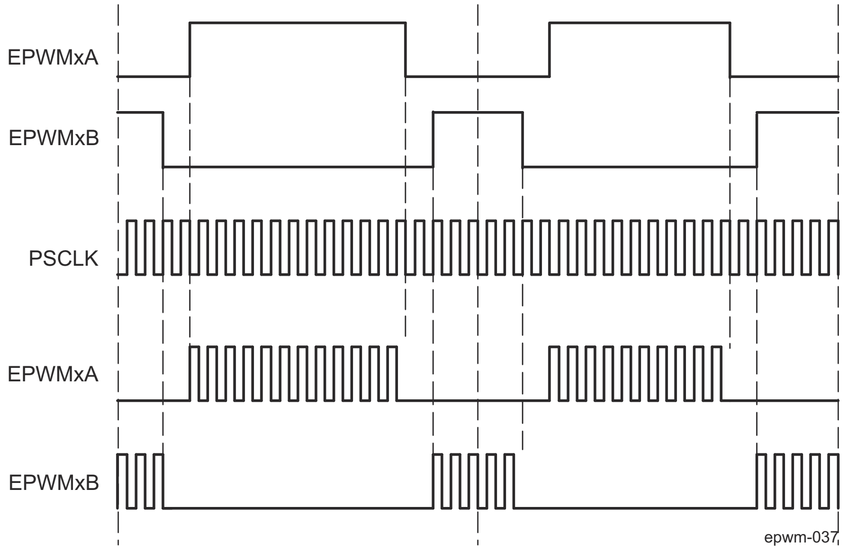

Figure 12-353. Simple EPWM-Chopper Submodule Waveforms Showing Chopping Action Only

12.5.3.4.6.5.1 EPWM-Chopper One-Shot Pulse

The width of the first pulse can be programmed to any of 16 possible pulse width values. The width or period of the first pulse is given by:

$T_{1stpulse} = T_{FICLK} \times 8 \times OSHTWTH$

Where T_{FICLK} is the period of the system clock (FICLK) and OSHTWTH is the four control bits (value from 1 to 16)

Figure 12-354 shows the first and subsequent sustaining pulses.

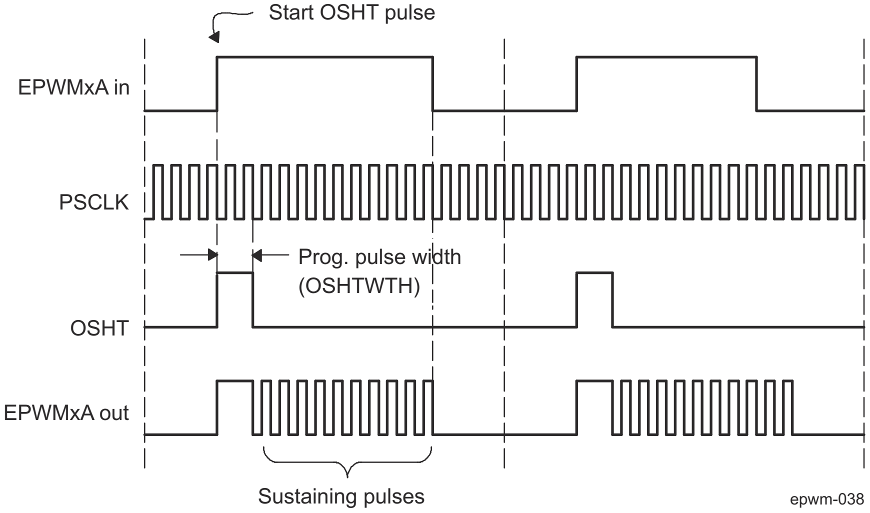

Figure 12-354. EPWM-Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses

12.5.3.4.6.5.2 EPWM-Chopper Duty Cycle Control

Pulse transformer-based gate drive designs need to comprehend the magnetic properties or characteristics of the transformer and associated circuitry. Saturation is one such consideration. To assist the gate drive designer, the duty cycles of the second and subsequent pulses have been made programmable. These sustaining pulses ensure the correct drive strength and polarity is maintained on the power switch gate during the on period, and hence a programmable duty cycle allows a design to be tuned or optimized via software control.

Figure 12-355 shows the duty cycle control that is possible by programming the CHPDUTY bits. One of seven possible duty ratios can be selected ranging from 12.5 to 87.5%.

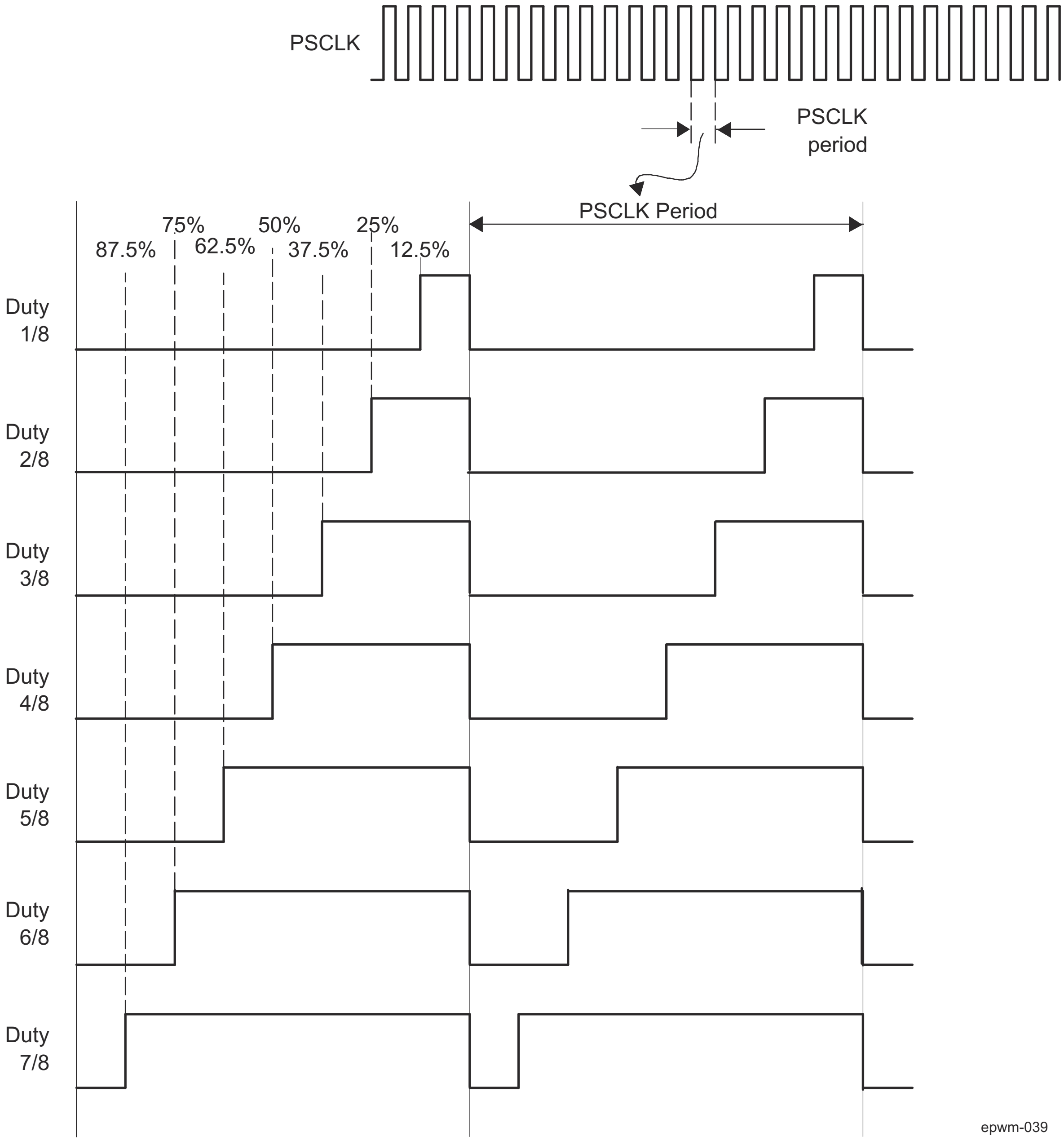

Figure 12-355. EPWM-Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses

12.5.3.4.7 EPWM Trip-Zone (TZ) Submodule

This section describes the Trip-Zone (TZ) submodule in the PWM module.

12.5.3.4.7.1 Overview

Figure 12-356 shows how the trip-zone (TZ) submodule fits within the EPWM module. Each EPWM module is connected to six $\overline{\text{TZ}}$ signals ($\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$) that are sourced from the GPIO MUX. These signals indicates external fault or trip conditions, and the EPWM outputs can be programmed to respond accordingly when faults occur. See *EPWM Integration* to determine the number of trip-zone pins available for the device.

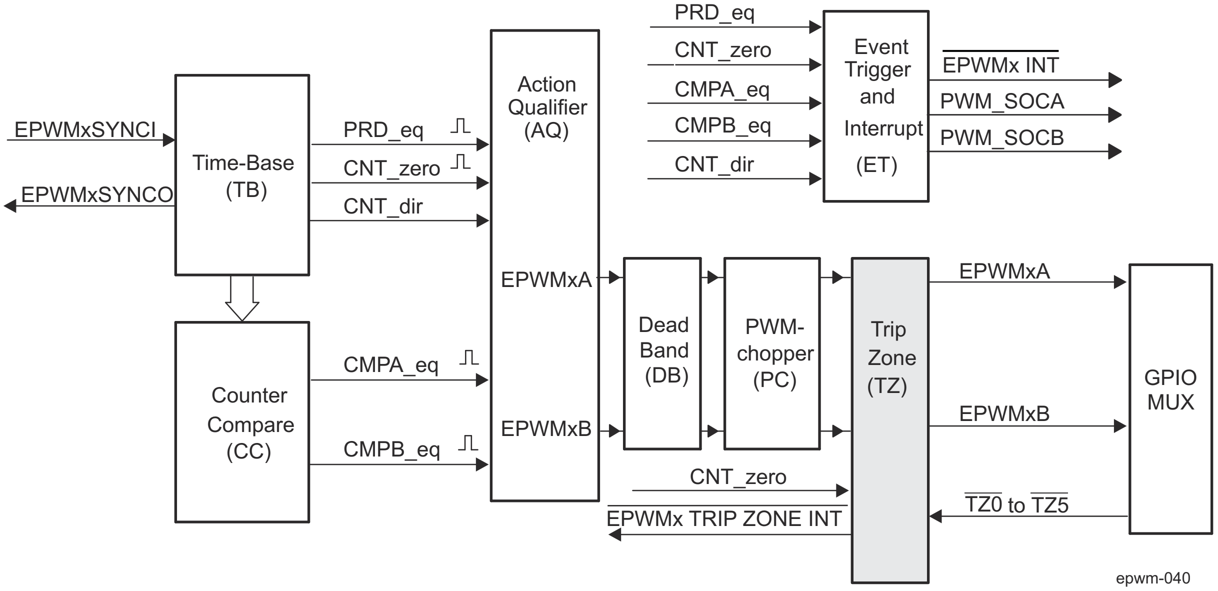

Figure 12-356. EPWM Trip-Zone Submodule

The key functions of the trip-zone submodule are:

- Trip inputs $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ can be flexibly mapped to any EPWM module.
- Upon a fault condition, outputs EPWMxA and EPWMxB can be forced to one of the following:
  - High
  - Low
  - High-impedance
  - No action taken
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Each trip-zone input pin can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone pin.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if it is not required.

Note

For each EPWMx module, 6 tripzone input events are supported ($\overline{\text{EPWMx\_TRIP\_TZ[5:0]}}$). Each tripzone input for all EPWMx modules are tied to a common tripzone input pin, so that any EPWMx can be triggered by any of the six tripzone inputs.

12.5.3.4.7.2 Controlling and Monitoring the EPWM Trip-Zone Submodule

The trip-zone submodule operation is controlled and monitored through the following registers:

Table 12-319. EPWM Trip-Zone Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TZSEL	Trip-Zone Select Register (1)	24h	No
EPWM_TZCTL	Trip-Zone Control Register (1)	28h	No
EPWM_TZEINT	Trip-Zone Enable Interrupt Register (1)	2Ah	No
EPWM_TZFLG	Trip-Zone Flag Register (1)	2Ch	No
EPWM_TZCLR	Trip-Zone Clear Register (1)	2Eh	No
EPWM_TZFRC	Trip-Zone Force Register (1)	30h	No

(1) All trip-zone registers are EALLOW protected and can be modified only after executing the EALLOW instruction.

12.5.3.4.7.3 Operational Highlights for the EPWM Trip-Zone Submodule

The trip-zone signals at pin $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ is an active-low input signal. When the pin goes low, it indicates that a trip event has occurred. Each EPWM module can be individually configured to ignore or use each of the trip-zone pins. Which trip-zone pins are used by a particular EPWM module is determined by the EPWM_TZSEL register for that specific EPWM module. The trip-zone signal may or may not be synchronized to the system clock (FICLK). A minimum of 1 FICLK low pulse on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs is sufficient to trigger a fault condition in the EPWM module. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs.

The $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs can be individually configured to provide either a cycle-by-cycle or one-shot trip event for a EPWM module. The configuration is determined by the EPWM_TZSEL[5-0] CBCk and EPWM_TZSEL[13-8] OSHTk bit field (where k = 0 to 5 corresponds to the trip pin), respectively.

- **Cycle-by-Cycle (CBC):** When a cycle-by-cycle trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-308 lists the possible actions. In addition, the cycle-by-cycle trip event flag (EPWM_TZFLG[1] CBC) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register.

  The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h) if the trip event is no longer present. Therefore, in this mode, the trip event is cleared or reset every PWM cycle. The EPWM_TZFLG[1] CBC flag bit will remain set until it is manually cleared by writing to the EPWM_TZCLR[1] CBC bit. If the cycle-by-cycle trip event is still present when the EPWM_TZFLG[1] CBC bit is cleared, then it will again be immediately set.
- **One-Shot (OSHT):** When a one-shot trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-308 lists the possible actions. In addition, the one-shot trip event flag (EPWM_TZFLG[2] OST) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register. The one-shot trip condition must be cleared manually by writing to the EPWM_TZCLR[2] OST bit.

The action taken when a trip event occurs can be configured individually for each of the EPWM output pins by way of the EPWM_TZCTL[1-0] TZA and EPWM_TZCTL[3-2] TZB register bit field. One of four possible actions, shown in Table 12-308, can be taken on a trip event.

Table 12-320. Possible Actions On an EPWM Trip Event

EPWM_TZCTL[1-0] TZA and/or EPWM_TZCTL[3-2] TZB	EPWMxA and/or EPWMxB	Comment
0	High-Impedance	Tripped
1h	Force to High State	Tripped
2h	Force to Low State	Tripped
3h	No Change	Do Nothing. No change is made to the output.

Example of EPWM Trip-Zone Configurations

A one-shot trip event on $\overline{\text{TZ0}}$ pulls both EPWM1A, EPWM1B low and also forces EPWM2A and EPWM2B high.

- Configure the EPWM1 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{\text{TZ}}$ as a one-shot event source for EPWM1
  - EPWM_TZCTL[1-0] TZA = 2: EPWM1A will be forced low on a trip event
  - EPWM_TZCTL[3-2] TZB = 2: EPWM1B will be forced low on a trip event
- Configure the EPWM2 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{\text{TZ}}$ as a one-shot event source for EPWM2
  - EPWM_TZCTL[1-0] TZA = 1: EPWM2A will be forced high on a trip event
  - EPWM_TZCTL[3-2] TZB = 1: EPWM2B will be forced high on a trip event

12.5.3.4.7.4 Generating EPWM Trip-Event Interrupts

Figure 12-357 and Figure 12-358 illustrate the trip-zone submodule control and interrupt logic, respectively.

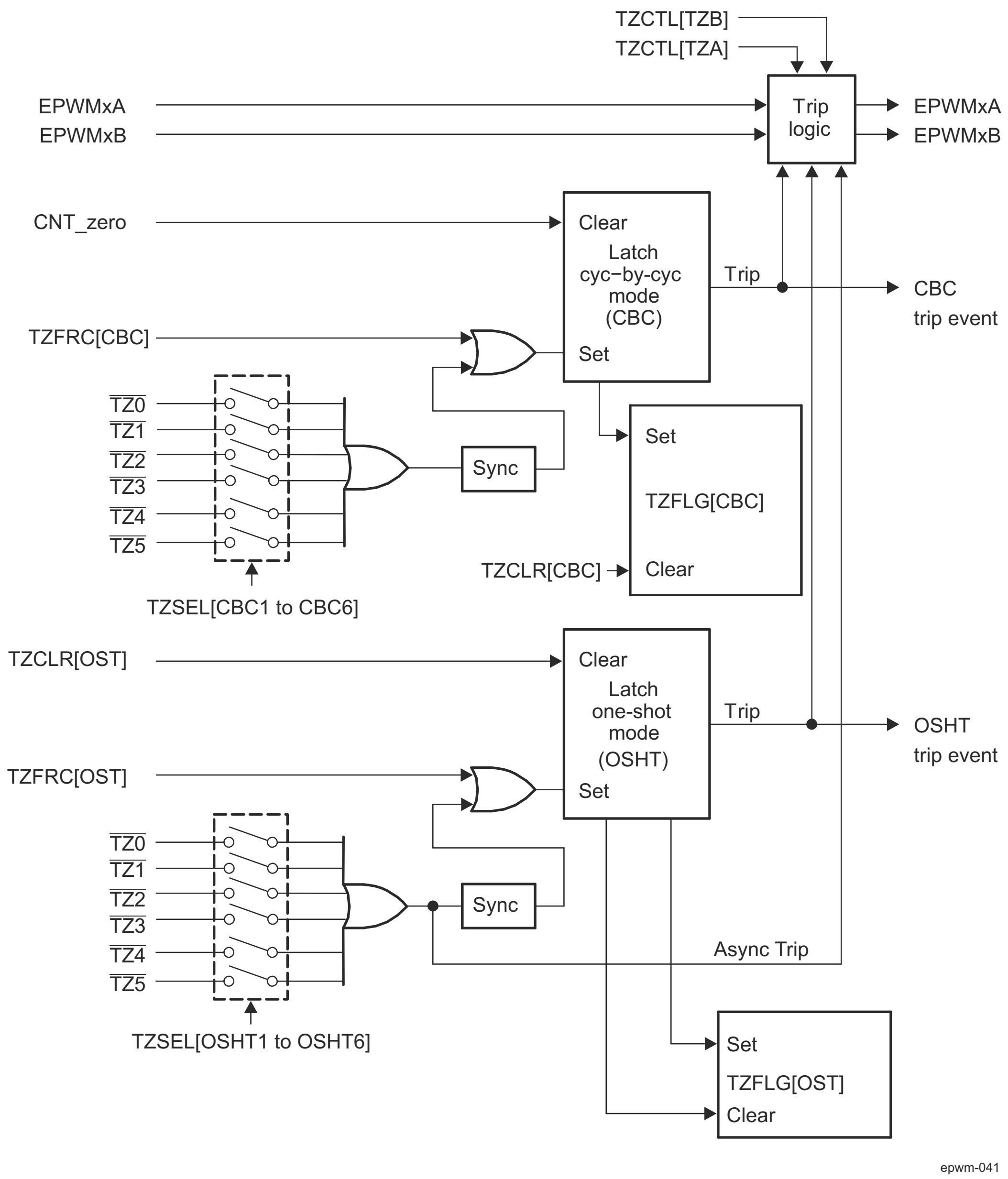

Figure 12-357. EPWM Trip-Zone Submodule Mode Control Logic

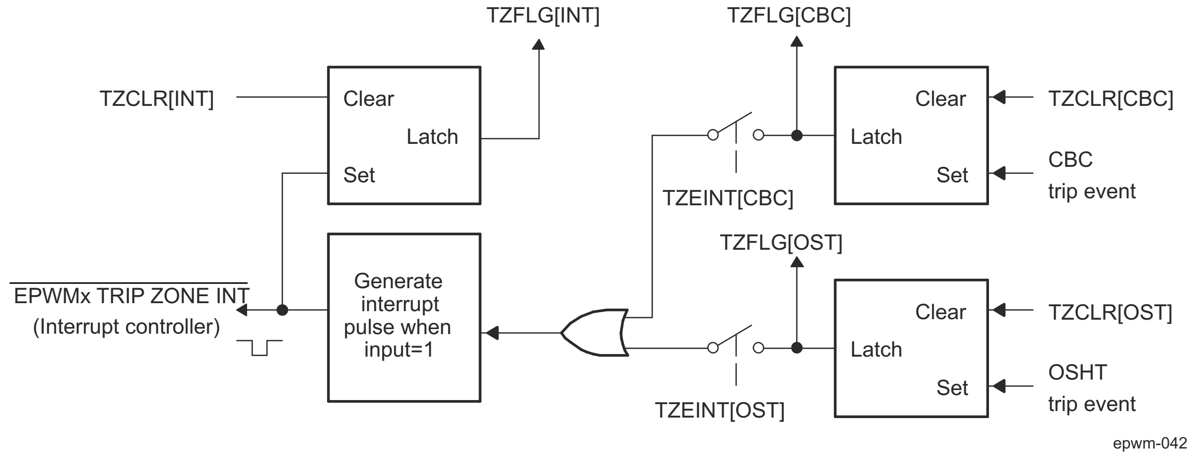

Figure 12-358. EPWM Trip-Zone Submodule Interrupt Logic

12.5.3.4.8 EPWM Event-Trigger (ET) Submodule

This section describes the Event-Trigger (ET) submodule in the PWM module.

12.5.3.4.8.1 Overview

Figure 12-359 shows the event-trigger (ET) submodule in the EPWM system. The event-trigger submodule manages the events generated by the time-base submodule and the counter-compare submodule to generate an aggregated interrupt request.

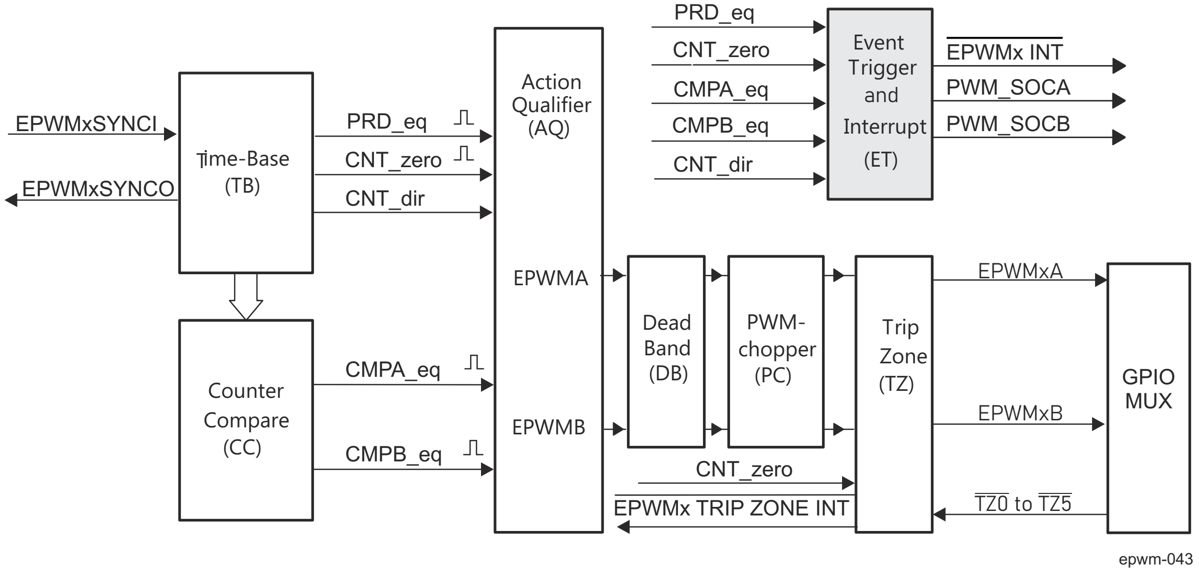

Figure 12-359. EPWM Event-Trigger Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base and counter-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests at:
  - Every event
  - Every second event
  - Every third event
- Provides full visibility of event generation via event counters and flags

12.5.3.4.8.2 Controlling and Monitoring the EPWM Event-Trigger Submodule

The key registers used to configure the event-trigger submodule are shown in Table 12-309:

Table 12-321. EPWM Event-Trigger Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_ETSEL	Event-Trigger Selection Register	32h	No
EPWM_ETPS	Event-Trigger Prescale Register	34h	No
EPWM_ETFLG	Event-Trigger Flag Register	36h	No
EPWM_ETCLR	Event-Trigger Clear Register	38h	No
EPWM_ETFRC	Event-Trigger Force Register	3Ah	No

12.5.3.4.8.3 Operational Overview of the EPWM Event-Trigger Submodule

Each EPWM module has one interrupt request line as shown in Figure 12-360. Mapping interrupt lines to device host interrupt controllers is device specific and is covered in *EPWM Integration*.

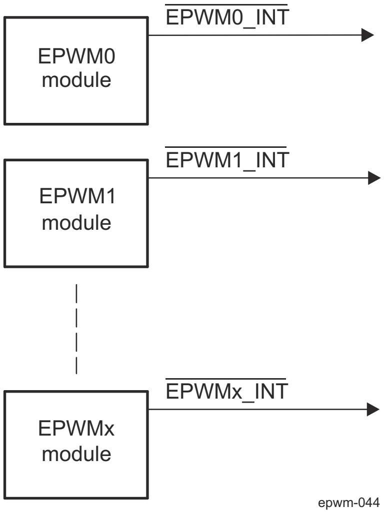

Figure 12-360. EPWM Event-Trigger Submodule Inter-Connectivity to Interrupt Controller

The event-trigger submodule monitors various event conditions (the left side inputs to event-trigger submodule shown in Figure 12-361) and can be configured to prescale these events before issuing an Interrupt request. The event-trigger prescaling logic can issue Interrupt requests at:

- Every event
- Every second event
- Every third event

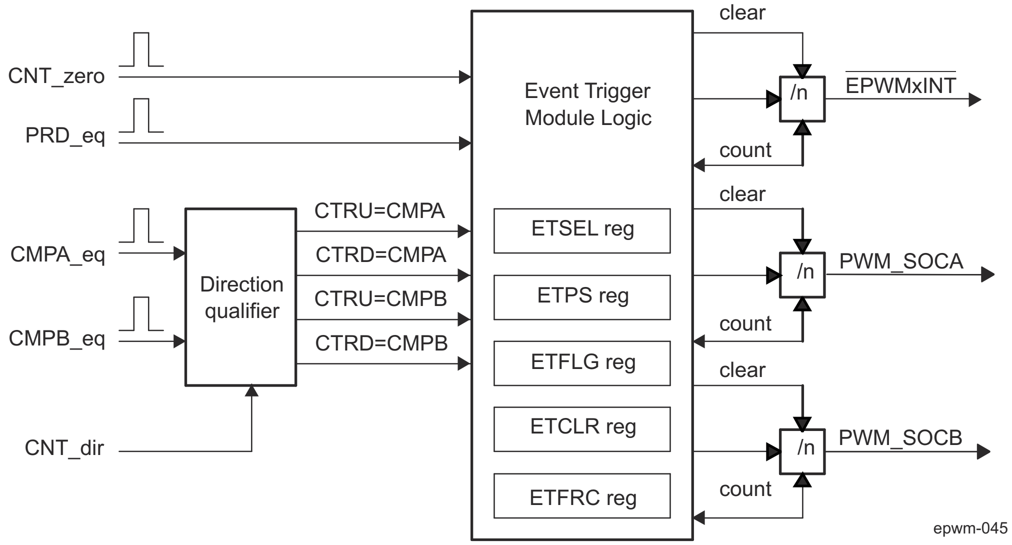

Figure 12-361. EPWM Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs

- ETSEL — This selects which of the possible events will trigger an interrupt.
- ETPS — This programs the event prescaling options previously mentioned.
- ETFLG — These are flag bits indicating status of the selected and prescaled events.
- ETCLR — These bits allow to clear the flag bits in the EPWM_ETFLG register via software.
- ETFRC — These bits allow software forcing of an event. Useful for debugging or software intervention.

A more detailed look at how the various register bits interact with the Interrupt is shown in Figure 12-362.

Figure 12-362 shows the event-trigger's interrupt generation logic. The interrupt-period (EPWM_ETPS[1-0] INTPRD) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt
- Generate an interrupt on every event
- Generate an interrupt on every second event
- Generate an interrupt on every third event

An interrupt cannot be generated on every fourth or more events.

Which event can cause an interrupt is configured by the interrupt selection (EPWM_ETSEL[2-0] INTSEL) bits. The event can be one of the following:

- Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h).
- Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD).
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is decrementing.

The number of events that have occurred can be read from the interrupt event counter (EPWM_ETPS[3-2] INTCNT) register bits. That is, when the specified event occurs the EPWM_ETPS[3-2] INTCNT bits are incremented until they reach the value specified by the EPWM_ETPS[1-0] INTPRD bit field. When EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD the counter stops counting and its output is set. The counter is only cleared when an interrupt is sent to the interrupt controller.

When EPWM_ETPS[3-2] INTCNT reaches EPWM_ETPS[1-0] INTPRD, one of the following behaviors will occur:

- If interrupts are enabled, EPWM_ETSEL[3] INTEN = 1h and the interrupt flag is clear, EPWM_ETFLG[0] INT = 0h, then an interrupt pulse is generated and the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, and the event counter is cleared EPWM_ETPS[3-2] INTCNT = 0h. The counter will begin counting events again.
- If interrupts are disabled, EPWM_ETSEL[3] INTEN = 0h, or the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, the counter stops counting events when it reaches the period value EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD.
- If interrupts are enabled, but the interrupt flag is already set, then the counter will hold its output high until the ENTFLG[0] INT flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing to the INTPRD bits will automatically clear the counter INTCNT = 0 and the counter output will be reset (so no interrupts are generated). Writing a 1h to the EPWM_ETFRC[0] INT bit will increment the event counter INTCNT. The counter will behave as described above when INTCNT = INTPRD. When INTPRD = 0h, the counter is disabled and hence no events will be detected and the EPWM_ETFRC[0] INT bit is also ignored.

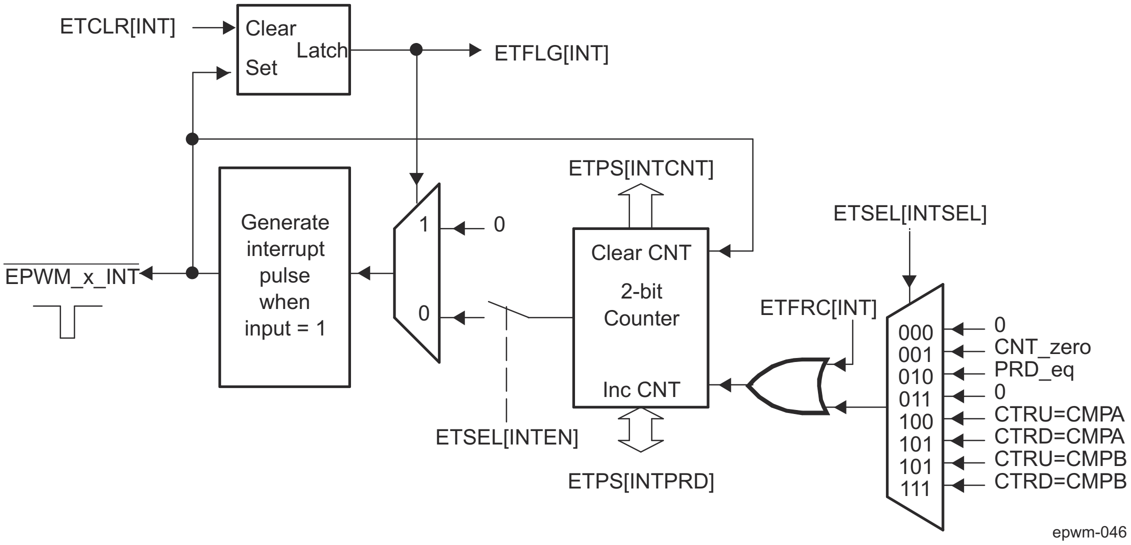

Figure 12-362. EPWM Event-Trigger Interrupt Generator

12.5.3.4.8.4 Operation Overview of the EPWM SOCx Pulse Generator

Figure 12-363 shows the operation of the event-trigger's start-of-conversion-A (SOCA) pulse generator. The EPWM_ETPS[11-10] SOCACNT counter and EPWM_ETPS[9-8] SOCAPRD period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag EPWM_ETFLG[2] SOCA is latched when a pulse is generated, but it does not stop further pulse generation. The enable/disable EPWM_ETSEL[11] SOCAEN bit stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that will trigger an SOCA and SOCB pulse can be configured separately in the EPWM_ETSEL[10-8] SOCASEL and EPWM_ETSEL[14-12] SOCBSEL bit field. The possible events are the same events that can be specified for the interrupt generation logic.

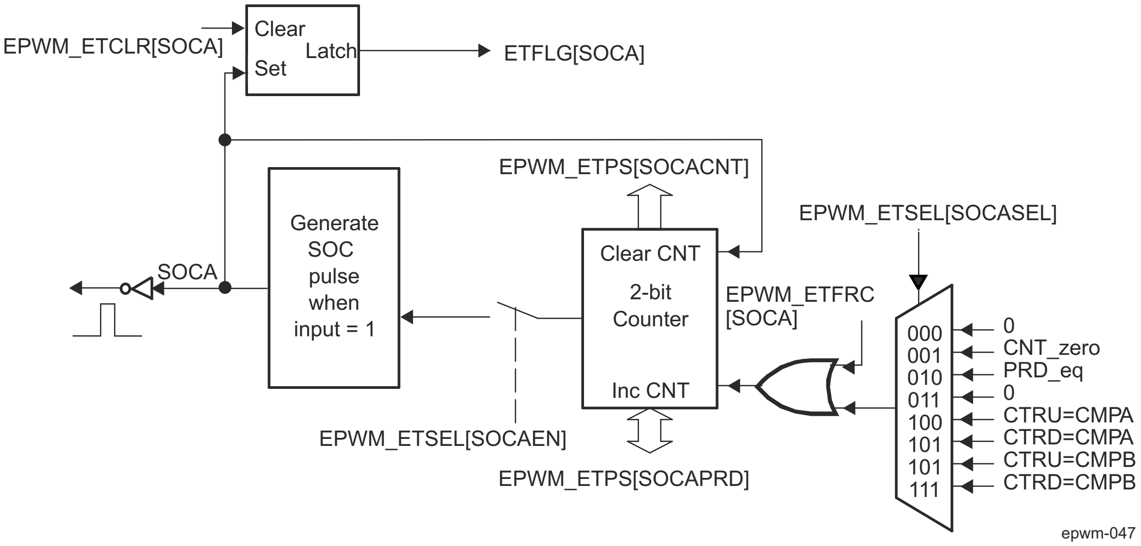

Figure 12-363. EPWM Event-Trigger SOCA Pulse Generator

Figure 12-364 shows the operation of the event-trigger's start-of-conversion-B (SOCB) pulse generator. The event-trigger's SOCB pulse generator operates the same way as the SOCA.

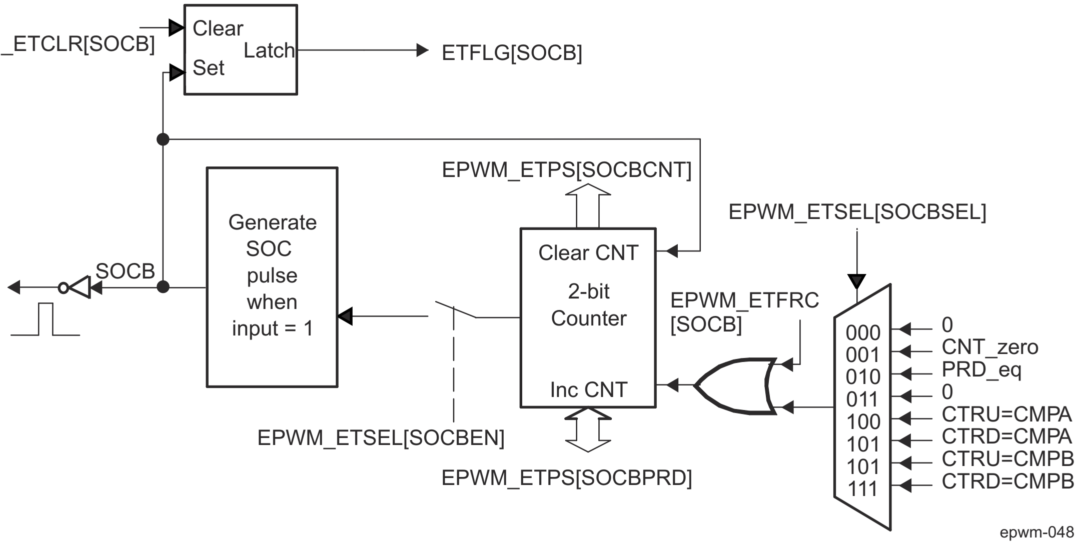

Figure 12-364. EPWM Event-Trigger SOCB Pulse Generator

12.5.3.4.9 EPWM Functional Register Groups

The Table 12-310 lists the groups of EPWM module registers according to their functionalities.

Table 12-322. EPWM Module Control and Status Registers Grouped by Submodule

Register Name	Offset	Size (×16)	Shadow	Register Description
Time-Base (TB) Submodule Registers				
EPWM_TBCTL	0h	1	No	Time-Base Control Register
EPWM_TBSTS	2h	1	No	Time-Base Status Register
EPWM_TBPHS	6h	1	No	Time-Base Phase Register
EPWM_TBCNT	8h	1	No	Time-Base Counter Register
EPWM_TBPRD	Ah	1	Yes	Time-Base Period Register
Counter-Compare (CC) Submodule Registers				
EPWM_CMPCTL	Eh	1	No	Counter-Compare Control Register
EPWM_CMPA	12h	1	Yes	Counter-Compare A Register
EPWM_CMPB	14h	1	Yes	Counter-Compare B Register
Action-Qualifier (AQ) Submodule Registers				
EPWM_AQCTLA	16h	1	No	Action-Qualifier Control Register for Output A (EPWMxA)
EPWM_AQCTLB	18h	1	No	Action-Qualifier Control Register for Output B (EPWMxB)
EPWM_AQSFRC	1Ah	1	No	Action-Qualifier Software Force Register
EPWM_AQCSFRC	1Ch	1	Yes	Action-Qualifier Continuous S/W Force Register Set
Dead-Band (DB) Generator Submodule Registers				
EPWM_DBCTL	1Eh	1	No	Dead-Band Generator Control Register
EPWM_DBRED	20h	1	No	Dead-Band Generator Rising Edge Delay Count Register
EPWM_DBFED	22h	1	No	Dead-Band Generator Falling Edge Delay Count Register
Trip-Zone (TZ) Submodule Registers				
EPWM_TZSEL	24h	1	No	Trip-Zone Select Register(1)
EPWM_TZCTL	28h	1	No	Trip-Zone Control Register (1)
EPWM_TZEINT	2Ah	1	No	Trip-Zone Enable Interrupt Register (1)

Table 12-322. EPWM Module Control and Status Registers Grouped by Submodule (continued)

Register Name	Offset	Size (×16)	Shadow	Register Description
EPWM_TZFLG	2Ch	1	No	Trip-Zone Flag Register (1)
EPWM_TZCLR	2Eh	1	No	Trip-Zone Clear Register (1)
EPWM_TZFRC	30h	1	No	Trip-Zone Force Register (1)
Event-Trigger (ET) Submodule Registers				
EPWM_ETSEL	32h	1	No	Event-Trigger Selection Register
EPWM_ETPS	34h	1	No	Event-Trigger Pre-Scale Register
EPWM_ETFLG	36h	1	No	Event-Trigger Flag Register
EPWM_ETCLR	38h	1	No	Event-Trigger Clear Register
EPWM_ETFRC	3Ah	1	No	Event-Trigger Force Register
PWM-Chopper Submodule Registers				
EPWM_PCCTL	3Ch	1	No	PWM-Chopper Control Register

(1) EALLOW protected registers.

12.5.3.4.10 Proper EPWM Interrupt Initialization Procedure

When the EPWM peripheral clock is enabled it is possible that interrupt flags may be set due to spurious events as the EPWM registers not being properly initialized. The proper procedure for initializing the EPWM peripheral is:

1. Disable global interrupts (CPU INTM flag)
2. Disable EPWM interrupts
3. Initialize peripheral registers
4. Clear any spurious EPWM flags
5. Enable EPWM interrupts
6. Enable global interrupts

12.5.4 Enhanced Quadrature Encoder Pulse (EQEP) Module

This section describes the Enhanced Quadrature Encoder Pulse (EQEP) module in the device.

12.5.4.1 EQEP Overview

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns, as shown in Figure 12-365. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

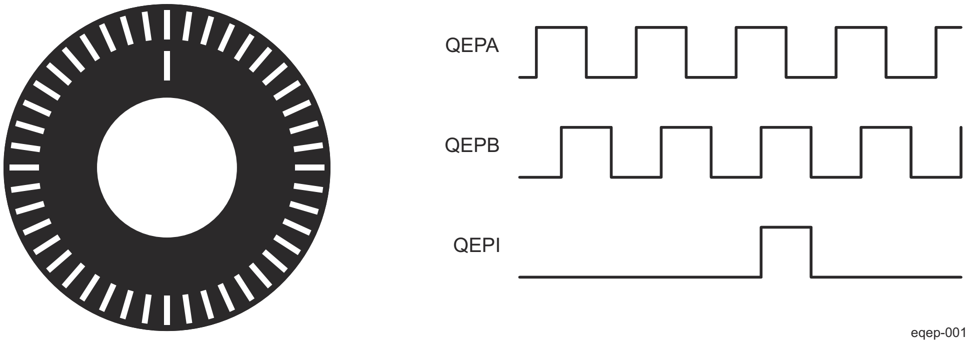

Figure 12-365. Optical Encoder Disk

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa as shown in Figure 12-366.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

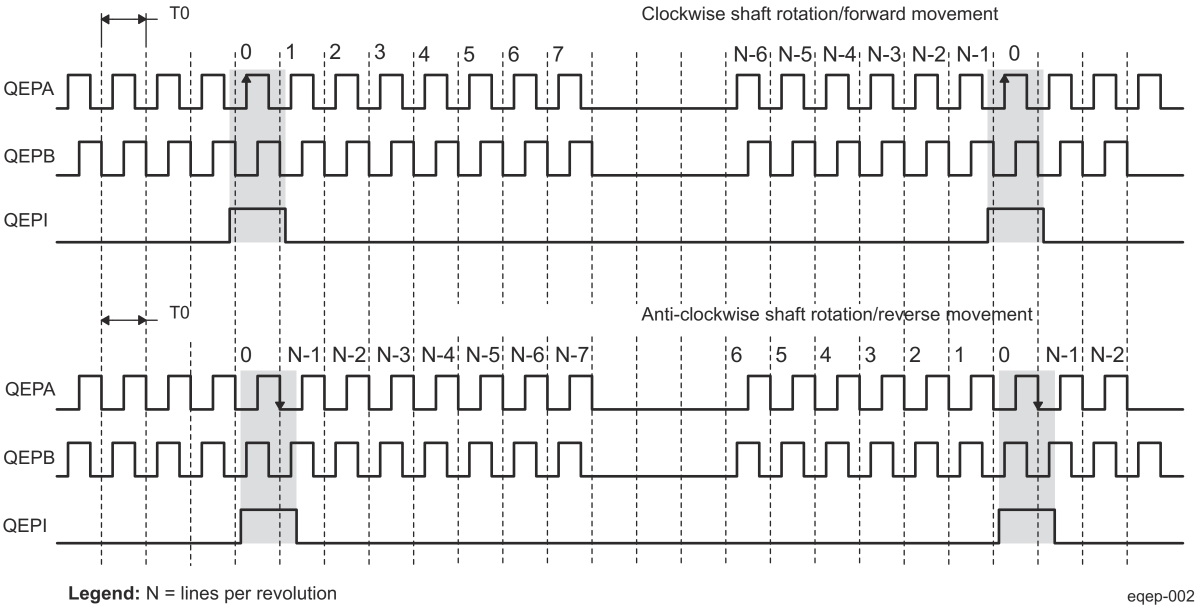

Figure 12-366. QEP Encoder Output Signal for Forward/Reverse Movement

Quadrature encoders from different manufacturers come with two forms of index pulse (gated index pulse or ungated index pulse) as shown in Figure 12-367. A nonstandard form of index pulse is ungated. In the ungated configuration, the index edges are not necessarily coincident with A and B signals. The gated index pulse is aligned to any of the four quadrature edges and width of the index pulse and can be equal to a quarter, half, or full period of the quadrature signal.

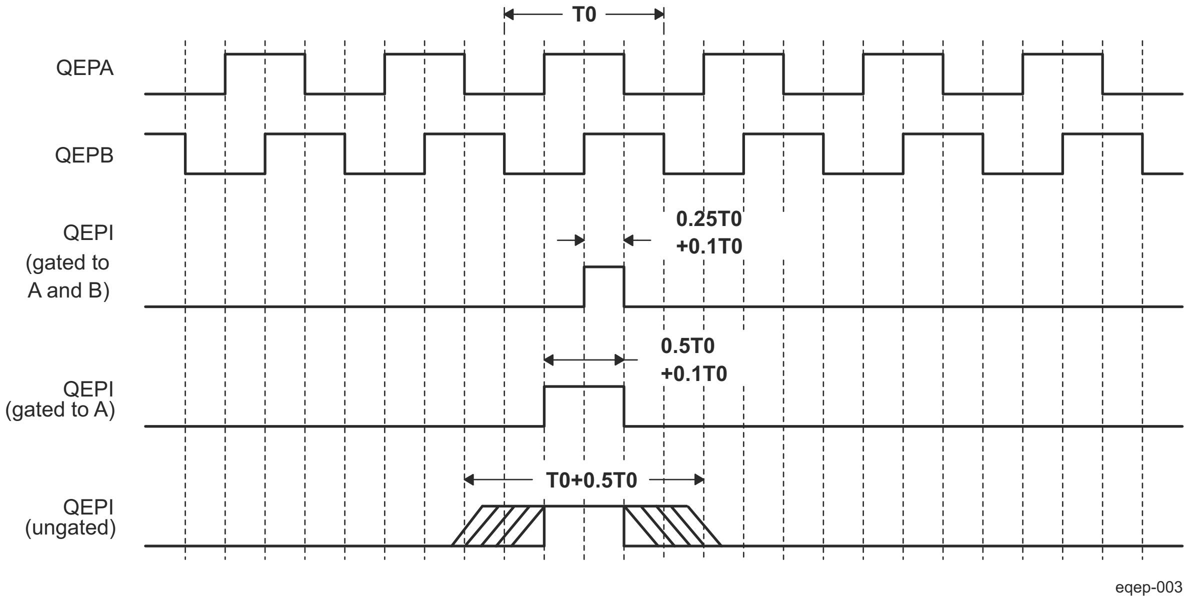

Figure 12-367. Index Pulse Example

Some typical applications for rotary encoders range from fax machines to motor controllers, and even robot localization. Rotary sensors are fundamental to the robotics and motion control systems found today. The optical shaft encoder can be used to improve a robot in various ways. The encoder can measure rotational distance traveled and speed, which can be used to monitor, for example, the angular position of a robot gripper arm or the speed of a robot.

General Issues: Estimating velocity from a digital position sensor is a cost-effective strategy in motor control. Two different first order approximations for velocity may be written as:

$$V(k) \approx \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad (2)$$

$$V(k) \approx \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (3)$$

where

v(k): Velocity at time instant k

x(k): Position at time instant k

x(k-1): Position at time instant k - 1

T: Fixed unit time or inverse of velocity calculation rate

ΔX: Incremental position movement in unit time

t(k): Time instant "k"

t(k-1): Time instant "k - 1"

X: Fixed unit position

ΔT: Incremental time elapsed for unit position movement.

Equation 2 is the conventional approach to velocity estimation and it requires a time base to provide unit time event for velocity calculation. Unit time is the inverse of the velocity calculation rate.

The encoder count (position) is read once during each unit time event. The quantity [x(k) - x(k-1)] is formed by subtracting the previous reading from the current reading. Then the velocity estimate is computed by multiplying by the known constant 1/T (where T is the constant time between unit time events and is known in advance).

Estimation based on Equation 2 has an inherent accuracy limit directly related to the resolution of the position sensor and the unit time period T. For example, consider a 500-line per revolution quadrature encoder with a velocity calculation rate of 400 Hz. When used for position the quadrature encoder gives a four-fold increase in resolution, in this case, 2000 counts per revolution. The minimum rotation that can be detected is therefore 0.0005 revolutions, which gives a velocity resolution of 12 rpm when sampled at 400 Hz. While this resolution may be satisfactory at moderate or high speeds, for example, 1% error at 1200 rpm, it would clearly prove inadequate at low speeds. In fact, at speeds below 12 rpm, the speed estimate would erroneously be zero much of the time.

At low speed, Equation 3 provides a more accurate approach. It requires a position sensor that outputs a fixed interval pulse train, such as the aforementioned quadrature encoder. The width of each pulse is defined by motor speed for a given sensor resolution. Equation 3 can be used to calculate motor speed by measuring the elapsed time between successive quadrature pulse edges. However, this method suffers from the opposite limitation of Equation 2. A combination of relatively large motor speeds and high sensor resolution makes the time interval ΔT small, and thus more greatly influenced by the timer resolution. This can introduce considerable error into high-speed estimates.

For systems with a large speed range (that is, speed estimation is needed at both low and high speeds), one approach is to use Equation 3 at low speed and have the software switch over to Equation 2 when the motor speed rises above some specified threshold.

Figure 12-368 shows the EQEP module overview.

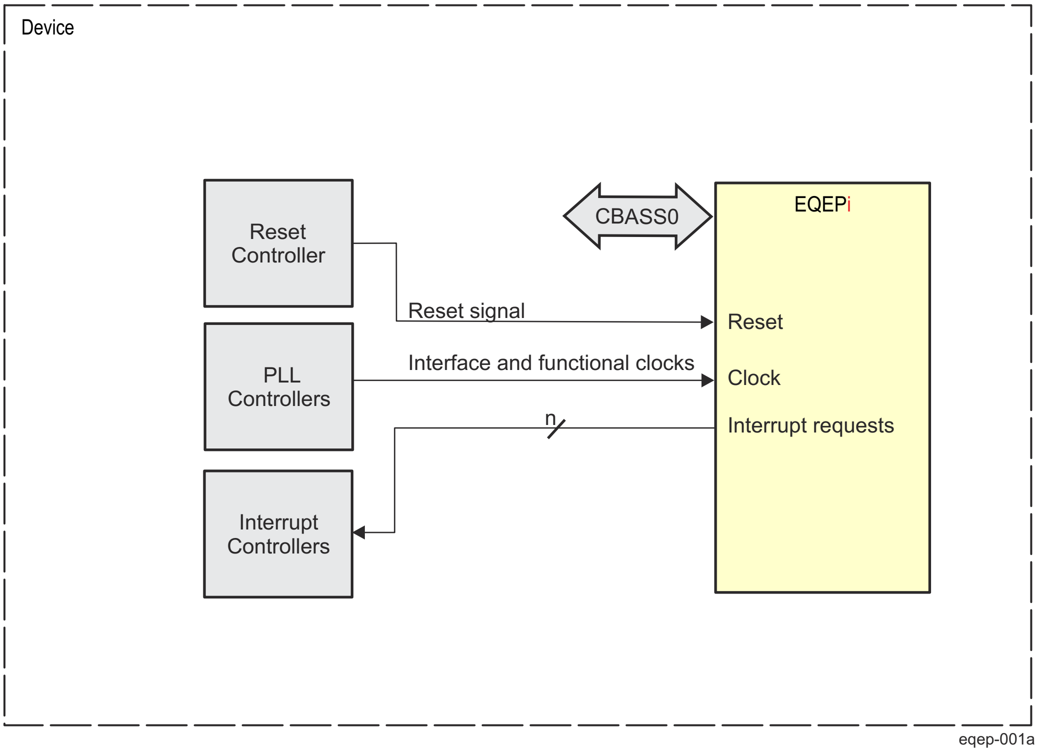

Note

i = 0 to number of instances - 1.

Figure 12-368. EQEP Overview

12.5.4.1.1 EQEP Features

The EQEP module includes the following features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low-speed measurement
- Unit time base for speed and frequency measurement
- Watchdog timer for detecting stalls
- EQEP inputs (A/B/INDEX and STROBE) are available at chip level
- EQEP phase error output is also available. The status of the phase error can be observed by software through the MAIN_CTRL_MMR_CFG0_EQEP_STAT register in the CTRL_MMR0 module.

- Counting modes:
  - Quadrature
  - Clockwise / Counter Clockwise
  - Count / Direction
- Start of Convert input for on-chip Strobe
- EQEP internal strobe (EQEP Strobe input is logically ORed with EQEP A and B inputs) may be used to:
  - Initialize the Position Counter with a non-zero value (for example, due to a limit switch input becoming active)
  - Snapshot the Position Counter into the EQEP_QPOSSLAT register
  - Gate the EQEP Index input preventing it from resetting the Position Counter

12.5.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.5.4.2 EQEP Environment

12.5.4.2.1 EQEP I/O Interface

The EQEPi (where i = 0 to 2) module is hereinafter referred to as EQEP module.

This section describes the EQEP external connections (environment).

Figure 12-369 shows the EQEP interface signals.

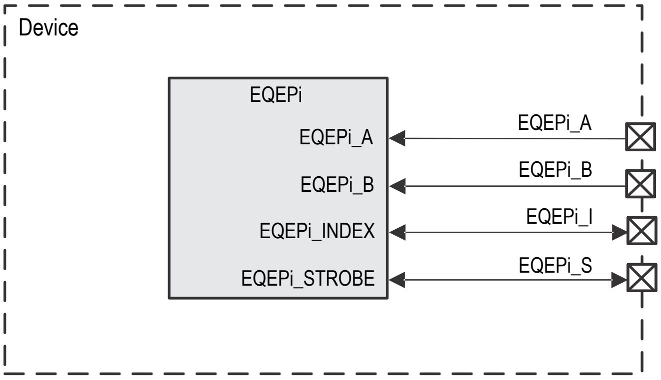

eqep-6a

Figure 12-369. EQEP External Interface I/Os

Table 12-311 describes the EQEP I/O signals.

Table 12-323. EQEP I/O Signals

Module Pin	Device Level Signal Name	I/O Type(1)	Description	Module Pin Reset Value(2)
		EQEPi(4)		
EQEPi(4)_A	EQEPi(4)_A	I	EQEPi(4) Quadrature input A	HiZ
EQEPi(4)_B	EQEPi(4)_B	I	EQEPi(4) Quadrature input B	HiZ
EQEPi(4)_INDEX	EQEPi(4)_I	I/O(3)	EQEPi(4) Index input/output	HiZ
EQEPi(4)_STROBE	EQEPi(4)_S	I/O(3)	EQEPi(4) Strobe input/output	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Output functionality is not supported. Only inputs are pinned out. For more information see *Device Specific EQEP Features*.

(4) i represents an EQEP instance. See the device datasheet for available domains and EQEP instances

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.5.4.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.4.4 EQEP Functional Description

This section provides the EQEP functional description and corresponding functional details about EQEPx inputs.

Note

Multiple identical EQEP modules can be contained in a system. For actual number of EQEP modules integrated in the device, refer to *EQEP Integration*. The letter x within a signal or module name is used to indicate a generic EQEP instance on a device. For example, output interrupt request, EQEP0_EQEP_INT_OUT_0 belongs to EQEP0, EQEP1_EQEP_INT_OUT_0 belongs to EQEP1, and so forth.

The EQEP peripheral contains the following major functional units (as shown in Figure 12-370):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Three stage/six stage digital noise filter
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG).

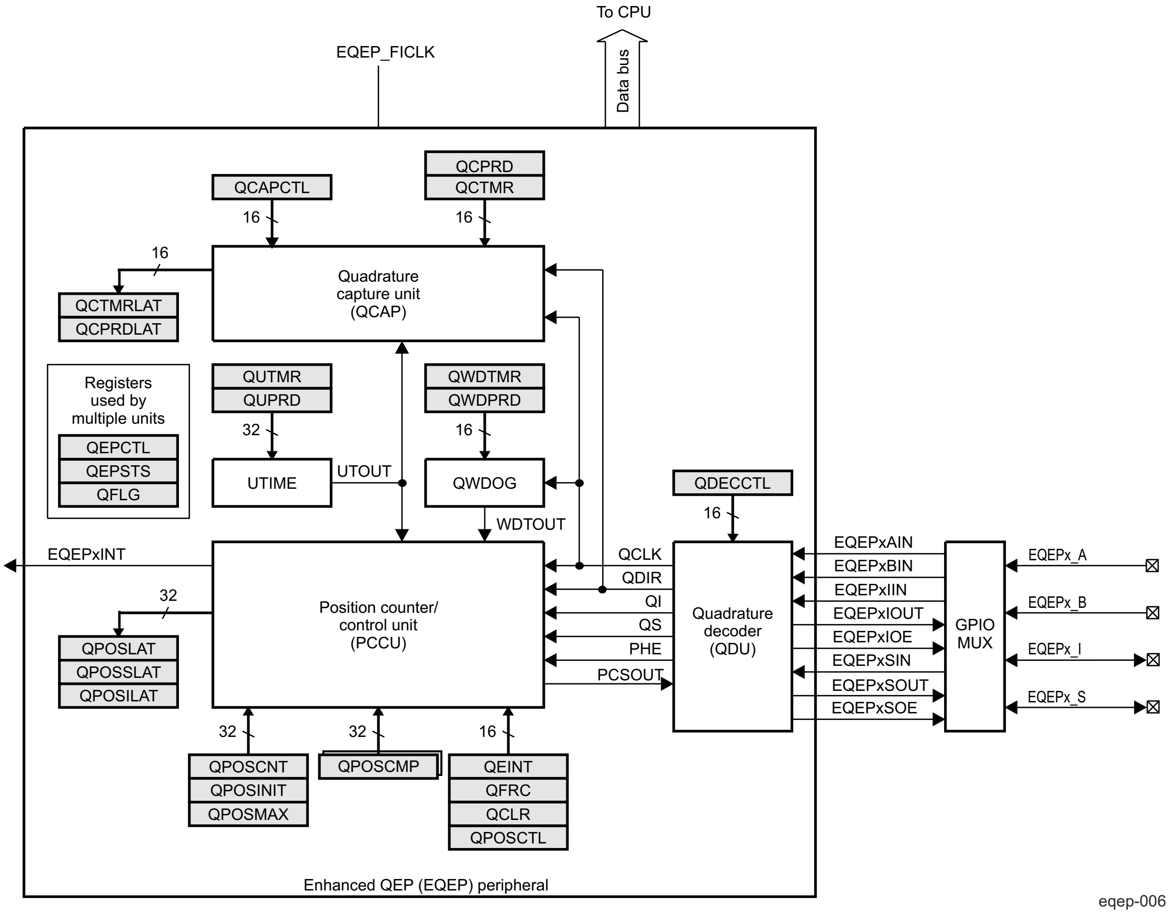

Figure 12-370. Functional Block Diagram of the EQEP Peripheral

12.5.4.4.1 EQEP Inputs

The EQEP inputs include two pins for quadrature-clock mode or direction-count mode, an index (or 0 marker), and a strobe input.

- EQEPx_A and EQEPx_B: These two pins can be used in quadrature-clock mode or direction-count mode.
  - Quadrature-clock mode: The EQEP encoders provide two square wave signals (A and B) 90 electrical degrees out of phase whose phase relationship is used to determine the direction of rotation of the input shaft and number of EQEP pulses from the index position to derive the relative position information. For forward or clockwise rotation, QEPA signal leads QEPB signal and vice versa. The quadrature decoder uses these two inputs to generate quadrature-clock and direction signals.
  - Direction-count mode: In direction-count mode, direction and clock signals are provided directly from the external source. Some position encoders have this type of output instead of quadrature output. The EQEPx_A pin provides the clock input and the EQEPx_B pin provides the direction input.
- EQEPx_I: Index or Zero Marker: The EQEP encoder uses an index signal to assign an absolute start position from which position information is incrementally encoded using quadrature pulses. This pin is connected to the index output of the EQEP encoder to optionally reset the position counter for each revolution. This signal can be used to initialize or latch the position counter on the occurrence of a desired event on the index pin.
- EQEPx_S: Strobe Input: This general-purpose strobe signal can initialize or latch the position counter on the occurrence of a desired event on the strobe pin. This signal is typically connected to a sensor or limit switch to notify that the motor has reached a defined position.

12.5.4.4.2 EQEP Quadrature Decoder Unit (QDU)

Figure 12-371 shows a functional block diagram of the QDU.

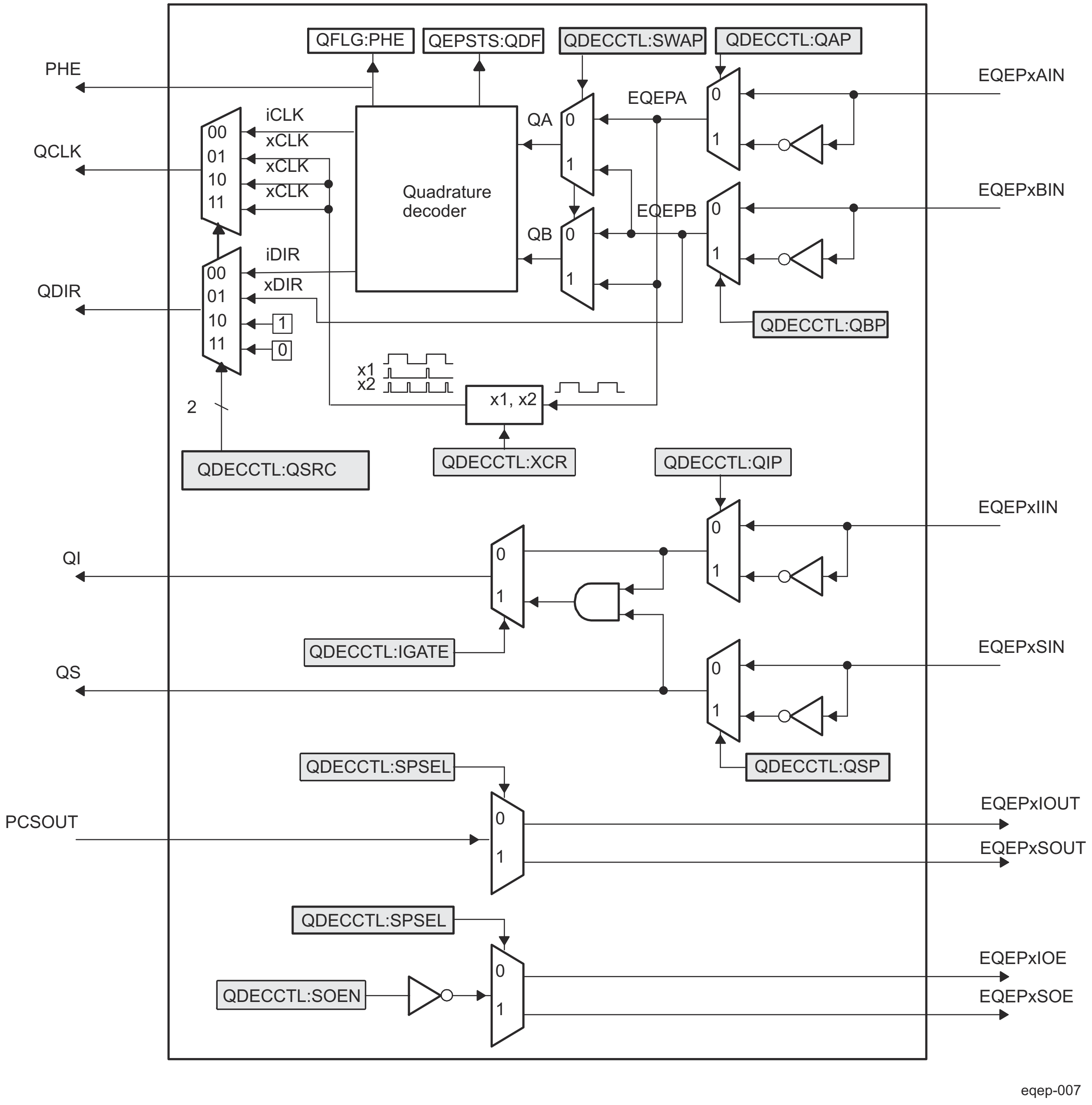

Figure 12-371. Functional Block Diagram of Decoder Unit

12.5.4.4.2.1 EQEP Position Counter Input Modes

Clock and direction input to position counter is selected using the QSRC bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL), based on interface input requirement as follows:

- Quadrature-count mode
- Direction-count mode
- UP-count mode
- DOWN-count mode.

12.5.4.4.2.1.1 Quadrature Count Mode

The quadrature decoder generates the direction and clock to the position counter in quadrature count mode.

Direction Decoding The direction decoding logic of the EQEP circuit determines which one of the sequences (EQEPA, EQEPB) is the leading sequence and accordingly updates the direction information in the QDF bit in the EQEP status register (EQEP_QEP_STS_CT). Table 12-312 and Figure 12-372 show the direction decoding logic in truth table and state machine form. Both edges of the EQEPA and EQEPB signals are sensed to generate count pulses for the position counter. Therefore, the frequency of the clock generated by the EQEP logic is four times that of each input sequence. Figure 12-373 shows the direction decoding and clock generation from the EQEP input signals.

Phase Error Flag In normal operating conditions, quadrature inputs EQEPA and EQEPB will be 90 degrees out of phase. The phase error flag (QPEI_FLG) is set in the EQEP_QINT_EN_FLG register when edge transition is detected simultaneously on the EQEPA and EQEPB signals to optionally generate interrupts. State transitions marked by dashed lines in Figure 12-372 are invalid transitions that generate a phase error.

Count Multiplication The EQEP position counter provides 4× times the resolution of an input clock by generating a quadrature-clock (QCLK) on the rising/falling edges of both EQEP input clocks (EQEPA and EQEPB) as shown in Figure 12-373.

Reverse Count In normal quadrature count operation, EQEPA input is fed to the QA input of the quadrature decoder and the EQEPB input is fed to the QB input of the quadrature decoder. Reverse counting is enabled by setting the SWAP bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL). This will swap the input to the quadrature decoder thereby reversing the counting direction.

Table 12-324. Quadrature Decoder Truth Table

Previous Edge	Present Edge	QDIR	QPOSCNT
QA↑	QB↑	UP	Increment (+1)
	QB↓	DOWN	Decrement (-1)
	QA↓	TOGGLE	Increment (+1) or Decrement (-1)
QA↓	QB↓	UP	Increment (+1)
	QB↑	DOWN	Decrement(-1)
	QA↑	TOGGLE	Increment (+1) or Decrement (-1)
QB↑	QA↑	DOWN	Increment (+1)
	QA↓	UP	Decrement (-1)
	QB↓	TOGGLE	Increment (+1) or Decrement (-1)
QB↓	QA↓	DOWN	Increment (+1)
	QA↑	UP	Decrement (-1)
	QB↑	TOGGLE	Increment (+1) or Decrement (-1)

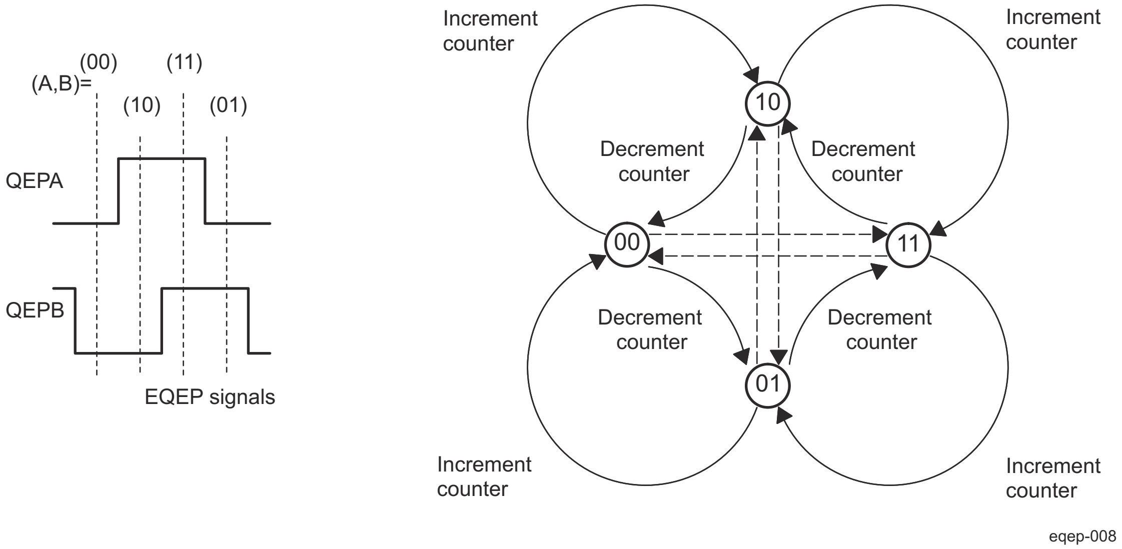

Figure 12-372. Quadrature Decoder State Machine

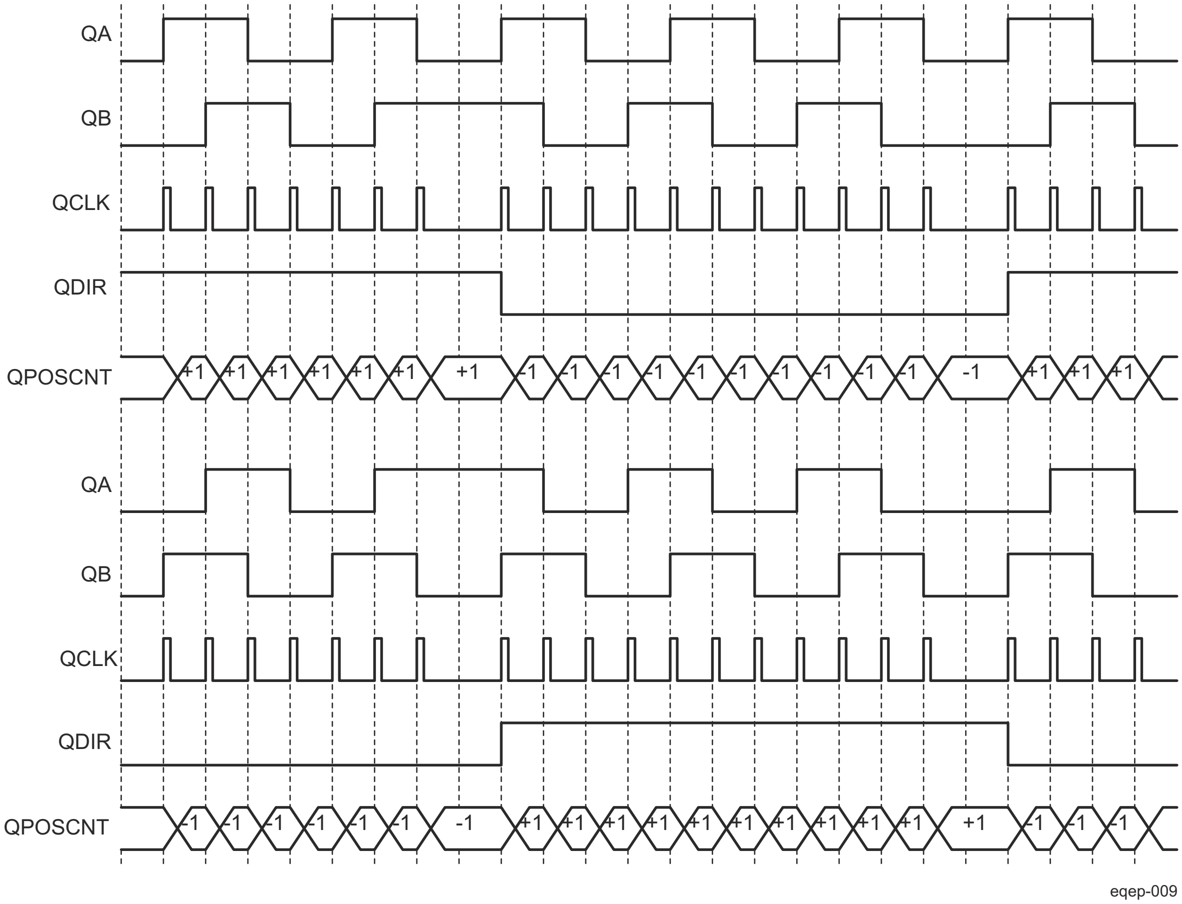

Figure 12-373. Quadrature-clock and Direction Decoding

12.5.4.4.2.1.2 EQEP Direction-count Mode

Some position encoders provide direction and clock outputs, instead of quadrature outputs. In such cases, direction-count mode can be used. EQEPA input will provide the clock for position counter and the EQEPB input will have the direction information. The position counter is incremented on every rising edge of a EQEPA input when the direction input is high and decremented when the direction input is low.

12.5.4.4.2.1.3 EQEP Up-Count Mode

The counter direction signal is hard-wired for up count and the position counter is used to measure the frequency of the EQEPA input. Setting of the XCR bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables clock generation to the position counter on both edges of the QEPA input, thereby increasing the measurement resolution by 2× factor.

12.5.4.4.2.1.4 EQEP Down-Count Mode

The counter direction signal is hardwired for a down count and the position counter is used to measure the frequency of the EQEPA input. Setting of the XCR bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables clock generation to the position counter on both edges of a EQEPA input, thereby increasing the measurement resolution by 2× factor.

12.5.4.4.2.2 EQEP Input Polarity Selection

Each EQEP input can be inverted using the in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL[8-5]) control bits. As an example, setting of the QIP bit in EQEP_QDEC_QEP_CTL inverts the index input.

12.5.4.4.2.3 EQEP Position-Compare Sync Output

The EQEP peripheral includes a position-compare unit that is used to generate the position-compare sync signal on compare match between the position counter register (EQEP_QPOSCNT) and the position-compare register (EQEP_QPOSCMP). This sync signal can be output using an index pin or strobe pin of the EQEP peripheral.

Setting the SOEN bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables the position-compare sync output and the SPSEL bit in EQEP_QDEC_QEP_CTL selects either an EQEP index pin or an EQEP strobe pin.

12.5.4.4.3 EQEP Position Counter and Control Unit (PCCU)

The position counter and control unit provides two configuration registers (EQEP_QDEC_QEP_CTL and EQEP_QCAP_QPOS_CTL) for setting up position counter operational modes, position counter initialization/latch modes and position-compare logic for sync signal generation.

12.5.4.4.3.1 EQEP Position Counter Operating Modes

Position counter data may be captured in different manners. In some systems, the position counter is accumulated continuously for multiple revolutions and the position counter value provides the position information with respect to the known reference. An example of this is the quadrature encoder mounted on the motor controlling the print head in the printer. Here the position counter is reset by moving the print head to the home position and then position counter provides absolute position information with respect to home position.

In other systems, the position counter is reset on every revolution using index pulse and position counter provides rotor angle with respect to index pulse position.

Position counter can be configured to operate in following four modes

- Position Counter Reset on Index Event
- Position Counter Reset on Maximum Position
- Position Counter Reset on the first Index Event
- Position Counter Reset on Unit Time Out Event (Frequency Measurement).

In all the above operating modes, position counter is reset to 0 on overflow and to QPOSMAX bifield value in EQEP_QPOSMAX register on underflow. Overflow occurs when the position counter counts up after QPOSMAX value. Underflow occurs when position counter counts down after "0". Interrupt flag is set to indicate overflow/underflow in EQEP_QINT_EN_FLG register.

12.5.4.4.3.1.1 EQEP Position Counter Reset on Index Event (EQEP_QDEC_QEP_CTL[29-28] PCRM] = 0b00)

If the index event occurs during the forward movement, then position counter is reset to 0 on the next EQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the EQEP_QPOSMAX register on the next EQEP clock.

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in EQEP_QEP_STS_CT registers, it also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for index event reset operation.

For example, if the first reset operation occurs on the falling edge of EQEPB during the forward direction, then all the subsequent reset must be aligned with the falling edge of EQEPB for the forward rotation and on the rising edge of EQEPB for the reverse rotation as shown in Figure 12-374.

The position-counter value is latched to the EQEP_QPOSILAT register and direction information is recorded in the EQEP_QEP_STS_CT[4] QDLF bit on every index event marker. The position-counter error flag (EQEP_QEP_STS_CT[0] PCEF) and error interrupt flag (EQEP_QINT_EN_FLG[17] PCEI_FLG) are set if the latched value is not equal to 0 or QPOSMAX. The position-counter error flag (EQEP_QEP_STS_CT[0] PCEF) is updated on every index event marker and an interrupt flag (EQEP_QINT_EN_FLG[17] PCEI_FLG) will be set on error that can be cleared only through software.

The index event latch configuration EQEP_QDEC_QEP_CTL[21-20] IEL bits are ignored in this mode and position counter error flag/interrupt flag are generated only in index event reset mode.

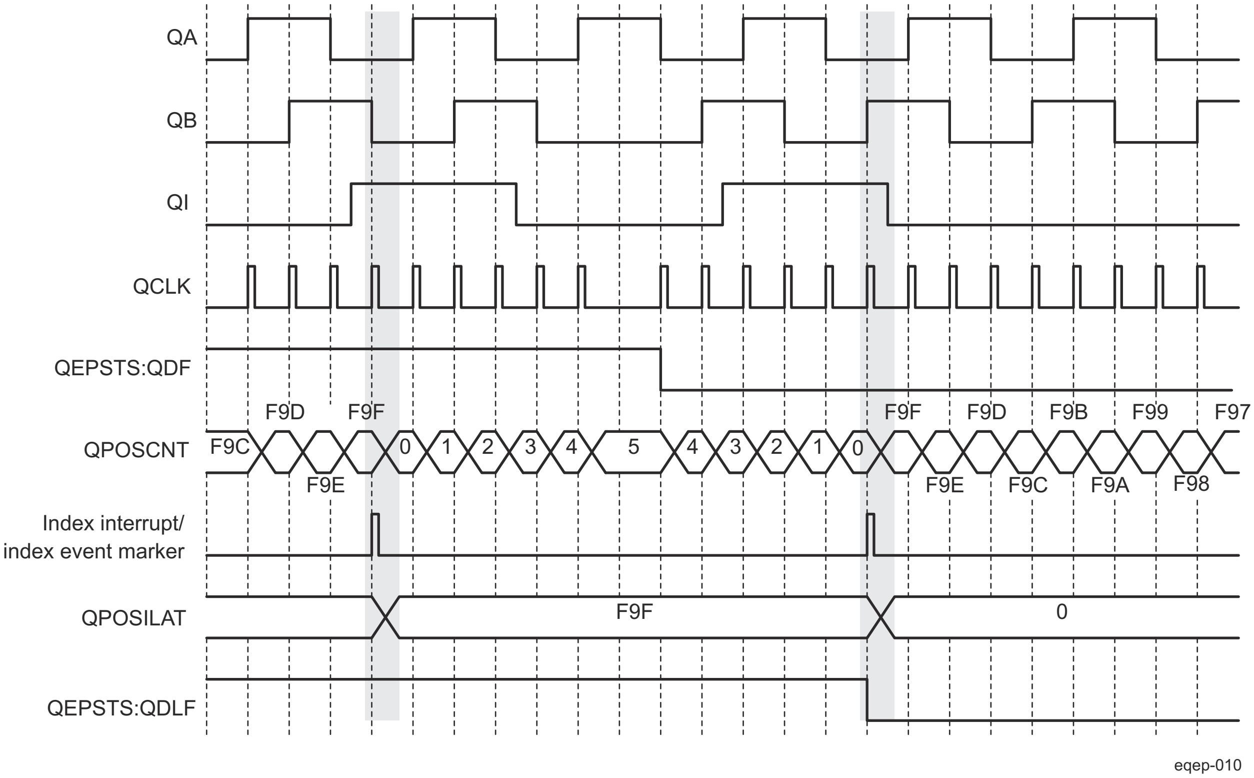

Figure 12-374. Position Counter Reset by Index Pulse for 1000 Line Encoder (QPOSMAX = 3999 or F9Fh)

12.5.4.4.3.1.2 EQEP Position Counter Reset on Maximum Position (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b01)

If the position counter is equal to QPOSMAX (in EQEP_QPOSMAX register), then the position counter is reset to 0 on the next EQEP clock for forward movement and position counter overflow flag is set. If the position counter is equal to 0, then the position counter is reset to QPOSMAX on the next QEP clock for reverse movement and position counter underflow flag is set. Figure 12-375 shows the position counter reset operation in this mode.

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF); it also remembers the quadrature edge on the first index marker so that the same relative quadrature transition is used for the software index marker (EQEP_QDEC_QEP_CTL[21-20] IEL= 0b11).

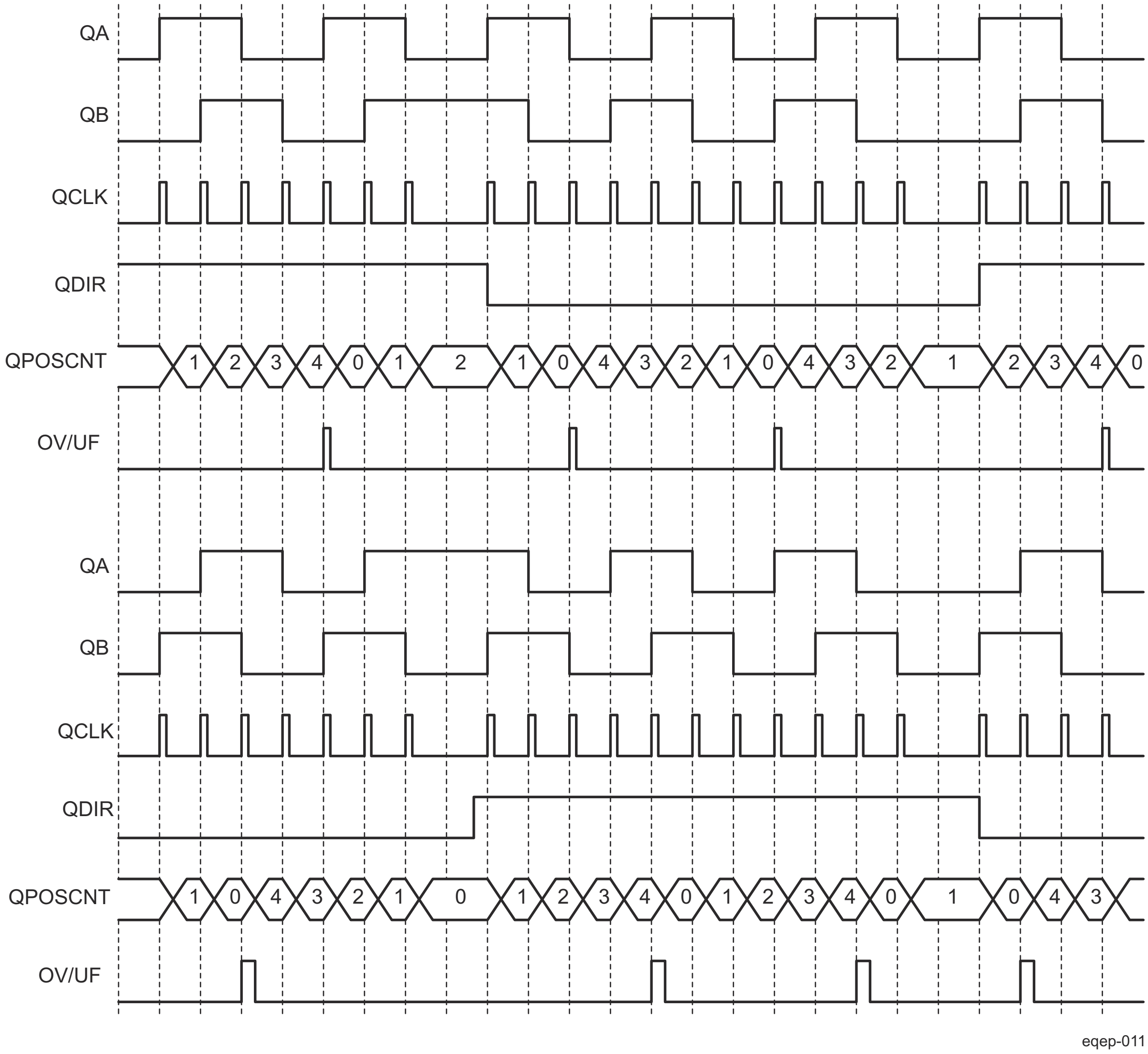

Figure 12-375. Position Counter Underflow/Overflow (QPOSMAX = 4)

12.5.4.4.3.1.3 Position Counter Reset on the First Index Event (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b10)

If the index event occurs during forward movement, then the position counter is reset to 0 on the next EQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the EQEP_QPOSMAX register on the next EQEP clock. Note that this is done only on the first occurrence and subsequently the position counter value is not reset on an index event; rather, it is reset based on maximum position as described in Section 12.5.4.4.3.1.2 .

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in EQEP_QEP_STS_CT registers. It also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for software index marker (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11).

12.5.4.4.3.1.4 Position Counter Reset on Unit Time out Event (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b11)

In this mode, the QPOSCNT value is latched to the EQEP_QPOSLAT register and then the QPOSCNT field is reset (to 0 or the QPOSMAX value in the EQEP_QPOSMAX register, depending on the direction mode selected by EQEP_QDEC_QEP_CTL[15-14] QSRC bits on a unit time event). This is useful for frequency measurement.

12.5.4.4.3.2 EQEP Position Counter Latch

The EQEP index and strobe input can be configured to latch the position counter QPOSCNT (EQEP_QPOSCNT) into QPOSILAT (EQEP_QPOSILAT register) and QPOSSLAT (EQEP_QPOSSLAT register) bitfields, respectively, on occurrence of a definite event on these pins.

12.5.4.4.3.2.1 Index Event Latch

In some applications, it may not be desirable to reset the position counter on every index event and instead it may be required to operate the position counter in full 32-bit mode (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b01 and EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b10 modes).

In such cases, the EQEP position counter can be configured to latch on the following events and direction information is recorded in the EQEP_QEP_STS_CT[4] QDLF bit on every index event marker.

- Latch on Rising edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)
- Latch on Falling edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b10)
- Latch on Index Event Marker (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11)

This is particularly useful as an error checking mechanism to check if the position counter accumulated the correct number of counts between index events. As an example, the 1000-line encoder must count 4000 times when moving in the same direction between the index events.

The index event latch interrupt flag (EQEP_QINT_EN_FLG[26] IELI_FLG) is set when the position counter is latched to the EQEP_QPOSILAT register. The index event latch configuration bits are ignored when EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b00.

When Position counter reset on an index event mode is selected through EQEP_QDEC_QEP_CTL[29-28] PCRM bit field (value: 0h), EQEP_QDEC_QEP_CTL[21-20] IEL bit field must be configured to 0h and position counter value is latched into the EQEP_QPOSILAT[31-0] QPOSILAT register for every index marker.

Latch on Rising Edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)	The position counter value (QPOSCNT) is latched to the EQEP_QPOSILAT register on every rising edge of an index input.
Latch on Falling Edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b10)	The position counter value (QPOSCNT) is latched to the EQEP_QPOSILAT register on every falling edge of index input.
Latch on Index Event Marker/Software Index Marker (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11)	The first index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and

direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in the EQEP_QEP_STS_CT registers. It also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for latching the position counter (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11).

Figure 12-376 shows the position counter latch using an index event marker.

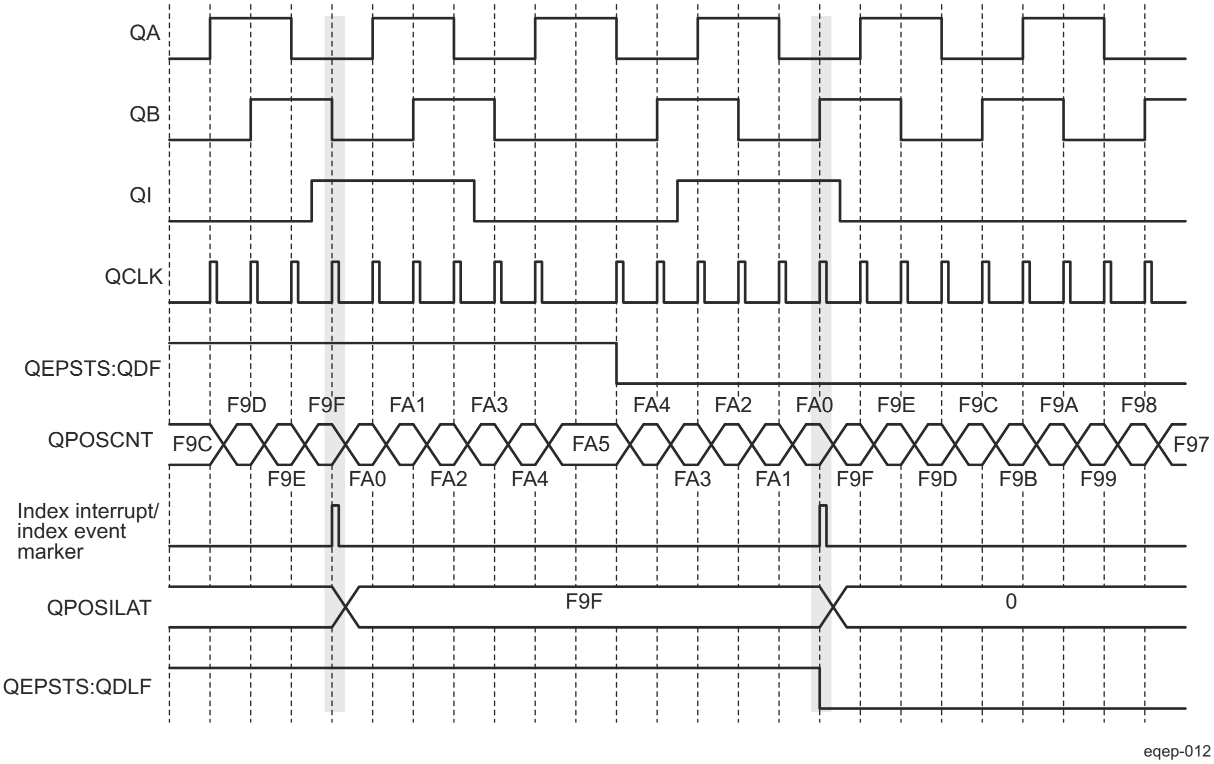

Figure 12-376. Software Index Marker for 1000-line Encoder (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)

12.5.4.4.3.2.2 EQEP Strobe Event Latch

The position-counter value is latched to the EQEP_QPOSSLAT register on the rising edge of the strobe input (QCLK) by clearing the EQEP_QDEC_QEP_CTL[22] SEL bit. Latching on the falling edge of the strobe input (QCLK) can be done by inverting the strobe input using the EQEP_QDEC_QEP_CTL[5] QSP bit.

If the EQEP_QDEC_QEP_CTL[22] SEL bit is set, then the position counter value is latched to the EQEP_QPOSSLAT register on the rising edge of the strobe input for forward direction and on the falling edge of the strobe input for reverse direction as shown in Figure 12-377.

The strobe event latch interrupt flag (EQEP_QINT_EN_FLG[25] SELI_FLG) is set when the position counter is latched to the EQEP_QPOSSLAT register.

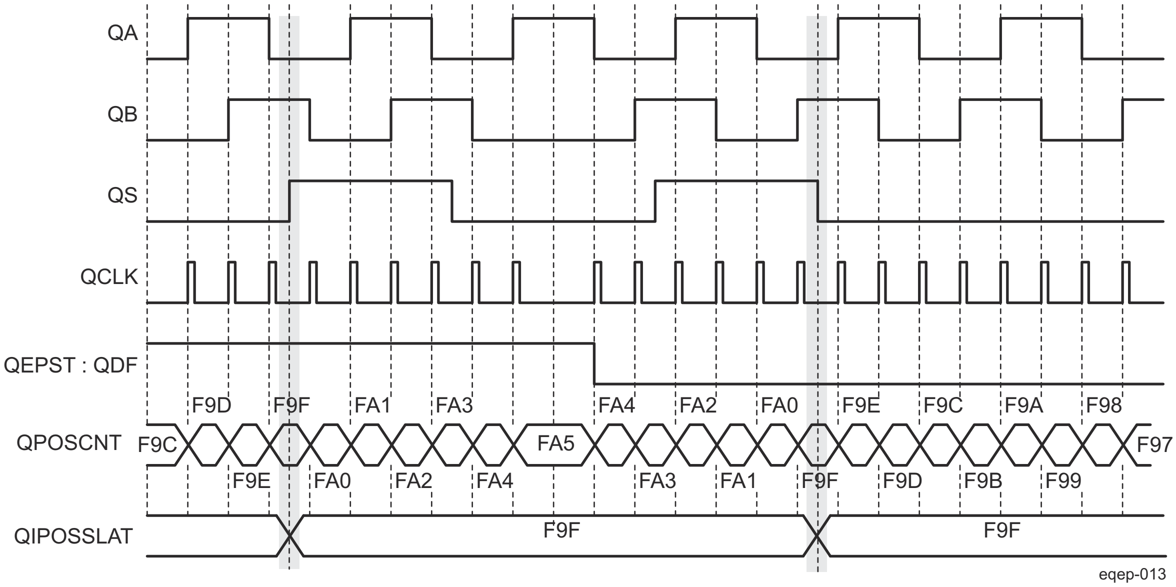

Figure 12-377. EQEP Strobe Event Latch (EQEP_QDEC_QEP_CTL[22] SEL = 0b1)

12.5.4.4.3.3 EQEP Position Counter Initialization

The position counter can be initialized using following events:

- Index event
- Strobe event
- Software initialization

Note

When all of the above events occur simultaneously, the sequence of priority is as follows: 1) Software Initialization, 2) strobe event initialization, 3) Index Event Initialization.

Index Event Initialization (IEI)

The EQEPx_I index input can be used to trigger the initialization of the position counter at the rising or falling edge of the index input.

If the EQEP_QDEC_QEP_CTL[25-24] IEI bits are 2h, then the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.

The index event initialization interrupt flag (EQEP_QDEC_QEP_CTL[25-24] IEI) is set when the position counter is initialized with a value in the EQEP_QPOSINIT register.

If EQEP_QDEC_QEP_CTL[25-24] IEI bit field is configured with value 0h (default) or 1h, the index event initialization of position counter is disabled.

If EQEP_QDEC_QEP_CTL[25-24] IEI bit field is configured with value 3h, then the the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the falling edge of strobe input signal.

Strobe Event Initialization (SEI)

If the EQEP_QDEC_QEP_CTL[27-26] SEI bits are 2h, then the position counter is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input.

If the EQEP_QDEC_QEP_CTL[27-26] SEI bits are 3h, then the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.

The strobe event initialization interrupt flag (EQEP_QDEC_QEP_CTL[27-26] SEI) is set when the position counter is initialized with a value in the EQEP_QPOSINIT register.

If EQEP_QDEC_QEP_CTL[27-26] SEI bit field is configured with value 0h (default) or 1h, the strobe event initialization of position counter is disabled.

Software Initialization (SWI)

The position counter can be initialized in software by writing a 1h to the EQEP_QDEC_QEP_CTL[23] SWI bit, which will automatically be cleared after initialization.

12.5.4.4.3.4 EQEP Position-Compare Unit

The EQEP peripheral includes a position-compare unit that is used to generate a sync output and/or interrupt on a position-compare match. Figure 12-378 shows a diagram. The position-compare (EQEP_QPOSCMP) register is shadowed and shadow mode can be enabled or disabled using the EQEP_QCAP_QPOS_CTL[31] PCSHDW bit. If the shadow mode is not enabled, the CPU writes directly to the active position compare register.

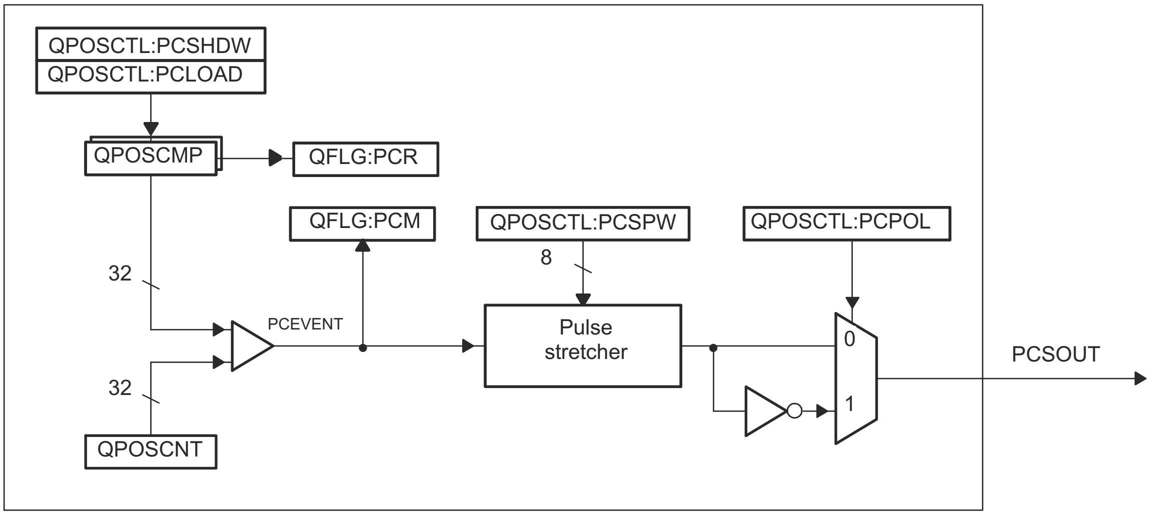

Figure 12-378. EQEP Position-compare Unit

In shadow mode, SW can configure the position-compare unit (EQEP_QCAP_QPOS_CTL[30] PCLOAD) to load the shadow register value into the active register on the following events and to generate the position-compare ready (EQEP_QINT_EN_FLG[23] PCRI_FLG) interrupt after loading.

- Load on compare match
- Load on position-counter zero event.

The position-compare match (EQEP_QINT_EN_FLG[24] PCMI_FLG) is set when the position-counter value (QPOSCNT) matches with the active position-compare register (EQEP_QPOSCMP) and the position-compare sync output of the programmable pulse width is generated on compare match to trigger an external device.

For example, if EQEP_QPOSCMP bitfield POSCMP = 0x2, the position-compare unit generates a position-compare event on the transition from 1 to 2 of the EQEP position counter for forward counting direction and on the transition from 3 to 2 of the EQEP position counter for reverse counting direction (see Figure 12-379).

Note

When EQEP_QCAP_QPOS_CTL[30] PCLOAD = 0h, the shadow register is loaded into the active register as soon as POSCNT becomes zero, and it should not generate another shadow load if the POSCNT continues to stay at zero

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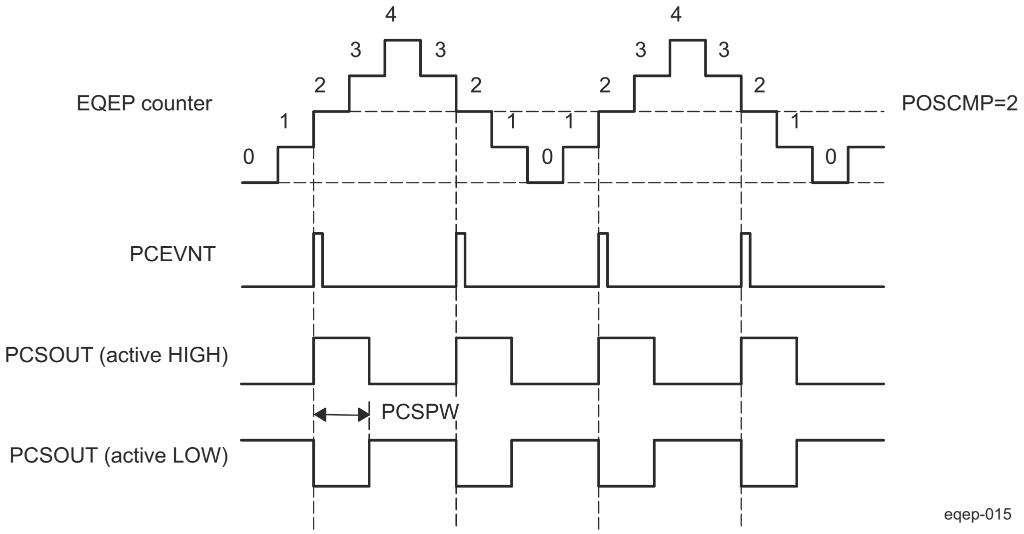

Figure 12-379. EQEP Position-compare Event Generation Points

The pulse stretcher logic in the position-compare unit generates a programmable position-compare sync pulse output on the position-compare match. In the event of a new position-compare match while a previous position-compare pulse is still active, then the pulse stretcher generates a pulse of specified duration from the new position-compare event as shown in Figure 12-380.

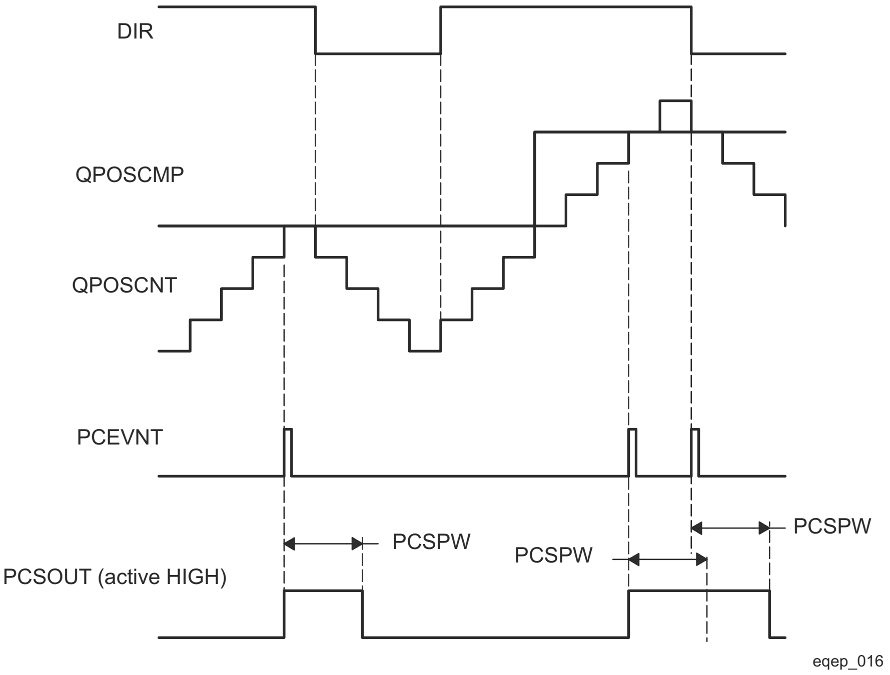

Figure 12-380. EQEP Position-compare Sync Output Pulse Stretcher

12.5.4.4.4 EQEP Edge Capture Unit

The EQEP peripheral includes an integrated edge capture unit to measure the elapsed time between the unit position events as shown in Figure 12-381. This feature is typically used for low speed measurement using the following equation:

$$V(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \tag{4}$$

where,

- X - Unit position is defined by integer multiple of quadrature edges (see Figure 12-382)
- ΔT - Elapsed time between unit position events
- v(k) - Velocity at time instant "k"

The EQEP capture timer (QCTMR bitfield in EQEP_QCTMR register) runs from prescaled SYSCLKOUT and the prescaler is programmed by the EQEP_QCAP_QPOS_CTL[6-4] CCPS bits. The capture timer QCTMR value is latched into the capture period register (EQEP_QC_PRD_TLAT) on every unit position event and then the capture timer is reset.

Time measurement (ΔT) between unit position events will be correct if the following conditions are met:

- No more than 65,535 counts have occurred between unit position events.
- No direction change between unit position events.

The capture unit sets the EQEP overflow error flag (EQEP_QEP_STS_CT[3] COEF) in the event of capture timer overflow between unit position events. If a direction change occurs between the unit position events, then an error flag is set in the status register (EQEP_QEP_STS_CT[2] CDEF).

Capture Timer (EQEP_QCTMR register) and Capture period register (EQEP_QC_PRD_TLAT) can be configured to latch on following events.

- CPU read of EQEP_QPOSCNT register
- Unit time-out event

If the EQEP_QDEC_QEP_CTL[18] QCLM bit is cleared, then the capture timer and capture period values are latched into the EQEP_QC_PRD_TLAT and EQEP_QCPRDLAT registers, respectively, when the CPU reads the position counter in EQEP_QPOSCNT.

Note

Capture timer and capture period values are not latched for an emulation read.

If the EQEP_QDEC_QEP_CTL[18] QCLM bit is set, then the position counter, capture timer, and capture period values are latched into the EQEP_QPOSLAT, EQEP_QC_PRD_TLAT and EQEP_QCPRDLAT registers, respectively, on unit time out.

Figure 12-383 shows the capture unit operation along with the position counter.

Note

The EQEP_QCAP_QPOS_CTL register should not be modified dynamically (such as switching CAPCLK prescaling mode from SYSCLKOUT/4 to SYSCLKOUT/8, where SYSCLKOUT is equivalent to EQEPx_FICLK). The capture unit must be disabled before changing the prescaler.

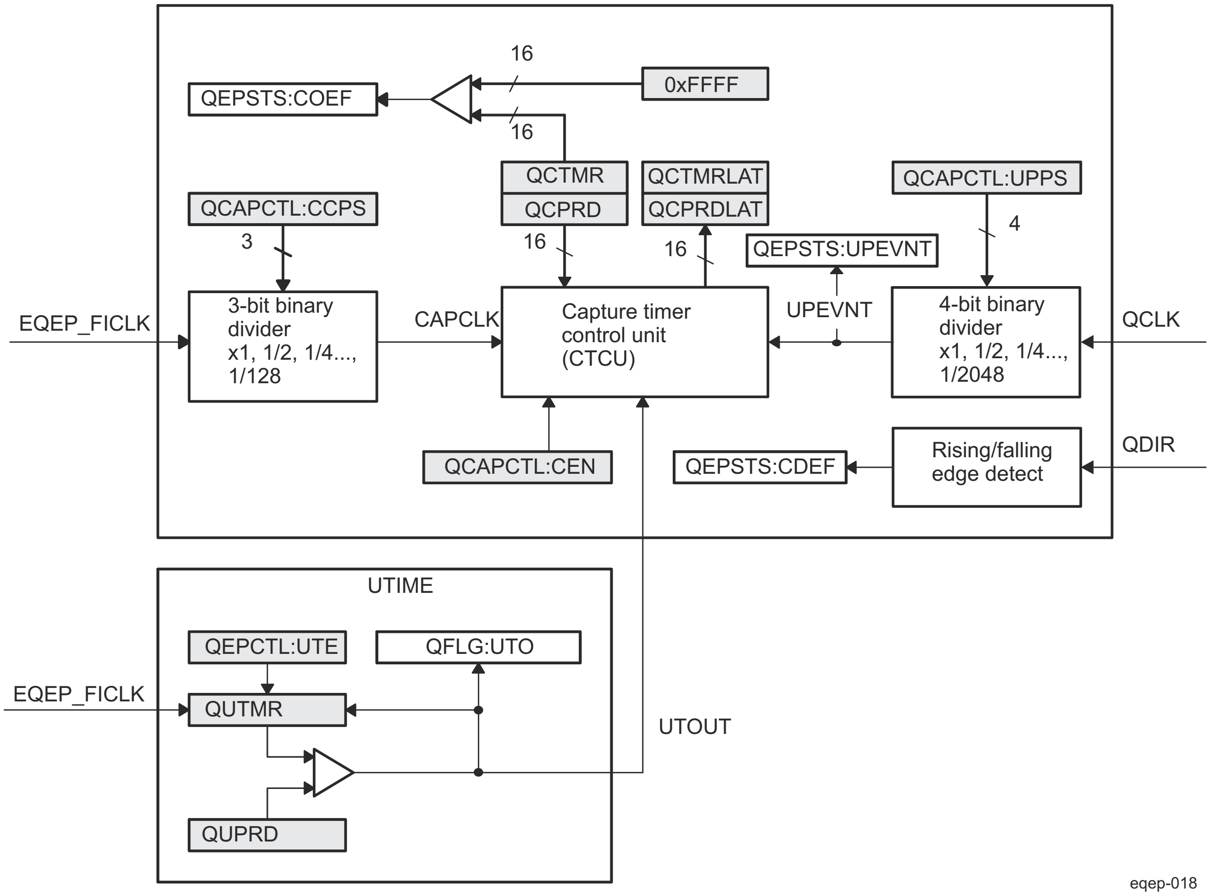

Figure 12-381. EQEP Edge Capture Unit

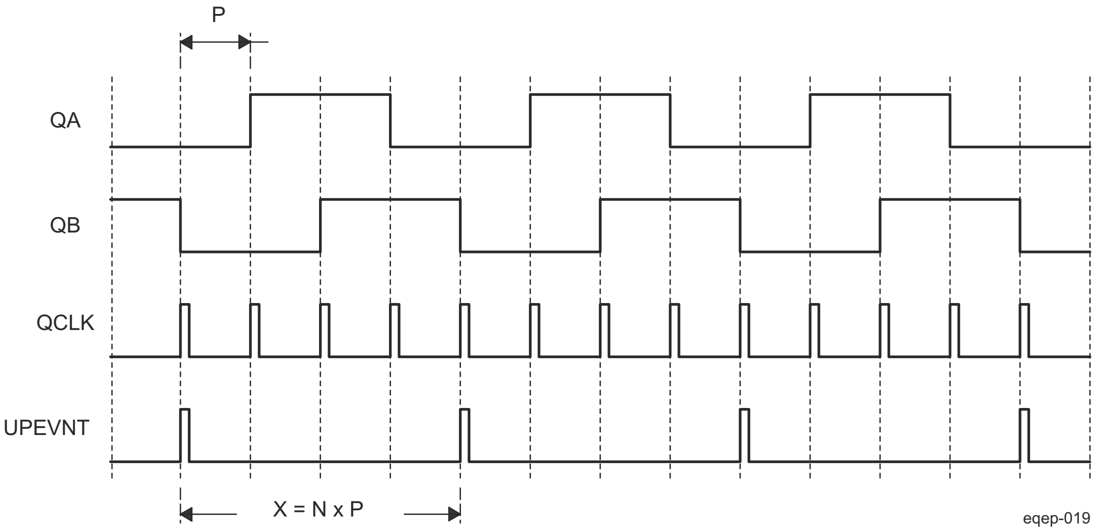

Note

N - Number of quadrature periods selected using EQEP_QCAP_QPOS_CTL[3-0] UPPS bits

Figure 12-382. Unit Position Event for Low Speed Measurement (EQEP_QCAP_QPOS_CTL[UPPS] = 0010)

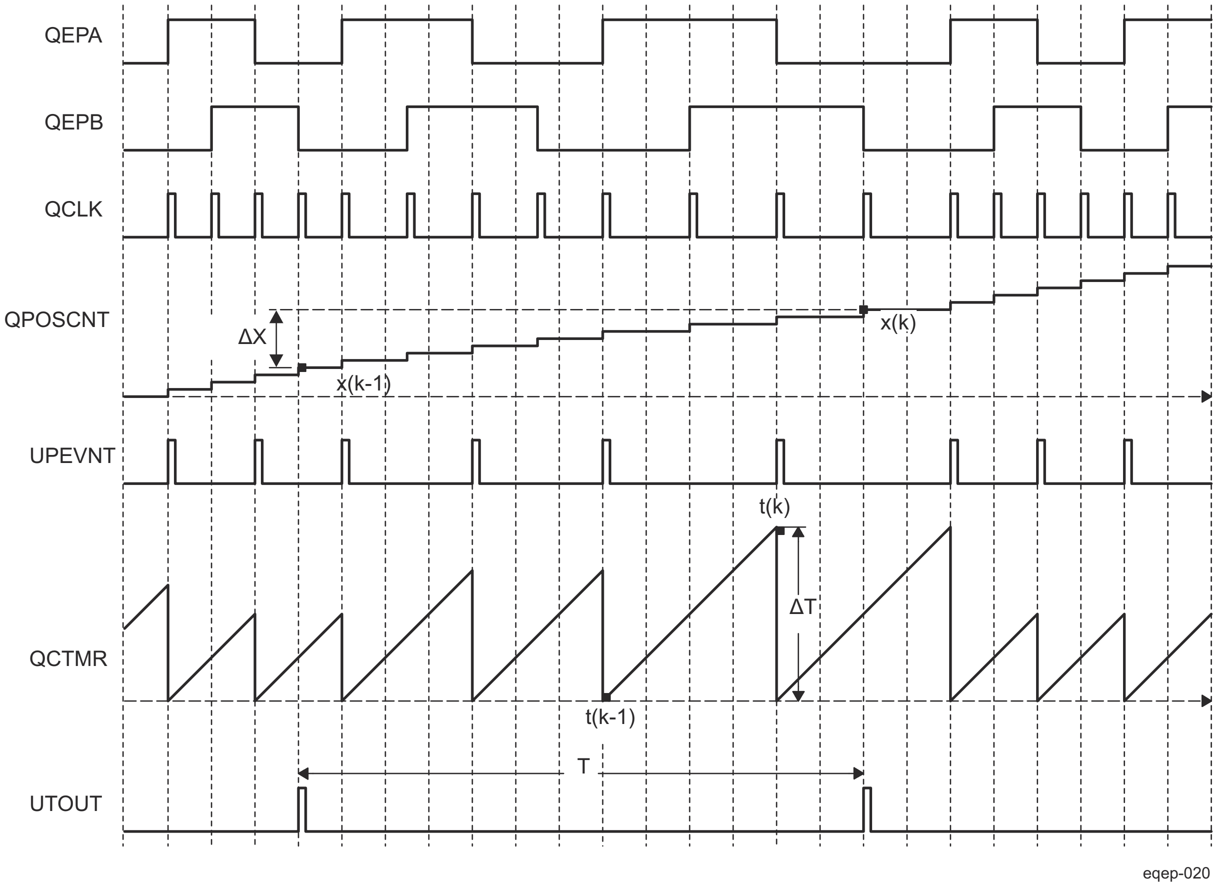

Figure 12-383. EQEP Edge Capture Unit - Timing Details

Velocity Calculation Equations:

$$V(k) = \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \tag{5}$$

OR

$$V(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \tag{6}$$

where

v(k): Velocity at time instant k

x(k): Position at time instant k

x(k-1): Position at time instant k - 1

T: Fixed unit time or inverse of velocity calculation rate

ΔX: Incremental position movement in unit time

X: Fixed unit position

ΔT: Incremental time elapsed for unit position movement

t(k): Time instant "k"

t(k-1): Time instant "k - 1"

Unit time (T) and unit period (X) are configured using the EQEP_QUPRD and EQEP_QCAP_QPOS_CTL[3-0] UPPS registers. Incremental position output and incremental time output is available in the EQEP_QPOSLAT and EQEP_QCPRDLAT registers.

Parameter	Relevant Register to Configure or Read the Information
T	Unit Period Register (EQEP_QUPRD)
ΔX	Incremental Position = QPOSLAT(k) - QPOSLAT(k - 1)
X	Fixed unit position defined by sensor resolution and QCAPCTL[3-0] UPPS bits
ΔT	Capture Period Latch (EQEP_QCPRDLAT)

12.5.4.4.5 EQEP Watchdog

The EQEP peripheral contains a 16-bit watchdog timer that monitors the quadrature-clock to indicate proper operation of the motion-control system. The EQEP watchdog timer is clocked from SYSCLKOUT/64 and the quadrate clock event (pulse) resets the watchdog timer. If no quadrature-clock event is detected until a period match (QWDPRD = QWDTMR), then the watchdog timer will time out and the watchdog interrupt flag will be set (EQEP_QINT_EN_FLG[20] WTOI_FLG). The time-out value is programmable through the watchdog period bit field (EQEP_QWD_TMR_PRD[31-16] QWDPRD).

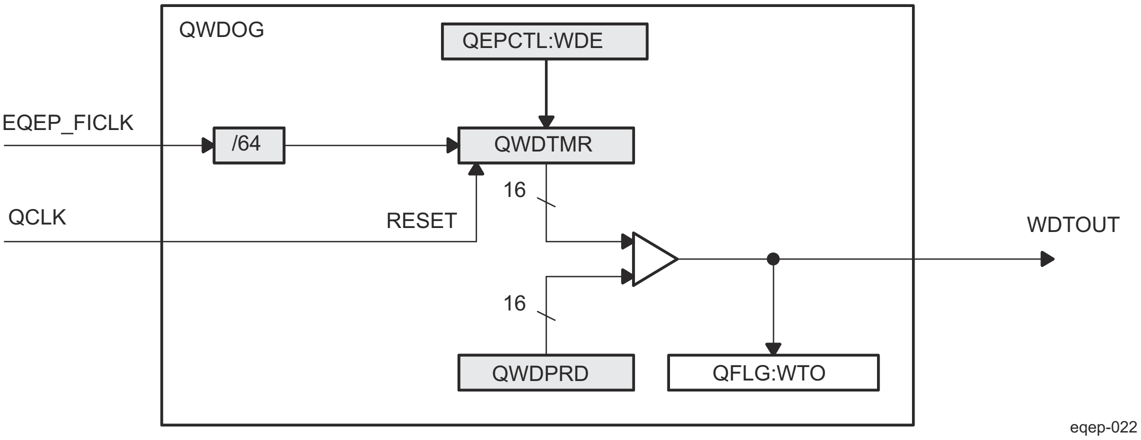

Figure 12-384. EQEP Watchdog Timer

12.5.4.4.6 Unit Timer Base

The EQEP peripheral includes a 32-bit timer (QUTMR) that is clocked by SYSCLKOUT to generate periodic interrupts for velocity calculations. The unit time out interrupt is set (EQEP_QINT_EN_FLG[27] UTOI_FLG) when the unit timer (QUTMR) matches the unit period register (EQEP_QUPRD).

The EQEP peripheral can be configured to latch the position counter, capture timer, and capture period values on a unit time out event. The latched values are used for velocity calculation as described in Section Section 12.5.4.4.4 .

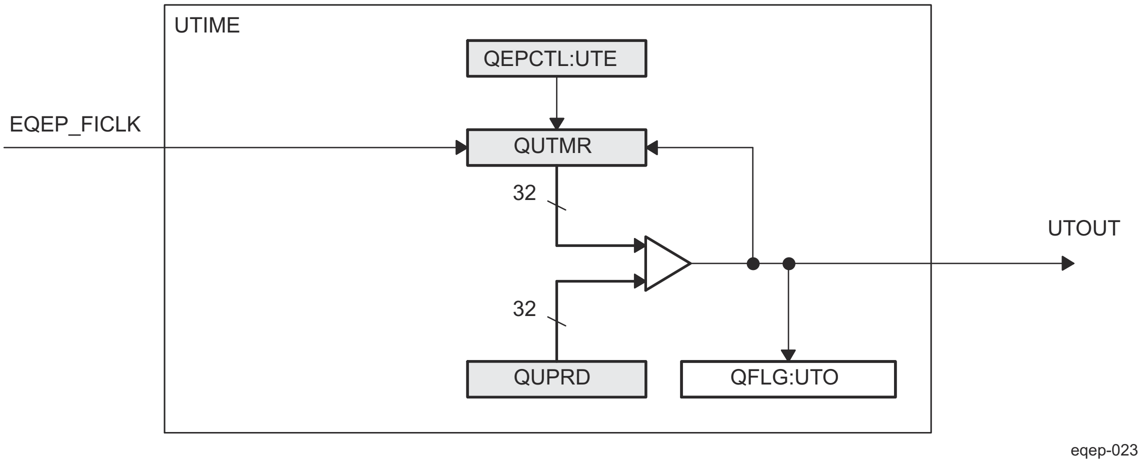

Figure 12-385. EQEP Unit Time Base

12.5.4.4.7 EQEP Interrupt Structure

Figure 12-386 shows how the interrupt mechanism works in the EQEP module.

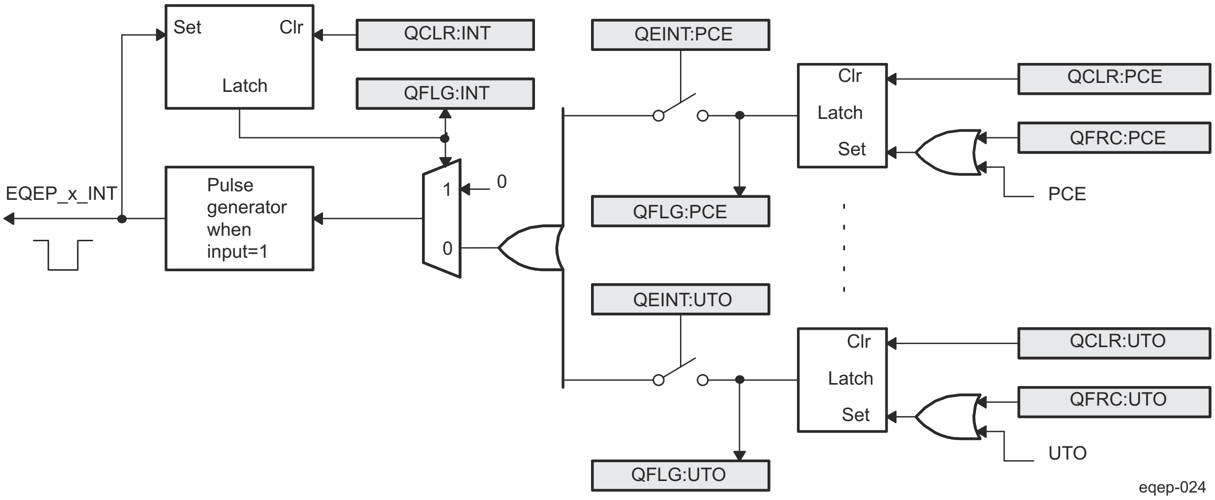

Figure 12-386. EQEP Interrupt Generation

Eleven interrupt events (PCE, PHE, QDC, WTO, PCU, PCO, PCR, PCM, SEL, IEL, and UTO) can be generated. The interrupt control register (EQEP_QINT_EN_FLG) is used to enable/disable individual interrupt event sources. The interrupt flag register (EQEP_QINT_EN_FLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is only generated to the interrupt controller if any of the interrupt events is enabled, the flag bit is 1 and the INT flag bit is 0. The interrupt service routine will need to clear the global interrupt flag bit and the serviced event, via the interrupt clear register (EQEP_QINT_CLR_FRC), before any other interrupt pulses are generated. SW can force an interrupt event by way of the interrupt force register (EQEP_QINT_CLR_FRC), which is useful for test purposes.

12.5.4.4.8 Summary of EQEP Functional Registers

Table 12-313 lists the registers with their memory locations, sizes, and reset values.

Table 12-325. EQEP Control and Status Functional Registers

Offset	Acronym	Register Description	Size (×16)/ #shadow
0h	EQEP_QPOSCNT	EQEP Position Counter Register	2/0
4h	EQEP_QPOSINIT	EQEP Position Counter Initialization Register	2/0
8h	EQEP_QPOSMAX	EQEP Maximum Position Count Register	2/0
Ch	EQEP_QPOSCMP	EQEP Position-Compare Register	2/1
10h	EQEP_QPOSILAT	EQEP Index Position Latch Register	2/0
14h	EQEP_QPOSSLAT	EQEP Strobe Position Latch Register	2/0
18h	EQEP_QPOSLAT	EQEP Position Counter Latch Register	2/0
1Ch	EQEP_QUTMR	EQEP Unit Timer Register	2/0
20h	EQEP_QUPRD	EQEP Unit Period Register	2/0
24h	EQEP_QWDTMR	EQEP Watchdog Timer Register	1/0
26h	EQEP_QWDPRD	EQEP Watchdog Period Register	1/0
28h	EQEP_QDECCTL	EQEP Decoder Control Register	1/0
2Ah	EQEP_QEPCTL	EQEP Control Register	1/0
2Ch	EQEP_QCAPCTL	EQEP Capture Control Register	1/0
2Eh	EQEP_QPOSCTL	EQEP Position Compare Control Register	1/0
30h	EQEP_QEINT	EQEP Interrupt Control Register	1/0
32h	EQEP_QFLG	EQEP Interrupt Flag Register	1/0
34h	EQEP_QCLR	EQEP Interrupt Clear Register	1/0
36h	EQEP_QFRC	EQEP Interrupt Force Register	1/0
38h	EQEP_QEPSTS	EQEP Status Register	1/0
3Ah	EQEP_QCTRM	EQEP Capture Timer Register	1/0
3Ch	EQEP_QCPRD	EQEP Capture Period Register	1/0
3Eh	EQEP_QCTMRLAT	EQEP Capture Timer Latch Register	1/0
40h	EQEP_QCPRDLAT	EQEP Capture Period Latch Register	1/0
5Ch	EQEP_PID	EQEP Peripheral ID Register	2/0

12.6 Camera Subsystem and Peripherals

12.6.1 MIPI D-PHY Receiver (DPHY_RX)

The following sections describe the MIPI D-PHY receiver (DPHY_RX) module(s) in the device.

12.6.1.1 DPHY_RX Overview

The integration of the DPHY_RX camera physical port module allows the device to grab video streams from external sensor cameras and other CSI2 compliant sources.

Figure 12-387 shows the DPHY_RX module overview.

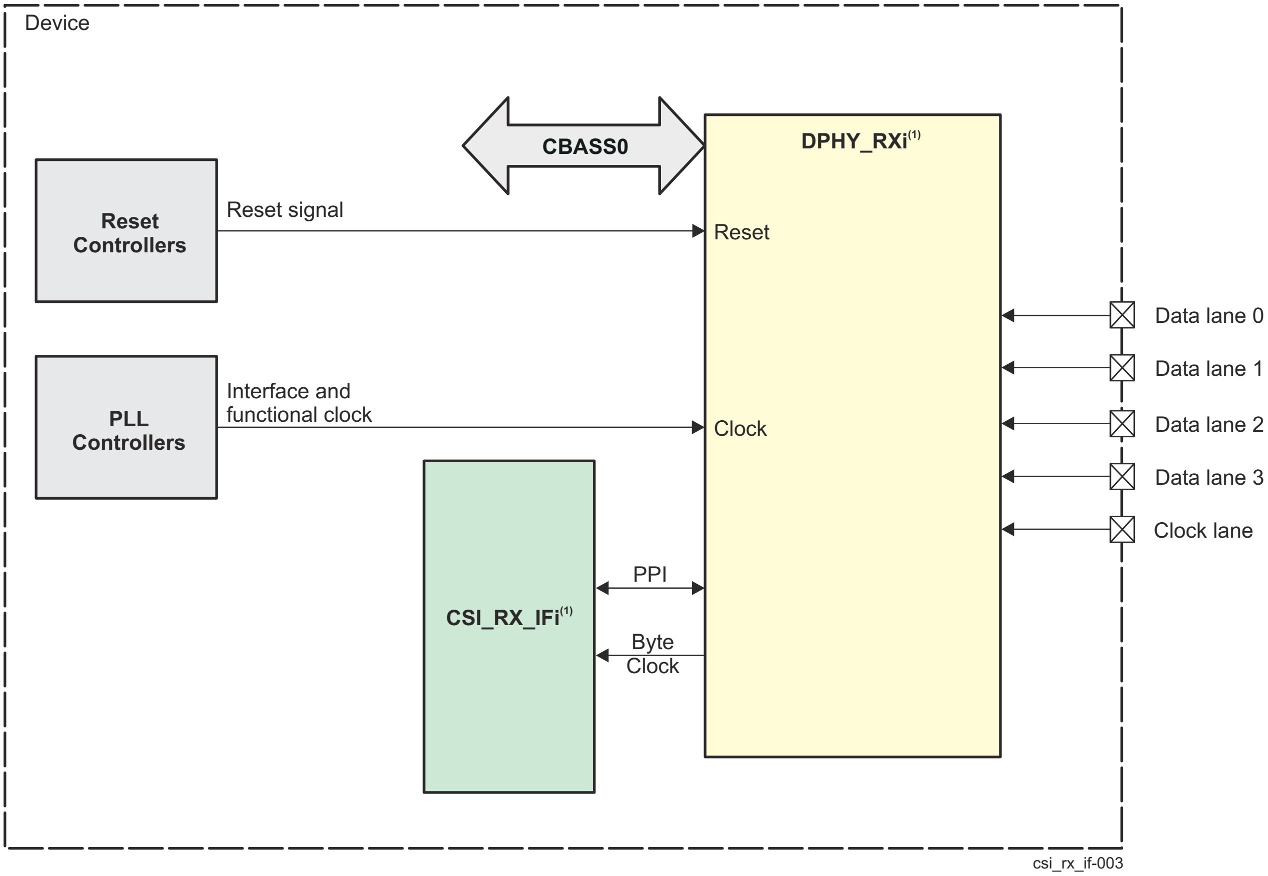

Note

i represents a DPHY_RX instance. See the device datasheet for available domains and DPHY_RX instances.

Figure 12-387. DPHY_RX Module Overview

12.6.1.1.1 DPHY_RX Features

The DPHY_RX module supports the following features:

- Compliant to MIPI D-PHY standard v1.2
- Supports up to 4 data and 1 clock lanes
- Supports up to 2.5 Gbps (with deskew) and 1.5 Gbps (without deskew) per data lane
- Clock lane control / interface logic type is **CIL-SCNN** for HS and low power receiving:
    1. **(S)** Peripheral
    2. **C**lock
    3. **N**/A forward, **N**/A reverse escape mode features
- Data lane control / interface logic type is **CIL-SFAN** for HS and low power receiving:

1. **(S)** Peripheral
2. **F**orward direction only for high speed mode
3. **A**ll forward direction escape mode features are supported
4. **N**o reverse direction escape mode features are supported

- Data lanes can be independently operated in HS or ULP mode
- Swapping of DP/DN signals within each clock/data pair (Facilitated by CSI_RX_IF controller)

12.6.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.6.1.2 DPHY_RX Environment

This section describes the DPHY_RX application fields from an environment point of view (external connections).

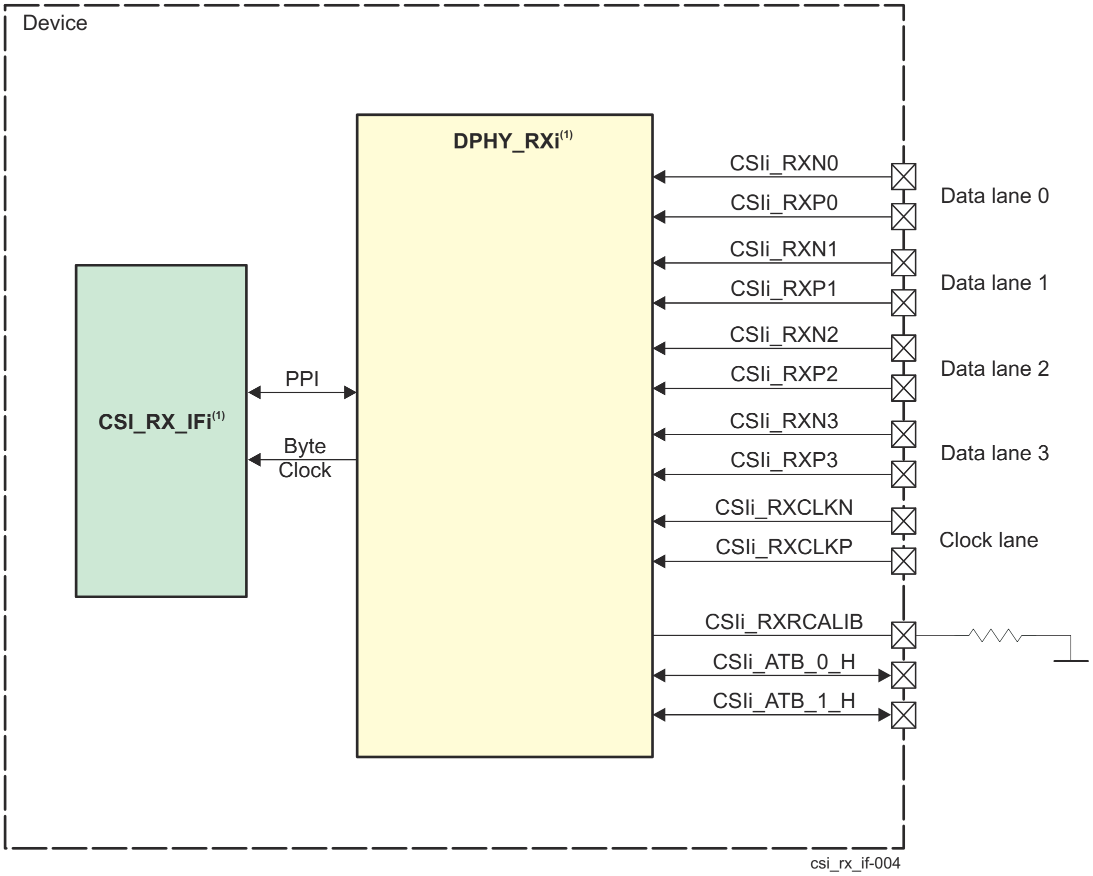

Note

i represents a DPHY_RX instance. See the device datasheet for available domains and DPHY_RX instances.

Figure 12-388. DPHY_RX Enviroment

Table 12-314 describes the external signals of the DPHY_RX.

Table 12-326. DPHY_RX I/O Signals

Device Level Signal	I/O	Description
		DPHY_RXi[1]
CSIi[1]_RXN0	I	Lane 0 Receive Differential Data (Negative)
CSIi[1]_RXP0	I	Lane 0 Receive Differential Data (Positive)
CSIi[1]_RXN1	I	Lane 1 Receive Differential Data (Negative)
CSIi[1]_RXP1	I	Lane 1 Receive Differential Data (Positive)
CSIi[1]_RXN2	I	Lane 2 Receive Differential Data (Negative)
CSIi[1]_RXP2	I	Lane 2 Receive Differential Data (Positive)
CSIi[1]_RXN3	I	Lane 3 Receive Differential Data (Negative)
CSIi[1]_RXP3	I	Lane 3 Receive Differential Data (Positive)
CSIi[1]_RXCLKN	I	Lane 3 Receive Differential Clock (Negative)
CSIi[1]_RXCLKP	I	Lane 3 Receive Differential Clock (Positive)
CSIi[1]_RXRCALIB	A	Pin for external calibration resistor. An external resistor must be connected between this pin and package ground. Refer to the device-specific Datasheet for a recommended resistor value.

(1) i represents a DPHY_RX instance. See the device datasheet for available domains and DPHY_RX instances

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.6.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.6.1.4 DPHY_RX Functional Description

12.6.1.4.1 DPHY_RX Programming Guide

12.6.1.4.1.1 Overview

This section details specific steps on how to program the DPHY_RX

12.6.1.4.1.2 Initial Configuration Programming

The DPHY_RX operation shows the registers that are written during the startup sequence.

This section provides description and timing diagrams for DPHY_RX operation. Unless otherwise described in this subsection, the DPHY_RX PPI interface is compliant with the timing diagrams described in the MIPI D-PHY v1.2 specification.

12.6.1.4.1.2.1 Start-up Sequence Timing Diagram

The common configuration pins noted in Figure 12-389 are ipconfig_cmn, pll_ipdiv, pll_fbdiv, pll_opdiv, psm_clock_freq_cmn. Drive these pins as per the pin description given in PHY pin list.

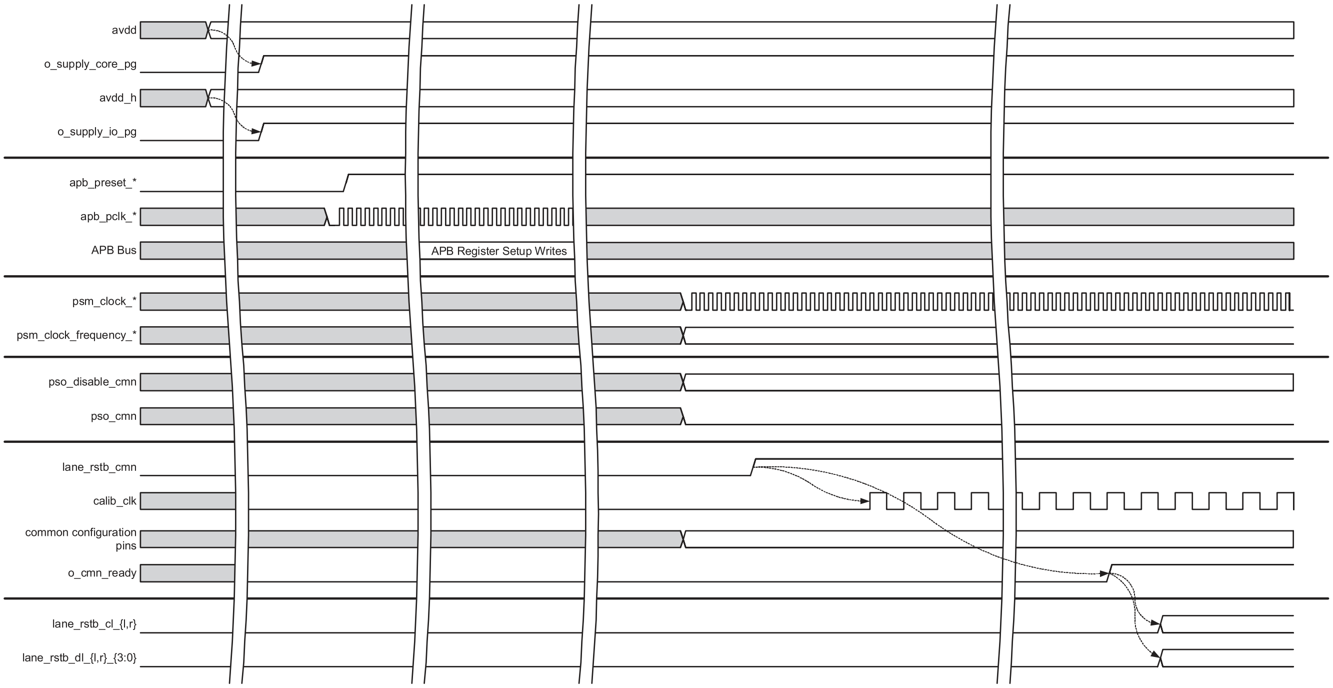

Figure 12-389. Common Power Up and Initialization Timing Diagram

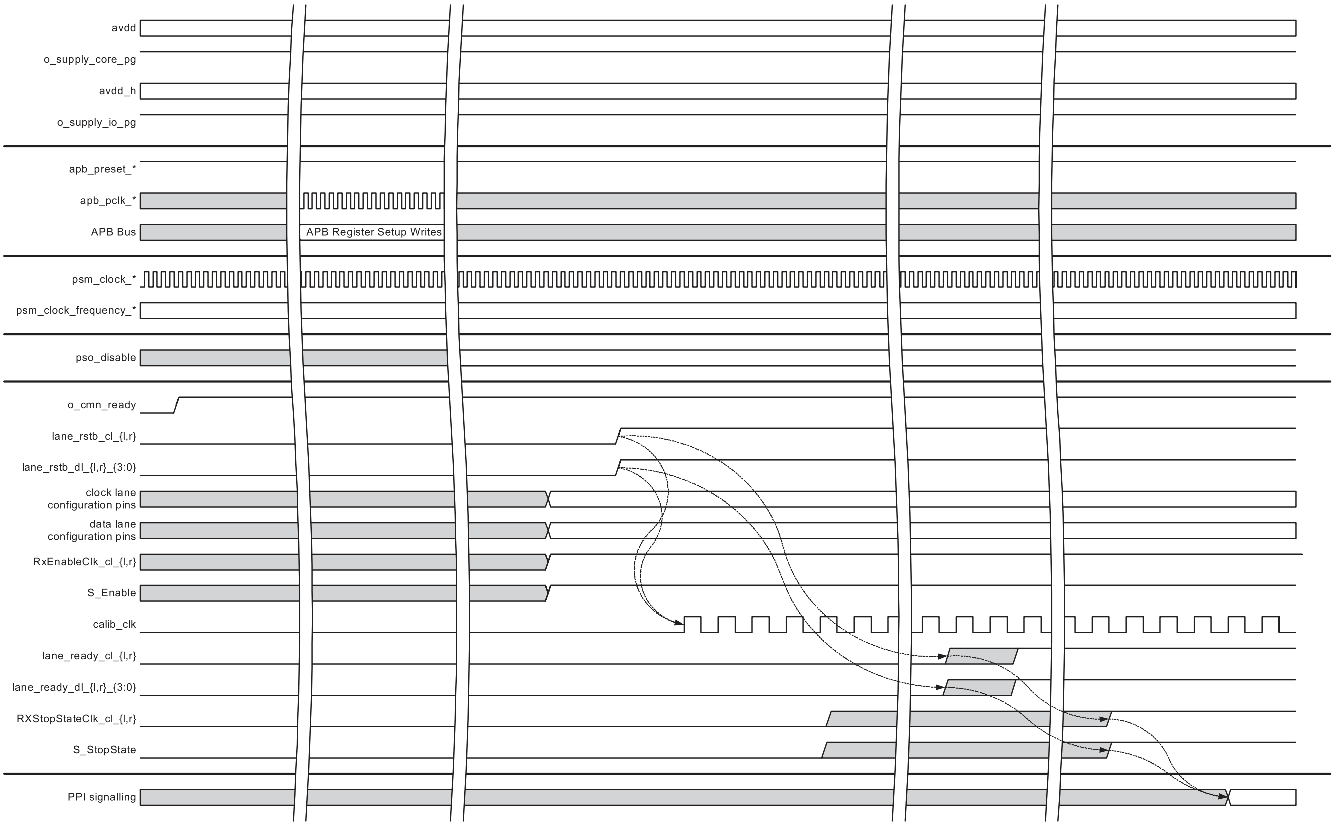

Figure 12-390. Lane Power Up and Initialization Timing Diagram

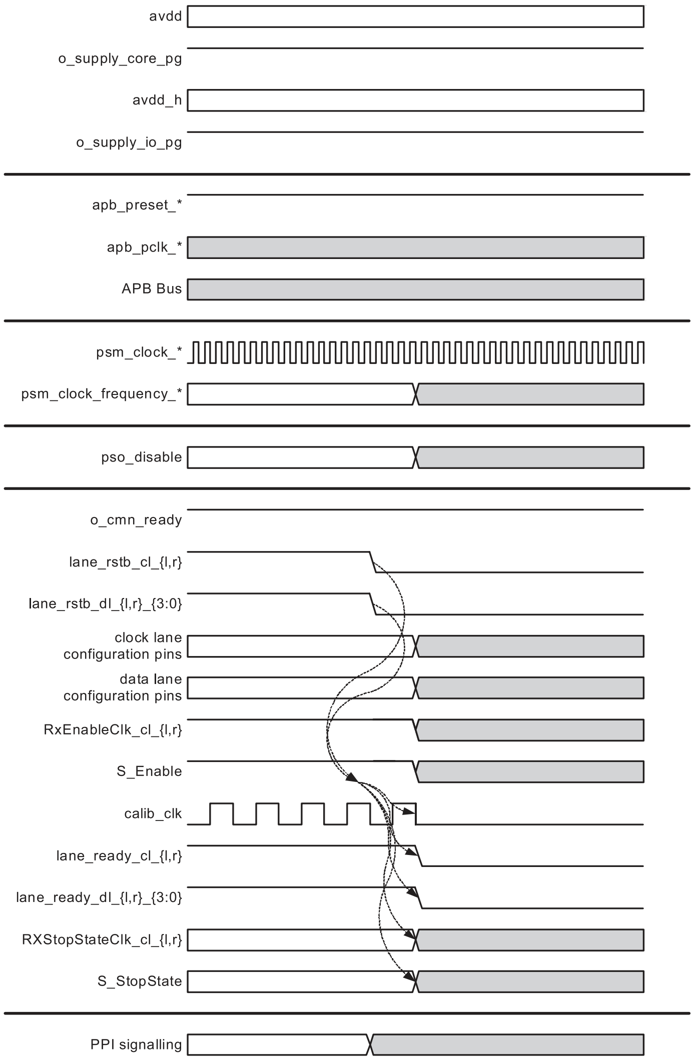

Figure 12-391. PHY Disable Timing Diagram

For initial set up, the DPHY_RX must be configured/set (registers and configuration input pins) for the common module prior to releasing it from reset, and the lane modules prior to releasing them from reset. Registers shall be configured (as required) between releasing the APB from reset and releasing the common / lanes from reset.

Note that in some cases, the option exists to configure a function using either a pin or a register. In such cases, both options will be specified and the you can select the preferred option.

12.6.1.4.1.3 Common Configuration

Table 12-327. Common Configuration-Related Setup

Configuration Register / Pin	Configuration Requirement
PHY Pin: psm_clock_freq PHY Register: DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1	Set the PMA state machine clock frequency divider. Set either the pin or the register, as specified in the respective description, for the required PMA state machine clock.
PHY Pin: ipconfig_cmn PHY Register: DPHY_RX_MMR_SLV_LANE[11-9] IPCONFIG_CMN	Set the clock lane configuration. Set as specified in the description for the required clock lane configuration.

Table 12-327. Common Configuration-Related Setup (continued)

Configuration Register / Pin	Configuration Requirement
PMA Register: DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2[0] O_CMN_SSM_EN, DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2[10] O_CMN_RX_MODE_EN	Enable the startup state machines for TX mode of operation. Set both register bits to 1'b1.
PHY Register: DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2	Set the required power island phase 2 time. Set the register to 32'hAAAAAAAA.
PHY Register: DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3[7:4] POWER_SW_2_TIME_CL_R, DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3[3:0] POWER_SW_2_TIME_CL_L	Set the required power island phase 2 time. Set the register to 8'hAA

12.6.1.4.1.4 Lane Configuration

Table 12-328. Lane Configuration-Related Setup

Configuration Register / Pin	Configuration Requirement
PHY Register: DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0	Set the lane band control value. Set the register fields, as specified in the register description for the required data rate.

12.7 Timer Modules

This section describes the timer modules in the device.

12.7.1 Global Timebase Counter (GTC)

This section describes the global timebase counter (GTC) in the device.

12.7.1.1 GTC Overview

The GTC module provides a continuous running counter that can be used for time synchronization and debug trace time stamping.

12.7.1.1.1 GTC Features

The GTC supports the following features:

- 64-bit up counter
- No rollover during the lifetime of the device
- Compatible with ARMv8 system counter requirements:
  - Disabled at power-up
  - Register definition and memory map aligned to ARMv8 definition
  - Implements memory-mapped counter control and status frames
- Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
- Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols

12.7.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.7.1.2 GTC Functional Description

12.7.1.2.1 GTC Block Diagram

The GTC is essentially comprised of a 64-bit up counter, a Gray encoder, a 64-bit multiplexer, and memory-mapped control registers. Figure 12-392 shows a high-level block diagram of the GTC.

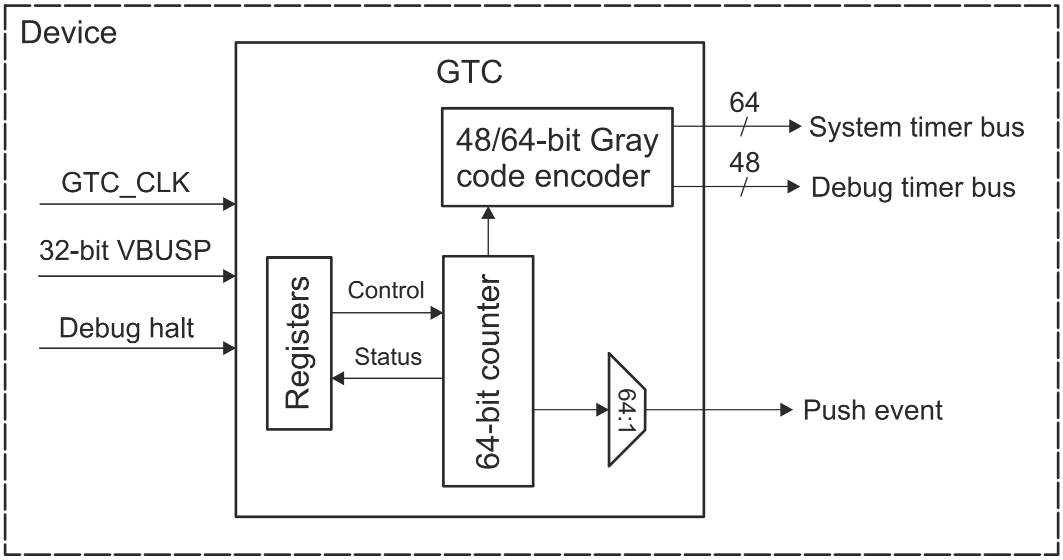

Figure 12-392. GTC Block Diagram

12.7.1.2.2 GTC Counter

The counter is a 64-bit binary up counter that increments on every GTC_CLK rising edge. The source for GTC_CLK is selected through a mux which is controlled via the GTC_CLKSEL[2-0] register bit field.

The counter is disabled by default (at power-on-reset) and increments only when enabled by setting the *GTC_CFG1_CNTCR*[0] EN bit to '1'. The current counter value is readable via the combined COUNTVALUE bit field of both *GTC_CFG1_CNTCV_HI* (upper 32 bits) and *GTC_CFG1_CNTCV_LO* (lower 32 bits) registers.

When counting is disabled, a new counter value can be loaded via a software write to the combined COUNTVALUE bit field. In this case, when the counter gets re-enabled, it will start counting from the last value written to this field.

The counter can be optionally configured to stop incrementing when a debug halt signal is issued, by writing a '1' to the *GTC_CFG1_CNTCR*[1] HDBG bit. This condition is indicated through the *GTC_CFG1_CNTSR*[1] DBGH status bit.

12.7.1.2.2.1 Steps to Clear the Counter Value to Zero

1. Disable the GTC
2. Clear GTC_CNTCV_LO (First)
3. Clear GTC_CNTCV_HI (Second)
4. Enable the GTC

Once the GTC is enabled, the GTC_CNTCV_HI bit will be cleared to zero.

12.7.1.2.3 GTC Register Partitioning

The ARMv8 architecture spec requires specific system-level components, each with one or two register frames. To accommodate this, the GTC memory-mapped registers (MMRs) are divided into four separate regions (4KB each):

- Peripheral MMRs (GTC0_GTC_CFG0): This region includes standard peripheral identification registers and any other control registers not associated with the ARMv8 system timer functions.

- Counter control MMRs (GTC0_GTC_CFG1): This region includes registers that provide control over the operation of the system timer.
- Counter status MMRs (GTC0_GTC_CFG2): This region includes registers that provide a mechanism for reading the status of the system timer.
- Timer control MMRs (GTC0_GTC_CFG3): This region includes registers that identify and provide a control mechanism for memory-mapped timer implementations. For this device, no memory-mapped timers are implemented and only the minimum registers required to indicate the presence of no timers are necessary.

12.7.2 RTI-Windowed Watchdog Timer (WWDT)

This section describes the Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module in the device.

CAUTION

The RTI module shall be used to serve only as a Digital Windowed Watchdog (DWWD).

The Real Time Interrupt module provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

The timers also provide the ability to benchmark certain areas of code by reading the counter contents at the beginning and the end of the desired code range and calculating the difference between the values.

12.7.2.1 RTI Features

The RTI modules include the following main features:

- Windowed Watchdog Timer (WWDT) feature.
- Two independent 64 bit counter blocks (counter block0 or counter block1). Each block consists of
  - One 32 bit up counter
  - One 32 bit free running counter
  - Two capture registers for capturing the prescale and free running counter on a special event.
- Free running counter 0 can be incremented by either the internal prescale counter or by an external event.
- Four configurable compare registers for generating operating system ticks . Each event can be driven by either counter block0 or counter block1.
- Fast enabling/disabling of events.
- RTI clock input derived from any of the available clock sources, selectable in the System Module
- Optional capability to drive a pulse-width modulated signal out on an interrupt line.

12.7.2.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.7.2.3 RTI Functional Description

The MCU_RTI0 and RTI modules are hereinafter referred to as RTI module.

12.7.2.3.1 RTI Digital Windowed Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Note

Digital windowed watchdog (DWWD) timer is implemented using the digital windowed watchdog function of the RTI modules. Real time interrupt functionality is not supported. In this mode, the timer should default to disabled and user can adjust the period as desired before enabling the watchdog.

In addition to the time-out boundary configurable via the digital watchdog (DWD), some applications may also want to configure the start-time boundary of the watchdog. This is enabled by the digital windowed watchdog (DWWD) feature.

Functional Behavior

The DWWD opens a configurable time window in which the watchdog must be serviced. Any attempt to service the watchdog outside this time window, or a failure to service the watchdog in this time window, will cause the watchdog to generate either a reset or a non-maskable interrupt to the CPU. This is controlled by configuring the RTI_RTIDWWDRXNCTRL register. As stated earlier, when the watchdog needs to be enabled by software, the watchdog counter is disabled on a system reset. When the DWWD is configured to generate a non-maskable interrupt on a window violation, the watchdog counter continues to count down. The RTI_INTR_WWD interrupt handler needs to clear the watchdog violation status flag(s) and then service the watchdog by writing the correct sequence in the watchdog key RTI_RTIWDKEY register. This service will cause the watchdog counter to get reloaded from the preload value and start counting down. If the RTI_INTR_WWD handler does not service the watchdog in time, it could count down all the way to zero and wrap around. No second exception for a time out is generated in this case.

Configuration of DWWD

The DWWD preload value (same as DWD preload) can only be configured when the DWWD counter is disabled. The window size and watchdog reaction to a violation can be configured even after the watchdog has been enabled. Any changes to the window size and watchdog reaction configurations will only take effect after the next servicing of the DWWD.

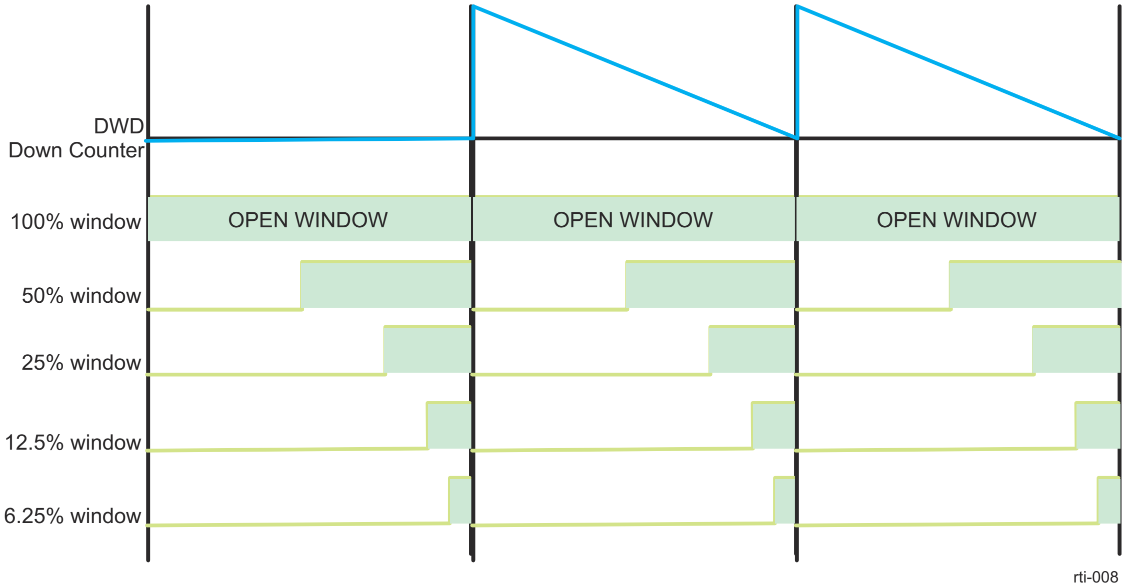

Figure 12-393. RTI Digital Windowed Watchdog Timing Example

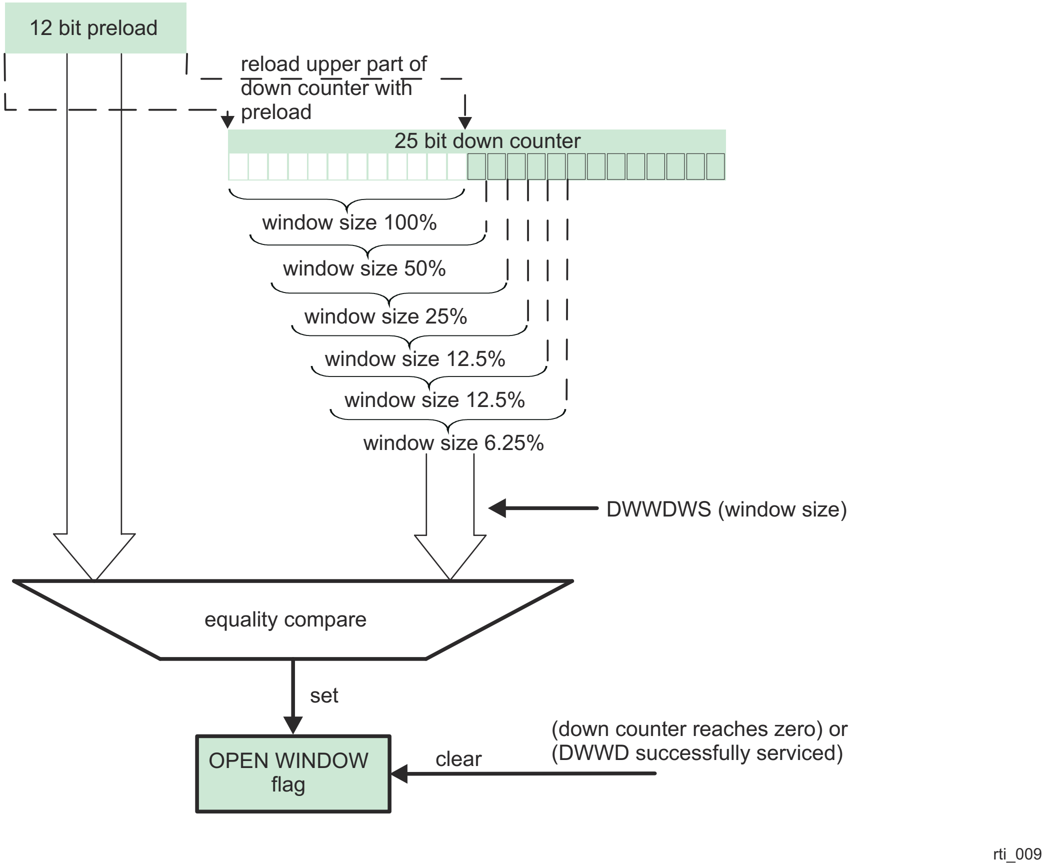

Figure 12-394. RTI Digital Windowed Watchdog Operation Block Diagram

12.7.2.3.1.1 RTI Debug Mode Behavior

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Once the system enters debug mode, the behavior of the RTI depends on the RTI_RTIGCTRL[15] COS bit. If the bit is cleared and debug mode is active, all counters will stop operation. If the bit is set to one, all counters will be clocked normally and the RTI will work like in normal mode.

The DWD counter will not decrement in debug mode and will hold its current value, regardless of the RTI_RTIGCTRL[15] COS bit.

Note

The user must not service the watchdog while in debug mode.

12.7.2.3.1.2 RTI Low Power Mode Operation

The operation of the RTI module is guaranteed in run, doze and snooze mode. In sleep or hibernate mode all clocks will be switched off and the RTI module will not work.

In doze and snooze modes all parts of the RTI are active, since it has to be able to wake up the device with compare and timebases interrupts. Capturing events generated by the interrupt module is also possible since in both modes the peripheral modules are able to generate interrupts, which can trigger capture events. The RTI module will generate compare and timebases interrupts. The compare interrupts will periodically wake up the device.

Note

In the special case of doze mode with DPLL off, RTI_FCLK might have a different period than with DPLL enabled, since RTI_FCLK will be derived from the oscillator output. It has to be ensured that the RTI_ICLK to RTI_FCLK ratio is at least 3:1.

The DWD/DWWD remains active when the device enters low power mode as long as the RTI_FCLK is kept active.

Whenever the LPSC that controls an RTI is in any state other than Enable (see , *Module States*), the RTI cannot count or generate interrupts. For more information, see , *Power Control Modules*.

During standard SoC warm reset the RTI and the rest of the SoC are reset. In this case, the RTI counters are stopped and interrupts are not issued. During reset-isolated warm reset, if an R5FSS is put in reset-isolation, then the associated RTI also becomes reset isolated. As such, the R5FSS and the RTI are not reset, but RTI stops counting and cannot generate interrupts until R5FSS is taken out of CLKSTOP (brought to Enable state).

12.7.2.3.2 RTI Digital Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Some applications might use a digital watchdog (DWD) integrated in the RTI module. The digital watchdog generates resets after a programmable period, if no correct key sequence is written to the RTI_RTIWDKEY register. Figure 12-395 shows the digital watchdog functional block.

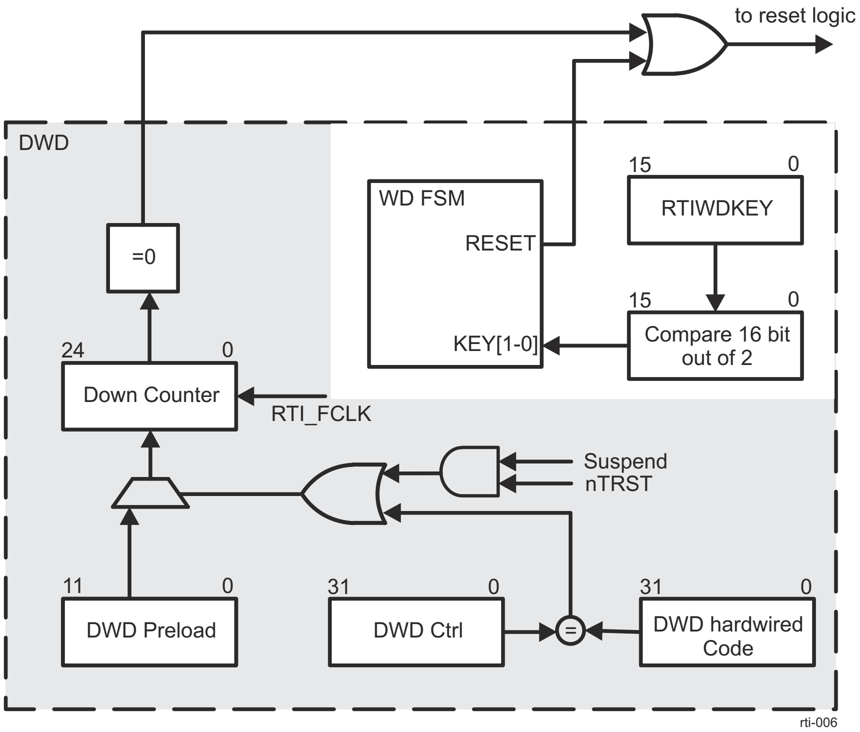

Figure 12-395. RTI Digital Watchdog Functional Block Diagram

The digital watchdog functionality is implemented such that it can be enabled by software.

The DWD starts counting down from the reset value of the RTI_RTIDWDCNTR (DWD Counter Register). The DWD preload register can be configured at any time by the application according to the desired time-out period.

When enabled by software, the digital watchdog is disabled after system reset. If it should be used, it has to be enabled by writing A98559DAh to the RTI_RTIDWDCTRL register. The DWD timeout period must be configured using the DWD preload register before the DWD is enabled. The DWD cannot be disabled by the application once it is enabled.

Note

When the DWD is enabled by software, any system reset will disable the DWD. This reset could have been generated by the watchdog itself.

If the correct key sequence is written to the RTI_RTIWDKEY register (E51Ah followed by A35Ch), the 25-bit DWD Down Counter is reloaded with the 12-bit preload value stored in RTI_RTIDWDPRLD register. If any incorrect value is written to the RTI_RTIWDKEY register, a watchdog reset will occur immediately. A reset will also be generated, when the DWD Down Counter is decremented to 0.

The user has to take into account that the write to the RTI_RTIWDKEY register takes 3 RTI_ICLK cycles. This needs to be considered for the DWD expiration calculation.

The DWD Down Counter will be decremented with RTI_FCLK frequency. If the RTI_FCLK is switched off via the disable registers of the Clock management, the DWD counter stops decrementing. The DWD module cannot generate a reset under this condition.

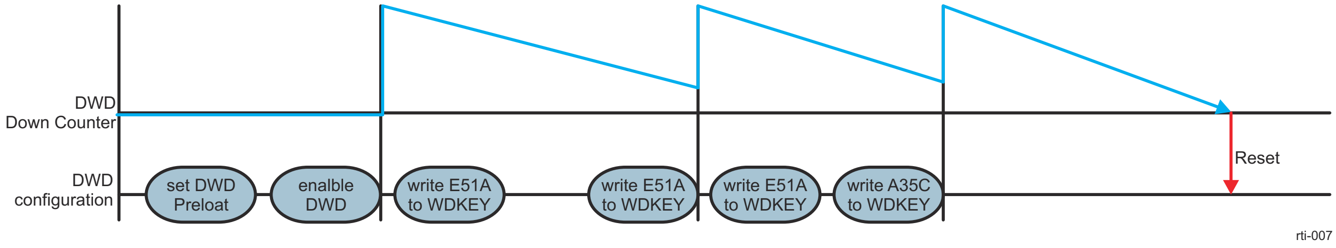

Figure 12-396. RTI Digital Watchdog Operation

The expiration time of the DWD Down Counter can be determined with following equation:

$$t_{exp} = (\text{RTI\_RTIDWDPRLD} + 1) \times 2^{13} / \text{RTI\_FCLK} \quad (7)$$

where RTI_RTIDWDPRLD = 0...4095

12.7.2.3.3 RTI Counter Operation

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Figure 12-397 shows the RTI module counter blocks. The RTI module supports two counter blocks.

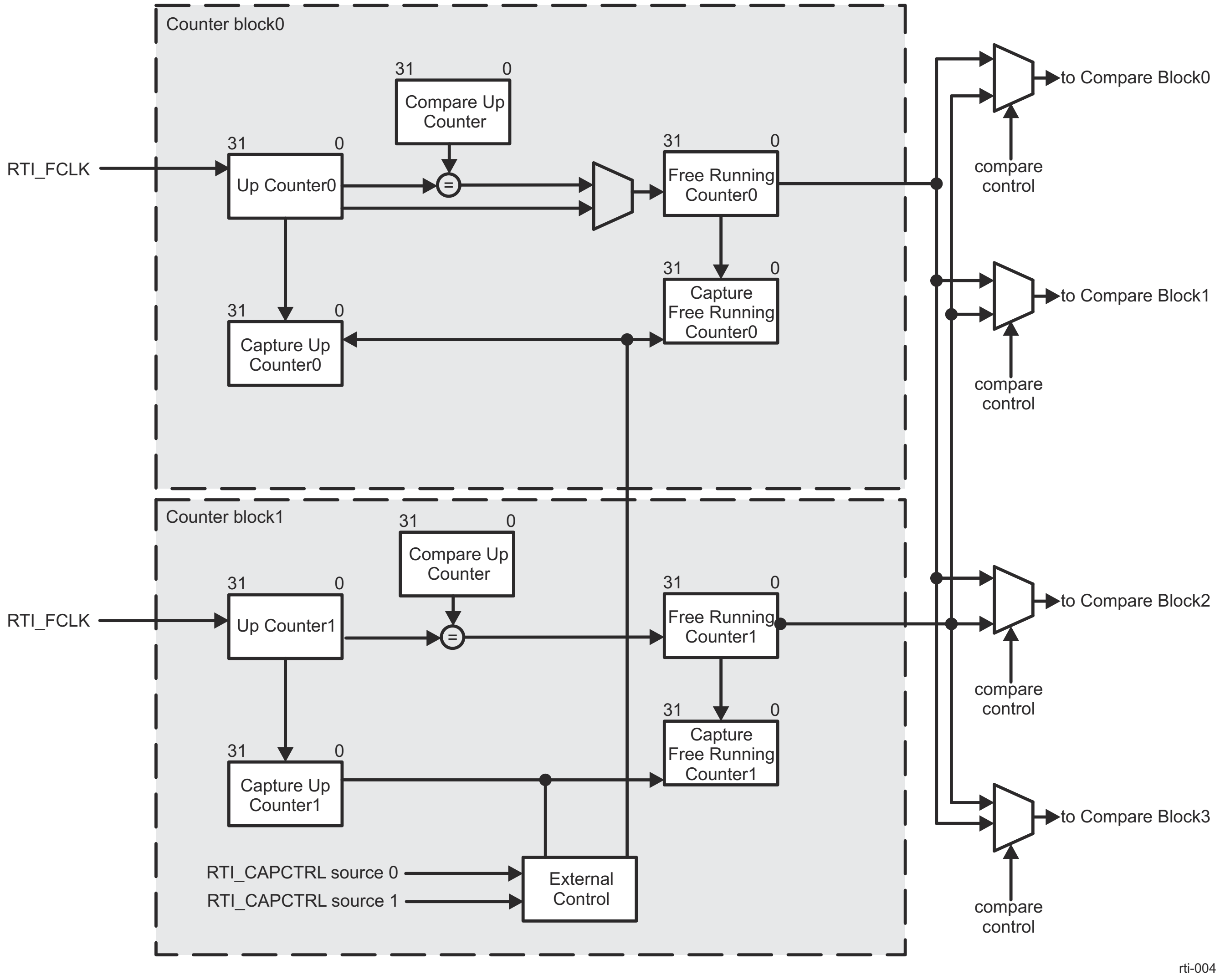

Figure 12-397. RTI Counters Block Diagram

Each block consists of two 32 bit up counters - Up Counter (UC) and Free Running Counter (FRC). The Up Counter (RTI_RTICAUC0 or RTI_RTICAUC1 register) is driven by the RTI_FCLK and counts up until the compare value in the Compare Up Counter register (RTI_RTICPUC0 or RTI_RTICPUC1) is reached. When the compare matches, the second counter (RTI_RTICAFRC0 or RTI_RTICAFRC1 register), which is a free running counter, is incremented. At the same time UCx is reset to zero.

To ensure the consistency of the counters, when both counter value have to be determined, the Free Running Counter has to be read first. This will ensure that at the CPU read cycle, the Up Counter value is stored in the counter register. The second read is done on the Up Counter register, which holds then the value of the counter cycle of the previous read on the Free Running Counter register.

Both blocks provide also a capture feature on external events. Two capture sources can trigger the capture event. Which event triggers block 0 or block 1 is configurable from the RTI_RTICAPCTRL register. The sources are coming from the interrupt manager, in order to be able to generate a capture event when one of the peripheral modules has generated an interrupt. The peripheral, which can generate an event is configured in the interrupt manager. When the event is detected, UCx and FRCx are stored in Capture Up Counter (RTI_RTICAUC0 or RTI_RTICAUC1) and Capture Free Running Counter (RTI_RTICAFRC0 or RTI_RTICAFRC1) registers. The read order of the captured values has to be like the order of the actual counters. So the CAFRCx has to be read first and the CAUCx registers has to be read after the CAFRCx value was determined. While the CAFRCx is read the CAUCx value is loaded into a shadow register to ensure data consistency, if during the two reads of the captured data another capture event happens. If the application fails to read the two registers before a second capture event happens, the previous data will be overwritten.

Figure 12-398 shows the block diagram for one compare block. The RTI module supports four compare blocks.

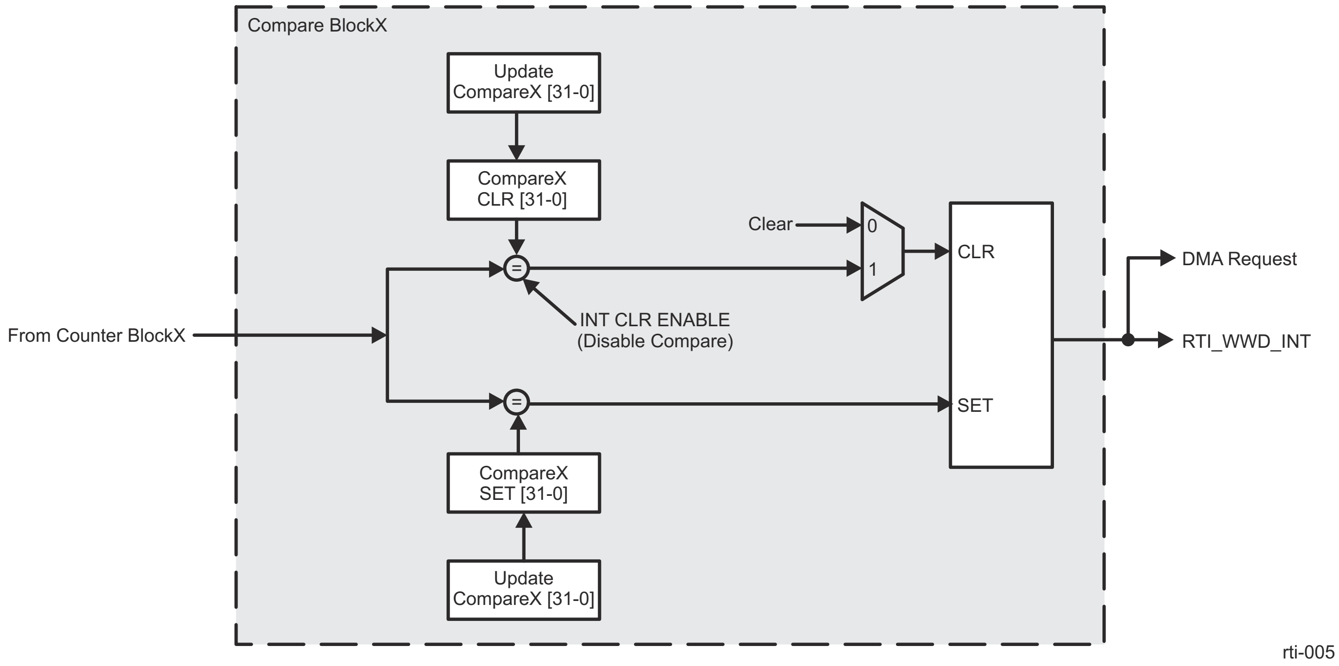

Figure 12-398. RTI Compare Block Diagram

In order to generate interrupt requests to the interrupt manager, there are four compare registers (RTI_RTICOMP0, RTI_RTICOMP1, RTI_RTICOMP2, and RTI_RTICOMP3). Each of the compare registers can be configured to work either on FRC0 (Counter block0) or FRC1 (Counter block1). When the counter value matches the compare value, an interrupt is generated. This sets an interrupt request line to the interrupt manager. The compare value gets updated automatically with the value stored in Update Compare (RTI_RTIUDCP0, RTI_RTIUDCP1, RTI_RTIUDCP2, and RTI_RTIUDCP3) registers when the compare matches. This gives the ability to generate periodic interrupts/DMA requests without having to update the compare value by software.

An optional feature allows an application to program another compare value which is then used to clear the interrupt request line. This feature is supported by four compare clear registers (RTI_RTICOMP0CLR, RTI_RTICOMP1CLR, RTI_RTICOMP2CLR, and RTI_RTICOMP3CLR). When the counter value matches the compare clear value, the interrupt line is cleared. This clears the interrupt request line to the interrupt manager. The compare clear value gets updated automatically with the value stored in Update Compare (RTI_RTIUDCPx) registers when the compare matches.

12.7.3 Real-Time Clock (RTC)

12.7.3.1 Overview

The objective of the Real-Time Clock Sub-System (RTCSS or RTC) is to provide a time counter that has accurate timekeeping at a sub-second granularity. With IP integration support to provide a battery-backed voltage domain, this time counter is persistent from one device standby until the next power-on.

DIG_ON is the same as battery-backed domain, or the always ON domain.

DIG_CORE is the CORE domain which powers off and on while the ON domain remains ON.

The major design problems that this subsystem needs to solve are:

- Providing software atomic read access to a large 63-bit time value.
- Clock accuracy calibration to compensate for any time period inaccuracy from the oscillator.

When this subsystem is integrated with Analog IP support, including the battery-backed always-on voltage domain, this subsystem also needs to address these problems:

- Synchronizing time counter data between the DIG_CORE, or volatile, voltage domain and the DIG_ON, or battery-backed, voltage domain.
- Voltage isolation between the Core and On voltage domains.

Additionally, RTC provides interrupts that are triggered when the time counter reaches a particular time. These can be used to trigger an SoC wakeup in the case of the OFF_ON event or to trigger an SoC low-power transition in the case of the ON_OFF event.

12.7.3.1.1 RTC Features

- 48-bit seconds counter supporting roll-over every 8.9 million solar years
- 15-bit sub-second counter, to be incremented at 32768Hz
- Total time resolution of 63 bits
- Simplified software interface compared to previous generations of RTC implementation. Reads and writes to time counter MMRs can happen at any phase of the 32768Hz low-frequency timekeeping clock. Previous RTC implementations required software to poll until a specific phase of the clock period.
- Event output, ON_OFF and OFF_ON. Each supports a 63-bit timestamp in the same format as the RTC count (48-bit seconds and 15-bit sub-second count). Can generate interrupts from these events even when the VBUS interface has been clock gated by using the 32768Hz clock. Also, the 4 external wakeup events if enable will also assert the event.
- Total of 256 bits of scratch pad register space.
- Supports active 32768Hz clock (normal RTC functionality).
- Instant off functionality. Even with Analog IP integration, no special requirements before removing voltage from Digital Core voltage domain.
- Functional lockout of MMR writes over VBUSP to protect RTC timer values from writes caused by glitches.
- DFT lockout of MMR writes over p1500 to protect RTC timer values from writes caused by glitches.
- 32-bit general-purpose IP configuration output signals from RTC_ANALOG MMR.

12.7.3.1.1.1 Features Supported with No-Analog IP Integration

- 1 Digital voltage domain
- Level-shifter and isolation cells are unnecessary and are removed to save power in this integration.
- Supports use as a general-purpose timer

12.7.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.7.3.2 RTC Integration

This device includes a Real-Time (RTC) module to allow easy tracking of time and date and the generation of real time alarms.

The following tables provide pin level detail for each of the interfaces on this module.

Table 12-317 describes the 1500 Interface for the DFT unlock circuit.

Table 12-329. 1500 Interface

Signal Name	Direction	Default Value	Description
jtag_wrck	In	1'd0	1500 wrapper clock

Table 12-329. 1500 Interface (continued)

Signal Name	Direction	Default Value	Description
jtag_wrstn_n	In	1'd1	1500 wrapper reset (active low)
jtag_wsi	In	1'd0	1500 wrapper serial input
jtag_selectwir	In	1'd0	1500 select wrapper instruction register
jtag_shiftwr	In	1'd0	1500 shift wrapper register
jtag_updatewr	In	1'd0	1500 update wrapper register
jtag_capturewr	In	1'd0	1500 capture wrapper register
jtag_wso	Out	1'd0	1500 wrapper serial out

Table 12-318 describes the PMIC Control External Wakeup and PMIC ON/OFF Control IOs.

Table 12-330. PMIC Control IOs

Signal Name	Direction	Default Value	Description
pmic_ext_wakeup0_io	In	1'd0	RTC Wakeup0
pmic_ext_wakeup1_io	In	1'd0	RTC Wakeup1
pmic_ext_wakeup2_io	In	1'd0	RTC Wakeup2
pmic_ext_wakeup3_io	In	1'd0	RTC Wakeup3
pmic_pmic_enable_io	Out	1'd1	RTC PMIC Enable 1 = ON 0 = OFF

Table 12-331. Analog Interface

Signal Name	Direction	Default Value	Description
ana_osc32k_clk	In	NA	Analog 32768 buffered Crystal clock If no analog, provide a near 32768 clock
ana_iso	In	1'd0	Analog ISO 1 = Isolated 0 = Not Isolated If no analog, tie 1’b0

Table 12-331. Analog Interface (continued)

Signal Name	Direction	Default Value	Description
ana_porz	In	NA	Analog PowerOnReset 1 = not asserted 0 = asserted This will assert when ON/BAT domain is powering up If no analog, then you can connect same reset which was used for rst_mod_g_rst_n You can also use por_rst_n class, it's a don't care
ana_cfg[31:0]	Out	TBD	Analog config If no analog, NC

Table 12-332. PSC Interface

Signal	Direction	Default Value	Description
pwri_clkstop_idle	Out	1'd1	The IP is in IDLE state, output of an IP
pwrs_clkstop_req	In	1'd0	Clock stop request
pwrs_clkstop_ack	Out	1'd0	Clock stop acknowledge
pwrw_clkstop_wakeup	Out	1'd0	Wakeup It requires clock stop protocol to be active and active vclk_clk
pwr_clk_clk_en	In	1'd1	Clock-gate enable to IP
pwr_clk_clk_en_ack	Out	pwr_clk_clk_en	Clock-gate enable acknowledge from IP

Table 12-321 describes the Main IP DFT Interface.

Table 12-333. IP DFT Interface

Signal Name	Direction	Default Value	Description
dft_partition_en	In	1'd0	dft_partition_en
dft_scan_en	In	1'd0	dft_scan_en
dft_clk_force_en	In	1'd0	dft_clk_force_en
dft_async_rst_sel	In	1'd0	dft_async_rst_sel
dft_test_async_rst_n	In	1'd1	dft_test_async_rst_n
dft_tft_mcp_dis	In	1'd0	Assert High to block MCP path
dft_local_clk_en	In	1'd0	dft_local_clk_en
dft_mode_atpg	In	1'd0	ATPG

The reset shown in Table 12-322 only goes to the core domain.

Table 12-334. Reset Interface

Signal Name	Direction	Default Value	Description
rst_mod_g_rst_n	In	1'd1	Module level main reset

Table 12-323 describes the Main on only VBUSP target port

Table 12-335. VBUSP Target Port

Signal Name	Direction	Default Value	Description
pr1_slv_req	In	1'b0	Request
pr1_slv_dir	In	1'b0	Direction
pr1_slv_address[31:0]	In	32'd0	Address
pr1_slv_xcnt[2:0]	In	3'd4	Good Byte Count
pr1_slv_byten[3:0]	In	{4{1'b1}}	Byte Enables
pr1_slv_wdata[31:0]	In	32'd0	Write Data
pr1_slv_wready	Out	1'b1	Write Ready
pr1_slv_rdatap[31:0]	Out	32'd0	Read Data (Pipelined)
pr1_slv_rready	Out	1'b1	Read Ready
pr1_slv_emudbg	In	1'b0	Emulation Debug Attribute

12.7.3.3 Functional Description

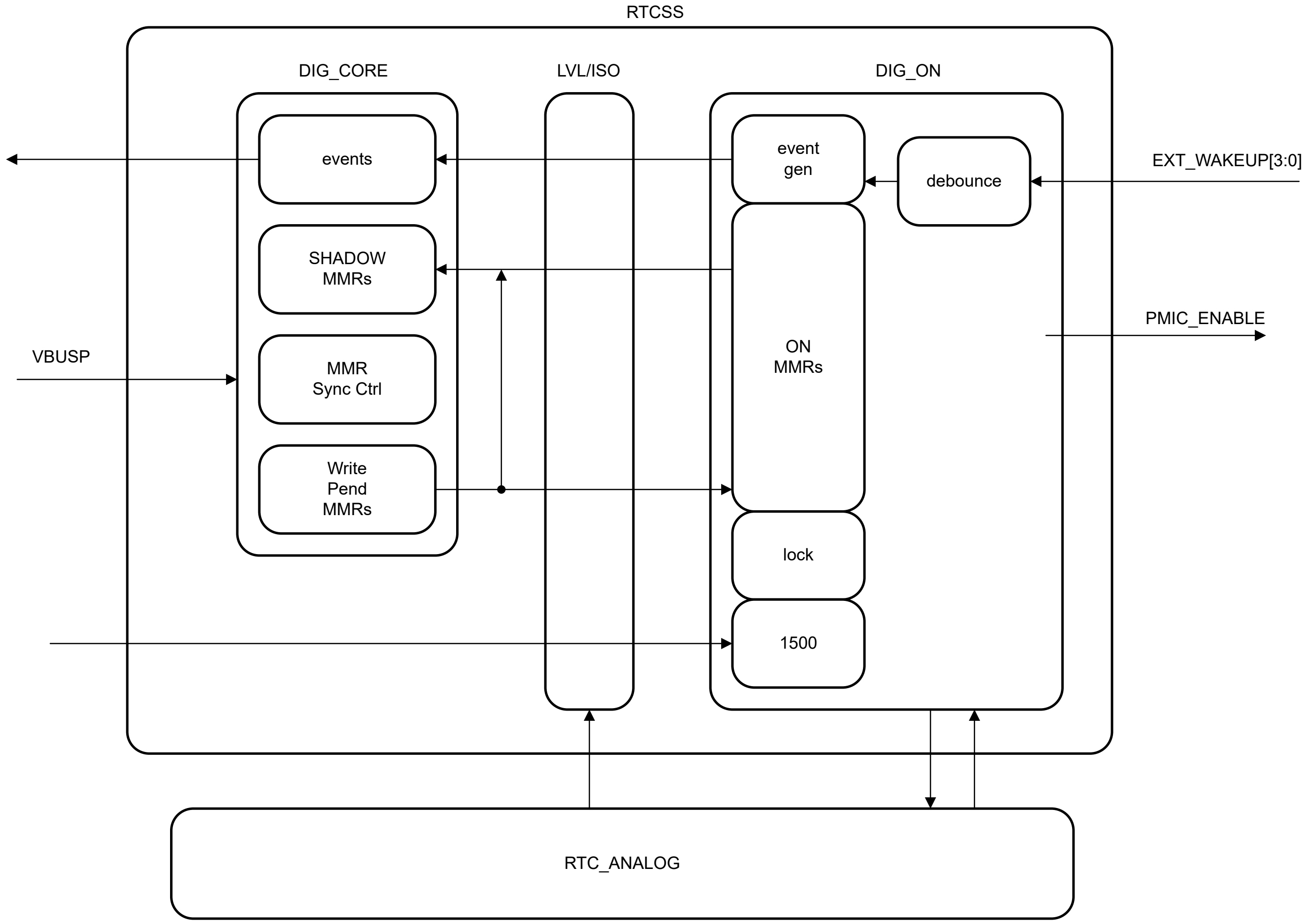

Figure 12-399. RTC Block Diagram

12.7.3.3.1 Architecture of RTC

The RTC is composed of 3 major blocks; the Core Domain block (DIG_CORE), the Battery Domain block (DIG_ON), and the Isolation block (LVL_ISO). The Core Domain block comprises the VBUSP interface logic, the MMR synchronization engine, the Keystone 3 Clock Stop interface, and the shadow MMRs. The Battery Domain block comprises the time counter, the IEEE 1500 DFT engine, the non-volatile MMR copies, the event processing and generation logic, and the analog configuration interface. The Battery Domain block also interfaces with the system I/O pins that provide support for external wake-up events and signal to an external Power Management IC (PMIC) that power needs to be applied to the SoC’s core domain. The Isolation block provides level shifters and voltage isolation between the two other blocks, which can be in different power domains when RTC is integrated with Analog IP support. All communication between the Core Domain block and the Battery Domain block occurs through the Isolation block.

12.7.3.3.1.1 RTC Microarchitecture

12.7.3.3.1.1.1 DIG_CORE Microarchitecture

This block is in the Core power domain. It can be reset or clock gated without affecting most functionality of RTC. It contains the VBUSP interface logic, the MMR synchronization engine, the Keystone 3 Clock Stop interface, the shadow MMRs, and the pending write value MMRs.

The Clock Stop interface clock-gates the vbusp clock on the DIG_CORE side. Wakeup event generation and timestamp event generation still function if the vbusp clock is gated.

The MMR interface and synchronization engine are the main functionality in the DIG_CORE block. The main operation details of these components are explained in the sections below.

12.7.3.3.1.1.1.1 Cross-domain MMR Access Details

VBUS read accesses to RTC are satisfied from the Shadow MMR register bank. VBUS write accesses to RTC have their write data written to the Write Pending MMR register bank.

On Domain MMRs have their register values synchronized from the Write Pending MMR register bank to the Shadow MMRs and to the On Domain MMRs. Their value is synchronized into both of the alternate register banks simultaneously. The exact time depends on O32K_OSC_DEP_EN as described.

Core Domain MMRs have no such synchronization behavior. Values written to the Core Domain MMRs have their Shadow MMR copy updated.

12.7.3.3.1.1.1.2 MMR Synchronization on Core Reset

After any reset of the Core power domain, the MMR Synchronization engine will synchronize MMRs from the battery-backed domain to the core domain.

The behavior of this synchronization depends on the GENRAL_CTL register copy that has been saved in DIG_ON since the last reset of the DIG_ON domain. If the saved value of the O32K_OSC_DEP_EN register field is 1, then the state machine will begin reading register values from DIG_ON starting when the 32KHz clock from DIG_ON falls. Otherwise, when O32K_OSC_DEP_EN is 0, then the state machine will begin transferring register values on the next vbus_clk clock cycle after the write is accepted. As a result, some timing requirements are imposed on register writes when O32K_OSC_DEP_EN is 0.

During this synchronization, the MMRs from DIG_ON in the address range 0x04 – 0x4C, inclusive, will be read and copied into the Shadow MMRs in the DIG_CORE block. The MMRs will be copied in increasing address order. The RTC_SYNCPEND register’s RD_PEND bit will be 1 while this operation is in progress and will be deasserted to 0 when the operation completes. Reading the MMRs in this address range is invalid while RD_PEND is 1.

This operation can also be initiated without a reset of the Core domain by writing 1 to the RELOAD_FROM_BBD field of the RTC_SYNCPEND register. This should be done after writing other RTC registers through the P1500 interface.

The DIG_CORE and DIG_ON domains can also get out of sync if the vbus_clk is stopped using the Keystone3 Clock Stop Protocol. If the vbus_clk is restarted after stopping the clock, then the DIG_CORE domain either needs to be reset, or the RELOAD_FROM_BBD field of the RTC_SYNCPEND register needs to be written 1. Otherwise, the time counters in the DIG_CORE and DIG_ON domains will de-synchronize from each other once the vbus_clk is restarted.

12.7.3.3.1.1.1.3 MMR Write Synchronization to DIG_ON

An MMR write will be synchronized to the DIG_ON copy of the MMRs if the write is done while the functional lockout is currently unlocked. Depending on the value of O32K_OSC_DEP_EN, MMR writes to DIG_ON may be delayed until the next falling edge of the 32KHz clock. If O32K_OSC_DEP_EN is 0, then an MMR write should only be done when two successive reads to RTC_SYNCPEND demonstrate a falling edge of the main 32KHz clock and that the 32KHz clock is currently low.

If the functional lockout is currently locked, then if MMR writes to KICK0 and KICK1 are done before other MMR writes, the functional lockout will be unlocked for any ensuing writes. In principle, these MMR writes to open the functional lockout may be done at any time. Once these writes are done, further writes will be accepted and held pending in the CORE domain. A following MMR write to KICK0 or KICK1 will close the functional lockout for any subsequent writes. In order to support functionally correct operation, the functional lockout should be closed promptly once it’s open.

The RTC_SYNCPEND register's WR_PEND status bit will be 1 while any writes are held in the CORE domain. The written value will be sent to the battery-backed domain to update the battery-backed domain's register value. Once all pending write data has been sent to the battery-backed domain and all written values are saved there, then the WR_PEND status bit returns to 0.

12.7.3.3.1.1.1.4 Interrupt Clear Synchronization to DIG_ON

The ON_OFF and OFF_ON interrupts can be cleared by a write to the RTC_IRQSTATUS_SYS register. Writes to this register will be synchronized to DIG_ON regardless of the state of functional lockout.

12.7.3.3.1.1.1.5 Cross-domain Synchronization Status

The RTC_SYNCPEND register can be accessed to determine if read or write synchronization between the DIG_CORE and DIG_ON domains is in progress. The RD_PEND bit will only be 1 if the register is read very early during boot, if it is very shortly after a module-level reset, or if the RELOAD_FROM_BBD feature has been used to re-run the on-reset MMR synchronization sequence. The WR_PEND bit will be 1 if writes to On Domain registers have been made to the Write Pending MMRs since the last falling edge of the 32KHz clock.

When RD_PEND is 0, the Shadow MMRs are in sync with the ON domain MMRs. As a slight exception to this rule, reads to the RTC_SUB_S_CNT, RTC_S_CNT_LSW, and RTC_S_CNT_MSW time counter registers are handled specially depending on the value of the CNT_FMODE field of the RTC_GENRAL_CTL register. This field controls the "freeze mode" of the aforementioned time counter registers. The use of "freeze mode" is to enable atomic read of the three time counter registers by preventing updates of more significant bits between the successive reads of those registers. Two "freeze modes" are available. In the first freeze mode, S_CNT_LSW, a read to RTC_S_CNT_LSW causes the MSW register to be frozen until read. In the second freeze mode, a read to RTC_SUB_S_CNT causes both RTC_S_CNT_LSW and RTC_S_CNT_MSW to freeze until they are read.

This "freeze mode" only affects read operations. Writes to the RTC_SUB_S_CNT, RTC_S_CNT_LSW, and RTC_S_CNT_MSW registers are always handled with atomic write protection. This atomic write protection must be invoked by writing SUB_S_CNT, S_CNT_LSW, and S_CNT_MSW in that order. Other write patterns to these registers not supported for RTC.

12.7.3.3.1.1.2 DIG_ON Microarchitecture

This block is in the Battery domain, and when this IP is configured with Analog block support, it is assumed that the RTC components in this block's power domain have power applied consistently even when the rest of the SoC is powered off. This should let the time counter and the clock source for it in this power domain continue counting time while the rest of the SoC is powered off, letting the SoC maintain an accurate record of the current time even while disconnected from network and time resources on its next power-up.

Because it has a separate power domain from the rest of the chip, this domain can control power for the rest of the chip when integrated with a PMIC.

The DIG_ON block has two 63-bit time comparators to compare the configured OFF_ON and ON_OFF event timestamps to the current time counter value. Upon a match, the DIG_ON block generates an event which may cause an interrupt to the rest of the SoC. The OFF_ON event can also cause a wakeup or power-up for the SoC.

When the PWR_OFF_EN bit in RTC_GENRAL_CTL is 1, the ON_OFF event will cause the PMIC control line to toggle, powering off the chip. This could be used to trigger a scheduled power-off even while all processor cores on the chip are inactive; otherwise, when PWR_OFF_EN is 0, the ON_OFF event interrupt could trigger a core to wake up and do other processing in preparation for power off.

The DIG_ON block also processes the RTC_GENRAL_CTL.SW_OFF bit. When this bit is written, like other MMR writes in this IP, the MMR write will be transferred from the DIG_CORE to the DIG_ON domain. Upon completion of the synchronization to DIG_ON, the DIG_ON block will disable the PMIC_ENABLE signal output. This will cause an immediate power-off of the rest of the chip in the assumed power integration.

The DIG_ON block has External Wakeup events. The DIG_ON block also has configurable de-bounce timers which can set the number of 32KHz periods that the external wakeup events need to be asserted before creating a wakeup condition. These wakeup events can control the PMIC_ENABLE output in order to cause a power-up for the SoC along with event output if enabled.

The functional lockout and the dft lockout (1500) logic resides in this domain. The state of the lockout logic is persisted in this domain, but the lockout state is returned to a locked state whenever either domain is reset. When the lockout state is locked, uncontrolled power-down of the CORE domain given an always-on battery-backed domain is supported. The main memory interface and the DFT P1500 port may be in invalid states without isolation being asserted during this uncontrolled power-down scenario, but the functional lockout shall prevent any corruption of ON domain logic or state as a result of these inputs.

12.7.3.3.1.1.3 ISO_LVL Microarchitecture

The level shifters and isolation cells in this module are instanced using the tibox library. The SoC integration team can replace the full implementation of these cells with simple wires if this module is integrated without Analog support in order to save power and area. This module provides electrical safety and low-power operation when the core domain is off and battery-backed domain is on.

12.7.3.3.1.1.4 Power scenarios

When the RTC block is integrated with analog support, the different domains in the subsystem can have different combinations of power states. Typically, the DIG_CORE domain is ON if and only if the DIG_ON domain is also ON. The RTC system will lose or corrupt its battery-backed state without any indication of error if the DIG_ON domain is powered OFF while the DIG_CORE domain is ON. Refer to the SoC product's power sequencing requirements in regard to avoiding the loss of the persistent state in the DIG_ON domain.

The DIG_CORE domain can transition from the OFF state to the ON state by two methods:

1. The SoC can be powered up by external input from the power supply system, for example when a user presses a switch to turn on the system.
2. The RTC subsystem's DIG_ON domain changes its PMIC_ENABLE output from 0 to 1 and subsequently causes the power supply system to apply power. This can be caused by either the expiration of the OFF_ON timer or a signal on an enabled EXT_WAKEUP input signal.

The DIG_CORE domain can transition from the ON state to the OFF state by two methods:

1. The RTC subsystem changes its PMIC_ENABLE output from 1 to 0 and subsequently causes the power supply system to remove power. This can be caused by either the expiration of the ON_OFF timer or a write to the SW_OFF register field.
2. The power supply system autonomously removes power from the system, for example when an unexpected power loss occurs.

Note

In order to minimize the possibility of data corruption in the battery-backed domain, make sure that RTC's Functional Protection state machine is in the Locked state before turning the DIG_CORE domain OFF. Since power may be lost unexpectedly, the RTC state machine should be left Locked while not accessing RTC.

12.7.3.3.2 Timekeeping

12.7.3.3.2.1 Multiple Time Counters

The CORE domain has its own copy of the full time counter and the crystal compensation logic. Because of the rules and implementation which require that all updates to MMRs be done after the falling edge of the 32KHz clock, the time counter in the Core domain and the time counter in the Battery domain will be in sync after a write or after a post-reset synchronization.

This is because the time counter counts on the rising edge of the 32KHz clock. All synchronization between the two domains must occur between counts of the RTC in order to maintain this synchronization.

12.7.3.3.2.2 Crystal Compensation

In order to compensate for any inaccuracy of the 32768Hz oscillator, the host processor can calibrate the oscillator frequency and program a compensation value in order to adjust for any individual characteristics of the oscillator crystal. If automatic crystal compensation is enabled by programming a non-zero value to the RTC_COMP register, then some seconds are extended or shortened by a number of counts of the 32KHz clock. The compensation value is used every 4096 seconds, just before or just after letting the sub-second time counter roll over. The overall function of this is to add or subtract up to 32766 periods of the 32KHz clock from the evaluated duration of 4096 seconds. This lets the compensation add or subtract counts to deal with up to a 0.024% defect in crystal frequency, or about one second per hour.

If compensation is enabled and the sub-second time counter is about to roll over at a 4096th count of the seconds counter, then the compensation value is evaluated. If the compensation value is a positive two's complement value (0x0001 to 0x7FFE), then time will jump from (N seconds plus 0x7FFF sub-seconds) to (N+1 seconds plus COMP sub-seconds). This means that a positive compensation value makes the time value "skip forwards". The compensated sub-second count is subtracted from the next second. If the compensation value is a negative two's complement value (0x8001 to 0xFFFF), then time will "hold back" instead. In that case, time will go from (N seconds plus 0x7FFF sub-seconds) to (N seconds plus COMP[15:0] sub-seconds). The compensated sub-second count is added to the second currently in progress.

If using RTC to measure a time interval of less than two seconds, there may be an uncertainty of up to one second if the time interval includes an evaluation of the crystal compensation value. Software should be aware of the crystal compensation settings when programming the RTC OFF_ON and ON_OFF timers so that these timers expire close to the intended time instead of being affected by the compensation settings.

Note

During negative compensation when SW updates time it is possible to miss one compensation cycle.

12.7.3.3.3 Durability

The RTC module is unique in supporting a battery-backed voltage domain. Clock transmission between the two domains is necessarily complex, as well as isolating the battery-backed domain from invalid signals while the core domain changes its power state.

The battery-backed voltage domain is understood to be powered on once and left running for approximately the entire lifetime of the device powered by a standard off-the-shelf coin cell battery. The design of the battery-backed domain, which will usually include an oscillator for high-precision clock generation, is assumed to be implemented to minimize power at the expense of performance.

12.7.3.3.3.1 MMR Retention

The MMR values in the battery-backed domain are the "golden" copy of the RTC state. The RTC acts as though accesses to RTC read or write state which correspond to the values in the battery-backed domain. In order to reduce the complexity and scope of the synchronization logic, MMR accesses are only conditionally valid. Software needs to be aware of the state of certain MMRs which can indicate that certain MMR accesses would be invalid.

The RTC_SYNCPEND register needs to be read after device boot in order to ensure that the MMR Synchronization on Core Reset state machine has completed successfully. Doing any unlock or MMR writes before ensuring RD_PEND is 0 may cause a write error (signaled only by the WRT_ERR bit in the RTC_SYNCPEND register).

Generally, the MMRs stored in the battery-backed domain do not have deterministic reset values implemented in order to save area and power. On the first power-on, software will need to configure and initialize the time counter before using any RTC functionality.

12.7.3.3.3.2 Power Application

The power to RTC needs to be applied in an orderly fashion to operate correctly. The battery-backed domain should be powered on at or before when the core domain is powered on. If the battery-backed domain loses power while the CORE domain is on, then the state of the RTC time counter will be lost.

Additionally, the assertion of PMIC_ENABLE to high would be lost if the battery-backed domain lost power, and this may cause the entire SoC to lose power or reset. This would result losing in the RTC time counter state.

12.7.3.3.3.3 Functional Protection

The state of the RTC time counter must be kept safe from corruption in the event of an uncontrolled power-down scenario. Since an uncontrolled power-down may cause metastable or unexpected inputs to the battery-backed domain while the core voltage drops, some mechanism needs to be in place to prevent those transient signals from writing invalid data into the battery-backed domain.

The solution implemented by RTC is the RTC_KICK0 and RTC_KICK1 registers. In order to benefit from this functional protection, the functional protection state machine must be left in the locked state when RTC MMRs are not being written. Practically speaking, these registers make it very unlikely for the transient behavior on power loss to appear like a “KICK0+KICK1+other” MMR write sequence. This functional protection affects both P1500 and VBUS accesses.

When the power-off functionality is enabled in the RTC_GENRAL_CTL register, then writing 1 to the SW_OFF bit will re-lock the functional protection mechanism. This affects the possible write sequences when approaching the OFF condition. Writing SW_OFF also leaves RTC in a non-functional state where further operations are not possible unless the RTC CORE domain is reset with rst_mod_g_rst_n signal, or unless the power-off recovery sequence is used. Resetting the RTC CORE domain is likely to be faster than having software recover RTC from the power-down condition in many cases because the power-down recovery sequence requires a certain number of 32768Hz clock cycles to complete.

It is an error to write the unlock sequence when the functional protection mechanism is already in the unlocked state. The consequence of the error would be that the core domain and the battery domain no longer agree on the unlocked status of the functional protection mechanism. This would not be diagnosable in software and there is no recommended error recovery sequence for this condition.

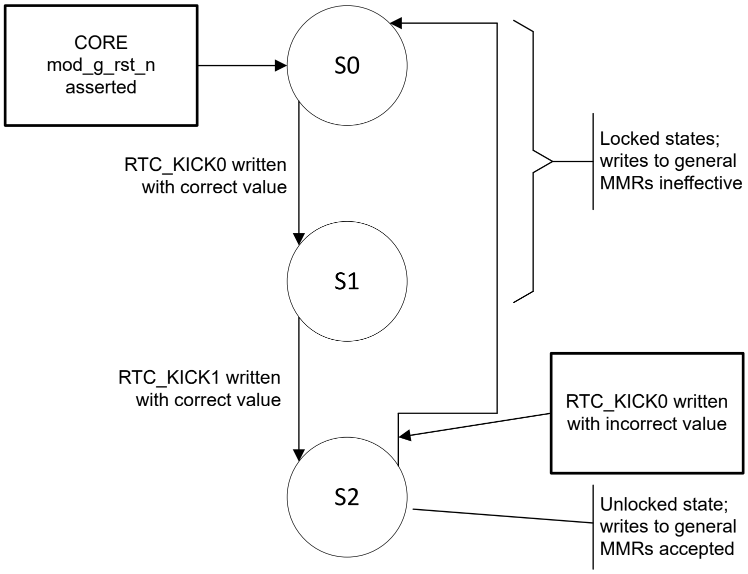

Figure 12-400. Functional Protection Lock/Unlock State Machine

12.7.3.3.3.4 Isolation

The ISO_LVL block provides electrical safety and functional correctness when the core domain is off and the battery-backed domain is on. A very low-power circuit detects if power is lost in the core domain and asserts an isolation signal which directs the cells in the ISO_LVL block to use the isolation tie-off values instead of trying to connect to the outputs from the powered-off circuitry.

However, because the power-loss-detection circuit must run with very low power, it cannot detect a loss of power early on in an uncontrolled power loss situation. A higher-power op-amp circuit would be needed to detect power loss earlier. Therefore, there is some possibility of invalid and metastable inputs being presented to the battery-backed domain through the ISO_LVL block in the case of an uncontrolled power loss situation. Data corruption in the battery-backed domain is prevented by the functional protection lockout circuit. The assertion of the isolation signal in this case prevents RTC from using too much power due to a short-circuit condition.

12.7.3.4 Programming Usage Guide

12.7.3.4.1 Single-Power-Domain Initialization

These initialization steps should be done after bringing the RTC module out of reset.

1. Unlock RTC by writing the correct values to RTC_KICK0 and RTC_KICK1.
    a. In this single-voltage-domain use case, you will never read or write these registers again after this step. This will leave the functional lockout in the unlocked state. You should ignore any steps that request any writes to RTC_KICK0 or RTC_KICK1 for this device.
2. Enable the 32KHz clock if it is not already enabled. Wait until the clock is stable before proceeding. In some SoCs, the 32KHz clock should be always running and this step can be
    a. The RTC_SYNCPEND register can be used to check if the 32KHz clock is toggling.
3. Read the RTC_SYNCPEND register and verify that the RD_PEND register is 0. Poll until RD_PEND is 0 if it is not already.
4. Write 1 to RTC_GENRAL_CTL.O32K_OSC_DEP_EN.
    a. This write must respect the timing requirements that are implied by the reset value of 0 for this register field. The RTC_SYNCPEND register should be read to observe a falling edge of the 32KHz clock based on the O32K_CLK_OBS bit.
    b. Wait for 60 microseconds in order to synchronize this register field bit.
    c. If the ana_osc32k_clk is the preferred clock for the use case, the AUX_32K_EN field of RTC_GENRAL_CTL needs to be written 0 as well.
5. Initialize the ON domain RTC MMRs in the order of increasing address offset.
    a. RTC_SUB_S_CNT
    b. RTC_S_CNT_LSW
    c. RTC_S_CNT_MSW
    d. RTC_COMP
    e. RTC_OFF_ON_S_CNT_LSW
    f. RTC_OFF_ON_S_CNT_MSW
    g. RTC_ON_OFF_S_CNT_LSW
    h. RTC_ON_OFF_S_CNT_MSW
    i. RTC_DEBOUNCE
    j. RTC_ANALOG
    k. RTC_SCRATCH0[a]
    l. RTC_GENRAL_CTL
6. Poll RTC_SYNCPEND.WR_PEND until 0.

12.7.3.4.2 Two-Voltage-Domain Initialization

These initialization steps should be done after the first power-on of the ON domain. In the two-voltage-domain integration, the durability of writes to the ON domain must be protected. All unlock/re-lock writes to RTC_KICK0 and RTC_KICK1 must be included for this device. Note you can get false WRT_ERR if you wrt before UNLOCK bit is set. To prevent this SW should always poll UNLOCK to insure it is set before Wrt to mmrs

1. Read the RTC_SYNCPEND register and verify that the RD_PEND register is 0. Poll until RD_PEND is 0 if it is not already.
2. Enable the 32KHz clock if it not already enabled.
   a. If this is done by writing registers in RTC, then this must be done by writing RTC_KICK0 and RTC_KICK1, then writing some or all of the RTC_ANALOG registers then writing zeros to RTC_KICK0 to re-lock the functional lockout.
   b. The RTC_SYNCPEND register can be used to check if the 32KHz clock is toggling.
3. Wait until the 32KHz clock is stable before proceeding.
4. Write 1 to RTC_GENRAL_CTL.O32K_OSC_DEP_EN.
   a. This write must be preceded by unlock writes to RTC_KICK0 and RTC_KICK1 and followed by a zero write to RTC_KICK0.
   b. This write must respect the timing requirements that are implied by the reset value of 0 for this register field. The RTC_SYNCPEND register should be read to observe a falling edge of the 32KHz clock based on the O32K_CLK_OBS bit.
   c. If the ana_osc32k_clk is the preferred clock for the use case, the AUX_32K_EN field of RTC_GENRAL_CTL needs to be written 0 as well at this time.
   d. Wait until RTC_SYNCPEND.WR_PEND is 0 after writing this in order to ensure that the newly activated synchronization logic is done. A fixed wait of 60 microseconds can be used instead of polling RTC_SYNCPEND.WR_PEND.
5. Initialize the ON domain RTC MMRs in the order of increasing address offset. The RTC_ANALOG registers can be omitted if initialized in an earlier step.
   a. RTC_SUB_S_CNT
   b. RTC_S_CNT_LSW
   c. RTC_S_CNT_MSW
   d. RTC_COMP
   e. RTC_OFF_ON_S_CNT_LSW
   f. RTC_OFF_ON_S_CNT_MSW
   g. RTC_ON_OFF_S_CNT_LSW
   h. RTC_ON_OFF_S_CNT_MSW
   i. RTC_DEBOUNCE
   j. RTC_ANALOG
   k. RTC_SCRATCH0[a]
   l. RTC_GENRAL_CTL
6. Poll RTC_SYNCPEND.WR_PEND until 0.

12.7.3.4.3 Read Current Time

The time counter registers span multiple 32-bit words. In order to read the time counter in an atomically consistent fashion, the time counter must be read by reading RTC_SUB_S_CNT, then reading RTC_S_CNT_LSW, and finally RTC_S_CNT_MSW.

The behavior of reading the time counter registers in this way depends on the value of RTC_GENRAL_CTL.CNT_FMODE. If the freeze mode is disabled or does not include RTC_SUB_S_CNT, then short sub-second waits may be implemented by reading RTC_SUB_S_CNT in a loop. However, in this usage, the crystal compensation feature may cause repeated, missing, or unexpected sub-second count values. The configuration of RTC should be checked if the sub-second counter is expected to be a clean, rolling binary count value.

12.7.3.4.4 Reading Other Registers

Other registers in RTC, that is, registers not part of the time counter, can be read in any order and at any time provided that RD_PEND is 0. Only 32-bit (4-byte) reads are supported on VBUSP in order to simplify the cross-domain synchronization logic.

12.7.3.4.5 Writing Registers

The procedure for writing registers in the RTC module depends on the current value of 32K_OSC_DEP_EN. This register field affects the timing requirements relevant to writing RTC registers. When this field is 0, then RTC register writes require synchronization to the 32KHz clock. When this field is 1, then RTC register writes are asynchronously enqueued for cross-domain synchronization.

If RTC_SYNCPEND.RD_PEND is 1, then it is not allowed to write any MMR in RTC.

If RTC_SYNCPEND.WR_PEND is 1, then it is not allowed to write the functional unlock sequence.

If RTC_GENRAL_CTL.UNLOCK is 1, then it is not allowed to write the functional unlock sequence.

In the two-voltage-domain integration option, then the functional lockout must be kept in a locked state whenever not actively performing writes to RTC. Leaving the functional lockout unlocked would pose a risk of corrupting the RTC time counter state in an uncontrolled power loss situation. In this case, software must also ensure that at least 61 microseconds (61 uS) elapse between a ‘lock’ and the next ‘unlock’ to occur. This delay usually naturally corresponds to two increments of the RTC sub-second field.

This IP only supports 32-bit (4-byte) writes on VBUSP in order to simplify the cross-domain synchronization logic and to reduce the number of signals which pass through the ISO_LVL sub-block.

12.7.3.4.5.1 With O32K_OSC_DEP_EN set to 0

In this mode, software must explicitly perform write operations when safe to do so. This condition needs to be ensured by specific time-sensitive code.

In this mode, write operations are safe to do immediately after a falling edge of the 32KHz clock. Software should do the following sequence in order to prepare for MMR writes in this mode.

1. Identify the MMR writes to be performed and prepare a buffer of the writes to be performed, so that a tight loop can perform the MMR writes.
2. Poll RTC_SYNCPEND until two subsequent reads see a 1 and a 0 for the value of O32K_CLK_OBS, which indicates the falling edge.
3. If required, write RTC_KICK0 and RTC_KICK1 with the unlock values.
4. Poll RTC_GENRAL_CTL.
5. Perform each MMR write in sequence. MMR writes should be done in order of increasing address offset.
6. If required, write RTC_KICK0 with zeros to lock the functional lockout.

Once these steps are completed, MMR values should be stored safely in the ON domain.

12.7.3.4.5.2 With O32K_OSC_DEP_EN set to 1

In this mode, software can perform MMR writes at any time. The MMR synchronization controller will wait until the next valid point in time for synchronizing the written values between the two domains. The WR_PEND signal will indicate whether or not synchronization is in progress.

1. Identify the MMR writes to be performed and prepare a buffer of the writes to be performed.
2. (recommended) Poll RTC_SYNCPEND.WR_PEND until it is 0. WR_PEND must be zero before writing the unlock values. Polling WR_PEND before unlock is the higher-performance approach.
3. If required, write RTC_KICK0 and RTC_KICK1 with the unlock values.
    a. (recommended) The host processor should execute a memory barrier instruction in order to flush the unlock writes before proceeding with the MMR writes to RTC.
4. Perform each MMR write in sequence. MMR writes should be done in order of increasing address offset.
5. If required, write RTC_KICK0 with zeros to lock the functional lockout.

    a. (optional) Poll RTC_SYNCPEND.WR_PEND until it is 0 to ensure that the writes are committed to the battery domain.

Once these steps are completed, RTC will synchronize the written values into the ON domain. The synchronization should take a maximum of 61 microseconds.

12.7.3.4.6 Update Current Time (drift compensation)

This sequence should be done if the current value of the time counter is inaccurate and requires adjustment.

1. If required, write RTC_KICK0 and RTC_KICK1 with the unlock values.
2. Read the RTC time counter’s full value as described above.
3. Write the RTC time counter’s full value by writing the following MMRs in the order listed.
    a. RTC_SUB_S_CNT
    b. RTC_S_CNT_LSW
    c. RTC_S_CNT_MSW
4. If crystal compensation is enabled and the drift rate/compensation values have changed since the last update operation, also write RTC_COMP with a new compensation ratio.
5. If required, write RTC_KICK0 with zeros to lock the functional lockout.

12.7.3.4.7 Update Timer Event Configuration

The ON_OFF and OFF_ON timers produce their respective events when the time counter reaches the time value stored in the MMRs associated for the timer. The timer’s MMRs must be updated in a single write action as described earlier. Updating the scratch registers and/or RTC_GENRAL_CTL.PWR_OFF_EN can be done in the same MMR write operation as the timer MMRs.

A new ON_OFF time needs to be set at least a minimum duration into the future otherwise the timer event may fail to occur. This minimum duration may be at least 2 seconds.

12.7.3.4.8 Power Off RTC

This sequence should be performed when RTC should de-assert its PMIC_ENABLE output signal. This should have the outcome of powering off the SoC. Before performing this sequence, the PWR_OFF_EN field of RTC_GENRAL_CTL must be set to 1.

1. If required, write RTC_KICK0 and RTC_KICK1 with the unlock values.
2. Optionally, write RTC_SCRATCH0 through RTC_SCRATCH7 with any updated scratch pad values.
3. Write RTC_GENRAL_CTL with SW_OFF = 1.
    a. This MMR write automatically re-locks the functional lockout. You must not do any subsequent MMR write to RTC_KICK0 or RTC_KICK1 in this case as that will prevent the correct operation of the Recovering From Power Off sequence as explained in the next section.

It is not permitted to write any register with an offset higher than the RTC_GENRAL_CTL in the same sequence as performing the write to SW_OFF. The following registers are therefore not permitted to be written in the same sequence:

1. RTC_IRQSTATUS_RAW_SYS
2. RTC_IRQSTATUS_SYS
3. RTC_IRQENABLE_SET_SYS
4. RTC_IRQENABLE_CLR_SYS
5. RTC_SYNCPEND

If these registers need to be written before performing a SW_OFF, then these register need to be written in a prior MMR write section. Software may wish to ensure that the writes are persisted by checking WR_PEND in this case.

12.7.3.4.8.1 Recovering from Power Off

After SW_OFF is performed, then RTC will be left in a state where further operations are not possible, even if a power-on is performed by the OFF_ON timer or the wakeup events. The RTC CORE domain should be reset after a power off in order to return RTC to a functional state. If this is not architecturally possible, then the following sequence can be used instead to restore functionality. This sequence takes about 100 microseconds to execute (between 3 and 4 cycles of the 32768Hz clock).

This sequence needs to be done after receiving a wakeup event that requires the device to re-enable RTC and return to full power. This sequence causes a write error. In order to return RTC to the prior state, you will also need to clear the write error.

1. After writing SW_OFF, you MUST NOT do an explicit re-lock of the RTC_KICK0 or RTC_KICK1 registers. Continue to step 2 when recovery from power off needs to be done.
2. Read the current value of RTC_GENRAL_CTL, and clear the SW_OFF bit. Write the resulting value to RTC_GENRAL_CTL. The SW_OFF bit should never read as 1, but an explicit bitmask operation to ensure that SW_OFF is written as 0 is appropriate for software clarity.
3. Poll RTC_SYNCPEND until WR_PEND reads as 0. This should take up to 1 cycle of the 32KHz clock.
4. Write RTC_KICK0 with 0 to explicitly re-lock RTC_CD.
5. Poll RTC_SYNCPEND until WR_PEND reads as 0. This should take up to 1 cycle of the 32KHz clock.
6. The preceding sequence caused a write error and leaves RTC in the locked state. To clear the write error, perform a normal write sequence to write 0x00000008 to RTC_SYNCPEND. This is an important step to return this debug field to its normal value.
7. After clearing the write error, you should also do a Reload From Battery Backed Domain operation to ensure that RTC will read the correct time value.

12.7.3.4.9 AUX_32K_EN MMR usage model

12.7.3.4.9.1 aux_32k_clk is only used

In this case, leave the reset state of AUX_32K_EN to be a 1 which will always select aux_32k_clk input.

In this mode, you cannot power off the CORE.

Also Write 1 to RTC_GENRAL_CTL.O32K_OSC_DEP_EN since this clock needs to be active.

12.7.3.4.9.2 ana_osc32k_clk will get used

In this case, SW clears AUX_32K_EN to enable the ana_osc32k_clk then initials the RTCs MMR.

Note, crystal can take time 1 to 2 Secs before it is locked on 32768 Hz. SW needs to wait until this happens before it initializes the RTCs MMR to insure clock is stable and time will advance correctly. SW can/should verify the accuracy of time and adjust if required.

The switch is 1-time event per power up of ON domain.

Also Write 1 to RTC_GENRAL_CTL.O32K_OSC_DEP_EN since this clock needs to be active.

12.7.3.4.10 Interrupt Service Routine

The following sequence should be used for the interrupt service routine.

The interrupt service routine **must** be aware of the requirement that the functional unlock sequence must not be written while the functional protection mechanism is already in the unlocked state. An appropriate mutual exclusion mechanism should be used to prevent that scenario between the normal operation of the device and the interrupt service routine.

The wakeup event generation logic is level-sensitive and not edge-sensitive. Attempts to clear the status of an EXT_WAKEUP interrupt event may appear to fail if debounce is enabled and the wakeup signal is still in the active state. This can happen because the event immediately occurs again after the event status has been cleared. If debounce of these signals is enabled, then the debounce interval must elapse before the wakeup event reaches the inactive level. Because the debounce interval can be several milliseconds, waiting for the event to deassert in an interrupt service routine might negatively affect system performance. An external wakeup event should be deactivated when responding to it in an interrupt service routine instead.

1. Read RTC_IRQSTATUS_SYS in order to identify the interrupt causes.
2. If an EXT_WAKEUP event is active, then first service the external peripheral providing the EXT_WAKEUP input.
3. If the functional protection mechanism is locked by default, perform the unlock sequence.
4. If an EXT_WAKEUP event was active, and that EXT_WAKEUP input is still active, then write the RTC_GENRAL_CTL register and clear the associated WKUP_EN bits for those external wakeup events.
5. Write RTC_IRQSTATUS_SYS in order to clear the interrupts.
6. If an EXT_WAKEUP event had its WKUP_EN bit cleared, then also disable the interrupt event for that EXT_WAKEUP event by writing to RTC_IRQENABLE_CLR_SYS.
7. Write 0 to RTC_KICK0 to re-lock the functional protection mechanism.
8. Poll RTC_SYNCPEND.WR_PEND until it is 0 to ensure that the interrupt condition is cleared before returning from the ISR.

Clearing the EXT_WAKEUP bits in the RTC_IRQENABLE_CLR_SYS register does not prevent the external wakeup event from causing a new interrupt status in the RTC_IRQSTATUS_RAW_SYS. To keep the status in RTC_IRQSTATUS_RAW_SYS clear, you must disable the wakeup event generation in the WKUP_EN field of the RTC_GENRAL_CTL register.

12.7.3.4.11 Reload from Battery Backed Domain

The RELOAD_FROM_BBD bit of the RTC_SYNCPEND register behaves specially compared to the other registers in RTC. This register bit has the following special properties:

1. It can be written 1 when RTC is in the locked state or when RTC is in the unlocked state. In other words, it can be written 1 regardless of the status of the Functional Protection state machine.
2. It can be written 1 only when all of the following bits are 0:
   a. RTC_SYNCPEND.RD_PEND
   b. RTC_SYNCPEND.WR_PEND
   c. All interrupt status bits from RTC_IRQSTATUS_RAW_SYS

In order to perform a successful RELOAD_FROM_BBD write, software should ensure that these preconditions are met and then let the operation complete before further accesses to RTC according to the following procedure.

1. Check if any interrupts are set in RTC_IRQSTATUS_RAW_SYS.
2. If any interrupt bits are set, use the steps from the previous Interrupt Service Routine section in to clear all interrupt status bits.
3. Poll the RTC_SYNCPEND register until RD_PEND and WR_PEND are both 0.
4. Write 0x80000000 to RTC_SYNCPEND to trigger the RELOAD_FROM_BBD functionality.
5. The register field RTC_SYNCPEND.RD_PEND will be set to 1 after this write. Further reads and writes must wait until RD_PEND is 0 as per other sections.

12.7.4 Timers

This section describes the Timer modules for the device.

12.7.4.1 Timers Overview

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from the TIMERn_CLKSEL registers, where n is in the instance .

In the MCU domain the device provides up to 4 timer pins, one for each instance, to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. (See *Module Integration* and the device specific datasheet to see if MCU Timers apply)

In the MAIN domain the device provides up to 11 timer pins, one for each instance, to be used as Timer Capture inputs or as Timer PWM outputs. (See device specific datasheet to see details on timer pins.)

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU_TIMER1 may be cascaded to MCU_TIMER0, etc.

When cascaded, TIMERi acts as a 32-bit prescaler to TIMERi+1, as well as MCU_TIMERn acts as a 32-bit prescaler to MCU_TIMERn+1. TIMERi / MCU_TIMERn must be configured to generate a PWM output edge at the desired rate to increment the TIMERi+1/ MCU_TIMERn+1 counter.

Figure 12-401 is an overview of the timers.

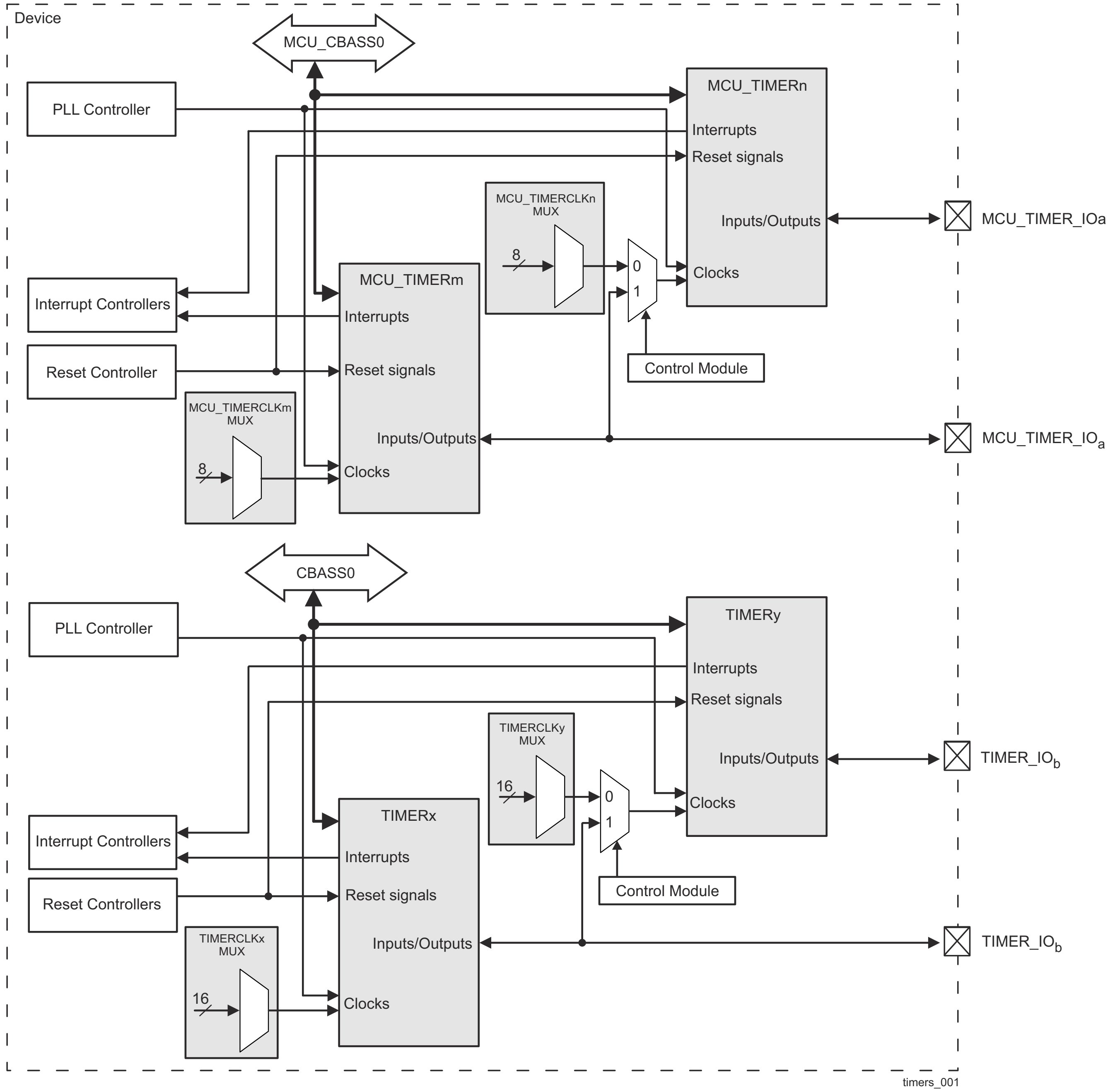

Note

m = even instances of MCU Timer. See the device datasheet for valid domains and instances.

Note

n = odd instances of MCU Timer. See the device datasheet for valid domains and instances.

Note

x = even instances of Timer. See the device datasheet for valid domains and instances

Note

y = odd instances of Timer. See the device datasheet for valid domains and instances

Figure 12-401. Timers Overview

12.7.4.1.1 Timers Features

The following are the main features of the timer controllers:

- Target interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 10-bit address bus width
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n, where n = [0-8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- Generates a 1-ms tick clock with a 32.768 kHz functional clock sourced from the LFOSC

12.7.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.7.4.2 Timers Environment

The MCU_TIMER[3-0] and TIMER[11-0] modules are hereinafter referred to as timer module.

This section describes the timers external connections (environment).

12.7.4.2.1 Timer External System Interface

Each timer can send or receive stimulus to/from the external (off-chip) system. In the device all timers are configured to output a PWM pulse or receive an external event signal used as a trigger to capture the current timer count.

Figure 12-402 shows the external system interface for the timers, and Table 12-324 describes the timer inputs and outputs.

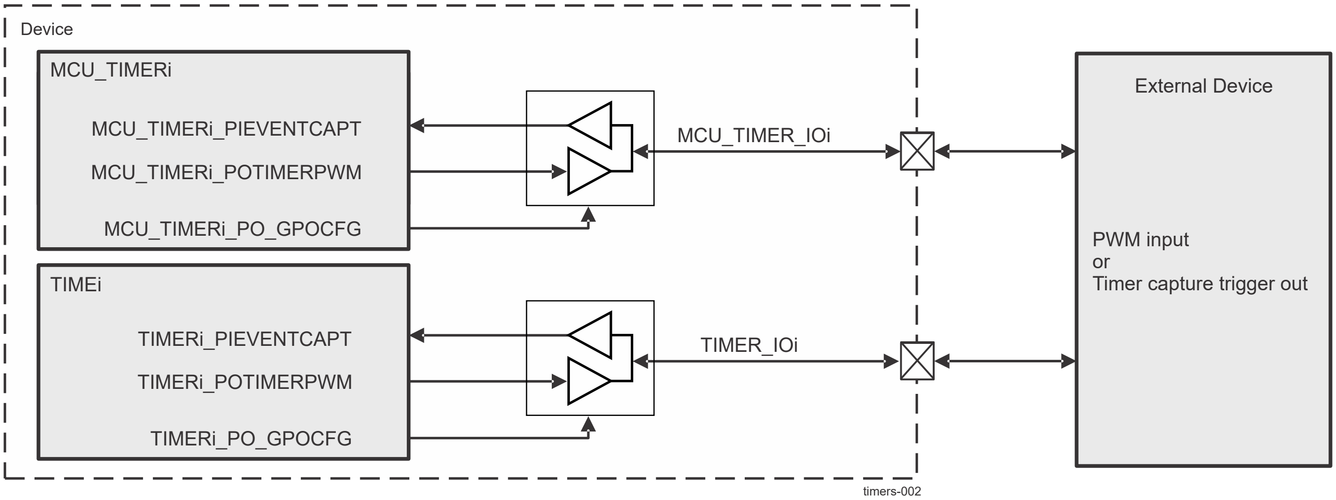

Note

i represents a TIMER instance. See the device datasheet for available domains and TIMER instances.

Figure 12-402. Timers External System Interface

Table 12-336. Timer I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		MCU_TIMERi[2]		
MCU_TIMER_IOi[2]	MCU_TIMERi[2]_PIEVENTCAPT MCU_TIMERi[2]_POTIMERPWM	I/O	MCU_TIMERi[2] trigger input or MCU_TIMERi[2] output	0
		TIMERi[2]		
TIMER_IOi[2]	TIMERi[2]_PIEVENTCAPT TIMERi[2]_POTIMERPWM	I/O	TIMERi[2] trigger input or TIMERi[2] PWM output	0

(1) When configured for that function; I = Input, O = Output

(2) i represents a TIMER instance. See the device datasheet for available domains and TIMER instances.

Note

Each MCU_TIMER_PO_GPOCFG and TIMER_PO_GPOCFG signals are used as an output enable to control the function of the MCU_TIMER_IO[3-0], and respectively TIMER_IO[11-0], as the PWM output (PO_GPOCFG = 0) or capture input (PO_GPOCFG = 1).

Note

For more information about device level signals (pull-up/down resistors, buffer type, and others), see tables *Pin Attributes* in the device-specific Datasheet.

12.7.4.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.7.4.4 Timers Functional Description

Each timer contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). Each timer includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on either an overflow or a match event. This offers time-stamp trigger signaling or PWM signal sources. A dedicated input signal can be used to trigger an automatic timer counter capture or an interrupt event on a programmable input signal transition. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line.

Each internal interrupt source can be independently enabled and disabled by a dedicated bit in the DMTIMER1MS_IRQSTATUS_SET and DMTIMER1MS_IRQSTATUS_CLR register for the interrupt features, and a dedicated bit of the DMTIMER1MS_IRQWAKEEN register for a wake-up. In addition, timers have a mechanism implemented to generate an accurate tick interrupt.

For each timer implemented in the device, there are two possible clock sources:

- 32-kHz clock (sourced from the LFOSC)
- System clock

For more information of the selection of the input clock source, see *Clocking*.

Note

Application software must ensure that DMTIMER bus interface clock frequency be greater than input clock frequency before accessing DMTIMER registers. Failure to do so will result in bus hang condition.

Each timer supports three functional modes:

- Timer mode
- Capture mode
- Compare mode

The capture and compare modes are disabled by default after core reset.

12.7.4.4.1 Timer Block Diagram

Figure 12-403 is a block diagram of the timers.

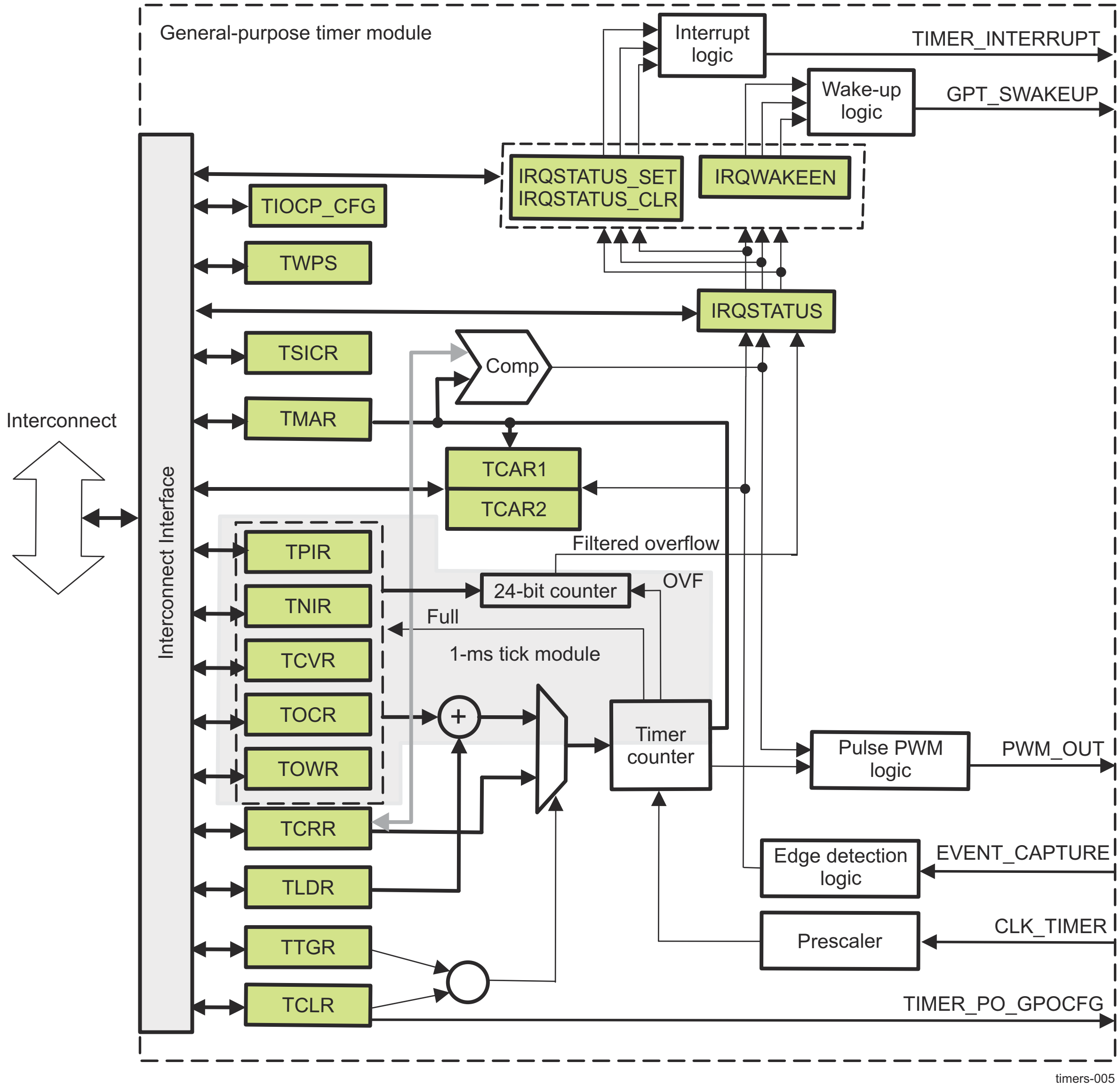

Figure 12-403. Timer Block Diagram

12.7.4.4.2 Timer Power Management

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see *Module Integration* for specifics..

The way the timer acknowledges the LPSC clock stop request is configurable through the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field.

Table 12-325 lists the IDLEMODE settings and the related acknowledgment modes.

Table 12-337. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The clock stop request is unconditionally acknowledged from the timer, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.

Table 12-337. IDLEMODE Settings (continued)

IDLEMODE Value	Selected Mode	Description
01	No-idle	The clock stop request is never acknowledged from the timer. This mode is safe from a module point of view but is not efficient from a power-saving perspective because the clocks remain active.
10	Smart-idle	The timer acknowledges the clock stop request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and interrupt requests are treated. This is the best approach to efficient system power management.
11	Smart-idleWakeup	The module behaves like in Smart-idle mode, with the exception, that it can issue a wake-up request in sleep mode, if the functional clock is not cut off.

12.7.4.4.2.1 Wake-Up Capability

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see *Timers Not Supported Features*.

If the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field sets the smart-idle mode or smart-idle with wake-up mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the clock stop acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request if configured in smart-idle with wake-up mode.

Figure 12-404 shows the wake-up request generation.

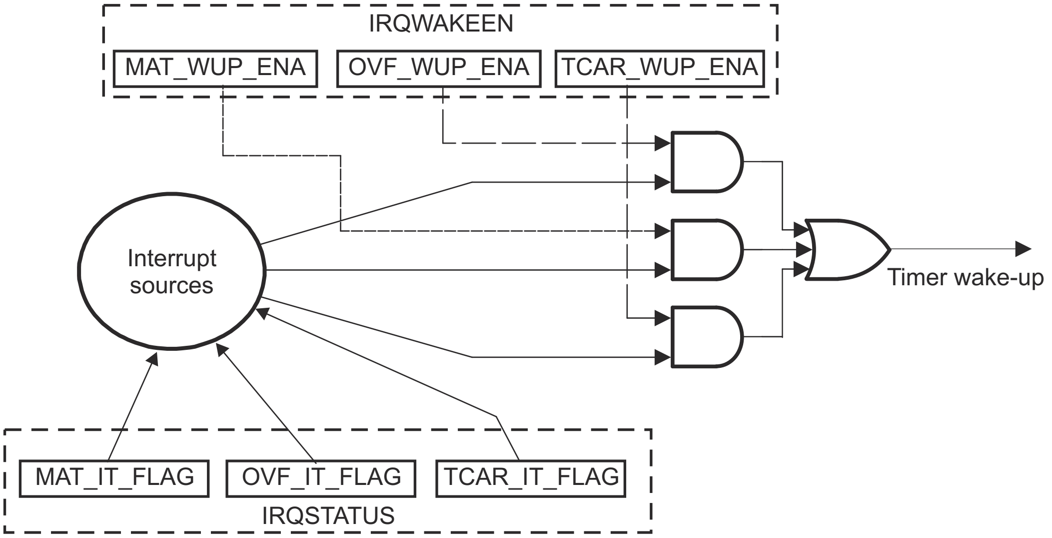

timers-006

Figure 12-404. Wake-Up Request Generation

The timer wake-up-enable register allows masking of the expected source of the wake-up event that generates a wake-up request. The register is synchronously programmed with the interface clock before the Clock magagemet sends a clock stop request. The expected source of the wake-up event is an overflow (DMTIMER1MS_TCRR), a timer match (the compare result of DMTIMER1MS_TCRR and DMTIMER1MS_TMAR matches the counter value), and a timer capture (detection of an external pulse transition of the correct polarity on the TIMER_PIEVENTCAPT).

When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS). The pending wake-up event is reset when the set status bit is overwritten with 1.

Note

The status bit must be reset to re-enter idle mode.

12.7.4.4.3 Timer Software Reset

DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit can initiate a software reset of the timer. This bit is autocleared to 0 when the reset is complete.

Before accessing or using the timer, the local host must ensure that internal reset is released by reading the DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit. This bit monitors the internal reset status.

12.7.4.4.4 Timer Interrupts

The timer can issue an overflow interrupt, a timer match interrupt, and a timer capture interrupt. Each internal interrupt source can be independently enabled and disabled in the interrupt-enable register (DMTIMER1MS_IRQSTATUS_SET) and disabled in the interrupt-disable register (DMTIMER1MS_IRQSTATUS_CLR). When the interrupt event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS).

12.7.4.4.5 Timer Mode Functionality

The timer is an upward counter that can be started and stopped at any time through the timer control register (the DMTIMER1MS_TCLR[0] ST bit). The timer counter register (DMTIMER1MS_TCRR) can be loaded when stopped or on-the-fly (while counting). DMTIMER1MS_TCRR can be loaded directly by a DMTIMER1MS_TCRR write access with a new timer value. DMTIMER1MS_TCRR can also be loaded with the value held in the timer load register (DMTIMER1MS_TLDR) by a trigger register (DMTIMER1MS_TTGR) write access. The loading of DMTIMER1MS_TCRR is done regardless of the written value of DMTIMER1MS_TTGR. The value of DMTIMER1MS_TCRR can be read when stopped or captured on-the-fly by a DMTIMER1MS_TCRR read access. The timer is stopped and the counter value is set to 0 when the module reset is asserted. The timer is maintained at stop after the reset is released.

In one-shot mode (the DMTIMER1MS_TCLR[1] AR bit is set to 0), the counter is stopped after counting overflow occurs (the counter value remains at 0).

When the autoreload mode is enabled (the DMTIMER1MS_TCLR[1] AR bit is set to 1), DMTIMER1MS_TCRR is reloaded with the value of DMTIMER1MS_TLDR after a counting overflow occurs.

CAUTION

Do not put the overflow value (0xFFFF FFFF) in the DMTIMER1MS_TLDR register because it can lead to undesirable results.

An interrupt can be issued on overflow if the overflow interrupt-enable bit is set in the timer interrupt-enable register (the DMTIMER1MS_IRQSTATUS_SET[1] OVF_EN_FLAG bit is set to 1). A dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] (PT and TRG bits) to generate one positive pulse (prescaler duration) or to invert the current value (toggle mode) when an overflow occurs. The DMTIMER1MS_TCLR[12] PT bit selects pulse/toggle modulation (the DMTIMER1MS_TCLR[11-10] TRG bit field selects trigger mode).

Figure 12-405 shows the DMTIMER1MS_TCRR timing value.

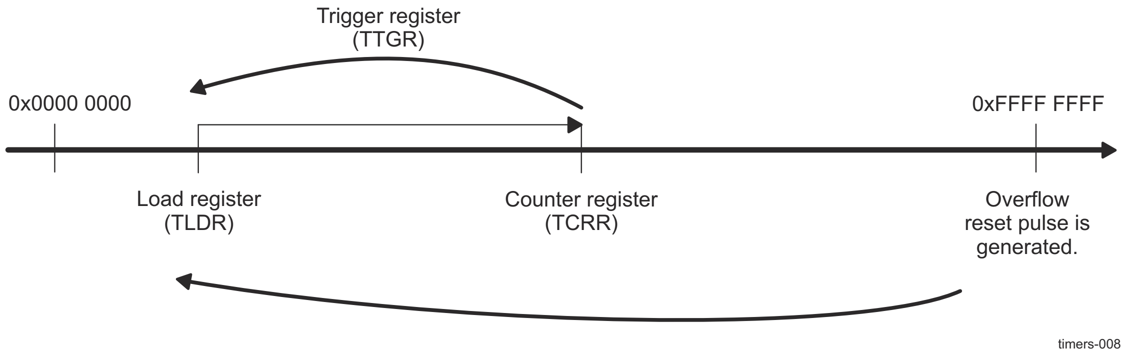

Figure 12-405. DMTIMER1MS_TCRR Timing Value

12.7.4.4.5.1 1-ms Tick Generation

The interrupt period is not exactly 1 ms, because the timer input clock is 32.768 kHz. If the clock counts up to 32, it obtains a 0.977-ms period; if it counts up to 33, it obtains a 1.007-ms period. For large granularity, the error is cumulative and can generate important deviations from the standard value.

To minimize the error between a true 1-ms tick and the tick generated by the 32.768-kHz timer, the sequencing of periods less than 1 ms and periods greater than 1 ms must be shuffled. An additional 1-ms block is used to correct this error. See Figure 12-406.

Note

The only available source for a 32.768-kHz clock is the LFOSC. The HFOSC is not capable of generating a true 32.788-kHz frequency.

In this implementation, the increment sequencing is automatically managed by the timer to minimize the error. The user must define only the value of the timer positive increment register (the DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE bit field) and the timer negative increment register (the DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE bit field). An automatic adaptation mechanism is used to simplify the programming model.

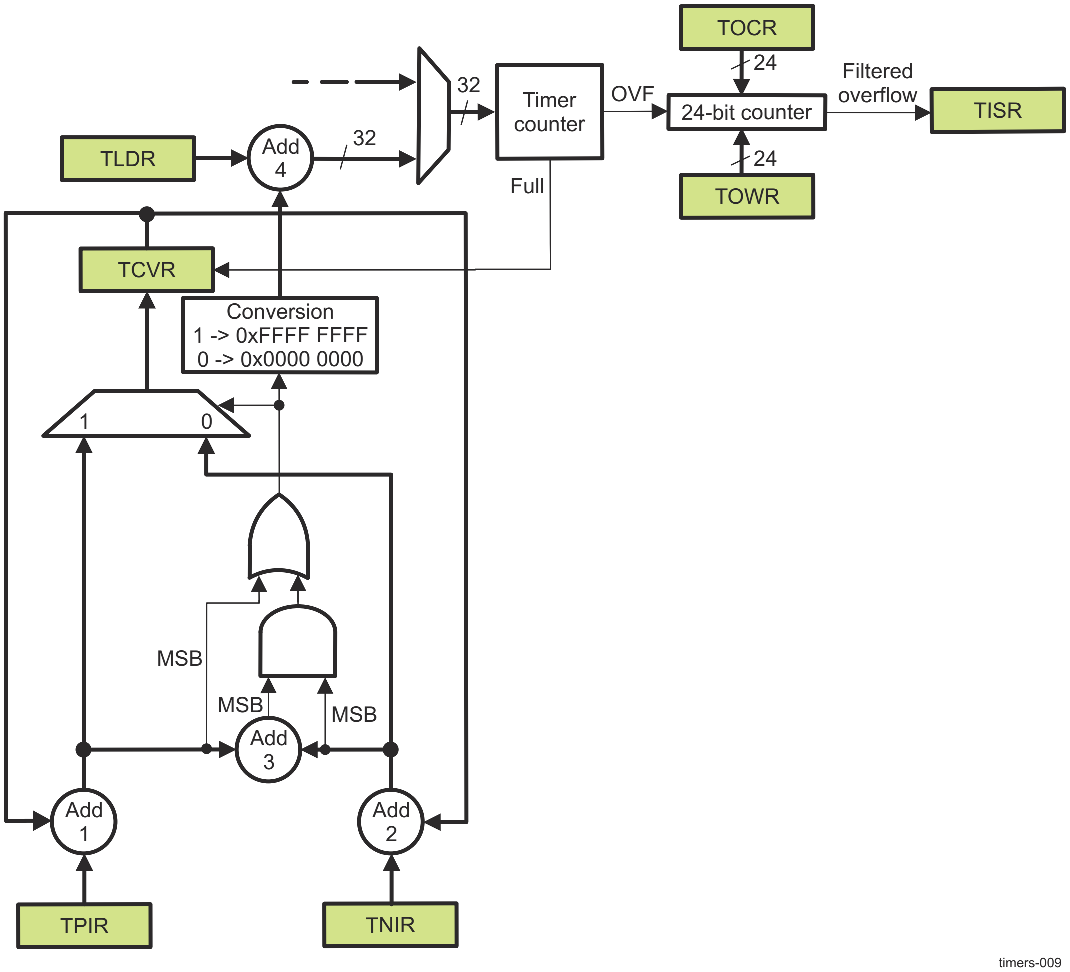

Figure 12-406. Block Diagram of the 1-ms Tick Module

The DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TCVR registers and adders Add1, Add2, and Add3 are used to define whether the next value loaded in the timer counter register (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is the value of the DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field (period less than 1 ms) or the value of DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1 (period greater than 1 ms).

Table 12-326 lists the value loaded in the DMTIMER1MS_TCRR according to the sign of the result of Add1, Add2, and Add3.

MSB = 0: Positive value; MSB = 1: Negative value

Table 12-338. Value Loaded in DMTIMER1MS_TCRR to Generate 1-ms Tick

Add1 MSB	Add2 MSB	Add3 MSB	Value of DMTIMER1MS_TCRR Register
0	0	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	0	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	0	0	N/A
1	0	1	N/A
1	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1

The values of the DMTIMER1MS_TPIR and DMTIMER1MS_TNIR registers are calculated using the following formulas:

- Positive increment value = (INTEGER[F_{clk} × T_{tick}] + 1) × 1e6) – (F_{clk} × T_{tick} × 1e6)
- Negative increment value = (INTEGER[F_{clk} × T_{tick}] × 1e6) – (F_{clk} × T_{tick} × 1e6)

Note

F_{clk} clock frequency (kHz)

T_{tick} tick period (ms)

The timer overflow counter register (DMTIMER1MS_TOCR) and the timer overflow wrapping register (DMTIMER1MS_TOWR) are used to filter interrupts. When the timer overflows, it increments the 24-bit DMTIMER1MS_TOCR. When the values in the 24-bit DMTIMER1MS_TOCR match the values in the 24-bit DMTIMER1MS_TOWR and the timer overflow is asserted, the DMTIMER1MS_TOCR is reset and an interrupt is generated to the DMTIMER1MS_IRQSTATUS register.

Note

DMTIMER1MS_TOWR has to be set to requested value. For example, if no interrupt needs to be masked DMTIMER1MS_TOWR must be set to 0, if one interrupt needs to be masked DMTIMER1MS_TOWR must be set to 1, if two interrupts need to be masked DMTIMER1MS_TOWR must be set to 2 and so on.

It is important to have in mind that the case when FFFFFF interrupts need to be masked is not possible.

With the conversion block in reset state (the positive increment register, negative increment register, and counter value register are zeroed), the programming model and the behavior of timers remain unchanged.

For 1-ms tick with a 32.768-kHz clock:

- DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE = 232,000
- DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE = –768,000
- DMTIMER1MS_TLDR[31-0] LOAD_VALUE = 0xFFFF FFE0

Note

Any value of the tick period can be generated with the appropriate value of the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TLDR.

By default, the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR and the associated logic are in reset mode (all 0s) and have no effect on the programming model.

12.7.4.4.6 Timer Capture Mode Functionality

When a transition is detected on the module input pin (PIEVENTCAPT), the timer value in the DMTIMER1MS_TCRR can be captured and saved in the DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2 register function of the mode selected in the DMTIMER1MS_TCLR[13] CAPT_MODE bit. The edge detection circuitry monitors transitions on the input pin (PIEVENTCAPT).

The rising edge, falling edge, or both, can be selected in the DMTIMER1MS_TCLR[9-8] TCM bit field to trigger the timer counter capture. The module sets the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit when an active edge is detected, and at the same time, the counter value DMTIMER1MS_TCRR is stored in timer capture register DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2, as follows:

- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and the next events are ignored (no update on the DMTIMER1MS_TCAR1 register and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG is cleared by writing 1 to it.
- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and on the second enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR2 register. If a capture interrupt is enabled, the interrupt triggers on the second event capture. All other events are ignored (no update on DMTIMER1MS_TCAR1/DMTIMER1MS_TCAR2 and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it. This mechanism is useful for period calculation of a clock, if that clock is connected to the PIEVENTCAPT input pin.

The edge detection logic is reset (a new capture is enabled) when the active capture interrupt is served. The DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it or when the edge detection mode bits (the DMTIMER1MS_TCLR[9-8] TCM bit field) are changed from no-capture mode detection to any other mode. The timer functional clock (input to prescaler) is used to sample the input pin (PIEVENTCAPT). A negative or positive pulse input can be detected when the pulse time is greater than the functional clock period. An interrupt is issued on edge detection if the capture interrupt-enable bit is set in the DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG bit. See the examples in Figure 12-407 and Figure 12-408.

In Figure 12-407, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers, and only the DMTIMER1MS_TCAR1 register updates.

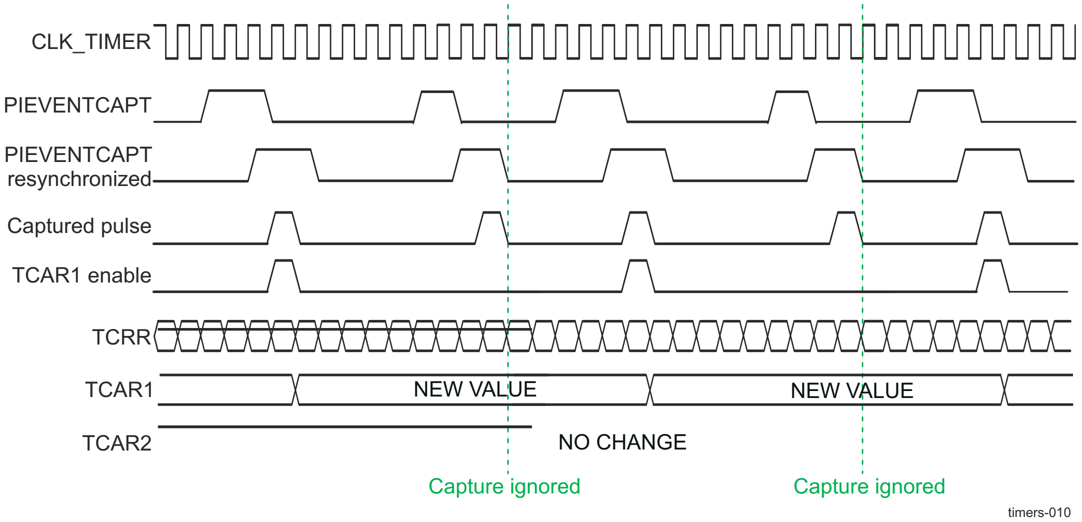

Figure 12-407. Capture Wave Example for DMTIMER1MS_TCLR[13] CAPT_MODE = 0

In Figure 12-408, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 register on the first enabled event, and the DMTIMER1MS_TCAR2 register updates on the second enabled event.

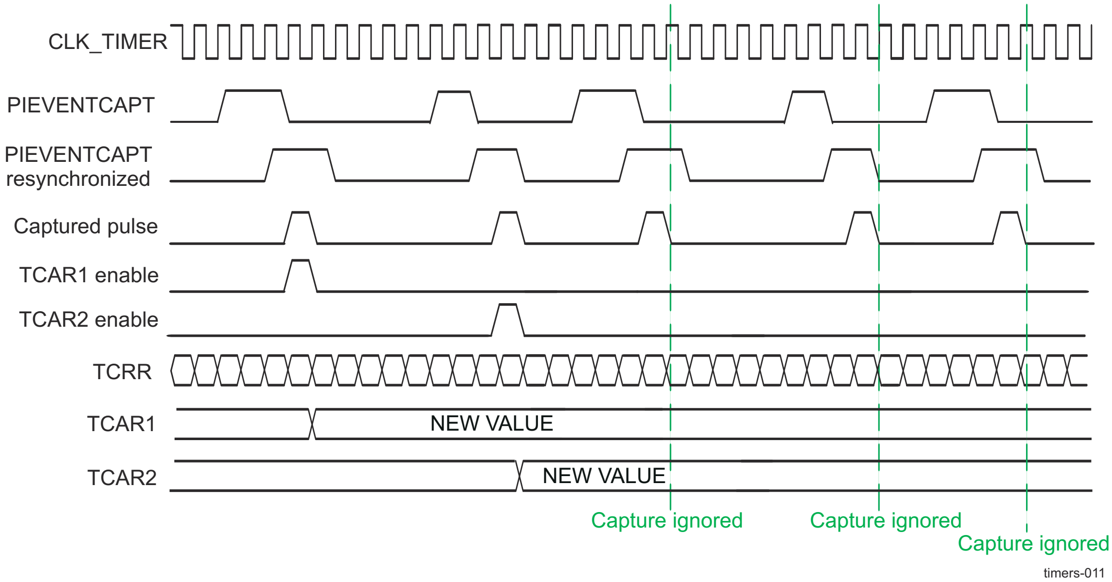

Figure 12-408. Capture Wave Example for DMTIMER1MS_TCLR[13] CAPT_MODE = 1

12.7.4.4.7 Timer Compare Mode Functionality

When the compare-enable register DMTIMER1MS_TCLR[6] CE bit is set to 1, the timer value (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is continuously compared to the value held in the timer match register (DMTIMER1MS_TMAR). The value of the DMTIMER1MS_TMAR[31-0] COMPARE_VALUE bit field can be loaded at any time (timer counting or stopped). When the DMTIMER1MS_TCRR and the DMTIMER1MS_TMAR values match, an interrupt is issued, if the DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG bit is set.

To prevent any unwanted interrupts due to reset value matching effect, write a compare value to the DMTIMER1MS_TMAR before setting the DMTIMER1MS_TCLR[6] CE bit.

The dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] TRG bit field to generate one positive pulse (timer clock duration) or to invert the current value (toggle mode) when an overflow or a match occurs.

12.7.4.4.8 Timer Prescaler Functionality

A prescaler can be used to divide the timer counter input clock frequency. The prescaler is enabled when the DMTIMER1MS_TCLR[5] PRE bit is set. The DMTIMER1MS_TCLR[4-2] PTV bit field sets the 2^n division ratio (prescaler value is $2^{(PTV + 1)}$. The prescaler counter is reset when the timer counter is stopped or reloaded on-the-fly.

Table 12-327 lists the prescaler/timer reload values versus contexts.

Table 12-339. Prescaler/Timer Reload Values Versus Contexts

Context	Prescaler	Timer Counter
Overflow (when autoreload is on)	Reset	DMTIMER1MS_TLDR[31-0]
DMTIMER1MS_TCRR write	Reset	DMTIMER1MS_TCRR[31-0]
DMTIMER1MS_TTGR write	Reset	DMTIMER1MS_TLDR[31-0]
Stop	Reset	Frozen

12.7.4.4.9 Timer Pulse-Width Modulation

The timer can be configured to provide a programmable PWM output. The timer PWM (POTIMERPWM) output pin can be configured to toggle on an event. The DMTIMER1MS_TCLR[11-10] TRG bit field determines on which register value the PWM pin toggles. Either overflow or both overflow and match can be selected to toggle the timer PWM pin when a compare condition occurs.

Note

In toggle mode, when DMTIMER1MS_TCLR[11-10] TRG = 0x2 (overflow and match), the first event that toggles the PWM line is an overflow event.

The DMTIMER1MS_TCLR[7] SCPWM bit can be programmed to set or clear the timer PWM output signal only while the counter is stopped or the trigger is off. This allows setting the output pin to a known state before modulation starts. Modulation synchronously stops when the DMTIMER1MS_TCLR[11-10] TRG bit field is cleared and overflow occurs. This allows fixing a deterministic state of the output pin when modulation stops.

In Figure 12-409, the internal overflow pulse is set each time the (0xFFFF FFFF – DMTIMER1MS_TLDR[31-0] LOAD_VALUE + 1) value is reached, and the internal match pulse is set when the counter reaches the value of DMTIMER1MS_TMAR. Depending on the value of the DMTIMER1MS_TCLR[12] PT bit and DMTIMER1MS_TCLR[11-10] TRG bit field, the timer provides pulse or PWM event on the output pin (POTIMERPWM).

The DMTIMER1MS_TLDR and DMTIMER1MS_TMAR must keep values below the overflow value (0xFFFF FFFF) by at least two units. If the PWM trigger events are both overflow and match, the difference between the values kept in the DMTIMER1MS_TMAR and the value in the DMTIMER1MS_TLDR must be at least two units. When match event is used, the compare mode DMTIMER1MS_TCLR[6] CE bit must be set.

In Figure 12-409, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 0. In Figure 12-410, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 1. To obtain the desired wave form, start the counter at 0xFFFF FFFE value (to ensure an overflow first) or adjust the line polarity (DMTIMER1MS_TCLR[7] SCPWM bit).

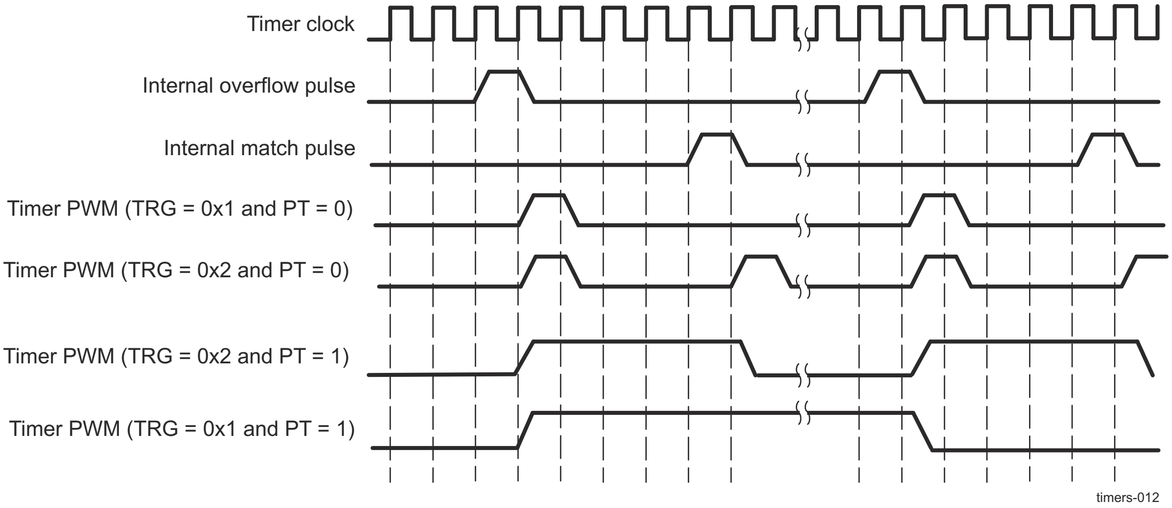

Figure 12-409. Timing Diagram of PWM With DMTIMER1MS_TCLR[7] SCPWM Bit = 0

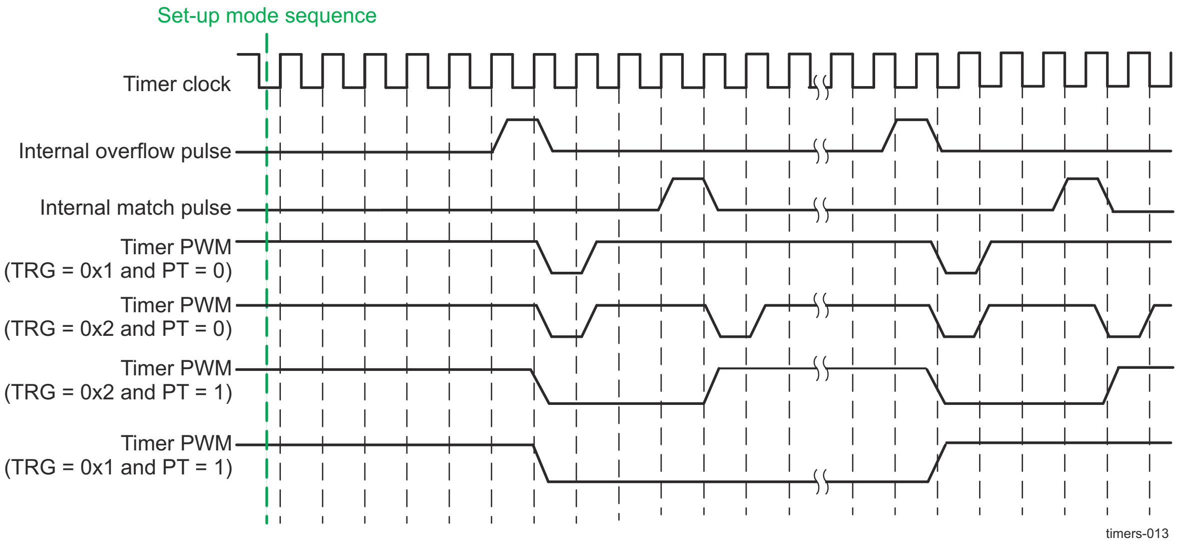

Figure 12-410. Timing Diagram of PWM With DMTIMER1MS_TCLR[7] SCPWM Bit = 1

12.7.4.4.10 Timer Counting Rate

The timer rate is defined by the following values:

- Value of the prescaler fields (the DMTIMER1MS_TCLR[5] PRE bit and DMTIMER1MS_TCLR[4-2] PTV bit field)
- Value loaded into the DMTIMER1MS_TLDR

Table 12-328 lists the prescaler clock ratio values.

Table 12-340. Prescaler Clock Ratio Values

DMTIMER1MS_TCLR[5] PRE	DMTIMER1MS_TCLR[4-2] PTV	Divisor (PS)
0	X	1
1	0	2
1	1	4
1	2	8
1	3	16
1	4	32
1	5	64
1	6	128
1	7	256

Thus, the timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – DMTIMER1MS_TLDR + 1) × (timer-functional clock period) × PS

With (timer-functional clock period) = 1/(timer-functional clock frequency) and PS = $2^{(PTV + 1)}$ if prescaler is enabled, or PS = 1 if prescaler is disabled.

CAUTION

Internal resynchronization causes any write to the DMTIMER1MS_TCLR[1] ST bit to have some latency before the register is updated:

2.5 × functional clock cycles write_DMTIMER1MS_TCLR_latency 3.5 × functional clock cycles

Remember to consider this latency whenever the timer must be started or stopped by a software change to the DMTIMER1MS_TCLR[1] ST bit.

CAUTION

- In non-PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFE.
- In PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFD.

For example, with a timer clock input of 32 kHz and the DMTIMER1MS_TCLR[5] PRE bit set to 0, the timer output period is as listed in Table 12-329.

Table 12-341. Value and Corresponding Interrupt Period

DMTIMER1MS_TLDR[31-0] LOAD_VALUE	Interrupt Period
0x0000 0000	37 h
0xFFFF 0000	2 s
0xFFFF FFF0	500 µs
0xFFFF FFFE	62.5 µs

12.7.4.4.11 Timer Under Emulation

During emulation mode, the timer continues to run according to the value of the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 1, timer execution is not stopped in emulation mode and the interrupt is still generated when overflow or match is reached.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 0, the prescaler and timer are frozen and both resume on exit from emulation mode. The asynchronous external input pin (MCU_TIMER_IO[9-0] or TIMER_IO[7-0]) is internally synchronized on two timer-clock rising edges.

12.7.4.4.12 Accessing Timer Registers

All accesses are posted mode, under the assumption that freq(timer clock) < freq(interface clock)/4, until software reconfiguration. In addition, it is not recommended to access the timer registers prior to the PLLs generating the timer and interface clocks have been configured and the clocks have stabilized. All registers are 32 bits wide, accessible through the configuration interface with 32-bit access (read/write).

Write operations to the following functional registers must be complete (the MSB must be written even if the MSB data is not used):

- DMTIMER1MS_TCLR
- DMTIMER1MS_TCRR
- DMTIMER1MS_TLDR
- DMTIMER1MS_TTGR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

The following registers are not affected by the posted/nonposted mode selection; the write/read operation is effective and acknowledged (command accepted) after one interface clock cycle from command assertion:

- DMTIMER1MS_TIDR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_RAW
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TWPS
- DMTIMER1MS_TSICR

12.7.4.4.12.1 Writing to Timer Registers

The host uses the configuration interface to write to the following registers synchronously with the timer interface clock:

- DMTIMER1MS_TLDR
- DMTIMER1MS_TCRR
- DMTIMER1MS_TCLR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TTGR
- DMTIMER1MS_TSICR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

12.7.4.4.12.1.1 Write Posting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 1 (default value).

This mode uses a posted write scheme to update any internal register (DMTIMER1MS_TCLR, DMTIMER1MS_TCRR, DMTIMER1MS_TLDR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR). Therefore, the write transaction is immediately acknowledged on the configuration interface, although the effective write operation occurs later because of a resynchronization in the timer clock domain. The advantage is that neither the interconnect, nor the device that requested the write transaction is stalled.

For each register, a status bit is provided in the timer write-posted status (DMTIMER1MS_TWPS) register. In this mode, it is mandatory that software check this status bit before any write access. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice.

The timer module updates the value of the timer counter register synchronously with the interface clock. Consequently, any read access to DMTIMER1MS_TCRR does not add any resynchronization latency; the current value is always available.

Note

Because the overflow IRQ is generated when the value of DMTIMER1MS_TCRR reaches 0xFFFF FFFF, and not when it changes its value to the value after overflow, it is necessary to wait a delay of (1 × PS × timer functional clock period) before any read access to DMTIMER1MS_TCRR to ensure a correct reading of its content.

Note

If DMTIMER1MS_TTGR register is written during a posted write to DMTIMER1MS_TCRR, the value to be written to DMTIMER1MS_TCRR will be discarded.

If a posted write to DMTIMER1MS_TCVR is started, the user must not write to DMTIMER1MS_TPIR or DMTIMER1MS_TNIR before the DMTIMER1MS_TCVR write is finished, because the value of DMTIMER1MS_TCVR is re-evaluated, so both the value to be written, and the recalculated value will be discarded.

If a write access is pending for a register, reading from this register does not yield a correct result. Software synchronization must be used to avoid incorrect results.

Functional frequency range: freq(timer clock) < freq(interface clock)/4.

12.7.4.4.12.1.2 Write Nonposting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 0. It uses a nonposted write scheme to update any internal register. Therefore, the write transaction is not acknowledged on the configuration interface until the effective write operation occurs after the resynchronization in the timer functional clock domain. The drawback is that the interconnect and the device that requested the write transaction are stalled during this period.

The same full resynchronization scheme is used for a read transaction, and the same stall period applies. A register read following a write to the same register is always coherent.

This mode is functional regardless of the ratio between the configuration interface frequency and the timer clock frequency.

12.7.4.4.12.2 Reading From Timer Counter Registers

Note

LSB/MSB accesses cannot be interleaved (that is, the sequence LSB register 1, LSB register 2, MSB register 1, MSB register 2 is not supported).

The DMTIMER1MS_TCRR is a 32-bit “atomic datum” and its 16-bit capture is done on the 16-bit LSB first to allow atomic LSB16 + MSB16 capture. This capture scheme is also performed for the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers as they can be changed due to internal processes too.

12.7.4.4.12.2.1 Read Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. The recommended functional frequency range is freq(timer) < freq(interface clock)/4.

Read posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x1 or DMTIMER1MS_TSICR[3] READ_MODE is set to 0. This mode uses a posted-read scheme for reading any internal timer register. The read transaction is immediately acknowledged on the configuration interface, prior to the value to be read has been resynchronized. With this method, neither the interconnect nor the device that requested the read transaction are stalled.

Read posted mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which needs resynchronization from functional to interface clock domains.

Note that in Posted mode, if the DMTIMER1MS_TCRR is read immediately after wake-up and the interface clock is off during idle state, then it is possible to get an old value from just before going to idle state due to the fact the interface clock is needed for synchronization.

In order to avoid this situation, another synchronization mechanism is used for the first read operation after idle state. The DMTIMER1MS_TSICR[4] READ_AFTER_IDLE bit is used to enable/disable the mechanism.

When the synchronization mechanism is disabled (READ_AFTER_IDLE bit is set to 1), first read transaction takes only 2 interface clock cycles, but the read value of DMTIMER1MS_TCRR could be wrong.

When the synchronization mechanism is enabled (READ_AFTER_IDLE bit is set to 0), first read value of DMTIMER1MS_TCRR is correct, but the read transaction takes more than 2 interface clock cycles.

12.7.4.4.12.2.2 Read Non-Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. Recommended functional frequency range is freq(timer) >= freq(interface clock)/4.

Read non-posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1. This mode uses a non-posted read scheme for reading internal timer registers. The read transaction is not acknowledged on the configuration interface until the effective read operation occurs, after the resynchronization in the timer clock domain. The result is that both the interconnect and the device that requested the read transaction are stalled during this period.

This mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which need resynchronization from functional to interface clock domains.

12.7.4.4.13 Timer Posted Mode Selection

A choice between two synchronization modes is made taking into account the frequency ratio and the stall periods that can be supported by the system, without impacting the global performance.

The posted mode selection applies only to registers that require synchronization on or from the timer clock domain. For write operation, the registers affected by posted and non-posted selection are DMTIMER1MS_TCLR, DMTIMER1MS_TLDR, DMTIMER1MS_TCRR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR. For read operation, the registers affected by this selection are: DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR.

The interface clock domain synchronous registers DMTIMER1MS_TIDR, DMTIMER1MS_TIOCP_CFG, DMTIMER1MS_IRQSTATUS, DMTIMER1MS_IRQSTATUS_SET, DMTIMER1MS_IRQWAKEEN, DMTIMER1MS_TWPS, and DMTIMER1MS_TSICR are not affected by posted and non-posted mode selection. The operation (read or write) is effective and acknowledged after one interface clock cycle from the command assertion.

The configuration of posted or non-posted mode can be changed (overwritten) by software by writing in DMTIMER1MS_TSICR[2] POSTED bit. The DMTIMER1MS_TSICR[3] READ_MODE defines how the read operation is performed when the module is configured in non-posted mode (see DMTIMER1MS_TSICR). The following cases are possible:

- DMTIMER1MS_TSICR[2] POSTED = 0x1 and DMTIMER1MS_TSICR[3] READ_MODE = x (don’t care): read and write operations are expected in posted mode.
- DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x0: the write operation is executed in non-posted mode and read is executed in posted mode.

- DMTIMER1MS_TSICR[2]POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1: write is executed in non-posted mode and read is executed in non-posted mode.

12.7.4.5 Timers Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

12.7.4.5.1 Timer Global Initialization

12.7.4.5.1.1 Main Sequence – Timer Module Global Initialization

Table 12-330 identifies the main steps for initializing the timer module when the module is to be used for the first time.

Table 12-342. Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x1
Wait until reset release?	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x0
Configure idle mode.	DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE	0x-
Enable wake-up interrupt events.	DMTIMER1MS_IRQWAKEEN[2-0]	0x-
Select posted mode.	DMTIMER1MS_TSICR[2] POSTED	0x-

12.7.4.5.2 Timer Operational Mode Configuration

12.7.4.5.2.1 Timer Mode

12.7.4.5.2.1.1 Main Sequence – Timer Mode Configuration

Table 12-331 lists the steps in the timer mode configuration.

Table 12-343. Timer Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable overflow interrupt.	DMTIMER1MS_IRQSTATUS_SET[1] OVF_EN_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer load value.	DMTIMER1MS_TLDR	0x-
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.7.4.5.2.2 Timer Compare Mode

12.7.4.5.2.2.1 Main Sequence – Timer Compare Mode Configuration

Table 12-332 lists the steps in the timer compare mode configuration.

Table 12-344. Timer Compare Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable match interrupt.	DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer compare value.	DMTIMER1MS_TMAR	0x-
Enable compare mode.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.7.4.5.2.3 Timer Capture Mode

12.7.4.5.2.3.1 Main Sequence – Timer Capture Mode Configuration

Table 12-333 lists the steps in the timer capture mode configuration.

Table 12-345. Timer Capture Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Initialize capture mode.	See Section 12.7.4.5.2.3.2 .	
Enable capture interrupt.	DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1
Detect event.	See Section 12.7.4.5.2.3.3 .	

12.7.4.5.2.3.2 Subsequence – Initialize Capture Mode

Table 12-334 lists the steps to initialize capture mode.

Table 12-346. Initialize Capture Mode

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select TIMER[11-0] or MCU_TIMER[3-0] Capture input at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x1
Select single or second event capture.	DMTIMER1MS_TCLR[13] CAPT_MODE	0x-
Select transition capture mode.	DMTIMER1MS_TCLR[9-8] TCM	0x-

12.7.4.5.2.3.3 Subsequence – Detect Event

Table 12-335 lists the steps in detecting an event.

Table 12-347. Detect Event

Step	Register/Bit Field/Programming Model	Value
Wait until event detected?	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	= 0x1
Read timer capture value.	DMTIMER1MS_TCAR1 and/or DMTIMER1MS_TCAR2	
Clear capture interrupt request.	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	0x1

12.7.4.5.2.4 Timer PWM Mode

12.7.4.5.2.4.1 Main Sequence – Timer PWM Mode Configuration

Table 12-336 lists the steps in the timer PWM mode configuration.

Table 12-348. Timer PWM Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select trigger output mode.	DMTIMER1MS_TCLR[11-10] TRG	0x-
Select pulse or toggle modulation PWM mode.	DMTIMER1MS_TCLR[12] PT	0x-
Select TIMER[11-0] or MCU_TIMER[3-0] PWM output at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x0
Configure PWM output pin default value.	DMTIMER1MS_TCLR[7] SCPWM	0x-

Table 12-348. Timer PWM Mode Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Load timer load value.	DMTIMER1MS_TLDR	0x-
Load timer compare value.	DMTIMER1MS_TMAR	0x-
Enable compare.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.8 Internal Diagnostics Modules

This section describes the internal diagnostics modules in the device.

12.8.1 Dual Clock Comparator (DCC)

This section describes the Dual Clock Comparator (DCC) modules in the device.

12.8.1.1 DCC Overview

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has instances of DCC modules.

Figure 12-411 shows the DCC modules overview.

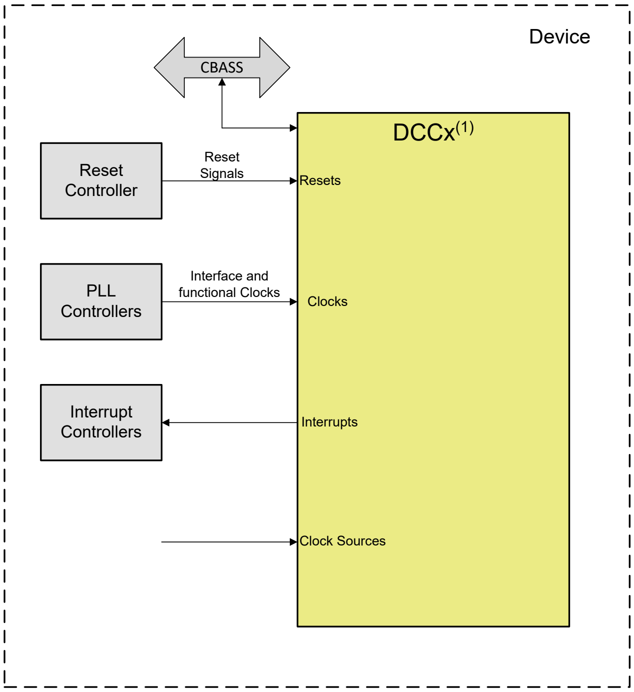

1. x represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-411. DCC Modules Overview

12.8.1.1.1 DCC Features

The DCC uses two independent clock sources to detect when one is out of specification. Each DCC module implements the following features:

- Two independent counter blocks count clock pulses from each clock source
- Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
- Configurable timebase for error signal
- Error signal generation when one of the clocks is out of specification
- Clock frequency measurement

12.8.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.8.1.2 DCC Functional Description

The DCC module supports two selectable clock sources for Counter0 and Counter1. Figure 12-412 shows the DCC functional block diagram.

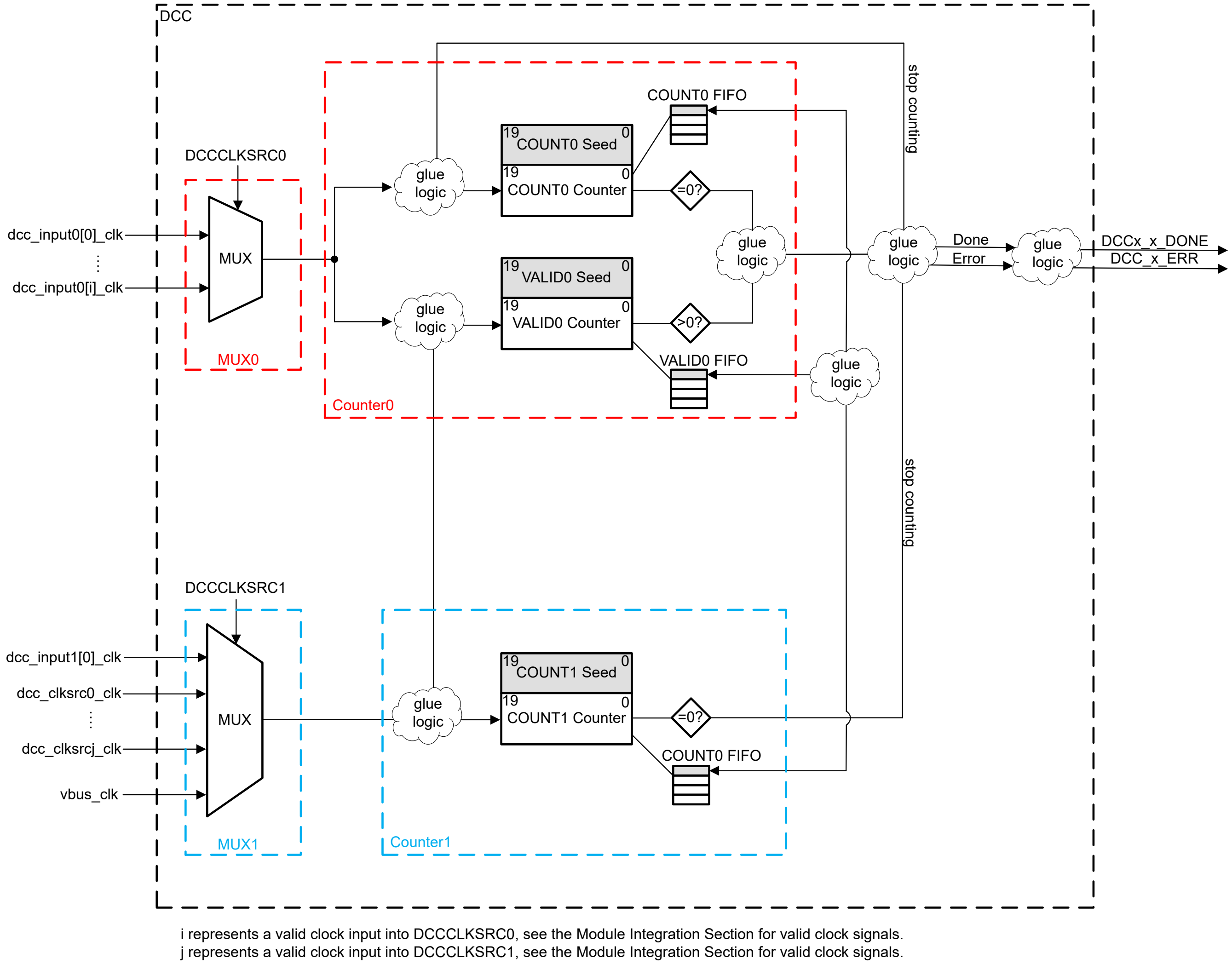

i represents a valid clock input into DCCCLKSRC0, see the Module Integration Section for valid clock signals.
j represents a valid clock input into DCCCLKSRC1, see the Module Integration Section for valid clock signals.

Figure 12-412. DCC Functional Block Diagram

12.8.1.2.1 DCC Counter Operation

Note

For detailed DCC compute calculations, refer to Continuous Monitor of the PLL Frequency With the DCC App Note.

The DCC has two parallel counters that count clock pulses for two independent clock sources:

- Counter0 generates a fixed-width counting window (VALID0) after a pre-programmed number of pulses (COUNT0). The values for VALID0 and COUNT0 can be programmed in DCC2_DCCVALIDSEED0 and DCC2_DCCCNTSEED0 registers respectively.
- Counter1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses (COUNT1). This pulse sets an error signal if Counter1 does not reach 0 during the time when VALID0 is running. The seed value for COUNT1 can be programmed in DCC2_DCCCNTSEED1 register.

The error signal is generated by any one of the following conditions:

- Clock1 expires before the COUNT0 reaches 0.
- Clock1 expires after both COUNT0 and VALID0 reach 0.
- Clock1 not present.
- Clock0 not present.

Any of these errors causes the counters to stop counting. An application must then read out the counter values to determine what caused the error. Once the error is detected, the counters are stopped after 3 FICLK and 2 source clock cycles due to the cross clock domain synchronisation.

Reloads or restarts occur under two conditions:

- The module is reset or restarted through software (that is, software starts the module after reset, or software checks an error condition and decides to restart the module).
- COUNT0, COUNT1, and VALID0 all reach 0 without error.

CAUTION

The DCC module does not check jitter for Clock0 or Clock1.

As the counter preset signal is synchronized to either of the source clock domains, the counters begin downcounting after two corresponding source clock cycles.

The error signal is captured to the FICLK domain. There is 1 FICLK period uncertainty on either side of the fixed width counting window (VALID0) in generating the error signal since the counters work in different clock domains. This should be accounted for when setting the count value for VALID0.

Figure 12-413 through Figure 12-417 shows examples of counters relationship and error generation.

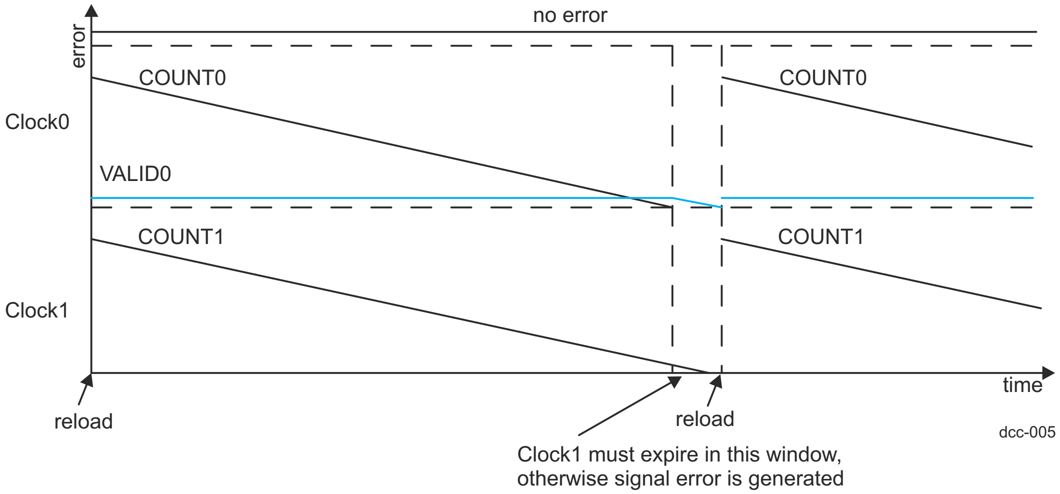

Figure 12-413. DCC Clock0 and Clock1 With no Error

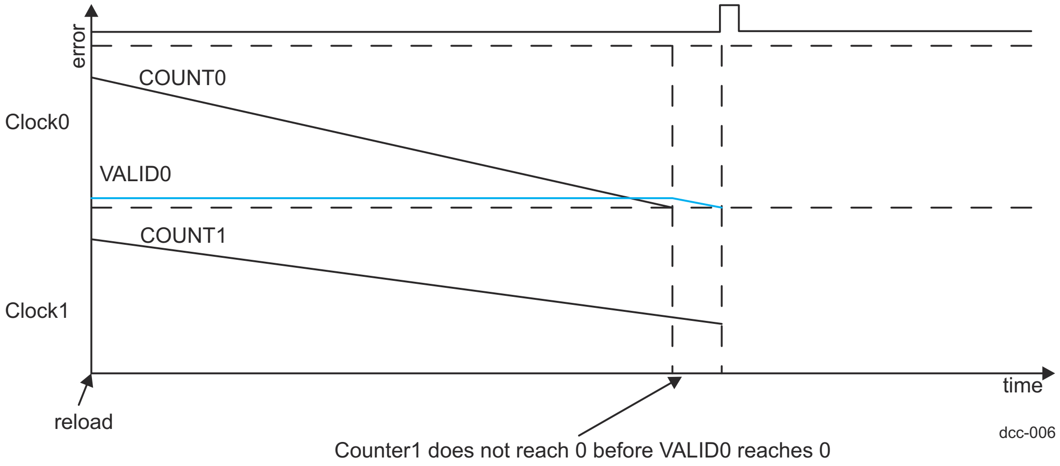

Figure 12-414. DCC Clock1 slower than Clock0 results in an error and stops counting

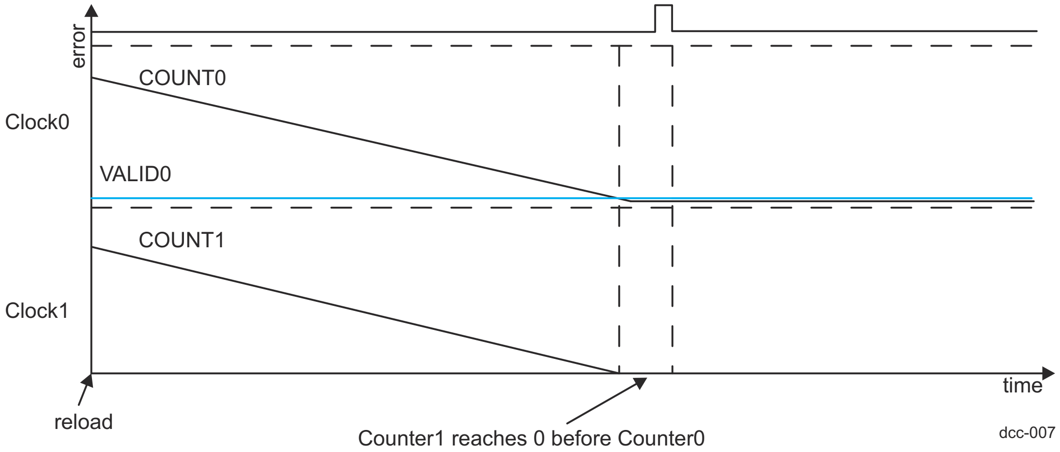

Figure 12-415. DCC Clock1 faster than Clock0 results in an error and stops counting

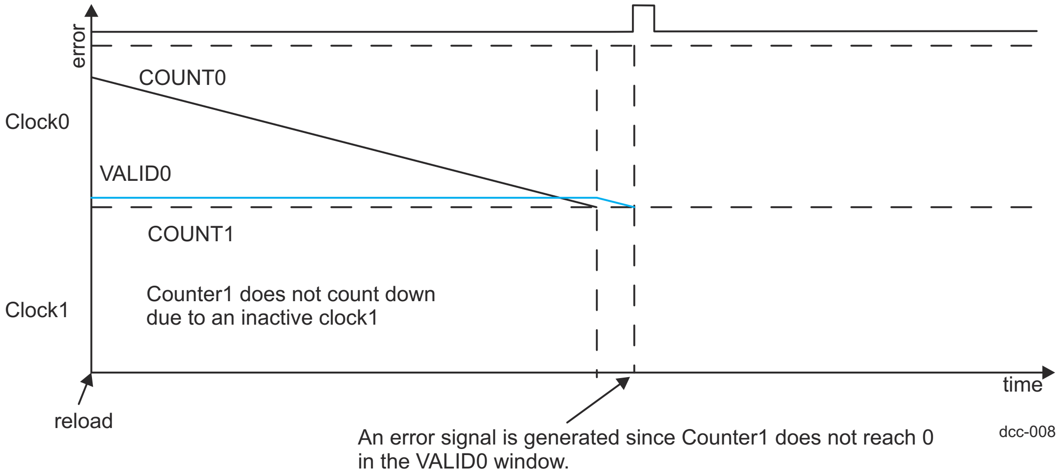

Figure 12-416. DCC Clock1 not present results in an error and stops counting

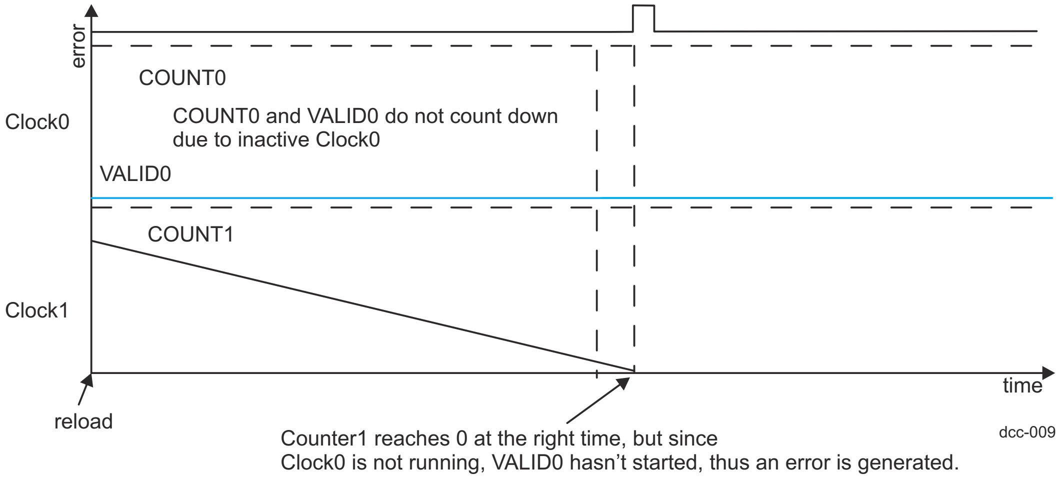

Figure 12-417. DCC Clock0 not present results in an error and stops counting

12.8.1.2.2 DCC Low Power Mode Operation

The DCC module does not function in Low Power Mode. It is the responsibility of software to stop the module before entering low power mode and to restart the module after exiting low power mode.

12.8.1.2.3 DCC Suspend Mode Behavior

The DCC module will continue running regardless of the state of emulation. All registers are readable via emulation reads.

12.8.1.2.4 DCC Single-Shot Mode

The DCC can be programmed to count down one time using single-shot mode. In this mode, the DCC stops operation when both COUNT0 and VALID0 reach 0.

At the end of one sequence in single-shot mode the DCC2_DCCGCTRL[3-0] DCCENA bitfield is set to disabled, which stops further counting. Single-shot mode is enabled from the DCC2_DCCGCTRL[11-8] SINGLESHOT bitfield.

At the end of one sequence in single-shot mode, if there is no error which stops counting, then the done status bit is set in the DCC2_DCCSTATUS[1] DONEFLG bitfield and a done interrupt DCC_x_INT is generated. Software must clear the done bit before restarting the counting.

12.8.1.2.5 DCC Continuous mode

When DCC runs in continuous mode both the counts shall get reloaded with seed value upon completion of counts without error. If the counts end in error DCC stops the operation and counts are not reloaded.

12.8.1.2.5.1 DCC Continue on Error

During debug, if there are events which are causing clocks to be anomalous over short period covering more than one evaluation window then it would be important to capture trajectory of error event and period around such event. To allow capturing the successive error events DCC can be programmed to continue after error. [3-0] CONT_ON_ERR shall be set to value other than "0101" to enable this mode. It is recommended to write "1010" to avoid single soft errors.

12.8.1.2.5.2 DCC Error Count

DCC also counts the number of error pulses generated since reset or since last time the error count is cleared. This is read/write register for CPU to clear when new trace of number of errors is required to be maintained.

12.8.1.2.6 DCC Control and count hand-off across clock domains

As the counters run in two different selectable clock domains and the register interface runs on the fixed bus clock domain, control signals and counter value hand-off have synchronizers implemented. These add to the margins of error while comparing the counts.

1. With all three counts synchronized to FICLK domain for comparison error detection there is delay in terms of FICLK domain.
2. Based on the error signal, the enable for the counters is synchronized back to the respective clock domains of the counters, which adds latency in terms of clock periods which are different, this would create a skew between start of count. Depending upon frequency ratios of the clocks used, the difference between two could vary.

Application needs to consider the worst case delay differences while measuring the clocks.

12.8.1.2.7 DCC Error Trajectory record

Once the clock errors out, the host can read the counter values to determine the extent of error to analyze type of failure. For short window comparisons this would become difficult, specially if there are back to back errors due to some transient event. Secondly, for random events which can cause an interrupt during the critical phase of application running, then event if not recorded may get overwritten and also not provide meaningful trace of error.

12.8.1.2.7.1 DCC FIFO capturing for Errors

DCC provides the FIFO for capturing COUNT0, VALID0, and COUNT1 information which captures all three counts upon "Error" event. For "Done" event no results are captured by default.

12.8.1.2.7.2 DCC FIFO in continuous capture mode

To track the VALID0 counter values regardless of "Error" or not, FIFOs can be configured to capture the count for each compare window. This is useful in validation and characterization exercise. [11-7] FIFO_NONERR control when set to value other than "0101" this mode is set; it is recommended to write "1010" to avoid single soft errors. Note, this capture is applicable only in continuous mode and not in single shot mode.

12.8.1.2.7.3 DCC FIFO Details

The FIFO is 4 deep for each count and updates new count information for all the non-full FIFOs. Information is updated on every configured trigger of error or cycle completion. If full, the next values are not written till at-least one entry is read. Application owns responsibility to read the FIFOs uniformly to keep synchronisation between three entries of the FIFO. Both empty and full indications for individual FIFOs is provided through the .

12.8.1.2.7.4 DCC FIFO Debug mode behavior

Upon debug access, the FIFO pointers should not advance hence not impacting the functional behavior. This requirement is same as other functional blocks in the device.

12.8.1.2.8 DCC Count read registers

DCC has provision to read the counts during operation. This is performed using , , and registers. Read from these registers in default mode allows reading the present value of count. This is useful when in single shot mode or mode where DCC stops upon error.

These registers can be used to read the FIFO through the [7-4] FIFO_READ configuration. Reads on the empty FIFO shall provide the contents of last pointed location. Application shall track the empty/full conditions of the FIFOs to track the count records consistently.

Regardless of FIFO_READ configuration, the FIFO internally keeps updating records based on configured triggers till full.

12.8.2 Error Signaling Module (ESM)

This section describes the Error Signaling Module (ESM) in the device.

12.8.2.1 ESM Overview

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

Figure 12-418 shows the ESM modules overview.

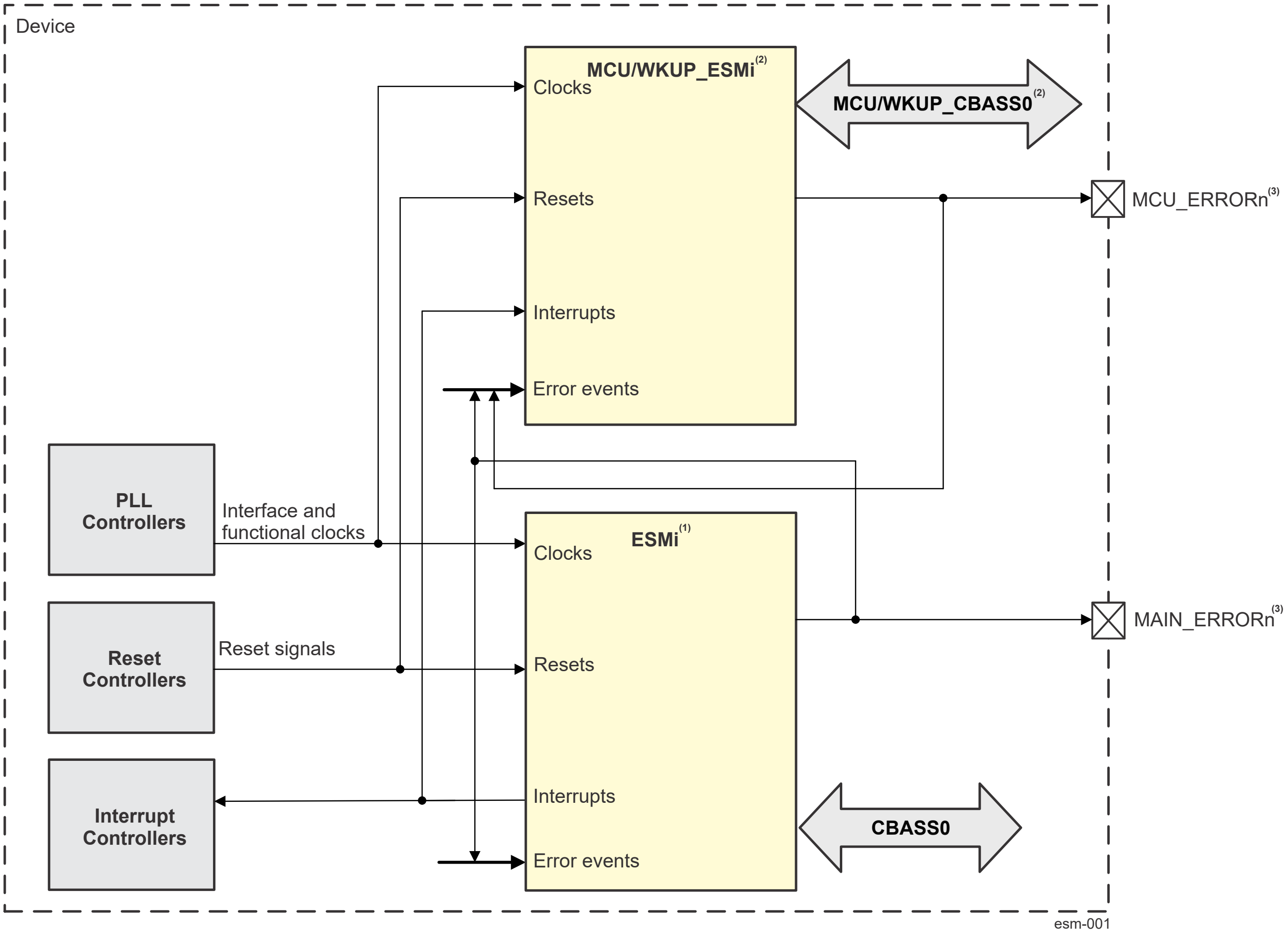

1. i represents a valid instance of ESM in a domain. Consult the device datasheet for available domains and ESM instances.
2. i represents a valid instance of ESM in a MCU or WKUP domain. Consult the device datasheet for available domains and ESM instances.
3. Not all pins are valid for all devices. Consult the device datasheet for specifics.

Note

The MAIN_ERRORn pin, if valid, is used for observation only.

Figure 12-418. ESM Modules Overview

12.8.2.1.1 ESM Features

Each ESM module implements the following features:

- Up to 1024 error event inputs
  - Implemented in groups of 32 events
  - Level or Pulse inputs (Pulse inputs are triple redundant)
- Selectable low and high priority interrupt error pin prioritization of each error event
- Error pin to signal severe device failure
  - Support of level or PWM modes
- Configurable timebase for error signal
- Error forcing capability
- Internal redundant flops on critical fields

12.8.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.8.2.2 ESM Environment

The MCU_ESM0 and ESM0 modules are hereinafter referred to as ESM module.

This section describes the ESM external connections (environment).

Figure 12-419 shows the ESM pins used for typical connections with external devices.

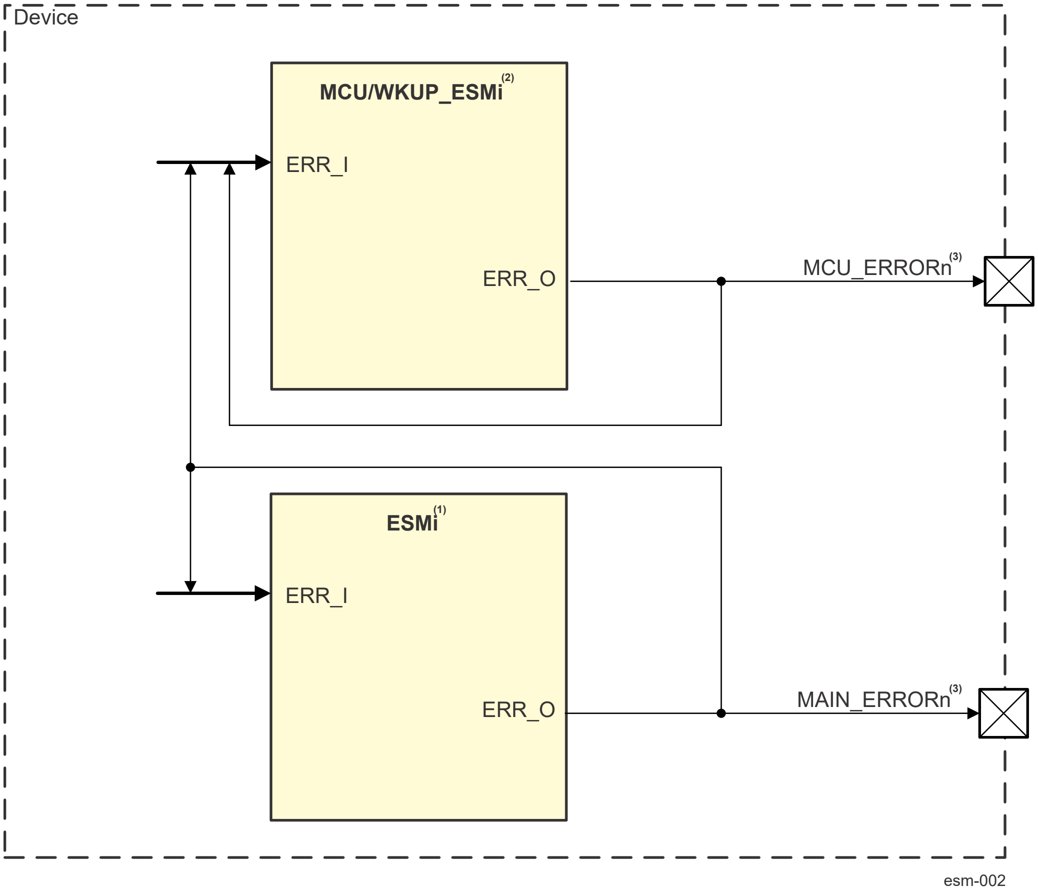

1. i represents a valid instance of ESM in a domain. See the device specific datasheet for available domains and ESM instances.
2. i represents a valid instance of ESM in a MCU or WKUP domain. See the device specific datasheet for available domains and ESM instances.
3. Not all pins are valid. See the device datasheet for specifics.

Note

The MAIN_ERRORn pin, if valid, is used for observation only.

Figure 12-419. ESM Modules Environment

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.8.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.8.2.4 ESM Functional Description

The Error Signaling Module (ESM) centralizes fault reports. It provides mechanisms to classify errors by severity and to provide programmable error response. The error classification in the ESM is determined by programmed configuration for each individual error input. For each individual error input the configuration can be set to assert an output error pin, or generate an interrupt to a CPU, or both. When an individual error input is configured to generate an interrupt, the configuration will also select whether the interrupt that is generated will be one of high priority or low priority.

By reporting the faults in a central location, the system may determine what caused the fault and what action can be taken. In general, the faults can be split into two categories:

- Corrected faults
- Non-corrected faults

The ESM reports errors in two ways:

- An interrupt to a processor in the device. This allows the device to analyze and try to recover from an error.
- An external ERROR pin. This allows the system outside of the SoC to monitor for potentially fatal errors(errors that the device cannot self-recover from). Moreover, the external I/O (ERROR pin) can operate in level or PWM modes. In level mode, the output will remain asserted (active low) for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin will go inactive (high). If it does not go inactive in that time, then an external agent should intervene, as there may be an unrecoverable error. In PWM mode, the error will cause the output pin to maintain its value for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin will continue the PWM pattern. If it does not go inactive in that time, then an external agent should intervene, as there may be an unrecoverable error.

Both mechanisms can be used at the same time for the same fault, signaling both an interrupt and the external ERROR pin. This allows the device to attempt to recover, but if it fails, then the external system is still alerted. If it succeeds, then it can remove the ERROR pin assertion so that the external system knows that a potentially unsafe condition was avoided.

Lastly, the ESM does not specify any methods of intervention, only the process of alerting internal CPUs and external monitor(s) of an existing error event.

Figure 12-420 shows the ESM module block diagram. Note that not all instances may be pinned out in the device. For more information, see Section 12.8.2.2 , *ESM Environment*.

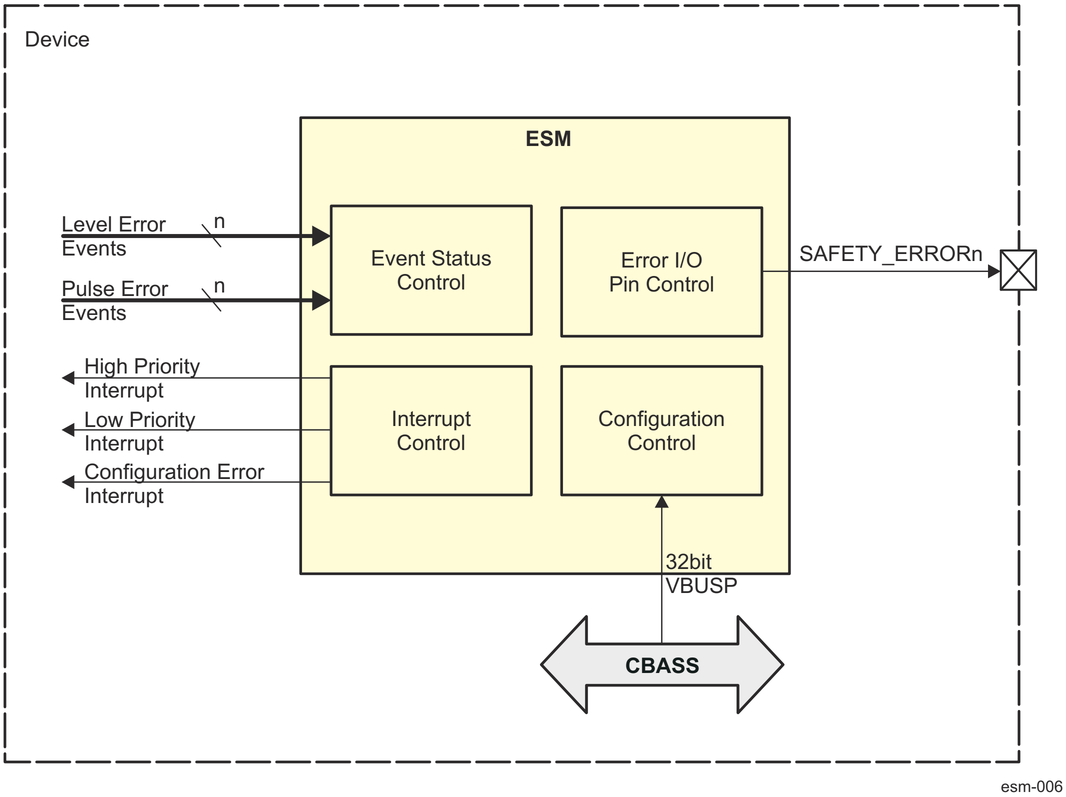

Figure 12-420. ESM Block Diagram

12.8.2.4.1 ESM Interrupt Requests

The ESM module generates three output interrupts to the device interrupt controllers:

- Configuration error interrupt (see Section 12.8.2.4.1.1)
- High priority error interrupt (see Section 12.8.2.4.1.2)
- Low priority error interrupt (see Section 12.8.2.4.1.3)

The error interrupt outputs are provided so that a processor in the device can be signaled to intervene when an error event occurs. Each error event input can be enabled, via software, to cause an error interrupt to occur (via the ESM_INTR_EN_SET_j register). Additionally, each error event input can be programmed to influence either the low priority (default) interrupt or the high priority interrupt (via the ESM_INT_PRIO_j). The low priority interrupt is intended for events that are of interest, but do not require immediate intervention. For example, an indication that there was a single bit error that was corrected may signal a low priority interrupt, so that information can be collected for statistical purposes. A high priority interrupt is intended for events that need immediate attention. For example, an indication that there was an uncorrected two-bit error may be signaled as a high priority interrupt.

12.8.2.4.1.1 ESM Configuration Error Interrupt

The configuration error interrupt (ESM_INT_CFG_LVL_0) indicates that there is an inconsistency in the configuration of one (or more) error group *j* registers (MMRs).

In such inconsistency in the internal copies of any of the MMRs caused by fault associated with error group *j*, the corresponding raw status will be set in the ESM_ERR_RAW register. If the corresponding bit is enabled in the ESM_ERR_EN_SET register, a configuration error interrupt will be triggered.

When a configuration error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_ERR_STS register to determine which group has a configuration error
2. Write the correct values to the following group registers:

Note

If there has been a configuration error, the values in the below registers cannot be guaranteed to be correct anymore. Therefore, software should maintain a copy of the correct values prior to an error to ensure that they can be re-programmed with the correct configuration.

   a. ESM_INTR_EN_SET_j
   b. ESM_INTR_EN_CLR_j
   c. ESM_INT_PRIO_j
   d. ESM_PIN_EN_SET_j
   e. ESM_PIN_EN_CLR_j
3. Service any pending interrupts in steps 4, 5, and 6 below

Note

The raw status of any pending interrupts may be inconsistent. Servicing the interrupt will return it to consistency via the error group ESM_RAW_j register.

4. Write 0x1 to the appropriate bits in the ESM_ERR_STS register. This step will clear the raw status
   a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
   b. If there are no additional errors, the level interrupt will go low
5. Write the end of interrupt vector to the ESM_EOI register
   a. If there are additional configuration error interrupts pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional low priority error interrupts pending, there will be no new pulse.

12.8.2.4.1.2 ESM Low Priority Error Interrupt

Events mapped to the low priority error interrupt (ESM_INT_LOW_LVL_0) are intended to be events of interest that should be addressed eventually, not events that require immediate attention. An example would be an event indicating a corrected error. The system may want to track this for statistical purposes, but it does not require immediate attention.

Any error event can be mapped to the low priority error interrupt. A low priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j register) and mapped to the low priority error interrupt (via ESM_INT_PRIO_j register) and the raw status is set (via the ESM_RAW_j register).

When a low priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_LOW_PRI register
   a. If both [31-16]PLS and [15-0]LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
   b. If either [31-16]PLS or [15-0]LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
      i. First option: Record the value in [31-16]PLS and [15-0]LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority low priority error event

Note

The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

      ii. Second option:

        1. Read the ESM_LOW register to determine which event group(s) have pending low priority error interrupts
        2. Read the desired error group *j*ESM_STS_j register
        3. Identify which low priority interrupt to service

2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
    a. The system may take several actions including (but not limited to):
        i. Fixing the error
        ii. Resetting the errored IP peripheral
        iii. Resetting the device
        iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.8.2.4.1.2.1) or pulse (see Section 12.8.2.4.1.2.2) event.

12.8.2.4.1.2.1 ESM Low Priority Error Level Event

When a low priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the low priority error level event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status
    a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
    b. If there are no error events, the level will de-assert

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

3. Write the end of interrupt vector to the ESM_EOI interrupt register
    a. If there are low priority error level events enabled and pending, then a new pulse will be generated
    b. If there are no additional low priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.8.2.4.1.2.2 ESM Low Priority Error Pulse Event

When a low priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
    a. If there are additional low priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
    b. If there are no additional low priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM

4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.8.2.4.1.3 ESM High Priority Error Interrupt

Events mapped to the high priority error interrupt are intended to be events that require immediate intervention from the system because a potentially dangerous error has occurred. An example would be an event indicating an uncorrected error. The system will want to diagnose the issue and intervene to ensure there are no violations.

Any error event can be mapped to the high priority error interrupt. A high priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j) register and mapped to the high priority interrupt (via the ESM_INT_PRIO_j) register and the raw status is set (via the ESM_RAW_j).

When a high priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_HI_PRI register
    a. If both [31-16] PLS and [15-0] LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
    b. If either [31-16] PLS or [15-0] LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
        i. First option: Record the value in [31-16] PLS and [15-0] LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority high priority error event.

            Note

            The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

        ii. Second option:
            1. Read the ESM_HI register to determine which event group(s) have pending high priority error interrupts
            2. Read the desired error group *j*ESM_STS_j register
            3. Identify which high priority error interrupt to service

2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
    a. The system may take several actions including (but not limited to):
        i. Fixing the error
        ii. Resetting the errored IP peripheral
        iii. Resetting the device
        iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.8.2.4.1.3.1) or pulse (see Section 12.8.2.4.1.3.2) event.

12.8.2.4.1.3.1 ESM High Priority Error Level Event

When a high priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the error event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status

  a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
  b. If there are no error events, the level will de-assert

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

---

3. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error level events enabled and pending, then a new pulse will be generated
   b. If there are no additional high priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register, but may be done regardless as an extra CLEAR is not harmful.

12.8.2.4.1.3.2 ESM High Priority Error Pulse Event

When a high priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional high priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.8.2.4.2 ESM Error Event Inputs

The ESM can have up to 1024 error event inputs, configurable by groups of 32. For the mapping of system interrupt error events to ESM interrupt inputs, see *Interrupt Sources*.

Level error events (active high) are synchronized to the ESM clock. This synchronized value is captured in to a flop.

Pulse error events use rising edge detection. Each pulse error event has 3 redundant inputs. Each input has its own edge detection logic. Multiple transmission protects against Single Event Upsets (SEUs, transient errors) causing a pulse to be lost during transmission and against failure of the edge detection logic. Once an edge has been detected on any of the three inputs, the ESM_RAW_j status is set. Subsequent pulses are likely to come concurrently or quickly enough that software will not have reacted yet. This logic is intentionally biased against false negatives and towards false positives. An SEU that causes an event where none actually occurred will cause software to be called in to action. Software must observe that there is no real error and clear the false status.

12.8.2.4.3 ESM Error Pin Output

The error pin output (ERR_O) is used to signal an external agent that it needs to (or may need to) intervene because of an error. Each error event input can be programmed, via software, to influence the error pin output (via the ESM_PIN_EN_SET_j register). The error pin output is active low or PWM based on the ESM_EN[7-4] PWM_EN field. This bit field should only be modified when the ESM is disabled, based on the ESM_EN register.

During Power-On Reset (POR), the error pin is active (asserted low) and the device drives this via a weak internal pull-down. The I/O is under the control of the device. When POR is removed from the ESM, it will be driving the error pin so the device can hand over control to the ESM. The user may also add an external pull-down that is only active when the device is in reset.

During a warm reset the state of the error pin is unchanged, that is the error pin logic is only reset by a POR. The device leaves the I/O active during a warm reset.

The ESM has also a software error forcing capability on the error pin. That is, a force error can be set via the ESM_EN[3-0] KEY bit field.

CAUTION

The isolation value for the ERR_O output of ESM is active (0). This is intended and supposed to protect against an accidental transition to a low power state. If the actual low power mode transition is intended, the PMIC should be made aware by software to ignore the ESM error signal. Otherwise device resets will be asserted from companion chip.

Figure 12-421 describes the behavior of the error pin. Not shown is that a reset (Power-On-Reset only) will immediately transition the error pin to the ESM_RESET state and a Global Soft Reset will immediately transition the error pin to the ESM_IDLE state. A pending error interrupt event is any error event with the raw state set and the error pin Influence enabled. There are two types of "clear" events associated with servicing the error pin. The first is to clear the status of the pending event (see Section 12.8.2.4.1 for how to clear level and pulse pending events). The second is the CLEAR event meant to de-assert the error pin.

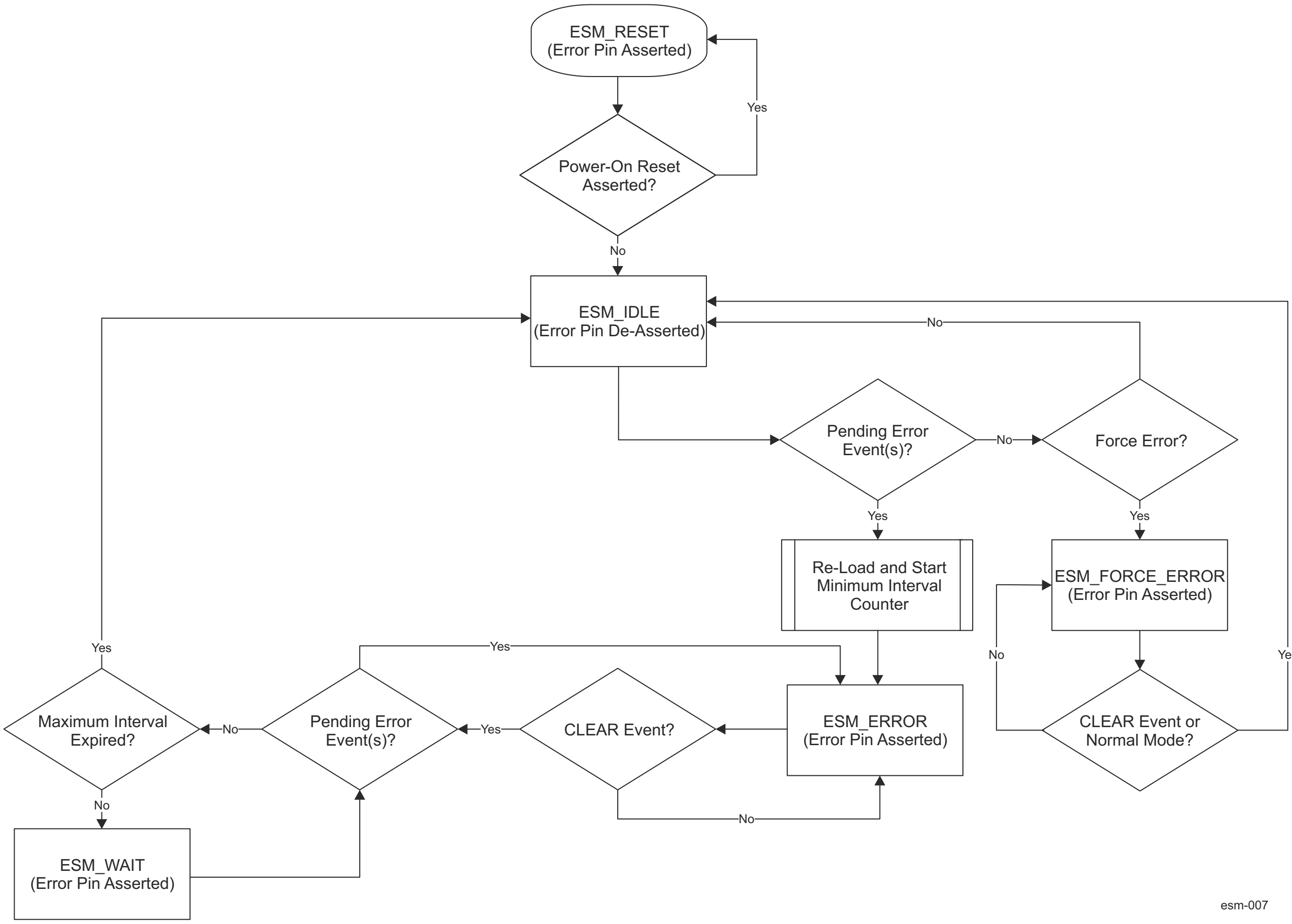

Figure 12-421. ESM Error Pin State Flowchart

If an error event happens that has been programmed to influence the error pin, the error pin will assert (active low) for a minimum time (as programmed by the ESM_PIN_CNTR_PRE register). In order for the error pin to de-assert, the following 3 things must happen:

1. The minimum time interval must expire
2. The event that caused the error pin to assert must be cleared (see Section 12.8.2.4.1)
3. A CLEAR (0x5) must be written to the ESM_PIN_CTRL register.

Note

Step 3 should happen after step 2, but either (or both) of these steps may happen before or after step 1.

Figure 12-422 shows a typical error pin assertion.

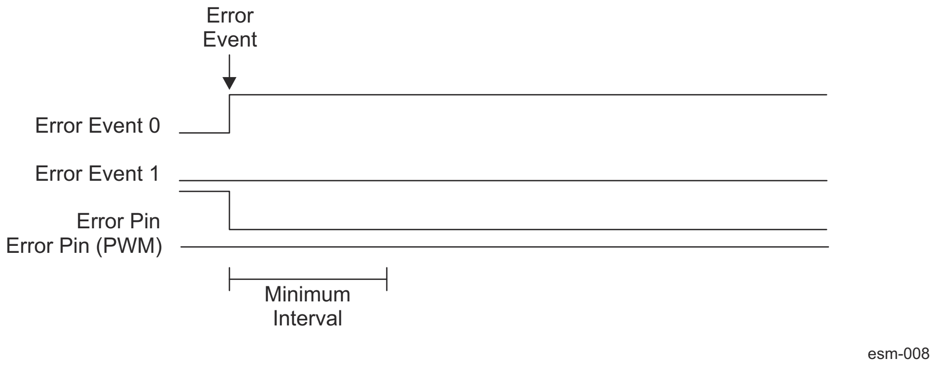

Figure 12-422. ESM Error Pin Assertion

If, during the minimum time, CLEAR is written to the error key, then the error pin will de-assert after the minimum time interval, as shown in Figure 12-423.

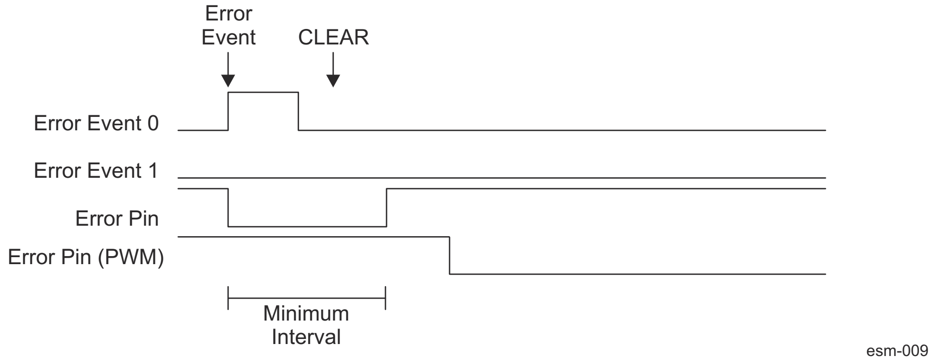

Figure 12-423. ESM Error Pin Assertion with CLEAR during Minimum Interval

If CLEAR is not written till after the minimum time interval, the error pin will de-assert when CLEAR is written. This is regardless of whether the error interrupt event itself is removed before or after the minimum time interval, as shown by the dotted line in Figure 12-424.

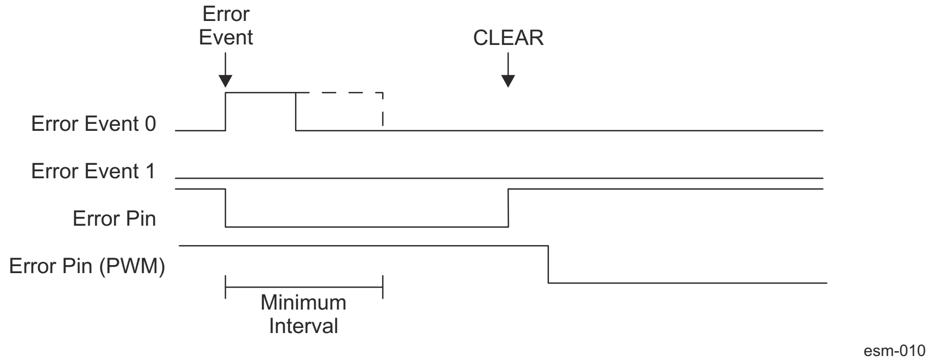

Figure 12-424. ESM Error Pin Asserting with CLEAR after Minimum Interval

When in the ESM_ERROR state and a CLEAR event happen, if there are still pending error events, the ESM stays in the ESM_ERROR state with the error pin asserted. Multiple error events when in the ESM_ERROR state do not reset the minimum time interval counter as shown in Figure 12-425.

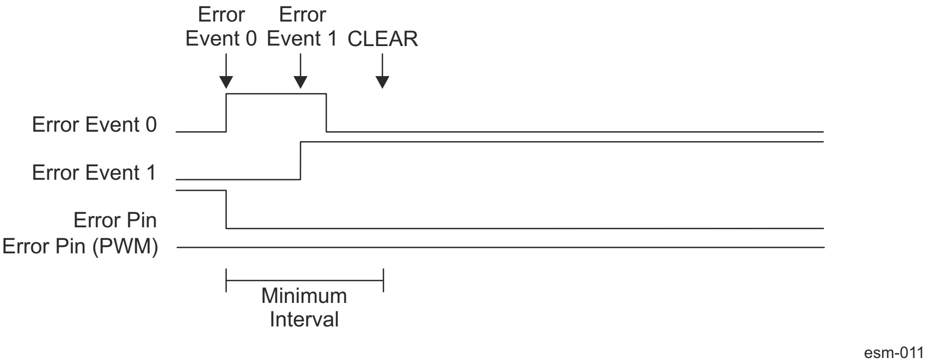

Figure 12-425. ESM Error Pin Asserting with Interval Reset by Additional Error Event(s)

A CLEAR event causes a re-evaluation of whether there are any pending error events. As such, a single CLEAR can be used to clear the error pin after multiple error events. Multiple CLEAR events can occur (such as the one with the dotted arrow shown in Figure 12-426), but are not necessary. No matter how many error events occur nor when (or how many) CLEAR events occur, the error pin will always be asserted for at least the minimum time interval

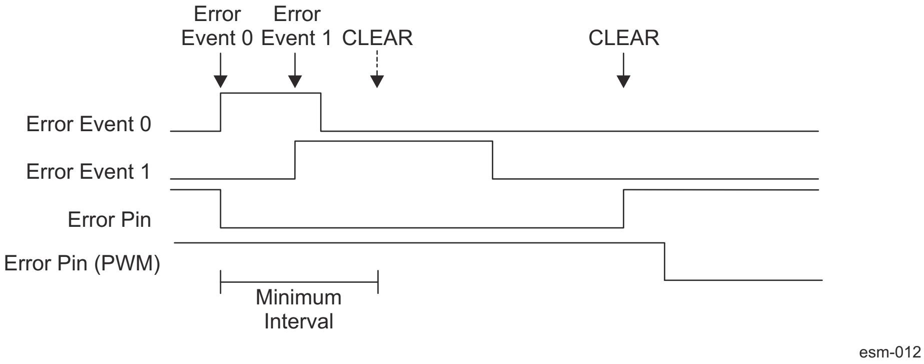

Figure 12-426. ESM Error Pin Asserting with Single CLEAR for Multiple Events

If all error events are cleared and the ESM is in the ESM_WAIT state, waiting for the minimum time interval to expire, and a new error interrupt event occurs, the ESM will go back to the ESM_ERROR state. The minimum time interval will not reset, but a new CLEAR event will be required as shown in Figure 12-427.

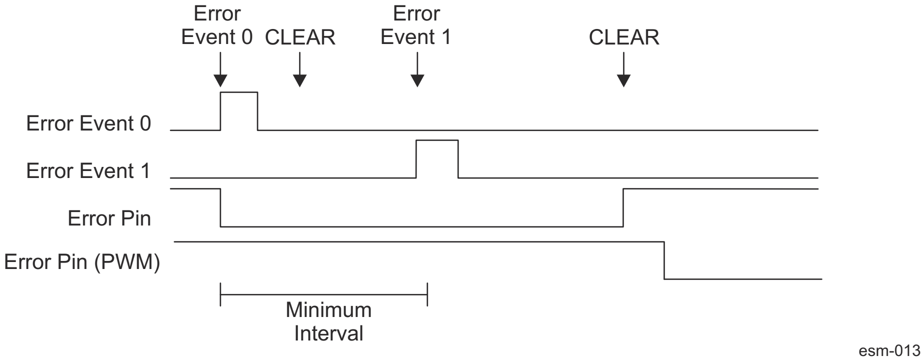

Figure 12-427. ESM Error Pin Asserting with New Error During Minimum Time Interval

Table 12-337 shows some common scenarios of how the error pin as well as the two associated registers (ESM_PIN_CTRL and ESM_PIN_STS) will be set.

Table 12-349. ESM Error Pin Scenarios

Scenario	Error Pin State Value	ESM_PIN_CTRL[3-0] KEY	ESM_PIN_STS[0] VAL status value	Additional Notes
POR Asserted	0	N/A	N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
After de-assertion of POR	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was not asserted when reset asserted)	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was asserted when reset asserted)	0	0x0 (Normal Mode)	0x1	-
Force error pin	0	0xA (Force Error Mode)	0x0	Forcing error on the pin via software.

12.8.2.4.4 PWM Mode

If the error output pin is in PWM mode then when no error is detected it will toggle according to programmable MMR widths for high and low periods. When an error occurs, the error pin stops toggling and remains constant until the error is cleared. An external PMIC that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external PMIC.

12.8.2.4.5 ESM Minimum Time Interval

The minimum time interval is the minimum amount of time that the error pin will be asserted (active low) when an enabled error interrupt event happens. This value is system dependent, but should be enough time so that the external monitoring agent can always see the error pin asserted, but short enough so that if all of the error events are cleared, then the error pin can be de-asserted before the external agent decides to intervene. This is highly dependent on the application and the Fault Tolerant Time Interval.

The Minimum Time Interval counter is clock cycle based, therefore the time of the interval is a combination of the value in the ESM_PIN_CNTR_PRE register and the clock frequency of the ESM. Software must calculate the value accordingly. The Minimum Time Interval should be set according to the needs of the application.

12.8.2.4.6 ESM Protection for Registers

The configuration for each error group *j* of registers are backed up by 3 flops in order to protect against single or double-bit errors. When written, all 3 bits are set to the same value. When read (and for functioning of the internal state machines) the value is the OR of all 3 bits. Whenever any of the bits disagree, the Configuration Error interrupt is asserted (if enabled). The registers covered by this mechanism are:

- ESM_ERR_RAW
- ESM_ERR_STS
- ESM_ERR_EN_SET
- ESM_ERR_EN_CLR
- ESM_RAW_j
- ESM_STS_j
- ESM_INTR_EN_SET_j
- ESM_INTR_EN_CLR_j
- ESM_INT_PRIO_j
- ESM_PIN_EN_SET_j
- ESM_PIN_EN_CLR_j

The error pin control register ESM_PIN_CTRL contains a multi-bit field KEY. The key value ensures normal operation on the error pin and that an error even will be generated if one occurs. Software should periodically read check the KEY bit field value and make sure it is 0x0. If the value is not 0x0, software must re-write it to this key value (unless in test mode forcing an error on the pin) to ensure the normal operation. Table 12-338 lists the KEY values and their respective meaning.

Table 12-350. ESM Error Pin Control Values

ESM_PIN_CTRL[3-0] KEY	Description
N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
0x0 (Normal)	Normal operation mode - Error pin will activate when an enabled error event occurs.
0xA (Force Error)	Force error mode - Forces the error pin active. To clear the error pin (return to the ESM_IDLE state) write this field back to normal mode (writing a CLEAR event will also work). Force error mode must be set only while in IDLE. Attempting force error while in another state will have no effect.
0x5 (CLEAR)	CLEAR Event - generates a CLEAR event to the ESM state machine. KEY will return to normal mode (0x0) on the next cycle.
Other Values	All other values - Normal mode. Writing any of these values will have no effect. When reading any of these values indicates that one or more bits have experienced a single event upset, software should write the field back to 0x0. The ESM will continue to operate in normal mode.

The error pin counter pre-load register ESM_PIN_CNTR_PRE should also be read and checked periodically by software.

12.8.2.4.7 ESM Clock Stop

The ESM can only be put in to clock stop if all of the internal state machines are idle and the [3-0] KEY bit field for the global enable command is cleared in the ESM_EN register.

12.8.3 Memory Cyclic Redundancy Check (MCRC) Controller

This chapter describes the Memory Cyclic Redundancy Check (MCRC) controller in the device.

12.8.3.1 MCRC Overview

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system.

12.8.3.1.1 MCRC Features

MCRC has the following features:

- Four channels to perform background signature verification on any memory subsystem
- Data compression on 8-, 16-, 32-, and 64-bit data size
- Maximum-length PSA (Parallel Signature Analysis) register constructed based on 64-bit primitive polynomial
- Each channel has a CRC Value Register which contains the pre-determined CRC value
- Use timed base event trigger from timer to initiate DMA data transfer
- Programmable 20-bit pattern counter per channel to count the number of data patterns for compression
- Three modes of operation:
  - Auto
  - Semi-CPU
  - Full-CPU
- For each channel, CRC can be performed either by MCRC Controller or by CPU
- Automatically performs signature verification without CPU intervention in AUTO mode
- Generates interrupt to CPU in Semi-CPU mode to allow CPU to perform signature verification itself
- Generates CRC fail interrupt in AUTO mode if signature verification fails
- Generates Timeout interrupt if CRC is not performed within the time limit
- Generates DMA request per channel to initiate CRC value transfer
- An 128-byte block burst address for the PSA register to DMA without constant mode bus attribute

12.8.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.8.3.2 MCRC Functional Description

12.8.3.2.1 MCRC Block Diagram

Figure 12-428 shows the MCRC internal blocks.

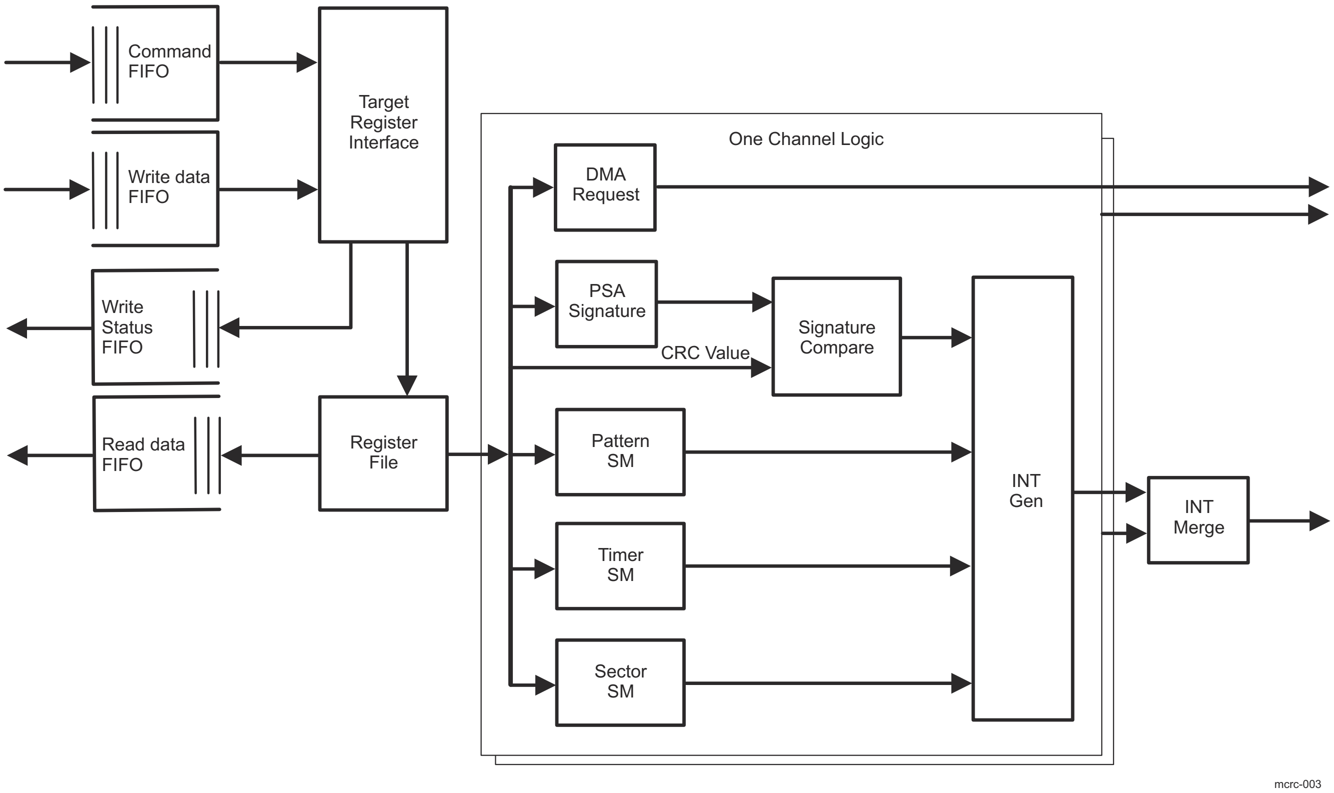

Figure 12-428. MCRC Block Diagram

- **Command FIFO**: The Command FIFO pipelines the commands to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 4 elements deep.
- **Write FIFO**: The Write FIFO pipelines the write data to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 2 elements deep.
- **Write Status FIFO**: The Write Status FIFO pipelines the write status back to the VBUSM. A write status will be issued on the final data phase of a write command. This FIFO is 2 elements deep.
- **Read Data FIFO**: The Read Data FIFO pipelines the read data back to the VBUSM. This FIFO is 3 elements deep.
- **Target Register Interface**: The Target Register Interface directs the written data to the register file.
- **PSA Signature**: The PSA Signature creates the signature of the data written. This data will then be compared to the CRC Value or read by software to determine goodness.
- **Pattern State Machine**: The Pattern State Machine determines when a block of data has been serviced.
- **Timer State Machine**: The Timer State Machine determines when overrun and under-run events are detected.
- **Sector State Machine**: The Sector State Machine determines when a sector error should be captured so the software can determine the errant block of data.
- **Signature Compare**: The Signature Compare block compares the current signature to the CRC Value register and sends the result to the Interrupt Generation block.

12.8.3.2.2 MCRC General Operation

There are four channels in MCRC controller and for each channel there is a PSA (Parallel Signature Analysis) Signature Register (MCRC64_0_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC64_0_CRC_REGL1-4).

A memory can be organized into multiple sectors with each sector consisting of multiple data patterns. A data pattern can be a 8-, 16-, 32-, or 64-bit data. MCRC module performs the signature calculation and compares the signature to a pre-determined value. The PSA Signature Register compresses an incoming data pattern into a signature when it is written. When one sector of data patterns are written into PSA Signature Register, a final signature corresponding to the sector is obtained. CRC Value Register stores the pre-determined signature corresponding to one sector of data patterns. The calculated signature and the pre-determined signature are then compared to each other for signature verification. To minimize CPU’s involvement, data patterns transfer can be carried out at the background of CPU using DMA controller. DMA is setup to transfer data from memory of which the contents to be verified to the memory mapped PSA Signature Register. When DMA transfers data to the memory mapped PSA Signature Register, a signature is generated.

A programmable 20-bit data pattern counter is used for each channel to define the number of data patterns to calculate for each sector. Signature verification can be performed automatically by MCRC controller in AUTO mode or by CPU itself in Semi-CPU or Full-CPU mode. In AUTO mode, a self-sustained CRC signature calculation can be achieved without any CPU intervention.

12.8.3.2.3 MCRC Modes of Operation

MCRC Controller can operate in AUTO, Semi-CPU, and Full-CPU modes.

12.8.3.2.3.1 AUTO Mode

In AUTO mode, MCRC Controller in conjunction with DMA controller can perform CRC without CPU intervention. A sustained transfer of data to both the PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC64_0_CRC_REGL1-4) are performed in the background of CPU. When a mismatch is detected, an interrupt is generated to the CPU. A 16-bit, current sector ID register (MCRC64_0_CRC_CURSEC_REG1-4) is provided to identify which sector causes a CRC failure.

12.8.3.2.3.2 Semi-CPU Mode

In Semi-CPU mode, DMA controller is also utilized to perform data patterns transfer to PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4). Instead of performing signature verification automatically, the CRC controller generates an compression complete interrupt to CPU after each sector is compressed. Upon responding to the interrupt the CPU performs the signature verification by reading the calculated signature stored at the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4) and compare it to a pre-determined CRC value.

12.8.3.2.3.3 Full-CPU Mode

In Full-CPU mode, the CPU does the data patterns transfer and signature verification all by itself. When CPU has enough throughput, it can perform data patterns transfer by reading data from the memory system to the PSA Signature Register (MCRC64_0_PSA_SIGREGL1). After certain number of data patterns are compressed, the CPU can read from the PSA Signature Register and compare the calculated signature to the pre-determined CRC signature value. In Full-CPU mode, neither interrupt nor DMA request is generated. All counters are also disabled.

12.8.3.2.4 PSA Signature Register

The 64-bit PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4 and MCRC64_0_PSA_SIGREGH1-4) is based on the primitive polynomial found in (EQ 1) to produce the maximum length LFSR (Linear Feedback Shift Register).

$$f(x) = x^{64} + x^4 + x^3 + x + 1 \tag{8}$$

Note

More details of the 64-bit primitive polynomial can be found at W. Stahnke, Primitive binary polynomials, Math. Comp. 27 (1973), 977--980.

There is one PSA Signature Register per CRC channel. PSA Signature Register can be both read and written. When it is written, it can either compress the data or just capture the data depending on the state of CHi_MODE bits (where i = 1 to 4). If CHi_MODE=0x0 (Data Capture), a seed value can be planted in the PSA Signature Register without compression. Other modes other than Data Capture will result with the data compressed by PSA Signature Register when it is written. Each channel can be planted with different seed value before compression starts. When PSA Signature Register is read, it gives the calculated signature.

MCRC Controller should be used in conjunction with the on-chip DMA controller to produce optimal system performance. The incoming data pattern to PSA Signature Register is typically initiated by the DMA controller. When DMA is properly setup, it would read data from the pre-determined memory system and write them to the memory mapped PSA Signature Register. Each time PSA Signature Register is written a signature is generated. CPU itself can also perform data transfer by reading from the memory system and perform write operation to PSA Signature Register if CPU has enough throughput to handle data patterns transfer.

After a system reset and when AUTO mode is enabled, MCRC Controller automatically generates a DMA request to request the pre-determined CRC value corresponding to the first sector of memory to be checked.

In AUTO mode, when one sector of data patterns is compressed, the signature stored at the PSA Signature Register is first copied to the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4) and PSA Signature Register is then cleared out to all zeros. An automatic signature verification is then performed by comparing the signature stored at the PSA Sector Signature Register to the CRC Value Register (MCRC64_0_CRC_REGL1-4). After the comparison the MCRC Controller can generate a DMA request. Upon receiving the DMA request the DMA controller will update the CRC Value Register by transferring the next pre-determined signature value associated with the next sector of memory system. If the signature verification fails then MCRC Controller can generate a CRC fail interrupt.

In Full-CPU mode, no DMA request and interrupt are generated at all. The number of data patterns to be compressed is determined by CPU itself. Full-CPU mode is useful when DMA controller is not available to perform background data patterns transfer. Software can periodically generate a software interrupt to CPU and use CPU to accomplish data transfer and signature verification.

MCRC Controller supports double word, word, half word and byte access to the PSA Signature Register. During a non-doubleword write access, all unwritten byte lanes are padded with zeros before compression. Note that comparison between PSA Sector Signature Register and CRC Value Register is always in 64 bits because a compressed value is always expressed in 64 bits.

There is a software reset per channel for PSA Signature Register. When set, the PSA Signature Register is reset to all zeros.

PSA Signature Register is reset to zero under the following conditions:

- System reset
- PSA Software reset
- One sector of data patterns are compressed

12.8.3.2.5 PSA Sector Signature Register

After one sector of data is compressed, the final resulting signature calculated by PSA Signature Register is transferred to the 64-bit PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4 and MCRC64_0_PSA_SECSIGREGH1-4). PSA Signature Register is a read-only register. During Semi-CPU mode, the host CPU must read from the PSA Sector Signature Register instead of reading from PSA Signature Register for signature verification to avoid data coherency issue. The PSA Signature Register can be updated with new signature before the host CPU is able to retrieve it.

In Semi-CPU mode, no DMA request is generated. When one sector of data patterns is compressed, CRC controller first generates a compression complete interrupt. Responding to the interrupt, CPU will read the PSA Sector Signature Register and compare it to the known good signature or write the signature value to another memory location to build a signature file. In Semi-CPU mode, CPU must perform the signature verification in a manner to prevent any overrun condition. The overrun condition occurs when the compression complete interrupt is generated after one sector of data patterns is compressed and CPU has not read from the PSA Sector Signature Register to perform necessary signature verification before PSA Sector Signature Register is overridden with a new value. An overrun interrupt can be enabled to generate when overrun condition occurs.

12.8.3.2.6 CRC Value Register

Associated with each channel there is a 64-bit CRC Value Register (MCRC64_0_CRC_REGL1-4 and MCRC64_0_CRC_REGH1-4).

The CRC Value Register stores the pre-determined CRC value. After one sector of data patterns is compressed by PSA Signature Register, MCRC Controller can automatically compare the resulting signature stored at the PSA Sector Signature Register with the pre-determined value stored at the CRC Value Register if AUTO mode is enabled. If the signature verification fails, MCRC Controller can be enabled to generate an CRC fail interrupt. When the channel is set up for Semi-CPU mode, CRC controller first generates a compression complete interrupt to CPU. Upon servicing the interrupt, CPU will then read the PSA Sector Signature Register and then read the corresponding CRC value stored at another location and compare them. CPU must not read from the CRC Value Register during Semi-CPU or Full-CPU mode because the CRC Value Register is not updated during these two modes.

In AUTO mode, for first sector’s signature, DMA request is generated when mode is programmed to AUTO. For subsequent sectors, DMA request is generated after each sector is compressed. Responding to the DMA request, DMA controller reloads the CRC Value Register for the next sector of memory system to be checked. The user software needs to configure the DMA to ensure that the DMA first writes to the MCRC64_0_CRC_REGL1 followed by the MCRC64_0_CRC_REGH1 register in during the AUTO Mode.

When CRC Value Register is updated with a new CRC value, an internal flag is set to indicate that CRC Value Register contains the most current value. This flag is cleared when CRC comparison is performed. Each time at the end of the final data pattern compression of a sector, MCRC Controller first checks to see if the corresponding CRC Value Register has the most current CRC value stored in it by polling the flag. If the flag is set then the CRC comparison can be performed. If the flag is not set then it means the CRC Value Register contains stale information. A CRC underrun interrupt is generated. When an underrun condition is detected, signature verification is not performed.

MCRC Controller supports double word, word, half word and byte access to the CRC Value Register. As noted before comparison between PSA Sector Signature Register and CRC Value Register during AUTO mode is carried out in 64 bits.

12.8.3.2.7 Raw Data Register

The raw or un-compressed data written to the PSA Signature Register is also saved in the 64-bit Raw Data Register (MCRC64_0_RAW_DATAREGL1-4 and MCRC64_0_RAW_DATAREGH1-4). This register is read only.

12.8.3.2.8 Example DMA Controller Setup

DMA controller needs to be setup properly in either AUTO or Semi-CPU mode as DMA controller is used to transfer data patterns. Hardware or a combination of hardware and software DMA triggering are supported.

12.8.3.2.8.1 AUTO Mode Using Hardware Timer Trigger

There are two DMA channels associated with each CRC channel when in AUTO mode. One DMA channel is setup to transfer data patterns from the source memory to the PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4). The second DMA channel is setup to transfer the pre-determined signature to the CRC Value Register (MCRC64_0_CRC_REGL1-4). The trigger source for the first DMA channel can be either by hardware or by software. As illustrated in Figure 12-429, a timer can be used to trigger a DMA request to initiate transfer from the source memory system to PSA Signature Register. In AUTO mode, MCRC Controller also generates DMA request after one sector of data patterns is compressed to initiate transfer of the next CRC value corresponding to the next sector of memory. Thus a new CRC value is always updated in the CRC Value Register (MCRC64_0_CRC_REGL1-4)by DMA synchronized to each sector of memory.

A block of system memory is usually divided into many sectors. All sectors are the same size. The sector size is programmed in the MCRC64_0_CRC_PCOUNT_REG1-4 and the number of sectors in one block is programmed in the MCRC64_0_CRC_SCOUNT_REG1-4 of the respective channel. MCRC64_0_CRC_PCOUNT_REG1-4 multiplies MCRC64_0_CRC_SCOUNT_REG1-4 and multiplies transfer size of each data pattern should give the total block size in number of bytes.

The total size of the memory system to be examined is also programmed in the respective transfer count register inside DMA module. The DMA transfer count register is divided into two parts. They are element count and frame count. Note that a hardware DMA request can be programmed to trigger either one frame or one entire block transfer. In Figure 12-429, a hardware DMA request from a timer is used as a trigger source to initiate DMA transfer. If all four CRC channels are active in AUTO mode then a total of four DMA requests would be generated by MCRC Controller.

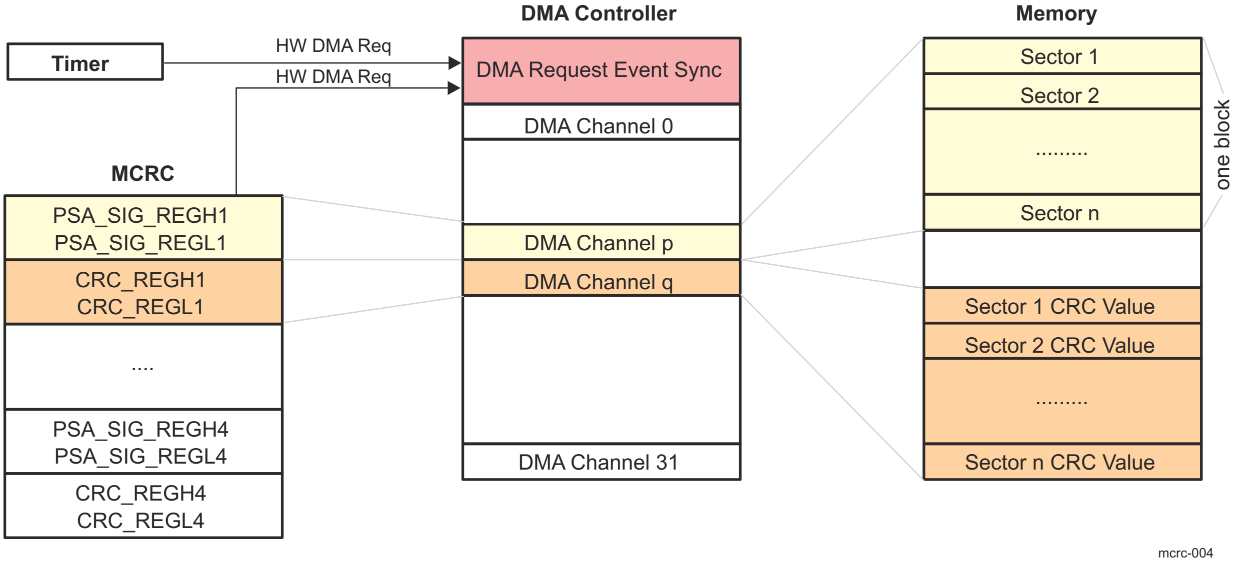

Figure 12-429. AUTO Mode Using Hardware Timer Trigger

12.8.3.2.8.2 AUTO Mode Using Software Trigger

The data patterns transfer can also be initiated by software. CPU can generate a software DMA request to activate the DMA channel to transfer data patterns from source memory system to the PSA Signature Register. To generate a software DMA request CPU needs to set the corresponding DMA channel in the DMA software trigger register. Note that just one software DMA request from CPU is enough to complete the entire data patterns transfer for all sectors. Please see Figure 12-430 for illustration.

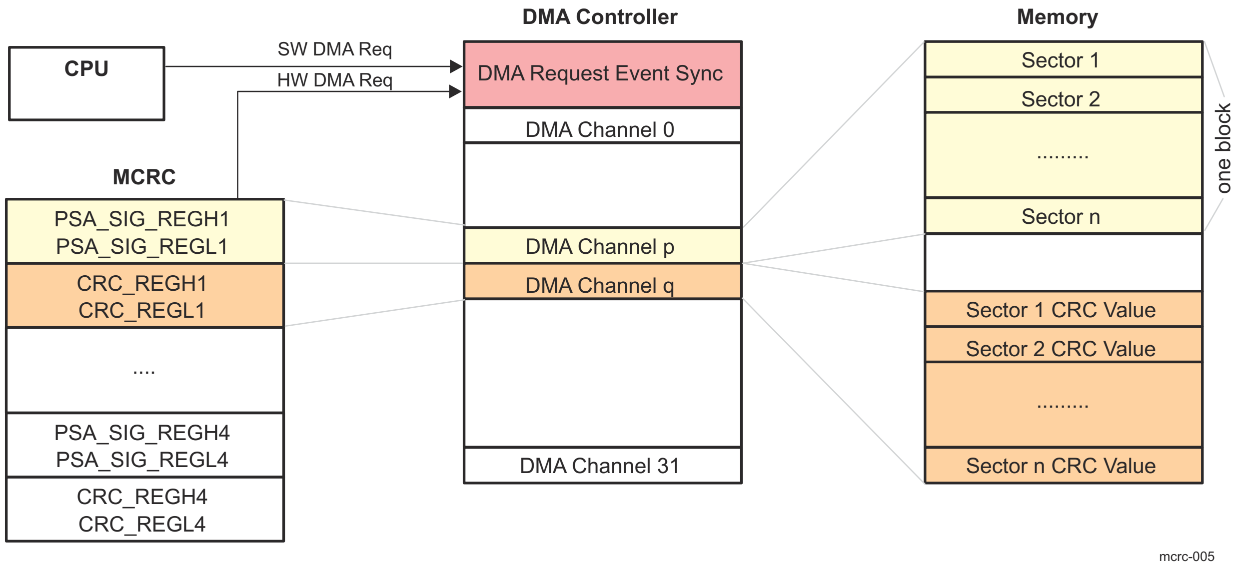

Figure 12-430. AUTO Mode With Software CPU Trigger

12.8.3.2.8.3 Semi-CPU Mode Using Hardware Timer Trigger

During Semi-CPU mode, no DMA request is generated by CRC controller. Therefore, no DMA channel is allocated to update CRC Value Register. CPU should not read from CRC Value Register in semi-CPU mode as it contains stale value. Note that no signature verification is performed at all during this mode. Similar to AUTO mode, either by hardware or by software DMA request can be used as a trigger for data patterns transfer. Figure 12-431 illustrates the DMA setup using semi-CPU mode with hardware timer trigger.

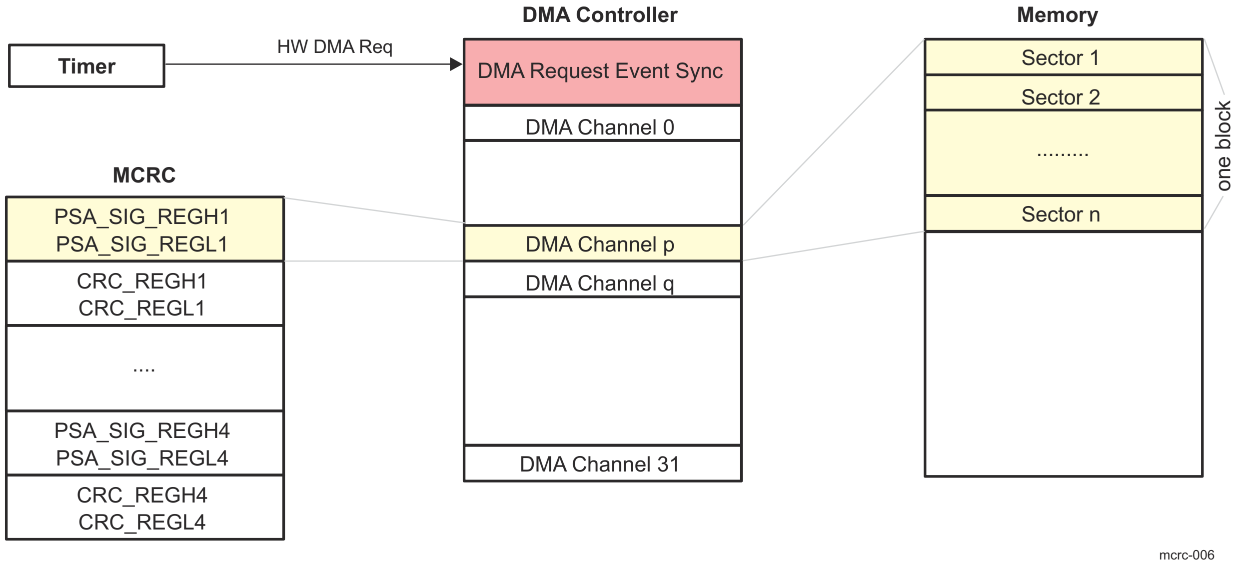

Figure 12-431. Semi-CPU Mode With Hardware Timer Trigger

Table 12-351. DMA Request and Counter Logic Operation According to CRC Mode

CRC Mode	DMA Request	Pattern Counter	Sector Counter	Timeout Counter
AUTO	Active	Active	Active	Active
Semi-CPU	Inactive	Active	Active	Active
Full CPU	Inactive	Inactive	Inactive	Inactive

12.8.3.2.9 Pattern Count Register

There is a 20-bit data pattern counter for every CRC channel. The data pattern counter is a down counter and can be pre-loaded with a programmable value stored in the Pattern Count Register (MCRC64_0_CRC_PCOUNT_REG1-4). When the data pattern counter reaches zero, a compression complete interrupt is generated in Semi-CPU mode and an automatic signature verification is performed in AUTO mode. In AUTO only, DMA request is generated to trigger the DMA controller to update the CRC Value Register.

Note

The data pattern count must be divisible by the total transfer count as programmed in DMA controller. The total transfer count is the product of element count and frame count.

12.8.3.2.10 Sector Count Register/Current Sector Register

Each channel contains a 16-bit sector counter. The sector count register stores the number of sectors. Sector counter is a free running counter and is incremented by one each time when one sector of data patterns is compressed. When the signature verification fails, the current value stored in the sector counter is saved into current sector register (MCRC64_0_CRC_CURSEC_REG1-4). If signature verification fails, CPU can read from the current sector register to identify the sector which causes the CRC mismatch. To aid and facilitate the CPU in determining the cause of a CRC failure it is advisable to use the following equation during CRC and DMA setup.

$$\text{CRC Pattern Count} \times \text{CRC Sector Count} = \text{DMA Element Count} \times \text{DMA Frame Count} \quad (9)$$

The current sector register is frozen from being updated until both the current sector register is read and CRC fail (CHi_CRC_FAIL) status bit is cleared by CPU. If CPU does not respond to the CRC failure in a timely manner before another sector produces a signature verification failure, the current sector register is not updated with the new sector number. An overrun interrupt is generate instead. If current sector register is already frozen with an erroneous sector and emulation is entered with SUSPEND signal goes to high then the register still remains frozen even it is read.

In Semi-CPU mode, the current sector register is used to indicate the sector for which the compression complete has last happened.

Current sector register is reset when the PSA software reset is enabled.

Note

Both data pattern count and sector count registers must be greater than or equal to one for the counters to count. After reset, pattern count and sector count registers default to zero and the associated counters are inactive.

12.8.3.2.11 Interrupts

CRC generate several types of interrupts per channel. Associated with each interrupt there is a interrupt enable bit (see MCRC64_0_CRC_INTS). No interrupt is generated in Full-CPU mode.

- Compression complete interrupt
- CRC fail interrupt
- Overrun interrupt
- Underrun interrupt
- Timeout interrupt

Table 12-352. Interrupt Conditions Per CRC Mode

CRC Mode	Compression Complete	CRC Fail	Overrun	Underrun	Timeout
AUTO	No	Yes	Yes	Yes	Yes
Semi-CPU	Yes	No	Yes	No	Yes

Table 12-352. Interrupt Conditions Per CRC Mode (continued)

CRC Mode	Compression Complete	CRC Fail	Overrun	Underrun	Timeout
Full-CPU	No	No	No	No	No

12.8.3.2.11.1 Overrun Interrupt

Overrun Interrupt is generated in either AUTO or Semi-CPU mode. During AUTO mode, if a CRC fail is detected then the current sector number is recorded in the current sector register (MCRC64_0_CRC_CURSEC_REG1-4). If CRC fail status bit is not cleared and current sector register is not read by the host CPU before another CRC fail is detected for another sector then an overrun interrupt is generated. During Semi-CPU mode, when the data pattern counter finishes counting, it generates a compression complete interrupt. At the same time the signature is copied into the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4). If the host CPU does not read the signature from PSA Sector Signature Register before it is updated again with a new signature value then an overrun interrupt is generated.

12.8.3.2.11.2 Timeout Interrupt

To ensure that the memory system is examined within a pre-defined time frame and no loss of incoming data there is a 24-bit timeout counter per CRC channel. The timeout counter can be pre-loaded with two different pre-load values, watchdog timeout pre-load value (MCRC64_0_CRC_WDTOPLD1-4) and block complete timeout pre-load value (MCRC64_0_CRC_BCTOPLD1-4). The timeout counter is clocked by a prescaler clock which is permanently running at division 64 of FICLK clock.

Watchdog timeout pre-load register (MCRC64_0_CRC_WDTOPLD1-4) is used to check if DMA does supply a block of data responding to a request in a given time frame. Block complete timeout pre-load register (MCRC64_0_CRC_BCTOPLD1-4) is used to check if one complete block of data patterns are compressed within a specific time frame. The timeout counter is first pre-loaded with MCRC64_0_CRC_WDTOPLD1-4 after either AUTO or Semi-CPU mode is selected and starts to down count. If the timeout counter expires before DMA transfers any data pattern to PSA Signature Register then a timeout interrupt is generated. An incoming data pattern before the timeout counter expires will automatically pre-load the timeout counter with MCRC64_0_CRC_BCTOPLD1-4 the block complete timeout pre-load value.

Block complete timeout pre-load value is used to check it one block of data patterns are compressed within a given time limit. If the timeout counter pre-loaded with MCRC64_0_CRC_BCTOPLD1-4 value expires before one block of data patterns are compressed a timeout interrupt is generated. When one block (pattern count × sector count) of data patterns are compressed before the counter has expired, the counter is pre-loaded with MCRC64_0_CRC_WDTOPLD1-4 value again. If the timeout counter is pre-loaded with zero then the counter is disable and no timeout interrupt is generated.

12.8.3.2.11.3 Underrun Interrupt

Underrun interrupt only occurs in AUTO mode. The interrupt is generated when the CRC Value Register is not updated with the corresponding signature when the data pattern counter finishes counting. During AUTO mode, MCRC Controller generates DMA request to update CRC Value Register in synchronization to the corresponding sector of the memory. Signature verification is also performed if underrun condition is detected. And CRC fail interrupt is generated at the same time as the underrun interrupt.

12.8.3.2.11.4 Compression Complete Interrupt

Compression complete interrupt is generated in Semi-CPU mode only. When the data pattern counter reaches zero, the compression complete flag is set and the interrupt is generated

12.8.3.2.11.5 Interrupt Offset Register

MCRC Controller only generates one interrupt request to interrupt manager. An interrupt offset register (MCRC64_0_CRC_INT_OFFSET_REG) is provided to indicate the source of the pending interrupt with highest priority. Table 12-341 shows the offset interrupt vector address of each interrupt in an ascending order of priority.

Table 12-353. Interrupt Offset Mapping

Interrupt Condition	Offset Value
Phantom	0x0
Ch1 CRC Fail	0x1
Ch2 CRC Fail	0x2
Ch3 CRC Fail	0x3
Ch4 CRC Fail	0x4
reserved	0x5-0x8
Ch1 Compression Complete	0x9
Ch2 Compression Complete	0xA
Ch3 Compression Complete	0xB
Ch4 Compression Complete	0xC
reserved	0xD-0x10
Ch1 Overrun	0x11
Ch2 Overrun	0x12
Ch3 Overrun	0x13
Ch4 Overrun	0x14
reserved	0x15-0x18
Ch1 Underrun	0x19
Ch2 Underrun	0x1A
Ch3 Underrun	0x1B
Ch4 Underrun	0x1C
reserved	0x1D-0x20
Ch1 Timeout	0x21
Ch2 Timeout	0x22
Ch3 Timeout	0x23
Ch4 Timeout	0x24

12.8.3.2.11.6 Error Handling

When an interrupt is generated, host CPU must take appropriate actions to identify the source of error and restart the respective channel in DMA and MCRC module. To restart a CRC channel user must perform the following steps in the ISR:

1. Write to software reset bit in MCRC64_0_CRC_CTRL0 register to reset the respective PSA Signature Register
2. Reset the CHi_MODE bits to 0 in MCRC64_0_CRC_CTRL2 register as Data capture mode
3. Set the CHi_MODE bits in MCRC64_0_CRC_CTRL2 register to desired new mode again
4. Release software reset

The host CPU must use byte write to restart each individual channel.

12.8.3.2.12 Power Down Mode

MCRC module can be put into power down mode when the power down control bit MCRC64_0_CRC_CTRL1[0] PWDN is set. The module wakes up when the PWDN bit is cleared. When MCRC controller is in power down mode, no data tracing alone will happen.

12.8.3.2.13 Emulation

A read access from a register in functional mode can sometimes trigger a certain internal event to follow. For example, reading interrupt offset register triggers an event to clear the corresponding interrupt status flag. During emulation when SUSPEND signal is high, a read access from any register should only return the register contents to the bus and should not trigger or mask any event as it would have in functional mode. This is to prevent debugger from reading the interrupt offset register, that is, during refreshing screen and cause the corresponding interrupt status flag to get cleared. Timeout counters are stopped to generate timeout interrupts in emulation mode. No VBUSM bus error will be generated if reading from the unimplemented locations. .

CEMUDBG is the VBUSM suspend signal which need not explicitly indicate that whether CPU is in suspend mode or not. In data trace mode, a separate suspend signal CPU_EMUSP, is used to indicate MCRC controller that the CPU is in suspend mode or not.

12.8.3.3 MCRC Programming Examples

12.8.3.3.1 Example: Auto Mode Using Time Based Event Triggering

A large memory area with 2 Mbyte (256 k × 32-bit [doubleword]) is to be checked in the background of CPU. CRC is to be performed every 1 Kbyte (128 doubleword). Therefore there will be 2048 pre-recorded CRC values. For illustration purpose, we map MCRC64_0_CRC_REGL1 register to DMA channel 1 and MCRC64_0_PSA_SIGREGL1 register to DMA channel 2. Let's assume all DMA transfers are carried out in 64-bit transfer size.

12.8.3.3.1.1 DMA Setup

- Setup DMA channel 1 with the starting address from which the pre-determined CRC values are stored. Setup the destination address to the MCRC64_0_CRC_REGL1. Put the source address at post increment addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1 to trigger a frame transfer.
- Setup DMA channel 2 with the source address from which the contents of memory to be verified. Setup the destination address to the MCRC64_0_PSA_SIGREGL1. Program the element transfer count to 128 and the frame transfer count to 2048. Program the read and write element size to 64 bits. Put the source address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request for channel 2 to trigger an entire block transfer.

12.8.3.3.1.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 2. For example, software can setup the timer to generate a DMA request every 10 ms.

12.8.3.3.1.3 CRC Setup

- Program the pattern count MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the sector count MCRC64_0_CRC_SCOUNT_REG1 to 2048
- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load (MCRC64_0_CRC_BCTOPLD1-4) value to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz.
- Enable AUTO mode and all interrupts.

After AUTO mode is selected MCRC Controller automatically generates a DMA request on channel 1. Around the same time the timer module also generates a DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the CMCRC_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC64_0_PSA_SECSIGREGL1/H1 does not match the MCRC64_0_CRC_REGL1/H1 Register. MCRC Controller generates a DMA request on DMA channel 1 when one sector of data patterns are compressed. This routine will continue until the entire 2 Mbytes are consumed. If the timeout counter reached zero before the entire 2 Mbytes are compressed, a timeout interrupt is generated. After 2Mbytes are transferred, the DMA can generate an interrupt to CPU. The entire operation will continue again when DMA responds to the DMA request from both the timer and MCRC Controller. The CRC is performed totally without any CPU intervention.

12.8.3.3.2 Example: Auto Mode Without Using Time Based Triggering

A small but highly secured memory area with 1 Kbytes is to be checked in the background of CPU. CRC is to be performed every 1 Kbytes. Therefore, there is only one pre-recorded CRC value. For illustration purpose, we map channel 1 MCRC64_0_CRC_REGL1/H1 to DMA channel 1 and channel 1 MCRC64_0_PSA_SIGREGL1/H1 to DMA channel 2. Assume all transfers carried out by DMA are in 64-bit transfer size.

12.8.3.3.2.1 DMA Setup

- Setup DMA channel 1 with the source address from which the pre-determined CRC value is stored. Setup the destination address to the MCRC64_0_CRC_REGL1 Register. Put the source address at constant addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1.
- Setup DMA channel 2 with the source address from which the memory area to be verified. Setup the destination address to the MCRC64_0_PSA_SIGREGL1/H1. Program the element transfer count to 128 and the frame transfer count to 1. Put the source address at post increment addressing mode and put the destination address at constant address mode. Generate a software DMA request on channel 2 after CRC has completed its setup. Enable autoinitiation for DMA channel 2.

12.8.3.3.2.2 CRC Setup

- Program the MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the MCRC64_0_CRC_SCOUNT_REG1 to 1
- Leaving the timeout count MCRC64_0_CRC_BCTOPLD1 register with the reset value of zero means no timeout interrupt is generated
- Enable AUTO mode and all interrupts

After AUTO mode is selected the MCRC Controller automatically generates a DMA request on channel 1. At the same time the CPU generates a software DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the MCRC64_0_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC64_0_PSA_SECSIGREGL1/H1 does not match the MCRC64_0_CRC_REGL1/H1. MCRC Controller generate a DMA request on DMA channel 1 again after one sector is compressed. After 1 Kbytes are transferred, the DMA can generate an interrupt to CPU. Responding to the DMA interrupt CPU can restart the CRC routine by generating a software DMA request onto channel 2 again.

12.8.3.3.3 Example: Semi-CPU Mode

If DMA controller is available in a system the CRC module can also operate in semi-CPU mode. This means that CPU can still make use of the DMA to perform data patterns transfer to CRC controller in the background. The difference between semi-CPU mode and AUTO mode is that CRC controller does not automatically perform the signature verification. CRC controllers generates a compression complete interrupt to CPU when the one sector of data patterns are compressed. CPU needs to perform the signature verification itself.

A memory area with 2 Mbytes is to be verified with the help of the CPU. CRC operation is to be performed every 1 Kbyte. Since there are 2 Mbytes (256 K doublewords) of memory to be check and we want to perform a CRC every 1 Kbytes (128 doublewords) and therefore there must be 2048 pre-recorded CRC values. In Semi-CPU mode, the MCRC64_0_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.8.3.3.3.1 DMA Setup

- Setup DMA channel 1 with the source address from which the memory area to be verified are mapped. Setup the destination address to the MCRC64_0_PSA_SIGREGL1/H1. Put the starting address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request to trigger an entire block transfer for channel 1. Disable autoinitiation for DMA channel 1.

12.8.3.3.3.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time-based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 1. For example, software can setup the timer to generate a DMA request every 10 ms.

12.8.3.3.3.3 CRC Setup

- Program the MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the MCRC64_0_CRC_SCOUNT_REG1 to 2048

- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load value MCRC64_0_CRC_BCTOPLD1 to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz
- Enable AUTO mode and all interrupts.

The timer module first generates a DMA request on DMA channel 1 when it is enabled. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the CRC controller will compress it. After one sector of data patterns are compressed, the CRC controller generate a compression complete interrupt. Upon responding to the interrupt the CPU would read from the MCRC64_0_PSA_SECSIGREGL1/H1. It is up to the CPU on how to deal with the PSA value just read. It can compare it to a known signature value or it can write it to another memory location to build a signature file or even transfer the signature out of the device via SCI or SPI. This routine will continue until the entire 2 Mbytes are consumed. The latency of the interrupt response from CPU can cause overrun condition. If CPU does not read from MCRC64_0_PSA_SECSIGREGL1 before the PSA value is overridden with the signature of the next sector of memory, an overrun interrupt will be generated by CRC controller.

12.8.3.3.4 Example: Full-CPU Mode

In a system without the availability of DMA controller, the CRC routine can be operated by CPU provided the CPU has enough throughput. CPU needs to read from the memory area from which CRC is to be performed.

A memory area with 2 Mbytes is to be checked with the help of the CPU. CRC operation is to be performed every 1 Kbyte. In CPU mode, the MCRC64_0_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.8.3.3.4.1 CRC Setup

- All control registers can be left in their reset state. Only enable Full-CPU mode.

CPU itself reads from the memory and write the data to the MCRC64_0_PSA_SIGREGL1/H1 inside MCRC Controller. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After n data patterns are compressed, CPU can read from the MCRC64_0_PSA_SIGREGL1/H1. It is up to the CPU on how to deal with the PSA signature value just read. It can compare it to a known signature value stored at another memory location.

12.8.4 ECC Aggregator

This section describes the common ECC aggregator functionality.

12.8.4.1 ECC Aggregator Overview

To increase functional and system reliability the memories (for example, FIFOs, queues, SRAMs and others) in many device modules and subsystems are protected by error correcting code (ECC). This is accomplished through an ECC aggregator and ECC wrapper. The ECC aggregator is connected to these memories (hereinafter ECC RAMs) and involved in the ECC process. Each memory is surrounded by an ECC wrapper which performs the ECC detection and correction. The wrapper communicates via serial interface with the aggregator which has memory mapped configuration interface.

The ECC aggregator is also connected to interconnect ECC components that protect the command, address and data buses of the system interconnect. ECC is calculated for the data bus and parity and redundancy for the command and address buses. Each interconnect ECC component has the same serial interface for communication with the aggregator as the ECC wrapper. An ECC aggregator may be connected to both endpoints - the ECC wrapper and interconnect ECC component.

The ECC aggregator, ECC wrapper and interconnect ECC component are considered as single entity and are hereinafter referred to as ECC aggregator unless otherwise explicitly specified.

See *Module Integration* for device modules and subsystems which have ECC aggregator.

12.8.4.1.1 ECC Aggregator Features

The ECC aggregator has the following features:

- Reduces memory software errors via single error correction (SEC) and double error detection (DED)
- Provides a mechanism to control and monitor the ECC protected memories in a module or subsystem
- SEC and DED over the system interconnect data bus and parity and redundancy for the system interconnect command and address buses
- Generates an interrupt for correctable error
- Generates an interrupt for non-correctable error
- Supports inject only mode for diagnostic purposes
- Supports software readable status for single and double-bit ECC errors and associated information such as row address where error has occurred and data bits that have been flipped
- Supports up to 256 ECC endpoints. An ECC endpoint can be either ECC RAM or interconnect ECC component.
- Detects single bit error via parity checking on:
  - Memory mapped configuration interface FIFO
  - Serial interface FIFO
  - Serial interface transaction
- Single bit error detection via parity checking results in a non-correctable error interrupt
- Supports timeout mechanism on transactions over the ECC serial interface. Timeout occurrence results in a non-correctable error interrupt.
- Certain control bits have redundancy and if a bit flips an interrupt is generated

12.8.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

12.8.4.2 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.8.4.3 ECC Aggregator Functional Description

This section describes the architecture and functional details of the ECC aggregator.

12.8.4.3.1 ECC Aggregator Block Diagram

Figure 12-432 shows the ECC aggregator block diagram.

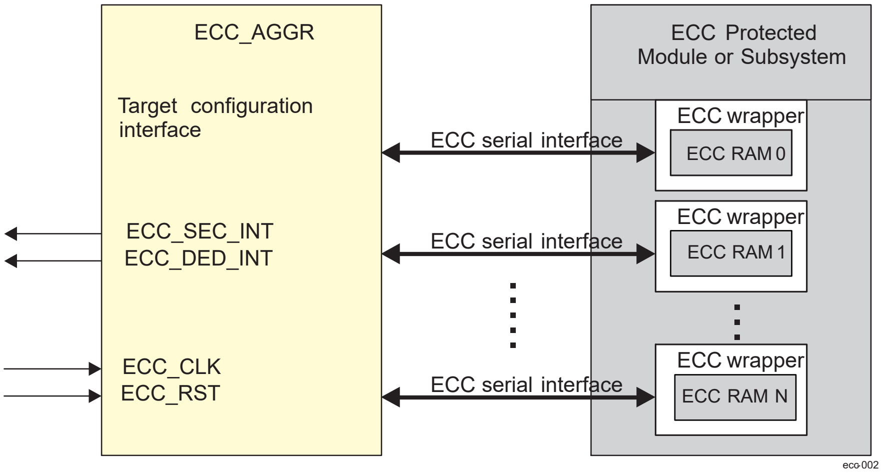

Figure 12-432. ECC Aggregator Block Diagram

The ECC aggregator is connected to one or more ECC endpoints each of which has assigned a unique ID used when the endpoint is accessed for status information or configuration. The ECC aggregator provides software access to all ECC related registers through its memory mapped target configuration interface while the serial interface is used to communicate with the ECC endpoints. Upon detection of single or double-bit error the corresponding interrupt line is asserted.

12.8.4.3.2 ECC Aggregator Register Groups

The ECC aggregator has ECC control, status and interrupt registers for each ECC endpoint in a module or subsystem. These registers are memory mapped and occupy 1 KB address space although part of it may contain reserved locations. The registers are split in the following types:

- **Global registers**. They are common to all ECC endpoints associated with the ECC aggregator and include the ECC_VECTOR and ECC_REV registers. Each ECC endpoint has assigned a unique ID. When this ID is written to the ECC_VECTOR[10-0] ECC_VECTOR field the corresponding endpoint is selected either for control or for status reading.
- **ECC control and status registers**. These registers are specific to each ECC endpoint and reside in the range from address offset 0x10 to 0x28, if the endpoint is ECC RAM or from 0x10 to 0x24, if the endpoint is interconnect ECC component. They are memory mapped but are accessed through the ECC serial interface. They are also selected by the ECC endpoint ID written to the ECC_VECTOR[10-0] ECC_VECTOR field. Because of latency on the serial interface the ECC control and status registers are read by performing special sequence as described in Section 12.8.4.3.3 . These registers have also different functionality for both types of endpoints - ECC RAM and interconnect ECC component.
- **Interrupt registers**. They include interrupt status, interrupt enable, interrupt disable, and EOI registers. For more information, see *Interrupts*.

Note

For description of each register, see *ECC_AGGR Registers*.

12.8.4.3.3 Read Access to the ECC Control and Status Registers

Read accesses to the ECC control and status registers for each ECC endpoint represent read operations over the ECC serial interface and are triggered by performing the following sequence:

1. Software writes the following in the ECC_VECTOR register:
   - The ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field to select particular ECC endpoint.
   - The register read address in the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field to select which register has to be read through the ECC serial interface.
   - A value of 0x1 in the ECC_VECTOR[15] RD_SVBUS bit to trigger read operation through the ECC serial interface.
2. Software polls the ECC_VECTOR[24] RD_SVBUS_DONE bit to check if it is 0x1. This indicates that the read operation on the ECC serial interface has completed.
3. Software reads the data from the register previously selected by the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field.

The following is an example for serial read operation:

1. Write 0x0010 8005 to the ECC_VECTOR register. This sends read request to the ECC_WRAP_REV or ECC_CBASS_REV register (address = 0x10) associated with ECC endpoint with ID = 5.
2. Poll the ECC_VECTOR[24] RD_SVBUS_DONE bit until value of 0x1 is read.
3. Read the ECC_WRAP_REV or ECC_CBASS_REV register to get its value.

12.8.4.3.4 Serial Write Operation

Write operations over the ECC serial interface are performed as follows:

1. Software specifies the ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field. The ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field is a don't care but the ECC_VECTOR[15] RD_SVBUS bit must be set to 0x0.
2. Software performs regular write operation to the desired address. If the ECC endpoint ID has already been specified, step 1 can be skipped. Unlike serial read operations it is not necessary to always specify the endpoint ID before performing serial write operation.

The following is an example for serial write operation:

1. Write 0x0000 0008 to the ECC_VECTOR register.
2. Write 0x0000 000F to the ECC_CTRL register. This sends write request with data 0x0000 000F to the ECC_CTRL register associated with ECC RAM with ID = 8.

12.8.4.3.5 Interrupts

The ECC aggregator generates the following interrupts:

- Correctable interrupt (ECC_SEC_INT) where hardware can correct the error but notifies the system in case of SEC.
- Non-correctable interrupt (ECC_DED_INT) where hardware cannot correct the error in cases of DED, parity check, redundancy check or timeout occurrence.

The following is the sequence for servicing interrupts:

- Software enables the interrupts for an ECC endpoint by writing 0x1 to the corresponding bit of the following interrupt enable registers:
  - ECC_SEC_ENABLE_SET_REG0 through ECC_SEC_ENABLE_SET_REG7 for the correctable interrupt
  - ECC_DED_ENABLE_SET_REG0 through ECC_DED_ENABLE_SET_REG7 for the non-correctable interrupt
- On receiving an interrupt, software checks which ECC endpoint has caused the error by reading the following interrupt status registers:
  - ECC_SEC_STATUS_REG0 through ECC_SEC_STATUS_REG7 for the correctable interrupt
  - ECC_DED_STATUS_REG0 through ECC_DED_STATUS_REG7 for the non-correctable interrupt

- Software performs serial read operations as described in Section 12.8.4.3.3 to read the following status registers that contain details about the error:
  - If the endpoint is ECC RAM:
    - ECC_ERR_STAT1
    - ECC_ERR_STAT2
    - ECC_ERR_STAT3
  - If the endpoint is interconnect ECC component:
    - ECC_CBASS_ERR_STAT1
    - ECC_CBASS_ERR_STAT2
- After the interrupt has been serviced, depending on the error type, software should clear the corresponding status bits in the ECC_ERR_STAT1 and ECC_ERR_STAT3 registers or in the ECC_CBASS_ERR_STAT1 register. Software has to poll these registers to guarantee that status bits are cleared as there is no other indication for write completion over the ECC serial interface.
  The value of the *_PEND_CLR fields in the ECC_CBASS_ERR_STAT1 register must be read and then written back to decrement the count of each field back to 0x0. A further error capture into the ECC_CBASS_ERR_STAT1 register does not occur unless all its fields are 0x0. The decrement value should not be larger than the read value. If a field in the ECC_CBASS_ERR_STAT1 register should not be modified, write a value of 0x0 to that field.
- Software writes 0x1 to the corresponding end of interrupt register to clear the interrupt:
  - ECC_SEC_EOI_REG for the correctable interrupt
  - ECC_DED_EOI_REG for the non-correctable interrupt

12.8.4.3.6 Inject Only Mode

There are modules that already perform the ECC generation and checking as part of their data path. In this case, the ECC wrapper may be configured in inject only mode, if needed. In this mode the ECC wrapper does not perform ECC detection and correction. The inject only mode allows users to inject single or double-bit errors so that the module logic can be tested for diagnostic purposes.

Note

There is no software control to enable inject only mode. It is configured via tie-off value. Inject only and ECC modes are mutually exclusive.

The interconnect ECC component also supports error injection mode. There is error injection logic for testing of the error checking logic (checkers). The injection logic can be configured to inject either single or double bit error and what data pattern to be used for injection (ECC_CBASS_CTRL[11-8] ECC_PATTERN). The ECC_CBASS_ERR_CTRL1 and ECC_CBASS_ERR_CTRL2 registers should be written first to setup the injection. Then, either the ECC_CBASS_CTRL[3] FORCE_SE or the ECC_CBASS_CTRL[4] FORCE_DE bit must be set to 0x1 to start the injection. Both bits must not be set at the same time. If the injection should continue in incrementing mode, then the ECC_CBASS_CTRL[5] FORCE_N_BIT bit should be set to 0x1. Once the FORCE_N_BIT is set, then each successive injection can simply write the ECC_CBASS_CTRL register to set the FORCE_SE or FORCE_DE again. Reading 0x0 from either the FORCE_SE or the FORCE_DE bit indicates that the injection has completed, as these bits automatically clear when the checker indicates that it has performed the injection. The time for an injection to complete is not guaranteed, so some delay is needed between successive injections.

12.8.4.3.7 ECC Error Injection Sequence

The ECC aggregator is a critical component for enhancing system reliability by protecting memories in various device modules and subsystems. The ECC Aggregator is connected to these memory and interconnect components which have the ECC, to provide access to control and monitor the ECC protected memories in a module or subsystem.

The ECC aggregator supports error injection to aid in diagnostic purposes and to evaluate robustness. The Error Injection feature supported by the ECC aggregator allows users to deliberately introduce errors into their system to test the resilience and effectiveness of error correction mechanisms. This feature helps in evaluating the robustness of the ECC aggregator by simulating real-world error scenarios, enabling users to identify potential vulnerabilities and improve their error handling strategies.

This feature includes configurable parameters such as ECC aggregator type, subtype, error type, and injection location, allowing users to customize their testing scenarios based on their specific requirements.

12.8.4.3.7.1 Types of Error Injection

ECC is a mechanism for providing increased protection against soft errors by allowing single bit errors to be detected and corrected and double bit errors to be detected. The ECC Control Register can be used to inject single bit or double bit errors. For more information on this register, refer to Section 12.8.4.3.2 . These errors are then reported through the Error Signal Module (ESM).

- Single Error Correction (SEC): In the event of single bit errors, the ECC aggregator has the ability to both detect and correct these errors, ensuring the integrity of the data. Single bit error injection is supported for all endpoints and checkers. Single bit error correction is not supported for parity and redundancy type of checkers.
- Double Error Detection (DED): For double bit errors, the ECC aggregator can detect these errors. However, it does not have the capability to correct them. Instead, it signals the presence of these errors to the Central Processing Unit (CPU) via ESM interrupts. This is supported for all RAM wrapper types and interconnect EDC checker type of endpoints. Parity and Redundant checker types do not support double bit ECC error injection.

The ECC aggregator plays a crucial role in maintaining data accuracy by correcting single bit errors and detecting double bit errors, although it cannot correct the latter. This process helps in enhancing the overall system reliability. Each ECC aggregator connects to two kinds of ESM events – Correctable error events (for SEC events) and Un-correctable error events (for DED events and parity and redundancy checker types). ESM is used for notification of events from endpoints which are not Inject-Only. Inject-Only endpoints notify errors through IP-specific mechanisms. Sometimes a separate ESM event (not via ECC aggregator) is available. Please refer to the individual IP sections for more details on the ESM events generated.

The ECC aggregator provides support for injecting single and double bit errors. In the case of RAM wrapper type endpoints, errors can be injected to a specific row or can be requested to be injected on the next row access (n_row). Errors can be requested to be injected once or on repeated reads. For Interconnect endpoint types, single and double bit errors (depending on the checker type) can be injected.

12.8.4.3.7.1.1 ECC Wrapper Type Endpoints

Each memory is surrounded by an ECC wrapper which performs the ECC detection and correction. The wrapper communicates via serial interface with the aggregator which has memory a mapped configuration interface. For RAM wrapper types, after injecting the error, the RAM location where the error was injected needs to be accessed in order to trigger the error interrupt. If the “force_n_row” option is selected during error injection, then any RAM access will trigger the interrupt and the specific row is not needed.

12.8.4.3.7.1.2 EDC Interconnect Type Endpoints

The ECC aggregator is also connected to interconnect ECC components that protect the command, address and data buses of the system interconnect. ECC is calculated for the data bus and parity and redundancy for the command and address buses. For the interconnect types, the type of checker must be verified to determine if they are parity or redundant types.

12.8.4.3.7.1.3 Inject Only ECC Endpoints

Some modules may already do the generation of and checking of ECC as part of their data path. In this case, the ECC wrapper does not have to perform ECC detection and correction and is configured in inject only mode. The wrapper will not add extra bits to the ram, generate, nor check ECC. It will, however, allow the user to inject single or double-bit errors so that the IP’s logic can be tested for diagnostic purposes. Detection and correction occurs in the IP itself. In some cases, the error may also be routed to ESM, but not to the same ESM event as the ECC aggregator. For more information on these memories, refer to Section 12.8.4.3.6 .

12.8.4.3.7.1.4 Full Functionality Error Capture ECC Endpoints

These ECC aggregators possess the ability to perform Error Injection alongside Error Capture. The wrapper can be utilized to introduce either single or double-bit errors, while also having the capability to detect and correct errors.

For more information regarding the ECC endpoint types, refer to the Appendix spreadsheet.

12.8.4.3.7.2 Types of ECC Checkers

There are various checkers for bus signals, MMRs, or internal registers in the interconnect.

12.8.4.3.7.2.1 Parity Type Checkers

The most common checker type is parity. The parity type refers to checkers where a parity bit is added to cover the entire signal. The parity bit is the ~^signal, where the signal width can be any number of bits.

12.8.4.3.7.2.2 Redundant Type Checkers

The redundant type refers to checkers for critical signals (like request). The redundant signal is the opposite of the signal it is protecting.

12.8.4.3.7.2.3 Error Detect and Correct (EDC) Type Checkers

The EDC type refers to SECDED error-correcting code that can correct single bit error, and detect a two bit error.

For more information regarding the ECC checker type for each aggregator, refer to the Appendix spreadsheet.

12.8.4.3.7.3 Recommendations for Testing Error Injection

The following are the general recommendations on when the error injection on ECC aggregators must be performed:

- The ECC error injection and monitoring of the error response should be run at ‘startup’ where possible.
- An alternative recommended approach is to run ECC error injection at ‘shutdown’.

When running of ECC error injection during ‘runtime’, the system integrator must be aware of the below:

For interconnect endpoints:

- The ECC SEC error injection runs during idle cycles, so can be run during ‘runtime’ for checkers of all types.
  - Parity and redundant bit error injections are non-destructive and can be done at runtime.
- The ECC DED error injection runs during idle cycles, so can be run during ‘runtime’.
  - Only single bit error injections are to be done on parity/redundant checker types. This is because these protect odd number of injections. A 2 bit injection on parity will not cause a failure.

For RAM memories:

- ECC self-test for SEC on RAM memories, can be run at runtime:
  - The ECC self-test for SEC injects a single-bit error that is corrected in-line.
- ECC DED error injection during ‘runtime’ for RAM memories, should only be done for memories with direct read access
  - Two examples of direct read access memories are MSMC SRAM and MCU SRAM
  - Double-bit error injection on all other embedded SRAMS could possibly result in the downstream IP reading bad data if run during ‘runtime’
- CC error injection on inject-only memories, should be run at ‘startup’, they are not recommended to be run during ‘runtime’. For more information on these memories, refer to Section 12.8.4.3.6 .

12.8.4.3.7.4 Error Injection Programming Sequence

12.8.4.3.7.4.1 ESM Initialization

The ESM instance must beinitializedwith the following sequence. This initialization will allow the application to specify for each event whether the interrupt is enabled or disabled, the priority of the event, and whether the nErrorPin assertion is enabled or disabled for the event. This needs to be done only once. All the required ESM events can be initialized at the same time.

For more information on the ESM, refer to Error Signaling Module (ESM)..

To initialize the ESM module for a specified instance:

1. Clear all raw status and enable bits by setting ESM_SFT_RST Register bits [3:0] to 0Fh, to reset the ESM
2. Write 0x1 to the appropriate bits in the ESM_ERR_STS register. This step will clear the configuration interrupt raw status
3. Write 0x1 to the appropriate bits in the ESM_ERR_EN_SET register, to n enable the configuration error interrupt as described in ESM Configuration Error Interrupt..
4. Write 0x1 to the appropriate bits in the error group j of the ESM_STS_j register. This step will clear the level interrupt raw status.
5. Write 0x1 to the appropriate bits in the error group j of the ESM_INTR_EN_SET_j register, to enable the level error interrupt.
6. Write 0x1 to the appropriate bits in the error group j of the ESM_INT_PRIO_j register, to indicate which interrupt the corresponding event influences (if enabled) for event group j.
7. If required, write 0x1 to the appropriate bits in the error group j of the ESM_PIN_EN_SET_j register, to set error output corresponding to the desired events.
8. Enable the global interrupts by setting ESM_EN Register bits [3:0] to 0Fh

12.8.4.3.7.4.2 ECC Initialization

1. Setting the timeout bit is required to enable notification for ECC serial interface timeout errors. The parity bit must be set to enable notification for parity errors. To enable the timeout (bit 1) and parity (bit 0) bits, write 0x1 to the ECC_AGGR_ENABLE_SET register.
2. Write 0x1 to the ECC_SEC_ENABLE_SET_REGx (to enable correctable SEC error interrupts) and ECC_DED_ENABLE_SET_REGx (to enable uncorrectable DED error interrupts) registers for required endpoints.

The following register configurations are per endpoint and done through the SVBUS programming interface. Refer to Section 12.8.4.3.4 for more information.

1. Write 0x1 to the ECC_CHECK field of the ECC_CBASS_CTRL register to enable ECC check for interconnect endpoints.
2. Write 0x1 to the ENABLE_RMW, ECC_CHECK and ECC_ENABLE bit fields of the ECC_CTRL register to enable ECC check for wrapper type endpoints.

12.8.4.3.7.4.3 Error Injection

For ECC Wrapper Type Endpoints:

1. Write to the ECC_ERR_CTRL1 Register to set the row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.
2. Configure the ECC_RAM_CTRL bits[6:3] register based on the type of error injection.
3. Perform a read back of the ECC_RAM_CTRL register to confirm error injection. The read value may not be same as what is written as some fields in the register are not writable or can self-clear.
4. For RAM wrapper types, after injecting the error, the RAM needs to be accessed in the row where the error was injected (if FORCE_N_ROW is used, any row can be accessed) in order to trigger the error interrupt.
5. For Inject-only Wrapper endpoints, only error injection is possible via the ECC aggregator, the detection and correction is be done by the IP itself.

Field	Name	Type	Reset	Description
0	ecc_enable	r/w	1	Enable ECC generation. **Reset to 1 with inject only configuration, but any write to this register byte clears this bit to 0. Resets to 1 in all other configurations.**

Field	Name	Type	Reset	Description
1	ecc_check	r/w	1/0	Enable ECC check. ECC is completely bypassed if both ecc_enable and ecc_check are ‘0’. **Reset to 0 with inject only configuration, and not writable. Reset to 1 in all other configurations.**
2	enable_rmw	r/w	1/0	Enable read-modify-write on partial word writes. **If disabled ecc detection and correction will no longer work and if re-enabled the ram contents must all be rewritten to correct ecc codes. Reset to 0 with inject only configuration, and not writable. Reset to 1 in all other configurations.**
3	force_sec	r/w	0	Force single-bit error. Cleared the cycle following the error if error_once is asserted. for write through mode this applies to writes as well as reads.
4	force_ded	r/w	0	Force double-bit error. Cleared the cycle following the error if error_once is asserted. for write through mode this applies to writes as well as reads.
5	force_n_row	r/w	0	Force single/double-bit error on the next RAM access. for write through mode this applies to writes as well as reads.
6	error_once	r/w	0	If this bit is set, the force_sec/force_ded will inject an error to the specified row only once. The force_sec bit will be cleared the cycle after the error is generated. For double-bit errors, the force_ded bit will be cleared the cycle following the double-bit error. In either case force_n_row will be cleared as well. Any subsequent reads will not force an error.
7	check_parity	r/w	1	Enables parity checking on internal data
8	Check svbus timeout	r/w	1	Enable svbus timeout mechanism
9-31	Reserved			

For ECC Interconnect Type Endpoints:

1. Clear any pending error injection by writing 0x0 to the bit fields of the ECC_CBASS_CTRL register
2. Configure the ECC_CBASS_ERR_CTRL1 and ECC_CBASS_ERR_CTRL2 registers based on the error group and type of error injection.
3. Write to the ECC_CBASS_CTRL register to inject the error.
4. For interconnect types, the error injection happens on idle cycles, so no additional access of the memory is required.

12.8.4.3.7.4.4 Error Handling

1. When an error event occurs, the user can query and collect the information about the endpoint and offset information for the location relative to the start of the associated RAM.
2. To clear the ECC error event, clear the pending status of the ECC error events by configuring the ECC_RAM_ERR_STAT1 (for Wrapper type endpoints) and SDL_EDC_CTL_ERR_STATUS1(for Interconnect type endpoints) register.
3. The ECC_SEC_EOI_REG register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the ECC_SEC_EOI_REG register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the ECC_SEC_EOI_REG register is not functional and must not be used.

4. Clear the ESM error interrupt using the ESM registers.

12.8.4.4 ECC Aggregator Registers

1 ECC_AGGR Registers

Table 12-342 lists the memory-mapped registers for an ECC Aggregator (ECC_AGGR).

Table 12-354. ECC Wrapper Registers

Offset	Register Name	Description
		ECC Wrapper Registers
10h	ECC_WRAP_REV	ECC Wrapper Revision Register
14h	ECC_CTRL	ECC RAM Control Register
18h	ECC_ERR_CTRL1	ECC RAM Error Control 1 Register
1Ch	ECC_ERR_CTRL2	ECC RAM Error Control 2 Register
20h	ECC_ERR_STAT1	ECC RAM Error Status 1 Register
24h	ECC_ERR_STAT2	ECC RAM Error Status 2 Register
28h	ECC_ERR_STAT3	ECC RAM Error Status 3 Register
		Interconnect ECC Component Registers
10h	ECC_CBASS_REV	Interconnect ECC Component Revision Register
14h	ECC_CBASS_CTRL	Interconnect ECC Component Control Register
18h	ECC_CBASS_ERR_CTRL1	Interconnect ECC Component Error Control 1 Register
1Ch	ECC_CBASS_ERR_CTRL2	Interconnect ECC Component Error Control 2 Register
20h	ECC_CBASS_ERR_STAT1	Interconnect ECC Component Error Status 1 Register
24h	ECC_CBASS_ERR_STAT2	Interconnect ECC Component Error Status 2 Register

2 ECC_WRAP_REV Register (Offset = 10h)

Return to Summary Table.

ECC Wrapper Revision Register

Revision parameters.

Figure 12-433. ECC_WRAP_REV Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">REV</td></tr>
<tr><td colspan="16">R-66A49A02h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">REV</td></tr>
<tr><td colspan="16">R-66A49A02h</td></tr>
</table>

Table 12-356. ECC_WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66A49A02h	TI internal data.

3 ECC_CTRL Register (Offset = 14h)

Return to Summary Table.

ECC RAM Control Register

The Global control register controls ECC control bits for the selected ECC RAM

Figure 12-434. ECC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CHECK_SVBUS_TIMEOUT
R-0h							R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

Table 12-358. ECC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED			Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	Enable ECC serial interface timeout mechanism 0h - Timeout mechanism disabled 1h - Timeout mechanism enabled
7	CHECK_PARITY	R/W	1h	Enables parity checking on internal data 0h - Parity checking disabled 1h - Parity checking enabled
6	ERROR_ONCE	R/W	0h	Force error only once. If this bit is set to 1h, the FORCE_SEC/FORCE_DED injects an error to the specified row only once. The FORCE_SEC bit is cleared the cycle after the error is generated. For double-bit errors, the FORCE_DED bit is cleared the cycle following the double-bit error. Any subsequent reads do not force an error.
5	FORCE_N_ROW	R/W	0h	Force error on any RAM read Force single or double-bit error on the next RAM access. For write through mode this applies to writes as well as reads.
4	FORCE_DED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is 1h. For write through mode this applies to writes as well as reads.
3	FORCE_SEC	R/W	0h	Force single-bit error. Cleared the cycle following the error if ERROR_ONCE is 1h. For write through mode this applies to writes as well as reads.

Table 12-358. ECC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ENABLE_RMW	R/W	1h	Enable read-modify-write on partial word writes. 0h - Read-modify-write disabled 1h - Read-modify-write enabled **Note** If disabled, ECC detection and correction does no longer work and if re-enabled the RAM contents must all be rewritten to correct ECC codes. The reset value of this bit is 0h in inject only mode and 1h in ECC mode.
1	ECC_CHECK	R/W	1h	Enable ECC check. 0h - ECC check disabled 1h - ECC check enabled **Note** ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are 0h. The reset value of this bit is 0h in inject only mode and 1h in ECC mode.
0	ECC_ENABLE	R/W	1h	Enable ECC generation. 0h - ECC generation disabled 1h - ECC generation enabled

Note

All registers in this region have redundancy and if a bit flips and there is an inconsistency an interrupt will be generated and the effective value will be the reset value.

4 ECC_ERR_CTRL1 Register (Offset = 18h)

Return to Summary Table.

Contains row number and data bit that needs to be flipped to force single-bit error

This register contains ECC error control bits for the selected ECC RAM

Figure 12-435. ECC_ERR_CTRL1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">ECC_ROW</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">ECC_ROW</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

Table 12-360. ECC_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if ECC_CTRL[5] FORCE_N_ROW bit is set to 1h.

5 ECC_ERR_CTRL2 Register (Offset = 1Ch)

Return to Summary Table.

Contains data bit that needs to be flipped for forcing double-bit error

This register contains ECC error control bits for the selected ECC RAM

Figure 12-436. ECC_ERR_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
R/W-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_BIT1															
R/W-0h															

Table 12-362. ECC_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double-bit error has to be forced. The ECC_CTRL[4] FORCE_DED bit must be set to 1h for these values to take affect.
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped if single-bit error has to be forced. The ECC_CTRL[3] FORCE_SEC bit must be set to 1h for these values to take affect.

6 ECC_ERR_STAT1 Register (Offset = 20h)

Return to Summary Table.

Contains single-bit/double-bit error status and row corresponding to the error status.

This register contains ECC status bits for the selected ECC RAM

Figure 12-437. ECC_ERR_STAT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERROR	CLR_PARITY_ERROR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTRL_REG_ERROR	PARITY_ERROR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h	

Table 12-364. ECC_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R	0h	Indicates the bit position in the RAM data that is in error. For example, a value of 1h indicates that bit [1] in the RAM data is in error. This is valid only for single-bit errors. **Note** Not used in inject only mode. Always read as 0h.
15	CLR_CTRL_REG_ERROR	R/W	0h	Clear the CTR_REG_ERR bit. A write of 1h clears this bit and the CTR_REG_ERR bit, but if the redundancy protected bits in the ECC_CTRL register have not been written to a known state to correct the error, this flag is immediately set again.
14:13	CLR_PARITY_ERROR	R/W	0h	A write of a non-zero value to this field decrements the CLR_ECC_DED and ECC_DED fields by that value. If the value written is less than the current one, the non-correctable interrupt (ECC_DED_INT) stays asserted. If the value to decrement is more than the current value, the result is 0. 0h – No parity errors have occurred 1h – 1 parity has occurred 2h – 2 parity have occurred 3h – 3 or more parity have occurred
12	CLR_ECC_OTHER	R/W	0h	Clear other error status. 1h indicates a successive single-bit error. Writing 1h clears the status bit.

Table 12-364. ECC_ERR_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	CLR_ECC_DED	R/W	0h	A write of a non-zero value to this field decrements it and the ECC_DED field by that value. If the value written is less than the current one, the non-correctable interrupt (ECC_DED_INT) stays asserted. If the value to decrement is more than the current value, the result is 0. 0h – No DED errors have occurred 1h – 1 DED has occurred 2h – 2 DED have occurred 3h – 3 or more DED have occurred **Note** Not used in inject only mode. Always read as 0h.
9:8	CLR_ECC_SEC	R/W	0h	A write of a non-zero value to this field decrements it and the ECC_SEC field by that value. If the value written is less than the current one, the correctable interrupt (ECC_SEC_INT) stays asserted. If the value to decrement is more than the current value, the result is 0. 0h – No SEC errors have occurred 1h – 1 SEC has occurred 2h – 2 SEC have occurred 3h – 3 or more SEC have occurred **Note** Not used in inject only mode. Always read as 0h.
7	CTRL_REG_ERROR	R/W	0h	Indicates that a redundancy protected bit in the ECC_CTRL register has been flipped. This means that the redundancy logic have detected a state where not all values are the same and has defaulted to the reset state. Software needs to re-write these registers to a known state. A write of 1h sets this bit. 0h - Bit not flipped 1h - Bit flipped
6:5	PARITY_ERROR	R/W	0h	2-bit saturating counter for the number of parity errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_PARITY_ERR field to decrement this counter. 0h - No parity errors have occurred 1h - 1 parity error has occurred 2h - 2 parity errors have occurred 3h - 3 or more parity errors have occurred

Table 12-364. ECC_ERR_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ECC_OTHER	R/W	0h	1h - Indicates that successive single-bit errors have occurred while a write-back is still pending. Software can also write 1h to set the pending status and write 1h to the corresponding clear bit to clear the status. **Note** Not used in inject only mode. Always read as 0h.
3:2	ECC_DED	R/W	0h	2-bit saturating counter for the number of double-bit errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_ECC_SEC field to decrement this counter. 0h - No double-bit errors have occurred 1h - 1 double-bit has error occurred 2h - 2 double-bit have errors occurred 3h - 3 or more double-bit errors have occurred **Note** Not used in inject only mode. Always read as 0h.
1:0	ECC_SEC	R/W	0h	2-bit saturating counter for the number of single-bit errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_ECC_SEC field to decrement this counter. 0h - No single-bit errors have occurred 1h - 1 single-bit has occurred 2h - 2 single-bit have occurred 3h - 3 or more single-bit have occurred **Note** Not used in inject only mode. Always read as 0h.

7 ECC_ERR_STAT2 Register (Offset = 24h)

Return to Summary Table.

Contains data bit(s) corresponding to the single/double-bit error status.

This register contains ECC status bits for the selected ECC RAM

Figure 12-438. ECC_ERR_STAT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R-0h															

Table 12-366. ECC_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred. **Note** Not used in inject only mode. Always read as 0h.

8 ECC_ERR_STAT3 Register (Offset = 28h)

Return to Summary Table.

Contains error status information

This register contains ECC status bits for the selected ECC RAM

Figure 12-439. ECC_ERR_STAT3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLR_SVBUS_TIMEOUT	RESERVED							SVBUS_TIMEOUT	WB_PEND
R-0h						R-0h	R-0h							R/W-0h	R-0h

Table 12-368. ECC_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	CLR_SVBUS_TIMEOUT	R/W	0h	Clear ECC serial interface timeout error status 0h - No effect 1h - Clears this bit and the SVBUS_TIMEOUT_ERR bit
8:2	RESERVED	R	0h	Reserved
1	SVBUS_TIMEOUT	R/W	0h	ECC serial interface timeout error. Write a 1h to set the flag 0h - No timeout error 1h - Timeout error
0	WB_PEND	R	0h	Delayed write-back pending status. 0h - An ECC data correction write-back is not pending 1h - An ECC data correction write-back is pending **Note** Not used in inject only mode. Always read as 0h.

9 ECC_CBASS_REV Register (Offset = 10h)

Return to Summary Table.

Revision Register

The Revision Register contains the major and minor revisions.

Figure 12-440. ECC_CBASS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REV															
R-Xh															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV															
R-Xh															

Table 12-370. ECC_CBASS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	Xh	TI Internal data

10 ECC_CBASS_CTRL Register (Offset = 14h)

Return to Summary Table.

Control Register

The Control Register allows control over the checkers and injection.

Figure 12-441. ECC_CBASS_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECC_PATTERN				RESERVED		FORCE_N_BIT	FORCE_DE	FORCE_SE	RESERVED	ECC_CHECK	RESERVED
				R/W-0h						R/W-0h	R/W-0h	R/W-0h		R/W-1/0	

Table 12-372. ECC_CBASS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED		0h	Reserved
11:8	ECC_PATTERN	R/W	0h	The data pattern to use for injection. 0h = 0s 1h = Fs 2h = As 3h = 5s
7:6	RESERVED	R	0h	Always read as 0.
5	FORCE_N_BIT	R/W	0h	Update injection fields after the injection to setup for the next incremental injection. 0h = keep current settings after injection. 1h = increment to next bit or group after injection.
4	FORCE_DE	R/W	0h	Inject a double bit error when set. Will be automatically cleared when injection has completed.
3	FORCE_SE	R/W	0h	Inject a single bit error when set. Will be automatically cleared when injection has completed.
2	RESERVED	R/W	0h	Reserved
1	ECC_CHECK	R/W	1h	Enable checkers. 0h = Disabled 1h = Enabled
0	RESERVED	R	0h	Reserved.

11 ECC_CBASS_ERR_CTRL1 Register (Offset = 18h)

Return to Summary Table.

Error 1 Register

The Error 1 Register allows setting the injection data.

Figure 12-442. ECC_CBASS_ERR_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							ECC_BIT1								
							R/W-0h								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_GRP															
R/W-0h															

Table 12-374. ECC_CBASS_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24:16	ECC_BIT1	R/W	0h	First bit to inject an error.
15:0	ECC_GRP	R/W	0h	Group of checker to inject.

12 ECC_CBASS_ERR_CTRL2 Register (Offset = 1Ch)

Return to Summary Table.

Error 2 Register

The Error 2 Register allows setting the injection data.

Figure 12-443. ECC_CBASS_ERR_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							ECC_BIT2								
							R/W-0h								

Table 12-376. ECC_CBASS_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED			Reserved
8:0	ECC_BIT2	R/W	0h	Second bit to inject an error. Only valid if ECC_CBASS_CTRL[4] FORCE_DE is set.

13 ECC_CBASS_ERR_STAT1 Register (Offset = 20h)

Return to Summary Table.

Error Status 1 Register

The Error Status 1 Register allows reading the captured error data.

Figure 12-444. ECC_CBASS_ERR_STAT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_GRP															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INJ_UNC_PEND_CLR		INJ_COR_PEND_CLR		UNC_PEND_CLR		COR_PEND_CLR		INJ_UNC_PEND		INJ_COR_PEND		UNC_PEND		COR_PEND	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 12-378. ECC_CBASS_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_GRP	R	0h	Specific checker that reported the error. The exact mapping to signals is IP dependent.
15:14	INJ_UNC_PEND_CLR	R/W	0h	Number of injected uncorrected pending interrupts (same value as UNC_PEND). Writing decrements INJ_UNC_PEND by that value.
13:12	INJ_COR_PEND_CLR	R/W	0h	Number of injected corrected pending interrupts (same value as COR_PEND). Writing decrements INJ_COR_PEND by that value.
11:10	UNC_PEND_CLR	R/W	0h	Number of uncorrected pending interrupts (same value as UNC_PEND). Writing decrements UNC_PEND by that value.
9:8	COR_PEND_CLK	R/W	0h	Number of corrected pending interrupts (same value as COR_PEND). Writing decrements COR_PEND by that value.
7:6	INJ_UNC_PEND	R/W	0h	Number of injected uncorrected pending interrupts. Writing increments by that value.
5:4	INJ_COR_PEND	R/W	0h	Number of injected corrected pending interrupts. Writing increments by that value.
3:2	UNC_PEND	R/W	0h	Number of uncorrected pending interrupts. Writing increments by that value.
1:0	COR_PEND	R/W	0h	Number of corrected pending interrupts. Writing increments by that value.

14 ECC_CBASS_ERR_STAT2 Register (Offset = 24h)

Return to Summary Table.

Error Status 2 Register

The Error Status 2 Register allows reading the captured error data.

Figure 12-445. ECC_CBASS_ERR_STAT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR_TYPE															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_BIT															
R-0h															

Table 12-380. ECC_CBASS_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ERR_TYPE	R	0h	This field is not supported and can read any value and be ignored.
15:0	ERR_BIT	R	0h	Bit that caused the error. Always valid for EDC single bit corrected errors or redundant errors. Will identify parity segment number (but not the exact bit) with a parity error. Is not valid for EDC double bit errors.

Chapter 13

On-Chip Debug

This chapter describes the on-chip debug support.

Note

This chapter serves to provide the reader an understanding of the device's debug capability and does not provide the sufficient operational and integration details necessary to develop tooling support around it. Tools developers that wish to provide support for this device can contact TI for more information on how to obtain the appropriate documentation.

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13.1 On-Chip Debug Overview

This chapter describes the properties and capabilities of the various features available through the On-Chip Debug framework deployed on this device.

The On-Chip Debug framework enables various Debug and Trace use-cases, including:

- **JTAG Tooling** – Access to on-chip debug resources is supported by an IEEE 1149.1 (JTAG) compliant interface that is supported by an Arm® CoreSight™ DAP JTAG-DP.
- **Self-Hosted Tooling** – code running on programmable cores within the device is able to use on-chip debug resources to enable embedded tooling solutions.
- **PCB-level interconnect testing** – IEEE 1149.1 and IEEE 1149.6 compliant Boundary Scan supports product level integration testing
- **Low Power Operation** – When on-chip JTAG and debug management logic is in a low power state, activity sensed on the JTAG interface will cause this logic to be placed in a functional state.
- **Stop Mode debugging** – Debug of embedded processors is supported using various mechanisms that can halt the pipeline of a CPU. Breakpoints (Software and Hardware), Watchpoints, Cross-Triggering, and On-demand (e.g. user requested) halt request mechanisms may be supported based on the capabilities of a given processor.
- **Debug-aware Peripherals** – Peripheral awareness of processor execution state allows safe suspension of peripheral operation. Supported by select peripherals.
- **Synchronized Debug** – Wide deployment of Cross-Triggering allows multiple processors and/or debug elements to be grouped together to process various actions based on a common event occurrence.
- **Processor Trace** – Support for the generation of a trace stream with the encoding of processor state that may include some combination of program flow, timing details (execution and stall), and memory references (address and/or data) with the goal of facilitating processor state reconstruction for debug purposes.
- **Software Messaging Trace** – Support for software messaging trace where embedded code running within the device can be instrumented to use memory writes to send important debug information to a trace stream.
- **System Traffic Trace** – Strategically selected points in the SoC topology are instrumented with trace-capable bus probes that support transaction trace, read-latency monitoring, and throughput computation.
- **Trace Correlation (through timestamping)** – Support for the correlation of different trace streams is enabled through the use of a common global timestamp that is distributed to supported trace sources.
- **Trace data movement** – Trace data movement on chip is supported using standard Arm ATB trace infrastructure components. Concurrent use of the trace bus by multiple trace sources is supported, with each trace source identifiable through a unique ID. An Arm® CoreSight™ Trace Router supports sending a trace stream off-chip (TPIU), to dedicated memory on-chip (TBR), or broadcasted to both (TPIU + TBR).
- **On-Chip trace collection via dedicated buffer** – An on-chip trace buffer is supported by logic that implements capturing trace data until either the memory fills (stop-on-full, system-bridge) or continuously until a request to stop is received (circular buffer). Interleaving of multiple trace streams is made possible through the use of a standardized encoding that embeds trace data along with the corresponding trace source ID.
- **Trace export over TPIU** – Trace data is exported over device LVCMOS pins using a standard protocol that embeds trace data along with the corresponding trace source ID.
- **Trace export over USB** – The on-chip trace buffer is used as an intermediate buffer allowing trace data to be exported over an USB endpoint in real-time.

CAUTION

Debug features that are intrusive in nature may affect the ability of the system to meet critical real-time deadlines and should be used with caution.

13.2 On-Chip Debug Features

The On-Chip Debug framework provides a comprehensive hardware platform for a rich debug and development experience. The On-Chip Debug framework supports these features:

- An IEEE 1149.1 (JTAG and Boundary Scan) compliant device interface
- Cross-triggering and Debug boot mode device interface

- Trace port device interface
- Advanced power, reset, and clock management to facilitate debug across complex low power modes
- Breakpoint-based debug
- Cross-triggering
- Program flow trace
- System traffic monitoring trace
- Software instrumentation trace
- Trace export via trace port device interface
- Trace capture on-chip via dedicated buffer with options to support stop-on-full, circular-buffer, or data hand-off to various peripherals
- Arm® CoreSight™ compliant debug components deployed to streamline 3rd party tooling support

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

13.3 APB-AP Memory Map

The debug components are discoverable via the APB ROM Table. Table 13-1 summarizes the relevant portion of the APB-AP memory map:

Table 13-1. APB-AP Memory Map

APB-AP Address	Description
0x00001000	DebugSS CTI
0x00004000	DebugSS TPIU
0x00005000	DebugSS Trace Funnel
0x10000000	Cortex-A53SS *(ROM Table)*
0x10010000	Cortex-A53SS (Core 0 Debug)
0x10020000	Cortex-A53SS (Core 0 CTI)
0x10030000	Cortex-A53SS (Core 0 PMU)
0x10040000	Cortex-A53SS (Core 0 Trace)
0x10110000	Cortex-A53SS (Core 1 Debug)
0x10120000	Cortex-A53SS (Core 1 CTI)
0x10130000	Cortex-A53SS (Core 1 PMU)
0x10140000	Cortex-A53SS (Core 1 Trace)
0x10210000	Cortex-A53SS (Core 2 Debug)
0x10220000	Cortex-A53SS (Core 2 CTI)
0x10230000	Cortex-A53SS (Core 2 PMU)
0x10240000	Cortex-A53SS (Core 2 Trace)
0x10310000	Cortex-A53SS (Core 3 Debug)
0x10320000	Cortex-A53SS (Core 3 CTI)
0x10330000	Cortex-A53SS (Core 3 PMU)
0x10340000	Cortex-A53SS (Core 3 Trace)
0x1C000000	DebugCell SOC *(ROM Table)*
0x1C004000	DebugCell SOC (ATBREPLICATOR)
0x1C005000	DebugCell SOC (TBR)
0x1C006000	DebugCell SOC (CSCTI 0)
0x1C008000	DebugCell SOC (CSCTI 1)
0x1C009000	DebugCell SOC (CSCTI 2)
0x1C00A000	DebugCell SOC (CSCTI 3)

Table 13-1. APB-AP Memory Map (continued)

APB-AP Address	Description
0x1C00B000	DebugCell SOC (CSCTI 4)
0x1C00C000	DebugCell SOC (CSCTI 5)
0x1C00D000	DebugCell SOC (CSCTI 6)
0x1C00E000	DebugCell SOC (CSCTI 7)
0x1C00F000	DebugCell SOC (CSCTI 8)
0x1D200000	STMSS
0x1D400000	WKUP_R5FSS *(ROM Table)*
0x1D410000	WKUP_R5FSS (Core 0 Debug)
0x1D411000	WKUP_R5FSS (Core 0 PMU)
0x1D418000	WKUP_R5FSS (Core 0 CTI)
0x1D41C000	WKUP_R5FSS (Core 0 Trace)
0x1D800000	MCU_R5FSS *(ROM Table)*
0x1D810000	MCU_R5FSS (Core 0 Debug)
0x1D811000	MCU_R5FSS (Core 0 PMU)
0x1D818000	MCU_R5FSS (Core 0 CTI)
0x1D81C000	MCU_R5FSS (Core 0 Trace)

13.4 On-Chip Debug Functional Description

13.4.1 On-Chip Debug Block Diagram

A logical partitioning of the On-Chip Debug features deployed on this device is illustrated in Figure 13-1.

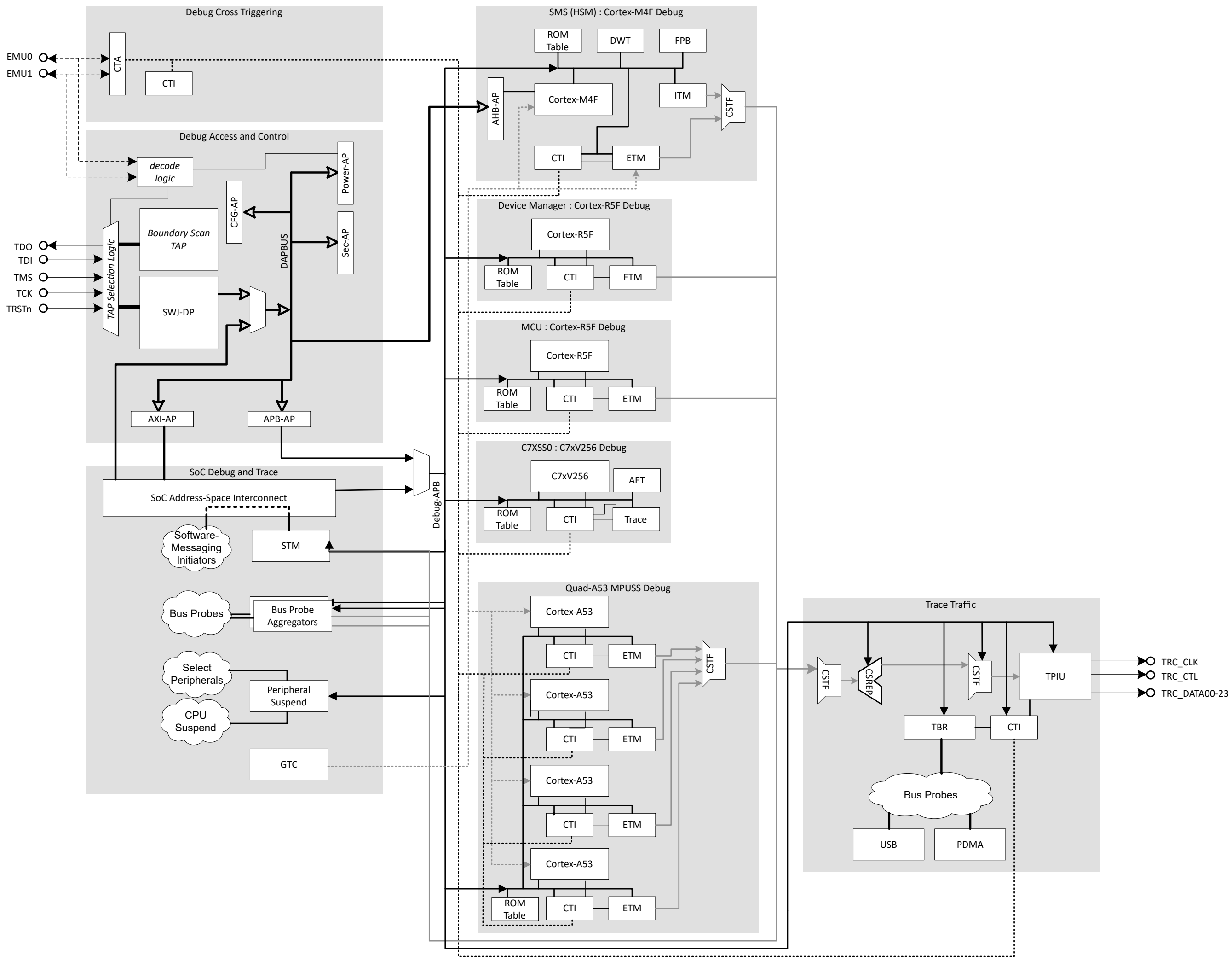

Figure 13-1. On-Chip Debug Block Diagram

Note

SMS0_TIFSM is intentionally omitted from the block diagram as it is not a debuggable entity.

13.4.2 Device Interfaces

AM62Dx On-Chip Debug features are supported through three device interfaces:

- **JTAG**: IEEE 1149.1 compliant interface that provides access to Boundary Scan and acts as the primary interface for off-chip access to On-Chip debug resources (See Section 13.4.2.1)
- **Trigger and Debug Boot Mode**: Multi-functional interface that supports product level cross-triggering and debug-related boot modes (See Section 13.4.7 , Section 13.4.4)
- **Trace Port**: Arm TPIU compliant Trace Port interface is used to facilitate export of trace (See Section 13.4.13)

Texas Instruments supports a variety of eXtended Development System (XDS™) JTAG controllers with various debug capabilities beyond only JTAG support. The following document is a good reference for guidelines: Emulation and Trace Headers. More information can also be found here:XDS Target Connection Guide .

The previous link connects to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4.2.1 JTAG Interface

Table 13-2. JTAG Interface Signals

SignalName	I/OType(1)	Description
TRSTn	I	*Test Reset*. Initializes and disables the test interface.
TCK	I	*Test Clock*. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device.
TMS	I	*Test Mode Select*. Controls the transitions of the test interface state machine.
TDI	I	*Test Data Input*. Supplies the data to the JTAG registers.
TDO	O/Z	*Test Data Output*. Used to serially output the data from the JTAG registers to the equipment controlling the test.

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

13.4.2.2 Trigger and Debug Boot Mode Interface

Table 13-3. Trigger and Debug Boot Mode Interface Signals

Signal Name	I/O Type(1)	Description
EMU0	I/O	Channel 0 trigger or boot mode select
EMU1	I/O	Channel 1 trigger or boot mode select

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

13.4.2.3 Trace Port Interface

Table 13-4. Trace Port Signals

Pin Name	TPIU Signal Name	I/O Type(1)	Description
TRC_CLK	TRACECLK	O	TraceClock
TRC_CTL	TRACECTL	O	TraceControl
TRC_DATA[*n*:0]	TRACEDATA[*n*:0]	O	TraceData [*n*:0]

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

Note

The Trace Port interface signals are associated with device pins that are multiplexed with other signal functions.

13.4.3 Debug and Boundary Scan Access and Control

On-Chip debug resources are made available through three mechanisms:

- JTAG access via DAP and related APs
- JTAG access via Boundary Scan TAP
- Embedded access to debug resources via SoC address space

DAP

Off-chip debug tools are able to access On-Chip debug resources via the JTAG interface when not in Boundary Scan mode (see below). A CoreSight™ Compliant DAP architecture provides access via a DP and a collection of APs:

- SWJ-DP: Arm® CoreSight™ compliant SWJ Debug Port provides support for a JTAG interface with a 4-bit IR

Note

Even though an SWJ-DP is implemented on-chip, only JTAG is supported. This device does not support SWD.

- APB-AP: Arm® CoreSight™ APB Access Port provides access to the Debug-APB address space which is the primary configuration space for On-Chip Debug resources.
- AXI-AP: Arm® CoreSight™ AXI Access Port provides access to the SoC address space, allowing visibility and control over system resources.
- Config-AP: TI Configuration AP supports access to SoC debug management registers
- Power-AP: TI Configuration AP supports advanced power, reset, and clock management. (See *Power, Reset, Clock Management*)

Table 13-5 describes the APSEL assignment for this device.

Table 13-5. DAP APSEL Assignment

APSEL	AP	Description
0	Config-AP	TI AP - Reserved
1	APB-AP	Provides access to Debug Config Plane
2	AXI-AP	Provides access to SoC Address Space
3	Power-AP	TI AP - Extended Power/Reset/Clock Control
4-5	Reserved	Reserved for future use
6	SEC-AP	TI AP - Authentication Interface
7	SMS TIFS M4F	
8	Reserved	Reserved for future use
9	SMS HSM M4F	
10-31	Reserved	Reserved for future use

Boundary Scan

This device supports boundary scan using an IEEE 1149.1 compliant JTAG TAP that is made visible through the use of a compliance-enable mode (see *Debug Boot Modes and Boundary Scan Compliance*). IEEE 1149.1 and 1149.6 Boundary Scan support are defined in device-specific BSDL files that can be found in the respective device's product folder on ti.com.

SoC Address Space

The device architecture provides access to On-Chip debug resources through the SoC Address Space. This includes access to all DAP Access Ports (APs) as well as the Debug-APB address space.

13.4.4 Debug Boot Modes and Boundary Scan Compliance

The EMU1 and EMU0 device pins are used to convey debug boot mode behavior and can also be used as part of a boundary scan compliance sequence to enable boundary scan features.

Debug Boot Mode

EMU1 and EMU0 are sampled when MCU_PORz is de-asserted and the decoded value determines the debug boot mode behavior as detailed in Table 13-6.

Table 13-6. Debug Boot Modes

Sample Time	EMU1	EMU0	Boot Mode	Behavior
MCU_PORz deassertion	0	0	Reserved	Reserved for future use
	0	1	Reserved	Reserved for future use

Table 13-6. Debug Boot Modes (continued)

Sample Time	EMU1	EMU0	Boot Mode	Behavior
	1	0	Wait-In-Reset (WIR)	Device will remain quiescent until a debug connection is established and the debugger releases WIR. This mode is useful for debugging boot sequences.
	1	1	Normal	Device boots normally. Debug can connect at any time but the context will be post-boot.

Boundary Scan Compliance

EMU1 and EMU0 are sampled when TRSTz is de-asserted and the decoded value determines the debug boot mode behavior as detailed in Table 13-7.

Table 13-7. Boundary Scan Compliance

Sample Time	EMU1	EMU0	Boundary Scan Compliance	Behavior
TRSTn deassertion	0	1	Boundary Scan Enabled	The device's Boundary Scan TAP is connected to the device's JTAG interface.
	0	0		
	1	0	Boundary Scan Disabled	The device's SWJ-DP is connected to the device's JTAG interface.
	1	1		

13.4.5 Peripheral Suspend

Some peripherals on the device include support for a debug suspend capability that allows the peripheral's behavior to alter when an assigned CPU enters the debug suspend state. In order to use this feature, it must be enabled within the peripheral and a connection made between the desired suspend source (CPU) and the suspend destination (peripheral) of interest.

Details on the debug suspend feature for a specific peripheral, including how to enable it, is covered in the associated peripheral section.

On this device, there is a dedicated interrupt router (INTR) (DBGSUSPENDROUTER0 that supports the routing of a suspend source to a suspend destination. Details on the assignment of DBGSUSPENDROUTER0 inputs and outputs are provided .

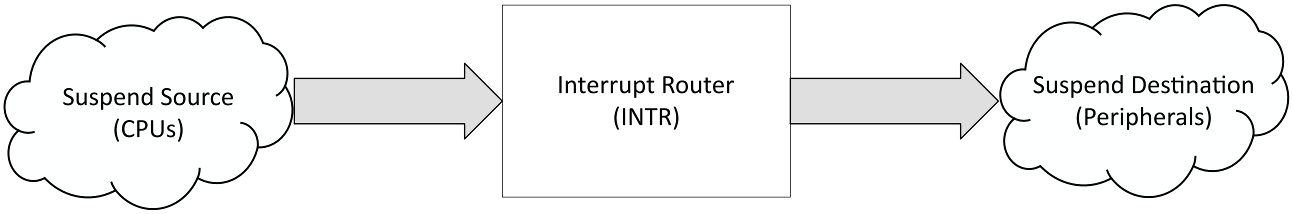

Figure 13-2. Peripheral Suspend Support

Table 13-8. Suspend Source Assignment

Index	Suspend Source	Description
1	A53SS0_0	A53SS0 Core 0
2	A53SS0_1	A53SS0 Core 1
3	A53SS0_2	A53SS0 Core 2
4	A53SS0_3	A53SS0 Core 3
9	C7X256V0	C7x DSP / Deep Learning Acc.
23	WKUP_R5FSS	Device Management Cortex R5F
24	MCU_M4FSS	MCU M4F
26	SMS0_HSM	SMS HSM

Table 13-9. Suspend Destination Assignment

Index	Suspend Destination	Description
0	WKUP_GTC0	Global Time Counter
1	CPSW0	Ethernet Switch (SoC)
2	DMSS	DMA SS (SoC)
3	DMSS_HSM	SA3SS DMSS_HSM
4	DMSS_CSI	DMA SS (CSI-RX)
7-5	Reserved	Reserved
8	TIMER0	Dual Mode Timer (Main)
9	TIMER1	
10	TIMER2	
11	TIMER3	
12	TIMER4	
13	TIMER5	
14	TIMER6	
15	TIMER7	
16	MCU_TIMER0	Dual Mode Timer (MCU)
17	MCU_TIMER1	
18	MCU_TIMER2	
19	MCU_TIMER3	
20	Reserved	Reserved
21	WKUP_TIMER0	Dual Mode Timer (Wakeup)
22	WKUP_TIMER1	
23	Reserved	Reserved
24	EPWM0	Enhanced PWM (Main)
25	EPWM1	
26	EPWM2	
27	Reserved	Reserved
28	MCAN0	MCAN (Main)
29	MCU_MCAN0	MCAN (MCU)
30	MCU_MCAN1	
31	Reserved	Reserved
32	MCRC64_0	CRC (Main)
33	MCU_MCRC64_1	CRC (MCU)
34	Reserved	Reserved
35	I2C0	I2C (Main)
36	I2C1	
37	I2C2	
38	I2C3	
39	MCU_I2C0	I2C (MCU)
40	WKUP_I2C0	I2C (Wakeup)
41	Reserved	Reserved
42	ECAP0	ECAP (Main)
43	ECAP1	
44	ECAP2	
45	EQEP0	EQEP (Main)
46	EQEP1	

Table 13-9. Suspend Destination Assignment (continued)

Index	Suspend Destination	Description
47	EQEP2	
49-48	Reserved	Reserved
50	PDMA0	Peripheral DMA
51	PDMA1	
52	PDMA2	
53	Reserved	Reserved
54	RTI2	Real-time Interrupt (A53)
55	RTI3	
56	RTI0	
57	RTI1	
58	RTI4	Real-time Interrupt (C71)
59	MCU_RTI0	Real-time Interrupt (MCU)
60	WKUP_RTI0	Real-time Interrupt (DM)
127-61	Reserved	Reserved

13.4.6 Power, Reset, Clock Management

This device includes advanced power, reset, and clock management debug capabilities, including:

- **Wakeup support for debug logic**: logic within the device is able to sense JTAG activity and ensure that debug logic is on and able to service JTAG requests.
- **Reset isolation**: critical configuration and trace datapaths and logic are not sensitive to warm reset
- **Configuration independence**: debug configuration occurs over a debug-only interconnect, separate from SoC traffic to ensure debug logic remains available even during deadlock scenarios.
- **Power-AP**: a CoreSight™ compliant Access Port (AP) developed by TI that provides a standard interface for debug tooling to access status and control over power, reset, and clocking for the system and various LPSC-defined sub-domains.

13.4.7 Debug Cross Triggering

This device supports an Arm® CoreSight™ compliant four-channel programmable on-chip Cross Triggering network. In addition to the four-channel on-chip network, this device implements two channels of product level triggering via the EMU0 and EMU1 device pins.

Conceptually, each channel of Cross Triggering can be viewed as mapping of a user-defined set of events to a user-defined set of actions, where the occurrence of any event in the set-of-events results in the generation of the set-of-actions. Table 13-10 provides a domain-level summary of the supported events and actions.

Table 13-10. Domain-Level Summary of Triggering Capability

Domain	Events	Actions
Product-Level	Zero detected on EMU0 input pin	EMU0 output pin driven to Zero
	Zero detected on EMU1 input pin	EMU1 output pin driven to Zero
SoC Debug	TBR Acquisition Complete	TPIU insert trigger packet
	TBR Embedded buffer is full	TPIU start flush process
	System reset asserted	TBR insert trigger packet
	Bus Probe-n match	TBR start flush process
	STM write to a TRIG location	Bus Probe-n Start
	STM write to a trigger-enabled stimulus port	Bus Probe-n Stop
SMS0_HSM	SMS0_HSM has halted	SMS0_HSM – halt request
	ETM External Out (EXTOUT) trigger	SMS0_HSM – resume request
	--	ETM External In (EXTIN) trigger

Table 13-10. Domain-Level Summary of Triggering Capability (continued)

Domain	Events	Actions
MCU_R5F	MCU_R5F has halted	MCU_R5F - halt request
	PMU generated interrupt	MCU_R5F - resume request
	ETM External Out (EXTOUT) trigger	ETM External In (EXTIN) trigger
WKUP_R5F	WKUP_R5F has halted	WKUP_R5F – halt request
	PMU generated interrupt	WKUP_R5F – resume request
	ETM External Out (EXTOUT) trigger	ETM External In (EXTIN) trigger
A53SS0	A53SS0 core-n has halted	A53SS0 core-n – halt request
	PMU generated interrupt	A53SS0 core-n – resume request
	ETM generated trigger	CTI interrupt
	--	ETM External In (EXTIN) trigger
C7XSS0	C7XSS0 core has halted	C7XSS0 core - halt request
	--	C7XSS0 core - resume request
	C7XSS0 AET External Out trigger	C7XSS0 AET External In trigger

13.4.8 WKUP_R5F and MCU_R5F Debug

Both WKUP_R5F and MCU_R5F include an Arm Cortex R5F with embedded debug capability, including:

- Independent debug configuration
- ROM Table
- Basic debug functionality
- Cross Triggering
- PMU: Performance Monitor Unit
- ETM: Embedded Trace Macrocell

A summary of the WKUP_R5F and MCU_R5F debug capabilities is detailed in Table 13-11.

Table 13-11. WKUP_R5F and MCU_R5F Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM table	Facilitates discovery of debug resources within debug configuration address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Hardware breakpoints	Eight Debug Breakpoint resources support hardware breakpoints
	Hardware watchpoints	Eight Debug Watchpoint resources support data address breakpoints
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU
	Vector catch	Halting in response to an exception
	Arm TrustZone debug authentication	Provisioning for DBGEN and NIDEN
Cross Triggering	Debug state	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	PMU	PMU interrupt trigger
	ETM	Five ETM external triggers (one ETM Trigger, two external out event triggers, two external in event triggers)
PMU	Profile Counters	Three counters can be used to count different events available for gathering statistics on the operation of the processor and memory system
	Cycle Counter	One dedicated counter available for counting CPU clock cycles

Table 13-11. WKUP_R5F and MCU_R5F Debug Capabilities (continued)

Capability	Feature	Notes
ETM	Triggering Infrastructure	Comprehensive triggering infrastructure supports use of comparators (address, data value, context ID), counters, sequencer state, an external inputs and outputs to control the enabling of trace.
	Instruction trace	Supports tracing of instruction flow
	Cycle-accurate tracing	Supports inclusion of a precise cycle count of executed instructions.
	Branch broadcast tracing	Support for tracing branch address details even in circumstances where that information might be discoverable from object code
	Data tracing	Support for data address and data value tracing

13.4.9 SMS0_HSM Debug

SMS0_HSM includes an Arm Cortex M4F with embedded debug capability, including:

- Independent debug configuration via AHB-AP
- ROM Table
- Basic debug functionality
- Cross Triggering
- DWT : Data Watchpoint and Trace
- FPB : Flash Patch Breakpoint
- ITM : Instrumentation Trace Macrocell
- ETM : Embedded Trace Macrocell

A summary of the SMS0_HSM debug capability is detailed in Table 13-12.

Table 13-12. SMS0_HSM Debug Capability

Capability	Feature	Notes
Basic Debug	AHB-AP	AHB-AP provides access to resources
	ROM table	Facilitates discovery of debug resources within AHB-AP address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Core register access	Access to processor core registers
	Vector catch	Halting in response to an exception
	Software breakpoints	Software breakpoints are supported via opcode replacement
	System memory access	Access to M4F address space is supported via AHB-AP
	Arm TrustZone debug authentication	Provisioning for DBGEN and NIDEN
Cross Triggering	Cross Triggering	Cross Triggering support via CoreSight CTI
DWT	Watchpoints	Four comparators implemented that can be configured to support watchpoints, data address trace, ETM signaling and PC sampling
	Data address trace	
	ETM signaling	
	PC sampling trace	
	Cycle count matching	
	Performance counting	Profiling counter support provides visibility into instruction cycle count, exception overhead, sleep overhead, load-store overhead, and folded instruction count
FPB	Hardware breakpoints	Six instruction address comparators support hardware breakpoints

Table 13-12. SMS0_HSM Debug Capability (continued)

Capability	Feature	Notes
	Remapping of literal and instruction fetch accesses	Two comparators support address remapping of literal or instruction accesses to facilitate software patching
ITM	Software trace	Software writes to ITM stimulus registers provoke the generation of trace packets that convey the values written
	DWT hardware trace	Support for conveying DWT output using trace
	Timestamping	Support for attaching a local timestamp to trace traffic
	Global timestamping	Support for attaching a global timestamp to trace traffic
ETM	Program execution trace	Support for tracing instruction execution
	Global timestamping	Support for attaching a global timestamp to trace traffic

13.4.10 A53SS0 Debug

The A53SS0 is a multi-core Arm Cortex-A53 subsystem with embedded debug capability and features, including:

- Independent debug configuration
- ROM Table
- Basic debug functionality
- Cross Triggering
- PMU: Performance Monitor Unit
- ETM: Embedded Trace Macrocell

A summary of the A53SS0 debug capabilities and features is detailed in Table 13-13.

Table 13-13. A53SS0 Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM table	Facilitates discovery of debug resources within debug configuration address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Hardware breakpoints	Six Debug Breakpoint resources support hardware breakpoints
	Hardware watchpoints	Four Debug Watchpoint resources support data address breakpoints
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU
	Vector catch	Halting in response to an exception
	Arm® TrustZone® debug authentication	Provisioning for DBGEN, NIDEN, SPIDEN, SPNIDEN, SUIDEN, and SUNIDEN
Cross Triggering	Debug state	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	PMU	PMU interrupt trigger
	ETM	Four ETM external triggers
	CPU	CTI interrupt into CPU
PMU	Profile Counters	Six counters can be used to count different events available for gathering statistics on the operation of the processor and memory system
	Cycle Counter	One dedicated counter available for counting CPU clock cycles

Table 13-13. A53SS0 Debug Capabilities (continued)

Capability	Feature	Notes
ETM	Instruction trace with cycle counting	Support for tracing instruction execution with timing information
	Branch broadcast tracing	Support for tracing branch address details even in circumstances where that information might be discoverable from object code
	Return stack tracing	Support for tracing of the return stack
	Stall Control	Support for stalling the A53 processor to avoid ETM overflows
	Global timestamping	Support for attaching a global timestamp to trace traffic

13.4.11 C7XSS0 Debug

The C7XSS0 is a single-core C7xV-256 subsystem with embedded debug capability and features, including:

- Independent debug configuration
- Basic debug functionality
- Cross Triggering
- AET: Advanced Event Triggering
- Processor Trace
- Traffic Monitoring Trace

A summary of the C7XSS0 debug capabilities and features is detailed in Table 13-14.

Table 13-14. C7XSS0 Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM table	Facilitates discovery of debug resources within debug configuration address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Hardware breakpoints	Four Debug Breakpoint resources support hardware breakpoints
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU
	Arm TrustZone debug authentication	Provisioning for DBGEN, NIDEN, SPIDEN, SPNIDEN, SUIDEN, and SUNIDEN
Cross Triggering	Debug state	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	AET	Two channels of AET external triggers (input and output)
AET	Profile Counters	Two counters can be used to count different events available for gathering statistics on the operation of the processor and memory system. Includes watermark support.
	Application Context Sensitive Triggering	Supports generation of events based on the context of application execution (e.g. Thread-ID, Virtual Machine ID, Program bus activity, Memory bus activity)
	Visibility and detection of events	provided by CPU, Subsystem, and SOC
	Range detection	of Program and Memory bus activity
	Programmable State Machine	supports complex, state-based event detection
	Trace Stream Filtering / Windowing	supports the management of trace windows
Trace	Historical Record	Creates a customized (based on trace stream filtering/windowing) historical account of the CPU’s behavior through the use of different types of trace streams
	Program Flow Trace	records program flow execution, including discontinuities resulting from branches, interrupts, or exceptions
	Cycle Accurate Trace	records cycle-accurate timing information
	Memory Reference Trace	records data log activity (address, data, address and data)

Table 13-14. C7XSS0 Debug Capabilities (continued)

Capability	Feature	Notes
	Event Trace	records information about the occurrence, duration, or relationship of one or more events
	Stream Buffer Parameter Trace	records the parameters used to start a stream buffer operation allowing off-line reconstruction
	Application Context Trace	records changes in the context of the application (virtual machine ID, thread-ID)
	Stall Control	Support for stalling the C71 processor to avoid Trace overflows
	Global timestamping	Support for attaching a global timestamp to trace traffic
	Traffic Monitoring	Traffic monitoring bus probes are deployed within C7XSS0 memory subsystem

13.4.12 SoC Debug and Trace

This device includes debug capabilities deployed at the system level, including:

- Software messaging trace
- Debug-aware peripherals
- Traffic monitoring with bus probes
- Global timestamping for trace

More details for each of these capability areas can be found in the corresponding sections below.

13.4.12.1 Software Messaging Trace

Software messaging trace is supported on this device by an MIPI STP-V2 compliant Arm® CoreSight™ STM with supporting logic that maps initiator IDs to specific STP Major Source IDs. The following device initiators support software messaging:

- A53SS0 cores
- C7XSS0
- MCU_R5F
- WKUP_R5F
- SMS0_HSM
- DMSS BCDMA
- DMSS PktDMA
- DAP AXI-AP

13.4.12.2 Debug-Aware Peripherals

Select peripherals support a debug feature that allows them to react to the debug state of a controlling processor. For instance, a timer peripheral that is allocated to a particular processor could be configured to stop counting when the associated processor is in the halted state.

This device includes programmable support for shared peripherals that allows the developer to select the processor whose debug state a given peripheral should receive. Peripherals that are debug aware include programmable support to enable or disable sensitivity to debug.

A list of the processors and peripherals that support this debug model can be found in Table 13-15.

Table 13-15. Debug-Aware Peripheral Support

Supported Processors	Supported Peripherals
A53SS0 cores	GTC
C7XSS0	CPSW3G
MCU_R5F	DMSS
WKUP_R5F	SA3SS
SMS0_HSM	TIMER instances
SMS0_TIFS	EPWM instances
--	MCAN instances

Table 13-15. Debug-Aware Peripheral Support (continued)

Supported Processors	Supported Peripherals
--	I2C instances
--	MCRC64 instances
--	ECAP instances
--	EQEP instances
--	PDMA_SPI
--	PDMA_UART
--	PDMA_MCASP
--	RTI/WWDT instances(1)

(1) RTI/WWDT suspend is associated with the processor that it is allocated to

13.4.12.3 Traffic Monitoring With Bus Probes

Traffic monitoring bus probes are deployed at strategic points in the system interconnect and support the following capabilities:

- MIPI STP-V2 compliant trace messaging support with global timestamping support
- Latency Statistics Collection: Statistics on the timeliness of responses to read requests are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Throughput Statistics Collection: Statistics on the amount of data moving across an interface are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Transaction Trace: Information about specific transactions occurring at a probed location are captured and encoded into a trace message
- Complex filtering support allows discrimination of traffic being monitored
- Cross-Trigger support for enabling and disabling probe monitoring

Table 13-16 details the locations in the system interconnect that are probed:

Table 13-16. Bus Probe Points

Probe Point	Bus Monitoring Details
A53SS0 Write Initiator	Provides visibility to all write requests initiated by A53SS0
A53SS0 Read Initiator	Provides visibility to all read requests initiated by A53SS0
A53SS0 ACP Target	Monitors traffic to the A53SS0 ACP port
DDR Target	Monitors RT and Non-RT traffic to DDR
GMPC Target	Monitors traffic to GPMC
FSS Target	Monitors traffic to FSS0
Peripheral CBASS Targets	Monitors traffic to these targets: ECAP# EQEP# I2C# MCAN# PDMA_SPI PDMA_UART SPI# UART#

Table 13-16. Bus Probe Points (continued)

Probe Point	Bus Monitoring Details
McASP CBASS Targets	Monitors traffic to these targets: EPWM# MCASP#
WKUP CBASS Targets	Monitors traffic from MAIN to WKUP, including these targets: WKUP_GTC WKUP_R5F WKUP_TIMER# WKUP_RTI WKUP_I2C0 WKUP_CTRL_MMR0 WKUP_VTM0
GPU Write Initiator	Provides visibility to all write requests initiated by GPU
GPU Read Initiator	Provides visibility to all read requests initiated by GPU
C7XSS0 MDMA Initiator	Provides visibility to access initiated by C7XSS0 MDMA port
C7XSS0 SDMA Target	Provides visibility to all requests to C7XSS0 SDMA port
C7XSS0 Memory Subsystem	Monitors traffic within L2, including accesses: to CMMU From L2 to L1D$ From L1D$ to L2 From L1I$ to L2 Streaming Buffer to L2
On-Chip SRAM	Monitors traffic to 64KB of MAIN OCSRAM
MCU SRAM	Monitors traffic to 512KB of MCU OCSRAM
MCU CBASS Targets	Monitors traffic from MAIN to MCU, including these targets: MCU_R5F MCU_SPI# MCU_MCRC64 MCU_UART0 MCU_MCAN# MCU_TIMER# MCU_DCC0 MCU_RTI0 MCU_I2C0

Table 13-16. Bus Probe Points (continued)

Probe Point	Bus Monitoring Details
Infrastructure CBASS Targets	Monitors traffic to these targets: CMP_EVENT_INTROUTER CTRL_MMR DCC# DDPA DFTSS ESM PSRAM# GPIO# EFUSE GPIOMUX_INTROUTER PADCFG_CTRL_MMR0 PLL_MMR0 PLLCTRL PSC TIMESYNC_EVENT_ROUTER

13.4.12.4 Global Timestamping for Trace

Support for a global timestamp for use by debug is enabled by a 48-bit continuous timestamp managed by the device’s GTC. This 48-bit global timestamp is readable by embedded software, via the GTC, and distributed across the device to various trace sources where it is used as a time reference when timestamping trace streams. Trace sources that support global timestamping, include:

- A53SS0 cores: ETM
- C7XSS0: Trace
- SMS0_HSM: ITM and ETM
- STM
- Bus Probes

13.4.13 Trace Traffic

Trace traffic originates from a trace source, is distributed across the device using Arm® CoreSight™ compliant trace infrastructure components, and reaches one of two possible trace sinks.

13.4.13.1 Trace Sources

A summary of the trace sources present on this device is included in Table 13-17.

Table 13-17. Trace Sources

Domain	Trace Source
SoC Debug	Bus Probes
	STM
MCU_R5F	ETM
WKUP_R5F	ETM
A53SS0	ETM (each core)
C7XSS0	Trace

13.4.13.2 Trace Infrastructure

Trace distribution is accomplished using standard Arm® CoreSight™ compliant trace infrastructure components:

- CoreSight™ Trace Funnels (CSTF): Non-programmable CSTFs are used at points of interleaving where multiple trace sources converge and form a single stream of trace traffic. This device includes one instance of a programmable CSTF that is deployed immediately before the TPIU.
- CoreSight™ Trace Replicator (CSREP): A programmable CSREP is used as a routing device, that can be used to forward trace traffic, based on its ID, to one, both, or none of the device trace sinks.

13.4.13.3 Trace Sinks

Two trace sinks are supported on this device:

- Arm® CoreSight™ TPIU: TPIU supports export of trace off-chip via LVCMOS device pins (See 1.3.3.3) for capture by an external receiver.
- TI Trace Buffer Router (TBR) with 64KB of storage: the TBR can function as a trace buffer or as a system bridge. As a trace buffer, the TBR can be setup to capture trace data until the internal buffer fills or it can operate as a circular buffer that will capture continuously. When configured as a system bridge the TBR's storage becomes an elastic buffer that supports the concurrent queueing and dequeuing of trace traffic. The system bridge mode supports interrupt and event notification capabilities that support integration with device level CPUs and/or DMAs to support a variety of use cases, including, for e.g., relocation of trace data to DDR and off-chip export over USB.

13.4.14 Application Support

TI includes a set of system level debug facilities in the Debug Subsystem of devices known as Chip Tools (CTools). For easy integration of A53 processor trace and system trace into applications, a set of libraries commonly referred to as CToolsLib are provided. CToolsLib is a collection of embedded target APIs/libraries focused on enabling easy access to the CTools. CToolsLib encompasses the following libraries to assist in trace integration:

- STM Library
- CP Tracer Library
- TBR Library
- ETM Library

For more information about these libraries, downloadable files, and other useful links, please visit the CToolsLib Wiki site.

The previous link connects to TI community resources. Linked contents are provided "AS IS" by the respectivecontributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Chapter 14

Registers

14.1 System Interconnect Registers

14.1.1 cbass

cbass

14.1.1.1 cbass Summaries

cbass Summaries

Table 14-1. CBASS_ERR Registers, Base Address=3A00 0000h, Length=1024

Offset	Length	Register Name	CBASS0 Physical Address
0h	32	CBASS_ERR_PID	3A00 0000h
4h	32	CBASS_ERR_DESTINATION_ID	3A00 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	3A00 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	3A00 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	3A00 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	3A00 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	3A00 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	3A00 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	3A00 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	3A00 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	3A00 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	3A00 005Ch
60h	32	CBASS_ERR_EOI	3A00 0060h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384

Offset	Length	Register Name	CBASS0 Physical Address
0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_CONTROL	4500 0000h
4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0	4500 0004h
8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1	4500 0008h
Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2	4500 000Ch
10h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_L	4500 0010h
14h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_H	4500 0014h
18h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_L	4500 0018h
1Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_H	4500 001Ch
20h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_CONTROL	4500 0020h
24h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0	4500 0024h
28h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1	4500 0028h
2Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2	4500 002Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
30h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_L	4500 0030h
34h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_H	4500 0034h
38h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_L	4500 0038h
3Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_H	4500 003Ch
40h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_CONTROL	4500 0040h
44h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0	4500 0044h
48h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1	4500 0048h
4Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2	4500 004Ch
50h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_L	4500 0050h
54h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_H	4500 0054h
58h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_L	4500 0058h
5Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_H	4500 005Ch
60h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_CONTROL	4500 0060h
64h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0	4500 0064h
68h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1	4500 0068h
6Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2	4500 006Ch
70h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_L	4500 0070h
74h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_H	4500 0074h
78h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_L	4500 0078h
7Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_H	4500 007Ch
80h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_CONTROL	4500 0080h
84h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0	4500 0084h
88h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1	4500 0088h
8Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2	4500 008Ch
90h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_L	4500 0090h
94h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_H	4500 0094h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
98h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_L	4500 0098h
9Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_H	4500 009Ch
A0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_CONTROL	4500 00A0h
A4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0	4500 00A4h
A8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1	4500 00A8h
ACh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2	4500 00ACh
B0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_L	4500 00B0h
B4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_H	4500 00B4h
B8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_L	4500 00B8h
BCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_H	4500 00BCh
C0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_CONTROL	4500 00C0h
C4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0	4500 00C4h
C8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1	4500 00C8h
CCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2	4500 00CCh
D0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_L	4500 00D0h
D4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_H	4500 00D4h
D8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_L	4500 00D8h
DCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_H	4500 00DCh
E0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_CONTROL	4500 00E0h
E4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0	4500 00E4h
E8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1	4500 00E8h
ECh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2	4500 00ECh
F0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_L	4500 00F0h
F4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_H	4500 00F4h
F8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_L	4500 00F8h
FCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_H	4500 00FCh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
400h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL	4500 0400h
404h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0	4500 0404h
408h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1	4500 0408h
40Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2	4500 040Ch
410h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L	4500 0410h
414h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H	4500 0414h
418h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L	4500 0418h
41Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H	4500 041Ch
420h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL	4500 0420h
424h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0	4500 0424h
428h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1	4500 0428h
42Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2	4500 042Ch
430h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L	4500 0430h
434h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H	4500 0434h
438h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L	4500 0438h
43Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H	4500 043Ch
440h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL	4500 0440h
444h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0	4500 0444h
448h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1	4500 0448h
44Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2	4500 044Ch
450h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L	4500 0450h
454h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H	4500 0454h
458h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L	4500 0458h
45Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H	4500 045Ch
460h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL	4500 0460h
464h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0	4500 0464h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
468h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1	4500 0468h
46Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2	4500 046Ch
470h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L	4500 0470h
474h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H	4500 0474h
478h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L	4500 0478h
47Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H	4500 047Ch
480h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL	4500 0480h
484h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0	4500 0484h
488h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1	4500 0488h
48Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2	4500 048Ch
490h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L	4500 0490h
494h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H	4500 0494h
498h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L	4500 0498h
49Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H	4500 049Ch
4A0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL	4500 04A0h
4A4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0	4500 04A4h
4A8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1	4500 04A8h
4ACh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2	4500 04ACh
4B0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L	4500 04B0h
4B4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H	4500 04B4h
4B8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L	4500 04B8h
4BCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H	4500 04BCh
4C0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL	4500 04C0h
4C4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0	4500 04C4h
4C8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1	4500 04C8h
4CCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2	4500 04CCh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
4D0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L	4500 04D0h
4D4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H	4500 04D4h
4D8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L	4500 04D8h
4DCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H	4500 04DCh
4E0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL	4500 04E0h
4E4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0	4500 04E4h
4E8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1	4500 04E8h
4ECh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2	4500 04ECh
4F0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L	4500 04F0h
4F4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H	4500 04F4h
4F8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L	4500 04F8h
4FCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H	4500 04FCh
500h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_CONTROL	4500 0500h
504h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0	4500 0504h
508h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1	4500 0508h
50Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2	4500 050Ch
510h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_L	4500 0510h
514h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_H	4500 0514h
518h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_L	4500 0518h
51Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_H	4500 051Ch
520h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_CONTROL	4500 0520h
524h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0	4500 0524h
528h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1	4500 0528h
52Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2	4500 052Ch
530h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_L	4500 0530h
534h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_H	4500 0534h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
538h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_L	4500 0538h
53Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_H	4500 053Ch
540h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_CONTROL	4500 0540h
544h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0	4500 0544h
548h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1	4500 0548h
54Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2	4500 054Ch
550h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_L	4500 0550h
554h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_H	4500 0554h
558h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_L	4500 0558h
55Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_H	4500 055Ch
560h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_CONTROL	4500 0560h
564h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0	4500 0564h
568h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1	4500 0568h
56Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2	4500 056Ch
570h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_L	4500 0570h
574h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_H	4500 0574h
578h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_L	4500 0578h
57Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_H	4500 057Ch
580h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_CONTROL	4500 0580h
584h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0	4500 0584h
588h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1	4500 0588h
58Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2	4500 058Ch
590h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_L	4500 0590h
594h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_H	4500 0594h
598h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_L	4500 0598h
59Ch	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_H	4500 059Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
5A0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_CONTROL	4500 05A0h
5A4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0	4500 05A4h
5A8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1	4500 05A8h
5ACh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2	4500 05ACh
5B0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_L	4500 05B0h
5B4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_H	4500 05B4h
5B8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_L	4500 05B8h
5BCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_H	4500 05BCh
5C0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_CONTROL	4500 05C0h
5C4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0	4500 05C4h
5C8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1	4500 05C8h
5CCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2	4500 05CCh
5D0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_L	4500 05D0h
5D4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_H	4500 05D4h
5D8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_L	4500 05D8h
5DCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_H	4500 05DCh
5E0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_CONTROL	4500 05E0h
5E4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0	4500 05E4h
5E8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1	4500 05E8h
5ECh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2	4500 05ECh
5F0h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_L	4500 05F0h
5F4h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_H	4500 05F4h
5F8h	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_L	4500 05F8h
5FCh	32	CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_H	4500 05FCh
800h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL	4500 0800h
804h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0	4500 0804h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
808h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1	4500 0808h
80Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2	4500 080Ch
810h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L	4500 0810h
814h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H	4500 0814h
818h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L	4500 0818h
81Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H	4500 081Ch
820h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL	4500 0820h
824h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0	4500 0824h
828h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1	4500 0828h
82Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2	4500 082Ch
830h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L	4500 0830h
834h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H	4500 0834h
838h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L	4500 0838h
83Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H	4500 083Ch
840h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL	4500 0840h
844h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0	4500 0844h
848h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1	4500 0848h
84Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2	4500 084Ch
850h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L	4500 0850h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
854h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H	4500 0854h
858h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L	4500 0858h
85Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H	4500 085Ch
860h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL	4500 0860h
864h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0	4500 0864h
868h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1	4500 0868h
86Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2	4500 086Ch
870h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L	4500 0870h
874h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H	4500 0874h
878h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L	4500 0878h
87Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H	4500 087Ch
880h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL	4500 0880h
884h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0	4500 0884h
888h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1	4500 0888h
88Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2	4500 088Ch
890h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L	4500 0890h
894h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H	4500 0894h
898h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L	4500 0898h
89Ch	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H	4500 089Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
8A0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL	4500 08A0h
8A4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0	4500 08A4h
8A8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1	4500 08A8h
8ACh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2	4500 08ACh
8B0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L	4500 08B0h
8B4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H	4500 08B4h
8B8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L	4500 08B8h
8BCh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H	4500 08BCh
8C0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL	4500 08C0h
8C4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0	4500 08C4h
8C8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1	4500 08C8h
8CCh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2	4500 08CCh
8D0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L	4500 08D0h
8D4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H	4500 08D4h
8D8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L	4500 08D8h
8DCh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H	4500 08DCh
8E0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL	4500 08E0h
8E4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0	4500 08E4h
8E8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1	4500 08E8h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
8ECh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2	4500 08ECh
8F0h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L	4500 08F0h
8F4h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H	4500 08F4h
8F8h	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L	4500 08F8h
8FCh	32	CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H	4500 08FCh
C00h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_CONTROL	4500 0C00h
C04h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0	4500 0C04h
C08h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1	4500 0C08h
C0Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2	4500 0C0Ch
C10h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_L	4500 0C10h
C14h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_H	4500 0C14h
C18h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_L	4500 0C18h
C1Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_H	4500 0C1Ch
C20h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_CONTROL	4500 0C20h
C24h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0	4500 0C24h
C28h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1	4500 0C28h
C2Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2	4500 0C2Ch
C30h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_L	4500 0C30h
C34h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_H	4500 0C34h
C38h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_L	4500 0C38h
C3Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_H	4500 0C3Ch
C40h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_CONTROL	4500 0C40h
C44h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0	4500 0C44h
C48h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1	4500 0C48h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
C4Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2	4500 0C4Ch
C50h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_L	4500 0C50h
C54h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_H	4500 0C54h
C58h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_L	4500 0C58h
C5Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_H	4500 0C5Ch
C60h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_CONTROL	4500 0C60h
C64h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0	4500 0C64h
C68h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1	4500 0C68h
C6Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2	4500 0C6Ch
C70h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_L	4500 0C70h
C74h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_H	4500 0C74h
C78h	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_L	4500 0C78h
C7Ch	32	CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_H	4500 0C7Ch
1000h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL	4500 1000h
1004h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0	4500 1004h
1008h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1	4500 1008h
100Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2	4500 100Ch
1010h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L	4500 1010h
1014h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H	4500 1014h
1018h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L	4500 1018h
101Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H	4500 101Ch
1020h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL	4500 1020h
1024h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0	4500 1024h
1028h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1	4500 1028h
102Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2	4500 102Ch
1030h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L	4500 1030h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1034h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H	4500 1034h
1038h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L	4500 1038h
103Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H	4500 103Ch
1040h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL	4500 1040h
1044h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0	4500 1044h
1048h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1	4500 1048h
104Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2	4500 104Ch
1050h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L	4500 1050h
1054h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H	4500 1054h
1058h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L	4500 1058h
105Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H	4500 105Ch
1060h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL	4500 1060h
1064h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0	4500 1064h
1068h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1	4500 1068h
106Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2	4500 106Ch
1070h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L	4500 1070h
1074h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H	4500 1074h
1078h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L	4500 1078h
107Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H	4500 107Ch
1080h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL	4500 1080h
1084h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0	4500 1084h
1088h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1	4500 1088h
108Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2	4500 108Ch
1090h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L	4500 1090h
1094h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H	4500 1094h
1098h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L	4500 1098h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
109Ch	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H	4500 109Ch
10A0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL	4500 10A0h
10A4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0	4500 10A4h
10A8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1	4500 10A8h
10ACh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2	4500 10ACh
10B0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L	4500 10B0h
10B4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H	4500 10B4h
10B8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L	4500 10B8h
10BCh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H	4500 10BCh
10C0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL	4500 10C0h
10C4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0	4500 10C4h
10C8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1	4500 10C8h
10CCh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2	4500 10CCh
10D0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L	4500 10D0h
10D4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H	4500 10D4h
10D8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L	4500 10D8h
10DCh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H	4500 10DCh
10E0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL	4500 10E0h
10E4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0	4500 10E4h
10E8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1	4500 10E8h
10ECh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2	4500 10ECh
10F0h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L	4500 10F0h
10F4h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H	4500 10F4h
10F8h	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L	4500 10F8h
10FCh	32	CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H	4500 10FCh
1400h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_CONTROL	4500 1400h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1404h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0	4500 1404h
1408h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1	4500 1408h
140Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2	4500 140Ch
1410h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_L	4500 1410h
1414h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_H	4500 1414h
1418h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_L	4500 1418h
141Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_H	4500 141Ch
1420h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_CONTROL	4500 1420h
1424h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0	4500 1424h
1428h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1	4500 1428h
142Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2	4500 142Ch
1430h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_L	4500 1430h
1434h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_H	4500 1434h
1438h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_L	4500 1438h
143Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_H	4500 143Ch
1440h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_CONTROL	4500 1440h
1444h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0	4500 1444h
1448h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1	4500 1448h
144Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2	4500 144Ch
1450h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_L	4500 1450h
1454h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_H	4500 1454h
1458h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_L	4500 1458h
145Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_H	4500 145Ch
1460h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_CONTROL	4500 1460h
1464h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0	4500 1464h
1468h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1	4500 1468h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
146Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2	4500 146Ch
1470h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_L	4500 1470h
1474h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_H	4500 1474h
1478h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_L	4500 1478h
147Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_H	4500 147Ch
1480h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_CONTROL	4500 1480h
1484h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0	4500 1484h
1488h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1	4500 1488h
148Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2	4500 148Ch
1490h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_L	4500 1490h
1494h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_H	4500 1494h
1498h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_L	4500 1498h
149Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_H	4500 149Ch
14A0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_CONTROL	4500 14A0h
14A4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0	4500 14A4h
14A8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1	4500 14A8h
14ACh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2	4500 14ACh
14B0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_L	4500 14B0h
14B4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_H	4500 14B4h
14B8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_L	4500 14B8h
14BCh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_H	4500 14BCh
14C0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_CONTROL	4500 14C0h
14C4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0	4500 14C4h
14C8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1	4500 14C8h
14CCh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2	4500 14CCh
14D0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_L	4500 14D0h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
14D4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_H	4500 14D4h
14D8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_L	4500 14D8h
14DCh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_H	4500 14DCh
14E0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_CONTROL	4500 14E0h
14E4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0	4500 14E4h
14E8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1	4500 14E8h
14ECh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2	4500 14ECh
14F0h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_L	4500 14F0h
14F4h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_H	4500 14F4h
14F8h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_L	4500 14F8h
14FCh	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_H	4500 14FCh
1800h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_CONTROL	4500 1800h
1804h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0	4500 1804h
1808h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1	4500 1808h
180Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2	4500 180Ch
1810h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_L	4500 1810h
1814h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_H	4500 1814h
1818h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_L	4500 1818h
181Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_H	4500 181Ch
1820h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_CONTROL	4500 1820h
1824h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0	4500 1824h
1828h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1	4500 1828h
182Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2	4500 182Ch
1830h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_L	4500 1830h
1834h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_H	4500 1834h
1838h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_L	4500 1838h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
183Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_H	4500 183Ch
1840h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_CONTROL	4500 1840h
1844h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0	4500 1844h
1848h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1	4500 1848h
184Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2	4500 184Ch
1850h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_L	4500 1850h
1854h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_H	4500 1854h
1858h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_L	4500 1858h
185Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_H	4500 185Ch
1860h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_CONTROL	4500 1860h
1864h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0	4500 1864h
1868h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1	4500 1868h
186Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2	4500 186Ch
1870h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_L	4500 1870h
1874h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_H	4500 1874h
1878h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_L	4500 1878h
187Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_H	4500 187Ch
1880h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_CONTROL	4500 1880h
1884h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0	4500 1884h
1888h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1	4500 1888h
188Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2	4500 188Ch
1890h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_L	4500 1890h
1894h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_H	4500 1894h
1898h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_L	4500 1898h
189Ch	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_H	4500 189Ch
18A0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_CONTROL	4500 18A0h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
18A4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0	4500 18A4h
18A8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1	4500 18A8h
18ACh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2	4500 18ACh
18B0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_L	4500 18B0h
18B4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_H	4500 18B4h
18B8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_L	4500 18B8h
18BCh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_H	4500 18BCh
18C0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_CONTROL	4500 18C0h
18C4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0	4500 18C4h
18C8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1	4500 18C8h
18CCh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2	4500 18CCh
18D0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_L	4500 18D0h
18D4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_H	4500 18D4h
18D8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_L	4500 18D8h
18DCh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_H	4500 18DCh
18E0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_CONTROL	4500 18E0h
18E4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0	4500 18E4h
18E8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1	4500 18E8h
18ECh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2	4500 18ECh
18F0h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_L	4500 18F0h
18F4h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_H	4500 18F4h
18F8h	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_L	4500 18F8h
18FCh	32	CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_H	4500 18FCh
1C00h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_CONTROL	4500 1C00h
1C04h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0	4500 1C04h
1C08h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1	4500 1C08h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1C0Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2	4500 1C0Ch
1C10h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_L	4500 1C10h
1C14h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_H	4500 1C14h
1C18h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_L	4500 1C18h
1C1Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_H	4500 1C1Ch
1C20h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_CONTROL	4500 1C20h
1C24h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0	4500 1C24h
1C28h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1	4500 1C28h
1C2Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2	4500 1C2Ch
1C30h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_L	4500 1C30h
1C34h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_H	4500 1C34h
1C38h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_L	4500 1C38h
1C3Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_H	4500 1C3Ch
1C40h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_CONTROL	4500 1C40h
1C44h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0	4500 1C44h
1C48h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1	4500 1C48h
1C4Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2	4500 1C4Ch
1C50h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_L	4500 1C50h
1C54h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_H	4500 1C54h
1C58h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_L	4500 1C58h
1C5Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_H	4500 1C5Ch
1C60h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_CONTROL	4500 1C60h
1C64h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0	4500 1C64h
1C68h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1	4500 1C68h
1C6Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2	4500 1C6Ch
1C70h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_L	4500 1C70h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1C74h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_H	4500 1C74h
1C78h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_L	4500 1C78h
1C7Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_H	4500 1C7Ch
1C80h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_CONTROL	4500 1C80h
1C84h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0	4500 1C84h
1C88h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1	4500 1C88h
1C8Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2	4500 1C8Ch
1C90h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_L	4500 1C90h
1C94h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_H	4500 1C94h
1C98h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_L	4500 1C98h
1C9Ch	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_H	4500 1C9Ch
1CA0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_CONTROL	4500 1CA0h
1CA4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0	4500 1CA4h
1CA8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1	4500 1CA8h
1CACh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2	4500 1CACh
1CB0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_L	4500 1CB0h
1CB4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_H	4500 1CB4h
1CB8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_L	4500 1CB8h
1CBCh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_H	4500 1CBCh
1CC0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_CONTROL	4500 1CC0h
1CC4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0	4500 1CC4h
1CC8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1	4500 1CC8h
1CCCh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2	4500 1CCCh
1CD0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_L	4500 1CD0h
1CD4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_H	4500 1CD4h
1CD8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_L	4500 1CD8h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1CDCh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_H	4500 1CDCh
1CE0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_CONTROL	4500 1CE0h
1CE4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0	4500 1CE4h
1CE8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1	4500 1CE8h
1CECh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2	4500 1CECh
1CF0h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_L	4500 1CF0h
1CF4h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_H	4500 1CF4h
1CF8h	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_L	4500 1CF8h
1CFCh	32	CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_H	4500 1CFCh
2000h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 2000h
2004h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 2004h
2008h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 2008h
200Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 200Ch
2010h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 2010h
2014h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 2014h
2018h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 2018h
201Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 201Ch
2020h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 2020h
2024h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 2024h
2028h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 2028h
202Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 202Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2030h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 2030h
2034h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 2034h
2038h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 2038h
203Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 203Ch
2040h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 2040h
2044h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 2044h
2048h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 2048h
204Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 204Ch
2050h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 2050h
2054h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 2054h
2058h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 2058h
205Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 205Ch
2060h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 2060h
2064h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 2064h
2068h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 2068h
206Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 206Ch
2070h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 2070h
2074h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 2074h
2078h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 2078h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
207Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 207Ch
2080h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 2080h
2084h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 2084h
2088h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 2088h
208Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 208Ch
2090h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 2090h
2094h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 2094h
2098h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 2098h
209Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 209Ch
20A0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 20A0h
20A4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 20A4h
20A8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 20A8h
20ACh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 20ACh
20B0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 20B0h
20B4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 20B4h
20B8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 20B8h
20BCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 20BCh
20C0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 20C0h
20C4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 20C4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
20C8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 20C8h
20CCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 20CCh
20D0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 20D0h
20D4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 20D4h
20D8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 20D8h
20DCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 20DCh
20E0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 20E0h
20E4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 20E4h
20E8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 20E8h
20ECh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 20ECh
20F0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 20F0h
20F4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 20F4h
20F8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 20F8h
20FCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 20FCh
2100h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL	4500 2100h
2104h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0	4500 2104h
2108h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1	4500 2108h
210Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2	4500 210Ch
2110h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L	4500 2110h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2114h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H	4500 2114h
2118h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L	4500 2118h
211Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H	4500 211Ch
2120h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL	4500 2120h
2124h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0	4500 2124h
2128h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1	4500 2128h
212Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2	4500 212Ch
2130h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L	4500 2130h
2134h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H	4500 2134h
2138h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L	4500 2138h
213Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H	4500 213Ch
2140h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL	4500 2140h
2144h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0	4500 2144h
2148h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1	4500 2148h
214Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2	4500 214Ch
2150h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L	4500 2150h
2154h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H	4500 2154h
2158h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L	4500 2158h
215Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H	4500 215Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2160h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL	4500 2160h
2164h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0	4500 2164h
2168h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1	4500 2168h
216Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2	4500 216Ch
2170h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L	4500 2170h
2174h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H	4500 2174h
2178h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L	4500 2178h
217Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H	4500 217Ch
2180h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL	4500 2180h
2184h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0	4500 2184h
2188h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1	4500 2188h
218Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2	4500 218Ch
2190h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L	4500 2190h
2194h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H	4500 2194h
2198h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L	4500 2198h
219Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H	4500 219Ch
21A0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL	4500 21A0h
21A4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0	4500 21A4h
21A8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1	4500 21A8h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
21ACh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2	4500 21ACh
21B0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L	4500 21B0h
21B4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H	4500 21B4h
21B8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L	4500 21B8h
21BCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H	4500 21BCh
21C0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL	4500 21C0h
21C4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0	4500 21C4h
21C8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1	4500 21C8h
21CCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2	4500 21CCh
21D0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L	4500 21D0h
21D4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H	4500 21D4h
21D8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L	4500 21D8h
21DCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H	4500 21DCh
21E0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL	4500 21E0h
21E4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0	4500 21E4h
21E8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1	4500 21E8h
21ECh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2	4500 21ECh
21F0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L	4500 21F0h
21F4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H	4500 21F4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
21F8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L	4500 21F8h
21FCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H	4500 21FCh
2400h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL	4500 2400h
2404h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0	4500 2404h
2408h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1	4500 2408h
240Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2	4500 240Ch
2410h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_L	4500 2410h
2414h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_H	4500 2414h
2418h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_L	4500 2418h
241Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_H	4500 241Ch
2420h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL	4500 2420h
2424h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0	4500 2424h
2428h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1	4500 2428h
242Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2	4500 242Ch
2430h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_L	4500 2430h
2434h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_H	4500 2434h
2438h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_L	4500 2438h
243Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_H	4500 243Ch
2440h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL	4500 2440h
2444h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0	4500 2444h
2448h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1	4500 2448h
244Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2	4500 244Ch
2450h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_L	4500 2450h
2454h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_H	4500 2454h
2458h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_L	4500 2458h
245Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_H	4500 245Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2460h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL	4500 2460h
2464h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0	4500 2464h
2468h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1	4500 2468h
246Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2	4500 246Ch
2470h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_L	4500 2470h
2474h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_H	4500 2474h
2478h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_L	4500 2478h
247Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_H	4500 247Ch
2480h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL	4500 2480h
2484h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0	4500 2484h
2488h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1	4500 2488h
248Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2	4500 248Ch
2490h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_L	4500 2490h
2494h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_H	4500 2494h
2498h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_L	4500 2498h
249Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_H	4500 249Ch
24A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL	4500 24A0h
24A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0	4500 24A4h
24A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1	4500 24A8h
24ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2	4500 24ACh
24B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_L	4500 24B0h
24B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_H	4500 24B4h
24B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_L	4500 24B8h
24BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_H	4500 24BCh
24C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL	4500 24C0h
24C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0	4500 24C4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
24C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1	4500 24C8h
24CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2	4500 24CCh
24D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_L	4500 24D0h
24D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_H	4500 24D4h
24D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_L	4500 24D8h
24DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_H	4500 24DCh
24E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL	4500 24E0h
24E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0	4500 24E4h
24E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1	4500 24E8h
24ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2	4500 24ECh
24F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_L	4500 24F0h
24F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_H	4500 24F4h
24F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_L	4500 24F8h
24FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_H	4500 24FCh
2500h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL	4500 2500h
2504h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0	4500 2504h
2508h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1	4500 2508h
250Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2	4500 250Ch
2510h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_L	4500 2510h
2514h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_H	4500 2514h
2518h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_L	4500 2518h
251Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_H	4500 251Ch
2520h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL	4500 2520h
2524h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0	4500 2524h
2528h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1	4500 2528h
252Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2	4500 252Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2530h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_L	4500 2530h
2534h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_H	4500 2534h
2538h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_L	4500 2538h
253Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_H	4500 253Ch
2540h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL	4500 2540h
2544h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0	4500 2544h
2548h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1	4500 2548h
254Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2	4500 254Ch
2550h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_L	4500 2550h
2554h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_H	4500 2554h
2558h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_L	4500 2558h
255Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_H	4500 255Ch
2560h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL	4500 2560h
2564h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0	4500 2564h
2568h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1	4500 2568h
256Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2	4500 256Ch
2570h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_L	4500 2570h
2574h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_H	4500 2574h
2578h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_L	4500 2578h
257Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_H	4500 257Ch
2580h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL	4500 2580h
2584h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0	4500 2584h
2588h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1	4500 2588h
258Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2	4500 258Ch
2590h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_L	4500 2590h
2594h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_H	4500 2594h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2598h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_L	4500 2598h
259Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_H	4500 259Ch
25A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL	4500 25A0h
25A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0	4500 25A4h
25A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1	4500 25A8h
25ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2	4500 25ACh
25B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_L	4500 25B0h
25B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_H	4500 25B4h
25B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_L	4500 25B8h
25BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_H	4500 25BCh
25C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL	4500 25C0h
25C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0	4500 25C4h
25C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1	4500 25C8h
25CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2	4500 25CCh
25D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_L	4500 25D0h
25D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_H	4500 25D4h
25D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_L	4500 25D8h
25DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_H	4500 25DCh
25E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL	4500 25E0h
25E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0	4500 25E4h
25E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1	4500 25E8h
25ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2	4500 25ECh
25F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_L	4500 25F0h
25F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_H	4500 25F4h
25F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_L	4500 25F8h
25FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_H	4500 25FCh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2600h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL	4500 2600h
2604h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0	4500 2604h
2608h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1	4500 2608h
260Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2	4500 260Ch
2610h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_L	4500 2610h
2614h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_H	4500 2614h
2618h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_L	4500 2618h
261Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_H	4500 261Ch
2620h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL	4500 2620h
2624h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0	4500 2624h
2628h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1	4500 2628h
262Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2	4500 262Ch
2630h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_L	4500 2630h
2634h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_H	4500 2634h
2638h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_L	4500 2638h
263Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_H	4500 263Ch
2640h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL	4500 2640h
2644h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0	4500 2644h
2648h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1	4500 2648h
264Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2	4500 264Ch
2650h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_L	4500 2650h
2654h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_H	4500 2654h
2658h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_L	4500 2658h
265Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_H	4500 265Ch
2660h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL	4500 2660h
2664h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0	4500 2664h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2668h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1	4500 2668h
266Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2	4500 266Ch
2670h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_L	4500 2670h
2674h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_H	4500 2674h
2678h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_L	4500 2678h
267Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_H	4500 267Ch
2680h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL	4500 2680h
2684h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0	4500 2684h
2688h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1	4500 2688h
268Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2	4500 268Ch
2690h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_L	4500 2690h
2694h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_H	4500 2694h
2698h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_L	4500 2698h
269Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_H	4500 269Ch
26A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL	4500 26A0h
26A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0	4500 26A4h
26A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1	4500 26A8h
26ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2	4500 26ACh
26B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_L	4500 26B0h
26B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_H	4500 26B4h
26B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_L	4500 26B8h
26BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_H	4500 26BCh
26C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL	4500 26C0h
26C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0	4500 26C4h
26C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1	4500 26C8h
26CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2	4500 26CCh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
26D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_L	4500 26D0h
26D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_H	4500 26D4h
26D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_L	4500 26D8h
26DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_H	4500 26DCh
26E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL	4500 26E0h
26E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0	4500 26E4h
26E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1	4500 26E8h
26ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2	4500 26ECh
26F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_L	4500 26F0h
26F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_H	4500 26F4h
26F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_L	4500 26F8h
26FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_H	4500 26FCh
2700h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL	4500 2700h
2704h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0	4500 2704h
2708h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1	4500 2708h
270Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2	4500 270Ch
2710h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_L	4500 2710h
2714h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_H	4500 2714h
2718h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_L	4500 2718h
271Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_H	4500 271Ch
2720h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL	4500 2720h
2724h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0	4500 2724h
2728h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1	4500 2728h
272Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2	4500 272Ch
2730h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_L	4500 2730h
2734h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_H	4500 2734h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2738h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_L	4500 2738h
273Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_H	4500 273Ch
2740h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL	4500 2740h
2744h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0	4500 2744h
2748h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1	4500 2748h
274Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2	4500 274Ch
2750h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_L	4500 2750h
2754h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_H	4500 2754h
2758h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_L	4500 2758h
275Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_H	4500 275Ch
2760h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL	4500 2760h
2764h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0	4500 2764h
2768h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1	4500 2768h
276Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2	4500 276Ch
2770h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_L	4500 2770h
2774h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_H	4500 2774h
2778h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_L	4500 2778h
277Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_H	4500 277Ch
2780h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL	4500 2780h
2784h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0	4500 2784h
2788h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1	4500 2788h
278Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2	4500 278Ch
2790h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_L	4500 2790h
2794h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_H	4500 2794h
2798h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_L	4500 2798h
279Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_H	4500 279Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
27A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL	4500 27A0h
27A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0	4500 27A4h
27A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1	4500 27A8h
27ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2	4500 27ACh
27B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_L	4500 27B0h
27B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_H	4500 27B4h
27B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_L	4500 27B8h
27BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_H	4500 27BCh
27C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL	4500 27C0h
27C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0	4500 27C4h
27C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1	4500 27C8h
27CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2	4500 27CCh
27D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_L	4500 27D0h
27D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_H	4500 27D4h
27D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_L	4500 27D8h
27DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_H	4500 27DCh
27E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL	4500 27E0h
27E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0	4500 27E4h
27E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1	4500 27E8h
27ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2	4500 27ECh
27F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_L	4500 27F0h
27F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_H	4500 27F4h
27F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_L	4500 27F8h
27FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_H	4500 27FCh
2800h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_CONTROL	4500 2800h
2804h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0	4500 2804h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2808h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1	4500 2808h
280Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2	4500 280Ch
2810h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_L	4500 2810h
2814h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_H	4500 2814h
2818h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_L	4500 2818h
281Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_H	4500 281Ch
2820h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_CONTROL	4500 2820h
2824h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0	4500 2824h
2828h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1	4500 2828h
282Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2	4500 282Ch
2830h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_L	4500 2830h
2834h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_H	4500 2834h
2838h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_L	4500 2838h
283Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_H	4500 283Ch
2840h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_CONTROL	4500 2840h
2844h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0	4500 2844h
2848h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1	4500 2848h
284Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2	4500 284Ch
2850h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_L	4500 2850h
2854h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_H	4500 2854h
2858h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_L	4500 2858h
285Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_H	4500 285Ch
2860h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_CONTROL	4500 2860h
2864h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0	4500 2864h
2868h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1	4500 2868h
286Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2	4500 286Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2870h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_L	4500 2870h
2874h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_H	4500 2874h
2878h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_L	4500 2878h
287Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_H	4500 287Ch
2880h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_CONTROL	4500 2880h
2884h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0	4500 2884h
2888h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1	4500 2888h
288Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2	4500 288Ch
2890h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_L	4500 2890h
2894h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_H	4500 2894h
2898h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_L	4500 2898h
289Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_H	4500 289Ch
28A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_CONTROL	4500 28A0h
28A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0	4500 28A4h
28A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1	4500 28A8h
28ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2	4500 28ACh
28B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_L	4500 28B0h
28B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_H	4500 28B4h
28B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_L	4500 28B8h
28BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_H	4500 28BCh
28C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_CONTROL	4500 28C0h
28C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0	4500 28C4h
28C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1	4500 28C8h
28CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2	4500 28CCh
28D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_L	4500 28D0h
28D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_H	4500 28D4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
28D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_L	4500 28D8h
28DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_H	4500 28DCh
28E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_CONTROL	4500 28E0h
28E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0	4500 28E4h
28E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1	4500 28E8h
28ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2	4500 28ECh
28F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_L	4500 28F0h
28F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_H	4500 28F4h
28F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_L	4500 28F8h
28FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_H	4500 28FCh
2900h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_CONTROL	4500 2900h
2904h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0	4500 2904h
2908h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1	4500 2908h
290Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2	4500 290Ch
2910h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_L	4500 2910h
2914h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_H	4500 2914h
2918h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_L	4500 2918h
291Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_H	4500 291Ch
2920h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_CONTROL	4500 2920h
2924h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0	4500 2924h
2928h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1	4500 2928h
292Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2	4500 292Ch
2930h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_L	4500 2930h
2934h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_H	4500 2934h
2938h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_L	4500 2938h
293Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_H	4500 293Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2940h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_CONTROL	4500 2940h
2944h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0	4500 2944h
2948h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1	4500 2948h
294Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2	4500 294Ch
2950h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_L	4500 2950h
2954h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_H	4500 2954h
2958h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_L	4500 2958h
295Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_H	4500 295Ch
2960h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_CONTROL	4500 2960h
2964h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0	4500 2964h
2968h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1	4500 2968h
296Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2	4500 296Ch
2970h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_L	4500 2970h
2974h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_H	4500 2974h
2978h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_L	4500 2978h
297Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_H	4500 297Ch
2980h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_CONTROL	4500 2980h
2984h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0	4500 2984h
2988h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1	4500 2988h
298Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2	4500 298Ch
2990h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_L	4500 2990h
2994h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_H	4500 2994h
2998h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_L	4500 2998h
299Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_H	4500 299Ch
29A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_CONTROL	4500 29A0h
29A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0	4500 29A4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
29A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1	4500 29A8h
29ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2	4500 29ACh
29B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_L	4500 29B0h
29B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_H	4500 29B4h
29B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_L	4500 29B8h
29BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_H	4500 29BCh
29C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_CONTROL	4500 29C0h
29C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0	4500 29C4h
29C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1	4500 29C8h
29CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2	4500 29CCh
29D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_L	4500 29D0h
29D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_H	4500 29D4h
29D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_L	4500 29D8h
29DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_H	4500 29DCh
29E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_CONTROL	4500 29E0h
29E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0	4500 29E4h
29E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1	4500 29E8h
29ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2	4500 29ECh
29F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_L	4500 29F0h
29F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_H	4500 29F4h
29F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_L	4500 29F8h
29FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_H	4500 29FCh
2C00h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL	4500 2C00h
2C04h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0	4500 2C04h
2C08h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1	4500 2C08h
2C0Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2	4500 2C0Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2C10h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_L	4500 2C10h
2C14h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_H	4500 2C14h
2C18h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_L	4500 2C18h
2C1Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_H	4500 2C1Ch
2C20h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL	4500 2C20h
2C24h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0	4500 2C24h
2C28h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1	4500 2C28h
2C2Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2	4500 2C2Ch
2C30h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_L	4500 2C30h
2C34h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_H	4500 2C34h
2C38h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_L	4500 2C38h
2C3Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_H	4500 2C3Ch
2C40h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL	4500 2C40h
2C44h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0	4500 2C44h
2C48h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1	4500 2C48h
2C4Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2	4500 2C4Ch
2C50h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_L	4500 2C50h
2C54h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_H	4500 2C54h
2C58h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_L	4500 2C58h
2C5Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_H	4500 2C5Ch
2C60h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL	4500 2C60h
2C64h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0	4500 2C64h
2C68h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1	4500 2C68h
2C6Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2	4500 2C6Ch
2C70h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_L	4500 2C70h
2C74h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_H	4500 2C74h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2C78h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_L	4500 2C78h
2C7Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_H	4500 2C7Ch
2C80h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_CONTROL	4500 2C80h
2C84h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0	4500 2C84h
2C88h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1	4500 2C88h
2C8Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2	4500 2C8Ch
2C90h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_L	4500 2C90h
2C94h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_H	4500 2C94h
2C98h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_L	4500 2C98h
2C9Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_H	4500 2C9Ch
2CA0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_CONTROL	4500 2CA0h
2CA4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0	4500 2CA4h
2CA8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1	4500 2CA8h
2CACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2	4500 2CACh
2CB0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_L	4500 2CB0h
2CB4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_H	4500 2CB4h
2CB8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_L	4500 2CB8h
2CBCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_H	4500 2CBCh
2CC0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_CONTROL	4500 2CC0h
2CC4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0	4500 2CC4h
2CC8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1	4500 2CC8h
2CCCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2	4500 2CCCh
2CD0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_L	4500 2CD0h
2CD4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_H	4500 2CD4h
2CD8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_L	4500 2CD8h
2CDCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_H	4500 2CDCh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2CE0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_CONTROL	4500 2CE0h
2CE4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0	4500 2CE4h
2CE8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1	4500 2CE8h
2CECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2	4500 2CECh
2CF0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_L	4500 2CF0h
2CF4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_H	4500 2CF4h
2CF8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_L	4500 2CF8h
2CFCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_H	4500 2CFCh
2D00h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_CONTROL	4500 2D00h
2D04h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0	4500 2D04h
2D08h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1	4500 2D08h
2D0Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2	4500 2D0Ch
2D10h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_L	4500 2D10h
2D14h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_H	4500 2D14h
2D18h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_L	4500 2D18h
2D1Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_H	4500 2D1Ch
2D20h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_CONTROL	4500 2D20h
2D24h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0	4500 2D24h
2D28h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1	4500 2D28h
2D2Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2	4500 2D2Ch
2D30h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_L	4500 2D30h
2D34h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_H	4500 2D34h
2D38h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_L	4500 2D38h
2D3Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_H	4500 2D3Ch
2D40h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL	4500 2D40h
2D44h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0	4500 2D44h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2D48h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1	4500 2D48h
2D4Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2	4500 2D4Ch
2D50h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_L	4500 2D50h
2D54h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_H	4500 2D54h
2D58h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_L	4500 2D58h
2D5Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_H	4500 2D5Ch
2D60h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL	4500 2D60h
2D64h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0	4500 2D64h
2D68h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1	4500 2D68h
2D6Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2	4500 2D6Ch
2D70h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_L	4500 2D70h
2D74h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_H	4500 2D74h
2D78h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_L	4500 2D78h
2D7Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_H	4500 2D7Ch
2D80h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL	4500 2D80h
2D84h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0	4500 2D84h
2D88h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1	4500 2D88h
2D8Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2	4500 2D8Ch
2D90h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_L	4500 2D90h
2D94h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_H	4500 2D94h
2D98h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_L	4500 2D98h
2D9Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_H	4500 2D9Ch
2DA0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL	4500 2DA0h
2DA4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0	4500 2DA4h
2DA8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1	4500 2DA8h
2DACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2	4500 2DACh

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2DB0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_L	4500 2DB0h
2DB4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_H	4500 2DB4h
2DB8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_L	4500 2DB8h
2DBCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_H	4500 2DBCh
2DC0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL	4500 2DC0h
2DC4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0	4500 2DC4h
2DC8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1	4500 2DC8h
2DCCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2	4500 2DCCh
2DD0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_L	4500 2DD0h
2DD4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_H	4500 2DD4h
2DD8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_L	4500 2DD8h
2DDCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_H	4500 2DDCh
2DE0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL	4500 2DE0h
2DE4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0	4500 2DE4h
2DE8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1	4500 2DE8h
2DECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2	4500 2DECh
2DF0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_L	4500 2DF0h
2DF4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_H	4500 2DF4h
2DF8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_L	4500 2DF8h
2DFCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_H	4500 2DFCh
3400h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_CONTROL	4500 3400h
3404h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0	4500 3404h
3408h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1	4500 3408h
340Ch	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2	4500 340Ch
3410h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_L	4500 3410h
3414h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_H	4500 3414h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3418h	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_L	4500 3418h
341Ch	32	CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_H	4500 341Ch
3800h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 3800h
3804h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 3804h
3808h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 3808h
380Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 380Ch
3810h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 3810h
3814h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 3814h
3818h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 3818h
381Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 381Ch
3820h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 3820h
3824h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 3824h
3828h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 3828h
382Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 382Ch
3830h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 3830h
3834h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 3834h
3838h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 3838h
383Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 383Ch
3840h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 3840h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3844h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 3844h
3848h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 3848h
384Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 384Ch
3850h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 3850h
3854h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 3854h
3858h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 3858h
385Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 385Ch
3860h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 3860h
3864h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 3864h
3868h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 3868h
386Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 386Ch
3870h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 3870h
3874h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 3874h
3878h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 3878h
387Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 387Ch
3880h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 3880h
3884h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 3884h
3888h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 3888h
388Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 388Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3890h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 3890h
3894h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 3894h
3898h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 3898h
389Ch	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 389Ch
38A0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 38A0h
38A4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 38A4h
38A8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 38A8h
38ACh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 38ACh
38B0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 38B0h
38B4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 38B4h
38B8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 38B8h
38BCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 38BCh
38C0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 38C0h
38C4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 38C4h
38C8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 38C8h
38CCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 38CCh
38D0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 38D0h
38D4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 38D4h
38D8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 38D8h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
38DCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 38DCh
38E0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 38E0h
38E4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 38E4h
38E8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 38E8h
38ECh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 38ECh
38F0h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 38F0h
38F4h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 38F4h
38F8h	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 38F8h
38FCh	32	CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 38FCh
3C00h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL	4500 3C00h
3C04h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0	4500 3C04h
3C08h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1	4500 3C08h
3C0Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2	4500 3C0Ch
3C10h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L	4500 3C10h
3C14h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H	4500 3C14h
3C18h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L	4500 3C18h
3C1Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H	4500 3C1Ch
3C20h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL	4500 3C20h
3C24h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0	4500 3C24h
3C28h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1	4500 3C28h
3C2Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2	4500 3C2Ch
3C30h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L	4500 3C30h
3C34h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H	4500 3C34h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3C38h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L	4500 3C38h
3C3Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H	4500 3C3Ch
3C40h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL	4500 3C40h
3C44h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0	4500 3C44h
3C48h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1	4500 3C48h
3C4Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2	4500 3C4Ch
3C50h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L	4500 3C50h
3C54h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H	4500 3C54h
3C58h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L	4500 3C58h
3C5Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H	4500 3C5Ch
3C60h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL	4500 3C60h
3C64h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0	4500 3C64h
3C68h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1	4500 3C68h
3C6Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2	4500 3C6Ch
3C70h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L	4500 3C70h
3C74h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H	4500 3C74h
3C78h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L	4500 3C78h
3C7Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H	4500 3C7Ch
3C80h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL	4500 3C80h
3C84h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0	4500 3C84h
3C88h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1	4500 3C88h
3C8Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2	4500 3C8Ch
3C90h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L	4500 3C90h
3C94h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H	4500 3C94h
3C98h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L	4500 3C98h
3C9Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H	4500 3C9Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3CA0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL	4500 3CA0h
3CA4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0	4500 3CA4h
3CA8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1	4500 3CA8h
3CACh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2	4500 3CACh
3CB0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L	4500 3CB0h
3CB4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H	4500 3CB4h
3CB8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L	4500 3CB8h
3CBCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H	4500 3CBCh
3CC0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL	4500 3CC0h
3CC4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0	4500 3CC4h
3CC8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1	4500 3CC8h
3CCCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2	4500 3CCCh
3CD0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L	4500 3CD0h
3CD4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H	4500 3CD4h
3CD8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L	4500 3CD8h
3CDCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H	4500 3CDCh
3CE0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL	4500 3CE0h
3CE4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0	4500 3CE4h
3CE8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1	4500 3CE8h
3CECh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2	4500 3CECh
3CF0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L	4500 3CF0h
3CF4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H	4500 3CF4h
3CF8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L	4500 3CF8h
3CFCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H	4500 3CFCh
3D00h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_CONTROL	4500 3D00h
3D04h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0	4500 3D04h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3D08h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1	4500 3D08h
3D0Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2	4500 3D0Ch
3D10h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_L	4500 3D10h
3D14h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_H	4500 3D14h
3D18h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_L	4500 3D18h
3D1Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_H	4500 3D1Ch
3D20h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_CONTROL	4500 3D20h
3D24h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0	4500 3D24h
3D28h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1	4500 3D28h
3D2Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2	4500 3D2Ch
3D30h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_L	4500 3D30h
3D34h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_H	4500 3D34h
3D38h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_L	4500 3D38h
3D3Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_H	4500 3D3Ch
3D40h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_CONTROL	4500 3D40h
3D44h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0	4500 3D44h
3D48h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1	4500 3D48h
3D4Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2	4500 3D4Ch
3D50h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_L	4500 3D50h
3D54h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_H	4500 3D54h
3D58h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_L	4500 3D58h
3D5Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_H	4500 3D5Ch
3D60h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_CONTROL	4500 3D60h
3D64h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0	4500 3D64h
3D68h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1	4500 3D68h
3D6Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2	4500 3D6Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3D70h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_L	4500 3D70h
3D74h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_H	4500 3D74h
3D78h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_L	4500 3D78h
3D7Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_H	4500 3D7Ch
3D80h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_CONTROL	4500 3D80h
3D84h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0	4500 3D84h
3D88h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1	4500 3D88h
3D8Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2	4500 3D8Ch
3D90h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_L	4500 3D90h
3D94h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_H	4500 3D94h
3D98h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_L	4500 3D98h
3D9Ch	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_H	4500 3D9Ch
3DA0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_CONTROL	4500 3DA0h
3DA4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0	4500 3DA4h
3DA8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1	4500 3DA8h
3DACh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2	4500 3DACh
3DB0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_L	4500 3DB0h
3DB4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_H	4500 3DB4h
3DB8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_L	4500 3DB8h
3DBCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_H	4500 3DBCh
3DC0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_CONTROL	4500 3DC0h
3DC4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0	4500 3DC4h
3DC8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1	4500 3DC8h
3DCCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2	4500 3DCCh
3DD0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_L	4500 3DD0h
3DD4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_H	4500 3DD4h

Table 14-2. CBASS_FW Registers, Base Address=4500 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3DD8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_L	4500 3DD8h
3DDCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_H	4500 3DDCh
3DE0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_CONTROL	4500 3DE0h
3DE4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0	4500 3DE4h
3DE8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1	4500 3DE8h
3DECh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2	4500 3DECh
3DF0h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_L	4500 3DF0h
3DF4h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_H	4500 3DF4h
3DF8h	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_L	4500 3DF8h
3DFCh	32	CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_H	4500 3DFCh

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536

Offset	Length	Register Name	CBASS0 Physical Address
400h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL	4582 0400h
410h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L	4582 0410h
414h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H	4582 0414h
418h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L	4582 0418h
41Ch	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H	4582 041Ch
420h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL	4582 0420h
800h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL	4582 0800h
810h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L	4582 0810h
814h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H	4582 0814h
818h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L	4582 0818h
81Ch	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H	4582 081Ch

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
820h	32	CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL	4582 0820h
1400h	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL	4582 1400h
1410h	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L	4582 1410h
1414h	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H	4582 1414h
1418h	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L	4582 1418h
141Ch	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H	4582 141Ch
1420h	32	CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL	4582 1420h
1800h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL	4582 1800h
1810h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L	4582 1810h
1814h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H	4582 1814h
1818h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L	4582 1818h
181Ch	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H	4582 181Ch
1820h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL	4582 1820h
1C00h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL	4582 1C00h
1C10h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L	4582 1C10h
1C14h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H	4582 1C14h
1C18h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L	4582 1C18h
1C1Ch	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H	4582 1C1Ch
1C20h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL	4582 1C20h
2000h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL	4582 2000h
2010h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L	4582 2010h
2014h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H	4582 2014h
2018h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L	4582 2018h
201Ch	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H	4582 201Ch
2020h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL	4582 2020h
2400h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL	4582 2400h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
2410h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L	4582 2410h
2414h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H	4582 2414h
2418h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L	4582 2418h
241Ch	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H	4582 241Ch
2420h	32	CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL	4582 2420h
2800h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL	4582 2800h
2810h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L	4582 2810h
2814h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H	4582 2814h
2818h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L	4582 2818h
281Ch	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H	4582 281Ch
2820h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL	4582 2820h
2C00h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL	4582 2C00h
2C10h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L	4582 2C10h
2C14h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H	4582 2C14h
2C18h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L	4582 2C18h
2C1Ch	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H	4582 2C1Ch
2C20h	32	CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL	4582 2C20h
3000h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL	4582 3000h
3010h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L	4582 3010h
3014h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H	4582 3014h
3018h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L	4582 3018h
301Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H	4582 301Ch
3020h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL	4582 3020h
3400h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL	4582 3400h
3410h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L	4582 3410h
3414h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H	4582 3414h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
3418h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L	4582 3418h
341Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H	4582 341Ch
3420h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL	4582 3420h
3800h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL	4582 3800h
3810h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L	4582 3810h
3814h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H	4582 3814h
3818h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L	4582 3818h
381Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H	4582 381Ch
3820h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL	4582 3820h
3C00h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL	4582 3C00h
3C10h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L	4582 3C10h
3C14h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H	4582 3C14h
3C18h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L	4582 3C18h
3C1Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H	4582 3C1Ch
3C20h	32	CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL	4582 3C20h
4000h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL	4582 4000h
4010h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L	4582 4010h
4014h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H	4582 4014h
4018h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L	4582 4018h
401Ch	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H	4582 401Ch
4020h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL	4582 4020h
4400h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL	4582 4400h
4410h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L	4582 4410h
4414h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H	4582 4414h
4418h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L	4582 4418h
441Ch	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H	4582 441Ch

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
4420h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL	4582 4420h
4800h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL	4582 4800h
4810h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_L	4582 4810h
4814h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_H	4582 4814h
4818h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_L	4582 4818h
481Ch	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_H	4582 481Ch
4820h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL	4582 4820h
4C00h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL	4582 4C00h
4C10h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_L	4582 4C10h
4C14h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_H	4582 4C14h
4C18h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_L	4582 4C18h
4C1Ch	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_H	4582 4C1Ch
4C20h	32	CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL	4582 4C20h
5000h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL	4582 5000h
5010h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_L	4582 5010h
5014h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_H	4582 5014h
5018h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_L	4582 5018h
501Ch	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_H	4582 501Ch
5020h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL	4582 5020h
5030h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_L	4582 5030h
5034h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_H	4582 5034h
5038h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_L	4582 5038h
503Ch	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_H	4582 503Ch
5040h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL	4582 5040h
5050h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_L	4582 5050h
5054h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_H	4582 5054h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
5058h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_L	4582 5058h
505Ch	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_H	4582 505Ch
5060h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL	4582 5060h
5070h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_L	4582 5070h
5074h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_H	4582 5074h
5078h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_L	4582 5078h
507Ch	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_H	4582 507Ch
5080h	32	CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL	4582 5080h
5400h	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL	4582 5400h
5410h	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L	4582 5410h
5414h	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H	4582 5414h
5418h	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L	4582 5418h
541Ch	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H	4582 541Ch
5420h	32	CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL	4582 5420h
5800h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL	4582 5800h
5810h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_L	4582 5810h
5814h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_H	4582 5814h
5818h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_L	4582 5818h
581Ch	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_H	4582 581Ch
5820h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL	4582 5820h
5C00h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL	4582 5C00h
5C10h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_L	4582 5C10h
5C14h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_H	4582 5C14h
5C18h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_L	4582 5C18h
5C1Ch	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_H	4582 5C1Ch
5C20h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL	4582 5C20h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
5C30h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_L	4582 5C30h
5C34h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_H	4582 5C34h
5C38h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_L	4582 5C38h
5C3Ch	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_H	4582 5C3Ch
5C40h	32	CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL	4582 5C40h
6000h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL	4582 6000h
6010h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_L	4582 6010h
6014h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_H	4582 6014h
6018h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_L	4582 6018h
601Ch	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_H	4582 601Ch
6020h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL	4582 6020h
6400h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL	4582 6400h
6410h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_L	4582 6410h
6414h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_H	4582 6414h
6418h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_L	4582 6418h
641Ch	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_H	4582 641Ch
6420h	32	CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL	4582 6420h
6800h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL	4582 6800h
6810h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L	4582 6810h
6814h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H	4582 6814h
6818h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L	4582 6818h
681Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H	4582 681Ch
6820h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL	4582 6820h
6830h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_L	4582 6830h
6834h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_H	4582 6834h
6838h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_L	4582 6838h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
683Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_H	4582 683Ch
6840h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL	4582 6840h
6850h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_L	4582 6850h
6854h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_H	4582 6854h
6858h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_L	4582 6858h
685Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_H	4582 685Ch
6860h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL	4582 6860h
6870h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_L	4582 6870h
6874h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_H	4582 6874h
6878h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_L	4582 6878h
687Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_H	4582 687Ch
6880h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL	4582 6880h
6890h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_L	4582 6890h
6894h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_H	4582 6894h
6898h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_L	4582 6898h
689Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_H	4582 689Ch
68A0h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL	4582 68A0h
6C00h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL	4582 6C00h
6C10h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L	4582 6C10h
6C14h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H	4582 6C14h
6C18h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L	4582 6C18h
6C1Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H	4582 6C1Ch
6C20h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL	4582 6C20h
6C30h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_L	4582 6C30h
6C34h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_H	4582 6C34h
6C38h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_L	4582 6C38h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
6C3Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_H	4582 6C3Ch
6C40h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL	4582 6C40h
6C50h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_L	4582 6C50h
6C54h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_H	4582 6C54h
6C58h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_L	4582 6C58h
6C5Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_H	4582 6C5Ch
6C60h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL	4582 6C60h
6C70h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_L	4582 6C70h
6C74h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_H	4582 6C74h
6C78h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_L	4582 6C78h
6C7Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_H	4582 6C7Ch
6C80h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL	4582 6C80h
6C90h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_L	4582 6C90h
6C94h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_H	4582 6C94h
6C98h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_L	4582 6C98h
6C9Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_H	4582 6C9Ch
6CA0h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL	4582 6CA0h
7000h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL	4582 7000h
7010h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L	4582 7010h
7014h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H	4582 7014h
7018h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L	4582 7018h
701Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H	4582 701Ch
7020h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL	4582 7020h
7400h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL	4582 7400h
7410h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L	4582 7410h
7414h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H	4582 7414h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
7418h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L	4582 7418h
741Ch	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H	4582 741Ch
7420h	32	CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL	4582 7420h
7800h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL	4582 7800h
7810h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L	4582 7810h
7814h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H	4582 7814h
7818h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L	4582 7818h
781Ch	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H	4582 781Ch
7820h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL	4582 7820h
7830h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L	4582 7830h
7834h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H	4582 7834h
7838h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L	4582 7838h
783Ch	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H	4582 783Ch
7840h	32	CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL	4582 7840h
7C00h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL	4582 7C00h
7C10h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_L	4582 7C10h
7C14h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_H	4582 7C14h
7C18h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_L	4582 7C18h
7C1Ch	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_H	4582 7C1Ch
7C20h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL	4582 7C20h
8000h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL	4582 8000h
8010h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_L	4582 8010h
8014h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_H	4582 8014h
8018h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_L	4582 8018h
801Ch	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_H	4582 801Ch
8020h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL	4582 8020h

Table 14-3. CBASS_ISC Registers, Base Address=4582 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
8400h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL	4582 8400h
8410h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_L	4582 8410h
8414h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_H	4582 8414h
8418h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_L	4582 8418h
841Ch	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_H	4582 841Ch
8420h	32	CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL	4582 8420h

Table 14-4. CBASS_GLB Registers, Base Address=45B0 8000h, Length=1024

Offset	Length	Register Name	CBASS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 8000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 8004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 8020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 8024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 8028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 802Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 8030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 8034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 8038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 8040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 8044h

Table 14-5. CBASS_QOS Registers, Base Address=45D2 0000h, Length=65536

Offset	Length	Register Name	CBASS0 Physical Address
400h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1	45D2 0400h
404h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2	45D2 0404h
500h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0	45D2 0500h
800h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1	45D2 0800h
804h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2	45D2 0804h
900h	32	CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0	45D2 0900h
1800h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1	45D2 1800h
1804h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2	45D2 1804h
1900h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0	45D2 1900h
1C00h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1	45D2 1C00h

Table 14-5. CBASS_QOS Registers, Base Address=45D2 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
1C04h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2	45D2 1C04h
1D00h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0	45D2 1D00h
2000h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1	45D2 2000h
2004h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2	45D2 2004h
2100h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0	45D2 2100h
2400h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1	45D2 2400h
2404h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2	45D2 2404h
2500h	32	CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0	45D2 2500h
2800h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1	45D2 2800h
2804h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2	45D2 2804h
2900h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_MAP0	45D2 2900h
2C00h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1	45D2 2C00h
2C04h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2	45D2 2C04h
2D00h	32	CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_MAP0	45D2 2D00h
3000h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1	45D2 3000h
3004h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2	45D2 3004h
3100h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0	45D2 3100h
3400h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1	45D2 3400h
3404h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2	45D2 3404h
3500h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0	45D2 3500h
3800h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1	45D2 3800h
3804h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2	45D2 3804h
3900h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_MAP0	45D2 3900h
3C00h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1	45D2 3C00h
3C04h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2	45D2 3C04h
3D00h	32	CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_MAP0	45D2 3D00h

Table 14-5. CBASS_QOS Registers, Base Address=45D2 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
4000h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1	45D2 4000h
4004h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2	45D2 4004h
4100h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_MAP0	45D2 4100h
4400h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1	45D2 4400h
4404h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2	45D2 4404h
4500h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_MAP0	45D2 4500h
4800h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1	45D2 4800h
4804h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2	45D2 4804h
4900h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_MAP0	45D2 4900h
4C00h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1	45D2 4C00h
4C04h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2	45D2 4C04h
4D00h	32	CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_MAP0	45D2 4D00h
5000h	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1	45D2 5000h
5004h	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2	45D2 5004h
5100h	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP0	45D2 5100h
5104h	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP1	45D2 5104h
5108h	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP2	45D2 5108h
510Ch	32	CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP3	45D2 510Ch
5400h	32	CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1	45D2 5400h
5404h	32	CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2	45D2 5404h
5500h	32	CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0	45D2 5500h
5800h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1	45D2 5800h
5804h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2	45D2 5804h
5900h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0	45D2 5900h
5C00h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1	45D2 5C00h
5C04h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2	45D2 5C04h
5D00h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0	45D2 5D00h
5D04h	32	CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1	45D2 5D04h

Table 14-5. CBASS_QOS Registers, Base Address=45D2 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
6800h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1	45D2 6800h
6804h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2	45D2 6804h
6900h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0	45D2 6900h
6904h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1	45D2 6904h
6908h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2	45D2 6908h
690Ch	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3	45D2 690Ch
6910h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4	45D2 6910h
6C00h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1	45D2 6C00h
6C04h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2	45D2 6C04h
6D00h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0	45D2 6D00h
6D04h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1	45D2 6D04h
6D08h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2	45D2 6D08h
6D0Ch	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3	45D2 6D0Ch
6D10h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4	45D2 6D10h
7000h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1	45D2 7000h
7004h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2	45D2 7004h
7100h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0	45D2 7100h
7400h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1	45D2 7400h
7404h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2	45D2 7404h
7500h	32	CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0	45D2 7500h
7800h	32	CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1	45D2 7800h
7804h	32	CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2	45D2 7804h
7900h	32	CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP0	45D2 7900h
7904h	32	CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP1	45D2 7904h
8000h	32	CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1	45D2 8000h
8004h	32	CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2	45D2 8004h

Table 14-5. CBASS_QOS Registers, Base Address=45D2 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS0 Physical Address
8100h	32	CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0	45D2 8100h
8104h	32	CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1	45D2 8104h
8108h	32	CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2	45D2 8108h

14.1.1.2 cbass Registers

cbass Registers

14.1.1.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-6. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0000h**

Figure 14-1. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-8. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-9. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0004h**

Figure 14-2. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-12. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0024h**

Figure 14-3. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-15. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0028h**

Figure 14-4. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CODE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-17. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-18. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 002Ch**

Figure 14-5. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-20. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-21. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0030h**

Figure 14-6. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-23. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-24. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0034h**

Figure 14-7. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-26. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

Table 14-26. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-27. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0038h**

Figure 14-8. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-30. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0050h**

Figure 14-9. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-32. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-33. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0054h**

Figure 14-10. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-35. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-36. Instance Table

Instance Name	Physical Address
CBASS0	3A00 0058h

Figure 14-11. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-38. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-39. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 005Ch**

Figure 14-12. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-41. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-42. Instance Table

Instance Name	Physical Address
CBASS0	**3A00 0060h**

Figure 14-13. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-44. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.1.2.14 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-45. Instance Table

Instance Name	Physical Address
CBASS0	4500 0000h

Figure 14-14. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-47. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.15 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-48. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0004h**

Figure 14-15. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-50. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-50. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.16 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-51. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0008h**

Figure 14-16. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-53. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-53. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.17 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-54. Instance Table

Instance Name	Physical Address
CBASS0	**4500 000Ch**

Figure 14-17. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-56. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-56. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.18 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 80000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-57. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0010h**

Figure 14-18. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
80000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
80000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
80000h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-59. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	80000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.19 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-60. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0014h**

Figure 14-19. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-62. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.20 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 7FFFFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-63. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0018h**

Figure 14-20. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7FFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7FFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7FFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-65. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7FFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.21 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 8h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 0 firewall.

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Table 14-66. Instance Table

Instance Name	Physical Address
CBASS0	**4500 001Ch**

Figure 14-21. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
8h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
8h							

Table 14-68. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	8h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.22 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-69. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0020h**

Figure 14-22. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-71. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.23 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-72. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0024h**

Figure 14-23. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-74. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-74. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.24 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-75. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0028h**

Figure 14-24. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-77. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-77. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.25 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-78. Instance Table

Instance Name	Physical Address
CBASS0	**4500 002Ch**

Figure 14-25. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-80. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-80. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.26 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-81. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0030h**

Figure 14-26. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-83. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.27 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-84. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0034h**

Figure 14-27. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-86. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.28 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-87. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0038h**

Figure 14-28. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-89. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.29 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 1 firewall.

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Table 14-90. Instance Table

Instance Name	Physical Address
CBASS0	**4500 003Ch**

Figure 14-29. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-92. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.30 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-93. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0040h**

Figure 14-30. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-95. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.31 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-96. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0044h**

Figure 14-31. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-98. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-98. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.32 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-99. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0048h**

Figure 14-32. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-101. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-101. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.33 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-102. Instance Table

Instance Name	Physical Address
CBASS0	**4500 004Ch**

Figure 14-33. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-104. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-104. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.34 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-105. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0050h**

Figure 14-34. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-107. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.35 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-108. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0054h**

Figure 14-35. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-110. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.36 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-111. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0058h**

Figure 14-36. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-113. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.37 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 2 firewall.

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Table 14-114. Instance Table

Instance Name	Physical Address
CBASS0	**4500 005Ch**

Figure 14-37. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-116. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.38 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-117. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0060h**

Figure 14-38. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-119. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.39 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-120. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0064h**

Figure 14-39. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-122. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-122. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.40 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-123. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0068h**

Figure 14-40. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-125. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-125. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.41 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-126. Instance Table

Instance Name	Physical Address
CBASS0	**4500 006Ch**

Figure 14-41. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-128. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-128. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.42 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-129. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0070h**

Figure 14-42. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-131. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.43 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-132. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0074h**

Figure 14-43. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-134. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.44 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-135. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0078h**

Figure 14-44. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-137. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.45 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 3 firewall.

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Table 14-138. Instance Table

Instance Name	Physical Address
CBASS0	**4500 007Ch**

Figure 14-45. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-140. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.46 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-141. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0080h**

Figure 14-46. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-143. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.47 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-144. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0084h**

Figure 14-47. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-146. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-146. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.48 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-147. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0088h**

Figure 14-48. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-149. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-149. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.49 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-150. Instance Table

Instance Name	Physical Address
CBASS0	**4500 008Ch**

Figure 14-49. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-152. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-152. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.50 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_L Register (Offset = 90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-153. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0090h**

Figure 14-50. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-155. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.51 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_H Register (Offset = 94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-156. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0094h**

Figure 14-51. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-158. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.52 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_L Register (Offset = 98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-159. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0098h**

Figure 14-52. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-161. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.53 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_H Register (Offset = 9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 4 firewall.

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Table 14-162. Instance Table

Instance Name	Physical Address
CBASS0	**4500 009Ch**

Figure 14-53. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-164. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.54 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_CONTROL Register (Offset = A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-165. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00A0h**

Figure 14-54. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-167. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.55 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0 Register (Offset = A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-168. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00A4h**

Figure 14-55. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-170. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-170. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.56 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1 Register (Offset = A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-171. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00A8h**

Figure 14-56. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-173. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-173. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.57 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2 Register (Offset = ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-174. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 00ACh**

Figure 14-57. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-176. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-176. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.58 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_L Register (Offset = B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-177. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00B0h**

Figure 14-58. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-179. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.59 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_H Register (Offset = B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-180. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00B4h**

Figure 14-59. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-182. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.60 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_L Register (Offset = B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-183. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00B8h**

Figure 14-60. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-185. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.61 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_H Register (Offset = BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 5 firewall.

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Table 14-186. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00BCh**

Figure 14-61. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-188. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.62 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-189. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00C0h**

Figure 14-62. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-191. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.63 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0 Register (Offset = C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-192. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00C4h**

Figure 14-63. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-194. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-194. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.64 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1 Register (Offset = C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-195. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00C8h**

Figure 14-64. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-197. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-197. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.65 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2 Register (Offset = CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-198. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00CCh**

Figure 14-65. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-200. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-200. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.66 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_L Register (Offset = D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-201. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00D0h**

Figure 14-66. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-203. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.67 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_H Register (Offset = D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-204. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00D4h**

Figure 14-67. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-206. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.68 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_L Register (Offset = D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-207. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 00D8h**

Figure 14-68. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-209. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.69 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_H Register (Offset = DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 6 firewall.

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Table 14-210. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00DCh**

Figure 14-69. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-212. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.70 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_CONTROL Register (Offset = E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-213. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00E0h**

Figure 14-70. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-215. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.71 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0 Register (Offset = E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-216. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 00E4h**

Figure 14-71. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-218. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-218. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.72 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1 Register (Offset = E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-219. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00E8h**

Figure 14-72. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-221. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-221. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.73 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2 Register (Offset = ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-222. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00ECh**

Figure 14-73. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-224. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-224. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.74 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_L Register (Offset = F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-225. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00F0h**

Figure 14-74. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-227. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.75 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_H Register (Offset = F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-228. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00F4h**

Figure 14-75. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-230. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.76 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_L Register (Offset = F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-231. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00F8h**

Figure 14-76. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-233. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.77 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_H Register (Offset = FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss_hpt region 7 firewall.

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Table 14-234. Instance Table

Instance Name	Physical Address
CBASS0	**4500 00FCh**

Figure 14-77. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-236. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_HPT_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.78 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-237. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0400h**

Figure 14-78. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-239. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.79 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-240. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0404h**

Figure 14-79. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-242. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-242. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.80 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-243. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0408h**

Figure 14-80. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-245. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-245. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.81 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-246. Instance Table

Instance Name	Physical Address
CBASS0	**4500 040Ch**

Figure 14-81. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-248. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-248. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.82 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-249. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0410h**

Figure 14-82. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-251. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.83 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 9h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-252. Instance Table

Instance Name	Physical Address
CBASS0	4500 0414h

Figure 14-83. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
9h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
9h							

Table 14-254. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	9h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.84 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFFFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-255. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0418h**

Figure 14-84. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
FFFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
FFFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
FFFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-257. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	FFFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.85 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 10h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-258. Instance Table

Instance Name	Physical Address
CBASS0	**4500 041Ch**

Figure 14-85. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
10h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
10h							

Table 14-260. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	10h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.86 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-261. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0420h**

Figure 14-86. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-263. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.87 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-264. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0424h**

Figure 14-87. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-266. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-266. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.88 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-267. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0428h**

Figure 14-88. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-269. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-269. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.89 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-270. Instance Table

Instance Name	Physical Address
CBASS0	**4500 042Ch**

Figure 14-89. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-272. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-272. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.90 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-273. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0430h**

Figure 14-90. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-275. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.91 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-276. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0434h**

Figure 14-91. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-278. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.92 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-279. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0438h**

Figure 14-92. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-281. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.93 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-282. Instance Table

Instance Name	Physical Address
CBASS0	**4500 043Ch**

Figure 14-93. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-284. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.94 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-285. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0440h**

Figure 14-94. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-287. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.95 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-288. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0444h**

Figure 14-95. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-290. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-290. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.96 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-291. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0448h**

Figure 14-96. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-293. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-293. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.97 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-294. Instance Table

Instance Name	Physical Address
CBASS0	**4500 044Ch**

Figure 14-97. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-296. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-296. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.98 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-297. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0450h**

Figure 14-98. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-299. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.99 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-300. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0454h**

Figure 14-99. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-302. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.100 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-303. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0458h**

Figure 14-100. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-305. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.101 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-306. Instance Table

Instance Name	Physical Address
CBASS0	**4500 045Ch**

Figure 14-101. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-308. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.102 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-309. Instance Table

Instance Name	Physical Address
CBASS0	4500 0460h

Figure 14-102. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-311. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.103 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-312. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0464h**

Figure 14-103. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-314. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-314. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.104 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-315. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0468h**

Figure 14-104. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-317. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-317. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.105 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-318. Instance Table

Instance Name	Physical Address
CBASS0	**4500 046Ch**

Figure 14-105. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-320. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-320. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.106 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-321. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0470h**

Figure 14-106. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-323. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.107 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-324. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0474h**

Figure 14-107. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-326. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.108 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-327. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0478h**

Figure 14-108. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-329. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.109 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-330. Instance Table

Instance Name	Physical Address
CBASS0	4500 047Ch

Figure 14-109. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-332. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.110 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-333. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0480h**

Figure 14-110. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-335. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.111 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-336. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0484h**

Figure 14-111. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-338. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-338. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.112 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-339. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0488h**

Figure 14-112. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-341. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-341. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.113 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-342. Instance Table

Instance Name	Physical Address
CBASS0	**4500 048Ch**

Figure 14-113. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-344. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-344. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.114 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-345. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0490h**

Figure 14-114. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-347. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.115 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-348. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0494h**

Figure 14-115. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-350. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.116 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-351. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0498h**

Figure 14-116. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-353. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.117 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-354. Instance Table

Instance Name	Physical Address
CBASS0	**4500 049Ch**

Figure 14-117. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-356. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.118 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-357. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04A0h**

Figure 14-118. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-359. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.119 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-360. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04A4h**

Figure 14-119. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-362. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-362. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.120 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-363. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04A8h**

Figure 14-120. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-365. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-365. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.121 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-366. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 04ACh**

Figure 14-121. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-368. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-368. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.122 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-369. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04B0h**

Figure 14-122. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-371. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.123 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-372. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04B4h**

Figure 14-123. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-374. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.124 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-375. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04B8h**

Figure 14-124. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-377. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.125 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-378. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04BCh**

Figure 14-125. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-380. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.126 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-381. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04C0h**

Figure 14-126. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-383. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.127 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-384. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04C4h**

Figure 14-127. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-386. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-386. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.128 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-387. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04C8h**

Figure 14-128. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-389. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-389. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.129 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-390. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04CCh**

Figure 14-129. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-392. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-392. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.130 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-393. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04D0h**

Figure 14-130. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-395. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.131 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-396. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04D4h**

Figure 14-131. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-398. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.132 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-399. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04D8h**

Figure 14-132. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-401. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.133 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-402. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04DCh**

Figure 14-133. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-404. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.134 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-405. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04E0h**

Figure 14-134. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-407. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.135 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-408. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04E4h**

Figure 14-135. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-410. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-410. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.136 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-411. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04E8h**

Figure 14-136. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-413. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-413. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.137 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-414. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04ECh**

Figure 14-137. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-416. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-416. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.138 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-417. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04F0h**

Figure 14-138. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-419. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.139 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-420. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04F4h**

Figure 14-139. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-422. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.140 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-423. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04F8h**

Figure 14-140. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-425. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.141 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-426. Instance Table

Instance Name	Physical Address
CBASS0	**4500 04FCh**

Figure 14-141. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-428. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.142 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_CONTROL Register (Offset = 500h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-429. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0500h**

Figure 14-142. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-431. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.143 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0 Register (Offset = 504h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-432. Instance Table

Instance Name	Physical Address
CBASS0	4500 0504h

Figure 14-143. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-434. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-434. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.144 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1 Register (Offset = 508h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-435. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0508h**

Figure 14-144. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-437. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-437. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.145 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2 Register (Offset = 50Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-438. Instance Table

Instance Name	Physical Address
CBASS0	**4500 050Ch**

Figure 14-145. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-440. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-440. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.146 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_L Register (Offset = 510h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-441. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0510h**

Figure 14-146. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-443. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.147 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_H Register (Offset = 514h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-444. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0514h**

Figure 14-147. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-446. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.148 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_L Register (Offset = 518h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-447. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0518h**

Figure 14-148. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-449. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.149 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_H Register (Offset = 51Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 8 firewall.

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Table 14-450. Instance Table

Instance Name	Physical Address
CBASS0	**4500 051Ch**

Figure 14-149. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-452. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.150 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_CONTROL Register (Offset = 520h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-453. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0520h**

Figure 14-150. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-455. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.151 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0 Register (Offset = 524h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-456. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0524h**

Figure 14-151. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-458. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-458. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.152 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1 Register (Offset = 528h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-459. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0528h**

Figure 14-152. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-461. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-461. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.153 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2 Register (Offset = 52Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-462. Instance Table

Instance Name	Physical Address
CBASS0	**4500 052Ch**

Figure 14-153. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-464. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-464. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.154 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_L Register (Offset = 530h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-465. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0530h**

Figure 14-154. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-467. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.155 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_H Register (Offset = 534h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-468. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0534h**

Figure 14-155. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-470. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.156 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_L Register (Offset = 538h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-471. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0538h**

Figure 14-156. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-473. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.157 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_H Register (Offset = 53Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 9 firewall.

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Table 14-474. Instance Table

Instance Name	Physical Address
CBASS0	**4500 053Ch**

Figure 14-157. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-476. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.158 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_CONTROL Register (Offset = 540h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-477. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0540h**

Figure 14-158. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_CONTROL Name Register

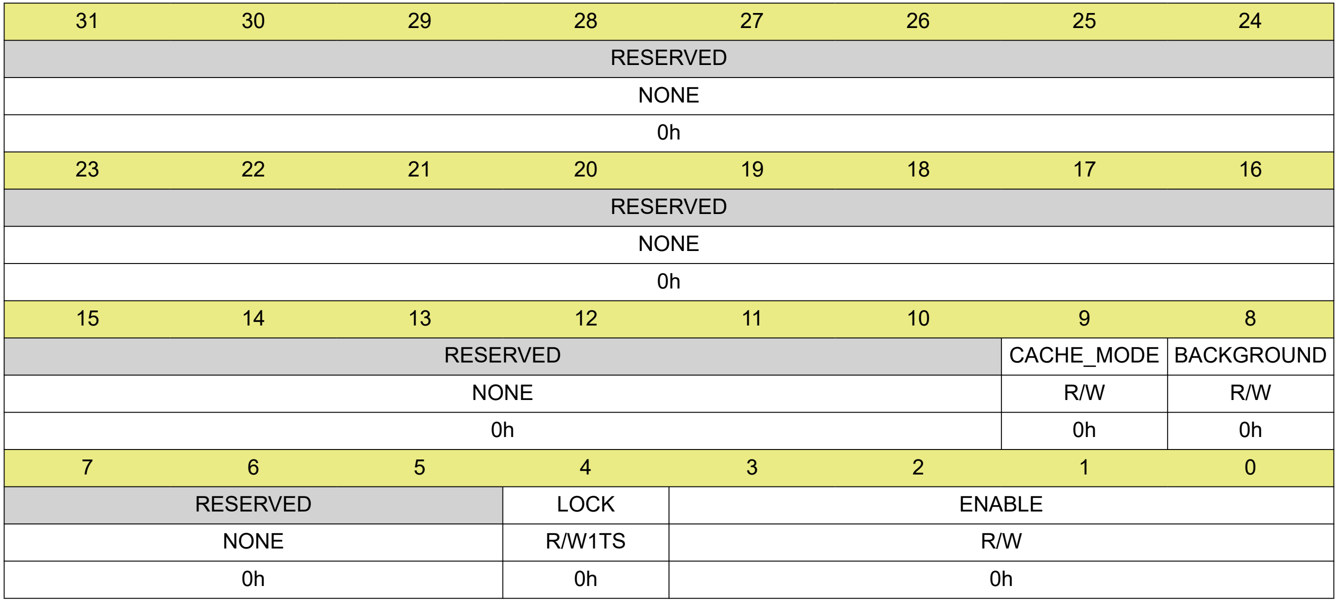

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-479. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.159 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0 Register (Offset = 544h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-480. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0544h**

Figure 14-159. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-482. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-482. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.160 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1 Register (Offset = 548h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-483. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0548h**

Figure 14-160. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-485. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-485. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.161 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2 Register (Offset = 54Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-486. Instance Table

Instance Name	Physical Address
CBASS0	**4500 054Ch**

Figure 14-161. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-488. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-488. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.162 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_L Register (Offset = 550h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-489. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0550h**

Figure 14-162. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-491. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.163 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_H Register (Offset = 554h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

Return to Summary Table

Table 14-492. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0554h**

Figure 14-163. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-494. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.164 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_L Register (Offset = 558h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-495. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0558h**

Figure 14-164. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-497. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.165 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_H Register (Offset = 55Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 10 firewall.

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Table 14-498. Instance Table

Instance Name	Physical Address
CBASS0	4500 055Ch

Figure 14-165. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-500. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.166 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_CONTROL Register (Offset = 560h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-501. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0560h**

Figure 14-166. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-503. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.167 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0 Register (Offset = 564h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-504. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0564h**

Figure 14-167. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-506. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-506. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.168 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1 Register (Offset = 568h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-507. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0568h**

Figure 14-168. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-509. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-509. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.169 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2 Register (Offset = 56Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-510. Instance Table

Instance Name	Physical Address
CBASS0	**4500 056Ch**

Figure 14-169. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-512. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-512. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.170 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_L Register (Offset = 570h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-513. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0570h**

Figure 14-170. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-515. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.171 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_H Register (Offset = 574h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-516. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0574h**

Figure 14-171. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-518. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.172 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_L Register (Offset = 578h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-519. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0578h**

Figure 14-172. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-521. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.173 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_H Register (Offset = 57Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 11 firewall.

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Table 14-522. Instance Table

Instance Name	Physical Address
CBASS0	**4500 057Ch**

Figure 14-173. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-524. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.174 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_CONTROL Register (Offset = 580h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-525. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0580h**

Figure 14-174. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-527. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.175 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0 Register (Offset = 584h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-528. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0584h**

Figure 14-175. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-530. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-530. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.176 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1 Register (Offset = 588h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-531. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0588h**

Figure 14-176. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-533. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-533. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.177 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2 Register (Offset = 58Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-534. Instance Table

Instance Name	Physical Address
CBASS0	**4500 058Ch**

Figure 14-177. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-536. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-536. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.178 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_L Register (Offset = 590h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-537. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0590h**

Figure 14-178. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-539. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.179 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_H Register (Offset = 594h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-540. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0594h**

Figure 14-179. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-542. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.180 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_L Register (Offset = 598h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-543. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0598h**

Figure 14-180. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-545. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.181 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_H Register (Offset = 59Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 12 firewall.

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Table 14-546. Instance Table

Instance Name	Physical Address
CBASS0	**4500 059Ch**

Figure 14-181. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-548. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.182 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_CONTROL Register (Offset = 5A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

Return to Summary Table

Table 14-549. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05A0h**

Figure 14-182. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-551. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.183 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0 Register (Offset = 5A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

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Table 14-552. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05A4h**

Figure 14-183. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-554. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-554. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.184 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1 Register (Offset = 5A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

Return to Summary Table

Table 14-555. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05A8h**

Figure 14-184. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-557. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-557. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.185 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2 Register (Offset = 5ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

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Table 14-558. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05ACh**

Figure 14-185. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-560. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-560. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.186 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_L Register (Offset = 5B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

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Table 14-561. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05B0h**

Figure 14-186. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-563. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.187 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_H Register (Offset = 5B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

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Table 14-564. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05B4h**

Figure 14-187. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-566. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.188 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_L Register (Offset = 5B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

Return to Summary Table

Table 14-567. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05B8h**

Figure 14-188. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-569. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.189 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_H Register (Offset = 5BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 13 firewall.

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Table 14-570. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05BCh**

Figure 14-189. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-572. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.190 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_CONTROL Register (Offset = 5C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-573. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05C0h**

Figure 14-190. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-575. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.191 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0 Register (Offset = 5C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-576. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05C4h**

Figure 14-191. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-578. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-578. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.192 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1 Register (Offset = 5C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-579. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05C8h**

Figure 14-192. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-581. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-581. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.193 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2 Register (Offset = 5CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-582. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 05CCh**

Figure 14-193. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-584. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-584. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.194 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_L Register (Offset = 5D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-585. Instance Table

Instance Name	Physical Address
CBASS0	4500 05D0h

Figure 14-194. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-587. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.195 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_H Register (Offset = 5D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-588. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05D4h**

Figure 14-195. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-590. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.196 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_L Register (Offset = 5D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-591. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05D8h**

Figure 14-196. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-593. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.197 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_H Register (Offset = 5DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 14 firewall.

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Table 14-594. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05DCh**

Figure 14-197. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-596. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.198 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_CONTROL Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_CONTROL Register (Offset = 5E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-597. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05E0h**

Figure 14-198. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-599. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.199 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0 Register (Offset = 5E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

Return to Summary Table

Table 14-600. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05E4h**

Figure 14-199. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-602. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-602. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.200 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1 Register (Offset = 5E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-603. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05E8h**

Figure 14-200. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-605. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-605. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.201 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2 Register (Offset = 5ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-606. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05ECh**

Figure 14-201. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-608. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-608. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.202 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_L Register (Offset = 5F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-609. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05F0h**

Figure 14-202. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-611. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.203 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_H Register (Offset = 5F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-612. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05F4h**

Figure 14-203. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-614. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.204 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_L Register (Offset = 5F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-615. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05F8h**

Figure 14-204. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-617. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.205 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_H Register (Offset = 5FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_ddr_wrap_main_0.ddrss region 15 firewall.

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Table 14-618. Instance Table

Instance Name	Physical Address
CBASS0	**4500 05FCh**

Figure 14-205. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-620. CBASS_FW_ISAM62A_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.206 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-621. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0800h**

Figure 14-206. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-623. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-623. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.207 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-624. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0804h**

Figure 14-207. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-626. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-626. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.208 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-627. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0808h**

Figure 14-208. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-629. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-629. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.209 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-630. Instance Table

Instance Name	Physical Address
CBASS0	**4500 080Ch**

Figure 14-209. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-632. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-632. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.210 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-633. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0810h**

Figure 14-210. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-635. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.211 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-636. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0814h**

Figure 14-211. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-638. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.212
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFFFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-639. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0818h**

Figure 14-212. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
FFFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
FFFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
FFFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-641. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	FFFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.213 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = Fh]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 0 firewall.

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Table 14-642. Instance Table

Instance Name	Physical Address
CBASS0	**4500 081Ch**

Figure 14-213. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
Fh							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
Fh							

Table 14-644. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	Fh	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.214 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-645. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0820h**

Figure 14-214. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-647. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-647. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.215 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-648. Instance Table

Instance Name	Physical Address
CBASS0	4500 0824h

Figure 14-215. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-650. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-650. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.216 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-651. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0828h**

Figure 14-216. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-653. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-653. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.217
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-654. Instance Table

Instance Name	Physical Address
CBASS0	**4500 082Ch**

Figure 14-217. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-656. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-656. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.218 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-657. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0830h**

Figure 14-218. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-659. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.219 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-660. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0834h**

Figure 14-219. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-662. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.220 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-663. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0838h**

Figure 14-220. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-665. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.221 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 1 firewall.

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Table 14-666. Instance Table

Instance Name	Physical Address
CBASS0	**4500 083Ch**

Figure 14-221. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-668. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.222 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-669. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0840h**

Figure 14-222. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-671. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-671. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.223 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-672. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0844h**

Figure 14-223. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-674. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-674. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.224

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-675. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0848h**

Figure 14-224. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-677. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-677. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.225 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-678. Instance Table

Instance Name	Physical Address
CBASS0	4500 084Ch

Figure 14-225. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-680. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-680. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.226 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-681. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0850h**

Figure 14-226. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-683. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.227 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-684. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0854h**

Figure 14-227. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-686. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.228
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-687. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0858h**

Figure 14-228. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-689. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.229 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 2 firewall.

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Table 14-690. Instance Table

Instance Name	Physical Address
CBASS0	**4500 085Ch**

Figure 14-229. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-692. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.230
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-693. Instance Table

Instance Name	Physical Address
CBASS0	4500 0860h

Figure 14-230. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-695. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-695. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.231 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-696. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0864h**

Figure 14-231. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-698. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-698. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.232 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-699. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0868h**

Figure 14-232. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-701. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-701. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.233 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-702. Instance Table

Instance Name	Physical Address
CBASS0	**4500 086Ch**

Figure 14-233. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-704. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-704. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.234
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-705. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0870h**

Figure 14-234. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-707. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.235 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-708. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0874h**

Figure 14-235. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-710. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.236 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-711. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0878h**

Figure 14-236. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-713. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.237 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 3 firewall.

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Table 14-714. Instance Table

Instance Name	Physical Address
CBASS0	**4500 087Ch**

Figure 14-237. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-716. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.238 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-717. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0880h**

Figure 14-238. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-719. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-719. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.239
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-720. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0884h**

Figure 14-239. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-722. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-722. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.240 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-723. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0888h**

Figure 14-240. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-725. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-725. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.241 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-726. Instance Table

Instance Name	Physical Address
CBASS0	**4500 088Ch**

Figure 14-241. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-728. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-728. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.242 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-729. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0890h**

Figure 14-242. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-731. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.243 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-732. Instance Table

Instance Name	Physical Address
CBASS0	4500 0894h

Figure 14-243. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-734. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.244 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-735. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0898h**

Figure 14-244. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-737. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.245 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 4 firewall.

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Table 14-738. Instance Table

Instance Name	Physical Address
CBASS0	**4500 089Ch**

Figure 14-245. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-740. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.246 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-741. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08A0h**

Figure 14-246. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-743. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-743. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.247
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-744. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08A4h**

Figure 14-247. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-746. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-746. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.248 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-747. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08A8h**

Figure 14-248. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-749. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-749. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.249 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-750. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08ACh**

Figure 14-249. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-752. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-752. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.250 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

Return to Summary Table

Table 14-753. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08B0h**

Figure 14-250. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-755. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.251 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-756. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08B4h**

Figure 14-251. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-758. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.252 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-759. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08B8h**

Figure 14-252. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-761. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.253 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 5 firewall.

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Table 14-762. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08BCh**

Figure 14-253. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-764. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.254 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

Return to Summary Table

Table 14-765. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08C0h**

Figure 14-254. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-767. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-767. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.255 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

Return to Summary Table

Table 14-768. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08C4h**

Figure 14-255. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-770. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-770. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.256 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

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Table 14-771. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08C8h**

Figure 14-256. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-773. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-773. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.257 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

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Table 14-774. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08CCh**

Figure 14-257. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-776. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-776. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.258 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

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Table 14-777. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08D0h**

Figure 14-258. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-779. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.259 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

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Table 14-780. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08D4h**

Figure 14-259. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-782. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.260
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

Return to Summary Table

Table 14-783. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08D8h**

Figure 14-260. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-785. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.261 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 6 firewall.

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Table 14-786. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08DCh**

Figure 14-261. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-788. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.262 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-789. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08E0h**

Figure 14-262. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-791. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-791. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.263 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-792. Instance Table

Instance Name	Physical Address
CBASS0	4500 08E4h

Figure 14-263. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-794. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-794. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.264
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-795. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08E8h**

Figure 14-264. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-797. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-797. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.265 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-798. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08ECh**

Figure 14-265. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-800. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-800. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.266 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-801. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08F0h**

Figure 14-266. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-803. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.267 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-804. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08F4h**

Figure 14-267. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-806. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.268
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register

1
CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-807. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08F8h**

Figure 14-268. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-809. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.269

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_acp_w region 7 firewall.

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Table 14-810. Instance Table

Instance Name	Physical Address
CBASS0	**4500 08FCh**

Figure 14-269. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-812. CBASS_FW_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.270 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_CONTROL Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-813. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C00h**

Figure 14-270. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-815. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.271 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-816. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C04h**

Figure 14-271. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-818. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-818. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.272 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-819. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C08h**

Figure 14-272. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-821. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-821. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.273 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-822. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C0Ch**

Figure 14-273. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-824. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-824. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.274 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-825. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C10h**

Figure 14-274. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-827. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.275 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 7h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-828. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C14h**

Figure 14-275. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
7h							

Table 14-830. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	7h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.276 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-831. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C18h**

Figure 14-276. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-833. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.277 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 7h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 0 firewall.

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Table 14-834. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0C1Ch**

Figure 14-277. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7h</td></tr>
</table>

Table 14-836. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	7h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.278 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_CONTROL Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_CONTROL Register (Offset = C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

Return to Summary Table

Table 14-837. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C20h**

Figure 14-278. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-839. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.279 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0 Register (Offset = C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

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Table 14-840. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C24h**

Figure 14-279. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-842. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-842. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.280 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1 Register (Offset = C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

Return to Summary Table

Table 14-843. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C28h**

Figure 14-280. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-845. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-845. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.281 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2 Register (Offset = C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

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Table 14-846. Instance Table

Instance Name	Physical Address
CBASS0	4500 0C2Ch

Figure 14-281. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-848. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-848. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.282 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 1000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

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Table 14-849. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C30h**

Figure 14-282. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
1h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
1h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
1h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-851. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	1h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.283 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 7h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

Return to Summary Table

Table 14-852. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C34h**

Figure 14-283. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
7h							

Table 14-854. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	7h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.284 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = 1FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

Return to Summary Table

Table 14-855. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C38h**

Figure 14-284. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-857. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	1h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.285 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 7h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 1 firewall.

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Table 14-858. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C3Ch**

Figure 14-285. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
7h							

Table 14-860. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	7h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.286 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_CONTROL Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_CONTROL Register (Offset = C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

Return to Summary Table

Table 14-861. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C40h**

Figure 14-286. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-863. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.287 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0 Register (Offset = C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

Return to Summary Table

Table 14-864. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C44h**

Figure 14-287. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-866. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-866. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.288 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1 Register (Offset = C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

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Table 14-867. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C48h**

Figure 14-288. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-869. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-869. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.289 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2 Register (Offset = C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

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Table 14-870. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C4Ch**

Figure 14-289. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-872. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-872. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.290 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 2000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

Return to Summary Table

Table 14-873. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C50h**

Figure 14-290. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-875. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.291 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 7h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

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Table 14-876. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 0C54h**

Figure 14-291. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
7h							

Table 14-878. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	7h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.292 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = 2FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

Return to Summary Table

Table 14-879. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C58h**

Figure 14-292. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-881. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.293 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 7h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 2 firewall.

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Table 14-882. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C5Ch**

Figure 14-293. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
7h							

Table 14-884. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	7h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.294 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_CONTROL Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_CONTROL Register (Offset = C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-885. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C60h**

Figure 14-294. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-887. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.295 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0 Register (Offset = C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-888. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C64h**

Figure 14-295. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-890. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-890. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.296 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1 Register (Offset = C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-891. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C68h**

Figure 14-296. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-893. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-893. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.297 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2 Register (Offset = C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

Return to Summary Table

Table 14-894. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C6Ch**

Figure 14-297. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-896. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-896. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.298 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 2000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

Return to Summary Table

Table 14-897. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C70h**

Figure 14-298. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-899. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.299 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 7h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-900. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C74h**

Figure 14-299. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
7h							

Table 14-902. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	7h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.300 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = 2FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-903. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C78h**

Figure 14-300. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-905. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.301 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 7h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Idebugss_k3_wrap_cv0_main_0.vbusp_cfg region 3 firewall.

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Table 14-906. Instance Table

Instance Name	Physical Address
CBASS0	**4500 0C7Ch**

Figure 14-301. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
7h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
7h							

Table 14-908. CBASS_FW_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSP_CFG_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	7h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.302 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register (Offset = 1000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-909. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1000h**

Figure 14-302. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-911. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.303 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register (Offset = 1004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-912. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1004h**

Figure 14-303. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-914. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-914. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.304 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register (Offset = 1008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-915. Instance Table

Instance Name	Physical Address
CBASS0	4500 1008h

Figure 14-304. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-917. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-917. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.305 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register (Offset = 100Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-918. Instance Table

Instance Name	Physical Address
CBASS0	**4500 100Ch**

Figure 14-305. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-920. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-920. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.306 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 7E000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-921. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1010h**

Figure 14-306. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7E000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-923. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7E000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.307 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-924. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1014h**

Figure 14-307. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-926. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.308 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = 7E0FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-927. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1018h**

Figure 14-308. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7E0FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7E0FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7E0FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-929. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7E0FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.309 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 0 firewall.

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Table 14-930. Instance Table

Instance Name	Physical Address
CBASS0	**4500 101Ch**

Figure 14-309. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-932. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.310 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register (Offset = 1020h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-933. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1020h**

Figure 14-310. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-935. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.311 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register (Offset = 1024h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-936. Instance Table

Instance Name	Physical Address
CBASS0	4500 1024h

Figure 14-311. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-938. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-938. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.312 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register (Offset = 1028h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-939. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1028h**

Figure 14-312. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-941. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-941. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.313 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register (Offset = 102Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-942. Instance Table

Instance Name	Physical Address
CBASS0	4500 102Ch

Figure 14-313. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-944. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-944. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.314 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1030h) [reset = 7F000000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-945. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1030h**

Figure 14-314. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7F000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7F000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7F000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-947. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7F000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.315 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1034h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-948. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1034h**

Figure 14-315. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-950. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.316 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1038h) [reset = 7F03FFFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-951. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1038h**

Figure 14-316. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7F03Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
7F03Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7F03Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-953. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7F03Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.317 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register (Offset = 103Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 1 firewall.

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Table 14-954. Instance Table

Instance Name	Physical Address
CBASS0	**4500 103Ch**

Figure 14-317. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-956. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.318 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register (Offset = 1040h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-957. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1040h**

Figure 14-318. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-959. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.319 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register (Offset = 1044h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-960. Instance Table

Instance Name	Physical Address
CBASS0	4500 1044h

Figure 14-319. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-962. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-962. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.320 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register (Offset = 1048h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-963. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1048h**

Figure 14-320. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-965. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-965. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.321 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register (Offset = 104Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-966. Instance Table

Instance Name	Physical Address
CBASS0	**4500 104Ch**

Figure 14-321. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-968. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-968. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.322 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1050h) [reset = 7C000000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-969. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1050h**

Figure 14-322. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7C000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-971. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.323 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1054h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-972. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1054h**

Figure 14-323. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-974. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.324 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1058h) [reset = 7C01FFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-975. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1058h**

Figure 14-324. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C01Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C01Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C01Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-977. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C01Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.325 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register (Offset = 105Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 2 firewall.

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Table 14-978. Instance Table

Instance Name	Physical Address
CBASS0	**4500 105Ch**

Figure 14-325. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-980. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.326 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register (Offset = 1060h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-981. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1060h**

Figure 14-326. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-983. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.327 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register (Offset = 1064h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-984. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1064h**

Figure 14-327. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-986. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-986. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.328 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register (Offset = 1068h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-987. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1068h**

Figure 14-328. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-989. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-989. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.329 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register (Offset = 106Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-990. Instance Table

Instance Name	Physical Address
CBASS0	**4500 106Ch**

Figure 14-329. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-992. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-992. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.330 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1070h) [reset = 7C400000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-993. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1070h**

Figure 14-330. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C400h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7C400h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C400h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-995. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C400h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.331 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1074h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-996. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1074h**

Figure 14-331. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-998. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.332 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1078h) [reset = 7C403FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-999. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1078h**

Figure 14-332. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C403h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C403h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C403h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1001. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C403h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.333 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register (Offset = 107Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 3 firewall.

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Table 14-1002. Instance Table

Instance Name	Physical Address
CBASS0	**4500 107Ch**

Figure 14-333. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1004. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.334 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register (Offset = 1080h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1005. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1080h**

Figure 14-334. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1007. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.335 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register (Offset = 1084h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1008. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1084h**

Figure 14-335. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1010. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1010. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.336 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register (Offset = 1088h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1011. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1088h**

Figure 14-336. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1013. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1013. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.337 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register (Offset = 108Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1014. Instance Table

Instance Name	Physical Address
CBASS0	**4500 108Ch**

Figure 14-337. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1016. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1016. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.338 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1090h) [reset = 7C408000h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1017. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1090h**

Figure 14-338. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C408h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7C408h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C408h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1019. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C408h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.339 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1094h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1020. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1094h**

Figure 14-339. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1022. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.340 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1098h) [reset = 7C40FFFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1023. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1098h**

Figure 14-340. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C40Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
7C40Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C40Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1025. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C40Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.341 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register (Offset = 109Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 4 firewall.

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Table 14-1026. Instance Table

Instance Name	Physical Address
CBASS0	**4500 109Ch**

Figure 14-341. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1028. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.342 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register (Offset = 10A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1029. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10A0h**

Figure 14-342. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1031. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.343 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register (Offset = 10A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1032. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10A4h**

Figure 14-343. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1034. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1034. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.344 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register (Offset = 10A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1035. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10A8h**

Figure 14-344. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1037. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1037. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.345 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register (Offset = 10ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1038. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10ACh**

Figure 14-345. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1040. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1040. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.346 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register (Offset = 10B0h) [reset = 7C404000h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1041. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10B0h**

Figure 14-346. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C404h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C404h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C404h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1043. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C404h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.347 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register (Offset = 10B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1044. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10B4h**

Figure 14-347. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1046. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.348 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register (Offset = 10B8h) [reset = 7C407FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1047. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10B8h**

Figure 14-348. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C407h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C407h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C407h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1049. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C407h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.349 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register (Offset = 10BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 5 firewall.

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Table 14-1050. Instance Table

Instance Name	Physical Address
CBASS0	4500 10BCh

Figure 14-349. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1052. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.350 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register (Offset = 10C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1053. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10C0h**

Figure 14-350. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1055. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.351 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register (Offset = 10C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1056. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10C4h**

Figure 14-351. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1058. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1058. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.352 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register (Offset = 10C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1059. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10C8h**

Figure 14-352. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1061. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1061. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.353 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register (Offset = 10CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1062. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10CCh**

Figure 14-353. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1064. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1064. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.354 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register (Offset = 10D0h) [reset = 7C440000h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1065. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10D0h**

Figure 14-354. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C440h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C440h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C440h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1067. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C440h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.355 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register (Offset = 10D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1068. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10D4h**

Figure 14-355. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1070. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.356 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register (Offset = 10D8h) [reset = 7C45FFFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1071. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10D8h**

Figure 14-356. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C45Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
7C45Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C45Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1073. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C45Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.357 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register (Offset = 10DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 6 firewall.

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Table 14-1074. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10DCh**

Figure 14-357. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1076. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.358 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register (Offset = 10E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1077. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10E0h**

Figure 14-358. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1079. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.359 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register (Offset = 10E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1080. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10E4h**

Figure 14-359. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1082. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1082. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.360 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register (Offset = 10E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1083. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10E8h**

Figure 14-360. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1085. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1085. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.361 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register (Offset = 10ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1086. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10ECh**

Figure 14-361. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1088. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1088. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.362 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register (Offset = 10F0h) [reset = 7C460000h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1089. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10F0h**

Figure 14-362. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C460h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7C460h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C460h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1091. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C460h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.363 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register (Offset = 10F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1092. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10F4h**

Figure 14-363. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1094. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.364 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register (Offset = 10F8h) [reset = 7C47FFFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1095. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10F8h**

Figure 14-364. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C47Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C47Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C47Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1097. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C47Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.365 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register (Offset = 10FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_c7xv_wrap_main_0.soc_c7xv region 7 firewall.

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Table 14-1098. Instance Table

Instance Name	Physical Address
CBASS0	**4500 10FCh**

Figure 14-365. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1100. CBASS_FW_ISAM62A_C7XV_WRAP_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.366 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_CONTROL Register (Offset = 1400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1101. Instance Table

Instance Name	Physical Address
CBASS0	4500 1400h

Figure 14-366. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1103. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.367 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 1404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1104. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1404h**

Figure 14-367. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1106. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1106. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.368 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 1408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1107. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1408h**

Figure 14-368. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1109. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1109. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.369 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 140Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1110. Instance Table

Instance Name	Physical Address
CBASS0	**4500 140Ch**

Figure 14-369. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1112. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1112. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.370 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 71000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1113. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1410h**

Figure 14-370. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">71000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">71000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">71000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1115. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	71000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.371 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1116. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1414h**

Figure 14-371. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1118. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.372 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = 7107FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1119. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1418h**

Figure 14-372. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7107Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7107Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7107Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1121. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7107Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.373 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 0 firewall.

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Table 14-1122. Instance Table

Instance Name	Physical Address
CBASS0	**4500 141Ch**

Figure 14-373. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1124. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.374 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_CONTROL Register (Offset = 1420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1125. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1420h**

Figure 14-374. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1127. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.375 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 1424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1128. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1424h**

Figure 14-375. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1130. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1130. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.376 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 1428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1131. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1428h**

Figure 14-376. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1133. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1133. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.377 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 142Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1134. Instance Table

Instance Name	Physical Address
CBASS0	**4500 142Ch**

Figure 14-377. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1136. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1136. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.378 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1137. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1430h**

Figure 14-378. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1139. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.379 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1140. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1434h**

Figure 14-379. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1142. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.380 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1143. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1438h**

Figure 14-380. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1145. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.381 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 143Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 1 firewall.

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Table 14-1146. Instance Table

Instance Name	Physical Address
CBASS0	**4500 143Ch**

Figure 14-381. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1148. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.382 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_CONTROL Register (Offset = 1440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1149. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1440h**

Figure 14-382. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1151. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.383 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 1444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1152. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1444h**

Figure 14-383. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1154. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1154. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.384 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 1448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1155. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1448h**

Figure 14-384. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1157. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1157. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.385 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 144Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1158. Instance Table

Instance Name	Physical Address
CBASS0	**4500 144Ch**

Figure 14-385. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1160. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1160. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.386 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1161. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1450h**

Figure 14-386. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1163. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.387 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1164. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1454h**

Figure 14-387. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1166. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.388 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1167. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1458h**

Figure 14-388. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1169. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.389 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 145Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 2 firewall.

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Table 14-1170. Instance Table

Instance Name	Physical Address
CBASS0	4500 145Ch

Figure 14-389. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-1172. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.390 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_CONTROL Register (Offset = 1460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1173. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1460h**

Figure 14-390. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1175. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.391 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 1464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1176. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1464h**

Figure 14-391. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1178. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1178. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.392 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 1468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1179. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1468h**

Figure 14-392. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1181. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1181. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.393 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 146Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1182. Instance Table

Instance Name	Physical Address
CBASS0	**4500 146Ch**

Figure 14-393. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1184. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1184. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.394 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1185. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1470h**

Figure 14-394. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1187. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.395 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1188. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1474h**

Figure 14-395. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1190. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.396 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1191. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1478h**

Figure 14-396. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1193. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.397 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 147Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 3 firewall.

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Table 14-1194. Instance Table

Instance Name	Physical Address
CBASS0	**4500 147Ch**

Figure 14-397. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1196. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.398 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_CONTROL Register (Offset = 1480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1197. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1480h**

Figure 14-398. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1199. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.399 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 1484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1200. Instance Table

Instance Name	Physical Address
CBASS0	4500 1484h

Figure 14-399. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1202. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1202. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.400 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 1488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1203. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1488h**

Figure 14-400. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1205. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1205. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.401 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 148Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1206. Instance Table

Instance Name	Physical Address
CBASS0	**4500 148Ch**

Figure 14-401. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1208. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1208. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.402 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1209. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1490h**

Figure 14-402. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1211. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.403 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1212. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1494h**

Figure 14-403. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1214. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.404 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1215. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1498h**

Figure 14-404. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1217. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.405 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 149Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 4 firewall.

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Table 14-1218. Instance Table

Instance Name	Physical Address
CBASS0	**4500 149Ch**

Figure 14-405. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1220. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.406 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_CONTROL Register (Offset = 14A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1221. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14A0h**

Figure 14-406. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1223. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.407 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 14A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1224. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 14A4h**

Figure 14-407. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1226. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1226. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.408 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 14A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1227. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14A8h**

Figure 14-408. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1229. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1229. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.409 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 14ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1230. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14ACh**

Figure 14-409. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1232. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1232. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.410 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 14B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1233. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14B0h**

Figure 14-410. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1235. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.411 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 14B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1236. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14B4h**

Figure 14-411. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1238. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.412 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 14B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1239. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14B8h**

Figure 14-412. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1241. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.413 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 14BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 5 firewall.

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Table 14-1242. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14BCh**

Figure 14-413. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1244. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.414 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_CONTROL Register (Offset = 14C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1245. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14C0h**

Figure 14-414. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1247. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.415 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 14C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1248. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14C4h**

Figure 14-415. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1250. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1250. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.416 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 14C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1251. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14C8h**

Figure 14-416. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1253. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1253. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.417 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 14CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1254. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14CCh**

Figure 14-417. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1256. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1256. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.418 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 14D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1257. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14D0h**

Figure 14-418. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1259. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.419 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 14D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1260. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14D4h**

Figure 14-419. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1262. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.420 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 14D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1263. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 14D8h**

Figure 14-420. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1265. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.421 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 14DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 6 firewall.

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Table 14-1266. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14DCh**

Figure 14-421. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1268. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.422 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_CONTROL Register (Offset = 14E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1269. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14E0h**

Figure 14-422. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1271. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.423 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 14E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1272. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14E4h**

Figure 14-423. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1274. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1274. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.424 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 14E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1275. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14E8h**

Figure 14-424. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1277. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1277. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.425 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 14ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1278. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14ECh**

Figure 14-425. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1280. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1280. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.426 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 14F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1281. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14F0h**

Figure 14-426. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1283. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.427 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 14F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1284. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14F4h**

Figure 14-427. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1286. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.428 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 14F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1287. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14F8h**

Figure 14-428. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1289. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.429 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 14FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.mem_slv region 7 firewall.

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Table 14-1290. Instance Table

Instance Name	Physical Address
CBASS0	**4500 14FCh**

Figure 14-429. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1292. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_MEM_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.430 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_CONTROL Register (Offset = 1800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1293. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1800h**

Figure 14-430. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1295. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.431 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0 Register (Offset = 1804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1296. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1804h**

Figure 14-431. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1298. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1298. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.432 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1 Register (Offset = 1808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1299. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1808h**

Figure 14-432. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1301. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1301. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.433 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2 Register (Offset = 180Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1302. Instance Table

Instance Name	Physical Address
CBASS0	**4500 180Ch**

Figure 14-433. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1304. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1304. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.434 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_L Register (Offset = 1810h) [reset = 50000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target lgpmc_main_0.gpmc region 0 firewall.

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Table 14-1305. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1810h**

Figure 14-434. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">50000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">50000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">50000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1307. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	50000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.435 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_H Register (Offset = 1814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1308. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1814h**

Figure 14-435. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1310. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.436 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_L Register (Offset = 1818h) [reset = 8FFFFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1311. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1818h**

Figure 14-436. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
8FFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
8FFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
8FFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1313. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	8FFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.437 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_H Register (Offset = 181Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 0 firewall.

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Table 14-1314. Instance Table

Instance Name	Physical Address
CBASS0	**4500 181Ch**

Figure 14-437. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1316. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.438 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_CONTROL Register (Offset = 1820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1317. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1820h**

Figure 14-438. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1319. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.439 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0 Register (Offset = 1824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1320. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1824h**

Figure 14-439. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1322. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1322. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.440 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1 Register (Offset = 1828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1323. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1828h**

Figure 14-440. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1325. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1325. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.441 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2 Register (Offset = 182Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1326. Instance Table

Instance Name	Physical Address
CBASS0	**4500 182Ch**

Figure 14-441. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1328. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1328. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.442 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_L Register (Offset = 1830h) [reset = 3B000000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1329. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1830h**

Figure 14-442. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3B000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3B000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">3B000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1331. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	3B000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.443 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_H Register (Offset = 1834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1332. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1834h**

Figure 14-443. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1334. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.444 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_L Register (Offset = 1838h) [reset = 3B000FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target lgpmc_main_0.gpmc region 1 firewall.

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Table 14-1335. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1838h**

Figure 14-444. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3B000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3B000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">3B000h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1337. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	3B000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.445 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_H Register (Offset = 183Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 1 firewall.

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Table 14-1338. Instance Table

Instance Name	Physical Address
CBASS0	**4500 183Ch**

Figure 14-445. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1340. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.446 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_CONTROL Register (Offset = 1840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1341. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1840h**

Figure 14-446. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1343. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.447 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0 Register (Offset = 1844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1344. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1844h**

Figure 14-447. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1346. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1346. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.448 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1 Register (Offset = 1848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1347. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1848h**

Figure 14-448. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1349. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1349. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.449 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2 Register (Offset = 184Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1350. Instance Table

Instance Name	Physical Address
CBASS0	**4500 184Ch**

Figure 14-449. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1352. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1352. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.450 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_L Register (Offset = 1850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1353. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1850h**

Figure 14-450. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1355. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.451 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_H Register (Offset = 1854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1356. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1854h**

Figure 14-451. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1358. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.452 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_L Register (Offset = 1858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 2 firewall.

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Table 14-1359. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1858h**

Figure 14-452. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1361. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.453 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_H Register (Offset = 185Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target lgpmc_main_0.gpmc region 2 firewall.

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Table 14-1362. Instance Table

Instance Name	Physical Address
CBASS0	**4500 185Ch**

Figure 14-453. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1364. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.454 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_CONTROL Register (Offset = 1860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1365. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1860h**

Figure 14-454. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1367. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.455 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0 Register (Offset = 1864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1368. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1864h**

Figure 14-455. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1370. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1370. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.456 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1 Register (Offset = 1868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1371. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1868h**

Figure 14-456. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1373. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1373. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.457 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2 Register (Offset = 186Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1374. Instance Table

Instance Name	Physical Address
CBASS0	**4500 186Ch**

Figure 14-457. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1376. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1376. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.458 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_L Register (Offset = 1870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1377. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1870h**

Figure 14-458. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1379. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.459 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_H Register (Offset = 1874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1380. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1874h**

Figure 14-459. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1382. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.460 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_L Register (Offset = 1878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1383. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1878h**

Figure 14-460. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1385. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.461 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_H Register (Offset = 187Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 3 firewall.

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Table 14-1386. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 187Ch**

Figure 14-461. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1388. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.462 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_CONTROL Register (Offset = 1880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1389. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1880h**

Figure 14-462. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1391. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.463 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0 Register (Offset = 1884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1392. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1884h**

Figure 14-463. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1394. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1394. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.464 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1 Register (Offset = 1888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1395. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1888h**

Figure 14-464. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1397. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1397. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.465 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2 Register (Offset = 188Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1398. Instance Table

Instance Name	Physical Address
CBASS0	**4500 188Ch**

Figure 14-465. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1400. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1400. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.466 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_L Register (Offset = 1890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1401. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1890h**

Figure 14-466. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1403. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.467 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_H Register (Offset = 1894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1404. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1894h**

Figure 14-467. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1406. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.468 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_L Register (Offset = 1898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1407. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1898h**

Figure 14-468. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1409. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.469 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_H Register (Offset = 189Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 4 firewall.

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Table 14-1410. Instance Table

Instance Name	Physical Address
CBASS0	**4500 189Ch**

Figure 14-469. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1412. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.470 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_CONTROL Register (Offset = 18A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1413. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18A0h**

Figure 14-470. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1415. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.471 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0 Register (Offset = 18A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1416. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18A4h**

Figure 14-471. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1418. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1418. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.472 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1 Register (Offset = 18A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1419. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18A8h**

Figure 14-472. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1421. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1421. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.473 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2 Register (Offset = 18ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1422. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18ACh**

Figure 14-473. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1424. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1424. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.474 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_L Register (Offset = 18B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1425. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18B0h**

Figure 14-474. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1427. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.475 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_H Register (Offset = 18B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1428. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18B4h**

Figure 14-475. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1430. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.476 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_L Register (Offset = 18B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1431. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18B8h**

Figure 14-476. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1433. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.477 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_H Register (Offset = 18BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 5 firewall.

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Table 14-1434. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 18BCh**

Figure 14-477. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1436. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.478 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_CONTROL Register (Offset = 18C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1437. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18C0h**

Figure 14-478. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1439. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.479 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0 Register (Offset = 18C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1440. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18C4h**

Figure 14-479. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1442. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1442. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.480 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1 Register (Offset = 18C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1443. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18C8h**

Figure 14-480. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1445. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1445. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.481 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2 Register (Offset = 18CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1446. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18CCh**

Figure 14-481. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1448. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1448. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.482 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_L Register (Offset = 18D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1449. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18D0h**

Figure 14-482. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1451. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.483 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_H Register (Offset = 18D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1452. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18D4h**

Figure 14-483. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1454. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.484 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_L Register (Offset = 18D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1455. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18D8h**

Figure 14-484. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1457. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.485 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_H Register (Offset = 18DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 6 firewall.

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Table 14-1458. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 18DCh**

Figure 14-485. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1460. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.486 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_CONTROL Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_CONTROL Register (Offset = 18E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1461. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18E0h**

Figure 14-486. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1463. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.487 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0 Register (Offset = 18E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1464. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18E4h**

Figure 14-487. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1466. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1466. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.488 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1 Register (Offset = 18E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1467. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18E8h**

Figure 14-488. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1469. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1469. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.489 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2 Register (Offset = 18ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1470. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18ECh**

Figure 14-489. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1472. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1472. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.490 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_L Register (Offset = 18F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target lgpmc_main_0.gpmc region 7 firewall.

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Table 14-1473. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18F0h**

Figure 14-490. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1475. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.491 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_H Register (Offset = 18F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1476. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18F4h**

Figure 14-491. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1478. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.492 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_L Register (Offset = 18F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1479. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18F8h**

Figure 14-492. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1481. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.493 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_H Register (Offset = 18FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Igpmc_main_0.gpmc region 7 firewall.

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Table 14-1482. Instance Table

Instance Name	Physical Address
CBASS0	**4500 18FCh**

Figure 14-493. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1484. CBASS_FW_IGPMC_MAIN_0_GPMC_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.494 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_CONTROL Register (Offset = 1C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1485. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C00h**

Figure 14-494. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1487. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.495 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0 Register (Offset = 1C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1488. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C04h**

Figure 14-495. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1490. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1490. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.496 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1 Register (Offset = 1C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1491. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C08h**

Figure 14-496. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1493. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1493. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.497 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2 Register (Offset = 1C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1494. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1C0Ch**

Figure 14-497. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1496. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1496. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.498 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_L Register (Offset = 1C10h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1497. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C10h**

Figure 14-498. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1499. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.499 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_H Register (Offset = 1C14h) [reset = 4h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1500. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C14h**

Figure 14-499. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
4h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
4h							

Table 14-1502. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	4h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.500 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_L Register (Offset = 1C18h) [reset = FFFFFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1503. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C18h**

Figure 14-500. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
FFFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
FFFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
FFFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1505. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	FFFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.501 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_H Register (Offset = 1C1Ch) [reset = 4h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 0 firewall.

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Table 14-1506. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C1Ch**

Figure 14-501. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
4h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
4h							

Table 14-1508. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	4h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.502 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_CONTROL Register (Offset = 1C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1509. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C20h**

Figure 14-502. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1511. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.503 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0 Register (Offset = 1C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1512. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C24h**

Figure 14-503. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1514. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1514. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.504 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1 Register (Offset = 1C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1515. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C28h**

Figure 14-504. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1517. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1517. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.505 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2 Register (Offset = 1C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1518. Instance Table

Instance Name	Physical Address
CBASS0	4500 1C2Ch

Figure 14-505. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1520. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1520. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.506 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_L Register (Offset = 1C30h) [reset = 60000000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1521. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C30h**

Figure 14-506. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
60000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
60000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
60000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1523. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	60000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.507 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_H Register (Offset = 1C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1524. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C34h**

Figure 14-507. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1526. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.508 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_L Register (Offset = 1C38h) [reset = 67FFFFFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1527. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C38h**

Figure 14-508. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
67FFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
67FFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
67FFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1529. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	67FFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.509 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_H Register (Offset = 1C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 1 firewall.

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Table 14-1530. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C3Ch**

Figure 14-509. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1532. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.510 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_CONTROL Register (Offset = 1C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1533. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C40h**

Figure 14-510. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1535. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.511 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0 Register (Offset = 1C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1536. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C44h**

Figure 14-511. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1538. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1538. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.512 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1 Register (Offset = 1C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1539. Instance Table

Instance Name	Physical Address
CBASS0	4500 1C48h

Figure 14-512. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1541. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1541. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.513 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2 Register (Offset = 1C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1542. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C4Ch**

Figure 14-513. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1544. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1544. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.514 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_L Register (Offset = 1C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1545. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C50h**

Figure 14-514. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1547. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.515 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_H Register (Offset = 1C54h) [reset = 5h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1548. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C54h**

Figure 14-515. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
5h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
5h							

Table 14-1550. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	5h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.516 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_L Register (Offset = 1C58h) [reset = FFFFFFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1551. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C58h**

Figure 14-516. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">FFFFFh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1553. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	FFFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.517 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_H Register (Offset = 1C5Ch) [reset = 5h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 2 firewall.

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Table 14-1554. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C5Ch**

Figure 14-517. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
5h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
5h							

Table 14-1556. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	5h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.518 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_CONTROL Register (Offset = 1C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1557. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C60h**

Figure 14-518. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1559. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.519 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0 Register (Offset = 1C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1560. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C64h**

Figure 14-519. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1562. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1562. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.520 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1 Register (Offset = 1C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1563. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C68h**

Figure 14-520. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1565. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1565. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.521 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2 Register (Offset = 1C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1566. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C6Ch**

Figure 14-521. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1568. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1568. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.522 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_L Register (Offset = 1C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1569. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C70h**

Figure 14-522. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1571. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.523 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_H Register (Offset = 1C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1572. Instance Table

Instance Name	Physical Address
CBASS0	4500 1C74h

Figure 14-523. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1574. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.524 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_L Register (Offset = 1C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1575. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C78h**

Figure 14-524. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1577. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.525 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_H Register (Offset = 1C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 3 firewall.

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Table 14-1578. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C7Ch**

Figure 14-525. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1580. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.526 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_CONTROL Register (Offset = 1C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1581. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C80h**

Figure 14-526. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1583. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.527 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0 Register (Offset = 1C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1584. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C84h**

Figure 14-527. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1586. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1586. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.528 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1 Register (Offset = 1C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1587. Instance Table

Instance Name	Physical Address
CBASS0	4500 1C88h

Figure 14-528. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1589. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1589. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.529 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2 Register (Offset = 1C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1590. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C8Ch**

Figure 14-529. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1592. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1592. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.530 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_L Register (Offset = 1C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1593. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C90h**

Figure 14-530. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1595. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.531 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_H Register (Offset = 1C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1596. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C94h**

Figure 14-531. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1598. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.532 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_L Register (Offset = 1C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1599. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C98h**

Figure 14-532. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1601. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.533 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_H Register (Offset = 1C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 4 firewall.

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Table 14-1602. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1C9Ch**

Figure 14-533. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1604. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.534 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_CONTROL Register (Offset = 1CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1605. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1CA0h**

Figure 14-534. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1607. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.535 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0 Register (Offset = 1CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1608. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CA4h**

Figure 14-535. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1610. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1610. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.536 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1 Register (Offset = 1CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1611. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CA8h**

Figure 14-536. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1613. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1613. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.537 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2 Register (Offset = 1CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1614. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CACh**

Figure 14-537. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1616. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1616. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.538 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_L Register (Offset = 1CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1617. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CB0h**

Figure 14-538. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1619. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.539 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_H Register (Offset = 1CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1620. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CB4h**

Figure 14-539. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1622. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.540 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_L Register (Offset = 1CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1623. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CB8h**

Figure 14-540. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1625. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.541 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_H Register (Offset = 1CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 5 firewall.

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Table 14-1626. Instance Table

Instance Name	Physical Address
CBASS0	4500 1CBCh

Figure 14-541. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1628. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.542 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_CONTROL Register (Offset = 1CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1629. Instance Table

Instance Name	Physical Address
CBASS0	4500 1CC0h

Figure 14-542. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1631. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.543 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0 Register (Offset = 1CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1632. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CC4h**

Figure 14-543. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1634. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1634. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.544 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1 Register (Offset = 1CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1635. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CC8h**

Figure 14-544. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1637. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1637. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.545 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2 Register (Offset = 1CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1638. Instance Table

Instance Name	Physical Address
CBASS0	4500 1CCCh

Figure 14-545. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1640. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1640. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.546 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_L Register (Offset = 1CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1641. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CD0h**

Figure 14-546. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1643. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.547 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_H Register (Offset = 1CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1644. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CD4h**

Figure 14-547. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1646. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.548 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_L Register (Offset = 1CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1647. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CD8h**

Figure 14-548. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1649. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.549 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_H Register (Offset = 1CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 6 firewall.

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Table 14-1650. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CDCh**

Figure 14-549. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1652. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.550 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_CONTROL Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_CONTROL Register (Offset = 1CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1653. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CE0h**

Figure 14-550. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1655. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.551 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0 Register (Offset = 1CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1656. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CE4h**

Figure 14-551. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1658. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1658. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.552 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1 Register (Offset = 1CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1659. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CE8h**

Figure 14-552. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1661. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1661. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.553 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2 Register (Offset = 1CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1662. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CECh**

Figure 14-553. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1664. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1664. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.554 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_L Register (Offset = 1CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1665. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CF0h**

Figure 14-554. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1667. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.555 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_H Register (Offset = 1CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1668. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1CF4h**

Figure 14-555. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1670. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.556 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_L Register (Offset = 1CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1671. Instance Table

Instance Name	Physical Address
CBASS0	**4500 1CF8h**

Figure 14-556. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1673. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.557 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_H Register (Offset = 1CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Ifss_ul_main_0.fss_s0 region 7 firewall.

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Table 14-1674. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 1CFCh**

Figure 14-557. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1676. CBASS_FW_IFSS_UL_MAIN_0_FSS_S0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.558 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = 2000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1677. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2000h**

Figure 14-558. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1679. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1679. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.559 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 2004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1680. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2004h**

Figure 14-559. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1682. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1682. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.560
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 2008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1683. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2008h**

Figure 14-560. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1685. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1685. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.561 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 200Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1686. Instance Table

Instance Name	Physical Address
CBASS0	**4500 200Ch**

Figure 14-561. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1688. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1688. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.562 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1689. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2010h**

Figure 14-562. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1691. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.563 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1692. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2014h**

Figure 14-563. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1694. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.564
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1695. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2018h**

Figure 14-564. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1697. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.565 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 0 firewall.

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Table 14-1698. Instance Table

Instance Name	Physical Address
CBASS0	**4500 201Ch**

Figure 14-565. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1700. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.566 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = 2020h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1701. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2020h**

Figure 14-566. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1703. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1703. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.567 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 2024h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1704. Instance Table

Instance Name	Physical Address
CBASS0	4500 2024h

Figure 14-567. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1706. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1706. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.568 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 2028h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1707. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2028h**

Figure 14-568. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1709. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1709. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.569 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 202Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1710. Instance Table

Instance Name	Physical Address
CBASS0	**4500 202Ch**

Figure 14-569. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1712. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1712. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.570 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 2030h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1713. Instance Table

Instance Name	Physical Address
CBASS0	4500 2030h

Figure 14-570. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1715. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.571 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 2034h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1716. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2034h**

Figure 14-571. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1718. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.572 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 2038h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1719. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2038h**

Figure 14-572. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1721. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.573
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 203Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 1 firewall.

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Table 14-1722. Instance Table

Instance Name	Physical Address
CBASS0	**4500 203Ch**

Figure 14-573. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1724. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.574 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = 2040h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1725. Instance Table

Instance Name	Physical Address
CBASS0	4500 2040h

Figure 14-574. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1727. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1727. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.575 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 2044h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1728. Instance Table

Instance Name	Physical Address
CBASS0	4500 2044h

Figure 14-575. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1730. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1730. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.576 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 2048h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1731. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2048h**

Figure 14-576. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1733. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1733. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.577 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 204Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1734. Instance Table

Instance Name	Physical Address
CBASS0	**4500 204Ch**

Figure 14-577. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1736. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1736. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.578 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 2050h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1737. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2050h**

Figure 14-578. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1739. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.579
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 2054h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1740. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2054h**

Figure 14-579. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1742. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.580
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 2058h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1743. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2058h**

Figure 14-580. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1745. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.581 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 205Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 2 firewall.

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Table 14-1746. Instance Table

Instance Name	Physical Address
CBASS0	**4500 205Ch**

Figure 14-581. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1748. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.582 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = 2060h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-1749. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2060h**

Figure 14-582. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1751. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1751. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.583 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 2064h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1752. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2064h**

Figure 14-583. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1754. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1754. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.584 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 2068h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1755. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2068h**

Figure 14-584. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1757. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1757. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.585 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 206Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1758. Instance Table

Instance Name	Physical Address
CBASS0	4500 206Ch

Figure 14-585. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1760. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1760. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.586 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 2070h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1761. Instance Table

Instance Name	Physical Address
CBASS0	4500 2070h

Figure 14-586. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1763. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.587 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 2074h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-1764. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2074h**

Figure 14-587. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1766. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.588 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 2078h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1767. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2078h**

Figure 14-588. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1769. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.589 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 207Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 3 firewall.

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Table 14-1770. Instance Table

Instance Name	Physical Address
CBASS0	**4500 207Ch**

Figure 14-589. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1772. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.590 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = 2080h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1773. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2080h**

Figure 14-590. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1775. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1775. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.591 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 2084h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1776. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2084h**

Figure 14-591. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1778. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1778. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.592 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 2088h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1779. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2088h**

Figure 14-592. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1781. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1781. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.593 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 208Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1782. Instance Table

Instance Name	Physical Address
CBASS0	**4500 208Ch**

Figure 14-593. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1784. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1784. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.594 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 2090h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1785. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2090h**

Figure 14-594. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1787. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.595 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 2094h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1788. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2094h**

Figure 14-595. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1790. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.596 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 2098h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1791. Instance Table

Instance Name	Physical Address
CBASS0	4500 2098h

Figure 14-596. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1793. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.597 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 209Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 4 firewall.

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Table 14-1794. Instance Table

Instance Name	Physical Address
CBASS0	**4500 209Ch**

Figure 14-597. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1796. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.598 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = 20A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1797. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20A0h**

Figure 14-598. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1799. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1799. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.599 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 20A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1800. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20A4h**

Figure 14-599. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1802. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1802. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.600 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 20A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1803. Instance Table

Instance Name	Physical Address
CBASS0	4500 20A8h

Figure 14-600. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1805. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1805. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.601 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 20ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1806. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20ACh**

Figure 14-601. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1808. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1808. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.602 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 20B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1809. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20B0h**

Figure 14-602. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1811. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.603 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 20B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1812. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20B4h**

Figure 14-603. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1814. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.604
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 20B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1815. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20B8h**

Figure 14-604. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1817. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.605 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 20BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 5 firewall.

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Table 14-1818. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20BCh**

Figure 14-605. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1820. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.606 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = 20C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1821. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20C0h**

Figure 14-606. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1823. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1823. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.607 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 20C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1824. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20C4h**

Figure 14-607. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1826. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1826. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.608 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 20C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1827. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20C8h**

Figure 14-608. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1829. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1829. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.609 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 20CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1830. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20CCh**

Figure 14-609. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1832. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1832. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.610 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 20D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1833. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20D0h**

Figure 14-610. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1835. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.611
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 20D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1836. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20D4h**

Figure 14-611. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1838. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.612 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 20D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1839. Instance Table

Instance Name	Physical Address
CBASS0	4500 20D8h

Figure 14-612. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1841. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.613 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 20DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 6 firewall.

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Table 14-1842. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20DCh**

Figure 14-613. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1844. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.614 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = 20E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1845. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20E0h**

Figure 14-614. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1847. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1847. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.615 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 20E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1848. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20E4h**

Figure 14-615. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1850. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1850. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.616 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 20E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1851. Instance Table

Instance Name	Physical Address
CBASS0	4500 20E8h

Figure 14-616. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1853. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1853. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.617 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 20ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1854. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20ECh**

Figure 14-617. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1856. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1856. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.618 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 20F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1857. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20F0h**

Figure 14-618. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1859. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.619 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 20F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1860. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20F4h**

Figure 14-619. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1862. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.620 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 20F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1863. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20F8h**

Figure 14-620. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1865. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.621 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 20FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 7 firewall.

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Table 14-1866. Instance Table

Instance Name	Physical Address
CBASS0	**4500 20FCh**

Figure 14-621. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1868. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.622 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL Register (Offset = 2100h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1869. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2100h**

Figure 14-622. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1871. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1871. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.623
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 2104h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1872. Instance Table

Instance Name	Physical Address
CBASS0	4500 2104h

Figure 14-623. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1874. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1874. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.624
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 2108h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1875. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2108h**

Figure 14-624. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1877. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1877. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.625 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 210Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1878. Instance Table

Instance Name	Physical Address
CBASS0	**4500 210Ch**

Figure 14-625. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1880. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1880. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.626 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 2110h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1881. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2110h**

Figure 14-626. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1883. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.627 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 2114h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1884. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2114h**

Figure 14-627. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1886. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.628 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 2118h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1887. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2118h**

Figure 14-628. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1889. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.629

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 211Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 8 firewall.

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Table 14-1890. Instance Table

Instance Name	Physical Address
CBASS0	**4500 211Ch**

Figure 14-629. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1892. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.630 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL Register (Offset = 2120h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1893. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2120h**

Figure 14-630. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1895. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1895. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.631 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 2124h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1896. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2124h**

Figure 14-631. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1898. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1898. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.632 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 2128h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1899. Instance Table

Instance Name	Physical Address
CBASS0	4500 2128h

Figure 14-632. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1901. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1901. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.633
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 212Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1902. Instance Table

Instance Name	Physical Address
CBASS0	**4500 212Ch**

Figure 14-633. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1904. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1904. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.634 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 2130h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1905. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2130h**

Figure 14-634. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1907. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.635 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 2134h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

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Table 14-1908. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2134h**

Figure 14-635. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1910. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.636 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 2138h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

Return to Summary Table

Table 14-1911. Instance Table

Instance Name	Physical Address
CBASS0	4500 2138h

Figure 14-636. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1913. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.637 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 213Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 9 firewall.

Return to Summary Table

Table 14-1914. Instance Table

Instance Name	Physical Address
CBASS0	4500 213Ch

Figure 14-637. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1916. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.638 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL Register (Offset = 2140h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-1917. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2140h**

Figure 14-638. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1919. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1919. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.639 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 2144h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

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Table 14-1920. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2144h**

Figure 14-639. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1922. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1922. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.640
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 2148h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-1923. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2148h**

Figure 14-640. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1925. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1925. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.641 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 214Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

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Table 14-1926. Instance Table

Instance Name	Physical Address
CBASS0	4500 214Ch

Figure 14-641. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1928. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1928. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.642 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 2150h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-1929. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2150h**

Figure 14-642. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1931. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.643 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 2154h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

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Table 14-1932. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2154h**

Figure 14-643. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1934. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.644
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 2158h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

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Table 14-1935. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2158h**

Figure 14-644. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1937. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.645 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 215Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 10 firewall.

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Table 14-1938. Instance Table

Instance Name	Physical Address
CBASS0	**4500 215Ch**

Figure 14-645. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1940. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.646 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL Register (Offset = 2160h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-1941. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2160h**

Figure 14-646. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1943. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1943. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.647 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 2164h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

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Table 14-1944. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2164h**

Figure 14-647. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1946. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1946. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.648 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 2168h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-1947. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2168h**

Figure 14-648. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1949. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1949. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.649 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 216Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

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Table 14-1950. Instance Table

Instance Name	Physical Address
CBASS0	4500 216Ch

Figure 14-649. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1952. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1952. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.650 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 2170h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-1953. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2170h**

Figure 14-650. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1955. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.651
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 2174h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

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Table 14-1956. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2174h**

Figure 14-651. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1958. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.652 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 2178h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

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Table 14-1959. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2178h**

Figure 14-652. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1961. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.653 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 217Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 11 firewall.

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Table 14-1962. Instance Table

Instance Name	Physical Address
CBASS0	**4500 217Ch**

Figure 14-653. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1964. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.654 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL Register (Offset = 2180h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1965. Instance Table

Instance Name	Physical Address
CBASS0	4500 2180h

Figure 14-654. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1967. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1967. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.655
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 2184h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1968. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2184h**

Figure 14-655. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1970. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1970. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.656
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 2188h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1971. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2188h**

Figure 14-656. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1973. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1973. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.657 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 218Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1974. Instance Table

Instance Name	Physical Address
CBASS0	4500 218Ch

Figure 14-657. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1976. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1976. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.658 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 2190h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1977. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2190h**

Figure 14-658. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1979. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.659 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 2194h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1980. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2194h**

Figure 14-659. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1982. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.660 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 2198h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1983. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2198h**

Figure 14-660. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1985. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.661 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 219Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 12 firewall.

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Table 14-1986. Instance Table

Instance Name	Physical Address
CBASS0	**4500 219Ch**

Figure 14-661. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1988. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.662 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL Register (Offset = 21A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-1989. Instance Table

Instance Name	Physical Address
CBASS0	4500 21A0h

Figure 14-662. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1991. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1991. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.663 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 21A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-1992. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21A4h**

Figure 14-663. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1994. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1994. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.664 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 21A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-1995. Instance Table

Instance Name	Physical Address
CBASS0	4500 21A8h

Figure 14-664. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1997. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1997. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.665 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 21ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-1998. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21ACh**

Figure 14-665. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2000. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2000. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.666 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 21B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-2001. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21B0h**

Figure 14-666. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2003. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.667 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 21B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-2004. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21B4h**

Figure 14-667. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-2006. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.668 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 21B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-2007. Instance Table

Instance Name	Physical Address
CBASS0	4500 21B8h

Figure 14-668. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2009. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.669

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 21BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 13 firewall.

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Table 14-2010. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21BCh**

Figure 14-669. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2012. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.670 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL Register (Offset = 21C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2013. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21C0h**

Figure 14-670. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2015. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2015. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.671 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 21C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2016. Instance Table

Instance Name	Physical Address
CBASS0	4500 21C4h

Figure 14-671. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2018. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2018. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.672 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 21C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2019. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21C8h**

Figure 14-672. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2021. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2021. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.673 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 21CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2022. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21CCh**

Figure 14-673. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2024. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2024. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.674 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 21D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2025. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21D0h**

Figure 14-674. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2027. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.675 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 21D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2028. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21D4h**

Figure 14-675. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2030. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.676 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 21D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2031. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21D8h**

Figure 14-676. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2033. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.677 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 21DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 14 firewall.

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Table 14-2034. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21DCh**

Figure 14-677. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2036. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.678 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL Register (Offset = 21E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2037. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21E0h**

Figure 14-678. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2039. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2039. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.679 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 21E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2040. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21E4h**

Figure 14-679. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2042. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2042. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.680 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 21E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2043. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21E8h**

Figure 14-680. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2045. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2045. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.681 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 21ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2046. Instance Table

Instance Name	Physical Address
CBASS0	4500 21ECh

Figure 14-681. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2048. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2048. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.682 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 21F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2049. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21F0h**

Figure 14-682. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2051. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.683 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 21F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2052. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21F4h**

Figure 14-683. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2054. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.684 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 21F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2055. Instance Table

Instance Name	Physical Address
CBASS0	4500 21F8h

Figure 14-684. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2057. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.685 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 21FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_misc_peri_cbass_data_l0.slv region 15 firewall.

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Table 14-2058. Instance Table

Instance Name	Physical Address
CBASS0	**4500 21FCh**

Figure 14-685. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2060. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MISC_PERI_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.686 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL Register (Offset = 2400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2061. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2400h**

Figure 14-686. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2063. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2063. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.687 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 2404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2064. Instance Table

Instance Name	Physical Address
CBASS0	4500 2404h

Figure 14-687. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2066. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2066. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.688 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 2408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2067. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2408h**

Figure 14-688. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2069. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2069. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.689 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 240Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2070. Instance Table

Instance Name	Physical Address
CBASS0	**4500 240Ch**

Figure 14-689. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2072. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2072. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.690 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2073. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2410h**

Figure 14-690. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2075. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

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CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2076. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2414h**

Figure 14-691. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2078. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.692 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2079. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2418h**

Figure 14-692. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2081. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.693 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 0 firewall.

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Table 14-2082. Instance Table

Instance Name	Physical Address
CBASS0	**4500 241Ch**

Figure 14-693. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2084. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.694 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL Register (Offset = 2420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2085. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2420h**

Figure 14-694. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2087. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2087. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.695 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 2424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2088. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2424h**

Figure 14-695. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2090. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2090. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.696 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 2428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2091. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2428h**

Figure 14-696. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2093. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2093. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.697 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 242Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2094. Instance Table

Instance Name	Physical Address
CBASS0	**4500 242Ch**

Figure 14-697. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2096. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2096. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.698
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 2430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2097. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2430h**

Figure 14-698. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2099. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.699 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 2434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2100. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2434h**

Figure 14-699. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2102. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.700 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 2438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2103. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2438h**

Figure 14-700. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2105. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.701 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 243Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 1 firewall.

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Table 14-2106. Instance Table

Instance Name	Physical Address
CBASS0	**4500 243Ch**

Figure 14-701. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2108. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.702 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL Register (Offset = 2440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2109. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2440h**

Figure 14-702. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2111. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2111. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.703 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 2444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2112. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2444h**

Figure 14-703. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2114. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2114. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.704 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 2448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2115. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2448h**

Figure 14-704. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2117. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2117. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.705 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 244Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2118. Instance Table

Instance Name	Physical Address
CBASS0	**4500 244Ch**

Figure 14-705. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2120. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2120. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.706 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 2450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2121. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2450h**

Figure 14-706. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2123. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.707 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 2454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2124. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2454h**

Figure 14-707. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2126. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.708 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 2458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2127. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2458h**

Figure 14-708. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2129. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.709 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 245Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 2 firewall.

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Table 14-2130. Instance Table

Instance Name	Physical Address
CBASS0	**4500 245Ch**

Figure 14-709. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2132. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.710 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL Register (Offset = 2460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2133. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2460h**

Figure 14-710. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2135. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2135. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.711 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 2464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2136. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2464h**

Figure 14-711. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2138. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2138. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.712 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 2468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2139. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2468h**

Figure 14-712. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2141. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2141. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.713 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 246Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2142. Instance Table

Instance Name	Physical Address
CBASS0	4500 246Ch

Figure 14-713. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2144. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2144. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.714 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 2470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2145. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2470h**

Figure 14-714. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2147. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.715 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 2474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2148. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2474h**

Figure 14-715. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2150. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.716 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 2478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2151. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2478h**

Figure 14-716. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2153. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.717 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 247Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 3 firewall.

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Table 14-2154. Instance Table

Instance Name	Physical Address
CBASS0	**4500 247Ch**

Figure 14-717. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2156. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.718 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL Register (Offset = 2480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2157. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2480h**

Figure 14-718. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2159. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2159. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.719 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 2484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2160. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2484h**

Figure 14-719. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2162. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2162. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.720 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 2488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2163. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2488h**

Figure 14-720. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2165. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2165. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.721 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 248Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2166. Instance Table

Instance Name	Physical Address
CBASS0	**4500 248Ch**

Figure 14-721. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2168. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2168. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.722 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 2490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2169. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2490h**

Figure 14-722. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2171. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.723 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 2494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2172. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2494h**

Figure 14-723. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2174. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.724 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 2498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2175. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2498h**

Figure 14-724. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2177. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.725 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 249Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 4 firewall.

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Table 14-2178. Instance Table

Instance Name	Physical Address
CBASS0	**4500 249Ch**

Figure 14-725. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2180. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.726 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL Register (Offset = 24A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2181. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24A0h**

Figure 14-726. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2183. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2183. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.727 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 24A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2184. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24A4h**

Figure 14-727. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2186. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2186. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.728 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 24A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2187. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24A8h**

Figure 14-728. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2189. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2189. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.729 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 24ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2190. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24ACh**

Figure 14-729. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2192. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2192. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.730 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 24B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2193. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24B0h**

Figure 14-730. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2195. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.731 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 24B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2196. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24B4h**

Figure 14-731. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2198. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.732 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 24B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2199. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24B8h**

Figure 14-732. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2201. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.733 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 24BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 5 firewall.

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Table 14-2202. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24BCh**

Figure 14-733. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2204. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.734 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL Register (Offset = 24C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2205. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24C0h**

Figure 14-734. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2207. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2207. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.735 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 24C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2208. Instance Table

Instance Name	Physical Address
CBASS0	4500 24C4h

Figure 14-735. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2210. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2210. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.736 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 24C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2211. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 24C8h**

Figure 14-736. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2213. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2213. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.737 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 24CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2214. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24CCh**

Figure 14-737. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2216. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2216. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.738 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 24D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2217. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24D0h**

Figure 14-738. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2219. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.739 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 24D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2220. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24D4h**

Figure 14-739. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2222. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.740 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 24D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2223. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24D8h**

Figure 14-740. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2225. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.741 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 24DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 6 firewall.

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Table 14-2226. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24DCh**

Figure 14-741. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2228. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.742 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL Register (Offset = 24E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2229. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24E0h**

Figure 14-742. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2231. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2231. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.743 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 24E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2232. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24E4h**

Figure 14-743. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2234. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2234. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.744 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 24E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2235. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24E8h**

Figure 14-744. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2237. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2237. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.745 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 24ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2238. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24ECh**

Figure 14-745. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2240. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2240. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.746
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 24F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2241. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24F0h**

Figure 14-746. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2243. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.747 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 24F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2244. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24F4h**

Figure 14-747. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2246. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.748 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 24F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2247. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24F8h**

Figure 14-748. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2249. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.749 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 24FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 7 firewall.

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Table 14-2250. Instance Table

Instance Name	Physical Address
CBASS0	**4500 24FCh**

Figure 14-749. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2252. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.750 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL Register (Offset = 2500h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2253. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2500h**

Figure 14-750. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2255. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2255. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.751 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 2504h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2256. Instance Table

Instance Name	Physical Address
CBASS0	4500 2504h

Figure 14-751. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2258. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2258. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.752 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 2508h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2259. Instance Table

Instance Name	Physical Address
CBASS0	4500 2508h

Figure 14-752. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2261. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2261. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.753 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 250Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2262. Instance Table

Instance Name	Physical Address
CBASS0	**4500 250Ch**

Figure 14-753. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2264. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2264. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.754 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 2510h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2265. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2510h**

Figure 14-754. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2267. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.755 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 2514h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2268. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2514h**

Figure 14-755. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2270. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.756 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 2518h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2271. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2518h**

Figure 14-756. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2273. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.757 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 251Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 8 firewall.

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Table 14-2274. Instance Table

Instance Name	Physical Address
CBASS0	**4500 251Ch**

Figure 14-757. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2276. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.758 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL Register (Offset = 2520h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2277. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2520h**

Figure 14-758. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2279. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2279. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.759 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 2524h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2280. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2524h**

Figure 14-759. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2282. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2282. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.760 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 2528h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2283. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2528h**

Figure 14-760. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2285. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2285. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.761 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 252Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2286. Instance Table

Instance Name	Physical Address
CBASS0	**4500 252Ch**

Figure 14-761. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2288. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2288. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.762 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 2530h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2289. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2530h**

Figure 14-762. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2291. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.763 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 2534h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2292. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2534h**

Figure 14-763. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2294. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.764 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 2538h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2295. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2538h**

Figure 14-764. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2297. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.765 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 253Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 9 firewall.

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Table 14-2298. Instance Table

Instance Name	Physical Address
CBASS0	**4500 253Ch**

Figure 14-765. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2300. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.766 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL Register (Offset = 2540h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2301. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2540h**

Figure 14-766. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2303. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2303. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.767 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 2544h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2304. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2544h**

Figure 14-767. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2306. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2306. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.768 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 2548h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2307. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2548h**

Figure 14-768. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2309. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2309. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.769 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 254Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2310. Instance Table

Instance Name	Physical Address
CBASS0	**4500 254Ch**

Figure 14-769. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2312. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2312. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.770 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 2550h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2313. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2550h**

Figure 14-770. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2315. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.771 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 2554h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2316. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2554h**

Figure 14-771. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2318. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.772 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 2558h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2319. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2558h**

Figure 14-772. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2321. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.773 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 255Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 10 firewall.

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Table 14-2322. Instance Table

Instance Name	Physical Address
CBASS0	**4500 255Ch**

Figure 14-773. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2324. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.774 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL Register (Offset = 2560h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2325. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2560h**

Figure 14-774. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2327. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2327. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.775 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 2564h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2328. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2564h**

Figure 14-775. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2330. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2330. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.776 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 2568h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2331. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2568h**

Figure 14-776. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2333. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2333. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.777 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 256Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2334. Instance Table

Instance Name	Physical Address
CBASS0	**4500 256Ch**

Figure 14-777. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2336. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2336. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.778 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 2570h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2337. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2570h**

Figure 14-778. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2339. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.779
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 2574h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2340. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2574h**

Figure 14-779. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2342. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.780 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 2578h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2343. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2578h**

Figure 14-780. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2345. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.781 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 257Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 11 firewall.

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Table 14-2346. Instance Table

Instance Name	Physical Address
CBASS0	**4500 257Ch**

Figure 14-781. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2348. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.782 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL Register (Offset = 2580h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2349. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2580h**

Figure 14-782. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2351. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2351. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.783 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 2584h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2352. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2584h**

Figure 14-783. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2354. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2354. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.784 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 2588h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2355. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2588h**

Figure 14-784. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2357. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2357. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.785 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 258Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2358. Instance Table

Instance Name	Physical Address
CBASS0	**4500 258Ch**

Figure 14-785. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2360. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2360. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.786 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 2590h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2361. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2590h**

Figure 14-786. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2363. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.787
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 2594h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2364. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2594h**

Figure 14-787. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2366. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.788 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 2598h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2367. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2598h**

Figure 14-788. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2369. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.789 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 259Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 12 firewall.

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Table 14-2370. Instance Table

Instance Name	Physical Address
CBASS0	**4500 259Ch**

Figure 14-789. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2372. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.790 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL Register (Offset = 25A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2373. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25A0h**

Figure 14-790. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2375. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2375. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.791 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 25A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2376. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25A4h**

Figure 14-791. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2378. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2378. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.792 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 25A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2379. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25A8h**

Figure 14-792. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2381. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2381. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.793 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 25ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2382. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25ACh**

Figure 14-793. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2384. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2384. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.794
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 25B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2385. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25B0h**

Figure 14-794. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2387. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.795

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 25B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2388. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25B4h**

Figure 14-795. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2390. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.796
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 25B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2391. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25B8h**

Figure 14-796. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2393. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.797 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 25BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 13 firewall.

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Table 14-2394. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25BCh**

Figure 14-797. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2396. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.798 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL Register (Offset = 25C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2397. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25C0h**

Figure 14-798. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2399. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2399. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.799 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 25C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2400. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25C4h**

Figure 14-799. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2402. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2402. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.800 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 25C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2403. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25C8h**

Figure 14-800. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2405. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2405. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.801 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 25CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2406. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25CCh**

Figure 14-801. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2408. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2408. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.802 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 25D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2409. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25D0h**

Figure 14-802. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2411. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.803 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 25D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2412. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25D4h**

Figure 14-803. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2414. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.804 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 25D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2415. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25D8h**

Figure 14-804. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2417. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.805
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 25DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 14 firewall.

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Table 14-2418. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25DCh**

Figure 14-805. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2420. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.806 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL Register (Offset = 25E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2421. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25E0h**

Figure 14-806. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2423. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2423. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.807 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 25E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2424. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25E4h**

Figure 14-807. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2426. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2426. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.808 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 25E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2427. Instance Table

Instance Name	Physical Address
CBASS0	4500 25E8h

Figure 14-808. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2429. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2429. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.809 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 25ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2430. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25ECh**

Figure 14-809. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2432. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2432. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.810
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 25F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2433. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25F0h**

Figure 14-810. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2435. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.811 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 25F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2436. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25F4h**

Figure 14-811. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2438. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.812 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 25F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2439. Instance Table

Instance Name	Physical Address
CBASS0	4500 25F8h

Figure 14-812. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2441. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.813 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 25FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 15 firewall.

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Table 14-2442. Instance Table

Instance Name	Physical Address
CBASS0	**4500 25FCh**

Figure 14-813. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2444. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.814 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL Register (Offset = 2600h) [reset = 0h]

The FW Region 16 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2445. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2600h**

Figure 14-814. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2447. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2447. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.815 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0 Register (Offset = 2604h) [reset = 0h]

The FW Region 16 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2448. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2604h**

Figure 14-815. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2450. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2450. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.816 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1 Register (Offset = 2608h) [reset = 0h]

The FW Region 16 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2451. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2608h**

Figure 14-816. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2453. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2453. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.817 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2 Register (Offset = 260Ch) [reset = 0h]

The FW Region 16 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2454. Instance Table

Instance Name	Physical Address
CBASS0	**4500 260Ch**

Figure 14-817. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2456. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2456. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.818
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_L Register (Offset = 2610h) [reset = 0h]

The FW Region 16 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2457. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2610h**

Figure 14-818. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2459. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.819 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_H Register (Offset = 2614h) [reset = 0h]

The FW Region 16 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2460. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2614h**

Figure 14-819. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2462. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.820 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_L Register (Offset = 2618h) [reset = FFFh]

The FW Region 16 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2463. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2618h**

Figure 14-820. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2465. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.821 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_H Register (Offset = 261Ch) [reset = 0h]

The FW Region 16 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 16 firewall.

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Table 14-2466. Instance Table

Instance Name	Physical Address
CBASS0	**4500 261Ch**

Figure 14-821. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2468. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_16_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.822 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL Register (Offset = 2620h) [reset = 0h]

The FW Region 17 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2469. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2620h**

Figure 14-822. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2471. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2471. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.823 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0 Register (Offset = 2624h) [reset = 0h]

The FW Region 17 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2472. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2624h**

Figure 14-823. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2474. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2474. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.824 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1 Register (Offset = 2628h) [reset = 0h]

The FW Region 17 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2475. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2628h**

Figure 14-824. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2477. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2477. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.825 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2 Register (Offset = 262Ch) [reset = 0h]

The FW Region 17 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2478. Instance Table

Instance Name	Physical Address
CBASS0	**4500 262Ch**

Figure 14-825. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2480. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2480. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.826
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_L Register (Offset = 2630h) [reset = 0h]

The FW Region 17 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2481. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2630h**

Figure 14-826. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2483. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.827
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_H Register (Offset = 2634h) [reset = 0h]

The FW Region 17 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2484. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2634h**

Figure 14-827. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2486. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.828 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_L Register (Offset = 2638h) [reset = FFFh]

The FW Region 17 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2487. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2638h**

Figure 14-828. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2489. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.829 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_H Register (Offset = 263Ch) [reset = 0h]

The FW Region 17 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 17 firewall.

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Table 14-2490. Instance Table

Instance Name	Physical Address
CBASS0	**4500 263Ch**

Figure 14-829. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2492. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_17_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.830 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL Register (Offset = 2640h) [reset = 0h]

The FW Region 18 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2493. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2640h**

Figure 14-830. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2495. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2495. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.831 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0 Register (Offset = 2644h) [reset = 0h]

The FW Region 18 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2496. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2644h**

Figure 14-831. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2498. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2498. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.832 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1 Register (Offset = 2648h) [reset = 0h]

The FW Region 18 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2499. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2648h**

Figure 14-832. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2501. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2501. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.833 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2 Register (Offset = 264Ch) [reset = 0h]

The FW Region 18 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2502. Instance Table

Instance Name	Physical Address
CBASS0	**4500 264Ch**

Figure 14-833. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2504. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2504. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.834 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_L Register (Offset = 2650h) [reset = 0h]

The FW Region 18 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2505. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2650h**

Figure 14-834. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2507. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.835 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_H Register (Offset = 2654h) [reset = 0h]

The FW Region 18 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2508. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2654h**

Figure 14-835. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2510. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.836 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_L Register (Offset = 2658h) [reset = FFFh]

The FW Region 18 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2511. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2658h**

Figure 14-836. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2513. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.837 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_H Register (Offset = 265Ch) [reset = 0h]

The FW Region 18 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 18 firewall.

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Table 14-2514. Instance Table

Instance Name	Physical Address
CBASS0	**4500 265Ch**

Figure 14-837. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2516. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_18_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.838 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL Register (Offset = 2660h) [reset = 0h]

The FW Region 19 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2517. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2660h**

Figure 14-838. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2519. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2519. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.839 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0 Register (Offset = 2664h) [reset = 0h]

The FW Region 19 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2520. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2664h**

Figure 14-839. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2522. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2522. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.840 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1 Register (Offset = 2668h) [reset = 0h]

The FW Region 19 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2523. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2668h**

Figure 14-840. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2525. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2525. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.841 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2 Register (Offset = 266Ch) [reset = 0h]

The FW Region 19 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2526. Instance Table

Instance Name	Physical Address
CBASS0	**4500 266Ch**

Figure 14-841. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2528. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2528. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.842 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_L Register (Offset = 2670h) [reset = 0h]

The FW Region 19 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2529. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2670h**

Figure 14-842. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2531. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.843 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_H Register (Offset = 2674h) [reset = 0h]

The FW Region 19 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2532. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2674h**

Figure 14-843. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2534. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.844 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_L Register (Offset = 2678h) [reset = FFFh]

The FW Region 19 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2535. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2678h**

Figure 14-844. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2537. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.845 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_H Register (Offset = 267Ch) [reset = 0h]

The FW Region 19 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 19 firewall.

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Table 14-2538. Instance Table

Instance Name	Physical Address
CBASS0	**4500 267Ch**

Figure 14-845. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2540. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_19_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.846 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL Register (Offset = 2680h) [reset = 0h]

The FW Region 20 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2541. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2680h**

Figure 14-846. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2543. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2543. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.847 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0 Register (Offset = 2684h) [reset = 0h]

The FW Region 20 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2544. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2684h**

Figure 14-847. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2546. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2546. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.848 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1 Register (Offset = 2688h) [reset = 0h]

The FW Region 20 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2547. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2688h**

Figure 14-848. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2549. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2549. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.849 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2 Register (Offset = 268Ch) [reset = 0h]

The FW Region 20 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2550. Instance Table

Instance Name	Physical Address
CBASS0	**4500 268Ch**

Figure 14-849. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2552. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2552. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.850
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_L Register (Offset = 2690h) [reset = 0h]

The FW Region 20 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2553. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2690h**

Figure 14-850. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2555. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.851 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_H Register (Offset = 2694h) [reset = 0h]

The FW Region 20 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2556. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2694h**

Figure 14-851. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2558. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.852

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_L Register (Offset = 2698h) [reset = FFFh]

The FW Region 20 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2559. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2698h**

Figure 14-852. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2561. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.853 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_H Register (Offset = 269Ch) [reset = 0h]

The FW Region 20 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 20 firewall.

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Table 14-2562. Instance Table

Instance Name	Physical Address
CBASS0	**4500 269Ch**

Figure 14-853. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2564. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_20_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.854 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL Register (Offset = 26A0h) [reset = 0h]

The FW Region 21 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2565. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26A0h**

Figure 14-854. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2567. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2567. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.855 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0 Register (Offset = 26A4h) [reset = 0h]

The FW Region 21 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2568. Instance Table

Instance Name	Physical Address
CBASS0	4500 26A4h

Figure 14-855. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2570. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2570. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.856 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1 Register (Offset = 26A8h) [reset = 0h]

The FW Region 21 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2571. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26A8h**

Figure 14-856. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2573. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2573. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.857 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2 Register (Offset = 26ACh) [reset = 0h]

The FW Region 21 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2574. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26ACh**

Figure 14-857. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2576. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2576. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.858 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_L Register (Offset = 26B0h) [reset = 0h]

The FW Region 21 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2577. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26B0h**

Figure 14-858. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2579. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.859 *CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_H Register*

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_H Register (Offset = 26B4h) [reset = 0h]

The FW Region 21 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2580. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26B4h**

Figure 14-859. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2582. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.860 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_L Register (Offset = 26B8h) [reset = FFFh]

The FW Region 21 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2583. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26B8h**

Figure 14-860. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2585. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.861
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_H Register (Offset = 26BCh) [reset = 0h]

The FW Region 21 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 21 firewall.

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Table 14-2586. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26BCh**

Figure 14-861. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2588. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_21_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.862 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL Register (Offset = 26C0h) [reset = 0h]

The FW Region 22 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2589. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26C0h**

Figure 14-862. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2591. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2591. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.863 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0 Register (Offset = 26C4h) [reset = 0h]

The FW Region 22 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2592. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26C4h**

Figure 14-863. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2594. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2594. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.864 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1 Register (Offset = 26C8h) [reset = 0h]

The FW Region 22 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2595. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26C8h**

Figure 14-864. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2597. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2597. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.865 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2 Register (Offset = 26CCh) [reset = 0h]

The FW Region 22 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2598. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26CCh**

Figure 14-865. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2600. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2600. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.866
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_L Register (Offset = 26D0h) [reset = 0h]

The FW Region 22 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2601. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26D0h**

Figure 14-866. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2603. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.867 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_H Register (Offset = 26D4h) [reset = 0h]

The FW Region 22 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2604. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26D4h**

Figure 14-867. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2606. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.868 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_L Register (Offset = 26D8h) [reset = FFFh]

The FW Region 22 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2607. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26D8h**

Figure 14-868. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2609. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.869 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_H Register (Offset = 26DCh) [reset = 0h]

The FW Region 22 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 22 firewall.

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Table 14-2610. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26DCh**

Figure 14-869. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-2612. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_22_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.870 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL Register (Offset = 26E0h) [reset = 0h]

The FW Region 23 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2613. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26E0h**

Figure 14-870. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2615. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2615. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.871 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0 Register (Offset = 26E4h) [reset = 0h]

The FW Region 23 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2616. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26E4h**

Figure 14-871. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2618. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2618. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.872 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1 Register (Offset = 26E8h) [reset = 0h]

The FW Region 23 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2619. Instance Table

Instance Name	Physical Address
CBASS0	4500 26E8h

Figure 14-872. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2621. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2621. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.873 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2 Register (Offset = 26ECh) [reset = 0h]

The FW Region 23 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2622. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26ECh**

Figure 14-873. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2624. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2624. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.874
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_L Register (Offset = 26F0h) [reset = 0h]

The FW Region 23 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2625. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26F0h**

Figure 14-874. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2627. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.875

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_H Register (Offset = 26F4h) [reset = 0h]

The FW Region 23 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2628. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26F4h**

Figure 14-875. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2630. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.876

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_L Register (Offset = 26F8h) [reset = FFFh]

The FW Region 23 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2631. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26F8h**

Figure 14-876. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2633. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.877 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_H Register (Offset = 26FCh) [reset = 0h]

The FW Region 23 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 23 firewall.

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Table 14-2634. Instance Table

Instance Name	Physical Address
CBASS0	**4500 26FCh**

Figure 14-877. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2636. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_23_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.878 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL Register (Offset = 2700h) [reset = 0h]

The FW Region 24 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2637. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2700h**

Figure 14-878. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2639. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2639. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.879 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0 Register (Offset = 2704h) [reset = 0h]

The FW Region 24 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2640. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2704h**

Figure 14-879. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2642. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2642. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.880 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1 Register (Offset = 2708h) [reset = 0h]

The FW Region 24 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2643. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2708h**

Figure 14-880. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2645. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2645. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.881 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2 Register (Offset = 270Ch) [reset = 0h]

The FW Region 24 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2646. Instance Table

Instance Name	Physical Address
CBASS0	**4500 270Ch**

Figure 14-881. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2648. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2648. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.882

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_L Register (Offset = 2710h) [reset = 0h]

The FW Region 24 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2649. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2710h**

Figure 14-882. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2651. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.883 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_H Register (Offset = 2714h) [reset = 0h]

The FW Region 24 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2652. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2714h**

Figure 14-883. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2654. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.884

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_L Register (Offset = 2718h) [reset = FFFh]

The FW Region 24 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2655. Instance Table

Instance Name	Physical Address
CBASS0	4500 2718h

Figure 14-884. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2657. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.885
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_H Register (Offset = 271Ch) [reset = 0h]

The FW Region 24 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 24 firewall.

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Table 14-2658. Instance Table

Instance Name	Physical Address
CBASS0	**4500 271Ch**

Figure 14-885. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2660. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_24_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.886 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL Register (Offset = 2720h) [reset = 0h]

The FW Region 25 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2661. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2720h**

Figure 14-886. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2663. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2663. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.887 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0 Register (Offset = 2724h) [reset = 0h]

The FW Region 25 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2664. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2724h**

Figure 14-887. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2666. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2666. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.888 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1 Register (Offset = 2728h) [reset = 0h]

The FW Region 25 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2667. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2728h**

Figure 14-888. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2669. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2669. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.889 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2 Register (Offset = 272Ch) [reset = 0h]

The FW Region 25 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2670. Instance Table

Instance Name	Physical Address
CBASS0	**4500 272Ch**

Figure 14-889. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2672. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2672. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.890 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_L Register (Offset = 2730h) [reset = 0h]

The FW Region 25 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2673. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2730h**

Figure 14-890. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2675. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.891 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_H Register (Offset = 2734h) [reset = 0h]

The FW Region 25 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2676. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2734h**

Figure 14-891. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2678. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.892 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_L Register (Offset = 2738h) [reset = FFFh]

The FW Region 25 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2679. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2738h**

Figure 14-892. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2681. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.893 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_H Register (Offset = 273Ch) [reset = 0h]

The FW Region 25 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 25 firewall.

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Table 14-2682. Instance Table

Instance Name	Physical Address
CBASS0	**4500 273Ch**

Figure 14-893. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2684. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_25_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.894 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL Register (Offset = 2740h) [reset = 0h]

The FW Region 26 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2685. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2740h**

Figure 14-894. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2687. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2687. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.895 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0 Register (Offset = 2744h) [reset = 0h]

The FW Region 26 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2688. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2744h**

Figure 14-895. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2690. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2690. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.896 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1 Register (Offset = 2748h) [reset = 0h]

The FW Region 26 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2691. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2748h**

Figure 14-896. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2693. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2693. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.897 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2 Register (Offset = 274Ch) [reset = 0h]

The FW Region 26 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2694. Instance Table

Instance Name	Physical Address
CBASS0	**4500 274Ch**

Figure 14-897. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2696. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2696. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.898
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_L Register (Offset = 2750h) [reset = 0h]

The FW Region 26 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2697. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2750h**

Figure 14-898. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2699. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.899 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_H Register (Offset = 2754h) [reset = 0h]

The FW Region 26 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2700. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2754h**

Figure 14-899. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2702. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.900

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_L Register (Offset = 2758h) [reset = FFFh]

The FW Region 26 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2703. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2758h**

Figure 14-900. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2705. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.901 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_H Register (Offset = 275Ch) [reset = 0h]

The FW Region 26 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 26 firewall.

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Table 14-2706. Instance Table

Instance Name	Physical Address
CBASS0	**4500 275Ch**

Figure 14-901. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2708. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_26_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.902 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL Register (Offset = 2760h) [reset = 0h]

The FW Region 27 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2709. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2760h**

Figure 14-902. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2711. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2711. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.903 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0 Register (Offset = 2764h) [reset = 0h]

The FW Region 27 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2712. Instance Table

Instance Name	Physical Address
CBASS0	4500 2764h

Figure 14-903. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2714. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2714. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.904 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1 Register (Offset = 2768h) [reset = 0h]

The FW Region 27 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2715. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2768h**

Figure 14-904. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2717. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2717. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.905 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2 Register (Offset = 276Ch) [reset = 0h]

The FW Region 27 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2718. Instance Table

Instance Name	Physical Address
CBASS0	**4500 276Ch**

Figure 14-905. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2720. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2720. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.906
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_L Register (Offset = 2770h) [reset = 0h]

The FW Region 27 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2721. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2770h**

Figure 14-906. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2723. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.907 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_H Register (Offset = 2774h) [reset = 0h]

The FW Region 27 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2724. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2774h**

Figure 14-907. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2726. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.908
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_L Register (Offset = 2778h) [reset = FFFh]

The FW Region 27 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2727. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2778h**

Figure 14-908. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2729. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.909 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_H Register (Offset = 277Ch) [reset = 0h]

The FW Region 27 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 27 firewall.

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Table 14-2730. Instance Table

Instance Name	Physical Address
CBASS0	**4500 277Ch**

Figure 14-909. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2732. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_27_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.910 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL Register (Offset = 2780h) [reset = 0h]

The FW Region 28 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2733. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2780h**

Figure 14-910. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2735. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2735. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.911 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0 Register (Offset = 2784h) [reset = 0h]

The FW Region 28 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2736. Instance Table

Instance Name	Physical Address
CBASS0	4500 2784h

Figure 14-911. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2738. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2738. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.912 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1 Register (Offset = 2788h) [reset = 0h]

The FW Region 28 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2739. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2788h**

Figure 14-912. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2741. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2741. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.913 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2 Register (Offset = 278Ch) [reset = 0h]

The FW Region 28 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2742. Instance Table

Instance Name	Physical Address
CBASS0	**4500 278Ch**

Figure 14-913. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2744. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2744. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.914 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_L Register (Offset = 2790h) [reset = 0h]

The FW Region 28 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2745. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2790h**

Figure 14-914. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2747. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.915 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_H Register (Offset = 2794h) [reset = 0h]

The FW Region 28 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2748. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2794h**

Figure 14-915. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2750. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.916 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_L Register (Offset = 2798h) [reset = FFFh]

The FW Region 28 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2751. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2798h**

Figure 14-916. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2753. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.917 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_H Register (Offset = 279Ch) [reset = 0h]

The FW Region 28 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 28 firewall.

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Table 14-2754. Instance Table

Instance Name	Physical Address
CBASS0	**4500 279Ch**

Figure 14-917. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2756. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_28_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.918 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL Register (Offset = 27A0h) [reset = 0h]

The FW Region 29 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2757. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27A0h**

Figure 14-918. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2759. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2759. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.919 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0 Register (Offset = 27A4h) [reset = 0h]

The FW Region 29 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2760. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27A4h**

Figure 14-919. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2762. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2762. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.920 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1 Register (Offset = 27A8h) [reset = 0h]

The FW Region 29 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2763. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27A8h**

Figure 14-920. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2765. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2765. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.921 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2 Register (Offset = 27ACh) [reset = 0h]

The FW Region 29 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2766. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27ACh**

Figure 14-921. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2768. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2768. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.922 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_L Register (Offset = 27B0h) [reset = 0h]

The FW Region 29 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2769. Instance Table

Instance Name	Physical Address
CBASS0	4500 27B0h

Figure 14-922. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2771. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.923 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_H Register (Offset = 27B4h) [reset = 0h]

The FW Region 29 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2772. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27B4h**

Figure 14-923. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2774. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.924 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_L Register (Offset = 27B8h) [reset = FFFh]

The FW Region 29 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2775. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27B8h**

Figure 14-924. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2777. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.925 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_H Register (Offset = 27BCh) [reset = 0h]

The FW Region 29 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 29 firewall.

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Table 14-2778. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27BCh**

Figure 14-925. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2780. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_29_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.926 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL Register (Offset = 27C0h) [reset = 0h]

The FW Region 30 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2781. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27C0h**

Figure 14-926. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2783. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2783. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.927 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0 Register (Offset = 27C4h) [reset = 0h]

The FW Region 30 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2784. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27C4h**

Figure 14-927. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2786. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2786. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.928 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1 Register (Offset = 27C8h) [reset = 0h]

The FW Region 30 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2787. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27C8h**

Figure 14-928. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2789. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2789. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.929 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2 Register (Offset = 27CCh) [reset = 0h]

The FW Region 30 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2790. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27CCh**

Figure 14-929. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2792. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2792. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.930 *CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_L Register*

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_L Register (Offset = 27D0h) [reset = 0h]

The FW Region 30 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2793. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27D0h**

Figure 14-930. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2795. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.931
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_H Register (Offset = 27D4h) [reset = 0h]

The FW Region 30 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2796. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27D4h**

Figure 14-931. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2798. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.932
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_L Register (Offset = 27D8h) [reset = FFFh]

The FW Region 30 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2799. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27D8h**

Figure 14-932. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2801. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.933 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_H Register (Offset = 27DCh) [reset = 0h]

The FW Region 30 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 30 firewall.

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Table 14-2802. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27DCh**

Figure 14-933. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2804. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_30_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.934 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL Register (Offset = 27E0h) [reset = 0h]

The FW Region 31 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2805. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27E0h**

Figure 14-934. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2807. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2807. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.935 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0 Register (Offset = 27E4h) [reset = 0h]

The FW Region 31 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2808. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27E4h**

Figure 14-935. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2810. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2810. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.936 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1 Register (Offset = 27E8h) [reset = 0h]

The FW Region 31 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2811. Instance Table

Instance Name	Physical Address
CBASS0	4500 27E8h

Figure 14-936. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2813. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2813. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.937 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2 Register (Offset = 27ECh) [reset = 0h]

The FW Region 31 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2814. Instance Table

Instance Name	Physical Address
CBASS0	4500 27ECh

Figure 14-937. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2816. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2816. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.938 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_L Register (Offset = 27F0h) [reset = 0h]

The FW Region 31 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2817. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27F0h**

Figure 14-938. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2819. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.939 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_H Register (Offset = 27F4h) [reset = 0h]

The FW Region 31 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2820. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27F4h**

Figure 14-939. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2822. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.940 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_L Register (Offset = 27F8h) [reset = FFFh]

The FW Region 31 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2823. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27F8h**

Figure 14-940. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2825. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.941 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_H Register (Offset = 27FCh) [reset = 0h]

The FW Region 31 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk2_dma_cfg_l0 region 31 firewall.

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Table 14-2826. Instance Table

Instance Name	Physical Address
CBASS0	**4500 27FCh**

Figure 14-941. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2828. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK2_DMA_CFG_L0_FW_REGION_31_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.942 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_CONTROL Register (Offset = 2800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2829. Instance Table

Instance Name	Physical Address
CBASS0	4500 2800h

Figure 14-942. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2831. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.943 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 2804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2832. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2804h**

Figure 14-943. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2834. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2834. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.944 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 2808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2835. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2808h**

Figure 14-944. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2837. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2837. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.945 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 280Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2838. Instance Table

Instance Name	Physical Address
CBASS0	**4500 280Ch**

Figure 14-945. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2840. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2840. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.946 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 2810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2841. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2810h**

Figure 14-946. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2843. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.947 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 2814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2844. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2814h**

Figure 14-947. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2846. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.948 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 2818h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2847. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2818h**

Figure 14-948. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2849. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.949 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 281Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 0 firewall.

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Table 14-2850. Instance Table

Instance Name	Physical Address
CBASS0	**4500 281Ch**

Figure 14-949. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2852. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.950 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_CONTROL Register (Offset = 2820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2853. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2820h**

Figure 14-950. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2855. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.951 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 2824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2856. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2824h**

Figure 14-951. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2858. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2858. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.952 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 2828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2859. Instance Table

Instance Name	Physical Address
CBASS0	4500 2828h

Figure 14-952. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2861. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2861. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.953 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 282Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2862. Instance Table

Instance Name	Physical Address
CBASS0	**4500 282Ch**

Figure 14-953. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2864. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2864. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.954 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 2830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2865. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2830h**

Figure 14-954. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2867. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.955 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 2834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2868. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2834h**

Figure 14-955. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2870. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.956 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 2838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2871. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2838h**

Figure 14-956. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2873. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.957 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 283Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 1 firewall.

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Table 14-2874. Instance Table

Instance Name	Physical Address
CBASS0	**4500 283Ch**

Figure 14-957. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2876. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.958 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_CONTROL Register (Offset = 2840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2877. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2840h**

Figure 14-958. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2879. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.959 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 2844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2880. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2844h**

Figure 14-959. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2882. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2882. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.960 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 2848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2883. Instance Table

Instance Name	Physical Address
CBASS0	4500 2848h

Figure 14-960. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2885. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2885. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.961 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 284Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2886. Instance Table

Instance Name	Physical Address
CBASS0	**4500 284Ch**

Figure 14-961. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2888. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2888. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.962 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 2850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2889. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2850h**

Figure 14-962. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2891. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.963 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 2854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2892. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2854h**

Figure 14-963. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2894. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.964 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 2858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2895. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2858h**

Figure 14-964. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2897. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.965 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 285Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 2 firewall.

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Table 14-2898. Instance Table

Instance Name	Physical Address
CBASS0	**4500 285Ch**

Figure 14-965. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2900. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.966 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_CONTROL Register (Offset = 2860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2901. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2860h**

Figure 14-966. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2903. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.967 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 2864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2904. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2864h**

Figure 14-967. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2906. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2906. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.968 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 2868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2907. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2868h**

Figure 14-968. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2909. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2909. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.969 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 286Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2910. Instance Table

Instance Name	Physical Address
CBASS0	4500 286Ch

Figure 14-969. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2912. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2912. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.970 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 2870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2913. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2870h**

Figure 14-970. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2915. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.971 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 2874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2916. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2874h**

Figure 14-971. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2918. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.972 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 2878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2919. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2878h**

Figure 14-972. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2921. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.973 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 287Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 3 firewall.

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Table 14-2922. Instance Table

Instance Name	Physical Address
CBASS0	**4500 287Ch**

Figure 14-973. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2924. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.974 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_CONTROL Register (Offset = 2880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2925. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2880h**

Figure 14-974. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2927. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.975 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 2884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2928. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2884h**

Figure 14-975. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2930. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2930. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.976 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 2888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2931. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2888h**

Figure 14-976. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2933. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2933. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.977 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 288Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2934. Instance Table

Instance Name	Physical Address
CBASS0	**4500 288Ch**

Figure 14-977. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2936. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2936. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.978 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 2890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2937. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2890h**

Figure 14-978. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2939. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.979 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 2894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2940. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2894h**

Figure 14-979. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2942. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.980 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 2898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2943. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2898h**

Figure 14-980. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2945. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.981 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 289Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 4 firewall.

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Table 14-2946. Instance Table

Instance Name	Physical Address
CBASS0	**4500 289Ch**

Figure 14-981. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2948. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.982 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_CONTROL Register (Offset = 28A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2949. Instance Table

Instance Name	Physical Address
CBASS0	4500 28A0h

Figure 14-982. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2951. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.983 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 28A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2952. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28A4h**

Figure 14-983. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2954. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2954. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.984 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 28A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2955. Instance Table

Instance Name	Physical Address
CBASS0	4500 28A8h

Figure 14-984. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2957. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2957. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.985 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 28ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2958. Instance Table

Instance Name	Physical Address
CBASS0	4500 28ACh

Figure 14-985. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2960. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2960. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.986 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 28B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2961. Instance Table

Instance Name	Physical Address
CBASS0	4500 28B0h

Figure 14-986. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2963. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.987 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 28B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2964. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28B4h**

Figure 14-987. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2966. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.988 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 28B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2967. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28B8h**

Figure 14-988. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2969. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.989 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 28BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 5 firewall.

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Table 14-2970. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28BCh**

Figure 14-989. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2972. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.990 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_CONTROL Register (Offset = 28C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2973. Instance Table

Instance Name	Physical Address
CBASS0	4500 28C0h

Figure 14-990. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2975. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.991 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 28C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2976. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28C4h**

Figure 14-991. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2978. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2978. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.992 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 28C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2979. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28C8h**

Figure 14-992. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2981. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2981. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.993 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 28CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2982. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28CCh**

Figure 14-993. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2984. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2984. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.994 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 28D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2985. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28D0h**

Figure 14-994. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2987. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.995 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 28D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2988. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28D4h**

Figure 14-995. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2990. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.996 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 28D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2991. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28D8h**

Figure 14-996. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2993. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.997 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 28DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 6 firewall.

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Table 14-2994. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28DCh**

Figure 14-997. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2996. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.998 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_CONTROL Register (Offset = 28E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-2997. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28E0h**

Figure 14-998. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2999. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.999 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 28E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3000. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28E4h**

Figure 14-999. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3002. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3002. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1000 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 28E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3003. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28E8h**

Figure 14-1000. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3005. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3005. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1001 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 28ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3006. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28ECh**

Figure 14-1001. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3008. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3008. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1002 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 28F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3009. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28F0h**

Figure 14-1002. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3011. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1003 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 28F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3012. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28F4h**

Figure 14-1003. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3014. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1004 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 28F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3015. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28F8h**

Figure 14-1004. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3017. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1005 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 28FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 7 firewall.

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Table 14-3018. Instance Table

Instance Name	Physical Address
CBASS0	**4500 28FCh**

Figure 14-1005. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3020. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1006 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_CONTROL Register (Offset = 2900h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3021. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2900h**

Figure 14-1006. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3023. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1007 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 2904h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3024. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2904h**

Figure 14-1007. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3026. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3026. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1008 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 2908h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3027. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2908h**

Figure 14-1008. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3029. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3029. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1009 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 290Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3030. Instance Table

Instance Name	Physical Address
CBASS0	**4500 290Ch**

Figure 14-1009. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3032. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3032. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1010 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 2910h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3033. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2910h**

Figure 14-1010. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3035. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1011 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 2914h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3036. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2914h**

Figure 14-1011. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3038. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1012 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 2918h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3039. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2918h**

Figure 14-1012. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3041. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1013 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 291Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 8 firewall.

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Table 14-3042. Instance Table

Instance Name	Physical Address
CBASS0	**4500 291Ch**

Figure 14-1013. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3044. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1014 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_CONTROL Register (Offset = 2920h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3045. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2920h**

Figure 14-1014. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3047. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1015 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 2924h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3048. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2924h**

Figure 14-1015. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3050. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3050. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1016 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 2928h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3051. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2928h**

Figure 14-1016. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3053. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3053. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1017 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 292Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3054. Instance Table

Instance Name	Physical Address
CBASS0	**4500 292Ch**

Figure 14-1017. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3056. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3056. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1018 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 2930h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3057. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2930h**

Figure 14-1018. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3059. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1019 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 2934h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3060. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2934h**

Figure 14-1019. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3062. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1020 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 2938h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3063. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2938h**

Figure 14-1020. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3065. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1021 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 293Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 9 firewall.

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Table 14-3066. Instance Table

Instance Name	Physical Address
CBASS0	**4500 293Ch**

Figure 14-1021. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3068. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1022 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_CONTROL Register (Offset = 2940h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3069. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2940h**

Figure 14-1022. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3071. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1023 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 2944h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3072. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2944h**

Figure 14-1023. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3074. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3074. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1024 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 2948h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3075. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2948h**

Figure 14-1024. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3077. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3077. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1025 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 294Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3078. Instance Table

Instance Name	Physical Address
CBASS0	**4500 294Ch**

Figure 14-1025. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3080. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3080. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1026 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 2950h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3081. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2950h**

Figure 14-1026. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3083. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1027 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 2954h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3084. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2954h**

Figure 14-1027. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3086. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1028 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 2958h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3087. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2958h**

Figure 14-1028. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3089. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1029 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 295Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 10 firewall.

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Table 14-3090. Instance Table

Instance Name	Physical Address
CBASS0	**4500 295Ch**

Figure 14-1029. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3092. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1030 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_CONTROL Register (Offset = 2960h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3093. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2960h**

Figure 14-1030. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3095. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1031 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 2964h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3096. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2964h**

Figure 14-1031. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3098. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3098. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1032 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 2968h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3099. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2968h**

Figure 14-1032. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3101. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3101. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1033 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 296Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3102. Instance Table

Instance Name	Physical Address
CBASS0	**4500 296Ch**

Figure 14-1033. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3104. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3104. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1034 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 2970h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3105. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2970h**

Figure 14-1034. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3107. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1035 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 2974h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3108. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2974h**

Figure 14-1035. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3110. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1036 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 2978h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3111. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2978h**

Figure 14-1036. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3113. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1037 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 297Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 11 firewall.

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Table 14-3114. Instance Table

Instance Name	Physical Address
CBASS0	**4500 297Ch**

Figure 14-1037. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3116. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1038 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_CONTROL Register (Offset = 2980h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3117. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2980h**

Figure 14-1038. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3119. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1039 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 2984h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

Return to Summary Table

Table 14-3120. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2984h**

Figure 14-1039. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3122. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3122. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1040 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 2988h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3123. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2988h**

Figure 14-1040. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3125. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3125. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1041 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 298Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3126. Instance Table

Instance Name	Physical Address
CBASS0	**4500 298Ch**

Figure 14-1041. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3128. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3128. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1042 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 2990h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

Return to Summary Table

Table 14-3129. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2990h**

Figure 14-1042. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3131. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1043 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 2994h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3132. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2994h**

Figure 14-1043. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3134. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1044 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 2998h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3135. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2998h**

Figure 14-1044. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3137. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1045 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 299Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 12 firewall.

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Table 14-3138. Instance Table

Instance Name	Physical Address
CBASS0	**4500 299Ch**

Figure 14-1045. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3140. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1046 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_CONTROL Register (Offset = 29A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3141. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29A0h**

Figure 14-1046. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3143. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1047 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 29A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3144. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29A4h**

Figure 14-1047. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3146. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3146. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1048 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 29A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3147. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29A8h**

Figure 14-1048. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3149. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3149. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1049 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 29ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3150. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29ACh**

Figure 14-1049. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3152. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3152. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1050 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 29B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3153. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29B0h**

Figure 14-1050. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3155. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1051 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 29B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3156. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29B4h**

Figure 14-1051. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3158. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1052 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 29B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3159. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29B8h**

Figure 14-1052. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3161. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1053 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 29BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 13 firewall.

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Table 14-3162. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29BCh**

Figure 14-1053. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3164. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1054 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_CONTROL Register (Offset = 29C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3165. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29C0h**

Figure 14-1054. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3167. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1055 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 29C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3168. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29C4h**

Figure 14-1055. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3170. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3170. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1056 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 29C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3171. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29C8h**

Figure 14-1056. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3173. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3173. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1057 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 29CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3174. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29CCh**

Figure 14-1057. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3176. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3176. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1058 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 29D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3177. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29D0h**

Figure 14-1058. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3179. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1059 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 29D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3180. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29D4h**

Figure 14-1059. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3182. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1060 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 29D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3183. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29D8h**

Figure 14-1060. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3185. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1061 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 29DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 14 firewall.

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Table 14-3186. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29DCh**

Figure 14-1061. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3188. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1062 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_CONTROL Register (Offset = 29E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3189. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29E0h**

Figure 14-1062. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3191. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1063 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 29E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3192. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29E4h**

Figure 14-1063. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3194. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3194. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1064 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 29E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3195. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29E8h**

Figure 14-1064. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3197. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3197. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1065 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 29ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3198. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29ECh**

Figure 14-1065. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3200. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3200. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1066 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 29F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3201. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29F0h**

Figure 14-1066. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3203. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1067 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 29F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3204. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29F4h**

Figure 14-1067. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3206. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1068 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 29F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3207. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29F8h**

Figure 14-1068. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3209. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1069 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 29FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_clk4_cfg_l0 region 15 firewall.

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Table 14-3210. Instance Table

Instance Name	Physical Address
CBASS0	**4500 29FCh**

Figure 14-1069. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3212. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_CLK4_CFG_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1070 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL Register (Offset = 2C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3213. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C00h**

Figure 14-1070. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3215. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3215. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1071 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 2C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3216. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C04h**

Figure 14-1071. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3218. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3218. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1072 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 2C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3219. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C08h**

Figure 14-1072. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3221. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3221. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1073 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 2C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3222. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C0Ch**

Figure 14-1073. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3224. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3224. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1074 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 2C10h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3225. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C10h**

Figure 14-1074. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3227. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1075 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 2C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3228. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C14h**

Figure 14-1075. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3230. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1076 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 2C18h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3231. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C18h**

Figure 14-1076. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3233. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1077 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 2C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 0 firewall.

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Table 14-3234. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C1Ch**

Figure 14-1077. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3236. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1078 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL Register (Offset = 2C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3237. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C20h**

Figure 14-1078. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3239. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3239. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1079 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 2C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3240. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C24h**

Figure 14-1079. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3242. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3242. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1080 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 2C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3243. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C28h**

Figure 14-1080. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3245. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3245. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1081 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 2C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3246. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C2Ch**

Figure 14-1081. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3248. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3248. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1082 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 2C30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3249. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C30h**

Figure 14-1082. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3251. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1083 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 2C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3252. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C34h**

Figure 14-1083. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3254. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1084 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 2C38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3255. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C38h**

Figure 14-1084. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3257. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1085 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 2C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 1 firewall.

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Table 14-3258. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C3Ch**

Figure 14-1085. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3260. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1086 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL Register (Offset = 2C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3261. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C40h**

Figure 14-1086. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3263. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3263. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1087 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 2C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3264. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C44h**

Figure 14-1087. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3266. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3266. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1088 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 2C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3267. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C48h**

Figure 14-1088. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3269. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3269. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1089 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 2C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3270. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C4Ch**

Figure 14-1089. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3272. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3272. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1090

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 2C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3273. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C50h**

Figure 14-1090. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3275. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1091 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 2C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3276. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C54h**

Figure 14-1091. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3278. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1092 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 2C58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3279. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C58h**

Figure 14-1092. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3281. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1093 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 2C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 2 firewall.

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Table 14-3282. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C5Ch**

Figure 14-1093. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3284. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1094 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL Register (Offset = 2C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3285. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C60h**

Figure 14-1094. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3287. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3287. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1095 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 2C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3288. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C64h**

Figure 14-1095. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3290. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3290. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1096 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 2C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3291. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C68h**

Figure 14-1096. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3293. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3293. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1097 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 2C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3294. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C6Ch**

Figure 14-1097. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3296. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3296. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1098 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 2C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3297. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C70h**

Figure 14-1098. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3299. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1099 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 2C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3300. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C74h**

Figure 14-1099. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3302. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1100 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 2C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3303. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C78h**

Figure 14-1100. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3305. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1101 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 2C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 3 firewall.

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Table 14-3306. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C7Ch**

Figure 14-1101. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3308. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1102 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_CONTROL Register (Offset = 2C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3309. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C80h**

Figure 14-1102. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3311. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1103 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 2C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3312. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C84h**

Figure 14-1103. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3314. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3314. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1104 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 2C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3315. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C88h**

Figure 14-1104. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3317. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3317. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1105 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 2C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3318. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C8Ch**

Figure 14-1105. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3320. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3320. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1106 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 2C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3321. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C90h**

Figure 14-1106. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3323. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1107 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 2C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3324. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C94h**

Figure 14-1107. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3326. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1108 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 2C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3327. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C98h**

Figure 14-1108. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3329. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1109 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 2C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 4 firewall.

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Table 14-3330. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2C9Ch**

Figure 14-1109. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3332. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1110 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_CONTROL Register (Offset = 2CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3333. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CA0h**

Figure 14-1110. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3335. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1111 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 2CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3336. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CA4h**

Figure 14-1111. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3338. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3338. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1112 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 2CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3339. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CA8h**

Figure 14-1112. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3341. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3341. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1113 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 2CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3342. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CACh**

Figure 14-1113. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3344. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3344. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1114
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 2CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3345. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CB0h**

Figure 14-1114. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3347. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1115 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 2CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3348. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CB4h**

Figure 14-1115. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3350. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1116 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 2CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3351. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CB8h**

Figure 14-1116. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3353. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1117 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 2CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 5 firewall.

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Table 14-3354. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CBCh**

Figure 14-1117. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3356. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1118 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_CONTROL Register (Offset = 2CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3357. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CC0h**

Figure 14-1118. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3359. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1119 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 2CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3360. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CC4h**

Figure 14-1119. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3362. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3362. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1120 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 2CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3363. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CC8h**

Figure 14-1120. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3365. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3365. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1121 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 2CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3366. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CCCh**

Figure 14-1121. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3368. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3368. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1122 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 2CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3369. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CD0h**

Figure 14-1122. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3371. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1123 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 2CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3372. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CD4h**

Figure 14-1123. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3374. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1124 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 2CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3375. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CD8h**

Figure 14-1124. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3377. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1125 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 2CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 6 firewall.

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Table 14-3378. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CDCh**

Figure 14-1125. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3380. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1126 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_CONTROL Register (Offset = 2CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3381. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CE0h**

Figure 14-1126. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3383. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1127 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 2CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3384. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CE4h**

Figure 14-1127. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3386. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3386. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1128 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 2CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3387. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CE8h**

Figure 14-1128. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3389. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3389. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1129 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 2CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3390. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CECh**

Figure 14-1129. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3392. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3392. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1130 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 2CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3393. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CF0h**

Figure 14-1130. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3395. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1131 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 2CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3396. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CF4h**

Figure 14-1131. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3398. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1132 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 2CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3399. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CF8h**

Figure 14-1132. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3401. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1133 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 2CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 7 firewall.

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Table 14-3402. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2CFCh**

Figure 14-1133. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3404. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1134 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_CONTROL Register (Offset = 2D00h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3405. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D00h**

Figure 14-1134. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3407. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1135 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 2D04h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3408. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D04h**

Figure 14-1135. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3410. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3410. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1136 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 2D08h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3411. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D08h**

Figure 14-1136. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3413. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3413. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1137 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 2D0Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3414. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D0Ch**

Figure 14-1137. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3416. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3416. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1138 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 2D10h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3417. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D10h**

Figure 14-1138. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3419. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1139 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 2D14h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3420. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D14h**

Figure 14-1139. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3422. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1140 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 2D18h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3423. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D18h**

Figure 14-1140. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3425. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1141 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 2D1Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 8 firewall.

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Table 14-3426. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2D1Ch**

Figure 14-1141. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3428. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1142 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_CONTROL Register (Offset = 2D20h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3429. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D20h**

Figure 14-1142. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3431. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1143 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 2D24h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3432. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D24h**

Figure 14-1143. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3434. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3434. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1144 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 2D28h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

Return to Summary Table

Table 14-3435. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D28h**

Figure 14-1144. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3437. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3437. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1145 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 2D2Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3438. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D2Ch**

Figure 14-1145. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3440. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3440. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1146 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 2D30h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3441. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D30h**

Figure 14-1146. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3443. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1147 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 2D34h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3444. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2D34h**

Figure 14-1147. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3446. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1148 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 2D38h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3447. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D38h**

Figure 14-1148. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3449. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1149 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 2D3Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 9 firewall.

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Table 14-3450. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D3Ch**

Figure 14-1149. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3452. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1150 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL Register (Offset = 2D40h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3453. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D40h**

Figure 14-1150. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3455. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3455. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1151 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 2D44h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3456. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D44h**

Figure 14-1151. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3458. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3458. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1152 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 2D48h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3459. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D48h**

Figure 14-1152. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3461. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3461. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1153 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 2D4Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3462. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D4Ch**

Figure 14-1153. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3464. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3464. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1154 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 2D50h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3465. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D50h**

Figure 14-1154. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3467. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1155
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 2D54h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3468. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D54h**

Figure 14-1155. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3470. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1156 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 2D58h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3471. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D58h**

Figure 14-1156. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3473. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1157 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 2D5Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 10 firewall.

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Table 14-3474. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D5Ch**

Figure 14-1157. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3476. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1158 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL Register (Offset = 2D60h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3477. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2D60h**

Figure 14-1158. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3479. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3479. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1159 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 2D64h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3480. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D64h**

Figure 14-1159. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3482. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3482. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1160 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 2D68h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3483. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D68h**

Figure 14-1160. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3485. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3485. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1161 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 2D6Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3486. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D6Ch**

Figure 14-1161. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3488. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3488. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1162
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 2D70h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3489. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D70h**

Figure 14-1162. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3491. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1163 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 2D74h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3492. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D74h**

Figure 14-1163. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3494. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1164 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 2D78h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3495. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D78h**

Figure 14-1164. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3497. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1165 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 2D7Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 11 firewall.

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Table 14-3498. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2D7Ch**

Figure 14-1165. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3500. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1166 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL Register (Offset = 2D80h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3501. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D80h**

Figure 14-1166. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3503. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3503. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1167 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 2D84h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3504. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D84h**

Figure 14-1167. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3506. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3506. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1168 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 2D88h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3507. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D88h**

Figure 14-1168. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3509. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3509. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1169 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 2D8Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3510. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D8Ch**

Figure 14-1169. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3512. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3512. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1170 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 2D90h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3513. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D90h**

Figure 14-1170. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3515. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1171 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 2D94h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3516. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D94h**

Figure 14-1171. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3518. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1172 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 2D98h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3519. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D98h**

Figure 14-1172. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3521. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1173 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 2D9Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 12 firewall.

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Table 14-3522. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2D9Ch**

Figure 14-1173. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3524. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1174 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL Register (Offset = 2DA0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3525. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DA0h**

Figure 14-1174. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3527. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3527. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1175 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 2DA4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3528. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DA4h**

Figure 14-1175. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3530. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3530. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1176 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 2DA8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3531. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DA8h**

Figure 14-1176. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3533. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3533. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1177 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 2DACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3534. Instance Table

Instance Name	Physical Address
CBASS0	4500 2DACh

Figure 14-1177. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3536. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3536. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1178
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 2DB0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3537. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DB0h**

Figure 14-1178. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3539. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1179 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 2DB4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3540. Instance Table

Instance Name	Physical Address
CBASS0	4500 2DB4h

Figure 14-1179. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3542. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1180 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 2DB8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3543. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DB8h**

Figure 14-1180. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3545. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1181 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 2DBCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 13 firewall.

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Table 14-3546. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DBCh**

Figure 14-1181. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3548. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1182 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL Register (Offset = 2DC0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3549. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 2DC0h**

Figure 14-1182. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3551. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3551. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1183 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 2DC4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3552. Instance Table

Instance Name	Physical Address
CBASS0	4500 2DC4h

Figure 14-1183. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3554. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3554. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1184 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 2DC8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3555. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DC8h**

Figure 14-1184. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3557. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3557. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1185 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 2DCCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3558. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DCCh**

Figure 14-1185. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3560. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3560. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1186 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 2DD0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3561. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DD0h**

Figure 14-1186. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3563. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1187 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 2DD4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3564. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DD4h**

Figure 14-1187. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3566. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1188 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 2DD8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3567. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DD8h**

Figure 14-1188. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3569. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1189
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 2DDCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 14 firewall.

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Table 14-3570. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DDCh**

Figure 14-1189. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3572. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1190 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL Register (Offset = 2DE0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3573. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DE0h**

Figure 14-1190. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3575. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3575. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1191 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 2DE4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3576. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DE4h**

Figure 14-1191. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3578. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3578. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1192 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 2DE8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3579. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DE8h**

Figure 14-1192. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3581. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3581. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1193 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 2DECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3582. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DECh**

Figure 14-1193. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3584. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3584. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1194 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 2DF0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3585. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DF0h**

Figure 14-1194. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3587. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1195 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 2DF4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3588. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DF4h**

Figure 14-1195. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3590. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1196 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 2DF8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3591. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DF8h**

Figure 14-1196. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3593. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1197
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 2DFCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64b_clk2_to_SCRP_32_clk2_misc_l0 region 15 firewall.

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Table 14-3594. Instance Table

Instance Name	Physical Address
CBASS0	**4500 2DFCh**

Figure 14-1197. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3596. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_32_CLK2_MISC_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1198 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_CONTROL Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_CONTROL Register (Offset = 3400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3597. Instance Table

Instance Name	Physical Address
CBASS0	4500 3400h

Figure 14-1198. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3599. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1199 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 3404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3600. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3404h**

Figure 14-1199. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3602. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3602. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1200 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 3408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3603. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3408h**

Figure 14-1200. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3605. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3605. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1201 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 340Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3606. Instance Table

Instance Name	Physical Address
CBASS0	**4500 340Ch**

Figure 14-1201. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3608. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3608. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1202 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 3410h) [reset = 30300000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3609. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3410h**

Figure 14-1202. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">30300h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">30300h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">30300h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3611. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	30300h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1203 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 3414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3612. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3414h**

Figure 14-1203. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3614. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1204 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 3418h) [reset = 30300FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3615. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3418h**

Figure 14-1204. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
30300h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
30300h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
30300h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3617. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	30300h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1205 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 341Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcrc64_main_0.s_cfg region 0 firewall.

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Table 14-3618. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 341Ch**

Figure 14-1205. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3620. CBASS_FW_IMCRC64_MAIN_0_S_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1206
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = 3800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3621. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3800h**

Figure 14-1206. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3623. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3623. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1207 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 3804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3624. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3804h**

Figure 14-1207. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3626. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3626. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1208 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 3808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3627. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3808h**

Figure 14-1208. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3629. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3629. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1209 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 380Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3630. Instance Table

Instance Name	Physical Address
CBASS0	4500 380Ch

Figure 14-1209. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3632. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3632. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1210 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 3810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3633. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3810h**

Figure 14-1210. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3635. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1211 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 3814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3636. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3814h**

Figure 14-1211. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3638. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1212
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 3818h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3639. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3818h**

Figure 14-1212. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3641. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1213 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 381Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 0 firewall.

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Table 14-3642. Instance Table

Instance Name	Physical Address
CBASS0	4500 381Ch

Figure 14-1213. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3644. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1214 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = 3820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3645. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3820h**

Figure 14-1214. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3647. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3647. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1215 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 3824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3648. Instance Table

Instance Name	Physical Address
CBASS0	4500 3824h

Figure 14-1215. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3650. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3650. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1216 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 3828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3651. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3828h**

Figure 14-1216. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3653. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3653. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1217 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 382Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3654. Instance Table

Instance Name	Physical Address
CBASS0	**4500 382Ch**

Figure 14-1217. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3656. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3656. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1218

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 3830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3657. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3830h**

Figure 14-1218. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3659. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1219 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 3834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3660. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3834h**

Figure 14-1219. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3662. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1220 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 3838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3663. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3838h**

Figure 14-1220. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3665. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1221
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 383Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 1 firewall.

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Table 14-3666. Instance Table

Instance Name	Physical Address
CBASS0	**4500 383Ch**

Figure 14-1221. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3668. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1222
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = 3840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3669. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3840h**

Figure 14-1222. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3671. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3671. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1223 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 3844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3672. Instance Table

Instance Name	Physical Address
CBASS0	4500 3844h

Figure 14-1223. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3674. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3674. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1224 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 3848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3675. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3848h**

Figure 14-1224. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3677. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3677. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1225 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 384Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3678. Instance Table

Instance Name	Physical Address
CBASS0	**4500 384Ch**

Figure 14-1225. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3680. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3680. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1226 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 3850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3681. Instance Table

Instance Name	Physical Address
CBASS0	4500 3850h

Figure 14-1226. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3683. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1227 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 3854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3684. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3854h**

Figure 14-1227. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3686. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1228 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 3858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3687. Instance Table

Instance Name	Physical Address
CBASS0	4500 3858h

Figure 14-1228. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3689. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1229 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 385Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 2 firewall.

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Table 14-3690. Instance Table

Instance Name	Physical Address
CBASS0	**4500 385Ch**

Figure 14-1229. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3692. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1230
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = 3860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3693. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3860h**

Figure 14-1230. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3695. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3695. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1231 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 3864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3696. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3864h**

Figure 14-1231. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3698. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3698. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1232 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 3868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3699. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3868h**

Figure 14-1232. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3701. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3701. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1233 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 386Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3702. Instance Table

Instance Name	Physical Address
CBASS0	**4500 386Ch**

Figure 14-1233. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3704. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3704. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1234 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 3870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3705. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3870h**

Figure 14-1234. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3707. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1235 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 3874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3708. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3874h**

Figure 14-1235. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3710. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1236 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 3878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3711. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3878h**

Figure 14-1236. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3713. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1237 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 387Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 3 firewall.

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Table 14-3714. Instance Table

Instance Name	Physical Address
CBASS0	**4500 387Ch**

Figure 14-1237. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3716. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1238
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = 3880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3717. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3880h**

Figure 14-1238. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3719. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3719. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1239 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 3884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3720. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3884h**

Figure 14-1239. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3722. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3722. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1240 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 3888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3723. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3888h**

Figure 14-1240. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3725. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3725. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1241 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 388Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3726. Instance Table

Instance Name	Physical Address
CBASS0	**4500 388Ch**

Figure 14-1241. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3728. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3728. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1242 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 3890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3729. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3890h**

Figure 14-1242. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3731. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1243 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 3894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3732. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3894h**

Figure 14-1243. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3734. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1244 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 3898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3735. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3898h**

Figure 14-1244. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3737. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1245 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 389Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 4 firewall.

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Table 14-3738. Instance Table

Instance Name	Physical Address
CBASS0	**4500 389Ch**

Figure 14-1245. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3740. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1246
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = 38A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3741. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38A0h**

Figure 14-1246. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3743. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3743. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1247 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 38A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3744. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38A4h**

Figure 14-1247. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3746. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3746. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1248 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 38A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3747. Instance Table

Instance Name	Physical Address
CBASS0	4500 38A8h

Figure 14-1248. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3749. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3749. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1249 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 38ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3750. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38ACh**

Figure 14-1249. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3752. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3752. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1250 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 38B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3753. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38B0h**

Figure 14-1250. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3755. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1251 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 38B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3756. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38B4h**

Figure 14-1251. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3758. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1252 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 38B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3759. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38B8h**

Figure 14-1252. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3761. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1253 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 38BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 5 firewall.

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Table 14-3762. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38BCh**

Figure 14-1253. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3764. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1254 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = 38C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3765. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38C0h**

Figure 14-1254. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3767. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3767. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1255 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 38C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3768. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38C4h**

Figure 14-1255. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3770. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3770. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1256 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 38C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3771. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 38C8h**

Figure 14-1256. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3773. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3773. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1257 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 38CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3774. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38CCh**

Figure 14-1257. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3776. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3776. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1258 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 38D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3777. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38D0h**

Figure 14-1258. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3779. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1259
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 38D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3780. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38D4h**

Figure 14-1259. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3782. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1260
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 38D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3783. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38D8h**

Figure 14-1260. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3785. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1261 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 38DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 6 firewall.

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Table 14-3786. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38DCh**

Figure 14-1261. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3788. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1262 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = 38E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3789. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38E0h**

Figure 14-1262. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3791. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3791. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1263 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 38E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3792. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38E4h**

Figure 14-1263. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3794. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3794. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1264 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 38E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3795. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38E8h**

Figure 14-1264. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3797. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3797. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1265 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 38ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3798. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38ECh**

Figure 14-1265. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3800. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3800. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1266

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 38F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3801. Instance Table

Instance Name	Physical Address
CBASS0	4500 38F0h

Figure 14-1266. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3803. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1267 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 38F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3804. Instance Table

Instance Name	Physical Address
CBASS0	**4500 38F4h**

Figure 14-1267. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3806. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1268 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 38F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3807. Instance Table

Instance Name	Physical Address
CBASS0	4500 38F8h

Figure 14-1268. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3809. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1269 CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 38FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_main_data_cbass_to_am62a_main_mcasp_cbass_data_l0.slv region 7 firewall.

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Table 14-3810. Instance Table

Instance Name	Physical Address
CBASS0	4500 38FCh

Figure 14-1269. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3812. CBASS_FW_EXPORT_AM62A_MAIN_DATA_CBASS_TO_AM62A_MAIN_MCASP_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1270 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register (Offset = 3C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3813. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C00h**

Figure 14-1270. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3815. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1271 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 3C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3816. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C04h**

Figure 14-1271. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3818. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3818. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1272 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 3C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3819. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C08h**

Figure 14-1272. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3821. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3821. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1273 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 3C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3822. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C0Ch**

Figure 14-1273. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3824. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3824. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1274 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 3C10h) [reset = 43C40000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3825. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C10h**

Figure 14-1274. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">43C40h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">43C40h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">43C40h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3827. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	43C40h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1275 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 3C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 0 firewall.

Return to Summary Table

Table 14-3828. Instance Table

Instance Name	Physical Address
CBASS0	4500 3C14h

Figure 14-1275. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3830. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1276 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 3C18h) [reset = 43C4FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3831. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C18h**

Figure 14-1276. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">43C4Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">43C4Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">43C4Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3833. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	43C4Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1277 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 3C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 0 firewall.

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Table 14-3834. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C1Ch**

Figure 14-1277. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3836. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1278 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register (Offset = 3C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3837. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C20h**

Figure 14-1278. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3839. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1279 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 3C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3840. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C24h**

Figure 14-1279. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3842. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3842. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1280 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 3C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3843. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C28h**

Figure 14-1280. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3845. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3845. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1281 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 3C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3846. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C2Ch**

Figure 14-1281. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3848. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3848. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1282 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 3C30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3849. Instance Table

Instance Name	Physical Address
CBASS0	4500 3C30h

Figure 14-1282. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3851. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1283 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 3C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3852. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C34h**

Figure 14-1283. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3854. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1284 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 3C38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3855. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C38h**

Figure 14-1284. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3857. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1285 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 3C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 1 firewall.

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Table 14-3858. Instance Table

Instance Name	Physical Address
CBASS0	4500 3C3Ch

Figure 14-1285. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3860. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1286 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register (Offset = 3C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3861. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C40h**

Figure 14-1286. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3863. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1287 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 3C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3864. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C44h**

Figure 14-1287. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3866. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3866. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1288 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 3C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3867. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C48h**

Figure 14-1288. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3869. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3869. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1289 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 3C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3870. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C4Ch**

Figure 14-1289. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3872. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3872. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1290 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 3C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3873. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3C50h**

Figure 14-1290. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3875. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1291 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 3C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3876. Instance Table

Instance Name	Physical Address
CBASS0	4500 3C54h

Figure 14-1291. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3878. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1292 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 3C58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3879. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C58h**

Figure 14-1292. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3881. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1293 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 3C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 2 firewall.

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Table 14-3882. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C5Ch**

Figure 14-1293. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3884. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1294 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register (Offset = 3C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3885. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C60h**

Figure 14-1294. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3887. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1295 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 3C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3888. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C64h**

Figure 14-1295. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3890. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3890. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1296 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 3C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3891. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C68h**

Figure 14-1296. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3893. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3893. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1297 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 3C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 3 firewall.

Return to Summary Table

Table 14-3894. Instance Table

Instance Name	Physical Address
CBASS0	4500 3C6Ch

Figure 14-1297. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3896. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3896. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1298 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 3C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3897. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C70h**

Figure 14-1298. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3899. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1299 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 3C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3900. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C74h**

Figure 14-1299. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3902. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1300 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 3C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3903. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C78h**

Figure 14-1300. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3905. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1301 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 3C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 3 firewall.

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Table 14-3906. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C7Ch**

Figure 14-1301. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3908. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1302 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register (Offset = 3C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3909. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C80h**

Figure 14-1302. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3911. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1303 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 3C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3912. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C84h**

Figure 14-1303. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3914. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3914. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1304 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 3C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3915. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C88h**

Figure 14-1304. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3917. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3917. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1305 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 3C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3918. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C8Ch**

Figure 14-1305. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3920. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3920. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1306 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 3C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3921. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C90h**

Figure 14-1306. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3923. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1307 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 3C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3924. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C94h**

Figure 14-1307. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3926. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1308 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 3C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3927. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C98h**

Figure 14-1308. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3929. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1309 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 3C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 4 firewall.

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Table 14-3930. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3C9Ch**

Figure 14-1309. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3932. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1310 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register (Offset = 3CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3933. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CA0h**

Figure 14-1310. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3935. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1311 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 3CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3936. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CA4h**

Figure 14-1311. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3938. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3938. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1312 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 3CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3939. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CA8h**

Figure 14-1312. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3941. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3941. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1313 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 3CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3942. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CACh**

Figure 14-1313. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3944. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3944. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1314 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 3CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3945. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CB0h**

Figure 14-1314. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3947. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1315 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 3CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3948. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CB4h**

Figure 14-1315. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3950. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1316 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 3CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3951. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CB8h**

Figure 14-1316. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3953. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1317 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 3CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 5 firewall.

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Table 14-3954. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CBCh**

Figure 14-1317. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3956. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1318 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register (Offset = 3CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3957. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3CC0h**

Figure 14-1318. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3959. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1319 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 3CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3960. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CC4h**

Figure 14-1319. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3962. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3962. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1320 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 3CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3963. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CC8h**

Figure 14-1320. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3965. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3965. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1321 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 3CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3966. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CCCh**

Figure 14-1321. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3968. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3968. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1322 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 3CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3969. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CD0h**

Figure 14-1322. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3971. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1323 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 3CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3972. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CD4h**

Figure 14-1323. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3974. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1324 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 3CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3975. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3CD8h**

Figure 14-1324. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3977. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1325 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 3CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 6 firewall.

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Table 14-3978. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CDCh**

Figure 14-1325. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3980. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1326 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register (Offset = 3CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3981. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CE0h**

Figure 14-1326. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3983. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1327 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 3CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3984. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CE4h**

Figure 14-1327. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3986. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3986. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1328 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 3CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3987. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CE8h**

Figure 14-1328. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3989. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3989. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1329 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 3CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3990. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CECh**

Figure 14-1329. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3992. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3992. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1330 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 3CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3993. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CF0h**

Figure 14-1330. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3995. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1331 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 3CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3996. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CF4h**

Figure 14-1331. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3998. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1332 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 3CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-3999. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CF8h**

Figure 14-1332. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4001. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1333 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 3CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 7 firewall.

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Table 14-4002. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3CFCh**

Figure 14-1333. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4004. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1334 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_CONTROL Register (Offset = 3D00h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4005. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D00h**

Figure 14-1334. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4007. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1335 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0 Register (Offset = 3D04h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4008. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D04h**

Figure 14-1335. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4010. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4010. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1336 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1 Register (Offset = 3D08h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4011. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D08h**

Figure 14-1336. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4013. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4013. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1337 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2 Register (Offset = 3D0Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4014. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D0Ch**

Figure 14-1337. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4016. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4016. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1338 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_L Register (Offset = 3D10h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4017. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D10h**

Figure 14-1338. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4019. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1339 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_H Register (Offset = 3D14h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4020. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D14h**

Figure 14-1339. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4022. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1340 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_L Register (Offset = 3D18h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4023. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D18h**

Figure 14-1340. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4025. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1341 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_H Register (Offset = 3D1Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 8 firewall.

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Table 14-4026. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D1Ch**

Figure 14-1341. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4028. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1342 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_CONTROL Register (Offset = 3D20h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4029. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D20h**

Figure 14-1342. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4031. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1343 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0 Register (Offset = 3D24h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4032. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D24h**

Figure 14-1343. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4034. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4034. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1344 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1 Register (Offset = 3D28h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4035. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D28h**

Figure 14-1344. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4037. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4037. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1345 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2 Register (Offset = 3D2Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4038. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D2Ch**

Figure 14-1345. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4040. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4040. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1346 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_L Register (Offset = 3D30h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4041. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D30h**

Figure 14-1346. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4043. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1347 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_H Register (Offset = 3D34h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4044. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D34h**

Figure 14-1347. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4046. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1348 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_L Register (Offset = 3D38h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4047. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D38h**

Figure 14-1348. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4049. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1349 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_H Register (Offset = 3D3Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 9 firewall.

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Table 14-4050. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D3Ch**

Figure 14-1349. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4052. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1350 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_CONTROL Register (Offset = 3D40h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4053. Instance Table

Instance Name	Physical Address
CBASS0	4500 3D40h

Figure 14-1350. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4055. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1351 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0 Register (Offset = 3D44h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4056. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D44h**

Figure 14-1351. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4058. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4058. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1352 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1 Register (Offset = 3D48h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4059. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D48h**

Figure 14-1352. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4061. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4061. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1353 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2 Register (Offset = 3D4Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4062. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D4Ch**

Figure 14-1353. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-4064. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4064. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1354 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_L Register (Offset = 3D50h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4065. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D50h**

Figure 14-1354. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4067. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1355 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_H Register (Offset = 3D54h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4068. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D54h**

Figure 14-1355. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4070. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1356 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_L Register (Offset = 3D58h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4071. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D58h**

Figure 14-1356. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4073. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1357 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_H Register (Offset = 3D5Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 10 firewall.

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Table 14-4074. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3D5Ch**

Figure 14-1357. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4076. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1358 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_CONTROL Register (Offset = 3D60h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4077. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D60h**

Figure 14-1358. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4079. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1359 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0 Register (Offset = 3D64h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4080. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D64h**

Figure 14-1359. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4082. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4082. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1360 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1 Register (Offset = 3D68h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4083. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D68h**

Figure 14-1360. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-4085. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4085. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1361 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2 Register (Offset = 3D6Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4086. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D6Ch**

Figure 14-1361. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4088. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4088. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1362 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_L Register (Offset = 3D70h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4089. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D70h**

Figure 14-1362. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4091. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1363 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_H Register (Offset = 3D74h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4092. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D74h**

Figure 14-1363. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4094. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1364 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_L Register (Offset = 3D78h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4095. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D78h**

Figure 14-1364. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4097. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1365 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_H Register (Offset = 3D7Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 11 firewall.

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Table 14-4098. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D7Ch**

Figure 14-1365. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4100. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1366 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_CONTROL Register (Offset = 3D80h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4101. Instance Table

Instance Name	Physical Address
CBASS0	4500 3D80h

Figure 14-1366. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4103. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1367 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0 Register (Offset = 3D84h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4104. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D84h**

Figure 14-1367. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4106. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4106. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1368 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1 Register (Offset = 3D88h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4107. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D88h**

Figure 14-1368. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4109. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4109. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1369 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2 Register (Offset = 3D8Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4110. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D8Ch**

Figure 14-1369. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4112. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4112. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1370 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_L Register (Offset = 3D90h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4113. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D90h**

Figure 14-1370. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4115. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1371 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_H Register (Offset = 3D94h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4116. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D94h**

Figure 14-1371. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4118. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1372 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_L Register (Offset = 3D98h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4119. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D98h**

Figure 14-1372. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4121. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1373 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_H Register (Offset = 3D9Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 12 firewall.

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Table 14-4122. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3D9Ch**

Figure 14-1373. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4124. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1374 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_CONTROL Register (Offset = 3DA0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4125. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DA0h**

Figure 14-1374. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4127. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1375 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0 Register (Offset = 3DA4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4128. Instance Table

Instance Name	**Physical Address**
CBASS0	**4500 3DA4h**

Figure 14-1375. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4130. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4130. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1376 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1 Register (Offset = 3DA8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4131. Instance Table

Instance Name	Physical Address
CBASS0	4500 3DA8h

Figure 14-1376. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4133. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4133. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1377 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2 Register (Offset = 3DACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4134. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DACh**

Figure 14-1377. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4136. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4136. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1378 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_L Register (Offset = 3DB0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4137. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DB0h**

Figure 14-1378. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4139. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1379 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_H Register (Offset = 3DB4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4140. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DB4h**

Figure 14-1379. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4142. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1380 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_L Register (Offset = 3DB8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4143. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DB8h**

Figure 14-1380. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4145. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1381 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_H Register (Offset = 3DBCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 13 firewall.

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Table 14-4146. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DBCh**

Figure 14-1381. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4148. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1382 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_CONTROL Register (Offset = 3DC0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4149. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DC0h**

Figure 14-1382. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4151. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1383 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0 Register (Offset = 3DC4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4152. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DC4h**

Figure 14-1383. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4154. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4154. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1384 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1 Register (Offset = 3DC8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4155. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DC8h**

Figure 14-1384. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4157. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4157. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1385 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2 Register (Offset = 3DCCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4158. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DCCh**

Figure 14-1385. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4160. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4160. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1386 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_L Register (Offset = 3DD0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4161. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DD0h**

Figure 14-1386. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4163. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1387 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_H Register (Offset = 3DD4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4164. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DD4h**

Figure 14-1387. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4166. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1388 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_L Register (Offset = 3DD8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4167. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DD8h**

Figure 14-1388. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4169. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1389 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_H Register (Offset = 3DDCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 14 firewall.

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Table 14-4170. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DDCh**

Figure 14-1389. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4172. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1390 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_CONTROL Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_CONTROL Register (Offset = 3DE0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4173. Instance Table

Instance Name	Physical Address
CBASS0	4500 3DE0h

Figure 14-1390. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4175. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1391 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0 Register (Offset = 3DE4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4176. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DE4h**

Figure 14-1391. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4178. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4178. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1392 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1 Register (Offset = 3DE8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4179. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DE8h**

Figure 14-1392. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4181. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4181. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1393 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2 Register (Offset = 3DECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4182. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DECh**

Figure 14-1393. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4184. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4184. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1394 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_L Register (Offset = 3DF0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4185. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DF0h**

Figure 14-1394. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4187. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1395 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_H Register (Offset = 3DF4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4188. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DF4h**

Figure 14-1395. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4190. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1396 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_L Register (Offset = 3DF8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4191. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DF8h**

Figure 14-1396. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4193. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1397 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_H Register

1 CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_H Register (Offset = 3DFCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram2kx256e_main_0.slv region 15 firewall.

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Table 14-4194. Instance Table

Instance Name	Physical Address
CBASS0	**4500 3DFCh**

Figure 14-1397. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4196. CBASS_FW_IMSRAM2KX256E_MAIN_0_SLV_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1398 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 400h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 0 ISC.

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Table 14-4197. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0400h**

Figure 14-1398. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4199. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4199. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1399 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 0 ISC.

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Table 14-4200. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0410h**

Figure 14-1399. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4202. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1400 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 0 ISC.

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Table 14-4203. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0414h**

Figure 14-1400. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4205. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1401
CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register

1
CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 0 ISC.

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Table 14-4206. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0418h**

Figure 14-1401. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4208. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1402 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 0 ISC.

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Table 14-4209. Instance Table

Instance Name	Physical Address
CBASS0	**4582 041Ch**

Figure 14-1402. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-4211. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1403 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register (Offset = 420h) [reset = 44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r region 1 ISC.

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Table 14-4212. Instance Table

Instance Name	Physical Address
CBASS0	4582 0420h

Figure 14-1403. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-4214. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-4214. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1404 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 400h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 0 ISC.

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Table 14-4215. Instance Table

Instance Name	Physical Address
CBASS0	4582 0800h

Figure 14-1404. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
4h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4217. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4217. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1405
CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register

1
CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 0 ISC.

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Table 14-4218. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0810h**

Figure 14-1405. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4220. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1406 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 0 ISC.

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Table 14-4221. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0814h**

Figure 14-1406. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4223. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1407 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 0 ISC.

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Table 14-4224. Instance Table

Instance Name	Physical Address
CBASS0	**4582 0818h**

Figure 14-1407. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4226. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1408 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 0 ISC.

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Table 14-4227. Instance Table

Instance Name	Physical Address
CBASS0	4582 081Ch

Figure 14-1408. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4229. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1409 CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register

1

CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register (Offset = 820h) [reset = 44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w region 1 ISC.

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Table 14-4230. Instance Table

Instance Name	Physical Address
CBASS0	4582 0820h

Figure 14-1409. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4232. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-4232. CBASS_ISC_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1410 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register (Offset = 1400h) [reset = 10B000h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_led2vbus_main_0.vbusp region 0 ISC.

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Table 14-4233. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1400h**

Figure 14-1410. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4235. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4235. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1411 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_led2vbus_main_0.vbusp region 0 ISC.

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Table 14-4236. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1410h**

Figure 14-1411. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4238. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1412 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_led2vbus_main_0.vbusp region 0 ISC.

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Table 14-4239. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1414h**

Figure 14-1412. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4241. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1413 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator lk3_led2vbus_main_0.vbusp region 0 ISC.

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Table 14-4242. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1418h**

Figure 14-1413. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4244. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1414 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_led2vbus_main_0.vbusp region 0 ISC.

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Table 14-4245. Instance Table

Instance Name	Physical Address
CBASS0	**4582 141Ch**

Figure 14-1414. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4247. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1415 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register (Offset = 1420h) [reset = 10B04Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_led2vbus_main_0.vbusp region 1 ISC.

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Table 14-4248. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1420h**

Figure 14-1415. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B0h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4250. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4250. CBASS_ISC_IK3_LED2VBUS_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B0h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1416 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register (Offset = 1800h) [reset = B100h]

The ISC Region 0 Control Register defines the control fields for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-4251. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1800h**

Figure 14-1416. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4253. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4253. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B1h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1417 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-4254. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1810h**

Figure 14-1417. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4256. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1418 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-4257. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1814h**

Figure 14-1418. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4259. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1419 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-4260. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1818h**

Figure 14-1419. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4262. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1420 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register (Offset = 181Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-4263. Instance Table

Instance Name	Physical Address
CBASS0	**4582 181Ch**

Figure 14-1420. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4265. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1421 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register (Offset = 1820h) [reset = B14Ah]

The ISC Default Region Control Register defines the control fields for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw region 1 ISC.

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Table 14-4266. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1820h**

Figure 14-1421. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4268. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4268. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B1h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1422 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register (Offset = 1C00h) [reset = B100h]

The ISC Region 0 Control Register defines the control fields for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-4269. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C00h**

Figure 14-1422. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4271. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4271. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B1h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1423 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-4272. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C10h**

Figure 14-1423. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4274. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1424 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-4275. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C14h**

Figure 14-1424. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4277. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1425 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-4278. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C18h**

Figure 14-1425. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4280. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1426 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-4281. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C1Ch**

Figure 14-1426. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4283. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1427 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register (Offset = 1C20h) [reset = B14Ah]

The ISC Default Region Control Register defines the control fields for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr region 1 ISC.

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Table 14-4284. Instance Table

Instance Name	Physical Address
CBASS0	**4582 1C20h**

Figure 14-1427. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4286. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4286. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B1h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1428 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 2000h) [reset = 9A00h]

The ISC Region 0 Control Register defines the control fields for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-4287. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2000h**

Figure 14-1428. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ah							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4289. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4289. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ah	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1429 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-4290. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2010h**

Figure 14-1429. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4292. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1430 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-4293. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2014h**

Figure 14-1430. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4295. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1431 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-4296. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2018h**

Figure 14-1431. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4298. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1432 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-4299. Instance Table

Instance Name	Physical Address
CBASS0	**4582 201Ch**

Figure 14-1432. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4301. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1433 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 2020h) [reset = 9A4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm region 1 ISC.

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Table 14-4302. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2020h**

Figure 14-1433. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ah							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4304. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4304. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ah	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1434 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 2400h) [reset = 9A00h]

The ISC Region 0 Control Register defines the control fields for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-4305. Instance Table

Instance Name	Physical Address
CBASS0	4582 2400h

Figure 14-1434. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ah							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4307. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4307. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ah	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1435 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-4308. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2410h**

Figure 14-1435. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4310. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1436 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-4311. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2414h**

Figure 14-1436. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4313. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1437 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-4314. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2418h**

Figure 14-1437. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4316. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1438 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-4317. Instance Table

Instance Name	Physical Address
CBASS0	**4582 241Ch**

Figure 14-1438. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4319. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1439 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 2420h) [reset = 9A4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm region 1 ISC.

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Table 14-4320. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2420h**

Figure 14-1439. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Ah							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4322. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4322. CBASS_ISC_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ah	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1440 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register (Offset = 2800h) [reset = 108000h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4323. Instance Table

Instance Name	Physical Address
CBASS0	4582 2800h

Figure 14-1440. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
80h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4325. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4325. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	80h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1441 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4326. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2810h**

Figure 14-1441. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4328. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1442 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4329. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2814h**

Figure 14-1442. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4331. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1443 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4332. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2818h**

Figure 14-1443. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4334. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1444 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 281Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4335. Instance Table

Instance Name	Physical Address
CBASS0	**4582 281Ch**

Figure 14-1444. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4337. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1445 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register (Offset = 2820h) [reset = 10804Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd8ss_main_0.emmcsdss_rd region 1 ISC.

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Table 14-4338. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2820h**

Figure 14-1445. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
80h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4340. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4340. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	80h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1446 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register (Offset = 2C00h) [reset = 108000h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4341. Instance Table

Instance Name	Physical Address
CBASS0	4582 2C00h

Figure 14-1446. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
80h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4343. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4343. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	80h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1447 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4344. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2C10h**

Figure 14-1447. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4346. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1448 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4347. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2C14h**

Figure 14-1448. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4349. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1449 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4350. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2C18h**

Figure 14-1449. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4352. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1450 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 2C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4353. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2C1Ch**

Figure 14-1450. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4355. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1451 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register (Offset = 2C20h) [reset = 10804Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd8ss_main_0.emmcsdss_wr region 1 ISC.

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Table 14-4356. Instance Table

Instance Name	Physical Address
CBASS0	**4582 2C20h**

Figure 14-1451. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
80h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4358. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4358. CBASS_ISC_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	80h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1452 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register (Offset = 3000h) [reset = 108100h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4359. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3000h**

Figure 14-1452. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
81h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4361. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4361. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	81h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1453 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 3010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4362. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3010h**

Figure 14-1453. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4364. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1454 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 3014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4365. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3014h**

Figure 14-1454. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4367. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1455 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 3018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4368. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3018h**

Figure 14-1455. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4370. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1456 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 301Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-4371. Instance Table

Instance Name	Physical Address
CBASS0	**4582 301Ch**

Figure 14-1456. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4373. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1457 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register (Offset = 3020h) [reset = 10814Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd4ss_main_0.emmcsdss_rd region 1 ISC.

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Table 14-4374. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3020h**

Figure 14-1457. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
81h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4376. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4376. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	81h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1458 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register (Offset = 3400h) [reset = 108100h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4377. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3400h**

Figure 14-1458. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
81h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4379. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4379. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	81h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1459 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 3410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4380. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3410h**

Figure 14-1459. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4382. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1460 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 3414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4383. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3414h**

Figure 14-1460. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4385. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1461 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 3418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4386. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3418h**

Figure 14-1461. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4388. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1462 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 341Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-4389. Instance Table

Instance Name	Physical Address
CBASS0	**4582 341Ch**

Figure 14-1462. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4391. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1463 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register (Offset = 3420h) [reset = 10814Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd4ss_main_0.emmcsdss_wr region 1 ISC.

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Table 14-4392. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3420h**

Figure 14-1463. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
81h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4394. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4394. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	81h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1464 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register (Offset = 3800h) [reset = 108200h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 0 ISC.

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Table 14-4395. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3800h**

Figure 14-1464. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
82h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4397. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4397. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	82h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1465 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 3810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 0 ISC.

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Table 14-4398. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3810h**

Figure 14-1465. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4400. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1466 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 3814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 0 ISC.

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Table 14-4401. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3814h**

Figure 14-1466. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4403. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1467 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 3818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 0 ISC.

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Table 14-4404. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3818h**

Figure 14-1467. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4406. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1468 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 381Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 0 ISC.

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Table 14-4407. Instance Table

Instance Name	Physical Address
CBASS0	**4582 381Ch**

Figure 14-1468. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4409. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1469 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register (Offset = 3820h) [reset = 10824Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd4ss_main_1.emmcsdss_wr region 1 ISC.

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Table 14-4410. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3820h**

Figure 14-1469. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
82h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4412. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4412. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	82h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1470 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register (Offset = 3C00h) [reset = 108200h]

The ISC Region 0 Control Register defines the control fields for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 0 ISC.

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Table 14-4413. Instance Table

Instance Name	Physical Address
CBASS0	4582 3C00h

Figure 14-1470. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
82h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4415. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4415. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	82h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1471 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 3C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 0 ISC.

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Table 14-4416. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3C10h**

Figure 14-1471. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4418. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1472 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 3C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 0 ISC.

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Table 14-4419. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3C14h**

Figure 14-1472. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4421. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1473 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 3C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 0 ISC.

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Table 14-4422. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3C18h**

Figure 14-1473. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4424. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1474 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 3C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 0 ISC.

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Table 14-4425. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3C1Ch**

Figure 14-1474. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4427. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1475 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register (Offset = 3C20h) [reset = 10824Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iemmcsd4ss_main_1.emmcsdss_rd region 1 ISC.

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Table 14-4428. Instance Table

Instance Name	Physical Address
CBASS0	**4582 3C20h**

Figure 14-1475. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
82h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4430. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4430. CBASS_ISC_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	82h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1476 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register (Offset = 4000h) [reset = 109B00h]

The ISC Region 0 Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-4431. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4000h**

Figure 14-1476. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4433. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4433. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1477 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 4010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-4434. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 4010h**

Figure 14-1477. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4436. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1478 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 4014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-4437. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4014h**

Figure 14-1478. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-4439. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1479 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 4018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-4440. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4018h**

Figure 14-1479. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4442. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1480 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 401Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-4443. Instance Table

Instance Name	Physical Address
CBASS0	**4582 401Ch**

Figure 14-1480. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4445. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1481 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register (Offset = 4020h) [reset = 109B4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-4446. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 4020h**

Figure 14-1481. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4448. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4448. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Bh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1482 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register (Offset = 4400h) [reset = 109B00h]

The ISC Region 0 Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-4449. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4400h**

Figure 14-1482. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4451. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4451. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1483 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 4410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-4452. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 4410h**

Figure 14-1483. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4454. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1484 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 4414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-4455. Instance Table

Instance Name	Physical Address
CBASS0	4582 4414h

Figure 14-1484. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4457. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1485 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 4418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-4458. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4418h**

Figure 14-1485. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4460. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1486 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 441Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-4461. Instance Table

Instance Name	Physical Address
CBASS0	**4582 441Ch**

Figure 14-1486. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4463. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1487 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register (Offset = 4420h) [reset = 109B4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-4464. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 4420h**

Figure 14-1487. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4466. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4466. CBASS_ISC_IUSB2SS_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Bh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1488 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL Register (Offset = 4800h) [reset = 109C00h]

The ISC Region 0 Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_1.mstr0 region 0 ISC.

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Table 14-4467. Instance Table

Instance Name	Physical Address
CBASS0	4582 4800h

Figure 14-1488. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ch							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4469. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4469. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ch	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1489 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 4810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_1.mstr0 region 0 ISC.

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Table 14-4470. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4810h**

Figure 14-1489. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4472. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1490 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 4814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_1.mstr0 region 0 ISC.

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Table 14-4473. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4814h**

Figure 14-1490. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4475. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1491 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 4818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_1.mstr0 region 0 ISC.

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Table 14-4476. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4818h**

Figure 14-1491. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4478. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1492 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 481Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_1.mstr0 region 0 ISC.

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Table 14-4479. Instance Table

Instance Name	Physical Address
CBASS0	**4582 481Ch**

Figure 14-1492. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4481. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1493 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL Register (Offset = 4820h) [reset = 109C4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_1.mstr0 region 1 ISC.

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Table 14-4482. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4820h**

Figure 14-1493. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ch							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4484. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4484. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ch	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1494 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL Register (Offset = 4C00h) [reset = 109C00h]

The ISC Region 0 Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_1.mstw0 region 0 ISC.

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Table 14-4485. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4C00h**

Figure 14-1494. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4487. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4487. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ch	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1495 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 4C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_1.mstw0 region 0 ISC.

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Table 14-4488. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4C10h**

Figure 14-1495. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4490. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1496 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 4C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_1.mstw0 region 0 ISC.

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Table 14-4491. Instance Table

Instance Name	Physical Address
CBASS0	4582 4C14h

Figure 14-1496. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4493. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1497 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 4C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iusb2ss_16ffc_main_1.mstw0 region 0 ISC.

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Table 14-4494. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4C18h**

Figure 14-1497. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4496. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1498 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 4C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iusb2ss_16ffc_main_1.mstw0 region 0 ISC.

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Table 14-4497. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4C1Ch**

Figure 14-1498. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4499. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1499 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL Register (Offset = 4C20h) [reset = 109C4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iusb2ss_16ffc_main_1.mstw0 region 1 ISC.

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Table 14-4500. Instance Table

Instance Name	Physical Address
CBASS0	**4582 4C20h**

Figure 14-1499. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ch							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4502. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4502. CBASS_ISC_IUSB2SS_16FFC_MAIN_1_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ch	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1500 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL Register (Offset = 5000h) [reset = 10AD00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_dss_ul_main_0.vbusm_dma region 0 ISC.

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Table 14-4503. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5000h**

Figure 14-1500. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
ADh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4505. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4505. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	ADh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1501 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 0 ISC.

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Table 14-4506. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5010h**

Figure 14-1501. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4508. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1502 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 0 ISC.

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Table 14-4509. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5014h**

Figure 14-1502. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4511. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1503 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 0 ISC.

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Table 14-4512. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5018h**

Figure 14-1503. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4514. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1504 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_H Register (Offset = 501Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 0 ISC.

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Table 14-4515. Instance Table

Instance Name	Physical Address
CBASS0	**4582 501Ch**

Figure 14-1504. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-4517. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1505 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL Register (Offset = 5020h) [reset = 10AD00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ik3_dss_ul_main_0.vbusm_dma region 1 ISC.

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Table 14-4518. Instance Table

Instance Name	Physical Address
CBASS0	4582 5020h

Figure 14-1505. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
ADh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4520. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4520. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	ADh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1506 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_L Register (Offset = 5030h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 1 ISC.

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Table 14-4521. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5030h**

Figure 14-1506. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4523. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1507 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_H Register (Offset = 5034h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 1 ISC.

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Table 14-4524. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5034h**

Figure 14-1507. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4526. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1508 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_L Register (Offset = 5038h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 1 ISC.

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Table 14-4527. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5038h**

Figure 14-1508. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4529. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1509 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_H Register (Offset = 503Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 1 ISC.

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Table 14-4530. Instance Table

Instance Name	Physical Address
CBASS0	4582 503Ch

Figure 14-1509. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4532. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1510 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL Register (Offset = 5040h) [reset = 10AD00h]

The ISC Region 2 Control Register defines the control fields for the initiator Ik3_dss_ul_main_0.vbusm_dma region 2 ISC.

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Table 14-4533. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5040h**

Figure 14-1510. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
ADh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4535. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4535. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	ADh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1511 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_L Register (Offset = 5050h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 2 ISC.

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Table 14-4536. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5050h**

Figure 14-1511. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4538. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1512 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_H Register (Offset = 5054h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 2 ISC.

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Table 14-4539. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 5054h**

Figure 14-1512. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4541. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1513 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_L Register (Offset = 5058h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 2 ISC.

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Table 14-4542. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5058h**

Figure 14-1513. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4544. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1514 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_H Register (Offset = 505Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 2 ISC.

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Table 14-4545. Instance Table

Instance Name	Physical Address
CBASS0	4582 505Ch

Figure 14-1514. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4547. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1515 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL Register (Offset = 5060h) [reset = 10AD00h]

The ISC Region 3 Control Register defines the control fields for the initiator Ik3_dss_ul_main_0.vbusm_dma region 3 ISC.

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Table 14-4548. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5060h**

Figure 14-1515. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
ADh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4550. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4550. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	ADh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1516 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_L Register (Offset = 5070h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 3 ISC.

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Table 14-4551. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5070h**

Figure 14-1516. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4553. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1517 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_H Register (Offset = 5074h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 3 ISC.

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Table 14-4554. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5074h**

Figure 14-1517. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4556. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1518 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_L Register (Offset = 5078h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 3 ISC.

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Table 14-4557. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5078h**

Figure 14-1518. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4559. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1519 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_H Register (Offset = 507Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_dss_ul_main_0.vbusm_dma region 3 ISC.

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Table 14-4560. Instance Table

Instance Name	Physical Address
CBASS0	**4582 507Ch**

Figure 14-1519. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4562. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1520 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL Register (Offset = 5080h) [reset = 10AD4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_dss_ul_main_0.vbusm_dma region 4 ISC.

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Table 14-4563. Instance Table

Instance Name	Physical Address
CBASS0	4582 5080h

Figure 14-1520. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
ADh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4565. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4565. CBASS_ISC_IK3_DSS_UL_MAIN_0_VBUSM_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	ADh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1521 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register (Offset = 5400h) [reset = 109800h]

The ISC Region 0 Control Register defines the control fields for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-4566. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5400h**

Figure 14-1521. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
98h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4568. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4568. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	98h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1522 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-4569. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5410h**

Figure 14-1522. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4571. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1523 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-4572. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5414h**

Figure 14-1523. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4574. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1524 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-4575. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5418h**

Figure 14-1524. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4577. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1525 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register (Offset = 541Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-4578. Instance Table

Instance Name	Physical Address
CBASS0	**4582 541Ch**

Figure 14-1525. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4580. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1526 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register (Offset = 5420h) [reset = 10984Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma region 1 ISC.

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Table 14-4581. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5420h**

Figure 14-1526. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
98h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4583. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4583. CBASS_ISC_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	98h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1527 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL Register (Offset = 5800h) [reset = 10BE00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 0 ISC.

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Table 14-4584. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5800h**

Figure 14-1527. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BEh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4586. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4586. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	BEh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1528 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 0 ISC.

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Table 14-4587. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5810h**

Figure 14-1528. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4589. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1529 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 0 ISC.

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Table 14-4590. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5814h**

Figure 14-1529. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4592. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1530 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 0 ISC.

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Table 14-4593. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5818h**

Figure 14-1530. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4595. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1531 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_H Register (Offset = 581Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 0 ISC.

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Table 14-4596. Instance Table

Instance Name	Physical Address
CBASS0	**4582 581Ch**

Figure 14-1531. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4598. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1532 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL Register (Offset = 5820h) [reset = 10BE4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w region 1 ISC.

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Table 14-4599. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5820h**

Figure 14-1532. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BEh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4601. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4601. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BEh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1533 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL Register (Offset = 5C00h) [reset = 10BE00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 0 ISC.

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Table 14-4602. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C00h**

Figure 14-1533. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BEh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4604. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4604. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	BEh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1534 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 0 ISC.

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Table 14-4605. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C10h**

Figure 14-1534. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4607. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1535 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 0 ISC.

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Table 14-4608. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C14h**

Figure 14-1535. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4610. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1536 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 0 ISC.

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Table 14-4611. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C18h**

Figure 14-1536. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4613. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1537 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_H Register (Offset = 5C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 0 ISC.

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Table 14-4614. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C1Ch**

Figure 14-1537. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4616. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1538 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL Register (Offset = 5C20h) [reset = 10BE00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 1 ISC.

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Table 14-4617. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C20h**

Figure 14-1538. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BEh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4619. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4619. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	BEh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1539 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_L Register (Offset = 5C30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 1 ISC.

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Table 14-4620. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C30h**

Figure 14-1539. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4622. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1540 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_H Register (Offset = 5C34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 1 ISC.

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Table 14-4623. Instance Table

Instance Name	Physical Address
CBASS0	4582 5C34h

Figure 14-1540. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4625. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1541 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_L Register (Offset = 5C38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 1 ISC.

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Table 14-4626. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C38h**

Figure 14-1541. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4628. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1542 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_H Register (Offset = 5C3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 1 ISC.

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Table 14-4629. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C3Ch**

Figure 14-1542. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4631. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1543 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL Register (Offset = 5C40h) [reset = 10BE4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r region 2 ISC.

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Table 14-4632. Instance Table

Instance Name	Physical Address
CBASS0	**4582 5C40h**

Figure 14-1543. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BEh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4634. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4634. CBASS_ISC_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BEh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1544 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL Register (Offset = 6000h) [reset = 106500h]

The ISC Region 0 Control Register defines the control fields for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 0 ISC.

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Table 14-4635. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6000h**

Figure 14-1544. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
65h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4637. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4637. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	65h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1545 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 0 ISC.

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Table 14-4638. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6010h**

Figure 14-1545. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4640. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1546 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 0 ISC.

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Table 14-4641. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6014h**

Figure 14-1546. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4643. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1547 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 0 ISC.

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Table 14-4644. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6018h**

Figure 14-1547. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4646. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1548 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 601Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 0 ISC.

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Table 14-4647. Instance Table

Instance Name	Physical Address
CBASS0	**4582 601Ch**

Figure 14-1548. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4649. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1549 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL Register (Offset = 6020h) [reset = 10654Ah]

The ISC Default Region Control Register defines the control fields for the initiator Idmss_csi_am62a_main_0.bcdma_memr region 1 ISC.

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Table 14-4650. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6020h**

Figure 14-1549. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
65h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4652. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4652. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	65h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1550 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL Register (Offset = 6400h) [reset = 106500h]

The ISC Region 0 Control Register defines the control fields for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 0 ISC.

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Table 14-4653. Instance Table

Instance Name	Physical Address
CBASS0	4582 6400h

Figure 14-1550. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
65h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4655. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4655. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	65h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1551 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 0 ISC.

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Table 14-4656. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6410h**

Figure 14-1551. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4658. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1552 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 0 ISC.

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Table 14-4659. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6414h**

Figure 14-1552. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4661. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1553 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 0 ISC.

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Table 14-4662. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6418h**

Figure 14-1553. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4664. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1554 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_H Register (Offset = 641Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 0 ISC.

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Table 14-4665. Instance Table

Instance Name	Physical Address
CBASS0	**4582 641Ch**

Figure 14-1554. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4667. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1555 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL Register (Offset = 6420h) [reset = 10654Ah]

The ISC Default Region Control Register defines the control fields for the initiator Idmss_csi_am62a_main_0.bcdma_memw region 1 ISC.

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Table 14-4668. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6420h**

Figure 14-1555. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
65h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4670. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4670. CBASS_ISC_IDMSS_CSI_AM62A_MAIN_0_BCDMA_MEMW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	65h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1556 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register (Offset = 6800h) [reset = 10BF00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 0 ISC.

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Table 14-4671. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6800h**

Figure 14-1556. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4673. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4673. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1557 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 0 ISC.

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Table 14-4674. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6810h**

Figure 14-1557. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4676. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1558 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 0 ISC.

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Table 14-4677. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6814h**

Figure 14-1558. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4679. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1559 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 0 ISC.

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Table 14-4680. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6818h**

Figure 14-1559. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4682. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1560 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 681Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 0 ISC.

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Table 14-4683. Instance Table

Instance Name	Physical Address
CBASS0	**4582 681Ch**

Figure 14-1560. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4685. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1561 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL Register (Offset = 6820h) [reset = 10BF00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 1 ISC.

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Table 14-4686. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6820h**

Figure 14-1561. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BFh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4688. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4688. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1562 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_L Register (Offset = 6830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 1 ISC.

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Table 14-4689. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6830h**

Figure 14-1562. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4691. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1563 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_H Register (Offset = 6834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 1 ISC.

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Table 14-4692. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6834h**

Figure 14-1563. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4694. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1564 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_L Register (Offset = 6838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 1 ISC.

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Table 14-4695. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6838h**

Figure 14-1564. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4697. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1565
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_H Register (Offset = 683Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 1 ISC.

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Table 14-4698. Instance Table

Instance Name	Physical Address
CBASS0	4582 683Ch

Figure 14-1565. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4700. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1566 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL Register (Offset = 6840h) [reset = 10BF00h]

The ISC Region 2 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 2 ISC.

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Table 14-4701. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6840h**

Figure 14-1566. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4703. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4703. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1567 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_L Register (Offset = 6850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 2 ISC.

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Table 14-4704. Instance Table

Instance Name	Physical Address
CBASS0	4582 6850h

Figure 14-1567. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4706. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1568 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_H Register (Offset = 6854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 2 ISC.

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Table 14-4707. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6854h**

Figure 14-1568. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4709. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1569 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_L Register (Offset = 6858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 2 ISC.

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Table 14-4710. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6858h**

Figure 14-1569. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4712. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1570
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_H Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_H Register (Offset = 685Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 2 ISC.

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Table 14-4713. Instance Table

Instance Name	Physical Address
CBASS0	**4582 685Ch**

Figure 14-1570. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4715. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1571 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL Register (Offset = 6860h) [reset = 10BF00h]

The ISC Region 3 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 3 ISC.

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Table 14-4716. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6860h**

Figure 14-1571. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4718. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4718. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1572 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_L Register (Offset = 6870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 3 ISC.

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Table 14-4719. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6870h**

Figure 14-1572. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4721. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1573 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_H Register (Offset = 6874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 3 ISC.

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Table 14-4722. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6874h**

Figure 14-1573. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4724. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1574 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_L Register (Offset = 6878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 3 ISC.

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Table 14-4725. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6878h**

Figure 14-1574. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4727. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1575 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_H Register (Offset = 687Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 3 ISC.

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Table 14-4728. Instance Table

Instance Name	Physical Address
CBASS0	**4582 687Ch**

Figure 14-1575. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4730. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1576 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL Register (Offset = 6880h) [reset = 10BF00h]

The ISC Region 4 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 4 ISC.

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Table 14-4731. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 6880h**

Figure 14-1576. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">BFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4733. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4733. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1577 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_L Register (Offset = 6890h) [reset = 0h]

The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 4 ISC.

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Table 14-4734. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6890h**

Figure 14-1577. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4736. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1578
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_H Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_H Register (Offset = 6894h) [reset = 0h]

The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 4 ISC.

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Table 14-4737. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6894h**

Figure 14-1578. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4739. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1579 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_L Register (Offset = 6898h) [reset = FFFh]

The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 4 ISC.

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Table 14-4740. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6898h**

Figure 14-1579. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4742. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1580
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_H Register (Offset = 689Ch) [reset = 0h]

The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 4 ISC.

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Table 14-4743. Instance Table

Instance Name	Physical Address
CBASS0	**4582 689Ch**

Figure 14-1580. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4745. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1581 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register (Offset = 68A0h) [reset = 10BF4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async region 5 ISC.

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Table 14-4746. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 68A0h**

Figure 14-1581. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4748. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4748. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1582 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register (Offset = 6C00h) [reset = 10BF00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 0 ISC.

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Table 14-4749. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C00h**

Figure 14-1582. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BFh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4751. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4751. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1583 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 0 ISC.

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Table 14-4752. Instance Table

Instance Name	**Physical Address**
CBASS0	**4582 6C10h**

Figure 14-1583. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4754. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1584 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 0 ISC.

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Table 14-4755. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C14h**

Figure 14-1584. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4757. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1585
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 0 ISC.

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Table 14-4758. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C18h**

Figure 14-1585. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4760. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1586 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 6C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 0 ISC.

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Table 14-4761. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C1Ch**

Figure 14-1586. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4763. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1587 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL Register (Offset = 6C20h) [reset = 10BF00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 1 ISC.

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Table 14-4764. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C20h**

Figure 14-1587. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4766. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4766. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1588
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_L Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_L Register (Offset = 6C30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 1 ISC.

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Table 14-4767. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C30h**

Figure 14-1588. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4769. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1589
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_H Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_H Register (Offset = 6C34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 1 ISC.

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Table 14-4770. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C34h**

Figure 14-1589. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4772. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1590 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_L Register (Offset = 6C38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 1 ISC.

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Table 14-4773. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C38h**

Figure 14-1590. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4775. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1591 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_H Register (Offset = 6C3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 1 ISC.

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Table 14-4776. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C3Ch**

Figure 14-1591. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4778. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1592 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL Register (Offset = 6C40h) [reset = 10BF00h]

The ISC Region 2 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 2 ISC.

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Table 14-4779. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C40h**

Figure 14-1592. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4781. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4781. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1593 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_L Register (Offset = 6C50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 2 ISC.

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Table 14-4782. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C50h**

Figure 14-1593. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4784. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1594 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_H Register (Offset = 6C54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 2 ISC.

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Table 14-4785. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C54h**

Figure 14-1594. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4787. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1595 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_L Register (Offset = 6C58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 2 ISC.

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Table 14-4788. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C58h**

Figure 14-1595. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4790. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1596 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_H Register (Offset = 6C5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 2 ISC.

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Table 14-4791. Instance Table

Instance Name	Physical Address
CBASS0	4582 6C5Ch

Figure 14-1596. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4793. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1597 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL Register (Offset = 6C60h) [reset = 10BF00h]

The ISC Region 3 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 3 ISC.

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Table 14-4794. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C60h**

Figure 14-1597. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4796. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4796. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1598 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_L Register (Offset = 6C70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 3 ISC.

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Table 14-4797. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C70h**

Figure 14-1598. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4799. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1599 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_H Register (Offset = 6C74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 3 ISC.

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Table 14-4800. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C74h**

Figure 14-1599. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4802. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1600 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_L Register (Offset = 6C78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 3 ISC.

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Table 14-4803. Instance Table

Instance Name	Physical Address
CBASS0	4582 6C78h

Figure 14-1600. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4805. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1601 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_H Register (Offset = 6C7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 3 ISC.

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Table 14-4806. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C7Ch**

Figure 14-1601. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4808. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1602 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL Register (Offset = 6C80h) [reset = 10BF00h]

The ISC Region 4 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 4 ISC.

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Table 14-4809. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C80h**

Figure 14-1602. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BFh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4811. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4811. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1603
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_L Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_L Register (Offset = 6C90h) [reset = 0h]

The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 4 ISC.

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Table 14-4812. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C90h**

Figure 14-1603. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4814. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1604 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_H Register (Offset = 6C94h) [reset = 0h]

The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 4 ISC.

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Table 14-4815. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C94h**

Figure 14-1604. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4817. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1605 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_L Register (Offset = 6C98h) [reset = FFFh]

The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 4 ISC.

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Table 14-4818. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C98h**

Figure 14-1605. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4820. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1606 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_H Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_H Register (Offset = 6C9Ch) [reset = 0h]

The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 4 ISC.

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Table 14-4821. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6C9Ch**

Figure 14-1606. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4823. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1607 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register (Offset = 6CA0h) [reset = 10BF4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async region 5 ISC.

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Table 14-4824. Instance Table

Instance Name	Physical Address
CBASS0	**4582 6CA0h**

Figure 14-1607. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4826. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4826. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1608 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register (Offset = 7000h) [reset = 10BF00h]

The ISC Region 0 Control Register defines the control fields for the initiator lk3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 0 ISC.

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Table 14-4827. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7000h**

Figure 14-1608. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4829. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4829. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1609 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 0 ISC.

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Table 14-4830. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7010h**

Figure 14-1609. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4832. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1610 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 0 ISC.

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Table 14-4833. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7014h**

Figure 14-1610. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4835. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1611 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 0 ISC.

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Table 14-4836. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7018h**

Figure 14-1611. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4838. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1612 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 701Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 0 ISC.

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Table 14-4839. Instance Table

Instance Name	Physical Address
CBASS0	**4582 701Ch**

Figure 14-1612. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4841. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1613
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register (Offset = 7020h) [reset = 10BF4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async region 1 ISC.

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Table 14-4842. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7020h**

Figure 14-1613. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">BFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-4844. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4844. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1614 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register (Offset = 7400h) [reset = 10BF00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 0 ISC.

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Table 14-4845. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7400h**

Figure 14-1614. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
BFh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4847. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4847. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1615 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 0 ISC.

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Table 14-4848. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7410h**

Figure 14-1615. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4850. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1616 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 0 ISC.

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Table 14-4851. Instance Table

Instance Name	Physical Address
CBASS0	4582 7414h

Figure 14-1616. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4853. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1617 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register

1

CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 0 ISC.

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Table 14-4854. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7418h**

Figure 14-1617. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4856. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1618
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register

1
CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 741Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 0 ISC.

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Table 14-4857. Instance Table

Instance Name	Physical Address
CBASS0	**4582 741Ch**

Figure 14-1618. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-4859. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1619 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register (Offset = 7420h) [reset = 10BF4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async region 1 ISC.

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Table 14-4860. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7420h**

Figure 14-1619. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
BFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4862. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4862. CBASS_ISC_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	BFh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1620 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register (Offset = 7800h) [reset = 102000h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 0 ISC.

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Table 14-4863. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7800h**

Figure 14-1620. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
20h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4865. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4865. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	20h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1621 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 0 ISC.

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Table 14-4866. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7810h**

Figure 14-1621. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4868. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1622 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 0 ISC.

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Table 14-4869. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7814h**

Figure 14-1622. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4871. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1623 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 0 ISC.

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Table 14-4872. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7818h**

Figure 14-1623. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4874. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1624 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 781Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 0 ISC.

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Table 14-4875. Instance Table

Instance Name	Physical Address
CBASS0	**4582 781Ch**

Figure 14-1624. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4877. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1625 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register (Offset = 7820h) [reset = 102000h]

The ISC Region 1 Control Register defines the control fields for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 1 ISC.

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Table 14-4878. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7820h**

Figure 14-1625. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4880. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4880. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	20h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1626 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register (Offset = 7830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 1 ISC.

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Table 14-4881. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7830h**

Figure 14-1626. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4883. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1627 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register (Offset = 7834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 1 ISC.

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Table 14-4884. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7834h**

Figure 14-1627. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4886. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1628 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register (Offset = 7838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 1 ISC.

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Table 14-4887. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7838h**

Figure 14-1628. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4889. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1629 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register (Offset = 783Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 1 ISC.

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Table 14-4890. Instance Table

Instance Name	Physical Address
CBASS0	**4582 783Ch**

Figure 14-1629. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4892. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1630 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register (Offset = 7840h) [reset = 10204Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc region 2 ISC.

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Table 14-4893. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7840h**

Figure 14-1630. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-4895. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4895. CBASS_ISC_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	20h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1631 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL Register (Offset = 7C00h) [reset = 106600h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 0 ISC.

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Table 14-4896. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C00h**

Figure 14-1631. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
66h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4898. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4898. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	66h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1632 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 0 ISC.

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Table 14-4899. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C10h**

Figure 14-1632. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4901. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1633 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 0 ISC.

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Table 14-4902. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C14h**

Figure 14-1633. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4904. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1634 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 0 ISC.

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Table 14-4905. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C18h**

Figure 14-1634. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4907. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1635 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 7C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 0 ISC.

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Table 14-4908. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C1Ch**

Figure 14-1635. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4910. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1636 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL Register (Offset = 7C20h) [reset = 10664Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.data_mst_0 region 1 ISC.

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Table 14-4911. Instance Table

Instance Name	Physical Address
CBASS0	**4582 7C20h**

Figure 14-1636. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
66h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4913. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4913. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	66h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1637 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL Register (Offset = 8000h) [reset = 106800h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 0 ISC.

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Table 14-4914. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8000h**

Figure 14-1637. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
68h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4916. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4916. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	68h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1638 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 0 ISC.

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Table 14-4917. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8010h**

Figure 14-1638. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4919. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1639 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 0 ISC.

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Table 14-4920. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8014h**

Figure 14-1639. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4922. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1640 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 0 ISC.

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Table 14-4923. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8018h**

Figure 14-1640. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4925. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1641 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 801Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 0 ISC.

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Table 14-4926. Instance Table

Instance Name	Physical Address
CBASS0	**4582 801Ch**

Figure 14-1641. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4928. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1642 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL Register (Offset = 8020h) [reset = 10684Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst region 1 ISC.

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Table 14-4929. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8020h**

Figure 14-1642. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
68h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4931. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4931. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	68h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1643 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL Register (Offset = 8400h) [reset = 106700h]

The ISC Region 0 Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 0 ISC.

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Table 14-4932. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8400h**

Figure 14-1643. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
67h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4934. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4934. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	67h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1644 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 0 ISC.

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Table 14-4935. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8410h**

Figure 14-1644. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4937. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1645 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 0 ISC.

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Table 14-4938. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8414h**

Figure 14-1645. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4940. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1646 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 0 ISC.

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Table 14-4941. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8418h**

Figure 14-1646. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4943. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1647 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_H Register (Offset = 841Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 0 ISC.

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Table 14-4944. Instance Table

Instance Name	Physical Address
CBASS0	**4582 841Ch**

Figure 14-1647. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4946. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1648 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL Register (Offset = 8420h) [reset = 10674Ah]

The ISC Default Region Control Register defines the control fields for the initiator Isam62a_vpac_wrap_main_0.data_mst_1 region 1 ISC.

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Table 14-4947. Instance Table

Instance Name	Physical Address
CBASS0	**4582 8420h**

Figure 14-1648. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
67h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4949. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4949. CBASS_ISC_ISAM62A_VPAC_WRAP_MAIN_0_DATA_MST_1_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	67h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1649 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-4950. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8000h**

Figure 14-1649. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-4952. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1650 CBASS_GLB_DESTINATION_ID Register

1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-4953. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8004h**

Figure 14-1650. CBASS_GLB_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4955. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1651 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-4956. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8020h**

Figure 14-1651. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-4958. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1652 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-4959. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8024h**

Figure 14-1652. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-4961. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1653 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-4962. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8028h**

Figure 14-1653. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4964. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.2.1654 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-4965. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 802Ch**

Figure 14-1654. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4967. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1655 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-4968. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8030h**

Figure 14-1655. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-4970. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1656 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-4971. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8034h**

Figure 14-1656. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4973. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4973. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1657 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-4974. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8038h**

Figure 14-1657. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-4976. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1658 CBASS_GLB_EXCEPTION_PEND_SET Register

1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-4977. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8040h**

Figure 14-1658. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-4979. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1659 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-4980. Instance Table

Instance Name	Physical Address
CBASS0	**45B0 8044h**

Figure 14-1659. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-4982. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1660 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1 Register

1

CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1 Register (Offset = 400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r for group slv_grp_0.

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Table 14-4983. Instance Table

Instance Name	Physical Address
CBASS0	45D2 0400h

Figure 14-1660. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-4985. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4985. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1661 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2 Register (Offset = 404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_r for group slv_grp_0.

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Table 14-4986. Instance Table

Instance Name	Physical Address
CBASS0	45D2 0404h

Figure 14-1661. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-4988. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4988. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1662 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0 Register

1 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0 Register (Offset = 500h) [reset = 7000h]

The Map Register defines the fields for the initiator A53SS0 Read Port per channel

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Table 14-4989. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 0500h**

Figure 14-1662. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-4991. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4991. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_R_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1663 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1 Register (Offset = 800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w for group slv_grp_0.

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Table 14-4992. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 0800h**

Figure 14-1663. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-4994. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4994. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1664 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2 Register (Offset = 804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_a53_512kb_wrap_main_0.a53_quad_wrap_cba_axi_w for group slv_grp_0.

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Table 14-4995. Instance Table

Instance Name	Physical Address
CBASS0	45D2 0804h

Figure 14-1664. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-4997. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4997. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1665 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0 Register

1 CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator A53SS0 Write Port per channel

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Table 14-4998. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 0900h**

Figure 14-1665. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5000. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5000. CBASS_QOS_ISAM62A_A53_512KB_WRAP_MAIN_0_A53_QUAD_WRAP_CBA_AXI_W_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1666 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1 Register (Offset = 1800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw for group slv_grp_0.

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Table 14-5001. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 1800h**

Figure 14-1666. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5003. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5003. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1667 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2 Register (Offset = 1804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmw for group slv_grp_0.

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Table 14-5004. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 1804h**

Figure 14-1667. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5006. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5006. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1668 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register (Offset = 1900h) [reset = 7000h]

The Map Register defines the fields for the initiator DEBUGSS0 Write Port per channel

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Table 14-5007. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 1900h**

Figure 14-1668. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5009. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5009. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1669 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1 Register (Offset = 1C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr for group slv_grp_0.

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Table 14-5010. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 1C00h**

Figure 14-1669. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5012. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5012. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1670 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2 Register (Offset = 1C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Idebugss_k3_wrap_cv0_main_0.vbusmr for group slv_grp_0.

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Table 14-5013. Instance Table

Instance Name	**Physical Address**
CBASS0	**45D2 1C04h**

Figure 14-1670. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5015. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5015. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1671 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register

1 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register (Offset = 1D00h) [reset = 7000h]

The Map Register defines the fields for the initiator DEBUGSS0 Read Port per channel

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Table 14-5016. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 1D00h**

Figure 14-1671. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5018. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5018. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1672 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1 Register (Offset = 2000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm for group slv_grp_0.

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Table 14-5019. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2000h**

Figure 14-1672. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5021. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5021. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1673 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2 Register (Offset = 2004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Igic500ss_1_4_main_0.mem_wr_vbusm for group slv_grp_0.

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Table 14-5022. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2004h**

Figure 14-1673. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5024. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5024. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1674 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0 Register (Offset = 2100h) [reset = 7000h]

The Map Register defines the fields for the initiator GICSS0 Write Port per channel

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Table 14-5025. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2100h**

Figure 14-1674. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5027. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5027. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_WR_VBUSM_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1675 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1 Register (Offset = 2400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm for group slv_grp_0.

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Table 14-5028. Instance Table

Instance Name	Physical Address
CBASS0	45D2 2400h

Figure 14-1675. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5030. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5030. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1676 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2 Register (Offset = 2404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Igic500ss_1_4_main_0.mem_rd_vbusm for group slv_grp_0.

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Table 14-5031. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2404h**

Figure 14-1676. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5033. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5033. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1677 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0 Register

1 CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0 Register (Offset = 2500h) [reset = 7000h]

The Map Register defines the fields for the initiator GICSS0 Read Port per channel

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Table 14-5034. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2500h**

Figure 14-1677. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5036. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5036. CBASS_QOS_IGIC500SS_1_4_MAIN_0_MEM_RD_VBUSM_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1678 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register (Offset = 2800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd8ss_main_0.emmcsdss_rd for group slv_grp_0.

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Table 14-5037. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2800h**

Figure 14-1678. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5039. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5039. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1679 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register (Offset = 2804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd8ss_main_0.emmcsdss_rd for group slv_grp_0.

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Table 14-5040. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2804h**

Figure 14-1679. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">ORDERID15</td><td colspan="4">ORDERID14</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">ORDERID13</td><td colspan="4">ORDERID12</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">ORDERID11</td><td colspan="4">ORDERID10</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID9</td><td colspan="4">ORDERID8</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5042. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5042. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1680 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_MAP0 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_MAP0 Register (Offset = 2900h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD0 Read Port per channel

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Table 14-5043. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2900h**

Figure 14-1680. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5045. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1681 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register (Offset = 2C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd8ss_main_0.emmcsdss_wr for group slv_grp_0.

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Table 14-5046. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2C00h**

Figure 14-1681. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5048. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5048. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1682 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register (Offset = 2C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd8ss_main_0.emmcsdss_wr for group slv_grp_0.

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Table 14-5049. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2C04h**

Figure 14-1682. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5051. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5051. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1683 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_MAP0 Register

1 CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_MAP0 Register (Offset = 2D00h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD0 Write Port per channel

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Table 14-5052. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 2D00h**

Figure 14-1683. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5054. CBASS_QOS_IEMMCSD8SS_MAIN_0_EMMCSDSS_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1684 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register (Offset = 3000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_0.emmcsdss_rd for group slv_grp_0.

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Table 14-5055. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3000h**

Figure 14-1684. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5057. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5057. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1685 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register (Offset = 3004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_0.emmcsdss_rd for group slv_grp_0.

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Table 14-5058. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3004h**

Figure 14-1685. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5060. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5060. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1686 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register (Offset = 3100h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD1 Read Port per channel

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Table 14-5061. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3100h**

Figure 14-1686. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5063. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1687 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register (Offset = 3400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_0.emmcsdss_wr for group slv_grp_0.

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Table 14-5064. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3400h**

Figure 14-1687. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5066. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5066. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1688 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register (Offset = 3404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_0.emmcsdss_wr for group slv_grp_0.

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Table 14-5067. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3404h**

Figure 14-1688. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5069. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5069. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1689 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register (Offset = 3500h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD1 Write Port per channel

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Table 14-5070. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3500h**

Figure 14-1689. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5072. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1690 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register (Offset = 3800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_1.emmcsdss_wr for group slv_grp_0.

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Table 14-5073. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3800h**

Figure 14-1690. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5075. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5075. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1691 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register (Offset = 3804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_1.emmcsdss_wr for group slv_grp_0.

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Table 14-5076. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3804h**

Figure 14-1691. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5078. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5078. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1692 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_MAP0 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_MAP0 Register (Offset = 3900h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD2 Write Port per channel

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Table 14-5079. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3900h**

Figure 14-1692. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5081. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1693 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register (Offset = 3C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_1.emmcsdss_rd for group slv_grp_0.

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Table 14-5082. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3C00h**

Figure 14-1693. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5084. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5084. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1694 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register (Offset = 3C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iemmcsd4ss_main_1.emmcsdss_rd for group slv_grp_0.

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Table 14-5085. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3C04h**

Figure 14-1694. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5087. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5087. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1695 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_MAP0 Register

1 CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_MAP0 Register (Offset = 3D00h) [reset = 7000h]

The Map Register defines the fields for the initiator MMCSD2 Read Port per channel

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Table 14-5088. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 3D00h**

Figure 14-1695. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5090. CBASS_QOS_IEMMCSD4SS_MAIN_1_EMMCSDSS_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1696 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1 Register (Offset = 4000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_0.mstw0 for group slv_grp_0.

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Table 14-5091. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4000h**

Figure 14-1696. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5093. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5093. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1697 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2 Register (Offset = 4004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_0.mstw0 for group slv_grp_0.

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Table 14-5094. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4004h**

Figure 14-1697. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5096. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5096. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1698 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_MAP0 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_MAP0 Register (Offset = 4100h) [reset = 7000h]

The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-5097. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4100h**

Figure 14-1698. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5099. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTW0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1699 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1 Register (Offset = 4400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_0.mstr0 for group slv_grp_0.

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Table 14-5100. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4400h**

Figure 14-1699. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5102. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5102. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1700 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2 Register (Offset = 4404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_0.mstr0 for group slv_grp_0.

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Table 14-5103. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4404h**

Figure 14-1700. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5105. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5105. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1701 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_MAP0 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_MAP0 Register (Offset = 4500h) [reset = 7000h]

The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-5106. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4500h**

Figure 14-1701. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5108. CBASS_QOS_IUSB2SS_16FFC_MAIN_0_MSTR0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1702 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1 Register (Offset = 4800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_1.mstr0 for group slv_grp_0.

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Table 14-5109. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4800h**

Figure 14-1702. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5111. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5111. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1703 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2 Register (Offset = 4804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_1.mstr0 for group slv_grp_0.

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Table 14-5112. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4804h**

Figure 14-1703. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5114. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5114. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1704 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_MAP0 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_MAP0 Register (Offset = 4900h) [reset = 7000h]

The Map Register defines the fields for the initiator USB1 Read Port per channel

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Table 14-5115. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4900h**

Figure 14-1704. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5117. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTR0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1705 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1 Register (Offset = 4C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_1.mstw0 for group slv_grp_0.

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Table 14-5118. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4C00h**

Figure 14-1705. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5120. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5120. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1706 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2 Register (Offset = 4C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Iusb2ss_16ffc_main_1.mstw0 for group slv_grp_0.

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Table 14-5121. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 4C04h**

Figure 14-1706. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5123. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5123. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1707 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_MAP0 Register

1 CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_MAP0 Register (Offset = 4D00h) [reset = 7000h]

The Map Register defines the fields for the initiator USB1 Write Port per channel

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Table 14-5124. Instance Table

Instance Name	Physical Address
CBASS0	45D2 4D00h

Figure 14-1707. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5126. CBASS_QOS_IUSB2SS_16FFC_MAIN_1_MSTW0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1708 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1 Register (Offset = 5000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_dss_ul_main_0.vbusm_dma for group slv_grp_0.

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Table 14-5127. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5000h**

Figure 14-1708. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5129. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5129. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1709 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2 Register (Offset = 5004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_dss_ul_main_0.vbusm_dma for group slv_grp_0.

Return to Summary Table

Table 14-5130. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5004h**

Figure 14-1709. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5132. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5132. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1710 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP0 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP0 Register (Offset = 5100h) [reset = 0h]

The Map Register defines the fields for the initiator DSS0 Port per channel

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Table 14-5133. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5100h**

Figure 14-1710. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				ASEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5135. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1711 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP1 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP1 Register (Offset = 5104h) [reset = 0h]

The Map Register defines the fields for the initiator DSS0 Port per channel

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Table 14-5136. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5104h**

Figure 14-1711. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ASEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5138. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1712 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP2 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP2 Register (Offset = 5108h) [reset = 0h]

The Map Register defines the fields for the initiator DSS0 Port per channel

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Table 14-5139. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5108h**

Figure 14-1712. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ASEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5141. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1713 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP3 Register

1 CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP3 Register (Offset = 510Ch) [reset = 0h]

The Map Register defines the fields for the initiator DSS0 Port per channel

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Table 14-5142. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 510Ch**

Figure 14-1713. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ASEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5144. CBASS_QOS_IK3_DSS_UL_MAIN_0_VBUSM_DMA_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1714 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1 Register (Offset = 5400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma for group slv_grp_0.

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Table 14-5145. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5400h**

Figure 14-1714. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5147. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5147. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1715 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2 Register (Offset = 5404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma for group slv_grp_0.

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Table 14-5148. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5404h**

Figure 14-1715. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5150. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5150. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1716 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register

1 CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register (Offset = 5500h) [reset = 7000h]

The Map Register defines the fields for the initiator Isa3ss_am62a_main_0.ctxcach_ext_dma per channel.

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Table 14-5151. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5500h**

Figure 14-1716. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5153. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5153. CBASS_QOS_ISA3SS_AM62A_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1717 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1 Register (Offset = 5800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w for group slv_grp_0.

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Table 14-5154. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5800h**

Figure 14-1717. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5156. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5156. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1718 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2 Register (Offset = 5804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w for group slv_grp_0.

Return to Summary Table

Table 14-5157. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5804h**

Figure 14-1718. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5159. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5159. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1719 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0 Register (Offset = 5900h) [reset = 7000h]

The Map Register defines the fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_w per channel.

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Table 14-5160. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5900h**

Figure 14-1719. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5162. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5162. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_W_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1720 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1 Register (Offset = 5C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r for group slv_grp_0.

Return to Summary Table

Table 14-5163. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5C00h**

Figure 14-1720. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">ORDERID7</td><td colspan="4">ORDERID6</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">ORDERID5</td><td colspan="4">ORDERID4</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">ORDERID3</td><td colspan="4">ORDERID2</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID1</td><td colspan="4">ORDERID0</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5165. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5165. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1721 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2 Register (Offset = 5C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r for group slv_grp_0.

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Table 14-5166. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5C04h**

Figure 14-1721. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5168. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5168. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1722 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0 Register (Offset = 5D00h) [reset = 7000h]

The Map Register defines the fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r per channel.

Return to Summary Table

Table 14-5169. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5D00h**

Figure 14-1722. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5171. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5171. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1723 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1 Register

1 CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1 Register (Offset = 5D04h) [reset = 7000h]

The Map Register defines the fields for the initiator Ik3_jpgenc_e5010_main_0.m_vbusm_r per channel.

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Table 14-5172. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 5D04h**

Figure 14-1723. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5174. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5174. CBASS_QOS_IK3_JPGENC_E5010_MAIN_0_M_VBUSM_R_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1724 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register (Offset = 6800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async for group slv_grp_0.

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Table 14-5175. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6800h**

Figure 14-1724. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5177. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5177. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1725 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register (Offset = 6804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_r_async for group slv_grp_0.

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Table 14-5178. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6804h**

Figure 14-1725. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5180. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5180. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1726 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0 Register (Offset = 6900h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5181. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6900h**

Figure 14-1726. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5183. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5183. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1727 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1 Register (Offset = 6904h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5184. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6904h**

Figure 14-1727. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5186. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5186. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1728 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2 Register (Offset = 6908h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5187. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6908h**

Figure 14-1728. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5189. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5189. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1729 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3 Register (Offset = 690Ch) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5190. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 690Ch**

Figure 14-1729. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5192. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5192. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1730 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4 Register (Offset = 6910h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5193. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6910h**

Figure 14-1730. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5195. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5195. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_R_ASYNC_MAP4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1731 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register (Offset = 6C00h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async for group slv_grp_0.

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Table 14-5196. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6C00h**

Figure 14-1731. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5198. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5198. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1732 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register (Offset = 6C04h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.pri_m_vbusm_w_async for group slv_grp_0.

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Table 14-5199. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6C04h**

Figure 14-1732. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5201. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5201. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1733 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0 Register (Offset = 6D00h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5202. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6D00h**

Figure 14-1733. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5204. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5204. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1734 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1 Register (Offset = 6D04h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5205. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6D04h**

Figure 14-1734. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5207. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5207. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1735 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2 Register (Offset = 6D08h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5208. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6D08h**

Figure 14-1735. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5210. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5210. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1736 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3 Register (Offset = 6D0Ch) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5211. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6D0Ch**

Figure 14-1736. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5213. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5213. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1737 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4 Register (Offset = 6D10h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5214. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 6D10h**

Figure 14-1737. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5216. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5216. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_PRI_M_VBUSM_W_ASYNC_MAP4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1738 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register (Offset = 7000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async for group slv_grp_0.

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Table 14-5217. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7000h**

Figure 14-1738. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5219. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5219. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1739 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register (Offset = 7004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_r_async for group slv_grp_0.

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Table 14-5220. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7004h**

Figure 14-1739. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5222. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5222. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1740 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0 Register (Offset = 7100h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Read Port per channel

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Table 14-5223. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7100h**

Figure 14-1740. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5225. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5225. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_R_ASYNC_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1741 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register (Offset = 7400h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async for group slv_grp_0.

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Table 14-5226. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7400h**

Figure 14-1741. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5228. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5228. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1742 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register (Offset = 7404h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Ik3_vpu_wave521cl_main_0.sec_m_vbusm_w_async for group slv_grp_0.

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Table 14-5229. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7404h**

Figure 14-1742. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5231. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5231. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1743 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0 Register

1 CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0 Register (Offset = 7500h) [reset = 7000h]

The Map Register defines the fields for the initiator CODEC0 Write Port per channel

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Table 14-5232. Instance Table

Instance Name	Physical Address
CBASS0	45D2 7500h

Figure 14-1743. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5234. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5234. CBASS_QOS_IK3_VPU_WAVE521CL_MAIN_0_SEC_M_VBUSM_W_ASYNC_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1744 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1 Register (Offset = 7800h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc for group slv_grp_0.

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Table 14-5235. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7800h**

Figure 14-1744. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5237. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5237. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1745 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2 Register (Offset = 7804h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc for group slv_grp_0.

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Table 14-5238. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7804h**

Figure 14-1745. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5240. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5240. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1746 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP0 Register

1 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP0 Register (Offset = 7900h) [reset = 0h]

The Map Register defines the fields for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc per channel.

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Table 14-5241. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7900h**

Figure 14-1746. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5243. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1747 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP1 Register

1 CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP1 Register (Offset = 7904h) [reset = 0h]

The Map Register defines the fields for the initiator Isam62a_c7xv_wrap_main_0.c7xv_soc per channel.

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Table 14-5244. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 7904h**

Figure 14-1747. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5246. CBASS_QOS_ISAM62A_C7XV_WRAP_MAIN_0_C7XV_SOC_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1748 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1 Register

1 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1 Register (Offset = 8000h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst for group slv_grp_0.

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Table 14-5247. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 8000h**

Figure 14-1748. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1 Name Register

31	30	29	28	27	26	25	24
ORDERID7				ORDERID6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID5				ORDERID4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID3				ORDERID2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID1				ORDERID0			
R/W				R/W			
0h				0h			

Table 14-5249. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID7	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID6	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID5	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID4	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID3	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID2	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID1	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5249. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID0	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1749 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2 Register

1 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2 Register (Offset = 8004h) [reset = 0h]

The Group Map Register defines the final orderid for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst for group slv_grp_0.

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Table 14-5250. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 8004h**

Figure 14-1749. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2 Name Register

31	30	29	28	27	26	25	24
ORDERID15				ORDERID14			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ORDERID13				ORDERID12			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ORDERID11				ORDERID10			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ORDERID9				ORDERID8			
R/W				R/W			
0h				0h			

Table 14-5252. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	ORDERID15	R/W	0h	orderid signal for 7. Reset Source: domain_default_rst_mod_g_rst_n
27:24	ORDERID14	R/W	0h	orderid signal for 6. Reset Source: domain_default_rst_mod_g_rst_n
23:20	ORDERID13	R/W	0h	orderid signal for 5. Reset Source: domain_default_rst_mod_g_rst_n
19:16	ORDERID12	R/W	0h	orderid signal for 4. Reset Source: domain_default_rst_mod_g_rst_n
15:12	ORDERID11	R/W	0h	orderid signal for 3. Reset Source: domain_default_rst_mod_g_rst_n
11:8	ORDERID10	R/W	0h	orderid signal for 2. Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID9	R/W	0h	orderid signal for 1. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5252. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_SLV_GRP_0_GRP_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ORDERID8	R/W	0h	orderid signal for 0. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.1750 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0 Register

1 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0 Register (Offset = 8100h) [reset = 7000h]

The Map Register defines the fields for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst per channel.

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Table 14-5253. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 8100h**

Figure 14-1750. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5255. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5255. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1751 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1 Register

1 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1 Register (Offset = 8104h) [reset = 7000h]

The Map Register defines the fields for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst per channel.

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Table 14-5256. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 8104h**

Figure 14-1751. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5258. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5258. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

14.1.1.2.1752 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2 Register

1 CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2 Register (Offset = 8108h) [reset = 7000h]

The Map Register defines the fields for the initiator Isam62a_vpac_wrap_main_0.ldc0_m_mst per channel.

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Table 14-5259. Instance Table

Instance Name	Physical Address
CBASS0	**45D2 8108h**

Figure 14-1752. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5261. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5261. CBASS_QOS_ISAM62A_VPAC_WRAP_MAIN_0_LDC0_M_MST_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved

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cbass

14.1.2.1 cbass Summaries

cbass Summaries

Table 14-5262. CBASS_ERR Registers, Base Address=0472 0000h, Length=1024

Offset	Length	Register Name	MCU_CBASS0 Physical Address
0h	32	CBASS_ERR_PID	0472 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0472 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0472 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0472 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0472 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0472 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0472 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0472 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0472 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0472 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0472 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0472 005Ch
60h	32	CBASS_ERR_EOI	0472 0060h

Table 14-5263. CBASS_ISC Registers, Base Address=4581 8000h, Length=4096

Offset	Length	Register Name	MCU_CBASS0 Physical Address
0h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL	4581 8000h
10h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L	4581 8010h
14h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H	4581 8014h
18h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L	4581 8018h
1Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H	4581 801Ch
20h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL	4581 8020h
30h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L	4581 8030h
34h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H	4581 8034h
38h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L	4581 8038h
3Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H	4581 803Ch
40h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL	4581 8040h
50h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L	4581 8050h

Table 14-5263. CBASS_ISC Registers, Base Address=4581 8000h, Length=4096 (continued)

Offset	Length	Register Name	MCU_CBASS0 Physical Address
54h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H	4581 8054h
58h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L	4581 8058h
5Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H	4581 805Ch
60h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL	4581 8060h
70h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L	4581 8070h
74h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H	4581 8074h
78h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L	4581 8078h
7Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H	4581 807Ch
80h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL	4581 8080h
400h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL	4581 8400h
410h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L	4581 8410h
414h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H	4581 8414h
418h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L	4581 8418h
41Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H	4581 841Ch
420h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL	4581 8420h
430h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L	4581 8430h
434h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H	4581 8434h
438h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L	4581 8438h
43Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H	4581 843Ch
440h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL	4581 8440h
450h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L	4581 8450h
454h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H	4581 8454h
458h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L	4581 8458h
45Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H	4581 845Ch
460h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL	4581 8460h
470h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L	4581 8470h

Table 14-5263. CBASS_ISC Registers, Base Address=4581 8000h, Length=4096 (continued)

Offset	Length	Register Name	MCU_CBASS0 Physical Address
474h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H	4581 8474h
478h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L	4581 8478h
47Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H	4581 847Ch
480h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL	4581 8480h
800h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL	4581 8800h
810h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4581 8810h
814h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4581 8814h
818h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4581 8818h
81Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4581 881Ch
820h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL	4581 8820h
830h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L	4581 8830h
834h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H	4581 8834h
838h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L	4581 8838h
83Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H	4581 883Ch
840h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL	4581 8840h
850h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L	4581 8850h
854h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H	4581 8854h
858h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L	4581 8858h
85Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H	4581 885Ch
860h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL	4581 8860h
870h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L	4581 8870h
874h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H	4581 8874h
878h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L	4581 8878h
87Ch	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H	4581 887Ch
880h	32	CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL	4581 8880h

Table 14-5264. CBASS_GLB Registers, Base Address=45B0 2000h, Length=1024

Offset	Length	Register Name	MCU_CBASS0 Physical Address	WKUP_CBASS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 2000h	45B0 3000h

Table 14-5265. CBASS_QOS Registers, Base Address=45D1 8000h, Length=4096

Offset	Length	Register Name	MCU_CBASS0 Physical Address
100h	32	CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_RMST_MAP0	45D1 8100h
500h	32	CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_WMST_MAP0	45D1 8500h
900h	32	CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_PMST_MAP0	45D1 8900h

14.1.2.2 cbass Registers

cbass Registers

14.1.2.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-5266. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0000h**

Figure 14-1753. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-5268. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-5269. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0004h**

Figure 14-1754. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-5271. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-5272. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0024h**

Figure 14-1755. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-5274. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-5275. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0028h**

Figure 14-1756. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5277. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.2.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to Summary Table

Table 14-5278. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 002Ch**

Figure 14-1757. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-5280. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-5281. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0030h**

Figure 14-1758. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-5283. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-5284. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0034h**

Figure 14-1759. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-5286. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

Table 14-5286. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-5287. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0038h**

Figure 14-1760. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-5289. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-5290. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0050h**

Figure 14-1761. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-5292. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-5293. Instance Table

Instance Name	**Physical Address**
MCU_CBASS0	**0472 0054h**

Figure 14-1762. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ENABLED_INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-5295. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-5296. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0058h**

Figure 14-1763. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-5298. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-5299. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 005Ch**

Figure 14-1764. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-5301. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-5302. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**0472 0060h**

Figure 14-1765. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-5304. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32b_clk2_rst_mod_g_rst_n

14.1.2.2.14 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 106000h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 0 ISC.

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Table 14-5305. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8000h**

Figure 14-1766. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5307. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5307. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.15 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 0 ISC.

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Table 14-5308. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8010h**

Figure 14-1767. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5310. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.16 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 0 ISC.

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Table 14-5311. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8014h**

Figure 14-1768. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5313. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.17 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 0 ISC.

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Table 14-5314. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8018h**

Figure 14-1769. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5316. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.18 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 0 ISC.

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Table 14-5317. Instance Table

Instance Name	Physical Address
MCU_CBASS0	4581 801Ch

Figure 14-1770. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5319. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.19 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL Register (Offset = 20h) [reset = 106000h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 1 ISC.

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Table 14-5320. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8020h**

Figure 14-1771. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
60h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5322. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5322. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.20 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 1 ISC.

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Table 14-5323. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8030h**

Figure 14-1772. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5325. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.21 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 1 ISC.

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Table 14-5326. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8034h**

Figure 14-1773. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5328. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.22 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 1 ISC.

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Table 14-5329. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8038h**

Figure 14-1774. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5331. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.23 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 1 ISC.

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Table 14-5332. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 803Ch**

Figure 14-1775. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5334. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.24 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL Register (Offset = 40h) [reset = 106000h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 2 ISC.

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Table 14-5335. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8040h**

Figure 14-1776. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5337. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5337. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.25 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 2 ISC.

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Table 14-5338. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8050h**

Figure 14-1777. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5340. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.26 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 2 ISC.

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Table 14-5341. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8054h**

Figure 14-1778. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5343. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.27 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 2 ISC.

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Table 14-5344. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8058h**

Figure 14-1779. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5346. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.28 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 2 ISC.

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Table 14-5347. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 805Ch**

Figure 14-1780. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5349. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.29 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL Register (Offset = 60h) [reset = 106000h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 3 ISC.

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Table 14-5350. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8060h**

Figure 14-1781. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5352. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5352. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.30 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 3 ISC.

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Table 14-5353. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8070h**

Figure 14-1782. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5355. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.31 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 3 ISC.

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Table 14-5356. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8074h**

Figure 14-1783. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5358. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.32 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 3 ISC.

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Table 14-5359. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8078h**

Figure 14-1784. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5361. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.33 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 3 ISC.

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Table 14-5362. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 807Ch**

Figure 14-1785. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5364. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.34 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 80h) [reset = 10604Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_rmst region 4 ISC.

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Table 14-5365. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8080h**

Figure 14-1786. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-5367. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5367. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	60h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.35 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 106000h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 0 ISC.

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Table 14-5368. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8400h**

Figure 14-1787. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
60h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5370. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5370. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.36 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 0 ISC.

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Table 14-5371. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8410h**

Figure 14-1788. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5373. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.37 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 0 ISC.

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Table 14-5374. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8414h**

Figure 14-1789. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5376. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.38 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 0 ISC.

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Table 14-5377. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8418h**

Figure 14-1790. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5379. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.39 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 0 ISC.

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Table 14-5380. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 841Ch**

Figure 14-1791. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5382. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.40 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL Register (Offset = 420h) [reset = 106000h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 1 ISC.

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Table 14-5383. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8420h**

Figure 14-1792. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5385. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5385. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.41 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 1 ISC.

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Table 14-5386. Instance Table

Instance Name	**Physical Address**
MCU_CBASS0	**4581 8430h**

Figure 14-1793. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5388. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.42 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 1 ISC.

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Table 14-5389. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8434h**

Figure 14-1794. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5391. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.43 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 1 ISC.

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Table 14-5392. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8438h**

Figure 14-1795. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5394. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.44 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 1 ISC.

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Table 14-5395. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 843Ch**

Figure 14-1796. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-5397. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.45 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL Register (Offset = 440h) [reset = 106000h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 2 ISC.

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Table 14-5398. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8440h**

Figure 14-1797. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5400. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5400. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.46 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 2 ISC.

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Table 14-5401. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8450h**

Figure 14-1798. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5403. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.47 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 2 ISC.

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Table 14-5404. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8454h**

Figure 14-1799. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5406. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.48 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 2 ISC.

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Table 14-5407. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8458h**

Figure 14-1800. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5409. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.49 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 2 ISC.

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Table 14-5410. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 845Ch**

Figure 14-1801. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5412. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.50 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL Register (Offset = 460h) [reset = 106000h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 3 ISC.

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Table 14-5413. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8460h**

Figure 14-1802. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">60h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5415. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5415. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.51 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 3 ISC.

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Table 14-5416. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8470h**

Figure 14-1803. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5418. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.52 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 3 ISC.

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Table 14-5419. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8474h**

Figure 14-1804. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5421. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.53 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 3 ISC.

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Table 14-5422. Instance Table

Instance Name	Physical Address
MCU_CBASS0	4581 8478h

Figure 14-1805. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5424. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.54 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 3 ISC.

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Table 14-5425. Instance Table

Instance Name	Physical Address
MCU_CBASS0	4581 847Ch

Figure 14-1806. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5427. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.55 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 480h) [reset = 10604Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_wmst region 4 ISC.

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Table 14-5428. Instance Table

Instance Name	Physical Address
MCU_CBASS0	4581 8480h

Figure 14-1807. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-5430. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5430. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	60h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.56 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 106000h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 0 ISC.

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Table 14-5431. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8800h**

Figure 14-1808. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5433. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5433. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.57 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 0 ISC.

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Table 14-5434. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8810h**

Figure 14-1809. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5436. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.58 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 0 ISC.

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Table 14-5437. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8814h**

Figure 14-1810. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5439. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.59 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 0 ISC.

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Table 14-5440. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8818h**

Figure 14-1811. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5442. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.60 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 0 ISC.

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Table 14-5443. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 881Ch**

Figure 14-1812. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5445. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.61 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL Register (Offset = 820h) [reset = 106000h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 1 ISC.

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Table 14-5446. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8820h**

Figure 14-1813. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5448. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5448. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.62 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 1 ISC.

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Table 14-5449. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8830h**

Figure 14-1814. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5451. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.63 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 1 ISC.

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Table 14-5452. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8834h**

Figure 14-1815. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5454. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.64 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 1 ISC.

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Table 14-5455. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8838h**

Figure 14-1816. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5457. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.65 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 1 ISC.

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Table 14-5458. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 883Ch**

Figure 14-1817. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5460. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.66 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL Register (Offset = 840h) [reset = 106000h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 2 ISC.

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Table 14-5461. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8840h**

Figure 14-1818. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
60h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5463. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5463. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.67 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 2 ISC.

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Table 14-5464. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8850h**

Figure 14-1819. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5466. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.68 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 2 ISC.

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Table 14-5467. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8854h**

Figure 14-1820. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5469. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.69 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 2 ISC.

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Table 14-5470. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8858h**

Figure 14-1821. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5472. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.70 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 2 ISC.

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Table 14-5473. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 885Ch**

Figure 14-1822. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5475. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.71 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL Register (Offset = 860h) [reset = 106000h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 3 ISC.

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Table 14-5476. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8860h**

Figure 14-1823. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
60h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-5478. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5478. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	60h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.72 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 3 ISC.

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Table 14-5479. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8870h**

Figure 14-1824. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-5481. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.73 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 3 ISC.

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Table 14-5482. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8874h**

Figure 14-1825. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5484. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.74 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 3 ISC.

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Table 14-5485. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8878h**

Figure 14-1826. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5487. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.75 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 3 ISC.

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Table 14-5488. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 887Ch**

Figure 14-1827. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5490. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.76 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 880h) [reset = 10604Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst region 4 ISC.

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Table 14-5491. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**4581 8880h**

Figure 14-1828. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
60h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-5493. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5493. CBASS_ISC_IPULSAR_ULS_MCU_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	60h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.77 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-5494. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**45B0 2000h**
WKUP_CBASS0	**45B0 3000h**

Figure 14-1829. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			

23	22	21	20	19	18	17	16
FUNC							
R							
600h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-5496. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.2.78 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_RMST_MAP0 Register

1 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_RMST_MAP0 Register (Offset = 100h) [reset = 7000h]

The Map Register defines the fields for the initiator MCU_R5FSS0 CPU0 Read Port per channel

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Table 14-5497. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**45D1 8100h**

Figure 14-1830. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5499. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.2.2.79 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_WMST_MAP0 Register

1 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_WMST_MAP0 Register (Offset = 500h) [reset = 7000h]

The Map Register defines the fields for the initiator MCU_R5FSS0 CPU0 Write Port per channel

Return to Summary Table

Table 14-5500. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**45D1 8500h**

Figure 14-1831. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-5502. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.2.2.80 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_PMST_MAP0 Register

1 CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_PMST_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_uls_mcu_0.cpu0_pmst per channel.

Return to Summary Table

Table 14-5503. Instance Table

Instance Name	Physical Address
MCU_CBASS0	**45D1 8900h**

Figure 14-1832. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_PMST_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RSVD</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5505. CBASS_QOS_IPULSAR_ULS_MCU_0_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.3 cbass

cbass

14.1.3.1 cbass Summaries

cbass Summaries

Table 14-5506. CBASS_ERR Registers, Base Address=2B40 0000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_ERR_PID	2B40 0000h
4h	32	CBASS_ERR_DESTINATION_ID	2B40 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	2B40 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	2B40 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	2B40 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	2B40 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	2B40 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	2B40 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	2B40 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	2B40 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	2B40 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	2B40 005Ch
60h	32	CBASS_ERR_EOI	2B40 0060h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL	4500 8000h
4h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0	4500 8004h
8h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1	4500 8008h
Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2	4500 800Ch
10h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L	4500 8010h
14h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H	4500 8014h
18h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L	4500 8018h
1Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H	4500 801Ch
20h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL	4500 8020h
24h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0	4500 8024h
28h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1	4500 8028h
2Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2	4500 802Ch

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
30h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L	4500 8030h
34h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H	4500 8034h
38h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L	4500 8038h
3Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H	4500 803Ch
40h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL	4500 8040h
44h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0	4500 8044h
48h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1	4500 8048h
4Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2	4500 804Ch
50h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L	4500 8050h
54h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H	4500 8054h
58h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L	4500 8058h
5Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H	4500 805Ch
60h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL	4500 8060h
64h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0	4500 8064h
68h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1	4500 8068h
6Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2	4500 806Ch
70h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L	4500 8070h
74h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H	4500 8074h
78h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L	4500 8078h
7Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H	4500 807Ch
400h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 8400h
404h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 8404h
408h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 8408h
40Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 840Ch

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
410h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 8410h
414h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 8414h
418h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 8418h
41Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 841Ch
420h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 8420h
424h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 8424h
428h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 8428h
42Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 842Ch
430h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 8430h
434h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 8434h
438h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 8438h
43Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 843Ch
440h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 8440h
444h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 8444h
448h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 8448h
44Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 844Ch
450h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 8450h
454h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 8454h
458h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 8458h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
45Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 845Ch
460h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 8460h
464h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 8464h
468h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 8468h
46Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 846Ch
470h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 8470h
474h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 8474h
478h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 8478h
47Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 847Ch
480h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 8480h
484h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 8484h
488h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 8488h
48Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 848Ch
490h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 8490h
494h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 8494h
498h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 8498h
49Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 849Ch
4A0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 84A0h
4A4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 84A4h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
4A8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 84A8h
4ACh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 84ACh
4B0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 84B0h
4B4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 84B4h
4B8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 84B8h
4BCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 84BCh
4C0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 84C0h
4C4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 84C4h
4C8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 84C8h
4CCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 84CCh
4D0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 84D0h
4D4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 84D4h
4D8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 84D8h
4DCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 84DCh
4E0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 84E0h
4E4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 84E4h
4E8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 84E8h
4ECh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 84ECh
4F0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 84F0h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
4F4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 84F4h
4F8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 84F8h
4FCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 84FCh
500h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL	4500 8500h
504h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0	4500 8504h
508h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1	4500 8508h
50Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2	4500 850Ch
510h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L	4500 8510h
514h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H	4500 8514h
518h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L	4500 8518h
51Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H	4500 851Ch
520h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL	4500 8520h
524h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0	4500 8524h
528h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1	4500 8528h
52Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2	4500 852Ch
530h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L	4500 8530h
534h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H	4500 8534h
538h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L	4500 8538h
53Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H	4500 853Ch

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
540h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL	4500 8540h
544h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0	4500 8544h
548h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1	4500 8548h
54Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2	4500 854Ch
550h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L	4500 8550h
554h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H	4500 8554h
558h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L	4500 8558h
55Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H	4500 855Ch
560h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL	4500 8560h
564h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0	4500 8564h
568h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1	4500 8568h
56Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2	4500 856Ch
570h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L	4500 8570h
574h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H	4500 8574h
578h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L	4500 8578h
57Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H	4500 857Ch
580h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL	4500 8580h
584h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0	4500 8584h
588h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1	4500 8588h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
58Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2	4500 858Ch
590h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L	4500 8590h
594h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H	4500 8594h
598h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L	4500 8598h
59Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H	4500 859Ch
5A0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL	4500 85A0h
5A4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0	4500 85A4h
5A8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1	4500 85A8h
5ACh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2	4500 85ACh
5B0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L	4500 85B0h
5B4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H	4500 85B4h
5B8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L	4500 85B8h
5BCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H	4500 85BCh
5C0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL	4500 85C0h
5C4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0	4500 85C4h
5C8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1	4500 85C8h
5CCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2	4500 85CCh
5D0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L	4500 85D0h
5D4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H	4500 85D4h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
5D8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L	4500 85D8h
5DCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H	4500 85DCh
5E0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL	4500 85E0h
5E4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0	4500 85E4h
5E8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1	4500 85E8h
5ECh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2	4500 85ECh
5F0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L	4500 85F0h
5F4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H	4500 85F4h
5F8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L	4500 85F8h
5FCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H	4500 85FCh
800h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_CONTROL	4500 8800h
804h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0	4500 8804h
808h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1	4500 8808h
80Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2	4500 880Ch
810h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L	4500 8810h
814h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H	4500 8814h
818h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L	4500 8818h
81Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H	4500 881Ch
820h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_CONTROL	4500 8820h
824h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0	4500 8824h
828h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1	4500 8828h
82Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2	4500 882Ch

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
830h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L	4500 8830h
834h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H	4500 8834h
838h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L	4500 8838h
83Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H	4500 883Ch
840h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_CONTROL	4500 8840h
844h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0	4500 8844h
848h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1	4500 8848h
84Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2	4500 884Ch
850h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L	4500 8850h
854h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H	4500 8854h
858h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L	4500 8858h
85Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H	4500 885Ch
860h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_CONTROL	4500 8860h
864h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0	4500 8864h
868h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1	4500 8868h
86Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2	4500 886Ch
870h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L	4500 8870h
874h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H	4500 8874h
878h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L	4500 8878h
87Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H	4500 887Ch
880h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_CONTROL	4500 8880h
884h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0	4500 8884h
888h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1	4500 8888h
88Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2	4500 888Ch
890h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L	4500 8890h
894h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H	4500 8894h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
898h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L	4500 8898h
89Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H	4500 889Ch
8A0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_CONTROL	4500 88A0h
8A4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0	4500 88A4h
8A8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1	4500 88A8h
8ACh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2	4500 88ACh
8B0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L	4500 88B0h
8B4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H	4500 88B4h
8B8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L	4500 88B8h
8BCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H	4500 88BCh
8C0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_CONTROL	4500 88C0h
8C4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0	4500 88C4h
8C8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1	4500 88C8h
8CCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2	4500 88CCh
8D0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L	4500 88D0h
8D4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H	4500 88D4h
8D8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L	4500 88D8h
8DCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H	4500 88DCh
8E0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_CONTROL	4500 88E0h
8E4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0	4500 88E4h
8E8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1	4500 88E8h
8ECh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2	4500 88ECh
8F0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L	4500 88F0h
8F4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H	4500 88F4h
8F8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L	4500 88F8h
8FCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H	4500 88FCh

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
900h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_CONTROL	4500 8900h
904h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0	4500 8904h
908h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1	4500 8908h
90Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2	4500 890Ch
910h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L	4500 8910h
914h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H	4500 8914h
918h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L	4500 8918h
91Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H	4500 891Ch
920h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_CONTROL	4500 8920h
924h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0	4500 8924h
928h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1	4500 8928h
92Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2	4500 892Ch
930h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L	4500 8930h
934h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H	4500 8934h
938h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L	4500 8938h
93Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H	4500 893Ch
940h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_CONTROL	4500 8940h
944h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0	4500 8944h
948h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1	4500 8948h
94Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2	4500 894Ch
950h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L	4500 8950h
954h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H	4500 8954h
958h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L	4500 8958h
95Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H	4500 895Ch
960h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_CONTROL	4500 8960h
964h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0	4500 8964h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
968h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1	4500 8968h
96Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2	4500 896Ch
970h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L	4500 8970h
974h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H	4500 8974h
978h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L	4500 8978h
97Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H	4500 897Ch
980h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_CONTROL	4500 8980h
984h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0	4500 8984h
988h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1	4500 8988h
98Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2	4500 898Ch
990h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L	4500 8990h
994h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H	4500 8994h
998h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L	4500 8998h
99Ch	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H	4500 899Ch
9A0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_CONTROL	4500 89A0h
9A4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0	4500 89A4h
9A8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1	4500 89A8h
9ACh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2	4500 89ACh
9B0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L	4500 89B0h
9B4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H	4500 89B4h
9B8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L	4500 89B8h
9BCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H	4500 89BCh
9C0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_CONTROL	4500 89C0h
9C4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0	4500 89C4h
9C8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1	4500 89C8h
9CCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2	4500 89CCh

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
9D0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L	4500 89D0h
9D4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H	4500 89D4h
9D8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L	4500 89D8h
9DCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H	4500 89DCh
9E0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_CONTROL	4500 89E0h
9E4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0	4500 89E4h
9E8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1	4500 89E8h
9ECh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2	4500 89ECh
9F0h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L	4500 89F0h
9F4h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H	4500 89F4h
9F8h	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L	4500 89F8h
9FCh	32	CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H	4500 89FCh
C00h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 8C00h
C04h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 8C04h
C08h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 8C08h
C0Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 8C0Ch
C10h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 8C10h
C14h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 8C14h
C18h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 8C18h
C1Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 8C1Ch
C20h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 8C20h
C24h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 8C24h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
C28h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 8C28h
C2Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 8C2Ch
C30h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 8C30h
C34h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 8C34h
C38h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 8C38h
C3Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 8C3Ch
C40h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 8C40h
C44h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 8C44h
C48h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 8C48h
C4Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 8C4Ch
C50h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 8C50h
C54h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 8C54h
C58h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 8C58h
C5Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 8C5Ch
C60h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 8C60h
C64h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 8C64h
C68h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 8C68h
C6Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 8C6Ch
C70h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 8C70h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
C74h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 8C74h
C78h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 8C78h
C7Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 8C7Ch
C80h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 8C80h
C84h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 8C84h
C88h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 8C88h
C8Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 8C8Ch
C90h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 8C90h
C94h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 8C94h
C98h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 8C98h
C9Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 8C9Ch
CA0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 8CA0h
CA4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 8CA4h
CA8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 8CA8h
CACh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 8CACh
CB0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 8CB0h
CB4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 8CB4h
CB8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 8CB8h
CBCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 8CBCh

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
CC0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 8CC0h
CC4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 8CC4h
CC8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 8CC8h
CCCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 8CCCh
CD0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 8CD0h
CD4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 8CD4h
CD8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 8CD8h
CDCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 8CDCh
CE0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 8CE0h
CE4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 8CE4h
CE8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 8CE8h
CECh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 8CECh
CF0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 8CF0h
CF4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 8CF4h
CF8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 8CF8h
CFCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 8CFCh
D00h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL	4500 8D00h
D04h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0	4500 8D04h
D08h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1	4500 8D08h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
D0Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2	4500 8D0Ch
D10h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L	4500 8D10h
D14h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H	4500 8D14h
D18h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L	4500 8D18h
D1Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H	4500 8D1Ch
D20h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL	4500 8D20h
D24h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0	4500 8D24h
D28h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1	4500 8D28h
D2Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2	4500 8D2Ch
D30h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L	4500 8D30h
D34h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H	4500 8D34h
D38h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L	4500 8D38h
D3Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H	4500 8D3Ch
D40h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL	4500 8D40h
D44h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0	4500 8D44h
D48h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1	4500 8D48h
D4Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2	4500 8D4Ch
D50h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L	4500 8D50h
D54h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H	4500 8D54h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
D58h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L	4500 8D58h
D5Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H	4500 8D5Ch
D60h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL	4500 8D60h
D64h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0	4500 8D64h
D68h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1	4500 8D68h
D6Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2	4500 8D6Ch
D70h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L	4500 8D70h
D74h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H	4500 8D74h
D78h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L	4500 8D78h
D7Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H	4500 8D7Ch
D80h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL	4500 8D80h
D84h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0	4500 8D84h
D88h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1	4500 8D88h
D8Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2	4500 8D8Ch
D90h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L	4500 8D90h
D94h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H	4500 8D94h
D98h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L	4500 8D98h
D9Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H	4500 8D9Ch
DA0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL	4500 8DA0h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
DA4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0	4500 8DA4h
DA8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1	4500 8DA8h
DACh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2	4500 8DACh
DB0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L	4500 8DB0h
DB4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H	4500 8DB4h
DB8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L	4500 8DB8h
DBCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H	4500 8DBCh
DC0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL	4500 8DC0h
DC4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0	4500 8DC4h
DC8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1	4500 8DC8h
DCCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2	4500 8DCCh
DD0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L	4500 8DD0h
DD4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H	4500 8DD4h
DD8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L	4500 8DD8h
DDCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H	4500 8DDCh
DE0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL	4500 8DE0h
DE4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0	4500 8DE4h
DE8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1	4500 8DE8h
DECh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2	4500 8DECh

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
DF0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L	4500 8DF0h
DF4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H	4500 8DF4h
DF8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L	4500 8DF8h
DFCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H	4500 8DFCh
1000h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 9000h
1004h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 9004h
1008h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 9008h
100Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 900Ch
1010h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 9010h
1014h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 9014h
1018h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 9018h
101Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 901Ch
1020h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 9020h
1024h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 9024h
1028h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 9028h
102Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 902Ch
1030h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 9030h
1034h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 9034h
1038h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 9038h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
103Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 903Ch
1040h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 9040h
1044h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 9044h
1048h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 9048h
104Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 904Ch
1050h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 9050h
1054h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 9054h
1058h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 9058h
105Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 905Ch
1060h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 9060h
1064h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 9064h
1068h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 9068h
106Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 906Ch
1070h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 9070h
1074h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 9074h
1078h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 9078h
107Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 907Ch
1080h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 9080h
1084h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 9084h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
1088h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 9088h
108Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 908Ch
1090h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 9090h
1094h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 9094h
1098h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 9098h
109Ch	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 909Ch
10A0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 90A0h
10A4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 90A4h
10A8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 90A8h
10ACh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 90ACh
10B0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 90B0h
10B4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 90B4h
10B8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 90B8h
10BCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 90BCh
10C0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 90C0h
10C4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 90C4h
10C8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 90C8h
10CCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 90CCh
10D0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 90D0h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
10D4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 90D4h
10D8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 90D8h
10DCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 90DCh
10E0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 90E0h
10E4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 90E4h
10E8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 90E8h
10ECh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 90ECh
10F0h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 90F0h
10F4h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 90F4h
10F8h	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 90F8h
10FCh	32	CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 90FCh
1400h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_CONTROL	4500 9400h
1404h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0	4500 9404h
1408h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1	4500 9408h
140Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2	4500 940Ch
1410h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_L	4500 9410h
1414h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_H	4500 9414h
1418h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_L	4500 9418h
141Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_H	4500 941Ch
1420h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_CONTROL	4500 9420h
1424h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0	4500 9424h
1428h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1	4500 9428h

Table 14-5507. CBASS_FW Registers, Base Address=4500 8000h, Length=8192 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
142Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2	4500 942Ch
1430h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_L	4500 9430h
1434h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_H	4500 9434h
1438h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_L	4500 9438h
143Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_H	4500 943Ch
1440h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_CONTROL	4500 9440h
1444h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0	4500 9444h
1448h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1	4500 9448h
144Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2	4500 944Ch
1450h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_L	4500 9450h
1454h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_H	4500 9454h
1458h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_L	4500 9458h
145Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_H	4500 945Ch
1460h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_CONTROL	4500 9460h
1464h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0	4500 9464h
1468h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1	4500 9468h
146Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2	4500 946Ch
1470h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_L	4500 9470h
1474h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_H	4500 9474h
1478h	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_L	4500 9478h
147Ch	32	CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_H	4500 947Ch

Table 14-5508. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL	4581 4000h
10h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L	4581 4010h
14h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H	4581 4014h

Table 14-5508. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
18h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L	4581 4018h
1Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H	4581 401Ch
20h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL	4581 4020h
30h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L	4581 4030h
34h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H	4581 4034h
38h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L	4581 4038h
3Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H	4581 403Ch
40h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL	4581 4040h
50h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L	4581 4050h
54h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H	4581 4054h
58h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L	4581 4058h
5Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H	4581 405Ch
60h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL	4581 4060h
70h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L	4581 4070h
74h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H	4581 4074h
78h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L	4581 4078h
7Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H	4581 407Ch
80h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL	4581 4080h
400h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL	4581 4400h
410h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L	4581 4410h
414h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H	4581 4414h
418h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L	4581 4418h
41Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H	4581 441Ch
420h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL	4581 4420h
430h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L	4581 4430h
434h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H	4581 4434h

Table 14-5508. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
438h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L	4581 4438h
43Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H	4581 443Ch
440h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL	4581 4440h
450h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L	4581 4450h
454h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H	4581 4454h
458h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L	4581 4458h
45Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H	4581 445Ch
460h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL	4581 4460h
470h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L	4581 4470h
474h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H	4581 4474h
478h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L	4581 4478h
47Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H	4581 447Ch
480h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL	4581 4480h
800h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL	4581 4800h
810h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4581 4810h
814h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4581 4814h
818h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4581 4818h
81Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4581 481Ch
820h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL	4581 4820h
830h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L	4581 4830h
834h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H	4581 4834h
838h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L	4581 4838h
83Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H	4581 483Ch
840h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL	4581 4840h
850h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L	4581 4850h
854h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H	4581 4854h

Table 14-5508. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
858h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L	4581 4858h
85Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H	4581 485Ch
860h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL	4581 4860h
870h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L	4581 4870h
874h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H	4581 4874h
878h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L	4581 4878h
87Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H	4581 487Ch
880h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL	4581 4880h

Table 14-5509. CBASS_GLB Registers, Base Address=45B0 3000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 3000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 3004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 3020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 3024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 3028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 302Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 3030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 3034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 3038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 3040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 3044h

Table 14-5510. CBASS_QOS Registers, Base Address=45D1 4000h, Length=4096

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
100h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0	45D1 4100h
500h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0	45D1 4500h
900h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0	45D1 4900h

14.1.3.2 cbass Registers

cbass Registers

14.1.3.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-5511. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0000h**

Figure 14-1833. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
6h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-5513. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-5514. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0004h**

Figure 14-1834. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5516. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-5517. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0024h**

Figure 14-1835. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-5519. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-5520. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0028h**

Figure 14-1836. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5522. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.3.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to Summary Table

Table 14-5523. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 002Ch**

Figure 14-1837. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5525. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-5526. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0030h**

Figure 14-1838. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-5528. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-5529. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0034h**

Figure 14-1839. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-5531. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

Table 14-5531. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-5532. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0038h**

Figure 14-1840. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-5534. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-5535. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0050h**

Figure 14-1841. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-5537. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-5538. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0054h**

Figure 14-1842. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-5540. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-5541. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0058h**

Figure 14-1843. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-5543. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-5544. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 005Ch**

Figure 14-1844. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-5546. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-5547. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**2B40 0060h**

Figure 14-1845. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-5549. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRM_DM_clk1_rst_mod_g_rst_n

14.1.3.2.14 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5550. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8000h**

Figure 14-1846. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5552. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.15 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5553. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8004h**

Figure 14-1847. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5555. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5555. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.16 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5556. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8008h**

Figure 14-1848. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-5558. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5558. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.17 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5559. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 800Ch**

Figure 14-1849. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5561. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5561. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.18 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 78000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5562. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8010h**

Figure 14-1850. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
78000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
78000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
78000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5564. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	78000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.19 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5565. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8014h**

Figure 14-1851. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5567. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.20 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 78007FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5568. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8018h**

Figure 14-1852. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
78007h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
78007h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
78007h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5570. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	78007h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.21 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-5571. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 801Ch**

Figure 14-1853. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5573. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.22 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5574. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8020h**

Figure 14-1854. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5576. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.23 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5577. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8024h**

Figure 14-1855. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5579. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5579. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.24 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5580. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8028h**

Figure 14-1856. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5582. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5582. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.25 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5583. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 802Ch**

Figure 14-1857. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5585. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5585. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.26 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 78100000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5586. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8030h**

Figure 14-1858. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
78100h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
78100h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
78100h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5588. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	78100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.27 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5589. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8034h**

Figure 14-1859. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5591. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.28 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = 78107FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5592. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8038h**

Figure 14-1860. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">78107h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">78107h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">78107h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5594. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	78107h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.29 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-5595. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 803Ch**

Figure 14-1861. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5597. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.30 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5598. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8040h**

Figure 14-1862. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5600. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.31 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5601. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8044h**

Figure 14-1863. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5603. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5603. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.32 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5604. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8048h**

Figure 14-1864. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5606. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5606. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.33 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5607. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 804Ch**

Figure 14-1865. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-5609. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5609. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.34 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 74000000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5610. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8050h**

Figure 14-1866. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
74000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
74000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
74000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5612. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	74000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.35 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5613. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8054h**

Figure 14-1867. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5615. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.36 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = 747FFFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5616. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8058h**

Figure 14-1868. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
747FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
747FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
747FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5618. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	747FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.37 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-5619. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 805Ch**

Figure 14-1869. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5621. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.38 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5622. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8060h

Figure 14-1870. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5624. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.39 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5625. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8064h**

Figure 14-1871. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5627. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5627. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.40 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5628. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8068h**

Figure 14-1872. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5630. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5630. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.41 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5631. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 806Ch**

Figure 14-1873. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5633. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5633. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.42 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 74800000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5634. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8070h**

Figure 14-1874. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
74800h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
74800h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
74800h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-5636. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	74800h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.43 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5637. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8074h**

Figure 14-1875. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5639. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.44 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = 74FFFFFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5640. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8078h**

Figure 14-1876. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
74FFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
74FFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
74FFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5642. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	74FFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.45 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-5643. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 807Ch**

Figure 14-1877. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5645. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.46 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5646. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8400h**

Figure 14-1878. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5648. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5648. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.47 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5649. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8404h

Figure 14-1879. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5651. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5651. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.48 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5652. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8408h**

Figure 14-1880. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5654. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5654. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.49 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5655. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 840Ch**

Figure 14-1881. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5657. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5657. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.50
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5658. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8410h**

Figure 14-1882. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5660. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.51 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5661. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8414h**

Figure 14-1883. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5663. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.52 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5664. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8418h**

Figure 14-1884. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5666. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.53 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-5667. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 841Ch**

Figure 14-1885. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5669. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.54 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5670. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8420h**

Figure 14-1886. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5672. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5672. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.55 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5673. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8424h**

Figure 14-1887. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5675. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5675. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.56 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5676. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8428h**

Figure 14-1888. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5678. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5678. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.57 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5679. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 842Ch**

Figure 14-1889. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5681. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5681. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.58 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5682. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8430h**

Figure 14-1890. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-5684. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.59 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5685. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8434h**

Figure 14-1891. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5687. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.60 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5688. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8438h**

Figure 14-1892. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5690. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.61 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-5691. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 843Ch**

Figure 14-1893. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5693. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.62

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5694. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8440h**

Figure 14-1894. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5696. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5696. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.63 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5697. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8444h

Figure 14-1895. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5699. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5699. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.64 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5700. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8448h**

Figure 14-1896. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5702. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5702. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.65 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5703. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 844Ch**

Figure 14-1897. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5705. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5705. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.66
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5706. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8450h**

Figure 14-1898. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5708. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.67 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5709. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8454h**

Figure 14-1899. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5711. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.68 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5712. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8458h

Figure 14-1900. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5714. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.69 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-5715. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 845Ch**

Figure 14-1901. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5717. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.70 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5718. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8460h**

Figure 14-1902. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5720. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5720. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.71

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5721. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8464h**

Figure 14-1903. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5723. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5723. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.72 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5724. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8468h

Figure 14-1904. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5726. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5726. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.73 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5727. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 846Ch**

Figure 14-1905. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5729. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5729. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.74 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5730. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8470h**

Figure 14-1906. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-5732. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.75
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5733. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8474h**

Figure 14-1907. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5735. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.76

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5736. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8478h

Figure 14-1908. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5738. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.77 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-5739. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 847Ch**

Figure 14-1909. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5741. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.78 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5742. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8480h**

Figure 14-1910. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5744. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5744. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.79 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5745. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8484h**

Figure 14-1911. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-5747. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5747. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.80 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5748. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8488h**

Figure 14-1912. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5750. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5750. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.81 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5751. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 848Ch**

Figure 14-1913. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5753. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5753. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.82 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5754. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8490h**

Figure 14-1914. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5756. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.83
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5757. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8494h**

Figure 14-1915. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5759. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.84 *CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register*

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5760. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8498h**

Figure 14-1916. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5762. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.85
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 4 firewall.

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Table 14-5763. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 849Ch**

Figure 14-1917. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5765. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.86 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5766. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84A0h**

Figure 14-1918. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5768. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5768. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.87 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5769. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84A4h**

Figure 14-1919. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5771. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5771. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.88 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5772. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84A8h**

Figure 14-1920. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5774. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5774. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.89 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5775. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84ACh**

Figure 14-1921. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5777. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5777. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.90 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5778. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84B0h**

Figure 14-1922. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5780. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.91 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5781. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 84B4h**

Figure 14-1923. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5783. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.92 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5784. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84B8h**

Figure 14-1924. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5786. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.93 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-5787. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84BCh**

Figure 14-1925. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5789. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.94 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5790. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84C0h**

Figure 14-1926. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5792. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5792. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.95 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5793. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84C4h**

Figure 14-1927. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5795. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5795. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.96 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5796. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84C8h**

Figure 14-1928. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5798. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5798. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.97 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5799. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84CCh**

Figure 14-1929. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5801. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5801. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.98 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5802. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84D0h**

Figure 14-1930. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-5804. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.99 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5805. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84D4h**

Figure 14-1931. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5807. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.100

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5808. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84D8h**

Figure 14-1932. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5810. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.101 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-5811. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84DCh**

Figure 14-1933. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5813. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.102 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5814. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84E0h**

Figure 14-1934. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5816. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5816. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.103 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5817. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84E4h**

Figure 14-1935. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5819. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5819. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.104
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5820. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84E8h**

Figure 14-1936. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5822. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5822. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.105 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5823. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84ECh**

Figure 14-1937. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5825. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5825. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.106
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5826. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84F0h**

Figure 14-1938. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5828. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.107 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5829. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84F4h**

Figure 14-1939. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5831. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.108 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5832. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84F8h**

Figure 14-1940. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5834. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.109 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-5835. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 84FCh**

Figure 14-1941. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5837. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.110 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register (Offset = 500h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5838. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8500h**

Figure 14-1942. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5840. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5840. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.111 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 504h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5841. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8504h**

Figure 14-1943. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5843. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5843. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.112 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 508h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5844. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8508h

Figure 14-1944. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5846. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5846. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.113 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 50Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5847. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 850Ch**

Figure 14-1945. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5849. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5849. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.114 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 510h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5850. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8510h**

Figure 14-1946. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5852. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.115 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 514h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5853. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8514h**

Figure 14-1947. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5855. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.116 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 518h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5856. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8518h**

Figure 14-1948. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5858. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.117 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 51Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-5859. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 851Ch**

Figure 14-1949. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5861. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.118
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register (Offset = 520h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5862. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8520h

Figure 14-1950. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5864. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5864. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.119 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 524h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5865. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8524h**

Figure 14-1951. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5867. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5867. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.120
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 528h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5868. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8528h**

Figure 14-1952. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5870. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5870. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.121 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 52Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5871. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 852Ch**

Figure 14-1953. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5873. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5873. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.122 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 530h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5874. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8530h**

Figure 14-1954. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5876. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.123 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 534h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5877. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8534h**

Figure 14-1955. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5879. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.124 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 538h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5880. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8538h**

Figure 14-1956. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5882. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.125 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 53Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-5883. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 853Ch**

Figure 14-1957. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5885. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.126 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register (Offset = 540h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5886. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8540h**

Figure 14-1958. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5888. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5888. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.127
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 544h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5889. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8544h**

Figure 14-1959. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5891. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5891. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.128 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 548h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5892. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8548h**

Figure 14-1960. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5894. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5894. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.129 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 54Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5895. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 854Ch**

Figure 14-1961. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5897. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5897. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.130 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 550h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5898. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8550h**

Figure 14-1962. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5900. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.131
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 554h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5901. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8554h**

Figure 14-1963. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5903. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.132 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 558h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5904. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8558h**

Figure 14-1964. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5906. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.133 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 55Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-5907. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 855Ch**

Figure 14-1965. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5909. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.134 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register (Offset = 560h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5910. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8560h**

Figure 14-1966. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5912. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5912. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.135 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 564h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5913. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8564h**

Figure 14-1967. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5915. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5915. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.136 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 568h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5916. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8568h**

Figure 14-1968. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5918. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5918. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.137 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 56Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5919. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 856Ch**

Figure 14-1969. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5921. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5921. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.138 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 570h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5922. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8570h**

Figure 14-1970. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5924. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.139 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 574h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5925. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8574h**

Figure 14-1971. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5927. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.140 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 578h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5928. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8578h**

Figure 14-1972. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-5930. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.141 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 57Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-5931. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 857Ch**

Figure 14-1973. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5933. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.142 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register (Offset = 580h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5934. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8580h**

Figure 14-1974. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5936. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5936. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.143 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 584h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5937. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8584h**

Figure 14-1975. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5939. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5939. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.144 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 588h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5940. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8588h**

Figure 14-1976. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5942. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5942. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.145 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 58Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5943. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 858Ch**

Figure 14-1977. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5945. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5945. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.146 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 590h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5946. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8590h**

Figure 14-1978. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-5948. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.147 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 594h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5949. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8594h**

Figure 14-1979. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5951. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.148

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 598h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5952. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8598h**

Figure 14-1980. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5954. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.149 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 59Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-5955. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 859Ch**

Figure 14-1981. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5957. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.150
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register (Offset = 5A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5958. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85A0h**

Figure 14-1982. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5960. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5960. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.151 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 5A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5961. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85A4h

Figure 14-1983. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5963. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5963. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.152 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 5A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5964. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85A8h**

Figure 14-1984. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5966. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5966. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.153 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 5ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5967. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85ACh**

Figure 14-1985. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5969. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5969. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.154 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 5B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5970. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85B0h**

Figure 14-1986. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5972. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.155 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 5B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5973. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85B4h**

Figure 14-1987. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-5975. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.156
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 5B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5976. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85B8h**

Figure 14-1988. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-5978. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.157 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 5BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-5979. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85BCh**

Figure 14-1989. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-5981. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.158 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register (Offset = 5C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-5982. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85C0h**

Figure 14-1990. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-5984. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5984. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.159 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 5C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-5985. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85C4h**

Figure 14-1991. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5987. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5987. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.160 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 5C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-5988. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85C8h**

Figure 14-1992. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5990. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5990. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.161 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 5CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-5991. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85CCh

Figure 14-1993. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5993. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-5993. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.162 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 5D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-5994. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85D0h

Figure 14-1994. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5996. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.163 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 5D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-5997. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85D4h**

Figure 14-1995. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-5999. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.164 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 5D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-6000. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85D8h**

Figure 14-1996. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6002. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.165 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 5DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 14 firewall.

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Table 14-6003. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85DCh**

Figure 14-1997. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6005. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.166 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register (Offset = 5E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6006. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85E0h**

Figure 14-1998. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6008. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6008. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.167

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 5E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6009. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85E4h**

Figure 14-1999. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6011. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6011. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.168 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 5E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6012. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85E8h**

Figure 14-2000. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6014. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6014. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.169 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 5ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6015. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85ECh

Figure 14-2001. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6017. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6017. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.170 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 5F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6018. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85F0h**

Figure 14-2002. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6020. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.171 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 5F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6021. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85F4h**

Figure 14-2003. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6023. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.172

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 5F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6024. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85F8h**

Figure 14-2004. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6026. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.173 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 5FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_main_infra_cbass_data_l0.slv region 15 firewall.

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Table 14-6027. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 85FCh**

Figure 14-2005. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6029. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.174 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6030. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8800h**

Figure 14-2006. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6032. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.175 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6033. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8804h**

Figure 14-2007. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6035. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6035. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.176 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6036. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8808h**

Figure 14-2008. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6038. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6038. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.177 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6039. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 880Ch**

Figure 14-2009. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6041. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6041. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.178 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6042. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8810h**

Figure 14-2010. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6044. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.179 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6045. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8814h**

Figure 14-2011. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6047. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.180 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6048. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8818h

Figure 14-2012. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6050. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.181 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 0 firewall.

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Table 14-6051. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 881Ch**

Figure 14-2013. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6053. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.182 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6054. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8820h**

Figure 14-2014. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6056. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.183 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6057. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8824h**

Figure 14-2015. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6059. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6059. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.184 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6060. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8828h**

Figure 14-2016. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6062. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6062. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.185 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6063. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 882Ch**

Figure 14-2017. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6065. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6065. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.186 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6066. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8830h**

Figure 14-2018. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-6068. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.187 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6069. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8834h**

Figure 14-2019. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6071. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.188 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6072. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8838h**

Figure 14-2020. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6074. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.189 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 1 firewall.

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Table 14-6075. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 883Ch**

Figure 14-2021. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6077. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.190 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6078. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8840h**

Figure 14-2022. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6080. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.191 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6081. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8844h**

Figure 14-2023. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6083. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6083. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.192 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6084. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8848h**

Figure 14-2024. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6086. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6086. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.193 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6087. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 884Ch**

Figure 14-2025. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6089. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6089. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.194 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6090. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8850h**

Figure 14-2026. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6092. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.195 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6093. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8854h**

Figure 14-2027. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6095. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.196 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6096. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8858h**

Figure 14-2028. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6098. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.197 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 2 firewall.

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Table 14-6099. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 885Ch**

Figure 14-2029. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6101. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.198 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6102. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8860h**

Figure 14-2030. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6104. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.199 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6105. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8864h**

Figure 14-2031. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6107. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6107. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.200 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6108. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8868h**

Figure 14-2032. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6110. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6110. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.201 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6111. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 886Ch**

Figure 14-2033. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6113. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6113. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.202 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6114. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8870h**

Figure 14-2034. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6116. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.203 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6117. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8874h**

Figure 14-2035. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6119. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.204 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6120. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8878h**

Figure 14-2036. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6122. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.205 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 3 firewall.

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Table 14-6123. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 887Ch**

Figure 14-2037. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6125. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.206 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6126. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8880h**

Figure 14-2038. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6128. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.207 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6129. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8884h**

Figure 14-2039. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6131. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6131. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.208 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6132. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8888h**

Figure 14-2040. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6134. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6134. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.209 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6135. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 888Ch

Figure 14-2041. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6137. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6137. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.210 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6138. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8890h**

Figure 14-2042. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6140. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.211 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

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Table 14-6141. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8894h**

Figure 14-2043. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6143. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.212 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

Return to Summary Table

Table 14-6144. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8898h**

Figure 14-2044. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6146. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.213 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 4 firewall.

Return to Summary Table

Table 14-6147. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 889Ch**

Figure 14-2045. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6149. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.214 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6150. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88A0h**

Figure 14-2046. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6152. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.215 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6153. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88A4h**

Figure 14-2047. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6155. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6155. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.216 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6156. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88A8h**

Figure 14-2048. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6158. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6158. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.217 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6159. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88ACh**

Figure 14-2049. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6161. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6161. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.218 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6162. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88B0h**

Figure 14-2050. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6164. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.219 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6165. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88B4h**

Figure 14-2051. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6167. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.220 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6168. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 88B8h**

Figure 14-2052. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6170. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.221 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 5 firewall.

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Table 14-6171. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88BCh**

Figure 14-2053. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6173. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.222 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6174. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88C0h**

Figure 14-2054. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6176. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.223 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6177. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88C4h**

Figure 14-2055. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6179. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6179. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.224 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6180. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88C8h**

Figure 14-2056. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6182. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6182. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.225 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6183. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88CCh**

Figure 14-2057. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6185. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6185. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.226 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6186. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88D0h**

Figure 14-2058. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6188. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.227 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6189. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88D4h**

Figure 14-2059. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6191. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.228 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6192. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88D8h**

Figure 14-2060. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6194. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.229 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 6 firewall.

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Table 14-6195. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88DCh**

Figure 14-2061. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6197. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.230 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6198. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88E0h**

Figure 14-2062. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6200. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.231 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6201. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88E4h**

Figure 14-2063. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6203. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6203. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.232 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6204. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88E8h**

Figure 14-2064. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6206. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6206. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.233 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6207. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88ECh**

Figure 14-2065. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6209. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6209. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.234 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6210. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88F0h**

Figure 14-2066. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6212. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.235 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6213. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88F4h**

Figure 14-2067. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6215. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.236 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6216. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88F8h**

Figure 14-2068. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6218. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.237 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 7 firewall.

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Table 14-6219. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 88FCh**

Figure 14-2069. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6221. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.238 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_CONTROL Register (Offset = 900h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6222. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8900h**

Figure 14-2070. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6224. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.239 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 904h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6225. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8904h**

Figure 14-2071. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6227. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6227. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.240 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 908h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6228. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8908h

Figure 14-2072. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6230. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6230. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.241 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 90Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6231. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 890Ch**

Figure 14-2073. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6233. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6233. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.242 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 910h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6234. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8910h**

Figure 14-2074. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6236. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.243 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 914h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6237. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8914h**

Figure 14-2075. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6239. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.244 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 918h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6240. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8918h**

Figure 14-2076. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6242. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.245 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 91Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 8 firewall.

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Table 14-6243. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 891Ch**

Figure 14-2077. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6245. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.246 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_CONTROL Register (Offset = 920h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6246. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8920h**

Figure 14-2078. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6248. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.247 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 924h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6249. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8924h**

Figure 14-2079. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6251. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6251. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.248 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 928h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6252. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8928h**

Figure 14-2080. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6254. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6254. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.249 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 92Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6255. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 892Ch**

Figure 14-2081. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6257. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6257. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.250 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 930h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6258. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8930h**

Figure 14-2082. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6260. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.251 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 934h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6261. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8934h**

Figure 14-2083. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6263. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.252 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 938h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6264. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8938h**

Figure 14-2084. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6266. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.253 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 93Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 9 firewall.

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Table 14-6267. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 893Ch**

Figure 14-2085. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6269. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.254 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_CONTROL Register (Offset = 940h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6270. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8940h**

Figure 14-2086. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6272. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.255 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 944h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6273. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8944h**

Figure 14-2087. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6275. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6275. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.256 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 948h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6276. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8948h**

Figure 14-2088. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6278. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6278. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.257 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 94Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6279. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 894Ch

Figure 14-2089. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6281. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6281. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.258 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 950h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6282. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8950h**

Figure 14-2090. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6284. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.259 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 954h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6285. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8954h**

Figure 14-2091. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6287. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.260 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 958h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6288. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8958h**

Figure 14-2092. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6290. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.261 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 95Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 10 firewall.

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Table 14-6291. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 895Ch**

Figure 14-2093. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6293. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.262 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_CONTROL Register (Offset = 960h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6294. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8960h**

Figure 14-2094. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6296. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.263 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 964h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6297. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8964h**

Figure 14-2095. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6299. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6299. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.264 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 968h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6300. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8968h**

Figure 14-2096. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6302. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6302. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.265 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 96Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6303. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 896Ch**

Figure 14-2097. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6305. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6305. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.266
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 970h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6306. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8970h**

Figure 14-2098. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6308. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.267 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 974h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6309. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8974h**

Figure 14-2099. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6311. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.268 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 978h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6312. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8978h**

Figure 14-2100. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6314. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.269 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 97Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 11 firewall.

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Table 14-6315. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 897Ch**

Figure 14-2101. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6317. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.270 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_CONTROL Register (Offset = 980h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6318. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8980h**

Figure 14-2102. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6320. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.271 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 984h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6321. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8984h**

Figure 14-2103. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6323. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6323. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.272 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 988h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6324. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8988h**

Figure 14-2104. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6326. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6326. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.273 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 98Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6327. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 898Ch**

Figure 14-2105. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6329. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6329. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.274 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 990h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6330. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8990h**

Figure 14-2106. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6332. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.275
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 994h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6333. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8994h**

Figure 14-2107. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6335. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.276 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 998h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6336. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8998h**

Figure 14-2108. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6338. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.277 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 99Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 12 firewall.

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Table 14-6339. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 899Ch**

Figure 14-2109. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6341. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.278 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_CONTROL Register (Offset = 9A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6342. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89A0h**

Figure 14-2110. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6344. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.279 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 9A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6345. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89A4h**

Figure 14-2111. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6347. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6347. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.280 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 9A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6348. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89A8h**

Figure 14-2112. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6350. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6350. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.281 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 9ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6351. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89ACh**

Figure 14-2113. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6353. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6353. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.282
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 9B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6354. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 89B0h**

Figure 14-2114. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6356. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.283 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 9B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6357. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89B4h**

Figure 14-2115. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6359. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.284 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 9B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6360. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89B8h**

Figure 14-2116. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6362. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.285 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 9BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 13 firewall.

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Table 14-6363. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89BCh**

Figure 14-2117. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							

7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6365. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.286 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_CONTROL Register (Offset = 9C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6366. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 89C0h**

Figure 14-2118. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6368. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.287 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 9C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6369. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89C4h**

Figure 14-2119. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6371. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6371. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.288 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 9C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6372. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89C8h**

Figure 14-2120. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6374. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6374. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.289 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 9CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6375. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89CCh**

Figure 14-2121. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6377. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6377. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.290 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 9D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6378. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89D0h**

Figure 14-2122. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6380. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.291 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register

1

CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 9D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6381. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89D4h**

Figure 14-2123. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6383. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.292 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 9D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6384. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89D8h**

Figure 14-2124. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6386. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.293 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 9DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 14 firewall.

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Table 14-6387. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89DCh**

Figure 14-2125. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6389. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.294 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_CONTROL Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_CONTROL Register (Offset = 9E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6390. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89E0h**

Figure 14-2126. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6392. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.295 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 9E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6393. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89E4h**

Figure 14-2127. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6395. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6395. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.296 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 9E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6396. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89E8h

Figure 14-2128. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6398. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6398. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.297 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 9ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6399. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89ECh**

Figure 14-2129. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6401. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6401. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.298 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 9F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6402. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89F0h**

Figure 14-2130. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6404. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.299
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 9F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6405. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89F4h**

Figure 14-2131. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6407. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.300 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 9F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6408. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89F8h**

Figure 14-2132. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6410. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.301 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register

1 CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 9FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_DM_clk1_to_SCRP_32b_DM_clk4_l0 region 15 firewall.

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Table 14-6411. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 89FCh**

Figure 14-2133. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6413. CBASS_FW_BR_SCRM_DM_CLK1_TO_SCRP_32B_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.302 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6414. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C00h**

Figure 14-2134. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6416. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6416. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.303 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6417. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C04h**

Figure 14-2135. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6419. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6419. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.304 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6420. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C08h**

Figure 14-2136. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6422. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6422. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.305 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

Return to Summary Table

Table 14-6423. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C0Ch

Figure 14-2137. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6425. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6425. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.306 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6426. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8C10h**

Figure 14-2138. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6428. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.307 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6429. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C14h**

Figure 14-2139. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6431. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.308 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6432. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C18h**

Figure 14-2140. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6434. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.309 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-6435. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C1Ch**

Figure 14-2141. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6437. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.310 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6438. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8C20h**

Figure 14-2142. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6440. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6440. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.311 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6441. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C24h**

Figure 14-2143. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6443. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6443. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.312 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6444. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C28h

Figure 14-2144. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6446. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6446. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.313 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6447. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C2Ch**

Figure 14-2145. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6449. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6449. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.314
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6450. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C30h**

Figure 14-2146. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6452. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.315 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6453. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C34h**

Figure 14-2147. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6455. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.316 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6456. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C38h

Figure 14-2148. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6458. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.317 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-6459. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C3Ch**

Figure 14-2149. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6461. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.318 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6462. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C40h**

Figure 14-2150. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6464. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6464. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.319 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6465. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C44h**

Figure 14-2151. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6467. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6467. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.320 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6468. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C48h**

Figure 14-2152. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6470. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6470. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.321 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6471. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C4Ch**

Figure 14-2153. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6473. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6473. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.322 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6474. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C50h**

Figure 14-2154. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6476. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.323 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6477. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C54h**

Figure 14-2155. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6479. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.324 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6480. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C58h**

Figure 14-2156. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6482. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.325 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-6483. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C5Ch**

Figure 14-2157. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6485. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.326 *CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register*

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6486. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C60h**

Figure 14-2158. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6488. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6488. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.327
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6489. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C64h

Figure 14-2159. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6491. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6491. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.328 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6492. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C68h

Figure 14-2160. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6494. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6494. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.329 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6495. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C6Ch**

Figure 14-2161. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6497. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6497. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.330
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6498. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C70h**

Figure 14-2162. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6500. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.331

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6501. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8C74h**

Figure 14-2163. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6503. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.332 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6504. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C78h

Figure 14-2164. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6506. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.333 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-6507. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C7Ch**

Figure 14-2165. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6509. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.334

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6510. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C80h**

Figure 14-2166. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6512. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6512. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.335
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6513. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C84h**

Figure 14-2167. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6515. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6515. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.336 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6516. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C88h**

Figure 14-2168. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6518. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6518. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.337 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6519. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C8Ch**

Figure 14-2169. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6521. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6521. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.338 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6522. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C90h

Figure 14-2170. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6524. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.339 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6525. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C94h**

Figure 14-2171. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6527. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.340 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6528. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C98h**

Figure 14-2172. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6530. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.341 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-6531. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8C9Ch**

Figure 14-2173. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6533. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.342 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6534. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CA0h**

Figure 14-2174. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6536. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6536. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.343

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6537. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CA4h**

Figure 14-2175. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6539. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6539. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.344 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6540. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CA8h**

Figure 14-2176. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6542. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6542. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.345 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6543. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CACh

Figure 14-2177. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6545. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6545. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.346
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6546. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CB0h

Figure 14-2178. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6548. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.347 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6549. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CB4h**

Figure 14-2179. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6551. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.348 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6552. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CB8h**

Figure 14-2180. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6554. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.349 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-6555. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CBCh**

Figure 14-2181. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6557. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.350 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6558. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CC0h

Figure 14-2182. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6560. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6560. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.351 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6561. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CC4h**

Figure 14-2183. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6563. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6563. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.352 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6564. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CC8h**

Figure 14-2184. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6566. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6566. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.353 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6567. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CCCh**

Figure 14-2185. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6569. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6569. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.354 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6570. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CD0h**

Figure 14-2186. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6572. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.355 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6573. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CD4h**

Figure 14-2187. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6575. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.356 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6576. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CD8h**

Figure 14-2188. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6578. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.357 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-6579. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CDCh**

Figure 14-2189. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6581. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.358 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6582. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CE0h**

Figure 14-2190. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6584. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6584. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.359 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6585. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CE4h**

Figure 14-2191. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6587. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6587. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.360 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6588. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CE8h**

Figure 14-2192. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6590. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6590. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.361 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6591. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CECh**

Figure 14-2193. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6593. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6593. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.362 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6594. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CF0h

Figure 14-2194. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6596. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.363

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6597. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CF4h**

Figure 14-2195. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6599. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.364 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6600. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CF8h**

Figure 14-2196. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6602. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.365 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-6603. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8CFCh**

Figure 14-2197. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6605. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.366 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register (Offset = D00h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6606. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D00h**

Figure 14-2198. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6608. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6608. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.367 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register (Offset = D04h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6609. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D04h**

Figure 14-2199. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6611. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6611. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.368 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register (Offset = D08h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6612. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D08h**

Figure 14-2200. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6614. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6614. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.369 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register (Offset = D0Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6615. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D0Ch

Figure 14-2201. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6617. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6617. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.370 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = D10h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6618. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D10h**

Figure 14-2202. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6620. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.371 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = D14h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6621. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D14h**

Figure 14-2203. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6623. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.372 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = D18h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6624. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D18h**

Figure 14-2204. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6626. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.373 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = D1Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-6627. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D1Ch**

Figure 14-2205. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6629. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.374

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register (Offset = D20h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6630. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D20h**

Figure 14-2206. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6632. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6632. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.375 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register (Offset = D24h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6633. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D24h

Figure 14-2207. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6635. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6635. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.376 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register (Offset = D28h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6636. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D28h**

Figure 14-2208. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6638. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6638. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.377 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register (Offset = D2Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6639. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D2Ch**

Figure 14-2209. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6641. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6641. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.378 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = D30h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6642. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D30h**

Figure 14-2210. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6644. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.379 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = D34h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6645. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D34h**

Figure 14-2211. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6647. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.380 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = D38h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6648. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D38h**

Figure 14-2212. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6650. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.381 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = D3Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-6651. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D3Ch**

Figure 14-2213. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6653. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.382 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register (Offset = D40h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6654. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D40h**

Figure 14-2214. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6656. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6656. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.383 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register (Offset = D44h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6657. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D44h**

Figure 14-2215. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-6659. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6659. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.384

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register (Offset = D48h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6660. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D48h**

Figure 14-2216. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6662. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6662. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.385 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register (Offset = D4Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6663. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D4Ch

Figure 14-2217. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6665. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6665. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.386
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = D50h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-6666. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D50h**

Figure 14-2218. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-6668. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.387 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = D54h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6669. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D54h**

Figure 14-2219. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6671. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.388 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = D58h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-6672. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D58h**

Figure 14-2220. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6674. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.389

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = D5Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-6675. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D5Ch**

Figure 14-2221. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6677. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.390 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register (Offset = D60h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6678. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D60h**

Figure 14-2222. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6680. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6680. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.391 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register (Offset = D64h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6681. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D64h

Figure 14-2223. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6683. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6683. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.392 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register (Offset = D68h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6684. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D68h

Figure 14-2224. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6686. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6686. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.393 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register (Offset = D6Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6687. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D6Ch**

Figure 14-2225. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6689. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6689. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.394 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = D70h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6690. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D70h**

Figure 14-2226. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6692. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.395
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = D74h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6693. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D74h**

Figure 14-2227. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6695. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.396 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = D78h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6696. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D78h

Figure 14-2228. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6698. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.397 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = D7Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-6699. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D7Ch**

Figure 14-2229. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6701. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.398 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register (Offset = D80h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6702. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D80h**

Figure 14-2230. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6704. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6704. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.399 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register (Offset = D84h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6705. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D84h

Figure 14-2231. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6707. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6707. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.400 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register (Offset = D88h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

Return to Summary Table

Table 14-6708. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D88h**

Figure 14-2232. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6710. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6710. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.401 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register (Offset = D8Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6711. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D8Ch

Figure 14-2233. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6713. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6713. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.402 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = D90h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6714. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D90h**

Figure 14-2234. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6716. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.403 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = D94h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6717. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D94h

Figure 14-2235. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6719. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.404 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = D98h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6720. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D98h**

Figure 14-2236. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6722. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.405 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = D9Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-6723. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8D9Ch**

Figure 14-2237. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6725. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.406 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register (Offset = DA0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6726. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DA0h**

Figure 14-2238. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6728. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6728. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.407 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register (Offset = DA4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6729. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DA4h**

Figure 14-2239. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6731. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6731. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.408 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register (Offset = DA8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6732. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DA8h**

Figure 14-2240. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6734. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6734. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.409 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register (Offset = DACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6735. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DACh

Figure 14-2241. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6737. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6737. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.410
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = DB0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6738. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DB0h

Figure 14-2242. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6740. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.411

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = DB4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6741. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DB4h**

Figure 14-2243. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6743. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.412
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = DB8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6744. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DB8h**

Figure 14-2244. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6746. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.413 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = DBCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-6747. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 8DBCh**

Figure 14-2245. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6749. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.414 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register (Offset = DC0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6750. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DC0h**

Figure 14-2246. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6752. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6752. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.415 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register (Offset = DC4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6753. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DC4h**

Figure 14-2247. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6755. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6755. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.416 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register (Offset = DC8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6756. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DC8h**

Figure 14-2248. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6758. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6758. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.417 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register (Offset = DCCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6759. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DCCh**

Figure 14-2249. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6761. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6761. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.418 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = DD0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6762. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DD0h**

Figure 14-2250. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6764. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.419 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = DD4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6765. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DD4h**

Figure 14-2251. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6767. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.420 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = DD8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6768. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DD8h**

Figure 14-2252. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6770. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.421 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = DDCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-6771. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DDCh**

Figure 14-2253. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6773. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.422 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register (Offset = DE0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6774. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DE0h**

Figure 14-2254. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6776. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6776. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.423 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register (Offset = DE4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6777. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DE4h

Figure 14-2255. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6779. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6779. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.424 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register (Offset = DE8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6780. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DE8h**

Figure 14-2256. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6782. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6782. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.425 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register (Offset = DECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6783. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DECh**

Figure 14-2257. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6785. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6785. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.426 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = DF0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6786. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DF0h**

Figure 14-2258. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6788. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.427 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = DF4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6789. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DF4h**

Figure 14-2259. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6791. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.428 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = DF8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6792. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DF8h

Figure 14-2260. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6794. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.429 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = DFCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-6795. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 8DFCh**

Figure 14-2261. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6797. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.430 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = 1000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6798. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9000h**

Figure 14-2262. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6800. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6800. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.431 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 1004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6801. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 9004h

Figure 14-2263. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6803. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6803. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.432
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 1008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6804. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9008h**

Figure 14-2264. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-6806. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6806. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.433 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 100Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6807. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 900Ch**

Figure 14-2265. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6809. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6809. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.434 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6810. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 9010h

Figure 14-2266. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6812. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.435
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6813. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9014h**

Figure 14-2267. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6815. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.436 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6816. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9018h**

Figure 14-2268. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6818. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.437 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 0 firewall.

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Table 14-6819. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 901Ch**

Figure 14-2269. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6821. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.438 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = 1020h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6822. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9020h**

Figure 14-2270. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6824. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6824. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.439 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 1024h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6825. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9024h**

Figure 14-2271. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6827. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6827. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.440 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 1028h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6828. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9028h**

Figure 14-2272. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6830. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6830. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.441 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 102Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6831. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 902Ch**

Figure 14-2273. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6833. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6833. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.442
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 1030h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6834. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9030h**

Figure 14-2274. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-6836. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.443 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 1034h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6837. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9034h**

Figure 14-2275. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6839. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.444 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 1038h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6840. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9038h**

Figure 14-2276. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6842. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.445 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 103Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 1 firewall.

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Table 14-6843. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 903Ch**

Figure 14-2277. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6845. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.446 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = 1040h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6846. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9040h**

Figure 14-2278. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6848. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6848. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.447 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 1044h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6849. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9044h**

Figure 14-2279. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6851. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6851. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.448 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 1048h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6852. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9048h**

Figure 14-2280. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6854. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6854. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.449 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 104Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6855. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 904Ch**

Figure 14-2281. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6857. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6857. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.450 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 1050h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6858. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9050h**

Figure 14-2282. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6860. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.451 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 1054h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6861. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9054h**

Figure 14-2283. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6863. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.452 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 1058h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6864. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9058h**

Figure 14-2284. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6866. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.453
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 105Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 2 firewall.

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Table 14-6867. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 905Ch**

Figure 14-2285. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6869. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.454
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = 1060h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6870. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9060h**

Figure 14-2286. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6872. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6872. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.455 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 1064h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6873. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9064h**

Figure 14-2287. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6875. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6875. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.456 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 1068h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6876. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9068h**

Figure 14-2288. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6878. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6878. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.457 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 106Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6879. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 906Ch**

Figure 14-2289. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6881. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6881. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.458
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 1070h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6882. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9070h**

Figure 14-2290. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6884. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.459 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 1074h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6885. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9074h**

Figure 14-2291. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6887. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.460 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 1078h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6888. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9078h**

Figure 14-2292. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6890. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.461 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 107Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 3 firewall.

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Table 14-6891. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 907Ch**

Figure 14-2293. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6893. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.462 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = 1080h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6894. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9080h**

Figure 14-2294. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6896. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6896. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.463 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 1084h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6897. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9084h**

Figure 14-2295. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6899. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6899. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.464 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 1088h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6900. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9088h**

Figure 14-2296. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6902. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6902. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.465 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 108Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6903. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 908Ch**

Figure 14-2297. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6905. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6905. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.466 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 1090h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6906. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9090h**

Figure 14-2298. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6908. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.467 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 1094h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6909. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9094h**

Figure 14-2299. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6911. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.468 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 1098h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6912. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 9098h

Figure 14-2300. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6914. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.469 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 109Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 4 firewall.

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Table 14-6915. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 909Ch**

Figure 14-2301. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-6917. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.470 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = 10A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6918. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4500 90A0h**

Figure 14-2302. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6920. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6920. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.471
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 10A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6921. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90A4h**

Figure 14-2303. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6923. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6923. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.472 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 10A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6924. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90A8h**

Figure 14-2304. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6926. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6926. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.473 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 10ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6927. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90ACh**

Figure 14-2305. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6929. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6929. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.474 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 10B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6930. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90B0h**

Figure 14-2306. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-6932. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.475 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 10B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6933. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90B4h**

Figure 14-2307. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6935. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.476 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 10B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6936. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90B8h**

Figure 14-2308. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6938. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.477 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 10BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 5 firewall.

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Table 14-6939. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90BCh**

Figure 14-2309. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6941. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.478 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = 10C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6942. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90C0h**

Figure 14-2310. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6944. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6944. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.479 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 10C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6945. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 90C4h

Figure 14-2311. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6947. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6947. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.480 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 10C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6948. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90C8h**

Figure 14-2312. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6950. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6950. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.481 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 10CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6951. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 90CCh

Figure 14-2313. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6953. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6953. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.482 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 10D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6954. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90D0h**

Figure 14-2314. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-6956. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.483
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 10D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6957. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90D4h**

Figure 14-2315. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6959. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.484 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 10D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6960. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90D8h**

Figure 14-2316. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-6962. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.485 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 10DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 6 firewall.

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Table 14-6963. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90DCh**

Figure 14-2317. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6965. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.486 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = 10E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6966. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 90E0h

Figure 14-2318. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6968. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6968. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.487 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 10E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6969. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90E4h**

Figure 14-2319. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6971. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6971. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.488 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 10E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6972. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90E8h**

Figure 14-2320. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6974. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6974. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.489 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

1

CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 10ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6975. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90ECh**

Figure 14-2321. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6977. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6977. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.490 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 10F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6978. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 90F0h

Figure 14-2322. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-6980. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.491 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 10F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6981. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90F4h**

Figure 14-2323. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-6983. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.492
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 10F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6984. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90F8h**

Figure 14-2324. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-6986. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.493
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

1
CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 10FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0.slv region 7 firewall.

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Table 14-6987. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 90FCh**

Figure 14-2325. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-6989. CBASS_FW_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.494 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_CONTROL Register (Offset = 1400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-6990. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9400h**

Figure 14-2326. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-6992. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.495 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 1404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-6993. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9404h**

Figure 14-2327. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6995. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6995. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.496 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 1408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-6996. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9408h**

Figure 14-2328. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6998. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-6998. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.497 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 140Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-6999. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 940Ch**

Figure 14-2329. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7001. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7001. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.498 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 2B604000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-7002. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9410h**

Figure 14-2330. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2B604h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2B604h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2B604h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7004. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2B604h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.499 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-7005. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9414h**

Figure 14-2331. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7007. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.500 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = 2B604FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-7008. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9418h**

Figure 14-2332. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B604h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B604h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2B604h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7010. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2B604h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.501 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 0 firewall.

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Table 14-7011. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 941Ch**

Figure 14-2333. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7013. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.502 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_CONTROL Register (Offset = 1420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7014. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9420h**

Figure 14-2334. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7016. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.503 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 1424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7017. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9424h**

Figure 14-2335. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7019. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7019. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.504 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 1428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7020. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9428h**

Figure 14-2336. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7022. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7022. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.505 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 142Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7023. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 942Ch**

Figure 14-2337. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7025. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7025. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.506 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1430h) [reset = 2B607000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7026. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9430h**

Figure 14-2338. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2B607h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
2B607h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2B607h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-7028. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2B607h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.507 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7029. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9434h**

Figure 14-2339. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7031. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.508 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1438h) [reset = 2B607FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7032. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9438h**

Figure 14-2340. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2B607h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
2B607h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2B607h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7034. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2B607h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.509 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 143Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 1 firewall.

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Table 14-7035. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 943Ch**

Figure 14-2341. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7037. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.510 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_CONTROL Register (Offset = 1440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7038. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9440h**

Figure 14-2342. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7040. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.511 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 1444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7041. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9444h**

Figure 14-2343. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7043. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7043. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.512 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 1448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7044. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9448h**

Figure 14-2344. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7046. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7046. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.513 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 144Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7047. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 944Ch**

Figure 14-2345. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7049. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7049. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.514 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1450h) [reset = 2B605000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7050. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9450h**

Figure 14-2346. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2B605h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2B605h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2B605h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7052. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2B605h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.515 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7053. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9454h**

Figure 14-2347. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7055. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.516 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1458h) [reset = 2B605FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7056. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9458h**

Figure 14-2348. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B605h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B605h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2B605h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7058. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2B605h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.517 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 145Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 2 firewall.

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Table 14-7059. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 945Ch**

Figure 14-2349. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7061. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.518 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_CONTROL Register (Offset = 1460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7062. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9460h**

Figure 14-2350. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7064. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.519 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 1464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7065. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9464h**

Figure 14-2351. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7067. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7067. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.520 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 1468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7068. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9468h**

Figure 14-2352. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7070. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7070. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.521 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 146Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7071. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 946Ch**

Figure 14-2353. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7073. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7073. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.522 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1470h) [reset = 2C000000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7074. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9470h**

Figure 14-2354. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2C000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2C000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2C000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7076. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2C000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.523 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7077. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9474h**

Figure 14-2355. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7079. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.524 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1478h) [reset = 2C000FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7080. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 9478h**

Figure 14-2356. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2C000h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
2C000h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2C000h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7082. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2C000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.525 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 147Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62a_vpac_wrap_main_0.cfg_slv region 3 firewall.

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Table 14-7083. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4500 947Ch**

Figure 14-2357. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7085. CBASS_FW_ISAM62A_VPAC_WRAP_MAIN_0_CFG_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.526 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-7086. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4000h**

Figure 14-2358. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7088. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7088. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.527 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-7089. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4010h**

Figure 14-2359. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7091. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.528 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-7092. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4014h**

Figure 14-2360. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7094. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.529 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-7095. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4018h**

Figure 14-2361. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7097. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.530 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-7098. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 401Ch**

Figure 14-2362. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7100. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.531 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register (Offset = 20h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-7101. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4020h**

Figure 14-2363. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7103. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7103. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.532 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-7104. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4030h**

Figure 14-2364. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7106. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.533 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-7107. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4034h**

Figure 14-2365. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7109. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.534 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-7110. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4038h**

Figure 14-2366. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7112. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.535 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-7113. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 403Ch**

Figure 14-2367. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7115. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.536 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register (Offset = 40h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-7116. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4040h

Figure 14-2368. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7118. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7118. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.537 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-7119. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4050h**

Figure 14-2369. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7121. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.538 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-7122. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4054h**

Figure 14-2370. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7124. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.539 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-7125. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4058h**

Figure 14-2371. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7127. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.540 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-7128. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 405Ch**

Figure 14-2372. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7130. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.541 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register (Offset = 60h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-7131. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4060h**

Figure 14-2373. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">D4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7133. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7133. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.542 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-7134. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4070h**

Figure 14-2374. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7136. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.543 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-7137. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4074h**

Figure 14-2375. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7139. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.544 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-7140. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4078h**

Figure 14-2376. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7142. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.545 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-7143. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 407Ch**

Figure 14-2377. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7145. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.546 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 80h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 4 ISC.

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Table 14-7146. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4080h**

Figure 14-2378. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-7148. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7148. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.547 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-7149. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	**4581 4400h**

Figure 14-2379. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7151. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7151. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.548 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-7152. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4410h**

Figure 14-2380. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7154. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.549 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-7155. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4414h**

Figure 14-2381. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7157. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.550 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-7158. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4418h**

Figure 14-2382. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7160. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.551 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-7161. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 441Ch**

Figure 14-2383. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7163. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.552 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register (Offset = 420h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-7164. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4420h**

Figure 14-2384. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7166. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7166. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.553 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-7167. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4430h**

Figure 14-2385. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7169. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.554 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-7170. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4434h**

Figure 14-2386. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7172. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.555 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-7173. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4438h**

Figure 14-2387. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7175. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.556 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-7176. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 443Ch**

Figure 14-2388. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7178. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.557 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register (Offset = 440h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-7179. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4440h**

Figure 14-2389. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7181. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7181. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.558 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-7182. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4450h**

Figure 14-2390. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7184. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.559 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-7185. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4454h**

Figure 14-2391. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7187. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.560 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-7188. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4458h**

Figure 14-2392. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7190. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.561 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-7191. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 445Ch**

Figure 14-2393. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7193. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.562 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register (Offset = 460h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-7194. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4460h**

Figure 14-2394. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7196. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7196. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.563 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-7197. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4470h**

Figure 14-2395. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7199. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.564 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-7200. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4474h**

Figure 14-2396. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7202. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.565 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-7203. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4478h**

Figure 14-2397. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7205. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.566 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-7206. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 447Ch**

Figure 14-2398. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7208. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.567 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 480h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 4 ISC.

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Table 14-7209. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4480h**

Figure 14-2399. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-7211. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7211. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.568 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-7212. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4800h**

Figure 14-2400. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7214. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7214. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.569 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-7215. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4810h**

Figure 14-2401. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7217. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.570 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-7218. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4814h**

Figure 14-2402. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7220. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.571 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator lpulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-7221. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4818h**

Figure 14-2403. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7223. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.572 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-7224. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 481Ch**

Figure 14-2404. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7226. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.573 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register (Offset = 820h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-7227. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4820h**

Figure 14-2405. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7229. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7229. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.574 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-7230. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4830h**

Figure 14-2406. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7232. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.575 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-7233. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4834h**

Figure 14-2407. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7235. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.576 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-7236. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4838h**

Figure 14-2408. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7238. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.577 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-7239. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 483Ch**

Figure 14-2409. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7241. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.578 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register (Offset = 840h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-7242. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4840h

Figure 14-2410. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-7244. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7244. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.579 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-7245. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4850h**

Figure 14-2411. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7247. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.580 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-7248. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4854h**

Figure 14-2412. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7250. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.581 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-7251. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4858h**

Figure 14-2413. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7253. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.582 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-7254. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 485Ch**

Figure 14-2414. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7256. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.583 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register (Offset = 860h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-7257. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4860h**

Figure 14-2415. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">D4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7259. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7259. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.584 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-7260. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4870h**

Figure 14-2416. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-7262. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.585 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-7263. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4874h**

Figure 14-2417. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7265. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.586 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-7266. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4878h**

Figure 14-2418. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7268. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.587 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-7269. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 487Ch**

Figure 14-2419. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7271. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.588 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 880h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 4 ISC.

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Table 14-7272. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**4581 4880h**

Figure 14-2420. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-7274. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7274. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.589 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7275. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3000h**

Figure 14-2421. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7277. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.590 CBASS_GLB_DESTINATION_ID Register

1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7278. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3004h**

Figure 14-2422. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-7280. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.591 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-7281. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3020h**

Figure 14-2423. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-7283. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.592 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7284. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3024h**

Figure 14-2424. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7286. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.593 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7287. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3028h**

Figure 14-2425. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7289. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.3.2.594 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7290. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 302Ch**

Figure 14-2426. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7292. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.595 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7293. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3030h**

Figure 14-2427. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7295. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.596 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7296. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3034h**

Figure 14-2428. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7298. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7298. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.597 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7299. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3038h**

Figure 14-2429. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-7301. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.598 CBASS_GLB_EXCEPTION_PEND_SET Register

1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-7302. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3040h**

Figure 14-2430. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-7304. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.599 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-7305. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45B0 3044h**

Figure 14-2431. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-7307. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.600 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register

1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register (Offset = 100h) [reset = 7000h]

The Map Register defines the fields for the initiator WKUP_R5FSS0 CPU0 Read Port per channel

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Table 14-7308. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45D1 4100h**

Figure 14-2432. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-7310. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.3.2.601 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register

1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register (Offset = 500h) [reset = 7000h]

The Map Register defines the fields for the initiator WKUP_R5FSS0 CPU0 Write Port per channel

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Table 14-7311. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45D1 4500h**

Figure 14-2433. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-7313. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.3.2.602 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register

1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst per channel.

Return to Summary Table

Table 14-7314. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	**45D1 4900h**

Figure 14-2434. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RSVD		
R/W				NONE			
0h				0h	0h		

Table 14-7316. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.4 cbass_central

cbass_central

14.1.4.1 cbass_central Summaries

cbass_central Summaries

Table 14-7317. CBASS_ERR Registers, Base Address=3F01 2000h, Length=1024

Offset	Length	Register Name	CBASS_CENTRAL2 Physical Address
0h	32	CBASS_ERR_PID	3F01 2000h
4h	32	CBASS_ERR_DESTINATION_ID	3F01 2004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	3F01 2024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	3F01 2028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	3F01 202Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	3F01 2030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	3F01 2034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	3F01 2038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	3F01 2050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	3F01 2054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	3F01 2058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	3F01 205Ch
60h	32	CBASS_ERR_EOI	3F01 2060h

Table 14-7318. CBASS_FW Registers, Base Address=4501 0000h, Length=4096

Offset	Length	Register Name	CBASS_CENTRAL2 Physical Address
800h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_CONTROL	4501 0800h
804h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0	4501 0804h
808h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1	4501 0808h
80Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2	4501 080Ch
810h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_L	4501 0810h
814h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_H	4501 0814h
818h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_L	4501 0818h
81Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_H	4501 081Ch
820h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_CONTROL	4501 0820h
824h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0	4501 0824h
828h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1	4501 0828h
82Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2	4501 082Ch

Table 14-7318. CBASS_FW Registers, Base Address=4501 0000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_CENTRAL2 Physical Address
830h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_L	4501 0830h
834h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_H	4501 0834h
838h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_L	4501 0838h
83Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_H	4501 083Ch
840h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_CONTROL	4501 0840h
844h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0	4501 0844h
848h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1	4501 0848h
84Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2	4501 084Ch
850h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_L	4501 0850h
854h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_H	4501 0854h
858h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_L	4501 0858h
85Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_H	4501 085Ch
860h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_CONTROL	4501 0860h
864h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0	4501 0864h
868h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1	4501 0868h
86Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2	4501 086Ch
870h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_L	4501 0870h
874h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_H	4501 0874h
878h	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_L	4501 0878h
87Ch	32	CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_H	4501 087Ch

Table 14-7319. CBASS_GLB Registers, Base Address=45B0 4000h, Length=1024

Offset	Length	Register Name	CBASS_CENTRAL2 Physical Address
0h	32	CBASS_GLB_PID	45B0 4000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 4004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 4020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 4024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 4028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 402Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 4030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 4034h

Table 14-7319. CBASS_GLB Registers, Base Address=45B0 4000h, Length=1024 (continued)

Offset	Length	Register Name	CBASS_CENTRAL2 Physical Address
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 4038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 4040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 4044h

14.1.4.2 cbass_central Registers

cbass_central Registers

14.1.4.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7320. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2000h**

Figure 14-2435. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7322. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7323. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2004h**

Figure 14-2436. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-7325. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7326. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	3F01 2024h

Figure 14-2437. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-7328. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7329. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2028h**

Figure 14-2438. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7331. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.4.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7332. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 202Ch**

Figure 14-2439. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7334. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7335. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	3F01 2030h

Figure 14-2440. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7337. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7338. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2034h**

Figure 14-2441. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-7340. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

Table 14-7340. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7341. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2038h**

Figure 14-2442. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7343. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-7344. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2050h**

Figure 14-2443. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-7346. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-7347. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2054h**

Figure 14-2444. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-7349. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-7350. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2058h**

Figure 14-2445. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-7352. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-7353. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 205Ch**

Figure 14-2446. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-7355. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-7356. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**3F01 2060h**

Figure 14-2447. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-7358. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32b_dmsc_hsm_rst_mod_g_rst_n

14.1.4.2.14 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_CONTROL Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7359. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0800h

Figure 14-2448. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7361. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.15 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7362. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0804h**

Figure 14-2449. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7364. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7364. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.16 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7365. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0808h

Figure 14-2450. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7367. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7367. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.17 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7368. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 080Ch

Figure 14-2451. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7370. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7370. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.18 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7371. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0810h**

Figure 14-2452. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7373. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.19 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7374. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0814h**

Figure 14-2453. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7376. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.20 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7377. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0818h**

Figure 14-2454. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7379. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.21 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 0 firewall.

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Table 14-7380. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 081Ch**

Figure 14-2455. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7382. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.22 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_CONTROL Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

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Table 14-7383. Instance Table

Instance Name	**Physical Address**
CBASS_CENTRAL2	**4501 0820h**

Figure 14-2456. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7385. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.23 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

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Table 14-7386. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0824h

Figure 14-2457. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7388. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7388. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.24 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

Return to Summary Table

Table 14-7389. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0828h

Figure 14-2458. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7391. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7391. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.25 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

Return to Summary Table

Table 14-7392. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 082Ch

Figure 14-2459. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7394. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7394. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.26
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

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Table 14-7395. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0830h**

Figure 14-2460. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7397. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.27
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register

1
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

Return to Summary Table

Table 14-7398. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0834h**

Figure 14-2461. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7400. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.28 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

Return to Summary Table

Table 14-7401. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0838h**

Figure 14-2462. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7403. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.29 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 1 firewall.

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Table 14-7404. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 083Ch**

Figure 14-2463. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7406. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.30 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_CONTROL Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7407. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0840h**

Figure 14-2464. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7409. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.31 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7410. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0844h

Figure 14-2465. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7412. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7412. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.32 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7413. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0848h**

Figure 14-2466. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7415. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7415. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.33 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7416. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 084Ch**

Figure 14-2467. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7418. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7418. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.34
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register

1
CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7419. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0850h**

Figure 14-2468. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7421. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.35 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7422. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0854h**

Figure 14-2469. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7424. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.36 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7425. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0858h**

Figure 14-2470. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7427. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.37 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 2 firewall.

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Table 14-7428. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 085Ch**

Figure 14-2471. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7430. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.38 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_CONTROL Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7431. Instance Table

Instance Name	**Physical Address**
CBASS_CENTRAL2	**4501 0860h**

Figure 14-2472. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7433. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.39 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7434. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0864h

Figure 14-2473. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7436. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7436. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.40 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7437. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0868h

Figure 14-2474. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7439. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7439. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.41 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7440. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 086Ch

Figure 14-2475. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7442. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7442. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.42 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7443. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	4501 0870h

Figure 14-2476. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7445. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.43 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7446. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0874h**

Figure 14-2477. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7448. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.44 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7449. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 0878h**

Figure 14-2478. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7451. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.45 CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register

1

CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRP_32b_dmsc_hsm_to_scrp_hsm_clk2_l0 region 3 firewall.

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Table 14-7452. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**4501 087Ch**

Figure 14-2479. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7454. CBASS_FW_BR_SCRP_32B_DMSC_HSM_TO_SCRP_HSM_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.46 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-7455. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4000h**

Figure 14-2480. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7457. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.47 CBASS_GLB_DESTINATION_ID Register

1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7458. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4004h**

Figure 14-2481. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-7460. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.48 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-7461. Instance Table

Instance Name	**Physical Address**
CBASS_CENTRAL2	**45B0 4020h**

Figure 14-2482. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-7463. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.49 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7464. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4024h**

Figure 14-2483. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7466. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.50 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7467. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4028h**

Figure 14-2484. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7469. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.4.2.51 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7470. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	45B0 402Ch

Figure 14-2485. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7472. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.52 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7473. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4030h**

Figure 14-2486. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7475. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.53 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7476. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4034h**

Figure 14-2487. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-7478. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7478. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.54 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7479. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4038h**

Figure 14-2488. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-7481. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.55 CBASS_GLB_EXCEPTION_PEND_SET Register

1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-7482. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4040h**

Figure 14-2489. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-7484. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.2.56 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

Return to Summary Table

Table 14-7485. Instance Table

Instance Name	Physical Address
CBASS_CENTRAL2	**45B0 4044h**

Figure 14-2490. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7487. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5 cbass_dbg

cbass_dbg

14.1.5.1 cbass_dbg Summaries

cbass_dbg Summaries

Table 14-7488. CBASS_ERR Registers, Base Address=0020 0000h, Length=1024

Offset	Length	Register Name	CBASS_DBG0 Physical Address
0h	32	CBASS_ERR_PID	0020 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0020 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0020 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0020 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0020 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0020 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0020 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0020 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0020 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0020 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0020 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0020 005Ch
60h	32	CBASS_ERR_EOI	0020 0060h

14.1.5.2 cbass_dbg Registers

cbass_dbg Registers

14.1.5.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7489. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0000h**

Figure 14-2491. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7491. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7492. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0004h**

Figure 14-2492. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-7494. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7495. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0024h**

Figure 14-2493. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-7497. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7498. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0028h**

Figure 14-2494. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7500. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.5.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7501. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 002Ch

Figure 14-2495. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7503. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7504. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0030h

Figure 14-2496. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7506. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7507. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0034h**

Figure 14-2497. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-7509. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

Table 14-7509. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7510. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0038h**

Figure 14-2498. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7512. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-7513. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0050h**

Figure 14-2499. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-7515. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-7516. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0054h**

Figure 14-2500. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ENABLED_INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7518. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-7519. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0058h**

Figure 14-2501. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-7521. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-7522. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 005Ch**

Figure 14-2502. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-7524. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-7525. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0060h**

Figure 14-2503. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7527. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.6 cbass_fw

cbass_fw

14.1.6.1 cbass_fw Summaries

cbass_fw Summaries

Table 14-7528. CBASS_ERR Registers, Base Address=0022 0000h, Length=1024

Offset	Length	Register Name	CBASS_FW0 Physical Address
0h	32	CBASS_ERR_PID	0022 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0022 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0022 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0022 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0022 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0022 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0022 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0022 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0022 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0022 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0022 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0022 005Ch
60h	32	CBASS_ERR_EOI	0022 0060h

14.1.6.2 cbass_fw Registers

cbass_fw Registers

14.1.6.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7529. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0000h**

Figure 14-2504. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7531. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7532. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0004h**

Figure 14-2505. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7534. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7535. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0024h**

Figure 14-2506. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7537. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7538. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0028h**

Figure 14-2507. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7540. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.6.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7541. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 002Ch**

Figure 14-2508. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7543. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7544. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0030h**

Figure 14-2509. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7546. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7547. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0034h**

Figure 14-2510. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-7549. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

Table 14-7549. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7550. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0038h**

Figure 14-2511. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-7552. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-7553. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0050h**

Figure 14-2512. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-7555. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-7556. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0054h**

Figure 14-2513. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-7558. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-7559. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0058h**

Figure 14-2514. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-7561. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-7562. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 005Ch**

Figure 14-2515. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-7564. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.6.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-7565. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0060h**

Figure 14-2516. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7567. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: scrp_32b_clk2_rst_mod_g_rst_n

14.1.7 cbass_infra

cbass_infra

14.1.7.1 cbass_infra Summaries

cbass_infra Summaries

Table 14-7568. CBASS_ERR Registers, Base Address=0021 0000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA1 Physical Address
0h	32	CBASS_ERR_PID	0021 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0021 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0021 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0021 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0021 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0021 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0021 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0021 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0021 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0021 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0021 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0021 005Ch
60h	32	CBASS_ERR_EOI	0021 0060h

14.1.7.2 cbass_infra Registers

cbass_infra Registers

14.1.7.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7569. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0000h

Figure 14-2517. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7571. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7572. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0004h**

Figure 14-2518. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7574. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7575. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0024h

Figure 14-2519. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-7577. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7578. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0028h**

Figure 14-2520. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7580. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.7.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7581. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 002Ch**

Figure 14-2521. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7583. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7584. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0030h**

Figure 14-2522. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7586. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7587. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0034h**

Figure 14-2523. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-7589. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

Table 14-7589. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7590. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0038h

Figure 14-2524. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-7592. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-7593. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0050h**

Figure 14-2525. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-7595. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-7596. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0054h**

Figure 14-2526. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-7598. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-7599. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0058h**

Figure 14-2527. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7601. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-7602. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 005Ch**

Figure 14-2528. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-7604. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.7.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-7605. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	**0021 0060h**

Figure 14-2529. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-7607. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_CLK4_cfg_rst_mod_g_rst_n

14.1.8 cbass_ipcss

cbass_ipcss

14.1.8.1 cbass_ipcss Summaries

cbass_ipcss Summaries

Table 14-7608. CBASS_ERR Registers, Base Address=0023 0000h, Length=1024

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
0h	32	CBASS_ERR_PID	0023 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0023 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0023 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0023 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0023 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0023 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0023 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0023 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0023 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0023 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0023 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0023 005Ch
60h	32	CBASS_ERR_EOI	0023 0060h

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL	4502 8000h
4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0	4502 8004h
8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1	4502 8008h
Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2	4502 800Ch
10h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L	4502 8010h
14h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H	4502 8014h
18h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L	4502 8018h
1Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H	4502 801Ch
20h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL	4502 8020h
24h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0	4502 8024h
28h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1	4502 8028h
2Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2	4502 802Ch

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
30h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L	4502 8030h
34h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H	4502 8034h
38h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L	4502 8038h
3Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H	4502 803Ch
40h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL	4502 8040h
44h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0	4502 8044h
48h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1	4502 8048h
4Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2	4502 804Ch
50h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L	4502 8050h
54h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H	4502 8054h
58h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L	4502 8058h
5Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H	4502 805Ch
60h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL	4502 8060h
64h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0	4502 8064h
68h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1	4502 8068h
6Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2	4502 806Ch
70h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L	4502 8070h
74h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H	4502 8074h
78h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L	4502 8078h
7Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H	4502 807Ch
80h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL	4502 8080h
84h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0	4502 8084h
88h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1	4502 8088h
8Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2	4502 808Ch
90h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L	4502 8090h
94h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H	4502 8094h

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
98h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L	4502 8098h
9Ch	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H	4502 809Ch
A0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL	4502 80A0h
A4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0	4502 80A4h
A8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1	4502 80A8h
ACh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2	4502 80ACh
B0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L	4502 80B0h
B4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H	4502 80B4h
B8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L	4502 80B8h
BCh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H	4502 80BCh
C0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL	4502 80C0h
C4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0	4502 80C4h
C8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1	4502 80C8h
CCh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2	4502 80CCh
D0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L	4502 80D0h
D4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H	4502 80D4h
D8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L	4502 80D8h
DCh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H	4502 80DCh
E0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL	4502 80E0h
E4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0	4502 80E4h
E8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1	4502 80E8h
ECh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2	4502 80ECh
F0h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L	4502 80F0h
F4h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H	4502 80F4h
F8h	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L	4502 80F8h
FCh	32	CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H	4502 80FCh

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
400h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL	4502 8400h
404h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0	4502 8404h
408h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1	4502 8408h
40Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2	4502 840Ch
410h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L	4502 8410h
414h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H	4502 8414h
418h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L	4502 8418h
41Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H	4502 841Ch
420h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL	4502 8420h
424h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0	4502 8424h
428h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1	4502 8428h
42Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2	4502 842Ch
430h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L	4502 8430h
434h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H	4502 8434h
438h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L	4502 8438h
43Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H	4502 843Ch
440h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL	4502 8440h
444h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0	4502 8444h
448h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1	4502 8448h
44Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2	4502 844Ch
450h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L	4502 8450h
454h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H	4502 8454h
458h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L	4502 8458h
45Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H	4502 845Ch
460h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL	4502 8460h
464h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0	4502 8464h

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
468h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1	4502 8468h
46Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2	4502 846Ch
470h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L	4502 8470h
474h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H	4502 8474h
478h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L	4502 8478h
47Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H	4502 847Ch
480h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL	4502 8480h
484h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0	4502 8484h
488h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1	4502 8488h
48Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2	4502 848Ch
490h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L	4502 8490h
494h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H	4502 8494h
498h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L	4502 8498h
49Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H	4502 849Ch
4A0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL	4502 84A0h
4A4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0	4502 84A4h
4A8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1	4502 84A8h
4ACh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2	4502 84ACh
4B0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L	4502 84B0h
4B4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H	4502 84B4h
4B8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L	4502 84B8h
4BCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H	4502 84BCh
4C0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL	4502 84C0h
4C4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0	4502 84C4h
4C8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1	4502 84C8h
4CCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2	4502 84CCh

Table 14-7609. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
4D0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L	4502 84D0h
4D4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H	4502 84D4h
4D8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L	4502 84D8h
4DCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H	4502 84DCh
4E0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL	4502 84E0h
4E4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0	4502 84E4h
4E8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1	4502 84E8h
4ECh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2	4502 84ECh
4F0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L	4502 84F0h
4F4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H	4502 84F4h
4F8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L	4502 84F8h
4FCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H	4502 84FCh

Table 14-7610. CBASS_GLB Registers, Base Address=45B0 1000h, Length=1024

Offset	Length	Register Name	CBASS_IPCSS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 1000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 1004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 1020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 1024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 1028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 102Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 1030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 1034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 1038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 1040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 1044h

14.1.8.2 cbass_ipcss Registers

cbass_ipcss Registers

14.1.8.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-7611. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0000h**

Figure 14-2530. CBASS_ERR_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">6h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-7613. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-7614. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0004h**

Figure 14-2531. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-7616. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-7617. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0024h**

Figure 14-2532. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-7619. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-7620. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0028h**

Figure 14-2533. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7622. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.8.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-7623. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 002Ch**

Figure 14-2534. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-7625. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-7626. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0030h**

Figure 14-2535. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-7628. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-7629. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0034h**

Figure 14-2536. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-7631. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

Table 14-7631. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-7632. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0038h**

Figure 14-2537. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7634. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-7635. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0050h**

Figure 14-2538. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-7637. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-7638. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0054h**

Figure 14-2539. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-7640. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-7641. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0058h**

Figure 14-2540. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-7643. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-7644. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 005Ch**

Figure 14-2541. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-7646. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-7647. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**0023 0060h**

Figure 14-2542. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-7649. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRM_64b_clk2_rst_mod_g_rst_n

14.1.8.2.14 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7650. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8000h**

Figure 14-2543. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7652. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.15 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

Return to Summary Table

Table 14-7653. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 8004h

Figure 14-2544. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7655. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7655. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.16 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7656. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8008h**

Figure 14-2545. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7658. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7658. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.17 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7659. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 800Ch**

Figure 14-2546. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7661. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7661. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.18 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 4D000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7662. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8010h**

Figure 14-2547. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4D000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4D000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">4D000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7664. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	4D000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.19 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7665. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8014h**

Figure 14-2548. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7667. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.20 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 4D07FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7668. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8018h**

Figure 14-2549. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
4D07Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
4D07Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
4D07Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7670. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	4D07Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.21 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7671. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 801Ch**

Figure 14-2550. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7673. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.22 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7674. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8020h**

Figure 14-2551. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7676. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.23 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7677. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8024h**

Figure 14-2552. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7679. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7679. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.24 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7680. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8028h**

Figure 14-2553. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7682. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7682. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.25 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7683. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 802Ch**

Figure 14-2554. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7685. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7685. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.26 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7686. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8030h**

Figure 14-2555. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7688. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.27 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7689. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8034h**

Figure 14-2556. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7691. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.28 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7692. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 8038h**

Figure 14-2557. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7694. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.29 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7695. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 803Ch**

Figure 14-2558. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7697. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.30 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7698. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8040h**

Figure 14-2559. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7700. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.31 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7701. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8044h**

Figure 14-2560. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7703. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7703. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.32 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7704. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 8048h

Figure 14-2561. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7706. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7706. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.33 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7707. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 804Ch**

Figure 14-2562. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7709. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7709. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.34 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7710. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8050h**

Figure 14-2563. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-7712. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.35 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7713. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 8054h**

Figure 14-2564. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7715. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.36 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7716. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8058h**

Figure 14-2565. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7718. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.37 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7719. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 805Ch**

Figure 14-2566. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7721. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.38 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7722. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8060h**

Figure 14-2567. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7724. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.39 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7725. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 8064h

Figure 14-2568. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7727. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7727. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.40 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7728. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8068h**

Figure 14-2569. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7730. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7730. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.41 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7731. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 806Ch**

Figure 14-2570. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7733. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7733. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.42 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7734. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8070h**

Figure 14-2571. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7736. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.43 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7737. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8074h**

Figure 14-2572. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7739. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.44 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7740. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8078h**

Figure 14-2573. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7742. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.45 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7743. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 807Ch**

Figure 14-2574. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7745. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.46 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7746. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8080h**

Figure 14-2575. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7748. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.47 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7749. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8084h**

Figure 14-2576. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7751. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7751. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.48 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7752. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8088h**

Figure 14-2577. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7754. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7754. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.49 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7755. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 808Ch**

Figure 14-2578. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7757. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7757. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.50 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register (Offset = 90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7758. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8090h**

Figure 14-2579. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7760. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.51 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register (Offset = 94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7761. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8094h**

Figure 14-2580. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7763. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.52 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register (Offset = 98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7764. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8098h**

Figure 14-2581. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7766. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.53 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register (Offset = 9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7767. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 809Ch**

Figure 14-2582. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7769. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.54 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register (Offset = A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7770. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80A0h**

Figure 14-2583. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7772. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.55 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register (Offset = A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7773. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80A4h**

Figure 14-2584. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7775. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7775. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.56 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register (Offset = A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7776. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80A8h**

Figure 14-2585. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7778. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7778. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.57 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register (Offset = ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7779. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80ACh**

Figure 14-2586. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7781. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7781. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.58 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register (Offset = B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7782. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80B0h**

Figure 14-2587. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7784. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.59 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register (Offset = B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7785. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80B4h**

Figure 14-2588. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7787. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.60 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register (Offset = B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7788. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80B8h**

Figure 14-2589. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7790. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.61 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register (Offset = BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7791. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80BCh**

Figure 14-2590. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7793. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.62 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7794. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80C0h**

Figure 14-2591. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7796. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.63 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register (Offset = C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7797. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80C4h**

Figure 14-2592. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7799. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7799. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.64 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register (Offset = C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7800. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 80C8h

Figure 14-2593. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7802. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7802. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.65 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register (Offset = CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7803. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80CCh**

Figure 14-2594. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7805. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7805. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.66 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register (Offset = D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7806. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80D0h**

Figure 14-2595. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7808. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.67 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register (Offset = D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7809. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80D4h**

Figure 14-2596. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7811. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.68 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register (Offset = D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7812. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80D8h**

Figure 14-2597. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7814. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.69 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register (Offset = DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7815. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80DCh**

Figure 14-2598. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7817. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.70 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register (Offset = E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7818. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80E0h**

Figure 14-2599. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7820. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.71 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register (Offset = E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7821. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 80E4h

Figure 14-2600. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7823. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7823. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.72 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register (Offset = E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7824. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80E8h**

Figure 14-2601. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7826. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7826. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.73 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register (Offset = ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7827. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80ECh**

Figure 14-2602. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7829. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7829. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.74 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register (Offset = F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7830. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80F0h**

Figure 14-2603. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7832. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.75 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register (Offset = F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7833. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80F4h**

Figure 14-2604. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-7835. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.76 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register (Offset = F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7836. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80F8h**

Figure 14-2605. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7838. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.77 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register (Offset = FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-7839. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 80FCh**

Figure 14-2606. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7841. CBASS_FW_IDMSS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.78 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7842. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8400h**

Figure 14-2607. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7844. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.79 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7845. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 8404h**

Figure 14-2608. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7847. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7847. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.80 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7848. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8408h**

Figure 14-2609. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7850. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7850. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.81 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7851. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 840Ch**

Figure 14-2610. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7853. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7853. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.82 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 43600000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7854. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8410h**

Figure 14-2611. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
43600h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
43600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
43600h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-7856. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	43600h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.83 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7857. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8414h**

Figure 14-2612. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7859. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.84 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = 4360FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7860. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8418h**

Figure 14-2613. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
4360Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
4360Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
4360Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7862. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	4360Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.85 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-7863. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 841Ch**

Figure 14-2614. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7865. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.86 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7866. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8420h**

Figure 14-2615. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7868. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.87 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7869. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8424h**

Figure 14-2616. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7871. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7871. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.88 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7872. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8428h**

Figure 14-2617. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7874. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7874. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.89 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7875. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 842Ch**

Figure 14-2618. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7877. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7877. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.90 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7878. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8430h**

Figure 14-2619. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7880. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.91 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7881. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8434h**

Figure 14-2620. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7883. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.92 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7884. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8438h**

Figure 14-2621. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7886. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.93 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-7887. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 843Ch**

Figure 14-2622. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7889. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.94 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7890. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8440h**

Figure 14-2623. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7892. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.95 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7893. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8444h**

Figure 14-2624. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7895. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7895. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.96 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7896. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8448h**

Figure 14-2625. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7898. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7898. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.97 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7899. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 844Ch**

Figure 14-2626. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7901. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7901. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.98 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7902. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8450h**

Figure 14-2627. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7904. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.99 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7905. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 8454h**

Figure 14-2628. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7907. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.100 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7908. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8458h**

Figure 14-2629. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7910. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.101 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-7911. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 845Ch**

Figure 14-2630. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7913. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.102 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7914. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8460h**

Figure 14-2631. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7916. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.103 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7917. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 8464h

Figure 14-2632. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7919. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7919. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.104 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7920. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8468h**

Figure 14-2633. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7922. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7922. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.105 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7923. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 846Ch**

Figure 14-2634. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7925. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7925. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.106 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7926. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8470h**

Figure 14-2635. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7928. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.107 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7929. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8474h**

Figure 14-2636. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7931. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.108 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7932. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8478h**

Figure 14-2637. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-7934. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.109 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-7935. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 847Ch**

Figure 14-2638. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7937. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.110 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7938. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8480h**

Figure 14-2639. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-7940. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.111 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7941. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8484h**

Figure 14-2640. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7943. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7943. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.112 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7944. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8488h**

Figure 14-2641. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7946. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7946. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.113 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7947. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 848Ch**

Figure 14-2642. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7949. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7949. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.114 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7950. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8490h**

Figure 14-2643. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-7952. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.115 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7953. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8494h**

Figure 14-2644. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-7955. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.116 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7956. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 8498h**

Figure 14-2645. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7958. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.117 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-7959. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	4502 849Ch

Figure 14-2646. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7961. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.118 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7962. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84A0h**

Figure 14-2647. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7964. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.119 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7965. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84A4h**

Figure 14-2648. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7967. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7967. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.120 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7968. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84A8h**

Figure 14-2649. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7970. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7970. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.121 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7971. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 84ACh**

Figure 14-2650. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7973. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7973. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.122 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7974. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84B0h**

Figure 14-2651. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7976. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.123 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7977. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84B4h**

Figure 14-2652. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7979. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.124 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7980. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84B8h**

Figure 14-2653. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-7982. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.125 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-7983. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84BCh**

Figure 14-2654. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-7985. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.126 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7986. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84C0h**

Figure 14-2655. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7988. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.127 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7989. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84C4h**

Figure 14-2656. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7991. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7991. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.128 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7992. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84C8h**

Figure 14-2657. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7994. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7994. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.129 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7995. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84CCh**

Figure 14-2658. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7997. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-7997. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.130 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-7998. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84D0h**

Figure 14-2659. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-8000. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.131 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-8001. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84D4h**

Figure 14-2660. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-8003. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.132 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-8004. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84D8h**

Figure 14-2661. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-8006. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.133 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-8007. Instance Table

Instance Name	**Physical Address**
CBASS_IPCSS0	**4502 84DCh**

Figure 14-2662. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-8009. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.134 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8010. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84E0h**

Figure 14-2663. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-8012. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.135 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8013. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84E4h**

Figure 14-2664. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8015. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-8015. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.136 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8016. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84E8h**

Figure 14-2665. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8018. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-8018. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.137 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8019. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84ECh**

Figure 14-2666. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8021. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-8021. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.138 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8022. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84F0h**

Figure 14-2667. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-8024. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.139 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8025. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84F4h**

Figure 14-2668. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-8027. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.140 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8028. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84F8h**

Figure 14-2669. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-8030. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.141 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register

1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-8031. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**4502 84FCh**

Figure 14-2670. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-8033. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.142 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-8034. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1000h**

Figure 14-2671. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-8036. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.143 CBASS_GLB_DESTINATION_ID Register

1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-8037. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1004h**

Figure 14-2672. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-8039. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.144 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-8040. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1020h**

Figure 14-2673. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-8042. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.145 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-8043. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1024h**

Figure 14-2674. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-8045. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.146 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-8046. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1028h**

Figure 14-2675. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8048. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.8.2.147 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-8049. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 102Ch**

Figure 14-2676. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-8051. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.148 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

Return to Summary Table

Table 14-8052. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1030h**

Figure 14-2677. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-8054. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.149 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

Return to Summary Table

Table 14-8055. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1034h**

Figure 14-2678. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-8057. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-8057. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.150 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-8058. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1038h**

Figure 14-2679. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-8060. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.151 CBASS_GLB_EXCEPTION_PEND_SET Register

1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-8061. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1040h**

Figure 14-2680. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-8063. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.152 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-8064. Instance Table

Instance Name	Physical Address
CBASS_IPCSS0	**45B0 1044h**

Figure 14-2681. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-8066. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.9 cbass_mcasp

cbass_mcasp

14.1.9.1 cbass_mcasp Summaries

cbass_mcasp Summaries

Table 14-8067. CBASS_ERR Registers, Base Address=0024 0000h, Length=1024

Offset	Length	Register Name	CBASS_MCASP0 Physical Address
0h	32	CBASS_ERR_PID	0024 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0024 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0024 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0024 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0024 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0024 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0024 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0024 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0024 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0024 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0024 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0024 005Ch
60h	32	CBASS_ERR_EOI	0024 0060h

14.1.9.2 cbass_mcasp Registers

cbass_mcasp Registers

14.1.9.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-8068. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0000h**

Figure 14-2682. CBASS_ERR_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">6h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-8070. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-8071. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0004h**

Figure 14-2683. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-8073. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-8074. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0024h**

Figure 14-2684. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-8076. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-8077. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0028h**

Figure 14-2685. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8079. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.9.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-8080. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 002Ch**

Figure 14-2686. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-8082. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-8083. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0030h**

Figure 14-2687. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-8085. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-8086. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0034h**

Figure 14-2688. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-8088. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

Table 14-8088. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-8089. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0038h**

Figure 14-2689. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8091. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-8092. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0050h**

Figure 14-2690. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-8094. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-8095. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0054h**

Figure 14-2691. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-8097. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-8098. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0058h**

Figure 14-2692. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-8100. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

Return to Summary Table

Table 14-8101. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 005Ch**

Figure 14-2693. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-8103. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.9.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

Return to Summary Table

Table 14-8104. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	**0024 0060h**

Figure 14-2694. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EOI_WR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOI_WR							
R/W							
0h							

Table 14-8106. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_clk2_32b_rst_mod_g_rst_n

14.1.10 cbass_misc_peri

cbass_misc_peri

14.1.10.1 cbass_misc_peri Summaries

cbass_misc_peri Summaries

Table 14-8107. CBASS_ERR Registers, Base Address=201F 0000h, Length=1024

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
0h	32	CBASS_ERR_PID	201F 0000h
4h	32	CBASS_ERR_DESTINATION_ID	201F 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	201F 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	201F 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	201F 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	201F 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	201F 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	201F 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	201F 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	201F 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	201F 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	201F 005Ch
60h	32	CBASS_ERR_EOI	201F 0060h

14.1.10.2 cbass_misc_peri Registers

cbass_misc_peri Registers

14.1.10.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-8108. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0000h**

Figure 14-2695. CBASS_ERR_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">6h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-8110. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-8111. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0004h

Figure 14-2696. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-8113. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-8114. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0024h**

Figure 14-2697. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-8116. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-8117. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0028h

Figure 14-2698. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8119. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.10.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-8120. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 002Ch**

Figure 14-2699. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-8122. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-8123. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0030h**

Figure 14-2700. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-8125. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-8126. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0034h

Figure 14-2701. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-8128. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

Table 14-8128. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-8129. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0038h**

Figure 14-2702. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8131. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-8132. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0050h**

Figure 14-2703. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-8134. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-8135. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0054h

Figure 14-2704. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-8137. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-8138. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0058h**

Figure 14-2705. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-8140. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-8141. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 005Ch**

Figure 14-2706. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-8143. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.10.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-8144. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	**201F 0060h**

Figure 14-2707. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8146. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_clk4_32b_rst_mod_g_rst_n

14.1.11 cbass_safe

cbass_safe

14.1.11.1 cbass_safe Summaries

cbass_safe Summaries

Table 14-8147. CBASS_ERR Registers, Base Address=0460 0000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS_SAFE1 Physical Address
0h	32	CBASS_ERR_PID	0460 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0460 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0460 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0460 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0460 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0460 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0460 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0460 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0460 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0460 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0460 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0460 005Ch
60h	32	CBASS_ERR_EOI	0460 0060h

14.1.11.2 cbass_safe Registers

cbass_safe Registers

14.1.11.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66003102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-8148. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0000h**

Figure 14-2708. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
6h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-8150. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-8151. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0004h**

Figure 14-2709. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-8153. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-8154. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0024h**

Figure 14-2710. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SRC_ID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SRC_ID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEST_ID							
R							
0h							

Table 14-8156. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-8157. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0028h**

Figure 14-2711. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8159. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.11.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-8160. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 002Ch**

Figure 14-2712. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-8162. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-8163. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0030h**

Figure 14-2713. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-8165. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-8166. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0034h**

Figure 14-2714. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-8168. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

Table 14-8168. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-8169. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0038h**

Figure 14-2715. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8171. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-8172. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0050h**

Figure 14-2716. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-8174. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-8175. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0054h**

Figure 14-2717. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ENABLED_INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8177. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-8178. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0058h

Figure 14-2718. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-8180. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-8181. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 005Ch**

Figure 14-2719. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-8183. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.1.11.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-8184. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	**0460 0060h**

Figure 14-2720. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-8186. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_safe_clk4_rst_mod_g_rst_n

14.2 Device Configuration Registers

14.2.1 CTRL_MMR Registers

14.2.1.1 General Purpose Control Registers

14.2.1.1.1 MAIN_CTRL_MMR

MAIN_CTRL_MMR

14.2.1.1.1.1 MAIN_CTRL_MMR Summaries

MAIN_CTRL_MMR Summaries

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072

Offset	Length	Register Name	CTRL_MMR0 Physical Address
0h	32	MAIN_CTRL_MMR_CFG0_PID	0010 0000h
8h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1	0010 0008h
100h	32	MAIN_CTRL_MMR_CFG0_IPC_SET0	0010 0100h
180h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR0	0010 0180h
1008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	0010 1008h
100Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	0010 100Ch
1010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS	0010 1010h
1014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0010 1014h
1018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE	0010 1018h
101Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0010 101Ch
1020h	32	MAIN_CTRL_MMR_CFG0_EOI	0010 1020h
1024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS	0010 1024h
1028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0010 1028h
102Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0010 102Ch
1030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR	0010 1030h
1100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0010 1100h
1104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY	0010 1104h
1108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY	0010 1108h
110Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY	0010 110Ch
1110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY	0010 1110h
1114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY	0010 1114h
1118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY	0010 1118h
2000h	32	MAIN_CTRL_MMR_CFG0_PID_PROXY	0010 2000h
2008h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0010 2008h
2100h	32	MAIN_CTRL_MMR_CFG0_IPC_SET0_PROXY	0010 2100h
2180h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR0_PROXY	0010 2180h
3008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0010 3008h
300Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0010 300Ch
3010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0010 3010h
3014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0010 3014h
3018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0010 3018h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
301Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0010 301Ch
3020h	32	MAIN_CTRL_MMR_CFG0_EOI_PROXY	0010 3020h
3024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0010 3024h
3028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0010 3028h
302Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0010 302Ch
3030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0010 3030h
3100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0010 3100h
3104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1	0010 3104h
3108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2	0010 3108h
310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3	0010 310Ch
3110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4	0010 3110h
3114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5	0010 3114h
3118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6	0010 3118h
4044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL	0010 4044h
4048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL	0010 4048h
4130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN	0010 4130h
4140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL	0010 4140h
4144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL	0010 4144h
4148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL	0010 4148h
4180h	32	MAIN_CTRL_MMR_CFG0_EQEP0_CTRL	0010 4180h
4184h	32	MAIN_CTRL_MMR_CFG0_EQEP1_CTRL	0010 4184h
4188h	32	MAIN_CTRL_MMR_CFG0_EQEP2_CTRL	0010 4188h
41A0h	32	MAIN_CTRL_MMR_CFG0_EQEP_STAT	0010 41A0h
4204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL	0010 4204h
420Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL	0010 420Ch
4214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL	0010 4214h
421Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL	0010 421Ch
4300h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL0	0010 4300h
44C0h	32	MAIN_CTRL_MMR_CFG0_EMMC0_STAT	0010 44C0h
44C4h	32	MAIN_CTRL_MMR_CFG0_EMMC1_STAT	0010 44C4h
44C8h	32	MAIN_CTRL_MMR_CFG0_EMMC2_STAT	0010 44C8h
4700h	32	MAIN_CTRL_MMR_CFG0_FSS_CTRL	0010 4700h
4750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT	0010 4750h
5008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	0010 5008h
500Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	0010 500Ch
5100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0010 5100h
5104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	0010 5104h
5108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	0010 5108h
510Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	0010 510Ch

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
5110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	0010 5110h
5114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	0010 5114h
5118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	0010 5118h
511Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY	0010 511Ch
5120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	0010 5120h
5124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	0010 5124h
5128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY	0010 5128h
512Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY	0010 512Ch
5130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	0010 5130h
5134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY	0010 5134h
5138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY	0010 5138h
6044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY	0010 6044h
6048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY	0010 6048h
6130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY	0010 6130h
6140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY	0010 6140h
6144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY	0010 6144h
6148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY	0010 6148h
6180h	32	MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY	0010 6180h
6184h	32	MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY	0010 6184h
6188h	32	MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY	0010 6188h
61A0h	32	MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY	0010 61A0h
6204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY	0010 6204h
620Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY	0010 620Ch
6214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY	0010 6214h
621Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY	0010 621Ch
6300h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY	0010 6300h
64C0h	32	MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY	0010 64C0h
64C4h	32	MAIN_CTRL_MMR_CFG0_EMMC1_STAT_PROXY	0010 64C4h
64C8h	32	MAIN_CTRL_MMR_CFG0_EMMC2_STAT_PROXY	0010 64C8h
6700h	32	MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY	0010 6700h
6750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY	0010 6750h
7008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0010 7008h
700Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0010 700Ch
7100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0010 7100h
7104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0010 7104h
7108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2	0010 7108h
710Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3	0010 710Ch

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
7110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4	0010 7110h
7114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5	0010 7114h
7118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6	0010 7118h
711Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7	0010 711Ch
7120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8	0010 7120h
7124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9	0010 7124h
7128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10	0010 7128h
712Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11	0010 712Ch
7130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12	0010 7130h
7134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13	0010 7134h
7138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14	0010 7138h
8000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL	0010 8000h
8010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL	0010 8010h
8060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL	0010 8060h
8064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL	0010 8064h
8068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL	0010 8068h
8074h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL	0010 8074h
807Ch	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL	0010 807Ch
8080h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL	0010 8080h
8090h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL	0010 8090h
80A4h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL	0010 80A4h
8140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL	0010 8140h
8160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL	0010 8160h
8168h	32	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL	0010 8168h
816Ch	32	MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL	0010 816Ch
8180h	32	MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL	0010 8180h
81B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL	0010 81B0h
81B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL	0010 81B4h
81B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL	0010 81B8h
81BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL	0010 81BCh
81C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL	0010 81C0h
81C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL	0010 81C4h
81C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL	0010 81C8h
81CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL	0010 81CCh
8200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL	0010 8200h
8204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL	0010 8204h
8208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL	0010 8208h
8240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL	0010 8240h
8244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL	0010 8244h
8248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL	0010 8248h
824Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL	0010 824Ch
8250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL	0010 8250h
8254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL	0010 8254h
8258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL	0010 8258h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
8280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL	0010 8280h
8284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL	0010 8284h
8288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL	0010 8288h
828Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL	0010 828Ch
8290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL	0010 8290h
8294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL	0010 8294h
8298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL	0010 8298h
82E0h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL	0010 82E0h
82E4h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL	0010 82E4h
8300h	32	MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL	0010 8300h
8320h	32	MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1	0010 8320h
8330h	32	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL	0010 8330h
8334h	32	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL	0010 8334h
8338h	32	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL	0010 8338h
8350h	32	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL	0010 8350h
8354h	32	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL	0010 8354h
8358h	32	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL	0010 8358h
8380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL	0010 8380h
8384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL	0010 8384h
8388h	32	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL	0010 8388h
838Ch	32	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL	0010 838Ch
8390h	32	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL	0010 8390h
8480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL	0010 8480h
8500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL	0010 8500h
9008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	0010 9008h
900Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	0010 900Ch
9100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	0010 9100h
9104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	0010 9104h
9108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY	0010 9108h
910Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY	0010 910Ch
9110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY	0010 9110h
9114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY	0010 9114h
9118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY	0010 9118h
911Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY	0010 911Ch
9120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY	0010 9120h
9124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY	0010 9124h
9128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY	0010 9128h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
A000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY	0010 A000h
A010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY	0010 A010h
A060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY	0010 A060h
A064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY	0010 A064h
A068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY	0010 A068h
A074h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL_PROXY	0010 A074h
A07Ch	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY	0010 A07Ch
A080h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY	0010 A080h
A090h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY	0010 A090h
A0A4h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL_PROXY	0010 A0A4h
A140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY	0010 A140h
A160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY	0010 A160h
A168h	32	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY	0010 A168h
A16Ch	32	MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL_PROXY	0010 A16Ch
A180h	32	MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY	0010 A180h
A1B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY	0010 A1B0h
A1B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY	0010 A1B4h
A1B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY	0010 A1B8h
A1BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY	0010 A1BCh
A1C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY	0010 A1C0h
A1C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY	0010 A1C4h
A1C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY	0010 A1C8h
A1CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY	0010 A1CCh
A200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY	0010 A200h
A204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY	0010 A204h
A208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY	0010 A208h
A240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY	0010 A240h
A244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY	0010 A244h
A248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY	0010 A248h
A24Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY	0010 A24Ch
A250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY	0010 A250h
A254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY	0010 A254h
A258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY	0010 A258h
A280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY	0010 A280h
A284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY	0010 A284h
A288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY	0010 A288h
A28Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY	0010 A28Ch
A290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY	0010 A290h
A294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY	0010 A294h
A298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY	0010 A298h
A2E0h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY	0010 A2E0h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
A2E4h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY	0010 A2E4h
A300h	32	MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL_PROXY	0010 A300h
A320h	32	MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1_PROXY	0010 A320h
A330h	32	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY	0010 A330h
A334h	32	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY	0010 A334h
A338h	32	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY	0010 A338h
A350h	32	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY	0010 A350h
A354h	32	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY	0010 A354h
A358h	32	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY	0010 A358h
A380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY	0010 A380h
A384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY	0010 A384h
A388h	32	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY	0010 A388h
A38Ch	32	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY	0010 A38Ch
A390h	32	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY	0010 A390h
A480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY	0010 A480h
A500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY	0010 A500h
B008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	0010 B008h
B00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	0010 B00Ch
B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0	0010 B100h
B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1	0010 B104h
B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2	0010 B108h
B10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3	0010 B10Ch
B110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4	0010 B110h
B114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5	0010 B114h
B118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6	0010 B118h
B11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7	0010 B11Ch
B120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8	0010 B120h
B124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9	0010 B124h
B128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10	0010 B128h
10500h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL	0011 0500h
11008h	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK0	0011 1008h
1100Ch	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK1	0011 100Ch
11100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	0011 1100h
11104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY	0011 1104h
11108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY	0011 1108h
1110Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY	0011 110Ch
11110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY	0011 1110h
11114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY	0011 1114h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
11118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY	0011 1118h
1111Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY	0011 111Ch
11120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	0011 1120h
11124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY	0011 1124h
11128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY	0011 1128h
12500h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY	0011 2500h
13008h	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY	0011 3008h
1300Ch	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY	0011 300Ch
13100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0	0011 3100h
13104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1	0011 3104h
13108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2	0011 3108h
1310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3	0011 310Ch
13110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4	0011 3110h
13114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5	0011 3114h
13118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6	0011 3118h
1311Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7	0011 311Ch
13120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8	0011 3120h
13124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9	0011 3124h
13128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10	0011 3128h
19008h	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK0	0011 9008h
1900Ch	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK1	0011 900Ch
19100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	0011 9100h
19104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	0011 9104h
19108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	0011 9108h
1910Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY	0011 910Ch
19110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY	0011 9110h
19114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY	0011 9114h
19118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY	0011 9118h
1911Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY	0011 911Ch
19120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY	0011 9120h
1B008h	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	0011 B008h
1B00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	0011 B00Ch
1B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0	0011 B100h
1B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1	0011 B104h

Table 14-8187. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
1B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2	0011 B108h
1B10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3	0011 B10Ch
1B110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4	0011 B110h
1B114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5	0011 B114h
1B118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6	0011 B118h
1B11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7	0011 B11Ch
1B120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8	0011 B120h

14.2.1.1.1.2 MAIN_CTRL_MMR Registers

MAIN_CTRL_MMR Registers

14.2.1.1.1.2.1 MAIN_CTRL_MMR_CFG0_PID Register

1 MAIN_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-8188. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 0000h**

Figure 14-2721. MAIN_CTRL_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-8190. MAIN_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.2 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-8191. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 0008h**

Figure 14-2722. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-8193. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.3 MAIN_CTRL_MMR_CFG0_IPC_SET0 Register

1 MAIN_CTRL_MMR_CFG0_IPC_SET0 Register (Offset = 100h) [reset = 0h]

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Table 14-8194. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 0100h**

Figure 14-2723. MAIN_CTRL_MMR_CFG0_IPC_SET0 Name Register

31	30	29	28	27	26	25	24
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET0_IPC_SRC_SET				RESERVED			IPC_SET0_IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-8196. MAIN_CTRL_MMR_CFG0_IPC_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.4 MAIN_CTRL_MMR_CFG0_IPC_CLR0 Register

1 MAIN_CTRL_MMR_CFG0_IPC_CLR0 Register (Offset = 180h) [reset = 0h]

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Table 14-8197. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 0180h**

Figure 14-2724. MAIN_CTRL_MMR_CFG0_IPC_CLR0 Name Register

31	30	29	28	27	26	25	24
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR0_IPC_SRC_CLR				RESERVED			IPC_CLR0_IPC_CLR
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-8199. MAIN_CTRL_MMR_CFG0_IPC_CLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.5 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-8200. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1008h**

Figure 14-2725. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-8202. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.6 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-8203. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 100Ch**

Figure 14-2726. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-8205. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.7 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-8206. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1010h**

Figure 14-2727. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-8208. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.8 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-8209. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1014h**

Figure 14-2728. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-8211. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.9 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-8212. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1018h**

Figure 14-2729. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-8214. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.10 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-8215. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 101Ch**

Figure 14-2730. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-8217. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.11 MAIN_CTRL_MMR_CFG0_EOI Register

1 MAIN_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-8218. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1020h**

Figure 14-2731. MAIN_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-8220. MAIN_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.12 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-8221. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1024h**

Figure 14-2732. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-8223. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.13 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-8224. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 1028h

Figure 14-2733. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-8226. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.14 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-8227. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 102Ch**

Figure 14-2734. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8229. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.15 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-8230. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1030h**

Figure 14-2735. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-8232. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.16 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8233. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1100h**

Figure 14-2736. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-8235. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.17 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register (Offset = 1104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8236. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1104h**

Figure 14-2737. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1_READONLY							
R							
0h							

Table 14-8238. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.18 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8239. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1108h**

Figure 14-2738. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2_READONLY							
R							
0h							

Table 14-8241. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.19 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-8242. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 110Ch**

Figure 14-2739. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3_READONLY							
R							
0h							

Table 14-8244. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.20 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8245. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1110h**

Figure 14-2740. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4_READONLY							
R							
0h							

Table 14-8247. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.21 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8248. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1114h**

Figure 14-2741. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-8250. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.22 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register (Offset = 1118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8251. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 1118h**

Figure 14-2742. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6_READONLY							
R							
0h							

Table 14-8253. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.23 MAIN_CTRL_MMR_CFG0_PID_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-8254. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0010 2000h**

Figure 14-2743. MAIN_CTRL_MMR_CFG0_PID_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC_PROXY</td><td colspan="3">PID_MAJOR_PROXY</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM_PROXY</td><td colspan="6">PID_MINOR_PROXY</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-8256. MAIN_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.24 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-8257. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0010 2008h**

Figure 14-2744. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-8259. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.25 MAIN_CTRL_MMR_CFG0_IPC_SET0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_IPC_SET0_PROXY Register (Offset = 2100h) [reset = 0h]

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Table 14-8260. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 2100h**

Figure 14-2745. MAIN_CTRL_MMR_CFG0_IPC_SET0_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SET0_IPC_SRC_SET_PROXY				RESERVED			IPC_SET0_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-8262. MAIN_CTRL_MMR_CFG0_IPC_SET0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.26 MAIN_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register (Offset = 2180h) [reset = 0h]

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Table 14-8263. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 2180h**

Figure 14-2746. MAIN_CTRL_MMR_CFG0_IPC_CLR0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR0_IPC_SRC_CLR_PROXY</td><td colspan="3">RESERVED</td><td>IPC_CLR0_IPC_CLR_PROXY</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-8265. MAIN_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.27 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-8266. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3008h**

Figure 14-2747. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-8268. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.28 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-8269. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 300Ch

Figure 14-2748. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-8271. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.29 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-8272. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3010h**

Figure 14-2749. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-8274. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.30 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-8275. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3014h**

Figure 14-2750. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-8277. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.31 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-8278. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3018h**

Figure 14-2751. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-8280. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.32 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-8281. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 301Ch**

Figure 14-2752. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-8283. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.33 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-8284. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3020h**

Figure 14-2753. MAIN_CTRL_MMR_CFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-8286. MAIN_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.34 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-8287. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3024h**

Figure 14-2754. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-8289. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.35 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-8290. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3028h**

Figure 14-2755. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-8292. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.36 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-8293. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 302Ch**

Figure 14-2756. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ROUTEID_PROXY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-8295. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.37 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-8296. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3030h**

Figure 14-2757. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-8298. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.38 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8299. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3100h**

Figure 14-2758. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-8301. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.39 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8302. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3104h**

Figure 14-2759. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-8304. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.40 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8305. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 3108h

Figure 14-2760. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-8307. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.41 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-8308. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 310Ch**

Figure 14-2761. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-8310. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.42 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8311. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3110h**

Figure 14-2762. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4							
R/W							
0h							

Table 14-8313. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.43 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8314. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3114h**

Figure 14-2763. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-8316. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.44 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register (Offset = 3118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-8317. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 3118h**

Figure 14-2764. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6							
R/W							
0h							

Table 14-8319. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.45 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register (Offset = 4044h) [reset = 2h]

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Table 14-8320. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4044h**

Figure 14-2765. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET1_CTRL_PORT_MODE_SEL		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-8322. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port1 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII (not supported) 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.46 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register (Offset = 4048h) [reset = 2h]

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Table 14-8323. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4048h**

Figure 14-2766. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET2_CTRL_PORT_MODE_SEL		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-8325. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port2 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII (not supported) 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.47 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register (Offset = 4130h) [reset = 0h]

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Table 14-8326. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4130h**

Figure 14-2767. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM_TB_CLKEN_EPWM2_TB_CLKEN	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	EPWM_TB_CLKEN_EPWM0_TB_CLKEN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8328. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM2 When Set Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM1 When Set Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM0 When Set Reset Source: mod_g_rst_n

14.2.1.1.1.2.48 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register (Offset = 4140h) [reset = 0h]

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Table 14-8329. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4140h**

Figure 14-2768. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM0_CTRL_SYNCIN_SEL		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM0_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8331. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL	R/W	0h	Selects the source of the EPWM0 synchronization input Field values (others are reserved): 3'b000 - EPWM0_SYNCIN Pin 3'b001 - None 3'b010 - Time Sync Router 19 3'b011 - Compare Event Router 32 undefined - undefined 3'b100 - None 3'b101 - None 3'b110 - None 3'b111 - None Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.49 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register (Offset = 4144h) [reset = 0h]

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Table 14-8332. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4144h**

Figure 14-2769. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM1_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8334. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.50 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register (Offset = 4148h) [reset = 0h]

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Table 14-8335. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4148h**

Figure 14-2770. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8337. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.51 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register (Offset = 4180h) [reset = 0h]

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Table 14-8338. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4180h**

Figure 14-2771. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP0_CTRL_SOCA_SEL				
NONE			R/W				
0h			0h				

Table 14-8340. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP0_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP0 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.52 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register (Offset = 4184h) [reset = 0h]

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Table 14-8341. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4184h**

Figure 14-2772. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EQEP1_CTRL_SOCA_SEL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-8343. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP1_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP1 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.53 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register (Offset = 4188h) [reset = 0h]

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Table 14-8344. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4188h**

Figure 14-2773. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EQEP2_CTRL_SOCA_SEL				
NONE			R/W				
0h			0h				

Table 14-8346. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP2_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP2 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.54 MAIN_CTRL_MMR_CFG0_EQEP_STAT Register

1 MAIN_CTRL_MMR_CFG0_EQEP_STAT Register (Offset = 41A0h) [reset = 0h]

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Table 14-8347. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 41A0h**

Figure 14-2774. MAIN_CTRL_MMR_CFG0_EQEP_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EQEP_STAT_PHASE_ERR2	EQEP_STAT_PHASE_ERR1	EQEP_STAT_PHASE_ERR0
NONE					R	R	R
0h					X	X	X

Table 14-8349. MAIN_CTRL_MMR_CFG0_EQEP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EQEP_STAT_PHASE_ERR2	R	X	EQEP2 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n
1	EQEP_STAT_PHASE_ERR1	R	X	EQEP1 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n
0	EQEP_STAT_PHASE_ERR0	R	X	EQEP0 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n

14.2.1.1.1.2.55 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

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Table 14-8350. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4204h**

Figure 14-2775. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8352. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.56 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

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Table 14-8353. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 420Ch**

Figure 14-2776. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TIMER3_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-8355. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.57 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register (Offset = 4214h) [reset = 0h]

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Table 14-8356. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4214h**

Figure 14-2777. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER5_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8358. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER5 to TIMER4 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.58 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register (Offset = 421Ch) [reset = 0h]

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Table 14-8359. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 421Ch

Figure 14-2778. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER7_CTRL_CASCADE_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8361. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER7 to TIMER6 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.59 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register

1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register (Offset = 4300h) [reset = 3F3Fh]

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Table 14-8362. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 4300h**

Figure 14-2779. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL0_ORD15	C7XV_CTRL0_ORD14	C7XV_CTRL0_ORD13	C7XV_CTRL0_ORD12	C7XV_CTRL0_ORD11	C7XV_CTRL0_ORD10	C7XV_CTRL0_ORD9	C7XV_CTRL0_ORD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL0_ORD7	C7XV_CTRL0_ORD6	C7XV_CTRL0_ORD5	C7XV_CTRL0_ORD4	C7XV_CTRL0_ORD3	C7XV_CTRL0_ORD2	C7XV_CTRL0_ORD1	C7XV_CTRL0_ORD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-8364. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL0_ORD15	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
14	C7XV_CTRL0_ORD14	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
13	C7XV_CTRL0_ORD13	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
12	C7XV_CTRL0_ORD12	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

Table 14-8364. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	C7XV_CTRL0_ORD11	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
10	C7XV_CTRL0_ORD10	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
9	C7XV_CTRL0_ORD9	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
8	C7XV_CTRL0_ORD8	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
7	C7XV_CTRL0_ORD7	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
6	C7XV_CTRL0_ORD6	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
5	C7XV_CTRL0_ORD5	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
4	C7XV_CTRL0_ORD4	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
3	C7XV_CTRL0_ORD3	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
2	C7XV_CTRL0_ORD2	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
1	C7XV_CTRL0_ORD1	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

Table 14-8364. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	C7XV_CTRL0_ORD0	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

14.2.1.1.1.2.60 MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register (Offset = 44C0h) [reset = 0h]

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Table 14-8365. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 44C0h**

Figure 14-2780. MAIN_CTRL_MMR_CFG0_EMMC0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_STAT_SIG1P8_EN
NONE							R
0h							X

Table 14-8367. MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_STAT_SIG1P8_EN	R	X	Status of 1.8V Signal Activate from EMMC0 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.61 MAIN_CTRL_MMR_CFG0_EMMC1_STAT Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_STAT Register (Offset = 44C4h) [reset = 0h]

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Table 14-8368. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 44C4h**

Figure 14-2781. MAIN_CTRL_MMR_CFG0_EMMC1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC1_STAT_SIG1P8_EN
NONE							R
0h							X

Table 14-8370. MAIN_CTRL_MMR_CFG0_EMMC1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC1_STAT_SIG1P8_EN	R	X	Status of 1.8V Signal Activate from EMMC1 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.62 MAIN_CTRL_MMR_CFG0_EMMC2_STAT Register

1 MAIN_CTRL_MMR_CFG0_EMMC2_STAT Register (Offset = 44C8h) [reset = 0h]

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Table 14-8371. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 44C8h**

Figure 14-2782. MAIN_CTRL_MMR_CFG0_EMMC2_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC2_STAT_SIG1P8_EN
NONE							R
0h							X

Table 14-8373. MAIN_CTRL_MMR_CFG0_EMMC2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC2_STAT_SIG1P8_EN	R	X	Status of 1.8V Signal Activate from EMMC2 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.63 MAIN_CTRL_MMR_CFG0_FSS_CTRL Register

1 MAIN_CTRL_MMR_CFG0_FSS_CTRL Register (Offset = 4700h) [reset = 0h]

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Table 14-8374. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 4700h

Figure 14-2783. MAIN_CTRL_MMR_CFG0_FSS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSS_CTRL_S0_BOOT_SIZE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">FSS_CTRL_S0_BOOT_SEG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-8376. MAIN_CTRL_MMR_CFG0_FSS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	FSS_CTRL_S0_BOOT_SIZE	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI0) flash interface 0 - S0 boot size is 64 MB 1 - S0 boot size is 128 MB Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS_CTRL_S0_BOOT_SEG	R/W	0h	Selects the boot block to be used for the S0 (OSPI0) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are activated for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) 6'h00 - Use block 0 6'h01 - Use block 1 : 6'h3F - Use block 63 Reset Source: mod_g_rst_n

14.2.1.1.1.2.64 MAIN_CTRL_MMR_CFG0_DCC_STAT Register

1 MAIN_CTRL_MMR_CFG0_DCC_STAT Register (Offset = 4750h) [reset = 0h]

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Table 14-8377. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 4750h

Figure 14-2784. MAIN_CTRL_MMR_CFG0_DCC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						DCC_STAT_MCU_DCC1_INTR_DONE	DCC_STAT_MCU_DCC0_INTR_DONE
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DCC_STAT_DCC6_INTR_DONE	DCC_STAT_DCC5_INTR_DONE	DCC_STAT_DCC4_INTR_DONE	DCC_STAT_DCC3_INTR_DONE	DCC_STAT_DCC2_INTR_DONE	DCC_STAT_DCC1_INTR_DONE	DCC_STAT_DCC0_INTR_DONE
NONE	R	R	R	R	R	R	R
0h	X	X	X	X	X	X	X

Table 14-8379. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DCC_STAT_MCU_DCC1_INTR_DONE	R	X	MCU_DCC1 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
16	DCC_STAT_MCU_DCC0_INTR_DONE	R	X	MCU_DCC0 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
15:7	RESERVED	NONE	0h	Reserved
6	DCC_STAT_DCC6_INTR_DONE	R	X	DCC6 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
5	DCC_STAT_DCC5_INTR_DONE	R	X	DCC5 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n

Table 14-8379. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DCC_STAT_DCC4_INTR_DONE	R	X	DCC4 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE	R	X	DCC3 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE	R	X	DCC2 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE	R	X	DCC1 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
0	DCC_STAT_DCC0_INTR_DONE	R	X	DCC0 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n

14.2.1.1.1.2.65 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-8380. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5008h**

Figure 14-2785. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-8382. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.66 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-8383. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 500Ch**

Figure 14-2786. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8385. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.67 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8386. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5100h**

Figure 14-2787. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-8388. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.68 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8389. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5104h**

Figure 14-2788. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-8391. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.69 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8392. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5108h**

Figure 14-2789. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-8394. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.70 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8395. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 510Ch**

Figure 14-2790. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-8397. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.71 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8398. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5110h**

Figure 14-2791. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-8400. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.72 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8401. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5114h**

Figure 14-2792. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-8403. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.73 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8404. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5118h**

Figure 14-2793. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-8406. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.74 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register (Offset = 511Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8407. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 511Ch**

Figure 14-2794. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7_READONLY							
R							
0h							

Table 14-8409. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.75 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8410. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5120h**

Figure 14-2795. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-8412. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.76 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8413. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5124h**

Figure 14-2796. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-8415. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.77 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register (Offset = 5128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8416. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5128h**

Figure 14-2797. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10_READONLY							
R							
0h							

Table 14-8418. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.78 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register (Offset = 512Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8419. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 512Ch**

Figure 14-2798. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11_READONLY							
R							
0h							

Table 14-8421. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.79 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8422. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5130h**

Figure 14-2799. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12_READONLY							
R							
0h							

Table 14-8424. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.80 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register (Offset = 5134h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8425. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5134h**

Figure 14-2800. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R13_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R13_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R13_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R13_READONLY							
R							
0h							

Table 14-8427. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R13_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.81 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register (Offset = 5138h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8428. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 5138h**

Figure 14-2801. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R14_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R14_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R14_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R14_READONLY							
R							
0h							

Table 14-8430. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R14_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.82 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register (Offset = 6044h) [reset = 2h]

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Table 14-8431. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6044h**

Figure 14-2802. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET1_CTRL_PORT_MODE_SEL_PROXY		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-8433. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port1 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII (not supported) 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.83 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register (Offset = 6048h) [reset = 2h]

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Table 14-8434. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 6048h

Figure 14-2803. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET2_CTRL_PORT_MODE_SEL_PROXY		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-8436. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port2 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII (not supported) 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.84 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register (Offset = 6130h) [reset = 0h]

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Table 14-8437. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6130h**

Figure 14-2804. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8439. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM2 When Set Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM1 When Set Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM0 When Set Reset Source: mod_g_rst_n

14.2.1.1.1.2.85 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register (Offset = 6140h) [reset = 0h]

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Table 14-8440. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 6140h

Figure 14-2805. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM0_CTRL_SYNCIN_SEL_PROXY		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM0_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8442. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL_PROXY	R/W	0h	Selects the source of the EPWM0 synchronization input Field values (others are reserved): 3'b000 - EPWM0_SYNCIN Pin 3'b001 - None 3'b010 - Time Sync Router 19 3'b011 - Compare Event Router 32 undefined - undefined 3'b100 - None 3'b101 - None 3'b110 - None 3'b111 - None Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.86 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register (Offset = 6144h) [reset = 0h]

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Table 14-8443. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6144h**

Figure 14-2806. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM1_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8445. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.87 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register (Offset = 6148h) [reset = 0h]

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Table 14-8446. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6148h**

Figure 14-2807. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-8448. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers 0 - Deactivated 1 - Activated Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.88 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register (Offset = 6180h) [reset = 0h]

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Table 14-8449. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6180h**

Figure 14-2808. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP0_CTRL_SOCA_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-8451. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP0_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP0 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.89 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register (Offset = 6184h) [reset = 0h]

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Table 14-8452. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6184h**

Figure 14-2809. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EQEP1_CTRL_SOCA_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-8454. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP1_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP1 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.90 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register (Offset = 6188h) [reset = 0h]

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Table 14-8455. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6188h**

Figure 14-2810. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP2_CTRL_SOCA_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-8457. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP2_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP2 Field values (others are reserved): undefined - undefined undefined - undefined 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - MCU_TIMER0 PWM 5'b00101 - MCU_TIMER1 PWM 5'b00110 - MCU_TIMER2 PWM 5'b00111 - MCU_TIMER3 PWM 5'b01000 - TIMER0 PWM 5'b01001 - TIMER1 PWM 5'b01010 - TIMER2 PWM 5'b01011 - TIMER3 PWM 5'b01100 - TIMER4 PWM 5'b01101 - TIMER5 PWM 5'b01110 - TIMER6 PWM 5'b01111 - TIMER7 PWM 5'b10000 - WKUP TIMER0 PWM 5'b10001 - WKUP TIMER1 PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.91 MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register (Offset = 61A0h) [reset = 0h]

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Table 14-8458. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 61A0h

Figure 14-2811. MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EQEP_STAT_PHASE_ERR2_PROXY	EQEP_STAT_PHASE_ERR1_PROXY	EQEP_STAT_PHASE_ERR0_PROXY
NONE					R	R	R
0h					X	X	X

Table 14-8460. MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EQEP_STAT_PHASE_ERR2_PROXY	R	X	EQEP2 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n
1	EQEP_STAT_PHASE_ERR1_PROXY	R	X	EQEP1 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n
0	EQEP_STAT_PHASE_ERR0_PROXY	R	X	EQEP0 Phase error status 0 - No error 1 - Phase error occurred Reset Source: mod_g_rst_n

14.2.1.1.1.2.92 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

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Table 14-8461. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 6204h

Figure 14-2812. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8463. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.93 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register (Offset = 620Ch) [reset = 0h]

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Table 14-8464. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 620Ch

Figure 14-2813. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER3_CTRL_CASCADE_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8466. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.94 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register (Offset = 6214h) [reset = 0h]

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Table 14-8467. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6214h**

Figure 14-2814. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER5_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8469. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER5 to TIMER4 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.95 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register (Offset = 621Ch) [reset = 0h]

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Table 14-8470. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 621Ch

Figure 14-2815. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER7_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8472. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER7 to TIMER6 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.96 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register (Offset = 6300h) [reset = 3F3Fh]

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Table 14-8473. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6300h**

Figure 14-2816. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL0_ORD15_PROXY	C7XV_CTRL0_ORD14_PROXY	C7XV_CTRL0_ORD13_PROXY	C7XV_CTRL0_ORD12_PROXY	C7XV_CTRL0_ORD11_PROXY	C7XV_CTRL0_ORD10_PROXY	C7XV_CTRL0_ORD9_PROXY	C7XV_CTRL0_ORD8_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL0_ORD7_PROXY	C7XV_CTRL0_ORD6_PROXY	C7XV_CTRL0_ORD5_PROXY	C7XV_CTRL0_ORD4_PROXY	C7XV_CTRL0_ORD3_PROXY	C7XV_CTRL0_ORD2_PROXY	C7XV_CTRL0_ORD1_PROXY	C7XV_CTRL0_ORD0_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-8475. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL0_ORD15_PROXY	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
14	C7XV_CTRL0_ORD14_PROXY	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
13	C7XV_CTRL0_ORD13_PROXY	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

Table 14-8475. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	C7XV_CTRL0_ORD12_PROXY	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
11	C7XV_CTRL0_ORD11_PROXY	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
10	C7XV_CTRL0_ORD10_PROXY	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
9	C7XV_CTRL0_ORD9_PROXY	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
8	C7XV_CTRL0_ORD8_PROXY	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
7	C7XV_CTRL0_ORD7_PROXY	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
6	C7XV_CTRL0_ORD6_PROXY	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
5	C7XV_CTRL0_ORD5_PROXY	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
4	C7XV_CTRL0_ORD4_PROXY	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
3	C7XV_CTRL0_ORD3_PROXY	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
2	C7XV_CTRL0_ORD2_PROXY	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

Table 14-8475. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	C7XV_CTRL0_ORD1_PROXY	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n
0	C7XV_CTRL0_ORD0_PROXY	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b1 - RELAXED_R_TO_W 1'b0 - RELAXED_READ Reset Source: mod_por_rst_n

14.2.1.1.1.2.97 MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register (Offset = 64C0h) [reset = 0h]

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Table 14-8476. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 64C0h**

Figure 14-2817. MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_STAT_SIG1P8_EN_PROXY
NONE							R
0h							X

Table 14-8478. MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_STAT_SIG1P8_EN_PROXY	R	X	Status of 1.8V Signal Activate from EMMC0 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.98 MAIN_CTRL_MMR_CFG0_EMMC1_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_STAT_PROXY Register (Offset = 64C4h) [reset = 0h]

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Table 14-8479. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 64C4h**

Figure 14-2818. MAIN_CTRL_MMR_CFG0_EMMC1_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC1_STAT_SIG1P8_EN_PROXY
NONE							R
0h							X

Table 14-8481. MAIN_CTRL_MMR_CFG0_EMMC1_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC1_STAT_SIG1P8_EN_PROXY	R	X	Status of 1.8V Signal Activate from EMMC1 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.99 MAIN_CTRL_MMR_CFG0_EMMC2_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC2_STAT_PROXY Register (Offset = 64C8h) [reset = 0h]

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Table 14-8482. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 64C8h**

Figure 14-2819. MAIN_CTRL_MMR_CFG0_EMMC2_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC2_STAT_SIG1P8_EN_PROXY
NONE							R
0h							X

Table 14-8484. MAIN_CTRL_MMR_CFG0_EMMC2_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC2_STAT_SIG1P8_EN_PROXY	R	X	Status of 1.8V Signal Activate from EMMC2 Module Reset Source: mod_g_rst_n

14.2.1.1.1.2.100 MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register (Offset = 6700h) [reset = 0h]

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Table 14-8485. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 6700h**

Figure 14-2820. MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSS_CTRL_S0_BOOT_SIZE_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">FSS_CTRL_S0_BOOT_SEG_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-8487. MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	FSS_CTRL_S0_BOOT_SIZE_PROXY	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI0) flash interface 0 - S0 boot size is 64 MB 1 - S0 boot size is 128 MB Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS_CTRL_S0_BOOT_SEG_PROXY	R/W	0h	Selects the boot block to be used for the S0 (OSPI0) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are activated for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) 6'h00 - Use block 0 6'h01 - Use block 1 : 6'h3F - Use block 63 Reset Source: mod_g_rst_n

14.2.1.1.1.2.101 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register (Offset = 6750h) [reset = 0h]

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Table 14-8488. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 6750h

Figure 14-2821. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						DCC_STAT_MCU_DCC1_INTR_DONE_PROXY	DCC_STAT_MCU_DCC0_INTR_DONE_PROXY
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DCC_STAT_DCC6_INTR_DONE_PROXY	DCC_STAT_DCC5_INTR_DONE_PROXY	DCC_STAT_DCC4_INTR_DONE_PROXY	DCC_STAT_DCC3_INTR_DONE_PROXY	DCC_STAT_DCC2_INTR_DONE_PROXY	DCC_STAT_DCC1_INTR_DONE_PROXY	DCC_STAT_DCC0_INTR_DONE_PROXY
NONE	R	R	R	R	R	R	R
0h	X	X	X	X	X	X	X

Table 14-8490. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DCC_STAT_MCU_DCC1_INTR_DONE_PROXY	R	X	MCU_DCC1 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
16	DCC_STAT_MCU_DCC0_INTR_DONE_PROXY	R	X	MCU_DCC0 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
15:7	RESERVED	NONE	0h	Reserved
6	DCC_STAT_DCC6_INTR_DONE_PROXY	R	X	DCC6 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
5	DCC_STAT_DCC5_INTR_DONE_PROXY	R	X	DCC5 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n

Table 14-8490. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DCC_STAT_DCC4_INTR_DONE_PROXY	R	X	DCC4 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE_PROXY	R	X	DCC3 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE_PROXY	R	X	DCC2 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE_PROXY	R	X	DCC1 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n
0	DCC_STAT_DCC0_INTR_DONE_PROXY	R	X	DCC0 Done Interrupt Status 0 = No Interrupt Pending 1 = Interrupt Pending Reset Source: mod_g_rst_n

14.2.1.1.1.2.102 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-8491. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7008h**

Figure 14-2822. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-8493. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.103 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-8494. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 700Ch**

Figure 14-2823. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-8496. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.104 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8497. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7100h**

Figure 14-2824. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-8499. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.105 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8500. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7104h**

Figure 14-2825. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-8502. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.106 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8503. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7108h**

Figure 14-2826. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-8505. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.107 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8506. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 710Ch**

Figure 14-2827. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-8508. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.108 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8509. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7110h**

Figure 14-2828. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-8511. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.109 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8512. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7114h**

Figure 14-2829. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-8514. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.110 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8515. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7118h**

Figure 14-2830. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-8517. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.111 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8518. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 711Ch**

Figure 14-2831. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-8520. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.112 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8521. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7120h**

Figure 14-2832. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-8523. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.113 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8524. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7124h**

Figure 14-2833. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-8526. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.114 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8527. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7128h**

Figure 14-2834. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-8529. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.115 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-8530. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 712Ch**

Figure 14-2835. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-8532. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.116 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8533. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 7130h

Figure 14-2836. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R12							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-8535. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.117 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register (Offset = 7134h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8536. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 7134h

Figure 14-2837. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R13							
R/W							
0h							

Table 14-8538. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R13	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.118 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register (Offset = 7138h) [reset = 0h]

Claim bits for Partition 1

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Table 14-8539. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 7138h**

Figure 14-2838. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R14							
R/W							
0h							

Table 14-8541. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R14	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.119 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register (Offset = 8000h) [reset = 7h]

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Table 14-8542. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8000h**

Figure 14-2839. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							OBSCLK0_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OBSCLK0_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OBSCLK0_CTRL_CLK_DIV							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			OBSCLK0_CTRL_CLK_SEL				
NONE			R/W				
0h			7h				

Table 14-8544. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	OBSCLK0_CTRL_OUT_MUX_SEL	R/W	0h	OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 5'b11111. 1'b0 - The output of the MCU_OBSCLK output divider is output on the pin 1'b1 - HFOSC0_CLK is output on the pin Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK0 divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_por_rst_n

Table 14-8544. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	OBSCLK0_CTRL_CLK_DIV	R/W	0h	OBSCLK0 output divider Divides the selected clock by clkdiv+1 for output to the OBSCLK0 pins. Supports divide by 1 to 256 (default to 1). To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	OBSCLK0_CTRL_CLK_SEL	R/W	7h	OBSCLK0 clock source selection. Selects the source of the clock to be divided by the OBSCLK0 divider and output on the OBSCLK0 pin. Field values (others are reserved): 5'b00000 - MAIN_PLL0_HSDIV0_CLKOUT 5'b00001 - MAIN_PLL1_HSDIV0_CLKOUT 5'b00010 - MAIN_PLL2_HSDIV0_CLKOUT 5'b00011 - MAIN_PLL8_HSDIV0_CLKOUT_DIV4 5'b00100 - MAIN_PLL12_HSDIV0_CLKOUT_DIV4 5'b00101 - CLK_12M_RC 5'b00110 - HFOSC0_CLKOUT_32K 5'b00111 - PLLCTRL_OBSCLK 5'b01000 - HFOSC0_CLKOUT 5'b01001 - CLK_32K 5'b01010 - cpsw2g_cpts_genf0 5'b01011 - cpsw2g_cpts_genf1 5'b01100 - MCU_PLL0_HSDIV0_CLKOUT 5'b01101 - MAIN_PLL15_HSDIV0_CLKOUT undefined - undefined 5'b01110 - reserved 5'b01111 - MAIN_PLL17_HSDIV0_CLKOUT 5'b10000 - MAIN_SYSCLK0 5'b10001 - DEVICE_CLKOUT_32K 5'b10010 - MAIN_PLL5_HSDIV0_CLKOUT 5'b10011 - MAIN_PLL7_HSDIV0_CLKOUT_DIV4 Reset Source: mod_por_rst_n

14.2.1.1.1.2.120 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register

1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register (Offset = 8010h) [reset = 0h]

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Table 14-8545. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8010h**

Figure 14-2840. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RSVD	RESERVED			CLKOUT_CTRL_CLK_SEL
NONE				NONE			R/W
0h			0h	0h			0h

Table 14-8547. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL	R/W	0h	Selects CLKOUT clock source Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV1_CLKOUT / 5 1'b1 - MAIN_PLL2_HSDIV1_CLKOUT / 10 Reset Source: mod_g_rst_n

14.2.1.1.1.2.121 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register (Offset = 8060h) [reset = 800000h]

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Table 14-8548. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8060h**

Figure 14-2841. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL0_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-8550. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b0) when a MAIN warm reset occurs to keep MAIN PLL0 from being bypassed, supporting reset isolation of the CPSW. 1'b0 = Exit bypass mode (based on MAIN PLL0_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.122 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register (Offset = 8064h) [reset = 800000h]

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Table 14-8551. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0010 8064h**

Figure 14-2842. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL1_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8553. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL1 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL1 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL1 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.123 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register (Offset = 8068h) [reset = 800000h]

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Table 14-8554. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8068h**

Figure 14-2843. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL2_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8556. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL2 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL2 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL2 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.124 MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL Register (Offset = 8074h) [reset = 800000h]

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Table 14-8557. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8074h**

Figure 14-2844. MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL5_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL5_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8559. MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL5_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL5. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL5_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL5 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL5_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.125 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register (Offset = 807Ch) [reset = 800000h]

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Table 14-8560. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 807Ch**

Figure 14-2845. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL7_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8562. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL7. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL7_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL7 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL7_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.126 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register (Offset = 8080h) [reset = 800000h]

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Table 14-8563. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8080h

Figure 14-2846. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL8_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8565. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL8. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL8_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL8 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL8_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.127 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register (Offset = 8090h) [reset = 800000h]

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Table 14-8566. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8090h**

Figure 14-2847. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
MAIN_PLL12_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8568. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL12. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL12_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL12 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL12_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.128 MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL Register (Offset = 80A4h) [reset = 800000h]

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Table 14-8569. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 80A4h

Figure 14-2848. MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL17_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL17_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-8571. MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL17_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL17 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL17_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL17 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL17 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.129 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register (Offset = 8140h) [reset = 7h]

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Table 14-8572. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8140h**

Figure 14-2849. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_CLKSEL_CPTS_CLKSEL		
NONE					R/W		
0h					7h		

Table 14-8574. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CLKSEL_CPTS_CLKSEL	R/W	7h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - MCU_SYSCLK0 undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_por_rst_n

14.2.1.1.1.2.130 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register (Offset = 8160h) [reset = 0h]

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Table 14-8575. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8160h**

Figure 14-2850. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-8577. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD0_CLKLB 1'b1 - Loopback from IO Pin MMCSD0_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD_REFCLK_SEL	R/W	0h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.131 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register (Offset = 8168h) [reset = 1h]

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Table 14-8578. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8168h**

Figure 14-2851. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC1_CLKSEL_EMMCSD_IO_CLKLB_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC1_CLKSEL_EMMCSD_REFCLK_SEL
NONE							R/W
0h							1h

Table 14-8580. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC1_CLKSEL_EMMCSD_IO_CLKLB_SEL	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD1_CLKLB 1'b1 - Loopback from IO Pin MMCSD1_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC1_CLKSEL_EMMCSD_REFCLK_SEL	R/W	1h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.132 MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL Register (Offset = 816Ch) [reset = 1h]

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Table 14-8581. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 816Ch**

Figure 14-2852. MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC2_CLKSEL_EMMCSD_IO_CLKLB_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC2_CLKSEL_EMMCSD_REFCLK_SEL
NONE							R/W
0h							1h

Table 14-8583. MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC2_CLKSEL_EMMCSD_IO_CLKLB_SEL	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD2_CLKLB 1'b1 - Loopback from IO Pin MMCSD2_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC2_CLKSEL_EMMCSD_REFCLK_SEL	R/W	1h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.133 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register (Offset = 8180h) [reset = 0h]

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Table 14-8584. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8180h**

Figure 14-2853. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GPMC_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8586. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GPMC_CLKSEL_CLK_SEL	R/W	0h	Selects the GPMC clock source: Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV3_CLKOUT 1'b1 - MAIN_PLL2_HSDIV7_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.134 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register (Offset = 81B0h) [reset = 0h]

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Table 14-8587. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 81B0h**

Figure 14-2854. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER0_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8589. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.135 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register (Offset = 81B4h) [reset = 0h]

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Table 14-8590. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 81B4h**

Figure 14-2855. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER1_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8592. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.136 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register (Offset = 81B8h) [reset = 0h]

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Table 14-8593. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 81B8h

Figure 14-2856. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER2_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8595. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.137 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register (Offset = 81BCh) [reset = 0h]

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Table 14-8596. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 81BCh**

Figure 14-2857. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER3_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8598. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.138 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register (Offset = 81C0h) [reset = 0h]

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Table 14-8599. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 81C0h

Figure 14-2858. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8601. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.139 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register (Offset = 81C4h) [reset = 0h]

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Table 14-8602. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 81C4h

Figure 14-2859. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER5_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8604. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.140 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register (Offset = 81C8h) [reset = 0h]

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Table 14-8605. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 81C8h

Figure 14-2860. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER6_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8607. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.141 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register (Offset = 81CCh) [reset = 0h]

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Table 14-8608. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 81CCh

Figure 14-2861. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER7_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-8610. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.142 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register (Offset = 8200h) [reset = 0h]

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Table 14-8611. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8200h

Figure 14-2862. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI0_CLKSEL_MSTR_LB_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8613. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.143 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register (Offset = 8204h) [reset = 0h]

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Table 14-8614. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8204h

Figure 14-2863. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI1_CLKSEL_MSTR_LB_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8616. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.144 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register (Offset = 8208h) [reset = 0h]

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Table 14-8617. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8208h**

Figure 14-2864. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI2_CLKSEL_MSTR_LB_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8619. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.145 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register (Offset = 8240h) [reset = 3h]

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Table 14-8620. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8240h**

Figure 14-2865. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART0_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART0_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-8622. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART0 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.146 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register (Offset = 8244h) [reset = 3h]

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Table 14-8623. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8244h**

Figure 14-2866. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART1_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART1_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-8625. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART1 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.147 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register (Offset = 8248h) [reset = 3h]

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Table 14-8626. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8248h**

Figure 14-2867. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART2_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART2_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-8628. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART2 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.148 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register (Offset = 824Ch) [reset = 3h]

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Table 14-8629. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 824Ch**

Figure 14-2868. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART3_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART3_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-8631. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART3 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.149 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register (Offset = 8250h) [reset = 3h]

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Table 14-8632. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8250h**

Figure 14-2869. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART4_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-8634. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART4 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.150 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register (Offset = 8254h) [reset = 3h]

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Table 14-8635. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8254h**

Figure 14-2870. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART5_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART5_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-8637. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART5 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.151 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register (Offset = 8258h) [reset = 3h]

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Table 14-8638. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8258h**

Figure 14-2871. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART6_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART6_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-8640. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART6 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.152 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register (Offset = 8280h) [reset = 0h]

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Table 14-8641. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8280h**

Figure 14-2872. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART0_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8643. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART0: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART0_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.153 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register (Offset = 8284h) [reset = 0h]

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Table 14-8644. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8284h**

Figure 14-2873. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART1_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8646. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART1: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART1_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.154 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register (Offset = 8288h) [reset = 0h]

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Table 14-8647. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8288h**

Figure 14-2874. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART2_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8649. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART2: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART2_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.155 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register (Offset = 828Ch) [reset = 0h]

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Table 14-8650. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 828Ch

Figure 14-2875. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART3_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8652. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART3: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART3_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.156 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register (Offset = 8290h) [reset = 0h]

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Table 14-8653. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8290h**

Figure 14-2876. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART4_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8655. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART4: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART4_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.157 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register (Offset = 8294h) [reset = 0h]

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Table 14-8656. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8294h**

Figure 14-2877. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8658. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART5: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART5_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.158 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register (Offset = 8298h) [reset = 0h]

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Table 14-8659. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8298h**

Figure 14-2878. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-8661. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART6: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART6_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.159 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register (Offset = 82E0h) [reset = 7h]

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Table 14-8662. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 82E0h**

Figure 14-2879. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_REFCLK0_CTRL_CLKOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					AUDIO_REFCLK0_CTRL_CLK_SEL		
NONE					R/W		
0h					7h		

Table 14-8664. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK0_CTRL_CLKOUT_EN	R/W	0h	AUDIO_REFCLK 0 output activate Field values (others are reserved): 1'b0 - Input Clock 1'b1 - Output Clock Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	AUDIO_REFCLK0_CTRL_CLK_SEL	R/W	7h	Selects the source of AUDIO_REFCLK0 Field values (others are reserved): 3'b000 - MCASP0_AHCLKR 3'b001 - MCASP1_AHCLKR 3'b010 - MCASP2_AHCLKR 3'b011 - MCASP0_AHCLKX 3'b100 - MCASP1_AHCLKX 3'b101 - MCASP2_AHCLKX 3'b110 - MAIN_PLL1_HSDIV6_CLKOUT 3'b111 - MAIN_PLL2_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.160 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register (Offset = 82E4h) [reset = 7h]

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Table 14-8665. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 82E4h**

Figure 14-2880. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_REFCLK1_CTRL_CLKOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					AUDIO_REFCLK1_CTRL_CLK_SEL		
NONE					R/W		
0h					7h		

Table 14-8667. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK1_CTRL_CLKOUT_EN	R/W	0h	AUDIO_REFCLK 1 output activate Field values (others are reserved): 1'b0 - Input Clock 1'b1 - Output Clock Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	AUDIO_REFCLK1_CTRL_CLK_SEL	R/W	7h	Selects the source of AUDIO_REFCLK1 Field values (others are reserved): 3'b000 - MCASP0_AHCLKR 3'b001 - MCASP1_AHCLKR 3'b010 - MCASP2_AHCLKR 3'b011 - MCASP0_AHCLKX 3'b100 - MCASP1_AHCLKX 3'b101 - MCASP2_AHCLKX 3'b110 - MAIN_PLL1_HSDIV6_CLKOUT 3'b111 - MAIN_PLL2_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.161 MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL Register (Offset = 8300h) [reset = 0h]

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Table 14-8668. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8300h

Figure 14-2881. MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						DPI0_CLK_CTRL_SYNC_CLK_INVDIS	DPI0_CLK_CTRL_DATA_CLK_INVDIS
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8670. MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	DPI0_CLK_CTRL_SYNC_CLK_INVDIS	R/W	0h	Clock edge select for DPI0 sync outputs Note that this value should be the same as the programmed value of DSS_POL_FREQ[16] RF. Reset Source: mod_por_rst_n 0 `HSYNC and VSYNC are driven on the falling edge of clk` 1 `HSYNC and VSYNC are driven on the rising edge of clk`
8	DPI0_CLK_CTRL_DATA_CLK_INVDIS	R/W	0h	Clock edge select for DPI0 data outputs Note that this value should be the same as the programmed value of DSS_POL_FREQ[14] IPC. Reset Source: mod_por_rst_n 0 `DATA and DE are driven on the falling edge of clk` 1 `DATA and DE are driven on the rising edge of clk`
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.162 MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1 Register

1 MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1 Register (Offset = 8320h) [reset = 0h]

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Table 14-8671. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8320h**

Figure 14-2882. MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DSS_DISPC0_CLKSEL1_DPI_PCLK
NONE							R/W
0h							0h

Table 14-8673. MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DSS_DISPC0_CLKSEL1_DPI_PCLK	R/W	0h	DPI pixel Clock Source Field values (others are reserved): 1'b0 - MAIN_PLL17_HSDIV0_CLKOUT 1'b1 - VOUT0_EXTPCLKIN Reset Source: mod_por_rst_n

14.2.1.1.1.2.163 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register (Offset = 8330h) [reset = 0h]

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Table 14-8674. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8330h**

Figure 14-2883. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP0_CLKSEL_AUXCLK_SEL
NONE							R/W
0h							0h

Table 14-8676. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP0_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.164 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register (Offset = 8334h) [reset = 0h]

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Table 14-8677. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8334h

Figure 14-2884. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP1_CLKSEL_AUXCLK_SEL
NONE							R/W
0h							0h

Table 14-8679. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP1_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.165 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register (Offset = 8338h) [reset = 0h]

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Table 14-8680. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8338h

Figure 14-2885. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP2_CLKSEL_AUXCLK_SEL
NONE							R/W
0h							0h

Table 14-8682. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP2_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.166 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register (Offset = 8350h) [reset = 0h]

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Table 14-8683. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8350h

Figure 14-2886. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP0_AHCLKSEL_AHCLKX_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP0_AHCLKSEL_AHCLKR_SEL	
NONE						R/W	
0h						0h	

Table 14-8685. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP0_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP0 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP0_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP0 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.167 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register (Offset = 8354h) [reset = 0h]

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Table 14-8686. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8354h**

Figure 14-2887. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP1_AHCLKSEL_AHCLKX_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP1_AHCLKSEL_AHCLKR_SEL	
NONE						R/W	
0h						0h	

Table 14-8688. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP1_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP1 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP1_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP1 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.168 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register (Offset = 8358h) [reset = 0h]

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Table 14-8689. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8358h**

Figure 14-2888. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP2_AHCLKSEL_AHCLKX_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP2_AHCLKSEL_AHCLKR_SEL	
NONE						R/W	
0h						0h	

Table 14-8691. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP2_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP2 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP2_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP2 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.169 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register (Offset = 8380h) [reset = 0h]

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Table 14-8692. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8380h

Figure 14-2889. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8694. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.170 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register (Offset = 8384h) [reset = 0h]

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Table 14-8695. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8384h

Figure 14-2890. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8697. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.171 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register (Offset = 8388h) [reset = 0h]

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Table 14-8698. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 8388h

Figure 14-2891. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD2_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD2_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8700. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD2_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD2_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD2_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.172 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register (Offset = 838Ch) [reset = 0h]

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Table 14-8701. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 838Ch

Figure 14-2892. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD3_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD3_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8703. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD3_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD3_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD3_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.173 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register (Offset = 8390h) [reset = 0h]

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Table 14-8704. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8390h**

Figure 14-2893. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD4_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD4_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8706. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD4_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD4_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD4_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.174 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register (Offset = 8480h) [reset = 0h]

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Table 14-8707. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8480h**

Figure 14-2894. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-8709. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL	R/W	0h	MAIN MCAN_CLK selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - EXT_REFCLK1 (pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.175 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register (Offset = 8500h) [reset = 0h]

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Table 14-8710. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 8500h**

Figure 14-2895. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL	RESERVED			OSPI0_CLKSEL_CLK_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-8712. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL	R/W	0h	OBSPI0 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL	R/W	0h	OSPI0 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.176 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-8713. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9008h**

Figure 14-2896. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-8715. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.177 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-8716. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 900Ch**

Figure 14-2897. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-8718. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.178 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8719. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9100h**

Figure 14-2898. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-8721. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.179 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8722. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9104h**

Figure 14-2899. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-8724. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.180 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register (Offset = 9108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8725. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9108h**

Figure 14-2900. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2_READONLY							
R							
0h							

Table 14-8727. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.181 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register (Offset = 910Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-8728. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 910Ch**

Figure 14-2901. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3_READONLY							
R							
0h							

Table 14-8730. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.182 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register (Offset = 9110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8731. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9110h**

Figure 14-2902. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4_READONLY							
R							
0h							

Table 14-8733. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.183 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register (Offset = 9114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8734. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9114h**

Figure 14-2903. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5_READONLY							
R							
0h							

Table 14-8736. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.184 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register (Offset = 9118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8737. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9118h**

Figure 14-2904. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6_READONLY							
R							
0h							

Table 14-8739. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.185 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register (Offset = 911Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-8740. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 911Ch**

Figure 14-2905. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7_READONLY							
R							
0h							

Table 14-8742. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.186 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register (Offset = 9120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8743. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9120h**

Figure 14-2906. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8_READONLY							
R							
0h							

Table 14-8745. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.187 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register (Offset = 9124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8746. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9124h**

Figure 14-2907. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9_READONLY							
R							
0h							

Table 14-8748. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.188 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register (Offset = 9128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8749. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 9128h**

Figure 14-2908. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R10_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R10_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R10_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R10_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8751. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.189 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register (Offset = A000h) [reset = 7h]

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Table 14-8752. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A000h**

Figure 14-2909. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							OBSCLK0_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OBSCLK0_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OBSCLK0_CTRL_CLK_DIV_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			OBSCLK0_CTRL_CLK_SEL_PROXY				
NONE			R/W				
0h			7h				

Table 14-8754. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	OBSCLK0_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 5'b11111. 1'b0 - The output of the MCU_OBSCLK output divider is output on the pin 1'b1 - HFOSC0_CLK is output on the pin Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK0 divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_por_rst_n

Table 14-8754. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	OBSCLK0_CTRL_CLK_DIV_PROXY	R/W	0h	OBSCLK0 output divider Divides the selected clock by clkdiv+1 for output to the OBSCLK0 pins. Supports divide by 1 to 256 (default to 1). To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	OBSCLK0_CTRL_CLK_SEL_PROXY	R/W	7h	OBSCLK0 clock source selection. Selects the source of the clock to be divided by the OBSCLK0 divider and output on the OBSCLK0 pin. Field values (others are reserved): 5'b00000 - MAIN_PLL0_HSDIV0_CLKOUT 5'b00001 - MAIN_PLL1_HSDIV0_CLKOUT 5'b00010 - MAIN_PLL2_HSDIV0_CLKOUT 5'b00011 - MAIN_PLL8_HSDIV0_CLKOUT_DIV4 5'b00100 - MAIN_PLL12_HSDIV0_CLKOUT_DIV4 5'b00101 - CLK_12M_RC 5'b00110 - HFOSC0_CLKOUT_32K 5'b00111 - PLLCTRL_OBSCLK 5'b01000 - HFOSC0_CLKOUT 5'b01001 - CLK_32K 5'b01010 - cpsw2g_cpts_genf0 5'b01011 - cpsw2g_cpts_genf1 5'b01100 - MCU_PLL0_HSDIV0_CLKOUT 5'b01101 - MAIN_PLL15_HSDIV0_CLKOUT undefined - undefined 5'b01110 - reserved 5'b01111 - MAIN_PLL17_HSDIV0_CLKOUT 5'b10000 - MAIN_SYSCLK0 5'b10001 - DEVICE_CLKOUT_32K 5'b10010 - MAIN_PLL5_HSDIV0_CLKOUT 5'b10011 - MAIN_PLL7_HSDIV0_CLKOUT_DIV4 Reset Source: mod_por_rst_n

14.2.1.1.1.2.190 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

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Table 14-8755. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A010h**

Figure 14-2910. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RSVD	RESERVED			CLKOUT_CTRL_CLK_SEL_PROXY
NONE				NONE			R/W
0h			0h	0h			0h

Table 14-8757. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL_PROXY	R/W	0h	Selects CLKOUT clock source Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV1_CLKOUT / 5 1'b1 - MAIN_PLL2_HSDIV1_CLKOUT / 10 Reset Source: mod_g_rst_n

14.2.1.1.1.2.191 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register (Offset = A060h) [reset = 800000h]

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Table 14-8758. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A060h

Figure 14-2911. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8760. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b0) when a MAIN warm reset occurs to keep MAIN PLL0 from being bypassed, supporting reset isolation of the CPSW. 1'b0 = Exit bypass mode (based on MAIN PLL0_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.192 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register (Offset = A064h) [reset = 800000h]

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Table 14-8761. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A064h**

Figure 14-2912. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8763. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL1 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL1 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL1 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.193 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register (Offset = A068h) [reset = 800000h]

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Table 14-8764. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A068h**

Figure 14-2913. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8766. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL2 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL2 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL2 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.194 MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL_PROXY Register (Offset = A074h) [reset = 800000h]

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Table 14-8767. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A074h**

Figure 14-2914. MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL5_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL5_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-8769. MAIN_CTRL_MMR_CFG0_MAIN_PLL5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL5_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL5. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL5_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL5 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL5_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.195 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register (Offset = A07Ch) [reset = 800000h]

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Table 14-8770. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A07Ch

Figure 14-2915. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL7_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8772. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL7. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL7_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL7 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL7_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.196 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register (Offset = A080h) [reset = 800000h]

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Table 14-8773. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A080h

Figure 14-2916. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL8_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-8775. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL8. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL8_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL8 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL8_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.197 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register (Offset = A090h) [reset = 800000h]

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Table 14-8776. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A090h**

Figure 14-2917. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL12_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8778. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a main_reset_z for MAIN PLL12. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL12_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL12 in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MAIN PLL12_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.198 MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL_PROXY Register (Offset = A0A4h) [reset = 800000h]

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Table 14-8779. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A0A4h**

Figure 14-2918. MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL17_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL17_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8781. MAIN_CTRL_MMR_CFG0_MAIN_PLL17_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL17_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL17 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL17_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is cleared to 1'b0 when a MAIN warm reset occurs which will cause MAIN PLL17 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL17 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.199 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register (Offset = A140h) [reset = 7h]

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Table 14-8782. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A140h**

Figure 14-2919. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_CLKSEL_CPTS_CLKSEL_PROXY		
NONE					R/W		
0h					7h		

Table 14-8784. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CLKSEL_CPTS_CLKSEL_PROXY	R/W	7h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - MCU_SYSCLK0 undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_por_rst_n

14.2.1.1.1.2.200 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register (Offset = A160h) [reset = 0h]

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Table 14-8785. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A160h**

Figure 14-2920. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8787. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD0_CLKLB 1'b1 - Loopback from IO Pin MMCSD0_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD_REFCLK_SEL_PROXY	R/W	0h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.201 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register (Offset = A168h) [reset = 1h]

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Table 14-8788. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A168h

Figure 14-2921. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>EMMC1_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EMMC1_CLKSEL_EMMCSD_REFCLK_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-8790. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC1_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD1_CLKLB 1'b1 - Loopback from IO Pin MMCSD1_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC1_CLKSEL_EMMCSD_REFCLK_SEL_PROXY	R/W	1h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.202 MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL_PROXY Register (Offset = A16Ch) [reset = 1h]

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Table 14-8791. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A16Ch

Figure 14-2922. MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC2_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC2_CLKSEL_EMMCSD_REFCLK_SEL_PROXY
NONE							R/W
0h							1h

Table 14-8793. MAIN_CTRL_MMR_CFG0_EMMC2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC2_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD2_CLKLB 1'b1 - Loopback from IO Pin MMCSD2_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC2_CLKSEL_EMMCSD_REFCLK_SEL_PROXY	R/W	1h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.203 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register (Offset = A180h) [reset = 0h]

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Table 14-8794. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A180h**

Figure 14-2923. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GPMC_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8796. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GPMC_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the GPMC clock source: Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV3_CLKOUT 1'b1 - MAIN_PLL2_HSDIV7_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.204 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register (Offset = A1B0h) [reset = 0h]

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Table 14-8797. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1B0h

Figure 14-2924. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER0_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8799. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.205 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register (Offset = A1B4h) [reset = 0h]

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Table 14-8800. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1B4h

Figure 14-2925. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER1_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8802. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.206 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register (Offset = A1B8h) [reset = 0h]

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Table 14-8803. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1B8h

Figure 14-2926. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER2_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8805. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.207 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register (Offset = A1BCh) [reset = 0h]

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Table 14-8806. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1BCh

Figure 14-2927. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER3_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8808. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.208 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register (Offset = A1C0h) [reset = 0h]

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Table 14-8809. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1C0h

Figure 14-2928. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8811. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.209 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register (Offset = A1C4h) [reset = 0h]

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Table 14-8812. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A1C4h**

Figure 14-2929. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER5_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8814. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.210 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register (Offset = A1C8h) [reset = 0h]

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Table 14-8815. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1C8h

Figure 14-2930. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				TIMER6_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8817. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.211 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register (Offset = A1CCh) [reset = 0h]

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Table 14-8818. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A1CCh

Figure 14-2931. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER7_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-8820. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (pin) 4'b0101 - EXT_REFCLK1 (pin) 4'b0110 - Reserved 4'b0111 - CPSW2G_CPTS_RFT_CLK 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW2G_CPTS_GENF0 4'b1011 - CPSW2G_CPTS_GENF1 4'b1100 - Reserved 4'b1101 - Reserved 4'b1110 - Reserved 4'b1111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.212 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register (Offset = A200h) [reset = 0h]

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Table 14-8821. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0010 A200h**

Figure 14-2932. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8823. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.213 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register (Offset = A204h) [reset = 0h]

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Table 14-8824. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A204h**

Figure 14-2933. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8826. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.214 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register (Offset = A208h) [reset = 0h]

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Table 14-8827. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A208h**

Figure 14-2934. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-8829. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - Internal Loopback 1'b1 - External Loopback Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.215 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register (Offset = A240h) [reset = 3h]

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Table 14-8830. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A240h

Figure 14-2935. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART0_CLK_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART0_CLK_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-8832. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART0 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.216 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register (Offset = A244h) [reset = 3h]

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Table 14-8833. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A244h

Figure 14-2936. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART1_CLK_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART1_CLK_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-8835. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART1 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.217 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register (Offset = A248h) [reset = 3h]

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Table 14-8836. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A248h

Figure 14-2937. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART2_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART2_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-8838. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART2 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.218 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register (Offset = A24Ch) [reset = 3h]

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Table 14-8839. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A24Ch

Figure 14-2938. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART3_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART3_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-8841. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART3 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.219 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register (Offset = A250h) [reset = 3h]

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Table 14-8842. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A250h

Figure 14-2939. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART4_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-8844. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART4 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.220 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register (Offset = A254h) [reset = 3h]

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Table 14-8845. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A254h

Figure 14-2940. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							USART5_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED						USART5_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-8847. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART5 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.221 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register (Offset = A258h) [reset = 3h]

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Table 14-8848. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A258h

Figure 14-2941. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART6_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART6_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-8850. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART6 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.222 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register (Offset = A280h) [reset = 0h]

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Table 14-8851. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A280h

Figure 14-2942. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART0_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8853. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART0: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART0_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.223 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register (Offset = A284h) [reset = 0h]

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Table 14-8854. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A284h**

Figure 14-2943. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART1_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8856. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART1: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART1_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.224 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register (Offset = A288h) [reset = 0h]

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Table 14-8857. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0010 A288h**

Figure 14-2944. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							USART2_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8859. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART2: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART2_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.225 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register (Offset = A28Ch) [reset = 0h]

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Table 14-8860. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A28Ch

Figure 14-2945. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART3_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8862. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART3: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART3_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.226 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register (Offset = A290h) [reset = 0h]

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Table 14-8863. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A290h**

Figure 14-2946. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART4_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8865. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART4: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART4_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.227 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register (Offset = A294h) [reset = 0h]

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Table 14-8866. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A294h

Figure 14-2947. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8868. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART5: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART5_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.228 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register (Offset = A298h) [reset = 0h]

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Table 14-8869. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A298h**

Figure 14-2948. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8871. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART6: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART6_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.229 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register (Offset = A2E0h) [reset = 7h]

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Table 14-8872. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A2E0h

Figure 14-2949. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>AUDIO_REFCLK0_CTRL_CLKOUT_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">AUDIO_REFCLK0_CTRL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">7h</td></tr>
</table>

Table 14-8874. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK0_CTRL_CLKOUT_EN_PROXY	R/W	0h	AUDIO_REFCLK 0 output activate Field values (others are reserved): 1'b0 - Input Clock 1'b1 - Output Clock Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	AUDIO_REFCLK0_CTRL_CLK_SEL_PROXY	R/W	7h	Selects the source of AUDIO_REFCLK0 Field values (others are reserved): 3'b000 - MCASP0_AHCLKR 3'b001 - MCASP1_AHCLKR 3'b010 - MCASP2_AHCLKR 3'b011 - MCASP0_AHCLKX 3'b100 - MCASP1_AHCLKX 3'b101 - MCASP2_AHCLKX 3'b110 - MAIN_PLL1_HSDIV6_CLKOUT 3'b111 - MAIN_PLL2_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.230 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register (Offset = A2E4h) [reset = 7h]

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Table 14-8875. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A2E4h**

Figure 14-2950. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_REFCLK1_CTRL_CLKOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					AUDIO_REFCLK1_CTRL_CLK_SEL_PROXY		
NONE					R/W		
0h					7h		

Table 14-8877. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK1_CTRL_CLKOUT_EN_PROXY	R/W	0h	AUDIO_REFCLK 1 output activate Field values (others are reserved): 1'b0 - Input Clock 1'b1 - Output Clock Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	AUDIO_REFCLK1_CTRL_CLK_SEL_PROXY	R/W	7h	Selects the source of AUDIO_REFCLK1 Field values (others are reserved): 3'b000 - MCASP0_AHCLKR 3'b001 - MCASP1_AHCLKR 3'b010 - MCASP2_AHCLKR 3'b011 - MCASP0_AHCLKX 3'b100 - MCASP1_AHCLKX 3'b101 - MCASP2_AHCLKX 3'b110 - MAIN_PLL1_HSDIV6_CLKOUT 3'b111 - MAIN_PLL2_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.231 MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL_PROXY Register (Offset = A300h) [reset = 0h]

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Table 14-8878. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A300h**

Figure 14-2951. MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>DPI0_CLK_CTRL_SYNC_CLK_INVDIS_PROXY</td><td>DPI0_CLK_CTRL_DATA_CLK_INVDIS_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8880. MAIN_CTRL_MMR_CFG0_DPI0_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	DPI0_CLK_CTRL_SYNC_CLK_INVDIS_PROXY	R/W	0h	Clock edge select for DPI0 sync outputs Note that this value should be the same as the programmed value of DSS_POL_FREQ[16] RF. Reset Source: mod_por_rst_n 0 `HSYNC and VSYNC are driven on the falling edge of clk` 1 `HSYNC and VSYNC are driven on the rising edge of clk`
8	DPI0_CLK_CTRL_DATA_CLK_INVDIS_PROXY	R/W	0h	Clock edge select for DPI0 data outputs Note that this value should be the same as the programmed value of DSS_POL_FREQ[14] IPC. Reset Source: mod_por_rst_n 0 `DATA and DE are driven on the falling edge of clk` 1 `DATA and DE are driven on the rising edge of clk`
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.232 MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1_PROXY Register (Offset = A320h) [reset = 0h]

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Table 14-8881. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A320h

Figure 14-2952. MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DSS_DISPC0_CLKSEL1_DPI_PCLK_PROXY
NONE							R/W
0h							0h

Table 14-8883. MAIN_CTRL_MMR_CFG0_DSS_DISPC0_CLKSEL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DSS_DISPC0_CLKSEL1_DPI_PCLK_PROXY	R/W	0h	DPI pixel Clock Source Field values (others are reserved): 1'b0 - MAIN_PLL17_HSDIV0_CLKOUT 1'b1 - VOUT0_EXTPCLKIN Reset Source: mod_por_rst_n

14.2.1.1.1.2.233 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register (Offset = A330h) [reset = 0h]

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Table 14-8884. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A330h**

Figure 14-2953. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP0_CLKSEL_AUXCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8886. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP0_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.234 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register (Offset = A334h) [reset = 0h]

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Table 14-8887. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A334h**

Figure 14-2954. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP1_CLKSEL_AUXCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8889. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP1_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.235 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register (Offset = A338h) [reset = 0h]

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Table 14-8890. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A338h

Figure 14-2955. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCASP2_CLKSEL_AUXCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-8892. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCASP2_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the AUXCLK input source for McASP0 Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV8_CLKOUT 1'b1 - MAIN_PLL1_HSDIV6_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.236 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register (Offset = A350h) [reset = 0h]

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Table 14-8893. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A350h**

Figure 14-2956. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP0_AHCLKSEL_AHCLKX_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP0_AHCLKSEL_AHCLKR_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8895. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP0_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP0 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP0_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP0 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.237 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register (Offset = A354h) [reset = 0h]

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Table 14-8896. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A354h

Figure 14-2957. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP1_AHCLKSEL_AHCLKX_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP1_AHCLKSEL_AHCLKR_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8898. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP1_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP1 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP1_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP1 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.238 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register (Offset = A358h) [reset = 0h]

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Table 14-8899. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A358h**

Figure 14-2958. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP2_AHCLKSEL_AHCLKX_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						MCASP2_AHCLKSEL_AHCLKR_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8901. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP2_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP2 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	MCASP2_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP2 Field values (others are reserved): 2'b00 - EXT_REFCLK1 (pin) 2'b01 - HFOSC0_CLKOUT 2'b10 - AUDIO_EXT_REFCLK0_IN 2'b11 - AUDIO_EXT_REFCLK1_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.239 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register (Offset = A380h) [reset = 0h]

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Table 14-8902. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A380h**

Figure 14-2959. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8904. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.240 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register (Offset = A384h) [reset = 0h]

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Table 14-8905. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A384h**

Figure 14-2960. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8907. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.241 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register (Offset = A388h) [reset = 0h]

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Table 14-8908. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0010 A388h

Figure 14-2961. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WWD2_CLKSEL_WRTLOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">WWD2_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-8910. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD2_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD2_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.242 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register (Offset = A38Ch) [reset = 0h]

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Table 14-8911. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A38Ch**

Figure 14-2962. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD3_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD3_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8913. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD3_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD3_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.243 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register (Offset = A390h) [reset = 0h]

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Table 14-8914. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A390h**

Figure 14-2963. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD4_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD4_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8916. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD4_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD4_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.244 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register (Offset = A480h) [reset = 0h]

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Table 14-8917. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A480h**

Figure 14-2964. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-8919. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL_PROXY	R/W	0h	MAIN MCAN_CLK selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - EXT_REFCLK1 (pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.245 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register (Offset = A500h) [reset = 0h]

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Table 14-8920. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 A500h**

Figure 14-2965. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	RESERVED			OSPI0_CLKSEL_CLK_SEL_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-8922. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	R/W	0h	OBSPI0 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL_PROXY	R/W	0h	OSPI0 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.246 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-8923. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B008h**

Figure 14-2966. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-8925. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.247 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-8926. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B00Ch**

Figure 14-2967. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-8928. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.248 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8929. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B100h**

Figure 14-2968. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-8931. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.249 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8932. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B104h**

Figure 14-2969. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-8934. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.250 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register (Offset = B108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8935. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B108h**

Figure 14-2970. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2							
R/W							
0h							

Table 14-8937. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.251 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register (Offset = B10Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-8938. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B10Ch**

Figure 14-2971. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8940. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.252 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register (Offset = B110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8941. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B110h**

Figure 14-2972. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4							
R/W							
0h							

Table 14-8943. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.253 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register (Offset = B114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8944. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B114h**

Figure 14-2973. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5							
R/W							
0h							

Table 14-8946. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.254 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register (Offset = B118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8947. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B118h**

Figure 14-2974. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6							
R/W							
0h							

Table 14-8949. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.255 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register (Offset = B11Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-8950. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B11Ch**

Figure 14-2975. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7							
R/W							
0h							

Table 14-8952. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.256 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register (Offset = B120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8953. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B120h**

Figure 14-2976. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8							
R/W							
0h							

Table 14-8955. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.257 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register (Offset = B124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8956. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B124h**

Figure 14-2977. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8958. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.258 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register (Offset = B128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-8959. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0010 B128h**

Figure 14-2978. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10							
R/W							
0h							

Table 14-8961. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.259 MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL Register (Offset = 10500h) [reset = 0h]

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Table 14-8962. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0011 0500h

Figure 14-2979. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL17	RESERVED
NONE						R/W	NONE
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL12	RESERVED			MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL8
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL7	RESERVED	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL5	RESERVED		MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL2	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL1	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL0
R/W	NONE	R/W	NONE		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-8964. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL17	R/W	0h	Selects the alternate clock source for MAIN PLL17 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
16:13	RESERVED	NONE	0h	Reserved
12	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL12	R/W	0h	Selects the alternate clock source for MAIN PLL12 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved

Table 14-8964. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL8	R/W	0h	Selects the alternate clock source for MAIN PLL8 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
7	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL7	R/W	0h	Selects the alternate clock source for MAIN PLL7 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
6	RESERVED	NONE	0h	Reserved
5	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL5	R/W	0h	Selects the alternate clock source for MAIN PLL5 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
4:3	RESERVED	NONE	0h	Reserved
2	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL2	R/W	0h	Selects the alternate clock source for MAIN PLL2 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
1	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL1	R/W	0h	Selects the alternate clock source for MAIN PLL1 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
0	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL0	R/W	0h	Selects the alternate clock source for MAIN PLL0 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n

14.2.1.1.1.2.260 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-8965. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1008h**

Figure 14-2980. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0							
R/W							
0h							

Table 14-8967. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.261 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-8968. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 100Ch**

Figure 14-2981. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-8970. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.262 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8971. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1100h**

Figure 14-2982. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-8973. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.263 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register (Offset = 11104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8974. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1104h**

Figure 14-2983. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8976. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.264 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register (Offset = 11108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8977. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1108h**

Figure 14-2984. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2_READONLY							
R							
0h							

Table 14-8979. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.265 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register (Offset = 1110Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-8980. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 110Ch**

Figure 14-2985. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3_READONLY							
R							
0h							

Table 14-8982. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.266 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register (Offset = 11110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8983. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1110h**

Figure 14-2986. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4_READONLY							
R							
0h							

Table 14-8985. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.267 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register (Offset = 11114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8986. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1114h**

Figure 14-2987. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5_READONLY							
R							
0h							

Table 14-8988. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.268 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register (Offset = 11118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8989. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1118h**

Figure 14-2988. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8991. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.269 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register (Offset = 1111Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-8992. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 111Ch**

Figure 14-2989. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7_READONLY							
R							
0h							

Table 14-8994. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.270 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8995. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1120h**

Figure 14-2990. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-8997. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.271 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register (Offset = 11124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-8998. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1124h**

Figure 14-2991. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9_READONLY							
R							
0h							

Table 14-9000. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.272 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register (Offset = 11128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9001. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 1128h**

Figure 14-2992. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P4_R10_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P4_R10_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P4_R10_READONLY							
R							
0h							

Table 14-9003. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.273 MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY Register (Offset = 12500h) [reset = 0h]

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Table 14-9004. Instance Table

Instance Name	Physical Address
CTRL_MMR0	0011 2500h

Figure 14-2993. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL17_PROXY	RESERVED
NONE						R/W	NONE
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL12_PROXY	RESERVED			MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL8_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL7_PROXY	RESERVED	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL5_PROXY	RESERVED		MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL2_PROXY	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL1_PROXY	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL0_PROXY
R/W	NONE	R/W	NONE		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-9006. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL17_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL17 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
16:13	RESERVED	NONE	0h	Reserved
12	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL12_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL12 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved

Table 14-9006. MAIN_CTRL_MMR_CFG0_MAIN_PLL_TEST_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL8_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL8 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
7	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL7_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL7 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
6	RESERVED	NONE	0h	Reserved
5	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL5_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL5 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
4:3	RESERVED	NONE	0h	Reserved
2	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL2_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL2 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
1	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL1_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL1 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n
0	MAIN_PLL_TEST_CLKSEL_CLK_SEL_PLL0_PROXY	R/W	0h	Selects the alternate clock source for MAIN PLL0 Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - EXT_REFCLK1 pin Reset Source: mod_por_rst_n

14.2.1.1.1.2.274 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-9007. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3008h**

Figure 14-2994. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-9009. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.275 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-9010. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 300Ch**

Figure 14-2995. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-9012. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.276 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9013. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3100h**

Figure 14-2996. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-9015. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.277 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9016. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3104h**

Figure 14-2997. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-9018. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.278 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9019. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3108h**

Figure 14-2998. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-9021. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.279 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9022. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 310Ch**

Figure 14-2999. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-9024. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.280 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9025. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3110h**

Figure 14-3000. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-9027. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.281 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9028. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3114h**

Figure 14-3001. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-9030. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.282 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9031. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3118h**

Figure 14-3002. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-9033. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.283 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9034. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 311Ch**

Figure 14-3003. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-9036. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.284 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9037. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3120h**

Figure 14-3004. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-9039. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.285 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9040. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3124h**

Figure 14-3005. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-9042. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.286 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9043. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 3128h**

Figure 14-3006. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9045. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.287 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-9046. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9008h**

Figure 14-3007. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-9048. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.288 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-9049. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 900Ch**

Figure 14-3008. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-9051. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.289 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9052. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9100h**

Figure 14-3009. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-9054. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.290 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9055. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9104h**

Figure 14-3010. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-9057. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.291 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9058. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9108h**

Figure 14-3011. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-9060. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.292 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9061. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 910Ch**

Figure 14-3012. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-9063. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.293 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9064. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9110h**

Figure 14-3013. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-9066. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.294 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9067. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**0011 9114h**

Figure 14-3014. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5_READONLY							
R							
0h							

Table 14-9069. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.295 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register (Offset = 19118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9070. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9118h**

Figure 14-3015. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6_READONLY							
R							
0h							

Table 14-9072. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.296 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register (Offset = 1911Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9073. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 911Ch**

Figure 14-3016. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7_READONLY							
R							
0h							

Table 14-9075. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.297 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register (Offset = 19120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9076. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 9120h**

Figure 14-3017. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8_READONLY							
R							
0h							

Table 14-9078. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.298 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-9079. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B008h**

Figure 14-3018. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-9081. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.299 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-9082. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B00Ch**

Figure 14-3019. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-9084. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.300 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9085. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B100h**

Figure 14-3020. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-9087. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.301 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9088. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B104h**

Figure 14-3021. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-9090. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.302 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9091. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B108h**

Figure 14-3022. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-9093. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.303 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9094. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B10Ch**

Figure 14-3023. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-9096. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.304 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9097. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B110h**

Figure 14-3024. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-9099. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.305 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9100. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B114h**

Figure 14-3025. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5							
R/W							
0h							

Table 14-9102. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.306 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register (Offset = 1B118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9103. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B118h**

Figure 14-3026. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6							
R/W							
0h							

Table 14-9105. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.307 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register (Offset = 1B11Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9106. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B11Ch**

Figure 14-3027. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7							
R/W							
0h							

Table 14-9108. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.308 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register (Offset = 1B120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9109. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**0011 B120h**

Figure 14-3028. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8							
R/W							
0h							

Table 14-9111. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2 MCU_CTRL_MMR

MCU_CTRL_MMR

14.2.1.1.2.1 MCU_CTRL_MMR Summaries

MCU_CTRL_MMR Summaries

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
0h	32	MCU_CTRL_MMR_CFG0_PID	0450 0000h
8h	32	MCU_CTRL_MMR_CFG0_MMR_CFG1	0450 0008h
100h	32	MCU_CTRL_MMR_CFG0_IPC_SET0	0450 0100h
180h	32	MCU_CTRL_MMR_CFG0_IPC_CLR0	0450 0180h
270h	32	MCU_CTRL_MMR_CFG0_CBA_ERR_STAT	0450 0270h
280h	32	MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT	0450 0280h
1008h	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK0	0450 1008h
100Ch	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK1	0450 100Ch
1010h	32	MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS	0450 1010h
1014h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0450 1014h
1018h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE	0450 1018h
101Ch	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0450 101Ch
1020h	32	MCU_CTRL_MMR_CFG0_EOI	0450 1020h
1024h	32	MCU_CTRL_MMR_CFG0_FAULT_ADDRESS	0450 1024h
1028h	32	MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0450 1028h
102Ch	32	MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0450 102Ch
1030h	32	MCU_CTRL_MMR_CFG0_FAULT_CLEAR	0450 1030h
1100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0450 1100h
1104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY	0450 1104h
1108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY	0450 1108h
110Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY	0450 110Ch
1110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY	0450 1110h
1114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY	0450 1114h
2000h	32	MCU_CTRL_MMR_CFG0_PID_PROXY	0450 2000h
2008h	32	MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0450 2008h
2100h	32	MCU_CTRL_MMR_CFG0_IPC_SET0_PROXY	0450 2100h
2180h	32	MCU_CTRL_MMR_CFG0_IPC_CLR0_PROXY	0450 2180h
2270h	32	MCU_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY	0450 2270h
2280h	32	MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY	0450 2280h
3008h	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0450 3008h
300Ch	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0450 300Ch
3010h	32	MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0450 3010h
3014h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0450 3014h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
3018h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0450 3018h
301Ch	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0450 301Ch
3020h	32	MCU_CTRL_MMR_CFG0_EOI_PROXY	0450 3020h
3024h	32	MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0450 3024h
3028h	32	MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0450 3028h
302Ch	32	MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0450 302Ch
3030h	32	MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0450 3030h
3100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0450 3100h
3104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1	0450 3104h
3108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2	0450 3108h
310Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3	0450 310Ch
3110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4	0450 3110h
3114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5	0450 3114h
4020h	32	MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL	0450 4020h
4084h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1	0450 4084h
4088h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2	0450 4088h
408Ch	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3	0450 408Ch
4090h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4	0450 4090h
4094h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5	0450 4094h
4098h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6	0450 4098h
40A0h	32	MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM	0450 40A0h
40B0h	32	MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT	0450 40B0h
4204h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL	0450 4204h
420Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL	0450 420Ch
42E0h	32	MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL	0450 42E0h
4604h	32	MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0	0450 4604h
4608h	32	MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1	0450 4608h
4610h	32	MCU_CTRL_MMR_CFG0_TOG_STAT	0450 4610h
5008h	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK0	0450 5008h
500Ch	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK1	0450 500Ch
5100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0450 5100h
5104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	0450 5104h
5108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	0450 5108h
510Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	0450 510Ch
5110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	0450 5110h
5114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	0450 5114h
5118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	0450 5118h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
511Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY	0450 511Ch
5120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	0450 5120h
5124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	0450 5124h
5128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY	0450 5128h
512Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY	0450 512Ch
5130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	0450 5130h
6020h	32	MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL_PROXY	0450 6020h
6084h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY	0450 6084h
6088h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY	0450 6088h
608Ch	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY	0450 608Ch
6090h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY	0450 6090h
6094h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY	0450 6094h
6098h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY	0450 6098h
60A0h	32	MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY	0450 60A0h
60B0h	32	MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY	0450 60B0h
6204h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY	0450 6204h
620Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY	0450 620Ch
62E0h	32	MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY	0450 62E0h
6604h	32	MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY	0450 6604h
6608h	32	MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY	0450 6608h
6610h	32	MCU_CTRL_MMR_CFG0_TOG_STAT_PROXY	0450 6610h
7008h	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0450 7008h
700Ch	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0450 700Ch
7100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0450 7100h
7104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0450 7104h
7108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2	0450 7108h
710Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3	0450 710Ch
7110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4	0450 7110h
7114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5	0450 7114h
7118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6	0450 7118h
711Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7	0450 711Ch
7120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8	0450 7120h
7124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9	0450 7124h
7128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10	0450 7128h
712Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11	0450 712Ch
7130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12	0450 7130h
8000h	32	MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL	0450 8000h
8010h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CTRL	0450 8010h
8018h	32	MCU_CTRL_MMR_CFG0_HFOSC0_TRIM	0450 8018h
8020h	32	MCU_CTRL_MMR_CFG0_HFOSC0_STAT	0450 8020h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
8024h	32	MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM	0450 8024h
8030h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL	0450 8030h
8038h	32	MCU_CTRL_MMR_CFG0_LFXOSC_CTRL	0450 8038h
803Ch	32	MCU_CTRL_MMR_CFG0_LFXOSC_TRIM	0450 803Ch
8050h	32	MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL	0450 8050h
8058h	32	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL	0450 8058h
8060h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL	0450 8060h
8064h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL	0450 8064h
8068h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL	0450 8068h
806Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL	0450 806Ch
8070h	32	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL	0450 8070h
8080h	32	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL	0450 8080h
8084h	32	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL	0450 8084h
80A0h	32	MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL	0450 80A0h
80A4h	32	MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL	0450 80A4h
80B0h	32	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL	0450 80B0h
9008h	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK0	0450 9008h
900Ch	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK1	0450 900Ch
9100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	0450 9100h
9104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	0450 9104h
A000h	32	MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY	0450 A000h
A010h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY	0450 A010h
A018h	32	MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY	0450 A018h
A020h	32	MCU_CTRL_MMR_CFG0_HFOSC0_STAT_PROXY	0450 A020h
A024h	32	MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY	0450 A024h
A030h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY	0450 A030h
A038h	32	MCU_CTRL_MMR_CFG0_LFXOSC_CTRL_PROXY	0450 A038h
A03Ch	32	MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY	0450 A03Ch
A050h	32	MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY	0450 A050h
A058h	32	MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL_PROXY	0450 A058h
A060h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY	0450 A060h
A064h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY	0450 A064h
A068h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY	0450 A068h
A06Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY	0450 A06Ch
A070h	32	MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL_PROXY	0450 A070h
A080h	32	MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL_PROXY	0450 A080h
A084h	32	MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL_PROXY	0450 A084h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
A0A0h	32	MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY	0450 A0A0h
A0A4h	32	MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY	0450 A0A4h
A0B0h	32	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY	0450 A0B0h
B008h	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	0450 B008h
B00Ch	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	0450 B00Ch
B100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0	0450 B100h
B104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1	0450 B104h
C020h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL	0450 C020h
C024h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT	0450 C024h
C028h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0	0450 C028h
C02Ch	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1	0450 C02Ch
C030h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0	0450 C030h
C034h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1	0450 C034h
C038h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT	0450 C038h
C03Ch	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR	0450 C03Ch
D008h	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK0	0450 D008h
D00Ch	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK1	0450 D00Ch
D100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	0450 D100h
E020h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY	0450 E020h
E024h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT_PROXY	0450 E024h
E028h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0_PROXY	0450 E028h
E02Ch	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1_PROXY	0450 E02Ch
E030h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0_PROXY	0450 E030h
E034h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1_PROXY	0450 E034h
E038h	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT_PROXY	0450 E038h
E03Ch	32	MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR_PROXY	0450 E03Ch
F008h	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	0450 F008h
F00Ch	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	0450 F00Ch
F100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0	0450 F100h
11008h	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK0	0451 1008h
1100Ch	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK1	0451 100Ch
11100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	0451 1100h
11104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY	0451 1104h
11108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY	0451 1108h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
1110Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY	0451 110Ch
11110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY	0451 1110h
11114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY	0451 1114h
11118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY	0451 1118h
1111Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY	0451 111Ch
11120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	0451 1120h
11124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY	0451 1124h
11128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY	0451 1128h
1112Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY	0451 112Ch
11130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY	0451 1130h
11134h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY	0451 1134h
11138h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY	0451 1138h
1113Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15_READONLY	0451 113Ch
11140h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16_READONLY	0451 1140h
11144h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17_READONLY	0451 1144h
11148h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18_READONLY	0451 1148h
1114Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19_READONLY	0451 114Ch
13008h	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY	0451 3008h
1300Ch	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY	0451 300Ch
13100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0	0451 3100h
13104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1	0451 3104h
13108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2	0451 3108h
1310Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3	0451 310Ch
13110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4	0451 3110h
13114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5	0451 3114h
13118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6	0451 3118h
1311Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7	0451 311Ch
13120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8	0451 3120h
13124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9	0451 3124h
13128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10	0451 3128h
1312Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11	0451 312Ch
13130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12	0451 3130h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
13134h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13	0451 3134h
13138h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14	0451 3138h
1313Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15	0451 313Ch
13140h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16	0451 3140h
13144h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17	0451 3144h
13148h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18	0451 3148h
1314Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19	0451 314Ch
18000h	32	MCU_CTRL_MMR_CFG0_POR_CTRL	0451 8000h
18004h	32	MCU_CTRL_MMR_CFG0_POR_STAT	0451 8004h
18100h	32	MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL	0451 8100h
18110h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL	0451 8110h
18114h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL	0451 8114h
18118h	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL	0451 8118h
1811Ch	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL	0451 811Ch
18120h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL	0451 8120h
18124h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL	0451 8124h
18138h	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL	0451 8138h
1813Ch	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL	0451 813Ch
18140h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL	0451 8140h
18144h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL	0451 8144h
18148h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL	0451 8148h
1814Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL	0451 814Ch
18150h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL	0451 8150h
18154h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL	0451 8154h
18160h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL	0451 8160h
18170h	32	MCU_CTRL_MMR_CFG0_RST_CTRL	0451 8170h
18174h	32	MCU_CTRL_MMR_CFG0_RST_STAT	0451 8174h
18178h	32	MCU_CTRL_MMR_CFG0_RST_SRC	0451 8178h
1817Ch	32	MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD	0451 817Ch
18180h	32	MCU_CTRL_MMR_CFG0_ISO_CTRL	0451 8180h
18190h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL	0451 8190h
181B0h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT	0451 81B0h
18200h	32	MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL	0451 8200h
18208h	32	MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL	0451 8208h
18280h	32	MCU_CTRL_MMR_CFG0_CLKGATE_CTRL	0451 8280h
19008h	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK0	0451 9008h
1900Ch	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK1	0451 900Ch
19100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	0451 9100h
19104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	0451 9104h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
19108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	0451 9108h
1910Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY	0451 910Ch
19110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY	0451 9110h
19114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY	0451 9114h
1A000h	32	MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY	0451 A000h
1A004h	32	MCU_CTRL_MMR_CFG0_POR_STAT_PROXY	0451 A004h
1A100h	32	MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY	0451 A100h
1A110h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY	0451 A110h
1A114h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY	0451 A114h
1A118h	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY	0451 A118h
1A11Ch	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY	0451 A11Ch
1A120h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY	0451 A120h
1A124h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY	0451 A124h
1A138h	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY	0451 A138h
1A13Ch	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY	0451 A13Ch
1A140h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY	0451 A140h
1A144h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY	0451 A144h
1A148h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY	0451 A148h
1A14Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY	0451 A14Ch
1A150h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY	0451 A150h
1A154h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY	0451 A154h
1A160h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY	0451 A160h
1A170h	32	MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY	0451 A170h
1A174h	32	MCU_CTRL_MMR_CFG0_RST_STAT_PROXY	0451 A174h
1A178h	32	MCU_CTRL_MMR_CFG0_RST_SRC_PROXY	0451 A178h
1A17Ch	32	MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY	0451 A17Ch
1A180h	32	MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY	0451 A180h
1A190h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY	0451 A190h
1A1B0h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY	0451 A1B0h

Table 14-9112. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
1A200h	32	MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY	0451 A200h
1A208h	32	MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY	0451 A208h
1A280h	32	MCU_CTRL_MMR_CFG0_CLKGATE_CTRL_PROXY	0451 A280h
1B008h	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	0451 B008h
1B00Ch	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	0451 B00Ch
1B100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0	0451 B100h
1B104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1	0451 B104h
1B108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2	0451 B108h
1B10Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3	0451 B10Ch
1B110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4	0451 B110h
1B114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5	0451 B114h

14.2.1.1.2.2 MCU_CTRL_MMR Registers

MCU_CTRL_MMR Registers

14.2.1.1.2.2.1 MCU_CTRL_MMR_CFG0_PID Register

1 MCU_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-9113. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0000h**

Figure 14-3029. MCU_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-9115. MCU_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.2 MCU_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MCU_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 8000005Fh]

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Table 14-9116. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0008h**

Figure 14-3030. MCU_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
5Fh							

Table 14-9118. MCU_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	5Fh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.3 MCU_CTRL_MMR_CFG0_IPC_SET0 Register

1 MCU_CTRL_MMR_CFG0_IPC_SET0 Register (Offset = 100h) [reset = 0h]

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Table 14-9119. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0100h**

Figure 14-3031. MCU_CTRL_MMR_CFG0_IPC_SET0 Name Register

31	30	29	28	27	26	25	24
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET0_IPC_SRC_SET							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET0_IPC_SRC_SET				RESERVED			IPC_SET0_IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-9121. MCU_CTRL_MMR_CFG0_IPC_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register Reset Source: mod_g_rst_n

14.2.1.1.2.2.4 MCU_CTRL_MMR_CFG0_IPC_CLR0 Register

1 MCU_CTRL_MMR_CFG0_IPC_CLR0 Register (Offset = 180h) [reset = 0h]

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Table 14-9122. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0180h**

Figure 14-3032. MCU_CTRL_MMR_CFG0_IPC_CLR0 Name Register

31	30	29	28	27	26	25	24
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR0_IPC_SRC_CLR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR0_IPC_SRC_CLR				RESERVED			IPC_CLR0_IPC_CLR
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-9124. MCU_CTRL_MMR_CFG0_IPC_CLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register Reset Source: mod_g_rst_n

14.2.1.1.2.2.5 MCU_CTRL_MMR_CFG0_CBA_ERR_STAT Register

1 MCU_CTRL_MMR_CFG0_CBA_ERR_STAT Register (Offset = 270h) [reset = 0h]

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Table 14-9125. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0270h**

Figure 14-3033. MCU_CTRL_MMR_CFG0_CBA_ERR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							CBA_ERR_STAT_WKUP_SAFE_CBA_ERR
NONE							R
0h							X
23	22	21	20	19	18	17	16
RESERVED			CBA_ERR_STAT_MCU_CBA_ERR	RESERVED			
NONE			R	NONE			
0h			X	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9127. MCU_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR	R	X	Access Error from Wkup Safe CBASS Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	CBA_ERR_STAT_MCU_CBA_ERR	R	X	Access Error from MCU CBASS Reset Source: mod_g_rst_n
19:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.6 MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register

1 MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register (Offset = 280h) [reset = 0h]

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Table 14-9128. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0280h**

Figure 14-3034. MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9	ACCESS_ERR_STAT_ACCESS_ERR_IN8
NONE						R	R
0h						X	X
7	6	5	4	3	2	1	0
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4	ACCESS_ERR_STAT_ACCESS_ERR_IN3	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0
NONE			R	R	NONE		R
0h			X	X	0h		X

Table 14-9130. MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9	R	X	Access Error Detected in MCU PadCfg MMR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8	R	X	Access Error Detected in MCU Ctrl MMR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4	R	X	Access Error Detected in MAIN PadCfg MMR Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3	R	X	Access Error Detected in MAIN Ctrl MMR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0	R	X	Access Error Detected in WKUP Ctrl MMR Reset Source: mod_por_rst_n

14.2.1.1.2.2.7 MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-9131. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1008h**

Figure 14-3035. MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-9133. MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.8 MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-9134. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 100Ch**

Figure 14-3036. MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-9136. MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.9 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-9137. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1010h**

Figure 14-3037. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9139. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.10 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-9140. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1014h**

Figure 14-3038. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9142. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.11 MCU_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-9143. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1018h**

Figure 14-3039. MCU_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9145. MCU_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.12 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-9146. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 101Ch**

Figure 14-3040. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9148. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.13 MCU_CTRL_MMR_CFG0_EOI Register

1 MCU_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-9149. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1020h**

Figure 14-3041. MCU_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-9151. MCU_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.14 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-9152. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1024h**

Figure 14-3042. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-9154. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.15 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-9155. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1028h**

Figure 14-3043. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-9157. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.16 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-9158. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 102Ch**

Figure 14-3044. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9160. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.17 MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-9161. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1030h**

Figure 14-3045. MCU_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-9163. MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.18 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9164. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1100h**

Figure 14-3046. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-9166. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.19 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register (Offset = 1104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9167. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1104h**

Figure 14-3047. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P0_R1_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P0_R1_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P0_R1_READONLY							
R							
0h							

Table 14-9169. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.20 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9170. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1108h**

Figure 14-3048. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2_READONLY							
R							
0h							

Table 14-9172. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.21 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-9173. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 110Ch**

Figure 14-3049. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9175. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.22 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9176. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1110h**

Figure 14-3050. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P0_R4_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P0_R4_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P0_R4_READONLY							
R							
0h							

Table 14-9178. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.23 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9179. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1114h**

Figure 14-3051. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-9181. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.24 MCU_CTRL_MMR_CFG0_PID_PROXY Register

1 MCU_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-9182. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2000h**

Figure 14-3052. MCU_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		15h					

Table 14-9184. MCU_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.25 MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 8000005Fh]

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Table 14-9185. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2008h**

Figure 14-3053. MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
5Fh							

Table 14-9187. MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	5Fh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.26 MCU_CTRL_MMR_CFG0_IPC_SET0_PROXY Register

1 MCU_CTRL_MMR_CFG0_IPC_SET0_PROXY Register (Offset = 2100h) [reset = 0h]

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Table 14-9188. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2100h**

Figure 14-3054. MCU_CTRL_MMR_CFG0_IPC_SET0_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SET0_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SET0_IPC_SRC_SET_PROXY				RESERVED			IPC_SET0_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-9190. MCU_CTRL_MMR_CFG0_IPC_SET0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register Reset Source: mod_g_rst_n

14.2.1.1.2.2.27 MCU_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register

1 MCU_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register (Offset = 2180h) [reset = 0h]

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Table 14-9191. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2180h**

Figure 14-3055. MCU_CTRL_MMR_CFG0_IPC_CLR0_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_CLR0_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_CLR0_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_CLR0_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_CLR0_IPC_SRC_CLR_PROXY				RESERVED			IPC_CLR0_IPC_CLR_PROXY
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-9193. MCU_CTRL_MMR_CFG0_IPC_CLR0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register Reset Source: mod_g_rst_n

14.2.1.1.2.2.28 MCU_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register (Offset = 2270h) [reset = 0h]

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Table 14-9194. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2270h**

Figure 14-3056. MCU_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>CBA_ERR_STAT_MCU_CBA_ERR_PROXY</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>X</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9196. MCU_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY	R	X	Access Error from Wkup Safe CBASS Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	CBA_ERR_STAT_MCU_CBA_ERR_PROXY	R	X	Access Error from MCU CBASS Reset Source: mod_g_rst_n
19:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.29 MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register (Offset = 2280h) [reset = 0h]

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Table 14-9197. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2280h**

Figure 14-3057. MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY
NONE						R	R
0h						X	X
7	6	5	4	3	2	1	0
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY
NONE			R	R	NONE		R
0h			X	X	0h		X

Table 14-9199. MCU_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	R	X	Access Error Detected in MCU PadCfg MMR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY	R	X	Access Error Detected in MCU Ctrl MMR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	R	X	Access Error Detected in MAIN PadCfg MMR Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	R	X	Access Error Detected in MAIN Ctrl MMR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY	R	X	Access Error Detected in WKUP Ctrl MMR Reset Source: mod_por_rst_n

14.2.1.1.2.2.30 MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-9200. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3008h**

Figure 14-3058. MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-9202. MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.31 MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-9203. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 300Ch**

Figure 14-3059. MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-9205. MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.32 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-9206. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3010h**

Figure 14-3060. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9208. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.33 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-9209. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3014h**

Figure 14-3061. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9211. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.34 MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-9212. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3018h**

Figure 14-3062. MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9214. MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.35 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-9215. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 301Ch**

Figure 14-3063. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9217. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.36 MCU_CTRL_MMR_CFG0_EOI_PROXY Register

1 MCU_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-9218. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3020h**

Figure 14-3064. MCU_CTRL_MMR_CFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-9220. MCU_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.37 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-9221. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3024h**

Figure 14-3065. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-9223. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.38 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-9224. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3028h**

Figure 14-3066. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-9226. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.39 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-9227. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 302Ch**

Figure 14-3067. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID_PROXY</td><td colspan="4">FAULT_ROUTEID_PROXY</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9229. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.40 MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-9230. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3030h**

Figure 14-3068. MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-9232. MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.41 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9233. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3100h**

Figure 14-3069. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-9235. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.42 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9236. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3104h**

Figure 14-3070. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-9238. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.43 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9239. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3108h**

Figure 14-3071. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9241. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.44 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-9242. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 310Ch**

Figure 14-3072. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-9244. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.45 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9245. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3110h**

Figure 14-3073. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4							
R/W							
0h							

Table 14-9247. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.46 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-9248. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3114h**

Figure 14-3074. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-9250. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.47 MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL Register (Offset = 4020h) [reset = 0h]

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Table 14-9251. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4020h**

Figure 14-3075. MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_GPIO_CTRL_WAKEN
NONE							R/W
0h							0h

Table 14-9253. MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_GPIO_CTRL_WAKEN	R/W	0h	Activates MCU_GPIO wakeup event operation by controling the MCU_GPIO LPSC clockstop_ack behavior. Field values (Others are reserved): 1'b0 - No MCU_GPIO wakeup support. MCU_GPIO vbus clock is gated on clkstop_ack from MCU_GPIO to LPSC 1'b1 - MCU_GPIO wakeup activated. MCU_GPIO vbus clock is NOT gated on LPSC clockstop_req. MCU_GPIO LPSC clkstop_ack input is driven by clkstop_req output. Reset Source: mod_por_rst_n

14.2.1.1.2.2.48 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register (Offset = 4084h) [reset = 0h]

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Table 14-9254. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4084h**

Figure 14-3076. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG1_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9256. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG1_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel1 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.49 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register (Offset = 4088h) [reset = 0h]

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Table 14-9257. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4088h**

Figure 14-3077. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG2_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9259. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG2_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel2 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.50 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register (Offset = 408Ch) [reset = 0h]

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Table 14-9260. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 408Ch**

Figure 14-3078. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG3_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9262. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG3_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel3 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.51 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register (Offset = 4090h) [reset = 0h]

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Table 14-9263. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4090h**

Figure 14-3079. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DBOUNCE_CFG4_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9265. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG4_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel4 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.52 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register (Offset = 4094h) [reset = 0h]

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Table 14-9266. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4094h**

Figure 14-3080. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG5_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9268. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG5_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel5 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.53 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register (Offset = 4098h) [reset = 0h]

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Table 14-9269. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4098h**

Figure 14-3081. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-9271. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG6_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel6 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.54 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register

1 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register (Offset = 40A0h) [reset = 0h]

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Table 14-9272. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 40A0h**

Figure 14-3082. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TEMP_DIODE_TRIM_TRIM					
NONE		R					
0h		X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEMP_DIODE_TRIM_TRIM							
R							
X							

Table 14-9274. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TEMP_DIODE_TRIM_TRIM	R	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down Reset Source: mod_por_rst_n

14.2.1.1.2.2.55 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register

1 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register (Offset = 40B0h) [reset = 0h]

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Table 14-9275. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 40B0h**

Figure 14-3083. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						IO_VOLTAGE_STAT_GPMC	IO_VOLTAGE_STAT_GEMAC
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				IO_VOLTAGE_STAT_MMC2	IO_VOLTAGE_STAT_MMC1	IO_VOLTAGE_STAT_MMC0	IO_VOLTAGE_STAT_GENERAL
NONE				R	R	R	R
0h				X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					IO_VOLTAGE_STAT_CANUART	IO_VOLTAGE_STAT_FLASH	IO_VOLTAGE_STAT_WKUP_MCU
NONE					R	R	R
0h					X	X	X

Table 14-9277. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	IO_VOLTAGE_STAT_GPMC	R	X	Indicates the voltage for the GPMC I/O group (VDDSHV3) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
16	IO_VOLTAGE_STAT_GEMAC	R	X	Indicates the voltage for the GEMAC I/O group (VDDSHV2) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	IO_VOLTAGE_STAT_MMC2	R	X	Indicates the voltage for the MMC2 I/O group (VDDSHV6) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n

Table 14-9277. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	IO_VOLTAGE_STAT_MMC1	R	X	Indicates the voltage for the MMC1 I/O group (VDDSHV5) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
9	IO_VOLTAGE_STAT_MMC0	R	X	Indicates the voltage for the MMC0 I/O group (VDDSHV4) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
8	IO_VOLTAGE_STAT_GENERAL	R	X	Indicates the voltage for the General I/O group (VDDSHV0) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2	IO_VOLTAGE_STAT_CANUART	R	X	Indicates the voltage for the CANUART I/O group (VDDSHV_WKUP) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
1	IO_VOLTAGE_STAT_FLASH	R	X	Indicates the voltage for the Flash I/O group (VDDSHV1) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
0	IO_VOLTAGE_STAT_WKUP_MCU	R	X	Indicates the voltage for the WKUP_MCU I/O group (VDDSHV_MCU) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n

14.2.1.1.2.2.56 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

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Table 14-9278. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4204h**

Figure 14-3084. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MCU_TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9280. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER1_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.57 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

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Table 14-9281. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 420Ch

Figure 14-3085. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MCU_TIMER3_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9283. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER3_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.58 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

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Table 14-9284. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 42E0h**

Figure 14-3086. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_I2C0_CTRL_HS_MCS_EN
NONE							R/W
0h							0h

Table 14-9286. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_I2C0_CTRL_HS_MCS_EN	R/W	0h	HS Mode controller current source activate. When set, activates the current-source pull-up on the SCL output. Only one controller on the I2C bus should activate SCL current sourcing. Reset Source: mod_g_rst_n

14.2.1.1.2.2.59 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0 Register

1 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0 Register (Offset = 4604h) [reset = 0h]

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Table 14-9287. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4604h**

Figure 14-3087. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0 Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL0_IDLE_STAT	RESERVED						
R	NONE						
X	0h						

23	22	21	20	19	18	17	16
WKUP_MTOG_CTRL0_FORCE_TIMEOUT							
R/W							
0h							

15	14	13	12	11	10	9	8
WKUP_MTOG_CTRL0_TIMEOUT_EN	RESERVED						
R/W	NONE						
0h	0h						

7	6	5	4	3	2	1	0
RESERVED					WKUP_MTOG_CTRL0_TIMEOUT_VAL		
NONE					R/W		
0h					0h		

Table 14-9289. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL0_IDLE_STAT	R	X	Idle Status Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL0_FORCE_TIMEOUT	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. 8'h95 - Force a gasket timeout All others - Normal operation Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL0_TIMEOUT_EN	R/W	0h	Timeout Activate 1'b0 - Deactivate the gasket. Clear the interrupt and reset the counter 1'b1 - Activate the timeout gasket functions Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-9289. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL0_TIMEOUT_VAL	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Reset Source: mod_g_rst_n

14.2.1.1.2.2.60 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1 Register

1 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1 Register (Offset = 4608h) [reset = 0h]

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Table 14-9290. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4608h**

Figure 14-3088. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1 Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL1_IDLE_STAT	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WKUP_MTOG_CTRL1_FORCE_TIMEOUT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WKUP_MTOG_CTRL1_TIMEOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WKUP_MTOG_CTRL1_TIMEOUT_VAL		
NONE					R/W		
0h					0h		

Table 14-9292. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL1_IDLE_STAT	R	X	Idle Status Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL1_FORCE_TIMEOUT	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. 8'h95 - Force a gasket timeout All others - Normal operation Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL1_TIMEOUT_EN	R/W	0h	Timeout Activate 1'b0 - Deactivate the gasket. Clear the interrupt and reset the counter 1'b1 - Activate the timeout gasket functions Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-9292. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL1_TIMEOUT_VAL	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Reset Source: mod_g_rst_n

14.2.1.1.2.2.61 MCU_CTRL_MMR_CFG0_TOG_STAT Register

1 MCU_CTRL_MMR_CFG0_TOG_STAT Register (Offset = 4610h) [reset = 0h]

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Table 14-9293. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4610h**

Figure 14-3089. MCU_CTRL_MMR_CFG0_TOG_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>TOG_STAT_SLV_TOG_STAT</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>X</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TOG_STAT_MST_TOG_STAT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">X</td></tr>
</table>

Table 14-9295. MCU_CTRL_MMR_CFG0_TOG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TOG_STAT_SLV_TOG_STAT	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 1'b0 - No Error 1'b1 - Error from mcu2dm timeout gasket MCU_TIMEOUT0 Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 2'b00 - No Error 2'b01 - Error from dm2mcu WKUP_TIMEOUT1 gasket 2'b10 - Error from dm2ws WKUP_TIMEOUT0 gasket 2'b11 - Error from both dm2mcu and dm2ws WKUP_TIMEOUT1 and WKUP_TIMEOUT0 gaskets Reset Source: mod_g_rst_n

14.2.1.1.2.2.62 MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-9296. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5008h**

Figure 14-3090. MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-9298. MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.63 MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-9299. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 500Ch**

Figure 14-3091. MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-9301. MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.64 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9302. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5100h**

Figure 14-3092. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-9304. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.65 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9305. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5104h**

Figure 14-3093. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-9307. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.66 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9308. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5108h**

Figure 14-3094. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-9310. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.67 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9311. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 510Ch**

Figure 14-3095. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9313. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.68 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9314. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5110h**

Figure 14-3096. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-9316. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.69 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9317. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5114h**

Figure 14-3097. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-9319. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.70 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9320. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5118h**

Figure 14-3098. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-9322. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.71 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register (Offset = 511Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9323. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 511Ch**

Figure 14-3099. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7_READONLY							
R							
0h							

Table 14-9325. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.72 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9326. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5120h**

Figure 14-3100. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-9328. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.73 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9329. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5124h**

Figure 14-3101. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-9331. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.74 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register (Offset = 5128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9332. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5128h**

Figure 14-3102. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10_READONLY							
R							
0h							

Table 14-9334. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.75 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register (Offset = 512Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9335. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 512Ch**

Figure 14-3103. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11_READONLY							
R							
0h							

Table 14-9337. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.76 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9338. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5130h**

Figure 14-3104. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12_READONLY							
R							
0h							

Table 14-9340. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.77 MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL_PROXY Register (Offset = 6020h) [reset = 0h]

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Table 14-9341. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6020h**

Figure 14-3105. MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_GPIO_CTRL_WAKEN_PROXY
NONE							R/W
0h							0h

Table 14-9343. MCU_CTRL_MMR_CFG0_MCU_GPIO_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_GPIO_CTRL_WAKEN_PROXY	R/W	0h	Activates MCU_GPIO wakeup event operation by controling the MCU_GPIO LPSC clockstop_ack behavior. Field values (Others are reserved): 1'b0 - No MCU_GPIO wakeup support. MCU_GPIO vbus clock is gated on clkstop_ack from MCU_GPIO to LPSC 1'b1 - MCU_GPIO wakeup activated. MCU_GPIO vbus clock is NOT gated on LPSC clockstop_req. MCU_GPIO LPSC clkstop_ack input is driven by clkstop_req output. Reset Source: mod_por_rst_n

14.2.1.1.2.2.78 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register (Offset = 6084h) [reset = 0h]

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Table 14-9344. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6084h**

Figure 14-3106. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG1_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-9346. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG1_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel1 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.79 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register (Offset = 6088h) [reset = 0h]

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Table 14-9347. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6088h**

Figure 14-3107. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG2_DB_CFG_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-9349. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG2_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel2 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.80 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register (Offset = 608Ch) [reset = 0h]

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Table 14-9350. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 608Ch**

Figure 14-3108. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG3_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-9352. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG3_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel3 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.81 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register (Offset = 6090h) [reset = 0h]

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Table 14-9353. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6090h**

Figure 14-3109. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG4_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-9355. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG4_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel4 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.82 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register (Offset = 6094h) [reset = 0h]

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Table 14-9356. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6094h**

Figure 14-3110. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG5_DB_CFG_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-9358. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG5_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel5 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.83 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register (Offset = 6098h) [reset = 0h]

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Table 14-9359. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6098h**

Figure 14-3111. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-9361. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG6_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel6 activated. Reset Source: mod_por_rst_n

14.2.1.1.2.2.84 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register (Offset = 60A0h) [reset = 0h]

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Table 14-9362. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 60A0h**

Figure 14-3112. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TEMP_DIODE_TRIM_TRIM_PROXY					
NONE		R					
0h		X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEMP_DIODE_TRIM_TRIM_PROXY							
R							
X							

Table 14-9364. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TEMP_DIODE_TRIM_TRIM_PROXY	R	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down Reset Source: mod_por_rst_n

14.2.1.1.2.2.85 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register (Offset = 60B0h) [reset = 0h]

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Table 14-9365. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 60B0h**

Figure 14-3113. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						IO_VOLTAGE_STAT_GPMC_PROXY	IO_VOLTAGE_STAT_GEMAC_PROXY
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				IO_VOLTAGE_STAT_MMC2_PROXY	IO_VOLTAGE_STAT_MMC1_PROXY	IO_VOLTAGE_STAT_MMC0_PROXY	IO_VOLTAGE_STAT_GENERAL_PROXY
NONE				R	R	R	R
0h				X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					IO_VOLTAGE_STAT_CANUART_PROXY	IO_VOLTAGE_STAT_FLASH_PROXY	IO_VOLTAGE_STAT_WKUP_MCU_PROXY
NONE					R	R	R
0h					X	X	X

Table 14-9367. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	IO_VOLTAGE_STAT_GPMC_PROXY	R	X	Indicates the voltage for the GPMC I/O group (VDDSHV3) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
16	IO_VOLTAGE_STAT_GEMAC_PROXY	R	X	Indicates the voltage for the GEMAC I/O group (VDDSHV2) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	IO_VOLTAGE_STAT_MMC2_PROXY	R	X	Indicates the voltage for the MMC2 I/O group (VDDSHV6) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n

Table 14-9367. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	IO_VOLTAGE_STAT_MMC1_PROXY	R	X	Indicates the voltage for the MMC1 I/O group (VDDSHV5) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
9	IO_VOLTAGE_STAT_MMC0_PROXY	R	X	Indicates the voltage for the MMC0 I/O group (VDDSHV4) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
8	IO_VOLTAGE_STAT_GENERAL_PROXY	R	X	Indicates the voltage for the General I/O group (VDDSHV0) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2	IO_VOLTAGE_STAT_CANUART_PROXY	R	X	Indicates the voltage for the CANUART I/O group (VDDSHV_WKUP) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
1	IO_VOLTAGE_STAT_FLASH_PROXY	R	X	Indicates the voltage for the Flash I/O group (VDDSHV1) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n
0	IO_VOLTAGE_STAT_WKUP_MCU_PROXY	R	X	Indicates the voltage for the WKUP_MCU I/O group (VDDSHV_MCU) Field values (others are reserved): 1'b0 - I/O group is set for 3.3V 1'b1 - I/O group is set for 1.8V Reset Source: mod_por_rst_n

14.2.1.1.2.2.86 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

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Table 14-9368. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6204h**

Figure 14-3114. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MCU_TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9370. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.87 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register (Offset = 620Ch) [reset = 0h]

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Table 14-9371. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 620Ch**

Figure 14-3115. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MCU_TIMER3_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9373. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER3_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.88 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register (Offset = 62E0h) [reset = 0h]

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Table 14-9374. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 62E0h**

Figure 14-3116. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_I2C0_CTRL_HS_MCS_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9376. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_I2C0_CTRL_HS_MCS_EN_PROXY	R/W	0h	HS Mode controller current source activate. When set, activates the current-source pull-up on the SCL output. Only one controller on the I2C bus should activate SCL current sourcing. Reset Source: mod_g_rst_n

14.2.1.1.2.2.89 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY Register

1 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY Register (Offset = 6604h) [reset = 0h]

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Table 14-9377. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6604h**

Figure 14-3117. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL0_IDLE_STAT_PROXY	RESERVED						
R	NONE						
X	0h						

23	22	21	20	19	18	17	16
WKUP_MTOG_CTRL0_FORCE_TIMEOUT_PROXY							
R/W							
0h							

15	14	13	12	11	10	9	8
WKUP_MTOG_CTRL0_TIMEOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						

7	6	5	4	3	2	1	0
RESERVED					WKUP_MTOG_CTRL0_TIMEOUT_VAL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9379. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL0_IDLE_STAT_PROXY	R	X	Idle Status Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL0_FORCE_TIMEOUT_PROXY	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. 8'h95 - Force a gasket timeout All others - Normal operation Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL0_TIMEOUT_EN_PROXY	R/W	0h	Timeout Activate 1'b0 - Deactivate the gasket. Clear the interrupt and reset the counter 1'b1 - Activate the timeout gasket functions Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-9379. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL0_TIMEOUT_VAL_PROXY	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Reset Source: mod_g_rst_n

14.2.1.1.2.2.90 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY Register

1 MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY Register (Offset = 6608h) [reset = 0h]

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Table 14-9380. Instance Table

Instance Name	**Physical Address**
MCU_CTRL_MMR0	**0450 6608h**

Figure 14-3118. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL1_IDLE_STAT_PROXY	RESERVED						
R	NONE						
X	0h						
23	22	21	20	19	18	17	16
WKUP_MTOG_CTRL1_FORCE_TIMEOUT_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
WKUP_MTOG_CTRL1_TIMEOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED					WKUP_MTOG_CTRL1_TIMEOUT_VAL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9382. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL1_IDLE_STAT_PROXY	R	X	Idle Status Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL1_FORCE_TIMEOUT_PROXY	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. 8'h95 - Force a gasket timeout All others - Normal operation Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL1_TIMEOUT_EN_PROXY	R/W	0h	Timeout Activate 1'b0 - Deactivate the gasket. Clear the interrupt and reset the counter 1'b1 - Activate the timeout gasket functions Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-9382. MCU_CTRL_MMR_CFG0_WKUP_MTOG_CTRL1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL1_TIMEOUT_VAL_PROXY	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Reset Source: mod_g_rst_n

14.2.1.1.2.2.91 MCU_CTRL_MMR_CFG0_TOG_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_TOG_STAT_PROXY Register (Offset = 6610h) [reset = 0h]

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Table 14-9383. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6610h**

Figure 14-3119. MCU_CTRL_MMR_CFG0_TOG_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TOG_STAT_SLV_TOG_STAT_PROXY	RESERVED						
R	NONE						
X	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TOG_STAT_MST_TOG_STAT_PROXY	
NONE						R	
0h						X	

Table 14-9385. MCU_CTRL_MMR_CFG0_TOG_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TOG_STAT_SLV_TOG_STAT_PROXY	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 1'b0 - No Error 1'b1 - Error from mcu2dm timeout gasket MCU_TIMEOUT0 Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT_PROXY	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 2'b00 - No Error 2'b01 - Error from dm2mcu WKUP_TIMEOUT1 gasket 2'b10 - Error from dm2ws WKUP_TIMEOUT0 gasket 2'b11 - Error from both dm2mcu and dm2ws WKUP_TIMEOUT1 and WKUP_TIMEOUT0 gaskets Reset Source: mod_g_rst_n

14.2.1.1.2.2.92 MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-9386. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7008h**

Figure 14-3120. MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-9388. MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.93 MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-9389. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 700Ch**

Figure 14-3121. MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-9391. MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.94 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9392. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7100h**

Figure 14-3122. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-9394. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.95 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9395. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7104h**

Figure 14-3123. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-9397. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.96 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9398. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7108h**

Figure 14-3124. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-9400. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.97 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9401. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 710Ch**

Figure 14-3125. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-9403. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.98 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9404. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7110h**

Figure 14-3126. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-9406. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.99 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9407. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7114h**

Figure 14-3127. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-9409. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.100 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9410. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7118h**

Figure 14-3128. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-9412. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.101 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9413. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 711Ch**

Figure 14-3129. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-9415. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.102 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9416. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7120h**

Figure 14-3130. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-9418. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.103 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9419. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7124h**

Figure 14-3131. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-9421. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.104 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9422. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7128h**

Figure 14-3132. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-9424. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.105 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-9425. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 712Ch**

Figure 14-3133. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-9427. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.106 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-9428. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7130h**

Figure 14-3134. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-9430. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.107 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register (Offset = 8000h) [reset = 0h]

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Table 14-9431. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8000h**

Figure 14-3135. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCU_OBSCLK_CTRL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-9433. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL	R/W	0h	MCU_OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 4'b0001. 1'b0 - The output of the MCU_OBSCLK output divider is output on the pin 1'b1 - HFOSC0_CLK is output on the pin Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved

Table 14-9433. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	MCU_OBSCLK_CTRL_CLK_DIV	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by clk_div+1 Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	MCU_OBSCLK_CTRL_CLK_SEL	R/W	0h	MCU_OBSCLK pin clock selection Field values (others are reserved): 4'b0000 - CLK_12M_RC 4'b0001 - '0' 4'b0010 - MCU_PLL0_HSDIV0_CLKOUT 4'b0011 - MCU_PLL0_HSDIV4_CLKOUT 4'b0100 - MCU_PLLCTRL_OBSCLK 4'b0101 - CLK_32K_RC 4'b0110 - HFOSC0_CLKOUT 4'b0111 - HFOSC0_CLKOUT_32K 4'b1000 - MCU_SYSCLK0 4'b1001 - DEVICE_CLKOUT_32K Reset Source: mod_por_rst_n

14.2.1.1.2.2.108 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register (Offset = 8010h) [reset = 0h]

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Table 14-9434. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8010h**

Figure 14-3136. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>HFOSC0_CTRL_PD_C</td><td colspan="2">RESERVED</td><td>HFOSC0_CTRL_BP_C</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9436. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC0_CTRL_PD_C	R/W	0h	Oscillator powerdown control. When set, oscillator is deactivated. Oscillator output is tristated if bp_c=0 Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C	R/W	0h	Reserved - Must Write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.109 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register (Offset = 8018h) [reset = 131022h]

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Table 14-9437. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8018h**

Figure 14-3137. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>HFOSC0_TRIM_TRIM_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">HFOSC0_TRIM_HYST</td><td>RESERVED</td><td colspan="3">HFOSC0_TRIM_I_MULT</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">1h</td><td>0h</td><td colspan="3">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">HFOSC0_TRIM_R_REF</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">HFOSC0_TRIM_I_IBIAS_COMP</td><td colspan="4">HFOSC0_TRIM_R_IBIAS_REF</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">2h</td><td colspan="4">2h</td></tr>
</table>

Table 14-9439. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_TRIM_TRIM_EN	R/W	0h	Apply MMR values to OSC trim inputs instead of tie-offs Reset Source: mod_por_rst_n
30:22	RESERVED	NONE	0h	Reserved
21:20	HFOSC0_TRIM_HYST	R/W	1h	Sets comparator hysterisis Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HFOSC0_TRIM_I_MULT	R/W	3h	AGC AMP current multiplication gain Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	HFOSC0_TRIM_R_REF	R/W	10h	Sets the AMP AGC bias current Reset Source: mod_por_rst_n
7:4	HFOSC0_TRIM_I_IBIAS_COMP	R/W	2h	Sets the COMP bias current Reset Source: mod_por_rst_n
3:0	HFOSC0_TRIM_R_IBIAS_REF	R/W	2h	Sets the base IBIAS reference Reset Source: mod_por_rst_n

14.2.1.1.2.2.110 MCU_CTRL_MMR_CFG0_HFOSC0_STAT Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_STAT Register (Offset = 8020h) [reset = 0h]

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Table 14-9440. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8020h**

Figure 14-3138. MCU_CTRL_MMR_CFG0_HFOSC0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							HFOSC0_STAT_DS_ON_WFI_STAT
NONE							R
0h							X

Table 14-9442. MCU_CTRL_MMR_CFG0_HFOSC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	HFOSC0_STAT_DS_ON_WFI_STAT	R	X	Allows MCU to monitor the DM attempting a Deep Sleep Reset Source: mod_g_rst_n

14.2.1.1.2.2.111 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register

1 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register (Offset = 8024h) [reset = 0h]

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Table 14-9443. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8024h**

Figure 14-3139. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR	RC12M_OSC_TRIM_TRIMOSC_COARSE			RC12M_OSC_TRIM_TRIMOSC_FINE		
NONE	R/W	R/W			R/W		
0h	X	X			X		

Table 14-9445. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR	R/W	X	Coarse adjustment direction. If output is greater than 12.5 0 - Coarse adjustment decreases frequency 1 - Coarse adjustment increases frequency Reset Source: mod_por_rst_n
5:3	RC12M_OSC_TRIM_TRIMOSC_COARSE	R/W	X	Coarse adjustment. Frequency is decreased or increased by 1.25 MHz per value based on the trimosc_coarse_dir value. Reset Source: mod_por_rst_n
2:0	RC12M_OSC_TRIM_TRIMOSC_FINE	R/W	X	Fine adjustment. Decreases the frequency by 250 KHz per value. Reset Source: mod_por_rst_n

14.2.1.1.2.2.112 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register (Offset = 8030h) [reset = 8065h]

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Table 14-9446. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8030h**

Figure 14-3140. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV						
NONE	R/W						
0h	65h						

Table 14-9448. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET	R/W	0h	Asynchronous Divider Reset 1 = Divider is Reset, HFOSC0_CLKOUT32K reset. 0 = Divider out of reset, HFOSC0_CLKOUT_32K running. Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	R/W	1h	HFOSC0_CLKOUT_32K activate: 0 = Synchronously Deactivate HFOSC0_CLKOUT_32KHz 1 = Synchronously Activate HFOSC0_CKLKOUT_32KHz Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Deactivate 0 = Divider Updates are shadowed and take effect on counter reset. 1 = Divider Updates are immediate and hazardous Do not set this bit to 1'b1 during normal use. Reset Source: sys_por_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-9448. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV	R/W	65h	HFOSC0_CLKOUT_32K divider: HFOSC0_CLKKOUT_32K Frequency = HFOSC0 Frequency / [8 * (hsdiv + 1)] Ex. HFOSC0 Frequency = 26MHz. hsdiv = 101 (Default) HFOSC0_CLKOUT_32K = 26MHz / (8 * (101+1)) = 26MHz / 816 = 31.9 KHz Reset Source: sys_por_rst_n

14.2.1.1.2.2.113 MCU_CTRL_MMR_CFG0_LFXOSC_CTRL Register

1 MCU_CTRL_MMR_CFG0_LFXOSC_CTRL Register (Offset = 8038h) [reset = 80h]

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Table 14-9449. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8038h**

Figure 14-3141. MCU_CTRL_MMR_CFG0_LFXOSC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFXOSC_CTRL_PD_C	RESERVED		LFXOSC_CTRL_BP_C	RESERVED			
R/W	NONE		R/W	NONE			
1h	0h		0h	0h			

Table 14-9451. MCU_CTRL_MMR_CFG0_LFXOSC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LFXOSC_CTRL_PD_C	R/W	1h	Oscillator powerdown control. When set, oscillator is deactivated. Oscillator output is tristated if bp_c=0 Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	LFXOSC_CTRL_BP_C	R/W	0h	Oscillator bypass control. When set, oscillator is in bypass mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.114 MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Register

1 MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Register (Offset = 803Ch) [reset = 121203h]

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Table 14-9452. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 803Ch**

Figure 14-3142. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		LFXOSC_TRIM_HYST		RESERVED	LFXOSC_TRIM_I_MULT		
NONE		R/W		NONE	R/W		
0h		1h		0h	2h		
15	14	13	12	11	10	9	8
RESERVED		LFXOSC_TRIM_R_REF					
NONE		R/W					
0h		12h					
7	6	5	4	3	2	1	0
LFXOSC_TRIM_I_IBIAS_COMP				LFXOSC_TRIM_R_IBIAS_REF			
R/W				R/W			
0h				3h			

Table 14-9454. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	LFXOSC_TRIM_HYST	R/W	1h	Sets comparator hysterisis Field values (others are reserved): 2'b00 - Hysteresis deactivated 2'b01 - Type 1 hysteresis activated (Default) 2'b10 - Type 2 hysteresis activated 2'b11 - Both types 1 & 2 hysteresis activated Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LFXOSC_TRIM_I_MULT	R/W	2h	AGC AMP current multiplication gain Field values (others are reserved): 3'b000 - 3x AMP_AGC IBIAS 3'b001 - 4x AMP_AGC IBIAS 3'b010 - 5x AMP_AGC IBIAS (Default) 3'b011 - 6x AMP_AGC IBIAS 3'b100 - 7x AMP_AGC IBIAS 3'b101 - 8x AMP_AGC IBIAS 3'b110 - 9x AMP_AGC IBIAS 3'b111 - 10x AMP_AGC IBIAS Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-9454. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	LFXOSC_TRIM_R_REF	R/W	12h	Sets the AMP AGC bias current Field values (others are reserved): 6'b000000 - 0 K Ohm 6'b000001 - 24 K Ohm 6'b000010 - 48 K Ohm 6'b000011 - 73 K Ohm 6'b000100 - 97 K Ohm 6'b000101 - 121 K Ohm 6'b000110 - 145 K Ohm 6'b000111 - 169 K Ohm 6'b001000 - 193 K Ohm 6'b001001 - 218 K Ohm 6'b001010 - 242 K Ohm 6'b001011 - 266 K Ohm 6'b001100 - 290 K Ohm 6'b001101 - 314 K Ohm 6'b001110 - 338 K Ohm 6'b001111 - 363 K Ohm 6'b010000 - 387 K Ohm 6'b010001 - 411 K Ohm 6'b010010 - 435 K Ohm (Default) 6'b010011 - 459 K Ohm 6'b010100 - 483 K Ohm 6'b010101 - 508 K Ohm 6'b010110 - 532 K Ohm 6'b010111 - 556 K Ohm 6'b011000 - 580 K Ohm 6'b011001 - 604 K Ohm 6'b011010 - 628 K Ohm 6'b011011 - 653 K Ohm 6'b011100 - 677 K Ohm 6'b011101 - 701 K Ohm 6'b011110 - 725 K Ohm 6'b011111 - 749 K Ohm 6'b100000 - 773 K Ohm 6'b100001 - 798 K Ohm 6'b100010 - 822 K Ohm 6'b100011 - 846 K Ohm 6'b100100 - 870 K Ohm 6'b100101 - 894 K Ohm 6'b100110 - 918 K Ohm 6'b100111 - 943 K Ohm 6'b101000 - 967 K Ohm 6'b101001 - 991 K Ohm 6'b101010 - 1015 K Ohm 6'b101011 - 1039 K Ohm 6'b101100 - 1063 K Ohm 6'b101101 - 1088 K Ohm 6'b101110 - 1112 K Ohm 6'b101111 - 1136 K Ohm 6'b110000 - 1160 K Ohm 6'b110001 - 1184 K Ohm 6'b110010 - 1208 K Ohm 6'b110011 - 1233 K Ohm 6'b110100 - 1257 K Ohm 6'b110101 - 1281 K Ohm 6'b110110 - 1305 K Ohm 6'b110111 - 1329 K Ohm 6'b111000 - 1353 K Ohm 6'b111001 - 1378 K Ohm 6'b111010 - 1402 K Ohm 6'b111011 - 1426 K Ohm 6'b111100 - 1450 K Ohm 6'b111101 - 1474 K Ohm 6'b111110 - 1498 K Ohm

Table 14-9454. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111111 - 1523 K Ohm Reset Source: mod_por_rst_n
7:4	LFXOSC_TRIM_I_IBIAS_COMP	R/W	0h	Sets the COMP bias current Field values (others are reserved): 4'b0000 - Base IBIAS ref x2 4'b0001 - Base IBIAS ref x3 4'b0010 - Base IBIAS ref x4 4'b0011 - Base IBIAS ref x5 4'b0100 - Base IBIAS ref x6 4'b0101 - Base IBIAS ref x7 4'b0110 - Base IBIAS ref x8 4'b0111 - Base IBIAS ref x9 4'b1000 - Base IBIAS ref x10 4'b1001 - Base IBIAS ref x11 4'b1010 - Base IBIAS ref x12 4'b1011 - Base IBIAS ref x13 4'b1100 - Base IBIAS ref x14 4'b1101 - Base IBIAS ref x15 4'b1110 - Base IBIAS ref x16 4'b1111 - Base IBIAS ref x17 Reset Source: mod_por_rst_n
3:0	LFXOSC_TRIM_R_IBIAS_REF	R/W	3h	Sets the base IBIAS reference Field values (others are reserved): 4'b0000 - 512 K Ohm 4'b0001 - 576 K Ohm 4'b0010 - 640 K Ohm 4'b0011 - 704 K Ohm (Default) 4'b0100 - 768 K Ohm 4'b0101 - 832 K Ohm 4'b0110 - 896 K Ohm 4'b0111 - 960 K Ohm 4'b1000 - 1024 K Ohm 4'b1001 - 1088 K Ohm 4'b1010 - 1152 K Ohm 4'b1011 - 1216 K Ohm 4'b1100 - 1280 K Ohm 4'b1101 - 1344 K Ohm 4'b1110 - 1408 K Ohm 4'b1111 - 1472 K Ohm Reset Source: mod_por_rst_n

14.2.1.1.2.2.115 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register (Offset = 8050h) [reset = 800000h]

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Table 14-9455. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8050h**

Figure 14-3143. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9457. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a mcu_reset_z for MCU PLL[2:0]. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MCU_PLL_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when an MCU warm reset occurs and will keep MCU PLL[2:0] in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MCU PLL[2:0]_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: mcu_chip1_rst_n
22:9	RESERVED	NONE	0h	Reserved

Table 14-9457. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN	R/W	0h	When set, activates automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if HFOSC0 clock loss is detected Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.116 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL Register

1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL Register (Offset = 8058h) [reset = 0h]

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Table 14-9458. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8058h**

Figure 14-3144. MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL	
NONE						R/W	
0h						0h	

Table 14-9460. MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL	R/W	0h	Selects the source of the device level 32KHz Clock Field values (others are reserved): 2'b00 - CLK_32K_RC 2'b01 - HFOSC0_CLKOUT_32K 2'b10 - Reserved - (implementation: CLK_32K_RC) 2'b11 - LFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.117 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register (Offset = 8060h) [reset = 0h]

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Table 14-9461. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8060h**

Figure 14-3145. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER0_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-9463. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.118 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register (Offset = 8064h) [reset = 0h]

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Table 14-9464. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8064h**

Figure 14-3146. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER1_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-9466. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.119 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register (Offset = 8068h) [reset = 0h]

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Table 14-9467. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8068h**

Figure 14-3147. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER2_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-9469. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER2_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.120 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register (Offset = 806Ch) [reset = 0h]

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Table 14-9470. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 806Ch**

Figure 14-3148. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER3_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-9472. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER3_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.121 MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL Register (Offset = 8070h) [reset = 0h]

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Table 14-9473. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8070h**

Figure 14-3149. MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_GPIO_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-9475. MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_GPIO_CLKSEL_CLK_SEL	R/W	0h	MCU_GPIO clock selection. Must be set to MCU_SYSCLK0/4 whenever MCU_GPIO VBUS interface is activated. Other clock source may be selected as a clk_sel up clock for DeepSleep modes after MCU_GPIO is gated off through LPSC. Field values (others are reserved): 2'b00 - MCU_SYSCLK0 / 8 2'b01 - LFOSC_CLKOUT 2'b10 - CLK_32K 2'b11 - CLK_12M_RC Reset Source: mod_por_rst_n

14.2.1.1.2.2.122 MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL Register (Offset = 8080h) [reset = 0h]

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Table 14-9476. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8080h**

Figure 14-3150. MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_MCAN0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-9478. MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_MCAN0_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for MCAN0 Field values (others are reserved): 2'b00 - MCU_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - HFOSC0_CLKOUT 2'b11 - HFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.123 MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL Register (Offset = 8084h) [reset = 0h]

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Table 14-9479. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8084h

Figure 14-3151. MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_MCAN1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-9481. MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_MCAN1_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for MCAN1 Field values (others are reserved): 2'b00 - MCU_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - HFOSC0_CLKOUT 2'b11 - HFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.124 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register (Offset = 80A0h) [reset = 0h]

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Table 14-9482. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80A0h**

Figure 14-3152. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9484. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection 1'b0 - Internal clock loopback 1'b1 - Loopback from pad Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.125 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register (Offset = 80A4h) [reset = 0h]

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Table 14-9485. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80A4h**

Figure 14-3153. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-9487. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection 1'b0 - Internal clock loopback 1'b1 - Loopback from pad Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.126 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register (Offset = 80B0h) [reset = 0h]

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Table 14-9488. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80B0h**

Figure 14-3154. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MCU_WWD0_CLKSEL_WRTLOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCU_WWD0_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9490. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	MCU_WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K_RC Reset Source: mod_g_rst_n

14.2.1.1.2.2.127 MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-9491. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9008h**

Figure 14-3155. MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-9493. MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.128 MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-9494. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 900Ch**

Figure 14-3156. MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-9496. MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.129 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-9497. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9100h**

Figure 14-3157. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-9499. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.130 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-9500. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9104h**

Figure 14-3158. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-9502. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.131 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register (Offset = A000h) [reset = 0h]

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Table 14-9503. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A000h**

Figure 14-3159. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV_PROXY			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCU_OBSCLK_CTRL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-9505. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	MCU_OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 4'b0001. 1'b0 - The output of the MCU_OBSCLK output divider is output on the pin 1'b1 - HFOSC0_CLK is output on the pin Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved

Table 14-9505. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	MCU_OBSCLK_CTRL_CLK_DIV_PROXY	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by clk_div+1 Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	MCU_OBSCLK_CTRL_CLK_SEL_PROXY	R/W	0h	MCU_OBSCLK pin clock selection Field values (others are reserved): 4'b0000 - CLK_12M_RC 4'b0001 - '0' 4'b0010 - MCU_PLL0_HSDIV0_CLKOUT 4'b0011 - MCU_PLL0_HSDIV4_CLKOUT 4'b0100 - MCU_PLLCTRL_OBSCLK 4'b0101 - CLK_32K_RC 4'b0110 - HFOSC0_CLKOUT 4'b0111 - HFOSC0_CLKOUT_32K 4'b1000 - MCU_SYSCLK0 4'b1001 - DEVICE_CLKOUT_32K Reset Source: mod_por_rst_n

14.2.1.1.2.2.132 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

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Table 14-9506. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A010h**

Figure 14-3160. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HFOSC0_CTRL_PD_C_PROXY	RESERVED		HFOSC0_CTRL_BP_C_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		0h	0h			

Table 14-9508. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC0_CTRL_PD_C_PROXY	R/W	0h	Oscillator powerdown control. When set, oscillator is deactivated. Oscillator output is tristated if bp_c=0 Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C_PROXY	R/W	0h	Reserved - Must Write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.133 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register (Offset = A018h) [reset = 131022h]

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Table 14-9509. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A018h**

Figure 14-3161. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
HFOSC0_TRIM_TRIM_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED		HFOSC0_TRIM_HYST_PROXY		RESERVED	HFOSC0_TRIM_I_MULT_PROXY		
NONE		R/W		NONE	R/W		
0h		1h		0h	3h		

15	14	13	12	11	10	9	8
RESERVED		HFOSC0_TRIM_R_REF_PROXY					
NONE		R/W					
0h		10h					

7	6	5	4	3	2	1	0
HFOSC0_TRIM_I_IBIAS_COMP_PROXY				HFOSC0_TRIM_R_IBIAS_REF_PROXY			
R/W				R/W			
2h				2h			

Table 14-9511. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_TRIM_TRIM_EN_PROXY	R/W	0h	Apply MMR values to OSC trim inputs instead of tie-offs Reset Source: mod_por_rst_n
30:22	RESERVED	NONE	0h	Reserved
21:20	HFOSC0_TRIM_HYST_PROXY	R/W	1h	Sets comparator hysterisis Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HFOSC0_TRIM_I_MULT_PROXY	R/W	3h	AGC AMP current multiplication gain Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	HFOSC0_TRIM_R_REF_PROXY	R/W	10h	Sets the AMP AGC bias current Reset Source: mod_por_rst_n
7:4	HFOSC0_TRIM_I_IBIAS_COMP_PROXY	R/W	2h	Sets the COMP bias current Reset Source: mod_por_rst_n
3:0	HFOSC0_TRIM_R_IBIAS_REF_PROXY	R/W	2h	Sets the base IBIAS reference Reset Source: mod_por_rst_n

14.2.1.1.2.2.134 MCU_CTRL_MMR_CFG0_HFOSC0_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_STAT_PROXY Register (Offset = A020h) [reset = 0h]

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Table 14-9512. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A020h**

Figure 14-3162. MCU_CTRL_MMR_CFG0_HFOSC0_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							HFOSC0_STAT_DS_ON_WFI_STAT_PROXY
NONE							R
0h							X

Table 14-9514. MCU_CTRL_MMR_CFG0_HFOSC0_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	HFOSC0_STAT_DS_ON_WFI_STAT_PROXY	R	X	Allows MCU to monitor the DM attempting a Deep Sleep Reset Source: mod_g_rst_n

14.2.1.1.2.2.135 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register (Offset = A024h) [reset = 0h]

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Table 14-9515. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A024h**

Figure 14-3163. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR_PROXY	RC12M_OSC_TRIM_TRIMOSC_COARSE_PROXY			RC12M_OSC_TRIM_TRIMOSC_FINE_PROXY		
NONE	R/W	R/W			R/W		
0h	X	X			X		

Table 14-9517. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR_PROXY	R/W	X	Coarse adjustment direction. If output is greater than 12.5 0 - Coarse adjustment decreases frequency 1 - Coarse adjustment increases frequency Reset Source: mod_por_rst_n
5:3	RC12M_OSC_TRIM_TRIMOSC_COARSE_PROXY	R/W	X	Coarse adjustment. Frequency is decreased or increased by 1.25 MHz per value based on the trimosc_coarse_dir value. Reset Source: mod_por_rst_n
2:0	RC12M_OSC_TRIM_TRIMOSC_FINE_PROXY	R/W	X	Fine adjustment. Decreases the frequency by 250 KHz per value. Reset Source: mod_por_rst_n

14.2.1.1.2.2.136 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register (Offset = A030h) [reset = 8065h]

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Table 14-9518. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A030h**

Figure 14-3164. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY						
NONE	R/W						
0h	65h						

Table 14-9520. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	R/W	0h	Asynchronous Divider Reset 1 = Divider is Reset, HFOSC0_CLKOUT32K reset. 0 = Divider out of reset, HFOSC0_CLKOUT_32K running. Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	R/W	1h	HFOSC0_CLKOUT_32K activate: 0 = Synchronously Deactivate HFOSC0_CLKOUT_32KHz 1 = Synchronously Activate HFOSC0_CKLKOUT_32KHz Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Deactivate 0 = Divider Updates are shadowed and take effect on counter reset. 1 = Divider Updates are immediate and hazardous Do not set this bit to 1'b1 during normal use. Reset Source: sys_por_rst_n

Table 14-9520. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	0h	Reserved
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY	R/W	65h	HFOSC0_CLKOUT_32K divider: HFOSC0_CLKKOUT_32K Frequency = HFOSC0 Frequency / [8 * (hsdiv + 1)] Ex. HFOSC0 Frequency = 26MHz. hsdiv = 101 (Default) HFOSC0_CLKOUT_32K = 26MHz / (8 * (101+1)) = 26MHz / 816 = 31.9 KHz Reset Source: sys_por_rst_n

14.2.1.1.2.2.137 MCU_CTRL_MMR_CFG0_LFXOSC_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_LFXOSC_CTRL_PROXY Register (Offset = A038h) [reset = 80h]

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Table 14-9521. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A038h**

Figure 14-3165. MCU_CTRL_MMR_CFG0_LFXOSC_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LFXOSC_CTRL_PD_C_PROXY	RESERVED		LFXOSC_CTRL_BP_C_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
1h	0h		0h	0h			

Table 14-9523. MCU_CTRL_MMR_CFG0_LFXOSC_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LFXOSC_CTRL_PD_C_PROXY	R/W	1h	Oscillator powerdown control. When set, oscillator is deactivated. Oscillator output is tristated if bp_c=0 Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	LFXOSC_CTRL_BP_C_PROXY	R/W	0h	Oscillator bypass control. When set, oscillator is in bypass mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.138 MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Register (Offset = A03Ch) [reset = 121203h]

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Table 14-9524. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A03Ch**

Figure 14-3166. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		LFXOSC_TRIM_HYST_PROXY		RESERVED	LFXOSC_TRIM_I_MULT_PROXY		
NONE		R/W		NONE	R/W		
0h		1h		0h	2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		LFXOSC_TRIM_R_REF_PROXY					
NONE		R/W					
0h		12h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFXOSC_TRIM_I_IBIAS_COMP_PROXY				LFXOSC_TRIM_R_IBIAS_REF_PROXY			
R/W				R/W			
0h				3h			

Table 14-9526. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	LFXOSC_TRIM_HYST_PROXY	R/W	1h	Sets comparator hysterisis Field values (others are reserved): 2'b00 - Hysteresis deactivated 2'b01 - Type 1 hysteresis activated (Default) 2'b10 - Type 2 hysteresis activated 2'b11 - Both types 1 & 2 hysteresis activated Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LFXOSC_TRIM_I_MULT_PROXY	R/W	2h	AGC AMP current multiplication gain Field values (others are reserved): 3'b000 - 3x AMP_AGC IBIAS 3'b001 - 4x AMP_AGC IBIAS 3'b010 - 5x AMP_AGC IBIAS (Default) 3'b011 - 6x AMP_AGC IBIAS 3'b100 - 7x AMP_AGC IBIAS 3'b101 - 8x AMP_AGC IBIAS 3'b110 - 9x AMP_AGC IBIAS 3'b111 - 10x AMP_AGC IBIAS Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-9526. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	LFXOSC_TRIM_R_REF_PROXY	R/W	12h	Sets the AMP AGC bias current Field values (others are reserved): 6'b000000 - 0 K Ohm 6'b000001 - 24 K Ohm 6'b000010 - 48 K Ohm 6'b000011 - 73 K Ohm 6'b000100 - 97 K Ohm 6'b000101 - 121 K Ohm 6'b000110 - 145 K Ohm 6'b000111 - 169 K Ohm 6'b001000 - 193 K Ohm 6'b001001 - 218 K Ohm 6'b001010 - 242 K Ohm 6'b001011 - 266 K Ohm 6'b001100 - 290 K Ohm 6'b001101 - 314 K Ohm 6'b001110 - 338 K Ohm 6'b001111 - 363 K Ohm 6'b010000 - 387 K Ohm 6'b010001 - 411 K Ohm 6'b010010 - 435 K Ohm (Default) 6'b010011 - 459 K Ohm 6'b010100 - 483 K Ohm 6'b010101 - 508 K Ohm 6'b010110 - 532 K Ohm 6'b010111 - 556 K Ohm 6'b011000 - 580 K Ohm 6'b011001 - 604 K Ohm 6'b011010 - 628 K Ohm 6'b011011 - 653 K Ohm 6'b011100 - 677 K Ohm 6'b011101 - 701 K Ohm 6'b011110 - 725 K Ohm 6'b011111 - 749 K Ohm 6'b100000 - 773 K Ohm 6'b100001 - 798 K Ohm 6'b100010 - 822 K Ohm 6'b100011 - 846 K Ohm 6'b100100 - 870 K Ohm 6'b100101 - 894 K Ohm 6'b100110 - 918 K Ohm 6'b100111 - 943 K Ohm 6'b101000 - 967 K Ohm 6'b101001 - 991 K Ohm 6'b101010 - 1015 K Ohm 6'b101011 - 1039 K Ohm 6'b101100 - 1063 K Ohm 6'b101101 - 1088 K Ohm 6'b101110 - 1112 K Ohm 6'b101111 - 1136 K Ohm 6'b110000 - 1160 K Ohm 6'b110001 - 1184 K Ohm 6'b110010 - 1208 K Ohm 6'b110011 - 1233 K Ohm 6'b110100 - 1257 K Ohm 6'b110101 - 1281 K Ohm 6'b110110 - 1305 K Ohm 6'b110111 - 1329 K Ohm 6'b111000 - 1353 K Ohm 6'b111001 - 1378 K Ohm 6'b111010 - 1402 K Ohm 6'b111011 - 1426 K Ohm 6'b111100 - 1450 K Ohm 6'b111101 - 1474 K Ohm 6'b111110 - 1498 K Ohm

Table 14-9526. MCU_CTRL_MMR_CFG0_LFXOSC_TRIM_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111111 - 1523 K Ohm Reset Source: mod_por_rst_n
7:4	LFXOSC_TRIM_I_IBIAS_COMP_PROXY	R/W	0h	Sets the COMP bias current Field values (others are reserved): 4'b0000 - Base IBIAS ref x2 4'b0001 - Base IBIAS ref x3 4'b0010 - Base IBIAS ref x4 4'b0011 - Base IBIAS ref x5 4'b0100 - Base IBIAS ref x6 4'b0101 - Base IBIAS ref x7 4'b0110 - Base IBIAS ref x8 4'b0111 - Base IBIAS ref x9 4'b1000 - Base IBIAS ref x10 4'b1001 - Base IBIAS ref x11 4'b1010 - Base IBIAS ref x12 4'b1011 - Base IBIAS ref x13 4'b1100 - Base IBIAS ref x14 4'b1101 - Base IBIAS ref x15 4'b1110 - Base IBIAS ref x16 4'b1111 - Base IBIAS ref x17 Reset Source: mod_por_rst_n
3:0	LFXOSC_TRIM_R_IBIAS_REF_PROXY	R/W	3h	Sets the base IBIAS reference Field values (others are reserved): 4'b0000 - 512 K Ohm 4'b0001 - 576 K Ohm 4'b0010 - 640 K Ohm 4'b0011 - 704 K Ohm (Default) 4'b0100 - 768 K Ohm 4'b0101 - 832 K Ohm 4'b0110 - 896 K Ohm 4'b0111 - 960 K Ohm 4'b1000 - 1024 K Ohm 4'b1001 - 1088 K Ohm 4'b1010 - 1152 K Ohm 4'b1011 - 1216 K Ohm 4'b1100 - 1280 K Ohm 4'b1101 - 1344 K Ohm 4'b1110 - 1408 K Ohm 4'b1111 - 1472 K Ohm Reset Source: mod_por_rst_n

14.2.1.1.2.2.139 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register (Offset = A050h) [reset = 800000h]

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Table 14-9527. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A050h**

Figure 14-3167. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9529. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, activates software control of exit from bypass mode on a mcu_reset_z for MCU PLL[2:0]. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved

Table 14-9529. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to activate bypass software override. This bit is set (1'b1) when an MCU warm reset occurs and will keep MCU PLL[2:0] in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MCU PLL[2:0]_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode. Reset Source: mcu_chip1_rst_n
22:9	RESERVED	NONE	0h	Reserved
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY	R/W	0h	When set, activates automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if HFOSC0 clock loss is detected Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.140 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register (Offset = A058h) [reset = 0h]

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Table 14-9530. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A058h**

Figure 14-3168. MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-9532. MCU_CTRL_MMR_CFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL_PROXY	R/W	0h	Selects the source of the device level 32KHz Clock Field values (others are reserved): 2'b00 - CLK_32K_RC 2'b01 - HFOSC0_CLKOUT_32K 2'b10 - Reserved - (implementation: CLK_32K_RC) 2'b11 - LFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.141 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register (Offset = A060h) [reset = 0h]

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Table 14-9533. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A060h**

Figure 14-3169. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER0_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9535. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.142 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register (Offset = A064h) [reset = 0h]

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Table 14-9536. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A064h**

Figure 14-3170. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER1_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9538. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.143 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register (Offset = A068h) [reset = 0h]

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Table 14-9539. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A068h**

Figure 14-3171. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER2_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9541. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.144 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register (Offset = A06Ch) [reset = 0h]

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Table 14-9542. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A06Ch**

Figure 14-3172. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER3_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-9544. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - MCU_SYSCLK0 / 2 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.2.2.145 MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL_PROXY Register (Offset = A070h) [reset = 0h]

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Table 14-9545. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A070h**

Figure 14-3173. MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_GPIO_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-9547. MCU_CTRL_MMR_CFG0_MCU_GPIO_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_GPIO_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCU_GPIO clock selection. Must be set to MCU_SYSCLK0/4 whenever MCU_GPIO VBUS interface is activated. Other clock source may be selected as a clk_sel up clock for DeepSleep modes after MCU_GPIO is gated off through LPSC. Field values (others are reserved): 2'b00 - MCU_SYSCLK0 / 8 2'b01 - LFSOSC_CLKOUT 2'b10 - CLK_32K 2'b11 - CLK_12M_RC Reset Source: mod_por_rst_n

14.2.1.1.2.2.146 MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL_PROXY Register (Offset = A080h) [reset = 0h]

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Table 14-9548. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A080h**

Figure 14-3174. MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_MCAN0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-9550. MCU_CTRL_MMR_CFG0_MCU_MCAN0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_MCAN0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for MCAN0 Field values (others are reserved): 2'b00 - MCU_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - HFOSC0_CLKOUT 2'b11 - HFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.147 MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL_PROXY Register (Offset = A084h) [reset = 0h]

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Table 14-9551. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A084h**

Figure 14-3175. MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_MCAN1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-9553. MCU_CTRL_MMR_CFG0_MCU_MCAN1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCU_MCAN1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for MCAN1 Field values (others are reserved): 2'b00 - MCU_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 2'b10 - HFOSC0_CLKOUT 2'b11 - HFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.148 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register (Offset = A0A0h) [reset = 0h]

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Table 14-9554. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0A0h**

Figure 14-3176. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9556. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection 1'b0 - Internal clock loopback 1'b1 - Loopback from pad Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.149 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register (Offset = A0A4h) [reset = 0h]

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Table 14-9557. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0A4h**

Figure 14-3177. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9559. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection 1'b0 - Internal clock loopback 1'b1 - Loopback from pad Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.150 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register (Offset = A0B0h) [reset = 0h]

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Table 14-9560. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0B0h**

Figure 14-3178. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-9562. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	MCU_WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K_RC Reset Source: mod_g_rst_n

14.2.1.1.2.2.151 MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-9563. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B008h**

Figure 14-3179. MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-9565. MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.152 MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-9566. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B00Ch**

Figure 14-3180. MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-9568. MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.153 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-9569. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B100h**

Figure 14-3181. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-9571. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.154 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-9572. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B104h**

Figure 14-3182. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-9574. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.155 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL Register (Offset = C020h) [reset = 0h]

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Table 14-9575. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C020h**

Figure 14-3183. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_CTRL_BIST_RESET	RESERVED			MCU_R5FSS0_LBIST_CTRL_BIST_RUN			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			MCU_R5FSS0_LBIST_CTRL_SUBCHIP_ID				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_R5FSS0_LBIST_CTRL_RUNBIST_MODE				RESERVED		MCU_R5FSS0_LBIST_CTRL_DC_DEF	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_R5FSS0_LBIST_CTRL_LOAD_DIV	RESERVED		MCU_R5FSS0_LBIST_CTRL_DIVIDE_RATIO				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-9577. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_R5FSS0_LBIST_CTRL_BIST_RESET	R/W	0h	This bitfield is not used. Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	MCU_R5FSS0_LBIST_CTRL_BIST_RUN	R/W	0h	This bitfield is not used. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	MCU_R5FSS0_LBIST_CTRL_SUBCHIP_ID	R/W	0h	Specifies which sub-chip is to be tested Reset Source: mod_g_rst_n
15:12	MCU_R5FSS0_LBIST_CTRL_RUNBIST_MODE	R/W	0h	Runbist mode activate if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	MCU_R5FSS0_LBIST_CTRL_DC_DEF	R/W	0h	Clock delay after scan_activate switching Reset Source: mod_g_rst_n
7	MCU_R5FSS0_LBIST_CTRL_LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n

Table 14-9577. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	RESERVED	NONE	0h	Reserved
4:0	MCU_R5FSS0_LBIST_CTRL_DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.2.2.156 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT Register (Offset = C024h) [reset = 0h]

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Table 14-9578. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C024h**

Figure 14-3184. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT Name Register

31	30	29	28	27	26	25	24
RESERVED		MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCU_R5FSS0_LBIST_PATCOUNT_SET_PC_DEF			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_PATCOUNT_RESET_PC_DEF				MCU_R5FSS0_LBIST_PATCOUNT_SCAN_PC_DEF			
R/W				R/W			
0h				0h			

Table 14-9580. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_R5FSS0_LBIST_PATCOUNT_SET_PC_DEF	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	MCU_R5FSS0_LBIST_PATCOUNT_RESET_PC_DEF	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	MCU_R5FSS0_LBIST_PATCOUNT_SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.2.2.157 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0 Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0 Register (Offset = C028h) [reset = 0h]

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Table 14-9581. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C028h**

Figure 14-3185. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0 Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							

Table 14-9583. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_SEED0_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.2.2.158 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1 Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1 Register (Offset = C02Ch) [reset = 0h]

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Table 14-9584. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C02Ch**

Figure 14-3186. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			MCU_R5FSS0_LBIST_SEED1_PRPG_DEF				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SEED1_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SEED1_PRPG_DEF							
R/W							
0h							

Table 14-9586. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	MCU_R5FSS0_LBIST_SEED1_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.2.2.159 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0 Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0 Register (Offset = C030h) [reset = 0h]

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Table 14-9587. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C030h**

Figure 14-3187. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MCU_R5FSS0_LBIST_SPARE0_SPARE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MCU_R5FSS0_LBIST_SPARE0_SPARE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MCU_R5FSS0_LBIST_SPARE0_SPARE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">MCU_R5FSS0_LBIST_SPARE0_SPARE0</td><td>MCU_R5FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN</td><td>MCU_R5FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9589. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MCU_R5FSS0_LBIST_SPARE0_SPARE0	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	MCU_R5FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	MCU_R5FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.2.2.160 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1 Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1 Register (Offset = C034h) [reset = 0h]

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Table 14-9590. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C034h**

Figure 14-3188. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1 Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							

Table 14-9592. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_SPARE1_SPARE1	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.161 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT Register (Offset = C038h) [reset = 0h]

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Table 14-9593. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C038h**

Figure 14-3189. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_STAT_BIST_DONE	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_R5FSS0_LBIST_STAT_BIST_RUNNING	RESERVED					MCU_R5FSS0_LBIST_STAT_OUT_MUX_CTL	
R	NONE					R/W	
X	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_R5FSS0_LBIST_STAT_MISR_MUX_CTL							
R/W							
0h							

Table 14-9595. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_R5FSS0_LBIST_STAT_BIST_DONE	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	MCU_R5FSS0_LBIST_STAT_BIST_RUNNING	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	MCU_R5FSS0_LBIST_STAT_OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	MCU_R5FSS0_LBIST_STAT_MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.2.2.162 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR Register (Offset = C03Ch) [reset = 0h]

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Table 14-9596. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C03Ch**

Figure 14-3190. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_MISR_MISR_RESULT							
R							
X							

Table 14-9598. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_MISR_MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.2.2.163 MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

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Table 14-9599. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D008h**

Figure 14-3191. MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-9601. MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.164 MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-9602. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D00Ch**

Figure 14-3192. MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-9604. MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.165 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-9605. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D100h**

Figure 14-3193. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0_READONLY							
R							
0h							

Table 14-9607. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.2.2.166 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY Register (Offset = E020h) [reset = 0h]

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Table 14-9608. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E020h**

Figure 14-3194. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MCU_R5FSS0_LBIST_CTRL_BIST_RESET_PROXY</td><td colspan="3">RESERVED</td><td colspan="4">MCU_R5FSS0_LBIST_CTRL_BIST_RUN_PROXY</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MCU_R5FSS0_LBIST_CTRL_SUBCHIP_ID_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MCU_R5FSS0_LBIST_CTRL_RUNBIST_MODE_PROXY</td><td colspan="2">RESERVED</td><td colspan="2">MCU_R5FSS0_LBIST_CTRL_DC_DEF_PROXY</td></tr>
<tr><td colspan="4">R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MCU_R5FSS0_LBIST_CTRL_LOAD_DIV_PROXY</td><td colspan="2">RESERVED</td><td colspan="5">MCU_R5FSS0_LBIST_CTRL_DIVIDE_RATIO_PROXY</td></tr>
<tr><td>R/W</td><td colspan="2">NONE</td><td colspan="5">R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-9610. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_R5FSS0_LBIST_CTRL_BIST_RESET_PROXY	R/W	0h	This bitfield is not used. Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	MCU_R5FSS0_LBIST_CTRL_BIST_RUN_PROXY	R/W	0h	This bitfield is not used. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	MCU_R5FSS0_LBIST_CTRL_SUBCHIP_ID_PROXY	R/W	0h	Specifies which sub-chip is to be tested Reset Source: mod_g_rst_n
15:12	MCU_R5FSS0_LBIST_CTRL_RUNBIST_MODE_PROXY	R/W	0h	Runbist mode activate if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	MCU_R5FSS0_LBIST_CTRL_DC_DEF_PROXY	R/W	0h	Clock delay after scan_activate switching Reset Source: mod_g_rst_n

Table 14-9610. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MCU_R5FSS0_LBIST_CTRL_LOAD_DIV_PROXY	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved
4:0	MCU_R5FSS0_LBIST_CTRL_DIVIDE_RATIO_PROXY	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.2.2.167 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT_PROXY Register (Offset = E024h) [reset = 0h]

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Table 14-9611. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E024h**

Figure 14-3195. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCU_R5FSS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY				MCU_R5FSS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY			
R/W				R/W			
0h				0h			

Table 14-9613. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_PATCOUNT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	MCU_R5FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_R5FSS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	MCU_R5FSS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	MCU_R5FSS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.2.2.168 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0_PROXY Register (Offset = E028h) [reset = 0h]

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Table 14-9614. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E028h**

Figure 14-3196. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							

Table 14-9616. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_SEED0_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.2.2.169 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1_PROXY Register (Offset = E02Ch) [reset = 0h]

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Table 14-9617. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E02Ch**

Figure 14-3197. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MCU_R5FSS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MCU_R5FSS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MCU_R5FSS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9619. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SEED1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	MCU_R5FSS0_LBIST_SEED1_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.2.2.170 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0_PROXY Register (Offset = E030h) [reset = 0h]

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Table 14-9620. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E030h**

Figure 14-3198. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SPARE0_SPARE0_PROXY						MCU_R5FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	MCU_R5FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY
R/W						R/W	R/W
0h						0h	0h

Table 14-9622. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MCU_R5FSS0_LBIST_SPARE0_SPARE0_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	MCU_R5FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	MCU_R5FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.2.2.171 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1_PROXY Register (Offset = E034h) [reset = 0h]

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Table 14-9623. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E034h**

Figure 14-3199. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_R5FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_R5FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_R5FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							

Table 14-9625. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_SPARE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_SPARE1_SPARE1_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.172 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT_PROXY Register (Offset = E038h) [reset = 0h]

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Table 14-9626. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E038h**

Figure 14-3200. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_STAT_BIST_DONE_PROXY	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_R5FSS0_LBIST_STAT_BIST_RUNNING_PROXY	RESERVED					MCU_R5FSS0_LBIST_STAT_OUT_MUX_CTL_PROXY	
R	NONE					R/W	
X	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_R5FSS0_LBIST_STAT_MISR_MUX_CTL_PROXY							
R/W							
0h							

Table 14-9628. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_R5FSS0_LBIST_STAT_BIST_DONE_PROXY	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	MCU_R5FSS0_LBIST_STAT_BIST_RUNNING_PROXY	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	MCU_R5FSS0_LBIST_STAT_OUT_MUX_CTL_PROXY	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	MCU_R5FSS0_LBIST_STAT_MISR_MUX_CTL_PROXY	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.2.2.173 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR_PROXY Register (Offset = E03Ch) [reset = 0h]

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Table 14-9629. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E03Ch**

Figure 14-3201. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_R5FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MCU_R5FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_R5FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_R5FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							

Table 14-9631. MCU_CTRL_MMR_CFG0_MCU_R5FSS0_LBIST_MISR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_R5FSS0_LBIST_MISR_MISR_RESULT_PROXY	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.2.2.174 MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-9632. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F008h**

Figure 14-3202. MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0_PROXY							
R/W							
0h							

Table 14-9634. MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.175 MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-9635. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F00Ch**

Figure 14-3203. MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1_PROXY							
R/W							
0h							

Table 14-9637. MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.176 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-9638. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F100h**

Figure 14-3204. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0							
R/W							
0h							

Table 14-9640. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.2.2.177 MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-9641. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1008h**

Figure 14-3205. MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0							
R/W							
0h							

Table 14-9643. MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.178 MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-9644. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 100Ch**

Figure 14-3206. MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-9646. MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.179 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9647. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1100h**

Figure 14-3207. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-9649. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.180 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register (Offset = 11104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9650. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1104h**

Figure 14-3208. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1_READONLY							
R							
0h							

Table 14-9652. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.181 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register (Offset = 11108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9653. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1108h**

Figure 14-3209. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2_READONLY							
R							
0h							

Table 14-9655. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.182 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register (Offset = 1110Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9656. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 110Ch**

Figure 14-3210. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3_READONLY							
R							
0h							

Table 14-9658. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.183 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register (Offset = 11110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9659. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1110h**

Figure 14-3211. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4_READONLY							
R							
0h							

Table 14-9661. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.184 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register (Offset = 11114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9662. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1114h**

Figure 14-3212. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5_READONLY							
R							
0h							

Table 14-9664. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.185 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register (Offset = 11118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9665. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1118h**

Figure 14-3213. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6_READONLY							
R							
0h							

Table 14-9667. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.186 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register (Offset = 1111Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9668. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 111Ch**

Figure 14-3214. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7_READONLY							
R							
0h							

Table 14-9670. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.187 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9671. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1120h**

Figure 14-3215. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-9673. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.188 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register (Offset = 11124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9674. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1124h**

Figure 14-3216. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9_READONLY							
R							
0h							

Table 14-9676. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.189 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register (Offset = 11128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9677. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1128h**

Figure 14-3217. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10_READONLY							
R							
0h							

Table 14-9679. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.190 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register (Offset = 1112Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9680. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 112Ch**

Figure 14-3218. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11_READONLY							
R							
0h							

Table 14-9682. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.191 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register (Offset = 11130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9683. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1130h**

Figure 14-3219. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12_READONLY							
R							
0h							

Table 14-9685. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.192 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register (Offset = 11134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9686. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1134h**

Figure 14-3220. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13_READONLY							
R							
0h							

Table 14-9688. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.193 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register (Offset = 11138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9689. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1138h**

Figure 14-3221. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14_READONLY							
R							
0h							

Table 14-9691. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.194 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15_READONLY Register (Offset = 1113Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9692. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 113Ch**

Figure 14-3222. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R15_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R15_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R15_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R15_READONLY							
R							
0h							

Table 14-9694. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R15_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.195 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16_READONLY Register (Offset = 11140h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9695. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1140h**

Figure 14-3223. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R16_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R16_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R16_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R16_READONLY							
R							
0h							

Table 14-9697. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R16_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.196 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17_READONLY Register (Offset = 11144h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9698. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1144h**

Figure 14-3224. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R17_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R17_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R17_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R17_READONLY							
R							
0h							

Table 14-9700. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R17_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.197 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18_READONLY Register (Offset = 11148h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9701. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1148h**

Figure 14-3225. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R18_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R18_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R18_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R18_READONLY							
R							
0h							

Table 14-9703. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R18_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.198 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19_READONLY Register (Offset = 1114Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9704. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 114Ch**

Figure 14-3226. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R19_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R19_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R19_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R19_READONLY							
R							
0h							

Table 14-9706. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R19_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.199 MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-9707. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3008h**

Figure 14-3227. MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-9709. MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.200 MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-9710. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 300Ch**

Figure 14-3228. MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-9712. MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.201 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9713. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3100h**

Figure 14-3229. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-9715. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.202 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9716. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3104h**

Figure 14-3230. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-9718. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.203 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9719. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3108h**

Figure 14-3231. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-9721. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.204 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9722. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 310Ch**

Figure 14-3232. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9724. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.205 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9725. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3110h**

Figure 14-3233. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-9727. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.206 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9728. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3114h**

Figure 14-3234. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-9730. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.207 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9731. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3118h**

Figure 14-3235. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9733. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.208 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9734. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 311Ch**

Figure 14-3236. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-9736. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.209 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9737. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3120h**

Figure 14-3237. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-9739. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.210 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9740. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3124h**

Figure 14-3238. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-9742. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.211 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9743. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3128h**

Figure 14-3239. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10							
R/W							
0h							

Table 14-9745. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.212 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register (Offset = 1312Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9746. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 312Ch**

Figure 14-3240. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11							
R/W							
0h							

Table 14-9748. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.213 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register (Offset = 13130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9749. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3130h**

Figure 14-3241. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12							
R/W							
0h							

Table 14-9751. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.214 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register (Offset = 13134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9752. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3134h**

Figure 14-3242. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13							
R/W							
0h							

Table 14-9754. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.215 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register (Offset = 13138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9755. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3138h**

Figure 14-3243. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14							
R/W							
0h							

Table 14-9757. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.216 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15 Register (Offset = 1313Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9758. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 313Ch**

Figure 14-3244. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R15							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R15							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R15							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R15							
R/W							
0h							

Table 14-9760. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R15	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.217 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16 Register (Offset = 13140h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9761. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3140h**

Figure 14-3245. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R16							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R16							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R16							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R16							
R/W							
0h							

Table 14-9763. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R16	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.218 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17 Register (Offset = 13144h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9764. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3144h**

Figure 14-3246. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9766. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R17	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.219 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18 Register (Offset = 13148h) [reset = 0h]

Claim bits for Partition 4

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Table 14-9767. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3148h**

Figure 14-3247. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R18							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R18							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R18							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R18							
R/W							
0h							

Table 14-9769. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R18	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.220 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19 Register (Offset = 1314Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-9770. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 314Ch**

Figure 14-3248. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R19</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R19</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R19</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R19</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9772. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R19	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.221 MCU_CTRL_MMR_CFG0_POR_CTRL Register

1 MCU_CTRL_MMR_CFG0_POR_CTRL Register (Offset = 18000h) [reset = 10h]

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Table 14-9773. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8000h**

Figure 14-3249. MCU_CTRL_MMR_CFG0_POR_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5	POR_CTRL_OVRD_SET4	POR_CTRL_OVRD_SET3	POR_CTRL_OVRD_SET2	POR_CTRL_OVRD_SET1	POR_CTRL_OVRD_SET0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED		POR_CTRL_OVRD5	POR_CTRL_OVRD4	POR_CTRL_OVRD3	POR_CTRL_OVRD2	POR_CTRL_OVRD1	POR_CTRL_OVRD0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POR_CTRL_TRIM_SEL	RESERVED		POR_CTRL_MASK_HHV	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-9775. MCU_CTRL_MMR_CFG0_POR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5	R/W	0h	Reserved override set Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4	R/W	0h	POKLVB override set Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3	R/W	0h	POKLVA override set Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2	R/W	0h	POKHV override set Reset Source: mod_por_rst_n
25	POR_CTRL_OVRD_SET1	R/W	0h	BGOK override set Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0	R/W	0h	PORHV override set Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	POR_CTRL_OVRD5	R/W	0h	Reserved override activate Reset Source: mod_por_rst_n

Table 14-9775. MCU_CTRL_MMR_CFG0_POR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POR_CTRL_OVRD4	R/W	0h	POKLVB override activate Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3	R/W	0h	POKLVA override activate Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2	R/W	0h	POKHV override activate Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1	R/W	0h	BGOK override activate Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0	R/W	0h	PORHV override activate Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL	R/W	0h	POR Trim Select 0 - Trim selections for Bandgap and POKs come from HHV defaults 1 - Trim selections for Bandgap and POKs come from POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.222 MCU_CTRL_MMR_CFG0_POR_STAT Register

1 MCU_CTRL_MMR_CFG0_POR_STAT Register (Offset = 18004h) [reset = 0h]

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Table 14-9776. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8004h**

Figure 14-3250. MCU_CTRL_MMR_CFG0_POR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							POR_STAT_BGOK
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED			POR_STAT_SOC_POR	RESERVED			
NONE			R	NONE			
0h			X	0h			

Table 14-9778. MCU_CTRL_MMR_CFG0_POR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK	R	X	Bandgap OK status Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR	R	X	POR module status 0 - Module is in functional mode 1 - Module is in reset mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.223 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register

1 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register (Offset = 18100h) [reset = 0h]

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Table 14-9779. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8100h**

Figure 14-3251. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">POR_BANDGAP_CTRL_BGAPI</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">POR_BANDGAP_CTRL_BGAPV</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">POR_BANDGAP_CTRL_BGAPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-9781. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	POR_BANDGAP_CTRL_BGAPI	R/W	X	Bandgap output current trim bits Reset Source: mod_por_rst_n
15:8	POR_BANDGAP_CTRL_BGAPV	R/W	X	Bandgap output voltage magnitude trim bits Reset Source: mod_por_rst_n
7:0	POR_BANDGAP_CTRL_BGAPC	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset Reset Source: mod_por_rst_n

14.2.1.1.2.2.224 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register (Offset = 18110h) [reset = 80000000h]

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Table 14-9782. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8110h**

Figure 14-3252. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET	POK_VDDA_MCU_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9784. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.225 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register (Offset = 18114h) [reset = 80000000h]

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Table 14-9785. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8114h**

Figure 14-3253. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET	POK_VDDA_MCU_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9787. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.226 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register (Offset = 18118h) [reset = 80000000h]

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Table 14-9788. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8118h**

Figure 14-3254. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET	POK_VDD_CORE_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9790. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.227 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register (Offset = 1811Ch) [reset = 80000000h]

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Table 14-9791. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 811Ch**

Figure 14-3255. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET	POK_VDD_CORE_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9793. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.228 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register (Offset = 18120h) [reset = 80000000h]

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Table 14-9794. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8120h**

Figure 14-3256. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET	POK_VDDR_CORE_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9796. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.229 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register (Offset = 18124h) [reset = 80000000h]

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Table 14-9797. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8124h**

Figure 14-3257. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET	POK_VDDR_CORE_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9799. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.230 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register (Offset = 18138h) [reset = 80000000h]

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Table 14-9800. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8138h**

Figure 14-3258. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9802. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.231 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register (Offset = 1813Ch) [reset = 80000000h]

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Table 14-9803. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 813Ch**

Figure 14-3259. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9805. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.232 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register (Offset = 18140h) [reset = 80000000h]

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Table 14-9806. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8140h**

Figure 14-3260. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVERVOLT_DET	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9808. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.233 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register (Offset = 18144h) [reset = 80000000h]

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Table 14-9809. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8144h**

Figure 14-3261. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9811. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.234 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register (Offset = 18148h) [reset = 80000000h]

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Table 14-9812. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8148h**

Figure 14-3262. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9814. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.235 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register (Offset = 1814Ch) [reset = 80000000h]

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Table 14-9815. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 814Ch**

Figure 14-3263. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9817. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.236 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register (Offset = 18150h) [reset = 80000000h]

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Table 14-9818. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8150h**

Figure 14-3264. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9820. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_UV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.237 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register (Offset = 18154h) [reset = 80000000h]

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Table 14-9821. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8154h**

Figure 14-3265. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-9823. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_OV_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.238 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register (Offset = 18160h) [reset = 80000000h]

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Table 14-9824. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8160h**

Figure 14-3266. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9826. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.239 MCU_CTRL_MMR_CFG0_RST_CTRL Register

1 MCU_CTRL_MMR_CFG0_RST_CTRL Register (Offset = 18170h) [reset = 420FFFh]

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Table 14-9827. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8170h**

Figure 14-3267. MCU_CTRL_MMR_CFG0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	RST_CTRL_DM_WDT_RST_EN_Z	RESERVED			RST_CTRL_MCU_RESET_ISO_DONE_Z	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z	RST_CTRL_SMS_COLD_RESET_EN_Z
NONE	R/W	NONE			R/W	R/W	R/W
0h	1h	0h			0h	1h	0h
15	14	13	12	11	10	9	8
RESERVED				RST_CTRL_SW_MCU_WARMRST			
NONE				R/W			
0h				Fh			
7	6	5	4	3	2	1	0
RST_CTRL_SW_MAIN_POR				RST_CTRL_SW_MAIN_WARMRST			
R/W				R/W			
Fh				Fh			

Table 14-9829. MCU_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	RST_CTRL_DM_WDT_RST_EN_Z	R/W	1h	Deactivate Reset from DM WDT propogating to MCU domain: 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
21:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MCU_RESET_ISO_DONE_Z	R/W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing main domain resources (peripherals, memory..). In this case, the MCU will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0 - Reset of Main Domain is not Blocked by MCU Domain 1 - Reset of Main Domain is Blocked by MCU Domain Reset Source: mcu_chip1_rst_n

Table 14-9829. MCU_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z	R/W	1h	Deactivate Reset of MCU by ESM 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z	R/W	0h	Deactivate Reset of MCU by SMS 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Causes MCU Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: mcu_chip1_rst_n
7:4	RST_CTRL_SW_MAIN_POR	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.2.2.240 MCU_CTRL_MMR_CFG0_RST_STAT Register

1 MCU_CTRL_MMR_CFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

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Table 14-9830. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8174h**

Figure 14-3268. MCU_CTRL_MMR_CFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MAIN_RESETSTATZ
NONE							R
0h							X

Table 14-9832. MCU_CTRL_MMR_CFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ	R	X	Status of Main Domain Reset: 0 = Reset Asserted 1 = Reset Deasserted Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.241 MCU_CTRL_MMR_CFG0_RST_SRC Register

1 MCU_CTRL_MMR_CFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

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Table 14-9833. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8178h**

Figure 14-3269. MCU_CTRL_MMR_CFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN	RST_SRC_SW_MAIN_POR_FROM_MCU
R/W1TC	R/W1TC	NONE				R/W1TC	R/W1TC
0h	0h	0h				0h	0h
23	22	21	20	19	18	17	16
RST_SRC_DS_MAIN_PORZ	RST_SRC_DM_WDT_RST	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	RESERVED			RST_SRC_SW_MCU_WARMRST
R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE			R/W1TC
0h	0h	0h	0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R/W1TC	R/W1TC	NONE			R/W1TC
0h		0h	0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST	RESERVED	RST_SRC_MAIN_RESET_REQ	RESERVED	RST_SRC_MCU_RESET_PIN
NONE			R/W1TC	NONE	R/W1TC	NONE	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-9835. MCU_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R/W1TC	0h	Reset Caused by MCU ESM Error Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R/W1TC	0h	Reset Caused by Main ESM Error Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN	R/W1TC	0h	Software Main Power On Reset From MAIN CTRL MMR Reset Source: mod_por_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU	R/W1TC	0h	Software Main Power On Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
23	RST_SRC_DS_MAIN_PORZ	R/W1TC	0h	Reset of Main/Wkup Domains while in Deep Sleep, as a result of an MCU Warm Reset Reset Source: mod_por_rst_n

Table 14-9835. MCU_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RST_SRC_DM_WDT_RST	R/W1TC	0h	Watchdog Initiated Reset Reset Source: mod_por_rst_n
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	R/W1TC	0h	Software Main Warm Reset from MAIN CTRL MMR Reset Source: mod_por_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	R/W1TC	0h	Software Main Warm Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R/W1TC	0h	Software Warm Reset Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST	R/W1TC	0h	SMS Warm Reset Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST	R/W1TC	0h	SMS Cold Reset Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R/W1TC	0h	Debug Subsystem Initiated Reset Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R/W1TC	0h	Thermal Reset Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ	R/W1TC	0h	Main Reset Pin Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R/W1TC	0h	Rest Caused by MCU Reset Pin Reset Source: mod_por_rst_n

14.2.1.1.2.2.242 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register

1 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

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Table 14-9836. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 817Ch**

Figure 14-3270. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							

Table 14-9838. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD	R/W	0h	After a MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any reset from the Main Domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it shall leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the MCU R5FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from any warm reset sources that triggers main_resetz, the value must be non-zero. If the value is nonzero and a Main domain warm reset that triggers main_resetz occurs in the main domain, the MCU R5FSS will not be reset. The Main domain bootloader must read this value to determine that the MCU R5FSS is already initialized, and has configured reset isolation. The Main domain bootloader then also skips any initialization steps involving bootstrapping the R5FSS (as it is is already running). Note that MCU_PORz reset is never blocked by a nonzero magic word. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.243 MCU_CTRL_MMR_CFG0_ISO_CTRL Register

1 MCU_CTRL_MMR_CFG0_ISO_CTRL Register (Offset = 18180h) [reset = 0h]

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Table 14-9839. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8180h**

Figure 14-3271. MCU_CTRL_MMR_CFG0_ISO_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ISO_CTRL_MCU_DBG_ISO_EN	ISO_CTRL_MCU_RST_ISO_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-9841. MCU_CTRL_MMR_CFG0_ISO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	ISO_CTRL_MCU_DBG_ISO_EN	R/W	0h	Isolates the MCU domain from Debug Field values (others are reserved): undefined - undefined undefined - undefined 1'b0 - R5FSS is not debug isolated 1'b1 - R5FSS is isolated from debug if RST_MAGIC_WORD is also nonzero Reset Source: mcu_chip1_rst_n
0	ISO_CTRL_MCU_RST_ISO_EN	R/W	0h	Isolates the MCU domain from Warm Reset initiated by Main Field values (others are reserved): undefined - undefined undefined - undefined 1'b0 - R5FSS is not reset isolated 1'b1 - R5FSS is isolated from main warm reset if RST_MAGIC_WORD is also nonzero Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.244 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register (Offset = 18190h) [reset = 0h]

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Table 14-9842. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8190h**

Figure 14-3272. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Name Register

31	30	29	28	27	26	25	24
VDD_CORE_GLDTC_CTRL_PWDB	VDD_CORE_GLDTC_CTRL_RSTB	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL		
NONE					R/W		
0h					X		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL					
NONE		R/W					
0h		X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL					
NONE		R/W					
0h		X					

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB	R/W	0h	Power down - active low. 0 - Deactivate all functions 1 - Activate glitch detectors Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0 - Reset glitch detector flags 1 - Glitch detection flags are activated Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth Field values (others are reserved): 3'b000 - 150 kHz 3'b001 - 125 kHz 3'b010 - 100 kHz 3'b011 - 80 kHz 3'b100 - 60 kHz 3'b101 - 45 kHz 3'b110 - 30 kHz 3'b111 - 15 kHz Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - 93.5% of VDD 6'b000001 - 94.0% of VDD 6'b000010 - 94.5% of VDD 6'b000011 - 95.0% of VDD 6'b000100 - 95.5% of VDD 6'b000101 - 96.0% of VDD 6'b000110 - 96.5% of VDD 6'b000111 - 97.0% of VDD 6'b001000 - 97.5% of VDD 6'b001001 - 98.0% of VDD 6'b001010 - 98.5% of VDD 6'b001011 - 99.0% of VDD 6'b001100 - 99.5% of VDD 6'b001101 - 100.0% of VDD 6'b001110 - 100.5% of VDD 6'b001111 - 101.0% of VDD 6'b010000 - 101.5% of VDD 6'b010001 - 102.0% of VDD 6'b010010 - 102.5% of VDD 6'b010011 - 103.0% of VDD 6'b010100 - 103.5% of VDD 6'b010101 - 104.0% of VDD 6'b010110 - 104.5% of VDD 6'b010111 - 105.0% of VDD 6'b011000 - 105.5% of VDD 6'b011001 - 106.0% of VDD 6'b011010 - 106.5% of VDD 6'b011011 - 107.0% of VDD 6'b011100 - 107.5% of VDD 6'b011101 - 108.0% of VDD 6'b011110 - 108.5% of VDD 6'b011111 - 109.0% of VDD 6'b100000 - 109.5% of VDD 6'b100001 - 110.0% of VDD 6'b100010 - 111.0% of VDD 6'b100011 - 112.0% of VDD 6'b100100 - 113.0% of VDD 6'b100101 - 114.0% of VDD 6'b100110 - 115.0% of VDD 6'b100111 - 116.0% of VDD 6'b101000 - 117.0% of VDD 6'b101001 - 118.0% of VDD 6'b101010 - 119.0% of VDD 6'b101011 - 120.0% of VDD 6'b101100 - 121.0% of VDD 6'b101101 - 122.0% of VDD 6'b101110 - 123.0% of VDD 6'b101111 - 124.0% of VDD 6'b110000 - 125.0% of VDD 6'b110001 - 126.0% of VDD 6'b110010 - 127.0% of VDD 6'b110011 - 128.0% of VDD 6'b110100 - 129.0% of VDD 6'b110101 - 130.0% of VDD 6'b110110 - 131.0% of VDD 6'b110111 - 132.0% of VDD 6'b111000 - 133.0% of VDD 6'b111001 - 134.0% of VDD 6'b111010 - 135.0% of VDD 6'b111011 - 136.0% of VDD 6'b111100 - 137.0% of VDD

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111101 - 138.0% of VDD 6'b111110 - 139.0% of VDD 6'b111111 - 140.0% of VDD Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - 106.5% of VDD 6'b000001 - 106.0% of VDD 6'b000010 - 105.5% of VDD 6'b000011 - 105.0% of VDD 6'b000100 - 104.5% of VDD 6'b000101 - 104.0% of VDD 6'b000110 - 103.5% of VDD 6'b000111 - 103.0% of VDD 6'b001000 - 102.5% of VDD 6'b001001 - 102.0% of VDD 6'b001010 - 101.5% of VDD 6'b001011 - 101.0% of VDD 6'b001100 - 100.5% of VDD 6'b001101 - 100.0% of VDD 6'b001110 - 99.5% of VDD 6'b001111 - 99.0% of VDD 6'b010000 - 98.5% of VDD 6'b010001 - 98.0% of VDD 6'b010010 - 97.5% of VDD 6'b010011 - 97.0% of VDD 6'b010100 - 96.5% of VDD 6'b010101 - 96.0% of VDD 6'b010110 - 95.5% of VDD 6'b010111 - 95.0% of VDD 6'b011000 - 94.5% of VDD 6'b011001 - 94.0% of VDD 6'b011010 - 93.5% of VDD 6'b011011 - 93.0% of VDD 6'b011100 - 92.5% of VDD 6'b011101 - 92.0% of VDD 6'b011110 - 91.5% of VDD 6'b011111 - 91.0% of VDD 6'b100000 - 90.5% of VDD 6'b100001 - 90.0% of VDD 6'b100010 - 89.0% of VDD 6'b100011 - 88.0% of VDD 6'b100100 - 87.0% of VDD 6'b100101 - 86.0% of VDD 6'b100110 - 85.0% of VDD 6'b100111 - 84.0% of VDD 6'b101000 - 83.0% of VDD 6'b101001 - 82.0% of VDD 6'b101010 - 81.0% of VDD 6'b101011 - 80.0% of VDD 6'b101100 - 79.0% of VDD 6'b101101 - 78.0% of VDD 6'b101110 - 77.0% of VDD 6'b101111 - 76.0% of VDD 6'b110000 - 75.0% of VDD 6'b110001 - 74.0% of VDD 6'b110010 - 73.0% of VDD 6'b110011 - 72.0% of VDD 6'b110100 - 71.0% of VDD 6'b110101 - 70.0% of VDD 6'b110110 - 69.0% of VDD 6'b110111 - 68.0% of VDD 6'b111000 - 67.0% of VDD 6'b111001 - 66.0% of VDD 6'b111010 - 65.0% of VDD 6'b111011 - 64.0% of VDD 6'b111100 - 63.0% of VDD

Table 14-9844. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111101 - 62.0% of VDD 6'b111110 - 61.0% of VDD 6'b111111 - 60.0% of VDD Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.245 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register (Offset = 181B0h) [reset = 0h]

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Table 14-9845. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 81B0h**

Figure 14-3273. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG
NONE							R
0h							X

Table 14-9847. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0 - No high voltage detected 1 - Voltage above the high voltage threshold was detected. Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0 - No low voltage detected 1 - Voltage below the low voltage threshold was detected. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.246 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register (Offset = 18200h) [reset = 2001Fh]

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Table 14-9848. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8200h**

Figure 14-3274. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-9850. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP0 POKs: 2'b00 - 5 us 2'b01 -10 us 2'b10 - 15 us 2'b11 - 20us Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL	R/W	0h	Select POK activate source 0 - POK activates come from hardware tie-offs 1 - POK activates come from PRG_PP0_CTRL register Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	R/W	1h	Activate VDDA_PMIC_IN undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n

Table 14-9850. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	R/W	1h	Activate VDD_MCU overvoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	R/W	1h	Activate VDD_MCU undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	R/W	1h	Activate 1.8V VDDA_MCU overvoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
0	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN	R/W	1h	Activate 1.8V VDDA_MCU undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n

14.2.1.1.2.2.247 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register (Offset = 18208h) [reset = 2007Fh]

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Table 14-9851. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8208h**

Figure 14-3275. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PRG_PP_1_CTRL_POK_PP_EN	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	
15	14	13	12	11	10	9	8
PRG_PP_1_CTRL_POK_EN_SEL	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL	RSVD	RSVD	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL
R/W	R/W	R/W	R/W	R/W			R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN	RSVD	RSVD	PRG_PP_1_CTRL_POK_VDDR_CORE_EN
NONE	R/W	R/W	R/W	R/W			R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-9853. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN	R/W	0h	POK ping-pong activate. When set, activatesautomatic switching between undervoltage andovervoltage detection on PRG_PP1 (POK_VDDR_CORE, POK_VDDSHV_MCU_1P8, POK_VDDSHV_MCU_3P3, POK_VMON_CAP_MCU_GENERAL, POK_VDDSHV_MAIN_1P8, POK_VDDSHV_MAIN_3P3, and POK_VDDS_DDRIO) POKs. This bit has no effect if the POK's ov_sel bit = 1. 0 - No pingpong operation. UV/OV operationselected by each POK ov_sel bit 1 - Pingpong operation activated . Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved

Table 14-9853. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP1 POKs: 2'b00 - 5 us 2'b01 -10 us 2'b10 - 15 us 2'b11 - 20us Reset Source: mod_por_rst_n
15	PRG_PP_1_CTRL_POK_EN_SEL	R/W	0h	Select POK activate source 0 - POK activates come from hardware tie-offs 1 - POK activates come from PRG_PP1_CTRL register Reset Source: mod_por_rst_n
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	R/W	0h	POK_VDDS_DDRIO mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_3P3 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_1P8 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL	R/W	0h	POK_VDDR_CORE Mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	R/W	1h	Activate POK_VDDS_DDRIO (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	R/W	1h	Activate POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	R/W	1h	Activate POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN	R/W	1h	Activate POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n

Table 14-9853. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN	R/W	1h	Activate POK_VDDR_CORE (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n

14.2.1.1.2.2.248 MCU_CTRL_MMR_CFG0_CLKGATE_CTRL Register

1 MCU_CTRL_MMR_CFG0_CLKGATE_CTRL Register (Offset = 18280h) [reset = 0h]

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Table 14-9854. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8280h**

Figure 14-3276. MCU_CTRL_MMR_CFG0_CLKGATE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKGATE_CTRL_MCUSS_NOGATE	CLKGATE_CTRL_MCU_CBA_NOGATE	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-9856. MCU_CTRL_MMR_CFG0_CLKGATE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CLKGATE_CTRL_MCUSS_NOGATE	R/W	0h	MCU Subsystem clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
1	CLKGATE_CTRL_MCU_CBA_NOGATE	R/W	0h	MCU domain Data bus (mcu_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
0	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE	R/W	0h	WKUP domain Infrastructure bus (wkup_safe_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.2.2.249 MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-9857. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9008h**

Figure 14-3277. MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-9859. MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.250 MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-9860. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 900Ch**

Figure 14-3278. MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-9862. MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.251 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9863. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9100h**

Figure 14-3279. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-9865. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.252 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9866. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9104h**

Figure 14-3280. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-9868. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.253 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9869. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9108h**

Figure 14-3281. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-9871. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.254 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9872. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 910Ch**

Figure 14-3282. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-9874. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.255 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9875. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9110h**

Figure 14-3283. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-9877. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.256 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9878. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9114h**

Figure 14-3284. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5_READONLY							
R							
0h							

Table 14-9880. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.257 MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register (Offset = 1A000h) [reset = 10h]

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Table 14-9881. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A000h**

Figure 14-3285. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5_PROXY	POR_CTRL_OVRD_SET4_PROXY	POR_CTRL_OVRD_SET3_PROXY	POR_CTRL_OVRD_SET2_PROXY	POR_CTRL_OVRD_SET1_PROXY	POR_CTRL_OVRD_SET0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED		POR_CTRL_OVRD5_PROXY	POR_CTRL_OVRD4_PROXY	POR_CTRL_OVRD3_PROXY	POR_CTRL_OVRD2_PROXY	POR_CTRL_OVRD1_PROXY	POR_CTRL_OVRD0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POR_CTRL_TRIM_SEL_PROXY	RESERVED		POR_CTRL_MASK_HHV_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-9883. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5_PROXY	R/W	0h	Reserved override set Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4_PROXY	R/W	0h	POKLVB override set Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3_PROXY	R/W	0h	POKLVA override set Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2_PROXY	R/W	0h	POKHV override set Reset Source: mod_por_rst_n
25	POR_CTRL_OVRD_SET1_PROXY	R/W	0h	BGOK override set Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0_PROXY	R/W	0h	PORHV override set Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-9883. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	POR_CTRL_OVRD5_PROXY	R/W	0h	Reserved override activate Reset Source: mod_por_rst_n
20	POR_CTRL_OVRD4_PROXY	R/W	0h	POKLVB override activate Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3_PROXY	R/W	0h	POKLVA override activate Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2_PROXY	R/W	0h	POKHV override activate Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1_PROXY	R/W	0h	BGOK override activate Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0_PROXY	R/W	0h	PORHV override activate Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL_PROXY	R/W	0h	POR Trim Select 0 - Trim selections for Bandgap and POKs come from HHV defaults 1 - Trim selections for Bandgap and POKs come from POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV_PROXY	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.258 MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register (Offset = 1A004h) [reset = 0h]

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Table 14-9884. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A004h**

Figure 14-3286. MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							POR_STAT_BGOK_PROXY
NONE							R
0h							X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POR_STAT_SOC_POR_PROXY	RESERVED			
NONE			R	NONE			
0h			X	0h			

Table 14-9886. MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK_PROXY	R	X	Bandgap OK status Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR_PROXY	R	X	POR module status 0 - Module is in functional mode 1 - Module is in reset mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.259 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register (Offset = 1A100h) [reset = 0h]

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Table 14-9887. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A100h**

Figure 14-3287. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				POR_BANDGAP_CTRL_BGAPI_PROXY			
NONE				R/W			
0h				X			
15	14	13	12	11	10	9	8
POR_BANDGAP_CTRL_BGAPV_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
POR_BANDGAP_CTRL_BGAPC_PROXY							
R/W							
X							

Table 14-9889. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	POR_BANDGAP_CTRL_BGAPI_PROXY	R/W	X	Bandgap output current trim bits Reset Source: mod_por_rst_n
15:8	POR_BANDGAP_CTRL_BGAPV_PROXY	R/W	X	Bandgap output voltage magnitude trim bits Reset Source: mod_por_rst_n
7:0	POR_BANDGAP_CTRL_BGAPC_PROXY	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset Reset Source: mod_por_rst_n

14.2.1.1.2.2.260 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register (Offset = 1A110h) [reset = 80000000h]

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Table 14-9890. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A110h**

Figure 14-3288. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDA_MCU_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9892. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.261 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register (Offset = 1A114h) [reset = 80000000h]

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Table 14-9893. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A114h**

Figure 14-3289. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDA_MCU_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9895. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.262 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register (Offset = 1A118h) [reset = 80000000h]

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Table 14-9896. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A118h**

Figure 14-3290. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDD_CORE_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9898. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.263 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register (Offset = 1A11Ch) [reset = 80000000h]

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Table 14-9899. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A11Ch**

Figure 14-3291. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDD_CORE_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9901. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.264 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register (Offset = 1A120h) [reset = 80000000h]

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Table 14-9902. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A120h**

Figure 14-3292. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDR_CORE_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9904. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.265 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register (Offset = 1A124h) [reset = 80000000h]

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Table 14-9905. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A124h**

Figure 14-3293. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDR_CORE_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9907. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.266 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register (Offset = 1A138h) [reset = 80000000h]

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Table 14-9908. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A138h**

Figure 14-3294. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9910. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.267 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register (Offset = 1A13Ch) [reset = 80000000h]

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Table 14-9911. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A13Ch

Figure 14-3295. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9913. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.268 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register (Offset = 1A140h) [reset = 80000000h]

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Table 14-9914. Instance Table

Instance Name	**Physical Address**
MCU_CTRL_MMR0	**0451 A140h**

Figure 14-3296. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9916. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.269 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register (Offset = 1A144h) [reset = 80000000h]

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Table 14-9917. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A144h**

Figure 14-3297. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY</td><td colspan="7">POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM_PROXY</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>X</td><td colspan="7">X</td></tr>
</table>

Table 14-9919. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.270 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register (Offset = 1A148h) [reset = 80000000h]

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Table 14-9920. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A148h**

Figure 14-3298. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9922. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.271 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register (Offset = 1A14Ch) [reset = 80000000h]

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Table 14-9923. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A14Ch**

Figure 14-3299. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9925. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.272 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register (Offset = 1A150h) [reset = 80000000h]

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Table 14-9926. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A150h**

Figure 14-3300. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9928. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_UV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.273 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register (Offset = 1A154h) [reset = 80000000h]

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Table 14-9929. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A154h**

Figure 14-3301. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-9931. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_OV_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.274 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register (Offset = 1A160h) [reset = 80000000h]

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Table 14-9932. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A160h**

Figure 14-3302. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	RESERVED						
R/W	NONE						
0h	0h						

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9934. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	R/W	1h	Activate POK hysteresis Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode 0 - Under voltage detection 1 - Over voltage detection Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.275 MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 420FFFh]

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Table 14-9935. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A170h**

Figure 14-3303. MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	RST_CTRL_DM_WDT_RST_EN_Z_PROXY	RESERVED			RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY
NONE	R/W	NONE			R/W	R/W	R/W
0h	1h	0h			0h	1h	0h

15	14	13	12	11	10	9	8
RESERVED				RST_CTRL_SW_MCU_WARMRST_PROXY			
NONE				R/W			
0h				Fh			

7	6	5	4	3	2	1	0
RST_CTRL_SW_MAIN_POR_PROXY				RST_CTRL_SW_MAIN_WARMRST_PROXY			
R/W				R/W			
Fh				Fh			

Table 14-9937. MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	RST_CTRL_DM_WDT_RST_EN_Z_PROXY	R/W	1h	Deactivate Reset from DM WDT propogating to MCU domain: 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
21:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	R/W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing main domain resources (peripherals, memory..). In this case, the MCU will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0 - Reset of Main Domain is not Blocked by MCU Domain 1 - Reset of Main Domain is Blocked by MCU Domain Reset Source: mcu_chip1_rst_n

Table 14-9937. MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Deactivate Reset of MCU by ESM 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY	R/W	0h	Deactivate Reset of MCU by SMS 0 - Activated 1 - Deactivated Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST_PROXY	R/W	Fh	This is a fault tolerant bitfield. Causes MCU Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: mcu_chip1_rst_n
7:4	RST_CTRL_SW_MAIN_POR_PROXY	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST_PROXY	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.2.2.276 MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

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Table 14-9938. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A174h**

Figure 14-3304. MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MAIN_RESETSTATZ_PROXY
NONE							R
0h							X

Table 14-9940. MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ_PROXY	R	X	Status of Main Domain Reset: 0 = Reset Asserted 1 = Reset Deasserted Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.277 MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

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Table 14-9941. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A178h**

Figure 14-3305. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY
R/W1TC	R/W1TC	NONE				R/W1TC	R/W1TC
0h	0h	0h				0h	0h
23	22	21	20	19	18	17	16
RST_SRC_DS_MAIN_PORZ_PROXY	RST_SRC_DM_WDT_RST_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE			R/W1TC
0h	0h	0h	0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R/W1TC	R/W1TC	NONE			R/W1TC
0h		0h	0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST_PROXY	RESERVED	RST_SRC_MAIN_RESET_REQ_PROXY	RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE			R/W1TC	NONE	R/W1TC	NONE	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-9943. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R/W1TC	0h	Reset Caused by MCU ESM Error Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R/W1TC	0h	Reset Caused by Main ESM Error Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	R/W1TC	0h	Software Main Power On Reset From MAIN CTRL MMR Reset Source: mod_por_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY	R/W1TC	0h	Software Main Power On Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
23	RST_SRC_DS_MAIN_PORZ_PROXY	R/W1TC	0h	Reset of Main/Wkup Domains while in Deep Sleep, as a result of an MCU Warm Reset Reset Source: mod_por_rst_n

Table 14-9943. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RST_SRC_DM_WDT_RST_PROXY	R/W1TC	0h	Watchdog Initiated Reset Reset Source: mod_por_rst_n
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	R/W1TC	0h	Software Main Warm Reset from MAIN CTRL MMR Reset Source: mod_por_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	R/W1TC	0h	Software Main Warm Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R/W1TC	0h	Software Warm Reset Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST_PROXY	R/W1TC	0h	SMS Warm Reset Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R/W1TC	0h	SMS Cold Reset Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R/W1TC	0h	Debug Subsystem Initiated Reset Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R/W1TC	0h	Thermal Reset Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ_PROXY	R/W1TC	0h	Main Reset Pin Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R/W1TC	0h	Rest Caused by MCU Reset Pin Reset Source: mod_por_rst_n

14.2.1.1.2.2.278 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register (Offset = 1A17Ch) [reset = 0h]

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Table 14-9944. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A17Ch**

Figure 14-3306. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9946. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY	R/W	0h	After a MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any reset from the Main Domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it shall leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the MCU R5FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from any warm reset sources that triggers main_resetz, the value must be non-zero. If the value is nonzero and a Main domain warm reset that triggers main_resetz occurs in the main domain, the MCU R5FSS will not be reset. The Main domain bootloader must read this value to determine that the MCU R5FSS is already initialized, and has configured reset isolation. The Main domain bootloader then also skips any initialization steps involving bootstrapping the R5FSS (as it is is already running). Note that MCU_PORz reset is never blocked by a nonzero magic word. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.279 MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register (Offset = 1A180h) [reset = 0h]

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Table 14-9947. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A180h**

Figure 14-3307. MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ISO_CTRL_MCU_DBG_ISO_EN_PROXY	ISO_CTRL_MCU_RST_ISO_EN_PROXY
NONE						R/W	R/W
0h						0h	0h

Table 14-9949. MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	ISO_CTRL_MCU_DBG_ISO_EN_PROXY	R/W	0h	Isolates the MCU domain from Debug Field values (others are reserved): undefined - undefined undefined - undefined 1'b0 - R5FSS is not debug isolated 1'b1 - R5FSS is isolated from debug if RST_MAGIC_WORD is also nonzero Reset Source: mcu_chip1_rst_n
0	ISO_CTRL_MCU_RST_ISO_EN_PROXY	R/W	0h	Isolates the MCU domain from Warm Reset initiated by Main Field values (others are reserved): undefined - undefined undefined - undefined 1'b0 - R5FSS is not reset isolated 1'b1 - R5FSS is isolated from main warm reset if RST_MAGIC_WORD is also nonzero Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.280 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register (Offset = 1A190h) [reset = 0h]

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Table 14-9950. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A190h**

Figure 14-3308. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>VDD_CORE_GLDTC_CTRL_PWDB_PROXY</td><td>VDD_CORE_GLDTC_CTRL_RSTB_PROXY</td><td colspan="6">RESERVED</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">X</td></tr>
</table>

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB_PROXY	R/W	0h	Power down - active low. 0 - Deactivate all functions 1 - Activate glitch detectors Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB_PROXY	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0 - Reset glitch detector flags 1 - Glitch detection flags are activated Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY	R/W	X	Selects the glitch detect low-pass filter bandwidth Field values (others are reserved): 3'b000 - 150 kHz 3'b001 - 125 kHz 3'b010 - 100 kHz 3'b011 - 80 kHz 3'b100 - 60 kHz 3'b101 - 45 kHz 3'b110 - 30 kHz 3'b111 - 15 kHz Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - 93.5% of VDD 6'b000001 - 94.0% of VDD 6'b000010 - 94.5% of VDD 6'b000011 - 95.0% of VDD 6'b000100 - 95.5% of VDD 6'b000101 - 96.0% of VDD 6'b000110 - 96.5% of VDD 6'b000111 - 97.0% of VDD 6'b001000 - 97.5% of VDD 6'b001001 - 98.0% of VDD 6'b001010 - 98.5% of VDD 6'b001011 - 99.0% of VDD 6'b001100 - 99.5% of VDD 6'b001101 - 100.0% of VDD 6'b001110 - 100.5% of VDD 6'b001111 - 101.0% of VDD 6'b010000 - 101.5% of VDD 6'b010001 - 102.0% of VDD 6'b010010 - 102.5% of VDD 6'b010011 - 103.0% of VDD 6'b010100 - 103.5% of VDD 6'b010101 - 104.0% of VDD 6'b010110 - 104.5% of VDD 6'b010111 - 105.0% of VDD 6'b011000 - 105.5% of VDD 6'b011001 - 106.0% of VDD 6'b011010 - 106.5% of VDD 6'b011011 - 107.0% of VDD 6'b011100 - 107.5% of VDD 6'b011101 - 108.0% of VDD 6'b011110 - 108.5% of VDD 6'b011111 - 109.0% of VDD 6'b100000 - 109.5% of VDD 6'b100001 - 110.0% of VDD 6'b100010 - 111.0% of VDD 6'b100011 - 112.0% of VDD 6'b100100 - 113.0% of VDD 6'b100101 - 114.0% of VDD 6'b100110 - 115.0% of VDD 6'b100111 - 116.0% of VDD 6'b101000 - 117.0% of VDD 6'b101001 - 118.0% of VDD 6'b101010 - 119.0% of VDD 6'b101011 - 120.0% of VDD 6'b101100 - 121.0% of VDD 6'b101101 - 122.0% of VDD 6'b101110 - 123.0% of VDD 6'b101111 - 124.0% of VDD 6'b110000 - 125.0% of VDD 6'b110001 - 126.0% of VDD 6'b110010 - 127.0% of VDD 6'b110011 - 128.0% of VDD 6'b110100 - 129.0% of VDD 6'b110101 - 130.0% of VDD 6'b110110 - 131.0% of VDD 6'b110111 - 132.0% of VDD 6'b111000 - 133.0% of VDD 6'b111001 - 134.0% of VDD 6'b111010 - 135.0% of VDD 6'b111011 - 136.0% of VDD 6'b111100 - 137.0% of VDD

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111101 - 138.0% of VDD 6'b111110 - 139.0% of VDD 6'b111111 - 140.0% of VDD Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - 106.5% of VDD 6'b000001 - 106.0% of VDD 6'b000010 - 105.5% of VDD 6'b000011 - 105.0% of VDD 6'b000100 - 104.5% of VDD 6'b000101 - 104.0% of VDD 6'b000110 - 103.5% of VDD 6'b000111 - 103.0% of VDD 6'b001000 - 102.5% of VDD 6'b001001 - 102.0% of VDD 6'b001010 - 101.5% of VDD 6'b001011 - 101.0% of VDD 6'b001100 - 100.5% of VDD 6'b001101 - 100.0% of VDD 6'b001110 - 99.5% of VDD 6'b001111 - 99.0% of VDD 6'b010000 - 98.5% of VDD 6'b010001 - 98.0% of VDD 6'b010010 - 97.5% of VDD 6'b010011 - 97.0% of VDD 6'b010100 - 96.5% of VDD 6'b010101 - 96.0% of VDD 6'b010110 - 95.5% of VDD 6'b010111 - 95.0% of VDD 6'b011000 - 94.5% of VDD 6'b011001 - 94.0% of VDD 6'b011010 - 93.5% of VDD 6'b011011 - 93.0% of VDD 6'b011100 - 92.5% of VDD 6'b011101 - 92.0% of VDD 6'b011110 - 91.5% of VDD 6'b011111 - 91.0% of VDD 6'b100000 - 90.5% of VDD 6'b100001 - 90.0% of VDD 6'b100010 - 89.0% of VDD 6'b100011 - 88.0% of VDD 6'b100100 - 87.0% of VDD 6'b100101 - 86.0% of VDD 6'b100110 - 85.0% of VDD 6'b100111 - 84.0% of VDD 6'b101000 - 83.0% of VDD 6'b101001 - 82.0% of VDD 6'b101010 - 81.0% of VDD 6'b101011 - 80.0% of VDD 6'b101100 - 79.0% of VDD 6'b101101 - 78.0% of VDD 6'b101110 - 77.0% of VDD 6'b101111 - 76.0% of VDD 6'b110000 - 75.0% of VDD 6'b110001 - 74.0% of VDD 6'b110010 - 73.0% of VDD 6'b110011 - 72.0% of VDD 6'b110100 - 71.0% of VDD 6'b110101 - 70.0% of VDD 6'b110110 - 69.0% of VDD 6'b110111 - 68.0% of VDD 6'b111000 - 67.0% of VDD 6'b111001 - 66.0% of VDD 6'b111010 - 65.0% of VDD 6'b111011 - 64.0% of VDD 6'b111100 - 63.0% of VDD

Table 14-9952. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				6'b111101 - 62.0% of VDD 6'b111110 - 61.0% of VDD 6'b111111 - 60.0% of VDD Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.281 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register (Offset = 1A1B0h) [reset = 0h]

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Table 14-9953. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A1B0h**

Figure 14-3309. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY
NONE							R
0h							X

Table 14-9955. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0 - No high voltage detected 1 - Voltage above the high voltage threshold was detected. Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0 - No low voltage detected 1 - Voltage below the low voltage threshold was detected. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.282 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register (Offset = 1A200h) [reset = 2001Fh]

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Table 14-9956. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A200h**

Figure 14-3310. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-9958. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP0 POKs: 2'b00 - 5 us 2'b01 -10 us 2'b10 - 15 us 2'b11 - 20us Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL_PROXY	R/W	0h	Select POK activate source 0 - POK activates come from hardware tie-offs 1 - POK activates come from PRG_PP0_CTRL register Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	R/W	1h	Activate VDDA_PMIC_IN undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n

Table 14-9958. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	R/W	1h	Activate VDD_MCU overvoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	R/W	1h	Activate VDD_MCU undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	R/W	1h	Activate 1.8V VDDA_MCU overvoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n
0	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY	R/W	1h	Activate 1.8V VDDA_MCU undervoltage POK detection 0 - POK detection deactivated 1 - POK detection activated Reset Source: mod_por_rst_n

14.2.1.1.2.2.283 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register (Offset = 1A208h) [reset = 2007Fh]

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Table 14-9959. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A208h**

Figure 14-3311. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PRG_PP_1_CTRL_POK_PP_EN_PROXY	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	
15	14	13	12	11	10	9	8
PRG_PP_1_CTRL_POK_EN_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY	RSVD	RSVD	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY
R/W	R/W	R/W	R/W	R/W			R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY	RSVD	RSVD	PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY
NONE	R/W	R/W	R/W	R/W			R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-9961. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN_PROXY	R/W	0h	POK ping-pong activate. When set, activatesautomatic switching between undervoltage andovervoltage detection on PRG_PP1 (POK_VDDR_CORE, POK_VDDSHV_MCU_1P8, POK_VDDSHV_MCU_3P3, POK_VMON_CAP_MCU_GENERAL, POK_VDDSHV_MAIN_1P8, POK_VDDSHV_MAIN_3P3, and POK_VDDS_DDRIO) POKs. This bit has no effect if the POK's ov_sel bit = 1. 0 - No pingpong operation. UV/OV operationselected by each POK ov_sel bit 1 - Pingpong operation activated . Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved

Table 14-9961. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP1 POKs: 2'b00 - 5 us 2'b01 -10 us 2'b10 - 15 us 2'b11 - 20us Reset Source: mod_por_rst_n
15	PRG_PP_1_CTRL_POK_EN_SEL_PROXY	R/W	0h	Select POK activate source 0 - POK activates come from hardware tie-offs 1 - POK activates come from PRG_PP1_CTRL register Reset Source: mod_por_rst_n
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	R/W	0h	POK_VDDS_DDRIO mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_3P3 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_1P8 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY	R/W	0h	POK_VDDR_CORE Mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x) Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	R/W	1h	Activate POK_VDDS_DDRIO (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	R/W	1h	Activate POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	R/W	1h	Activate POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY	R/W	1h	Activate POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n

Table 14-9961. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY	R/W	1h	Activate POK_VDDR_CORE (if pok_en_sel = 1): 0 = POK Detection Deactivated 1 = POK Detection Activated Reset Source: mod_por_rst_n

14.2.1.1.2.2.284 MCU_CTRL_MMR_CFG0_CLKGATE_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_CLKGATE_CTRL_PROXY Register (Offset = 1A280h) [reset = 0h]

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Table 14-9962. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A280h**

Figure 14-3312. MCU_CTRL_MMR_CFG0_CLKGATE_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKGATE_CTRL_MCUSS_NOGATE_PROXY	CLKGATE_CTRL_MCU_CBA_NOGATE_PROXY	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE_PROXY
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-9964. MCU_CTRL_MMR_CFG0_CLKGATE_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CLKGATE_CTRL_MCUSS_NOGATE_PROXY	R/W	0h	MCU Subsystem clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
1	CLKGATE_CTRL_MCU_CBA_NOGATE_PROXY	R/W	0h	MCU domain Data bus (mcu_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
0	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE_PROXY	R/W	0h	WKUP domain Infrastructure bus (wkup_safe_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.2.2.285 MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-9965. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B008h**

Figure 14-3313. MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-9967. MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.286 MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-9968. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B00Ch**

Figure 14-3314. MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK6_KICK1_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK6_KICK1_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-9970. MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.287 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9971. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B100h**

Figure 14-3315. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-9973. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.288 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9974. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B104h**

Figure 14-3316. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-9976. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.289 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9977. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B108h**

Figure 14-3317. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-9979. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.290 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-9980. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B10Ch**

Figure 14-3318. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-9982. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.291 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9983. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B110h**

Figure 14-3319. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-9985. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.292 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-9986. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B114h**

Figure 14-3320. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5							
R/W							
0h							

Table 14-9988. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3 WKUP_CTRL_MMR

WKUP_CTRL_MMR

14.2.1.1.3.1 WKUP_CTRL_MMR Summaries

WKUP_CTRL_MMR Summaries

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
0h	32	WKUP_CTRL_MMR_CFG0_PID	4300 0000h
8h	32	WKUP_CTRL_MMR_CFG0_MMR_CFG1	4300 0008h
14h	32	WKUP_CTRL_MMR_CFG0_JTAGID	4300 0014h
18h	32	WKUP_CTRL_MMR_CFG0_JTAG_USER_ID	4300 0018h
30h	32	WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT	4300 0030h
34h	32	WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG	4300 0034h
44h	32	WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS	4300 0044h
60h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0	4300 0060h
64h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1	4300 0064h
68h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2	4300 0068h
6Ch	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3	4300 006Ch
78h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6	4300 0078h
200h	32	WKUP_CTRL_MMR_CFG0_MAC_ID0	4300 0200h
204h	32	WKUP_CTRL_MMR_CFG0_MAC_ID1	4300 0204h
220h	32	WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0	4300 0220h
230h	32	WKUP_CTRL_MMR_CFG0_GP_SW0	4300 0230h
234h	32	WKUP_CTRL_MMR_CFG0_GP_SW1	4300 0234h
238h	32	WKUP_CTRL_MMR_CFG0_GP_SW2	4300 0238h
23Ch	32	WKUP_CTRL_MMR_CFG0_GP_SW3	4300 023Ch
270h	32	WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT	4300 0270h
280h	32	WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT	4300 0280h
1008h	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK0	4300 1008h
100Ch	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK1	4300 100Ch
1010h	32	WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS	4300 1010h
1014h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	4300 1014h
1018h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE	4300 1018h
101Ch	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	4300 101Ch
1020h	32	WKUP_CTRL_MMR_CFG0_EOI	4300 1020h
1024h	32	WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS	4300 1024h
1028h	32	WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	4300 1028h
102Ch	32	WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	4300 102Ch
1030h	32	WKUP_CTRL_MMR_CFG0_FAULT_CLEAR	4300 1030h
1100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	4300 1100h
1104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY	4300 1104h
1108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY	4300 1108h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
110Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY	4300 110Ch
1110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY	4300 1110h
1114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY	4300 1114h
1118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY	4300 1118h
2000h	32	WKUP_CTRL_MMR_CFG0_PID_PROXY	4300 2000h
2008h	32	WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY	4300 2008h
2014h	32	WKUP_CTRL_MMR_CFG0_JTAGID_PROXY	4300 2014h
2018h	32	WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY	4300 2018h
2030h	32	WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY	4300 2030h
2034h	32	WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY	4300 2034h
2044h	32	WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY	4300 2044h
2060h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY	4300 2060h
2064h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY	4300 2064h
2068h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY	4300 2068h
206Ch	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY	4300 206Ch
2078h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY	4300 2078h
2200h	32	WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY	4300 2200h
2204h	32	WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY	4300 2204h
2220h	32	WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY	4300 2220h
2230h	32	WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY	4300 2230h
2234h	32	WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY	4300 2234h
2238h	32	WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY	4300 2238h
223Ch	32	WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY	4300 223Ch
2270h	32	WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY	4300 2270h
2280h	32	WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY	4300 2280h
3008h	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	4300 3008h
300Ch	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	4300 300Ch
3010h	32	WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	4300 3010h
3014h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	4300 3014h
3018h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	4300 3018h
301Ch	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	4300 301Ch
3020h	32	WKUP_CTRL_MMR_CFG0_EOI_PROXY	4300 3020h
3024h	32	WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	4300 3024h
3028h	32	WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	4300 3028h
302Ch	32	WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	4300 302Ch
3030h	32	WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	4300 3030h
3100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0	4300 3100h
3104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1	4300 3104h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
3108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2	4300 3108h
310Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3	4300 310Ch
3110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4	4300 3110h
3114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5	4300 3114h
3118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6	4300 3118h
4008h	32	WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL	4300 4008h
4018h	32	WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL	4300 4018h
41B4h	32	WKUP_CTRL_MMR_CFG0_SDIO0_CTRL	4300 41B4h
41B8h	32	WKUP_CTRL_MMR_CFG0_SDIO1_CTRL	4300 41B8h
41BCh	32	WKUP_CTRL_MMR_CFG0_SDIO2_CTRL	4300 41BCh
4204h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL	4300 4204h
42E0h	32	WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL	4300 42E0h
4610h	32	WKUP_CTRL_MMR_CFG0_TOG_STAT	4300 4610h
5008h	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK0	4300 5008h
500Ch	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK1	4300 500Ch
5100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	4300 5100h
5104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	4300 5104h
5108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	4300 5108h
510Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	4300 510Ch
5110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	4300 5110h
5114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	4300 5114h
5118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	4300 5118h
511Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY	4300 511Ch
5120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	4300 5120h
5124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	4300 5124h
5128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY	4300 5128h
512Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY	4300 512Ch
5130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	4300 5130h
6008h	32	WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY	4300 6008h
6018h	32	WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY	4300 6018h
61B4h	32	WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY	4300 61B4h
61B8h	32	WKUP_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY	4300 61B8h
61BCh	32	WKUP_CTRL_MMR_CFG0_SDIO2_CTRL_PROXY	4300 61BCh
6204h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY	4300 6204h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
62E0h	32	WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY	4300 62E0h
6610h	32	WKUP_CTRL_MMR_CFG0_TOG_STAT_PROXY	4300 6610h
7008h	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	4300 7008h
700Ch	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	4300 700Ch
7100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0	4300 7100h
7104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1	4300 7104h
7108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2	4300 7108h
710Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3	4300 710Ch
7110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4	4300 7110h
7114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5	4300 7114h
7118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6	4300 7118h
711Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7	4300 711Ch
7120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8	4300 7120h
7124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9	4300 7124h
7128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10	4300 7128h
712Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11	4300 712Ch
7130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12	4300 7130h
8010h	32	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL	4300 8010h
8020h	32	WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL	4300 8020h
8030h	32	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL	4300 8030h
803Ch	32	WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL	4300 803Ch
80D0h	32	WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL	4300 80D0h
8190h	32	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL	4300 8190h
8194h	32	WKUP_CTRL_MMR_CFG0_USB1_CLKSEL	4300 8194h
81B0h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL	4300 81B0h
81B4h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL	4300 81B4h
8340h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL	4300 8340h
8380h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL	4300 8380h
8600h	32	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL	4300 8600h
9008h	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK0	4300 9008h
900Ch	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK1	4300 900Ch
9100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	4300 9100h
9104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	4300 9104h
9108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY	4300 9108h
910Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY	4300 910Ch
9110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY	4300 9110h
9114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY	4300 9114h
9118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY	4300 9118h
911Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY	4300 911Ch

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
9120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY	4300 9120h
9124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY	4300 9124h
9128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY	4300 9128h
912Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11_READONLY	4300 912Ch
9130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY	4300 9130h
A010h	32	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY	4300 A010h
A020h	32	WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY	4300 A020h
A030h	32	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY	4300 A030h
A03Ch	32	WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY	4300 A03Ch
A0D0h	32	WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY	4300 A0D0h
A190h	32	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY	4300 A190h
A194h	32	WKUP_CTRL_MMR_CFG0_USB1_CLKSEL_PROXY	4300 A194h
A1B0h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY	4300 A1B0h
A1B4h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY	4300 A1B4h
A340h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY	4300 A340h
A380h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY	4300 A380h
A600h	32	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY	4300 A600h
B008h	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	4300 B008h
B00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	4300 B00Ch
B100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0	4300 B100h
B104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1	4300 B104h
B108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2	4300 B108h
B10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3	4300 B10Ch
B110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4	4300 B110h
B114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5	4300 B114h
B118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6	4300 B118h
B11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7	4300 B11Ch
B120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8	4300 B120h
B124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9	4300 B124h
B128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10	4300 B128h
B12Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11	4300 B12Ch
B130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12	4300 B130h
C320h	32	WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT	4300 C320h
C340h	32	WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT	4300 C340h
C400h	32	WKUP_CTRL_MMR_CFG0_PBIST_EN	4300 C400h
D008h	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK0	4300 D008h
D00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK1	4300 D00Ch

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
D100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	4300 D100h
D104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY	4300 D104h
D108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY	4300 D108h
D10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY	4300 D10Ch
D110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY	4300 D110h
D114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY	4300 D114h
D118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY	4300 D118h
D11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY	4300 D11Ch
D120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY	4300 D120h
E320h	32	WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY	4300 E320h
E340h	32	WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY	4300 E340h
E400h	32	WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY	4300 E400h
F008h	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	4300 F008h
F00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	4300 F00Ch
F100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0	4300 F100h
F104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1	4300 F104h
F108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2	4300 F108h
F10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3	4300 F10Ch
F110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4	4300 F110h
F114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5	4300 F114h
F118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6	4300 F118h
F11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7	4300 F11Ch
F120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8	4300 F120h
11008h	32	WKUP_CTRL_MMR_CFG0_LOCK4_KICK0	4301 1008h
1100Ch	32	WKUP_CTRL_MMR_CFG0_LOCK4_KICK1	4301 100Ch
11100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	4301 1100h
11104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY	4301 1104h
11108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY	4301 1108h
1110Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY	4301 110Ch
11110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY	4301 1110h
11114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY	4301 1114h
11118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY	4301 1118h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
1111Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY	4301 111Ch
11120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	4301 1120h
13008h	32	WKUP_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY	4301 3008h
1300Ch	32	WKUP_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY	4301 300Ch
13100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0	4301 3100h
13104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1	4301 3104h
13108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2	4301 3108h
1310Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3	4301 310Ch
13110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4	4301 3110h
13114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5	4301 3114h
13118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6	4301 3118h
1311Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7	4301 311Ch
13120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8	4301 3120h
14000h	32	WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ	4301 4000h
14004h	32	WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK	4301 4004h
14080h	32	WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ	4301 4080h
140C0h	32	WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK	4301 40C0h
15008h	32	WKUP_CTRL_MMR_CFG0_LOCK5_KICK0	4301 5008h
1500Ch	32	WKUP_CTRL_MMR_CFG0_LOCK5_KICK1	4301 500Ch
15100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY	4301 5100h
15104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY	4301 5104h
16000h	32	WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY	4301 6000h
16004h	32	WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY	4301 6004h
16080h	32	WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY	4301 6080h
160C0h	32	WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY	4301 60C0h
17008h	32	WKUP_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY	4301 7008h
1700Ch	32	WKUP_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY	4301 700Ch
17100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0	4301 7100h
17104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1	4301 7104h
18040h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0	4301 8040h
18044h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET	4301 8044h
18048h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR	4301 8048h
1804Ch	32	WKUP_CTRL_MMR_CFG0_FW_STS_IN0	4301 804Ch
18050h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1	4301 8050h
18054h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET	4301 8054h
18058h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR	4301 8058h
1805Ch	32	WKUP_CTRL_MMR_CFG0_FW_STS_IN1	4301 805Ch
18080h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_SYS	4301 8080h
18084h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0	4301 8084h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
18088h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1	4301 8088h
18090h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC	4301 8090h
18098h	32	WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS	4301 8098h
1809Ch	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB	4301 809Ch
180A0h	32	WKUP_CTRL_MMR_CFG0_PM_PERMISSION	4301 80A0h
18160h	32	WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL	4301 8160h
18170h	32	WKUP_CTRL_MMR_CFG0_RST_CTRL	4301 8170h
18174h	32	WKUP_CTRL_MMR_CFG0_RST_STAT	4301 8174h
18178h	32	WKUP_CTRL_MMR_CFG0_RST_SRC	4301 8178h
1817Ch	32	WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD	4301 817Ch
18180h	32	WKUP_CTRL_MMR_CFG0_WKUP0_EN	4301 8180h
18280h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0	4301 8280h
18284h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1	4301 8284h
18300h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL	4301 8300h
18308h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0	4301 8308h
1830Ch	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1	4301 830Ch
18310h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE	4301 8310h
18318h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT	4301 8318h
18320h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_J	4301 8320h + formula
18340h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_J	4301 8340h + formula
18400h	32	WKUP_CTRL_MMR_CFG0_WFI_STATUS	4301 8400h
18410h	32	WKUP_CTRL_MMR_CFG0_SLEEP_STATUS	4301 8410h
18418h	32	WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD	4301 8418h
18420h	32	WKUP_CTRL_MMR_CFG0_DS_MAIN	4301 8420h
18440h	32	WKUP_CTRL_MMR_CFG0_DS_DM_RESET	4301 8440h
18460h	32	WKUP_CTRL_MMR_CFG0_DS_USB0_RESET	4301 8460h
18464h	32	WKUP_CTRL_MMR_CFG0_DS_USB1_RESET	4301 8464h
18480h	32	WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN	4301 8480h
18490h	32	WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK	4301 8490h
184A0h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ	4301 84A0h
184A4h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK	4301 84A4h
18500h	32	WKUP_CTRL_MMR_CFG0_DEVICE_TYPE	4301 8500h
19008h	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK0	4301 9008h
1900Ch	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK1	4301 900Ch
19100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	4301 9100h
19104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	4301 9104h
19108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	4301 9108h
1910Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY	4301 910Ch

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
19110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY	4301 9110h
19114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY	4301 9114h
19118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY	4301 9118h
1911Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY	4301 911Ch
19120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY	4301 9120h
19124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY	4301 9124h
19128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY	4301 9128h
1A040h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_PROXY	4301 A040h
1A044h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET_PROXY	4301 A044h
1A048h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR_PROXY	4301 A048h
1A04Ch	32	WKUP_CTRL_MMR_CFG0_FW_STS_IN0_PROXY	4301 A04Ch
1A050h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_PROXY	4301 A050h
1A054h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET_PROXY	4301 A054h
1A058h	32	WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR_PROXY	4301 A058h
1A05Ch	32	WKUP_CTRL_MMR_CFG0_FW_STS_IN1_PROXY	4301 A05Ch
1A080h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY	4301 A080h
1A084h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY	4301 A084h
1A088h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY	4301 A088h
1A090h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY	4301 A090h
1A098h	32	WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY	4301 A098h
1A09Ch	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB_PROXY	4301 A09Ch
1A0A0h	32	WKUP_CTRL_MMR_CFG0_PM_PERMISSION_PROXY	4301 A0A0h
1A160h	32	WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL_PROXY	4301 A160h
1A170h	32	WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY	4301 A170h
1A174h	32	WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY	4301 A174h
1A178h	32	WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY	4301 A178h
1A17Ch	32	WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY	4301 A17Ch
1A180h	32	WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY	4301 A180h
1A280h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY	4301 A280h
1A284h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY	4301 A284h
1A300h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY	4301 A300h
1A308h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY	4301 A308h
1A30Ch	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY	4301 A30Ch
1A310h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY	4301 A310h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
1A318h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY	4301 A318h
1A320h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_J	4301 A320h + formula
1A340h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_J	4301 A340h + formula
1A400h	32	WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY	4301 A400h
1A410h	32	WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY	4301 A410h
1A418h	32	WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD_PROXY	4301 A418h
1A420h	32	WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY	4301 A420h
1A440h	32	WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY	4301 A440h
1A460h	32	WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY	4301 A460h
1A464h	32	WKUP_CTRL_MMR_CFG0_DS_USB1_RESET_PROXY	4301 A464h
1A480h	32	WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY	4301 A480h
1A490h	32	WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY	4301 A490h
1A4A0h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY	4301 A4A0h
1A4A4h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK_PROXY	4301 A4A4h
1A500h	32	WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY	4301 A500h
1B008h	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	4301 B008h
1B00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	4301 B00Ch
1B100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0	4301 B100h
1B104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1	4301 B104h
1B108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2	4301 B108h
1B10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3	4301 B10Ch
1B110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4	4301 B110h
1B114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5	4301 B114h
1B118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6	4301 B118h
1B11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7	4301 B11Ch
1B120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8	4301 B120h
1B124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9	4301 B124h
1B128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10	4301 B128h
1C100h	32	WKUP_CTRL_MMR_CFG0_BACKUP_REG_J	4301 C100h + formula
1D008h	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK0	4301 D008h
1D00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK1	4301 D00Ch
1D100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY	4301 D100h
1D104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY	4301 D104h
1D108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY	4301 D108h
1E100h	32	WKUP_CTRL_MMR_CFG0_BACKUP_REG_PROXY_J	4301 E100h + formula
1F008h	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY	4301 F008h
1F00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY	4301 F00Ch
1F100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0	4301 F100h
1F104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1	4301 F104h

Table 14-9989. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
1F108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2	4301 F108h

14.2.1.1.3.2 WKUP_CTRL_MMR Registers

WKUP_CTRL_MMR Registers

14.2.1.1.3.2.1 WKUP_CTRL_MMR_CFG0_PID Register

1 WKUP_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-9990. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0000h**

Figure 14-3321. WKUP_CTRL_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-9992. WKUP_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.2 WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register

1 WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000FFh]

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Table 14-9993. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0008h**

Figure 14-3322. WKUP_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
FFh							

Table 14-9995. WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	FFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.3.2.3 WKUP_CTRL_MMR_CFG0_JTAGID Register

1 WKUP_CTRL_MMR_CFG0_JTAGID Register (Offset = 14h) [reset = BB8D02Fh]

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Table 14-9996. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0014h**

Figure 14-3323. WKUP_CTRL_MMR_CFG0_JTAGID Name Register

31	30	29	28	27	26	25	24
JTAGID_VARIANT				JTAGID_PARTNO			
R				R			
0h				BB8Dh			
23	22	21	20	19	18	17	16
JTAGID_PARTNO							
R							
BB8Dh							
15	14	13	12	11	10	9	8
JTAGID_PARTNO				JTAGID_MFG			
R				R			
BB8Dh				17h			
7	6	5	4	3	2	1	0
JTAGID_MFG							JTAGID_LSB
R							R
17h							1h

Table 14-9998. WKUP_CTRL_MMR_CFG0_JTAGID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	JTAGID_VARIANT	R	0h	Used to indicate new PGs Reset Source: mod_por_rst_n 0 `AM62D SR1.0`
27:12	JTAGID_PARTNO	R	BB8Dh	Part number for boundary scan Reset Source: mod_por_rst_n
11:1	JTAGID_MFG	R	17h	Indicates manufacturer Reset Source: mod_por_rst_n
0	JTAGID_LSB	R	1h	Always 1 Reset Source: mod_por_rst_n

14.2.1.1.3.2.4 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register

1 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register (Offset = 18h) [reset = 0h]

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Table 14-9999. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0018h**

Figure 14-3324. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Name Register

31	30	29	28	27	26	25	24
DEVICE_ID							
R							
0h							
23	22	21	20	19	18	17	16
DEVICE_ID							
R							
0h							
15	14	13	12	11	10	9	8
DEVICE_ID			SAFETY	SECURITY	SPEED		
R			R	R	R		
0h			0h	0h	0h		
7	6	5	4	3	2	1	0
SPEED		TEMP			PKG		
R		R			R		
0h		0h			X		

Table 14-10001. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	DEVICE_ID	R	0h	Refer to the Device Comparison table in the device specific datasheet for the combined DEVICE_ID and FEATURES value of a given part number.
12	SAFETY	R	0h	`0 Non-Functional Safety` `1 Functional Safety`
11	SECURITY	R	0h	`0 Non-Secure` `1 Secure`

10:6	SPEED	R	0h	Refer to the device-specific Datasheet for the supported speed grades and the definitions for a given device.
				`16 P Speed Designator`
				`18 R Speed Designator`
				`20 V Speed Designator`
				`OTHER Reserved`

5:3	TEMP	R	0h	Operating junction temperature range.
				`4 -40°C to 105°C`
				`5 -40°C to 125°C`
				`OTHER Reserved`

Table 14-10001. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2:0	PKG	R	X	Device information
				Reset Source: mod_por_rst_n
				`6      ANF`
				`OTHER  Reserved`

14.2.1.1.3.2.5 WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT Register

1 WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT Register (Offset = 30h) [reset = 0h]

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Table 14-10002. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0030h**

Figure 14-3325. WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_DEVSTAT_BOOTMODE							
R/W							
0h							
7	6	5	4	3	2	1	0
MAIN_DEVSTAT_BOOTMODE							
R/W							
0h							

Table 14-10004. WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_DEVSTAT_BOOTMODE	R/W	0h	Specifies the device Primary and Backup boot media. Reset Source: mod_por_rst_n

14.2.1.1.3.2.6 WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG Register

1 WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG Register (Offset = 34h) [reset = 0h]

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Table 14-10005. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0034h**

Figure 14-3326. WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_BOOTCFG_BOOTMODE							
R							
0h							
7	6	5	4	3	2	1	0
MAIN_BOOTCFG_BOOTMODE							
R							
0h							

Table 14-10007. WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_BOOTCFG_BOOTMODE	R	0h	Specifies the device Primary and Backup boot media as latched at PORz Reset Source: mod_por_rst_n

14.2.1.1.3.2.7 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register

1 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register (Offset = 44h) [reset = 0h]

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Table 14-10008. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0044h**

Figure 14-3327. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Name Register

31	30	29	28	27	26	25	24
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
BOOT_PROGRESS_PROGRESS							
R/W							
0h							

Table 14-10010. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.3.2.8 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register (Offset = 60h) [reset = 0h]

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Table 14-10011. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0060h**

Figure 14-3328. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>DEVICE_FEATURE0_MPU_CLUSTER0_CORE3</td><td>DEVICE_FEATURE0_MPU_CLUSTER0_CORE2</td><td>DEVICE_FEATURE0_MPU_CLUSTER0_CORE1</td><td>DEVICE_FEATURE0_MPU_CLUSTER0_CORE0</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>

Table 14-10013. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	DEVICE_FEATURE0_MPU_CLUSTER0_CORE3	R	X	MPU Cluster0 Core 3 is activated when set Reset Source: mod_por_rst_n
2	DEVICE_FEATURE0_MPU_CLUSTER0_CORE2	R	X	MPU Cluster0 Core 2 is activated when set Reset Source: mod_por_rst_n
1	DEVICE_FEATURE0_MPU_CLUSTER0_CORE1	R	X	MPU Cluster0 Core 1 is activated when set Reset Source: mod_por_rst_n
0	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0	R	X	MPU Cluster0 Core 0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.9 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register (Offset = 64h) [reset = 0h]

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Table 14-10014. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0064h**

Figure 14-3329. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DEVICE_FEATURE1_C7X_CORE_EN
NONE							R
0h							X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVICE_FEATURE1_VID_ENCODER_AVC_DECODE_EN	DEVICE_FEATURE1_VID_ENCODER_AVC_ENCODE_EN	DEVICE_FEATURE1_VID_ENCODER_HEVC_DECODE_EN	DEVICE_FEATURE1_VID_ENCODER_HEVC_ENCODE_EN	DEVICE_FEATURE1_VID_ENCODER_EN	DEVICE_FEATURE1_JPEG_ENC_EN	RESERVED	DEVICE_FEATURE1_VPAC0_EN
R	R	R	R	R	R	NONE	R
X	X	X	X	X	X	0h	X

Table 14-10016. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DEVICE_FEATURE1_C7X_CORE_EN	R	X	C7x is activated when set Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	DEVICE_FEATURE1_VID_ENCODER_AVC_DECODE_EN	R	X	Video CODEC HEVC decode feature activated when set Reset Source: mod_por_rst_n
6	DEVICE_FEATURE1_VID_ENCODER_AVC_ENCODE_EN	R	X	Video CODEC HEVC encode feature activated when set Reset Source: mod_por_rst_n
5	DEVICE_FEATURE1_VID_ENCODER_HEVC_DECODE_EN	R	X	Video CODEC AVC decode feature activated when set Reset Source: mod_por_rst_n
4	DEVICE_FEATURE1_VID_ENCODER_HEVC_ENCODE_EN	R	X	Video CODEC AVC encode feature activated when set Reset Source: mod_por_rst_n
3	DEVICE_FEATURE1_VID_ENCODER_EN	R	X	Video CODEC is activated when set Reset Source: mod_por_rst_n

Table 14-10016. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DEVICE_FEATURE1_JPEG_ENC_EN	R	X	JPEG Encoder is activated when set Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE1_VPAC0_EN	R	X	VPAC0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.10 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register (Offset = 68h) [reset = 0h]

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Table 14-10017. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0068h

Figure 14-3330. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				DEVICE_FEATURE2_CRYPTO_SM_EN	DEVICE_FEATURE2_CRYPTO_PKA_EN	DEVICE_FEATURE2_CRYPTO_ENCR_EN	DEVICE_FEATURE2_CRYPTO_SHA_EN
NONE				R	R	R	R
0h				X	X	X	X
7	6	5	4	3	2	1	0
DEVICE_FEATURE2_AES_AUTH_EN	RESERVED						DEVICE_FEATURE2_MCAN_FD_MODE
R	NONE						R
X	0h						X

Table 14-10019. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	DEVICE_FEATURE2_CRYPTO_SM_EN	R	X	SA3SS Crypto Module SM2, SM3, SM4 activated Reset Source: mod_por_rst_n
10	DEVICE_FEATURE2_CRYPTO_PKA_EN	R	X	SA3SS Crypto Module PKA activated Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN	R	X	SA3SS Crypto Module AES/3DES/DBRG activated Reset Source: mod_por_rst_n
8	DEVICE_FEATURE2_CRYPTO_SHA_EN	R	X	SA3SS Crypto Module SHA/MD5 activated Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN	R	X	AES authentication is activated in FlashSS and SMS when set Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE	R	X	FD mode is supported on all MCAN when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.11 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register (Offset = 6Ch) [reset = 0h]

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Table 14-10020. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 006Ch**

Figure 14-3331. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DEVICE_FEATURE3_VPAC_FEATURE_DIS1	DEVICE_FEATURE3_VPAC_FEATURE_DIS0	RESERVED			DEVICE_FEATURE3_MMA_PRESENT
NONE		R	R	NONE			R
0h		X	X	0h			X

Table 14-10022. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	DEVICE_FEATURE3_VPAC_FEATURE_DIS1	R	X	VPAC Feature 1 Deactivated When Set Reset Source: mod_por_rst_n
4	DEVICE_FEATURE3_VPAC_FEATURE_DIS0	R	X	VPAC Feature 0 DIsabled When Set Reset Source: mod_por_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE3_MMA_PRESENT	R	X	C7x MMA Present when Set Reset Source: mod_por_rst_n

14.2.1.1.3.2.12 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register (Offset = 78h) [reset = 0h]

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Table 14-10023. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0078h**

Figure 14-3332. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td>RSVD</td><td>RSVD</td><td>RSVD</td></tr>
<tr><td colspan="5">NONE</td><td></td><td></td><td></td></tr>
<tr><td colspan="5">0h</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>DEVICE_FEATURE6_SPARE1</td><td>DEVICE_FEATURE6_SPARE0</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>DEVICE_FEATURE6_SA3_UL</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td colspan="5">NONE</td></tr>
<tr><td colspan="2">0h</td><td>X</td><td colspan="5">0h</td></tr>
</table>

Table 14-10025. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
23:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE6_SPARE1	R	X	Spare1 LPSC is activated when set Reset Source: mod_por_rst_n
16	DEVICE_FEATURE6_SPARE0	R	X	Spare0 LPSC is activated when set Reset Source: mod_por_rst_n
15:6	RESERVED	NONE	0h	Reserved
5	DEVICE_FEATURE6_SA3_UL	R	X	SA3SS domain security accelerator is activated when set Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.13 WKUP_CTRL_MMR_CFG0_MAC_ID0 Register

1 WKUP_CTRL_MMR_CFG0_MAC_ID0 Register (Offset = 200h) [reset = 0h]

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Table 14-10026. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0200h**

Figure 14-3333. WKUP_CTRL_MMR_CFG0_MAC_ID0 Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO							
R/W							
X							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO							
R/W							
X							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO							
R/W							
X							

Table 14-10028. WKUP_CTRL_MMR_CFG0_MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO	R/W	X	32 lsbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.3.2.14 WKUP_CTRL_MMR_CFG0_MAC_ID1 Register

1 WKUP_CTRL_MMR_CFG0_MAC_ID1 Register (Offset = 204h) [reset = 0h]

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Table 14-10029. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0204h**

Figure 14-3334. WKUP_CTRL_MMR_CFG0_MAC_ID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI							
R/W							
X							

Table 14-10031. WKUP_CTRL_MMR_CFG0_MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI	R/W	X	16 msbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.3.2.15 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register

1 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register (Offset = 220h) [reset = 61650451h]

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Table 14-10032. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0220h**

Figure 14-3335. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0							
R/W							
61650451h							

Table 14-10034. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0	R/W	61650451h	ROM writes 32-bit Value from Customer OTP to Here Reset Source: mod_g_rst_n

14.2.1.1.3.2.16 WKUP_CTRL_MMR_CFG0_GP_SW0 Register

1 WKUP_CTRL_MMR_CFG0_GP_SW0 Register (Offset = 230h) [reset = 0h]

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Table 14-10035. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0230h**

Figure 14-3336. WKUP_CTRL_MMR_CFG0_GP_SW0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-10037. WKUP_CTRL_MMR_CFG0_GP_SW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.17 WKUP_CTRL_MMR_CFG0_GP_SW1 Register

1 WKUP_CTRL_MMR_CFG0_GP_SW1 Register (Offset = 234h) [reset = 0h]

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Table 14-10038. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0234h

Figure 14-3337. WKUP_CTRL_MMR_CFG0_GP_SW1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-10040. WKUP_CTRL_MMR_CFG0_GP_SW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.18 WKUP_CTRL_MMR_CFG0_GP_SW2 Register

1 WKUP_CTRL_MMR_CFG0_GP_SW2 Register (Offset = 238h) [reset = 0h]

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Table 14-10041. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0238h**

Figure 14-3338. WKUP_CTRL_MMR_CFG0_GP_SW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-10043. WKUP_CTRL_MMR_CFG0_GP_SW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.19 WKUP_CTRL_MMR_CFG0_GP_SW3 Register

1 WKUP_CTRL_MMR_CFG0_GP_SW3 Register (Offset = 23Ch) [reset = 0h]

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Table 14-10044. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 023Ch**

Figure 14-3339. WKUP_CTRL_MMR_CFG0_GP_SW3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
NONE				R			
0h				X			

Table 14-10046. WKUP_CTRL_MMR_CFG0_GP_SW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.20 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register

1 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register (Offset = 270h) [reset = 0h]

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Table 14-10047. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0270h**

Figure 14-3340. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Name Register

31	30	29	28	27	26	25	24
CBA_ERR_STAT_DBG_CBA_ERR	RESERVED					CBA_ERR_STAT_WKUP_DM_CBA_ERR	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR
R	NONE					R	R
X	0h					X	X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			CBA_ERR_STAT_MCU_CBA_ERR	RESERVED			
NONE			R	NONE			
0h			X	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR	CBA_ERR_STAT_MAIN_MCASP_CBA_ERR	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR	RESERVED		
NONE		R	R	R	NONE		
0h		X	X	X	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CBA_ERR_STAT_MAIN_FW_CBA_ERR	CBA_ERR_STAT_MAIN_DATA_CBA_ERR	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR	RESERVED		CBA_ERR_STAT_MAIN_INFRA_CBA_ERR
NONE		R	R	R	NONE		R
0h		X	X	X	0h		X

Table 14-10049. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR	R	X	Access Error from Main Debug CBASS Reset Source: mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	CBA_ERR_STAT_WKUP_DM_CBA_ERR	R	X	Access Error from Wkup Device Manager CBASS Reset Source: mod_g_rst_n
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR	R	X	Access Error from Wkup Safe CBASS Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	CBA_ERR_STAT_MCU_CBA_ERR	R	X	Access Error from MCU CBASS Reset Source: mod_g_rst_n
19:14	RESERVED	NONE	0h	Reserved

Table 14-10049. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR	R	X	Access Error from Main IPCSS CBASS Reset Source: mod_g_rst_n
12	CBA_ERR_STAT_MAIN_MCASP_CBA_ERR	R	X	Access Error from Main McASP CBASS Reset Source: mod_g_rst_n
11	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR	R	X	Access Errror from Main Misc. Peripheral CBASS Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CBA_ERR_STAT_MAIN_FW_CBA_ERR	R	X	Access Error from Main Firewall CBASS Reset Source: mod_g_rst_n
4	CBA_ERR_STAT_MAIN_DATA_CBA_ERR	R	X	Access Error from Main Data CBASS Reset Source: mod_g_rst_n
3	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR	R	X	Access Error from Main Central CBASS Reset Source: mod_g_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR	R	X	Access Error from Main Infrastructure CBASS Reset Source: mod_g_rst_n

14.2.1.1.3.2.21 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register

1 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register (Offset = 280h) [reset = 0h]

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Table 14-10050. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 0280h**

Figure 14-3341. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN9</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN8</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN4</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN3</td><td colspan="2">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN0</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td>R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>X</td><td>X</td><td colspan="2">0h</td><td>X</td></tr>
</table>

Table 14-10052. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9	R	X	Access Error Detected in MCU PadCfg MMR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8	R	X	Access Error Detected in MCU Ctrl MMR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4	R	X	Access Error Detected in MAIN PadCfg MMR Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3	R	X	Access Error Detected in MAIN Ctrl MMR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0	R	X	Access Error Detected in WKUP Ctrl MMR Reset Source: mod_por_rst_n

14.2.1.1.3.2.22 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-10053. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1008h**

Figure 14-3342. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-10055. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.23 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-10056. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 100Ch**

Figure 14-3343. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-10058. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.24 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-10059. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1010h**

Figure 14-3344. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-10061. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.25 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-10062. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1014h**

Figure 14-3345. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-10064. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.26 WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-10065. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1018h**

Figure 14-3346. WKUP_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-10067. WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.27 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-10068. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 101Ch**

Figure 14-3347. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-10070. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.28 WKUP_CTRL_MMR_CFG0_EOI Register

1 WKUP_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-10071. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1020h**

Figure 14-3348. WKUP_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-10073. WKUP_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.3.2.29 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-10074. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1024h**

Figure 14-3349. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-10076. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.3.2.30 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-10077. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1028h**

Figure 14-3350. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-10079. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.3.2.31 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-10080. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 102Ch**

Figure 14-3351. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-10082. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.3.2.32 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-10083. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1030h**

Figure 14-3352. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-10085. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.33 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10086. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1100h**

Figure 14-3353. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-10088. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.34 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register (Offset = 1104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10089. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1104h**

Figure 14-3354. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1_READONLY							
R							
0h							

Table 14-10091. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.35 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10092. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1108h**

Figure 14-3355. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2_READONLY							
R							
0h							

Table 14-10094. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.36 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-10095. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 110Ch**

Figure 14-3356. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3_READONLY							
R							
0h							

Table 14-10097. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.37 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10098. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1110h**

Figure 14-3357. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4_READONLY							
R							
0h							

Table 14-10100. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.38 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10101. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1114h**

Figure 14-3358. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-10103. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.39 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register (Offset = 1118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10104. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 1118h**

Figure 14-3359. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P0_R6_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P0_R6_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P0_R6_READONLY							
R							
0h							

Table 14-10106. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.40 WKUP_CTRL_MMR_CFG0_PID_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-10107. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2000h**

Figure 14-3360. WKUP_CTRL_MMR_CFG0_PID_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC_PROXY</td><td colspan="3">PID_MAJOR_PROXY</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM_PROXY</td><td colspan="6">PID_MINOR_PROXY</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-10109. WKUP_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.41 WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000FFh]

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Table 14-10110. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2008h**

Figure 14-3361. WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
FFh							

Table 14-10112. WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	FFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.3.2.42 WKUP_CTRL_MMR_CFG0_JTAGID_PROXY Register

1 WKUP_CTRL_MMR_CFG0_JTAGID_PROXY Register (Offset = 2014h) [reset = BB8D02Fh]

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Table 14-10113. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2014h**

Figure 14-3362. WKUP_CTRL_MMR_CFG0_JTAGID_PROXY Name Register

31	30	29	28	27	26	25	24
JTAGID_VARIANT_PROXY				JTAGID_PARTNO_PROXY			
R				R			
0h				BB8Dh			
23	22	21	20	19	18	17	16
JTAGID_PARTNO_PROXY							
R							
BB8Dh							
15	14	13	12	11	10	9	8
JTAGID_PARTNO_PROXY				JTAGID_MFG_PROXY			
R				R			
BB8Dh				17h			
7	6	5	4	3	2	1	0
JTAGID_MFG_PROXY							JTAGID_LSB_PROXY
R							R
17h							1h

Table 14-10115. WKUP_CTRL_MMR_CFG0_JTAGID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	JTAGID_VARIANT_PROXY	R	0h	Used to indicate new PGs Reset Source: mod_por_rst_n
27:12	JTAGID_PARTNO_PROXY	R	BB8Dh	Part number for boundary scan Reset Source: mod_por_rst_n
11:1	JTAGID_MFG_PROXY	R	17h	Indicates manufacturer Reset Source: mod_por_rst_n
0	JTAGID_LSB_PROXY	R	1h	Always 1 Reset Source: mod_por_rst_n

14.2.1.1.3.2.43 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register

1 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register (Offset = 2018h) [reset = 0h]

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Table 14-10116. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2018h**

Figure 14-3363. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Name Register

31	30	29	28	27	26	25	24
DEVICE_ID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DEVICE_ID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DEVICE_ID			SAFETY	SECURITY	SPEED		
R			R	R	R		
0h			0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED		TEMP			PKG		
R		R			R		
0h		0h			X		

Table 14-10118. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	DEVICE_ID	R	0h	Refer to the Device Comparison table in the device specific datasheet for the combined DEVICE_ID and FEATURES value of a given part number.
12	SAFETY	R	0h	0 Non-Functional Safety 1 Functional Safety
11	SECURITY	R	0h	0 Non-Secure 1 Secure
10:6	SPEED	R	0h	Refer to the device-specific Datasheet for the supported speed grades and the definitions for a given device. 16 P Speed Designator 18 R Speed Designator 20 V Speed Designator OTHER Reserved
5:3	TEMP	R	0h	Operating junction temperature range. 4 -40°C to 105°C 5 -40°C to 125°C OTHER Reserved

Table 14-10118. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2:0	PKG	R	X	Device information
				Reset Source: mod_por_rst_n
				`6      ANF`
				`OTHER  Reserved`

14.2.1.1.3.2.44 WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register (Offset = 2030h) [reset = 0h]

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Table 14-10119. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2030h**

Figure 14-3364. WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_DEVSTAT_BOOTMODE_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MAIN_DEVSTAT_BOOTMODE_PROXY							
R/W							
0h							

Table 14-10121. WKUP_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_DEVSTAT_BOOTMODE_PROXY	R/W	0h	Specifies the device Primary and Backup boot media. Reset Source: mod_por_rst_n

14.2.1.1.3.2.45 WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register

1 WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register (Offset = 2034h) [reset = 0h]

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Table 14-10122. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2034h**

Figure 14-3365. WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_BOOTCFG_BOOTMODE_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
MAIN_BOOTCFG_BOOTMODE_PROXY							
R							
0h							

Table 14-10124. WKUP_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_BOOTCFG_BOOTMODE_PROXY	R	0h	Specifies the device Primary and Backup boot media as latched at PORz Reset Source: mod_por_rst_n

14.2.1.1.3.2.46 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register (Offset = 2044h) [reset = 0h]

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Table 14-10125. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2044h**

Figure 14-3366. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Name Register

31	30	29	28	27	26	25	24
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							

Table 14-10127. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS_PROXY	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.3.2.47 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register (Offset = 2060h) [reset = 0h]

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Table 14-10128. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2060h**

Figure 14-3367. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DEVICE_FEATURE0_MPU_CLUSTER0_CORE3_PROXY	DEVICE_FEATURE0_MPU_CLUSTER0_CORE2_PROXY	DEVICE_FEATURE0_MPU_CLUSTER0_CORE1_PROXY	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0_PROXY
NONE				R	R	R	R
0h				X	X	X	X

Table 14-10130. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	DEVICE_FEATURE0_MPU_CLUSTER0_CORE3_PROXY	R	X	MPU Cluster0 Core 3 is activated when set Reset Source: mod_por_rst_n
2	DEVICE_FEATURE0_MPU_CLUSTER0_CORE2_PROXY	R	X	MPU Cluster0 Core 2 is activated when set Reset Source: mod_por_rst_n
1	DEVICE_FEATURE0_MPU_CLUSTER0_CORE1_PROXY	R	X	MPU Cluster0 Core 1 is activated when set Reset Source: mod_por_rst_n
0	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0_PROXY	R	X	MPU Cluster0 Core 0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.48 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register (Offset = 2064h) [reset = 0h]

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Table 14-10131. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2064h**

Figure 14-3368. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							DEVICE_FEATURE1_C7X_CORE_EN_PROXY
NONE							R
0h							X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEVICE_FEATURE1_VID_ENCODER_AVC_DECODE_EN_PROXY	DEVICE_FEATURE1_VID_ENCODER_AVC_ENCODE_EN_PROXY	DEVICE_FEATURE1_VID_ENCODER_HEVC_DECODE_EN_PROXY	DEVICE_FEATURE1_VID_ENCODER_HEVC_ENCODE_EN_PROXY	DEVICE_FEATURE1_VID_ENCODER_EN_PROXY	DEVICE_FEATURE1_JPEG_ENC_EN_PROXY	RESERVED	DEVICE_FEATURE1_VPAC0_EN_PROXY
R	R	R	R	R	R	NONE	R
X	X	X	X	X	X	0h	X

Table 14-10133. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DEVICE_FEATURE1_C7X_CORE_EN_PROXY	R	X	C7x is activated when set Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	DEVICE_FEATURE1_VID_ENCODER_AVC_DECODE_EN_PROXY	R	X	Video CODEC HEVC decode feature activated when set Reset Source: mod_por_rst_n
6	DEVICE_FEATURE1_VID_ENCODER_AVC_ENCODE_EN_PROXY	R	X	Video CODEC HEVC encode feature activated when set Reset Source: mod_por_rst_n
5	DEVICE_FEATURE1_VID_ENCODER_HEVC_DECODE_EN_PROXY	R	X	Video CODEC AVC decode feature activated when set Reset Source: mod_por_rst_n
4	DEVICE_FEATURE1_VID_ENCODER_HEVC_ENCODE_EN_PROXY	R	X	Video CODEC AVC encode feature activated when set Reset Source: mod_por_rst_n

Table 14-10133. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DEVICE_FEATURE1_VID_ENCODER_EN_PROXY	R	X	Video CODEC is activated when set Reset Source: mod_por_rst_n
2	DEVICE_FEATURE1_JPEG_ENC_EN_PROXY	R	X	JPEG Encoder is activated when set Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE1_VPAC0_EN_PROXY	R	X	VPAC0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.49 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register (Offset = 2068h) [reset = 0h]

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Table 14-10134. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2068h**

Figure 14-3369. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED				DEVICE_FEATURE2_CRYPTO_SM_EN_PROXY	DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY
NONE				R	R	R	R
0h				X	X	X	X

7	6	5	4	3	2	1	0
DEVICE_FEATURE2_AES_AUTH_EN_PROXY	RESERVED						DEVICE_FEATURE2_MCAN_FD_MODE_PROXY
R	NONE						R
X	0h						X

Table 14-10136. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	DEVICE_FEATURE2_CRYPTO_SM_EN_PROXY	R	X	SA3SS Crypto Module SM2, SM3, SM4 activated Reset Source: mod_por_rst_n
10	DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	R	X	SA3SS Crypto Module PKA activated Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	R	X	SA3SS Crypto Module AES/3DES/DBRG activated Reset Source: mod_por_rst_n
8	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY	R	X	SA3SS Crypto Module SHA/MD5 activated Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN_PROXY	R	X	AES authentication is activated in FlashSS and SMS when set Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE_PROXY	R	X	FD mode is supported on all MCAN when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.50 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register (Offset = 206Ch) [reset = 0h]

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Table 14-10137. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 206Ch**

Figure 14-3370. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DEVICE_FEATURE3_VPAC_FEATURE_DIS1_PROXY	DEVICE_FEATURE3_VPAC_FEATURE_DIS0_PROXY	RESERVED			DEVICE_FEATURE3_MMA_PRESENT_PROXY
NONE		R	R	NONE			R
0h		X	X	0h			X

Table 14-10139. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	DEVICE_FEATURE3_VPAC_FEATURE_DIS1_PROXY	R	X	VPAC Feature 1 Deactivated When Set Reset Source: mod_por_rst_n
4	DEVICE_FEATURE3_VPAC_FEATURE_DIS0_PROXY	R	X	VPAC Feature 0 DIsabled When Set Reset Source: mod_por_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE3_MMA_PRESENT_PROXY	R	X	C7x MMA Present when Set Reset Source: mod_por_rst_n

14.2.1.1.3.2.51 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register (Offset = 2078h) [reset = 0h]

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Table 14-10140. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2078h**

Figure 14-3371. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED					RSVD	RSVD	RSVD
NONE							
0h					X	X	X
23	22	21	20	19	18	17	16
RESERVED						DEVICE_FEATURE6_SPARE1_PROXY	DEVICE_FEATURE6_SPARE0_PROXY
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DEVICE_FEATURE6_SA3_UL_PROXY	RESERVED				
NONE		R	NONE				
0h		X	0h				

Table 14-10142. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
23:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE6_SPARE1_PROXY	R	X	Spare1 LPSC is activated when set Reset Source: mod_por_rst_n
16	DEVICE_FEATURE6_SPARE0_PROXY	R	X	Spare0 LPSC is activated when set Reset Source: mod_por_rst_n
15:6	RESERVED	NONE	0h	Reserved
5	DEVICE_FEATURE6_SA3_UL_PROXY	R	X	SA3SS domain security accelerator is activated when set Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.52 WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register (Offset = 2200h) [reset = 0h]

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Table 14-10143. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2200h**

Figure 14-3372. WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO_PROXY							
R/W							
X							

Table 14-10145. WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO_PROXY	R/W	X	32 lsbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.3.2.53 WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register (Offset = 2204h) [reset = 0h]

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Table 14-10146. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2204h**

Figure 14-3373. WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI_PROXY							
R/W							
X							

Table 14-10148. WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI_PROXY	R/W	X	16 msbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.3.2.54 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register (Offset = 2220h) [reset = 61650451h]

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Table 14-10149. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2220h**

Figure 14-3374. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							

Table 14-10151. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0_PROXY	R/W	61650451h	ROM writes 32-bit Value from Customer OTP to Here Reset Source: mod_g_rst_n

14.2.1.1.3.2.55 WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register (Offset = 2230h) [reset = 0h]

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Table 14-10152. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2230h**

Figure 14-3375. WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-10154. WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.56 WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register (Offset = 2234h) [reset = 0h]

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Table 14-10155. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2234h**

Figure 14-3376. WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-10157. WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.57 WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register

1 WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register (Offset = 2238h) [reset = 0h]

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Table 14-10158. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2238h**

Figure 14-3377. WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-10160. WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.58 WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register

1 WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register (Offset = 223Ch) [reset = 0h]

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Table 14-10161. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 223Ch**

Figure 14-3378. WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
NONE				R			
0h				X			

Table 14-10163. WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	RESERVED	R	X	Reserved

14.2.1.1.3.2.59 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register (Offset = 2270h) [reset = 0h]

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Table 14-10164. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2270h**

Figure 14-3379. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
CBA_ERR_STAT_DBG_CBA_ERR_PROXY	RESERVED					CBA_ERR_STAT_WKUP_DM_CBA_ERR_PROXY	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY
R	NONE					R	R
X	0h					X	X

23	22	21	20	19	18	17	16
RESERVED			CBA_ERR_STAT_MCU_CBA_ERR_PROXY	RESERVED			
NONE			R	NONE			
0h			X	0h			

15	14	13	12	11	10	9	8
RESERVED		CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_MCASP_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR_PROXY	RESERVED		
NONE		R	R	R	NONE		
0h		X	X	X	0h		

7	6	5	4	3	2	1	0
RESERVED		CBA_ERR_STAT_MAIN_FW_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_DATA_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR_PROXY	RESERVED		CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY
NONE		R	R	R	NONE		R
0h		X	X	X	0h		X

Table 14-10166. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR_PROXY	R	X	Access Error from Main Debug CBASS Reset Source: mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	CBA_ERR_STAT_WKUP_DM_CBA_ERR_PROXY	R	X	Access Error from Wkup Device Manager CBASS Reset Source: mod_g_rst_n
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY	R	X	Access Error from Wkup Safe CBASS Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	CBA_ERR_STAT_MCU_CBA_ERR_PROXY	R	X	Access Error from MCU CBASS Reset Source: mod_g_rst_n
19:14	RESERVED	NONE	0h	Reserved

Table 14-10166. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR_PROXY	R	X	Access Error from Main IPCSS CBASS Reset Source: mod_g_rst_n
12	CBA_ERR_STAT_MAIN_MCASP_CBA_ERR_PROXY	R	X	Access Error from Main McASP CBASS Reset Source: mod_g_rst_n
11	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR_PROXY	R	X	Access Errror from Main Misc. Peripheral CBASS Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CBA_ERR_STAT_MAIN_FW_CBA_ERR_PROXY	R	X	Access Error from Main Firewall CBASS Reset Source: mod_g_rst_n
4	CBA_ERR_STAT_MAIN_DATA_CBA_ERR_PROXY	R	X	Access Error from Main Data CBASS Reset Source: mod_g_rst_n
3	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR_PROXY	R	X	Access Error from Main Central CBASS Reset Source: mod_g_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY	R	X	Access Error from Main Infrastructure CBASS Reset Source: mod_g_rst_n

14.2.1.1.3.2.60 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register (Offset = 2280h) [reset = 0h]

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Table 14-10167. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 2280h**

Figure 14-3380. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY
NONE						R	R
0h						X	X
7	6	5	4	3	2	1	0
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY
NONE			R	R	NONE		R
0h			X	X	0h		X

Table 14-10169. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	R	X	Access Error Detected in MCU PadCfg MMR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY	R	X	Access Error Detected in MCU Ctrl MMR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	R	X	Access Error Detected in MAIN PadCfg MMR Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	R	X	Access Error Detected in MAIN Ctrl MMR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY	R	X	Access Error Detected in WKUP Ctrl MMR Reset Source: mod_por_rst_n

14.2.1.1.3.2.61 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-10170. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3008h**

Figure 14-3381. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-10172. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.62 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-10173. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 300Ch**

Figure 14-3382. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-10175. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.63 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-10176. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3010h**

Figure 14-3383. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-10178. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.64 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-10179. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3014h**

Figure 14-3384. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>ENABLED_PROXY_ERR_PROXY</td><td>ENABLED_KICK_ERR_PROXY</td><td>ENABLED_ADDR_ERR_PROXY</td><td>ENABLED_PROT_ERR_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10181. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.65 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-10182. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3018h**

Figure 14-3385. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-10184. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.66 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-10185. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 301Ch**

Figure 14-3386. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-10187. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.67 WKUP_CTRL_MMR_CFG0_EOI_PROXY Register

1 WKUP_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-10188. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3020h**

Figure 14-3387. WKUP_CTRL_MMR_CFG0_EOI_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10190. WKUP_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.3.2.68 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-10191. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3024h**

Figure 14-3388. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-10193. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.3.2.69 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-10194. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3028h**

Figure 14-3389. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-10196. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.3.2.70 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-10197. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 302Ch**

Figure 14-3390. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-10199. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.3.2.71 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-10200. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3030h**

Figure 14-3391. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-10202. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.72 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10203. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3100h**

Figure 14-3392. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10205. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.73 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10206. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3104h**

Figure 14-3393. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-10208. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.74 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10209. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3108h**

Figure 14-3394. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-10211. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.75 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-10212. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 310Ch**

Figure 14-3395. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-10214. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.76 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10215. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3110h**

Figure 14-3396. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10217. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.77 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10218. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3114h**

Figure 14-3397. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-10220. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.78 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register (Offset = 3118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-10221. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 3118h**

Figure 14-3398. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6							
R/W							
0h							

Table 14-10223. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.79 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register

1 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register (Offset = 4008h) [reset = 80000004h]

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Table 14-10224. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 4008h**

Figure 14-3399. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Name Register

31	30	29	28	27	26	25	24
USB0_PHY_CTRL_CORE_VOLTAGE	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL			
NONE				R/W			
0h				4h			

Table 14-10226. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB0_PHY_CTRL_CORE_VOLTAGE	R/W	1h	Selects the USB PHY Core Voltage 0 - Core Voltage is 0.85V 1 - Core Voltage is 0.75V/0.80V Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-10226. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB0_PHY_CTRL_PLL_REF_SEL	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB0 input clock, as selected by the USB0_CLKSEL register Field values (others are reserved): 4'b0000 - 9.6 MHz 4'b0001 - 10 MHz 4'b0010 - 12 MHz 4'b0011 - 19.2 MHZ 4'b0100 - 20 MHz 4'b0101 - 24 MHz 4'b0110 - 25 MHz 4'b0111 - 26 MHz 4'b1000 - 38.4 MHz 4'b1001 - 40 MHz 4'b1010 - 48 MHz 4'b1011 - 50 MHz 4'b1100 - 52 MHz Reset Source: mod_g_rst_n

14.2.1.1.3.2.80 WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL Register

1 WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL Register (Offset = 4018h) [reset = 80000004h]

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Table 14-10227. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 4018h**

Figure 14-3400. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL Name Register

31	30	29	28	27	26	25	24
USB1_PHY_CTRL_CORE_VOLTAGE	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				USB1_PHY_CTRL_PLL_REF_SEL			
NONE				R/W			
0h				4h			

Table 14-10229. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB1_PHY_CTRL_CORE_VOLTAGE	R/W	1h	Selects the USB PHY Core Voltage 0 - Core Voltage is 0.85V 1 - Core Voltage is 0.75V/0.80V Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-10229. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB1_PHY_CTRL_PLL_REF_SEL	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB1 input clock, as selected by the USB1_CLKSEL register Field values (others are reserved): 4'b0000 - 9.6 MHz 4'b0001 - 10 MHz 4'b0010 - 12 MHz 4'b0011 - 19.2 MHZ 4'b0100 - 20 MHz 4'b0101 - 24 MHz 4'b0110 - 25 MHz 4'b0111 - 26 MHz 4'b1000 - 38.4 MHz 4'b1001 - 40 MHz 4'b1010 - 48 MHz 4'b1011 - 50 MHz 4'b1100 - 52 MHz Reset Source: mod_g_rst_n

14.2.1.1.3.2.81 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register

1 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register (Offset = 41B4h) [reset = 0h]

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Table 14-10230. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 41B4h**

Figure 14-3401. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SDIO0_CTRL_DRV_STR				
NONE			R/W				
0h			X				

Table 14-10232. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO0_CTRL_DRV_STR	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.82 WKUP_CTRL_MMR_CFG0_SDIO1_CTRL Register

1 WKUP_CTRL_MMR_CFG0_SDIO1_CTRL Register (Offset = 41B8h) [reset = 0h]

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Table 14-10233. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 41B8h**

Figure 14-3402. WKUP_CTRL_MMR_CFG0_SDIO1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO1_CTRL_DRV_STR				
NONE			R/W				
0h			X				

Table 14-10235. WKUP_CTRL_MMR_CFG0_SDIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO1_CTRL_DRV_STR	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.83 WKUP_CTRL_MMR_CFG0_SDIO2_CTRL Register

1 WKUP_CTRL_MMR_CFG0_SDIO2_CTRL Register (Offset = 41BCh) [reset = 0h]

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Table 14-10236. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 41BCh**

Figure 14-3403. WKUP_CTRL_MMR_CFG0_SDIO2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO2_CTRL_DRV_STR				
NONE			R/W				
0h			X				

Table 14-10238. WKUP_CTRL_MMR_CFG0_SDIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO2_CTRL_DRV_STR	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.84 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

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Table 14-10239. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 4204h**

Figure 14-3404. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WKUP_TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-10241. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WKUP_TIMER1_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.85 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

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Table 14-10242. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 42E0h**

Figure 14-3405. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_I2C0_CTRL_HS_MCS_EN
NONE							R/W
0h							0h

Table 14-10244. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_I2C0_CTRL_HS_MCS_EN	R/W	0h	HS Mode controller current source activate. When set, activates the current-source pull-up on the SCL output. Only one controller on the I2C bus should activate SCL current sourcing. Reset Source: mod_g_rst_n

14.2.1.1.3.2.86 WKUP_CTRL_MMR_CFG0_TOG_STAT Register

1 WKUP_CTRL_MMR_CFG0_TOG_STAT Register (Offset = 4610h) [reset = 0h]

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Table 14-10245. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 4610h**

Figure 14-3406. WKUP_CTRL_MMR_CFG0_TOG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOG_STAT_SLV_TOG_STAT	RESERVED						
R	NONE						
X	0h						
7	6	5	4	3	2	1	0
RESERVED						TOG_STAT_MST_TOG_STAT	
NONE						R	
0h						X	

Table 14-10247. WKUP_CTRL_MMR_CFG0_TOG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TOG_STAT_SLV_TOG_STAT	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 1'b0 - No Error 1'b1 - Error from mcu2dm timeout gasket MCU_TIMEOUT0 Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 2'b00 - No Error 2'b01 - Error from dm2mcu WKUP_TIMEOUT1 gasket 2'b10 - Error from dm2ws WKUP_TIMEOUT0 gasket 2'b11 - Error from both dm2mcu and dm2ws WKUP_TIMEOUT1 and WKUP_TIMEOUT0 gaskets Reset Source: mod_g_rst_n

14.2.1.1.3.2.87 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-10248. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5008h**

Figure 14-3407. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-10250. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.88 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-10251. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 500Ch**

Figure 14-3408. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-10253. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.89 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10254. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5100h**

Figure 14-3409. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-10256. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.90 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10257. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5104h**

Figure 14-3410. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-10259. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.91 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10260. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5108h**

Figure 14-3411. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-10262. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.92 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10263. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 510Ch**

Figure 14-3412. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-10265. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.93 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10266. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5110h**

Figure 14-3413. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-10268. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.94 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10269. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5114h**

Figure 14-3414. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10271. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.95 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10272. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5118h**

Figure 14-3415. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-10274. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.96 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register (Offset = 511Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10275. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 511Ch**

Figure 14-3416. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7_READONLY							
R							
0h							

Table 14-10277. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.97 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10278. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5120h**

Figure 14-3417. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-10280. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.98 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10281. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5124h**

Figure 14-3418. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-10283. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.99 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register (Offset = 5128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10284. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5128h**

Figure 14-3419. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10_READONLY							
R							
0h							

Table 14-10286. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.100 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register (Offset = 512Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10287. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 512Ch**

Figure 14-3420. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11_READONLY							
R							
0h							

Table 14-10289. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.101 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10290. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 5130h**

Figure 14-3421. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10292. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.102 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register (Offset = 6008h) [reset = 80000004h]

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Table 14-10293. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 6008h**

Figure 14-3422. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
USB0_PHY_CTRL_CORE_VOLTAGE_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL_PROXY			
NONE				R/W			
0h				4h			

Table 14-10295. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB0_PHY_CTRL_CORE_VOLTAGE_PROXY	R/W	1h	Selects the USB PHY Core Voltage 0 - Core Voltage is 0.85V 1 - Core Voltage is 0.75V/0.80V Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-10295. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB0_PHY_CTRL_PLL_REF_SEL_PROXY	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB0 input clock, as selected by the USB0_CLKSEL register Field values (others are reserved): 4'b0000 - 9.6 MHz 4'b0001 - 10 MHz 4'b0010 - 12 MHz 4'b0011 - 19.2 MHZ 4'b0100 - 20 MHz 4'b0101 - 24 MHz 4'b0110 - 25 MHz 4'b0111 - 26 MHz 4'b1000 - 38.4 MHz 4'b1001 - 40 MHz 4'b1010 - 48 MHz 4'b1011 - 50 MHz 4'b1100 - 52 MHz Reset Source: mod_g_rst_n

14.2.1.1.3.2.103 WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY Register (Offset = 6018h) [reset = 80000004h]

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Table 14-10296. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 6018h**

Figure 14-3423. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
USB1_PHY_CTRL_CORE_VOLTAGE_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				USB1_PHY_CTRL_PLL_REF_SEL_PROXY			
NONE				R/W			
0h				4h			

Table 14-10298. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB1_PHY_CTRL_CORE_VOLTAGE_PROXY	R/W	1h	Selects the USB PHY Core Voltage 0 - Core Voltage is 0.85V 1 - Core Voltage is 0.75V/0.80V Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-10298. WKUP_CTRL_MMR_CFG0_USB1_PHY_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB1_PHY_CTRL_PLL_REF_SEL_PROXY	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB1 input clock, as selected by the USB1_CLKSEL register Field values (others are reserved): 4'b0000 - 9.6 MHz 4'b0001 - 10 MHz 4'b0010 - 12 MHz 4'b0011 - 19.2 MHZ 4'b0100 - 20 MHz 4'b0101 - 24 MHz 4'b0110 - 25 MHz 4'b0111 - 26 MHz 4'b1000 - 38.4 MHz 4'b1001 - 40 MHz 4'b1010 - 48 MHz 4'b1011 - 50 MHz 4'b1100 - 52 MHz Reset Source: mod_g_rst_n

14.2.1.1.3.2.104 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register (Offset = 61B4h) [reset = 0h]

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Table 14-10299. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 61B4h**

Figure 14-3424. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO0_CTRL_DRV_STR_PROXY				
NONE			R/W				
0h			X				

Table 14-10301. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO0_CTRL_DRV_STR_PROXY	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.105 WKUP_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register (Offset = 61B8h) [reset = 0h]

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Table 14-10302. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 61B8h**

Figure 14-3425. WKUP_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO1_CTRL_DRV_STR_PROXY				
NONE			R/W				
0h			X				

Table 14-10304. WKUP_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO1_CTRL_DRV_STR_PROXY	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.106 WKUP_CTRL_MMR_CFG0_SDIO2_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_SDIO2_CTRL_PROXY Register (Offset = 61BCh) [reset = 0h]

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Table 14-10305. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 61BCh**

Figure 14-3426. WKUP_CTRL_MMR_CFG0_SDIO2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO2_CTRL_DRV_STR_PROXY				
NONE			R/W				
0h			X				

Table 14-10307. WKUP_CTRL_MMR_CFG0_SDIO2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO2_CTRL_DRV_STR_PROXY	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.107 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

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Table 14-10308. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 6204h**

Figure 14-3427. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WKUP_TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-10310. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WKUP_TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.108 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register (Offset = 62E0h) [reset = 0h]

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Table 14-10311. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 62E0h**

Figure 14-3428. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_I2C0_CTRL_HS_MCS_EN_PROXY
NONE							R/W
0h							0h

Table 14-10313. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_I2C0_CTRL_HS_MCS_EN_PROXY	R/W	0h	HS Mode controller current source activate. When set, activates the current-source pull-up on the SCL output. Only one controller on the I2C bus should activate SCL current sourcing. Reset Source: mod_g_rst_n

14.2.1.1.3.2.109 WKUP_CTRL_MMR_CFG0_TOG_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_TOG_STAT_PROXY Register (Offset = 6610h) [reset = 0h]

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Table 14-10314. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 6610h**

Figure 14-3429. WKUP_CTRL_MMR_CFG0_TOG_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOG_STAT_SLV_TOG_STAT_PROXY	RESERVED						
R	NONE						
X	0h						
7	6	5	4	3	2	1	0
RESERVED						TOG_STAT_MST_TOG_STAT_PROXY	
NONE						R	
0h						X	

Table 14-10316. WKUP_CTRL_MMR_CFG0_TOG_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TOG_STAT_SLV_TOG_STAT_PROXY	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 1'b0 - No Error 1'b1 - Error from mcu2dm timeout gasket MCU_TIMEOUT0 Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT_PROXY	R	X	Error Status of Target Timeout Gaskets Field values (others are reserved): 2'b00 - No Error 2'b01 - Error from dm2mcu WKUP_TIMEOUT1 gasket 2'b10 - Error from dm2ws WKUP_TIMEOUT0 gasket 2'b11 - Error from both dm2mcu and dm2ws WKUP_TIMEOUT1 and WKUP_TIMEOUT0 gaskets Reset Source: mod_g_rst_n

14.2.1.1.3.2.110 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-10317. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7008h**

Figure 14-3430. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-10319. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.111 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-10320. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 700Ch**

Figure 14-3431. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-10322. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.112 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10323. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7100h**

Figure 14-3432. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-10325. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.113 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10326. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7104h**

Figure 14-3433. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-10328. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.114 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10329. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7108h**

Figure 14-3434. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-10331. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.115 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10332. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 710Ch**

Figure 14-3435. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-10334. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.116 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10335. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7110h**

Figure 14-3436. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-10337. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.117 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10338. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7114h**

Figure 14-3437. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-10340. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.118 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10341. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7118h**

Figure 14-3438. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-10343. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.119 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10344. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 711Ch**

Figure 14-3439. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-10346. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.120 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10347. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7120h**

Figure 14-3440. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-10349. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.121 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10350. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7124h**

Figure 14-3441. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-10352. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.122 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10353. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7128h**

Figure 14-3442. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-10355. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.123 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-10356. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 712Ch**

Figure 14-3443. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-10358. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.124 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-10359. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 7130h**

Figure 14-3444. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-10361. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.125 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register (Offset = 8010h) [reset = 0h]

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Table 14-10362. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8010h**

Figure 14-3445. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-10364. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_CLKSEL_CLK_SEL	R/W	0h	Selects Clock Source for Wakeup Domain (Device Manager and Peripherals) Field values (others are reserved): 1'b0 - CPU: MAIN_PLL15_HSDIV2_CLKOUT, Peripherals: MAIN_PLL15_HSDIV0_CLKOUT0 1'b1 - CPU and Peripherals: MCU_PLL0_HSDIV0_CKLOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.126 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register

1 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register (Offset = 8020h) [reset = 0h]

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Table 14-10365. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8020h**

Figure 14-3446. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							RSVD
NONE							
0h							0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKOUT_CTRL_WKUP_CLKOUT_SEL		
NONE					R/W		
0h					0h		

Table 14-10367. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
23:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT_CTRL_WKUP_CLKOUT_SEL	R/W	0h	Controls WKUP CLKOUT MUX for WKUP_CLKOUT0 Pin Reset Source: mod_por_rst_n 0 HFOSC0_CLK 1 LFOSC0_CLKOUT 2 MAIN_PLL0_HSDIV2_CLKOUT 3 MAIN_PLL1_HSDIV2_CLKOUT 4 MAIN_PLL2_HSDIV9_CLKOUT 5 DEVICE_CLKOUT_32K 6 CLK_12M_RC 7 HFOSC0_CLKOUT OTHER Reserved

14.2.1.1.3.2.127 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register (Offset = 8030h) [reset = 1h]

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Table 14-10368. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8030h**

Figure 14-3447. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">WKUP_GTC_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
</table>

Table 14-10370. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_GTC_CLKSEL_CLK_SEL	R/W	1h	Selects the GTC timebase clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CPSW2G_CPTS_RFT_CLK 3'b011 - Reserved '0' 3'b100 - MCU_EXT_REFCLK0 3'b101 - EXT_REFCLK1 3'b110 - MCU_SYSCLK0 undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.128 WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL Register (Offset = 803Ch) [reset = 0h]

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Table 14-10371. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 803Ch**

Figure 14-3448. WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EFUSE_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-10373. WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EFUSE_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_SYSCLK0/16 Reset Source: mod_por_rst_n

14.2.1.1.3.2.129 WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register

1 WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register (Offset = 80D0h) [reset = 0h]

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Table 14-10374. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 80D0h**

Figure 14-3449. WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL Name Register

31	30	29	28	27	26	25	24
DDR16SS_PMCTRL_DATA_RET_LD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DDR16SS_PMCTRL_DATA_RETENTION			
NONE				R/W			
0h				0h			

Table 14-10376. WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DDR16SS_PMCTRL_DATA_RET_LD	R/W	0h	Controls latching of the retention value Field values (others are reserved): 1'b0 - Latch Closed 1'b1 - Latch Open Reset Source: mcu_chip1_rst_n
30:4	RESERVED	NONE	0h	Reserved
3:0	DDR16SS_PMCTRL_DATA_RETENTION	R/W	0h	DDR16SS Retention: This is a fault tolerant bit field 0x06 Asserts DDRSS 'data_retention' which will Hi-Z most of the phy output pins except for CKE/RESET# All others (Default 0) : data_retention is deasserted for normal DDR16SS Operation Field values (others are reserved): 4'b0110 - Retention Activated 4'b0000 - Retention Deactivated Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.130 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register (Offset = 8190h) [reset = 0h]

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Table 14-10377. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8190h**

Figure 14-3450. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB0_CLKSEL_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-10379. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL	R/W	0h	Selects the clock source for the USB0 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.131 WKUP_CTRL_MMR_CFG0_USB1_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_USB1_CLKSEL Register (Offset = 8194h) [reset = 0h]

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Table 14-10380. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8194h**

Figure 14-3451. WKUP_CTRL_MMR_CFG0_USB1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB1_CLKSEL_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-10382. WKUP_CTRL_MMR_CFG0_USB1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB1_CLKSEL_REFCLK_SEL	R/W	0h	Selects the clock source for the USB1 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.132 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register (Offset = 81B0h) [reset = 0h]

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Table 14-10383. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 81B0h**

Figure 14-3452. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER0_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-10385. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 undefined - undefined 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV3_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW2G_CPTS_RFT_CLK 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.133 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register (Offset = 81B4h) [reset = 0h]

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Table 14-10386. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 81B4h**

Figure 14-3453. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER1_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-10388. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 undefined - undefined 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV3_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW2G_CPTS_RFT_CLK 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.134 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register (Offset = 8340h) [reset = 0h]

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Table 14-10389. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8340h**

Figure 14-3454. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				WKUP_WWD0_CTRL_WWD_STOP			
NONE				R/W			
0h				0h			

Table 14-10391. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	WKUP_WWD0_CTRL_WWD_STOP	R/W	0h	Controls Clocks to the WWD Watchdog Counter Field values (others are reserved): 4'b0000 - WWD Counter Running 4'b1010 - WWD Counter Stopped Reset Source: mod_g_rst_n

14.2.1.1.3.2.135 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register (Offset = 8380h) [reset = 0h]

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Table 14-10392. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8380h**

Figure 14-3455. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Name Register

31	30	29	28	27	26	25	24
WKUP_WWD0_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WKUP_WWD0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-10394. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WKUP_WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.3.2.136 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register

1 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register (Offset = 8600h) [reset = 0h]

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Table 14-10395. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 8600h**

Figure 14-3456. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_RTC_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-10397. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_RTC_CLKSEL_CLK_SEL	R/W	0h	Selects the source of the RTC functional clock Field values (others are reserved): 1'b0 - DEVICE_CLKOUT_32K 1'b1 - CLK_32K_RC Reset Source: mod_por_rst_n

14.2.1.1.3.2.137 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-10398. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9008h**

Figure 14-3457. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-10400. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.138 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-10401. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 900Ch**

Figure 14-3458. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-10403. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.139 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10404. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9100h**

Figure 14-3459. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-10406. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.140 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10407. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9104h**

Figure 14-3460. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-10409. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.141 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register (Offset = 9108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10410. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9108h**

Figure 14-3461. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2_READONLY							
R							
0h							

Table 14-10412. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.142 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register (Offset = 910Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10413. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 910Ch**

Figure 14-3462. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3_READONLY							
R							
0h							

Table 14-10415. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.143 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register (Offset = 9110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10416. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9110h**

Figure 14-3463. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4_READONLY							
R							
0h							

Table 14-10418. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.144 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register (Offset = 9114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10419. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9114h**

Figure 14-3464. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5_READONLY							
R							
0h							

Table 14-10421. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.145 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register (Offset = 9118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10422. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9118h**

Figure 14-3465. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R6_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10424. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.146 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register (Offset = 911Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10425. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 911Ch**

Figure 14-3466. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7_READONLY							
R							
0h							

Table 14-10427. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.147 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register (Offset = 9120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10428. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9120h**

Figure 14-3467. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8_READONLY							
R							
0h							

Table 14-10430. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.148 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register (Offset = 9124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10431. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9124h**

Figure 14-3468. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9_READONLY							
R							
0h							

Table 14-10433. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.149 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register (Offset = 9128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10434. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9128h**

Figure 14-3469. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10_READONLY							
R							
0h							

Table 14-10436. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.150 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11_READONLY Register (Offset = 912Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10437. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 912Ch**

Figure 14-3470. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R11_READONLY							
R							
0h							

Table 14-10439. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R11_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.151 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register (Offset = 9130h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10440. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 9130h**

Figure 14-3471. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R12_READONLY							
R							
0h							

Table 14-10442. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R12_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.152 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register (Offset = A010h) [reset = 0h]

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Table 14-10443. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A010h**

Figure 14-3472. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-10445. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects Clock Source for Wakeup Domain (Device Manager and Peripherals) Field values (others are reserved): 1'b0 - CPU: MAIN_PLL15_HSDIV2_CLKOUT, Peripherals: MAIN_PLL15_HSDIV0_CLKOUT0 1'b1 - CPU and Peripherals: MCU_PLL0_HSDIV0_CKLOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.153 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register (Offset = A020h) [reset = 0h]

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Table 14-10446. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A020h**

Figure 14-3473. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							RSVD
NONE							
0h							0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKOUT_CTRL_WKUP_CLKOUT_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-10448. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
23:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT_CTRL_WKUP_CLKOUT_SEL_PROXY	R/W	0h	Controls WKUP CLKOUT MUX for WKUP_CLKOUT0 Pin Reset Source: mod_por_rst_n 0 HFOSC0_CLK 1 LFOSC0_CLKOUT 2 MAIN_PLL0_HSDIV2_CLKOUT 3 MAIN_PLL1_HSDIV2_CLKOUT 4 MAIN_PLL2_HSDIV9_CLKOUT 5 DEVICE_CLKOUT_32K 6 CLK_12M_RC 7 HFOSC0_CLKOUT OTHER Reserved

14.2.1.1.3.2.154 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register (Offset = A030h) [reset = 1h]

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Table 14-10449. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A030h**

Figure 14-3474. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_GTC_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					1h		

Table 14-10451. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_GTC_CLKSEL_CLK_SEL_PROXY	R/W	1h	Selects the GTC timebase clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CPSW2G_CPTS_RFT_CLK 3'b011 - Reserved '0' 3'b100 - MCU_EXT_REFCLK0 3'b101 - EXT_REFCLK1 3'b110 - MCU_SYSCLK0 undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.155 WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register (Offset = A03Ch) [reset = 0h]

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Table 14-10452. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A03Ch**

Figure 14-3475. WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EFUSE_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-10454. WKUP_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EFUSE_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_SYSCLK0/16 Reset Source: mod_por_rst_n

14.2.1.1.3.2.156 WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register (Offset = A0D0h) [reset = 0h]

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Table 14-10455. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A0D0h**

Figure 14-3476. WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Name Register

31	30	29	28	27	26	25	24
DDR16SS_PMCTRL_DATA_RET_LD_PROXY	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				DDR16SS_PMCTRL_DATA_RETENTION_PROXY			
NONE				R/W			
0h				0h			

Table 14-10457. WKUP_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DDR16SS_PMCTRL_DATA_RET_LD_PROXY	R/W	0h	Controls latching of the retention value Field values (others are reserved): 1'b0 - Latch Closed 1'b1 - Latch Open Reset Source: mcu_chip1_rst_n
30:4	RESERVED	NONE	0h	Reserved
3:0	DDR16SS_PMCTRL_DATA_RETENTION_PROXY	R/W	0h	DDR16SS Retention: This is a fault tolerant bit field 0x06 Asserts DDRSS 'data_retention' which will Hi-Z most of the phy output pins except for CKE/RESET# All others (Default 0) : data_retention is deasserted for normal DDR16SS Operation Field values (others are reserved): 4'b0110 - Retention Activated 4'b0000 - Retention Deactivated Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.157 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register (Offset = A190h) [reset = 0h]

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Table 14-10458. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A190h**

Figure 14-3477. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB0_CLKSEL_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-10460. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL_PROXY	R/W	0h	Selects the clock source for the USB0 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.158 WKUP_CTRL_MMR_CFG0_USB1_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_USB1_CLKSEL_PROXY Register (Offset = A194h) [reset = 0h]

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Table 14-10461. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A194h**

Figure 14-3478. WKUP_CTRL_MMR_CFG0_USB1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>USB1_CLKSEL_REFCLK_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10463. WKUP_CTRL_MMR_CFG0_USB1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB1_CLKSEL_REFCLK_SEL_PROXY	R/W	0h	Selects the clock source for the USB1 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.159 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register (Offset = A1B0h) [reset = 0h]

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Table 14-10464. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A1B0h

Figure 14-3479. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER0_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-10466. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 undefined - undefined 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV3_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW2G_CPTS_RFT_CLK 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.160 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register (Offset = A1B4h) [reset = 0h]

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Table 14-10467. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A1B4h

Figure 14-3480. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER1_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-10469. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 undefined - undefined 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV3_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW2G_CPTS_RFT_CLK 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.161 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register (Offset = A340h) [reset = 0h]

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Table 14-10470. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A340h**

Figure 14-3481. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">WKUP_WWD0_CTRL_WWD_STOP_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-10472. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	WKUP_WWD0_CTRL_WWD_STOP_PROXY	R/W	0h	Controls Clocks to the WWD Watchdog Counter Field values (others are reserved): 4'b0000 - WWD Counter Running 4'b1010 - WWD Counter Stopped Reset Source: mod_g_rst_n

14.2.1.1.3.2.162 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register (Offset = A380h) [reset = 0h]

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Table 14-10473. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A380h**

Figure 14-3482. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP_WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WKUP_WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-10475. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WKUP_WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.3.2.163 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register (Offset = A600h) [reset = 0h]

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Table 14-10476. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 A600h**

Figure 14-3483. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_RTC_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-10478. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_RTC_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the source of the RTC functional clock Field values (others are reserved): 1'b0 - DEVICE_CLKOUT_32K 1'b1 - CLK_32K_RC Reset Source: mod_por_rst_n

14.2.1.1.3.2.164 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-10479. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B008h**

Figure 14-3484. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK2_KICK0_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK2_KICK0_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-10481. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.165 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-10482. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B00Ch**

Figure 14-3485. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-10484. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.166 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10485. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B100h**

Figure 14-3486. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-10487. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.167 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10488. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B104h**

Figure 14-3487. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-10490. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.168 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register (Offset = B108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10491. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B108h**

Figure 14-3488. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2							
R/W							
0h							

Table 14-10493. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.169 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register (Offset = B10Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10494. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B10Ch**

Figure 14-3489. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3							
R/W							
0h							

Table 14-10496. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.170 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register (Offset = B110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10497. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B110h**

Figure 14-3490. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4							
R/W							
0h							

Table 14-10499. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.171 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register (Offset = B114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10500. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B114h**

Figure 14-3491. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5							
R/W							
0h							

Table 14-10502. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.172 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register (Offset = B118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10503. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B118h**

Figure 14-3492. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6							
R/W							
0h							

Table 14-10505. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.173 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register (Offset = B11Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10506. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B11Ch**

Figure 14-3493. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7							
R/W							
0h							

Table 14-10508. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.174 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register (Offset = B120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10509. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B120h**

Figure 14-3494. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8							
R/W							
0h							

Table 14-10511. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.175 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register (Offset = B124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10512. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B124h**

Figure 14-3495. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9							
R/W							
0h							

Table 14-10514. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.176 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register (Offset = B128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10515. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B128h**

Figure 14-3496. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10							
R/W							
0h							

Table 14-10517. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.177 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register (Offset = B12Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-10518. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B12Ch**

Figure 14-3497. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R11							
R/W							
0h							

Table 14-10520. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R11	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.178 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register (Offset = B130h) [reset = 0h]

Claim bits for Partition 2

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Table 14-10521. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 B130h**

Figure 14-3498. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R12							
R/W							
0h							

Table 14-10523. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R12	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.179 WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT Register

1 WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT Register (Offset = C320h) [reset = 0h]

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Table 14-10524. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 C320h

Figure 14-3499. WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CRC_STAT_CRC_ERR_7	FUSE_CRC_STAT_CRC_ERR_6	FUSE_CRC_STAT_CRC_ERR_5	FUSE_CRC_STAT_CRC_ERR_4	FUSE_CRC_STAT_CRC_ERR_3	FUSE_CRC_STAT_CRC_ERR_2	FUSE_CRC_STAT_CRC_ERR_1	RESERVED
R	R	R	R	R	R	R	NONE
X	X	X	X	X	X	X	0h

Table 14-10526. WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CRC_STAT_CRC_ERR_7	R	X	Indicates eFuse CRC error on chain 7 Reset Source: mod_por_rst_n
6	FUSE_CRC_STAT_CRC_ERR_6	R	X	Indicates eFuse CRC error on chain 6 Reset Source: mod_por_rst_n
5	FUSE_CRC_STAT_CRC_ERR_5	R	X	Indicates eFuse CRC error on chain 5 Reset Source: mod_por_rst_n
4	FUSE_CRC_STAT_CRC_ERR_4	R	X	Indicates eFuse CRC error on chain 4 Reset Source: mod_por_rst_n
3	FUSE_CRC_STAT_CRC_ERR_3	R	X	Indicates eFuse CRC error on chain 3 Reset Source: mod_por_rst_n
2	FUSE_CRC_STAT_CRC_ERR_2	R	X	Indicates eFuse CRC error on chain 2 Reset Source: mod_por_rst_n
1	FUSE_CRC_STAT_CRC_ERR_1	R	X	Indicates eFuse CRC error on chain 1 Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.180 WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT Register

1 WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT Register (Offset = C340h) [reset = 0h]

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Table 14-10527. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 C340h

Figure 14-3500. WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CTRL_STAT_AUTOLOAD_ERR_7	FUSE_CTRL_STAT_AUTOLOAD_ERR_6	FUSE_CTRL_STAT_AUTOLOAD_ERR_5	FUSE_CTRL_STAT_AUTOLOAD_ERR_4	FUSE_CTRL_STAT_AUTOLOAD_ERR_3	FUSE_CTRL_STAT_AUTOLOAD_ERR_2	FUSE_CTRL_STAT_AUTOLOAD_ERR_1	FUSE_CTRL_STAT_AUTOLOAD_ERR_0
R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X

Table 14-10529. WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CTRL_STAT_AUTOLOAD_ERR_7	R	X	Autoload Error Status Chain 7 Reset Source: mod_por_rst_n
6	FUSE_CTRL_STAT_AUTOLOAD_ERR_6	R	X	Autoload Error Status Chain 6 Reset Source: mod_por_rst_n
5	FUSE_CTRL_STAT_AUTOLOAD_ERR_5	R	X	Autoload Error Status Chain 5 Reset Source: mod_por_rst_n
4	FUSE_CTRL_STAT_AUTOLOAD_ERR_4	R	X	Autoload Error Status Chain 4 Reset Source: mod_por_rst_n
3	FUSE_CTRL_STAT_AUTOLOAD_ERR_3	R	X	Autoload Error Status Chain 3 Reset Source: mod_por_rst_n
2	FUSE_CTRL_STAT_AUTOLOAD_ERR_2	R	X	Autoload Error Status Chain 2 Reset Source: mod_por_rst_n
1	FUSE_CTRL_STAT_AUTOLOAD_ERR_1	R	X	Autoload Error Status Chain 1 Reset Source: mod_por_rst_n
0	FUSE_CTRL_STAT_AUTOLOAD_ERR_0	R	X	Autoload Error Status Chain 0 Reset Source: mod_por_rst_n

14.2.1.1.3.2.181 WKUP_CTRL_MMR_CFG0_PBIST_EN Register

1 WKUP_CTRL_MMR_CFG0_PBIST_EN Register (Offset = C400h) [reset = 0h]

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Table 14-10530. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 C400h**

Figure 14-3501. WKUP_CTRL_MMR_CFG0_PBIST_EN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>PBIST_EN_DSS0</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>PBIST_EN_USB1</td><td>PBIST_EN_USB0</td><td>RESERVED</td><td>PBIST_EN_EMMC2</td><td>PBIST_EN_EMMC1</td><td>PBIST_EN_EMMC0</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10532. WKUP_CTRL_MMR_CFG0_PBIST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	PBIST_EN_DSS0	R/W	0h	Activates PBIST Access to DSS0 Memories Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	PBIST_EN_USB1	R/W	0h	Activates PBIST Access to USB1 Memories Reset Source: mod_g_rst_n
4	PBIST_EN_USB0	R/W	0h	Activates PBIST Access to USB0 Memories Reset Source: mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	PBIST_EN_EMMC2	R/W	0h	Activates PBIST Access to MMC2 Memories Reset Source: mod_g_rst_n
1	PBIST_EN_EMMC1	R/W	0h	Activates PBIST Access to MMC1 Memories Reset Source: mod_g_rst_n
0	PBIST_EN_EMMC0	R/W	0h	Activates PBIST Access to MMC0 Memories Reset Source: mod_g_rst_n

14.2.1.1.3.2.182 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

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Table 14-10533. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D008h**

Figure 14-3502. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-10535. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.183 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-10536. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D00Ch**

Figure 14-3503. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-10538. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.184 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10539. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D100h**

Figure 14-3504. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0_READONLY							
R							
0h							

Table 14-10541. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.185 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register (Offset = D104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10542. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D104h**

Figure 14-3505. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1_READONLY							
R							
0h							

Table 14-10544. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.186 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register (Offset = D108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10545. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D108h**

Figure 14-3506. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2_READONLY							
R							
0h							

Table 14-10547. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.187 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register (Offset = D10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-10548. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D10Ch**

Figure 14-3507. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3_READONLY							
R							
0h							

Table 14-10550. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.188 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register (Offset = D110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10551. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D110h**

Figure 14-3508. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4_READONLY							
R							
0h							

Table 14-10553. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.189 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register (Offset = D114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10554. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D114h**

Figure 14-3509. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5_READONLY							
R							
0h							

Table 14-10556. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.190 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register (Offset = D118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10557. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D118h**

Figure 14-3510. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6_READONLY							
R							
0h							

Table 14-10559. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.191 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register (Offset = D11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-10560. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D11Ch**

Figure 14-3511. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7_READONLY							
R							
0h							

Table 14-10562. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.192 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register (Offset = D120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10563. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 D120h**

Figure 14-3512. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R8_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R8_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R8_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R8_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10565. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.193 WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register (Offset = E320h) [reset = 0h]

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Table 14-10566. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 E320h**

Figure 14-3513. WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CRC_STAT_CRC_ERR_7_PROXY	FUSE_CRC_STAT_CRC_ERR_6_PROXY	FUSE_CRC_STAT_CRC_ERR_5_PROXY	FUSE_CRC_STAT_CRC_ERR_4_PROXY	FUSE_CRC_STAT_CRC_ERR_3_PROXY	FUSE_CRC_STAT_CRC_ERR_2_PROXY	FUSE_CRC_STAT_CRC_ERR_1_PROXY	RESERVED
R	R	R	R	R	R	R	NONE
X	X	X	X	X	X	X	0h

Table 14-10568. WKUP_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CRC_STAT_CRC_ERR_7_PROXY	R	X	Indicates eFuse CRC error on chain 7 Reset Source: mod_por_rst_n
6	FUSE_CRC_STAT_CRC_ERR_6_PROXY	R	X	Indicates eFuse CRC error on chain 6 Reset Source: mod_por_rst_n
5	FUSE_CRC_STAT_CRC_ERR_5_PROXY	R	X	Indicates eFuse CRC error on chain 5 Reset Source: mod_por_rst_n
4	FUSE_CRC_STAT_CRC_ERR_4_PROXY	R	X	Indicates eFuse CRC error on chain 4 Reset Source: mod_por_rst_n
3	FUSE_CRC_STAT_CRC_ERR_3_PROXY	R	X	Indicates eFuse CRC error on chain 3 Reset Source: mod_por_rst_n
2	FUSE_CRC_STAT_CRC_ERR_2_PROXY	R	X	Indicates eFuse CRC error on chain 2 Reset Source: mod_por_rst_n
1	FUSE_CRC_STAT_CRC_ERR_1_PROXY	R	X	Indicates eFuse CRC error on chain 1 Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.194 WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY Register (Offset = E340h) [reset = 0h]

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Table 14-10569. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 E340h**

Figure 14-3514. WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CTRL_STAT_AUTOLOAD_ERR_7_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_6_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_5_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_4_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_3_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_2_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_1_PROXY	FUSE_CTRL_STAT_AUTOLOAD_ERR_0_PROXY
R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X

Table 14-10571. WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CTRL_STAT_AUTOLOAD_ERR_7_PROXY	R	X	Autoload Error Status Chain 7 Reset Source: mod_por_rst_n
6	FUSE_CTRL_STAT_AUTOLOAD_ERR_6_PROXY	R	X	Autoload Error Status Chain 6 Reset Source: mod_por_rst_n
5	FUSE_CTRL_STAT_AUTOLOAD_ERR_5_PROXY	R	X	Autoload Error Status Chain 5 Reset Source: mod_por_rst_n
4	FUSE_CTRL_STAT_AUTOLOAD_ERR_4_PROXY	R	X	Autoload Error Status Chain 4 Reset Source: mod_por_rst_n
3	FUSE_CTRL_STAT_AUTOLOAD_ERR_3_PROXY	R	X	Autoload Error Status Chain 3 Reset Source: mod_por_rst_n
2	FUSE_CTRL_STAT_AUTOLOAD_ERR_2_PROXY	R	X	Autoload Error Status Chain 2 Reset Source: mod_por_rst_n
1	FUSE_CTRL_STAT_AUTOLOAD_ERR_1_PROXY	R	X	Autoload Error Status Chain 1 Reset Source: mod_por_rst_n

Table 14-10571. WKUP_CTRL_MMR_CFG0_FUSE_CTRL_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FUSE_CTRL_STAT_AUTOLOAD_ERR_0_PROXY	R	X	Autoload Error Status Chain 0 Reset Source: mod_por_rst_n

14.2.1.1.3.2.195 WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register (Offset = E400h) [reset = 0h]

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Table 14-10572. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 E400h

Figure 14-3515. WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PBIST_EN_DSS0_PROXY	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		
7	6	5	4	3	2	1	0
RESERVED		PBIST_EN_USB1_PROXY	PBIST_EN_USB0_PROXY	RESERVED	PBIST_EN_EMMC2_PROXY	PBIST_EN_EMMC1_PROXY	PBIST_EN_EMMC0_PROXY
NONE		R/W	R/W	NONE	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-10574. WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	PBIST_EN_DSS0_PROXY	R/W	0h	Activates PBIST Access to DSS0 Memories Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	PBIST_EN_USB1_PROXY	R/W	0h	Activates PBIST Access to USB1 Memories Reset Source: mod_g_rst_n
4	PBIST_EN_USB0_PROXY	R/W	0h	Activates PBIST Access to USB0 Memories Reset Source: mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	PBIST_EN_EMMC2_PROXY	R/W	0h	Activates PBIST Access to MMC2 Memories Reset Source: mod_g_rst_n
1	PBIST_EN_EMMC1_PROXY	R/W	0h	Activates PBIST Access to MMC1 Memories Reset Source: mod_g_rst_n
0	PBIST_EN_EMMC0_PROXY	R/W	0h	Activates PBIST Access to MMC0 Memories Reset Source: mod_g_rst_n

14.2.1.1.3.2.196 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-10575. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F008h**

Figure 14-3516. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0_PROXY							
R/W							
0h							

Table 14-10577. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.197 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-10578. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F00Ch**

Figure 14-3517. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1_PROXY							
R/W							
0h							

Table 14-10580. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.198 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10581. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F100h**

Figure 14-3518. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0							
R/W							
0h							

Table 14-10583. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.199 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register (Offset = F104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10584. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F104h**

Figure 14-3519. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1							
R/W							
0h							

Table 14-10586. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.200 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register (Offset = F108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10587. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F108h**

Figure 14-3520. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2							
R/W							
0h							

Table 14-10589. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.201 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register (Offset = F10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-10590. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F10Ch**

Figure 14-3521. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10592. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.202 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register (Offset = F110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10593. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F110h**

Figure 14-3522. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4							
R/W							
0h							

Table 14-10595. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.203 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register (Offset = F114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10596. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F114h**

Figure 14-3523. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5							
R/W							
0h							

Table 14-10598. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.204 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register (Offset = F118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10599. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F118h**

Figure 14-3524. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6							
R/W							
0h							

Table 14-10601. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.205 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register (Offset = F11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-10602. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F11Ch**

Figure 14-3525. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7							
R/W							
0h							

Table 14-10604. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.206 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register (Offset = F120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-10605. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4300 F120h**

Figure 14-3526. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R8							
R/W							
0h							

Table 14-10607. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.207 WKUP_CTRL_MMR_CFG0_LOCK4_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-10608. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1008h**

Figure 14-3527. WKUP_CTRL_MMR_CFG0_LOCK4_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0							
R/W							
0h							

Table 14-10610. WKUP_CTRL_MMR_CFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.208 WKUP_CTRL_MMR_CFG0_LOCK4_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-10611. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 100Ch**

Figure 14-3528. WKUP_CTRL_MMR_CFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-10613. WKUP_CTRL_MMR_CFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.209 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10614. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1100h**

Figure 14-3529. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-10616. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.210 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register (Offset = 11104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10617. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1104h**

Figure 14-3530. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1_READONLY							
R							
0h							

Table 14-10619. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.211 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register (Offset = 11108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10620. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1108h**

Figure 14-3531. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2_READONLY							
R							
0h							

Table 14-10622. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.212 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register (Offset = 1110Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-10623. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 110Ch**

Figure 14-3532. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3_READONLY							
R							
0h							

Table 14-10625. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.213 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register (Offset = 11110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10626. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1110h**

Figure 14-3533. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4_READONLY							
R							
0h							

Table 14-10628. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.214 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register (Offset = 11114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10629. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1114h**

Figure 14-3534. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5_READONLY							
R							
0h							

Table 14-10631. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.215 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register (Offset = 11118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10632. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1118h**

Figure 14-3535. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6_READONLY							
R							
0h							

Table 14-10634. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.216 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register (Offset = 1111Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-10635. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 111Ch**

Figure 14-3536. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7_READONLY							
R							
0h							

Table 14-10637. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.217 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10638. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 1120h**

Figure 14-3537. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-10640. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.218 WKUP_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-10641. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3008h**

Figure 14-3538. WKUP_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-10643. WKUP_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.219 WKUP_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-10644. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 300Ch**

Figure 14-3539. WKUP_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-10646. WKUP_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.220 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10647. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3100h**

Figure 14-3540. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-10649. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.221 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10650. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3104h**

Figure 14-3541. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-10652. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.222 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

Return to Summary Table

Table 14-10653. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3108h**

Figure 14-3542. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-10655. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.223 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-10656. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 310Ch**

Figure 14-3543. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-10658. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.224 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

Return to Summary Table

Table 14-10659. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3110h**

Figure 14-3544. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10661. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.225 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10662. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3114h**

Figure 14-3545. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-10664. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.226 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10665. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3118h**

Figure 14-3546. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10667. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.227 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-10668. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 311Ch**

Figure 14-3547. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-10670. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.228 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-10671. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 3120h**

Figure 14-3548. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P4_R8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P4_R8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-10673. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.229 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register

1 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register (Offset = 14000h) [reset = 0h]

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Table 14-10674. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 4000h**

Figure 14-3549. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHNG_DDR4_FSP_REQ_REQ
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						CHNG_DDR4_FSP_REQ_REQ_TYPE	
NONE						R/W	
0h						0h	

Table 14-10676. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHNG_DDR4_FSP_REQ_REQ	R/W	0h	Initiate FSP frequency change Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CHNG_DDR4_FSP_REQ_REQ_TYPE	R/W	0h	Frequency request type Indicates which DDR4 frequency set point to change to Reset Source: mod_por_rst_n

14.2.1.1.3.2.230 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register

1 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register (Offset = 14004h) [reset = 0h]

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Table 14-10677. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 4004h**

Figure 14-3550. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHNG_DDR4_FSP_ACK_ACK	RESERVED						CHNG_DDR4_FSP_ACK_ERROR
R	NONE						R
X	0h						X

Table 14-10679. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CHNG_DDR4_FSP_ACK_ACK	R	X	Frequency change acknowledge. This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 Indication from the DDR Controller that the FSP change operation is complete 0 - FSP change operation in progress 1 - FSP change operation complete Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	CHNG_DDR4_FSP_ACK_ERROR	R	X	Frequency change error This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 0 - FSP change was sucessful 1 - FSP change was not sucessful Reset Source: mod_por_rst_n

14.2.1.1.3.2.231 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register

1 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register (Offset = 14080h) [reset = 0h]

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Table 14-10680. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 4080h**

Figure 14-3551. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DDR4_FSP_CLKCHNG_REQ_REQ	RESERVED					DDR4_FSP_CLKCHNG_REQ_REQ_TYPE	
R	NONE					R	
X	0h					X	

Table 14-10682. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DDR4_FSP_CLKCHNG_REQ_REQ	R	X	DDR Controller FSP clock change request Indicates that the DDR controller needs the DDR clock changed to the frequency indicated by the req_type field. This bit is cleared when the DDR4_FSP_CLKCHNG_ACK_ack bit is set. Reset Source: mod_por_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	DDR4_FSP_CLKCHNG_REQ_REQ_TYPE	R	X	Frequency request type Indicates which DDR4 FSP frequency to which the DDR Controller wants the DDR clock set Reset Source: mod_por_rst_n

14.2.1.1.3.2.232 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register

1 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register (Offset = 140C0h) [reset = 0h]

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Table 14-10683. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 40C0h**

Figure 14-3552. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DDR4_FSP_CLKCHNG_ACK_ACK
NONE							R/W
0h							0h

Table 14-10685. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DDR4_FSP_CLKCHNG_ACK_ACK	R/W	0h	DDR FSP clock change ackowledge This bit should be set once the DDR clock has been sucessfully changed to the value requested by DDR4_FSP_CLKCHNG_REQ_req_type. Setting this bit will clear the DDR4_FSP_CLKCHNG_REQ_req bit and the associated change request interrupt. Reset Source: mod_por_rst_n

14.2.1.1.3.2.233 WKUP_CTRL_MMR_CFG0_LOCK5_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK5_KICK0 Register (Offset = 15008h) [reset = 0h]

- KICK0 component

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Table 14-10686. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 5008h**

Figure 14-3553. WKUP_CTRL_MMR_CFG0_LOCK5_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK0							
R/W							
0h							

Table 14-10688. WKUP_CTRL_MMR_CFG0_LOCK5_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.234 WKUP_CTRL_MMR_CFG0_LOCK5_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK5_KICK1 Register (Offset = 1500Ch) [reset = 0h]

- KICK1 component

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Table 14-10689. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 500Ch**

Figure 14-3554. WKUP_CTRL_MMR_CFG0_LOCK5_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK1							
R/W							
0h							

Table 14-10691. WKUP_CTRL_MMR_CFG0_LOCK5_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.235 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register (Offset = 15100h) [reset = 0h]

Claim bits for Partition 5

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Table 14-10692. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 5100h**

Figure 14-3555. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R0_READONLY							
R							
0h							

Table 14-10694. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R0_READONLY	R	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.3.2.236 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register (Offset = 15104h) [reset = 0h]

Claim bits for Partition 5

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Table 14-10695. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 5104h**

Figure 14-3556. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R1_READONLY							
R							
0h							

Table 14-10697. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R1_READONLY	R	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.3.2.237 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register (Offset = 16000h) [reset = 0h]

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Table 14-10698. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 6000h**

Figure 14-3557. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHNG_DDR4_FSP_REQ_REQ_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						CHNG_DDR4_FSP_REQ_REQ_TYPE_PROXY	
NONE						R/W	
0h						0h	

Table 14-10700. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHNG_DDR4_FSP_REQ_REQ_PROXY	R/W	0h	Initiate FSP frequency change Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CHNG_DDR4_FSP_REQ_REQ_TYPE_PROXY	R/W	0h	Frequency request type Indicates which DDR4 frequency set point to change to Reset Source: mod_por_rst_n

14.2.1.1.3.2.238 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register (Offset = 16004h) [reset = 0h]

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Table 14-10701. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 6004h**

Figure 14-3558. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHNG_DDR4_FSP_ACK_ACK_PROXY	RESERVED						CHNG_DDR4_FSP_ACK_ERROR_PROXY
R	NONE						R
X	0h						X

Table 14-10703. WKUP_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CHNG_DDR4_FSP_ACK_ACK_PROXY	R	X	Frequency change acknowledge. This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 Indication from the DDR Controller that the FSP change operation is complete 0 - FSP change operation in progress 1 - FSP change operation complete Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	CHNG_DDR4_FSP_ACK_ERROR_PROXY	R	X	Frequency change error This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 0 - FSP change was sucessful 1 - FSP change was not sucessful Reset Source: mod_por_rst_n

14.2.1.1.3.2.239 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register (Offset = 16080h) [reset = 0h]

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Table 14-10704. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 6080h**

Figure 14-3559. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DDR4_FSP_CLKCHNG_REQ_REQ_PROXY	RESERVED					DDR4_FSP_CLKCHNG_REQ_REQ_TYPE_PROXY	
R	NONE					R	
X	0h					X	

Table 14-10706. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DDR4_FSP_CLKCHNG_REQ_REQ_PROXY	R	X	DDR Controller FSP clock change request Indicates that the DDR controller needs the DDR clock changed to the frequency indicated by the req_type field. This bit is cleared when the DDR4_FSP_CLKCHNG_ACK_ack bit is set. Reset Source: mod_por_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	DDR4_FSP_CLKCHNG_REQ_REQ_TYPE_PROXY	R	X	Frequency request type Indicates which DDR4 FSP frequency to which the DDR Controller wants the DDR clock set Reset Source: mod_por_rst_n

14.2.1.1.3.2.240 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register (Offset = 160C0h) [reset = 0h]

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Table 14-10707. Instance Table

Instance Name	**Physical Address**
WKUP_CTRL_MMR0	**4301 60C0h**

Figure 14-3560. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DDR4_FSP_CLKCHNG_ACK_ACK_PROXY
NONE							R/W
0h							0h

Table 14-10709. WKUP_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DDR4_FSP_CLKCHNG_ACK_ACK_PROXY	R/W	0h	DDR FSP clock change ackowledge This bit should be set once the DDR clock has been sucessfully changed to the value requested by DDR4_FSP_CLKCHNG_REQ_req_type. Setting this bit will clear the DDR4_FSP_CLKCHNG_REQ_req bit and the associated change request interrupt. Reset Source: mod_por_rst_n

14.2.1.1.3.2.241 WKUP_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register (Offset = 17008h) [reset = 0h]

- KICK0 component

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Table 14-10710. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 7008h**

Figure 14-3561. WKUP_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK0_PROXY							
R/W							
0h							

Table 14-10712. WKUP_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.242 WKUP_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register (Offset = 1700Ch) [reset = 0h]

- KICK1 component

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Table 14-10713. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 700Ch**

Figure 14-3562. WKUP_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK1_PROXY							
R/W							
0h							

Table 14-10715. WKUP_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.243 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register (Offset = 17100h) [reset = 0h]

Claim bits for Partition 5

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Table 14-10716. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 7100h**

Figure 14-3563. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R0							
R/W							
0h							

Table 14-10718. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R0	R/W	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.3.2.244 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register (Offset = 17104h) [reset = 0h]

Claim bits for Partition 5

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Table 14-10719. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 7104h**

Figure 14-3564. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R1							
R/W							
0h							

Table 14-10721. WKUP_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R1	R/W	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.3.2.245 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0 Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0 Register (Offset = 18040h) [reset = 0h]

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Table 14-10722. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8040h**

Figure 14-3565. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0 Name Register

31	30	29	28	27	26	25	24
FW_CTRL_OUT0_FW_CTRL_OUT0							
R/W							
0h							
23	22	21	20	19	18	17	16
FW_CTRL_OUT0_FW_CTRL_OUT0							
R/W							
0h							
15	14	13	12	11	10	9	8
FW_CTRL_OUT0_FW_CTRL_OUT0							
R/W							
0h							
7	6	5	4	3	2	1	0
FW_CTRL_OUT0_FW_CTRL_OUT0							
R/W							
0h							

Table 14-10724. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FW_CTRL_OUT0_FW_CTRL_OUT0	R/W	0h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.246 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET Register (Offset = 18044h) [reset = 0h]

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Table 14-10725. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8044h**

Figure 14-3566. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.247 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR Register (Offset = 18048h) [reset = 0h]

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Table 14-10728. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8048h**

Figure 14-3567. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.248 WKUP_CTRL_MMR_CFG0_FW_STS_IN0 Register

1 WKUP_CTRL_MMR_CFG0_FW_STS_IN0 Register (Offset = 1804Ch) [reset = 0h]

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Table 14-10731. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 804Ch

Figure 14-3568. WKUP_CTRL_MMR_CFG0_FW_STS_IN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">X</td></tr>
</table>

14.2.1.1.3.2.249 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1 Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1 Register (Offset = 18050h) [reset = 0h]

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Table 14-10734. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8050h**

Figure 14-3569. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1 Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.250 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET Register (Offset = 18054h) [reset = 0h]

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Table 14-10737. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8054h**

Figure 14-3570. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

14.2.1.1.3.2.251 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR Register (Offset = 18058h) [reset = 0h]

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Table 14-10740. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8058h**

Figure 14-3571. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.252 WKUP_CTRL_MMR_CFG0_FW_STS_IN1 Register

1 WKUP_CTRL_MMR_CFG0_FW_STS_IN1 Register (Offset = 1805Ch) [reset = 0h]

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Table 14-10743. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 805Ch

Figure 14-3572. WKUP_CTRL_MMR_CFG0_FW_STS_IN1 Name Register

31	30	29	28	27	26	25	24
RSVD							
X							
23	22	21	20	19	18	17	16
RSVD							
X							
15	14	13	12	11	10	9	8
RSVD							
X							
7	6	5	4	3	2	1	0
RSVD							
X							

14.2.1.1.3.2.253 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register (Offset = 18080h) [reset = 10h]

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Table 14-10746. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8080h**

Figure 14-3573. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PMCTRL_SYS_PMIC_EN_WE	PMCTRL_SYS_PMIC_EN	PMCTRL_SYS_LPM_EN_WE	PMCTRL_SYS_LPM_EN		
NONE		R/W	R/W	R/W	R/W		
0h		0h	1h	0h	0h		

Table 14-10748. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PMCTRL_SYS_PMIC_EN_WE	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
4	PMCTRL_SYS_PMIC_EN	R/W	1h	Controls state of PMIC_LPM_EN_OUT when LPM_EN[2:0] is 000 Reset Source: mod_g_rst_n
3	PMCTRL_SYS_LPM_EN_WE	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
2:0	PMCTRL_SYS_LPM_EN	R/W	0h	Controls whether PMIC_LPM_EN_OUT is driven by the pmic_en bit, or by deep sleep logic. Field values (others are reserved): 3'b000 - PMIC_LPM_EN_OUT controlled by pmic_en bit. 3'b101 - PMIC_LPM_EN_OUT controlled by DeepSleep Logic Reset Source: mod_g_rst_n

14.2.1.1.3.2.254 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register (Offset = 18084h) [reset = 0h]

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Table 14-10749. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8084h**

Figure 14-3574. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Name Register

31	30	29	28	27	26	25	24
RESERVED						PMCTRL_IO_0_IO_ISO_STATUS_0	PMCTRL_IO_0_IO_ISO_CTRL_0
NONE						R	R/W
0h						X	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PMCTRL_IO_0_GLOBAL_WUEN_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PMCTRL_IO_0_WUCLK_STATUS_0	PMCTRL_IO_0_WUCLK_CTRL_0
NONE						R	R/W
0h						X	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PMCTRL_IO_0_ISOBYPASS_OVR_0	PMCTRL_IO_0_IO_ON_STATUS_0	PMCTRL_IO_0_ISOOVR_EXTEND_0	RESERVED		PMCTRL_IO_0_ISOCLK_STATUS_0	PMCTRL_IO_0_ISOCLK_OVRD_0
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-10751. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	PMCTRL_IO_0_IO_ISO_STATUS_0	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_0_IO_ISO_CTRL_0	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PMCTRL_IO_0_GLOBAL_WUEN_0	R/W	0h	Global IO wakeup activate. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n

Table 14-10751. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_0_WUCLK_STATUS_0	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_0_WUCLK_CTRL_0	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is activated. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_0_ISOBYPASS_OVR_0	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_0_IO_ON_STATUS_0	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_0_ISOOVR_EXTEND_0	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to activate when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global activate/deactivate for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_0_ISOCLK_STATUS_0	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_0_ISOCLK_OVRD_0	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.255 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register (Offset = 18088h) [reset = 0h]

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Table 14-10752. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8088h**

Figure 14-3575. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Name Register

31	30	29	28	27	26	25	24
RSVD						PMCTRL_IO_1_IO_ISO_STATUS_1	PMCTRL_IO_1_IO_ISO_CTRL_1
						R	R/W
X						X	0h

23	22	21	20	19	18	17	16
RESERVED							PMCTRL_IO_1_GLOBAL_WUEN_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						PMCTRL_IO_1_WUCLK_STATUS_1	PMCTRL_IO_1_WUCLK_CTRL_1
NONE						R	R/W
0h						X	0h

7	6	5	4	3	2	1	0
RESERVED	PMCTRL_IO_1_ISOBYPASS_OVR_1	PMCTRL_IO_1_IO_ON_STATUS_1	PMCTRL_IO_1_ISOOVR_EXTEND_1	RESERVED		PMCTRL_IO_1_ISOCLK_STATUS_1	PMCTRL_IO_1_ISOCLK_OVRD_1
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-10754. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
25	PMCTRL_IO_1_IO_ISO_STATUS_1	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_1_IO_ISO_CTRL_1	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PMCTRL_IO_1_GLOBAL_WUEN_1	R/W	0h	Global IO wakeup activate. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved

Table 14-10754. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PMCTRL_IO_1_WUCLK_STATUS_1	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_1_WUCLK_CTRL_1	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is activated. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_1_ISOBYPASS_OVR_1	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_1_IO_ON_STATUS_1	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_1_ISOOVR_EXTEND_1	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to activate when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global activate/deactivate for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_1_ISOCLK_STATUS_1	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_1_ISOCLK_OVRD_1	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.256 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register (Offset = 18090h) [reset = BC00h]

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Table 14-10755. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8090h**

Figure 14-3576. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Name Register

31	30	29	28	27	26	25	24
PMCTRL_MOSC_OSC_CG_ON_WFI	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PMCTRL_MOSC_SETUP_TIME			
NONE				R/W			
0h				BC00h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMCTRL_MOSC_SETUP_TIME							
R/W							
BC00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMCTRL_MOSC_SETUP_TIME							
R/W							
BC00h							

Table 14-10757. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PMCTRL_MOSC_OSC_CG_ON_WFI	R/W	0h	When set by Device Manager - the soc clock gating logic will gate the device manager clock once Device Manager has entered the WFI state. (Note: this was named osc_cg_dis but name didn't match function) Reset Source: mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:0	PMCTRL_MOSC_SETUP_TIME	R/W	BC00h	Keep the main oscillator clock gates for the number of HFOSC clock cycles This is the time it takes to stabilize the clock source supplier (i.e. Main Oscillator) Reset Source: mod_g_rst_n

14.2.1.1.3.2.257 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register

1 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register (Offset = 18098h) [reset = 0h]

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Table 14-10758. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8098h**

Figure 14-3577. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PM_MISC_STATUS_OSC_CG_STAT	
NONE						R	
0h						X	

Table 14-10760. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PM_MISC_STATUS_OSC_CG_STAT	R	X	Reflects the status of the request to clock-gate HF oscillator via MMR PMCTRL_MOSCundefined. 11: osc_cgen_req = '0' & osc_cgen_ack = '1' 10: osc_cgen_req = '1' & osc_cgen_ack = '0' 01: osc_cgen_req = '0' & osc_cgen_ack = '0' 00: osc_cgen_req = '1' & osc_cgen_ack = '1' Reset Source: mod_g_rst_n

14.2.1.1.3.2.258 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB Register (Offset = 1809Ch) [reset = 0h]

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Table 14-10761. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 809Ch**

Figure 14-3578. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PMCTRL_IO_GLB_DSEN_QUALIFIED	
NONE						R/W	
0h						0h	

Table 14-10763. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PMCTRL_IO_GLB_DSEN_QUALIFIED	R/W	0h	To dsen_qualified signal generation logic for daisychain[1:0] logic. Used to control I/O buffer ouput and output activate during deepsleep mode. See IO Integration spec for detail. Reset Source: mod_g_rst_n

14.2.1.1.3.2.259 WKUP_CTRL_MMR_CFG0_PM_PERMISSION Register

1 WKUP_CTRL_MMR_CFG0_PM_PERMISSION Register (Offset = 180A0h) [reset = 0h]

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Table 14-10764. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 80A0h**

Figure 14-3579. WKUP_CTRL_MMR_CFG0_PM_PERMISSION Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PM_PERMISSION_MCU_SAFETY_ACTIVE	PM_PERMISSION_SECURITY_ACTIVE	PM_PERMISSION_DEBUG_ACTIVE
NONE					R	R	R
0h					X	X	X

Table 14-10766. WKUP_CTRL_MMR_CFG0_PM_PERMISSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	PM_PERMISSION_MCU_SAFETY_ACTIVE	R	X	Read Only - Reads return a 1 when am62_mcu_ctrl_mmr.wkup_0.RST_MAGIC_WORD_mcu_magic_word_ipcfg[31:0] != 32'h0. When 1, indicates that the MCU is blocking reset and also deep sleep entry. Reset Source: mod_g_rst_n
1	PM_PERMISSION_SECURITY_ACTIVE	R	X	Read Only - Reads return the value of ms.main_0.sms_iopm_pmpermission_security_active. When 1, indicates that SMS is blocking deep sleep entry. Reset Source: mod_g_rst_n
0	PM_PERMISSION_DEBUG_ACTIVE	R	X	Read Only - Returns a 1 when IceMelter is blocking deep sleep entry. Reset Source: mod_g_rst_n

14.2.1.1.3.2.260 WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL Register

1 WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL Register (Offset = 18160h) [reset = 0h]

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Table 14-10767. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8160h**

Figure 14-3580. WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							DEEPSLEEP_CTRL_FORCE_DS_MAIN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							DEEPSLEEP_CTRL_FORCE_DS_WKUP
NONE							R/W
0h							0h

Table 14-10769. WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	DEEPSLEEP_CTRL_FORCE_DS_MAIN	R/W	0h	Force all MAIN IOs into deepsleep mode when set Reset Source: mod_por_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DEEPSLEEP_CTRL_FORCE_DS_WKUP	R/W	0h	Force all WKUP IOs into deepsleep mode when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.261 WKUP_CTRL_MMR_CFG0_RST_CTRL Register

1 WKUP_CTRL_MMR_CFG0_RST_CTRL Register (Offset = 18170h) [reset = 200FFh]

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Table 14-10770. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8170h**

Figure 14-3581. WKUP_CTRL_MMR_CFG0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					RST_CTRL_MAIN_RESET_ISO_DONE_Z	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z	RST_CTRL_SMS_COLD_RESET_EN_Z
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST_CTRL_SW_MAIN_POR				RST_CTRL_SW_MAIN_WARMRST			
R/W				R/W			
Fh				Fh			

Table 14-10772. WKUP_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z	R/W	0h	Main Domain CPUs can set this bit to block warm reset in the main domain which is useful when the Main domain may be accessing main domain resources (peripherals, memory..). In this case, the main domain cpus will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, Main needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0 - Reset of Main Domain is not Blocked by Main Domain 1 - Reset of Main Domain is Blocked by Main Domain Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z	R/W	1h	Deactivate Reset of Main by ESM 0 - Activated 1 - Deactivated Reset Source: main_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z	R/W	0h	Deactivate Reset of Main by SMS 0 - Activated 1 - Deactivated Reset Source: main_chip1_rst_n

Table 14-10772. WKUP_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:4	RST_CTRL_SW_MAIN_POR	R/W	Fh	Causes Main Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST	R/W	Fh	Causes Main Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.3.2.262 WKUP_CTRL_MMR_CFG0_RST_STAT Register

1 WKUP_CTRL_MMR_CFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

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Table 14-10773. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8174h**

Figure 14-3582. WKUP_CTRL_MMR_CFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z
NONE							R
0h							X

Table 14-10775. WKUP_CTRL_MMR_CFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z	R	X	is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding Reset Source: main_chip1_rst_n

14.2.1.1.3.2.263 WKUP_CTRL_MMR_CFG0_RST_SRC Register

1 WKUP_CTRL_MMR_CFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

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Table 14-10776. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8178h**

Figure 14-3583. WKUP_CTRL_MMR_CFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN	RST_SRC_SW_MAIN_POR_FROM_MCU
R	R	NONE				R	R
X	X	0h				X	X
23	22	21	20	19	18	17	16
RESERVED	RST_SRC_DM_WDT_RST	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	RESERVED			RST_SRC_SW_MCU_WARMRST
NONE	R	R	R	NONE			R
0h	X	X	X	0h			X
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R	R	NONE			R
0h		X	X	0h			X
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST	RESERVED	RST_SRC_MAIN_RESET_REQ	RESERVED	RST_SRC_MCU_RESET_PIN
NONE			R	NONE	R	NONE	R
0h			X	0h	X	0h	X

Table 14-10778. WKUP_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R	X	Reset Caused by MCU ESM Error Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R	X	Reset Caused by Main ESM Error Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN	R	X	Software Main Power On Reset From MAIN CTRL MMR Reset Source: main_chip1_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU	R	X	Software Main Power On Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
23	RESERVED	NONE	0h	Reserved
22	RST_SRC_DM_WDT_RST	R	X	Watchdog Initiated Reset Reset Source: main_chip1_rst_n

Table 14-10778. WKUP_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	R	X	Software Main Warm Reset from MAIN CTRL MMR Reset Source: main_chip1_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	R	X	Software Main Warm Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R	X	Software Warm Reset Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST	R	X	SMS Warm Reset Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST	R	X	SMS Cold Reset Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R	X	Debug Subsystem Initiated Reset Reset Source: main_chip1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R	X	Thermal Reset Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ	R	X	Main Reset Pin Reset Source: main_chip1_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R	X	Rest Caused by MCU Reset Pin Reset Source: main_chip1_rst_n

14.2.1.1.3.2.264 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register

1 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

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Table 14-10779. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 817Ch

Figure 14-3584. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							

Table 14-10781. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.3.2.265 WKUP_CTRL_MMR_CFG0_WKUP0_EN Register

1 WKUP_CTRL_MMR_CFG0_WKUP0_EN Register (Offset = 18180h) [reset = 0h]

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Table 14-10782. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8180h**

Figure 14-3585. WKUP_CTRL_MMR_CFG0_WKUP0_EN Name Register

31	30	29	28	27	26	25	24
WKUP0_EN_WKUPEN							
R/W							
0h							
23	22	21	20	19	18	17	16
WKUP0_EN_WKUPEN							
R/W							
0h							
15	14	13	12	11	10	9	8
WKUP0_EN_WKUPEN							
R/W							
0h							
7	6	5	4	3	2	1	0
WKUP0_EN_WKUPEN							
R/W							
0h							

Table 14-10784. WKUP_CTRL_MMR_CFG0_WKUP0_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WKUP0_EN_WKUPEN	R/W	0h	Activates Wakeup from: b0 - WKUP I2C0 b1 - WKUP USART0 b2 - MCU GPIO0 b3 - DEBUG (IceMelter) b4 - Reserved b5 - WKUP DMTIMER0 b6 - WKUP DMTIMER1 b7 - WKUP RTC b8 - Main RESET_REQz b9 - USB0 In Band b10 - USB1 In Band b16 - MAIN IO Daisy Chain b17 - MCU IO Daisy Chain b18 - CANUART IO Daisy Chain Reset Source: mod_g_rst_n

14.2.1.1.3.2.266 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register

1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register (Offset = 18280h) [reset = Eh]

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Table 14-10785. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8280h**

Figure 14-3586. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Name Register

31	30	29	28	27	26	25	24
CLKGATE_CTRL0_MAIN_SMS_NOGATE	RESERVED	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED	RSVD	RESERVED		CLKGATE_CTRL0_MAIN_PDMA2_NOGATE	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	CLKGATE_CTRL0_MAIN_DMSS_NOGATE
NONE		NONE		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

15	14	13	12	11	10	9	8
CLKGATE_CTRL0_MAIN_GIC500_NOGATE	RESERVED	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE	CLKGATE_CTRL0_MAIN_MCASP_CBA_NOGATE	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE	CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE	CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE	CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CLKGATE_CTRL0_MAIN_A53_0_NOGATE	RESERVED	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	1h	1h	0h

Table 14-10787. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKGATE_CTRL0_MAIN_SMS_NOGATE	R/W	0h	MAIN domain SMS (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE	R/W	0h	MAIN domain SA3SS clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
28	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	R/W	0h	MAIN domain Debug CBA (main_dbg_cba)clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

Table 14-10787. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:23	RESERVED	NONE	0h	Reserved
21:20	RESERVED	NONE	0h	Reserved
19	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE	R/W	0h	MAIN domain PDMA2 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
18	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	R/W	0h	MAIN domain PDMA1 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
17	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	R/W	0h	MAIN domain PDMA0 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
16	CLKGATE_CTRL0_MAIN_DMSS_NOGATE	R/W	0h	MAIN domain DMSS (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
15	CLKGATE_CTRL0_MAIN_GIC500_NOGATE	R/W	0h	MAIN A53SS0 (gic500_1_2) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
14	RESERVED	NONE	0h	Reserved
13	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (main_ipcss_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
12	CLKGATE_CTRL0_MAIN_MCASP_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (main_mcasp_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
11	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (main_misc_peri_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
10	CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE	R/W	0h	MAIN A53SS0 Debug Port clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
9	CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE	R/W	0h	MAIN A53SS0 Configuration Port clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
8	CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE	R/W	0h	MAIN A53SS0 ACP clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

Table 14-10787. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CLKGATE_CTRL0_MAIN_A53_0_NOGATE	R/W	0h	MAIN A53SS0 clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
6	RESERVED	NONE	0h	Reserved
5	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	R/W	0h	MAIN domain datal bus (main_fw_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
4	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE	R/W	0h	MAIN domain data bus (main_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
3	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE	R/W	1h	WKUP domain Infrastructure ECC aggregator(wkup_safe_ecc_aggr) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
2	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE	R/W	1h	WKUP domain Device Manager (wkup_dm_pwr_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
1	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE	R/W	1h	WKUP domain device manager CBA clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
0	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (main_infra_cbass and psc_fw_ch_br) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.3.2.267 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register

1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register (Offset = 18284h) [reset = 0h]

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Table 14-10788. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8284h**

Figure 14-3587. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKGATE_CTRL1_VPAC0_NOGATE	RESERVED			CLKGATE_CTRL1_C7X_NOGATE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
CLKGATE_CTRL1_JPEG_ENC_NOGATE	RESERVED			CLKGATE_CTRL1_VIDEO_CODEC_NOGATE	RESERVED		CLKGATE_CTRL1_DMSS_CSI_NOGATE
R/W	NONE			R/W	NONE		R/W
0h	0h			0h	0h		0h

Table 14-10790. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLKGATE_CTRL1_VPAC0_NOGATE	R/W	0h	VPAC0 clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLKGATE_CTRL1_C7X_NOGATE	R/W	0h	C7x clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLKGATE_CTRL1_JPEG_ENC_NOGATE	R/W	0h	JPEG Encoder clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved

Table 14-10790. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLKGATE_CTRL1_VIDEO_CODEC_NOGATE	R/W	0h	VIDEO CODEC clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CLKGATE_CTRL1_DMSS_CSI_NOGATE	R/W	0h	DMSS_CSI clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.3.2.268 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register (Offset = 18300h) [reset = 0h]

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Table 14-10791. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8300h**

Figure 14-3588. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CANUART_WAKE_CTRL_MW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CANUART_WAKE_CTRL_MW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CANUART_WAKE_CTRL_MW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">CANUART_WAKE_CTRL_MW</td><td>CANUART_WAKE_CTRL_MW_LOAD_EN</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10793. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_CTRL_MW	R/W	0h	CANUART IO magic word. This 31-bit value that activates placing of the CANUART I/Os into isolation for daisy-chain wakeup operation. The Upper 8 bits are software defined. The lower 23 bits are checked by hardware: - 0x5AAAAA - Magic word value to activate isolation whenqualified with mw_load bit - Others - Any other value will prevent isolation when mw_loadtransitions from 0 to 1 Reset Source: mcu_chip1_rst_n
0	CANUART_WAKE_CTRL_MW_LOAD_EN	R/W	0h	Magic word load activate Setting this bit to 1 loads and locks the mw field for CANUART IO isolation. If the mw field matches the magicword value then the value is latched into the CANUART IO voltage domain and CANUART IO isolation is activated. 0 - Unlock and do not load mw value for comparison 1 - Load and lock mw for magic word value comparison Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.269 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register (Offset = 18308h) [reset = 0h]

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Table 14-10794. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8308h**

Figure 14-3589. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_STAT0_MW_STAT							
R							
X							
23	22	21	20	19	18	17	16
CANUART_WAKE_STAT0_MW_STAT							
R							
X							
15	14	13	12	11	10	9	8
CANUART_WAKE_STAT0_MW_STAT							
R							
X							
7	6	5	4	3	2	1	0
CANUART_WAKE_STAT0_MW_STAT							CANUART_WAKE_STAT0_MW_LOAD_STAT
R							R
X							X

Table 14-10796. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_STAT0_MW_STAT	R	X	CANUART magic word status Indicates the latched value of the mw field. Reset Source: mod_por_rst_n
0	CANUART_WAKE_STAT0_MW_LOAD_STAT	R	X	Magic word load status. Indicates the latched value of the mw_load_en bit Reset Source: mod_por_rst_n

14.2.1.1.3.2.270 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register (Offset = 1830Ch) [reset = 0h]

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Table 14-10797. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 830Ch**

Figure 14-3590. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CANUART_WAKE_STAT1_CANUART_IO_MODE
NONE							R
0h							X

Table 14-10799. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CANUART_WAKE_STAT1_CANUART_IO_MODE	R	X	Indicates if CANUART IO wakeup mode is activated. 0 - Not activated (load_en not set or mw doesn't match magic word) 1 - CANUART IO mode activated Reset Source: mod_por_rst_n

14.2.1.1.3.2.271 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register (Offset = 18310h) [reset = 0h]

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Table 14-10800. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8310h**

Figure 14-3591. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							

Table 14-10802. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_MW	R/W	0h	magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.272 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register (Offset = 18318h) [reset = 0h]

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Table 14-10803. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8318h**

Figure 14-3592. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_STAT_MW							
R							
X							
23	22	21	20	19	18	17	16
CANUART_WAKE_OFF_MODE_STAT_MW							
R							
X							
15	14	13	12	11	10	9	8
CANUART_WAKE_OFF_MODE_STAT_MW							
R							
X							
7	6	5	4	3	2	1	0
CANUART_WAKE_OFF_MODE_STAT_MW							
R							
X							

Table 14-10805. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_STAT_MW	R	X	returned magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.273 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register (Offset = 18320h + formula) [reset = 0h]

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Offset = 18320h + (j * 4h); where j = 0 to 3d

Table 14-10806. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8320h + formula**

Figure 14-3593. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
KEYVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
KEYVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
KEYVAL							
R/W							
0h							

Table 14-10808. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL	R/W	0h	key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.274 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register (Offset = 18340h + formula) [reset = 0h]

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Offset = 18340h + (j * 4h); where j = 0 to 3d

Table 14-10809. Instance Table

Instance Name	**Physical Address**
WKUP_CTRL_MMR0	**4301 8340h + formula**

Figure 14-3594. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Name Register

31	30	29	28	27	26	25	24
KEYVAL							
R							
X							
23	22	21	20	19	18	17	16
KEYVAL							
R							
X							
15	14	13	12	11	10	9	8
KEYVAL							
R							
X							
7	6	5	4	3	2	1	0
KEYVAL							
R							
X							

Table 14-10811. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL	R	X	returned key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.275 WKUP_CTRL_MMR_CFG0_WFI_STATUS Register

1 WKUP_CTRL_MMR_CFG0_WFI_STATUS Register (Offset = 18400h) [reset = 0h]

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Table 14-10812. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8400h**

Figure 14-3595. WKUP_CTRL_MMR_CFG0_WFI_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			WFI_STATUS_A53SS0_CPU3_WFI	WFI_STATUS_A53SS0_CPU2_WFI	WFI_STATUS_A53SS0_CPU1_WFI	WFI_STATUS_A53SS0_CPU0_WFI	RESERVED
NONE			R	R	R	R	NONE
0h			X	X	X	X	0h
7	6	5	4	3	2	1	0
RESERVED			WFI_STATUS_MCU_R5F_WFI	WFI_STATUS_SMS_CPU1_WFI	WFI_STATUS_SMS_CPU0_WFI	RESERVED	WFI_STATUS_PULSAR_UL0_WFI
NONE			R	R	R	NONE	R
0h			X	X	X	0h	X

Table 14-10814. WKUP_CTRL_MMR_CFG0_WFI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	WFI_STATUS_A53SS0_CPU3_WFI	R	X	WFI status of A53SS0 CPU3 Reset Source: mod_por_rst_n
11	WFI_STATUS_A53SS0_CPU2_WFI	R	X	WFI status of A53SS0 CPU2 Reset Source: mod_por_rst_n
10	WFI_STATUS_A53SS0_CPU1_WFI	R	X	WFI status of A53SS0 CPU1 Reset Source: mod_por_rst_n
9	WFI_STATUS_A53SS0_CPU0_WFI	R	X	WFI status of A53SS0 CPU0 Reset Source: mod_por_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	WFI_STATUS_MCU_R5F_WFI	R	X	WFI status of MCU Cortex R5F Reset Source: mod_por_rst_n
3	WFI_STATUS_SMS_CPU1_WFI	R	X	WFI status of SMS Cortex M4F1 Reset Source: mod_por_rst_n
2	WFI_STATUS_SMS_CPU0_WFI	R	X	WFI status of SMS Cortex M4F0 Reset Source: mod_por_rst_n

Table 14-10814. WKUP_CTRL_MMR_CFG0_WFI_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	NONE	0h	Reserved
0	WFI_STATUS_PULSAR_UL0_WFI	R	X	WFI status of Device Manager Cortex R5F Reset Source: mod_por_rst_n

14.2.1.1.3.2.276 WKUP_CTRL_MMR_CFG0_SLEEP_STATUS Register

1 WKUP_CTRL_MMR_CFG0_SLEEP_STATUS Register (Offset = 18410h) [reset = 0h]

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Table 14-10815. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8410h**

Figure 14-3596. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS Name Register

31	30	29	28	27	26	25	24
SLEEP_STATUS_EXITED_SLEEP	RESERVED		SLEEP_STATUS_MAIN_DS	RESERVED			
R/W1TC	NONE		R/W1TC	NONE			
0h	0h		0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							SLEEP_STATUS_MAIN_RESETSTATZ
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED							RSVD
NONE							
0h							X

Table 14-10817. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SLEEP_STATUS_EXITED_SLEEP	R/W1TC	0h	Set when the HFXOSC clock gate is activated (rising edge capture of OSC_CG_ACK). To be read and cleared by DM after exiting WFI as a status signal distinguishing the case where WFI was entered and the clock was stopped, then exited with a wakeup (this bit will be set) from the case where an interrupt or other event caused the WFI sequence to stop and the HFXOSC was never stopped. Reset Source: sys_por_rst_n
30:29	RESERVED	NONE	0h	Reserved
28	SLEEP_STATUS_MAIN_DS	R/W1TC	0h	Set when the main domain deep sleep power on reset / power domain off is activated. (rising edge detect of am62_wkup_ctrl_mmr.wkup_0.DS_MAIN_por_pdoff_ft_out_ipcfg). This will be checked by the ROM on TIFS upon exiting from reset to determine if it is a power on reset or exiting deep sleep. Reset Source: sys_por_rst_n
27:9	RESERVED	NONE	0h	Reserved

Table 14-10817. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SLEEP_STATUS_MAIN_RESETSTATZ	R	X	Reflects the status of the main domain resetz signal Field values (others are reserved): 1'b0 - Main Domain In Reset 1'b1 - Main Domain Out of Reset Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.277 WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD Register

1 WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD Register (Offset = 18418h) [reset = 0h]

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Table 14-10818. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8418h**

Figure 14-3597. WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
DS_MAGIC_WORD_DS_MAGIC_WORD							
R/W							
0h							
23	22	21	20	19	18	17	16
DS_MAGIC_WORD_DS_MAGIC_WORD							
R/W							
0h							
15	14	13	12	11	10	9	8
DS_MAGIC_WORD_DS_MAGIC_WORD							
R/W							
0h							
7	6	5	4	3	2	1	0
DS_MAGIC_WORD_DS_MAGIC_WORD							
R/W							
0h							

Table 14-10820. WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DS_MAGIC_WORD_DS_MAGIC_WORD	R/W	0h	Magic Word Indicating State of Deep Sleep Reset Source: main_chip1_rst_n

14.2.1.1.3.2.278 WKUP_CTRL_MMR_CFG0_DS_MAIN Register

1 WKUP_CTRL_MMR_CFG0_DS_MAIN Register (Offset = 18420h) [reset = Fh]

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Table 14-10821. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8420h**

Figure 14-3598. WKUP_CTRL_MMR_CFG0_DS_MAIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DS_MAIN_POR_PDOFF</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-10823. WKUP_CTRL_MMR_CFG0_DS_MAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_MAIN_POR_PDOFF	R/W	Fh	Signal Puts main SMS, DebugSS and MainIP Power Domains into Power Off state, and asserts Main Power On Reset. Field values (others are reserved): 4'b0110 - Off 4'b1111 - On Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.279 WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register

1 WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register (Offset = 18440h) [reset = Fh]

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Table 14-10824. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8440h**

Figure 14-3599. WKUP_CTRL_MMR_CFG0_DS_DM_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_DM_RESET_MASK			
NONE				R/W			
0h				Fh			

Table 14-10826. WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_DM_RESET_MASK	R/W	Fh	Signal used to mask main domain resets from Device Manager / Wakeup and MCU Ips Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.280 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register

1 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register (Offset = 18460h) [reset = Fh]

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Table 14-10827. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8460h**

Figure 14-3600. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB0_RESET_MASK			
NONE				R/W			
0h				Fh			

Table 14-10829. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB0_RESET_MASK	R/W	Fh	Signal used to block reset to the USBSS0 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.281 WKUP_CTRL_MMR_CFG0_DS_USB1_RESET Register

1 WKUP_CTRL_MMR_CFG0_DS_USB1_RESET Register (Offset = 18464h) [reset = Fh]

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Table 14-10830. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8464h**

Figure 14-3601. WKUP_CTRL_MMR_CFG0_DS_USB1_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB1_RESET_MASK			
NONE				R/W			
0h				Fh			

Table 14-10832. WKUP_CTRL_MMR_CFG0_DS_USB1_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB1_RESET_MASK	R/W	Fh	Signal used to block reset to the USBSS1 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.282 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN Register

1 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN Register (Offset = 18480h) [reset = 0h]

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Table 14-10833. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8480h**

Figure 14-3602. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>DM_CLKSTOP_EN_EN_17</td><td>DM_CLKSTOP_EN_EN_16</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>DM_CLKSTOP_EN_EN_3</td><td colspan="2">RESERVED</td><td>DM_CLKSTOP_EN_EN_0</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-10835. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DM_CLKSTOP_EN_EN_17	R/W	0h	WKUP DMTIMER1 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.17 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.17 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
16	DM_CLKSTOP_EN_EN_16	R/W	0h	WKUP DMTIMER0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.16 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.16 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
15:4	RESERVED	NONE	0h	Reserved

Table 14-10835. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DM_CLKSTOP_EN_EN_3	R/W	0h	WKUP UART0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.3 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.3 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	DM_CLKSTOP_EN_EN_0	R/W	0h	WKUP I2C0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.0 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.0 reflects the IP clockstop_ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.283 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK Register

1 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK Register (Offset = 18490h) [reset = 0h]

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Table 14-10836. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8490h**

Figure 14-3603. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DM_CLKSTOP_ACK_ACK_17	DM_CLKSTOP_ACK_ACK_16
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DM_CLKSTOP_ACK_ACK_3	RESERVED		DM_CLKSTOP_ACK_ACK_0
NONE				R	NONE		R
0h				X	0h		X

Table 14-10838. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DM_CLKSTOP_ACK_ACK_17	R	X	WKUP DMTIMER1 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
16	DM_CLKSTOP_ACK_ACK_16	R	X	WKUP DMTIMER0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
15:4	RESERVED	NONE	0h	Reserved

Table 14-10838. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DM_CLKSTOP_ACK_ACK_3	R	X	WKUP UART0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	DM_CLKSTOP_ACK_ACK_0	R	X	WKUP I2C0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.284 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register

1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register (Offset = 184A0h) [reset = 0h]

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Table 14-10839. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 84A0h**

Figure 14-3604. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DM_GRP_CLKSTOP_REQ_REQ
NONE							R/W
0h							0h

Table 14-10841. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_REQ_REQ	R/W	0h	Assertion of Clockstop Req to IPs participating in Clockstop Req Group Field values (others are reserved): 1'b0 - Deassert CLKSTOP Req to all IPs participating in Clockstop Override Group 1'b1 - Assert CLKSTOP Req to all IPs participating in Clockstop Override Group Reset Source: mod_por_rst_n

14.2.1.1.3.2.285 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK Register

1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK Register (Offset = 184A4h) [reset = 0h]

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Table 14-10842. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 84A4h**

Figure 14-3605. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DM_GRP_CLKSTOP_ACK_ACK
NONE							R
0h							X

Table 14-10844. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_ACK_ACK	R	X	Status of IPs Participating in Clockstop Ack Group. If DM_CLKSTOP_EN is 0 (no IPs participating) this bit always reads 1. Field values (others are reserved): 1'b0 - At least one IP participating in Clockstop Override has not returned Ack 1'b1 - All IPs that are participating in Clockstop Override have returned Ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.286 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register (Offset = 18500h) [reset = 0h]

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Table 14-10845. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 8500h**

Figure 14-3606. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEVICE_TYPE_SMS_DEV_TYPE				RSVD			
R							
X				X			

Table 14-10847. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DEVICE_TYPE_SMS_DEV_TYPE	R	X	Reset Source: mod_por_rst_n

14.2.1.1.3.2.287 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-10848. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9008h**

Figure 14-3607. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-10850. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.288 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-10851. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 900Ch**

Figure 14-3608. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-10853. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.289 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10854. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9100h**

Figure 14-3609. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-10856. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.290 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10857. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9104h**

Figure 14-3610. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-10859. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.291 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10860. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9108h**

Figure 14-3611. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-10862. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.292 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-10863. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 910Ch**

Figure 14-3612. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-10865. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.293 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10866. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9110h**

Figure 14-3613. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-10868. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.294 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10869. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9114h**

Figure 14-3614. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5_READONLY							
R							
0h							

Table 14-10871. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.295 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register (Offset = 19118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10872. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9118h**

Figure 14-3615. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6_READONLY							
R							
0h							

Table 14-10874. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.296 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register (Offset = 1911Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-10875. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 911Ch**

Figure 14-3616. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7_READONLY							
R							
0h							

Table 14-10877. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.297 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register (Offset = 19120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10878. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9120h**

Figure 14-3617. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8_READONLY							
R							
0h							

Table 14-10880. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.298 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register (Offset = 19124h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10881. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9124h**

Figure 14-3618. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R9_READONLY							
R							
0h							

Table 14-10883. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R9_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.299 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register (Offset = 19128h) [reset = 0h]

Claim bits for Partition 6

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Table 14-10884. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 9128h**

Figure 14-3619. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R10_READONLY							
R							
0h							

Table 14-10886. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R10_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.300 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_PROXY Register (Offset = 1A040h) [reset = 0h]

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Table 14-10887. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A040h**

Figure 14-3620. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_PROXY Name Register

31	30	29	28	27	26	25	24
FW_CTRL_OUT0_FW_CTRL_OUT0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
FW_CTRL_OUT0_FW_CTRL_OUT0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
FW_CTRL_OUT0_FW_CTRL_OUT0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
FW_CTRL_OUT0_FW_CTRL_OUT0_PROXY							
R/W							
0h							

Table 14-10889. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FW_CTRL_OUT0_FW_CTRL_OUT0_PROXY	R/W	0h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.301 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET_PROXY Register (Offset = 1A044h) [reset = 0h]

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Table 14-10890. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A044h**

Figure 14-3621. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_SET_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.302 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR_PROXY Register (Offset = 1A048h) [reset = 0h]

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Table 14-10893. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A048h**

Figure 14-3622. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT0_CLR_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.303 WKUP_CTRL_MMR_CFG0_FW_STS_IN0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_STS_IN0_PROXY Register (Offset = 1A04Ch) [reset = 0h]

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Table 14-10896. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A04Ch**

Figure 14-3623. WKUP_CTRL_MMR_CFG0_FW_STS_IN0_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
X							
23	22	21	20	19	18	17	16
RSVD							
X							
15	14	13	12	11	10	9	8
RSVD							
X							
7	6	5	4	3	2	1	0
RSVD							
X							

14.2.1.1.3.2.304 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_PROXY Register (Offset = 1A050h) [reset = 0h]

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Table 14-10899. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A050h

Figure 14-3624. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.305 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET_PROXY Register (Offset = 1A054h) [reset = 0h]

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Table 14-10902. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A054h**

Figure 14-3625. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_SET_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.306 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR_PROXY Register (Offset = 1A058h) [reset = 0h]

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Table 14-10905. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A058h**

Figure 14-3626. WKUP_CTRL_MMR_CFG0_FW_CTRL_OUT1_CLR_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.1.3.2.307 WKUP_CTRL_MMR_CFG0_FW_STS_IN1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_FW_STS_IN1_PROXY Register (Offset = 1A05Ch) [reset = 0h]

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Table 14-10908. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A05Ch

Figure 14-3627. WKUP_CTRL_MMR_CFG0_FW_STS_IN1_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD							
X							
23	22	21	20	19	18	17	16
RSVD							
X							
15	14	13	12	11	10	9	8
RSVD							
X							
7	6	5	4	3	2	1	0
RSVD							
X							

14.2.1.1.3.2.308 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register (Offset = 1A080h) [reset = 10h]

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Table 14-10911. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A080h**

Figure 14-3628. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PMCTRL_SYS_PMIC_EN_WE_PROXY	PMCTRL_SYS_PMIC_EN_PROXY	PMCTRL_SYS_LPM_EN_WE_PROXY	PMCTRL_SYS_LPM_EN_PROXY		
NONE		R/W	R/W	R/W	R/W		
0h		0h	1h	0h	0h		

Table 14-10913. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PMCTRL_SYS_PMIC_EN_WE_PROXY	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
4	PMCTRL_SYS_PMIC_EN_PROXY	R/W	1h	Controls state of PMIC_LPM_EN_OUT when LPM_EN[2:0] is 000 Reset Source: mod_g_rst_n
3	PMCTRL_SYS_LPM_EN_WE_PROXY	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
2:0	PMCTRL_SYS_LPM_EN_PROXY	R/W	0h	Controls whether PMIC_LPM_EN_OUT is driven by the pmic_en bit, or by deep sleep logic. Field values (others are reserved): 3'b000 - PMIC_LPM_EN_OUT controlled by pmic_en bit. 3'b101 - PMIC_LPM_EN_OUT controlled by DeepSleep Logic Reset Source: mod_g_rst_n

14.2.1.1.3.2.309 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register (Offset = 1A084h) [reset = 0h]

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Table 14-10914. Instance Table

Instance Name	**Physical Address**
WKUP_CTRL_MMR0	**4301 A084h**

Figure 14-3629. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED						PMCTRL_IO_0_IO_ISO_STATUS_0_PROXY	PMCTRL_IO_0_IO_ISO_CTRL_0_PROXY
NONE						R	R/W
0h						X	0h
23	22	21	20	19	18	17	16
RESERVED							PMCTRL_IO_0_GLOBAL_WUEN_0_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PMCTRL_IO_0_WUCLK_STATUS_0_PROXY	PMCTRL_IO_0_WUCLK_CTRL_0_PROXY
NONE						R	R/W
0h						X	0h
7	6	5	4	3	2	1	0
RESERVED	PMCTRL_IO_0_ISOBYPASS_OVR_0_PROXY	PMCTRL_IO_0_IO_ON_STATUS_0_PROXY	PMCTRL_IO_0_ISOOVR_EXTEND_0_PROXY	RESERVED		PMCTRL_IO_0_ISOCLK_STATUS_0_PROXY	PMCTRL_IO_0_ISOCLK_OVRD_0_PROXY
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-10916. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	PMCTRL_IO_0_IO_ISO_STATUS_0_PROXY	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_0_IO_ISO_CTRL_0_PROXY	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved

Table 14-10916. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PMCTRL_IO_0_GLOBAL_WUEN_0_PROXY	R/W	0h	Global IO wakeup activate. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_0_WUCLK_STATUS_0_PROXY	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_0_WUCLK_CTRL_0_PROXY	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is activated. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_0_ISOBYPASS_OVR_0_PROXY	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_0_IO_ON_STATUS_0_PROXY	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_0_ISOOVR_EXTEND_0_PROXY	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to activate when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global activate/deactivate for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_0_ISOCLK_STATUS_0_PROXY	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_0_ISOCLK_OVRD_0_PROXY	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.310 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register (Offset = 1A088h) [reset = 0h]

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Table 14-10917. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A088h**

Figure 14-3630. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD						PMCTRL_IO_1_IO_ISO_STATUS_1_PROXY	PMCTRL_IO_1_IO_ISO_CTRL_1_PROXY
						R	R/W
X						X	0h

23	22	21	20	19	18	17	16
RESERVED							PMCTRL_IO_1_GLOBAL_WUEN_1_PROXY
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						PMCTRL_IO_1_WUCLK_STATUS_1_PROXY	PMCTRL_IO_1_WUCLK_CTRL_1_PROXY
NONE						R	R/W
0h						X	0h

7	6	5	4	3	2	1	0
RESERVED	PMCTRL_IO_1_ISOBYPASS_OVR_1_PROXY	PMCTRL_IO_1_IO_ON_STATUS_1_PROXY	PMCTRL_IO_1_ISOOVR_EXTEND_1_PROXY	RESERVED		PMCTRL_IO_1_ISOCLK_STATUS_1_PROXY	PMCTRL_IO_1_ISOCLK_OVRD_1_PROXY
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-10919. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
25	PMCTRL_IO_1_IO_ISO_STATUS_1_PROXY	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_1_IO_ISO_CTRL_1_PROXY	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PMCTRL_IO_1_GLOBAL_WUEN_1_PROXY	R/W	0h	Global IO wakeup activate. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n

Table 14-10919. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_1_WUCLK_STATUS_1_PROXY	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_1_WUCLK_CTRL_1_PROXY	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is activated. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_1_ISOBYPASS_OVR_1_PROXY	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_1_IO_ON_STATUS_1_PROXY	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_1_ISOOVR_EXTEND_1_PROXY	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to activate when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global activate/deactivate for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_1_ISOCLK_STATUS_1_PROXY	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_1_ISOCLK_OVRD_1_PROXY	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.311 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register (Offset = 1A090h) [reset = BC00h]

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Table 14-10920. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A090h**

Figure 14-3631. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Name Register

31	30	29	28	27	26	25	24
PMCTRL_MOSC_OSC_CG_ON_WFI_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PMCTRL_MOSC_SETUP_TIME_PROXY			
NONE				R/W			
0h				BC00h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMCTRL_MOSC_SETUP_TIME_PROXY							
R/W							
BC00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMCTRL_MOSC_SETUP_TIME_PROXY							
R/W							
BC00h							

Table 14-10922. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PMCTRL_MOSC_OSC_CG_ON_WFI_PROXY	R/W	0h	When set by Device Manager - the soc clock gating logic will gate the device manager clock once Device Manager has entered the WFI state. (Note: this was named osc_cg_dis but name didn't match function) Reset Source: mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:0	PMCTRL_MOSC_SETUP_TIME_PROXY	R/W	BC00h	Keep the main oscillator clock gates for the number of HFOSC clock cycles This is the time it takes to stabilize the clock source supplier (i.e. Main Oscillator) Reset Source: mod_g_rst_n

14.2.1.1.3.2.312 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register (Offset = 1A098h) [reset = 0h]

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Table 14-10923. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A098h**

Figure 14-3632. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PM_MISC_STATUS_OSC_CG_STAT_PROXY	
NONE						R	
0h						X	

Table 14-10925. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PM_MISC_STATUS_OSC_CG_STAT_PROXY	R	X	Reflects the status of the request to clock-gate HF oscillator via MMR PMCTRL_MOSCundefined. 11: osc_cgen_req = '0' & osc_cgen_ack = '1' 10: osc_cgen_req = '1' & osc_cgen_ack = '0' 01: osc_cgen_req = '0' & osc_cgen_ack = '0' 00: osc_cgen_req = '1' & osc_cgen_ack = '1' Reset Source: mod_g_rst_n

14.2.1.1.3.2.313 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB_PROXY Register (Offset = 1A09Ch) [reset = 0h]

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Table 14-10926. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A09Ch**

Figure 14-3633. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PMCTRL_IO_GLB_DSEN_QUALIFIED_PROXY	
NONE						R/W	
0h						0h	

Table 14-10928. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_GLB_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PMCTRL_IO_GLB_DSEN_QUALIFIED_PROXY	R/W	0h	To dsen_qualified signal generation logic for daisychain[1:0] logic. Used to control I/O buffer ouput and output activate during deepsleep mode. See IO Integration spec for detail. Reset Source: mod_g_rst_n

14.2.1.1.3.2.314 WKUP_CTRL_MMR_CFG0_PM_PERMISSION_PROXY Register

1 WKUP_CTRL_MMR_CFG0_PM_PERMISSION_PROXY Register (Offset = 1A0A0h) [reset = 0h]

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Table 14-10929. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A0A0h**

Figure 14-3634. WKUP_CTRL_MMR_CFG0_PM_PERMISSION_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PM_PERMISSION_MCU_SAFETY_ACTIVE_PROXY	PM_PERMISSION_SECURITY_ACTIVE_PROXY	PM_PERMISSION_DEBUG_ACTIVE_PROXY
NONE					R	R	R
0h					X	X	X

Table 14-10931. WKUP_CTRL_MMR_CFG0_PM_PERMISSION_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	PM_PERMISSION_MCU_SAFETY_ACTIVE_PROXY	R	X	Read Only - Reads return a 1 when am62_mcu_ctrl_mmr.wkup_0.RST_MAGIC_WORD_mcu_magic_word_ipcfg[31:0] != 32'h0. When 1, indicates that the MCU is blocking reset and also deep sleep entry. Reset Source: mod_g_rst_n
1	PM_PERMISSION_SECURITY_ACTIVE_PROXY	R	X	Read Only - Reads return the value of ms.main_0.sms_iopm_pmpermission_security_active. When 1, indicates that SMS is blocking deep sleep entry. Reset Source: mod_g_rst_n
0	PM_PERMISSION_DEBUG_ACTIVE_PROXY	R	X	Read Only - Returns a 1 when IceMelter is blocking deep sleep entry. Reset Source: mod_g_rst_n

14.2.1.1.3.2.315 WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL_PROXY Register (Offset = 1A160h) [reset = 0h]

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Table 14-10932. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A160h**

Figure 14-3635. WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							DEEPSLEEP_CTRL_FORCE_DS_MAIN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							DEEPSLEEP_CTRL_FORCE_DS_WKUP_PROXY
NONE							R/W
0h							0h

Table 14-10934. WKUP_CTRL_MMR_CFG0_DEEPSLEEP_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	DEEPSLEEP_CTRL_FORCE_DS_MAIN_PROXY	R/W	0h	Force all MAIN IOs into deepsleep mode when set Reset Source: mod_por_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DEEPSLEEP_CTRL_FORCE_DS_WKUP_PROXY	R/W	0h	Force all WKUP IOs into deepsleep mode when set Reset Source: mod_por_rst_n

14.2.1.1.3.2.316 WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 200FFh]

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Table 14-10935. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A170h**

Figure 14-3636. WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST_CTRL_SW_MAIN_POR_PROXY				RST_CTRL_SW_MAIN_WARMRST_PROXY			
R/W				R/W			
Fh				Fh			

Table 14-10937. WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	R/W	0h	Main Domain CPUs can set this bit to block warm reset in the main domain which is useful when the Main domain may be accessing main domain resources (peripherals, memory..). In this case, the main domain cpus will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, Main needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0 - Reset of Main Domain is not Blocked by Main Domain 1 - Reset of Main Domain is Blocked by Main Domain Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Deactivate Reset of Main by ESM 0 - Activated 1 - Deactivated Reset Source: main_chip1_rst_n

Table 14-10937. WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY	R/W	0h	Deactivate Reset of Main by SMS 0 - Activated 1 - Deactivated Reset Source: main_chip1_rst_n
15:8	RESERVED	NONE	0h	Reserved
7:4	RST_CTRL_SW_MAIN_POR_PROXY	R/W	Fh	Causes Main Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST_PROXY	R/W	Fh	Causes Main Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.3.2.317 WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

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Table 14-10938. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A174h**

Figure 14-3637. WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY
NONE							R
0h							X

Table 14-10940. WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY	R	X	is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding Reset Source: main_chip1_rst_n

14.2.1.1.3.2.318 WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register

1 WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

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Table 14-10941. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A178h**

Figure 14-3638. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY
R	R	NONE				R	R
X	X	0h				X	X
23	22	21	20	19	18	17	16
RESERVED	RST_SRC_DM_WDT_RST_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
NONE	R	R	R	NONE			R
0h	X	X	X	0h			X
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R	R	NONE			R
0h		X	X	0h			X
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST_PROXY	RESERVED	RST_SRC_MAIN_RESET_REQ_PROXY	RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE			R	NONE	R	NONE	R
0h			X	0h	X	0h	X

Table 14-10943. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R	X	Reset Caused by MCU ESM Error Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R	X	Reset Caused by Main ESM Error Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	R	X	Software Main Power On Reset From MAIN CTRL MMR Reset Source: main_chip1_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY	R	X	Software Main Power On Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
23	RESERVED	NONE	0h	Reserved
22	RST_SRC_DM_WDT_RST_PROXY	R	X	Watchdog Initiated Reset Reset Source: main_chip1_rst_n

Table 14-10943. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	R	X	Software Main Warm Reset from MAIN CTRL MMR Reset Source: main_chip1_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	R	X	Software Main Warm Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R	X	Software Warm Reset Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST_PROXY	R	X	SMS Warm Reset Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R	X	SMS Cold Reset Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R	X	Debug Subsystem Initiated Reset Reset Source: main_chip1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R	X	Thermal Reset Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ_PROXY	R	X	Main Reset Pin Reset Source: main_chip1_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R	X	Rest Caused by MCU Reset Pin Reset Source: main_chip1_rst_n

14.2.1.1.3.2.319 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register

1 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register (Offset = 1A17Ch) [reset = 0h]

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Table 14-10944. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A17Ch**

Figure 14-3639. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							

Table 14-10946. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.3.2.320 WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register (Offset = 1A180h) [reset = 0h]

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Table 14-10947. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A180h**

Figure 14-3640. WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							

Table 14-10949. WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WKUP0_EN_WKUPEN_PROXY	R/W	0h	Activates Wakeup from: b0 - WKUP I2C0 b1 - WKUP USART0 b2 - MCU GPIO0 b3 - DEBUG (IceMelter) b4 - Reserved b5 - WKUP DMTIMER0 b6 - WKUP DMTIMER1 b7 - WKUP RTC b8 - Main RESET_REQz b9 - USB0 In Band b10 - USB1 In Band b16 - MAIN IO Daisy Chain b17 - MCU IO Daisy Chain b18 - CANUART IO Daisy Chain Reset Source: mod_g_rst_n

14.2.1.1.3.2.321 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register (Offset = 1A280h) [reset = Eh]

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Table 14-10950. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A280h**

Figure 14-3641. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
CLKGATE_CTRL0_MAIN_SMS_NOGATE_PROXY	RESERVED	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DBGCBA_NOGATE_PROXY	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED	RSVD	RESERVED		CLKGATE_CTRL0_MAIN_PDMA2_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY
NONE		NONE		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

15	14	13	12	11	10	9	8
CLKGATE_CTRL0_MAIN_GIC500_NOGATE_PROXY	RESERVED	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_MCASP_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE_PROXY
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CLKGATE_CTRL0_MAIN_A53_0_NOGATE_PROXY	RESERVED	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE_PROXY	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE_PROXY	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	1h	1h	0h

Table 14-10952. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKGATE_CTRL0_MAIN_SMS_NOGATE_PROXY	R/W	0h	MAIN domain SMS (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE_PROXY	R/W	0h	MAIN domain SA3SS clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

Table 14-10952. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Debug CBA (main_dbg_cba)clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
27:23	RESERVED	NONE	0h	Reserved
21:20	RESERVED	NONE	0h	Reserved
19	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE_PROXY	R/W	0h	MAIN domain PDMA2 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
18	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	R/W	0h	MAIN domain PDMA1 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
17	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	R/W	0h	MAIN domain PDMA0 (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
16	CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY	R/W	0h	MAIN domain DMSS (pwr_dis_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
15	CLKGATE_CTRL0_MAIN_GIC500_NOGATE_PROXY	R/W	0h	MAIN A53SS0 (gic500_1_2) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
14	RESERVED	NONE	0h	Reserved
13	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (main_ipcss_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
12	CLKGATE_CTRL0_MAIN_MCASP_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (main_mcasp_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
11	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (main_misc_peri_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
10	CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE_PROXY	R/W	0h	MAIN A53SS0 Debug Port clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
9	CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE_PROXY	R/W	0h	MAIN A53SS0 Configuration Port clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

Table 14-10952. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE_PROXY	R/W	0h	MAIN A53SS0 ACP clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
7	CLKGATE_CTRL0_MAIN_A53_0_NOGATE_PROXY	R/W	0h	MAIN A53SS0 clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
6	RESERVED	NONE	0h	Reserved
5	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	R/W	0h	MAIN domain datal bus (main_fw_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
4	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE_PROXY	R/W	0h	MAIN domain data bus (main_cbass) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
3	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE_PROXY	R/W	1h	WKUP domain Infrastructure ECC aggregator(wkup_safe_ecc_aggr) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
2	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE_PROXY	R/W	1h	WKUP domain Device Manager (wkup_dm_pwr_nogate) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
1	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE_PROXY	R/W	1h	WKUP domain device manager CBA clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
0	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (main_infra_cbass and psc_fw_ch_br) clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.3.2.322 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register (Offset = 1A284h) [reset = 0h]

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Table 14-10953. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A284h**

Figure 14-3642. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKGATE_CTRL1_VPAC0_NOGATE_PROXY	RESERVED			CLKGATE_CTRL1_C7X_NOGATE_PROXY	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKGATE_CTRL1_JPEG_ENC_NOGATE_PROXY	RESERVED			CLKGATE_CTRL1_VIDEO_CODEC_NOGATE_PROXY	RESERVED		CLKGATE_CTRL1_DMSS_CSI_NOGATE_PROXY
R/W	NONE			R/W	NONE		R/W
0h	0h			0h	0h		0h

Table 14-10955. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLKGATE_CTRL1_VPAC0_NOGATE_PROXY	R/W	0h	VPAC0 clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLKGATE_CTRL1_C7X_NOGATE_PROXY	R/W	0h	C7x clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLKGATE_CTRL1_JPEG_ENC_NOGATE_PROXY	R/W	0h	JPEG Encoder clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved

Table 14-10955. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLKGATE_CTRL1_VIDEO_CODEC_NOGATE_PROXY	R/W	0h	VIDEO CODEC clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CLKGATE_CTRL1_DMSS_CSI_NOGATE_PROXY	R/W	0h	DMSS_CSI clock gate deactivate. 0 - Clocks are gated on idle for power savings 1 - Clocks are not gated on idle, power saving deactivated Reset Source: mod_por_rst_n

14.2.1.1.3.2.323 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register (Offset = 1A300h) [reset = 0h]

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Table 14-10956. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A300h**

Figure 14-3643. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_CTRL_MW_PROXY							CANUART_WAKE_CTRL_MW_LOAD_EN_PROXY
R/W							R/W
0h							0h

Table 14-10958. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_CTRL_MW_PROXY	R/W	0h	CANUART IO magic word. This 31-bit value that activates placing of the CANUART I/Os into isolation for daisy-chain wakeup operation. The Upper 8 bits are software defined. The lower 23 bits are checked by hardware: - 0x5AAAAA - Magic word value to activate isolation whenqualified with mw_load bit - Others - Any other value will prevent isolation when mw_loadtransitions from 0 to 1 Reset Source: mcu_chip1_rst_n
0	CANUART_WAKE_CTRL_MW_LOAD_EN_PROXY	R/W	0h	Magic word load activate Setting this bit to 1 loads and locks the mw field for CANUART IO isolation. If the mw field matches the magicword value then the value is latched into the CANUART IO voltage domain and CANUART IO isolation is activated. 0 - Unlock and do not load mw value for comparison 1 - Load and lock mw for magic word value comparison Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.324 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register (Offset = 1A308h) [reset = 0h]

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Table 14-10959. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A308h**

Figure 14-3644. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_STAT0_MW_STAT_PROXY							CANUART_WAKE_STAT0_MW_LOAD_STAT_PROXY
R							R
X							X

Table 14-10961. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_STAT0_MW_STAT_PROXY	R	X	CANUART magic word status Indicates the latched value of the mw field. Reset Source: mod_por_rst_n
0	CANUART_WAKE_STAT0_MW_LOAD_STAT_PROXY	R	X	Magic word load status. Indicates the latched value of the mw_load_en bit Reset Source: mod_por_rst_n

14.2.1.1.3.2.325 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register (Offset = 1A30Ch) [reset = 0h]

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Table 14-10962. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A30Ch**

Figure 14-3645. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CANUART_WAKE_STAT1_CANUART_IO_MODE_PROXY
NONE							R
0h							X

Table 14-10964. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CANUART_WAKE_STAT1_CANUART_IO_MODE_PROXY	R	X	Indicates if CANUART IO wakeup mode is activated. 0 - Not activated (load_en not set or mw doesn't match magic word) 1 - CANUART IO mode activated Reset Source: mod_por_rst_n

14.2.1.1.3.2.326 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register (Offset = 1A310h) [reset = 0h]

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Table 14-10965. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A310h**

Figure 14-3646. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							

Table 14-10967. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_MW_PROXY	R/W	0h	magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.327 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register (Offset = 1A318h) [reset = 0h]

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Table 14-10968. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A318h**

Figure 14-3647. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							

Table 14-10970. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_STAT_MW_PROXY	R	X	returned magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.328 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register (Offset = 1A320h + formula) [reset = 0h]

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Offset = 1A320h + (j * 4h); where j = 0 to 3d

Table 14-10971. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A320h + formula**

Figure 14-3648. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEYVAL_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEYVAL_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEYVAL_PROXY							
R/W							
0h							

Table 14-10973. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL_PROXY	R/W	0h	key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.329 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register

1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register (Offset = 1A340h + formula) [reset = 0h]

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Offset = 1A340h + (j * 4h); where j = 0 to 3d

Table 14-10974. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A340h + formula**

Figure 14-3649. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL_PROXY							
R							
X							
23	22	21	20	19	18	17	16
KEYVAL_PROXY							
R							
X							
15	14	13	12	11	10	9	8
KEYVAL_PROXY							
R							
X							
7	6	5	4	3	2	1	0
KEYVAL_PROXY							
R							
X							

Table 14-10976. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL_PROXY	R	X	returned key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.330 WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register (Offset = 1A400h) [reset = 0h]

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Table 14-10977. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A400h**

Figure 14-3650. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			WFI_STATUS_A53SS0_CPU3_WFI_PROXY	WFI_STATUS_A53SS0_CPU2_WFI_PROXY	WFI_STATUS_A53SS0_CPU1_WFI_PROXY	WFI_STATUS_A53SS0_CPU0_WFI_PROXY	RESERVED
NONE			R	R	R	R	NONE
0h			X	X	X	X	0h
7	6	5	4	3	2	1	0
RESERVED			WFI_STATUS_MCU_R5F_WFI_PROXY	WFI_STATUS_SMS_CPU1_WFI_PROXY	WFI_STATUS_SMS_CPU0_WFI_PROXY	RESERVED	WFI_STATUS_PULSAR_UL0_WFI_PROXY
NONE			R	R	R	NONE	R
0h			X	X	X	0h	X

Table 14-10979. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	WFI_STATUS_A53SS0_CPU3_WFI_PROXY	R	X	WFI status of A53SS0 CPU3 Reset Source: mod_por_rst_n
11	WFI_STATUS_A53SS0_CPU2_WFI_PROXY	R	X	WFI status of A53SS0 CPU2 Reset Source: mod_por_rst_n
10	WFI_STATUS_A53SS0_CPU1_WFI_PROXY	R	X	WFI status of A53SS0 CPU1 Reset Source: mod_por_rst_n
9	WFI_STATUS_A53SS0_CPU0_WFI_PROXY	R	X	WFI status of A53SS0 CPU0 Reset Source: mod_por_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	WFI_STATUS_MCU_R5F_WFI_PROXY	R	X	WFI status of MCU Cortex R5F Reset Source: mod_por_rst_n
3	WFI_STATUS_SMS_CPU1_WFI_PROXY	R	X	WFI status of SMS Cortex M4F1 Reset Source: mod_por_rst_n
2	WFI_STATUS_SMS_CPU0_WFI_PROXY	R	X	WFI status of SMS Cortex M4F0 Reset Source: mod_por_rst_n

Table 14-10979. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	NONE	0h	Reserved
0	WFI_STATUS_PULSAR_UL0_WFI_PROXY	R	X	WFI status of Device Manager Cortex R5F Reset Source: mod_por_rst_n

14.2.1.1.3.2.331 WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY Register

1 WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY Register (Offset = 1A410h) [reset = 0h]

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Table 14-10980. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A410h**

Figure 14-3651. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
SLEEP_STATUS_EXITED_SLEEP_PROXY	RESERVED		SLEEP_STATUS_MAIN_DS_PROXY	RESERVED			
R/W1TC	NONE		R/W1TC	NONE			
0h	0h		0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							SLEEP_STATUS_MAIN_RESETSTATZ_PROXY
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED							RSVD
NONE							
0h							X

Table 14-10982. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SLEEP_STATUS_EXITED_SLEEP_PROXY	R/W1TC	0h	Set when the HFXOSC clock gate is activated (rising edge capture of OSC_CG_ACK). To be read and cleared by DM after exiting WFI as a status signal distinguishing the case where WFI was entered and the clock was stopped, then exited with a wakeup (this bit will be set) from the case where an interrupt or other event caused the WFI sequence to stop and the HFXOSC was never stopped. Reset Source: sys_por_rst_n
30:29	RESERVED	NONE	0h	Reserved
28	SLEEP_STATUS_MAIN_DS_PROXY	R/W1TC	0h	Set when the main domain deep sleep power on reset / power domain off is activated. (rising edge detect of am62_wkup_ctrl_mmr.wkup_0.DS_MAIN_por_pdoff_ft_out_ipcfg). This will be checked by the ROM on TIFS upon exiting from reset to determine if it is a power on reset or exiting deep sleep. Reset Source: sys_por_rst_n
27:9	RESERVED	NONE	0h	Reserved

Table 14-10982. WKUP_CTRL_MMR_CFG0_SLEEP_STATUS_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SLEEP_STATUS_MAIN_RESETSTATZ_PROXY	R	X	Reflects the status of the main domain resetz signal Field values (others are reserved): 1'b0 - Main Domain In Reset 1'b1 - Main Domain Out of Reset Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.332 WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD_PROXY Register (Offset = 1A418h) [reset = 0h]

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Table 14-10983. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A418h**

Figure 14-3652. WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD_PROXY Name Register

31	30	29	28	27	26	25	24
DS_MAGIC_WORD_DS_MAGIC_WORD_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
DS_MAGIC_WORD_DS_MAGIC_WORD_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
DS_MAGIC_WORD_DS_MAGIC_WORD_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
DS_MAGIC_WORD_DS_MAGIC_WORD_PROXY							
R/W							
0h							

Table 14-10985. WKUP_CTRL_MMR_CFG0_DS_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DS_MAGIC_WORD_DS_MAGIC_WORD_PROXY	R/W	0h	Magic Word Indicating State of Deep Sleep Reset Source: main_chip1_rst_n

14.2.1.1.3.2.333 WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register (Offset = 1A420h) [reset = Fh]

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Table 14-10986. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A420h**

Figure 14-3653. WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_MAIN_POR_PDOFF_PROXY			
NONE				R/W			
0h				Fh			

Table 14-10988. WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_MAIN_POR_PDOFF_PROXY	R/W	Fh	Signal Puts main SMS, DebugSS and MainIP Power Domains into Power Off state, and asserts Main Power On Reset. Field values (others are reserved): 4'b0110 - Off 4'b1111 - On Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.334 WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register (Offset = 1A440h) [reset = Fh]

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Table 14-10989. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A440h**

Figure 14-3654. WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_DM_RESET_MASK_PROXY			
NONE				R/W			
0h				Fh			

Table 14-10991. WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_DM_RESET_MASK_PROXY	R/W	Fh	Signal used to mask main domain resets from Device Manager / Wakeup and MCU Ips Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.335 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register (Offset = 1A460h) [reset = Fh]

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Table 14-10992. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A460h**

Figure 14-3655. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB0_RESET_MASK_PROXY			
NONE				R/W			
0h				Fh			

Table 14-10994. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB0_RESET_MASK_PROXY	R/W	Fh	Signal used to block reset to the USBSS0 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.336 WKUP_CTRL_MMR_CFG0_DS_USB1_RESET_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DS_USB1_RESET_PROXY Register (Offset = 1A464h) [reset = Fh]

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Table 14-10995. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A464h**

Figure 14-3656. WKUP_CTRL_MMR_CFG0_DS_USB1_RESET_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB1_RESET_MASK_PROXY			
NONE				R/W			
0h				Fh			

Table 14-10997. WKUP_CTRL_MMR_CFG0_DS_USB1_RESET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB1_RESET_MASK_PROXY	R/W	Fh	Signal used to block reset to the USBSS1 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.337 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY Register (Offset = 1A480h) [reset = 0h]

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Table 14-10998. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A480h**

Figure 14-3657. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED						DM_CLKSTOP_EN_EN_17_PROXY	DM_CLKSTOP_EN_EN_16_PROXY
NONE						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				DM_CLKSTOP_EN_EN_3_PROXY	RESERVED		DM_CLKSTOP_EN_EN_0_PROXY
NONE				R/W	NONE		R/W
0h				0h	0h		0h

Table 14-11000. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DM_CLKSTOP_EN_EN_17_PROXY	R/W	0h	WKUP DMTIMER1 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.17 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.17 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
16	DM_CLKSTOP_EN_EN_16_PROXY	R/W	0h	WKUP DMTIMER0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.16 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.16 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
15:4	RESERVED	NONE	0h	Reserved

Table 14-11000. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_EN_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DM_CLKSTOP_EN_EN_3_PROXY	R/W	0h	WKUP UART0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.3 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.3 reflects the IP clockstop_ack Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	DM_CLKSTOP_EN_EN_0_PROXY	R/W	0h	WKUP I2C0 Participation in Clockstop Req Group Field values (others are reserved): 1'b0 - Not Participating in Clockstop Override Group. DM_CLKSTOP_ACK.0 always reads '1' 1'b1 - Participating in Clockstop Override Group. DM_CLKSTOP_ACK.0 reflects the IP clockstop_ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.338 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY Register (Offset = 1A490h) [reset = 0h]

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Table 14-11001. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A490h**

Figure 14-3658. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>DM_CLKSTOP_ACK_ACK_17_PROXY</td><td>DM_CLKSTOP_ACK_ACK_16_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>DM_CLKSTOP_ACK_ACK_3_PROXY</td><td colspan="2">RESERVED</td><td>DM_CLKSTOP_ACK_ACK_0_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>X</td><td colspan="2">0h</td><td>X</td></tr>
</table>

Table 14-11003. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DM_CLKSTOP_ACK_ACK_17_PROXY	R	X	WKUP DMTIMER1 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
16	DM_CLKSTOP_ACK_ACK_16_PROXY	R	X	WKUP DMTIMER0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
15:4	RESERVED	NONE	0h	Reserved

Table 14-11003. WKUP_CTRL_MMR_CFG0_DM_CLKSTOP_ACK_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DM_CLKSTOP_ACK_ACK_3_PROXY	R	X	WKUP UART0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	DM_CLKSTOP_ACK_ACK_0_PROXY	R	X	WKUP I2C0 Clockstop Ack Status Field values (others are reserved): 1'b0 - IP is Participating in Clockstop Override Group, and IP clockstop_ack is 0 1'b1 - IP Is either not Participating in Clockstop Override Group, or IP has returned IP clockstop_ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.339 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register (Offset = 1A4A0h) [reset = 0h]

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Table 14-11004. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A4A0h**

Figure 14-3659. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DM_GRP_CLKSTOP_REQ_PROXY
NONE							R/W
0h							0h

Table 14-11006. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_REQ_PROXY	R/W	0h	Assertion of Clockstop Req to IPs participating in Clockstop Req Group Field values (others are reserved): 1'b0 - Deassert CLKSTOP Req to all IPs participating in Clockstop Override Group 1'b1 - Assert CLKSTOP Req to all IPs participating in Clockstop Override Group Reset Source: mod_por_rst_n

14.2.1.1.3.2.340 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK_PROXY Register (Offset = 1A4A4h) [reset = 0h]

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Table 14-11007. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A4A4h**

Figure 14-3660. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DM_GRP_CLKSTOP_ACK_ACK_PROXY
NONE							R
0h							X

Table 14-11009. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_ACK_ACK_PROXY	R	X	Status of IPs Participating in Clockstop Ack Group. If DM_CLKSTOP_EN is 0 (no IPs participating) this bit always reads 1. Field values (others are reserved): 1'b0 - At least one IP participating in Clockstop Override has not returned Ack 1'b1 - All IPs that are participating in Clockstop Override have returned Ack Reset Source: mod_por_rst_n

14.2.1.1.3.2.341 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register

1 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register (Offset = 1A500h) [reset = 0h]

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Table 14-11010. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 A500h**

Figure 14-3661. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEVICE_TYPE_SMS_DEV_TYPE_PROXY				RSVD			
R							
X				X			

Table 14-11012. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DEVICE_TYPE_SMS_DEV_TYPE_PROXY	R	X	Reset Source: mod_por_rst_n

14.2.1.1.3.2.342 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-11013. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B008h**

Figure 14-3662. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-11015. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.343 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-11016. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B00Ch**

Figure 14-3663. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-11018. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.344 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-11019. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B100h**

Figure 14-3664. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-11021. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.345 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-11022. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B104h**

Figure 14-3665. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11024. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.346 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-11025. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B108h**

Figure 14-3666. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-11027. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.347 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-11028. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B10Ch**

Figure 14-3667. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-11030. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.348 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-11031. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B110h**

Figure 14-3668. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-11033. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.349 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-11034. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B114h**

Figure 14-3669. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5							
R/W							
0h							

Table 14-11036. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.350 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register (Offset = 1B118h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-11037. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B118h**

Figure 14-3670. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6							
R/W							
0h							

Table 14-11039. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.351 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register (Offset = 1B11Ch) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-11040. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B11Ch**

Figure 14-3671. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7							
R/W							
0h							

Table 14-11042. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.352 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register (Offset = 1B120h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-11043. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B120h**

Figure 14-3672. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8							
R/W							
0h							

Table 14-11045. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.353 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register (Offset = 1B124h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-11046. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B124h**

Figure 14-3673. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R9							
R/W							
0h							

Table 14-11048. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R9	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.354 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register (Offset = 1B128h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-11049. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 B128h**

Figure 14-3674. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R10							
R/W							
0h							

Table 14-11051. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R10	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.355 WKUP_CTRL_MMR_CFG0_BACKUP_REG_j Register

1 WKUP_CTRL_MMR_CFG0_BACKUP_REG_j Register (Offset = 1C100h + formula) [reset = 0h]

Return to Summary Table

Offset = 1C100h + (j * 4h); where j = 0 to 23d

Table 14-11052. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 C100h + formula**

Figure 14-3675. WKUP_CTRL_MMR_CFG0_BACKUP_REG_j Name Register

31	30	29	28	27	26	25	24
BACKUP_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
BACKUP_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
BACKUP_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
BACKUP_DATA							
R/W							
0h							

Table 14-11054. WKUP_CTRL_MMR_CFG0_BACKUP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BACKUP_DATA	R/W	0h	Storage for Backup Data During Deep Sleep Reset Source: mod_por_rst_n

14.2.1.1.3.2.356 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register

1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register (Offset = 1D008h) [reset = 0h]

- KICK0 component

Return to Summary Table

Table 14-11055. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 D008h**

Figure 14-3676. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK0							
R/W							
0h							

Table 14-11057. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.357 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register

1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register (Offset = 1D00Ch) [reset = 0h]

- KICK1 component

Return to Summary Table

Table 14-11058. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 D00Ch**

Figure 14-3677. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK1							
R/W							
0h							

Table 14-11060. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.358 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register (Offset = 1D100h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11061. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 D100h**

Figure 14-3678. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R0_READONLY							
R							
0h							

Table 14-11063. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R0_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.359 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register (Offset = 1D104h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11064. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 D104h**

Figure 14-3679. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R1_READONLY							
R							
0h							

Table 14-11066. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R1_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.360 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register (Offset = 1D108h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11067. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 D108h**

Figure 14-3680. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R2_READONLY							
R							
0h							

Table 14-11069. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R2_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.361 WKUP_CTRL_MMR_CFG0_BACKUP_REG_PROXY_j Register

1 WKUP_CTRL_MMR_CFG0_BACKUP_REG_PROXY_j Register (Offset = 1E100h + formula) [reset = 0h]

Return to Summary Table

Offset = 1E100h + (j * 4h); where j = 0 to 23d

Table 14-11070. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 E100h + formula**

Figure 14-3681. WKUP_CTRL_MMR_CFG0_BACKUP_REG_PROXY_j Name Register

31	30	29	28	27	26	25	24
BACKUP_DATA_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
BACKUP_DATA_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
BACKUP_DATA_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
BACKUP_DATA_PROXY							
R/W							
0h							

Table 14-11072. WKUP_CTRL_MMR_CFG0_BACKUP_REG_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BACKUP_DATA_PROXY	R/W	0h	Storage for Backup Data During Deep Sleep Reset Source: mod_por_rst_n

14.2.1.1.3.2.362 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register (Offset = 1F008h) [reset = 0h]

- KICK0 component

Return to Summary Table

Table 14-11073. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 F008h**

Figure 14-3682. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK0_PROXY							
R/W							
0h							

Table 14-11075. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.363 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register

1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register (Offset = 1F00Ch) [reset = 0h]

- KICK1 component

Return to Summary Table

Table 14-11076. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 F00Ch**

Figure 14-3683. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK1_PROXY							
R/W							
0h							

Table 14-11078. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.364 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register (Offset = 1F100h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11079. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 F100h**

Figure 14-3684. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11081. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R0	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.365 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register (Offset = 1F104h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11082. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 F104h**

Figure 14-3685. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R1							
R/W							
0h							

Table 14-11084. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R1	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.366 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register

1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register (Offset = 1F108h) [reset = 0h]

Claim bits for Partition 7

Return to Summary Table

Table 14-11085. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	**4301 F108h**

Figure 14-3686. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11087. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R2	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.2 Pad Configuration Registers

14.2.1.2.1 Pad Configuration Register Functional Description

The pad configuration registers are used to configure most of the device pads. Each pad configuration register is associated only with one pad and has bits as described in Table 14-7402.

Table 14-11088. Description Of The Pad Configuration Register Bits

Bit	Field	Type	Reset	Description

31	LOCK	R/W	(1)	Pad configuration register lock bit.
				`0h - The corresponding pad configuration register is unlocked. Its value can be modified. Further writes are allowed.`
				`1h - The corresponding pad configuration register is locked. Its value can not be modified. Further writes are not allowed.`
				Once the padconfig is locked a reset is the only allowed option to modify the padconfig.
				The lock bit can be reset only by PORz (MCU and Main Domain cold reset) event.

Table 14-11088. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description
30	WKUP_EVT	R/W	(1)	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	(1)	Wakeup enable 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	(1)	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	(1)	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	(1)	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	(1)	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	(1)	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	(1)	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed During Deepsleep mode and IO+DDR mode, we can configure IOs to generate a wake-up event to exit the low power mode. In this mode IOs go into low power retention state (driver is disabled and receiver is ON) and are hooked up in a daisy chain. If you do not want a particular IO to enter this mode, you can program ISO_BYP to bypass this mode.
22	RESERVED	R/W		Reserved
21	TX_DIS[3]	R/W	(1)	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20 - 19	DRV_STR[4]	R/W	(1)	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) 0h - Nominal 1h - Reserved 2h - Fast 3h - Reserved **Note** The nominal (default) DRV_STR settings should be used to ensure timings, unless specific instructions are given otherwise.
18	RXACTIVE[5]	R/W	(1)	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled

Table 14-11088. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description
17	PULLTYPESEL(2)	R/W	(1)	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN(2)	R/W	(1)	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	(1)	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	(1)	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13 - 11	DEBOUNCE_SEL	R/W	(1)	Selects the debounce period for select input signals. See I/O Debounce Control Registers for more information. 0h - Deactivated 1h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 2h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 3h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 4h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 5h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 6h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 7h - Reserved
10 - 9	RESERVED	R/W	0	Reserved
8	WK_LVL_POL	R/W	(1)	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1h. 0h - Low. A low (0) value on the pin causes a wakeup 1h - High. A high (1) value on the pin causes a wakeup
7	WK_LVL_EN	R/W	(1)	Level Sensitive Wakeup Enable 0h - Disabled. Wakeup is triggered by change of the pin input value 1h - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed)
6 - 4	RESERVED	R/W	0	Reserved
3 - 0	MUXMODE	R/W	(1)	Pad functional signal mux selection Field values (others are reserved): 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

(1) See *Pad Configuration Registers* for reset values for Pad Configuration registers.

(2) These bits do not apply to "I2C OD FS" buffer types as these IOs do not have internal pull registers.

(3) To prevent unwanted glitches, software should disable the output driver by setting the TX_DIS bit before writing a new MUXMODE value. Once the new MUXMODE value is written, the TX_DIS bit can be reset in order to re-enable the pin driver.

(4) Use of settings other than the reset value could invalidate datasheet timings.

(5) The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is very important since a floating input may damage the device.

Many of the device pads support pad multiplexing. This means that their function can be independently chosen from two or more options. The selection of functions available on each pad is enumerated in table “*Pin Multiplexing*” of the device-specific Datasheet. The desired function is selected via the MUXMODE field of the associated pad configuration register.

14.2.1.2.2 Pad Configuration PADCONFIG Registers

Table 14-11089. AM62D PADCONFIG Registers

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21](1)	DRV_STR[20:19](2)	RXACTIVE[18](3)	PULLTYPESEL[17](4)	PULLUDEN[16](4)	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG0	OSPI0_CLK		F4000h	F6000h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG1	OSPI0_LBCLKO		F4004h	F6004h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG2	OSPI0_DQS		F4008h	F6008h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG3	OSPI0_D0		F400Ch	F600Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG4	OSPI0_D1		F4010h	F6010h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG5	OSPI0_D2		F4014h	F6014h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG6	OSPI0_D3		F4018h	F6018h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG7	OSPI0_D4		F401Ch	F601Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG8	OSPI0_D5		F4020h	F6020h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG9	OSPI0_D6		F4024h	F6024h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG10	OSPI0_D7		F4028h	F6028h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG11	OSPI0_CSn0		F402Ch	F602Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG12	OSPI0_CSn1		F4030h	F6030h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG13	OSPI0_CSn2	GPIO0_13	F4034h	F6034h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG14	OSPI0_CSn3	GPIO0_14	F4038h	F6038h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG15	GPMC0_AD0		F403Ch	F603Ch	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG16	GPMC0_AD1		F4040h	F6040h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG17	GPMC0_AD2		F4044h	F6044h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG18	GPMC0_AD3		F4048h	F6048h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG19	GPMC0_AD4		F404Ch	F604Ch	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG20	GPMC0_AD5		F4050h	F6050h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG21	GPMC0_AD6		F4054h	F6054h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG22	GPMC0_AD7		F4058h	F6058h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG23	GPMC0_AD8		F405Ch	F605Ch	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG24	GPMC0_AD9		F4060h	F6060h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG25	GPMC0_AD10		F4064h	F6064h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG26	GPMC0_AD11		F4068h	F6068h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG27	GPMC0_AD12		F406Ch	F606Ch	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG28	GPMC0_AD13		F4070h	F6070h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG29	GPMC0_AD14		F4074h	F6074h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG30	GPMC0_AD15		F4078h	F6078h	LVCMOS	8254007h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG31	GPMC0_CLK		F407Ch	F607Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7

Table 14-11089. AM62D PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG33	GPMC0_ADVn_ALE		F4084h	F6084h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG34	GPMC0_OEn_REn		F4088h	F6088h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG35	GPMC0_WEn		F408Ch	F608Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG36	GPMC0_BE0n_CLE		F4090h	F6090h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG37	GPMC0_BE1n		F4094h	F6094h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG38	GPMC0_WAIT0		F4098h	F6098h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG39	GPMC0_WAIT1	EQEP2_I	F409Ch	F609Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG40	GPMC0_WPn		F40A0h	F60A0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG41	GPMC0_DIR	EQEP2_S	F40A4h	F60A4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG42	GPMC0_CSn0		F40A8h	F60A8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG43	GPMC0_CSn1		F40ACh	F60ACh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG44	GPMC0_CSn2	GPIO0_43	F40B0h	F60B0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG45	GPMC0_CSn3	GPIO0_44	F40B4h	F60B4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG46	GPIO0_45		F40B8h	F60B8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG47	GPIO0_46		F40BCh	F60BCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG48	GPIO0_47		F40C0h	F60C0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG49	GPIO0_48		F40C4h	F60C4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG50	GPIO0_49		F40C8h	F60C8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG51	GPIO0_50		F40CCh	F60CCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG52	GPIO0_51		F40D0h	F60D0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG53	GPIO0_52		F40D4h	F60D4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG54	GPIO0_53		F40D8h	F60D8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG55	GPIO0_54		F40DCh	F60DCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG56	GPIO0_55		F40E0h	F60E0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG57	GPIO0_56		F40E4h	F60E4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG58	GPIO0_57		F40E8h	F60E8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG59	GPIO0_58		F40ECh	F60ECh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG60	GPIO0_59		F40F0h	F60F0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG61	GPIO0_60		F40F4h	F60F4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG62	GPIO0_61		F40F8h	F60F8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG63	GPIO0_62		F40FCh	F60FCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG64	GPIO0_63		F4100h	F6100h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG65	GPIO0_64		F4104h	F6104h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG66	MMC2_DAT3	GPIO0_65	F4108h	F6108h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7

Table 14-11089. AM62D PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG67	MMC2_DAT2	GPIO0_66	F410Ch	F610Ch	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG68	MMC2_DAT1	GPIO0_67	F4110h	F6110h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG69	MMC2_DAT0	GPIO0_68	F4114h	F6114h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG70	MMC2_CLK	GPIO0_69	F4118h	F6118h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG72	MMC2_CMD	GPIO0_70	F4120h	F6120h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG73	MMC2_SDCD	GPIO0_71	F4124h	F6124h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG74	MMC2_SDWP	GPIO0_72	F4128h	F6128h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG75	RGMII1_TX_CTL		F412Ch	F612Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG76	RGMII1_TXC		F4130h	F6130h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG77	RGMII1_TD0		F4134h	F6134h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG78	RGMII1_TD1		F4138h	F6138h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG79	RGMII1_TD2		F413Ch	F613Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG80	RGMII1_TD3		F4140h	F6140h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG81	RGMII1_RX_CTL		F4144h	F6144h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG82	RGMII1_RXC		F4148h	F6148h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG83	RGMII1_RD0		F414Ch	F614Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG84	RGMII1_RD1		F4150h	F6150h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG85	RGMII1_RD2		F4154h	F6154h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG86	RGMII1_RD3		F4158h	F6158h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG87	MDIO0_MDIO		F415Ch	F615Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG88	MDIO0_MDC		F4160h	F6160h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG89	RGMII2_TX_CTL		F4164h	F6164h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG90	RGMII2_TXC		F4168h	F6168h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG91	RGMII2_TD0		F416Ch	F616Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG92	RGMII2_TD1		F4170h	F6170h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG93	RGMII2_TD2	EQEP2_I	F4174h	F6174h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG94	RGMII2_TD3	EQEP2_S	F4178h	F6178h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG95	RGMII2_RX_CTL		F417Ch	F617Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG96	RGMII2_RXC		F4180h	F6180h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG97	RGMII2_RD0		F4184h	F6184h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG98	RGMII2_RD1		F4188h	F6188h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG99	RGMII2_RD2	EQEP2_A	F418Ch	F618Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG100	RGMII2_RD3	EQEP2_B	F4190h	F6190h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG101	MCASP0_AXR3	EQEP0_A	F4194h	F6194h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7

Table 14-11089. AM62D PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG102	MCASP0_AXR2	EQEP0_B	F4198h	F6198h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG103	MCASP0_AXR1	EQEP0_S	F419Ch	F619Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG104	MCASP0_AXR0	EQEP0_I	F41A0h	F61A0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG105	MCASP0_ACLKX	EQEP1_A	F41A4h	F61A4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG106	MCASP0_AFSX	EQEP1_B	F41A8h	F61A8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG107	MCASP0_AFSR	EQEP1_S	F41ACh	F61ACh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG108	MCASP0_ACLKR	EQEP1_I	F41B0h	F61B0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG109	SPI0_CS0		F41B4h	F61B4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG110	SPI0_CS1	GPIO1_16	F41B8h	F61B8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG111	SPI0_CLK		F41BCh	F61BCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG112	SPI0_D0		F41C0h	F61C0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG113	SPI0_D1		F41C4h	F61C4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG114	UART0_RXD		F41C8h	F61C8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG115	UART0_TXD		F41CCh	F61CCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG116	UART0_CTSn		F41D0h	F61D0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG117	UART0_RTSn		F41D4h	F61D4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG118	MCAN0_TX	EQEP2_I	F41D8h	F61D8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG119	MCAN0_RX	EQEP2_S	F41DCh	F61DCh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG120	I2C0_SCL	EQEP2_A	F41E0h	F61E0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG121	I2C0_SDA	EQEP2_B	F41E4h	F61E4h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG122	I2C1_SCL		F41E8h	F61E8h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG123	I2C1_SDA		F41ECh	F61ECh	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG124	EXT_REFCLK1		F41F0h	F61F0h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG125	EXTINTn	GPIO1_31	F41F4h	F61F4h	I2C OPEN DRAIN	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG126	MMC0_DAT7	GPIO1_32	F41F8h	F61F8h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG127	MMC0_DAT6	GPIO1_33	F41FCh	F61FCh	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG128	MMC0_DAT5	GPIO1_34	F4200h	F6200h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG129	MMC0_DAT4	GPIO1_35	F4204h	F6204h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG130	MMC0_DAT3	GPIO1_36	F4208h	F6208h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG131	MMC0_DAT2	GPIO1_37	F420Ch	F620Ch	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG132	MMC0_DAT1	GPIO1_38	F4210h	F6210h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG133	MMC0_DAT0	GPIO1_39	F4214h	F6214h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG134	MMC0_CLK	GPIO1_40	F4218h	F6218h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7

Table 14-11089. AM62D PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21](1)	DRV_STR[20:19](2)	RXACTIVE[18](3)	PULLTYPESEL[17](4)	PULLUDEN[16](4)	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG136	MMC0_CMD	GPIO1_41	F4220h	F6220h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG137	MMC1_DAT3	GPIO1_42	F4224h	F6224h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG138	MMC1_DAT2	GPIO1_43	F4228h	F6228h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG139	MMC1_DAT1	GPIO1_44	F422Ch	F622Ch	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG140	MMC1_DAT0	GPIO1_45	F4230h	F6230h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG141	MMC1_CLK(5)	GPIO1_46	F4234h	F6234h	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG143	MMC1_CMD	GPIO1_47	F423Ch	F623Ch	SDIO	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG144	MMC1_SDCD	GPIO1_48	F4240h	F6240h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG145	MMC1_SDWP	GPIO1_49	F4244h	F6244h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG146	RESET_REQz		F4248h	F6248h	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG147	RESETSTATz		F424Ch	F624Ch	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG148	PORz_OUT		F4250h	F6250h	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG149	USB0_DRVVBUS		F4254h	F6254h	LVCMOS	8204007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG150	USB1_DRVVBUS		F4258h	F6258h	LVCMOS	8204007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG0	MCU_SPI0_CS0	MCU_GPIO0_0	4084000h	4086000h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG1	MCU_SPI0_CS1	MCU_GPIO0_1	4084004h	4086004h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG2	MCU_SPI0_CLK		4084008h	4086008h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG3	MCU_SPI0_D0		408400Ch	408600Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG4	MCU_SPI0_D1		4084010h	4086010h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG5	MCU_UART0_RXD		4084014h	4086014h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG6	MCU_UART0_TXD		4084018h	4086018h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG7	MCU_UART0_CTSn	MCU_GPIO0_7	408401Ch	408601Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG8	MCU_UART0_RTSn	MCU_GPIO0_8	4084020h	4086020h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG9	WKUP_UART0_RXD		4084024h	4086024h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG10	WKUP_UART0_TXD		4084028h	4086028h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG11	WKUP_UART0_CTSn	MCU_GPIO0_11	408402Ch	408602Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG12	WKUP_UART0_RTSn	MCU_GPIO0_12	4084030h	4086030h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG13	MCU_MCAN0_TX		4084034h	4086034h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG14	MCU_MCAN0_RX		4084038h	4086038h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG15	MCU_MCAN1_TX	MCU_GPIO0_15	408403Ch	408603Ch	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG16	MCU_MCAN1_RX	MCU_GPIO0_16	4084040h	4086040h	LVCMOS	8214007h	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG17	MCU_I2C0_SCL		4084044h	4086044h	I2C OPEN DRAIN	8054007h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG18	MCU_I2C0_SDA		4084048h	4086048h	I2C OPEN DRAIN	8054007h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	7

Table 14-11089. AM62D PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values																						
							LOCK[31]	WKUP_EVT[30]	WKUP_EN[29]	DS_PULLTYPE_SEL[28]	DS_PULLUD_EN[27]	DSOUT_VAL[26]	DSOUT_DIS[25]	DS_EN[24]	ISO_BYP[23]	RESERVED[22]	TX_DIS[21](1)	DRV_STR[20:19](2)	RXACTIVE[18](3)	PULLTYPESEL[17](4)	PULLUDEN[16](4)	FORCE_DS_EN[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:9]	WK_LVL_POL[8]	WK_LVL_EN[7]	RSVD[6:4]	MUXMODE[3:0]
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG19	WKUP_I2C0_SCL		408404Ch	408604Ch	I2C OPEN DRAIN	8054007h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG20	WKUP_I2C0_SDA		4084050h	4086050h	I2C OPEN DRAIN	8054007h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG21	MCU_RESETz		4084054h	4086054h	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG22	MCU_PORz		4084058h	4086058h	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG23	MCU_RESETSTATz		408405Ch	408605Ch	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG24	MCU_ERRORn		4084060h	4086060h	LVCMOS	8044000h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG25	TCK		4084064h	4086064h	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG26	TRSTn		4084068h	4086068h	LVCMOS	8244000h	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG27	TDI		408406Ch	408606Ch	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG28	TDO		4084070h	4086070h	LVCMOS	8024000h	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG29	TMS		4084074h	4086074h	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG30	EMU0		4084078h	4086078h	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG31	EMU1		408407Ch	408607Ch	LVCMOS	8264000h	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG32	PMIC_LPM_EN0		4084080h	4086080h	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG33	WKUP_CLKOUT0		4084084h	4086084h	LVCMOS	8014000h	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

(1) TX_DIS bit must be set before changing the MUXMODE value when the IO associated with a PADCONFIG register was previously configured to operate as an output. This is required to prevent a potential glitch propagating through the output buffer when the MUXMODE values is changed. A MUXMODE value change should be implemented with three PADCONFIG write operations, where the TX_DIS bit is set in the first write operation, the MUXMODE values is changed in the second write operation, and the TX_DIS bit is reset in the third write operation. This will disable the output buffer while the pin mux logic changes signal functions.

(2) Use of settings other than the reset value could invalidate datasheet timings.

(3) The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is very important since a floating input may damage the device.

(4) These bits do not apply to "I2C OD FS" buffer types as these IOs do not have internal pull registers.

(5) For MMC1_CLK signal to work properly, the RXACTIVE bit should be set to 0x1 because of retiming purposes.

14.2.1.2.3 MAIN_PADCFG_CTRL

MAIN_PADCFG_CTRL

14.2.1.2.3.1 MAIN_PADCFG_CTRL Summaries

MAIN_PADCFG_CTRL Summaries

Table 14-11090. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
0h	32	MAIN_PADCFG_CTRL_MMR_CFG0_PID	000F 0000h
4h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0	000F 0004h
8h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1	000F 0008h
1008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	000F 1008h
100Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	000F 100Ch
1010h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS	000F 1010h
1014h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	000F 1014h
1018h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE	000F 1018h
101Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	000F 101Ch
1020h	32	MAIN_PADCFG_CTRL_MMR_CFG0_EOI	000F 1020h
1024h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS	000F 1024h
1028h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	000F 1028h
102Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	000F 102Ch
1030h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR	000F 1030h
1100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	000F 1100h
2000h	32	MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY	000F 2000h
2004h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY	000F 2004h
2008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY	000F 2008h
3008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	000F 3008h
300Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	000F 300Ch
3010h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	000F 3010h
3014h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	000F 3014h
3018h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	000F 3018h
301Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	000F 301Ch
3020h	32	MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY	000F 3020h
3024h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	000F 3024h
3028h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	000F 3028h

Table 14-11090. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
302Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	000F 302Ch
3030h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	000F 3030h
3100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0	000F 3100h
5008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	000F 5008h
500Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	000F 500Ch
5100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	000F 5100h
5104h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	000F 5104h
5108h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	000F 5108h
510Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	000F 510Ch
5110h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	000F 5110h
7008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	000F 7008h
700Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	000F 700Ch
7100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0	000F 7100h
7104h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1	000F 7104h
7108h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2	000F 7108h
710Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3	000F 710Ch
7110h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4	000F 7110h

14.2.1.2.3.2 MAIN_PADCFG_CTRL Registers

MAIN_PADCFG_CTRL Registers

14.2.1.2.3.2.1 MAIN_PADCFG_CTRL_MMR_CFG0_PID Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800214h]

PID register

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Table 14-11091. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0000h**

Figure 14-3687. MAIN_PADCFG_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM		PID_MINOR					
R		R					
0h		14h					

Table 14-11093. MAIN_PADCFG_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	14h	Reset Source: mod_g_rst_n

14.2.1.2.3.2.2 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000001h]

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Table 14-11094. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0004h**

Figure 14-3688. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV							
R							
1h							

Table 14-11096. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.3.2.3 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-11097. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0008h**

Figure 14-3689. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-11099. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.3.2.4 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-11100. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1008h**

Figure 14-3690. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-11102. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.5 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-11103. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 100Ch**

Figure 14-3691. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-11105. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.6 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-11106. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1010h**

Figure 14-3692. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11108. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.7 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-11109. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1014h**

Figure 14-3693. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11111. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.8 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-11112. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1018h**

Figure 14-3694. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11114. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.9 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-11115. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 101Ch

Figure 14-3695. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11117. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.10 MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-11118. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1020h**

Figure 14-3696. MAIN_PADCFG_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-11120. MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.3.2.11 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-11121. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1024h**

Figure 14-3697. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-11123. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.3.2.12 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-11124. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1028h**

Figure 14-3698. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-11126. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.3.2.13 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-11127. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 102Ch**

Figure 14-3699. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ROUTEID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_PRIVID							
R							
0h							

Table 14-11129. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.3.2.14 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-11130. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1030h**

Figure 14-3700. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-11132. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.15 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-11133. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1100h**

Figure 14-3701. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-11135. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.3.2.16 MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800214h]

PID register

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Table 14-11136. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 2000h**

Figure 14-3702. MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		14h					

Table 14-11138. MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	14h	Reset Source: mod_g_rst_n

14.2.1.2.3.2.17 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000001h]

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Table 14-11139. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 2004h

Figure 14-3703. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							

Table 14-11141. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.3.2.18 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-11142. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 2008h**

Figure 14-3704. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-11144. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.3.2.19 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-11145. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3008h**

Figure 14-3705. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-11147. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.20 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-11148. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 300Ch**

Figure 14-3706. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK0_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK0_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK0_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK0_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11150. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.21 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-11151. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3010h**

Figure 14-3707. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11153. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.22 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-11154. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3014h**

Figure 14-3708. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11156. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.23 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-11157. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3018h**

Figure 14-3709. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11159. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.24 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-11160. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 301Ch**

Figure 14-3710. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11162. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.25 MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-11163. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3020h

Figure 14-3711. MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-11165. MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.3.2.26 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-11166. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3024h**

Figure 14-3712. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-11168. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.3.2.27 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-11169. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3028h**

Figure 14-3713. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-11171. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.3.2.28 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-11172. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 302Ch

Figure 14-3714. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ROUTEID_PROXY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-11174. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.3.2.29 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-11175. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3030h**

Figure 14-3715. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-11177. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.30 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-11178. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3100h**

Figure 14-3716. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-11180. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.3.2.31 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-11181. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5008h**

Figure 14-3717. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-11183. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.32 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-11184. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 500Ch**

Figure 14-3718. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-11186. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.33 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11187. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5100h**

Figure 14-3719. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-11189. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.34 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11190. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5104h

Figure 14-3720. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-11192. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.35 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11193. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5108h**

Figure 14-3721. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-11195. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.36 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-11196. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 510Ch

Figure 14-3722. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-11198. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.37 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11199. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5110h**

Figure 14-3723. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-11201. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.38 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-11202. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7008h**

Figure 14-3724. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-11204. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.39 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-11205. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 700Ch**

Figure 14-3725. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-11207. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.40 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11208. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7100h**

Figure 14-3726. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-11210. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.41 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11211. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7104h**

Figure 14-3727. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-11213. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.42 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11214. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7108h**

Figure 14-3728. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-11216. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.43 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-11217. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 710Ch**

Figure 14-3729. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-11219. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.44 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11220. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7110h**

Figure 14-3730. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-11222. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4 MCU_PADCFG_CTRL

MCU_PADCFG_CTRL

14.2.1.2.4.1 MCU_PADCFG_CTRL Summaries

MCU_PADCFG_CTRL Summaries

Table 14-11223. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
0h	32	MCU_PADCFG_CTRL_MMR_CFG0_PID	0408 0000h
4h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0	0408 0004h
8h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1	0408 0008h
1008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	0408 1008h
100Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	0408 100Ch
1010h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS	0408 1010h
1014h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0408 1014h
1018h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE	0408 1018h
101Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0408 101Ch
1020h	32	MCU_PADCFG_CTRL_MMR_CFG0_EOI	0408 1020h
1024h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS	0408 1024h
1028h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0408 1028h
102Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0408 102Ch
1030h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR	0408 1030h
1100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0408 1100h
2000h	32	MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY	0408 2000h
2004h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY	0408 2004h
2008h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0408 2008h
3008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0408 3008h
300Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0408 300Ch
3010h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0408 3010h
3014h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0408 3014h
3018h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0408 3018h
301Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0408 301Ch
3020h	32	MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY	0408 3020h
3024h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0408 3024h
3028h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0408 3028h
302Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0408 302Ch

Table 14-11223. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768 (continued)

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
3030h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0408 3030h
3100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0408 3100h
5008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	0408 5008h
500Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	0408 500Ch
5100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0408 5100h
5104h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	0408 5104h
7008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0408 7008h
700Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0408 700Ch
7100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0408 7100h
7104h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0408 7104h

14.2.1.2.4.2 MCU_PADCFG_CTRL Registers

MCU_PADCFG_CTRL Registers

14.2.1.2.4.2.1 MCU_PADCFG_CTRL_MMR_CFG0_PID Register

1 MCU_PADCFG_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800214h]

PID register

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Table 14-11224. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0000h**

Figure 14-3731. MCU_PADCFG_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		14h					

Table 14-11226. MCU_PADCFG_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	14h	Reset Source: mod_g_rst_n

14.2.1.2.4.2.2 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000001h]

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Table 14-11227. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0004h**

Figure 14-3732. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV							
R							
1h							

Table 14-11229. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.4.2.3 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-11230. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0008h**

Figure 14-3733. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-11232. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.4.2.4 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-11233. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1008h**

Figure 14-3734. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-11235. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.5 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-11236. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 100Ch**

Figure 14-3735. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-11238. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.6 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-11239. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1010h**

Figure 14-3736. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11241. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.7 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-11242. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1014h**

Figure 14-3737. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>ENABLED_PROXY_ERR</td><td>ENABLED_KICK_ERR</td><td>ENABLED_ADDR_ERR</td><td>ENABLED_PROT_ERR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11244. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.8 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-11245. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1018h

Figure 14-3738. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11247. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.9 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-11248. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 101Ch**

Figure 14-3739. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11250. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.10 MCU_PADCFG_CTRL_MMR_CFG0_EOI Register

1 MCU_PADCFG_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-11251. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1020h**

Figure 14-3740. MCU_PADCFG_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-11253. MCU_PADCFG_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.4.2.11 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-11254. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1024h**

Figure 14-3741. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_ADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_ADDR							
R							
0h							

Table 14-11256. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.4.2.12 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-11257. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1028h**

Figure 14-3742. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-11259. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.4.2.13 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-11260. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 102Ch**

Figure 14-3743. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-11262. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.4.2.14 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-11263. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1030h**

Figure 14-3744. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FAULT_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11265. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.15 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-11266. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1100h**

Figure 14-3745. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-11268. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.4.2.16 MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800214h]

PID register

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Table 14-11269. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2000h**

Figure 14-3746. MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC_PROXY</td><td colspan="3">PID_MAJOR_PROXY</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM_PROXY</td><td colspan="6">PID_MINOR_PROXY</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">14h</td></tr>
</table>

Table 14-11271. MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	14h	Reset Source: mod_g_rst_n

14.2.1.2.4.2.17 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000001h]

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Table 14-11272. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2004h**

Figure 14-3747. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							

Table 14-11274. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.4.2.18 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-11275. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2008h**

Figure 14-3748. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-11277. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.4.2.19 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-11278. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3008h**

Figure 14-3749. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-11280. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.20 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-11281. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 300Ch**

Figure 14-3750. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-11283. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.21 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-11284. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3010h**

Figure 14-3751. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11286. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.22 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-11287. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3014h**

Figure 14-3752. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11289. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.23 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-11290. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3018h

Figure 14-3753. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11292. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.24 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-11293. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 301Ch**

Figure 14-3754. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>PROXY_ERR_EN_CLR_PROXY</td><td>KICK_ERR_EN_CLR_PROXY</td><td>ADDR_ERR_EN_CLR_PROXY</td><td>PROT_ERR_EN_CLR_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11295. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.25 MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-11296. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3020h**

Figure 14-3755. MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11298. MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.4.2.26 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-11299. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3024h**

Figure 14-3756. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-11301. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.4.2.27 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-11302. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3028h**

Figure 14-3757. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-11304. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.4.2.28 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-11305. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 302Ch**

Figure 14-3758. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-11307. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.4.2.29 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-11308. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3030h**

Figure 14-3759. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-11310. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.30 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-11311. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3100h**

Figure 14-3760. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-11313. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.4.2.31 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-11314. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5008h**

Figure 14-3761. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-11316. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.32 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-11317. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 500Ch**

Figure 14-3762. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-11319. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.33 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11320. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5100h**

Figure 14-3763. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-11322. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.34 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11323. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5104h**

Figure 14-3764. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-11325. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.35 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-11326. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7008h**

Figure 14-3765. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-11328. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.36 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-11329. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 700Ch**

Figure 14-3766. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-11331. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.37 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11332. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7100h**

Figure 14-3767. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-11334. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.38 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-11335. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7104h**

Figure 14-3768. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11337. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.3 Kick Protection Registers

14.2.1.3.1 Kick Protection Registers

- CTRL_MMR0 Partition Unlock Values
- MCU_CTRL_MMR0 Partition Unlock Values
- WKUP_CTRL_MMR0 Partition Unlock Values
- PADCFG_CTRL0 Partition Unlock Values
- MCU_PADCFG_CTRL0 Partition Unlock Values

Table 14-11338. CTRL_MMR0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x000101008	0x000103008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x00010100C	0x00010300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x000105008	0x000107008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x00010500C	0x00010700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	0x68EF3490	0x000109008	0x00010B008	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	0xD172BC5A	0x00010900C	0x00010B00C	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MAIN_CTRL_MMR_CFG0_LOCK4_KICK0	Partition 4	0x68EF3490	0x000111008	0x000113008	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MAIN_CTRL_MMR_CFG0_LOCK4_KICK1	Partition 4	0xD172BC5A	0x00011100C	0x00011300C	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MAIN_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	0x68EF3490	0x000119008	0x00011B008	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
MAIN_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	0xD172BC5A	0x00011900C	0x00011B00C	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status

Table 14-11339. MCU_CTRL_MMR0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x004501008	0x004503008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MCU_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x00450100C	0x00450300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MCU_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x004505008	0x004507008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MCU_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x00450500C	0x00450700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MCU_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	0x68EF3490	0x004509008	0x00450B008	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MCU_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	0xD172BC5A	0x00450900C	0x00450B00C	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MCU_CTRL_MMR_CFG0_LOCK3_KICK0	Partition 3	0x68EF3490	0x00450D008	0x00450F008	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs

Table 14-11339. MCU_CTRL_MMR0 Partition Unlock Values (continued)

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_CTRL_MMR_CFG0_LOCK3_KICK1	Partition 3	0xD172BC5A	0x00450D00C	0x00450F00C	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
MCU_CTRL_MMR_CFG0_LOCK4_KICK0	Partition 4	0x68EF3490	0x004511008	0x004513008	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MCU_CTRL_MMR_CFG0_LOCK4_KICK1	Partition 4	0xD172BC5A	0x00451100C	0x00451300C	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MCU_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	0x68EF3490	0x004519008	0x00451B008	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
MCU_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	0xD172BC5A	0x00451900C	0x00451B00C	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status

Table 14-11340. WKUP_CTRL_MMR0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
WKUP_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x043001008	0x043003008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
WKUP_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x04300100C	0x04300300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
WKUP_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x043005008	0x043007008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
WKUP_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x04300500C	0x04300700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
WKUP_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	0x68EF3490	0x043009008	0x04300B008	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
WKUP_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	0xD172BC5A	0x04300900C	0x04300B00C	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
WKUP_CTRL_MMR_CFG0_LOCK3_KICK0	Partition 3	0x68EF3490	0x04300D008	0x04300F008	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
WKUP_CTRL_MMR_CFG0_LOCK3_KICK1	Partition 3	0xD172BC5A	0x04300D00C	0x04300F00C	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
WKUP_CTRL_MMR_CFG0_LOCK4_KICK0	Partition 4	0x68EF3490	0x043011008	0x043013008	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
WKUP_CTRL_MMR_CFG0_LOCK4_KICK1	Partition 4	0xD172BC5A	0x04301100C	0x04301300C	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
WKUP_CTRL_MMR_CFG0_LOCK5_KICK0	Partition 5	0x68EF3490	0x043015008	0x043017008	0x14000 to 0x15FFF	0x16000 to 0x17FFF	DDR Frequency Control
WKUP_CTRL_MMR_CFG0_LOCK5_KICK1	Partition 5	0xD172BC5A	0x04301500C	0x04301700C	0x14000 to 0x15FFF	0x16000 to 0x17FFF	DDR Frequency Control
WKUP_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	0x68EF3490	0x043019008	0x04301B008	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
WKUP_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	0xD172BC5A	0x04301900C	0x04301B00C	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
WKUP_CTRL_MMR_CFG0_LOCK7_KICK0	Partition 7	0x68EF3490	0x04301D008	0x04301F008	0x1C000 to 0x1DFFF	0x1E000 to 0x1FFFF	Backup Data for Deep Sleep
WKUP_CTRL_MMR_CFG0_LOCK7_KICK1	Partition 7	0xD172BC5A	0x04301D00C	0x04301F00C	0x1C000 to 0x1DFFF	0x1E000 to 0x1FFFF	Backup Data for Deep Sleep

Table 14-11341. PADCFG_CTRL0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x0000F1008	0x0000F3008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x0000F100C	0x0000F300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x0000F5008	0x0000F7008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x0000F500C	0x0000F700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers

Table 14-11342. MCU_PADCFG_CTRL0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x004081008	0x004083008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x00408100C	0x00408300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x004085008	0x004087008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers
MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x00408500C	0x00408700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers

14.2.1.4 Security Control Registers

14.2.1.4.1 main_sec_mmr

main_sec_mmr

14.2.1.4.1.1 main_sec_mmr Summaries

main_sec_mmr Summaries

Table 14-11343. MAIN_SEC_MMR_CFG2 Registers, Base Address=4590 0000h, Length=131072

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
9000h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG	4590 9000h
9040h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG	4590 9040h
9080h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE2_DBG_CFG	4590 9080h
90C0h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE3_DBG_CFG	4590 90C0h
D000h	32	MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG	4590 D000h

Table 14-11344. MAIN_SEC_MMR_CFG0 Registers, Base Address=45A0 0000h, Length=131072

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
0h	32	MAIN_SEC_MMR_CFG0_PID	45A0 0000h
9020h	32	MAIN_SEC_MMR_CFG0_CLSTR9_DEF	45A0 9020h
9040h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CFG	45A0 9040h
9080h	32	MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL	45A0 9080h
9090h	32	MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT	45A0 9090h
9110h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO	45A0 9110h
9114h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI	45A0 9114h
9190h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO	45A0 9190h
9194h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI	45A0 9194h
9210h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_LO	45A0 9210h
9214h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_HI	45A0 9214h
9290h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_LO	45A0 9290h
9294h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_HI	45A0 9294h
D020h	32	MAIN_SEC_MMR_CFG0_CLSTR13_DEF	45A0 D020h
D040h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CFG	45A0 D040h
D090h	32	MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT	45A0 D090h
D110h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO	45A0 D110h
D114h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI	45A0 D114h
18008h	32	MAIN_SEC_MMR_CFG0_GIC_CONFIG	45A1 8008h

14.2.1.4.1.2 main_sec_mmr Registers

main_sec_mmr Registers

14.2.1.4.1.2.1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register (Offset = 9000h) [reset = AAh]

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Table 14-11345. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 9000h**

Figure 14-3769. MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR9_CORE0_DBG_CFG_SPNIDEN				CLSTR9_CORE0_DBG_CFG_SPIDEN			
R				R			
X				X			
7	6	5	4	3	2	1	0
CLSTR9_CORE0_DBG_CFG_NIDEN				CLSTR9_CORE0_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-11347. MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE0_DBG_CFG_SPNIDEN	R	X	Core0 Secure Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE0_DBG_CFG_SPIDEN	R	X	Core0 Secure Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n

14.2.1.4.1.2.2 MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register (Offset = 9040h) [reset = AAh]

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Table 14-11348. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 9040h**

Figure 14-3770. MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR9_CORE1_DBG_CFG_SPNIDEN				CLSTR9_CORE1_DBG_CFG_SPIDEN			
R				R			
X				X			
7	6	5	4	3	2	1	0
CLSTR9_CORE1_DBG_CFG_NIDEN				CLSTR9_CORE1_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-11350. MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE1_DBG_CFG_SPNIDEN	R	X	Core1 Secure Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE1_DBG_CFG_SPIDEN	R	X	Core1 Secure Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n

14.2.1.4.1.2.3 MAIN_SEC_MMR_CFG2_CLSTR9_CORE2_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE2_DBG_CFG Register (Offset = 9080h) [reset = AAh]

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Table 14-11351. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 9080h**

Figure 14-3771. MAIN_SEC_MMR_CFG2_CLSTR9_CORE2_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR9_CORE2_DBG_CFG_SPNIDEN				CLSTR9_CORE2_DBG_CFG_SPIDEN			
R				R			
X				X			
7	6	5	4	3	2	1	0
CLSTR9_CORE2_DBG_CFG_NIDEN				CLSTR9_CORE2_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-11353. MAIN_SEC_MMR_CFG2_CLSTR9_CORE2_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE2_DBG_CFG_SPNIDEN	R	X	Core2 Secure Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE2_DBG_CFG_SPIDEN	R	X	Core2 Secure Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE2_DBG_CFG_NIDEN	R/W	Ah	Core2 Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE2_DBG_CFG_DBGEN	R/W	Ah	Core2 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n

14.2.1.4.1.2.4 MAIN_SEC_MMR_CFG2_CLSTR9_CORE3_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE3_DBG_CFG Register (Offset = 90C0h) [reset = AAh]

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Table 14-11354. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 90C0h**

Figure 14-3772. MAIN_SEC_MMR_CFG2_CLSTR9_CORE3_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR9_CORE3_DBG_CFG_SPNIDEN				CLSTR9_CORE3_DBG_CFG_SPIDEN			
R				R			
X				X			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR9_CORE3_DBG_CFG_NIDEN				CLSTR9_CORE3_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-11356. MAIN_SEC_MMR_CFG2_CLSTR9_CORE3_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE3_DBG_CFG_SPNIDEN	R	X	Core3 Secure Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE3_DBG_CFG_SPIDEN	R	X	Core3 Secure Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE3_DBG_CFG_NIDEN	R/W	Ah	Core3 Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE3_DBG_CFG_DBGEN	R/W	Ah	Core3 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n

14.2.1.4.1.2.5 MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register (Offset = D000h) [reset = AAh]

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Table 14-11357. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 D000h**

Figure 14-3773. MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR13_CORE0_DBG_CFG_SPNIDEN				CLSTR13_CORE0_DBG_CFG_SPIDEN			
R				R			
X				X			
7	6	5	4	3	2	1	0
CLSTR13_CORE0_DBG_CFG_NIDEN				CLSTR13_CORE0_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-11359. MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR13_CORE0_DBG_CFG_SPNIDEN	R	X	Core0 Secure Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR13_CORE0_DBG_CFG_SPIDEN	R	X	Core0 Secure Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:4	CLSTR13_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
3:0	CLSTR13_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n

14.2.1.4.1.2.6 MAIN_SEC_MMR_CFG0_PID Register

1 MAIN_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-11360. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0000h**

Figure 14-3774. MAIN_SEC_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							

23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							

15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		

7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-11362. MAIN_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.4.1.2.7 MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register (Offset = 9020h) [reset = 2FF00h]

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Table 14-11363. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9020h**

Figure 14-3775. MAIN_SEC_MMR_CFG0_CLSTR9_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					CLSTR9_DEF_CORE_NUM		
NONE					R		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR9_DEF_DSP_CORE_TYPE							
R							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR9_DEF_ARM_CORE_TYPE							
R							
0h							

Table 14-11365. MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR9_DEF_CORE_NUM	R	2h	Number of cores in cluster 000 - Single Core 001 - Dual Core 010 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR9_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR9_DEF_ARM_CORE_TYPE	R	0h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.4.1.2.8 MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register (Offset = 9040h) [reset = Fh]

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Table 14-11366. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9040h**

Figure 14-3776. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				CLSTR9_CONFIG0_CP15_DISABLE3	CLSTR9_CONFIG0_CP15_DISABLE2	CLSTR9_CONFIG0_CP15_DISABLE1	CLSTR9_CONFIG0_CP15_DISABLE0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR9_CONFIG0_CONFIG_TE3	CLSTR9_CONFIG0_CONFIG_TE2	CLSTR9_CONFIG0_CONFIG_TE1	CLSTR9_CONFIG0_CONFIG_TE0	CLSTR9_CONFIG0_AARCH3	CLSTR9_CONFIG0_AARCH2	CLSTR9_CONFIG0_AARCH1	CLSTR9_CONFIG0_AARCH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	1h	1h	1h

Table 14-11368. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	CLSTR9_CONFIG0_CP15_DISABLE3	R/W	0h	Deactivate write access to secure CP15 registers for Core3 0 - Access activated 1 - Access deactivated CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
10	CLSTR9_CONFIG0_CP15_DISABLE2	R/W	0h	Deactivate write access to secure CP15 registers for Core2 0 - Access activated 1 - Access deactivated CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
9	CLSTR9_CONFIG0_CP15_DISABLE1	R/W	0h	Deactivate write access to secure CP15 registers for Core1 0 - Access activated 1 - Access deactivated CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

Table 14-11368. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CLSTR9_CONFIG0_CP15_DISABLE0	R/W	0h	Deactivate write access to secure CP15 registers for Core0 0 - Access activated 1 - Access deactivated CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
7	CLSTR9_CONFIG0_CONFIG_TE3	R/W	0h	Activate T32 exceptions for Core3 Sets the initial value of the TE bit in the CP15 SCTLR register. This bitfield is sampled only during reset of the processor. 0 - TE bit is LOW 1 - TE bit is HIGH CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
6	CLSTR9_CONFIG0_CONFIG_TE2	R/W	0h	Activate T32 exceptions for Core2 Sets the initial value of the TE bit in the CP15 SCTLR register. This bitfield is sampled only during reset of the processor. 0 - TE bit is LOW 1 - TE bit is HIGH CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
5	CLSTR9_CONFIG0_CONFIG_TE1	R/W	0h	Activate T32 exceptions for Core1 Sets the initial value of the TE bit in the CP15 SCTLR register. This bitfield is sampled only during reset of the processor. 0 - TE bit is LOW 1 - TE bit is HIGH CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
4	CLSTR9_CONFIG0_CONFIG_TE0	R/W	0h	Activate T32 exceptions for Core0 Sets the initial value of the TE bit in the CP15 SCTLR register. This bitfield is sampled only during reset of the processor. 0 - TE bit is LOW 1 - TE bit is HIGH CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
3	CLSTR9_CONFIG0_AARCH3	R/W	1h	Core3 ARM Architecture configuration 0 - AArch32 1 - AArch64 CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
2	CLSTR9_CONFIG0_AARCH2	R/W	1h	Core2 ARM Architecture configuration 0 - AArch32 1 - AArch64 CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n
1	CLSTR9_CONFIG0_AARCH1	R/W	1h	Core1 ARM Architecture configuration 0 - AArch32 1 - AArch64 CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

Table 14-11368. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLSTR9_CONFIG0_AARCH0	R/W	1h	Core0 ARM Architecture configuration 0 - AArch32 1 - AArch64 CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.9 MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register (Offset = 9080h) [reset = F18h]

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Table 14-11369. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9080h**

Figure 14-3777. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			CLSTR9_PM_CONFIG_L2RSTDISABLE	CLSTR9_PM_CONFIG_DBGPWRUP3	CLSTR9_PM_CONFIG_DBGPWRUP2	CLSTR9_PM_CONFIG_DBGPWRUP1	CLSTR9_PM_CONFIG_DBGPWRUP0
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
CLSTR9_PM_CONFIG_DBGL1RSTDISABLE	CLSTR9_PM_CONFIG_CLEAR_MON	CLSTR9_PM_CONFIG_L2_FLUSHREQ	RSVD	RSVD	RSVD	CLSTR9_PM_CONFIG_ACP_MASTER	RSVD
R/W	R/W	R/W				R/W	
0h	0h	0h	1h	1h	0h	0h	0h

Table 14-11371. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	CLSTR9_PM_CONFIG_L2RSTDISABLE	R/W	0h	Deactivate L2 cache automatic invalidate on reset functionality. This pin is sampled only during reset of the processor. 0 - Activate automatic invalidation of L2 cache on reset. 1 - Deactivate automatic invalidation of L2 cache on reset. Reset Source: mod_g_rst_n
11	CLSTR9_PM_CONFIG_DBGPWRUP3	R/W	1h	Core3 powered up 0 - Core is powered down 1 - Core is powered up Reset Source: mod_g_rst_n
10	CLSTR9_PM_CONFIG_DBGPWRUP2	R/W	1h	Core2 powered up 0 - Core is powered down 1 - Core is powered up Reset Source: mod_g_rst_n
9	CLSTR9_PM_CONFIG_DBGPWRUP1	R/W	1h	Core1 powered up 0 - Core is powered down 1 - Core is powered up Reset Source: mod_g_rst_n

Table 14-11371. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CLSTR9_PM_CONFIG_DBGPWRUP0	R/W	1h	Core0 powered up 0 - Core is powered down 1 - Core is powered up Reset Source: mod_g_rst_n
7	CLSTR9_PM_CONFIG_DBGL1RSTDISABLE	R/W	0h	Deactivate L1 data cache automatic invalidate on reset functionality. This pin is sampled only during reset of the processor. 0 - Activate automatic invalidation of L1 data cache on reset. 1 - Deactivate automatic invalidation of L1 data cache on reset. Reset Source: mod_g_rst_n
6	CLSTR9_PM_CONFIG_CLEAR_MON	R/W	0h	Request to clear the external global exclusive monitor. This sends a WFE wake-up event to all cores in the cluster. When set HIGH the global exclusive monitor in the system is requesting the processor EVENT registers to be set HIGH. Reset Source: mod_g_rst_n
5	CLSTR9_PM_CONFIG_L2_FLUSHREQ	R/W	0h	ARM L2 hardware flush request Reset Source: mod_g_rst_n
1	CLSTR9_PM_CONFIG_ACP_MASTER	R/W	0h	ACP controller is inactive and is not participating in coherency. There must be no outstanding transactions when the controller asserts this signal, and while it is asserted the controller must not send any new transactions: 0 - ACP controller is active 1 - ACP controller is inactive Reset Source: mod_g_rst_n

14.2.1.4.1.2.10 MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register (Offset = 9090h) [reset = 0h]

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Table 14-11372. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9090h**

Figure 14-3778. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	RSVD	CLSTR9_PM_STATUS_STANDBY_WFI_L2	CLSTR9_PM_STATUS_L2_HW_FLUSH	CLSTR9_PM_STATUS_CORE3_SMPEN	CLSTR9_PM_STATUS_CORE2_SMPEN	CLSTR9_PM_STATUS_CORE1_SMPEN	CLSTR9_PM_STATUS_CORE0_SMPEN
NONE		R	R	R	R	R	R
0h	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
CLSTR9_PM_STATUS_CORE3_WFE	CLSTR9_PM_STATUS_CORE2_WFE	CLSTR9_PM_STATUS_CORE1_WFE	CLSTR9_PM_STATUS_CORE0_WFE	CLSTR9_PM_STATUS_CORE3_WFI	CLSTR9_PM_STATUS_CORE2_WFI	CLSTR9_PM_STATUS_CORE1_WFI	CLSTR9_PM_STATUS_CORE0_WFI
R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X

Table 14-11374. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
13	CLSTR9_PM_STATUS_STANDBY_WFI_L2	R	X	Indicates L2 low power state 0 - L2 not in low power state 1 - L2 is in WFI low power state Reset Source: mod_g_rst_n
12	CLSTR9_PM_STATUS_L2_HW_FLUSH	R	X	L2 hardware flush complete Reset Source: mod_g_rst_n
11	CLSTR9_PM_STATUS_CORE3_SMPEN	R	X	Core3 coherency indicator 0 - Core is taking part in coherency 1 - Core is not taking part in coherency Reset Source: mod_g_rst_n
10	CLSTR9_PM_STATUS_CORE2_SMPEN	R	X	Core2 coherency indicator 0 - Core is taking part in coherency 1 - Core is not taking part in coherency Reset Source: mod_g_rst_n

Table 14-11374. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CLSTR9_PM_STATUS_CORE1_SMPEN	R	X	Core1 coherency indicator 0 - Core is taking part in coherency 1 - Core is not taking part in coherency Reset Source: mod_g_rst_n
8	CLSTR9_PM_STATUS_CORE0_SMPEN	R	X	Core0 coherency indicator 0 - Core is taking part in coherency 1 - Core is not taking part in coherency Reset Source: mod_g_rst_n
7	CLSTR9_PM_STATUS_CORE3_WFE	R	X	Indicates Core3 in WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
6	CLSTR9_PM_STATUS_CORE2_WFE	R	X	Indicates Core2 in WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
5	CLSTR9_PM_STATUS_CORE1_WFE	R	X	Indicates Core1 in WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
4	CLSTR9_PM_STATUS_CORE0_WFE	R	X	Indicates Core0 in WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
3	CLSTR9_PM_STATUS_CORE3_WFI	R	X	Indicates Core3 in WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
2	CLSTR9_PM_STATUS_CORE2_WFI	R	X	Indicates Core2 in WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
1	CLSTR9_PM_STATUS_CORE1_WFI	R	X	Indicates Core1 in WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
0	CLSTR9_PM_STATUS_CORE0_WFI	R	X	Indicates Core0 in WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.11 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register (Offset = 9110h) [reset = 0h]

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Table 14-11375. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9110h**

Figure 14-3779. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-11377. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[33:2] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.12 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register (Offset = 9114h) [reset = 0h]

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Table 14-11378. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9114h**

Figure 14-3780. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						CLSTR9_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-11380. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[35:34] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.13 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register (Offset = 9190h) [reset = 0h]

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Table 14-11381. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9190h**

Figure 14-3781. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-11383. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO	R/W	0h	Core1 - Reset base vector (v8 Mode) Address[33:2] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.14 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register (Offset = 9194h) [reset = 0h]

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Table 14-11384. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9194h**

Figure 14-3782. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR9_RST_VEC_HI_CORE1_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-11386. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE1_RESET_BASE_VECTOR_HI	R/W	0h	Core1 - Reset base vector (v8 Mode) Address[35:34] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.15 MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_LO Register (Offset = 9210h) [reset = 0h]

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Table 14-11387. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9210h**

Figure 14-3783. MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE2_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE2_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE2_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE2_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-11389. MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE2_RESET_BASE_VECTOR_LO	R/W	0h	Core2 - Reset base vector (v8 Mode) Address[33:2] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.16 MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_HI Register (Offset = 9214h) [reset = 0h]

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Table 14-11390. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9214h**

Figure 14-3784. MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR9_RST_VEC_HI_CORE2_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-11392. MAIN_SEC_MMR_CFG0_CLSTR9_CORE2_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE2_RESET_BASE_VECTOR_HI	R/W	0h	Core2 - Reset base vector (v8 Mode) Address[35:34] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.17 MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_LO Register (Offset = 9290h) [reset = 0h]

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Table 14-11393. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9290h**

Figure 14-3785. MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE3_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE3_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE3_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE3_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-11395. MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE3_RESET_BASE_VECTOR_LO	R/W	0h	Core3 - Reset base vector (v8 Mode) Address[33:2] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.18 MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_HI Register (Offset = 9294h) [reset = 0h]

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Table 14-11396. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9294h**

Figure 14-3786. MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR9_RST_VEC_HI_CORE3_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-11398. MAIN_SEC_MMR_CFG0_CLSTR9_CORE3_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE3_RESET_BASE_VECTOR_HI	R/W	0h	Core3 - Reset base vector (v8 Mode) Address[35:34] CAUTION: This bit must not be modified while A53 CPU is released from reset. Reset Source: mod_g_rst_n

14.2.1.4.1.2.19 MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register (Offset = D020h) [reset = 10FFh]

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Table 14-11399. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 D020h**

Figure 14-3787. MAIN_SEC_MMR_CFG0_CLSTR13_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CLSTR13_DEF_CORE_NUM</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR13_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR13_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-11401. MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR13_DEF_CORE_NUM	R	0h	Number of cores in cluster 000 - Single Core 001 - Dual Core 010 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR13_DEF_DSP_CORE_TYPE	R	10h	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR13_DEF_ARM_CORE_TYPE	R	FFh	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.4.1.2.20 MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register (Offset = D040h) [reset = 2454h]

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Table 14-11402. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 D040h**

Figure 14-3788. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Name Register

31	30	29	28	27	26	25	24
CLSTR13_CONFIG0_ENDIAN	CLSTR13_CONFIG0_CPU_SYS_RISCV_MODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED				CLSTR13_CONFIG0_MMA_PRESENT	RESERVED		CLSTR13_CONFIG0_EL2SIZE
NONE				R/W	NONE		R
0h				X	0h		0h

15	14	13	12	11	10	9	8
CLSTR13_CONFIG0_EL2SIZE		CLSTR13_CONFIG0_L2SIZE			CLSTR13_CONFIG0_L1DSIZE		CLSTR13_CONFIG0_L1PSIZE
R		R			R		R
0h		4h			2h		0h

7	6	5	4	3	2	1	0
CLSTR13_CONFIG0_L1PSIZE	CLSTR13_CONFIG0_VWIDTH		CLSTR13_CONFIG0_RISCV	CLSTR13_CONFIG0_MMA		CLSTR13_CONFIG0_CPU	
R	R		R	R		R	
0h	2h		1h	1h		0h	

Table 14-11404. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLSTR13_CONFIG0_ENDIAN	R/W	0h	Reset value of Endian control. Valid for DSP only. 0 - Little Endian 1 - Big Endian Reset Source: mod_g_rst_n
30	CLSTR13_CONFIG0_CPU_SYS_RISCV_MODE	R/W	0h	Activates CPU Booting in RiscV Mode 0 - Boot in C7x ISA Mode 1 - Boot in RiscV ISA Mode Reset Source: mod_g_rst_n
29:20	RESERVED	NONE	0h	Reserved
19	CLSTR13_CONFIG0_MMA_PRESENT	R/W	X	MMA Present Based on EFUSE. This bit is intended to be read not modified and writes to this bit will not have any impact on the C7xv256 mma present which is directly controlled by efuse. Reset Source: mod_g_rst_n
18:17	RESERVED	NONE	0h	Reserved

Table 14-11404. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:14	CLSTR13_CONFIG0_EL2SIZE	R	0h	EL2 Size Field values (others are reserved): 3'b111 - 4MB 3'b110 - 3.5MB 3'b101 - 3MB 3'b100 - 2.5MB 3'b011 - 2MB 3'b010 - 1.5MB 3'b001 - 1MB 3'b000 - None Reset Source: mod_g_rst_n
13:11	CLSTR13_CONFIG0_L2SIZE	R	4h	L2 Size Field values (others are reserved): 3'b111 - 2MB 3'b110 - 1.75MB 3'b101 - 1.5MB 3'b100 - 1.25MB 3'b011 - 1.0MB 3'b010 - 768KB 3'b001 - 512KB 3'b000 - None Reset Source: mod_g_rst_n
10:9	CLSTR13_CONFIG0_L1DSIZE	R	2h	L1D Size Field values (others are reserved): 2'b11 - 128KB 2'b10 - 64KB 2'b01 - 48KB 2'b00 - 32KB Reset Source: mod_g_rst_n
8:7	CLSTR13_CONFIG0_L1PSIZE	R	0h	L1P Size Field values (others are reserved): 2'b11 - 128KB 2'b10 - 64KB 2'b01 - 48KB 2'b00 - 32KB Reset Source: mod_g_rst_n
6:5	CLSTR13_CONFIG0_VWIDTH	R	2h	Vector Width Field values (others are reserved): 2'b11 - 512b 2'b10 - 256b 2'b01 - 128b 2'b00 - 64b Reset Source: mod_g_rst_n
4	CLSTR13_CONFIG0_RISCV	R	1h	RISCV ISA SUPPORT Field values (others are reserved): 1'b1 - Supported 1'b0 - Not Supported Reset Source: mod_g_rst_n
3:2	CLSTR13_CONFIG0_MMA	R	1h	MMA Type Field values (others are reserved): 2'b11 - MMA2 2'b10 - MMA2P1 2'b01 - Reserved 2'b00 - Reserved Reset Source: mod_g_rst_n

Table 14-11404. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	CLSTR13_CONFIG0_CPU	R	0h	CPU Type Field values (others are reserved): 2'b11 - Reserved 2'b10 - Reserved 2'b01 - Reserved 2'b00 - AC72 R10 Reset Source: mod_g_rst_n

14.2.1.4.1.2.21 MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register (Offset = D090h) [reset = 0h]

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Table 14-11405. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 D090h**

Figure 14-3789. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT16</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>RSVD</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT8</td></tr>
<tr><td colspan="6">NONE</td><td></td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT7</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT6</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT5</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT4</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT3</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT2</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT1</td><td>CLSTR13_PM_STATUS_DSP_IDLE_STAT0</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>

Table 14-11407. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	CLSTR13_PM_STATUS_DSP_IDLE_STAT16	R	X	C7x PBIST Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
8	CLSTR13_PM_STATUS_DSP_IDLE_STAT8	R	X	C7x DRU Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
7	CLSTR13_PM_STATUS_DSP_IDLE_STAT7	R	X	C7x L2 Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n

Table 14-11407. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CLSTR13_PM_STATUS_DSP_IDLE_STAT6	R	X	C7x Debug Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
5	CLSTR13_PM_STATUS_DSP_IDLE_STAT5	R	X	C7x SE Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
4	CLSTR13_PM_STATUS_DSP_IDLE_STAT4	R	X	C7x DMC Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
3	CLSTR13_PM_STATUS_DSP_IDLE_STAT3	R	X	C7x PMC Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
2	CLSTR13_PM_STATUS_DSP_IDLE_STAT2	R	X	C7x CPU Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
1	CLSTR13_PM_STATUS_DSP_IDLE_STAT1	R	X	C7x Core LPSC Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n
0	CLSTR13_PM_STATUS_DSP_IDLE_STAT0	R	X	Composite Idle Status Field values (others are reserved): 1'b1 - Idle 1'b0 - Not Idle Reset Source: mod_g_rst_n

14.2.1.4.1.2.22 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register (Offset = D110h) [reset = 0h]

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Table 14-11408. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 D110h**

Figure 14-3790. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-11410. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO	R/W	0h	Reset Vector Base Address 33:2 for C7x DSP Reset Source: mod_g_rst_n

14.2.1.4.1.2.23 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register (Offset = D114h) [reset = 0h]

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Table 14-11411. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 D114h**

Figure 14-3791. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR13_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-11413. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR13_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	R/W	0h	Reset Vector Base Address 35:34 for C7x DSP Reset Source: mod_g_rst_n

14.2.1.4.1.2.24 MAIN_SEC_MMR_CFG0_GIC_CONFIG Register

1 MAIN_SEC_MMR_CFG0_GIC_CONFIG Register (Offset = 18008h) [reset = F00h]

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Table 14-11414. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A1 8008h**

Figure 14-3792. MAIN_SEC_MMR_CFG0_GIC_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				GIC_CONFIG_A53SS0_CORE3_ACTIVE	GIC_CONFIG_A53SS0_CORE2_ACTIVE	GIC_CONFIG_A53SS0_CORE1_ACTIVE	GIC_CONFIG_A53SS0_CORE0_ACTIVE
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11416. MAIN_SEC_MMR_CFG0_GIC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	GIC_CONFIG_A53SS0_CORE3_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core3. When a core is in a low-power mode (cpu_active=0), the GIC will not route shared-SPI events to the core which would wake up the core resulting in increased power consumption. 0 - Core is in a software-transparent low power mode 1 - Core is active and available for shared SPIs Reset Source: mod_g_rst_n
10	GIC_CONFIG_A53SS0_CORE2_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core2. When a core is in a low-power mode (cpu_active=0), the GIC will not route shared-SPI events to the core which would wake up the core resulting in increased power consumption. 0 - Core is in a software-transparent low power mode 1 - Core is active and available for shared SPIs Reset Source: mod_g_rst_n
9	GIC_CONFIG_A53SS0_CORE1_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core1. When a core is in a low-power mode (cpu_active=0), the GIC will not route shared-SPI events to the core which would wake up the core resulting in increased power consumption. 0 - Core is in a software-transparent low power mode 1 - Core is active and available for shared SPIs Reset Source: mod_g_rst_n

Table 14-11416. MAIN_SEC_MMR_CFG0_GIC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	GIC_CONFIG_A53SS0_CORE0_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core0. When a core is in a low-power mode (cpu_active=0), the GIC will not route shared-SPI events to the core which would wake up the core resulting in increased power consumption. 0 - Core is in a software-transparent low power mode 1 - Core is active and available for shared SPIs Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.2 mcu_sec_mmr

mcu_sec_mmr

14.2.1.4.2.1 mcu_sec_mmr Summaries

mcu_sec_mmr Summaries

Table 14-11417. MCU_SEC_MMR_CFG2 Registers, Base Address=4594 0000h, Length=1024

Offset	Length	Register Name	MCU_MCU_SEC_MMR0 Physical Address
0h	32	MCU_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG	4594 0000h
40h	32	MCU_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG	4594 0040h

Table 14-11418. MCU_SEC_MMR_CFG0 Registers, Base Address=45A4 0000h, Length=1024

Offset	Length	Register Name	MCU_MCU_SEC_MMR0 Physical Address
0h	32	MCU_SEC_MMR_CFG0_PID	45A4 0000h
20h	32	MCU_SEC_MMR_CFG0_CLSTR0_DEF	45A4 0020h
40h	32	MCU_SEC_MMR_CFG0_CLSTR0_CFG	45A4 0040h
80h	32	MCU_SEC_MMR_CFG0_CLSTR0_PMCTRL	45A4 0080h
90h	32	MCU_SEC_MMR_CFG0_CLSTR0_PMSTAT	45A4 0090h
100h	32	MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG	45A4 0100h
110h	32	MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO	45A4 0110h
114h	32	MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI	45A4 0114h
120h	32	MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL	45A4 0120h
130h	32	MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT	45A4 0130h

14.2.1.4.2.2 mcu_sec_mmr Registers

mcu_sec_mmr Registers

14.2.1.4.2.2.1 MCU_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register

1 MCU_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]

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Table 14-11419. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**4594 0000h**

Figure 14-3793. MCU_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_DBG_CFG_DBGEN				CLSTR0_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11421. MCU_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR0_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR0_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.2.2.2 MCU_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register

1 MCU_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = 0h]

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Table 14-11422. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**4594 0040h**

Figure 14-3794. MCU_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.4.2.2.3 MCU_SEC_MMR_CFG0_PID Register

1 MCU_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800214h]

PID register

Return to Summary Table

Table 14-11425. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0000h**

Figure 14-3795. MCU_SEC_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">14h</td></tr>
</table>

Table 14-11427. MCU_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	14h	Reset Source: mod_g_rst_n

14.2.1.4.2.2.4 MCU_SEC_MMR_CFG0_CLSTR0_DEF Register

1 MCU_SEC_MMR_CFG0_CLSTR0_DEF Register (Offset = 20h) [reset = 1FF10h]

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Table 14-11428. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	45A4 0020h

Figure 14-3796. MCU_SEC_MMR_CFG0_CLSTR0_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CLSTR0_DEF_CORE_NUM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR0_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR0_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-11430. MCU_SEC_MMR_CFG0_CLSTR0_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	CLSTR0_DEF_CORE_NUM	R	1h	Number of cores in cluster 01 - Single Core 10 - Dual Core Reset Source: mod_g_rst_n
15:8	CLSTR0_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR0_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.4.2.2.5 MCU_SEC_MMR_CFG0_CLSTR0_CFG Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CFG Register (Offset = 40h) [reset = 60h]

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Table 14-11431. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0040h**

Figure 14-3797. MCU_SEC_MMR_CFG0_CLSTR0_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	CLSTR0_CFG_SINGLE_CORE_ONLY	CLSTR0_CFG_SINGLE_CORE	CLSTR0_CFG_MEM_INIT_DIS	CLSTR0_CFG_LOCKSTEP_EN	CLSTR0_CFG_DBG_NO_CLKSTOP	CLSTR0_CFG_TEINIT	CLSTR0_CFG_LOCKSTEP
	R	R	R/W	R	R/W	R/W	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-11433. MCU_SEC_MMR_CFG0_CLSTR0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR0_CFG_SINGLE_CORE_ONLY	R	1h	Single / Dual CPU Mode Supported: 0 = Both Dual and Single Core are supported 1 = Only Single Core Mode is Supported Reset Source: sys_por_rst_n
5	CLSTR0_CFG_SINGLE_CORE	R	1h	Single / Dual CPU Mode: 0 = Both CPUs are activated 1 = CPU1 Core is deactivated or No CPU1 Core Reset Source: sys_por_rst_n
4	CLSTR0_CFG_MEM_INIT_DIS	R/W	0h	Deactivates SRAM initialization (TCM, Cache Tags, etc) at reset Initialization must be performed for proper initial ECC initialization. The mem_init_dis value must be selected prior to R5 reset assertion. 1'b0 - Perform memory initialization 1'b1 - Deactivate memory initialization Reset Source: mod_g_rst_n
3	CLSTR0_CFG_LOCKSTEP_EN	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n
2	CLSTR0_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0 - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1 - CPU clocks not stopped in standby mode Reset Source: sys_por_rst_n

Table 14-11433. MCU_SEC_MMR_CFG0_CLSTR0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLSTR0_CFG_TEINIT	R/W	0h	Exception handling state at reset: 0 - ARM mode 1 - Thumb mode CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
0	CLSTR0_CFG_LOCKSTEP	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n

14.2.1.4.2.2.6 MCU_SEC_MMR_CFG0_CLSTR0_PMCTRL Register

1 MCU_SEC_MMR_CFG0_CLSTR0_PMCTRL Register (Offset = 80h) [reset = 0h]

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Table 14-11434. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0080h**

Figure 14-3798. MCU_SEC_MMR_CFG0_CLSTR0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.4.2.2.7 MCU_SEC_MMR_CFG0_CLSTR0_PMSTAT Register

1 MCU_SEC_MMR_CFG0_CLSTR0_PMSTAT Register (Offset = 90h) [reset = 0h]

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Table 14-11437. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0090h**

Figure 14-3799. MCU_SEC_MMR_CFG0_CLSTR0_PMSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

14.2.1.4.2.2.8 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]

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Table 14-11440. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	45A4 0100h

Figure 14-3800. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_CFG_NMFI_EN	RESERVED			CLSTR0_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR0_CORE0_CFG_BTCM_EN	RESERVED			CLSTR0_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-11442. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR0_CORE0_CFG_NMFI_EN	R/W	0h	Activate Core0 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR0_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR0_CORE0_CFG_BTCM_EN	R/W	1h	Activate Core0 BTCM RAM at reset CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved

Table 14-11442. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLSTR0_CORE0_CFG_ATCM_EN	R/W	0h	Activate Core0 ATCM RAM at reset CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.2.2.9 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 200h]

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Table 14-11443. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0110h**

Figure 14-3801. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-11445. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.2.2.10 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]

Return to Summary Table

Table 14-11446. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0114h**

Figure 14-3802. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-11448. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.2.2.11 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]

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Table 14-11449. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0120h**

Figure 14-3803. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR0_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-11451. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR0_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Field values (others are reserved): 1'b0 - CPU is held waiting to begin execution after reset is released 1'b1 - CPU is released to execute Reset Source: sys_por_rst_n

14.2.1.4.2.2.12 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register

1 MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = 0h]

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Table 14-11452. Instance Table

Instance Name	Physical Address
MCU_MCU_SEC_MMR0	**45A4 0130h**

Figure 14-3804. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR0_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR0_CORE0_PMSTAT_WFE	CLSTR0_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-11454. MCU_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE0_PMSTAT_CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR0_CORE0_PMSTAT_WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
0	CLSTR0_CORE0_PMSTAT_WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n

14.2.1.4.3 wkup_sec_mmr

wkup_sec_mmr

14.2.1.4.3.1 wkup_sec_mmr Summaries

wkup_sec_mmr Summaries

Table 14-11455. WKUP_SEC_MMR_CFG2 Registers, Base Address=4592 0000h, Length=131072

Offset	Length	Register Name	WKUP_WKUP_SEC_MMR0 Physical Address
1C000h	32	WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG	4593 C000h
1C040h	32	WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG	4593 C040h

Table 14-11456. WKUP_SEC_MMR_CFG0 Registers, Base Address=45A2 0000h, Length=131072

Offset	Length	Register Name	WKUP_WKUP_SEC_MMR0 Physical Address
0h	32	WKUP_SEC_MMR_CFG0_PID	45A2 0000h
1C020h	32	WKUP_SEC_MMR_CFG0_CLSTR28_DEF	45A3 C020h
1C040h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CFG	45A3 C040h
1C080h	32	WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL	45A3 C080h
1C090h	32	WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT	45A3 C090h
1C100h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG	45A3 C100h
1C110h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO	45A3 C110h
1C114h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI	45A3 C114h
1C120h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL	45A3 C120h
1C130h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT	45A3 C130h

14.2.1.4.3.2 wkup_sec_mmr Registers

wkup_sec_mmr Registers

14.2.1.4.3.2.1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register

1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register (Offset = 1C000h) [reset = AA00h]

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Table 14-11457. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**4593 C000h**

Figure 14-3805. WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_DBG_CFG_DBGEN				CLSTR28_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11459. WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR28_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
11:8	CLSTR28_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug activate. This is a fault tolerant bitfield that must be set 4'hA to activate 4'b1010 - Activated others - Deactivated Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.3.2.2 WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Register

1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Register (Offset = 1C040h) [reset = 0h]

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Table 14-11460. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**4593 C040h**

Figure 14-3806. WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.4.3.2.3 WKUP_SEC_MMR_CFG0_PID Register

1 WKUP_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800214h]

PID register

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Table 14-11463. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A2 0000h**

Figure 14-3807. WKUP_SEC_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		14h					

Table 14-11465. WKUP_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	14h	Reset Source: mod_g_rst_n

14.2.1.4.3.2.4 WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register (Offset = 1C020h) [reset = 1FF10h]

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Table 14-11466. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C020h**

Figure 14-3808. WKUP_SEC_MMR_CFG0_CLSTR28_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CLSTR28_DEF_CORE_NUM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR28_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR28_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-11468. WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	CLSTR28_DEF_CORE_NUM	R	1h	Number of cores in cluster 001 - Single Core 010 - Dual Core Reset Source: mod_g_rst_n
15:8	CLSTR28_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR28_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.4.3.2.5 WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register (Offset = 1C040h) [reset = 60h]

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Table 14-11469. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C040h**

Figure 14-3809. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD	CLSTR28_CFG_SINGLE_CORE_ONLY	CLSTR28_CFG_SINGLE_CORE	CLSTR28_CFG_MEM_INIT_DIS	CLSTR28_CFG_LOCKSTEP_EN	CLSTR28_CFG_DBG_NO_CLKSTOP	CLSTR28_CFG_TEINIT	CLSTR28_CFG_LOCKSTEP
	R	R	R/W	R	R/W	R/W	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-11471. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR28_CFG_SINGLE_CORE_ONLY	R	1h	Single / Dual CPU Mode Supported: 0 = Both Dual and Single Core are supported 1 = Only Single Core Mode is Supported Reset Source: sys_por_rst_n
5	CLSTR28_CFG_SINGLE_CORE	R	1h	Single / Dual CPU Mode: 0 = Both CPUs are activated 1 = CPU1 Core is deactivated, TCM size of CPU1 is doubled (uses CPU0 TCMs) Reset Source: sys_por_rst_n
4	CLSTR28_CFG_MEM_INIT_DIS	R/W	0h	Deactivates SRAM initialization (TCM, Cache Tags, etc) at reset Initialization must be performed for proper initial ECC initialization. The mem_init_dis value must be selected prior to R5 reset assertion. 1'b0 - Perform memory initialization 1'b1 - Deactivate memory initialization Reset Source: mod_g_rst_n
3	CLSTR28_CFG_LOCKSTEP_EN	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n
2	CLSTR28_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0 - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1 - CPU clocks not stopped in standby mode Reset Source: sys_por_rst_n

Table 14-11471. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLSTR28_CFG_TEINIT	R/W	0h	Exception handling state at reset: 0 - ARM mode 1 - Thumb mode CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
0	CLSTR28_CFG_LOCKSTEP	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n

14.2.1.4.3.2.6 WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Register (Offset = 1C080h) [reset = 0h]

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Table 14-11472. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C080h**

Figure 14-3810. WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							
0h							

14.2.1.4.3.2.7 WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Register (Offset = 1C090h) [reset = 0h]

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Table 14-11475. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C090h**

Figure 14-3811. WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

14.2.1.4.3.2.8 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register (Offset = 1C100h) [reset = 880h]

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Table 14-11478. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C100h

Figure 14-3812. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_CFG_NMFI_EN	RESERVED			CLSTR28_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR28_CORE0_CFG_BTCM_EN	RESERVED			CLSTR28_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-11480. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR28_CORE0_CFG_NMFI_EN	R/W	0h	Activate Core0 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR28_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR28_CORE0_CFG_BTCM_EN	R/W	1h	Activate Core0 BTCM RAM at reset CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved

Table 14-11480. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLSTR28_CORE0_CFG_ATCM_EN	R/W	0h	Activate Core0 ATCM RAM at reset CAUTION: This bit must not be modified while R5F CPU is released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.3.2.9 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register (Offset = 1C110h) [reset = 200h]

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Table 14-11481. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C110h**

Figure 14-3813. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-11483. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.3.2.10 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register (Offset = 1C114h) [reset = 0h]

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Table 14-11484. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C114h**

Figure 14-3814. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-11486. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.3.2.11 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register (Offset = 1C120h) [reset = 0h]

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Table 14-11487. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C120h**

Figure 14-3815. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR28_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-11489. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR28_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Field values (others are reserved): 1'b0 - CPU is held waiting to begin execution after reset is released 1'b1 - CPU is released to execute Reset Source: sys_por_rst_n

14.2.1.4.3.2.12 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register

1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register (Offset = 1C130h) [reset = 0h]

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Table 14-11490. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	**45A3 C130h**

Figure 14-3816. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CLSTR28_CORE0_PMSTAT_CLK_GATE</td><td>RESERVED</td><td>CLSTR28_CORE0_PMSTAT_WFE</td><td>CLSTR28_CORE0_PMSTAT_WFI</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>X</td><td>0h</td><td>X</td><td>X</td></tr>
</table>

Table 14-11492. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR28_CORE0_PMSTAT_CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR28_CORE0_PMSTAT_WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n
0	CLSTR28_CORE0_PMSTAT_WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state Note: Informaton is only valid when core is out of reset. Reset Source: mod_g_rst_n

14.2.2 Power Registers

14.2.2.1 PSC

PSC

14.2.2.1.1 PSC Summaries

PSC Summaries

Table 14-11493. PSC Registers, Base Address=0040 0000h, Length=4096

Offset	Length	Register Name	PSC0 Physical Address
0h	32	PSC_PID	0040 0000h
10h	32	PSC_GBLCTL	0040 0010h
14h	32	PSC_GBLSTAT	0040 0014h
18h	32	PSC_INTEVAL	0040 0018h
40h	32	PSC_MERRPR_J	0040 0040h + formula
50h	32	PSC_MERRCR_J	0040 0050h + formula
60h	32	PSC_PERRPR	0040 0060h
68h	32	PSC_PERRCR	0040 0068h
70h	32	PSC_EPCPR	0040 0070h
78h	32	PSC_EPCCR	0040 0078h
100h	32	PSC_RAILSTAT	0040 0100h
104h	32	PSC_RAILCTL	0040 0104h
108h	32	PSC_RAILSEL	0040 0108h
120h	32	PSC_PTCMD	0040 0120h
128h	32	PSC_PTSTAT	0040 0128h
200h	32	PSC_PDSTAT_J	0040 0200h + formula
300h	32	PSC_PDCTL_J	0040 0300h + formula
400h	32	PSC_PDCFG_J	0040 0400h + formula
600h	32	PSC_MDCFG_J	0040 0600h + formula
800h	32	PSC_MDSTAT_J	0040 0800h + formula
A00h	32	PSC_MDCTL_J	0040 0A00h + formula

14.2.2.1.2 PSC Registers

PSC Registers

14.2.2.1.2.1 PSC_PID Register

1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

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Table 14-11494. Instance Table

Instance Name	Physical Address
PSC0	**0040 0000h**

Figure 14-3817. PSC_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">482h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">482h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-11496. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.2 PSC_GBLCTL Register

1 PSC_GBLCTL Register (Offset = 10h) [reset = 0h]

This register contains global control to PSC.

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Table 14-11497. Instance Table

Instance Name	Physical Address
PSC0	**0040 0010h**

Figure 14-3818. PSC_GBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
IO_ANA_CTL							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11499. PSC_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po[7:0] outputs. Reset Source: chip_rst.chip_1_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.3 PSC_GBLSTAT Register

1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

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Table 14-11500. Instance Table

Instance Name	Physical Address
PSC0	**0040 0014h**

Figure 14-3819. PSC_GBLSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
EF_SMRFLEX							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							OVRIDE
NONE							R
0h							0h

Table 14-11502. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.4 PSC_INTEVAL Register

1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-11503. Instance Table

Instance Name	Physical Address
PSC0	**0040 0018h**

Figure 14-3820. PSC_INTEVAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GOSET	EPCSET	ERRSET	RESERVED
NONE				W	W	W	NONE
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPCEV	ERREV	ALLEV
NONE					W	W	W
0h					0h	0h	0h

Table 14-11505. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt Reset Source: chip_rst.chip_1_rst_n 0 Write of 0 has no effect 1 Re-evaluate the combined PSC interrupt PSC_ALLINT

14.2.2.1.2.5 PSC_MERRPR_j Register

1 PSC_MERRPR_j Register (Offset = 40h + formula) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Offset = 40h + (j * 4h); where j = 0 to 1d

Table 14-11506. Instance Table

Instance Name	Physical Address
PSC0	**0040 0040h + formula**

Figure 14-3821. PSC_MERRPR_j Name Register

31	30	29	28	27	26	25	24
M							
R							
0h							
23	22	21	20	19	18	17	16
M							
R							
0h							
15	14	13	12	11	10	9	8
M							
R							
0h							
7	6	5	4	3	2	1	0
M							
R							
0h							

Table 14-11508. PSC_MERRPR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.6 PSC_MERRCR_j Register

1 PSC_MERRCR_j Register (Offset = 50h + formula) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Offset = 50h + (j * 4h); where j = 0 to 1d

Table 14-11509. Instance Table

Instance Name	Physical Address
PSC0	**0040 0050h + formula**

Figure 14-3822. PSC_MERRCR_j Name Register

31	30	29	28	27	26	25	24
M							
W1TC							
0h							
23	22	21	20	19	18	17	16
M							
W1TC							
0h							
15	14	13	12	11	10	9	8
M							
W1TC							
0h							
7	6	5	4	3	2	1	0
M							
W1TC							
0h							

Table 14-11511. PSC_MERRCR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.7 PSC_PERRPR Register

1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11512. Instance Table

Instance Name	Physical Address
PSC0	**0040 0060h**

Figure 14-3823. PSC_PERRPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11514. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.8 PSC_PERRCR Register

1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11515. Instance Table

Instance Name	Physical Address
PSC0	**0040 0068h**

Figure 14-3824. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-11517. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.9 PSC_EPCPR Register

1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11518. Instance Table

Instance Name	Physical Address
PSC0	**0040 0070h**

Figure 14-3825. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-11520. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.10 PSC_EPCCR Register

1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11521. Instance Table

Instance Name	Physical Address
PSC0	**0040 0078h**

Figure 14-3826. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-11523. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.11 PSC_RAILSTAT Register

1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Return to Summary Table

Table 14-11524. Instance Table

Instance Name	Physical Address
PSC0	**0040 0100h**

Figure 14-3827. PSC_RAILSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RAILNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAILCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11526. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.12 PSC_RAILCTL Register

1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

Return to Summary Table

Table 14-11527. Instance Table

Instance Name	Physical Address
PSC0	**0040 0104h**

Figure 14-3828. PSC_RAILCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RAILCTR1							
R/W							
X							
7	6	5	4	3	2	1	0
RAILCTR0							
R/W							
X							

Table 14-11529. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.13 PSC_RAILSEL Register

1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

Return to Summary Table

Table 14-11530. Instance Table

Instance Name	Physical Address
PSC0	**0040 0108h**

Figure 14-3829. PSC_RAILSEL Name Register

31	30	29	28	27	26	25	24
P							
R/W							
X							
23	22	21	20	19	18	17	16
P							
R/W							
X							
15	14	13	12	11	10	9	8
P							
R/W							
X							
7	6	5	4	3	2	1	0
P							
R/W							
X							

Table 14-11532. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.14 PSC_PTCMD Register

1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11533. Instance Table

Instance Name	Physical Address
PSC0	**0040 0120h**

Figure 14-3830. PSC_PTCMD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11535. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 `Write of 0 has no effect` 1 `Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.`

14.2.2.1.2.15 PSC_PTSTAT Register

1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11536. Instance Table

Instance Name	Physical Address
PSC0	**0040 0128h**

Figure 14-3831. PSC_PTSTAT Name Register

31	30	29	28	27	26	25	24
GOSTAT							
R							
0h							
23	22	21	20	19	18	17	16
GOSTAT							
R							
0h							
15	14	13	12	11	10	9	8
GOSTAT							
R							
0h							
7	6	5	4	3	2	1	0
GOSTAT							
R							
0h							

Table 14-11538. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GOSTAT	R	0h	Power Domain n Transition Command Status Reset Source: chip_rst.chip_1_rst_n 0 `No transitions in progress in Power Domain` 1 `Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.`

14.2.2.1.2.16 PSC_PDSTAT_j Register

1 PSC_PDSTAT_j Register (Offset = 200h + formula) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Return to Summary Table

Offset = 200h + (j * 4h); where j = 0 to 13d

Table 14-11539. Instance Table

Instance Name	Physical Address
PSC0	**0040 0200h + formula**

Figure 14-3832. PSC_PDSTAT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>EMUIHB</td><td>PWRBAD</td><td>PORDONE</td><td>PORZ</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">STATE</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-11541. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Power domain is off` 1 `Power domain is on`

14.2.2.1.2.17 PSC_PDCTL_j Register

1 PSC_PDCTL_j Register (Offset = 300h + formula) [reset = 0h]

This is a control register. One register per power domain.

Return to Summary Table

Offset = 300h + (j * 4h); where j = 0 to 13d

Table 14-11542. Instance Table

Instance Name	Physical Address
PSC0	**0040 0300h + formula**

Figure 14-3833. PSC_PDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
WAKECNT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
NONE	R/W			NONE		R/W	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
NONE							R/W
0h							0h

Table 14-11544. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-11544. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 `Core Off, RAM Array Off, RAM Periphery Off` 8 `Core Retention, RAM Array Off, RAM Periphery Off` 9 `Core Retention, RAM Array Retention, RAM Periphery Off` 10 `Core On, RAM Array Retention, RAM Periphery Off` 11 `Core On, RAM Array Retention, RAM Periphery On` 15 `Core On, RAM Array On, RAM Periphery On`
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Off` 1 `On`

14.2.2.1.2.18 PSC_PDCFG_j Register

1 PSC_PDCFG_j Register (Offset = 400h + formula) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

Return to Summary Table

Offset = 400h + (j * 4h); where j = 0 to 13d

Table 14-11545. Instance Table

Instance Name	Physical Address
PSC0	**0040 0400h + formula**

Figure 14-3834. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-11547. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ICEPICK	R	0h	Icepick support Reset Source: chip_rst.chip_1_rst_n 0 This domain does not have IcePick support 1 This domain has IcePick support because one or more of its LPSCs have IcePick support
2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n
0	ALWAYSON	R	0h	Always on power domain Reset Source: chip_rst.chip_1_rst_n 0 This domain is not an AlwaysON power domain 1 This domain is an AlwaysON power domain

14.2.2.1.2.19 PSC_MDCFG_j Register

1 PSC_MDCFG_j Register (Offset = 600h + formula) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

Return to Summary Table

Offset = 600h + (j * 4h); where j = 0 to 62d

Table 14-11548. Instance Table

Instance Name	Physical Address
PSC0	**0040 0600h + formula**

Figure 14-3835. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-11550. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n

Table 14-11550. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.20 PSC_MDSTAT_j Register

1 PSC_MDSTAT_j Register (Offset = 800h + formula) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

Return to Summary Table

Offset = 800h + (j * 4h); where j = 0 to 62d

Table 14-11551. Instance Table

Instance Name	Physical Address
PSC0	**0040 0800h + formula**

Figure 14-3836. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X
7	6	5	4	3	2	1	0
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-11553. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired module state 1 Emulation alters user-desired module state
16	EMURST	R	0h	Emulation Alters Reset Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired reset 1 Emulation has altered module reset to be different from what user desires
15:13	RESERVED	NONE	0h	Reserved
12	MCKOUT	R	0h	Actual modclk output to module Reset Source: chip_rst.chip_1_rst_n 0 modclk gated 1 modclk on

Table 14-11553. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	X	Module reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 module reset initialization not done 1 module reset initialization done
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) OTHER Reserved

14.2.2.1.2.21 PSC_MDCTL_j Register

1 PSC_MDCTL_j Register (Offset = A00h + formula) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

Return to Summary Table

Offset = A00h + (j * 4h); where j = 0 to 62d

Table 14-11554. Instance Table

Instance Name	Physical Address
PSC0	**0040 0A00h + formula**

Figure 14-3837. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-11556. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description

31	FORCE	R/W	X	Force Bit
				Reset Source: chip_rst.chip_1_rst_n
				`0 No force`
				`1 Force`

30:13	RESERVED	NONE	0h	Reserved

12	RESETISO	R/W	0h	Reset Isolation
				Reset Source: chip_rst.chip_1_rst_n
				`0 No reset isolation`
				`1 Enable reset isolation`

11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n

10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active.
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

Table 14-11556. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable Reset Source: chip_rst.chip_1_rst_n 0 Not enabled 1 Interrupt enabled
8	LRSTZ	R/W	0h	Module local reset control Reset Source: chip_rst.chip_1_rst_n 0 assert local reset 1 de-assert local reset
7:5	RESERVED	NONE	0h	Reserved
4:0	NEXT	R/W	0h	Module Next State Only key states can be selected in this field. If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable. If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable. Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake OTHER Reserved

14.2.2.2 PSC

PSC

14.2.2.2.1 PSC Summaries

PSC Summaries

Table 14-11557. PSC Registers, Base Address=0400 0000h, Length=4096

Offset	Length	Register Name	WKUP_PSC0 Physical Address
0h	32	PSC_PID	0400 0000h
10h	32	PSC_GBLCTL	0400 0010h
14h	32	PSC_GBLSTAT	0400 0014h
18h	32	PSC_INTEVAL	0400 0018h
40h	32	PSC_MERRPR	0400 0040h
50h	32	PSC_MERRCR	0400 0050h
60h	32	PSC_PERRPR	0400 0060h
68h	32	PSC_PERRCR	0400 0068h
70h	32	PSC_EPCPR	0400 0070h
78h	32	PSC_EPCCR	0400 0078h
100h	32	PSC_RAILSTAT	0400 0100h
104h	32	PSC_RAILCTL	0400 0104h
108h	32	PSC_RAILSEL	0400 0108h
120h	32	PSC_PTCMD	0400 0120h
128h	32	PSC_PTSTAT	0400 0128h
200h	32	PSC_PDSTAT_J	0400 0200h + formula
300h	32	PSC_PDCTL_J	0400 0300h + formula
400h	32	PSC_PDCFG_J	0400 0400h + formula
600h	32	PSC_MDCFG_J	0400 0600h + formula
800h	32	PSC_MDSTAT_J	0400 0800h + formula
A00h	32	PSC_MDCTL_J	0400 0A00h + formula

14.2.2.2.2 PSC Registers

PSC Registers

14.2.2.2.2.1 PSC_PID Register

1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Return to Summary Table

Table 14-11558. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0000h**

Figure 14-3838. PSC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		0h		482h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
482h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-11560. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.2 PSC_GBLCTL Register

1 PSC_GBLCTL Register (Offset = 10h) [reset = 0h]

This register contains global control to PSC.

Return to Summary Table

Table 14-11561. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0010h**

Figure 14-3839. PSC_GBLCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IO_ANA_CTL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11563. PSC_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po[7:0] outputs. Reset Source: chip_rst.chip_1_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.2.2.3 PSC_GBLSTAT Register

1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

Return to Summary Table

Table 14-11564. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0014h**

Figure 14-3840. PSC_GBLSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EF_SMRFLEX							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							OVRIDE
NONE							R
0h							0h

Table 14-11566. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.4 PSC_INTEVAL Register

1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-11567. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0018h**

Figure 14-3841. PSC_INTEVAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td>GOSET</td><td>EPCSET</td><td>ERRSET</td><td>RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td>W</td><td>W</td><td>W</td><td>NONE</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>EPCEV</td><td>ERREV</td><td>ALLEV</td></tr>
<tr><td colspan="5">NONE</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11569. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n

0	ALLEV	W	0h	Re_evaluate combined PSC interrupt
				Reset Source: chip_rst.chip_1_rst_n
				`0` `Write of 0 has no effect`
				`1` `Re-evaluate the combined PSC interrupt PSC_ALLINT`

14.2.2.2.2.5 PSC_MERRPR Register

1 PSC_MERRPR Register (Offset = 40h) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-11570. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0040h**

Figure 14-3842. PSC_MERRPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11572. PSC_MERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.6 PSC_MERRCR Register

1 PSC_MERRCR Register (Offset = 50h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-11573. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0050h

Figure 14-3843. PSC_MERRCR Name Register

31	30	29	28	27	26	25	24
M							
W1TC							
0h							
23	22	21	20	19	18	17	16
M							
W1TC							
0h							
15	14	13	12	11	10	9	8
M							
W1TC							
0h							
7	6	5	4	3	2	1	0
M							
W1TC							
0h							

Table 14-11575. PSC_MERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.7 PSC_PERRPR Register

1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11576. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0060h**

Figure 14-3844. PSC_PERRPR Name Register

31	30	29	28	27	26	25	24
P							
R							
0h							
23	22	21	20	19	18	17	16
P							
R							
0h							
15	14	13	12	11	10	9	8
P							
R							
0h							
7	6	5	4	3	2	1	0
P							
R							
0h							

Table 14-11578. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.8 PSC_PERRCR Register

1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11579. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0068h**

Figure 14-3845. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-11581. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.9 PSC_EPCPR Register

1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11582. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0070h**

Figure 14-3846. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-11584. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.10 PSC_EPCCR Register

1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11585. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0078h**

Figure 14-3847. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-11587. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.11 PSC_RAILSTAT Register

1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Return to Summary Table

Table 14-11588. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0100h**

Figure 14-3848. PSC_RAILSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED			RAILNUM				
NONE			R				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RAILCNT							
R							
0h							

Table 14-11590. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.12 PSC_RAILCTL Register

1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

Return to Summary Table

Table 14-11591. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0104h**

Figure 14-3849. PSC_RAILCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RAILCTR1							
R/W							
X							
7	6	5	4	3	2	1	0
RAILCTR0							
R/W							
X							

Table 14-11593. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.13 PSC_RAILSEL Register

1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

Return to Summary Table

Table 14-11594. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0108h**

Figure 14-3850. PSC_RAILSEL Name Register

31	30	29	28	27	26	25	24
P							
R/W							
X							
23	22	21	20	19	18	17	16
P							
R/W							
X							
15	14	13	12	11	10	9	8
P							
R/W							
X							
7	6	5	4	3	2	1	0
P							
R/W							
X							

Table 14-11596. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.14 PSC_PTCMD Register

1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11597. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0120h**

Figure 14-3851. PSC_PTCMD Name Register

31	30	29	28	27	26	25	24
GO							
W1TS							
0h							
23	22	21	20	19	18	17	16
GO							
W1TS							
0h							
15	14	13	12	11	10	9	8
GO							
W1TS							
0h							
7	6	5	4	3	2	1	0
GO							
W1TS							
0h							

Table 14-11599. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 `Write of 0 has no effect` 1 `Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.`

14.2.2.2.2.15 PSC_PTSTAT Register

1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-11600. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0128h**

Figure 14-3852. PSC_PTSTAT Name Register

31	30	29	28	27	26	25	24
GOSTAT							
R							
0h							
23	22	21	20	19	18	17	16
GOSTAT							
R							
0h							
15	14	13	12	11	10	9	8
GOSTAT							
R							
0h							
7	6	5	4	3	2	1	0
GOSTAT							
R							
0h							

Table 14-11602. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GOSTAT	R	0h	Power Domain n Transition Command Status Reset Source: chip_rst.chip_1_rst_n 0 No transitions in progress in Power Domain 1 Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

14.2.2.2.2.16 PSC_PDSTAT_j Register

1 PSC_PDSTAT_j Register (Offset = 200h + formula) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Return to Summary Table

Offset = 200h + (j * 4h); where j = 0 to 1d

Table 14-11603. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0200h + formula**

Figure 14-3853. PSC_PDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			STATE				
NONE			R				
0h			0h				

Table 14-11605. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 Power domain is off 1 Power domain is on

14.2.2.2.2.17 PSC_PDCTL_j Register

1 PSC_PDCTL_j Register (Offset = 300h + formula) [reset = 0h]

This is a control register. One register per power domain.

Return to Summary Table

Offset = 300h + (j * 4h); where j = 0 to 1d

Table 14-11606. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0300h + formula**

Figure 14-3854. PSC_PDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
WAKECNT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
NONE	R/W			NONE		R/W	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
NONE							R/W
0h							0h

Table 14-11608. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-11608. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 `Core Off, RAM Array Off, RAM Periphery Off` 8 `Core Retention, RAM Array Off, RAM Periphery Off` 9 `Core Retention, RAM Array Retention, RAM Periphery Off` 10 `Core On, RAM Array Retention, RAM Periphery Off` 11 `Core On, RAM Array Retention, RAM Periphery On` 15 `Core On, RAM Array On, RAM Periphery On`
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Off` 1 `On`

14.2.2.2.2.18 PSC_PDCFG_j Register

1 PSC_PDCFG_j Register (Offset = 400h + formula) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

Return to Summary Table

Offset = 400h + (j * 4h); where j = 0 to 1d

Table 14-11609. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0400h + formula**

Figure 14-3855. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-11611. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ICEPICK	R	0h	Icepick support Reset Source: chip_rst.chip_1_rst_n 0 This domain does not have IcePick support 1 This domain has IcePick support because one or more of its LPSCs have IcePick support
2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n
0	ALWAYSON	R	0h	Always on power domain Reset Source: chip_rst.chip_1_rst_n 0 This domain is not an AlwaysON power domain 1 This domain is an AlwaysON power domain

14.2.2.2.2.19 PSC_MDCFG_j Register

1 PSC_MDCFG_j Register (Offset = 600h + formula) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

Return to Summary Table

Offset = 600h + (j * 4h); where j = 0 to 10d

Table 14-11612. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0600h + formula

Figure 14-3856. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-11614. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n

Table 14-11614. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.20 PSC_MDSTAT_j Register

1 PSC_MDSTAT_j Register (Offset = 800h + formula) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

Return to Summary Table

Offset = 800h + (j * 4h); where j = 0 to 10d

Table 14-11615. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0800h + formula

Figure 14-3857. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-11617. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired module state 1 Emulation alters user-desired module state
16	EMURST	R	0h	Emulation Alters Reset Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired reset 1 Emulation has altered module reset to be different from what user desires
15:13	RESERVED	NONE	0h	Reserved
12	MCKOUT	R	0h	Actual modclk output to module Reset Source: chip_rst.chip_1_rst_n 0 modclk gated 1 modclk on

Table 14-11617. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	X	Module reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 module reset initialization not done 1 module reset initialization done
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) OTHER Reserved

14.2.2.2.2.21 PSC_MDCTL_j Register

1 PSC_MDCTL_j Register (Offset = A00h + formula) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

Return to Summary Table

Offset = A00h + (j * 4h); where j = 0 to 10d

Table 14-11618. Instance Table

Instance Name	Physical Address
WKUP_PSC0	**0400 0A00h + formula**

Figure 14-3858. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-11620. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description

31	FORCE	R/W	X	Force Bit
				Reset Source: chip_rst.chip_1_rst_n
				`0 No force`
				`1 Force`

30:13	RESERVED	NONE	0h	Reserved

12	RESETISO	R/W	0h	Reset Isolation
				Reset Source: chip_rst.chip_1_rst_n
				`0 No reset isolation`
				`1 Enable reset isolation`

11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n

10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active.
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

Table 14-11620. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable Reset Source: chip_rst.chip_1_rst_n 0 Not enabled 1 Interrupt enabled
8	LRSTZ	R/W	0h	Module local reset control Reset Source: chip_rst.chip_1_rst_n 0 assert local reset 1 de-assert local reset
7:5	RESERVED	NONE	0h	Reserved
4:0	NEXT	R/W	0h	Module Next State Only key states can be selected in this field. If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable. If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable. Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake OTHER Reserved

14.2.2.3 PSC_FW_0

PSC_FW_0

14.2.2.3.1 PSC_FW_0 Summaries

PSC_FW_0 Summaries

Table 14-11621. CBASS_FW Registers, Base Address=4502 0000h, Length=1024

Offset	Length	Register Name	PSC0_FW_0 Physical Address
0h	32	CBASS_FW_DST_FWCH_REGION_0_CH_0_CONTROL	4502 0000h
4h	32	CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0	4502 0004h
8h	32	CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1	4502 0008h
Ch	32	CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2	4502 000Ch
20h	32	CBASS_FW_DST_FWCH_REGION_1_CH_0_CONTROL	4502 0020h
24h	32	CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0	4502 0024h
28h	32	CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1	4502 0028h
2Ch	32	CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2	4502 002Ch
40h	32	CBASS_FW_DST_FWCH_REGION_2_CH_0_CONTROL	4502 0040h
44h	32	CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0	4502 0044h
48h	32	CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1	4502 0048h
4Ch	32	CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2	4502 004Ch
60h	32	CBASS_FW_DST_FWCH_REGION_3_CH_0_CONTROL	4502 0060h
64h	32	CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0	4502 0064h
68h	32	CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1	4502 0068h
6Ch	32	CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2	4502 006Ch
80h	32	CBASS_FW_DST_FWCH_REGION_4_CH_0_CONTROL	4502 0080h
84h	32	CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0	4502 0084h
88h	32	CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1	4502 0088h
8Ch	32	CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2	4502 008Ch

Table 14-11622. CBASS_GLB Registers, Base Address=45B0 9000h, Length=1024

Offset	Length	Register Name	PSC0_FW_0 Physical Address
0h	32	CBASS_GLB_PID	45B0 9000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 9004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 9020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 9024h

Table 14-11622. CBASS_GLB Registers, Base Address=45B0 9000h, Length=1024 (continued)

Offset	Length	Register Name	PSC0_FW_0 Physical Address
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 9028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 902Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 9030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 9034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 9038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 9040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 9044h

14.2.2.3.2 PSC_FW_0 Registers

PSC_FW_0 Registers

14.2.2.3.2.1 CBASS_FW_DST_FWCH_REGION_0_CH_0_CONTROL Register

1 CBASS_FW_DST_FWCH_REGION_0_CH_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Channel 0 Control Register defines the control fields for the target slv0.slv region 0 channel 0 firewall.

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Table 14-11623. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0000h**

Figure 14-3859. CBASS_FW_DST_FWCH_REGION_0_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11625. CBASS_FW_DST_FWCH_REGION_0_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: main_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: main_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: main_mod_g_rst_n

14.2.2.3.2.2 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0 Register

1 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Channel 0 Permission 0 Register defines the permissions for the target slv0.slv region 0 channel 0 firewall.

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Table 14-11626. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0004h**

Figure 14-3860. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11628. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11628. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.3 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1 Register

1 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Channel 0 Permission 1 Register defines the permissions for the target slv0.slv region 0 channel 0 firewall.

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Table 14-11629. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0008h**

Figure 14-3861. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11631. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11631. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.4 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2 Register

1 CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Channel 0 Permission 2 Register defines the permissions for the target slv0.slv region 0 channel 0 firewall.

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Table 14-11632. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 000Ch**

Figure 14-3862. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11634. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11634. CBASS_FW_DST_FWCH_REGION_0_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.5 CBASS_FW_DST_FWCH_REGION_1_CH_0_CONTROL Register

1 CBASS_FW_DST_FWCH_REGION_1_CH_0_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Channel 0 Control Register defines the control fields for the target slv0.slv region 1 channel 0 firewall.

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Table 14-11635. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0020h**

Figure 14-3863. CBASS_FW_DST_FWCH_REGION_1_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11637. CBASS_FW_DST_FWCH_REGION_1_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: main_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: main_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: main_mod_g_rst_n

14.2.2.3.2.6 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0 Register

1 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Channel 0 Permission 0 Register defines the permissions for the target slv0.slv region 1 channel 0 firewall.

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Table 14-11638. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0024h**

Figure 14-3864. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11640. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11640. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.7 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1 Register

1 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Channel 0 Permission 1 Register defines the permissions for the target slv0.slv region 1 channel 0 firewall.

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Table 14-11641. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0028h**

Figure 14-3865. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11643. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11643. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.8 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2 Register

1 CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Channel 0 Permission 2 Register defines the permissions for the target slv0.slv region 1 channel 0 firewall.

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Table 14-11644. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 002Ch**

Figure 14-3866. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11646. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11646. CBASS_FW_DST_FWCH_REGION_1_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.9 CBASS_FW_DST_FWCH_REGION_2_CH_0_CONTROL Register

1 CBASS_FW_DST_FWCH_REGION_2_CH_0_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Channel 0 Control Register defines the control fields for the target slv0.slv region 2 channel 0 firewall.

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Table 14-11647. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0040h**

Figure 14-3867. CBASS_FW_DST_FWCH_REGION_2_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11649. CBASS_FW_DST_FWCH_REGION_2_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: main_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: main_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: main_mod_g_rst_n

14.2.2.3.2.10 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0 Register

1 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Channel 0 Permission 0 Register defines the permissions for the target slv0.slv region 2 channel 0 firewall.

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Table 14-11650. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0044h**

Figure 14-3868. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11652. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11652. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.11 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1 Register

1 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Channel 0 Permission 1 Register defines the permissions for the target slv0.slv region 2 channel 0 firewall.

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Table 14-11653. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0048h**

Figure 14-3869. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11655. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11655. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.12 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2 Register

1 CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Channel 0 Permission 2 Register defines the permissions for the target slv0.slv region 2 channel 0 firewall.

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Table 14-11656. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 004Ch**

Figure 14-3870. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11658. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11658. CBASS_FW_DST_FWCH_REGION_2_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.13 CBASS_FW_DST_FWCH_REGION_3_CH_0_CONTROL Register

1 CBASS_FW_DST_FWCH_REGION_3_CH_0_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Channel 0 Control Register defines the control fields for the target slv0.slv region 3 channel 0 firewall.

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Table 14-11659. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0060h**

Figure 14-3871. CBASS_FW_DST_FWCH_REGION_3_CH_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	RESERVED
NONE						R/W	NONE
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-11661. CBASS_FW_DST_FWCH_REGION_3_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: main_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: main_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: main_mod_g_rst_n

14.2.2.3.2.14 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0 Register

1 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Channel 0 Permission 0 Register defines the permissions for the target slv0.slv region 3 channel 0 firewall.

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Table 14-11662. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0064h**

Figure 14-3872. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11664. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11664. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.15 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1 Register

1 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Channel 0 Permission 1 Register defines the permissions for the target slv0.slv region 3 channel 0 firewall.

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Table 14-11665. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0068h**

Figure 14-3873. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11667. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11667. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.16 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2 Register

1 CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Channel 0 Permission 2 Register defines the permissions for the target slv0.slv region 3 channel 0 firewall.

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Table 14-11668. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 006Ch**

Figure 14-3874. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11670. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11670. CBASS_FW_DST_FWCH_REGION_3_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.17 CBASS_FW_DST_FWCH_REGION_4_CH_0_CONTROL Register

1 CBASS_FW_DST_FWCH_REGION_4_CH_0_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Channel 0 Control Register defines the control fields for the target slv0.slv region 4 channel 0 firewall.

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Table 14-11671. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0080h**

Figure 14-3875. CBASS_FW_DST_FWCH_REGION_4_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11673. CBASS_FW_DST_FWCH_REGION_4_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: main_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: main_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: main_mod_g_rst_n

14.2.2.3.2.18 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0 Register

1 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Channel 0 Permission 0 Register defines the permissions for the target slv0.slv region 4 channel 0 firewall.

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Table 14-11674. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0084h**

Figure 14-3876. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11676. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11676. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.19 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1 Register

1 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Channel 0 Permission 1 Register defines the permissions for the target slv0.slv region 4 channel 0 firewall.

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Table 14-11677. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 0088h**

Figure 14-3877. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11679. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11679. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.20 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2 Register

1 CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Channel 0 Permission 2 Register defines the permissions for the target slv0.slv region 4 channel 0 firewall.

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Table 14-11680. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**4502 008Ch**

Figure 14-3878. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11682. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: main_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: main_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: main_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: main_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: main_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n

Table 14-11682. CBASS_FW_DST_FWCH_REGION_4_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: main_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: main_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: main_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: main_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: main_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: main_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: main_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: main_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: main_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: main_mod_g_rst_n

14.2.2.3.2.21 CBASS_GLB_PID Register

1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66002102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-11683. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9000h**

Figure 14-3879. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
4h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-11685. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: main_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: main_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: main_mod_g_rst_n
15:11	RTL	R	4h	RTL revision. Will vary depending on release. Reset Source: main_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: main_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: main_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: main_mod_g_rst_n

14.2.2.3.2.22 CBASS_GLB_DESTINATION_ID Register

1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-11686. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9004h**

Figure 14-3880. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-11688. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: main_mod_g_rst_n

14.2.2.3.2.23 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-11689. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9020h**

Figure 14-3881. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-11691. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: main_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: main_mod_g_rst_n

14.2.2.3.2.24 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-11692. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9024h**

Figure 14-3882. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-11694. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: main_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: main_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: main_mod_g_rst_n

14.2.2.3.2.25 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-11695. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9028h**

Figure 14-3883. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11697. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: main_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: main_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.26 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-11698. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 902Ch**

Figure 14-3884. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-11700. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: main_mod_g_rst_n

14.2.2.3.2.27 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-11701. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9030h**

Figure 14-3885. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11703. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: main_mod_g_rst_n

14.2.2.3.2.28 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-11704. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9034h**

Figure 14-3886. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-11706. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: main_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: main_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: main_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: main_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: main_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: main_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: main_mod_g_rst_n

Table 14-11706. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: main_mod_g_rst_n

14.2.2.3.2.29 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-11707. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9038h**

Figure 14-3887. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11709. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: main_mod_g_rst_n

14.2.2.3.2.30 CBASS_GLB_EXCEPTION_PEND_SET Register

1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-11710. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9040h**

Figure 14-3888. CBASS_GLB_EXCEPTION_PEND_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11712. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: main_mod_g_rst_n

14.2.2.3.2.31 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-11713. Instance Table

Instance Name	Physical Address
PSC0_FW_0	**45B0 9044h**

Figure 14-3889. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-11715. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: main_mod_g_rst_n

14.2.2.4 VTM

VTM

14.2.2.4.1 VTM Summaries

VTM Summaries

Table 14-11716. VTM_CFG1 Registers, Base Address=00B0 0000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
0h	32	VTM_CFG1_PID	00B0 0000h
4h	32	VTM_CFG1_DEVINFO_PWR0	00B0 0004h
204h	32	VTM_CFG1_GT_TH1_INT_RAW_STAT_SET	00B0 0204h
208h	32	VTM_CFG1_GT_TH1_INT_EN_STAT_CLR	00B0 0208h
214h	32	VTM_CFG1_GT_TH1_INT_EN_SET	00B0 0214h
218h	32	VTM_CFG1_GT_TH1_INT_EN_CLR	00B0 0218h
224h	32	VTM_CFG1_GT_TH2_INT_RAW_STAT_SET	00B0 0224h
228h	32	VTM_CFG1_GT_TH2_INT_EN_STAT_CLR	00B0 0228h
234h	32	VTM_CFG1_GT_TH2_INT_EN_SET	00B0 0234h
238h	32	VTM_CFG1_GT_TH2_INT_EN_CLR	00B0 0238h
244h	32	VTM_CFG1_LT_TH0_INT_RAW_STAT_SET	00B0 0244h
248h	32	VTM_CFG1_LT_TH0_INT_EN_STAT_CLR	00B0 0248h
254h	32	VTM_CFG1_LT_TH0_INT_EN_SET	00B0 0254h
258h	32	VTM_CFG1_LT_TH0_INT_EN_CLR	00B0 0258h
0h	32	VTM_CFG1_VD_DEVINFO_J	00B0 0000h + formula
4h	32	VTM_CFG1_VD_OPPVID_J	00B0 0004h + formula
8h	32	VTM_CFG1_VD_EVT_STAT_J	00B0 0008h + formula
Ch	32	VTM_CFG1_VD_EVT_SET_J	00B0 000Ch + formula
10h	32	VTM_CFG1_VD_EVT_CLR_J	00B0 0010h + formula
0h	32	VTM_CFG1_TMPSENS_CTRL_J	00B0 0000h + formula
8h	32	VTM_CFG1_TMPSENS_STAT_J	00B0 0008h + formula
Ch	32	VTM_CFG1_TMPSENS_TH_J	00B0 000Ch + formula
10h	32	VTM_CFG1_TMPSENS_TH2_J	00B0 0010h + formula

Table 14-11717. VTM_CFG2 Registers, Base Address=00B0 1000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
8h	32	VTM_CFG2_CLK_CTRL	00B0 1008h
Ch	32	VTM_CFG2_MISC_CTRL	00B0 100Ch
10h	32	VTM_CFG2_MISC_CTRL2	00B0 1010h
20h	32	VTM_CFG2_SAMPLE_CTRL	00B0 1020h
0h	32	VTM_CFG2_TMPSENS_CTRL_J	00B0 1000h + formula
4h	32	VTM_CFG2_TMPSENS_TRIM_J	00B0 1004h + formula

Table 14-11718. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
0h	32	ECC_AGGR_REV	00B0 2000h
8h	32	ECC_AGGR_VECTOR	00B0 2008h

Table 14-11718. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024 (continued)

Offset	Length	Register Name	WKUP_VTM0 Physical Address
Ch	32	ECC_AGGR_STAT	00B0 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00B0 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00B0 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00B0 2040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00B0 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00B0 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00B0 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00B0 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00B0 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00B0 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00B0 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00B0 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00B0 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00B0 220Ch

14.2.2.4.2 VTM Registers

VTM Registers

14.2.2.4.2.1 VTM_CFG1_PID Register

1 VTM_CFG1_PID Register (Offset = 0h) [reset = 661B8901h]

VTM Peripheral Identification Register

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Table 14-11719. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0000h**

Figure 14-3890. VTM_CFG1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		61Bh			
23	22	21	20	19	18	17	16
FUNC							
R							
61Bh							
15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
11h					1h		
7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		1h					

Table 14-11721. VTM_CFG1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Business unit - Processors Reset Source: mod_g_rst_n
27:16	FUNC	R	61Bh	Module functional identifier - CTRL MMR Reset Source: mod_g_rst_n
15:11	R_RTL	R	11h	RTL revision number - actual value determined by RTL Reset Source: mod_g_rst_n
10:8	X_MAJOR	R	1h	Major revision number - actual value determined by RTL Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom revision number - actual value determined by RTL Reset Source: mod_g_rst_n
5:0	Y_MINOR	R	1h	Minor revision number - actual value determined by RTL Reset Source: mod_g_rst_n

14.2.2.4.2.2 VTM_CFG1_DEVINFO_PWR0 Register

1 VTM_CFG1_DEVINFO_PWR0 Register (Offset = 4h) [reset = 0h]

Device specific voltage domain and temp sensor information register.

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Table 14-11722. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0004h**

Figure 14-3891. VTM_CFG1_DEVINFO_PWR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				VTM_VD_MAP			
NONE				R			
0h				X			
15	14	13	12	11	10	9	8
RESERVED			VD_RTC	RESERVED			
NONE			R	NONE			
0h			X	0h			
7	6	5	4	3	2	1	0
TMPSENS_CT				CVD_CT			
R				R			
X				X			

Table 14-11724. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VTM_VD_MAP	R	X	Core voltage domain, cVD, global mapping 4-bit code, in the context of this SOC. It shows in which cVD this VTM is instantiated/placed. This field indicates in which core voltage domain, cVD, has been physically placed this VTM. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vtm_vd_map. Reset Source: mod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12	VD_RTC	R	X	RTC voltage domain presence. 0: There is NO VD_RTC in this SOC. 1: There is a VD_RTC in this SOC. Reset value is a VTM tieoff, d_vd_rtc. Reset Source: mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	TMPSENS_CT	R	X	Number of temperature sensors associated with this VTM. Valid values are 4'h0 - 4'h8. 0x0: NO temp-sensor associated to this VTM. 0x8: 8 temp-sensors associated to this VTM. 0x9 to 0xF: invalid values. Reset value is a VTM tieoff, d_vtm_tmpsens_ct. Reset Source: mod_g_rst_n

Table 14-11724. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CVD_CT	R	X	Number of core voltage domains in device. VD0 is always allocated to VD_RTC, if it exists, and VD1 always to VD_WKUP. The maximum number of cVDs in an SOC is 15, 0xF. Reset value is a VTM tieoff, d_device_cvd_ct. Reset Source: mod_g_rst_n

14.2.2.4.2.3 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register

1 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register (Offset = 204h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11725. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0204h**

Figure 14-3892. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11727. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending stats regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.4.2.4 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register

1 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register (Offset = 208h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH1 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11728. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0208h**

Figure 14-3893. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-11730. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt masked pending bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that includes the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.4.2.5 VTM_CFG1_GT_TH1_INT_EN_SET Register

1 VTM_CFG1_GT_TH1_INT_EN_SET Register (Offset = 214h) [reset = 0h]

Enable set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11731. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0214h**

Figure 14-3894. VTM_CFG1_GT_TH1_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11733. VTM_CFG1_GT_TH1_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.6 VTM_CFG1_GT_TH1_INT_EN_CLR Register

1 VTM_CFG1_GT_TH1_INT_EN_CLR Register (Offset = 218h) [reset = 0h]

Enable clear MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11734. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0218h**

Figure 14-3895. VTM_CFG1_GT_TH1_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-11736. VTM_CFG1_GT_TH1_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.7 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register

1 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register (Offset = 224h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11737. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0224h**

Figure 14-3896. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11739. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending status regardless of the enable setting. Reset Source: mod_g_rst_n

14.2.2.4.2.8 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register

1 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register (Offset = 228h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH2 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11740. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0228h**

Figure 14-3897. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INT_VD</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11742. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status including the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.4.2.9 VTM_CFG1_GT_TH2_INT_EN_SET Register

1 VTM_CFG1_GT_TH2_INT_EN_SET Register (Offset = 234h) [reset = 0h]

Enable set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11743. Instance Table

Instance Name	**Physical Address**
WKUP_VTM0	**00B0 0234h**

Figure 14-3898. VTM_CFG1_GT_TH2_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11745. VTM_CFG1_GT_TH2_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.10 VTM_CFG1_GT_TH2_INT_EN_CLR Register

1 VTM_CFG1_GT_TH2_INT_EN_CLR Register (Offset = 238h) [reset = 0h]

Enable clear MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11746. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0238h**

Figure 14-3899. VTM_CFG1_GT_TH2_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-11748. VTM_CFG1_GT_TH2_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.11 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register

1 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register (Offset = 244h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11749. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0244h**

Figure 14-3900. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11751. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the raw pending status regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.4.2.12 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register

1 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register (Offset = 248h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt LT_TH0 per voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-11752. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0248h**

Figure 14-3901. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-11754. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending status bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that factors in the corresponding enable along with the pending status. Reset Source: mod_g_rst_n

14.2.2.4.2.13 VTM_CFG1_LT_TH0_INT_EN_SET Register

1 VTM_CFG1_LT_TH0_INT_EN_SET Register (Offset = 254h) [reset = 0h]

Enable set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11755. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0254h**

Figure 14-3902. VTM_CFG1_LT_TH0_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-11757. VTM_CFG1_LT_TH0_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.14 VTM_CFG1_LT_TH0_INT_EN_CLR Register

1 VTM_CFG1_LT_TH0_INT_EN_CLR Register (Offset = 258h) [reset = 0h]

Enable clear MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-11758. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0258h**

Figure 14-3903. VTM_CFG1_LT_TH0_INT_EN_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INT_VD</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11760. VTM_CFG1_LT_TH0_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.4.2.15 VTM_CFG1_VD_DEVINFO_j Register

1 VTM_CFG1_VD_DEVINFO_j Register (Offset = 0h + formula) [reset = 0h]

Voltage domain a information register. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Return to Summary Table

Offset = 100h + (j * 20h); where j = 0 to 7d

Table 14-11761. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0000h + formula**

Figure 14-3904. VTM_CFG1_VD_DEVINFO_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			AVS0_SUP	VD_MAP			
NONE			R/W	R			
0h			X	X			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-11763. VTM_CFG1_VD_DEVINFO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	AVS0_SUP	R/W	X	Indicates VD0 AVS class0 support. Indicates if the cVD associated with this VTM's VD MMR supports AVS-Class0: 0: No AVS-Class0. 1: Supports-AVS-Class0. Reset value is from e-fuse at module (POR) reset, efuse_vd[j]_avs_sup. Reset Source: mod_g_rst_n
11:8	VD_MAP	R	X	Indicates the core voltage domain mapping of VTM VD. Device specific field. This field indicates to which SOC cVD is this VD of this VTM map to. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vd[j]_vd_map_ipcfg (technically a direct connection, not latched, so reset agnostic). Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.4.2.16 VTM_CFG1_VD_OPPVID_j Register

1 VTM_CFG1_VD_OPPVID_j Register (Offset = 4h + formula) [reset = 0h]

Voltage domain a VID actual code used as reference by Firmware to set the various voltage domain supply voltages. Reset defaults are sourced from efuse for each OPP. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

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Offset = 104h + (j * 20h); where j = 0 to 7d

Table 14-11764. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0004h + formula**

Figure 14-3905. VTM_CFG1_VD_OPPVID_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OPP_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OPP_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OPP_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OPP_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-11766. VTM_CFG1_VD_OPPVID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	OPP_3	R/W	X	OPP 3 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_3. Reset Source: mod_por_rst_n
23:16	OPP_2	R/W	X	OPP 2 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_2. Reset Source: mod_por_rst_n
15:8	OPP_1	R/W	X	OPP 1 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_1. Reset Source: mod_por_rst_n

Table 14-11766. VTM_CFG1_VD_OPPVID_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	OPP_0	R/W	X	OPP 0 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_0. Reset Source: mod_por_rst_n

14.2.2.4.2.17 VTM_CFG1_VD_EVT_STAT_j Register

1 VTM_CFG1_VD_EVT_STAT_j Register (Offset = 8h + formula) [reset = 0h]

Voltage domain a event and control status register.

Return to Summary Table

Offset = 108h + (j * 20h); where j = 0 to 7d

Table 14-11767. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0008h + formula**

Figure 14-3906. VTM_CFG1_VD_EVT_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT
NONE					R	R	R
0h					X	X	X

Table 14-11769. VTM_CFG1_VD_EVT_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LT_TH0_ALERT	R	X	This bit reflects the status of the TH0 undertemp alert resulting from the OR of all the similar alerts produced by the temp sensors selected by VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. Reset Source: mod_g_rst_n
1	GT_TH2_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the combination of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present level of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n
0	GT_TH1_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the OR of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present value of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n

14.2.2.4.2.18 VTM_CFG1_VD_EVT_SET_j Register

1 VTM_CFG1_VD_EVT_SET_j Register (Offset = Ch + formula) [reset = 0h]

Voltage domain a event select and control set register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Return to Summary Table

Offset = 10Ch + (j * 20h); where j = 0 to 7d

Table 14-11770. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 000Ch + formula**

Figure 14-3907. VTM_CFG1_VD_EVT_SET_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TSENS_EVT_SEL							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-11772. VTM_CFG1_VD_EVT_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TS	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field sets to 1 the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.4.2.19 VTM_CFG1_VD_EVT_CLR_j Register

1 VTM_CFG1_VD_EVT_CLR_j Register (Offset = 10h + formula) [reset = 0h]

Voltage domain a event select and control clear register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Return to Summary Table

Offset = 110h + (j * 20h); where j = 0 to 7d

Table 14-11773. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0010h + formula**

Figure 14-3908. VTM_CFG1_VD_EVT_CLR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENS_EVT_SEL							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11775. VTM_CFG1_VD_EVT_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TC	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field clears, = 0, the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.4.2.20 VTM_CFG1_TMPSENS_CTRL_j Register

1 VTM_CFG1_TMPSENS_CTRL_j Register (Offset = 0h + formula) [reset = 0h]

Temperature Sensor Band-gap control register for sensor j.

Return to Summary Table

Offset = 300h + (j * 20h); where j = 0 to 7d

Table 14-11776. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0000h + formula**

Figure 14-3909. VTM_CFG1_TMPSENS_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>LT_TH0_EN</td><td>GT_TH2_EN</td><td>GT_TH1_EN</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11778. VTM_CFG1_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	LT_TH0_EN	R/W	0h	Enable under-threshold0 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is < value set for threshold point 0. Reset value is POR only. Reset Source: mod_por_rst_n
9	GT_TH2_EN	R/W	0h	Enable over-threshold2 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 2. Reset value is POR only. Reset Source: mod_por_rst_n
8	GT_TH1_EN	R/W	0h	Enable over-threshold1 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 1. Reset value is POR only. Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.4.2.21 VTM_CFG1_TMPSENS_STAT_j Register

1 VTM_CFG1_TMPSENS_STAT_j Register (Offset = 8h + formula) [reset = 0h]

Temperature Sensor Band-gap Status register for sensor j.

Return to Summary Table

Offset = 308h + (j * 20h); where j = 0 to 7d

Table 14-11779. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0008h + formula

Figure 14-3910. VTM_CFG1_TMPSENS_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				VD_MAP			
NONE				R			
0h				X			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAXT_OUTRG_ALERT	LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT	EOC_FC_UPDATE	DATA_VALID	DATA_OUT	
R	R	R	R	R	R	R	
X	0h	0h	0h	0h	X	X	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_OUT							
R							
X							

Table 14-11781. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VD_MAP	R	X	Indicates the core voltage domain placement of the temp sensor. Device specific field. This field indicates in which core voltage domain, cVD, has been physically placed the temp-monitor. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff at POR, d_VTM_TMPSENS[j]_STAT_vd_map_ipcfg. Reset Source: mod_por_rst_n
15	MAXT_OUTRG_ALERT	R	X	This bit will be driven to a level 1 for a given temperature monitor if it has its corresponding bit maxt_outrg_en = 1, and the temperature reading is reporting to be outside the max temperature supported, temp > programmed value. The level of this signal is a reflection, with some clock delays, of the temperature code reading. This is NOT an sticky bit. Reset value is POR only. Reset Source: mod_por_rst_n

Table 14-11781. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	LT_TH0_ALERT	R	0h	This field reflects the status of the lt_th0_alert comparator result during continuous mode. The control MMR field lt_th0_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
13	GT_TH2_ALERT	R	0h	This field reflects the status of the gt_th2_alert comparator result during continuous mode. The control MMR field gt_th2_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
12	GT_TH1_ALERT	R	0h	This field reflects the status of the gt_th1_alert comparator result during continuous mode. The control MMR field gt_th1_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
11	EOC_FC_UPDATE	R	0h	First time end of conversion. This field is reset to 0 every time VTM.por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. This bit will be set to 1 after the first time after reset release that data_valid transitions from 0 to 1, and remain at 1 until next time either of por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz, or continuous mode deassertion. Reset Source: mod_por_rst_n
10	DATA_VALID	R	X	Data_valid signal value from sensor: ADC End of Conversion. End of conversion indicated by 0 to 1 transition. When high data_out(9:0) out of the temp-monitor is valid. This field doesn't reflect the instantaneous output from the temp-monitor. This field gets latched/ updated in this VTM register when the data_valid value from temp-monitor toggles. Note the data_valid sensor output is asserted for only a short time window (on the order of a few clock cycles). Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz. Reset Source: mod_por_rst_n
9:0	DATA_OUT	R	X	Data_out signal value from sensor: Temperature data from the ADC in monitor. Valid after VTM_TMPSENS[j]_STAT.eoc_fc_update = 1. This value will be latched in this VTM register every time monitor output data_valid transitions from 0 to 1 (specifically one vbus cycle after data_valid asserts). Reset value is POR only. Reset Source: mod_por_rst_n

14.2.2.4.2.22 VTM_CFG1_TMPSENS_TH_j Register

1 VTM_CFG1_TMPSENS_TH_j Register (Offset = Ch + formula) [reset = 0h]

Temperature Sensor Band-gap Threshold register for sensor j.

Return to Summary Table

Offset = 30Ch + (j * 20h); where j = 0 to 7d

Table 14-11782. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 000Ch + formula**

Figure 14-3911. VTM_CFG1_TMPSENS_TH_j Name Register

31	30	29	28	27	26	25	24
RESERVED						TH1_VAL	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TH1_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TH0_VAL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TH0_VAL							
R/W							
0h							

Table 14-11784. VTM_CFG1_TMPSENS_TH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TH1_VAL	R/W	0h	Threshold point-1, thpt1, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th1_val[9:0] and gt_th1_en=1, that will cause the VTM to set the gt_th1_alert output. Once the current temp reading =< th1_val[9:0] then gt_th1_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TH0_VAL	R/W	0h	Threshold point-0, thpt0, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is < th0_val[9:0] and lt_th0_en=1, that will cause the VTM to set the lt_th0_alert output. Once the current temp reading => th0_val[9:0] then lt_th0_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.4.2.23 VTM_CFG1_TMPSENS_TH2_j Register

1 VTM_CFG1_TMPSENS_TH2_j Register (Offset = 10h + formula) [reset = 0h]

Temperature Sensor Band-gap Threshold register 2 for sensor j.

Return to Summary Table

Offset = 310h + (j * 20h); where j = 0 to 7d

Table 14-11785. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 0010h + formula**

Figure 14-3912. VTM_CFG1_TMPSENS_TH2_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TH2_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TH2_VAL							
R/W							
0h							

Table 14-11787. VTM_CFG1_TMPSENS_TH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TH2_VAL	R/W	0h	Threshold point-2, thpt2, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th2_val[9:0] and gt_th2_en=1, that will cause the VTM to set the gt_th2_alert output. Once the current temp reading =< th2_val[9:0] then gt_th2_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.4.2.24 VTM_CFG2_CLK_CTRL Register

1 VTM_CFG2_CLK_CTRL Register (Offset = 8h) [reset = 0h]

VTM clock related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_tsens_clk_src_div. The tsens_clks_src_div field is Device specific.

Return to Summary Table

Table 14-11788. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 1008h**

Figure 14-3913. VTM_CFG2_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
TSENS_CLK_SEL	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TSENS_CLK_DIV				
NONE			R/W				
0h			0h				

Table 14-11790. VTM_CFG2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TSENS_CLK_SEL	R/W	0h	Temperature sensor clock source selector. Device specific. 0 = fix_ref_clk as source. 1 = fix_ref2_clk as source. Reset value is at POR only. Reset Source: mod_por_rst_n
30:5	RESERVED	NONE	0h	Reserved
4:0	TSENS_CLK_DIV	R/W	0h	Temperature sensor clock source divider selector. Device specific. Default set by e-fuse or tie-off. Divider uses select reference clock as source. 1 = 2x divide. ... 15 = 16x divide. ... 63 = 64x divide. Setting the value to 0 (1x divide) prevents any further clock divider programming unless the clock divider is reset. Reset value is from e-fuse at POR, efuse_tsens_clk_src_div. Reset Source: mod_por_rst_n

14.2.2.4.2.25 VTM_CFG2_MISC_CTRL Register

1 VTM_CFG2_MISC_CTRL Register (Offset = Ch) [reset = 0h]

VTM miscellaneous control bits.

Return to Summary Table

Table 14-11791. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 100Ch**

Figure 14-3914. VTM_CFG2_MISC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							ANY_MAXT_OUTRG_ALERT_EN
NONE							R/W
0h							0h

Table 14-11793. VTM_CFG2_MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ANY_MAXT_OUTRG_ALERT_EN	R/W	0h	This bit when enabled will cause the VTM's output therm_maxtemp_outrange_alert to be driven high, if any of the sources for the maxt_outrg_alert, is set high. Whenever all the maxt_outrg_alert enabled sensor alerts, out of the 8 possible are back to 0 then the output, therm_maxtemp_outrange_alert, will also return to 0. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.4.2.26 VTM_CFG2_MISC_CTRL2 Register

1 VTM_CFG2_MISC_CTRL2 Register (Offset = 10h) [reset = 0h]

VTM miscellaneous control bits.

Return to Summary Table

Table 14-11794. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 1010h**

Figure 14-3915. VTM_CFG2_MISC_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED						MAXT_OUTRG_ALERT_THR0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
MAXT_OUTRG_ALERT_THR0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						MAXT_OUTRG_ALERT_THR	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
MAXT_OUTRG_ALERT_THR							
R/W							
0h							

Table 14-11796. VTM_CFG2_MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	MAXT_OUTRG_ALERT_THR0	R/W	0h	This defines the global max temperature out of range safe sample value. If the alert is enabled globally and for the sensor and the sensor reads a value <= this value then the alert is cleared after being triggered. This safe threshold defines at what temp the alert can be cleared. Reset is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	MAXT_OUTRG_ALERT_THR	R/W	0h	This defines the global max temperature out of range sample value. If the alert is enabled globally and for the sensor and the sensor reads a value >= this value then the alert is triggered. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.4.2.27 VTM_CFG2_SAMPLE_CTRL Register

1 VTM_CFG2_SAMPLE_CTRL Register (Offset = 20h) [reset = 0h]

VTM sample related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_sample_clk_cnt. The sample_clk_cnt field is Device specific.

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Table 14-11797. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 1020h**

Figure 14-3916. VTM_CFG2_SAMPLE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SAMPLE_PER_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SAMPLE_PER_CNT							
R/W							
0h							

Table 14-11799. VTM_CFG2_SAMPLE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SAMPLE_PER_CNT	R/W	0h	Temperature sensor sample period count selector. Device specific. Default set by e-fuse or tie-off. This defines the sample period or number of sensor clocks between consecutive samples of the sensor allowed, from the start of the previous sample request to the start of the next sample request. After the sample is received the sensor status MMR fields will not be updated and the sensor will remain disabled. Reset value is from e-fuse at POR, efuse_sample_per_cnt. Reset Source: mod_por_rst_n

14.2.2.4.2.28 VTM_CFG2_TMPSENS_CTRL_j Register

1 VTM_CFG2_TMPSENS_CTRL_j Register (Offset = 0h + formula) [reset = 40h]

Temperature Sensor Band-gap control register for sensor j.

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Offset = 300h + (j * 20h); where j = 0 to 7d

Table 14-11800. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 1000h + formula**

Figure 14-3917. VTM_CFG2_TMPSENS_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MAXT_OUTRG_EN	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		
7	6	5	4	3	2	1	0
RESERVED	CLRZ	SOC	CONT	RESERVED			
NONE	R/W	R/W	R/W	NONE			
0h	1h	0h	0h	0h			

Table 14-11802. VTM_CFG2_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MAXT_OUTRG_EN	R/W	0h	Enable out-of-range event. This bit enables generation of the alert in case the given temperature sensors generates a temp code above a programmed max. 0 = Don't generate alert. 1 = Generate alert. Reset value is POR only. Reset Source: mod_por_rst_n
10:7	RESERVED	NONE	0h	Reserved
6	CLRZ	R/W	1h	Temp-Monitor control: 0 = Reset all Temp-monitor digital outputs. 1 = Allow operation of sensor. Reset value is POR only. Reset Source: mod_por_rst_n
5	SOC	R/W	0h	Temp-Monitor control: ADC Start of Conversion. A transition from 0 to 1 starts a new ADC conversion cycle. The bit with automatically clear when the conversion has completed. This mode is not valid when already in continuous mode. Reset value is POR only. Reset Source: mod_por_rst_n

Table 14-11802. VTM_CFG2_TMPSENS_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CONT	R/W	0h	Temp-Monitor control: ADC Continuous mode. Setting this mode enables the VTM to continuously monitor the sensor automatically. Each sample period the sensor will be accessed and the results captured. Reset value is POR only. Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.2.4.2.29 VTM_CFG2_TMPSENS_TRIM_j Register

1 VTM_CFG2_TMPSENS_TRIM_j Register (Offset = 4h + formula) [reset = 0h]

Temperature Sensor Band-gap trim values register for sensor j. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Return to Summary Table

Offset = 304h + (j * 20h); where j = 0 to 7d

Table 14-11803. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 1004h + formula**

Figure 14-3918. VTM_CFG2_TMPSENS_TRIM_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TRIMO					
NONE		R/W					
0h		X					
7	6	5	4	3	2	1	0
RESERVED			TRIMG				
NONE			R/W				
0h			X				

Table 14-11805. VTM_CFG2_TMPSENS_TRIM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	TRIMO	R/W	X	Trim offset bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimo. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TRIMG	R/W	X	Trim gain bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimg. Reset Source: mod_por_rst_n

14.2.2.4.2.30 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-11806. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2000h**

Figure 14-3919. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-11808. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.2.2.4.2.31 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-11809. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2008h**

Figure 14-3920. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11811. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.2.2.4.2.32 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-11812. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 200Ch**

Figure 14-3921. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_RAMS							
R							
4h							

Table 14-11814. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.2.2.4.2.33 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-11815. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2010h + formula**

Figure 14-3922. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-11817. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.2.2.4.2.34 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-11818. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 203Ch**

Figure 14-3923. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-11820. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.4.2.35 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-11821. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2040h**

Figure 14-3924. ECC_AGGR_SEC_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND</td><td>K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND</td><td>K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND</td><td>ECCAGG_PEND</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11823. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.4.2.36 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-11824. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2080h**

Figure 14-3925. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11826. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-11826. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.4.2.37 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-11827. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 20C0h**

Figure 14-3926. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11829. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-11829. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.4.2.38 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-11830. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 213Ch**

Figure 14-3927. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-11832. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.4.2.39 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-11833. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2140h**

Figure 14-3928. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11835. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.4.2.40 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-11836. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2180h**

Figure 14-3929. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-11838. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-11838. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.4.2.41 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-11839. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 21C0h**

Figure 14-3930. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-11841. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-11841. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.4.2.42 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-11842. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2200h**

Figure 14-3931. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11844. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.2.2.4.2.43 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-11845. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2204h**

Figure 14-3932. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-11847. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.2.2.4.2.44 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-11848. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 2208h**

Figure 14-3933. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-11850. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.2.2.4.2.45 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-11851. Instance Table

Instance Name	Physical Address
WKUP_VTM0	**00B0 220Ch**

Figure 14-3934. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-11853. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.2.3 Clocking Registers

14.2.3.1 MAIN_PLL_MMR_CFG Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.1.1 main_pll_mmr

main_pll_mmr

14.2.3.1.1.1 main_pll_mmr Summaries

main_pll_mmr Summaries

Table 14-11854. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=131072

Offset	Length	Register Name	PLL0 Physical Address
0h	32	MAIN_PLL_MMR_CFG_PLL0_PID	0068 0000h
8h	32	MAIN_PLL_MMR_CFG_PLL0_CFG	0068 0008h
10h	32	MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0	0068 0010h
14h	32	MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1	0068 0014h
20h	32	MAIN_PLL_MMR_CFG_PLL0_CTRL	0068 0020h
24h	32	MAIN_PLL_MMR_CFG_PLL0_STAT	0068 0024h
30h	32	MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0	0068 0030h
34h	32	MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1	0068 0034h
38h	32	MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL	0068 0038h
40h	32	MAIN_PLL_MMR_CFG_PLL0_SS_CTRL	0068 0040h
44h	32	MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD	0068 0044h
60h	32	MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL	0068 0060h
64h	32	MAIN_PLL_MMR_CFG_PLL0_CAL_STAT	0068 0064h
80h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0	0068 0080h
84h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1	0068 0084h
88h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2	0068 0088h
8Ch	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3	0068 008Ch
90h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4	0068 0090h
94h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5	0068 0094h
98h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6	0068 0098h
9Ch	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7	0068 009Ch
A0h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8	0068 00A0h
A4h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9	0068 00A4h
1000h	32	MAIN_PLL_MMR_CFG_PLL1_PID	0068 1000h
1008h	32	MAIN_PLL_MMR_CFG_PLL1_CFG	0068 1008h
1010h	32	MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0	0068 1010h
1014h	32	MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1	0068 1014h
1020h	32	MAIN_PLL_MMR_CFG_PLL1_CTRL	0068 1020h
1024h	32	MAIN_PLL_MMR_CFG_PLL1_STAT	0068 1024h
1030h	32	MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0	0068 1030h
1034h	32	MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1	0068 1034h
1038h	32	MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL	0068 1038h
1040h	32	MAIN_PLL_MMR_CFG_PLL1_SS_CTRL	0068 1040h
1044h	32	MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD	0068 1044h
1060h	32	MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL	0068 1060h
1064h	32	MAIN_PLL_MMR_CFG_PLL1_CAL_STAT	0068 1064h
1080h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0	0068 1080h
1084h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1	0068 1084h

Table 14-11854. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=131072 (continued)

Offset	Length	Register Name	PLL0 Physical Address
1088h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2	0068 1088h
108Ch	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3	0068 108Ch
1090h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4	0068 1090h
1094h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5	0068 1094h
1098h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6	0068 1098h
2000h	32	MAIN_PLL_MMR_CFG_PLL2_PID	0068 2000h
2008h	32	MAIN_PLL_MMR_CFG_PLL2_CFG	0068 2008h
2010h	32	MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0	0068 2010h
2014h	32	MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1	0068 2014h
2020h	32	MAIN_PLL_MMR_CFG_PLL2_CTRL	0068 2020h
2024h	32	MAIN_PLL_MMR_CFG_PLL2_STAT	0068 2024h
2030h	32	MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0	0068 2030h
2034h	32	MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1	0068 2034h
2038h	32	MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL	0068 2038h
2040h	32	MAIN_PLL_MMR_CFG_PLL2_SS_CTRL	0068 2040h
2044h	32	MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD	0068 2044h
2060h	32	MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL	0068 2060h
2064h	32	MAIN_PLL_MMR_CFG_PLL2_CAL_STAT	0068 2064h
2080h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0	0068 2080h
2084h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1	0068 2084h
2088h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2	0068 2088h
208Ch	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3	0068 208Ch
2090h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4	0068 2090h
2094h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5	0068 2094h
2098h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6	0068 2098h
209Ch	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7	0068 209Ch
20A0h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8	0068 20A0h
20A4h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9	0068 20A4h
5000h	32	MAIN_PLL_MMR_CFG_PLL5_PID	0068 5000h
5008h	32	MAIN_PLL_MMR_CFG_PLL5_CFG	0068 5008h
5010h	32	MAIN_PLL_MMR_CFG_PLL5_LOCKKEY0	0068 5010h
5014h	32	MAIN_PLL_MMR_CFG_PLL5_LOCKKEY1	0068 5014h
5020h	32	MAIN_PLL_MMR_CFG_PLL5_CTRL	0068 5020h
5024h	32	MAIN_PLL_MMR_CFG_PLL5_STAT	0068 5024h
5030h	32	MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL0	0068 5030h
5034h	32	MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL1	0068 5034h
5038h	32	MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL	0068 5038h
5040h	32	MAIN_PLL_MMR_CFG_PLL5_SS_CTRL	0068 5040h
5044h	32	MAIN_PLL_MMR_CFG_PLL5_SS_SPREAD	0068 5044h
5060h	32	MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL	0068 5060h
5064h	32	MAIN_PLL_MMR_CFG_PLL5_CAL_STAT	0068 5064h
5080h	32	MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL0	0068 5080h
5084h	32	MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL1	0068 5084h
5088h	32	MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL2	0068 5088h
7000h	32	MAIN_PLL_MMR_CFG_PLL7_PID	0068 7000h

Table 14-11854. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=131072 (continued)

Offset	Length	Register Name	PLL0 Physical Address
7008h	32	MAIN_PLL_MMR_CFG_PLL7_CFG	0068 7008h
7010h	32	MAIN_PLL_MMR_CFG_PLL7_LOCKKEY0	0068 7010h
7014h	32	MAIN_PLL_MMR_CFG_PLL7_LOCKKEY1	0068 7014h
7020h	32	MAIN_PLL_MMR_CFG_PLL7_CTRL	0068 7020h
7024h	32	MAIN_PLL_MMR_CFG_PLL7_STAT	0068 7024h
7030h	32	MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL0	0068 7030h
7034h	32	MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL1	0068 7034h
7038h	32	MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL	0068 7038h
7040h	32	MAIN_PLL_MMR_CFG_PLL7_SS_CTRL	0068 7040h
7044h	32	MAIN_PLL_MMR_CFG_PLL7_SS_SPREAD	0068 7044h
7060h	32	MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL	0068 7060h
7064h	32	MAIN_PLL_MMR_CFG_PLL7_CAL_STAT	0068 7064h
7080h	32	MAIN_PLL_MMR_CFG_PLL7_HSDIV_CTRL0	0068 7080h
8000h	32	MAIN_PLL_MMR_CFG_PLL8_PID	0068 8000h
8008h	32	MAIN_PLL_MMR_CFG_PLL8_CFG	0068 8008h
8010h	32	MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0	0068 8010h
8014h	32	MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1	0068 8014h
8020h	32	MAIN_PLL_MMR_CFG_PLL8_CTRL	0068 8020h
8024h	32	MAIN_PLL_MMR_CFG_PLL8_STAT	0068 8024h
8030h	32	MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0	0068 8030h
8034h	32	MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1	0068 8034h
8038h	32	MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL	0068 8038h
8040h	32	MAIN_PLL_MMR_CFG_PLL8_SS_CTRL	0068 8040h
8044h	32	MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD	0068 8044h
8060h	32	MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL	0068 8060h
8064h	32	MAIN_PLL_MMR_CFG_PLL8_CAL_STAT	0068 8064h
8080h	32	MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0	0068 8080h
C000h	32	MAIN_PLL_MMR_CFG_PLL12_PID	0068 C000h
C008h	32	MAIN_PLL_MMR_CFG_PLL12_CFG	0068 C008h
C010h	32	MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0	0068 C010h
C014h	32	MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1	0068 C014h
C020h	32	MAIN_PLL_MMR_CFG_PLL12_CTRL	0068 C020h
C024h	32	MAIN_PLL_MMR_CFG_PLL12_STAT	0068 C024h
C030h	32	MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0	0068 C030h
C034h	32	MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1	0068 C034h
C038h	32	MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL	0068 C038h
C040h	32	MAIN_PLL_MMR_CFG_PLL12_SS_CTRL	0068 C040h
C044h	32	MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD	0068 C044h
C060h	32	MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL	0068 C060h
C064h	32	MAIN_PLL_MMR_CFG_PLL12_CAL_STAT	0068 C064h
C080h	32	MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0	0068 C080h
F000h	32	MAIN_PLL_MMR_CFG_PLL15_PID	0068 F000h
F008h	32	MAIN_PLL_MMR_CFG_PLL15_CFG	0068 F008h
F010h	32	MAIN_PLL_MMR_CFG_PLL15_LOCKKEY0	0068 F010h
F014h	32	MAIN_PLL_MMR_CFG_PLL15_LOCKKEY1	0068 F014h

Table 14-11854. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=131072 (continued)

Offset	Length	Register Name	PLL0 Physical Address
F020h	32	MAIN_PLL_MMR_CFG_PLL15_CTRL	0068 F020h
F024h	32	MAIN_PLL_MMR_CFG_PLL15_STAT	0068 F024h
F030h	32	MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL0	0068 F030h
F034h	32	MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL1	0068 F034h
F038h	32	MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL	0068 F038h
F040h	32	MAIN_PLL_MMR_CFG_PLL15_SS_CTRL	0068 F040h
F044h	32	MAIN_PLL_MMR_CFG_PLL15_SS_SPREAD	0068 F044h
F060h	32	MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL	0068 F060h
F064h	32	MAIN_PLL_MMR_CFG_PLL15_CAL_STAT	0068 F064h
F080h	32	MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL0	0068 F080h
F084h	32	MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL1	0068 F084h
F088h	32	MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL2	0068 F088h
11000h	32	MAIN_PLL_MMR_CFG_PLL17_PID	0069 1000h
11008h	32	MAIN_PLL_MMR_CFG_PLL17_CFG	0069 1008h
11010h	32	MAIN_PLL_MMR_CFG_PLL17_LOCKKEY0	0069 1010h
11014h	32	MAIN_PLL_MMR_CFG_PLL17_LOCKKEY1	0069 1014h
11020h	32	MAIN_PLL_MMR_CFG_PLL17_CTRL	0069 1020h
11024h	32	MAIN_PLL_MMR_CFG_PLL17_STAT	0069 1024h
11030h	32	MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL0	0069 1030h
11034h	32	MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL1	0069 1034h
11038h	32	MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL	0069 1038h
11040h	32	MAIN_PLL_MMR_CFG_PLL17_SS_CTRL	0069 1040h
11044h	32	MAIN_PLL_MMR_CFG_PLL17_SS_SPREAD	0069 1044h
11060h	32	MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL	0069 1060h
11064h	32	MAIN_PLL_MMR_CFG_PLL17_CAL_STAT	0069 1064h
11080h	32	MAIN_PLL_MMR_CFG_PLL17_HSDIV_CTRL0	0069 1080h

14.2.3.1.1.2 main_pll_mmr Registers

main_pll_mmr Registers

14.2.3.1.1.2.1 MAIN_PLL_MMR_CFG_PLL0_PID Register

1 MAIN_PLL_MMR_CFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-11855. Instance Table

Instance Name	Physical Address
PLL0	**0068 0000h**

Figure 14-3935. MAIN_PLL_MMR_CFG_PLL0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">MISC</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-11857. MAIN_PLL_MMR_CFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.2 MAIN_PLL_MMR_CFG_PLL0_CFG Register

1 MAIN_PLL_MMR_CFG_PLL0_CFG Register (Offset = 8h) [reset = 3FF0801h]

pll MMR Configuration

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Table 14-11858. Instance Table

Instance Name	Physical Address
PLL0	**0068 0008h**

Figure 14-3936. MAIN_PLL_MMR_CFG_PLL0_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-11860. MAIN_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-11860. MAIN_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.3 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

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Table 14-11861. Instance Table

Instance Name	Physical Address
PLL0	**0068 0010h**

Figure 14-3937. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11863. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.4 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

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Table 14-11864. Instance Table

Instance Name	Physical Address
PLL0	**0068 0014h**

Figure 14-3938. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-11866. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.1.1.2.5 MAIN_PLL_MMR_CFG_PLL0_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

PLL0_CTRL - PLL0 Control

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Table 14-11867. Instance Table

Instance Name	Physical Address
PLL0	**0068 0020h**

Figure 14-3939. MAIN_PLL_MMR_CFG_PLL0_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-11869. MAIN_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-11869. MAIN_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.6 MAIN_PLL_MMR_CFG_PLL0_STAT Register

1 MAIN_PLL_MMR_CFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

PLL0_STAT - PLL0 Status

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Table 14-11870. Instance Table

Instance Name	Physical Address
PLL0	**0068 0024h**

Figure 14-3940. MAIN_PLL_MMR_CFG_PLL0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-11872. MAIN_PLL_MMR_CFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.7 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

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Table 14-11873. Instance Table

Instance Name	Physical Address
PLL0	**0068 0030h**

Figure 14-3941. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-11875. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.8 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-11876. Instance Table

Instance Name	Physical Address
PLL0	**0068 0034h**

Figure 14-3942. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-11878. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.9 MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

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Table 14-11879. Instance Table

Instance Name	Physical Address
PLL0	**0068 0038h**

Figure 14-3943. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-11881. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-11881. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.10 MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

PLL_SS_CTRL register for pll0

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Table 14-11882. Instance Table

Instance Name	Physical Address
PLL0	**0068 0040h**

Figure 14-3944. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-11884. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-11884. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.11 MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

PLL_SS_SPREAD register for pll0

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Table 14-11885. Instance Table

Instance Name	Physical Address
PLL0	**0068 0044h**

Figure 14-3945. MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-11887. MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.12 MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

PLL0_CAL_CTRL - PLL0 Calibration Control Register

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Table 14-11888. Instance Table

Instance Name	Physical Address
PLL0	**0068 0060h**

Figure 14-3946. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-11890. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-11890. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.13 MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

PLL0_CAL_STAT - PLL0 Calibration Status Register

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Table 14-11891. Instance Table

Instance Name	Physical Address
PLL0	**0068 0064h**

Figure 14-3947. MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-11893. MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.14 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

HSDIV_CTRL0 register for pll0

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Table 14-11894. Instance Table

Instance Name	**Physical Address**
PLL0	**0068 0080h**

Figure 14-3948. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11896. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.15 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

HSDIV_CTRL1 register for pll0

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Table 14-11897. Instance Table

Instance Name	Physical Address
PLL0	**0068 0084h**

Figure 14-3949. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-11899. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.16 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

HSDIV_CTRL2 register for pll0

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Table 14-11900. Instance Table

Instance Name	Physical Address
PLL0	**0068 0088h**

Figure 14-3950. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11902. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.17 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

HSDIV_CTRL3 register for pll0

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Table 14-11903. Instance Table

Instance Name	Physical Address
PLL0	**0068 008Ch**

Figure 14-3951. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11905. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.18 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

HSDIV_CTRL4 register for pll0

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Table 14-11906. Instance Table

Instance Name	Physical Address
PLL0	**0068 0090h**

Figure 14-3952. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11908. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.19 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = 0h]

HSDIV_CTRL5 register for pll0

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Table 14-11909. Instance Table

Instance Name	Physical Address
PLL0	**0068 0094h**

Figure 14-3953. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11911. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.20 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = 0h]

HSDIV_CTRL6 register for pll0

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Table 14-11912. Instance Table

Instance Name	Physical Address
PLL0	**0068 0098h**

Figure 14-3954. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-11914. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.21 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register (Offset = 9Ch) [reset = 0h]

HSDIV_CTRL7 register for pll0

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Table 14-11915. Instance Table

Instance Name	Physical Address
PLL0	**0068 009Ch**

Figure 14-3955. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11917. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.22 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register (Offset = A0h) [reset = 0h]

HSDIV_CTRL8 register for pll0

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Table 14-11918. Instance Table

Instance Name	Physical Address
PLL0	**0068 00A0h**

Figure 14-3956. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11920. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.23 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register

1 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register (Offset = A4h) [reset = 0h]

HSDIV_CTRL9 register for pll0

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Table 14-11921. Instance Table

Instance Name	Physical Address
PLL0	**0068 00A4h**

Figure 14-3957. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11923. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.24 MAIN_PLL_MMR_CFG_PLL1_PID Register

1 MAIN_PLL_MMR_CFG_PLL1_PID Register (Offset = 1000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-11924. Instance Table

Instance Name	Physical Address
PLL0	**0068 1000h**

Figure 14-3958. MAIN_PLL_MMR_CFG_PLL1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-11926. MAIN_PLL_MMR_CFG_PLL1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.25 MAIN_PLL_MMR_CFG_PLL1_CFG Register

1 MAIN_PLL_MMR_CFG_PLL1_CFG Register (Offset = 1008h) [reset = 7F0801h]

pll MMR Configuration

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Table 14-11927. Instance Table

Instance Name	Physical Address
PLL0	**0068 1008h**

Figure 14-3959. MAIN_PLL_MMR_CFG_PLL1_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
7Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
7Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-11929. MAIN_PLL_MMR_CFG_PLL1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-11929. MAIN_PLL_MMR_CFG_PLL1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.26 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register (Offset = 1010h) [reset = 0h]

PLL1_LOCKKEY0 - PLL1 Lock Key 0 Register

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Table 14-11930. Instance Table

Instance Name	Physical Address
PLL0	**0068 1010h**

Figure 14-3960. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-11932. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.27 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register (Offset = 1014h) [reset = 0h]

PLL1_LOCKKEY1 - PLL1 Lock Key 1 RegisterAddr

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Table 14-11933. Instance Table

Instance Name	Physical Address
PLL0	**0068 1014h**

Figure 14-3961. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-11935. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n

14.2.3.1.1.2.28 MAIN_PLL_MMR_CFG_PLL1_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL1_CTRL Register (Offset = 1020h) [reset = 80010011h]

PLL1_CTRL - PLL1 Control

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Table 14-11936. Instance Table

Instance Name	Physical Address
PLL0	**0068 1020h**

Figure 14-3962. MAIN_PLL_MMR_CFG_PLL1_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h

15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-11938. MAIN_PLL_MMR_CFG_PLL1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-11938. MAIN_PLL_MMR_CFG_PLL1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.29 MAIN_PLL_MMR_CFG_PLL1_STAT Register

1 MAIN_PLL_MMR_CFG_PLL1_STAT Register (Offset = 1024h) [reset = 0h]

PLL1_STAT - PLL1 Status

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Table 14-11939. Instance Table

Instance Name	Physical Address
PLL0	**0068 1024h**

Figure 14-3963. MAIN_PLL_MMR_CFG_PLL1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-11941. MAIN_PLL_MMR_CFG_PLL1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.30 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register (Offset = 1030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL1 Frequency Control 1 Register

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Table 14-11942. Instance Table

Instance Name	Physical Address
PLL0	**0068 1030h**

Figure 14-3964. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-11944. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.31 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register (Offset = 1034h) [reset = 0h]

PLL1_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-11945. Instance Table

Instance Name	Physical Address
PLL0	**0068 1034h**

Figure 14-3965. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-11947. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.32 MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register (Offset = 1038h) [reset = 1020001h]

PLL1_DIV_CTRL - PLL1 Output Clock Divider Register

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Table 14-11948. Instance Table

Instance Name	Physical Address
PLL0	**0068 1038h**

Figure 14-3966. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-11950. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-11950. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.33 MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register (Offset = 1040h) [reset = 80000000h]

PLL_SS_CTRL register for pll1

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Table 14-11951. Instance Table

Instance Name	Physical Address
PLL0	**0068 1040h**

Figure 14-3967. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-11953. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-11953. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.34 MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register (Offset = 1044h) [reset = 10001h]

PLL_SS_SPREAD register for pll1

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Table 14-11954. Instance Table

Instance Name	Physical Address
PLL0	**0068 1044h**

Figure 14-3968. MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-11956. MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.35 MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register (Offset = 1060h) [reset = 20000h]

PLL1_CAL_CTRL - PLL1 Calibration Control Register

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Table 14-11957. Instance Table

Instance Name	Physical Address
PLL0	**0068 1060h**

Figure 14-3969. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W							
0h							

Table 14-11959. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-11959. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.36 MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register (Offset = 1064h) [reset = 0h]

PLL1_CAL_STAT - PLL1 Calibration Status Register

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Table 14-11960. Instance Table

Instance Name	Physical Address
PLL0	**0068 1064h**

Figure 14-3970. MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-11962. MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.37 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register (Offset = 1080h) [reset = 0h]

HSDIV_CTRL0 register for pll1

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Table 14-11963. Instance Table

Instance Name	Physical Address
PLL0	**0068 1080h**

Figure 14-3971. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11965. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.38 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register (Offset = 1084h) [reset = 0h]

HSDIV_CTRL1 register for pll1

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Table 14-11966. Instance Table

Instance Name	Physical Address
PLL0	**0068 1084h**

Figure 14-3972. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11968. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.39 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register (Offset = 1088h) [reset = 0h]

HSDIV_CTRL2 register for pll1

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Table 14-11969. Instance Table

Instance Name	Physical Address
PLL0	**0068 1088h**

Figure 14-3973. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11971. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.40 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register (Offset = 108Ch) [reset = 0h]

HSDIV_CTRL3 register for pll1

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Table 14-11972. Instance Table

Instance Name	Physical Address
PLL0	**0068 108Ch**

Figure 14-3974. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11974. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.41 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register (Offset = 1090h) [reset = 0h]

HSDIV_CTRL4 register for pll1

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Table 14-11975. Instance Table

Instance Name	Physical Address
PLL0	**0068 1090h**

Figure 14-3975. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-11977. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.42 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register (Offset = 1094h) [reset = 0h]

HSDIV_CTRL5 register for pll1

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Table 14-11978. Instance Table

Instance Name	Physical Address
PLL0	**0068 1094h**

Figure 14-3976. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11980. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.43 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register

1 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register (Offset = 1098h) [reset = 0h]

HSDIV_CTRL6 register for pll1

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Table 14-11981. Instance Table

Instance Name	Physical Address
PLL0	**0068 1098h**

Figure 14-3977. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-11983. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.44 MAIN_PLL_MMR_CFG_PLL2_PID Register

1 MAIN_PLL_MMR_CFG_PLL2_PID Register (Offset = 2000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-11984. Instance Table

Instance Name	Physical Address
PLL0	**0068 2000h**

Figure 14-3978. MAIN_PLL_MMR_CFG_PLL2_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-11986. MAIN_PLL_MMR_CFG_PLL2_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.45 MAIN_PLL_MMR_CFG_PLL2_CFG Register

1 MAIN_PLL_MMR_CFG_PLL2_CFG Register (Offset = 2008h) [reset = 3FF0801h]

pll MMR Configuration

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Table 14-11987. Instance Table

Instance Name	Physical Address
PLL0	**0068 2008h**

Figure 14-3979. MAIN_PLL_MMR_CFG_PLL2_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
3FFh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
3FFh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-11989. MAIN_PLL_MMR_CFG_PLL2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-11989. MAIN_PLL_MMR_CFG_PLL2_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.46 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register (Offset = 2010h) [reset = 0h]

PLL2_LOCKKEY0 - PLL2 Lock Key 0 Register

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Table 14-11990. Instance Table

Instance Name	Physical Address
PLL0	**0068 2010h**

Figure 14-3980. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-11992. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.47 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register (Offset = 2014h) [reset = 0h]

PLL2_LOCKKEY1 - PLL2 Lock Key 1 RegisterAddr

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Table 14-11993. Instance Table

Instance Name	Physical Address
PLL0	**0068 2014h**

Figure 14-3981. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-11995. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n

14.2.3.1.1.2.48 MAIN_PLL_MMR_CFG_PLL2_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL2_CTRL Register (Offset = 2020h) [reset = 80010011h]

PLL2_CTRL - PLL2 Control

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Table 14-11996. Instance Table

Instance Name	Physical Address
PLL0	**0068 2020h**

Figure 14-3982. MAIN_PLL_MMR_CFG_PLL2_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-11998. MAIN_PLL_MMR_CFG_PLL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-11998. MAIN_PLL_MMR_CFG_PLL2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.49 MAIN_PLL_MMR_CFG_PLL2_STAT Register

1 MAIN_PLL_MMR_CFG_PLL2_STAT Register (Offset = 2024h) [reset = 0h]

PLL2_STAT - PLL2 Status

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Table 14-11999. Instance Table

Instance Name	Physical Address
PLL0	**0068 2024h**

Figure 14-3983. MAIN_PLL_MMR_CFG_PLL2_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12001. MAIN_PLL_MMR_CFG_PLL2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.50 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register (Offset = 2030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL2 Frequency Control 2 Register

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Table 14-12002. Instance Table

Instance Name	Physical Address
PLL0	**0068 2030h**

Figure 14-3984. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-12004. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.51 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register (Offset = 2034h) [reset = 0h]

PLL2_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12005. Instance Table

Instance Name	Physical Address
PLL0	**0068 2034h**

Figure 14-3985. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12007. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.52 MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register (Offset = 2038h) [reset = 1020001h]

PLL2_DIV_CTRL - PLL2 Output Clock Divider Register

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Table 14-12008. Instance Table

Instance Name	Physical Address
PLL0	**0068 2038h**

Figure 14-3986. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12010. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12010. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.53 MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register (Offset = 2040h) [reset = 80000000h]

PLL_SS_CTRL register for pll2

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Table 14-12011. Instance Table

Instance Name	Physical Address
PLL0	**0068 2040h**

Figure 14-3987. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12013. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12013. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.54 MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register (Offset = 2044h) [reset = 10001h]

PLL_SS_SPREAD register for pll2

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Table 14-12014. Instance Table

Instance Name	Physical Address
PLL0	**0068 2044h**

Figure 14-3988. MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12016. MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.55 MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register (Offset = 2060h) [reset = 20000h]

PLL2_CAL_CTRL - PLL2 Calibration Control Register

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Table 14-12017. Instance Table

Instance Name	Physical Address
PLL0	**0068 2060h**

Figure 14-3989. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12019. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12019. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.56 MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register (Offset = 2064h) [reset = 0h]

PLL2_CAL_STAT - PLL2 Calibration Status Register

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Table 14-12020. Instance Table

Instance Name	Physical Address
PLL0	**0068 2064h**

Figure 14-3990. MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12022. MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.57 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register (Offset = 2080h) [reset = 0h]

HSDIV_CTRL0 register for pll2

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Table 14-12023. Instance Table

Instance Name	Physical Address
PLL0	**0068 2080h**

Figure 14-3991. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12025. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.58 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register (Offset = 2084h) [reset = 0h]

HSDIV_CTRL1 register for pll2

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Table 14-12026. Instance Table

Instance Name	Physical Address
PLL0	**0068 2084h**

Figure 14-3992. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12028. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.59 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register (Offset = 2088h) [reset = 0h]

HSDIV_CTRL2 register for pll2

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Table 14-12029. Instance Table

Instance Name	Physical Address
PLL0	**0068 2088h**

Figure 14-3993. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12031. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.60 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register (Offset = 208Ch) [reset = 0h]

HSDIV_CTRL3 register for pll2

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Table 14-12032. Instance Table

Instance Name	Physical Address
PLL0	**0068 208Ch**

Figure 14-3994. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12034. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.61 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register (Offset = 2090h) [reset = 0h]

HSDIV_CTRL4 register for pll2

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Table 14-12035. Instance Table

Instance Name	**Physical Address**
PLL0	**0068 2090h**

Figure 14-3995. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12037. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.62 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register (Offset = 2094h) [reset = 0h]

HSDIV_CTRL5 register for pll2

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Table 14-12038. Instance Table

Instance Name	Physical Address
PLL0	**0068 2094h**

Figure 14-3996. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12040. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.63 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register (Offset = 2098h) [reset = 0h]

HSDIV_CTRL6 register for pll2

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Table 14-12041. Instance Table

Instance Name	Physical Address
PLL0	**0068 2098h**

Figure 14-3997. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12043. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.64 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register (Offset = 209Ch) [reset = 0h]

HSDIV_CTRL7 register for pll2

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Table 14-12044. Instance Table

Instance Name	Physical Address
PLL0	**0068 209Ch**

Figure 14-3998. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12046. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.65 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register (Offset = 20A0h) [reset = 0h]

HSDIV_CTRL8 register for pll2

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Table 14-12047. Instance Table

Instance Name	Physical Address
PLL0	**0068 20A0h**

Figure 14-3999. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12049. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.66 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register

1 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register (Offset = 20A4h) [reset = 0h]

HSDIV_CTRL9 register for pll2

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Table 14-12050. Instance Table

Instance Name	Physical Address
PLL0	**0068 20A4h**

Figure 14-4000. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12052. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.67 MAIN_PLL_MMR_CFG_PLL5_PID Register

1 MAIN_PLL_MMR_CFG_PLL5_PID Register (Offset = 5000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12053. Instance Table

Instance Name	Physical Address
PLL0	**0068 5000h**

Figure 14-4001. MAIN_PLL_MMR_CFG_PLL5_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12055. MAIN_PLL_MMR_CFG_PLL5_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.68 MAIN_PLL_MMR_CFG_PLL5_CFG Register

1 MAIN_PLL_MMR_CFG_PLL5_CFG Register (Offset = 5008h) [reset = 70801h]

pll MMR Configuration

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Table 14-12056. Instance Table

Instance Name	Physical Address
PLL0	**0068 5008h**

Figure 14-4002. MAIN_PLL_MMR_CFG_PLL5_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
7h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
7h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12058. MAIN_PLL_MMR_CFG_PLL5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12058. MAIN_PLL_MMR_CFG_PLL5_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.69 MAIN_PLL_MMR_CFG_PLL5_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL5_LOCKKEY0 Register (Offset = 5010h) [reset = 0h]

PLL5_LOCKKEY0 - PLL5 Lock Key 0 Register

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Table 14-12059. Instance Table

Instance Name	Physical Address
PLL0	**0068 5010h**

Figure 14-4003. MAIN_PLL_MMR_CFG_PLL5_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12061. MAIN_PLL_MMR_CFG_PLL5_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition5 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.70 MAIN_PLL_MMR_CFG_PLL5_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL5_LOCKKEY1 Register (Offset = 5014h) [reset = 0h]

PLL5_LOCKKEY1 - PLL5 Lock Key 1 RegisterAddr

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Table 14-12062. Instance Table

Instance Name	Physical Address
PLL0	**0068 5014h**

Figure 14-4004. MAIN_PLL_MMR_CFG_PLL5_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12064. MAIN_PLL_MMR_CFG_PLL5_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition5 registers Reset Source: srst_n

14.2.3.1.1.2.71 MAIN_PLL_MMR_CFG_PLL5_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL5_CTRL Register (Offset = 5020h) [reset = 80010011h]

PLL5_CTRL - PLL5 Control

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Table 14-12065. Instance Table

Instance Name	Physical Address
PLL0	**0068 5020h**

Figure 14-4005. MAIN_PLL_MMR_CFG_PLL5_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12067. MAIN_PLL_MMR_CFG_PLL5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12067. MAIN_PLL_MMR_CFG_PLL5_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.72 MAIN_PLL_MMR_CFG_PLL5_STAT Register

1 MAIN_PLL_MMR_CFG_PLL5_STAT Register (Offset = 5024h) [reset = 0h]

PLL5_STAT - PLL5 Status

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Table 14-12068. Instance Table

Instance Name	Physical Address
PLL0	**0068 5024h**

Figure 14-4006. MAIN_PLL_MMR_CFG_PLL5_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12070. MAIN_PLL_MMR_CFG_PLL5_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.73 MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL0 Register (Offset = 5030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL5 Frequency Control 5 Register

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Table 14-12071. Instance Table

Instance Name	Physical Address
PLL0	**0068 5030h**

Figure 14-4007. MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-12073. MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.74 MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL1 Register (Offset = 5034h) [reset = 0h]

PLL5_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12074. Instance Table

Instance Name	Physical Address
PLL0	**0068 5034h**

Figure 14-4008. MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FB_DIV_FRAC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FB_DIV_FRAC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FB_DIV_FRAC							
R/W							
0h							

Table 14-12076. MAIN_PLL_MMR_CFG_PLL5_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.75 MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL Register (Offset = 5038h) [reset = 1020001h]

PLL5_DIV_CTRL - PLL5 Output Clock Divider Register

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Table 14-12077. Instance Table

Instance Name	Physical Address
PLL0	**0068 5038h**

Figure 14-4009. MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12079. MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12079. MAIN_PLL_MMR_CFG_PLL5_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.76 MAIN_PLL_MMR_CFG_PLL5_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL5_SS_CTRL Register (Offset = 5040h) [reset = 80000000h]

PLL_SS_CTRL register for pll5

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Table 14-12080. Instance Table

Instance Name	Physical Address
PLL0	**0068 5040h**

Figure 14-4010. MAIN_PLL_MMR_CFG_PLL5_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12082. MAIN_PLL_MMR_CFG_PLL5_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12082. MAIN_PLL_MMR_CFG_PLL5_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.77 MAIN_PLL_MMR_CFG_PLL5_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL5_SS_SPREAD Register (Offset = 5044h) [reset = 10001h]

PLL_SS_SPREAD register for pll5

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Table 14-12083. Instance Table

Instance Name	Physical Address
PLL0	**0068 5044h**

Figure 14-4011. MAIN_PLL_MMR_CFG_PLL5_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12085. MAIN_PLL_MMR_CFG_PLL5_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.78 MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL Register (Offset = 5060h) [reset = 20000h]

PLL5_CAL_CTRL - PLL5 Calibration Control Register

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Table 14-12086. Instance Table

Instance Name	Physical Address
PLL0	**0068 5060h**

Figure 14-4012. MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12088. MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12088. MAIN_PLL_MMR_CFG_PLL5_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.79 MAIN_PLL_MMR_CFG_PLL5_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL5_CAL_STAT Register (Offset = 5064h) [reset = 0h]

PLL5_CAL_STAT - PLL5 Calibration Status Register

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Table 14-12089. Instance Table

Instance Name	Physical Address
PLL0	**0068 5064h**

Figure 14-4013. MAIN_PLL_MMR_CFG_PLL5_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12091. MAIN_PLL_MMR_CFG_PLL5_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.80 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL0 Register (Offset = 5080h) [reset = 0h]

HSDIV_CTRL0 register for pll5

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Table 14-12092. Instance Table

Instance Name	Physical Address
PLL0	**0068 5080h**

Figure 14-4014. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12094. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.81 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL1 Register (Offset = 5084h) [reset = 0h]

HSDIV_CTRL1 register for pll5

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Table 14-12095. Instance Table

Instance Name	Physical Address
PLL0	**0068 5084h**

Figure 14-4015. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12097. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.82 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL2 Register

1 MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL2 Register (Offset = 5088h) [reset = 0h]

HSDIV_CTRL2 register for pll5

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Table 14-12098. Instance Table

Instance Name	Physical Address
PLL0	**0068 5088h**

Figure 14-4016. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12100. MAIN_PLL_MMR_CFG_PLL5_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.83 MAIN_PLL_MMR_CFG_PLL7_PID Register

1 MAIN_PLL_MMR_CFG_PLL7_PID Register (Offset = 7000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12101. Instance Table

Instance Name	Physical Address
PLL0	**0068 7000h**

Figure 14-4017. MAIN_PLL_MMR_CFG_PLL7_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			

23	22	21	20	19	18	17	16
MODULE							
R							
180h							

15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12103. MAIN_PLL_MMR_CFG_PLL7_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.84 MAIN_PLL_MMR_CFG_PLL7_CFG Register

1 MAIN_PLL_MMR_CFG_PLL7_CFG Register (Offset = 7008h) [reset = 10801h]

pll MMR Configuration

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Table 14-12104. Instance Table

Instance Name	Physical Address
PLL0	**0068 7008h**

Figure 14-4018. MAIN_PLL_MMR_CFG_PLL7_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12106. MAIN_PLL_MMR_CFG_PLL7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12106. MAIN_PLL_MMR_CFG_PLL7_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.85 MAIN_PLL_MMR_CFG_PLL7_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL7_LOCKKEY0 Register (Offset = 7010h) [reset = 0h]

PLL7_LOCKKEY0 - PLL7 Lock Key 0 Register

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Table 14-12107. Instance Table

Instance Name	Physical Address
PLL0	**0068 7010h**

Figure 14-4019. MAIN_PLL_MMR_CFG_PLL7_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12109. MAIN_PLL_MMR_CFG_PLL7_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition7 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.86 MAIN_PLL_MMR_CFG_PLL7_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL7_LOCKKEY1 Register (Offset = 7014h) [reset = 0h]

PLL7_LOCKKEY1 - PLL7 Lock Key 1 RegisterAddr

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Table 14-12110. Instance Table

Instance Name	Physical Address
PLL0	**0068 7014h**

Figure 14-4020. MAIN_PLL_MMR_CFG_PLL7_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12112. MAIN_PLL_MMR_CFG_PLL7_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition7 registers Reset Source: srst_n

14.2.3.1.1.2.87 MAIN_PLL_MMR_CFG_PLL7_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL7_CTRL Register (Offset = 7020h) [reset = 80010011h]

PLL7_CTRL - PLL7 Control

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Table 14-12113. Instance Table

Instance Name	Physical Address
PLL0	**0068 7020h**

Figure 14-4021. MAIN_PLL_MMR_CFG_PLL7_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12115. MAIN_PLL_MMR_CFG_PLL7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12115. MAIN_PLL_MMR_CFG_PLL7_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.88 MAIN_PLL_MMR_CFG_PLL7_STAT Register

1 MAIN_PLL_MMR_CFG_PLL7_STAT Register (Offset = 7024h) [reset = 0h]

PLL7_STAT - PLL7 Status

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Table 14-12116. Instance Table

Instance Name	**Physical Address**
PLL0	**0068 7024h**

Figure 14-4022. MAIN_PLL_MMR_CFG_PLL7_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-12118. MAIN_PLL_MMR_CFG_PLL7_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.89 MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL0 Register (Offset = 7030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL7 Frequency Control 7 Register

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Table 14-12119. Instance Table

Instance Name	Physical Address
PLL0	**0068 7030h**

Figure 14-4023. MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-12121. MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.90 MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL1 Register (Offset = 7034h) [reset = 0h]

PLL7_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12122. Instance Table

Instance Name	Physical Address
PLL0	**0068 7034h**

Figure 14-4024. MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12124. MAIN_PLL_MMR_CFG_PLL7_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.91 MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL Register (Offset = 7038h) [reset = 1020001h]

PLL7_DIV_CTRL - PLL7 Output Clock Divider Register

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Table 14-12125. Instance Table

Instance Name	Physical Address
PLL0	**0068 7038h**

Figure 14-4025. MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12127. MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12127. MAIN_PLL_MMR_CFG_PLL7_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.92 MAIN_PLL_MMR_CFG_PLL7_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL7_SS_CTRL Register (Offset = 7040h) [reset = 80000000h]

PLL_SS_CTRL register for pll7

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Table 14-12128. Instance Table

Instance Name	Physical Address
PLL0	**0068 7040h**

Figure 14-4026. MAIN_PLL_MMR_CFG_PLL7_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12130. MAIN_PLL_MMR_CFG_PLL7_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12130. MAIN_PLL_MMR_CFG_PLL7_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.93 MAIN_PLL_MMR_CFG_PLL7_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL7_SS_SPREAD Register (Offset = 7044h) [reset = 10001h]

PLL_SS_SPREAD register for pll7

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Table 14-12131. Instance Table

Instance Name	Physical Address
PLL0	**0068 7044h**

Figure 14-4027. MAIN_PLL_MMR_CFG_PLL7_SS_SPREAD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MOD_DIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">SPREAD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1h</td></tr>
</table>

Table 14-12133. MAIN_PLL_MMR_CFG_PLL7_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.94 MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL Register (Offset = 7060h) [reset = 20000h]

PLL7_CAL_CTRL - PLL7 Calibration Control Register

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Table 14-12134. Instance Table

Instance Name	Physical Address
PLL0	**0068 7060h**

Figure 14-4028. MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-12136. MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12136. MAIN_PLL_MMR_CFG_PLL7_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.95 MAIN_PLL_MMR_CFG_PLL7_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL7_CAL_STAT Register (Offset = 7064h) [reset = 0h]

PLL7_CAL_STAT - PLL7 Calibration Status Register

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Table 14-12137. Instance Table

Instance Name	Physical Address
PLL0	**0068 7064h**

Figure 14-4029. MAIN_PLL_MMR_CFG_PLL7_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12139. MAIN_PLL_MMR_CFG_PLL7_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.96 MAIN_PLL_MMR_CFG_PLL7_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL7_HSDIV_CTRL0 Register (Offset = 7080h) [reset = 0h]

HSDIV_CTRL0 register for pll7

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Table 14-12140. Instance Table

Instance Name	Physical Address
PLL0	**0068 7080h**

Figure 14-4030. MAIN_PLL_MMR_CFG_PLL7_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12142. MAIN_PLL_MMR_CFG_PLL7_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.97 MAIN_PLL_MMR_CFG_PLL8_PID Register

1 MAIN_PLL_MMR_CFG_PLL8_PID Register (Offset = 8000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12143. Instance Table

Instance Name	Physical Address
PLL0	**0068 8000h**

Figure 14-4031. MAIN_PLL_MMR_CFG_PLL8_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12145. MAIN_PLL_MMR_CFG_PLL8_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.98 MAIN_PLL_MMR_CFG_PLL8_CFG Register

1 MAIN_PLL_MMR_CFG_PLL8_CFG Register (Offset = 8008h) [reset = 10801h]

pll MMR Configuration

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Table 14-12146. Instance Table

Instance Name	Physical Address
PLL0	**0068 8008h**

Figure 14-4032. MAIN_PLL_MMR_CFG_PLL8_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12148. MAIN_PLL_MMR_CFG_PLL8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12148. MAIN_PLL_MMR_CFG_PLL8_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.99 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register (Offset = 8010h) [reset = 0h]

PLL8_LOCKKEY0 - PLL8 Lock Key 0 Register

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Table 14-12149. Instance Table

Instance Name	Physical Address
PLL0	**0068 8010h**

Figure 14-4033. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12151. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition8 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.100 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register (Offset = 8014h) [reset = 0h]

PLL8_LOCKKEY1 - PLL8 Lock Key 1 RegisterAddr

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Table 14-12152. Instance Table

Instance Name	Physical Address
PLL0	**0068 8014h**

Figure 14-4034. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12154. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition8 registers Reset Source: srst_n

14.2.3.1.1.2.101 MAIN_PLL_MMR_CFG_PLL8_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL8_CTRL Register (Offset = 8020h) [reset = 80010011h]

PLL8_CTRL - PLL8 Control

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Table 14-12155. Instance Table

Instance Name	Physical Address
PLL0	**0068 8020h**

Figure 14-4035. MAIN_PLL_MMR_CFG_PLL8_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12157. MAIN_PLL_MMR_CFG_PLL8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12157. MAIN_PLL_MMR_CFG_PLL8_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.102 MAIN_PLL_MMR_CFG_PLL8_STAT Register

1 MAIN_PLL_MMR_CFG_PLL8_STAT Register (Offset = 8024h) [reset = 0h]

PLL8_STAT - PLL8 Status

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Table 14-12158. Instance Table

Instance Name	Physical Address
PLL0	**0068 8024h**

Figure 14-4036. MAIN_PLL_MMR_CFG_PLL8_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-12160. MAIN_PLL_MMR_CFG_PLL8_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.103 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register (Offset = 8030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL8 Frequency Control 8 Register

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Table 14-12161. Instance Table

Instance Name	Physical Address
PLL0	**0068 8030h**

Figure 14-4037. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-12163. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.104 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register (Offset = 8034h) [reset = 0h]

PLL8_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12164. Instance Table

Instance Name	Physical Address
PLL0	**0068 8034h**

Figure 14-4038. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12166. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.105 MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register (Offset = 8038h) [reset = 1020001h]

PLL8_DIV_CTRL - PLL8 Output Clock Divider Register

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Table 14-12167. Instance Table

Instance Name	Physical Address
PLL0	**0068 8038h**

Figure 14-4039. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12169. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12169. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.106 MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register (Offset = 8040h) [reset = 80000001h]

PLL_SS_CTRL register for pll8

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Table 14-12170. Instance Table

Instance Name	Physical Address
PLL0	**0068 8040h**

Figure 14-4040. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>1h</td></tr>
</table>

Table 14-12172. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12172. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	1h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.107 MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register (Offset = 8044h) [reset = 10001h]

PLL_SS_SPREAD register for pll8

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Table 14-12173. Instance Table

Instance Name	Physical Address
PLL0	**0068 8044h**

Figure 14-4041. MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12175. MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.108 MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register (Offset = 8060h) [reset = 20000h]

PLL8_CAL_CTRL - PLL8 Calibration Control Register

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Table 14-12176. Instance Table

Instance Name	Physical Address
PLL0	**0068 8060h**

Figure 14-4042. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W							
0h							

Table 14-12178. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12178. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.109 MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register (Offset = 8064h) [reset = 0h]

PLL8_CAL_STAT - PLL8 Calibration Status Register

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Table 14-12179. Instance Table

Instance Name	Physical Address
PLL0	**0068 8064h**

Figure 14-4043. MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12181. MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.110 MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register (Offset = 8080h) [reset = 0h]

HSDIV_CTRL0 register for pll8

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Table 14-12182. Instance Table

Instance Name	**Physical Address**
PLL0	**0068 8080h**

Figure 14-4044. MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12184. MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.111 MAIN_PLL_MMR_CFG_PLL12_PID Register

1 MAIN_PLL_MMR_CFG_PLL12_PID Register (Offset = C000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12185. Instance Table

Instance Name	Physical Address
PLL0	**0068 C000h**

Figure 14-4045. MAIN_PLL_MMR_CFG_PLL12_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12187. MAIN_PLL_MMR_CFG_PLL12_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.112 MAIN_PLL_MMR_CFG_PLL12_CFG Register

1 MAIN_PLL_MMR_CFG_PLL12_CFG Register (Offset = C008h) [reset = 10801h]

pll MMR Configuration

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Table 14-12188. Instance Table

Instance Name	Physical Address
PLL0	**0068 C008h**

Figure 14-4046. MAIN_PLL_MMR_CFG_PLL12_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-12190. MAIN_PLL_MMR_CFG_PLL12_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12190. MAIN_PLL_MMR_CFG_PLL12_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.113 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register (Offset = C010h) [reset = 0h]

PLL12_LOCKKEY0 - PLL12 Lock Key 0 Register

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Table 14-12191. Instance Table

Instance Name	Physical Address
PLL0	**0068 C010h**

Figure 14-4047. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12193. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition12 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.114 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register (Offset = C014h) [reset = 0h]

PLL12_LOCKKEY1 - PLL12 Lock Key 1 RegisterAddr

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Table 14-12194. Instance Table

Instance Name	Physical Address
PLL0	**0068 C014h**

Figure 14-4048. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12196. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition12 registers Reset Source: srst_n

14.2.3.1.1.2.115 MAIN_PLL_MMR_CFG_PLL12_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL12_CTRL Register (Offset = C020h) [reset = 80010011h]

PLL12_CTRL - PLL12 Control

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Table 14-12197. Instance Table

Instance Name	Physical Address
PLL0	**0068 C020h**

Figure 14-4049. MAIN_PLL_MMR_CFG_PLL12_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12199. MAIN_PLL_MMR_CFG_PLL12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12199. MAIN_PLL_MMR_CFG_PLL12_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.116 MAIN_PLL_MMR_CFG_PLL12_STAT Register

1 MAIN_PLL_MMR_CFG_PLL12_STAT Register (Offset = C024h) [reset = 0h]

PLL12_STAT - PLL12 Status

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Table 14-12200. Instance Table

Instance Name	Physical Address
PLL0	**0068 C024h**

Figure 14-4050. MAIN_PLL_MMR_CFG_PLL12_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-12202. MAIN_PLL_MMR_CFG_PLL12_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.117 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register (Offset = C030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL12 Frequency Control 12 Register

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Table 14-12203. Instance Table

Instance Name	Physical Address
PLL0	**0068 C030h**

Figure 14-4051. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-12205. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.118 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register (Offset = C034h) [reset = 0h]

PLL12_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12206. Instance Table

Instance Name	Physical Address
PLL0	**0068 C034h**

Figure 14-4052. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12208. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.119 MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register (Offset = C038h) [reset = 1020001h]

PLL12_DIV_CTRL - PLL12 Output Clock Divider Register

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Table 14-12209. Instance Table

Instance Name	Physical Address
PLL0	**0068 C038h**

Figure 14-4053. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">REF_DIV</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-12211. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12211. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.120 MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register (Offset = C040h) [reset = 80000000h]

PLL_SS_CTRL register for pll12

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Table 14-12212. Instance Table

Instance Name	Physical Address
PLL0	**0068 C040h**

Figure 14-4054. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12214. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12214. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.121 MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register (Offset = C044h) [reset = 10001h]

PLL_SS_SPREAD register for pll12

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Table 14-12215. Instance Table

Instance Name	Physical Address
PLL0	**0068 C044h**

Figure 14-4055. MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12217. MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.122 MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register (Offset = C060h) [reset = 20000h]

PLL12_CAL_CTRL - PLL12 Calibration Control Register

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Table 14-12218. Instance Table

Instance Name	Physical Address
PLL0	**0068 C060h**

Figure 14-4056. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-12220. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12220. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.123 MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register (Offset = C064h) [reset = 0h]

PLL12_CAL_STAT - PLL12 Calibration Status Register

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Table 14-12221. Instance Table

Instance Name	Physical Address
PLL0	**0068 C064h**

Figure 14-4057. MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12223. MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.124 MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register (Offset = C080h) [reset = 0h]

HSDIV_CTRL0 register for pll12

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Table 14-12224. Instance Table

Instance Name	Physical Address
PLL0	**0068 C080h**

Figure 14-4058. MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12226. MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.125 MAIN_PLL_MMR_CFG_PLL15_PID Register

1 MAIN_PLL_MMR_CFG_PLL15_PID Register (Offset = F000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12227. Instance Table

Instance Name	Physical Address
PLL0	**0068 F000h**

Figure 14-4059. MAIN_PLL_MMR_CFG_PLL15_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12229. MAIN_PLL_MMR_CFG_PLL15_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.126 MAIN_PLL_MMR_CFG_PLL15_CFG Register

1 MAIN_PLL_MMR_CFG_PLL15_CFG Register (Offset = F008h) [reset = 70801h]

pll MMR Configuration

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Table 14-12230. Instance Table

Instance Name	Physical Address
PLL0	**0068 F008h**

Figure 14-4060. MAIN_PLL_MMR_CFG_PLL15_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
7h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
7h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12232. MAIN_PLL_MMR_CFG_PLL15_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12232. MAIN_PLL_MMR_CFG_PLL15_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.127 MAIN_PLL_MMR_CFG_PLL15_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL15_LOCKKEY0 Register (Offset = F010h) [reset = 0h]

PLL15_LOCKKEY0 - PLL15 Lock Key 0 Register

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Table 14-12233. Instance Table

Instance Name	Physical Address
PLL0	**0068 F010h**

Figure 14-4061. MAIN_PLL_MMR_CFG_PLL15_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12235. MAIN_PLL_MMR_CFG_PLL15_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition15 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.128 MAIN_PLL_MMR_CFG_PLL15_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL15_LOCKKEY1 Register (Offset = F014h) [reset = 0h]

PLL15_LOCKKEY1 - PLL15 Lock Key 1 RegisterAddr

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Table 14-12236. Instance Table

Instance Name	Physical Address
PLL0	**0068 F014h**

Figure 14-4062. MAIN_PLL_MMR_CFG_PLL15_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12238. MAIN_PLL_MMR_CFG_PLL15_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition15 registers Reset Source: srst_n

14.2.3.1.1.2.129 MAIN_PLL_MMR_CFG_PLL15_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL15_CTRL Register (Offset = F020h) [reset = 80010011h]

PLL15_CTRL - PLL15 Control

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Table 14-12239. Instance Table

Instance Name	Physical Address
PLL0	**0068 F020h**

Figure 14-4063. MAIN_PLL_MMR_CFG_PLL15_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12241. MAIN_PLL_MMR_CFG_PLL15_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12241. MAIN_PLL_MMR_CFG_PLL15_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.130 MAIN_PLL_MMR_CFG_PLL15_STAT Register

1 MAIN_PLL_MMR_CFG_PLL15_STAT Register (Offset = F024h) [reset = 0h]

PLL15_STAT - PLL15 Status

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Table 14-12242. Instance Table

Instance Name	Physical Address
PLL0	**0068 F024h**

Figure 14-4064. MAIN_PLL_MMR_CFG_PLL15_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-12244. MAIN_PLL_MMR_CFG_PLL15_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.131 MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL0 Register (Offset = F030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL15 Frequency Control 15 Register

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Table 14-12245. Instance Table

Instance Name	Physical Address
PLL0	**0068 F030h**

Figure 14-4065. MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-12247. MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.132 MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL1 Register (Offset = F034h) [reset = 0h]

PLL15_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12248. Instance Table

Instance Name	Physical Address
PLL0	**0068 F034h**

Figure 14-4066. MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12250. MAIN_PLL_MMR_CFG_PLL15_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.133 MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL Register (Offset = F038h) [reset = 1020001h]

PLL15_DIV_CTRL - PLL15 Output Clock Divider Register

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Table 14-12251. Instance Table

Instance Name	Physical Address
PLL0	**0068 F038h**

Figure 14-4067. MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12253. MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12253. MAIN_PLL_MMR_CFG_PLL15_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.134 MAIN_PLL_MMR_CFG_PLL15_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL15_SS_CTRL Register (Offset = F040h) [reset = 80000000h]

PLL_SS_CTRL register for pll15

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Table 14-12254. Instance Table

Instance Name	Physical Address
PLL0	**0068 F040h**

Figure 14-4068. MAIN_PLL_MMR_CFG_PLL15_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12256. MAIN_PLL_MMR_CFG_PLL15_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12256. MAIN_PLL_MMR_CFG_PLL15_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.135 MAIN_PLL_MMR_CFG_PLL15_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL15_SS_SPREAD Register (Offset = F044h) [reset = 10001h]

PLL_SS_SPREAD register for pll15

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Table 14-12257. Instance Table

Instance Name	Physical Address
PLL0	**0068 F044h**

Figure 14-4069. MAIN_PLL_MMR_CFG_PLL15_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12259. MAIN_PLL_MMR_CFG_PLL15_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.136 MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL Register (Offset = F060h) [reset = 20000h]

PLL15_CAL_CTRL - PLL15 Calibration Control Register

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Table 14-12260. Instance Table

Instance Name	Physical Address
PLL0	**0068 F060h**

Figure 14-4070. MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12262. MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12262. MAIN_PLL_MMR_CFG_PLL15_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.137 MAIN_PLL_MMR_CFG_PLL15_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL15_CAL_STAT Register (Offset = F064h) [reset = 0h]

PLL15_CAL_STAT - PLL15 Calibration Status Register

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Table 14-12263. Instance Table

Instance Name	Physical Address
PLL0	**0068 F064h**

Figure 14-4071. MAIN_PLL_MMR_CFG_PLL15_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12265. MAIN_PLL_MMR_CFG_PLL15_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.138 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL0 Register (Offset = F080h) [reset = 8000h]

HSDIV_CTRL0 register for pll15

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Table 14-12266. Instance Table

Instance Name	Physical Address
PLL0	**0068 F080h**

Figure 14-4072. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12268. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	1h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.139 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL1 Register (Offset = F084h) [reset = 0h]

HSDIV_CTRL1 register for pll15

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Table 14-12269. Instance Table

Instance Name	Physical Address
PLL0	**0068 F084h**

Figure 14-4073. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12271. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.140 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL2 Register

1 MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL2 Register (Offset = F088h) [reset = 8000h]

HSDIV_CTRL2 register for pll15

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Table 14-12272. Instance Table

Instance Name	Physical Address
PLL0	**0068 F088h**

Figure 14-4074. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12274. MAIN_PLL_MMR_CFG_PLL15_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	1h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.141 MAIN_PLL_MMR_CFG_PLL17_PID Register

1 MAIN_PLL_MMR_CFG_PLL17_PID Register (Offset = 11000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12275. Instance Table

Instance Name	Physical Address
PLL0	**0069 1000h**

Figure 14-4075. MAIN_PLL_MMR_CFG_PLL17_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">MISC</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-12277. MAIN_PLL_MMR_CFG_PLL17_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.142 MAIN_PLL_MMR_CFG_PLL17_CFG Register

1 MAIN_PLL_MMR_CFG_PLL17_CFG Register (Offset = 11008h) [reset = 10801h]

pll MMR Configuration

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Table 14-12278. Instance Table

Instance Name	Physical Address
PLL0	**0069 1008h**

Figure 14-4076. MAIN_PLL_MMR_CFG_PLL17_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12280. MAIN_PLL_MMR_CFG_PLL17_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12280. MAIN_PLL_MMR_CFG_PLL17_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.143 MAIN_PLL_MMR_CFG_PLL17_LOCKKEY0 Register

1 MAIN_PLL_MMR_CFG_PLL17_LOCKKEY0 Register (Offset = 11010h) [reset = 0h]

PLL17_LOCKKEY0 - PLL17 Lock Key 0 Register

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Table 14-12281. Instance Table

Instance Name	Physical Address
PLL0	**0069 1010h**

Figure 14-4077. MAIN_PLL_MMR_CFG_PLL17_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12283. MAIN_PLL_MMR_CFG_PLL17_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition17 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.2.144 MAIN_PLL_MMR_CFG_PLL17_LOCKKEY1 Register

1 MAIN_PLL_MMR_CFG_PLL17_LOCKKEY1 Register (Offset = 11014h) [reset = 0h]

PLL17_LOCKKEY1 - PLL17 Lock Key 1 RegisterAddr

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Table 14-12284. Instance Table

Instance Name	Physical Address
PLL0	**0069 1014h**

Figure 14-4078. MAIN_PLL_MMR_CFG_PLL17_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12286. MAIN_PLL_MMR_CFG_PLL17_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition17 registers Reset Source: srst_n

14.2.3.1.1.2.145 MAIN_PLL_MMR_CFG_PLL17_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL17_CTRL Register (Offset = 11020h) [reset = 80010011h]

PLL17_CTRL - PLL17 Control

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Table 14-12287. Instance Table

Instance Name	Physical Address
PLL0	**0069 1020h**

Figure 14-4079. MAIN_PLL_MMR_CFG_PLL17_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12289. MAIN_PLL_MMR_CFG_PLL17_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12289. MAIN_PLL_MMR_CFG_PLL17_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.146 MAIN_PLL_MMR_CFG_PLL17_STAT Register

1 MAIN_PLL_MMR_CFG_PLL17_STAT Register (Offset = 11024h) [reset = 0h]

PLL17_STAT - PLL17 Status

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Table 14-12290. Instance Table

Instance Name	Physical Address
PLL0	**0069 1024h**

Figure 14-4080. MAIN_PLL_MMR_CFG_PLL17_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-12292. MAIN_PLL_MMR_CFG_PLL17_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.147 MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL0 Register (Offset = 11030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL17 Frequency Control 17 Register

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Table 14-12293. Instance Table

Instance Name	Physical Address
PLL0	**0069 1030h**

Figure 14-4081. MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-12295. MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.148 MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL1 Register

1 MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL1 Register (Offset = 11034h) [reset = 0h]

PLL17_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12296. Instance Table

Instance Name	Physical Address
PLL0	**0069 1034h**

Figure 14-4082. MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12298. MAIN_PLL_MMR_CFG_PLL17_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.149 MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL Register (Offset = 11038h) [reset = 1020001h]

PLL17_DIV_CTRL - PLL17 Output Clock Divider Register

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Table 14-12299. Instance Table

Instance Name	Physical Address
PLL0	**0069 1038h**

Figure 14-4083. MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12301. MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12301. MAIN_PLL_MMR_CFG_PLL17_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.150 MAIN_PLL_MMR_CFG_PLL17_SS_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL17_SS_CTRL Register (Offset = 11040h) [reset = 80000000h]

PLL_SS_CTRL register for pll17

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Table 14-12302. Instance Table

Instance Name	Physical Address
PLL0	**0069 1040h**

Figure 14-4084. MAIN_PLL_MMR_CFG_PLL17_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12304. MAIN_PLL_MMR_CFG_PLL17_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12304. MAIN_PLL_MMR_CFG_PLL17_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.151 MAIN_PLL_MMR_CFG_PLL17_SS_SPREAD Register

1 MAIN_PLL_MMR_CFG_PLL17_SS_SPREAD Register (Offset = 11044h) [reset = 10001h]

PLL_SS_SPREAD register for pll17

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Table 14-12305. Instance Table

Instance Name	**Physical Address**
PLL0	**0069 1044h**

Figure 14-4085. MAIN_PLL_MMR_CFG_PLL17_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12307. MAIN_PLL_MMR_CFG_PLL17_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.152 MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL Register

1 MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL Register (Offset = 11060h) [reset = 20000h]

PLL17_CAL_CTRL - PLL17 Calibration Control Register

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Table 14-12308. Instance Table

Instance Name	Physical Address
PLL0	**0069 1060h**

Figure 14-4086. MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-12310. MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12310. MAIN_PLL_MMR_CFG_PLL17_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.153 MAIN_PLL_MMR_CFG_PLL17_CAL_STAT Register

1 MAIN_PLL_MMR_CFG_PLL17_CAL_STAT Register (Offset = 11064h) [reset = 0h]

PLL17_CAL_STAT - PLL17 Calibration Status Register

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Table 14-12311. Instance Table

Instance Name	Physical Address
PLL0	**0069 1064h**

Figure 14-4087. MAIN_PLL_MMR_CFG_PLL17_CAL_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LOCK_CNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CAL_OUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_OUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12313. MAIN_PLL_MMR_CFG_PLL17_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.2.154 MAIN_PLL_MMR_CFG_PLL17_HSDIV_CTRL0 Register

1 MAIN_PLL_MMR_CFG_PLL17_HSDIV_CTRL0 Register (Offset = 11080h) [reset = 0h]

HSDIV_CTRL0 register for pll17

Return to Summary Table

Table 14-12314. Instance Table

Instance Name	Physical Address
PLL0	**0069 1080h**

Figure 14-4088. MAIN_PLL_MMR_CFG_PLL17_HSDIV_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12316. MAIN_PLL_MMR_CFG_PLL17_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2 MCU_PLL_MMR_CFG Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.2.1 mcu_pll_mmr

mcu_pll_mmr

14.2.3.2.1.1 mcu_pll_mmr Summaries

mcu_pll_mmr Summaries

Table 14-12317. MCU_PLL_MMR_CFG Registers, Base Address=0404 0000h, Length=4096

Offset	Length	Register Name	WKUP_PLL0 Physical Address
0h	32	MCU_PLL_MMR_CFG_PLL0_PID	0404 0000h
8h	32	MCU_PLL_MMR_CFG_PLL0_CFG	0404 0008h
10h	32	MCU_PLL_MMR_CFG_PLL0_LOCKKEY0	0404 0010h
14h	32	MCU_PLL_MMR_CFG_PLL0_LOCKKEY1	0404 0014h
20h	32	MCU_PLL_MMR_CFG_PLL0_CTRL	0404 0020h
24h	32	MCU_PLL_MMR_CFG_PLL0_STAT	0404 0024h
30h	32	MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0	0404 0030h
34h	32	MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1	0404 0034h
38h	32	MCU_PLL_MMR_CFG_PLL0_DIV_CTRL	0404 0038h
40h	32	MCU_PLL_MMR_CFG_PLL0_SS_CTRL	0404 0040h
44h	32	MCU_PLL_MMR_CFG_PLL0_SS_SPREAD	0404 0044h
60h	32	MCU_PLL_MMR_CFG_PLL0_CAL_CTRL	0404 0060h
64h	32	MCU_PLL_MMR_CFG_PLL0_CAL_STAT	0404 0064h
80h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0	0404 0080h
84h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1	0404 0084h
88h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2	0404 0088h
8Ch	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3	0404 008Ch
90h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4	0404 0090h
94h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL5	0404 0094h
98h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL6	0404 0098h

14.2.3.2.1.2 mcu_pll_mmr Registers

mcu_pll_mmr Registers

14.2.3.2.1.2.1 MCU_PLL_MMR_CFG_PLL0_PID Register

1 MCU_PLL_MMR_CFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-12318. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0000h**

Figure 14-4089. MCU_PLL_MMR_CFG_PLL0_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-12320. MCU_PLL_MMR_CFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.2 MCU_PLL_MMR_CFG_PLL0_CFG Register

1 MCU_PLL_MMR_CFG_PLL0_CFG Register (Offset = 8h) [reset = 7F0801h]

pll MMR Configuration

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Table 14-12321. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0008h**

Figure 14-4090. MCU_PLL_MMR_CFG_PLL0_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
7Fh							

23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
7Fh							

15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h

7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-12323. MCU_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12323. MCU_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.3 MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register

1 MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

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Table 14-12324. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0010h**

Figure 14-4091. MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-12326. MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.2.1.2.4 MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register

1 MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

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Table 14-12327. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0014h**

Figure 14-4092. MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-12329. MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.2.1.2.5 MCU_PLL_MMR_CFG_PLL0_CTRL Register

1 MCU_PLL_MMR_CFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

PLL0_CTRL - PLL0 Control

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Table 14-12330. Instance Table

Instance Name	**Physical Address**
WKUP_PLL0	**0404 0020h**

Figure 14-4093. MCU_PLL_MMR_CFG_PLL0_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-12332. MCU_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-12332. MCU_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.6 MCU_PLL_MMR_CFG_PLL0_STAT Register

1 MCU_PLL_MMR_CFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

PLL0_STAT - PLL0 Status

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Table 14-12333. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0024h**

Figure 14-4094. MCU_PLL_MMR_CFG_PLL0_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12335. MCU_PLL_MMR_CFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.7 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register

1 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

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Table 14-12336. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0030h**

Figure 14-4095. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-12338. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.8 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register

1 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-12339. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0034h**

Figure 14-4096. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-12341. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.9 MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register

1 MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

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Table 14-12342. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0038h**

Figure 14-4097. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-12344. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-12344. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.10 MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register

1 MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

PLL_SS_CTRL register for pll0

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Table 14-12345. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0040h**

Figure 14-4098. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-12347. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-12347. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.11 MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register

1 MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

PLL_SS_SPREAD register for pll0

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Table 14-12348. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0044h**

Figure 14-4099. MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-12350. MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.12 MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register

1 MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

PLL0_CAL_CTRL - PLL0 Calibration Control Register

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Table 14-12351. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0060h**

Figure 14-4100. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W							
0h							

Table 14-12353. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-12353. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.13 MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register

1 MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

PLL0_CAL_STAT - PLL0 Calibration Status Register

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Table 14-12354. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0064h**

Figure 14-4101. MCU_PLL_MMR_CFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-12356. MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.14 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

HSDIV_CTRL0 register for pll0

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Table 14-12357. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0080h**

Figure 14-4102. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12359. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.15 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

HSDIV_CTRL1 register for pll0

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Table 14-12360. Instance Table

Instance Name	**Physical Address**
WKUP_PLL0	**0404 0084h**

Figure 14-4103. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12362. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.16 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

HSDIV_CTRL2 register for pll0

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Table 14-12363. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0088h**

Figure 14-4104. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12365. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.17 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

HSDIV_CTRL3 register for pll0

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Table 14-12366. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 008Ch**

Figure 14-4105. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12368. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.18 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

HSDIV_CTRL4 register for pll0

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Table 14-12369. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0090h**

Figure 14-4106. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12371. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.19 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = 0h]

HSDIV_CTRL5 register for pll0

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Table 14-12372. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0094h**

Figure 14-4107. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12374. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.2.20 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register

1 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = 0h]

HSDIV_CTRL6 register for pll0

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Table 14-12375. Instance Table

Instance Name	Physical Address
WKUP_PLL0	**0404 0098h**

Figure 14-4108. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-12377. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.3 PLLCTRL Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.3.1 PLLCTRL0 Registers

Table 14-8271 lists the PLLCTRL0 registers. All register offset addresses not listed in Table 14-8271 should be considered as reserved locations and the register contents should not be modified.

Table 14-12378. PLLCTRL0 Instances

Instance	Base Address
PLLCTRL0	0041 0000h
MCU_PLLCTRL0	4020 0000h

Table 14-12379. PLLCTRL0 Registers

Offset	Acronym	Register Name	PLLCTRL0 Physical Address	MCU_PLLCTRL0 Physical Address
0h	PID	Peripheral identification register	0041 0000h	4020 0000h
100h	PLLCTL	PLL control register	0041 0100h	4020 0100h
118h	PLLDIV1	PLL controller divider1 control register	0041 0118h	4020 0118h
11Ch	PLLDIV2	PLL controller divider2 control register	0041 011Ch	4020 011Ch
138h	PLLCMD	PLL Controller command register	0041 0138h	4020 0138h
13Ch	PLLSTAT	PLL Controller status register	0041 013Ch	4020 013Ch
140h	ALNCTL	PLL Controller clock align control register	0041 0140h	4020 0140h
144h	DCHANGE	PLLDIV ratio change register	0041 0144h	4020 0144h

1 PID Register (Offset = 0h) [reset = 44815C00h]

PID is shown in Figure 14-4109 and described in Table 14-8273.

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Peripheral identification register

Table 14-12380. PID Instances

Instance	Physical Address
PLLCTRL0	0041 0000h
MCU_PLLCTRL0	4020 0000h

Figure 14-4109. PID Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">FUNC</td></tr>
<tr><td colspan="2">R-1h</td><td colspan="2">R-0h</td><td colspan="12">R-481h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="5">R-Bh</td><td colspan="3">R-4h</td><td colspan="2">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12382. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Peripheral identification register scheme
29-28	BU	R	0h	Business Unit
27-16	FUNC	R	481h	Module ID
15-11	RTL	R	Bh	RTL revision. Will vary depending on release
10-8	MAJOR	R	4h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

2 PLLCTL Register (Offset = 100h) [reset = X]

PLLCTL is shown in Figure 14-4110 and described in Table 14-8275.

Return to the Summary Table.

PLL control register

Table 14-12383. PLLCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0100h
MCU_PLLCTRL0	4020 0100h

Figure 14-4110. PLLCTL Register

31	30	29	28	27	26	25	24
RSVD2							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD2						EXCLKSRC	CLKMODE
R/W-0h						R/W-0h	R/W-X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLLSELB	RSVD1	PLLENSRC	PLLDIS	PLLRST	RSVD	PLLPWRDN	PLLEN
R/W-0h	R/W-0h	R/W-1h	R/W-X	R/W-X	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12385. PLLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RSVD2	R/W	0h	Reserved
9	EXCLKSRC	R/W	0h	Selects between using bypass clock or an external clock source. 0 = bypass clock 1 = external clock source
8	CLKMODE	R/W	X	Reference Clock Selection. 1 = clkin_pi is the reference clock 0 = oscin_pi is the reference clock This bit is only applicable when d_clkmodesrc_pi = 1. It is otherwise don't care.
7	PLLSELB	R/W	0h	Selects PLL A versus PLL B. 1 = PLL B is selected. PLL A is put in power down (pll_a_pwrdn_po = 1) 0 = PLL A is selected. PLL B is put in power down. (pll_b_pwrdn_po = 1)
6	RSVD1	R/W	0h	Reserved
5	PLLENSRC	R/W	1h	PLLEN Mux Control Source 1 = PLLEN Mux is controlled by input pllen_pi. PLLCTL.PLLEN is don't care 0 = PLLEN Mux is controlled by PLLCTL.PLLEN. pllen_pi is don't care

Table 14-12385. PLLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLLDIS	R/W	X	Asserts DISABLE to PLL if Supported 1 = PLL Controller output pll_disable_po = 1. 0 = PLL Controller output pll_disable_po = 0. Chip team must pay attention to the disable signal polarity of the PLL they use. Some PLLs may require PLLDIS = 1 to disable PLL, some PLLs require PLLDIS = 0 to disable PLL. Note that PLL Controller only supports one pll_disable_po output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
3	PLLRST	R/W	X	Asserts RESET to PLL if Supported. Controls output pll_reset_po. 1 = PLL Controller output pll_reset_po = 1. 0 = PLL Controller output pll_reset_po = 0. Chip team must pay attention to the reset signal polarity of the PLL they use. Some PLLs require PLLRST = 1 to reset the PLL. Some PLLs require PLLRST = 0 to reset the PLL. Note that PLL Controller only supports one pll_reset_po output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
2	RSVD	R/W	0h	Reserved
1	PLLPWRDN	R/W	1h	Selects PLL Power Down for the PLL selected by PLLSELB. The PLL not selected by PLLSELB is NOT controlled by PLLPWRDN bit. The not-selected PLL will stay in power down regardless of PLLPWRDN value. 0 = Selected PLL Operational. If PLLSELB = 0 (PLLA selected), PLL controller output pll_a_pwrdn_po is deasserted low. If PLLSELB = 1 (PLLB selected), PLL controller output pll_b_pwrdn_po is deasserted low. 1 = Selected PLL Placed In Power Down State. If PLLSELB = 0 (PLLA selected), PLL controller outputs pll_a_pwrdn_po is asserted high. If PLLSELB = 1 (PLLB selected), pll_b_pwrdn_po is asserted
0	PLLEN	R/W	0h	PLL Mode Enable This bit controls the multiplexer before the SYSCLK dividers D1 to Dn. 0 = Bypass Mode PreDiv, PLL, and PostDiv are bypassed. SYSCLK divided down directly from input reference clock refclk. 1 = PLL Mode PLL is used. SYSCLK divided down from PostDiv output

3 PLLDIV1 Register (Offset = 118h) [reset = X]

PLLDIV1 is shown in Figure 14-4111 and described in Table 14-8277.

Return to the Summary Table.

PLL controller divider1 control register

Table 14-12386. PLLDIV1 Instances

Instance	Physical Address
PLLCTRL0	0041 0118h
MCU_PLLCTRL0	4020 0118h

Figure 14-4111. PLLDIV1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>DN_EN</td><td>HALF_RATIO</td><td colspan="6">RSVD</td></tr>
<tr><td>R/W-X</td><td>R/W-0h</td><td colspan="6">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATIO</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12388. PLLDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN_EN	R/W	X	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled
14	HALF_RATIO	R/W	0h	Ratio is in half steps. Example 1: if RATIO = 00000 and HALFRATIO = 1 the divider will be /1.5. Example 2: RATIO = 10111 and HALFRATIO = 1 divider will be /24.5. Example 3: if RATIO = 00011 and HALFRATIO = 0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. Note: To enable half step ratio dividers user must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidentally wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

Table 14-12388. PLLDIV1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000 = /1 00001 = /2 00010 = /3 00011 = /4 00100 = /5 00101 = /6 00110 = /7 00111 = /8 01000 = /9 01001 = /10 01010 = /11 01011 = /12 01100 = /13 01101 = /14 01110 = /15 01111 = /16 10000 = /17 10001 = /18 10010 = /19 10011 = /20 10100 = /21 10101 = /22 10110 = /23 10111 = /24 11000 = /25 11001 = /26 11010 = /27 11011 = /28 11100 = /29 11101 = /30 11110 = /31 11111 = /32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

4 PLLDIV2 Register (Offset = 11Ch) [reset = X]

PLLDIV2 is shown in Figure 14-4112 and described in Table 14-8279.

Return to the Summary Table.

PLL controller divider2 control register

Table 14-12389. PLLDIV2 Instances

Instance	Physical Address
PLLCTRL0	0041 011Ch
MCU_PLLCTRL0	4020 011Ch

Figure 14-4112. PLLDIV2 Register

31	30	29	28	27	26	25	24
RSVD1							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD1							
R/W-0h							
15	14	13	12	11	10	9	8
DN_EN	HALF_RATIO	RSVD					
R/W-X	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
RATIO							
R/W-X							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12391. PLLDIV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN_EN	R/W	X	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled
14	HALF_RATIO	R/W	0h	Ratio is in half steps. Example 1: if RATIO = 00000 and HALFRATIO = 1 the divider will be /1.5. Example 2: RATIO = 10111 and HALFRATIO = 1 divider will be /24.5. Example 3: if RATIO = 00011 and HALFRATIO = 0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. Note: To enable half step ratio dividers user must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidentally wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

Table 14-12391. PLLDIV2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000 = /1 00001 = /2 00010 = /3 00011 = /4 00100 = /5 00101 = 6 00110 = /7 00111 = /8 01000 = /9 01001 = /10 01010 = /11 01011 = /12 01100 = 13 01101 = /14 01110 = /15 01111 = /16 10000 = /17 10001 = /18 10010 = /19 10011 = /20 10100 = /21 10101 = /22 10110 = /23 10111 = /24 11000 = /25 11001 = /26 11010 = /27 11011 = /28 11100 = /29 11101 = /30 11110 = /31 11111 = /32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

5 PLLCMD Register (Offset = 138h) [reset = 0h]

PLLCMD is shown in Figure 14-4113 and described in Table 14-8281.

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PLL Controller command register

Table 14-12392. PLLCMD Instances

Instance	Physical Address
PLLCTRL0	0041 0138h
MCU_PLLCTRL0	4020 0138h

Figure 14-4113. PLLCMD Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RSVD</td><td>OSCPWRDN</td><td>GOSET</td></tr>
<tr><td colspan="6">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12394. PLLCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RSVD	R/W	0h	Reserved
1	OSCPWRDN	R/W	0h	Oscillator Power Down Command 1: A write of 1 (doesn't need to be a transition from 0 to 1) to this bit initiates oscillator power down command. 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. Once written a 1, the bit remains a 1 unless if user writes a 0 to it. Do not read this bit for status of oscillator power down. In the case when CLKMODE = 1 (CLKIN mode), write to OSCPWRDN bit still occurs, but no oscillator power down command is actually sent because osc is already in power down. Read from this bit returns the value written.

Table 14-12394. PLLCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GOSET	R/W	0h	GO bit for SYSCLKx phase alignment. GOSET = 1: A write of 1 to this bit signifies that the new divide ratios in PLLDIV [1:n] are taken into account at the nearest possible rising edge to phase align the clocks. The actual SYSCLKx to be aligned are selected in register ALNCTL. When divide-ratio change and clock alignment are completed, GOSET remains 1. Subsequent write of 1 to this register (even though the field was already a 1) causes the command for divide-ratio change and clock alignment. GOSET = 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. When writing consecutively to this field, the user must poll the GOSTAT between accesses to see if previous command for clock alignment and divide-ratio change has completed. Otherwise operation is undefined. Do not read GOSET in this command register for status.

6 PLLSTAT Register (Offset = 13Ch) [reset = X]

PLLSTAT is shown in Figure 14-4114 and described in Table 14-8283.

Return to the Summary Table.

PLL Controller status register

Table 14-12395. PLLSTAT Instances

Instance	Physical Address
PLLCTRL0	0041 013Ch
MCU_PLLCTRL0	4020 013Ch

Figure 14-4114. PLLSTAT Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD					STABLE	LOCK	GOSET
R/W-0h					R-X	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-12397. PLLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RSVD	R/W	0h	Reserved
2	STABLE	R	X	OSCIN Stable This bit shows the status of the rstclk_cnt_done_po signal. It indicates if the rstclk counter has finished counting, implying that the OSCIN/CLKIN is stable. The d_rstclk_cnt_pi must be set properly to allow rstclk counter to count sufficient amount of time for clock sources to become stable. 0 = rstclk counter not done counting, implying OSCIN/CLKIN input may not yet be stable. 1 = OSCIN/CLKIN is assumed to be stable. This bit is set to 1 if any one of the three cases is true: - rstclk counter has finished counting d_rstclk_cnt_pi number of rstclk cycles. - rstclk counter is parametrized out and does not exist, in which case OSCIN/CLKIN is assumed to be stable when por_pi_n is de-asserted.

Table 14-12397. PLLSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOCK	R	0h	PLL Core STATUS This bit returns the lock status of the selected PLL core (if supported by PLL core). For example, if PLLSELB = 0 (PLLA selected), it reflects the status of pll_a_lock_i. If PLLSELB-1 (PLLB selected), it reflects the status of pll_b_lock_i. 0 = PLL core not locked. The corresponding PLL Controller output pll_[x]_lock_out = 0. (where [x] is a or b depending on PLLSELB). 1 = PLL core locked. The corresponding PLL Controller output pll_[x]_lock_out = 1. (where [x] is a or b depending on PLLSELB). Note that not all PLL Core supports the lock signal. Check the PLL used to see if it has a functional lock output. Therefore this bit may not need to be documented to users.
0	GOSET	R	0h	Reflects the status of GO transition. Read from this register returns the status of the GO operation. Writes to the register are ignored. GOSTAT = 1: This bit goes to 1 as soon as GOSET in PLLCMD is written to. It remains a 1 when GO operation (divide-ratio change and clock alignment) is in progress. This bit automatically clears to 0 when GO operation is completed. GOSTAT = 0: No GO operation in progress. Software note: Users must not initiate another GOSET operation in PLLCMD until GOSTAT is cleared to 0.

7 ALNCTL Register (Offset = 140h) [reset = 3h]

ALNCTL is shown in Figure 14-4115 and described in Table 14-8285.

Return to the Summary Table.

PLL Controller clock align control register

Table 14-12398. ALNCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0140h
MCU_PLLCTRL0	4020 0140h

Figure 14-4115. ALNCTL Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
ALN							
R/W-1h							
7	6	5	4	3	2	1	0
ALN							ALN1
R/W-1h							R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-12400. ALNCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	ALN	R/W	1h	SYSCLKx needs to be aligned with other clocks selected in this register. ALNx = 0: Do not need to align SYSCLKx to other clocks. SYSCLKx is left free-running. ALNx = 1: Align SYSCLKx to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: In the case when a divider is disabled (DxEN = 0) but the respective ALNx = 1, GO operation should ignore ALNx = 1. DxEN takes priority. Existence of ALN [8:3] are determined by RTL parameter SYSCLK. If the corresponding SYSCLK does not exist, the ALNx bit will be read-only and default to 0.
0	ALN1	R/W	1h	SYSCLK1 needs to be aligned with other clocks selected in this register. ALN1 = 0: Do not need to align SYSCLK1 to other clocks. SYSCLK1 is left free-running. ALN1 = 1: Align SYSCLK1 to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: in the case when a divider is disabled (D1EN = 0) but ALN1 = 1, GO operation should ignore ALN1 = 1. D1EN takes priority.

8 DCHANGE Register (Offset = 144h) [reset = 0h]

DCHANGE is shown in Figure 14-4116 and described in Table 14-8287.

Return to the Summary Table.

PLLDIV ratio change register

Table 14-12401. DCHANGE Instances

Instance	Physical Address
PLLCTRL0	0041 0144h
MCU_PLLCTRL0	4020 0144h

Figure 14-4116. DCHANGE Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
SYS							
R-0h							
7	6	5	4	3	2	1	0
SYS							SYS1
R-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-12403. DCHANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	SYS	R	0h	SYSCLKx divide ratio has been modified. SYSCLKx ratio will be changed during GO operation. SYSx = 0: SYSCLKx ratio has not been modified. When GOSET is set, SYSCLKx will not be affected. SYSx = 1: SYSCLKx ratio has been modified. When GOSET is set, SYSCLKx will change to the new ratio.
0	SYS1	R	0h	SYSCLK1 divide ratio has been modified. SYSCLK1 ratio will be changed during GO operation. SYS1 = 0: SYSCLK1 ratio has not been modified. When GOSET is set, SYSCLK1 will not be affected. SYS1 = 1: SYSCLK1 ratio has been modified. When GOSET is set, SYSCLK1 will change to the new ratio.

14.3 Processors and Accelerators Registers

14.3.1 A53SS Registers

14.3.1.1 A53SS

A53SS

14.3.1.1.1 A53SS Summaries

A53SS Summaries

Table 14-12404. ECC_AGGR Registers, Base Address=0071 8000h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 8000h
8h	32	ECC_AGGR_VECTOR	0071 8008h
Ch	32	ECC_AGGR_STAT	0071 800Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 8010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 803Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 8040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 8080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 80C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 813Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 8140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 8180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 81C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 8200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 8204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 8208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 820Ch

Table 14-12405. ECC_AGGR Registers, Base Address=0071 8400h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 8400h
8h	32	ECC_AGGR_VECTOR	0071 8408h
Ch	32	ECC_AGGR_STAT	0071 840Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 8410h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 843Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 8440h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 8480h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 84C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 853Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 8540h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 8580h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 85C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 8600h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 8604h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 8608h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 860Ch

Table 14-12406. ECC_AGGR Registers, Base Address=0071 8800h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 8800h
8h	32	ECC_AGGR_VECTOR	0071 8808h
Ch	32	ECC_AGGR_STAT	0071 880Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 8810h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 883Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 8840h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 8880h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 88C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 893Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 8940h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 8980h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 89C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 8A00h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 8A04h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 8A08h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 8A0Ch

Table 14-12407. ECC_AGGR Registers, Base Address=0071 8C00h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 8C00h
8h	32	ECC_AGGR_VECTOR	0071 8C08h
Ch	32	ECC_AGGR_STAT	0071 8C0Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 8C10h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 8C3Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 8C40h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 8C80h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 8CC0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 8D3Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 8D40h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 8D80h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 8DC0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 8E00h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 8E04h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 8E08h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 8E0Ch

Table 14-12408. ECC_AGGR Registers, Base Address=0071 9000h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 9000h
8h	32	ECC_AGGR_VECTOR	0071 9008h
Ch	32	ECC_AGGR_STAT	0071 900Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 9010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 903Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 9040h

Table 14-12408. ECC_AGGR Registers, Base Address=0071 9000h, Length=1024 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 9080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 90C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 913Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 9140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 9180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 91C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 9200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 9204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 9208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 920Ch

Table 14-12409. A53SS_SS_ROM Registers, Base Address=0007 3000 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_SS_ROM_ROMENTRY0	0007 3000 0000h
4h	32	A53SS_SS_ROM_ROMENTRY1	0007 3000 0004h
8h	32	A53SS_SS_ROM_ROMENTRY2	0007 3000 0008h
Ch	32	A53SS_SS_ROM_ROMENTRY3	0007 3000 000Ch
10h	32	A53SS_SS_ROM_ROMENTRY4	0007 3000 0010h
14h	32	A53SS_SS_ROM_ROMENTRY5	0007 3000 0014h
18h	32	A53SS_SS_ROM_ROMENTRY6	0007 3000 0018h
1Ch	32	A53SS_SS_ROM_ROMENTRY7	0007 3000 001Ch
20h	32	A53SS_SS_ROM_ROMENTRY8	0007 3000 0020h
24h	32	A53SS_SS_ROM_ROMENTRY9	0007 3000 0024h
28h	32	A53SS_SS_ROM_ROMENTRY10	0007 3000 0028h
2Ch	32	A53SS_SS_ROM_ROMENTRY11	0007 3000 002Ch
30h	32	A53SS_SS_ROM_ROMENTRY12	0007 3000 0030h
34h	32	A53SS_SS_ROM_ROMENTRY13	0007 3000 0034h
38h	32	A53SS_SS_ROM_ROMENTRY14	0007 3000 0038h
3Ch	32	A53SS_SS_ROM_ROMENTRY15	0007 3000 003Ch
FD0h	32	A53SS_SS_ROM_ROM_PERIPHID4_VAL	0007 3000 0FD0h
FD4h	32	A53SS_SS_ROM_ROM_PERIPHID5_VAL	0007 3000 0FD4h
FD8h	32	A53SS_SS_ROM_ROM_PERIPHID6_VAL	0007 3000 0FD8h
FDCh	32	A53SS_SS_ROM_ROM_PERIPHID7_VAL	0007 3000 0FDCh
FE0h	32	A53SS_SS_ROM_ROM_PERIPHID0_VAL	0007 3000 0FE0h
FE4h	32	A53SS_SS_ROM_ROM_PERIPHID1_VAL	0007 3000 0FE4h
FE8h	32	A53SS_SS_ROM_ROM_PERIPHID2_VAL	0007 3000 0FE8h
FECh	32	A53SS_SS_ROM_ROM_PERIPHID3_VAL	0007 3000 0FECh
FF0h	32	A53SS_SS_ROM_ROM_COMPONID0_VAL	0007 3000 0FF0h
FF4h	32	A53SS_SS_ROM_ROM_COMPONID1_VAL	0007 3000 0FF4h
FF8h	32	A53SS_SS_ROM_ROM_COMPONID2_VAL	0007 3000 0FF8h
FFCh	32	A53SS_SS_ROM_ROM_COMPONID3_VAL	0007 3000 0FFCh

Table 14-12410. A53SS_CORE0_DBG Registers, Base Address=0007 3001 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_CORE0_DBG_EDESR	0007 3001 0020h
24h	32	A53SS_CORE0_DBG_EDECR	0007 3001 0024h
30h	32	A53SS_CORE0_DBG_EDWAR_31_0	0007 3001 0030h
34h	32	A53SS_CORE0_DBG_EDWAR_63_32	0007 3001 0034h
80h	32	A53SS_CORE0_DBG_DBGDTRRX_EL0	0007 3001 0080h
84h	32	A53SS_CORE0_DBG_EDITR	0007 3001 0084h
88h	32	A53SS_CORE0_DBG_EDSCR	0007 3001 0088h
8Ch	32	A53SS_CORE0_DBG_DBGDTRTX_EL0	0007 3001 008Ch
90h	32	A53SS_CORE0_DBG_EDRCR	0007 3001 0090h
94h	32	A53SS_CORE0_DBG_EDACR	0007 3001 0094h
98h	32	A53SS_CORE0_DBG_EDECCR	0007 3001 0098h
A0h	32	A53SS_CORE0_DBG_EDPCSR_31_0	0007 3001 00A0h
A4h	32	A53SS_CORE0_DBG_EDCIDSR	0007 3001 00A4h
A8h	32	A53SS_CORE0_DBG_EDVIDSR	0007 3001 00A8h
ACh	32	A53SS_CORE0_DBG_EDPCSR_63_32	0007 3001 00ACh
300h	32	A53SS_CORE0_DBG_OSLAR_EL1	0007 3001 0300h
310h	32	A53SS_CORE0_DBG_EDPRCR	0007 3001 0310h
314h	32	A53SS_CORE0_DBG_EDPRSR	0007 3001 0314h
400h	32	A53SS_CORE0_DBG_DBGBVR0_EL1_31_0	0007 3001 0400h
404h	32	A53SS_CORE0_DBG_DBGBVR0_EL1_63_32	0007 3001 0404h
408h	32	A53SS_CORE0_DBG_DBGBCR0_EL1	0007 3001 0408h
410h	32	A53SS_CORE0_DBG_DBGBVR1_EL1_31_0	0007 3001 0410h
414h	32	A53SS_CORE0_DBG_DBGBVR1_EL1_63_32	0007 3001 0414h
418h	32	A53SS_CORE0_DBG_DBGBCR1_EL1	0007 3001 0418h
420h	32	A53SS_CORE0_DBG_DBGBVR2_EL1_31_0	0007 3001 0420h
424h	32	A53SS_CORE0_DBG_DBGBVR2_EL1_63_32	0007 3001 0424h
428h	32	A53SS_CORE0_DBG_DBGBCR2_EL1	0007 3001 0428h
430h	32	A53SS_CORE0_DBG_DBGBVR3_EL1_31_0	0007 3001 0430h
434h	32	A53SS_CORE0_DBG_DBGBVR3_EL1_63_32	0007 3001 0434h
438h	32	A53SS_CORE0_DBG_DBGBCR3_EL1	0007 3001 0438h
440h	32	A53SS_CORE0_DBG_DBGBVR4_EL1_31_0	0007 3001 0440h
444h	32	A53SS_CORE0_DBG_DBGBVR4_EL1_63_32	0007 3001 0444h
448h	32	A53SS_CORE0_DBG_DBGBCR4_EL1	0007 3001 0448h
450h	32	A53SS_CORE0_DBG_DBGBVR5_EL1_31_0	0007 3001 0450h
454h	32	A53SS_CORE0_DBG_DBGBVR5_EL1_63_32	0007 3001 0454h
458h	32	A53SS_CORE0_DBG_DBGBCR5_EL1	0007 3001 0458h
800h	32	A53SS_CORE0_DBG_DBGWVR0_EL1_31_0	0007 3001 0800h
804h	32	A53SS_CORE0_DBG_DBGWVR0_EL1_63_32	0007 3001 0804h
808h	32	A53SS_CORE0_DBG_DBGWCR0_EL1	0007 3001 0808h
810h	32	A53SS_CORE0_DBG_DBGWVR1_EL1_31_0	0007 3001 0810h
814h	32	A53SS_CORE0_DBG_DBGWVR1_EL1_63_32	0007 3001 0814h
818h	32	A53SS_CORE0_DBG_DBGWCR1_EL1	0007 3001 0818h
820h	32	A53SS_CORE0_DBG_DBGWVR2_EL1_31_0	0007 3001 0820h
824h	32	A53SS_CORE0_DBG_DBGWVR2_EL1_63_32	0007 3001 0824h
828h	32	A53SS_CORE0_DBG_DBGWCR2_EL1	0007 3001 0828h

Table 14-12410. A53SS_CORE0_DBG Registers, Base Address=0007 3001 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
830h	32	A53SS_CORE0_DBG_DBGWVR3_EL1_31_0	0007 3001 0830h
834h	32	A53SS_CORE0_DBG_DBGWVR3_EL1_63_32	0007 3001 0834h
838h	32	A53SS_CORE0_DBG_DBGWCR3_EL1	0007 3001 0838h
D00h	32	A53SS_CORE0_DBG_MIDR_EL1	0007 3001 0D00h
D20h	32	A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0	0007 3001 0D20h
D24h	32	A53SS_CORE0_DBG_ID_AA64PFR0_EL1_63_32	0007 3001 0D24h
D28h	32	A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0	0007 3001 0D28h
D2Ch	32	A53SS_CORE0_DBG_ID_AA64DFR0_EL1_63_32	0007 3001 0D2Ch
D30h	32	A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0	0007 3001 0D30h
D34h	32	A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_63_32	0007 3001 0D34h
D38h	32	A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0	0007 3001 0D38h
D3Ch	32	A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_63_32	0007 3001 0D3Ch
D40h	32	A53SS_CORE0_DBG_ID_AA64PFR1_EL1_31_0	0007 3001 0D40h
D44h	32	A53SS_CORE0_DBG_ID_AA64PFR1_EL1_63_32	0007 3001 0D44h
D48h	32	A53SS_CORE0_DBG_ID_AA64DFR1_EL1_31_0	0007 3001 0D48h
D4Ch	32	A53SS_CORE0_DBG_ID_AA64DFR1_EL1_63_32	0007 3001 0D4Ch
D50h	32	A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_31_0	0007 3001 0D50h
D54h	32	A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_63_32	0007 3001 0D54h
D58h	32	A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_31_0	0007 3001 0D58h
D5Ch	32	A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_63_32	0007 3001 0D5Ch
F00h	32	A53SS_CORE0_DBG_EDITCTRL	0007 3001 0F00h
FA0h	32	A53SS_CORE0_DBG_DBGCLAIMSET_EL1	0007 3001 0FA0h
FA4h	32	A53SS_CORE0_DBG_DBGCLAIMCLR_EL1	0007 3001 0FA4h
FA8h	32	A53SS_CORE0_DBG_EDDEVAFF0	0007 3001 0FA8h
FACh	32	A53SS_CORE0_DBG_EDDEVAFF1	0007 3001 0FACh
FB0h	32	A53SS_CORE0_DBG_EDLAR	0007 3001 0FB0h
FB4h	32	A53SS_CORE0_DBG_EDLSR	0007 3001 0FB4h
FB8h	32	A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1	0007 3001 0FB8h
FBCh	32	A53SS_CORE0_DBG_EDDEVARCH	0007 3001 0FBCh
FC0h	32	A53SS_CORE0_DBG_EDDEVID2	0007 3001 0FC0h
FC4h	32	A53SS_CORE0_DBG_EDDEVID1	0007 3001 0FC4h
FC8h	32	A53SS_CORE0_DBG_EDDEVID	0007 3001 0FC8h
FCCh	32	A53SS_CORE0_DBG_EDDEVTYPE	0007 3001 0FCCh
FD0h	32	A53SS_CORE0_DBG_EDPIDR4	0007 3001 0FD0h
FE0h	32	A53SS_CORE0_DBG_EDPIDR0	0007 3001 0FE0h
FE4h	32	A53SS_CORE0_DBG_EDPIDR1	0007 3001 0FE4h
FE8h	32	A53SS_CORE0_DBG_EDPIDR2	0007 3001 0FE8h
FECh	32	A53SS_CORE0_DBG_EDPIDR3	0007 3001 0FECh
FF0h	32	A53SS_CORE0_DBG_EDCIDR0	0007 3001 0FF0h
FF4h	32	A53SS_CORE0_DBG_EDCIDR1	0007 3001 0FF4h
FF8h	32	A53SS_CORE0_DBG_EDCIDR2	0007 3001 0FF8h
FFCh	32	A53SS_CORE0_DBG_EDCIDR3	0007 3001 0FFCh

Table 14-12411. A53SS_CORE0_CTI Registers, Base Address=0007 3002 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE0_CTI_CTICONTROL	0007 3002 0000h
10h	32	A53SS_CORE0_CTI_CTIINTACK	0007 3002 0010h
14h	32	A53SS_CORE0_CTI_CTIAPPSET	0007 3002 0014h
18h	32	A53SS_CORE0_CTI_CTIAPPCLEAR	0007 3002 0018h
1Ch	32	A53SS_CORE0_CTI_CTIAPPPULSE	0007 3002 001Ch
20h	32	A53SS_CORE0_CTI_CTIINEN0	0007 3002 0020h
24h	32	A53SS_CORE0_CTI_CTIINEN1	0007 3002 0024h
28h	32	A53SS_CORE0_CTI_CTIINEN2	0007 3002 0028h
2Ch	32	A53SS_CORE0_CTI_CTIINEN3	0007 3002 002Ch
30h	32	A53SS_CORE0_CTI_CTIINEN4	0007 3002 0030h
34h	32	A53SS_CORE0_CTI_CTIINEN5	0007 3002 0034h
38h	32	A53SS_CORE0_CTI_CTIINEN6	0007 3002 0038h
3Ch	32	A53SS_CORE0_CTI_CTIINEN7	0007 3002 003Ch
A0h	32	A53SS_CORE0_CTI_CTIOUTEN0	0007 3002 00A0h
A4h	32	A53SS_CORE0_CTI_CTIOUTEN1	0007 3002 00A4h
A8h	32	A53SS_CORE0_CTI_CTIOUTEN2	0007 3002 00A8h
ACh	32	A53SS_CORE0_CTI_CTIOUTEN3	0007 3002 00ACh
B0h	32	A53SS_CORE0_CTI_CTIOUTEN4	0007 3002 00B0h
B4h	32	A53SS_CORE0_CTI_CTIOUTEN5	0007 3002 00B4h
B8h	32	A53SS_CORE0_CTI_CTIOUTEN6	0007 3002 00B8h
BCh	32	A53SS_CORE0_CTI_CTIOUTEN7	0007 3002 00BCh
130h	32	A53SS_CORE0_CTI_CTITRIGINSTATUS	0007 3002 0130h
134h	32	A53SS_CORE0_CTI_CTITRIGOUTSTATUS	0007 3002 0134h
138h	32	A53SS_CORE0_CTI_CTICHINSTATUS	0007 3002 0138h
13Ch	32	A53SS_CORE0_CTI_CTICHOUTSTATUS	0007 3002 013Ch
140h	32	A53SS_CORE0_CTI_CTIGATE	0007 3002 0140h
144h	32	A53SS_CORE0_CTI_ASICCTL	0007 3002 0144h
F00h	32	A53SS_CORE0_CTI_CTIITCTRL	0007 3002 0F00h
FA0h	32	A53SS_CORE0_CTI_CTICLAIMSET	0007 3002 0FA0h
FA4h	32	A53SS_CORE0_CTI_CTICLAIMCLR	0007 3002 0FA4h
FA8h	32	A53SS_CORE0_CTI_CTIDEVAFF0	0007 3002 0FA8h
FACh	32	A53SS_CORE0_CTI_CTIDEVAFF1	0007 3002 0FACh
FB0h	32	A53SS_CORE0_CTI_CTILAR	0007 3002 0FB0h
FB4h	32	A53SS_CORE0_CTI_CTILSR	0007 3002 0FB4h
FB8h	32	A53SS_CORE0_CTI_CTIAUTHSTATUS	0007 3002 0FB8h
FBCh	32	A53SS_CORE0_CTI_CTIDEVARCH	0007 3002 0FBCh
FC0h	32	A53SS_CORE0_CTI_CTIDEVID2	0007 3002 0FC0h
FC4h	32	A53SS_CORE0_CTI_CTIDEVID1	0007 3002 0FC4h
FC8h	32	A53SS_CORE0_CTI_CTIDEVID	0007 3002 0FC8h
FCCh	32	A53SS_CORE0_CTI_CTIDEVTYPE	0007 3002 0FCCh
FD0h	32	A53SS_CORE0_CTI_CTIPIDR4	0007 3002 0FD0h
FD4h	32	A53SS_CORE0_CTI_CTIPIDR5	0007 3002 0FD4h
FD8h	32	A53SS_CORE0_CTI_CTIPIDR6	0007 3002 0FD8h
FDCh	32	A53SS_CORE0_CTI_CTIPIDR7	0007 3002 0FDCh
FE0h	32	A53SS_CORE0_CTI_CTIPIDR0	0007 3002 0FE0h

Table 14-12411. A53SS_CORE0_CTI Registers, Base Address=0007 3002 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FE4h	32	A53SS_CORE0_CTI_CTIPIDR1	0007 3002 0FE4h
FE8h	32	A53SS_CORE0_CTI_CTIPIDR2	0007 3002 0FE8h
FECh	32	A53SS_CORE0_CTI_CTIPIDR3	0007 3002 0FECh
FF0h	32	A53SS_CORE0_CTI_CTICIDR0	0007 3002 0FF0h
FF4h	32	A53SS_CORE0_CTI_CTICIDR1	0007 3002 0FF4h
FF8h	32	A53SS_CORE0_CTI_CTICIDR2	0007 3002 0FF8h
FFCh	32	A53SS_CORE0_CTI_CTICIDR3	0007 3002 0FFCh

Table 14-12412. A53SS_CORE0_PMU Registers, Base Address=0007 3003 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE0_PMU_PMEVCNTR0_EL0	0007 3003 0000h
8h	32	A53SS_CORE0_PMU_PMEVCNTR1_EL0	0007 3003 0008h
10h	32	A53SS_CORE0_PMU_PMEVCNTR2_EL0	0007 3003 0010h
18h	32	A53SS_CORE0_PMU_PMEVCNTR3_EL0	0007 3003 0018h
20h	32	A53SS_CORE0_PMU_PMEVCNTR4_EL0	0007 3003 0020h
28h	32	A53SS_CORE0_PMU_PMEVCNTR5_EL0	0007 3003 0028h
F8h	32	A53SS_CORE0_PMU_PMCCNTR_EL0_31_0	0007 3003 00F8h
FCh	32	A53SS_CORE0_PMU_PMCCNTR_EL0_63_32	0007 3003 00FCh
400h	32	A53SS_CORE0_PMU_PMEVTYPER0_EL0	0007 3003 0400h
404h	32	A53SS_CORE0_PMU_PMEVTYPER1_EL0	0007 3003 0404h
408h	32	A53SS_CORE0_PMU_PMEVTYPER2_EL0	0007 3003 0408h
40Ch	32	A53SS_CORE0_PMU_PMEVTYPER3_EL0	0007 3003 040Ch
410h	32	A53SS_CORE0_PMU_PMEVTYPER4_EL0	0007 3003 0410h
414h	32	A53SS_CORE0_PMU_PMEVTYPER5_EL0	0007 3003 0414h
47Ch	32	A53SS_CORE0_PMU_PMCCFILTR_EL0	0007 3003 047Ch
C00h	32	A53SS_CORE0_PMU_PMCNTENSET_EL0	0007 3003 0C00h
C20h	32	A53SS_CORE0_PMU_PMCNTENCLR_EL0	0007 3003 0C20h
C40h	32	A53SS_CORE0_PMU_PMINTENSET_EL1	0007 3003 0C40h
C60h	32	A53SS_CORE0_PMU_PMINTENCLR_EL1	0007 3003 0C60h
C80h	32	A53SS_CORE0_PMU_PMOVSCLR_EL0	0007 3003 0C80h
CA0h	32	A53SS_CORE0_PMU_PMSWINC_EL0	0007 3003 0CA0h
CC0h	32	A53SS_CORE0_PMU_PMOVSSET_EL0	0007 3003 0CC0h
E00h	32	A53SS_CORE0_PMU_PMCFGR	0007 3003 0E00h
E04h	32	A53SS_CORE0_PMU_PMCR_EL0	0007 3003 0E04h
E20h	32	A53SS_CORE0_PMU_PMCEID0_EL0	0007 3003 0E20h
E24h	32	A53SS_CORE0_PMU_PMCEID1_EL0	0007 3003 0E24h
F00h	32	A53SS_CORE0_PMU_PMITCTRL	0007 3003 0F00h
FA8h	32	A53SS_CORE0_PMU_PMDEVAFF0	0007 3003 0FA8h
FACh	32	A53SS_CORE0_PMU_PMDEVAFF1	0007 3003 0FACh
FB0h	32	A53SS_CORE0_PMU_PMLAR	0007 3003 0FB0h
FB4h	32	A53SS_CORE0_PMU_PMLSR	0007 3003 0FB4h
FB8h	32	A53SS_CORE0_PMU_PMAUTHSTATUS	0007 3003 0FB8h
FBCh	32	A53SS_CORE0_PMU_PMDEVARCH	0007 3003 0FBCh
FCCh	32	A53SS_CORE0_PMU_PMDEVTYPE	0007 3003 0FCCh

Table 14-12412. A53SS_CORE0_PMU Registers, Base Address=0007 3003 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FD0h	32	A53SS_CORE0_PMU_PMPIDR4	0007 3003 0FD0h
FD4h	32	A53SS_CORE0_PMU_PMPIDR5	0007 3003 0FD4h
FD8h	32	A53SS_CORE0_PMU_PMPIDR6	0007 3003 0FD8h
FDCh	32	A53SS_CORE0_PMU_PMPIDR7	0007 3003 0FDCh
FE0h	32	A53SS_CORE0_PMU_PMPIDR0	0007 3003 0FE0h
FE4h	32	A53SS_CORE0_PMU_PMPIDR1	0007 3003 0FE4h
FE8h	32	A53SS_CORE0_PMU_PMPIDR2	0007 3003 0FE8h
FECh	32	A53SS_CORE0_PMU_PMPIDR3	0007 3003 0FECh
FF0h	32	A53SS_CORE0_PMU_PMCIDR0	0007 3003 0FF0h
FF4h	32	A53SS_CORE0_PMU_PMCIDR1	0007 3003 0FF4h
FF8h	32	A53SS_CORE0_PMU_PMCIDR2	0007 3003 0FF8h
FFCh	32	A53SS_CORE0_PMU_PMCIDR3	0007 3003 0FFCh

Table 14-12413. A53SS_CORE0_ETM Registers, Base Address=0007 3004 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_CORE0_ETM_TRCPRGCTLR	0007 3004 0004h
Ch	32	A53SS_CORE0_ETM_TRCSTATR	0007 3004 000Ch
10h	32	A53SS_CORE0_ETM_TRCCONFIGR	0007 3004 0010h
18h	32	A53SS_CORE0_ETM_TRCAUXCTLR	0007 3004 0018h
20h	32	A53SS_CORE0_ETM_TRCEVENTCTL0R	0007 3004 0020h
24h	32	A53SS_CORE0_ETM_TRCEVENTCTL1R	0007 3004 0024h
2Ch	32	A53SS_CORE0_ETM_TRCSTALLCTLR	0007 3004 002Ch
30h	32	A53SS_CORE0_ETM_TRCTSCTLR	0007 3004 0030h
34h	32	A53SS_CORE0_ETM_TRCSYNCPR	0007 3004 0034h
38h	32	A53SS_CORE0_ETM_TRCCCCTLR	0007 3004 0038h
3Ch	32	A53SS_CORE0_ETM_TRCBBCTLR	0007 3004 003Ch
40h	32	A53SS_CORE0_ETM_TRCTRACEIDR	0007 3004 0040h
80h	32	A53SS_CORE0_ETM_TRCVICTLR	0007 3004 0080h
84h	32	A53SS_CORE0_ETM_TRCVIIECTLR	0007 3004 0084h
88h	32	A53SS_CORE0_ETM_TRCVISSCTLR	0007 3004 0088h
100h	32	A53SS_CORE0_ETM_TRCSEQEVR0	0007 3004 0100h
104h	32	A53SS_CORE0_ETM_TRCSEQEVR1	0007 3004 0104h
108h	32	A53SS_CORE0_ETM_TRCSEQEVR2	0007 3004 0108h
118h	32	A53SS_CORE0_ETM_TRCSEQRSTEVR	0007 3004 0118h
11Ch	32	A53SS_CORE0_ETM_TRCSEQSTR	0007 3004 011Ch
120h	32	A53SS_CORE0_ETM_TRCEXTINSELR	0007 3004 0120h
140h	32	A53SS_CORE0_ETM_TRCCNTRLDVR0	0007 3004 0140h
144h	32	A53SS_CORE0_ETM_TRCCNTRLDVR1	0007 3004 0144h
150h	32	A53SS_CORE0_ETM_TRCCNTCTLR0	0007 3004 0150h
154h	32	A53SS_CORE0_ETM_TRCCNTCTLR1	0007 3004 0154h
160h	32	A53SS_CORE0_ETM_TRCCNTVR0	0007 3004 0160h
164h	32	A53SS_CORE0_ETM_TRCCNTVR1	0007 3004 0164h
180h	32	A53SS_CORE0_ETM_TRCIDR8	0007 3004 0180h
184h	32	A53SS_CORE0_ETM_TRCIDR9	0007 3004 0184h

Table 14-12413. A53SS_CORE0_ETM Registers, Base Address=0007 3004 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
188h	32	A53SS_CORE0_ETM_TRCIDR10	0007 3004 0188h
18Ch	32	A53SS_CORE0_ETM_TRCIDR11	0007 3004 018Ch
190h	32	A53SS_CORE0_ETM_TRCIDR12	0007 3004 0190h
194h	32	A53SS_CORE0_ETM_TRCIDR13	0007 3004 0194h
1C0h	32	A53SS_CORE0_ETM_TRCIMSPEC0	0007 3004 01C0h
1E0h	32	A53SS_CORE0_ETM_TRCIDR0	0007 3004 01E0h
1E4h	32	A53SS_CORE0_ETM_TRCIDR1	0007 3004 01E4h
1E8h	32	A53SS_CORE0_ETM_TRCIDR2	0007 3004 01E8h
1ECh	32	A53SS_CORE0_ETM_TRCIDR3	0007 3004 01ECh
1F0h	32	A53SS_CORE0_ETM_TRCIDR4	0007 3004 01F0h
1F4h	32	A53SS_CORE0_ETM_TRCIDR5	0007 3004 01F4h
208h	32	A53SS_CORE0_ETM_TRCRSCTLR2	0007 3004 0208h
20Ch	32	A53SS_CORE0_ETM_TRCRSCTLR3	0007 3004 020Ch
210h	32	A53SS_CORE0_ETM_TRCRSCTLR4	0007 3004 0210h
214h	32	A53SS_CORE0_ETM_TRCRSCTLR5	0007 3004 0214h
218h	32	A53SS_CORE0_ETM_TRCRSCTLR6	0007 3004 0218h
21Ch	32	A53SS_CORE0_ETM_TRCRSCTLR7	0007 3004 021Ch
220h	32	A53SS_CORE0_ETM_TRCRSCTLR8	0007 3004 0220h
224h	32	A53SS_CORE0_ETM_TRCRSCTLR9	0007 3004 0224h
228h	32	A53SS_CORE0_ETM_TRCRSCTLR10	0007 3004 0228h
22Ch	32	A53SS_CORE0_ETM_TRCRSCTLR11	0007 3004 022Ch
230h	32	A53SS_CORE0_ETM_TRCRSCTLR12	0007 3004 0230h
234h	32	A53SS_CORE0_ETM_TRCRSCTLR13	0007 3004 0234h
238h	32	A53SS_CORE0_ETM_TRCRSCTLR14	0007 3004 0238h
23Ch	32	A53SS_CORE0_ETM_TRCRSCTLR15	0007 3004 023Ch
280h	32	A53SS_CORE0_ETM_TRCSSCCR0	0007 3004 0280h
2A0h	32	A53SS_CORE0_ETM_TRCSSCSR0	0007 3004 02A0h
300h	32	A53SS_CORE0_ETM_TRCOSLAR	0007 3004 0300h
304h	32	A53SS_CORE0_ETM_TRCOSLSR	0007 3004 0304h
310h	32	A53SS_CORE0_ETM_TRCPDCR	0007 3004 0310h
314h	32	A53SS_CORE0_ETM_TRCPDSR	0007 3004 0314h
400h	32	A53SS_CORE0_ETM_TRCACVR0_31_0	0007 3004 0400h
404h	32	A53SS_CORE0_ETM_TRCACVR0_63_32	0007 3004 0404h
408h	32	A53SS_CORE0_ETM_TRCACVR1_31_0	0007 3004 0408h
40Ch	32	A53SS_CORE0_ETM_TRCACVR1_63_32	0007 3004 040Ch
410h	32	A53SS_CORE0_ETM_TRCACVR2_31_0	0007 3004 0410h
414h	32	A53SS_CORE0_ETM_TRCACVR2_63_32	0007 3004 0414h
418h	32	A53SS_CORE0_ETM_TRCACVR3_31_0	0007 3004 0418h
41Ch	32	A53SS_CORE0_ETM_TRCACVR3_63_32	0007 3004 041Ch
420h	32	A53SS_CORE0_ETM_TRCACVR4_31_0	0007 3004 0420h
424h	32	A53SS_CORE0_ETM_TRCACVR4_63_32	0007 3004 0424h
428h	32	A53SS_CORE0_ETM_TRCACVR5_31_0	0007 3004 0428h
42Ch	32	A53SS_CORE0_ETM_TRCACVR5_63_32	0007 3004 042Ch
430h	32	A53SS_CORE0_ETM_TRCACVR6_31_0	0007 3004 0430h

Table 14-12413. A53SS_CORE0_ETM Registers, Base Address=0007 3004 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
434h	32	A53SS_CORE0_ETM_TRCACVR6_63_32	0007 3004 0434h
438h	32	A53SS_CORE0_ETM_TRCACVR7_31_0	0007 3004 0438h
43Ch	32	A53SS_CORE0_ETM_TRCACVR7_63_32	0007 3004 043Ch
480h	32	A53SS_CORE0_ETM_TRCACATR0	0007 3004 0480h
488h	32	A53SS_CORE0_ETM_TRCACATR1	0007 3004 0488h
490h	32	A53SS_CORE0_ETM_TRCACATR2	0007 3004 0490h
498h	32	A53SS_CORE0_ETM_TRCACATR3	0007 3004 0498h
4A0h	32	A53SS_CORE0_ETM_TRCACATR4	0007 3004 04A0h
4A8h	32	A53SS_CORE0_ETM_TRCACATR5	0007 3004 04A8h
4B0h	32	A53SS_CORE0_ETM_TRCACATR6	0007 3004 04B0h
4B8h	32	A53SS_CORE0_ETM_TRCACATR7	0007 3004 04B8h
600h	32	A53SS_CORE0_ETM_TRCCIDCVR0	0007 3004 0600h
640h	32	A53SS_CORE0_ETM_TRCVMIDCVR0	0007 3004 0640h
680h	32	A53SS_CORE0_ETM_TRCCIDCCTLR0	0007 3004 0680h
EE4h	32	A53SS_CORE0_ETM_TRCITATBIDR	0007 3004 0EE4h
EECh	32	A53SS_CORE0_ETM_TRCITIDATAR	0007 3004 0EECh
EF4h	32	A53SS_CORE0_ETM_TRCITIATBINR	0007 3004 0EF4h
EFCh	32	A53SS_CORE0_ETM_TRCITIATBOUTR	0007 3004 0EFCh
F00h	32	A53SS_CORE0_ETM_TRCITCTRL	0007 3004 0F00h
FA0h	32	A53SS_CORE0_ETM_TRCCLAIMSET	0007 3004 0FA0h
FA4h	32	A53SS_CORE0_ETM_TRCCLAIMCLR	0007 3004 0FA4h
FA8h	32	A53SS_CORE0_ETM_TRCDEVAFF0	0007 3004 0FA8h
FACh	32	A53SS_CORE0_ETM_TRCDEVAFF1	0007 3004 0FACh
FB0h	32	A53SS_CORE0_ETM_TRCLAR	0007 3004 0FB0h
FB4h	32	A53SS_CORE0_ETM_TRCLSR	0007 3004 0FB4h
FB8h	32	A53SS_CORE0_ETM_TRCAUTHSTATUS	0007 3004 0FB8h
FBCh	32	A53SS_CORE0_ETM_TRCDEVARCH	0007 3004 0FBCh
FC8h	32	A53SS_CORE0_ETM_TRCDEVID	0007 3004 0FC8h
FCCh	32	A53SS_CORE0_ETM_TRCDEVTYPE	0007 3004 0FCCh
FD0h	32	A53SS_CORE0_ETM_TRCPIDR4	0007 3004 0FD0h
FD4h	32	A53SS_CORE0_ETM_TRCPIDR5	0007 3004 0FD4h
FD8h	32	A53SS_CORE0_ETM_TRCPIDR6	0007 3004 0FD8h
FDCh	32	A53SS_CORE0_ETM_TRCPIDR7	0007 3004 0FDCh
FE0h	32	A53SS_CORE0_ETM_TRCPIDR0	0007 3004 0FE0h
FE4h	32	A53SS_CORE0_ETM_TRCPIDR1	0007 3004 0FE4h
FE8h	32	A53SS_CORE0_ETM_TRCPIDR2	0007 3004 0FE8h
FECh	32	A53SS_CORE0_ETM_TRCPIDR3	0007 3004 0FECh
FF0h	32	A53SS_CORE0_ETM_TRCCIDR0	0007 3004 0FF0h
FF4h	32	A53SS_CORE0_ETM_TRCCIDR1	0007 3004 0FF4h
FF8h	32	A53SS_CORE0_ETM_TRCCIDR2	0007 3004 0FF8h
FFCh	32	A53SS_CORE0_ETM_TRCCIDR3	0007 3004 0FFCh

Table 14-12414. A53SS_CORE1_DBG Registers, Base Address=0007 3011 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_CORE1_DBG_EDESR	0007 3011 0020h
24h	32	A53SS_CORE1_DBG_EDECR	0007 3011 0024h
30h	32	A53SS_CORE1_DBG_EDWAR_31_0	0007 3011 0030h
34h	32	A53SS_CORE1_DBG_EDWAR_63_32	0007 3011 0034h
80h	32	A53SS_CORE1_DBG_DBGDTRRX_EL0	0007 3011 0080h
84h	32	A53SS_CORE1_DBG_EDITR	0007 3011 0084h
88h	32	A53SS_CORE1_DBG_EDSCR	0007 3011 0088h
8Ch	32	A53SS_CORE1_DBG_DBGDTRTX_EL0	0007 3011 008Ch
90h	32	A53SS_CORE1_DBG_EDRCR	0007 3011 0090h
94h	32	A53SS_CORE1_DBG_EDACR	0007 3011 0094h
98h	32	A53SS_CORE1_DBG_EDECCR	0007 3011 0098h
A0h	32	A53SS_CORE1_DBG_EDPCSR_31_0	0007 3011 00A0h
A4h	32	A53SS_CORE1_DBG_EDCIDSR	0007 3011 00A4h
A8h	32	A53SS_CORE1_DBG_EDVIDSR	0007 3011 00A8h
ACh	32	A53SS_CORE1_DBG_EDPCSR_63_32	0007 3011 00ACh
300h	32	A53SS_CORE1_DBG_OSLAR_EL1	0007 3011 0300h
310h	32	A53SS_CORE1_DBG_EDPRCR	0007 3011 0310h
314h	32	A53SS_CORE1_DBG_EDPRSR	0007 3011 0314h
400h	32	A53SS_CORE1_DBG_DBGBVR0_EL1_31_0	0007 3011 0400h
404h	32	A53SS_CORE1_DBG_DBGBVR0_EL1_63_32	0007 3011 0404h
408h	32	A53SS_CORE1_DBG_DBGBCR0_EL1	0007 3011 0408h
410h	32	A53SS_CORE1_DBG_DBGBVR1_EL1_31_0	0007 3011 0410h
414h	32	A53SS_CORE1_DBG_DBGBVR1_EL1_63_32	0007 3011 0414h
418h	32	A53SS_CORE1_DBG_DBGBCR1_EL1	0007 3011 0418h
420h	32	A53SS_CORE1_DBG_DBGBVR2_EL1_31_0	0007 3011 0420h
424h	32	A53SS_CORE1_DBG_DBGBVR2_EL1_63_32	0007 3011 0424h
428h	32	A53SS_CORE1_DBG_DBGBCR2_EL1	0007 3011 0428h
430h	32	A53SS_CORE1_DBG_DBGBVR3_EL1_31_0	0007 3011 0430h
434h	32	A53SS_CORE1_DBG_DBGBVR3_EL1_63_32	0007 3011 0434h
438h	32	A53SS_CORE1_DBG_DBGBCR3_EL1	0007 3011 0438h
440h	32	A53SS_CORE1_DBG_DBGBVR4_EL1_31_0	0007 3011 0440h
444h	32	A53SS_CORE1_DBG_DBGBVR4_EL1_63_32	0007 3011 0444h
448h	32	A53SS_CORE1_DBG_DBGBCR4_EL1	0007 3011 0448h
450h	32	A53SS_CORE1_DBG_DBGBVR5_EL1_31_0	0007 3011 0450h
454h	32	A53SS_CORE1_DBG_DBGBVR5_EL1_63_32	0007 3011 0454h
458h	32	A53SS_CORE1_DBG_DBGBCR5_EL1	0007 3011 0458h
800h	32	A53SS_CORE1_DBG_DBGWVR0_EL1_31_0	0007 3011 0800h
804h	32	A53SS_CORE1_DBG_DBGWVR0_EL1_63_32	0007 3011 0804h
808h	32	A53SS_CORE1_DBG_DBGWCR0_EL1	0007 3011 0808h
810h	32	A53SS_CORE1_DBG_DBGWVR1_EL1_31_0	0007 3011 0810h
814h	32	A53SS_CORE1_DBG_DBGWVR1_EL1_63_32	0007 3011 0814h
818h	32	A53SS_CORE1_DBG_DBGWCR1_EL1	0007 3011 0818h
820h	32	A53SS_CORE1_DBG_DBGWVR2_EL1_31_0	0007 3011 0820h
824h	32	A53SS_CORE1_DBG_DBGWVR2_EL1_63_32	0007 3011 0824h
828h	32	A53SS_CORE1_DBG_DBGWCR2_EL1	0007 3011 0828h

Table 14-12414. A53SS_CORE1_DBG Registers, Base Address=0007 3011 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
830h	32	A53SS_CORE1_DBG_DBGWVR3_EL1_31_0	0007 3011 0830h
834h	32	A53SS_CORE1_DBG_DBGWVR3_EL1_63_32	0007 3011 0834h
838h	32	A53SS_CORE1_DBG_DBGWCR3_EL1	0007 3011 0838h
D00h	32	A53SS_CORE1_DBG_MIDR_EL1	0007 3011 0D00h
D20h	32	A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0	0007 3011 0D20h
D24h	32	A53SS_CORE1_DBG_ID_AA64PFR0_EL1_63_32	0007 3011 0D24h
D28h	32	A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0	0007 3011 0D28h
D2Ch	32	A53SS_CORE1_DBG_ID_AA64DFR0_EL1_63_32	0007 3011 0D2Ch
D30h	32	A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0	0007 3011 0D30h
D34h	32	A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_63_32	0007 3011 0D34h
D38h	32	A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0	0007 3011 0D38h
D3Ch	32	A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_63_32	0007 3011 0D3Ch
D40h	32	A53SS_CORE1_DBG_ID_AA64PFR1_EL1_31_0	0007 3011 0D40h
D44h	32	A53SS_CORE1_DBG_ID_AA64PFR1_EL1_63_32	0007 3011 0D44h
D48h	32	A53SS_CORE1_DBG_ID_AA64DFR1_EL1_31_0	0007 3011 0D48h
D4Ch	32	A53SS_CORE1_DBG_ID_AA64DFR1_EL1_63_32	0007 3011 0D4Ch
D50h	32	A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_31_0	0007 3011 0D50h
D54h	32	A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_63_32	0007 3011 0D54h
D58h	32	A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_31_0	0007 3011 0D58h
D5Ch	32	A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_63_32	0007 3011 0D5Ch
F00h	32	A53SS_CORE1_DBG_EDITCTRL	0007 3011 0F00h
FA0h	32	A53SS_CORE1_DBG_DBGCLAIMSET_EL1	0007 3011 0FA0h
FA4h	32	A53SS_CORE1_DBG_DBGCLAIMCLR_EL1	0007 3011 0FA4h
FA8h	32	A53SS_CORE1_DBG_EDDEVAFF0	0007 3011 0FA8h
FACh	32	A53SS_CORE1_DBG_EDDEVAFF1	0007 3011 0FACh
FB0h	32	A53SS_CORE1_DBG_EDLAR	0007 3011 0FB0h
FB4h	32	A53SS_CORE1_DBG_EDLSR	0007 3011 0FB4h
FB8h	32	A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1	0007 3011 0FB8h
FBCh	32	A53SS_CORE1_DBG_EDDEVARCH	0007 3011 0FBCh
FC0h	32	A53SS_CORE1_DBG_EDDEVID2	0007 3011 0FC0h
FC4h	32	A53SS_CORE1_DBG_EDDEVID1	0007 3011 0FC4h
FC8h	32	A53SS_CORE1_DBG_EDDEVID	0007 3011 0FC8h
FCCh	32	A53SS_CORE1_DBG_EDDEVTYPE	0007 3011 0FCCh
FD0h	32	A53SS_CORE1_DBG_EDPIDR4	0007 3011 0FD0h
FE0h	32	A53SS_CORE1_DBG_EDPIDR0	0007 3011 0FE0h
FE4h	32	A53SS_CORE1_DBG_EDPIDR1	0007 3011 0FE4h
FE8h	32	A53SS_CORE1_DBG_EDPIDR2	0007 3011 0FE8h
FECh	32	A53SS_CORE1_DBG_EDPIDR3	0007 3011 0FECh
FF0h	32	A53SS_CORE1_DBG_EDCIDR0	0007 3011 0FF0h
FF4h	32	A53SS_CORE1_DBG_EDCIDR1	0007 3011 0FF4h
FF8h	32	A53SS_CORE1_DBG_EDCIDR2	0007 3011 0FF8h
FFCh	32	A53SS_CORE1_DBG_EDCIDR3	0007 3011 0FFCh

Table 14-12415. A53SS_CORE1_PMU Registers, Base Address=0007 3012 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE1_PMU_PMEVCNTR0_EL0	0007 3012 0000h
8h	32	A53SS_CORE1_PMU_PMEVCNTR1_EL0	0007 3012 0008h
10h	32	A53SS_CORE1_PMU_PMEVCNTR2_EL0	0007 3012 0010h
18h	32	A53SS_CORE1_PMU_PMEVCNTR3_EL0	0007 3012 0018h
20h	32	A53SS_CORE1_PMU_PMEVCNTR4_EL0	0007 3012 0020h
28h	32	A53SS_CORE1_PMU_PMEVCNTR5_EL0	0007 3012 0028h
F8h	32	A53SS_CORE1_PMU_PMCCNTR_EL0_31_0	0007 3012 00F8h
FCh	32	A53SS_CORE1_PMU_PMCCNTR_EL0_63_32	0007 3012 00FCh
400h	32	A53SS_CORE1_PMU_PMEVTYPER0_EL0	0007 3012 0400h
404h	32	A53SS_CORE1_PMU_PMEVTYPER1_EL0	0007 3012 0404h
408h	32	A53SS_CORE1_PMU_PMEVTYPER2_EL0	0007 3012 0408h
40Ch	32	A53SS_CORE1_PMU_PMEVTYPER3_EL0	0007 3012 040Ch
410h	32	A53SS_CORE1_PMU_PMEVTYPER4_EL0	0007 3012 0410h
414h	32	A53SS_CORE1_PMU_PMEVTYPER5_EL0	0007 3012 0414h
47Ch	32	A53SS_CORE1_PMU_PMCCFILTR_EL0	0007 3012 047Ch
C00h	32	A53SS_CORE1_PMU_PMCNTENSET_EL0	0007 3012 0C00h
C20h	32	A53SS_CORE1_PMU_PMCNTENCLR_EL0	0007 3012 0C20h
C40h	32	A53SS_CORE1_PMU_PMINTENSET_EL1	0007 3012 0C40h
C60h	32	A53SS_CORE1_PMU_PMINTENCLR_EL1	0007 3012 0C60h
C80h	32	A53SS_CORE1_PMU_PMOVSCLR_EL0	0007 3012 0C80h
CA0h	32	A53SS_CORE1_PMU_PMSWINC_EL0	0007 3012 0CA0h
CC0h	32	A53SS_CORE1_PMU_PMOVSSET_EL0	0007 3012 0CC0h
E00h	32	A53SS_CORE1_PMU_PMCFGR	0007 3012 0E00h
E04h	32	A53SS_CORE1_PMU_PMCR_EL0	0007 3012 0E04h
E20h	32	A53SS_CORE1_PMU_PMCEID0_EL0	0007 3012 0E20h
E24h	32	A53SS_CORE1_PMU_PMCEID1_EL0	0007 3012 0E24h
F00h	32	A53SS_CORE1_PMU_PMITCTRL	0007 3012 0F00h
FA8h	32	A53SS_CORE1_PMU_PMDEVAFF0	0007 3012 0FA8h
FACh	32	A53SS_CORE1_PMU_PMDEVAFF1	0007 3012 0FACh
FB0h	32	A53SS_CORE1_PMU_PMLAR	0007 3012 0FB0h
FB4h	32	A53SS_CORE1_PMU_PMLSR	0007 3012 0FB4h
FB8h	32	A53SS_CORE1_PMU_PMAUTHSTATUS	0007 3012 0FB8h
FBCh	32	A53SS_CORE1_PMU_PMDEVARCH	0007 3012 0FBCh
FCCh	32	A53SS_CORE1_PMU_PMDEVTYPE	0007 3012 0FCCh
FD0h	32	A53SS_CORE1_PMU_PMPIDR4	0007 3012 0FD0h
FD4h	32	A53SS_CORE1_PMU_PMPIDR5	0007 3012 0FD4h
FD8h	32	A53SS_CORE1_PMU_PMPIDR6	0007 3012 0FD8h
FDCh	32	A53SS_CORE1_PMU_PMPIDR7	0007 3012 0FDCh
FE0h	32	A53SS_CORE1_PMU_PMPIDR0	0007 3012 0FE0h
FE4h	32	A53SS_CORE1_PMU_PMPIDR1	0007 3012 0FE4h
FE8h	32	A53SS_CORE1_PMU_PMPIDR2	0007 3012 0FE8h
FECh	32	A53SS_CORE1_PMU_PMPIDR3	0007 3012 0FECh
FF0h	32	A53SS_CORE1_PMU_PMCIDR0	0007 3012 0FF0h
FF4h	32	A53SS_CORE1_PMU_PMCIDR1	0007 3012 0FF4h
FF8h	32	A53SS_CORE1_PMU_PMCIDR2	0007 3012 0FF8h

Table 14-12415. A53SS_CORE1_PMU Registers, Base Address=0007 3012 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FFCh	32	A53SS_CORE1_PMU_PMCIDR3	0007 3012 0FFCh

Table 14-12416. A53SS_CORE1_ETM Registers, Base Address=0007 3013 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_CORE1_ETM_TRCPRGCTLR	0007 3013 0004h
Ch	32	A53SS_CORE1_ETM_TRCSTATR	0007 3013 000Ch
10h	32	A53SS_CORE1_ETM_TRCCONFIGR	0007 3013 0010h
18h	32	A53SS_CORE1_ETM_TRCAUXCTLR	0007 3013 0018h
20h	32	A53SS_CORE1_ETM_TRCEVENTCTL0R	0007 3013 0020h
24h	32	A53SS_CORE1_ETM_TRCEVENTCTL1R	0007 3013 0024h
2Ch	32	A53SS_CORE1_ETM_TRCSTALLCTLR	0007 3013 002Ch
30h	32	A53SS_CORE1_ETM_TRCTSCTLR	0007 3013 0030h
34h	32	A53SS_CORE1_ETM_TRCSYNCPR	0007 3013 0034h
38h	32	A53SS_CORE1_ETM_TRCCCCTLR	0007 3013 0038h
3Ch	32	A53SS_CORE1_ETM_TRCBBCTLR	0007 3013 003Ch
40h	32	A53SS_CORE1_ETM_TRCTRACEIDR	0007 3013 0040h
80h	32	A53SS_CORE1_ETM_TRCVICTLR	0007 3013 0080h
84h	32	A53SS_CORE1_ETM_TRCVIIECTLR	0007 3013 0084h
88h	32	A53SS_CORE1_ETM_TRCVISSCTLR	0007 3013 0088h
100h	32	A53SS_CORE1_ETM_TRCSEQEVR0	0007 3013 0100h
104h	32	A53SS_CORE1_ETM_TRCSEQEVR1	0007 3013 0104h
108h	32	A53SS_CORE1_ETM_TRCSEQEVR2	0007 3013 0108h
118h	32	A53SS_CORE1_ETM_TRCSEQRSTEVR	0007 3013 0118h
11Ch	32	A53SS_CORE1_ETM_TRCSEQSTR	0007 3013 011Ch
120h	32	A53SS_CORE1_ETM_TRCEXTINSELR	0007 3013 0120h
140h	32	A53SS_CORE1_ETM_TRCCNTRLDVR0	0007 3013 0140h
144h	32	A53SS_CORE1_ETM_TRCCNTRLDVR1	0007 3013 0144h
150h	32	A53SS_CORE1_ETM_TRCCNTCTLR0	0007 3013 0150h
154h	32	A53SS_CORE1_ETM_TRCCNTCTLR1	0007 3013 0154h
160h	32	A53SS_CORE1_ETM_TRCCNTVR0	0007 3013 0160h
164h	32	A53SS_CORE1_ETM_TRCCNTVR1	0007 3013 0164h
180h	32	A53SS_CORE1_ETM_TRCIDR8	0007 3013 0180h
184h	32	A53SS_CORE1_ETM_TRCIDR9	0007 3013 0184h
188h	32	A53SS_CORE1_ETM_TRCIDR10	0007 3013 0188h
18Ch	32	A53SS_CORE1_ETM_TRCIDR11	0007 3013 018Ch
190h	32	A53SS_CORE1_ETM_TRCIDR12	0007 3013 0190h
194h	32	A53SS_CORE1_ETM_TRCIDR13	0007 3013 0194h
1C0h	32	A53SS_CORE1_ETM_TRCIMSPEC0	0007 3013 01C0h
1E0h	32	A53SS_CORE1_ETM_TRCIDR0	0007 3013 01E0h
1E4h	32	A53SS_CORE1_ETM_TRCIDR1	0007 3013 01E4h
1E8h	32	A53SS_CORE1_ETM_TRCIDR2	0007 3013 01E8h
1ECh	32	A53SS_CORE1_ETM_TRCIDR3	0007 3013 01ECh
1F0h	32	A53SS_CORE1_ETM_TRCIDR4	0007 3013 01F0h
1F4h	32	A53SS_CORE1_ETM_TRCIDR5	0007 3013 01F4h

Table 14-12416. A53SS_CORE1_ETM Registers, Base Address=0007 3013 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
208h	32	A53SS_CORE1_ETM_TRCRSCTLR2	0007 3013 0208h
20Ch	32	A53SS_CORE1_ETM_TRCRSCTLR3	0007 3013 020Ch
210h	32	A53SS_CORE1_ETM_TRCRSCTLR4	0007 3013 0210h
214h	32	A53SS_CORE1_ETM_TRCRSCTLR5	0007 3013 0214h
218h	32	A53SS_CORE1_ETM_TRCRSCTLR6	0007 3013 0218h
21Ch	32	A53SS_CORE1_ETM_TRCRSCTLR7	0007 3013 021Ch
220h	32	A53SS_CORE1_ETM_TRCRSCTLR8	0007 3013 0220h
224h	32	A53SS_CORE1_ETM_TRCRSCTLR9	0007 3013 0224h
228h	32	A53SS_CORE1_ETM_TRCRSCTLR10	0007 3013 0228h
22Ch	32	A53SS_CORE1_ETM_TRCRSCTLR11	0007 3013 022Ch
230h	32	A53SS_CORE1_ETM_TRCRSCTLR12	0007 3013 0230h
234h	32	A53SS_CORE1_ETM_TRCRSCTLR13	0007 3013 0234h
238h	32	A53SS_CORE1_ETM_TRCRSCTLR14	0007 3013 0238h
23Ch	32	A53SS_CORE1_ETM_TRCRSCTLR15	0007 3013 023Ch
280h	32	A53SS_CORE1_ETM_TRCSSCCR0	0007 3013 0280h
2A0h	32	A53SS_CORE1_ETM_TRCSSCSR0	0007 3013 02A0h
300h	32	A53SS_CORE1_ETM_TRCOSLAR	0007 3013 0300h
304h	32	A53SS_CORE1_ETM_TRCOSLSR	0007 3013 0304h
310h	32	A53SS_CORE1_ETM_TRCPDCR	0007 3013 0310h
314h	32	A53SS_CORE1_ETM_TRCPDSR	0007 3013 0314h
400h	32	A53SS_CORE1_ETM_TRCACVR0_31_0	0007 3013 0400h
404h	32	A53SS_CORE1_ETM_TRCACVR0_63_32	0007 3013 0404h
408h	32	A53SS_CORE1_ETM_TRCACVR1_31_0	0007 3013 0408h
40Ch	32	A53SS_CORE1_ETM_TRCACVR1_63_32	0007 3013 040Ch
410h	32	A53SS_CORE1_ETM_TRCACVR2_31_0	0007 3013 0410h
414h	32	A53SS_CORE1_ETM_TRCACVR2_63_32	0007 3013 0414h
418h	32	A53SS_CORE1_ETM_TRCACVR3_31_0	0007 3013 0418h
41Ch	32	A53SS_CORE1_ETM_TRCACVR3_63_32	0007 3013 041Ch
420h	32	A53SS_CORE1_ETM_TRCACVR4_31_0	0007 3013 0420h
424h	32	A53SS_CORE1_ETM_TRCACVR4_63_32	0007 3013 0424h
428h	32	A53SS_CORE1_ETM_TRCACVR5_31_0	0007 3013 0428h
42Ch	32	A53SS_CORE1_ETM_TRCACVR5_63_32	0007 3013 042Ch
430h	32	A53SS_CORE1_ETM_TRCACVR6_31_0	0007 3013 0430h
434h	32	A53SS_CORE1_ETM_TRCACVR6_63_32	0007 3013 0434h
438h	32	A53SS_CORE1_ETM_TRCACVR7_31_0	0007 3013 0438h
43Ch	32	A53SS_CORE1_ETM_TRCACVR7_63_32	0007 3013 043Ch
480h	32	A53SS_CORE1_ETM_TRCACATR0	0007 3013 0480h
488h	32	A53SS_CORE1_ETM_TRCACATR1	0007 3013 0488h
490h	32	A53SS_CORE1_ETM_TRCACATR2	0007 3013 0490h
498h	32	A53SS_CORE1_ETM_TRCACATR3	0007 3013 0498h
4A0h	32	A53SS_CORE1_ETM_TRCACATR4	0007 3013 04A0h
4A8h	32	A53SS_CORE1_ETM_TRCACATR5	0007 3013 04A8h
4B0h	32	A53SS_CORE1_ETM_TRCACATR6	0007 3013 04B0h
4B8h	32	A53SS_CORE1_ETM_TRCACATR7	0007 3013 04B8h

Table 14-12416. A53SS_CORE1_ETM Registers, Base Address=0007 3013 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
600h	32	A53SS_CORE1_ETM_TRCCIDCVR0	0007 3013 0600h
640h	32	A53SS_CORE1_ETM_TRCVMIDCVR0	0007 3013 0640h
680h	32	A53SS_CORE1_ETM_TRCCIDCCTLR0	0007 3013 0680h
EE4h	32	A53SS_CORE1_ETM_TRCITATBIDR	0007 3013 0EE4h
EECh	32	A53SS_CORE1_ETM_TRCITIDATAR	0007 3013 0EECh
EF4h	32	A53SS_CORE1_ETM_TRCITIATBINR	0007 3013 0EF4h
EFCh	32	A53SS_CORE1_ETM_TRCITIATBOUTR	0007 3013 0EFCh
F00h	32	A53SS_CORE1_ETM_TRCITCTRL	0007 3013 0F00h
FA0h	32	A53SS_CORE1_ETM_TRCCLAIMSET	0007 3013 0FA0h
FA4h	32	A53SS_CORE1_ETM_TRCCLAIMCLR	0007 3013 0FA4h
FA8h	32	A53SS_CORE1_ETM_TRCDEVAFF0	0007 3013 0FA8h
FACh	32	A53SS_CORE1_ETM_TRCDEVAFF1	0007 3013 0FACh
FB0h	32	A53SS_CORE1_ETM_TRCLAR	0007 3013 0FB0h
FB4h	32	A53SS_CORE1_ETM_TRCLSR	0007 3013 0FB4h
FB8h	32	A53SS_CORE1_ETM_TRCAUTHSTATUS	0007 3013 0FB8h
FBCh	32	A53SS_CORE1_ETM_TRCDEVARCH	0007 3013 0FBCh
FC8h	32	A53SS_CORE1_ETM_TRCDEVID	0007 3013 0FC8h
FCCh	32	A53SS_CORE1_ETM_TRCDEVTYPE	0007 3013 0FCCh
FD0h	32	A53SS_CORE1_ETM_TRCPIDR4	0007 3013 0FD0h
FD4h	32	A53SS_CORE1_ETM_TRCPIDR5	0007 3013 0FD4h
FD8h	32	A53SS_CORE1_ETM_TRCPIDR6	0007 3013 0FD8h
FDCh	32	A53SS_CORE1_ETM_TRCPIDR7	0007 3013 0FDCh
FE0h	32	A53SS_CORE1_ETM_TRCPIDR0	0007 3013 0FE0h
FE4h	32	A53SS_CORE1_ETM_TRCPIDR1	0007 3013 0FE4h
FE8h	32	A53SS_CORE1_ETM_TRCPIDR2	0007 3013 0FE8h
FECh	32	A53SS_CORE1_ETM_TRCPIDR3	0007 3013 0FECh
FF0h	32	A53SS_CORE1_ETM_TRCCIDR0	0007 3013 0FF0h
FF4h	32	A53SS_CORE1_ETM_TRCCIDR1	0007 3013 0FF4h
FF8h	32	A53SS_CORE1_ETM_TRCCIDR2	0007 3013 0FF8h
FFCh	32	A53SS_CORE1_ETM_TRCCIDR3	0007 3013 0FFCh

Table 14-12417. A53SS_CORE1_CTI Registers, Base Address=0007 3014 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE1_CTI_CTICONTROL	0007 3014 0000h
10h	32	A53SS_CORE1_CTI_CTIINTACK	0007 3014 0010h
14h	32	A53SS_CORE1_CTI_CTIAPPSET	0007 3014 0014h
18h	32	A53SS_CORE1_CTI_CTIAPPCLEAR	0007 3014 0018h
1Ch	32	A53SS_CORE1_CTI_CTIAPPPULSE	0007 3014 001Ch
20h	32	A53SS_CORE1_CTI_CTIINEN0	0007 3014 0020h
24h	32	A53SS_CORE1_CTI_CTIINEN1	0007 3014 0024h
28h	32	A53SS_CORE1_CTI_CTIINEN2	0007 3014 0028h
2Ch	32	A53SS_CORE1_CTI_CTIINEN3	0007 3014 002Ch
30h	32	A53SS_CORE1_CTI_CTIINEN4	0007 3014 0030h
34h	32	A53SS_CORE1_CTI_CTIINEN5	0007 3014 0034h

Table 14-12417. A53SS_CORE1_CTI Registers, Base Address=0007 3014 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
38h	32	A53SS_CORE1_CTI_CTIINEN6	0007 3014 0038h
3Ch	32	A53SS_CORE1_CTI_CTIINEN7	0007 3014 003Ch
A0h	32	A53SS_CORE1_CTI_CTIOUTEN0	0007 3014 00A0h
A4h	32	A53SS_CORE1_CTI_CTIOUTEN1	0007 3014 00A4h
A8h	32	A53SS_CORE1_CTI_CTIOUTEN2	0007 3014 00A8h
ACh	32	A53SS_CORE1_CTI_CTIOUTEN3	0007 3014 00ACh
B0h	32	A53SS_CORE1_CTI_CTIOUTEN4	0007 3014 00B0h
B4h	32	A53SS_CORE1_CTI_CTIOUTEN5	0007 3014 00B4h
B8h	32	A53SS_CORE1_CTI_CTIOUTEN6	0007 3014 00B8h
BCh	32	A53SS_CORE1_CTI_CTIOUTEN7	0007 3014 00BCh
130h	32	A53SS_CORE1_CTI_CTITRIGINSTATUS	0007 3014 0130h
134h	32	A53SS_CORE1_CTI_CTITRIGOUTSTATUS	0007 3014 0134h
138h	32	A53SS_CORE1_CTI_CTICHINSTATUS	0007 3014 0138h
13Ch	32	A53SS_CORE1_CTI_CTICHOUTSTATUS	0007 3014 013Ch
140h	32	A53SS_CORE1_CTI_CTIGATE	0007 3014 0140h
144h	32	A53SS_CORE1_CTI_ASICCTL	0007 3014 0144h
F00h	32	A53SS_CORE1_CTI_CTIITCTRL	0007 3014 0F00h
FA0h	32	A53SS_CORE1_CTI_CTICLAIMSET	0007 3014 0FA0h
FA4h	32	A53SS_CORE1_CTI_CTICLAIMCLR	0007 3014 0FA4h
FA8h	32	A53SS_CORE1_CTI_CTIDEVAFF0	0007 3014 0FA8h
FACh	32	A53SS_CORE1_CTI_CTIDEVAFF1	0007 3014 0FACh
FB0h	32	A53SS_CORE1_CTI_CTILAR	0007 3014 0FB0h
FB4h	32	A53SS_CORE1_CTI_CTILSR	0007 3014 0FB4h
FB8h	32	A53SS_CORE1_CTI_CTIAUTHSTATUS	0007 3014 0FB8h
FBCh	32	A53SS_CORE1_CTI_CTIDEVARCH	0007 3014 0FBCh
FC0h	32	A53SS_CORE1_CTI_CTIDEVID2	0007 3014 0FC0h
FC4h	32	A53SS_CORE1_CTI_CTIDEVID1	0007 3014 0FC4h
FC8h	32	A53SS_CORE1_CTI_CTIDEVID	0007 3014 0FC8h
FCCh	32	A53SS_CORE1_CTI_CTIDEVTYPE	0007 3014 0FCCh
FD0h	32	A53SS_CORE1_CTI_CTIPIDR4	0007 3014 0FD0h
FD4h	32	A53SS_CORE1_CTI_CTIPIDR5	0007 3014 0FD4h
FD8h	32	A53SS_CORE1_CTI_CTIPIDR6	0007 3014 0FD8h
FDCh	32	A53SS_CORE1_CTI_CTIPIDR7	0007 3014 0FDCh
FE0h	32	A53SS_CORE1_CTI_CTIPIDR0	0007 3014 0FE0h
FE4h	32	A53SS_CORE1_CTI_CTIPIDR1	0007 3014 0FE4h
FE8h	32	A53SS_CORE1_CTI_CTIPIDR2	0007 3014 0FE8h
FECh	32	A53SS_CORE1_CTI_CTIPIDR3	0007 3014 0FECh
FF0h	32	A53SS_CORE1_CTI_CTICIDR0	0007 3014 0FF0h
FF4h	32	A53SS_CORE1_CTI_CTICIDR1	0007 3014 0FF4h
FF8h	32	A53SS_CORE1_CTI_CTICIDR2	0007 3014 0FF8h
FFCh	32	A53SS_CORE1_CTI_CTICIDR3	0007 3014 0FFCh

Table 14-12418. A53SS_CORE2_DBG Registers, Base Address=0007 3021 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_CORE2_DBG_EDESR	0007 3021 0020h
24h	32	A53SS_CORE2_DBG_EDECR	0007 3021 0024h
30h	32	A53SS_CORE2_DBG_EDWAR_31_0	0007 3021 0030h
34h	32	A53SS_CORE2_DBG_EDWAR_63_32	0007 3021 0034h
80h	32	A53SS_CORE2_DBG_DBGDTRRX_EL0	0007 3021 0080h
84h	32	A53SS_CORE2_DBG_EDITR	0007 3021 0084h
88h	32	A53SS_CORE2_DBG_EDSCR	0007 3021 0088h
8Ch	32	A53SS_CORE2_DBG_DBGDTRTX_EL0	0007 3021 008Ch
90h	32	A53SS_CORE2_DBG_EDRCR	0007 3021 0090h
94h	32	A53SS_CORE2_DBG_EDACR	0007 3021 0094h
98h	32	A53SS_CORE2_DBG_EDECCR	0007 3021 0098h
A0h	32	A53SS_CORE2_DBG_EDPCSR_31_0	0007 3021 00A0h
A4h	32	A53SS_CORE2_DBG_EDCIDSR	0007 3021 00A4h
A8h	32	A53SS_CORE2_DBG_EDVIDSR	0007 3021 00A8h
ACh	32	A53SS_CORE2_DBG_EDPCSR_63_32	0007 3021 00ACh
300h	32	A53SS_CORE2_DBG_OSLAR_EL1	0007 3021 0300h
310h	32	A53SS_CORE2_DBG_EDPRCR	0007 3021 0310h
314h	32	A53SS_CORE2_DBG_EDPRSR	0007 3021 0314h
400h	32	A53SS_CORE2_DBG_DBGBVR0_EL1_31_0	0007 3021 0400h
404h	32	A53SS_CORE2_DBG_DBGBVR0_EL1_63_32	0007 3021 0404h
408h	32	A53SS_CORE2_DBG_DBGBCR0_EL1	0007 3021 0408h
410h	32	A53SS_CORE2_DBG_DBGBVR1_EL1_31_0	0007 3021 0410h
414h	32	A53SS_CORE2_DBG_DBGBVR1_EL1_63_32	0007 3021 0414h
418h	32	A53SS_CORE2_DBG_DBGBCR1_EL1	0007 3021 0418h
420h	32	A53SS_CORE2_DBG_DBGBVR2_EL1_31_0	0007 3021 0420h
424h	32	A53SS_CORE2_DBG_DBGBVR2_EL1_63_32	0007 3021 0424h
428h	32	A53SS_CORE2_DBG_DBGBCR2_EL1	0007 3021 0428h
430h	32	A53SS_CORE2_DBG_DBGBVR3_EL1_31_0	0007 3021 0430h
434h	32	A53SS_CORE2_DBG_DBGBVR3_EL1_63_32	0007 3021 0434h
438h	32	A53SS_CORE2_DBG_DBGBCR3_EL1	0007 3021 0438h
440h	32	A53SS_CORE2_DBG_DBGBVR4_EL1_31_0	0007 3021 0440h
444h	32	A53SS_CORE2_DBG_DBGBVR4_EL1_63_32	0007 3021 0444h
448h	32	A53SS_CORE2_DBG_DBGBCR4_EL1	0007 3021 0448h
450h	32	A53SS_CORE2_DBG_DBGBVR5_EL1_31_0	0007 3021 0450h
454h	32	A53SS_CORE2_DBG_DBGBVR5_EL1_63_32	0007 3021 0454h
458h	32	A53SS_CORE2_DBG_DBGBCR5_EL1	0007 3021 0458h
800h	32	A53SS_CORE2_DBG_DBGWVR0_EL1_31_0	0007 3021 0800h
804h	32	A53SS_CORE2_DBG_DBGWVR0_EL1_63_32	0007 3021 0804h
808h	32	A53SS_CORE2_DBG_DBGWCR0_EL1	0007 3021 0808h
810h	32	A53SS_CORE2_DBG_DBGWVR1_EL1_31_0	0007 3021 0810h
814h	32	A53SS_CORE2_DBG_DBGWVR1_EL1_63_32	0007 3021 0814h
818h	32	A53SS_CORE2_DBG_DBGWCR1_EL1	0007 3021 0818h
820h	32	A53SS_CORE2_DBG_DBGWVR2_EL1_31_0	0007 3021 0820h
824h	32	A53SS_CORE2_DBG_DBGWVR2_EL1_63_32	0007 3021 0824h
828h	32	A53SS_CORE2_DBG_DBGWCR2_EL1	0007 3021 0828h

Table 14-12418. A53SS_CORE2_DBG Registers, Base Address=0007 3021 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
830h	32	A53SS_CORE2_DBG_DBGWVR3_EL1_31_0	0007 3021 0830h
834h	32	A53SS_CORE2_DBG_DBGWVR3_EL1_63_32	0007 3021 0834h
838h	32	A53SS_CORE2_DBG_DBGWCR3_EL1	0007 3021 0838h
D00h	32	A53SS_CORE2_DBG_MIDR_EL1	0007 3021 0D00h
D20h	32	A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0	0007 3021 0D20h
D24h	32	A53SS_CORE2_DBG_ID_AA64PFR0_EL1_63_32	0007 3021 0D24h
D28h	32	A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0	0007 3021 0D28h
D2Ch	32	A53SS_CORE2_DBG_ID_AA64DFR0_EL1_63_32	0007 3021 0D2Ch
D30h	32	A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0	0007 3021 0D30h
D34h	32	A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_63_32	0007 3021 0D34h
D38h	32	A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0	0007 3021 0D38h
D3Ch	32	A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_63_32	0007 3021 0D3Ch
D40h	32	A53SS_CORE2_DBG_ID_AA64PFR1_EL1_31_0	0007 3021 0D40h
D44h	32	A53SS_CORE2_DBG_ID_AA64PFR1_EL1_63_32	0007 3021 0D44h
D48h	32	A53SS_CORE2_DBG_ID_AA64DFR1_EL1_31_0	0007 3021 0D48h
D4Ch	32	A53SS_CORE2_DBG_ID_AA64DFR1_EL1_63_32	0007 3021 0D4Ch
D50h	32	A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_31_0	0007 3021 0D50h
D54h	32	A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_63_32	0007 3021 0D54h
D58h	32	A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_31_0	0007 3021 0D58h
D5Ch	32	A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_63_32	0007 3021 0D5Ch
F00h	32	A53SS_CORE2_DBG_EDITCTRL	0007 3021 0F00h
FA0h	32	A53SS_CORE2_DBG_DBGCLAIMSET_EL1	0007 3021 0FA0h
FA4h	32	A53SS_CORE2_DBG_DBGCLAIMCLR_EL1	0007 3021 0FA4h
FA8h	32	A53SS_CORE2_DBG_EDDEVAFF0	0007 3021 0FA8h
FACh	32	A53SS_CORE2_DBG_EDDEVAFF1	0007 3021 0FACh
FB0h	32	A53SS_CORE2_DBG_EDLAR	0007 3021 0FB0h
FB4h	32	A53SS_CORE2_DBG_EDLSR	0007 3021 0FB4h
FB8h	32	A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1	0007 3021 0FB8h
FBCh	32	A53SS_CORE2_DBG_EDDEVARCH	0007 3021 0FBCh
FC0h	32	A53SS_CORE2_DBG_EDDEVID2	0007 3021 0FC0h
FC4h	32	A53SS_CORE2_DBG_EDDEVID1	0007 3021 0FC4h
FC8h	32	A53SS_CORE2_DBG_EDDEVID	0007 3021 0FC8h
FCCh	32	A53SS_CORE2_DBG_EDDEVTYPE	0007 3021 0FCCh
FD0h	32	A53SS_CORE2_DBG_EDPIDR4	0007 3021 0FD0h
FE0h	32	A53SS_CORE2_DBG_EDPIDR0	0007 3021 0FE0h
FE4h	32	A53SS_CORE2_DBG_EDPIDR1	0007 3021 0FE4h
FE8h	32	A53SS_CORE2_DBG_EDPIDR2	0007 3021 0FE8h
FECh	32	A53SS_CORE2_DBG_EDPIDR3	0007 3021 0FECh
FF0h	32	A53SS_CORE2_DBG_EDCIDR0	0007 3021 0FF0h
FF4h	32	A53SS_CORE2_DBG_EDCIDR1	0007 3021 0FF4h
FF8h	32	A53SS_CORE2_DBG_EDCIDR2	0007 3021 0FF8h
FFCh	32	A53SS_CORE2_DBG_EDCIDR3	0007 3021 0FFCh

Table 14-12419. A53SS_CORE2_PMU Registers, Base Address=0007 3022 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE2_PMU_PMEVCNTR0_EL0	0007 3022 0000h
8h	32	A53SS_CORE2_PMU_PMEVCNTR1_EL0	0007 3022 0008h
10h	32	A53SS_CORE2_PMU_PMEVCNTR2_EL0	0007 3022 0010h
18h	32	A53SS_CORE2_PMU_PMEVCNTR3_EL0	0007 3022 0018h
20h	32	A53SS_CORE2_PMU_PMEVCNTR4_EL0	0007 3022 0020h
28h	32	A53SS_CORE2_PMU_PMEVCNTR5_EL0	0007 3022 0028h
F8h	32	A53SS_CORE2_PMU_PMCCNTR_EL0_31_0	0007 3022 00F8h
FCh	32	A53SS_CORE2_PMU_PMCCNTR_EL0_63_32	0007 3022 00FCh
400h	32	A53SS_CORE2_PMU_PMEVTYPER0_EL0	0007 3022 0400h
404h	32	A53SS_CORE2_PMU_PMEVTYPER1_EL0	0007 3022 0404h
408h	32	A53SS_CORE2_PMU_PMEVTYPER2_EL0	0007 3022 0408h
40Ch	32	A53SS_CORE2_PMU_PMEVTYPER3_EL0	0007 3022 040Ch
410h	32	A53SS_CORE2_PMU_PMEVTYPER4_EL0	0007 3022 0410h
414h	32	A53SS_CORE2_PMU_PMEVTYPER5_EL0	0007 3022 0414h
47Ch	32	A53SS_CORE2_PMU_PMCCFILTR_EL0	0007 3022 047Ch
C00h	32	A53SS_CORE2_PMU_PMCNTENSET_EL0	0007 3022 0C00h
C20h	32	A53SS_CORE2_PMU_PMCNTENCLR_EL0	0007 3022 0C20h
C40h	32	A53SS_CORE2_PMU_PMINTENSET_EL1	0007 3022 0C40h
C60h	32	A53SS_CORE2_PMU_PMINTENCLR_EL1	0007 3022 0C60h
C80h	32	A53SS_CORE2_PMU_PMOVSCLR_EL0	0007 3022 0C80h
CA0h	32	A53SS_CORE2_PMU_PMSWINC_EL0	0007 3022 0CA0h
CC0h	32	A53SS_CORE2_PMU_PMOVSSET_EL0	0007 3022 0CC0h
E00h	32	A53SS_CORE2_PMU_PMCFGR	0007 3022 0E00h
E04h	32	A53SS_CORE2_PMU_PMCR_EL0	0007 3022 0E04h
E20h	32	A53SS_CORE2_PMU_PMCEID0_EL0	0007 3022 0E20h
E24h	32	A53SS_CORE2_PMU_PMCEID1_EL0	0007 3022 0E24h
F00h	32	A53SS_CORE2_PMU_PMITCTRL	0007 3022 0F00h
FA8h	32	A53SS_CORE2_PMU_PMDEVAFF0	0007 3022 0FA8h
FACh	32	A53SS_CORE2_PMU_PMDEVAFF1	0007 3022 0FACh
FB0h	32	A53SS_CORE2_PMU_PMLAR	0007 3022 0FB0h
FB4h	32	A53SS_CORE2_PMU_PMLSR	0007 3022 0FB4h
FB8h	32	A53SS_CORE2_PMU_PMAUTHSTATUS	0007 3022 0FB8h
FBCh	32	A53SS_CORE2_PMU_PMDEVARCH	0007 3022 0FBCh
FCCh	32	A53SS_CORE2_PMU_PMDEVTYPE	0007 3022 0FCCh
FD0h	32	A53SS_CORE2_PMU_PMPIDR4	0007 3022 0FD0h
FD4h	32	A53SS_CORE2_PMU_PMPIDR5	0007 3022 0FD4h
FD8h	32	A53SS_CORE2_PMU_PMPIDR6	0007 3022 0FD8h
FDCh	32	A53SS_CORE2_PMU_PMPIDR7	0007 3022 0FDCh
FE0h	32	A53SS_CORE2_PMU_PMPIDR0	0007 3022 0FE0h
FE4h	32	A53SS_CORE2_PMU_PMPIDR1	0007 3022 0FE4h
FE8h	32	A53SS_CORE2_PMU_PMPIDR2	0007 3022 0FE8h
FECh	32	A53SS_CORE2_PMU_PMPIDR3	0007 3022 0FECh
FF0h	32	A53SS_CORE2_PMU_PMCIDR0	0007 3022 0FF0h
FF4h	32	A53SS_CORE2_PMU_PMCIDR1	0007 3022 0FF4h
FF8h	32	A53SS_CORE2_PMU_PMCIDR2	0007 3022 0FF8h

Table 14-12419. A53SS_CORE2_PMU Registers, Base Address=0007 3022 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FFCh	32	A53SS_CORE2_PMU_PMCIDR3	0007 3022 0FFCh

Table 14-12420. A53SS_CORE2_ETM Registers, Base Address=0007 3023 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_CORE2_ETM_TRCPRGCTLR	0007 3023 0004h
Ch	32	A53SS_CORE2_ETM_TRCSTATR	0007 3023 000Ch
10h	32	A53SS_CORE2_ETM_TRCCONFIGR	0007 3023 0010h
18h	32	A53SS_CORE2_ETM_TRCAUXCTLR	0007 3023 0018h
20h	32	A53SS_CORE2_ETM_TRCEVENTCTL0R	0007 3023 0020h
24h	32	A53SS_CORE2_ETM_TRCEVENTCTL1R	0007 3023 0024h
2Ch	32	A53SS_CORE2_ETM_TRCSTALLCTLR	0007 3023 002Ch
30h	32	A53SS_CORE2_ETM_TRCTSCTLR	0007 3023 0030h
34h	32	A53SS_CORE2_ETM_TRCSYNCPR	0007 3023 0034h
38h	32	A53SS_CORE2_ETM_TRCCCCTLR	0007 3023 0038h
3Ch	32	A53SS_CORE2_ETM_TRCBBCTLR	0007 3023 003Ch
40h	32	A53SS_CORE2_ETM_TRCTRACEIDR	0007 3023 0040h
80h	32	A53SS_CORE2_ETM_TRCVICTLR	0007 3023 0080h
84h	32	A53SS_CORE2_ETM_TRCVIIECTLR	0007 3023 0084h
88h	32	A53SS_CORE2_ETM_TRCVISSCTLR	0007 3023 0088h
100h	32	A53SS_CORE2_ETM_TRCSEQEVR0	0007 3023 0100h
104h	32	A53SS_CORE2_ETM_TRCSEQEVR1	0007 3023 0104h
108h	32	A53SS_CORE2_ETM_TRCSEQEVR2	0007 3023 0108h
118h	32	A53SS_CORE2_ETM_TRCSEQRSTEVR	0007 3023 0118h
11Ch	32	A53SS_CORE2_ETM_TRCSEQSTR	0007 3023 011Ch
120h	32	A53SS_CORE2_ETM_TRCEXTINSELR	0007 3023 0120h
140h	32	A53SS_CORE2_ETM_TRCCNTRLDVR0	0007 3023 0140h
144h	32	A53SS_CORE2_ETM_TRCCNTRLDVR1	0007 3023 0144h
150h	32	A53SS_CORE2_ETM_TRCCNTCTLR0	0007 3023 0150h
154h	32	A53SS_CORE2_ETM_TRCCNTCTLR1	0007 3023 0154h
160h	32	A53SS_CORE2_ETM_TRCCNTVR0	0007 3023 0160h
164h	32	A53SS_CORE2_ETM_TRCCNTVR1	0007 3023 0164h
180h	32	A53SS_CORE2_ETM_TRCIDR8	0007 3023 0180h
184h	32	A53SS_CORE2_ETM_TRCIDR9	0007 3023 0184h
188h	32	A53SS_CORE2_ETM_TRCIDR10	0007 3023 0188h
18Ch	32	A53SS_CORE2_ETM_TRCIDR11	0007 3023 018Ch
190h	32	A53SS_CORE2_ETM_TRCIDR12	0007 3023 0190h
194h	32	A53SS_CORE2_ETM_TRCIDR13	0007 3023 0194h
1C0h	32	A53SS_CORE2_ETM_TRCIMSPEC0	0007 3023 01C0h
1E0h	32	A53SS_CORE2_ETM_TRCIDR0	0007 3023 01E0h
1E4h	32	A53SS_CORE2_ETM_TRCIDR1	0007 3023 01E4h
1E8h	32	A53SS_CORE2_ETM_TRCIDR2	0007 3023 01E8h
1ECh	32	A53SS_CORE2_ETM_TRCIDR3	0007 3023 01ECh
1F0h	32	A53SS_CORE2_ETM_TRCIDR4	0007 3023 01F0h
1F4h	32	A53SS_CORE2_ETM_TRCIDR5	0007 3023 01F4h

Table 14-12420. A53SS_CORE2_ETM Registers, Base Address=0007 3023 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
208h	32	A53SS_CORE2_ETM_TRCRSCTLR2	0007 3023 0208h
20Ch	32	A53SS_CORE2_ETM_TRCRSCTLR3	0007 3023 020Ch
210h	32	A53SS_CORE2_ETM_TRCRSCTLR4	0007 3023 0210h
214h	32	A53SS_CORE2_ETM_TRCRSCTLR5	0007 3023 0214h
218h	32	A53SS_CORE2_ETM_TRCRSCTLR6	0007 3023 0218h
21Ch	32	A53SS_CORE2_ETM_TRCRSCTLR7	0007 3023 021Ch
220h	32	A53SS_CORE2_ETM_TRCRSCTLR8	0007 3023 0220h
224h	32	A53SS_CORE2_ETM_TRCRSCTLR9	0007 3023 0224h
228h	32	A53SS_CORE2_ETM_TRCRSCTLR10	0007 3023 0228h
22Ch	32	A53SS_CORE2_ETM_TRCRSCTLR11	0007 3023 022Ch
230h	32	A53SS_CORE2_ETM_TRCRSCTLR12	0007 3023 0230h
234h	32	A53SS_CORE2_ETM_TRCRSCTLR13	0007 3023 0234h
238h	32	A53SS_CORE2_ETM_TRCRSCTLR14	0007 3023 0238h
23Ch	32	A53SS_CORE2_ETM_TRCRSCTLR15	0007 3023 023Ch
280h	32	A53SS_CORE2_ETM_TRCSSCCR0	0007 3023 0280h
2A0h	32	A53SS_CORE2_ETM_TRCSSCSR0	0007 3023 02A0h
300h	32	A53SS_CORE2_ETM_TRCOSLAR	0007 3023 0300h
304h	32	A53SS_CORE2_ETM_TRCOSLSR	0007 3023 0304h
310h	32	A53SS_CORE2_ETM_TRCPDCR	0007 3023 0310h
314h	32	A53SS_CORE2_ETM_TRCPDSR	0007 3023 0314h
400h	32	A53SS_CORE2_ETM_TRCACVR0_31_0	0007 3023 0400h
404h	32	A53SS_CORE2_ETM_TRCACVR0_63_32	0007 3023 0404h
408h	32	A53SS_CORE2_ETM_TRCACVR1_31_0	0007 3023 0408h
40Ch	32	A53SS_CORE2_ETM_TRCACVR1_63_32	0007 3023 040Ch
410h	32	A53SS_CORE2_ETM_TRCACVR2_31_0	0007 3023 0410h
414h	32	A53SS_CORE2_ETM_TRCACVR2_63_32	0007 3023 0414h
418h	32	A53SS_CORE2_ETM_TRCACVR3_31_0	0007 3023 0418h
41Ch	32	A53SS_CORE2_ETM_TRCACVR3_63_32	0007 3023 041Ch
420h	32	A53SS_CORE2_ETM_TRCACVR4_31_0	0007 3023 0420h
424h	32	A53SS_CORE2_ETM_TRCACVR4_63_32	0007 3023 0424h
428h	32	A53SS_CORE2_ETM_TRCACVR5_31_0	0007 3023 0428h
42Ch	32	A53SS_CORE2_ETM_TRCACVR5_63_32	0007 3023 042Ch
430h	32	A53SS_CORE2_ETM_TRCACVR6_31_0	0007 3023 0430h
434h	32	A53SS_CORE2_ETM_TRCACVR6_63_32	0007 3023 0434h
438h	32	A53SS_CORE2_ETM_TRCACVR7_31_0	0007 3023 0438h
43Ch	32	A53SS_CORE2_ETM_TRCACVR7_63_32	0007 3023 043Ch
480h	32	A53SS_CORE2_ETM_TRCACATR0	0007 3023 0480h
488h	32	A53SS_CORE2_ETM_TRCACATR1	0007 3023 0488h
490h	32	A53SS_CORE2_ETM_TRCACATR2	0007 3023 0490h
498h	32	A53SS_CORE2_ETM_TRCACATR3	0007 3023 0498h
4A0h	32	A53SS_CORE2_ETM_TRCACATR4	0007 3023 04A0h
4A8h	32	A53SS_CORE2_ETM_TRCACATR5	0007 3023 04A8h
4B0h	32	A53SS_CORE2_ETM_TRCACATR6	0007 3023 04B0h
4B8h	32	A53SS_CORE2_ETM_TRCACATR7	0007 3023 04B8h

Table 14-12420. A53SS_CORE2_ETM Registers, Base Address=0007 3023 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
600h	32	A53SS_CORE2_ETM_TRCCIDCVR0	0007 3023 0600h
640h	32	A53SS_CORE2_ETM_TRCVMIDCVR0	0007 3023 0640h
680h	32	A53SS_CORE2_ETM_TRCCIDCCTLR0	0007 3023 0680h
EE4h	32	A53SS_CORE2_ETM_TRCITATBIDR	0007 3023 0EE4h
EECh	32	A53SS_CORE2_ETM_TRCITIDATAR	0007 3023 0EECh
EF4h	32	A53SS_CORE2_ETM_TRCITIATBINR	0007 3023 0EF4h
EFCh	32	A53SS_CORE2_ETM_TRCITIATBOUTR	0007 3023 0EFCh
F00h	32	A53SS_CORE2_ETM_TRCITCTRL	0007 3023 0F00h
FA0h	32	A53SS_CORE2_ETM_TRCCLAIMSET	0007 3023 0FA0h
FA4h	32	A53SS_CORE2_ETM_TRCCLAIMCLR	0007 3023 0FA4h
FA8h	32	A53SS_CORE2_ETM_TRCDEVAFF0	0007 3023 0FA8h
FACh	32	A53SS_CORE2_ETM_TRCDEVAFF1	0007 3023 0FACh
FB0h	32	A53SS_CORE2_ETM_TRCLAR	0007 3023 0FB0h
FB4h	32	A53SS_CORE2_ETM_TRCLSR	0007 3023 0FB4h
FB8h	32	A53SS_CORE2_ETM_TRCAUTHSTATUS	0007 3023 0FB8h
FBCh	32	A53SS_CORE2_ETM_TRCDEVARCH	0007 3023 0FBCh
FC8h	32	A53SS_CORE2_ETM_TRCDEVID	0007 3023 0FC8h
FCCh	32	A53SS_CORE2_ETM_TRCDEVTYPE	0007 3023 0FCCh
FD0h	32	A53SS_CORE2_ETM_TRCPIDR4	0007 3023 0FD0h
FD4h	32	A53SS_CORE2_ETM_TRCPIDR5	0007 3023 0FD4h
FD8h	32	A53SS_CORE2_ETM_TRCPIDR6	0007 3023 0FD8h
FDCh	32	A53SS_CORE2_ETM_TRCPIDR7	0007 3023 0FDCh
FE0h	32	A53SS_CORE2_ETM_TRCPIDR0	0007 3023 0FE0h
FE4h	32	A53SS_CORE2_ETM_TRCPIDR1	0007 3023 0FE4h
FE8h	32	A53SS_CORE2_ETM_TRCPIDR2	0007 3023 0FE8h
FECh	32	A53SS_CORE2_ETM_TRCPIDR3	0007 3023 0FECh
FF0h	32	A53SS_CORE2_ETM_TRCCIDR0	0007 3023 0FF0h
FF4h	32	A53SS_CORE2_ETM_TRCCIDR1	0007 3023 0FF4h
FF8h	32	A53SS_CORE2_ETM_TRCCIDR2	0007 3023 0FF8h
FFCh	32	A53SS_CORE2_ETM_TRCCIDR3	0007 3023 0FFCh

Table 14-12421. A53SS_CORE2_CTI Registers, Base Address=0007 3024 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE2_CTI_CTICONTROL	0007 3024 0000h
10h	32	A53SS_CORE2_CTI_CTIINTACK	0007 3024 0010h
14h	32	A53SS_CORE2_CTI_CTIAPPSET	0007 3024 0014h
18h	32	A53SS_CORE2_CTI_CTIAPPCLEAR	0007 3024 0018h
1Ch	32	A53SS_CORE2_CTI_CTIAPPPULSE	0007 3024 001Ch
20h	32	A53SS_CORE2_CTI_CTIINEN0	0007 3024 0020h
24h	32	A53SS_CORE2_CTI_CTIINEN1	0007 3024 0024h
28h	32	A53SS_CORE2_CTI_CTIINEN2	0007 3024 0028h
2Ch	32	A53SS_CORE2_CTI_CTIINEN3	0007 3024 002Ch
30h	32	A53SS_CORE2_CTI_CTIINEN4	0007 3024 0030h
34h	32	A53SS_CORE2_CTI_CTIINEN5	0007 3024 0034h

Table 14-12421. A53SS_CORE2_CTI Registers, Base Address=0007 3024 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
38h	32	A53SS_CORE2_CTI_CTIINEN6	0007 3024 0038h
3Ch	32	A53SS_CORE2_CTI_CTIINEN7	0007 3024 003Ch
A0h	32	A53SS_CORE2_CTI_CTIOUTEN0	0007 3024 00A0h
A4h	32	A53SS_CORE2_CTI_CTIOUTEN1	0007 3024 00A4h
A8h	32	A53SS_CORE2_CTI_CTIOUTEN2	0007 3024 00A8h
ACh	32	A53SS_CORE2_CTI_CTIOUTEN3	0007 3024 00ACh
B0h	32	A53SS_CORE2_CTI_CTIOUTEN4	0007 3024 00B0h
B4h	32	A53SS_CORE2_CTI_CTIOUTEN5	0007 3024 00B4h
B8h	32	A53SS_CORE2_CTI_CTIOUTEN6	0007 3024 00B8h
BCh	32	A53SS_CORE2_CTI_CTIOUTEN7	0007 3024 00BCh
130h	32	A53SS_CORE2_CTI_CTITRIGINSTATUS	0007 3024 0130h
134h	32	A53SS_CORE2_CTI_CTITRIGOUTSTATUS	0007 3024 0134h
138h	32	A53SS_CORE2_CTI_CTICHINSTATUS	0007 3024 0138h
13Ch	32	A53SS_CORE2_CTI_CTICHOUTSTATUS	0007 3024 013Ch
140h	32	A53SS_CORE2_CTI_CTIGATE	0007 3024 0140h
144h	32	A53SS_CORE2_CTI_ASICCTL	0007 3024 0144h
F00h	32	A53SS_CORE2_CTI_CTIITCTRL	0007 3024 0F00h
FA0h	32	A53SS_CORE2_CTI_CTICLAIMSET	0007 3024 0FA0h
FA4h	32	A53SS_CORE2_CTI_CTICLAIMCLR	0007 3024 0FA4h
FA8h	32	A53SS_CORE2_CTI_CTIDEVAFF0	0007 3024 0FA8h
FACh	32	A53SS_CORE2_CTI_CTIDEVAFF1	0007 3024 0FACh
FB0h	32	A53SS_CORE2_CTI_CTILAR	0007 3024 0FB0h
FB4h	32	A53SS_CORE2_CTI_CTILSR	0007 3024 0FB4h
FB8h	32	A53SS_CORE2_CTI_CTIAUTHSTATUS	0007 3024 0FB8h
FBCh	32	A53SS_CORE2_CTI_CTIDEVARCH	0007 3024 0FBCh
FC0h	32	A53SS_CORE2_CTI_CTIDEVID2	0007 3024 0FC0h
FC4h	32	A53SS_CORE2_CTI_CTIDEVID1	0007 3024 0FC4h
FC8h	32	A53SS_CORE2_CTI_CTIDEVID	0007 3024 0FC8h
FCCh	32	A53SS_CORE2_CTI_CTIDEVTYPE	0007 3024 0FCCh
FD0h	32	A53SS_CORE2_CTI_CTIPIDR4	0007 3024 0FD0h
FD4h	32	A53SS_CORE2_CTI_CTIPIDR5	0007 3024 0FD4h
FD8h	32	A53SS_CORE2_CTI_CTIPIDR6	0007 3024 0FD8h
FDCh	32	A53SS_CORE2_CTI_CTIPIDR7	0007 3024 0FDCh
FE0h	32	A53SS_CORE2_CTI_CTIPIDR0	0007 3024 0FE0h
FE4h	32	A53SS_CORE2_CTI_CTIPIDR1	0007 3024 0FE4h
FE8h	32	A53SS_CORE2_CTI_CTIPIDR2	0007 3024 0FE8h
FECh	32	A53SS_CORE2_CTI_CTIPIDR3	0007 3024 0FECh
FF0h	32	A53SS_CORE2_CTI_CTICIDR0	0007 3024 0FF0h
FF4h	32	A53SS_CORE2_CTI_CTICIDR1	0007 3024 0FF4h
FF8h	32	A53SS_CORE2_CTI_CTICIDR2	0007 3024 0FF8h
FFCh	32	A53SS_CORE2_CTI_CTICIDR3	0007 3024 0FFCh

Table 14-12422. A53SS_CORE3_DBG Registers, Base Address=0007 3031 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_CORE3_DBG_EDESR	0007 3031 0020h
24h	32	A53SS_CORE3_DBG_EDECR	0007 3031 0024h
30h	32	A53SS_CORE3_DBG_EDWAR_31_0	0007 3031 0030h
34h	32	A53SS_CORE3_DBG_EDWAR_63_32	0007 3031 0034h
80h	32	A53SS_CORE3_DBG_DBGDTRRX_EL0	0007 3031 0080h
84h	32	A53SS_CORE3_DBG_EDITR	0007 3031 0084h
88h	32	A53SS_CORE3_DBG_EDSCR	0007 3031 0088h
8Ch	32	A53SS_CORE3_DBG_DBGDTRTX_EL0	0007 3031 008Ch
90h	32	A53SS_CORE3_DBG_EDRCR	0007 3031 0090h
94h	32	A53SS_CORE3_DBG_EDACR	0007 3031 0094h
98h	32	A53SS_CORE3_DBG_EDECCR	0007 3031 0098h
A0h	32	A53SS_CORE3_DBG_EDPCSR_31_0	0007 3031 00A0h
A4h	32	A53SS_CORE3_DBG_EDCIDSR	0007 3031 00A4h
A8h	32	A53SS_CORE3_DBG_EDVIDSR	0007 3031 00A8h
ACh	32	A53SS_CORE3_DBG_EDPCSR_63_32	0007 3031 00ACh
300h	32	A53SS_CORE3_DBG_OSLAR_EL1	0007 3031 0300h
310h	32	A53SS_CORE3_DBG_EDPRCR	0007 3031 0310h
314h	32	A53SS_CORE3_DBG_EDPRSR	0007 3031 0314h
400h	32	A53SS_CORE3_DBG_DBGBVR0_EL1_31_0	0007 3031 0400h
404h	32	A53SS_CORE3_DBG_DBGBVR0_EL1_63_32	0007 3031 0404h
408h	32	A53SS_CORE3_DBG_DBGBCR0_EL1	0007 3031 0408h
410h	32	A53SS_CORE3_DBG_DBGBVR1_EL1_31_0	0007 3031 0410h
414h	32	A53SS_CORE3_DBG_DBGBVR1_EL1_63_32	0007 3031 0414h
418h	32	A53SS_CORE3_DBG_DBGBCR1_EL1	0007 3031 0418h
420h	32	A53SS_CORE3_DBG_DBGBVR2_EL1_31_0	0007 3031 0420h
424h	32	A53SS_CORE3_DBG_DBGBVR2_EL1_63_32	0007 3031 0424h
428h	32	A53SS_CORE3_DBG_DBGBCR2_EL1	0007 3031 0428h
430h	32	A53SS_CORE3_DBG_DBGBVR3_EL1_31_0	0007 3031 0430h
434h	32	A53SS_CORE3_DBG_DBGBVR3_EL1_63_32	0007 3031 0434h
438h	32	A53SS_CORE3_DBG_DBGBCR3_EL1	0007 3031 0438h
440h	32	A53SS_CORE3_DBG_DBGBVR4_EL1_31_0	0007 3031 0440h
444h	32	A53SS_CORE3_DBG_DBGBVR4_EL1_63_32	0007 3031 0444h
448h	32	A53SS_CORE3_DBG_DBGBCR4_EL1	0007 3031 0448h
450h	32	A53SS_CORE3_DBG_DBGBVR5_EL1_31_0	0007 3031 0450h
454h	32	A53SS_CORE3_DBG_DBGBVR5_EL1_63_32	0007 3031 0454h
458h	32	A53SS_CORE3_DBG_DBGBCR5_EL1	0007 3031 0458h
800h	32	A53SS_CORE3_DBG_DBGWVR0_EL1_31_0	0007 3031 0800h
804h	32	A53SS_CORE3_DBG_DBGWVR0_EL1_63_32	0007 3031 0804h
808h	32	A53SS_CORE3_DBG_DBGWCR0_EL1	0007 3031 0808h
810h	32	A53SS_CORE3_DBG_DBGWVR1_EL1_31_0	0007 3031 0810h
814h	32	A53SS_CORE3_DBG_DBGWVR1_EL1_63_32	0007 3031 0814h
818h	32	A53SS_CORE3_DBG_DBGWCR1_EL1	0007 3031 0818h
820h	32	A53SS_CORE3_DBG_DBGWVR2_EL1_31_0	0007 3031 0820h
824h	32	A53SS_CORE3_DBG_DBGWVR2_EL1_63_32	0007 3031 0824h
828h	32	A53SS_CORE3_DBG_DBGWCR2_EL1	0007 3031 0828h

Table 14-12422. A53SS_CORE3_DBG Registers, Base Address=0007 3031 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
830h	32	A53SS_CORE3_DBG_DBGWVR3_EL1_31_0	0007 3031 0830h
834h	32	A53SS_CORE3_DBG_DBGWVR3_EL1_63_32	0007 3031 0834h
838h	32	A53SS_CORE3_DBG_DBGWCR3_EL1	0007 3031 0838h
D00h	32	A53SS_CORE3_DBG_MIDR_EL1	0007 3031 0D00h
D20h	32	A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0	0007 3031 0D20h
D24h	32	A53SS_CORE3_DBG_ID_AA64PFR0_EL1_63_32	0007 3031 0D24h
D28h	32	A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0	0007 3031 0D28h
D2Ch	32	A53SS_CORE3_DBG_ID_AA64DFR0_EL1_63_32	0007 3031 0D2Ch
D30h	32	A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0	0007 3031 0D30h
D34h	32	A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_63_32	0007 3031 0D34h
D38h	32	A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0	0007 3031 0D38h
D3Ch	32	A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_63_32	0007 3031 0D3Ch
D40h	32	A53SS_CORE3_DBG_ID_AA64PFR1_EL1_31_0	0007 3031 0D40h
D44h	32	A53SS_CORE3_DBG_ID_AA64PFR1_EL1_63_32	0007 3031 0D44h
D48h	32	A53SS_CORE3_DBG_ID_AA64DFR1_EL1_31_0	0007 3031 0D48h
D4Ch	32	A53SS_CORE3_DBG_ID_AA64DFR1_EL1_63_32	0007 3031 0D4Ch
D50h	32	A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_31_0	0007 3031 0D50h
D54h	32	A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_63_32	0007 3031 0D54h
D58h	32	A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_31_0	0007 3031 0D58h
D5Ch	32	A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_63_32	0007 3031 0D5Ch
F00h	32	A53SS_CORE3_DBG_EDITCTRL	0007 3031 0F00h
FA0h	32	A53SS_CORE3_DBG_DBGCLAIMSET_EL1	0007 3031 0FA0h
FA4h	32	A53SS_CORE3_DBG_DBGCLAIMCLR_EL1	0007 3031 0FA4h
FA8h	32	A53SS_CORE3_DBG_EDDEVAFF0	0007 3031 0FA8h
FACh	32	A53SS_CORE3_DBG_EDDEVAFF1	0007 3031 0FACh
FB0h	32	A53SS_CORE3_DBG_EDLAR	0007 3031 0FB0h
FB4h	32	A53SS_CORE3_DBG_EDLSR	0007 3031 0FB4h
FB8h	32	A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1	0007 3031 0FB8h
FBCh	32	A53SS_CORE3_DBG_EDDEVARCH	0007 3031 0FBCh
FC0h	32	A53SS_CORE3_DBG_EDDEVID2	0007 3031 0FC0h
FC4h	32	A53SS_CORE3_DBG_EDDEVID1	0007 3031 0FC4h
FC8h	32	A53SS_CORE3_DBG_EDDEVID	0007 3031 0FC8h
FCCh	32	A53SS_CORE3_DBG_EDDEVTYPE	0007 3031 0FCCh
FD0h	32	A53SS_CORE3_DBG_EDPIDR4	0007 3031 0FD0h
FE0h	32	A53SS_CORE3_DBG_EDPIDR0	0007 3031 0FE0h
FE4h	32	A53SS_CORE3_DBG_EDPIDR1	0007 3031 0FE4h
FE8h	32	A53SS_CORE3_DBG_EDPIDR2	0007 3031 0FE8h
FECh	32	A53SS_CORE3_DBG_EDPIDR3	0007 3031 0FECh
FF0h	32	A53SS_CORE3_DBG_EDCIDR0	0007 3031 0FF0h
FF4h	32	A53SS_CORE3_DBG_EDCIDR1	0007 3031 0FF4h
FF8h	32	A53SS_CORE3_DBG_EDCIDR2	0007 3031 0FF8h
FFCh	32	A53SS_CORE3_DBG_EDCIDR3	0007 3031 0FFCh

Table 14-12423. A53SS_CORE3_PMU Registers, Base Address=0007 3032 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE3_PMU_PMEVCNTR0_EL0	0007 3032 0000h
8h	32	A53SS_CORE3_PMU_PMEVCNTR1_EL0	0007 3032 0008h
10h	32	A53SS_CORE3_PMU_PMEVCNTR2_EL0	0007 3032 0010h
18h	32	A53SS_CORE3_PMU_PMEVCNTR3_EL0	0007 3032 0018h
20h	32	A53SS_CORE3_PMU_PMEVCNTR4_EL0	0007 3032 0020h
28h	32	A53SS_CORE3_PMU_PMEVCNTR5_EL0	0007 3032 0028h
F8h	32	A53SS_CORE3_PMU_PMCCNTR_EL0_31_0	0007 3032 00F8h
FCh	32	A53SS_CORE3_PMU_PMCCNTR_EL0_63_32	0007 3032 00FCh
400h	32	A53SS_CORE3_PMU_PMEVTYPER0_EL0	0007 3032 0400h
404h	32	A53SS_CORE3_PMU_PMEVTYPER1_EL0	0007 3032 0404h
408h	32	A53SS_CORE3_PMU_PMEVTYPER2_EL0	0007 3032 0408h
40Ch	32	A53SS_CORE3_PMU_PMEVTYPER3_EL0	0007 3032 040Ch
410h	32	A53SS_CORE3_PMU_PMEVTYPER4_EL0	0007 3032 0410h
414h	32	A53SS_CORE3_PMU_PMEVTYPER5_EL0	0007 3032 0414h
47Ch	32	A53SS_CORE3_PMU_PMCCFILTR_EL0	0007 3032 047Ch
C00h	32	A53SS_CORE3_PMU_PMCNTENSET_EL0	0007 3032 0C00h
C20h	32	A53SS_CORE3_PMU_PMCNTENCLR_EL0	0007 3032 0C20h
C40h	32	A53SS_CORE3_PMU_PMINTENSET_EL1	0007 3032 0C40h
C60h	32	A53SS_CORE3_PMU_PMINTENCLR_EL1	0007 3032 0C60h
C80h	32	A53SS_CORE3_PMU_PMOVSCLR_EL0	0007 3032 0C80h
CA0h	32	A53SS_CORE3_PMU_PMSWINC_EL0	0007 3032 0CA0h
CC0h	32	A53SS_CORE3_PMU_PMOVSSET_EL0	0007 3032 0CC0h
E00h	32	A53SS_CORE3_PMU_PMCFGR	0007 3032 0E00h
E04h	32	A53SS_CORE3_PMU_PMCR_EL0	0007 3032 0E04h
E20h	32	A53SS_CORE3_PMU_PMCEID0_EL0	0007 3032 0E20h
E24h	32	A53SS_CORE3_PMU_PMCEID1_EL0	0007 3032 0E24h
F00h	32	A53SS_CORE3_PMU_PMITCTRL	0007 3032 0F00h
FA8h	32	A53SS_CORE3_PMU_PMDEVAFF0	0007 3032 0FA8h
FACh	32	A53SS_CORE3_PMU_PMDEVAFF1	0007 3032 0FACh
FB0h	32	A53SS_CORE3_PMU_PMLAR	0007 3032 0FB0h
FB4h	32	A53SS_CORE3_PMU_PMLSR	0007 3032 0FB4h
FB8h	32	A53SS_CORE3_PMU_PMAUTHSTATUS	0007 3032 0FB8h
FBCh	32	A53SS_CORE3_PMU_PMDEVARCH	0007 3032 0FBCh
FCCh	32	A53SS_CORE3_PMU_PMDEVTYPE	0007 3032 0FCCh
FD0h	32	A53SS_CORE3_PMU_PMPIDR4	0007 3032 0FD0h
FD4h	32	A53SS_CORE3_PMU_PMPIDR5	0007 3032 0FD4h
FD8h	32	A53SS_CORE3_PMU_PMPIDR6	0007 3032 0FD8h
FDCh	32	A53SS_CORE3_PMU_PMPIDR7	0007 3032 0FDCh
FE0h	32	A53SS_CORE3_PMU_PMPIDR0	0007 3032 0FE0h
FE4h	32	A53SS_CORE3_PMU_PMPIDR1	0007 3032 0FE4h
FE8h	32	A53SS_CORE3_PMU_PMPIDR2	0007 3032 0FE8h
FECh	32	A53SS_CORE3_PMU_PMPIDR3	0007 3032 0FECh
FF0h	32	A53SS_CORE3_PMU_PMCIDR0	0007 3032 0FF0h
FF4h	32	A53SS_CORE3_PMU_PMCIDR1	0007 3032 0FF4h
FF8h	32	A53SS_CORE3_PMU_PMCIDR2	0007 3032 0FF8h

Table 14-12423. A53SS_CORE3_PMU Registers, Base Address=0007 3032 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FFCh	32	A53SS_CORE3_PMU_PMCIDR3	0007 3032 0FFCh

Table 14-12424. A53SS_CORE3_ETM Registers, Base Address=0007 3033 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_CORE3_ETM_TRCPRGCTLR	0007 3033 0004h
Ch	32	A53SS_CORE3_ETM_TRCSTATR	0007 3033 000Ch
10h	32	A53SS_CORE3_ETM_TRCCONFIGR	0007 3033 0010h
18h	32	A53SS_CORE3_ETM_TRCAUXCTLR	0007 3033 0018h
20h	32	A53SS_CORE3_ETM_TRCEVENTCTL0R	0007 3033 0020h
24h	32	A53SS_CORE3_ETM_TRCEVENTCTL1R	0007 3033 0024h
2Ch	32	A53SS_CORE3_ETM_TRCSTALLCTLR	0007 3033 002Ch
30h	32	A53SS_CORE3_ETM_TRCTSCTLR	0007 3033 0030h
34h	32	A53SS_CORE3_ETM_TRCSYNCPR	0007 3033 0034h
38h	32	A53SS_CORE3_ETM_TRCCCCTLR	0007 3033 0038h
3Ch	32	A53SS_CORE3_ETM_TRCBBCTLR	0007 3033 003Ch
40h	32	A53SS_CORE3_ETM_TRCTRACEIDR	0007 3033 0040h
80h	32	A53SS_CORE3_ETM_TRCVICTLR	0007 3033 0080h
84h	32	A53SS_CORE3_ETM_TRCVIIECTLR	0007 3033 0084h
88h	32	A53SS_CORE3_ETM_TRCVISSCTLR	0007 3033 0088h
100h	32	A53SS_CORE3_ETM_TRCSEQEVR0	0007 3033 0100h
104h	32	A53SS_CORE3_ETM_TRCSEQEVR1	0007 3033 0104h
108h	32	A53SS_CORE3_ETM_TRCSEQEVR2	0007 3033 0108h
118h	32	A53SS_CORE3_ETM_TRCSEQRSTEVR	0007 3033 0118h
11Ch	32	A53SS_CORE3_ETM_TRCSEQSTR	0007 3033 011Ch
120h	32	A53SS_CORE3_ETM_TRCEXTINSELR	0007 3033 0120h
140h	32	A53SS_CORE3_ETM_TRCCNTRLDVR0	0007 3033 0140h
144h	32	A53SS_CORE3_ETM_TRCCNTRLDVR1	0007 3033 0144h
150h	32	A53SS_CORE3_ETM_TRCCNTCTLR0	0007 3033 0150h
154h	32	A53SS_CORE3_ETM_TRCCNTCTLR1	0007 3033 0154h
160h	32	A53SS_CORE3_ETM_TRCCNTVR0	0007 3033 0160h
164h	32	A53SS_CORE3_ETM_TRCCNTVR1	0007 3033 0164h
180h	32	A53SS_CORE3_ETM_TRCIDR8	0007 3033 0180h
184h	32	A53SS_CORE3_ETM_TRCIDR9	0007 3033 0184h
188h	32	A53SS_CORE3_ETM_TRCIDR10	0007 3033 0188h
18Ch	32	A53SS_CORE3_ETM_TRCIDR11	0007 3033 018Ch
190h	32	A53SS_CORE3_ETM_TRCIDR12	0007 3033 0190h
194h	32	A53SS_CORE3_ETM_TRCIDR13	0007 3033 0194h
1C0h	32	A53SS_CORE3_ETM_TRCIMSPEC0	0007 3033 01C0h
1E0h	32	A53SS_CORE3_ETM_TRCIDR0	0007 3033 01E0h
1E4h	32	A53SS_CORE3_ETM_TRCIDR1	0007 3033 01E4h
1E8h	32	A53SS_CORE3_ETM_TRCIDR2	0007 3033 01E8h
1ECh	32	A53SS_CORE3_ETM_TRCIDR3	0007 3033 01ECh
1F0h	32	A53SS_CORE3_ETM_TRCIDR4	0007 3033 01F0h
1F4h	32	A53SS_CORE3_ETM_TRCIDR5	0007 3033 01F4h

Table 14-12424. A53SS_CORE3_ETM Registers, Base Address=0007 3033 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
208h	32	A53SS_CORE3_ETM_TRCRSCTLR2	0007 3033 0208h
20Ch	32	A53SS_CORE3_ETM_TRCRSCTLR3	0007 3033 020Ch
210h	32	A53SS_CORE3_ETM_TRCRSCTLR4	0007 3033 0210h
214h	32	A53SS_CORE3_ETM_TRCRSCTLR5	0007 3033 0214h
218h	32	A53SS_CORE3_ETM_TRCRSCTLR6	0007 3033 0218h
21Ch	32	A53SS_CORE3_ETM_TRCRSCTLR7	0007 3033 021Ch
220h	32	A53SS_CORE3_ETM_TRCRSCTLR8	0007 3033 0220h
224h	32	A53SS_CORE3_ETM_TRCRSCTLR9	0007 3033 0224h
228h	32	A53SS_CORE3_ETM_TRCRSCTLR10	0007 3033 0228h
22Ch	32	A53SS_CORE3_ETM_TRCRSCTLR11	0007 3033 022Ch
230h	32	A53SS_CORE3_ETM_TRCRSCTLR12	0007 3033 0230h
234h	32	A53SS_CORE3_ETM_TRCRSCTLR13	0007 3033 0234h
238h	32	A53SS_CORE3_ETM_TRCRSCTLR14	0007 3033 0238h
23Ch	32	A53SS_CORE3_ETM_TRCRSCTLR15	0007 3033 023Ch
280h	32	A53SS_CORE3_ETM_TRCSSCCR0	0007 3033 0280h
2A0h	32	A53SS_CORE3_ETM_TRCSSCSR0	0007 3033 02A0h
300h	32	A53SS_CORE3_ETM_TRCOSLAR	0007 3033 0300h
304h	32	A53SS_CORE3_ETM_TRCOSLSR	0007 3033 0304h
310h	32	A53SS_CORE3_ETM_TRCPDCR	0007 3033 0310h
314h	32	A53SS_CORE3_ETM_TRCPDSR	0007 3033 0314h
400h	32	A53SS_CORE3_ETM_TRCACVR0_31_0	0007 3033 0400h
404h	32	A53SS_CORE3_ETM_TRCACVR0_63_32	0007 3033 0404h
408h	32	A53SS_CORE3_ETM_TRCACVR1_31_0	0007 3033 0408h
40Ch	32	A53SS_CORE3_ETM_TRCACVR1_63_32	0007 3033 040Ch
410h	32	A53SS_CORE3_ETM_TRCACVR2_31_0	0007 3033 0410h
414h	32	A53SS_CORE3_ETM_TRCACVR2_63_32	0007 3033 0414h
418h	32	A53SS_CORE3_ETM_TRCACVR3_31_0	0007 3033 0418h
41Ch	32	A53SS_CORE3_ETM_TRCACVR3_63_32	0007 3033 041Ch
420h	32	A53SS_CORE3_ETM_TRCACVR4_31_0	0007 3033 0420h
424h	32	A53SS_CORE3_ETM_TRCACVR4_63_32	0007 3033 0424h
428h	32	A53SS_CORE3_ETM_TRCACVR5_31_0	0007 3033 0428h
42Ch	32	A53SS_CORE3_ETM_TRCACVR5_63_32	0007 3033 042Ch
430h	32	A53SS_CORE3_ETM_TRCACVR6_31_0	0007 3033 0430h
434h	32	A53SS_CORE3_ETM_TRCACVR6_63_32	0007 3033 0434h
438h	32	A53SS_CORE3_ETM_TRCACVR7_31_0	0007 3033 0438h
43Ch	32	A53SS_CORE3_ETM_TRCACVR7_63_32	0007 3033 043Ch
480h	32	A53SS_CORE3_ETM_TRCACATR0	0007 3033 0480h
488h	32	A53SS_CORE3_ETM_TRCACATR1	0007 3033 0488h
490h	32	A53SS_CORE3_ETM_TRCACATR2	0007 3033 0490h
498h	32	A53SS_CORE3_ETM_TRCACATR3	0007 3033 0498h
4A0h	32	A53SS_CORE3_ETM_TRCACATR4	0007 3033 04A0h
4A8h	32	A53SS_CORE3_ETM_TRCACATR5	0007 3033 04A8h
4B0h	32	A53SS_CORE3_ETM_TRCACATR6	0007 3033 04B0h
4B8h	32	A53SS_CORE3_ETM_TRCACATR7	0007 3033 04B8h

Table 14-12424. A53SS_CORE3_ETM Registers, Base Address=0007 3033 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
600h	32	A53SS_CORE3_ETM_TRCCIDCVR0	0007 3033 0600h
640h	32	A53SS_CORE3_ETM_TRCVMIDCVR0	0007 3033 0640h
680h	32	A53SS_CORE3_ETM_TRCCIDCCTLR0	0007 3033 0680h
EE4h	32	A53SS_CORE3_ETM_TRCITATBIDR	0007 3033 0EE4h
EECh	32	A53SS_CORE3_ETM_TRCITIDATAR	0007 3033 0EECh
EF4h	32	A53SS_CORE3_ETM_TRCITIATBINR	0007 3033 0EF4h
EFCh	32	A53SS_CORE3_ETM_TRCITIATBOUTR	0007 3033 0EFCh
F00h	32	A53SS_CORE3_ETM_TRCITCTRL	0007 3033 0F00h
FA0h	32	A53SS_CORE3_ETM_TRCCLAIMSET	0007 3033 0FA0h
FA4h	32	A53SS_CORE3_ETM_TRCCLAIMCLR	0007 3033 0FA4h
FA8h	32	A53SS_CORE3_ETM_TRCDEVAFF0	0007 3033 0FA8h
FACh	32	A53SS_CORE3_ETM_TRCDEVAFF1	0007 3033 0FACh
FB0h	32	A53SS_CORE3_ETM_TRCLAR	0007 3033 0FB0h
FB4h	32	A53SS_CORE3_ETM_TRCLSR	0007 3033 0FB4h
FB8h	32	A53SS_CORE3_ETM_TRCAUTHSTATUS	0007 3033 0FB8h
FBCh	32	A53SS_CORE3_ETM_TRCDEVARCH	0007 3033 0FBCh
FC8h	32	A53SS_CORE3_ETM_TRCDEVID	0007 3033 0FC8h
FCCh	32	A53SS_CORE3_ETM_TRCDEVTYPE	0007 3033 0FCCh
FD0h	32	A53SS_CORE3_ETM_TRCPIDR4	0007 3033 0FD0h
FD4h	32	A53SS_CORE3_ETM_TRCPIDR5	0007 3033 0FD4h
FD8h	32	A53SS_CORE3_ETM_TRCPIDR6	0007 3033 0FD8h
FDCh	32	A53SS_CORE3_ETM_TRCPIDR7	0007 3033 0FDCh
FE0h	32	A53SS_CORE3_ETM_TRCPIDR0	0007 3033 0FE0h
FE4h	32	A53SS_CORE3_ETM_TRCPIDR1	0007 3033 0FE4h
FE8h	32	A53SS_CORE3_ETM_TRCPIDR2	0007 3033 0FE8h
FECh	32	A53SS_CORE3_ETM_TRCPIDR3	0007 3033 0FECh
FF0h	32	A53SS_CORE3_ETM_TRCCIDR0	0007 3033 0FF0h
FF4h	32	A53SS_CORE3_ETM_TRCCIDR1	0007 3033 0FF4h
FF8h	32	A53SS_CORE3_ETM_TRCCIDR2	0007 3033 0FF8h
FFCh	32	A53SS_CORE3_ETM_TRCCIDR3	0007 3033 0FFCh

Table 14-12425. A53SS_CORE3_CTI Registers, Base Address=0007 3034 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_CORE3_CTI_CTICONTROL	0007 3034 0000h
10h	32	A53SS_CORE3_CTI_CTIINTACK	0007 3034 0010h
14h	32	A53SS_CORE3_CTI_CTIAPPSET	0007 3034 0014h
18h	32	A53SS_CORE3_CTI_CTIAPPCLEAR	0007 3034 0018h
1Ch	32	A53SS_CORE3_CTI_CTIAPPPULSE	0007 3034 001Ch
20h	32	A53SS_CORE3_CTI_CTIINEN0	0007 3034 0020h
24h	32	A53SS_CORE3_CTI_CTIINEN1	0007 3034 0024h
28h	32	A53SS_CORE3_CTI_CTIINEN2	0007 3034 0028h
2Ch	32	A53SS_CORE3_CTI_CTIINEN3	0007 3034 002Ch
30h	32	A53SS_CORE3_CTI_CTIINEN4	0007 3034 0030h
34h	32	A53SS_CORE3_CTI_CTIINEN5	0007 3034 0034h

Table 14-12425. A53SS_CORE3_CTI Registers, Base Address=0007 3034 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
38h	32	A53SS_CORE3_CTI_CTIINEN6	0007 3034 0038h
3Ch	32	A53SS_CORE3_CTI_CTIINEN7	0007 3034 003Ch
A0h	32	A53SS_CORE3_CTI_CTIOUTEN0	0007 3034 00A0h
A4h	32	A53SS_CORE3_CTI_CTIOUTEN1	0007 3034 00A4h
A8h	32	A53SS_CORE3_CTI_CTIOUTEN2	0007 3034 00A8h
ACh	32	A53SS_CORE3_CTI_CTIOUTEN3	0007 3034 00ACh
B0h	32	A53SS_CORE3_CTI_CTIOUTEN4	0007 3034 00B0h
B4h	32	A53SS_CORE3_CTI_CTIOUTEN5	0007 3034 00B4h
B8h	32	A53SS_CORE3_CTI_CTIOUTEN6	0007 3034 00B8h
BCh	32	A53SS_CORE3_CTI_CTIOUTEN7	0007 3034 00BCh
130h	32	A53SS_CORE3_CTI_CTITRIGINSTATUS	0007 3034 0130h
134h	32	A53SS_CORE3_CTI_CTITRIGOUTSTATUS	0007 3034 0134h
138h	32	A53SS_CORE3_CTI_CTICHINSTATUS	0007 3034 0138h
13Ch	32	A53SS_CORE3_CTI_CTICHOUTSTATUS	0007 3034 013Ch
140h	32	A53SS_CORE3_CTI_CTIGATE	0007 3034 0140h
144h	32	A53SS_CORE3_CTI_ASICCTL	0007 3034 0144h
F00h	32	A53SS_CORE3_CTI_CTIITCTRL	0007 3034 0F00h
FA0h	32	A53SS_CORE3_CTI_CTICLAIMSET	0007 3034 0FA0h
FA4h	32	A53SS_CORE3_CTI_CTICLAIMCLR	0007 3034 0FA4h
FA8h	32	A53SS_CORE3_CTI_CTIDEVAFF0	0007 3034 0FA8h
FACh	32	A53SS_CORE3_CTI_CTIDEVAFF1	0007 3034 0FACh
FB0h	32	A53SS_CORE3_CTI_CTILAR	0007 3034 0FB0h
FB4h	32	A53SS_CORE3_CTI_CTILSR	0007 3034 0FB4h
FB8h	32	A53SS_CORE3_CTI_CTIAUTHSTATUS	0007 3034 0FB8h
FBCh	32	A53SS_CORE3_CTI_CTIDEVARCH	0007 3034 0FBCh
FC0h	32	A53SS_CORE3_CTI_CTIDEVID2	0007 3034 0FC0h
FC4h	32	A53SS_CORE3_CTI_CTIDEVID1	0007 3034 0FC4h
FC8h	32	A53SS_CORE3_CTI_CTIDEVID	0007 3034 0FC8h
FCCh	32	A53SS_CORE3_CTI_CTIDEVTYPE	0007 3034 0FCCh
FD0h	32	A53SS_CORE3_CTI_CTIPIDR4	0007 3034 0FD0h
FD4h	32	A53SS_CORE3_CTI_CTIPIDR5	0007 3034 0FD4h
FD8h	32	A53SS_CORE3_CTI_CTIPIDR6	0007 3034 0FD8h
FDCh	32	A53SS_CORE3_CTI_CTIPIDR7	0007 3034 0FDCh
FE0h	32	A53SS_CORE3_CTI_CTIPIDR0	0007 3034 0FE0h
FE4h	32	A53SS_CORE3_CTI_CTIPIDR1	0007 3034 0FE4h
FE8h	32	A53SS_CORE3_CTI_CTIPIDR2	0007 3034 0FE8h
FECh	32	A53SS_CORE3_CTI_CTIPIDR3	0007 3034 0FECh
FF0h	32	A53SS_CORE3_CTI_CTICIDR0	0007 3034 0FF0h
FF4h	32	A53SS_CORE3_CTI_CTICIDR1	0007 3034 0FF4h
FF8h	32	A53SS_CORE3_CTI_CTICIDR2	0007 3034 0FF8h
FFCh	32	A53SS_CORE3_CTI_CTICIDR3	0007 3034 0FFCh

14.3.1.1.2 A53SS Registers

A53SS Registers

14.3.1.1.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-12426. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9000h**

Figure 14-4117. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12428. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12429. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9008h**

Figure 14-4118. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-12431. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-12432. Instance Table

Instance Name	Physical Address
A53SS0	**0071 900Ch**

Figure 14-4119. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-12434. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-12435. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9010h + formula**

Figure 14-4120. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12437. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12438. Instance Table

Instance Name	Physical Address
A53SS0	**0071 903Ch**

Figure 14-4121. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12440. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12441. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9040h**

Figure 14-4122. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12443. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12443. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12443. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12444. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9080h**

Figure 14-4123. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12446. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12446. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12446. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12447. Instance Table

Instance Name	Physical Address
A53SS0	**0071 90C0h**

Figure 14-4124. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12449. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12449. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12449. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12450. Instance Table

Instance Name	Physical Address
A53SS0	**0071 913Ch**

Figure 14-4125. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12452. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12453. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9140h**

Figure 14-4126. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12455. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12455. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12455. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12456. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9180h**

Figure 14-4127. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12458. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12458. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12458. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12459. Instance Table

Instance Name	Physical Address
A53SS0	**0071 91C0h**

Figure 14-4128. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12461. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12461. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12461. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12462. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9200h**

Figure 14-4129. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12464. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12465. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9204h**

Figure 14-4130. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12467. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12468. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9208h**

Figure 14-4131. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12470. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12471. Instance Table

Instance Name	Physical Address
A53SS0	**0071 920Ch**

Figure 14-4132. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12473. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.17 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-12474. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9000h**

Figure 14-4133. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12476. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.18 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12477. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9008h**

Figure 14-4134. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-12479. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.19 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-12480. Instance Table

Instance Name	Physical Address
A53SS0	**0071 900Ch**

Figure 14-4135. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-12482. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.20 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-12483. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9010h + formula**

Figure 14-4136. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12485. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.21 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12486. Instance Table

Instance Name	Physical Address
A53SS0	**0071 903Ch**

Figure 14-4137. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12488. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12489. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9040h**

Figure 14-4138. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12491. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12491. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12491. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12492. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9080h**

Figure 14-4139. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12494. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12494. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12494. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12495. Instance Table

Instance Name	Physical Address
A53SS0	**0071 90C0h**

Figure 14-4140. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12497. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12497. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12497. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.25 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12498. Instance Table

Instance Name	Physical Address
A53SS0	**0071 913Ch**

Figure 14-4141. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12500. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.26 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12501. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9140h**

Figure 14-4142. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12503. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12503. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12503. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12504. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9180h**

Figure 14-4143. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12506. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12506. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12506. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12507. Instance Table

Instance Name	Physical Address
A53SS0	**0071 91C0h**

Figure 14-4144. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12509. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12509. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12509. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12510. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9200h**

Figure 14-4145. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12512. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12513. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9204h**

Figure 14-4146. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12515. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.31 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12516. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9208h**

Figure 14-4147. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12518. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12519. Instance Table

Instance Name	Physical Address
A53SS0	**0071 920Ch**

Figure 14-4148. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12521. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.33 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-12522. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9000h**

Figure 14-4149. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12524. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.34 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12525. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9008h**

Figure 14-4150. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-12527. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.35 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-12528. Instance Table

Instance Name	Physical Address
A53SS0	**0071 900Ch**

Figure 14-4151. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-12530. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.36 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-12531. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9010h + formula**

Figure 14-4152. ECC_AGGR_RESERVED_SVBUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12533. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.37 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12534. Instance Table

Instance Name	Physical Address
A53SS0	**0071 903Ch**

Figure 14-4153. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12536. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.38 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12537. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9040h**

Figure 14-4154. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12539. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12539. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12539. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.39 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12540. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9080h**

Figure 14-4155. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12542. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12542. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12542. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.40 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12543. Instance Table

Instance Name	Physical Address
A53SS0	**0071 90C0h**

Figure 14-4156. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12545. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12545. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12545. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.41 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12546. Instance Table

Instance Name	Physical Address
A53SS0	**0071 913Ch**

Figure 14-4157. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12548. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.42 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12549. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9140h**

Figure 14-4158. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12551. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12551. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12551. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.43 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-12552. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9180h**

Figure 14-4159. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12554. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12554. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12554. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.44 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12555. Instance Table

Instance Name	Physical Address
A53SS0	**0071 91C0h**

Figure 14-4160. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12557. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12557. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12557. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.45 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12558. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9200h**

Figure 14-4161. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12560. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.46 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12561. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9204h**

Figure 14-4162. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12563. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.47 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12564. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9208h**

Figure 14-4163. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12566. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.48 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12567. Instance Table

Instance Name	Physical Address
A53SS0	**0071 920Ch**

Figure 14-4164. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12569. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.49 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-12570. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9000h**

Figure 14-4165. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-12572. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.50 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12573. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9008h**

Figure 14-4166. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-12575. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.51 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-12576. Instance Table

Instance Name	Physical Address
A53SS0	**0071 900Ch**

Figure 14-4167. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1Bh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1Bh</td></tr>
</table>

Table 14-12578. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.52 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-12579. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9010h + formula**

Figure 14-4168. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12581. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.53 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12582. Instance Table

Instance Name	Physical Address
A53SS0	**0071 903Ch**

Figure 14-4169. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12584. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.54 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12585. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9040h**

Figure 14-4170. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12587. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12587. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12587. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.55 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12588. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9080h**

Figure 14-4171. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12590. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12590. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12590. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.56 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12591. Instance Table

Instance Name	Physical Address
A53SS0	**0071 90C0h**

Figure 14-4172. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12593. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12593. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12593. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.57 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12594. Instance Table

Instance Name	Physical Address
A53SS0	**0071 913Ch**

Figure 14-4173. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12596. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.58 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12597. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9140h**

Figure 14-4174. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12599. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12599. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12599. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.59 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12600. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9180h**

Figure 14-4175. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12602. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12602. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12602. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.60 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12603. Instance Table

Instance Name	Physical Address
A53SS0	**0071 91C0h**

Figure 14-4176. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12605. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12605. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12605. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.61 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12606. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9200h**

Figure 14-4177. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12608. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.62 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12609. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9204h**

Figure 14-4178. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12611. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.63 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12612. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9208h**

Figure 14-4179. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12614. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.64 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12615. Instance Table

Instance Name	Physical Address
A53SS0	**0071 920Ch**

Figure 14-4180. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12617. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.65 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-12618. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9000h**

Figure 14-4181. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12620. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.66 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12621. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9008h**

Figure 14-4182. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-12623. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.67 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-12624. Instance Table

Instance Name	Physical Address
A53SS0	**0071 900Ch**

Figure 14-4183. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-12626. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.68 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-12627. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9010h + formula**

Figure 14-4184. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12629. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.69 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12630. Instance Table

Instance Name	Physical Address
A53SS0	**0071 903Ch**

Figure 14-4185. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12632. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.70 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12633. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9040h**

Figure 14-4186. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12635. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12635. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12635. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.71 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12636. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9080h**

Figure 14-4187. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12638. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12638. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12638. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.72 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12639. Instance Table

Instance Name	Physical Address
A53SS0	**0071 90C0h**

Figure 14-4188. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12641. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12641. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12641. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.73 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12642. Instance Table

Instance Name	Physical Address
A53SS0	**0071 913Ch**

Figure 14-4189. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12644. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.74 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12645. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9140h**

Figure 14-4190. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12647. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-12647. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-12647. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.75 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12648. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9180h**

Figure 14-4191. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12650. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12650. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12650. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.76 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12651. Instance Table

Instance Name	Physical Address
A53SS0	**0071 91C0h**

Figure 14-4192. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12653. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-12653. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU3_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU3_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU3_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU3_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU3_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU3_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU3_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-12653. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU3_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU3_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU3_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu3_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.77 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12654. Instance Table

Instance Name	Physical Address
A53SS0	0071 9200h

Figure 14-4193. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12656. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.78 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12657. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9204h**

Figure 14-4194. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12659. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.79 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12660. Instance Table

Instance Name	Physical Address
A53SS0	**0071 9208h**

Figure 14-4195. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12662. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.80 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12663. Instance Table

Instance Name	**Physical Address**
A53SS0	**0071 920Ch**

Figure 14-4196. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12665. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.81 A53SS_SS_ROM_ROMENTRY0 Register

1 A53SS_SS_ROM_ROMENTRY0 Register (Offset = 0h) [reset = 0h]

ROM Table Entry Register 0 (CPU 0 Debug Component)

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Table 14-12666. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0000h**

Figure 14-4197. A53SS_SS_ROM_ROMENTRY0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12668. A53SS_SS_ROM_ROMENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.82 A53SS_SS_ROM_ROMENTRY1 Register

1 A53SS_SS_ROM_ROMENTRY1 Register (Offset = 4h) [reset = 0h]

ROM Table Entry Register 1 (CPU 0 CTI Component)

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Table 14-12669. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0004h**

Figure 14-4198. A53SS_SS_ROM_ROMENTRY1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12671. A53SS_SS_ROM_ROMENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.83 A53SS_SS_ROM_ROMENTRY2 Register

1 A53SS_SS_ROM_ROMENTRY2 Register (Offset = 8h) [reset = 0h]

ROM Table Entry Register 2 (CPU 0 PMU Component)

Return to Summary Table

Table 14-12672. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0008h**

Figure 14-4199. A53SS_SS_ROM_ROMENTRY2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-12674. A53SS_SS_ROM_ROMENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.84 A53SS_SS_ROM_ROMENTRY3 Register

1 A53SS_SS_ROM_ROMENTRY3 Register (Offset = Ch) [reset = 0h]

ROM Table Entry Register 3 (CPU 0 ETM Component)

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Table 14-12675. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 000Ch**

Figure 14-4200. A53SS_SS_ROM_ROMENTRY3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12677. A53SS_SS_ROM_ROMENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.85 A53SS_SS_ROM_ROMENTRY4 Register

1 A53SS_SS_ROM_ROMENTRY4 Register (Offset = 10h) [reset = 0h]

ROM Table Entry Register 4 (CPU 1 Debug Component)

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Table 14-12678. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0010h**

Figure 14-4201. A53SS_SS_ROM_ROMENTRY4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12680. A53SS_SS_ROM_ROMENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.86 A53SS_SS_ROM_ROMENTRY5 Register

1 A53SS_SS_ROM_ROMENTRY5 Register (Offset = 14h) [reset = 0h]

ROM Table Entry Register 5 (CPU 1 CTI Component)

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Table 14-12681. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0014h**

Figure 14-4202. A53SS_SS_ROM_ROMENTRY5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12683. A53SS_SS_ROM_ROMENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.87 A53SS_SS_ROM_ROMENTRY6 Register

1 A53SS_SS_ROM_ROMENTRY6 Register (Offset = 18h) [reset = 0h]

ROM Table Entry Register 6 (CPU 1 PMU Component)

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Table 14-12684. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0018h**

Figure 14-4203. A53SS_SS_ROM_ROMENTRY6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12686. A53SS_SS_ROM_ROMENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.88 A53SS_SS_ROM_ROMENTRY7 Register

1 A53SS_SS_ROM_ROMENTRY7 Register (Offset = 1Ch) [reset = 0h]

ROM Table Entry Register 7 (CPU 1 ETM Component)

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Table 14-12687. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 001Ch**

Figure 14-4204. A53SS_SS_ROM_ROMENTRY7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12689. A53SS_SS_ROM_ROMENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.89 A53SS_SS_ROM_ROMENTRY8 Register

1 A53SS_SS_ROM_ROMENTRY8 Register (Offset = 20h) [reset = 0h]

ROM Table Entry Register 8 (CPU 2 Debug Component)

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Table 14-12690. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0020h**

Figure 14-4205. A53SS_SS_ROM_ROMENTRY8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12692. A53SS_SS_ROM_ROMENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.90 A53SS_SS_ROM_ROMENTRY9 Register

1 A53SS_SS_ROM_ROMENTRY9 Register (Offset = 24h) [reset = 0h]

ROM Table Entry Register 9 (CPU 2 CTI Component)

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Table 14-12693. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0024h**

Figure 14-4206. A53SS_SS_ROM_ROMENTRY9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12695. A53SS_SS_ROM_ROMENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.91 A53SS_SS_ROM_ROMENTRY10 Register

1 A53SS_SS_ROM_ROMENTRY10 Register (Offset = 28h) [reset = 0h]

ROM Table Entry Register 10 (CPU 2 PMU Component)

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Table 14-12696. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0028h**

Figure 14-4207. A53SS_SS_ROM_ROMENTRY10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12698. A53SS_SS_ROM_ROMENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.92 A53SS_SS_ROM_ROMENTRY11 Register

1 A53SS_SS_ROM_ROMENTRY11 Register (Offset = 2Ch) [reset = 0h]

ROM Table Entry Register 11 (CPU 2 ETM Component)

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Table 14-12699. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 002Ch**

Figure 14-4208. A53SS_SS_ROM_ROMENTRY11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12701. A53SS_SS_ROM_ROMENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.93 A53SS_SS_ROM_ROMENTRY12 Register

1 A53SS_SS_ROM_ROMENTRY12 Register (Offset = 30h) [reset = 0h]

ROM Table Entry Register 12 (CPU 3 Debug Component)

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Table 14-12702. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0030h**

Figure 14-4209. A53SS_SS_ROM_ROMENTRY12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12704. A53SS_SS_ROM_ROMENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.94 A53SS_SS_ROM_ROMENTRY13 Register

1 A53SS_SS_ROM_ROMENTRY13 Register (Offset = 34h) [reset = 0h]

ROM Table Entry Register 13 (CPU 3 CTI Component)

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Table 14-12705. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0034h**

Figure 14-4210. A53SS_SS_ROM_ROMENTRY13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12707. A53SS_SS_ROM_ROMENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.95 A53SS_SS_ROM_ROMENTRY14 Register

1 A53SS_SS_ROM_ROMENTRY14 Register (Offset = 38h) [reset = 0h]

ROM Table Entry Register 14 (CPU 3 PMU Component)

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Table 14-12708. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0038h**

Figure 14-4211. A53SS_SS_ROM_ROMENTRY14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12710. A53SS_SS_ROM_ROMENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.96 A53SS_SS_ROM_ROMENTRY15 Register

1 A53SS_SS_ROM_ROMENTRY15 Register (Offset = 3Ch) [reset = 0h]

ROM Table Entry Register 15 (CPU 3 ETM Component)

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Table 14-12711. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 003Ch**

Figure 14-4212. A53SS_SS_ROM_ROMENTRY15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12713. A53SS_SS_ROM_ROMENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.97 A53SS_SS_ROM_ROM_PERIPHID4_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID4_VAL Register (Offset = FD0h) [reset = 0h]

ROM Peripheral ID 4

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Table 14-12714. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD0h**

Figure 14-4213. A53SS_SS_ROM_ROM_PERIPHID4_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12716. A53SS_SS_ROM_ROM_PERIPHID4_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.98 A53SS_SS_ROM_ROM_PERIPHID5_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID5_VAL Register (Offset = FD4h) [reset = 0h]

ROM Peripheral ID 5

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Table 14-12717. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD4h**

Figure 14-4214. A53SS_SS_ROM_ROM_PERIPHID5_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12719. A53SS_SS_ROM_ROM_PERIPHID5_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.99 A53SS_SS_ROM_ROM_PERIPHID6_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID6_VAL Register (Offset = FD8h) [reset = 0h]

ROM Peripheral ID 6

Return to Summary Table

Table 14-12720. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD8h**

Figure 14-4215. A53SS_SS_ROM_ROM_PERIPHID6_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12722. A53SS_SS_ROM_ROM_PERIPHID6_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.100 A53SS_SS_ROM_ROM_PERIPHID7_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID7_VAL Register (Offset = FDCh) [reset = 0h]

ROM Peripheral ID 7

Return to Summary Table

Table 14-12723. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FDCh**

Figure 14-4216. A53SS_SS_ROM_ROM_PERIPHID7_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12725. A53SS_SS_ROM_ROM_PERIPHID7_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.101 A53SS_SS_ROM_ROM_PERIPHID0_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID0_VAL Register (Offset = FE0h) [reset = 0h]

ROM Peripheral ID 0

Return to Summary Table

Table 14-12726. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3000 0FE0h**

Figure 14-4217. A53SS_SS_ROM_ROM_PERIPHID0_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12728. A53SS_SS_ROM_ROM_PERIPHID0_VAL Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.102 A53SS_SS_ROM_ROM_PERIPHID1_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID1_VAL Register (Offset = FE4h) [reset = 0h]

ROM Peripheral ID 1

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Table 14-12729. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FE4h**

Figure 14-4218. A53SS_SS_ROM_ROM_PERIPHID1_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12731. A53SS_SS_ROM_ROM_PERIPHID1_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.103 A53SS_SS_ROM_ROM_PERIPHID2_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID2_VAL Register (Offset = FE8h) [reset = 0h]

ROM Peripheral ID 2

Return to Summary Table

Table 14-12732. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FE8h**

Figure 14-4219. A53SS_SS_ROM_ROM_PERIPHID2_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12734. A53SS_SS_ROM_ROM_PERIPHID2_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.104 A53SS_SS_ROM_ROM_PERIPHID3_VAL Register

1 A53SS_SS_ROM_ROM_PERIPHID3_VAL Register (Offset = FECh) [reset = 0h]

ROM Peripheral ID 3

Return to Summary Table

Table 14-12735. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FECh**

Figure 14-4220. A53SS_SS_ROM_ROM_PERIPHID3_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12737. A53SS_SS_ROM_ROM_PERIPHID3_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.105 A53SS_SS_ROM_ROM_COMPONID0_VAL Register

1 A53SS_SS_ROM_ROM_COMPONID0_VAL Register (Offset = FF0h) [reset = 0h]

ROM Component ID 0

Return to Summary Table

Table 14-12738. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FF0h**

Figure 14-4221. A53SS_SS_ROM_ROM_COMPONID0_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12740. A53SS_SS_ROM_ROM_COMPONID0_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.106 A53SS_SS_ROM_ROM_COMPONID1_VAL Register

1 A53SS_SS_ROM_ROM_COMPONID1_VAL Register (Offset = FF4h) [reset = 0h]

ROM Component ID 1

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Table 14-12741. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FF4h**

Figure 14-4222. A53SS_SS_ROM_ROM_COMPONID1_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12743. A53SS_SS_ROM_ROM_COMPONID1_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.107 A53SS_SS_ROM_ROM_COMPONID2_VAL Register

1 A53SS_SS_ROM_ROM_COMPONID2_VAL Register (Offset = FF8h) [reset = 0h]

ROM Component ID 2

Return to Summary Table

Table 14-12744. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FF8h**

Figure 14-4223. A53SS_SS_ROM_ROM_COMPONID2_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12746. A53SS_SS_ROM_ROM_COMPONID2_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.108 A53SS_SS_ROM_ROM_COMPONID3_VAL Register

1 A53SS_SS_ROM_ROM_COMPONID3_VAL Register (Offset = FFCh) [reset = 0h]

ROM Component ID 3

Return to Summary Table

Table 14-12747. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FFCh**

Figure 14-4224. A53SS_SS_ROM_ROM_COMPONID3_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-12749. A53SS_SS_ROM_ROM_COMPONID3_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.109 A53SS_CORE0_DBG_EDESR Register

1 A53SS_CORE0_DBG_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

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Table 14-12750. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0020h**

Figure 14-4225. A53SS_CORE0_DBG_EDESR Name Register

31	30	29	28	27	26	25	24
RES0_EDESR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDESR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDESR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDESR_31_3					SS	RC	OSUC
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-12752. A53SS_CORE0_DBG_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.110 A53SS_CORE0_DBG_EDECR Register

1 A53SS_CORE0_DBG_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

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Table 14-12753. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0024h**

Figure 14-4226. A53SS_CORE0_DBG_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDECR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDECR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-12755. A53SS_CORE0_DBG_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.111 A53SS_CORE0_DBG_EDWAR_31_0 Register

1 A53SS_CORE0_DBG_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

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Table 14-12756. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0030h**

Figure 14-4227. A53SS_CORE0_DBG_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-12758. A53SS_CORE0_DBG_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.112 A53SS_CORE0_DBG_EDWAR_63_32 Register

1 A53SS_CORE0_DBG_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

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Table 14-12759. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0034h**

Figure 14-4228. A53SS_CORE0_DBG_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-12761. A53SS_CORE0_DBG_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.113 A53SS_CORE0_DBG_DBGDTRRX_EL0 Register

1 A53SS_CORE0_DBG_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

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Table 14-12762. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0080h**

Figure 14-4229. A53SS_CORE0_DBG_DBGDTRRX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRRX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRRX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRRX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRRX_EL0							
R/W							
0h							

Table 14-12764. A53SS_CORE0_DBG_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.114 A53SS_CORE0_DBG_EDITR Register

1 A53SS_CORE0_DBG_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-12765. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0084h**

Figure 14-4230. A53SS_CORE0_DBG_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-12767. A53SS_CORE0_DBG_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.115 A53SS_CORE0_DBG_EDSCR Register

1 A53SS_CORE0_DBG_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

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Table 14-12768. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0088h**

Figure 14-4231. A53SS_CORE0_DBG_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	6	5	4	3	2	1	0
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-12770. A53SS_CORE0_DBG_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-12770. A53SS_CORE0_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-12770. A53SS_CORE0_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-12770. A53SS_CORE0_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.116 A53SS_CORE0_DBG_DBGDTRTX_EL0 Register

1 A53SS_CORE0_DBG_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-12771. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 008Ch**

Figure 14-4232. A53SS_CORE0_DBG_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-12773. A53SS_CORE0_DBG_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.117 A53SS_CORE0_DBG_EDRCR Register

1 A53SS_CORE0_DBG_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-12774. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0090h**

Figure 14-4233. A53SS_CORE0_DBG_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDRCR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDRCR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-12776. A53SS_CORE0_DBG_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-12776. A53SS_CORE0_DBG_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.118 A53SS_CORE0_DBG_EDACR Register

1 A53SS_CORE0_DBG_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-12777. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0094h**

Figure 14-4234. A53SS_CORE0_DBG_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-12779. A53SS_CORE0_DBG_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.119 A53SS_CORE0_DBG_EDECCR Register

1 A53SS_CORE0_DBG_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-12780. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0098h**

Figure 14-4235. A53SS_CORE0_DBG_EDECCR Name Register

31	30	29	28	27	26	25	24
RES0_EDECCR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDECCR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDECCR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
NSE				SE			
R/W				R/W			
0h				0h			

Table 14-12782. A53SS_CORE0_DBG_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-12782. A53SS_CORE0_DBG_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.120 A53SS_CORE0_DBG_EDPCSR_31_0 Register

1 A53SS_CORE0_DBG_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-12783. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A0h**

Figure 14-4236. A53SS_CORE0_DBG_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_31_0							
R/W							
0h							

Table 14-12785. A53SS_CORE0_DBG_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31:0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.121 A53SS_CORE0_DBG_EDCIDSR Register

1 A53SS_CORE0_DBG_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-12786. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A4h**

Figure 14-4237. A53SS_CORE0_DBG_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CONTEXTIDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CONTEXTIDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONTEXTIDR							
R/W							
0h							

Table 14-12788. A53SS_CORE0_DBG_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.122 A53SS_CORE0_DBG_EDVIDSR Register

1 A53SS_CORE0_DBG_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-12789. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A8h**

Figure 14-4238. A53SS_CORE0_DBG_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-12791. A53SS_CORE0_DBG_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63:32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63:32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.123 A53SS_CORE0_DBG_EDPCSR_63_32 Register

1 A53SS_CORE0_DBG_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-12792. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00ACh**

Figure 14-4239. A53SS_CORE0_DBG_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_63_32							
R/W							
0h							

Table 14-12794. A53SS_CORE0_DBG_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63:32] of the sampled PC.

14.3.1.1.2.124 A53SS_CORE0_DBG_OSLAR_EL1 Register

1 A53SS_CORE0_DBG_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-12795. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0300h**

Figure 14-4240. A53SS_CORE0_DBG_OSLAR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_OSLAR_EL1_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_OSLAR_EL1_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_OSLAR_EL1_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_OSLAR_EL1_31_1							OSLK
R/W							R/W
0h							0h

Table 14-12797. A53SS_CORE0_DBG_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.125 A53SS_CORE0_DBG_EDPRCR Register

1 A53SS_CORE0_DBG_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-12798. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0310h**

Figure 14-4241. A53SS_CORE0_DBG_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPRCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPRCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-12800. A53SS_CORE0_DBG_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-12800. A53SS_CORE0_DBG_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.126 A53SS_CORE0_DBG_EDPRSR Register

1 A53SS_CORE0_DBG_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-12801. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0314h**

Figure 14-4242. A53SS_CORE0_DBG_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPRSR_31_12							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-12803. A53SS_CORE0_DBG_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-12803. A53SS_CORE0_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-12803. A53SS_CORE0_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.127 A53SS_CORE0_DBG_DBGBVR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12804. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0400h**

Figure 14-4243. A53SS_CORE0_DBG_DBGBVR0_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGBVR0_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGBVR0_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGBVR0_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGBVR0_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12806. A53SS_CORE0_DBG_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.128 A53SS_CORE0_DBG_DBGBVR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12807. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0404h**

Figure 14-4244. A53SS_CORE0_DBG_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR0_EL1_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR0_EL1_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-12809. A53SS_CORE0_DBG_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.129 A53SS_CORE0_DBG_DBGBCR0_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-12810. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0408h**

Figure 14-4245. A53SS_CORE0_DBG_DBGBCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR0_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR0_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR0_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12812. A53SS_CORE0_DBG_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12812. A53SS_CORE0_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12812. A53SS_CORE0_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.130 A53SS_CORE0_DBG_DBGBVR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12813. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0410h**

Figure 14-4246. A53SS_CORE0_DBG_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-12815. A53SS_CORE0_DBG_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.131 A53SS_CORE0_DBG_DBGBVR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12816. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0414h**

Figure 14-4247. A53SS_CORE0_DBG_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR1_EL1_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR1_EL1_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-12818. A53SS_CORE0_DBG_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.132 A53SS_CORE0_DBG_DBGBCR1_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-12819. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0418h**

Figure 14-4248. A53SS_CORE0_DBG_DBGBCR1_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR1_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR1_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR1_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-12821. A53SS_CORE0_DBG_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12821. A53SS_CORE0_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12821. A53SS_CORE0_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.133 A53SS_CORE0_DBG_DBGBVR2_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12822. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0420h**

Figure 14-4249. A53SS_CORE0_DBG_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-12824. A53SS_CORE0_DBG_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.134 A53SS_CORE0_DBG_DBGBVR2_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12825. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0424h**

Figure 14-4250. A53SS_CORE0_DBG_DBGBVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR2_EL1_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR2_EL1_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR2_EL1_63_32							
R/W							
0h							

Table 14-12827. A53SS_CORE0_DBG_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.135 A53SS_CORE0_DBG_DBGBCR2_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-12828. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0428h**

Figure 14-4251. A53SS_CORE0_DBG_DBGBCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR2_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR2_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR2_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12830. A53SS_CORE0_DBG_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12830. A53SS_CORE0_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12830. A53SS_CORE0_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.136 A53SS_CORE0_DBG_DBGBVR3_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12831. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0430h**

Figure 14-4252. A53SS_CORE0_DBG_DBGBVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_31_0							
R/W							
0h							

Table 14-12833. A53SS_CORE0_DBG_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.137 A53SS_CORE0_DBG_DBGBVR3_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12834. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0434h**

Figure 14-4253. A53SS_CORE0_DBG_DBGBVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_63_32							
R/W							
0h							

Table 14-12836. A53SS_CORE0_DBG_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.138 A53SS_CORE0_DBG_DBGBCR3_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-12837. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0438h**

Figure 14-4254. A53SS_CORE0_DBG_DBGBCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR3_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR3_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR3_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12839. A53SS_CORE0_DBG_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12839. A53SS_CORE0_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12839. A53SS_CORE0_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.139 A53SS_CORE0_DBG_DBGBVR4_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12840. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0440h**

Figure 14-4255. A53SS_CORE0_DBG_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-12842. A53SS_CORE0_DBG_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.140 A53SS_CORE0_DBG_DBGBVR4_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12843. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0444h**

Figure 14-4256. A53SS_CORE0_DBG_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-12845. A53SS_CORE0_DBG_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.141 A53SS_CORE0_DBG_DBGBCR4_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

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Table 14-12846. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0448h**

Figure 14-4257. A53SS_CORE0_DBG_DBGBCR4_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR4_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR4_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR4_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-12848. A53SS_CORE0_DBG_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12848. A53SS_CORE0_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12848. A53SS_CORE0_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.142 A53SS_CORE0_DBG_DBGBVR5_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12849. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0450h**

Figure 14-4258. A53SS_CORE0_DBG_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR5_EL1_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR5_EL1_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-12851. A53SS_CORE0_DBG_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.143 A53SS_CORE0_DBG_DBGBVR5_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-12852. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0454h**

Figure 14-4259. A53SS_CORE0_DBG_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-12854. A53SS_CORE0_DBG_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.144 A53SS_CORE0_DBG_DBGBCR5_EL1 Register

1 A53SS_CORE0_DBG_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

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Table 14-12855. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0458h**

Figure 14-4260. A53SS_CORE0_DBG_DBGBCR5_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR5_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR5_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR5_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-12857. A53SS_CORE0_DBG_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-12857. A53SS_CORE0_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-12857. A53SS_CORE0_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.145 A53SS_CORE0_DBG_DBGWVR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

Return to Summary Table

Table 14-12858. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0800h**

Figure 14-4261. A53SS_CORE0_DBG_DBGWVR0_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">VA</td><td colspan="2">RES0_DBGWVR0_EL1_31_0_1_0</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12860. A53SS_CORE0_DBG_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.146 A53SS_CORE0_DBG_DBGWVR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

Return to Summary Table

Table 14-12861. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0804h**

Figure 14-4262. A53SS_CORE0_DBG_DBGWVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-12863. A53SS_CORE0_DBG_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.147 A53SS_CORE0_DBG_DBGWCR0_EL1 Register

1 A53SS_CORE0_DBG_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

Return to Summary Table

Table 14-12864. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0808h**

Figure 14-4263. A53SS_CORE0_DBG_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12866. A53SS_CORE0_DBG_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-12866. A53SS_CORE0_DBG_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.148 A53SS_CORE0_DBG_DBGWVR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

Return to Summary Table

Table 14-12867. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0810h**

Figure 14-4264. A53SS_CORE0_DBG_DBGWVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR1_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-12869. A53SS_CORE0_DBG_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.149 A53SS_CORE0_DBG_DBGWVR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

Return to Summary Table

Table 14-12870. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0814h**

Figure 14-4265. A53SS_CORE0_DBG_DBGWVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESS							VA
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA							
R/W							
0h							

Table 14-12872. A53SS_CORE0_DBG_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.150 A53SS_CORE0_DBG_DBGWCR1_EL1 Register

1 A53SS_CORE0_DBG_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

Return to Summary Table

Table 14-12873. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0818h**

Figure 14-4266. A53SS_CORE0_DBG_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12875. A53SS_CORE0_DBG_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-12875. A53SS_CORE0_DBG_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.151 A53SS_CORE0_DBG_DBGWVR2_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

Return to Summary Table

Table 14-12876. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0820h**

Figure 14-4267. A53SS_CORE0_DBG_DBGWVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR2_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-12878. A53SS_CORE0_DBG_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.152 A53SS_CORE0_DBG_DBGWVR2_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

Return to Summary Table

Table 14-12879. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0824h**

Figure 14-4268. A53SS_CORE0_DBG_DBGWVR2_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12881. A53SS_CORE0_DBG_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.153 A53SS_CORE0_DBG_DBGWCR2_EL1 Register

1 A53SS_CORE0_DBG_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

Return to Summary Table

Table 14-12882. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0828h**

Figure 14-4269. A53SS_CORE0_DBG_DBGWCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR2_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR2_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12884. A53SS_CORE0_DBG_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-12884. A53SS_CORE0_DBG_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.154 A53SS_CORE0_DBG_DBGWVR3_EL1_31_0 Register

1 A53SS_CORE0_DBG_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

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Table 14-12885. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0830h**

Figure 14-4270. A53SS_CORE0_DBG_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-12887. A53SS_CORE0_DBG_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.155 A53SS_CORE0_DBG_DBGWVR3_EL1_63_32 Register

1 A53SS_CORE0_DBG_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

Return to Summary Table

Table 14-12888. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0834h**

Figure 14-4271. A53SS_CORE0_DBG_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-12890. A53SS_CORE0_DBG_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.156 A53SS_CORE0_DBG_DBGWCR3_EL1 Register

1 A53SS_CORE0_DBG_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

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Table 14-12891. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0838h**

Figure 14-4272. A53SS_CORE0_DBG_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-12893. A53SS_CORE0_DBG_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-12893. A53SS_CORE0_DBG_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.157 A53SS_CORE0_DBG_MIDR_EL1 Register

1 A53SS_CORE0_DBG_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-12894. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D00h**

Figure 14-4273. A53SS_CORE0_DBG_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-12896. A53SS_CORE0_DBG_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.158 A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

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Table 14-12897. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D20h**

Figure 14-4274. A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EL3				EL2			
R/W				R/W			
2h				2h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-12899. A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-12899. A53SS_CORE0_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.159 A53SS_CORE0_DBG_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

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Table 14-12900. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D24h**

Figure 14-4275. A53SS_CORE0_DBG_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-12902. A53SS_CORE0_DBG_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.160 A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

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Table 14-12903. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D28h**

Figure 14-4276. A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	22	21	20	19	18	17	16
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	14	13	12	11	10	9	8
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	6	5	4	3	2	1	0
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-12905. A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-12905. A53SS_CORE0_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.161 A53SS_CORE0_DBG_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

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Table 14-12906. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D2Ch**

Figure 14-4277. A53SS_CORE0_DBG_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-12908. A53SS_CORE0_DBG_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.162 A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-12909. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D30h**

Figure 14-4278. A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	14	13	12	11	10	9	8
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-12911. A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-12911. A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.163 A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-12912. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D34h**

Figure 14-4279. A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-12914. A53SS_CORE0_DBG_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.164 A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

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Table 14-12915. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D38h**

Figure 14-4280. A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-12917. A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-12917. A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.165 A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

Return to Summary Table

Table 14-12918. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D3Ch**

Figure 14-4281. A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-12920. A53SS_CORE0_DBG_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.166 A53SS_CORE0_DBG_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

Return to Summary Table

Table 14-12921. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D40h**

Figure 14-4282. A53SS_CORE0_DBG_ID_AA64PFR1_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_ID_AA64PFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_ID_AA64PFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_ID_AA64PFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_ID_AA64PFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12923. A53SS_CORE0_DBG_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.167 A53SS_CORE0_DBG_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

Return to Summary Table

Table 14-12924. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D44h**

Figure 14-4283. A53SS_CORE0_DBG_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-12926. A53SS_CORE0_DBG_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.168 A53SS_CORE0_DBG_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

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Table 14-12927. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D48h**

Figure 14-4284. A53SS_CORE0_DBG_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-12929. A53SS_CORE0_DBG_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.169 A53SS_CORE0_DBG_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

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Table 14-12930. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D4Ch**

Figure 14-4285. A53SS_CORE0_DBG_ID_AA64DFR1_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_ID_AA64DFR1_EL1_63_32_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_ID_AA64DFR1_EL1_63_32_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_ID_AA64DFR1_EL1_63_32_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_ID_AA64DFR1_EL1_63_32_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12932. A53SS_CORE0_DBG_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.170 A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

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Table 14-12933. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D50h**

Figure 14-4286. A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-12935. A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.171 A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

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Table 14-12936. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D54h**

Figure 14-4287. A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-12938. A53SS_CORE0_DBG_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.172 A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-12939. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D58h**

Figure 14-4288. A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-12941. A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.173 A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

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Table 14-12942. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D5Ch**

Figure 14-4289. A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-12944. A53SS_CORE0_DBG_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.174 A53SS_CORE0_DBG_EDITCTRL Register

1 A53SS_CORE0_DBG_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

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Table 14-12945. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0F00h**

Figure 14-4290. A53SS_CORE0_DBG_EDITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_EDITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-12947. A53SS_CORE0_DBG_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.175 A53SS_CORE0_DBG_DBGCLAIMSET_EL1 Register

1 A53SS_CORE0_DBG_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-12948. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA0h**

Figure 14-4291. A53SS_CORE0_DBG_DBGCLAIMSET_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
FFh							

Table 14-12950. A53SS_CORE0_DBG_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.176 A53SS_CORE0_DBG_DBGCLAIMCLR_EL1 Register

1 A53SS_CORE0_DBG_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-12951. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA4h**

Figure 14-4292. A53SS_CORE0_DBG_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
0h							

Table 14-12953. A53SS_CORE0_DBG_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.177 A53SS_CORE0_DBG_EDDEVAFF0 Register

1 A53SS_CORE0_DBG_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

External Debug Device Affinity Register 0

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Table 14-12954. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA8h**

Figure 14-4293. A53SS_CORE0_DBG_EDDEVAFF0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EDDEVAFF0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EDDEVAFF0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EDDEVAFF0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000000h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EDDEVAFF0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000000h</td></tr>
</table>

Table 14-12956. A53SS_CORE0_DBG_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.178 A53SS_CORE0_DBG_EDDEVAFF1 Register

1 A53SS_CORE0_DBG_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

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Table 14-12957. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FACh**

Figure 14-4294. A53SS_CORE0_DBG_EDDEVAFF1 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EDDEVAFF1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EDDEVAFF1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDDEVAFF1							
R/W							
0h							

Table 14-12959. A53SS_CORE0_DBG_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.179 A53SS_CORE0_DBG_EDLAR Register

1 A53SS_CORE0_DBG_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

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Table 14-12960. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB0h**

Figure 14-4295. A53SS_CORE0_DBG_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-12962. A53SS_CORE0_DBG_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.180 A53SS_CORE0_DBG_EDLSR Register

1 A53SS_CORE0_DBG_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

Return to Summary Table

Table 14-12963. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB4h**

Figure 14-4296. A53SS_CORE0_DBG_EDLSR Name Register

31	30	29	28	27	26	25	24
RES0_EDLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-12965. A53SS_CORE0_DBG_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.181 A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1 Register

1 A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

Return to Summary Table

Table 14-12966. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB8h**

Figure 14-4297. A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSID		NSID	
R/W		R/W		R/W		R/W	
2h		2h		2h		2h	

Table 14-12968. A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-12968. A53SS_CORE0_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.182 A53SS_CORE0_DBG_EDDEVARCH Register

1 A53SS_CORE0_DBG_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

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Table 14-12969. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3001 0FBCh**

Figure 14-4298. A53SS_CORE0_DBG_EDDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
</table>

Table 14-12971. A53SS_CORE0_DBG_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.183 A53SS_CORE0_DBG_EDDEVID2 Register

1 A53SS_CORE0_DBG_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

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Table 14-12972. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC0h**

Figure 14-4299. A53SS_CORE0_DBG_EDDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID2_31_0							
R/W							
0h							

Table 14-12974. A53SS_CORE0_DBG_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.184 A53SS_CORE0_DBG_EDDEVID1 Register

1 A53SS_CORE0_DBG_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

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Table 14-12975. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC4h**

Figure 14-4300. A53SS_CORE0_DBG_EDDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID1_31_4				PCSROFFSET			
R/W				R/W			
0h				2h			

Table 14-12977. A53SS_CORE0_DBG_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.185 A53SS_CORE0_DBG_EDDEVID Register

1 A53SS_CORE0_DBG_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

Return to Summary Table

Table 14-12978. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC8h**

Figure 14-4301. A53SS_CORE0_DBG_EDDEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RES0_EDDEVID_31_28</td><td colspan="4">AUXREGS</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDDEVID_23_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDDEVID_23_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RES0_EDDEVID_23_4</td><td colspan="4">PCSAMPLE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">3h</td></tr>
</table>

Table 14-12980. A53SS_CORE0_DBG_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.186 A53SS_CORE0_DBG_EDDEVTYPE Register

1 A53SS_CORE0_DBG_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

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Table 14-12981. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FCCh**

Figure 14-4302. A53SS_CORE0_DBG_EDDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				5h			

Table 14-12983. A53SS_CORE0_DBG_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.187 A53SS_CORE0_DBG_EDPIDR4 Register

1 A53SS_CORE0_DBG_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

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Table 14-12984. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FD0h**

Figure 14-4303. A53SS_CORE0_DBG_EDPIDR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-12986. A53SS_CORE0_DBG_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.188 A53SS_CORE0_DBG_EDPIDR0 Register

1 A53SS_CORE0_DBG_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

Return to Summary Table

Table 14-12987. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE0h**

Figure 14-4304. A53SS_CORE0_DBG_EDPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
3h							

Table 14-12989. A53SS_CORE0_DBG_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.189 A53SS_CORE0_DBG_EDPIDR1 Register

1 A53SS_CORE0_DBG_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

Return to Summary Table

Table 14-12990. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE4h**

Figure 14-4305. A53SS_CORE0_DBG_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-12992. A53SS_CORE0_DBG_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.190 A53SS_CORE0_DBG_EDPIDR2 Register

1 A53SS_CORE0_DBG_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

Return to Summary Table

Table 14-12993. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE8h**

Figure 14-4306. A53SS_CORE0_DBG_EDPIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">3h</td></tr>
</table>

Table 14-12995. A53SS_CORE0_DBG_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.191 A53SS_CORE0_DBG_EDPIDR3 Register

1 A53SS_CORE0_DBG_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

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Table 14-12996. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FECh**

Figure 14-4307. A53SS_CORE0_DBG_EDPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-12998. A53SS_CORE0_DBG_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.192 A53SS_CORE0_DBG_EDCIDR0 Register

1 A53SS_CORE0_DBG_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

Return to Summary Table

Table 14-12999. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF0h**

Figure 14-4308. A53SS_CORE0_DBG_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-13001. A53SS_CORE0_DBG_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.193 A53SS_CORE0_DBG_EDCIDR1 Register

1 A53SS_CORE0_DBG_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

Return to Summary Table

Table 14-13002. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF4h**

Figure 14-4309. A53SS_CORE0_DBG_EDCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-13004. A53SS_CORE0_DBG_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.194 A53SS_CORE0_DBG_EDCIDR2 Register

1 A53SS_CORE0_DBG_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

Return to Summary Table

Table 14-13005. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF8h**

Figure 14-4310. A53SS_CORE0_DBG_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-13007. A53SS_CORE0_DBG_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.195 A53SS_CORE0_DBG_EDCIDR3 Register

1 A53SS_CORE0_DBG_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

Return to Summary Table

Table 14-13008. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FFCh**

Figure 14-4311. A53SS_CORE0_DBG_EDCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-13010. A53SS_CORE0_DBG_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.196 A53SS_CORE0_CTI_CTICONTROL Register

1 A53SS_CORE0_CTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

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Table 14-13011. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0000h**

Figure 14-4312. A53SS_CORE0_CTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICONTROL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICONTROL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-13013. A53SS_CORE0_CTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.197 A53SS_CORE0_CTI_CTIINTACK Register

1 A53SS_CORE0_CTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

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Table 14-13014. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0010h**

Figure 14-4313. A53SS_CORE0_CTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ACK_N							
R/W							
0h							

Table 14-13016. A53SS_CORE0_CTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.198 A53SS_CORE0_CTI_CTIAPPSET Register

1 A53SS_CORE0_CTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

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Table 14-13017. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0014h**

Figure 14-4314. A53SS_CORE0_CTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-13019. A53SS_CORE0_CTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.199 A53SS_CORE0_CTI_CTIAPPCLEAR Register

1 A53SS_CORE0_CTI_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

Return to Summary Table

Table 14-13020. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0018h**

Figure 14-4315. A53SS_CORE0_CTI_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPCLEAR_31_4				CTIAPPCLEARX			
R/W				R/W			
0h				0h			

Table 14-13022. A53SS_CORE0_CTI_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.200 A53SS_CORE0_CTI_CTIAPPPULSE Register

1 A53SS_CORE0_CTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

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Table 14-13023. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 001Ch**

Figure 14-4316. A53SS_CORE0_CTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPPULSE_31_4				CTIAPPPULSEX			
R/W				R/W			
0h				0h			

Table 14-13025. A53SS_CORE0_CTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.201 A53SS_CORE0_CTI_CTIINEN0 Register

1 A53SS_CORE0_CTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

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Table 14-13026. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0020h**

Figure 14-4317. A53SS_CORE0_CTI_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN0_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13028. A53SS_CORE0_CTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.202 A53SS_CORE0_CTI_CTIINEN1 Register

1 A53SS_CORE0_CTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

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Table 14-13029. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0024h**

Figure 14-4318. A53SS_CORE0_CTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13031. A53SS_CORE0_CTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.203 A53SS_CORE0_CTI_CTIINEN2 Register

1 A53SS_CORE0_CTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

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Table 14-13032. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0028h**

Figure 14-4319. A53SS_CORE0_CTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN2_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN2_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN2_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN2_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13034. A53SS_CORE0_CTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.204 A53SS_CORE0_CTI_CTIINEN3 Register

1 A53SS_CORE0_CTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-13035. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 002Ch**

Figure 14-4320. A53SS_CORE0_CTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN3_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN3_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN3_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN3_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13037. A53SS_CORE0_CTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.205 A53SS_CORE0_CTI_CTIINEN4 Register

1 A53SS_CORE0_CTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

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Table 14-13038. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0030h**

Figure 14-4321. A53SS_CORE0_CTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13040. A53SS_CORE0_CTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.206 A53SS_CORE0_CTI_CTIINEN5 Register

1 A53SS_CORE0_CTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-13041. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0034h**

Figure 14-4322. A53SS_CORE0_CTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13043. A53SS_CORE0_CTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.207 A53SS_CORE0_CTI_CTIINEN6 Register

1 A53SS_CORE0_CTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-13044. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0038h**

Figure 14-4323. A53SS_CORE0_CTI_CTIINEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN6_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN6_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN6_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN6_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13046. A53SS_CORE0_CTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.208 A53SS_CORE0_CTI_CTIINEN7 Register

1 A53SS_CORE0_CTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-13047. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 003Ch**

Figure 14-4324. A53SS_CORE0_CTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-13049. A53SS_CORE0_CTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.209 A53SS_CORE0_CTI_CTIOUTEN0 Register

1 A53SS_CORE0_CTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-13050. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A0h**

Figure 14-4325. A53SS_CORE0_CTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN0_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13052. A53SS_CORE0_CTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.210 A53SS_CORE0_CTI_CTIOUTEN1 Register

1 A53SS_CORE0_CTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

Return to Summary Table

Table 14-13053. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A4h**

Figure 14-4326. A53SS_CORE0_CTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN1_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13055. A53SS_CORE0_CTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.211 A53SS_CORE0_CTI_CTIOUTEN2 Register

1 A53SS_CORE0_CTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

Return to Summary Table

Table 14-13056. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A8h**

Figure 14-4327. A53SS_CORE0_CTI_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIOUTEN2_31_4</td><td colspan="4">OUTENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13058. A53SS_CORE0_CTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.212 A53SS_CORE0_CTI_CTIOUTEN3 Register

1 A53SS_CORE0_CTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

Return to Summary Table

Table 14-13059. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00ACh**

Figure 14-4328. A53SS_CORE0_CTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13061. A53SS_CORE0_CTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.213 A53SS_CORE0_CTI_CTIOUTEN4 Register

1 A53SS_CORE0_CTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

Return to Summary Table

Table 14-13062. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B0h**

Figure 14-4329. A53SS_CORE0_CTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13064. A53SS_CORE0_CTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.214 A53SS_CORE0_CTI_CTIOUTEN5 Register

1 A53SS_CORE0_CTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

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Table 14-13065. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B4h**

Figure 14-4330. A53SS_CORE0_CTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13067. A53SS_CORE0_CTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.215 A53SS_CORE0_CTI_CTIOUTEN6 Register

1 A53SS_CORE0_CTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

Return to Summary Table

Table 14-13068. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B8h**

Figure 14-4331. A53SS_CORE0_CTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13070. A53SS_CORE0_CTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.216 A53SS_CORE0_CTI_CTIOUTEN7 Register

1 A53SS_CORE0_CTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

Return to Summary Table

Table 14-13071. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00BCh**

Figure 14-4332. A53SS_CORE0_CTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-13073. A53SS_CORE0_CTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.217 A53SS_CORE0_CTI_CTITRIGINSTATUS Register

1 A53SS_CORE0_CTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-13074. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0130h**

Figure 14-4333. A53SS_CORE0_CTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TRINN							
R/W							
0h							

Table 14-13076. A53SS_CORE0_CTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.218 A53SS_CORE0_CTI_CTITRIGOUTSTATUS Register

1 A53SS_CORE0_CTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

Return to Summary Table

Table 14-13077. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0134h**

Figure 14-4334. A53SS_CORE0_CTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TROUTN							
R/W							
0h							

Table 14-13079. A53SS_CORE0_CTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.219 A53SS_CORE0_CTI_CTICHINSTATUS Register

1 A53SS_CORE0_CTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-13080. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0138h**

Figure 14-4335. A53SS_CORE0_CTI_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTICHINSTATUS_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTICHINSTATUS_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTICHINSTATUS_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTICHINSTATUS_31_4</td><td colspan="4">CHINN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13082. A53SS_CORE0_CTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.220 A53SS_CORE0_CTI_CTICHOUTSTATUS Register

1 A53SS_CORE0_CTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-13083. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 013Ch**

Figure 14-4336. A53SS_CORE0_CTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-13085. A53SS_CORE0_CTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.221 A53SS_CORE0_CTI_CTIGATE Register

1 A53SS_CORE0_CTI_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

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Table 14-13086. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0140h**

Figure 14-4337. A53SS_CORE0_CTI_CTIGATE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIGATE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIGATE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIGATE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIGATE_31_4</td><td colspan="4">GATEX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-13088. A53SS_CORE0_CTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.222 A53SS_CORE0_CTI_ASICCTL Register

1 A53SS_CORE0_CTI_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

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Table 14-13089. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0144h**

Figure 14-4338. A53SS_CORE0_CTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-13091. A53SS_CORE0_CTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.223 A53SS_CORE0_CTI_CTIITCTRL Register

1 A53SS_CORE0_CTI_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

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Table 14-13092. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0F00h**

Figure 14-4339. A53SS_CORE0_CTI_CTIITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_CTIITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-13094. A53SS_CORE0_CTI_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.224 A53SS_CORE0_CTI_CTICLAIMSET Register

1 A53SS_CORE0_CTI_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-13095. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA0h**

Figure 14-4340. A53SS_CORE0_CTI_CTICLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMSET_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMSET_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMSET_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTICLAIMSET_31_4</td><td colspan="4">CLAIMX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-13097. A53SS_CORE0_CTI_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.225 A53SS_CORE0_CTI_CTICLAIMCLR Register

1 A53SS_CORE0_CTI_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

Return to Summary Table

Table 14-13098. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA4h**

Figure 14-4341. A53SS_CORE0_CTI_CTICLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMCLR_31_4				CLAIMX			
R/W				R/W			
0h				0h			

Table 14-13100. A53SS_CORE0_CTI_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.226 A53SS_CORE0_CTI_CTIDEVAFF0 Register

1 A53SS_CORE0_CTI_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

CTI Device Affinity Register 0

Return to Summary Table

Table 14-13101. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA8h**

Figure 14-4342. A53SS_CORE0_CTI_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000000h							
23	22	21	20	19	18	17	16
CTIDEVAFF0							
R/W							
80000000h							
15	14	13	12	11	10	9	8
CTIDEVAFF0							
R/W							
80000000h							
7	6	5	4	3	2	1	0
CTIDEVAFF0							
R/W							
80000000h							

Table 14-13103. A53SS_CORE0_CTI_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.227 A53SS_CORE0_CTI_CTIDEVAFF1 Register

1 A53SS_CORE0_CTI_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-13104. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FACh**

Figure 14-4343. A53SS_CORE0_CTI_CTIDEVAFF1 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
CTIDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
CTIDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
CTIDEVAFF1							
R/W							
0h							

Table 14-13106. A53SS_CORE0_CTI_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.228 A53SS_CORE0_CTI_CTILAR Register

1 A53SS_CORE0_CTI_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

Return to Summary Table

Table 14-13107. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB0h**

Figure 14-4344. A53SS_CORE0_CTI_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-13109. A53SS_CORE0_CTI_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.229 A53SS_CORE0_CTI_CTILSR Register

1 A53SS_CORE0_CTI_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-13110. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB4h**

Figure 14-4345. A53SS_CORE0_CTI_CTILSR Name Register

31	30	29	28	27	26	25	24
RES0_CTILSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTILSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTILSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTILSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13112. A53SS_CORE0_CTI_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.230 A53SS_CORE0_CTI_CTIAUTHSTATUS Register

1 A53SS_CORE0_CTI_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-13113. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB8h**

Figure 14-4346. A53SS_CORE0_CTI_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-13115. A53SS_CORE0_CTI_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.231 A53SS_CORE0_CTI_CTIDEVARCH Register

1 A53SS_CORE0_CTI_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

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Table 14-13116. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FBCh**

Figure 14-4347. A53SS_CORE0_CTI_CTIDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
</table>

Table 14-13118. A53SS_CORE0_CTI_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.232 A53SS_CORE0_CTI_CTIDEVID2 Register

1 A53SS_CORE0_CTI_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

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Table 14-13119. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC0h**

Figure 14-4348. A53SS_CORE0_CTI_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-13121. A53SS_CORE0_CTI_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.233 A53SS_CORE0_CTI_CTIDEVID1 Register

1 A53SS_CORE0_CTI_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

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Table 14-13122. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC4h**

Figure 14-4349. A53SS_CORE0_CTI_CTIDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID1_31_0							
R/W							
0h							

Table 14-13124. A53SS_CORE0_CTI_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.234 A53SS_CORE0_CTI_CTIDEVID Register

1 A53SS_CORE0_CTI_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

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Table 14-13125. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC8h**

Figure 14-4350. A53SS_CORE0_CTI_CTIDEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RES0_CTIDEVID_31_26</td><td colspan="2">INOUT</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_CTIDEVID_23_22</td><td colspan="6">NUMCHAN</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RES0_CTIDEVID_15_14</td><td colspan="6">NUMTRIG</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_CTIDEVID_7_5</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-13127. A53SS_CORE0_CTI_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-13127. A53SS_CORE0_CTI_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.235 A53SS_CORE0_CTI_CTIDEVTYPE Register

1 A53SS_CORE0_CTI_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-13128. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FCCh**

Figure 14-4351. A53SS_CORE0_CTI_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-13130. A53SS_CORE0_CTI_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.236 A53SS_CORE0_CTI_CTIPIDR4 Register

1 A53SS_CORE0_CTI_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-13131. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD0h**

Figure 14-4352. A53SS_CORE0_CTI_CTIPIDR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-13133. A53SS_CORE0_CTI_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.237 A53SS_CORE0_CTI_CTIPIDR5 Register

1 A53SS_CORE0_CTI_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

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Table 14-13134. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD4h**

Figure 14-4353. A53SS_CORE0_CTI_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-13136. A53SS_CORE0_CTI_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.238 A53SS_CORE0_CTI_CTIPIDR6 Register

1 A53SS_CORE0_CTI_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

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Table 14-13137. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD8h**

Figure 14-4354. A53SS_CORE0_CTI_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-13139. A53SS_CORE0_CTI_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.239 A53SS_CORE0_CTI_CTIPIDR7 Register

1 A53SS_CORE0_CTI_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

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Table 14-13140. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FDCh**

Figure 14-4355. A53SS_CORE0_CTI_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-13142. A53SS_CORE0_CTI_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.240 A53SS_CORE0_CTI_CTIPIDR0 Register

1 A53SS_CORE0_CTI_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

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Table 14-13143. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE0h**

Figure 14-4356. A53SS_CORE0_CTI_CTIPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
A8h							

Table 14-13145. A53SS_CORE0_CTI_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.241 A53SS_CORE0_CTI_CTIPIDR1 Register

1 A53SS_CORE0_CTI_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

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Table 14-13146. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE4h**

Figure 14-4357. A53SS_CORE0_CTI_CTIPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-13148. A53SS_CORE0_CTI_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.242 A53SS_CORE0_CTI_CTIPIDR2 Register

1 A53SS_CORE0_CTI_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

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Table 14-13149. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE8h**

Figure 14-4358. A53SS_CORE0_CTI_CTIPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-13151. A53SS_CORE0_CTI_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.243 A53SS_CORE0_CTI_CTIPIDR3 Register

1 A53SS_CORE0_CTI_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

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Table 14-13152. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FECh**

Figure 14-4359. A53SS_CORE0_CTI_CTIPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-13154. A53SS_CORE0_CTI_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.244 A53SS_CORE0_CTI_CTICIDR0 Register

1 A53SS_CORE0_CTI_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

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Table 14-13155. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF0h**

Figure 14-4360. A53SS_CORE0_CTI_CTICIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTICIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTICIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTICIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-13157. A53SS_CORE0_CTI_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.245 A53SS_CORE0_CTI_CTICIDR1 Register

1 A53SS_CORE0_CTI_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

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Table 14-13158. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF4h**

Figure 14-4361. A53SS_CORE0_CTI_CTICIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-13160. A53SS_CORE0_CTI_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.246 A53SS_CORE0_CTI_CTICIDR2 Register

1 A53SS_CORE0_CTI_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

Return to Summary Table

Table 14-13161. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF8h**

Figure 14-4362. A53SS_CORE0_CTI_CTICIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-13163. A53SS_CORE0_CTI_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.247 A53SS_CORE0_CTI_CTICIDR3 Register

1 A53SS_CORE0_CTI_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

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Table 14-13164. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FFCh**

Figure 14-4363. A53SS_CORE0_CTI_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-13166. A53SS_CORE0_CTI_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.248 A53SS_CORE0_PMU_PMEVCNTR0_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

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Table 14-13167. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0000h**

Figure 14-4364. A53SS_CORE0_PMU_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-13169. A53SS_CORE0_PMU_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.249 A53SS_CORE0_PMU_PMEVCNTR1_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

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Table 14-13170. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0008h**

Figure 14-4365. A53SS_CORE0_PMU_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-13172. A53SS_CORE0_PMU_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.250 A53SS_CORE0_PMU_PMEVCNTR2_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

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Table 14-13173. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0010h**

Figure 14-4366. A53SS_CORE0_PMU_PMEVCNTR2_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR2_EL0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PMEVCNTR2_EL0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMEVCNTR2_EL0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMEVCNTR2_EL0							
R/W							
0h							

Table 14-13175. A53SS_CORE0_PMU_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.251 A53SS_CORE0_PMU_PMEVCNTR3_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

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Table 14-13176. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0018h**

Figure 14-4367. A53SS_CORE0_PMU_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-13178. A53SS_CORE0_PMU_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.252 A53SS_CORE0_PMU_PMEVCNTR4_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

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Table 14-13179. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0020h**

Figure 14-4368. A53SS_CORE0_PMU_PMEVCNTR4_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR4_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR4_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR4_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR4_EL0							
R/W							
0h							

Table 14-13181. A53SS_CORE0_PMU_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.253 A53SS_CORE0_PMU_PMEVCNTR5_EL0 Register

1 A53SS_CORE0_PMU_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

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Table 14-13182. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0028h**

Figure 14-4369. A53SS_CORE0_PMU_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR5_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR5_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-13184. A53SS_CORE0_PMU_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.254 A53SS_CORE0_PMU_PMCCNTR_EL0_31_0 Register

1 A53SS_CORE0_PMU_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

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Table 14-13185. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 00F8h**

Figure 14-4370. A53SS_CORE0_PMU_PMCCNTR_EL0_31_0 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-13187. A53SS_CORE0_PMU_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.255 A53SS_CORE0_PMU_PMCCNTR_EL0_63_32 Register

1 A53SS_CORE0_PMU_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

Return to Summary Table

Table 14-13188. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 00FCh**

Figure 14-4371. A53SS_CORE0_PMU_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-13190. A53SS_CORE0_PMU_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.256 A53SS_CORE0_PMU_PMEVTYPER0_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

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Table 14-13191. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0400h**

Figure 14-4372. A53SS_CORE0_PMU_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13193. A53SS_CORE0_PMU_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13193. A53SS_CORE0_PMU_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.257 A53SS_CORE0_PMU_PMEVTYPER1_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

Return to Summary Table

Table 14-13194. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0404h**

Figure 14-4373. A53SS_CORE0_PMU_PMEVTYPER1_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER1_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER1_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER1_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13196. A53SS_CORE0_PMU_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13196. A53SS_CORE0_PMU_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.258 A53SS_CORE0_PMU_PMEVTYPER2_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

Return to Summary Table

Table 14-13197. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0408h**

Figure 14-4374. A53SS_CORE0_PMU_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-13199. A53SS_CORE0_PMU_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13199. A53SS_CORE0_PMU_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.259 A53SS_CORE0_PMU_PMEVTYPER3_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-13200. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 040Ch**

Figure 14-4375. A53SS_CORE0_PMU_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13202. A53SS_CORE0_PMU_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13202. A53SS_CORE0_PMU_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.260 A53SS_CORE0_PMU_PMEVTYPER4_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

Return to Summary Table

Table 14-13203. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0410h**

Figure 14-4376. A53SS_CORE0_PMU_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13205. A53SS_CORE0_PMU_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13205. A53SS_CORE0_PMU_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.261 A53SS_CORE0_PMU_PMEVTYPER5_EL0 Register

1 A53SS_CORE0_PMU_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

Return to Summary Table

Table 14-13206. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0414h**

Figure 14-4377. A53SS_CORE0_PMU_PMEVTYPER5_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER5_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER5_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER5_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13208. A53SS_CORE0_PMU_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13208. A53SS_CORE0_PMU_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.262 A53SS_CORE0_PMU_PMCCFILTR_EL0 Register

1 A53SS_CORE0_PMU_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

Return to Summary Table

Table 14-13209. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 047Ch**

Figure 14-4378. A53SS_CORE0_PMU_PMCCFILTR_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>P</td><td>U</td><td>NSK</td><td>NSU</td><td>NSH</td><td>M</td><td colspan="2">RES0_PMCCFILTR_EL0_25_0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMCCFILTR_EL0_25_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMCCFILTR_EL0_25_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_PMCCFILTR_EL0_25_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13211. A53SS_CORE0_PMU_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-13211. A53SS_CORE0_PMU_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.263 A53SS_CORE0_PMU_PMCNTENSET_EL0 Register

1 A53SS_CORE0_PMU_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

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Table 14-13212. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C00h**

Figure 14-4379. A53SS_CORE0_PMU_PMCNTENSET_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>C</td><td colspan="7">P_X</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13214. A53SS_CORE0_PMU_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.264 A53SS_CORE0_PMU_PMCNTENCLR_EL0 Register

1 A53SS_CORE0_PMU_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

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Table 14-13215. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C20h**

Figure 14-4380. A53SS_CORE0_PMU_PMCNTENCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13217. A53SS_CORE0_PMU_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.265 A53SS_CORE0_PMU_PMINTENSET_EL1 Register

1 A53SS_CORE0_PMU_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

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Table 14-13218. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C40h**

Figure 14-4381. A53SS_CORE0_PMU_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13220. A53SS_CORE0_PMU_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.266 A53SS_CORE0_PMU_PMINTENCLR_EL1 Register

1 A53SS_CORE0_PMU_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

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Table 14-13221. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C60h**

Figure 14-4382. A53SS_CORE0_PMU_PMINTENCLR_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13223. A53SS_CORE0_PMU_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.267 A53SS_CORE0_PMU_PMOVSCLR_EL0 Register

1 A53SS_CORE0_PMU_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

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Table 14-13224. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C80h**

Figure 14-4383. A53SS_CORE0_PMU_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13226. A53SS_CORE0_PMU_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.268 A53SS_CORE0_PMU_PMSWINC_EL0 Register

1 A53SS_CORE0_PMU_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

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Table 14-13227. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0CA0h**

Figure 14-4384. A53SS_CORE0_PMU_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-13229. A53SS_CORE0_PMU_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.269 A53SS_CORE0_PMU_PMOVSSET_EL0 Register

1 A53SS_CORE0_PMU_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

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Table 14-13230. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0CC0h**

Figure 14-4385. A53SS_CORE0_PMU_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13232. A53SS_CORE0_PMU_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.270 A53SS_CORE0_PMU_PMCFGR Register

1 A53SS_CORE0_PMU_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-13233. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E00h**

Figure 14-4386. A53SS_CORE0_PMU_PMCFGR Name Register

31	30	29	28	27	26	25	24
RES0_PMCFGR_31_20							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCFGR_31_20				UEN	WT	NA	EX
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	1h
15	14	13	12	11	10	9	8
CCD	CC	SIZE					
R/W	R/W	R/W					
1h	1h	3Fh					
7	6	5	4	3	2	1	0
N							
R/W							
6h							

Table 14-13235. A53SS_CORE0_PMU_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-13235. A53SS_CORE0_PMU_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.271 A53SS_CORE0_PMU_PMCR_EL0 Register

1 A53SS_CORE0_PMU_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-13236. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E04h**

Figure 14-4387. A53SS_CORE0_PMU_PMCR_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCR_EL0_31_11							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCR_EL0_31_11							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCR_EL0_31_11					RES0_PMCR_EL0_10_7		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMCR_EL0_10_7	LC	DP	X	D	C	P	E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13238. A53SS_CORE0_PMU_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-13238. A53SS_CORE0_PMU_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.272 A53SS_CORE0_PMU_PMCEID0_EL0 Register

1 A53SS_CORE0_PMU_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-13239. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E20h**

Figure 14-4388. A53SS_CORE0_PMU_PMCEID0_EL0 Name Register

31	30	29	28	27	26	25	24
CE_31_0							
R/W							
67FFBFFFh							
23	22	21	20	19	18	17	16
CE_31_0							
R/W							
67FFBFFFh							
15	14	13	12	11	10	9	8
CE_31_0							
R/W							
67FFBFFFh							
7	6	5	4	3	2	1	0
CE_31_0							
R/W							
67FFBFFFh							

Table 14-13241. A53SS_CORE0_PMU_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.273 A53SS_CORE0_PMU_PMCEID1_EL0 Register

1 A53SS_CORE0_PMU_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-13242. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E24h**

Figure 14-4389. A53SS_CORE0_PMU_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-13244. A53SS_CORE0_PMU_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.274 A53SS_CORE0_PMU_PMITCTRL Register

1 A53SS_CORE0_PMU_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-13245. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0F00h**

Figure 14-4390. A53SS_CORE0_PMU_PMITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_PMITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-13247. A53SS_CORE0_PMU_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.275 A53SS_CORE0_PMU_PMDEVAFF0 Register

1 A53SS_CORE0_PMU_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

Performance Monitors Device Affinity Register 0

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Table 14-13248. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FA8h**

Figure 14-4391. A53SS_CORE0_PMU_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000000h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000000h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000000h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000000h							

Table 14-13250. A53SS_CORE0_PMU_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.276 A53SS_CORE0_PMU_PMDEVAFF1 Register

1 A53SS_CORE0_PMU_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-13251. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3003 0FACh**

Figure 14-4392. A53SS_CORE0_PMU_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
PMDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
PMDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
PMDEVAFF1							
R/W							
0h							

Table 14-13253. A53SS_CORE0_PMU_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.277 A53SS_CORE0_PMU_PMLAR Register

1 A53SS_CORE0_PMU_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

Return to Summary Table

Table 14-13254. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FB0h**

Figure 14-4393. A53SS_CORE0_PMU_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-13256. A53SS_CORE0_PMU_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.278 A53SS_CORE0_PMU_PMLSR Register

1 A53SS_CORE0_PMU_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

Return to Summary Table

Table 14-13257. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FB4h**

Figure 14-4394. A53SS_CORE0_PMU_PMLSR Name Register

31	30	29	28	27	26	25	24
RES0_PMLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	1h	1h

Table 14-13259. A53SS_CORE0_PMU_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.279 A53SS_CORE0_PMU_PMAUTHSTATUS Register

1 A53SS_CORE0_PMU_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-13260. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FB8h**

Figure 14-4395. A53SS_CORE0_PMU_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-13262. A53SS_CORE0_PMU_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.280 A53SS_CORE0_PMU_PMDEVARCH Register

1 A53SS_CORE0_PMU_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

Return to Summary Table

Table 14-13263. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FBCh**

Figure 14-4396. A53SS_CORE0_PMU_PMDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
2A16h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
2A16h							

Table 14-13265. A53SS_CORE0_PMU_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.281 A53SS_CORE0_PMU_PMDEVTYPE Register

1 A53SS_CORE0_PMU_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

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Table 14-13266. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FCCh**

Figure 14-4397. A53SS_CORE0_PMU_PMDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_PMDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				6h			

Table 14-13268. A53SS_CORE0_PMU_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.282 A53SS_CORE0_PMU_PMPIDR4 Register

1 A53SS_CORE0_PMU_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-13269. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD0h**

Figure 14-4398. A53SS_CORE0_PMU_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-13271. A53SS_CORE0_PMU_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.283 A53SS_CORE0_PMU_PMPIDR5 Register

1 A53SS_CORE0_PMU_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

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Table 14-13272. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD4h**

Figure 14-4399. A53SS_CORE0_PMU_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-13274. A53SS_CORE0_PMU_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.284 A53SS_CORE0_PMU_PMPIDR6 Register

1 A53SS_CORE0_PMU_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

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Table 14-13275. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD8h**

Figure 14-4400. A53SS_CORE0_PMU_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-13277. A53SS_CORE0_PMU_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.285 A53SS_CORE0_PMU_PMPIDR7 Register

1 A53SS_CORE0_PMU_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

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Table 14-13278. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FDCh**

Figure 14-4401. A53SS_CORE0_PMU_PMPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR7_31_0							
R/W							
0h							

Table 14-13280. A53SS_CORE0_PMU_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.286 A53SS_CORE0_PMU_PMPIDR0 Register

1 A53SS_CORE0_PMU_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

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Table 14-13281. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE0h**

Figure 14-4402. A53SS_CORE0_PMU_PMPIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">D3h</td></tr>
</table>

Table 14-13283. A53SS_CORE0_PMU_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.287 A53SS_CORE0_PMU_PMPIDR1 Register

1 A53SS_CORE0_PMU_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-13284. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE4h**

Figure 14-4403. A53SS_CORE0_PMU_PMPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-13286. A53SS_CORE0_PMU_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.288 A53SS_CORE0_PMU_PMPIDR2 Register

1 A53SS_CORE0_PMU_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

Return to Summary Table

Table 14-13287. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE8h**

Figure 14-4404. A53SS_CORE0_PMU_PMPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-13289. A53SS_CORE0_PMU_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.289 A53SS_CORE0_PMU_PMPIDR3 Register

1 A53SS_CORE0_PMU_PMPIDR3 Register (Offset = FECh) [reset = 0h]

Performance Monitors Peripheral Identification Register 3

Return to Summary Table

Table 14-13290. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FECh**

Figure 14-4405. A53SS_CORE0_PMU_PMPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-13292. A53SS_CORE0_PMU_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.290 A53SS_CORE0_PMU_PMCIDR0 Register

1 A53SS_CORE0_PMU_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

Return to Summary Table

Table 14-13293. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF0h**

Figure 14-4406. A53SS_CORE0_PMU_PMCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-13295. A53SS_CORE0_PMU_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.291 A53SS_CORE0_PMU_PMCIDR1 Register

1 A53SS_CORE0_PMU_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

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Table 14-13296. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF4h**

Figure 14-4407. A53SS_CORE0_PMU_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-13298. A53SS_CORE0_PMU_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.292 A53SS_CORE0_PMU_PMCIDR2 Register

1 A53SS_CORE0_PMU_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-13299. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF8h**

Figure 14-4408. A53SS_CORE0_PMU_PMCIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-13301. A53SS_CORE0_PMU_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.293 A53SS_CORE0_PMU_PMCIDR3 Register

1 A53SS_CORE0_PMU_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

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Table 14-13302. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FFCh**

Figure 14-4409. A53SS_CORE0_PMU_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-13304. A53SS_CORE0_PMU_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.294 A53SS_CORE0_ETM_TRCPRGCTLR Register

1 A53SS_CORE0_ETM_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

Return to Summary Table

Table 14-13305. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0004h**

Figure 14-4410. A53SS_CORE0_ETM_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-13307. A53SS_CORE0_ETM_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.295 A53SS_CORE0_ETM_TRCSTATR Register

1 A53SS_CORE0_ETM_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

Return to Summary Table

Table 14-13308. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 000Ch**

Figure 14-4411. A53SS_CORE0_ETM_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-13310. A53SS_CORE0_ETM_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.296 A53SS_CORE0_ETM_TRCCONFIGR Register

1 A53SS_CORE0_ETM_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

Return to Summary Table

Table 14-13311. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0010h**

Figure 14-4412. A53SS_CORE0_ETM_TRCCONFIGR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCONFIGR_31_18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RES0_TRCCONFIGR_31_18</td><td>DV</td><td>DA</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RES0_TRCCONFIGR_15_15</td><td colspan="2">QE</td><td>RS</td><td>TS</td><td colspan="3">COND</td></tr>
<tr><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>VMID</td><td>CID</td><td>RES0_TRCCONFIGR_5_5</td><td>CCI</td><td>BB</td><td colspan="2">INSTP0</td><td>RES1_TRCCONFIGR_0_0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td></tr>
</table>

Table 14-13313. A53SS_CORE0_ETM_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-13313. A53SS_CORE0_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-13313. A53SS_CORE0_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.297 A53SS_CORE0_ETM_TRCAUXCTLR Register

1 A53SS_CORE0_ETM_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

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Table 14-13314. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0018h**

Figure 14-4413. A53SS_CORE0_ETM_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13316. A53SS_CORE0_ETM_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.298 A53SS_CORE0_ETM_TRCEVENTCTL0R Register

1 A53SS_CORE0_ETM_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

Return to Summary Table

Table 14-13317. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0020h**

Figure 14-4414. A53SS_CORE0_ETM_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-13319. A53SS_CORE0_ETM_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.299 A53SS_CORE0_ETM_TRCEVENTCTL1R Register

1 A53SS_CORE0_ETM_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

Return to Summary Table

Table 14-13320. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0024h**

Figure 14-4415. A53SS_CORE0_ETM_TRCEVENTCTL1R Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCEVENTCTL1R_31_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCEVENTCTL1R_31_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_TRCEVENTCTL1R_31_13</td><td>LPOVERRIDE</td><td>ATB</td><td colspan="3">RESERVED_TRCEVENTCTL1R_10_4</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_TRCEVENTCTL1R_10_4</td><td colspan="4">EN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13322. A53SS_CORE0_ETM_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.300 A53SS_CORE0_ETM_TRCSTALLCTLR Register

1 A53SS_CORE0_ETM_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

Return to Summary Table

Table 14-13323. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 002Ch**

Figure 14-4416. A53SS_CORE0_ETM_TRCSTALLCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCSTALLCTLR_31_9							ISTALL
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_TRCSTALLCTLR_7_4				LEVEL		RESERVED_TRCSTALLCTLR_1_0	
R/W				R/W		R/W	
0h				0h		0h	

Table 14-13325. A53SS_CORE0_ETM_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.301 A53SS_CORE0_ETM_TRCTSCTLR Register

1 A53SS_CORE0_ETM_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

Return to Summary Table

Table 14-13326. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0030h**

Figure 14-4417. A53SS_CORE0_ETM_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-13328. A53SS_CORE0_ETM_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.302 A53SS_CORE0_ETM_TRCSYNCPR Register

1 A53SS_CORE0_ETM_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

Return to Summary Table

Table 14-13329. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0034h**

Figure 14-4418. A53SS_CORE0_ETM_TRCSYNCPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_TRCSYNCPR_31_5</td><td colspan="5">PERIOD</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-13331. A53SS_CORE0_ETM_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.303 A53SS_CORE0_ETM_TRCCCCTLR Register

1 A53SS_CORE0_ETM_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

Return to Summary Table

Table 14-13332. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0038h**

Figure 14-4419. A53SS_CORE0_ETM_TRCCCCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCCCTLR_31_12							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCCCTLR_31_12							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCCCTLR_31_12				THRESHOLD			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-13334. A53SS_CORE0_ETM_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.304 A53SS_CORE0_ETM_TRCBBCTLR Register

1 A53SS_CORE0_ETM_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

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Table 14-13335. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 003Ch**

Figure 14-4420. A53SS_CORE0_ETM_TRCBBCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCBBCTLR_31_9							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCBBCTLR_31_9							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCBBCTLR_31_9							MODE
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RANGE							
R/W							
0h							

Table 14-13337. A53SS_CORE0_ETM_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.305 A53SS_CORE0_ETM_TRCTRACEIDR Register

1 A53SS_CORE0_ETM_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-13338. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0040h**

Figure 14-4421. A53SS_CORE0_ETM_TRCTRACEIDR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCTRACEIDR_31_7	TRACEID						
R/W	R/W						
0h	0h						

Table 14-13340. A53SS_CORE0_ETM_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.306 A53SS_CORE0_ETM_TRCVICTLR Register

1 A53SS_CORE0_ETM_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-13341. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0080h**

Figure 14-4422. A53SS_CORE0_ETM_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-13343. A53SS_CORE0_ETM_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-13343. A53SS_CORE0_ETM_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.307 A53SS_CORE0_ETM_TRCVIIECTLR Register

1 A53SS_CORE0_ETM_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

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Table 14-13344. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0084h**

Figure 14-4423. A53SS_CORE0_ETM_TRCVIIECTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVIIECTLR_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXCLUDE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCVIIECTLR_15_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INCLUDE							
R/W							
0h							

Table 14-13346. A53SS_CORE0_ETM_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.308 A53SS_CORE0_ETM_TRCVISSCTLR Register

1 A53SS_CORE0_ETM_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

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Table 14-13347. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0088h**

Figure 14-4424. A53SS_CORE0_ETM_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STOP							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START							
R/W							
0h							

Table 14-13349. A53SS_CORE0_ETM_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.309 A53SS_CORE0_ETM_TRCSEQEVR0 Register

1 A53SS_CORE0_ETM_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

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Table 14-13350. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0100h**

Figure 14-4425. A53SS_CORE0_ETM_TRCSEQEVR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCSEQEVR0_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCSEQEVR0_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">B_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">F_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13352. A53SS_CORE0_ETM_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.310 A53SS_CORE0_ETM_TRCSEQEVR1 Register

1 A53SS_CORE0_ETM_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

Return to Summary Table

Table 14-13353. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0104h**

Figure 14-4426. A53SS_CORE0_ETM_TRCSEQEVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-13355. A53SS_CORE0_ETM_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.311 A53SS_CORE0_ETM_TRCSEQEVR2 Register

1 A53SS_CORE0_ETM_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

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Table 14-13356. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0108h**

Figure 14-4427. A53SS_CORE0_ETM_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-13358. A53SS_CORE0_ETM_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.312 A53SS_CORE0_ETM_TRCSEQRSTEVR Register

1 A53SS_CORE0_ETM_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

Return to Summary Table

Table 14-13359. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0118h**

Figure 14-4428. A53SS_CORE0_ETM_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST							
R/W							
0h							

Table 14-13361. A53SS_CORE0_ETM_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.313 A53SS_CORE0_ETM_TRCSEQSTR Register

1 A53SS_CORE0_ETM_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

Return to Summary Table

Table 14-13362. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 011Ch**

Figure 14-4429. A53SS_CORE0_ETM_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-13364. A53SS_CORE0_ETM_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.314 A53SS_CORE0_ETM_TRCEXTINSELR Register

1 A53SS_CORE0_ETM_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

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Table 14-13365. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0120h**

Figure 14-4430. A53SS_CORE0_ETM_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-13367. A53SS_CORE0_ETM_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.315 A53SS_CORE0_ETM_TRCCNTRLDVR0 Register

1 A53SS_CORE0_ETM_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

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Table 14-13368. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0140h**

Figure 14-4431. A53SS_CORE0_ETM_TRCCNTRLDVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-13370. A53SS_CORE0_ETM_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.316 A53SS_CORE0_ETM_TRCCNTRLDVR1 Register

1 A53SS_CORE0_ETM_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

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Table 14-13371. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0144h**

Figure 14-4432. A53SS_CORE0_ETM_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-13373. A53SS_CORE0_ETM_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.317 A53SS_CORE0_ETM_TRCCNTCTLR0 Register

1 A53SS_CORE0_ETM_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

Return to Summary Table

Table 14-13374. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0150h**

Figure 14-4433. A53SS_CORE0_ETM_TRCCNTCTLR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR0_31_18							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTCTLR0_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RLDEVENT_N							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTEVENT_N							
R/W							
0h							

Table 14-13376. A53SS_CORE0_ETM_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.318 A53SS_CORE0_ETM_TRCCNTCTLR1 Register

1 A53SS_CORE0_ETM_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

Return to Summary Table

Table 14-13377. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0154h**

Figure 14-4434. A53SS_CORE0_ETM_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RLDEVENT_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTEVENT_N							
R/W							
0h							

Table 14-13379. A53SS_CORE0_ETM_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.319 A53SS_CORE0_ETM_TRCCNTVR0 Register

1 A53SS_CORE0_ETM_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

Return to Summary Table

Table 14-13380. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0160h**

Figure 14-4435. A53SS_CORE0_ETM_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-13382. A53SS_CORE0_ETM_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.320 A53SS_CORE0_ETM_TRCCNTVR1 Register

1 A53SS_CORE0_ETM_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

Return to Summary Table

Table 14-13383. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0164h**

Figure 14-4436. A53SS_CORE0_ETM_TRCCNTVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-13385. A53SS_CORE0_ETM_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.321 A53SS_CORE0_ETM_TRCIDR8 Register

1 A53SS_CORE0_ETM_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

Return to Summary Table

Table 14-13386. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0180h**

Figure 14-4437. A53SS_CORE0_ETM_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							
23	22	21	20	19	18	17	16
MAXSPEC							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXSPEC							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXSPEC							
R/W							
0h							

Table 14-13388. A53SS_CORE0_ETM_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.322 A53SS_CORE0_ETM_TRCIDR9 Register

1 A53SS_CORE0_ETM_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-13389. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0184h**

Figure 14-4438. A53SS_CORE0_ETM_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-13391. A53SS_CORE0_ETM_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.323 A53SS_CORE0_ETM_TRCIDR10 Register

1 A53SS_CORE0_ETM_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-13392. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0188h**

Figure 14-4439. A53SS_CORE0_ETM_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-13394. A53SS_CORE0_ETM_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.324 A53SS_CORE0_ETM_TRCIDR11 Register

1 A53SS_CORE0_ETM_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-13395. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 018Ch**

Figure 14-4440. A53SS_CORE0_ETM_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-13397. A53SS_CORE0_ETM_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.325 A53SS_CORE0_ETM_TRCIDR12 Register

1 A53SS_CORE0_ETM_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-13398. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0190h**

Figure 14-4441. A53SS_CORE0_ETM_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-13400. A53SS_CORE0_ETM_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.326 A53SS_CORE0_ETM_TRCIDR13 Register

1 A53SS_CORE0_ETM_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

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Table 14-13401. Instance Table

Instance Name	Physical Address
A53SS0	0007 3004 0194h

Figure 14-4442. A53SS_CORE0_ETM_TRCIDR13 Name Register

31	30	29	28	27	26	25	24
NUMCONDSPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDSPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDSPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDSPC							
R/W							
0h							

Table 14-13403. A53SS_CORE0_ETM_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.327 A53SS_CORE0_ETM_TRCIMSPEC0 Register

1 A53SS_CORE0_ETM_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

Return to Summary Table

Table 14-13404. Instance Table

Instance Name	Physical Address
A53SS0	0007 3004 01C0h

Figure 14-4443. A53SS_CORE0_ETM_TRCIMSPEC0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EN				SUPPORT			
R/W				R/W			
0h				0h			

Table 14-13406. A53SS_CORE0_ETM_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.328 A53SS_CORE0_ETM_TRCIDR0 Register

1 A53SS_CORE0_ETM_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-13407. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E0h**

Figure 14-4444. A53SS_CORE0_ETM_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	22	21	20	19	18	17	16
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	6	5	4	3	2	1	0
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-13409. A53SS_CORE0_ETM_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-13409. A53SS_CORE0_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-13409. A53SS_CORE0_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.329 A53SS_CORE0_ETM_TRCIDR1 Register

1 A53SS_CORE0_ETM_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

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Table 14-13410. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E4h**

Figure 14-4445. A53SS_CORE0_ETM_TRCIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DESIGNER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">41h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCIDR1_23_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RES1_TRCIDR1_15_12</td><td colspan="4">TRCARCHMAJ</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Fh</td><td colspan="4">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TRCARCHMIN</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-13412. A53SS_CORE0_ETM_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-13412. A53SS_CORE0_ETM_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.330 A53SS_CORE0_ETM_TRCIDR2 Register

1 A53SS_CORE0_ETM_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

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Table 14-13413. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E8h**

Figure 14-4446. A53SS_CORE0_ETM_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h
23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	
7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-13415. A53SS_CORE0_ETM_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-13415. A53SS_CORE0_ETM_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.331 A53SS_CORE0_ETM_TRCIDR3 Register

1 A53SS_CORE0_ETM_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

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Table 14-13416. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01ECh**

Figure 14-4447. A53SS_CORE0_ETM_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	14	13	12	11	10	9	8
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	6	5	4	3	2	1	0
CCITMIN							
R/W							
4h							

Table 14-13418. A53SS_CORE0_ETM_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-13418. A53SS_CORE0_ETM_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.332 A53SS_CORE0_ETM_TRCIDR4 Register

1 A53SS_CORE0_ETM_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

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Table 14-13419. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01F0h**

Figure 14-4448. A53SS_CORE0_ETM_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-13421. A53SS_CORE0_ETM_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-13421. A53SS_CORE0_ETM_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.333 A53SS_CORE0_ETM_TRCIDR5 Register

1 A53SS_CORE0_ETM_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-13422. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01F4h**

Figure 14-4449. A53SS_CORE0_ETM_TRCIDR5 Name Register

31	30	29	28	27	26	25	24
REDFUNCNTR	NUMCNTR			NUMSEQSTATE			RES0_TRCIDR5_24_24
R/W	R/W			R/W			R/W
0h	2h			4h			0h

23	22	21	20	19	18	17	16
LPOVERRIDE	ATBTRIG	TRACEIDSIZE					
R/W	R/W	R/W					
1h	1h	7h					

15	14	13	12	11	10	9	8
RES0_TRCIDR5_15_12				NUMEXTINSEL			NUMEXTIN
R/W				R/W			R/W
0h				4h			1Eh

7	6	5	4	3	2	1	0
NUMEXTIN							
R/W							
1Eh							

Table 14-13424. A53SS_CORE0_ETM_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-13424. A53SS_CORE0_ETM_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.334 A53SS_CORE0_ETM_TRCRSCTLR2 Register

1 A53SS_CORE0_ETM_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

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Table 14-13425. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0208h**

Figure 14-4450. A53SS_CORE0_ETM_TRCRSCTLR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR2_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR2_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13427. A53SS_CORE0_ETM_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13427. A53SS_CORE0_ETM_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.335 A53SS_CORE0_ETM_TRCRSCTLR3 Register

1 A53SS_CORE0_ETM_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

Resource Selection Control Registers 3

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Table 14-13428. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 020Ch**

Figure 14-4451. A53SS_CORE0_ETM_TRCRSCTLR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR3_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR3_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13430. A53SS_CORE0_ETM_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13430. A53SS_CORE0_ETM_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.336 A53SS_CORE0_ETM_TRCRSCTLR4 Register

1 A53SS_CORE0_ETM_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

Resource Selection Control Registers 4

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Table 14-13431. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0210h**

Figure 14-4452. A53SS_CORE0_ETM_TRCRSCTLR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR4_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR4_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13433. A53SS_CORE0_ETM_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13433. A53SS_CORE0_ETM_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.337 A53SS_CORE0_ETM_TRCRSCTLR5 Register

1 A53SS_CORE0_ETM_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

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Table 14-13434. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0214h**

Figure 14-4453. A53SS_CORE0_ETM_TRCRSCTLR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR5_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR5_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-13436. A53SS_CORE0_ETM_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13436. A53SS_CORE0_ETM_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.338 A53SS_CORE0_ETM_TRCRSCTLR6 Register

1 A53SS_CORE0_ETM_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

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Table 14-13437. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0218h**

Figure 14-4454. A53SS_CORE0_ETM_TRCRSCTLR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR6_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR6_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13439. A53SS_CORE0_ETM_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13439. A53SS_CORE0_ETM_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.339 A53SS_CORE0_ETM_TRCRSCTLR7 Register

1 A53SS_CORE0_ETM_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

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Table 14-13440. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 021Ch**

Figure 14-4455. A53SS_CORE0_ETM_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13442. A53SS_CORE0_ETM_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13442. A53SS_CORE0_ETM_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.340 A53SS_CORE0_ETM_TRCRSCTLR8 Register

1 A53SS_CORE0_ETM_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-13443. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0220h**

Figure 14-4456. A53SS_CORE0_ETM_TRCRSCTLR8 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR8_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR8_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13445. A53SS_CORE0_ETM_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13445. A53SS_CORE0_ETM_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.341 A53SS_CORE0_ETM_TRCRSCTLR9 Register

1 A53SS_CORE0_ETM_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-13446. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0224h**

Figure 14-4457. A53SS_CORE0_ETM_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13448. A53SS_CORE0_ETM_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13448. A53SS_CORE0_ETM_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.342 A53SS_CORE0_ETM_TRCRSCTLR10 Register

1 A53SS_CORE0_ETM_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-13449. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3004 0228h**

Figure 14-4458. A53SS_CORE0_ETM_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-13451. A53SS_CORE0_ETM_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13451. A53SS_CORE0_ETM_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.343 A53SS_CORE0_ETM_TRCRSCTLR11 Register

1 A53SS_CORE0_ETM_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-13452. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 022Ch**

Figure 14-4459. A53SS_CORE0_ETM_TRCRSCTLR11 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR11_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR11_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13454. A53SS_CORE0_ETM_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13454. A53SS_CORE0_ETM_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.344 A53SS_CORE0_ETM_TRCRSCTLR12 Register

1 A53SS_CORE0_ETM_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

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Table 14-13455. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0230h**

Figure 14-4460. A53SS_CORE0_ETM_TRCRSCTLR12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR12_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR12_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13457. A53SS_CORE0_ETM_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13457. A53SS_CORE0_ETM_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.345 A53SS_CORE0_ETM_TRCRSCTLR13 Register

1 A53SS_CORE0_ETM_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

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Table 14-13458. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0234h**

Figure 14-4461. A53SS_CORE0_ETM_TRCRSCTLR13 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR13_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR13_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13460. A53SS_CORE0_ETM_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13460. A53SS_CORE0_ETM_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.346 A53SS_CORE0_ETM_TRCRSCTLR14 Register

1 A53SS_CORE0_ETM_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

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Table 14-13461. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0238h**

Figure 14-4462. A53SS_CORE0_ETM_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-13463. A53SS_CORE0_ETM_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13463. A53SS_CORE0_ETM_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.347 A53SS_CORE0_ETM_TRCRSCTLR15 Register

1 A53SS_CORE0_ETM_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

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Table 14-13464. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 023Ch**

Figure 14-4463. A53SS_CORE0_ETM_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-13466. A53SS_CORE0_ETM_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-13466. A53SS_CORE0_ETM_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.348 A53SS_CORE0_ETM_TRCSSCCR0 Register

1 A53SS_CORE0_ETM_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-13467. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0280h**

Figure 14-4464. A53SS_CORE0_ETM_TRCSSCCR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSSCCR0_31_25							RST
R/W							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SAC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAC							
R/W							
0h							

Table 14-13469. A53SS_CORE0_ETM_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-13469. A53SS_CORE0_ETM_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.349 A53SS_CORE0_ETM_TRCSSCSR0 Register

1 A53SS_CORE0_ETM_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-13470. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 02A0h**

Figure 14-4465. A53SS_CORE0_ETM_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-13472. A53SS_CORE0_ETM_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-13472. A53SS_CORE0_ETM_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.350 A53SS_CORE0_ETM_TRCOSLAR Register

1 A53SS_CORE0_ETM_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-13473. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0300h**

Figure 14-4466. A53SS_CORE0_ETM_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-13475. A53SS_CORE0_ETM_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.351 A53SS_CORE0_ETM_TRCOSLSR Register

1 A53SS_CORE0_ETM_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-13476. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0304h**

Figure 14-4467. A53SS_CORE0_ETM_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-13478. A53SS_CORE0_ETM_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.352 A53SS_CORE0_ETM_TRCPDCR Register

1 A53SS_CORE0_ETM_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-13479. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0310h**

Figure 14-4468. A53SS_CORE0_ETM_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPDCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPDCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-13481. A53SS_CORE0_ETM_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.353 A53SS_CORE0_ETM_TRCPDSR Register

1 A53SS_CORE0_ETM_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

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Table 14-13482. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0314h**

Figure 14-4469. A53SS_CORE0_ETM_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDSR_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDSR_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-13484. A53SS_CORE0_ETM_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-13484. A53SS_CORE0_ETM_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.354 A53SS_CORE0_ETM_TRCACVR0_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

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Table 14-13485. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0400h**

Figure 14-4470. A53SS_CORE0_ETM_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDRESS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDRESS							
R/W							
0h							

Table 14-13487. A53SS_CORE0_ETM_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.355 A53SS_CORE0_ETM_TRCACVR0_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

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Table 14-13488. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0404h**

Figure 14-4471. A53SS_CORE0_ETM_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13490. A53SS_CORE0_ETM_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.356 A53SS_CORE0_ETM_TRCACVR1_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-13491. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0408h**

Figure 14-4472. A53SS_CORE0_ETM_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDRESS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDRESS							
R/W							
0h							

Table 14-13493. A53SS_CORE0_ETM_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.357 A53SS_CORE0_ETM_TRCACVR1_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-13494. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 040Ch**

Figure 14-4473. A53SS_CORE0_ETM_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13496. A53SS_CORE0_ETM_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.358 A53SS_CORE0_ETM_TRCACVR2_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-13497. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0410h**

Figure 14-4474. A53SS_CORE0_ETM_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13499. A53SS_CORE0_ETM_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.359 A53SS_CORE0_ETM_TRCACVR2_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-13500. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0414h**

Figure 14-4475. A53SS_CORE0_ETM_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13502. A53SS_CORE0_ETM_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.360 A53SS_CORE0_ETM_TRCACVR3_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-13503. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0418h**

Figure 14-4476. A53SS_CORE0_ETM_TRCACVR3_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13505. A53SS_CORE0_ETM_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.361 A53SS_CORE0_ETM_TRCACVR3_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

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Table 14-13506. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 041Ch**

Figure 14-4477. A53SS_CORE0_ETM_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13508. A53SS_CORE0_ETM_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.362 A53SS_CORE0_ETM_TRCACVR4_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

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Table 14-13509. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0420h**

Figure 14-4478. A53SS_CORE0_ETM_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13511. A53SS_CORE0_ETM_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.363 A53SS_CORE0_ETM_TRCACVR4_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

Return to Summary Table

Table 14-13512. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0424h**

Figure 14-4479. A53SS_CORE0_ETM_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13514. A53SS_CORE0_ETM_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.364 A53SS_CORE0_ETM_TRCACVR5_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

Return to Summary Table

Table 14-13515. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0428h**

Figure 14-4480. A53SS_CORE0_ETM_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13517. A53SS_CORE0_ETM_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.365 A53SS_CORE0_ETM_TRCACVR5_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

Return to Summary Table

Table 14-13518. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 042Ch**

Figure 14-4481. A53SS_CORE0_ETM_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13520. A53SS_CORE0_ETM_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.366 A53SS_CORE0_ETM_TRCACVR6_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

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Table 14-13521. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0430h**

Figure 14-4482. A53SS_CORE0_ETM_TRCACVR6_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13523. A53SS_CORE0_ETM_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.367 A53SS_CORE0_ETM_TRCACVR6_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

Return to Summary Table

Table 14-13524. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0434h**

Figure 14-4483. A53SS_CORE0_ETM_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13526. A53SS_CORE0_ETM_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.368 A53SS_CORE0_ETM_TRCACVR7_31_0 Register

1 A53SS_CORE0_ETM_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

Return to Summary Table

Table 14-13527. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0438h**

Figure 14-4484. A53SS_CORE0_ETM_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13529. A53SS_CORE0_ETM_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.369 A53SS_CORE0_ETM_TRCACVR7_63_32 Register

1 A53SS_CORE0_ETM_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

Return to Summary Table

Table 14-13530. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 043Ch**

Figure 14-4485. A53SS_CORE0_ETM_TRCACVR7_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-13532. A53SS_CORE0_ETM_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.370 A53SS_CORE0_ETM_TRCACATR0 Register

1 A53SS_CORE0_ETM_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-13533. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0480h**

Figure 14-4486. A53SS_CORE0_ETM_TRCACATR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR0_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR0_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR0_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13535. A53SS_CORE0_ETM_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13535. A53SS_CORE0_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13535. A53SS_CORE0_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13535. A53SS_CORE0_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.371 A53SS_CORE0_ETM_TRCACATR1 Register

1 A53SS_CORE0_ETM_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-13536. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0488h**

Figure 14-4487. A53SS_CORE0_ETM_TRCACATR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR1_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR1_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR1_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13538. A53SS_CORE0_ETM_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13538. A53SS_CORE0_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13538. A53SS_CORE0_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13538. A53SS_CORE0_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.372 A53SS_CORE0_ETM_TRCACATR2 Register

1 A53SS_CORE0_ETM_TRCACATR2 Register (Offset = 490h) [reset = 0h]

Address Comparator Access Type Registers 2

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Table 14-13539. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0490h**

Figure 14-4488. A53SS_CORE0_ETM_TRCACATR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR2_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR2_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR2_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13541. A53SS_CORE0_ETM_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13541. A53SS_CORE0_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13541. A53SS_CORE0_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13541. A53SS_CORE0_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.373 A53SS_CORE0_ETM_TRCACATR3 Register

1 A53SS_CORE0_ETM_TRCACATR3 Register (Offset = 498h) [reset = 0h]

Address Comparator Access Type Registers 3

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Table 14-13542. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0498h**

Figure 14-4489. A53SS_CORE0_ETM_TRCACATR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR3_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR3_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13544. A53SS_CORE0_ETM_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13544. A53SS_CORE0_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13544. A53SS_CORE0_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13544. A53SS_CORE0_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.374 A53SS_CORE0_ETM_TRCACATR4 Register

1 A53SS_CORE0_ETM_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-13545. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04A0h**

Figure 14-4490. A53SS_CORE0_ETM_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13547. A53SS_CORE0_ETM_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13547. A53SS_CORE0_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13547. A53SS_CORE0_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13547. A53SS_CORE0_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.375 A53SS_CORE0_ETM_TRCACATR5 Register

1 A53SS_CORE0_ETM_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-13548. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04A8h**

Figure 14-4491. A53SS_CORE0_ETM_TRCACATR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR5_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR5_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR5_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13550. A53SS_CORE0_ETM_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13550. A53SS_CORE0_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13550. A53SS_CORE0_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13550. A53SS_CORE0_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.376 A53SS_CORE0_ETM_TRCACATR6 Register

1 A53SS_CORE0_ETM_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

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Table 14-13551. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04B0h**

Figure 14-4492. A53SS_CORE0_ETM_TRCACATR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR6_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR6_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR6_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13553. A53SS_CORE0_ETM_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13553. A53SS_CORE0_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13553. A53SS_CORE0_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13553. A53SS_CORE0_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.377 A53SS_CORE0_ETM_TRCACATR7 Register

1 A53SS_CORE0_ETM_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

Address Comparator Access Type Registers 7

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Table 14-13554. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04B8h**

Figure 14-4493. A53SS_CORE0_ETM_TRCACATR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR7_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR7_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR7_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-13556. A53SS_CORE0_ETM_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-13556. A53SS_CORE0_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-13556. A53SS_CORE0_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-13556. A53SS_CORE0_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.378 A53SS_CORE0_ETM_TRCCIDCVR0 Register

1 A53SS_CORE0_ETM_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-13557. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0600h**

Figure 14-4494. A53SS_CORE0_ETM_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-13559. A53SS_CORE0_ETM_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.379 A53SS_CORE0_ETM_TRCVMIDCVR0 Register

1 A53SS_CORE0_ETM_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-13560. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0640h**

Figure 14-4495. A53SS_CORE0_ETM_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-13562. A53SS_CORE0_ETM_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.380 A53SS_CORE0_ETM_TRCCIDCCTLR0 Register

1 A53SS_CORE0_ETM_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

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Table 14-13563. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0680h**

Figure 14-4496. A53SS_CORE0_ETM_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-13565. A53SS_CORE0_ETM_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.381 A53SS_CORE0_ETM_TRCITATBIDR Register

1 A53SS_CORE0_ETM_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

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Table 14-13566. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EE4h**

Figure 14-4497. A53SS_CORE0_ETM_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-13568. A53SS_CORE0_ETM_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.382 A53SS_CORE0_ETM_TRCITIDATAR Register

1 A53SS_CORE0_ETM_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

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Table 14-13569. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EECh**

Figure 14-4498. A53SS_CORE0_ETM_TRCITIDATAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_TRCITIDATAR_31_5</td><td>ATDATAM_31</td><td>ATDATAM_23</td><td>ATDATAM_15</td><td>ATDATAM_7</td><td>ATDATAM_0</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13571. A53SS_CORE0_ETM_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.383 A53SS_CORE0_ETM_TRCITIATBINR Register

1 A53SS_CORE0_ETM_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

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Table 14-13572. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EF4h**

Figure 14-4499. A53SS_CORE0_ETM_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-13574. A53SS_CORE0_ETM_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.384 A53SS_CORE0_ETM_TRCITIATBOUTR Register

1 A53SS_CORE0_ETM_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-13575. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EFCh**

Figure 14-4500. A53SS_CORE0_ETM_TRCITIATBOUTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_31_10</td><td colspan="2">BYTES</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_7_2</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13577. A53SS_CORE0_ETM_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.385 A53SS_CORE0_ETM_TRCITCTRL Register

1 A53SS_CORE0_ETM_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

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Table 14-13578. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0F00h**

Figure 14-4501. A53SS_CORE0_ETM_TRCITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_TRCITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITCTRL_31_1							ITEN
R/W							R/W
0h							0h

Table 14-13580. A53SS_CORE0_ETM_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.386 A53SS_CORE0_ETM_TRCCLAIMSET Register

1 A53SS_CORE0_ETM_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-13581. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA0h**

Figure 14-4502. A53SS_CORE0_ETM_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-13583. A53SS_CORE0_ETM_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.387 A53SS_CORE0_ETM_TRCCLAIMCLR Register

1 A53SS_CORE0_ETM_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-13584. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA4h**

Figure 14-4503. A53SS_CORE0_ETM_TRCCLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCCLAIMCLR_31_4				CLR			
R/W				R/W			
0h				0h			

Table 14-13586. A53SS_CORE0_ETM_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.388 A53SS_CORE0_ETM_TRCDEVAFF0 Register

1 A53SS_CORE0_ETM_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

Device Affinity Register 0

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Table 14-13587. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA8h**

Figure 14-4504. A53SS_CORE0_ETM_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000000h							
23	22	21	20	19	18	17	16
MPIDR_EL1_31_0							
R/W							
80000000h							
15	14	13	12	11	10	9	8
MPIDR_EL1_31_0							
R/W							
80000000h							
7	6	5	4	3	2	1	0
MPIDR_EL1_31_0							
R/W							
80000000h							

Table 14-13589. A53SS_CORE0_ETM_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000000h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.389 A53SS_CORE0_ETM_TRCDEVAFF1 Register

1 A53SS_CORE0_ETM_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

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Table 14-13590. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FACh**

Figure 14-4505. A53SS_CORE0_ETM_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-13592. A53SS_CORE0_ETM_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.390 A53SS_CORE0_ETM_TRCLAR Register

1 A53SS_CORE0_ETM_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

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Table 14-13593. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FB0h**

Figure 14-4506. A53SS_CORE0_ETM_TRCLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-13595. A53SS_CORE0_ETM_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.391 A53SS_CORE0_ETM_TRCLSR Register

1 A53SS_CORE0_ETM_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

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Table 14-13596. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FB4h**

Figure 14-4507. A53SS_CORE0_ETM_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13598. A53SS_CORE0_ETM_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.392 A53SS_CORE0_ETM_TRCAUTHSTATUS Register

1 A53SS_CORE0_ETM_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

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Table 14-13599. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FB8h**

Figure 14-4508. A53SS_CORE0_ETM_TRCAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-13601. A53SS_CORE0_ETM_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-13601. A53SS_CORE0_ETM_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.393 A53SS_CORE0_ETM_TRCDEVARCH Register

1 A53SS_CORE0_ETM_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

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Table 14-13602. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FBCh**

Figure 14-4509. A53SS_CORE0_ETM_TRCDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	22	21	20	19	18	17	16
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	14	13	12	11	10	9	8
ARCHID							
R/W							
4A13h							
7	6	5	4	3	2	1	0
ARCHID							
R/W							
4A13h							

Table 14-13604. A53SS_CORE0_ETM_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.394 A53SS_CORE0_ETM_TRCDEVID Register

1 A53SS_CORE0_ETM_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-13605. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FC8h**

Figure 14-4510. A53SS_CORE0_ETM_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVID							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVID							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVID							
R/W							
0h							

Table 14-13607. A53SS_CORE0_ETM_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.395 A53SS_CORE0_ETM_TRCDEVTYPE Register

1 A53SS_CORE0_ETM_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

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Table 14-13608. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FCCh**

Figure 14-4511. A53SS_CORE0_ETM_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-13610. A53SS_CORE0_ETM_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.396 A53SS_CORE0_ETM_TRCPIDR4 Register

1 A53SS_CORE0_ETM_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

Peripheral Identification Register 4

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Table 14-13611. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD0h**

Figure 14-4512. A53SS_CORE0_ETM_TRCPIDR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-13613. A53SS_CORE0_ETM_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.397 A53SS_CORE0_ETM_TRCPIDR5 Register

1 A53SS_CORE0_ETM_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

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Table 14-13614. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD4h**

Figure 14-4513. A53SS_CORE0_ETM_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-13616. A53SS_CORE0_ETM_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.398 A53SS_CORE0_ETM_TRCPIDR6 Register

1 A53SS_CORE0_ETM_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register 6

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Table 14-13617. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD8h**

Figure 14-4514. A53SS_CORE0_ETM_TRCPIDR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR6_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR6_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR6_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR6_7_0							
R/W							
0h							

Table 14-13619. A53SS_CORE0_ETM_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.399 A53SS_CORE0_ETM_TRCPIDR7 Register

1 A53SS_CORE0_ETM_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

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Table 14-13620. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FDCh**

Figure 14-4515. A53SS_CORE0_ETM_TRCPIDR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_TRCPIDR7_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13622. A53SS_CORE0_ETM_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.400 A53SS_CORE0_ETM_TRCPIDR0 Register

1 A53SS_CORE0_ETM_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

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Table 14-13623. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE0h**

Figure 14-4516. A53SS_CORE0_ETM_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
5Dh							

Table 14-13625. A53SS_CORE0_ETM_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.401 A53SS_CORE0_ETM_TRCPIDR1 Register

1 A53SS_CORE0_ETM_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

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Table 14-13626. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE4h**

Figure 14-4517. A53SS_CORE0_ETM_TRCPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-13628. A53SS_CORE0_ETM_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.402 A53SS_CORE0_ETM_TRCPIDR2 Register

1 A53SS_CORE0_ETM_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-13629. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE8h**

Figure 14-4518. A53SS_CORE0_ETM_TRCPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-13631. A53SS_CORE0_ETM_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.403 A53SS_CORE0_ETM_TRCPIDR3 Register

1 A53SS_CORE0_ETM_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

Return to Summary Table

Table 14-13632. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FECh**

Figure 14-4519. A53SS_CORE0_ETM_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-13634. A53SS_CORE0_ETM_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.404 A53SS_CORE0_ETM_TRCCIDR0 Register

1 A53SS_CORE0_ETM_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

Return to Summary Table

Table 14-13635. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF0h**

Figure 14-4520. A53SS_CORE0_ETM_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-13637. A53SS_CORE0_ETM_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.405 A53SS_CORE0_ETM_TRCCIDR1 Register

1 A53SS_CORE0_ETM_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

Return to Summary Table

Table 14-13638. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF4h**

Figure 14-4521. A53SS_CORE0_ETM_TRCCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-13640. A53SS_CORE0_ETM_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.406 A53SS_CORE0_ETM_TRCCIDR2 Register

1 A53SS_CORE0_ETM_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-13641. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF8h**

Figure 14-4522. A53SS_CORE0_ETM_TRCCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-13643. A53SS_CORE0_ETM_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.407 A53SS_CORE0_ETM_TRCCIDR3 Register

1 A53SS_CORE0_ETM_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

Return to Summary Table

Table 14-13644. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FFCh**

Figure 14-4523. A53SS_CORE0_ETM_TRCCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-13646. A53SS_CORE0_ETM_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.408 A53SS_CORE1_DBG_EDESR Register

1 A53SS_CORE1_DBG_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

Return to Summary Table

Table 14-13647. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0020h**

Figure 14-4524. A53SS_CORE1_DBG_EDESR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDESR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDESR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDESR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RES0_EDESR_31_3</td><td>SS</td><td>RC</td><td>OSUC</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13649. A53SS_CORE1_DBG_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.409 A53SS_CORE1_DBG_EDECR Register

1 A53SS_CORE1_DBG_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

Return to Summary Table

Table 14-13650. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0024h**

Figure 14-4525. A53SS_CORE1_DBG_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDECR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDECR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13652. A53SS_CORE1_DBG_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.410 A53SS_CORE1_DBG_EDWAR_31_0 Register

1 A53SS_CORE1_DBG_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

Return to Summary Table

Table 14-13653. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0030h**

Figure 14-4526. A53SS_CORE1_DBG_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-13655. A53SS_CORE1_DBG_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.411 A53SS_CORE1_DBG_EDWAR_63_32 Register

1 A53SS_CORE1_DBG_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

Return to Summary Table

Table 14-13656. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0034h**

Figure 14-4527. A53SS_CORE1_DBG_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-13658. A53SS_CORE1_DBG_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.412 A53SS_CORE1_DBG_DBGDTRRX_EL0 Register

1 A53SS_CORE1_DBG_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

Return to Summary Table

Table 14-13659. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0080h**

Figure 14-4528. A53SS_CORE1_DBG_DBGDTRRX_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGDTRRX_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGDTRRX_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGDTRRX_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGDTRRX_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13661. A53SS_CORE1_DBG_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.413 A53SS_CORE1_DBG_EDITR Register

1 A53SS_CORE1_DBG_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-13662. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0084h**

Figure 14-4529. A53SS_CORE1_DBG_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-13664. A53SS_CORE1_DBG_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.414 A53SS_CORE1_DBG_EDSCR Register

1 A53SS_CORE1_DBG_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

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Table 14-13665. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0088h**

Figure 14-4530. A53SS_CORE1_DBG_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-13667. A53SS_CORE1_DBG_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-13667. A53SS_CORE1_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-13667. A53SS_CORE1_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-13667. A53SS_CORE1_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.415 A53SS_CORE1_DBG_DBGDTRTX_EL0 Register

1 A53SS_CORE1_DBG_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-13668. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 008Ch**

Figure 14-4531. A53SS_CORE1_DBG_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-13670. A53SS_CORE1_DBG_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.416 A53SS_CORE1_DBG_EDRCR Register

1 A53SS_CORE1_DBG_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-13671. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0090h**

Figure 14-4532. A53SS_CORE1_DBG_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDRCR_31_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDRCR_31_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-13673. A53SS_CORE1_DBG_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-13673. A53SS_CORE1_DBG_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.417 A53SS_CORE1_DBG_EDACR Register

1 A53SS_CORE1_DBG_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-13674. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0094h**

Figure 14-4533. A53SS_CORE1_DBG_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-13676. A53SS_CORE1_DBG_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.418 A53SS_CORE1_DBG_EDECCR Register

1 A53SS_CORE1_DBG_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-13677. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0098h**

Figure 14-4534. A53SS_CORE1_DBG_EDECCR Name Register

31	30	29	28	27	26	25	24
RES0_EDECCR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDECCR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDECCR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NSE				SE			
R/W				R/W			
0h				0h			

Table 14-13679. A53SS_CORE1_DBG_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-13679. A53SS_CORE1_DBG_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.419 A53SS_CORE1_DBG_EDPCSR_31_0 Register

1 A53SS_CORE1_DBG_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-13680. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A0h**

Figure 14-4535. A53SS_CORE1_DBG_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_31_0							
R/W							
0h							

Table 14-13682. A53SS_CORE1_DBG_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31:0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.420 A53SS_CORE1_DBG_EDCIDSR Register

1 A53SS_CORE1_DBG_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-13683. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A4h**

Figure 14-4536. A53SS_CORE1_DBG_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXTIDR							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXTIDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXTIDR							
R/W							
0h							

Table 14-13685. A53SS_CORE1_DBG_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.421 A53SS_CORE1_DBG_EDVIDSR Register

1 A53SS_CORE1_DBG_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-13686. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A8h**

Figure 14-4537. A53SS_CORE1_DBG_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-13688. A53SS_CORE1_DBG_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63:32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63:32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.422 A53SS_CORE1_DBG_EDPCSR_63_32 Register

1 A53SS_CORE1_DBG_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-13689. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00ACh**

Figure 14-4538. A53SS_CORE1_DBG_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_63_32							
R/W							
0h							

Table 14-13691. A53SS_CORE1_DBG_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63:32] of the sampled PC.

14.3.1.1.2.423 A53SS_CORE1_DBG_OSLAR_EL1 Register

1 A53SS_CORE1_DBG_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-13692. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0300h**

Figure 14-4539. A53SS_CORE1_DBG_OSLAR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_OSLAR_EL1_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_OSLAR_EL1_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_OSLAR_EL1_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_OSLAR_EL1_31_1							OSLK
R/W							R/W
0h							0h

Table 14-13694. A53SS_CORE1_DBG_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.424 A53SS_CORE1_DBG_EDPRCR Register

1 A53SS_CORE1_DBG_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-13695. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0310h**

Figure 14-4540. A53SS_CORE1_DBG_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPRCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPRCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-13697. A53SS_CORE1_DBG_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-13697. A53SS_CORE1_DBG_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.425 A53SS_CORE1_DBG_EDPRSR Register

1 A53SS_CORE1_DBG_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-13698. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0314h**

Figure 14-4541. A53SS_CORE1_DBG_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRSR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-13700. A53SS_CORE1_DBG_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-13700. A53SS_CORE1_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-13700. A53SS_CORE1_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.426 A53SS_CORE1_DBG_DBGBVR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13701. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0400h**

Figure 14-4542. A53SS_CORE1_DBG_DBGBVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_31_0							
R/W							
0h							

Table 14-13703. A53SS_CORE1_DBG_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.427 A53SS_CORE1_DBG_DBGBVR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13704. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0404h**

Figure 14-4543. A53SS_CORE1_DBG_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-13706. A53SS_CORE1_DBG_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.428 A53SS_CORE1_DBG_DBGBCR0_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-13707. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0408h**

Figure 14-4544. A53SS_CORE1_DBG_DBGBCR0_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR0_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR0_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR0_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-13709. A53SS_CORE1_DBG_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13709. A53SS_CORE1_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13709. A53SS_CORE1_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.429 A53SS_CORE1_DBG_DBGBVR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13710. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0410h**

Figure 14-4545. A53SS_CORE1_DBG_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-13712. A53SS_CORE1_DBG_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.430 A53SS_CORE1_DBG_DBGBVR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13713. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0414h**

Figure 14-4546. A53SS_CORE1_DBG_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-13715. A53SS_CORE1_DBG_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.431 A53SS_CORE1_DBG_DBGBCR1_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-13716. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0418h**

Figure 14-4547. A53SS_CORE1_DBG_DBGBCR1_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR1_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR1_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR1_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-13718. A53SS_CORE1_DBG_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13718. A53SS_CORE1_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13718. A53SS_CORE1_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.432 A53SS_CORE1_DBG_DBGBVR2_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13719. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0420h**

Figure 14-4548. A53SS_CORE1_DBG_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-13721. A53SS_CORE1_DBG_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.433 A53SS_CORE1_DBG_DBGBVR2_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13722. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0424h**

Figure 14-4549. A53SS_CORE1_DBG_DBGBVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_63_32							
R/W							
0h							

Table 14-13724. A53SS_CORE1_DBG_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.434 A53SS_CORE1_DBG_DBGBCR2_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-13725. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0428h**

Figure 14-4550. A53SS_CORE1_DBG_DBGBCR2_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR2_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR2_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR2_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-13727. A53SS_CORE1_DBG_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13727. A53SS_CORE1_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13727. A53SS_CORE1_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.435 A53SS_CORE1_DBG_DBGBVR3_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13728. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0430h**

Figure 14-4551. A53SS_CORE1_DBG_DBGBVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_31_0							
R/W							
0h							

Table 14-13730. A53SS_CORE1_DBG_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.436 A53SS_CORE1_DBG_DBGBVR3_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13731. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0434h**

Figure 14-4552. A53SS_CORE1_DBG_DBGBVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_63_32							
R/W							
0h							

Table 14-13733. A53SS_CORE1_DBG_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.437 A53SS_CORE1_DBG_DBGBCR3_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-13734. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0438h**

Figure 14-4553. A53SS_CORE1_DBG_DBGBCR3_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR3_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR3_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR3_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-13736. A53SS_CORE1_DBG_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13736. A53SS_CORE1_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13736. A53SS_CORE1_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.438 A53SS_CORE1_DBG_DBGBVR4_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13737. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0440h**

Figure 14-4554. A53SS_CORE1_DBG_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-13739. A53SS_CORE1_DBG_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.439 A53SS_CORE1_DBG_DBGBVR4_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13740. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0444h**

Figure 14-4555. A53SS_CORE1_DBG_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-13742. A53SS_CORE1_DBG_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.440 A53SS_CORE1_DBG_DBGBCR4_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

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Table 14-13743. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0448h**

Figure 14-4556. A53SS_CORE1_DBG_DBGBCR4_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR4_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR4_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR4_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-13745. A53SS_CORE1_DBG_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13745. A53SS_CORE1_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13745. A53SS_CORE1_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.441 A53SS_CORE1_DBG_DBGBVR5_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13746. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0450h**

Figure 14-4557. A53SS_CORE1_DBG_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR5_EL1_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR5_EL1_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-13748. A53SS_CORE1_DBG_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.442 A53SS_CORE1_DBG_DBGBVR5_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-13749. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0454h**

Figure 14-4558. A53SS_CORE1_DBG_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-13751. A53SS_CORE1_DBG_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.443 A53SS_CORE1_DBG_DBGBCR5_EL1 Register

1 A53SS_CORE1_DBG_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

Debug Breakpoint Control Register 5

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Table 14-13752. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0458h**

Figure 14-4559. A53SS_CORE1_DBG_DBGBCR5_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR5_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR5_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR5_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-13754. A53SS_CORE1_DBG_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-13754. A53SS_CORE1_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-13754. A53SS_CORE1_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.444 A53SS_CORE1_DBG_DBGWVR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

Return to Summary Table

Table 14-13755. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0800h**

Figure 14-4560. A53SS_CORE1_DBG_DBGWVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR0_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-13757. A53SS_CORE1_DBG_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.445 A53SS_CORE1_DBG_DBGWVR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

Return to Summary Table

Table 14-13758. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0804h**

Figure 14-4561. A53SS_CORE1_DBG_DBGWVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESS							VA
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA							
R/W							
0h							

Table 14-13760. A53SS_CORE1_DBG_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.446 A53SS_CORE1_DBG_DBGWCR0_EL1 Register

1 A53SS_CORE1_DBG_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

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Table 14-13761. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0808h**

Figure 14-4562. A53SS_CORE1_DBG_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-13763. A53SS_CORE1_DBG_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-13763. A53SS_CORE1_DBG_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.447 A53SS_CORE1_DBG_DBGWVR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

Return to Summary Table

Table 14-13764. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0810h**

Figure 14-4563. A53SS_CORE1_DBG_DBGWVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA						RES0_DBGWVR1_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-13766. A53SS_CORE1_DBG_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.448 A53SS_CORE1_DBG_DBGWVR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

Return to Summary Table

Table 14-13767. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0814h**

Figure 14-4564. A53SS_CORE1_DBG_DBGWVR1_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13769. A53SS_CORE1_DBG_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.449 A53SS_CORE1_DBG_DBGWCR1_EL1 Register

1 A53SS_CORE1_DBG_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

Return to Summary Table

Table 14-13770. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0818h**

Figure 14-4565. A53SS_CORE1_DBG_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-13772. A53SS_CORE1_DBG_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-13772. A53SS_CORE1_DBG_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.450 A53SS_CORE1_DBG_DBGWVR2_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

Return to Summary Table

Table 14-13773. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0820h**

Figure 14-4566. A53SS_CORE1_DBG_DBGWVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR2_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-13775. A53SS_CORE1_DBG_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.451 A53SS_CORE1_DBG_DBGWVR2_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

Return to Summary Table

Table 14-13776. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0824h**

Figure 14-4567. A53SS_CORE1_DBG_DBGWVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-13778. A53SS_CORE1_DBG_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.452 A53SS_CORE1_DBG_DBGWCR2_EL1 Register

1 A53SS_CORE1_DBG_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

Return to Summary Table

Table 14-13779. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0828h**

Figure 14-4568. A53SS_CORE1_DBG_DBGWCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR2_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR2_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-13781. A53SS_CORE1_DBG_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-13781. A53SS_CORE1_DBG_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.453 A53SS_CORE1_DBG_DBGWVR3_EL1_31_0 Register

1 A53SS_CORE1_DBG_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

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Table 14-13782. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0830h**

Figure 14-4569. A53SS_CORE1_DBG_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-13784. A53SS_CORE1_DBG_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.454 A53SS_CORE1_DBG_DBGWVR3_EL1_63_32 Register

1 A53SS_CORE1_DBG_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

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Table 14-13785. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0834h**

Figure 14-4570. A53SS_CORE1_DBG_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-13787. A53SS_CORE1_DBG_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.455 A53SS_CORE1_DBG_DBGWCR3_EL1 Register

1 A53SS_CORE1_DBG_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

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Table 14-13788. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0838h**

Figure 14-4571. A53SS_CORE1_DBG_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-13790. A53SS_CORE1_DBG_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-13790. A53SS_CORE1_DBG_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.456 A53SS_CORE1_DBG_MIDR_EL1 Register

1 A53SS_CORE1_DBG_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-13791. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D00h**

Figure 14-4572. A53SS_CORE1_DBG_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-13793. A53SS_CORE1_DBG_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.457 A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

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Table 14-13794. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D20h**

Figure 14-4573. A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
EL3				EL2			
R/W				R/W			
2h				2h			
7	6	5	4	3	2	1	0
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-13796. A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-13796. A53SS_CORE1_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.458 A53SS_CORE1_DBG_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

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Table 14-13797. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D24h**

Figure 14-4574. A53SS_CORE1_DBG_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-13799. A53SS_CORE1_DBG_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.459 A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

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Table 14-13800. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D28h**

Figure 14-4575. A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-13802. A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-13802. A53SS_CORE1_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.460 A53SS_CORE1_DBG_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

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Table 14-13803. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D2Ch**

Figure 14-4576. A53SS_CORE1_DBG_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-13805. A53SS_CORE1_DBG_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.461 A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-13806. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D30h**

Figure 14-4577. A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-13808. A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-13808. A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.462 A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-13809. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D34h**

Figure 14-4578. A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-13811. A53SS_CORE1_DBG_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.463 A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

Return to Summary Table

Table 14-13812. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D38h**

Figure 14-4579. A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-13814. A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-13814. A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.464 A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

Return to Summary Table

Table 14-13815. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D3Ch**

Figure 14-4580. A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-13817. A53SS_CORE1_DBG_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.465 A53SS_CORE1_DBG_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

Return to Summary Table

Table 14-13818. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D40h**

Figure 14-4581. A53SS_CORE1_DBG_ID_AA64PFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-13820. A53SS_CORE1_DBG_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.466 A53SS_CORE1_DBG_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

Return to Summary Table

Table 14-13821. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D44h**

Figure 14-4582. A53SS_CORE1_DBG_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-13823. A53SS_CORE1_DBG_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.467 A53SS_CORE1_DBG_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

Return to Summary Table

Table 14-13824. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D48h**

Figure 14-4583. A53SS_CORE1_DBG_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-13826. A53SS_CORE1_DBG_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.468 A53SS_CORE1_DBG_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

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Table 14-13827. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D4Ch**

Figure 14-4584. A53SS_CORE1_DBG_ID_AA64DFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-13829. A53SS_CORE1_DBG_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.469 A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

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Table 14-13830. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D50h**

Figure 14-4585. A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-13832. A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.470 A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

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Table 14-13833. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D54h**

Figure 14-4586. A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-13835. A53SS_CORE1_DBG_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.471 A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-13836. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D58h**

Figure 14-4587. A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_ID_AA64MMFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_ID_AA64MMFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_ID_AA64MMFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_ID_AA64MMFR1_EL1_31_0_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13838. A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.472 A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

Return to Summary Table

Table 14-13839. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D5Ch**

Figure 14-4588. A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-13841. A53SS_CORE1_DBG_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.473 A53SS_CORE1_DBG_EDITCTRL Register

1 A53SS_CORE1_DBG_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

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Table 14-13842. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0F00h**

Figure 14-4589. A53SS_CORE1_DBG_EDITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_EDITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-13844. A53SS_CORE1_DBG_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.474 A53SS_CORE1_DBG_DBGCLAIMSET_EL1 Register

1 A53SS_CORE1_DBG_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-13845. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA0h**

Figure 14-4590. A53SS_CORE1_DBG_DBGCLAIMSET_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIM							
R/W							
FFh							

Table 14-13847. A53SS_CORE1_DBG_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.475 A53SS_CORE1_DBG_DBGCLAIMCLR_EL1 Register

1 A53SS_CORE1_DBG_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-13848. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA4h**

Figure 14-4591. A53SS_CORE1_DBG_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
0h							

Table 14-13850. A53SS_CORE1_DBG_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.476 A53SS_CORE1_DBG_EDDEVAFF0 Register

1 A53SS_CORE1_DBG_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

External Debug Device Affinity Register 0

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Table 14-13851. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA8h**

Figure 14-4592. A53SS_CORE1_DBG_EDDEVAFF0 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
EDDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
EDDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
EDDEVAFF0							
R/W							
80000001h							

Table 14-13853. A53SS_CORE1_DBG_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.477 A53SS_CORE1_DBG_EDDEVAFF1 Register

1 A53SS_CORE1_DBG_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

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Table 14-13854. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FACh**

Figure 14-4593. A53SS_CORE1_DBG_EDDEVAFF1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13856. A53SS_CORE1_DBG_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.478 A53SS_CORE1_DBG_EDLAR Register

1 A53SS_CORE1_DBG_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

Return to Summary Table

Table 14-13857. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB0h**

Figure 14-4594. A53SS_CORE1_DBG_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-13859. A53SS_CORE1_DBG_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.479 A53SS_CORE1_DBG_EDLSR Register

1 A53SS_CORE1_DBG_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

Return to Summary Table

Table 14-13860. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB4h**

Figure 14-4595. A53SS_CORE1_DBG_EDLSR Name Register

31	30	29	28	27	26	25	24
RES0_EDLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13862. A53SS_CORE1_DBG_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.480 A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1 Register

1 A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

Return to Summary Table

Table 14-13863. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB8h**

Figure 14-4596. A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		2h		2h		2h	

Table 14-13865. A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-13865. A53SS_CORE1_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.481 A53SS_CORE1_DBG_EDDEVARCH Register

1 A53SS_CORE1_DBG_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

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Table 14-13866. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FBCh**

Figure 14-4597. A53SS_CORE1_DBG_EDDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
6A15h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
6A15h							

Table 14-13868. A53SS_CORE1_DBG_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.482 A53SS_CORE1_DBG_EDDEVID2 Register

1 A53SS_CORE1_DBG_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

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Table 14-13869. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC0h**

Figure 14-4598. A53SS_CORE1_DBG_EDDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID2_31_0							
R/W							
0h							

Table 14-13871. A53SS_CORE1_DBG_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.483 A53SS_CORE1_DBG_EDDEVID1 Register

1 A53SS_CORE1_DBG_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

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Table 14-13872. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC4h**

Figure 14-4599. A53SS_CORE1_DBG_EDDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID1_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDDEVID1_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDDEVID1_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDDEVID1_31_4				PCSROFFSET			
R/W				R/W			
0h				2h			

Table 14-13874. A53SS_CORE1_DBG_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.484 A53SS_CORE1_DBG_EDDEVID Register

1 A53SS_CORE1_DBG_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

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Table 14-13875. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC8h**

Figure 14-4600. A53SS_CORE1_DBG_EDDEVID Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID_31_28				AUXREGS			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDDEVID_23_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDDEVID_23_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDDEVID_23_4				PCSAMPLE			
R/W				R/W			
0h				3h			

Table 14-13877. A53SS_CORE1_DBG_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.485 A53SS_CORE1_DBG_EDDEVTYPE Register

1 A53SS_CORE1_DBG_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

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Table 14-13878. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FCCh**

Figure 14-4601. A53SS_CORE1_DBG_EDDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				5h			

Table 14-13880. A53SS_CORE1_DBG_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.486 A53SS_CORE1_DBG_EDPIDR4 Register

1 A53SS_CORE1_DBG_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

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Table 14-13881. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FD0h**

Figure 14-4602. A53SS_CORE1_DBG_EDPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-13883. A53SS_CORE1_DBG_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.487 A53SS_CORE1_DBG_EDPIDR0 Register

1 A53SS_CORE1_DBG_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

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Table 14-13884. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE0h**

Figure 14-4603. A53SS_CORE1_DBG_EDPIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-13886. A53SS_CORE1_DBG_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.488 A53SS_CORE1_DBG_EDPIDR1 Register

1 A53SS_CORE1_DBG_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

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Table 14-13887. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE4h**

Figure 14-4604. A53SS_CORE1_DBG_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-13889. A53SS_CORE1_DBG_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.489 A53SS_CORE1_DBG_EDPIDR2 Register

1 A53SS_CORE1_DBG_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

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Table 14-13890. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE8h**

Figure 14-4605. A53SS_CORE1_DBG_EDPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-13892. A53SS_CORE1_DBG_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.490 A53SS_CORE1_DBG_EDPIDR3 Register

1 A53SS_CORE1_DBG_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

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Table 14-13893. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FECh**

Figure 14-4606. A53SS_CORE1_DBG_EDPIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13895. A53SS_CORE1_DBG_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.491 A53SS_CORE1_DBG_EDCIDR0 Register

1 A53SS_CORE1_DBG_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

Return to Summary Table

Table 14-13896. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF0h**

Figure 14-4607. A53SS_CORE1_DBG_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-13898. A53SS_CORE1_DBG_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.492 A53SS_CORE1_DBG_EDCIDR1 Register

1 A53SS_CORE1_DBG_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

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Table 14-13899. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF4h**

Figure 14-4608. A53SS_CORE1_DBG_EDCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-13901. A53SS_CORE1_DBG_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.493 A53SS_CORE1_DBG_EDCIDR2 Register

1 A53SS_CORE1_DBG_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

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Table 14-13902. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF8h**

Figure 14-4609. A53SS_CORE1_DBG_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-13904. A53SS_CORE1_DBG_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.494 A53SS_CORE1_DBG_EDCIDR3 Register

1 A53SS_CORE1_DBG_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

Return to Summary Table

Table 14-13905. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FFCh**

Figure 14-4610. A53SS_CORE1_DBG_EDCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-13907. A53SS_CORE1_DBG_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.495 A53SS_CORE1_PMU_PMEVCNTR0_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

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Table 14-13908. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0000h**

Figure 14-4611. A53SS_CORE1_PMU_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-13910. A53SS_CORE1_PMU_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.496 A53SS_CORE1_PMU_PMEVCNTR1_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

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Table 14-13911. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0008h**

Figure 14-4612. A53SS_CORE1_PMU_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-13913. A53SS_CORE1_PMU_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.497 A53SS_CORE1_PMU_PMEVCNTR2_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

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Table 14-13914. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0010h**

Figure 14-4613. A53SS_CORE1_PMU_PMEVCNTR2_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR2_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR2_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR2_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR2_EL0							
R/W							
0h							

Table 14-13916. A53SS_CORE1_PMU_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.498 A53SS_CORE1_PMU_PMEVCNTR3_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

Return to Summary Table

Table 14-13917. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0018h**

Figure 14-4614. A53SS_CORE1_PMU_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-13919. A53SS_CORE1_PMU_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.499 A53SS_CORE1_PMU_PMEVCNTR4_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

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Table 14-13920. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0020h**

Figure 14-4615. A53SS_CORE1_PMU_PMEVCNTR4_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR4_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR4_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR4_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR4_EL0							
R/W							
0h							

Table 14-13922. A53SS_CORE1_PMU_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.500 A53SS_CORE1_PMU_PMEVCNTR5_EL0 Register

1 A53SS_CORE1_PMU_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

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Table 14-13923. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0028h**

Figure 14-4616. A53SS_CORE1_PMU_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR5_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR5_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-13925. A53SS_CORE1_PMU_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.501 A53SS_CORE1_PMU_PMCCNTR_EL0_31_0 Register

1 A53SS_CORE1_PMU_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

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Table 14-13926. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 00F8h**

Figure 14-4617. A53SS_CORE1_PMU_PMCCNTR_EL0_31_0 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-13928. A53SS_CORE1_PMU_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.502 A53SS_CORE1_PMU_PMCCNTR_EL0_63_32 Register

1 A53SS_CORE1_PMU_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

Return to Summary Table

Table 14-13929. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 00FCh**

Figure 14-4618. A53SS_CORE1_PMU_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-13931. A53SS_CORE1_PMU_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.503 A53SS_CORE1_PMU_PMEVTYPER0_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

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Table 14-13932. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0400h**

Figure 14-4619. A53SS_CORE1_PMU_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-13934. A53SS_CORE1_PMU_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13934. A53SS_CORE1_PMU_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.504 A53SS_CORE1_PMU_PMEVTYPER1_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

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Table 14-13935. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0404h**

Figure 14-4620. A53SS_CORE1_PMU_PMEVTYPER1_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER1_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER1_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER1_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-13937. A53SS_CORE1_PMU_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13937. A53SS_CORE1_PMU_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.505 A53SS_CORE1_PMU_PMEVTYPER2_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

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Table 14-13938. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0408h**

Figure 14-4621. A53SS_CORE1_PMU_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-13940. A53SS_CORE1_PMU_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13940. A53SS_CORE1_PMU_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.506 A53SS_CORE1_PMU_PMEVTYPER3_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-13941. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 040Ch**

Figure 14-4622. A53SS_CORE1_PMU_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13943. A53SS_CORE1_PMU_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13943. A53SS_CORE1_PMU_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.507 A53SS_CORE1_PMU_PMEVTYPER4_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

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Table 14-13944. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0410h**

Figure 14-4623. A53SS_CORE1_PMU_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-13946. A53SS_CORE1_PMU_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13946. A53SS_CORE1_PMU_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.508 A53SS_CORE1_PMU_PMEVTYPER5_EL0 Register

1 A53SS_CORE1_PMU_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

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Table 14-13947. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0414h**

Figure 14-4624. A53SS_CORE1_PMU_PMEVTYPER5_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>P</td><td>U</td><td>NSK</td><td>NSU</td><td>NSH</td><td>M</td><td colspan="2">RES0_PMEVTYPER5_EL0_25_10</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMEVTYPER5_EL0_25_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RES0_PMEVTYPER5_EL0_25_10</td><td colspan="2">EVTCOUNT</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVTCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13949. A53SS_CORE1_PMU_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-13949. A53SS_CORE1_PMU_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.509 A53SS_CORE1_PMU_PMCCFILTR_EL0 Register

1 A53SS_CORE1_PMU_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

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Table 14-13950. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 047Ch**

Figure 14-4625. A53SS_CORE1_PMU_PMCCFILTR_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMCCFILTR_EL0_25_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							

Table 14-13952. A53SS_CORE1_PMU_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-13952. A53SS_CORE1_PMU_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.510 A53SS_CORE1_PMU_PMCNTENSET_EL0 Register

1 A53SS_CORE1_PMU_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

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Table 14-13953. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C00h**

Figure 14-4626. A53SS_CORE1_PMU_PMCNTENSET_EL0 Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>C</td><td colspan="7">P_X</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13955. A53SS_CORE1_PMU_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.511 A53SS_CORE1_PMU_PMCNTENCLR_EL0 Register

1 A53SS_CORE1_PMU_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

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Table 14-13956. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C20h**

Figure 14-4627. A53SS_CORE1_PMU_PMCNTENCLR_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>C</td><td colspan="7">P_X</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13958. A53SS_CORE1_PMU_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.512 A53SS_CORE1_PMU_PMINTENSET_EL1 Register

1 A53SS_CORE1_PMU_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

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Table 14-13959. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C40h**

Figure 14-4628. A53SS_CORE1_PMU_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13961. A53SS_CORE1_PMU_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.513 A53SS_CORE1_PMU_PMINTENCLR_EL1 Register

1 A53SS_CORE1_PMU_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

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Table 14-13962. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C60h**

Figure 14-4629. A53SS_CORE1_PMU_PMINTENCLR_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-13964. A53SS_CORE1_PMU_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.514 A53SS_CORE1_PMU_PMOVSCLR_EL0 Register

1 A53SS_CORE1_PMU_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

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Table 14-13965. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C80h**

Figure 14-4630. A53SS_CORE1_PMU_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-13967. A53SS_CORE1_PMU_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.515 A53SS_CORE1_PMU_PMSWINC_EL0 Register

1 A53SS_CORE1_PMU_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

Return to Summary Table

Table 14-13968. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0CA0h**

Figure 14-4631. A53SS_CORE1_PMU_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-13970. A53SS_CORE1_PMU_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.516 A53SS_CORE1_PMU_PMOVSSET_EL0 Register

1 A53SS_CORE1_PMU_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

Return to Summary Table

Table 14-13971. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0CC0h**

Figure 14-4632. A53SS_CORE1_PMU_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-13973. A53SS_CORE1_PMU_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.517 A53SS_CORE1_PMU_PMCFGR Register

1 A53SS_CORE1_PMU_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-13974. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E00h**

Figure 14-4633. A53SS_CORE1_PMU_PMCFGR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCFGR_31_20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RES0_PMCFGR_31_20</td><td>UEN</td><td>WT</td><td>NA</td><td>EX</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CCD</td><td>CC</td><td colspan="6">SIZE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td colspan="6">3Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6h</td></tr>
</table>

Table 14-13976. A53SS_CORE1_PMU_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-13976. A53SS_CORE1_PMU_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.518 A53SS_CORE1_PMU_PMCR_EL0 Register

1 A53SS_CORE1_PMU_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-13977. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E04h**

Figure 14-4634. A53SS_CORE1_PMU_PMCR_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCR_EL0_31_11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMCR_EL0_31_11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RES0_PMCR_EL0_31_11</td><td colspan="3">RES0_PMCR_EL0_10_7</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_PMCR_EL0_10_7</td><td>LC</td><td>DP</td><td>X</td><td>D</td><td>C</td><td>P</td><td>E</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13979. A53SS_CORE1_PMU_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-13979. A53SS_CORE1_PMU_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.519 A53SS_CORE1_PMU_PMCEID0_EL0 Register

1 A53SS_CORE1_PMU_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-13980. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E20h**

Figure 14-4635. A53SS_CORE1_PMU_PMCEID0_EL0 Name Register

31	30	29	28	27	26	25	24
CE_31_0							
R/W							
67FFBFFFh							
23	22	21	20	19	18	17	16
CE_31_0							
R/W							
67FFBFFFh							
15	14	13	12	11	10	9	8
CE_31_0							
R/W							
67FFBFFFh							
7	6	5	4	3	2	1	0
CE_31_0							
R/W							
67FFBFFFh							

Table 14-13982. A53SS_CORE1_PMU_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.520 A53SS_CORE1_PMU_PMCEID1_EL0 Register

1 A53SS_CORE1_PMU_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-13983. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E24h**

Figure 14-4636. A53SS_CORE1_PMU_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-13985. A53SS_CORE1_PMU_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.521 A53SS_CORE1_PMU_PMITCTRL Register

1 A53SS_CORE1_PMU_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-13986. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0F00h**

Figure 14-4637. A53SS_CORE1_PMU_PMITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_PMITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-13988. A53SS_CORE1_PMU_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.522 A53SS_CORE1_PMU_PMDEVAFF0 Register

1 A53SS_CORE1_PMU_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

Performance Monitors Device Affinity Register 0

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Table 14-13989. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FA8h**

Figure 14-4638. A53SS_CORE1_PMU_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000001h							

Table 14-13991. A53SS_CORE1_PMU_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.523 A53SS_CORE1_PMU_PMDEVAFF1 Register

1 A53SS_CORE1_PMU_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-13992. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FACh**

Figure 14-4639. A53SS_CORE1_PMU_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
PMDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
PMDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
PMDEVAFF1							
R/W							
0h							

Table 14-13994. A53SS_CORE1_PMU_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.524 A53SS_CORE1_PMU_PMLAR Register

1 A53SS_CORE1_PMU_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

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Table 14-13995. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB0h**

Figure 14-4640. A53SS_CORE1_PMU_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-13997. A53SS_CORE1_PMU_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.525 A53SS_CORE1_PMU_PMLSR Register

1 A53SS_CORE1_PMU_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

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Table 14-13998. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB4h**

Figure 14-4641. A53SS_CORE1_PMU_PMLSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RES0_PMLSR_31_3</td><td>NTT</td><td>SLK</td><td>SLI</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14000. A53SS_CORE1_PMU_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.526 A53SS_CORE1_PMU_PMAUTHSTATUS Register

1 A53SS_CORE1_PMU_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-14001. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB8h**

Figure 14-4642. A53SS_CORE1_PMU_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-14003. A53SS_CORE1_PMU_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.527 A53SS_CORE1_PMU_PMDEVARCH Register

1 A53SS_CORE1_PMU_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

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Table 14-14004. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FBCh**

Figure 14-4643. A53SS_CORE1_PMU_PMDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
2A16h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
2A16h							

Table 14-14006. A53SS_CORE1_PMU_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.528 A53SS_CORE1_PMU_PMDEVTYPE Register

1 A53SS_CORE1_PMU_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

Return to Summary Table

Table 14-14007. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FCCh**

Figure 14-4644. A53SS_CORE1_PMU_PMDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_PMDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				6h			

Table 14-14009. A53SS_CORE1_PMU_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.529 A53SS_CORE1_PMU_PMPIDR4 Register

1 A53SS_CORE1_PMU_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-14010. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD0h**

Figure 14-4645. A53SS_CORE1_PMU_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-14012. A53SS_CORE1_PMU_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.530 A53SS_CORE1_PMU_PMPIDR5 Register

1 A53SS_CORE1_PMU_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

Return to Summary Table

Table 14-14013. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD4h**

Figure 14-4646. A53SS_CORE1_PMU_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-14015. A53SS_CORE1_PMU_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.531 A53SS_CORE1_PMU_PMPIDR6 Register

1 A53SS_CORE1_PMU_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

Return to Summary Table

Table 14-14016. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD8h**

Figure 14-4647. A53SS_CORE1_PMU_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-14018. A53SS_CORE1_PMU_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.532 A53SS_CORE1_PMU_PMPIDR7 Register

1 A53SS_CORE1_PMU_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

Return to Summary Table

Table 14-14019. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FDCh**

Figure 14-4648. A53SS_CORE1_PMU_PMPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR7_31_0							
R/W							
0h							

Table 14-14021. A53SS_CORE1_PMU_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.533 A53SS_CORE1_PMU_PMPIDR0 Register

1 A53SS_CORE1_PMU_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

Return to Summary Table

Table 14-14022. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE0h**

Figure 14-4649. A53SS_CORE1_PMU_PMPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
D3h							

Table 14-14024. A53SS_CORE1_PMU_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.534 A53SS_CORE1_PMU_PMPIDR1 Register

1 A53SS_CORE1_PMU_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-14025. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE4h**

Figure 14-4650. A53SS_CORE1_PMU_PMPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-14027. A53SS_CORE1_PMU_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.535 A53SS_CORE1_PMU_PMPIDR2 Register

1 A53SS_CORE1_PMU_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

Return to Summary Table

Table 14-14028. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE8h**

Figure 14-4651. A53SS_CORE1_PMU_PMPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-14030. A53SS_CORE1_PMU_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.536 A53SS_CORE1_PMU_PMPIDR3 Register

1 A53SS_CORE1_PMU_PMPIDR3 Register (Offset = FECh) [reset = 0h]

Performance Monitors Peripheral Identification Register 3

Return to Summary Table

Table 14-14031. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FECh**

Figure 14-4652. A53SS_CORE1_PMU_PMPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-14033. A53SS_CORE1_PMU_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.537 A53SS_CORE1_PMU_PMCIDR0 Register

1 A53SS_CORE1_PMU_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

Return to Summary Table

Table 14-14034. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FF0h**

Figure 14-4653. A53SS_CORE1_PMU_PMCIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMCIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMCIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-14036. A53SS_CORE1_PMU_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.538 A53SS_CORE1_PMU_PMCIDR1 Register

1 A53SS_CORE1_PMU_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

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Table 14-14037. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FF4h**

Figure 14-4654. A53SS_CORE1_PMU_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-14039. A53SS_CORE1_PMU_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.539 A53SS_CORE1_PMU_PMCIDR2 Register

1 A53SS_CORE1_PMU_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-14040. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3012 0FF8h**

Figure 14-4655. A53SS_CORE1_PMU_PMCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-14042. A53SS_CORE1_PMU_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.540 A53SS_CORE1_PMU_PMCIDR3 Register

1 A53SS_CORE1_PMU_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

Return to Summary Table

Table 14-14043. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FFCh**

Figure 14-4656. A53SS_CORE1_PMU_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-14045. A53SS_CORE1_PMU_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.541 A53SS_CORE1_ETM_TRCPRGCTLR Register

1 A53SS_CORE1_ETM_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

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Table 14-14046. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0004h**

Figure 14-4657. A53SS_CORE1_ETM_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-14048. A53SS_CORE1_ETM_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.542 A53SS_CORE1_ETM_TRCSTATR Register

1 A53SS_CORE1_ETM_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

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Table 14-14049. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 000Ch**

Figure 14-4658. A53SS_CORE1_ETM_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-14051. A53SS_CORE1_ETM_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.543 A53SS_CORE1_ETM_TRCCONFIGR Register

1 A53SS_CORE1_ETM_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

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Table 14-14052. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0010h**

Figure 14-4659. A53SS_CORE1_ETM_TRCCONFIGR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCONFIGR_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCONFIGR_31_18						DV	DA
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCONFIGR_15_15	QE		RS	TS	COND		
R/W	R/W		R/W	R/W	R/W		
0h	0h		0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VMID	CID	RES0_TRCCONFIGR_5_5	CCI	BB	INSTP0		RES1_TRCCONFIGR_0_0
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		1h

Table 14-14054. A53SS_CORE1_ETM_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-14054. A53SS_CORE1_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-14054. A53SS_CORE1_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.544 A53SS_CORE1_ETM_TRCAUXCTLR Register

1 A53SS_CORE1_ETM_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

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Table 14-14055. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0018h**

Figure 14-4660. A53SS_CORE1_ETM_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14057. A53SS_CORE1_ETM_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.545 A53SS_CORE1_ETM_TRCEVENTCTL0R Register

1 A53SS_CORE1_ETM_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

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Table 14-14058. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0020h**

Figure 14-4661. A53SS_CORE1_ETM_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	14	13	12	11	10	9	8
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-14060. A53SS_CORE1_ETM_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.546 A53SS_CORE1_ETM_TRCEVENTCTL1R Register

1 A53SS_CORE1_ETM_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

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Table 14-14061. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0024h**

Figure 14-4662. A53SS_CORE1_ETM_TRCEVENTCTL1R Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEVENTCTL1R_31_13			LPOVERRIDE	ATB	RESERVED_TRCEVENTCTL1R_10_4		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEVENTCTL1R_10_4				EN			
R/W				R/W			
0h				0h			

Table 14-14063. A53SS_CORE1_ETM_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.547 A53SS_CORE1_ETM_TRCSTALLCTLR Register

1 A53SS_CORE1_ETM_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

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Table 14-14064. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 002Ch**

Figure 14-4663. A53SS_CORE1_ETM_TRCSTALLCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCSTALLCTLR_31_9							ISTALL
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_TRCSTALLCTLR_7_4				LEVEL		RESERVED_TRCSTALLCTLR_1_0	
R/W				R/W		R/W	
0h				0h		0h	

Table 14-14066. A53SS_CORE1_ETM_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.548 A53SS_CORE1_ETM_TRCTSCTLR Register

1 A53SS_CORE1_ETM_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

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Table 14-14067. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0030h**

Figure 14-4664. A53SS_CORE1_ETM_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-14069. A53SS_CORE1_ETM_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.549 A53SS_CORE1_ETM_TRCSYNCPR Register

1 A53SS_CORE1_ETM_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

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Table 14-14070. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0034h**

Figure 14-4665. A53SS_CORE1_ETM_TRCSYNCPR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSYNCPR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSYNCPR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSYNCPR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSYNCPR_31_5			PERIOD				
R/W			R/W				
0h			0h				

Table 14-14072. A53SS_CORE1_ETM_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.550 A53SS_CORE1_ETM_TRCCCCTLR Register

1 A53SS_CORE1_ETM_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

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Table 14-14073. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0038h**

Figure 14-4666. A53SS_CORE1_ETM_TRCCCCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCCCTLR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCCCTLR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCCCTLR_31_12				THRESHOLD			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THRESHOLD							
R/W							
0h							

Table 14-14075. A53SS_CORE1_ETM_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.551 A53SS_CORE1_ETM_TRCBBCTLR Register

1 A53SS_CORE1_ETM_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

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Table 14-14076. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 003Ch**

Figure 14-4667. A53SS_CORE1_ETM_TRCBBCTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCBBCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCBBCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RES0_TRCBBCTLR_31_9</td><td>MODE</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RANGE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14078. A53SS_CORE1_ETM_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.552 A53SS_CORE1_ETM_TRCTRACEIDR Register

1 A53SS_CORE1_ETM_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-14079. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0040h**

Figure 14-4668. A53SS_CORE1_ETM_TRCTRACEIDR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCTRACEIDR_31_7	TRACEID						
R/W	R/W						
0h	0h						

Table 14-14081. A53SS_CORE1_ETM_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.553 A53SS_CORE1_ETM_TRCVICTLR Register

1 A53SS_CORE1_ETM_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-14082. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0080h**

Figure 14-4669. A53SS_CORE1_ETM_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-14084. A53SS_CORE1_ETM_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-14084. A53SS_CORE1_ETM_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.554 A53SS_CORE1_ETM_TRCVIIECTLR Register

1 A53SS_CORE1_ETM_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

Return to Summary Table

Table 14-14085. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0084h**

Figure 14-4670. A53SS_CORE1_ETM_TRCVIIECTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVIIECTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXCLUDE							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCVIIECTLR_15_8							
R/W							
0h							
7	6	5	4	3	2	1	0
INCLUDE							
R/W							
0h							

Table 14-14087. A53SS_CORE1_ETM_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.555 A53SS_CORE1_ETM_TRCVISSCTLR Register

1 A53SS_CORE1_ETM_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

Return to Summary Table

Table 14-14088. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0088h**

Figure 14-4671. A53SS_CORE1_ETM_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	22	21	20	19	18	17	16
STOP							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 14-14090. A53SS_CORE1_ETM_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.556 A53SS_CORE1_ETM_TRCSEQEVR0 Register

1 A53SS_CORE1_ETM_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

Return to Summary Table

Table 14-14091. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0100h**

Figure 14-4672. A53SS_CORE1_ETM_TRCSEQEVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-14093. A53SS_CORE1_ETM_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.557 A53SS_CORE1_ETM_TRCSEQEVR1 Register

1 A53SS_CORE1_ETM_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

Return to Summary Table

Table 14-14094. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0104h**

Figure 14-4673. A53SS_CORE1_ETM_TRCSEQEVR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCSEQEVR1_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCSEQEVR1_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">B_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">F_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14096. A53SS_CORE1_ETM_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.558 A53SS_CORE1_ETM_TRCSEQEVR2 Register

1 A53SS_CORE1_ETM_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

Return to Summary Table

Table 14-14097. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0108h**

Figure 14-4674. A53SS_CORE1_ETM_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-14099. A53SS_CORE1_ETM_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.559 A53SS_CORE1_ETM_TRCSEQRSTEVR Register

1 A53SS_CORE1_ETM_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

Return to Summary Table

Table 14-14100. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0118h**

Figure 14-4675. A53SS_CORE1_ETM_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RST							
R/W							
0h							

Table 14-14102. A53SS_CORE1_ETM_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.560 A53SS_CORE1_ETM_TRCSEQSTR Register

1 A53SS_CORE1_ETM_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

Return to Summary Table

Table 14-14103. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 011Ch**

Figure 14-4676. A53SS_CORE1_ETM_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-14105. A53SS_CORE1_ETM_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.561 A53SS_CORE1_ETM_TRCEXTINSELR Register

1 A53SS_CORE1_ETM_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

Return to Summary Table

Table 14-14106. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0120h**

Figure 14-4677. A53SS_CORE1_ETM_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-14108. A53SS_CORE1_ETM_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.562 A53SS_CORE1_ETM_TRCCNTRLDVR0 Register

1 A53SS_CORE1_ETM_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

Return to Summary Table

Table 14-14109. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0140h**

Figure 14-4678. A53SS_CORE1_ETM_TRCCNTRLDVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE_N							
R/W							
0h							

Table 14-14111. A53SS_CORE1_ETM_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.563 A53SS_CORE1_ETM_TRCCNTRLDVR1 Register

1 A53SS_CORE1_ETM_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

Return to Summary Table

Table 14-14112. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0144h**

Figure 14-4679. A53SS_CORE1_ETM_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-14114. A53SS_CORE1_ETM_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.564 A53SS_CORE1_ETM_TRCCNTCTLR0 Register

1 A53SS_CORE1_ETM_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

Return to Summary Table

Table 14-14115. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0150h**

Figure 14-4680. A53SS_CORE1_ETM_TRCCNTCTLR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR0_31_18							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCCNTCTLR0_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
RLDEVENT_N							
R/W							
0h							

7	6	5	4	3	2	1	0
CNTEVENT_N							
R/W							
0h							

Table 14-14117. A53SS_CORE1_ETM_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.565 A53SS_CORE1_ETM_TRCCNTCTLR1 Register

1 A53SS_CORE1_ETM_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

Return to Summary Table

Table 14-14118. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0154h**

Figure 14-4681. A53SS_CORE1_ETM_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RLDEVENT_N							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTEVENT_N							
R/W							
0h							

Table 14-14120. A53SS_CORE1_ETM_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.566 A53SS_CORE1_ETM_TRCCNTVR0 Register

1 A53SS_CORE1_ETM_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

Return to Summary Table

Table 14-14121. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0160h**

Figure 14-4682. A53SS_CORE1_ETM_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-14123. A53SS_CORE1_ETM_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.567 A53SS_CORE1_ETM_TRCCNTVR1 Register

1 A53SS_CORE1_ETM_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

Return to Summary Table

Table 14-14124. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0164h**

Figure 14-4683. A53SS_CORE1_ETM_TRCCNTVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-14126. A53SS_CORE1_ETM_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.568 A53SS_CORE1_ETM_TRCIDR8 Register

1 A53SS_CORE1_ETM_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

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Table 14-14127. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0180h**

Figure 14-4684. A53SS_CORE1_ETM_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							

23	22	21	20	19	18	17	16
MAXSPEC							
R/W							
0h							

15	14	13	12	11	10	9	8
MAXSPEC							
R/W							
0h							

7	6	5	4	3	2	1	0
MAXSPEC							
R/W							
0h							

Table 14-14129. A53SS_CORE1_ETM_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.569 A53SS_CORE1_ETM_TRCIDR9 Register

1 A53SS_CORE1_ETM_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-14130. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0184h**

Figure 14-4685. A53SS_CORE1_ETM_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-14132. A53SS_CORE1_ETM_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.570 A53SS_CORE1_ETM_TRCIDR10 Register

1 A53SS_CORE1_ETM_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-14133. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0188h**

Figure 14-4686. A53SS_CORE1_ETM_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-14135. A53SS_CORE1_ETM_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.571 A53SS_CORE1_ETM_TRCIDR11 Register

1 A53SS_CORE1_ETM_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-14136. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 018Ch**

Figure 14-4687. A53SS_CORE1_ETM_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-14138. A53SS_CORE1_ETM_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.572 A53SS_CORE1_ETM_TRCIDR12 Register

1 A53SS_CORE1_ETM_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-14139. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0190h**

Figure 14-4688. A53SS_CORE1_ETM_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-14141. A53SS_CORE1_ETM_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.573 A53SS_CORE1_ETM_TRCIDR13 Register

1 A53SS_CORE1_ETM_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

Return to Summary Table

Table 14-14142. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0194h**

Figure 14-4689. A53SS_CORE1_ETM_TRCIDR13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NUMCONDSPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NUMCONDSPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMCONDSPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUMCONDSPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14144. A53SS_CORE1_ETM_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.574 A53SS_CORE1_ETM_TRCIMSPEC0 Register

1 A53SS_CORE1_ETM_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

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Table 14-14145. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01C0h**

Figure 14-4690. A53SS_CORE1_ETM_TRCIMSPEC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCIMSPEC0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCIMSPEC0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCIMSPEC0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">EN</td><td colspan="4">SUPPORT</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14147. A53SS_CORE1_ETM_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.575 A53SS_CORE1_ETM_TRCIDR0 Register

1 A53SS_CORE1_ETM_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-14148. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E0h**

Figure 14-4691. A53SS_CORE1_ETM_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	22	21	20	19	18	17	16
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	6	5	4	3	2	1	0
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-14150. A53SS_CORE1_ETM_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-14150. A53SS_CORE1_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-14150. A53SS_CORE1_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.576 A53SS_CORE1_ETM_TRCIDR1 Register

1 A53SS_CORE1_ETM_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

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Table 14-14151. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E4h**

Figure 14-4692. A53SS_CORE1_ETM_TRCIDR1 Name Register

31	30	29	28	27	26	25	24
DESIGNER							
R/W							
41h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIDR1_23_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES1_TRCIDR1_15_12				TRCARCHMAJ			
R/W				R/W			
Fh				4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRCARCHMIN				REVISION			
R/W				R/W			
0h				4h			

Table 14-14153. A53SS_CORE1_ETM_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-14153. A53SS_CORE1_ETM_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.577 A53SS_CORE1_ETM_TRCIDR2 Register

1 A53SS_CORE1_ETM_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

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Table 14-14154. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E8h**

Figure 14-4693. A53SS_CORE1_ETM_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h

23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			

15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	

7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-14156. A53SS_CORE1_ETM_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-14156. A53SS_CORE1_ETM_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.578 A53SS_CORE1_ETM_TRCIDR3 Register

1 A53SS_CORE1_ETM_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

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Table 14-14157. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01ECh**

Figure 14-4694. A53SS_CORE1_ETM_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	14	13	12	11	10	9	8
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	6	5	4	3	2	1	0
CCITMIN							
R/W							
4h							

Table 14-14159. A53SS_CORE1_ETM_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-14159. A53SS_CORE1_ETM_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.579 A53SS_CORE1_ETM_TRCIDR4 Register

1 A53SS_CORE1_ETM_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

Return to Summary Table

Table 14-14160. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01F0h**

Figure 14-4695. A53SS_CORE1_ETM_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			
23	22	21	20	19	18	17	16
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			
15	14	13	12	11	10	9	8
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-14162. A53SS_CORE1_ETM_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-14162. A53SS_CORE1_ETM_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.580 A53SS_CORE1_ETM_TRCIDR5 Register

1 A53SS_CORE1_ETM_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-14163. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3013 01F4h**

Figure 14-4696. A53SS_CORE1_ETM_TRCIDR5 Name Register

31	30	29	28	27	26	25	24
REDFUNCNTR	NUMCNTR			NUMSEQSTATE			RES0_TRCIDR5_24_24
R/W	R/W			R/W			R/W
0h	2h			4h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPOVERRIDE	ATBTRIG	TRACEIDSIZE					
R/W	R/W	R/W					
1h	1h	7h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCIDR5_15_12				NUMEXTINSEL			NUMEXTIN
R/W				R/W			R/W
0h				4h			1Eh
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMEXTIN							
R/W							
1Eh							

Table 14-14165. A53SS_CORE1_ETM_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-14165. A53SS_CORE1_ETM_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.581 A53SS_CORE1_ETM_TRCRSCTLR2 Register

1 A53SS_CORE1_ETM_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

Resource Selection Control Registers 2

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Table 14-14166. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0208h**

Figure 14-4697. A53SS_CORE1_ETM_TRCRSCTLR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR2_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR2_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14168. A53SS_CORE1_ETM_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14168. A53SS_CORE1_ETM_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.582 A53SS_CORE1_ETM_TRCRSCTLR3 Register

1 A53SS_CORE1_ETM_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

Resource Selection Control Registers 3

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Table 14-14169. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 020Ch**

Figure 14-4698. A53SS_CORE1_ETM_TRCRSCTLR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR3_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR3_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14171. A53SS_CORE1_ETM_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14171. A53SS_CORE1_ETM_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.583 A53SS_CORE1_ETM_TRCRSCTLR4 Register

1 A53SS_CORE1_ETM_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

Resource Selection Control Registers 4

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Table 14-14172. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0210h**

Figure 14-4699. A53SS_CORE1_ETM_TRCRSCTLR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR4_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR4_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14174. A53SS_CORE1_ETM_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14174. A53SS_CORE1_ETM_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.584 A53SS_CORE1_ETM_TRCRSCTLR5 Register

1 A53SS_CORE1_ETM_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

Resource Selection Control Registers 5

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Table 14-14175. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0214h**

Figure 14-4700. A53SS_CORE1_ETM_TRCRSCTLR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR5_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR5_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14177. A53SS_CORE1_ETM_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14177. A53SS_CORE1_ETM_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.585 A53SS_CORE1_ETM_TRCRSCTLR6 Register

1 A53SS_CORE1_ETM_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

Resource Selection Control Registers 6

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Table 14-14178. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0218h**

Figure 14-4701. A53SS_CORE1_ETM_TRCRSCTLR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR6_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR6_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14180. A53SS_CORE1_ETM_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14180. A53SS_CORE1_ETM_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.586 A53SS_CORE1_ETM_TRCRSCTLR7 Register

1 A53SS_CORE1_ETM_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

Resource Selection Control Registers 7

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Table 14-14181. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 021Ch**

Figure 14-4702. A53SS_CORE1_ETM_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14183. A53SS_CORE1_ETM_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14183. A53SS_CORE1_ETM_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.587 A53SS_CORE1_ETM_TRCRSCTLR8 Register

1 A53SS_CORE1_ETM_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-14184. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0220h**

Figure 14-4703. A53SS_CORE1_ETM_TRCRSCTLR8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR8_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR8_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14186. A53SS_CORE1_ETM_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14186. A53SS_CORE1_ETM_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.588 A53SS_CORE1_ETM_TRCRSCTLR9 Register

1 A53SS_CORE1_ETM_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-14187. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0224h**

Figure 14-4704. A53SS_CORE1_ETM_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14189. A53SS_CORE1_ETM_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14189. A53SS_CORE1_ETM_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.589 A53SS_CORE1_ETM_TRCRSCTLR10 Register

1 A53SS_CORE1_ETM_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-14190. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0228h**

Figure 14-4705. A53SS_CORE1_ETM_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14192. A53SS_CORE1_ETM_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14192. A53SS_CORE1_ETM_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.590 A53SS_CORE1_ETM_TRCRSCTLR11 Register

1 A53SS_CORE1_ETM_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-14193. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 022Ch**

Figure 14-4706. A53SS_CORE1_ETM_TRCRSCTLR11 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR11_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR11_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14195. A53SS_CORE1_ETM_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14195. A53SS_CORE1_ETM_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.591 A53SS_CORE1_ETM_TRCRSCTLR12 Register

1 A53SS_CORE1_ETM_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

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Table 14-14196. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0230h**

Figure 14-4707. A53SS_CORE1_ETM_TRCRSCTLR12 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR12_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR12_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-14198. A53SS_CORE1_ETM_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14198. A53SS_CORE1_ETM_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.592 A53SS_CORE1_ETM_TRCRSCTLR13 Register

1 A53SS_CORE1_ETM_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

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Table 14-14199. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0234h**

Figure 14-4708. A53SS_CORE1_ETM_TRCRSCTLR13 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR13_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR13_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14201. A53SS_CORE1_ETM_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14201. A53SS_CORE1_ETM_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.593 A53SS_CORE1_ETM_TRCRSCTLR14 Register

1 A53SS_CORE1_ETM_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

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Table 14-14202. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0238h**

Figure 14-4709. A53SS_CORE1_ETM_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-14204. A53SS_CORE1_ETM_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14204. A53SS_CORE1_ETM_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.594 A53SS_CORE1_ETM_TRCRSCTLR15 Register

1 A53SS_CORE1_ETM_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

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Table 14-14205. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 023Ch**

Figure 14-4710. A53SS_CORE1_ETM_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-14207. A53SS_CORE1_ETM_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-14207. A53SS_CORE1_ETM_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.595 A53SS_CORE1_ETM_TRCSSCCR0 Register

1 A53SS_CORE1_ETM_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-14208. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0280h**

Figure 14-4711. A53SS_CORE1_ETM_TRCSSCCR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSSCCR0_31_25							RST
R/W							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SAC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAC							
R/W							
0h							

Table 14-14210. A53SS_CORE1_ETM_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-14210. A53SS_CORE1_ETM_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.596 A53SS_CORE1_ETM_TRCSSCSR0 Register

1 A53SS_CORE1_ETM_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-14211. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 02A0h**

Figure 14-4712. A53SS_CORE1_ETM_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-14213. A53SS_CORE1_ETM_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-14213. A53SS_CORE1_ETM_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.597 A53SS_CORE1_ETM_TRCOSLAR Register

1 A53SS_CORE1_ETM_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-14214. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0300h**

Figure 14-4713. A53SS_CORE1_ETM_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-14216. A53SS_CORE1_ETM_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.598 A53SS_CORE1_ETM_TRCOSLSR Register

1 A53SS_CORE1_ETM_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-14217. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0304h**

Figure 14-4714. A53SS_CORE1_ETM_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-14219. A53SS_CORE1_ETM_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.599 A53SS_CORE1_ETM_TRCPDCR Register

1 A53SS_CORE1_ETM_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-14220. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0310h**

Figure 14-4715. A53SS_CORE1_ETM_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-14222. A53SS_CORE1_ETM_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.600 A53SS_CORE1_ETM_TRCPDSR Register

1 A53SS_CORE1_ETM_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

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Table 14-14223. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0314h**

Figure 14-4716. A53SS_CORE1_ETM_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPDSR_31_6							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPDSR_31_6							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-14225. A53SS_CORE1_ETM_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-14225. A53SS_CORE1_ETM_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.601 A53SS_CORE1_ETM_TRCACVR0_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

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Table 14-14226. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0400h**

Figure 14-4717. A53SS_CORE1_ETM_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14228. A53SS_CORE1_ETM_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.602 A53SS_CORE1_ETM_TRCACVR0_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

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Table 14-14229. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0404h**

Figure 14-4718. A53SS_CORE1_ETM_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14231. A53SS_CORE1_ETM_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.603 A53SS_CORE1_ETM_TRCACVR1_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-14232. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0408h**

Figure 14-4719. A53SS_CORE1_ETM_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14234. A53SS_CORE1_ETM_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.604 A53SS_CORE1_ETM_TRCACVR1_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-14235. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 040Ch**

Figure 14-4720. A53SS_CORE1_ETM_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14237. A53SS_CORE1_ETM_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.605 A53SS_CORE1_ETM_TRCACVR2_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-14238. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0410h**

Figure 14-4721. A53SS_CORE1_ETM_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14240. A53SS_CORE1_ETM_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.606 A53SS_CORE1_ETM_TRCACVR2_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-14241. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0414h**

Figure 14-4722. A53SS_CORE1_ETM_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14243. A53SS_CORE1_ETM_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.607 A53SS_CORE1_ETM_TRCACVR3_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-14244. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0418h**

Figure 14-4723. A53SS_CORE1_ETM_TRCACVR3_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14246. A53SS_CORE1_ETM_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.608 A53SS_CORE1_ETM_TRCACVR3_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

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Table 14-14247. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 041Ch**

Figure 14-4724. A53SS_CORE1_ETM_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14249. A53SS_CORE1_ETM_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.609 A53SS_CORE1_ETM_TRCACVR4_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

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Table 14-14250. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0420h**

Figure 14-4725. A53SS_CORE1_ETM_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14252. A53SS_CORE1_ETM_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.610 A53SS_CORE1_ETM_TRCACVR4_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

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Table 14-14253. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0424h**

Figure 14-4726. A53SS_CORE1_ETM_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14255. A53SS_CORE1_ETM_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.611 A53SS_CORE1_ETM_TRCACVR5_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

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Table 14-14256. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0428h**

Figure 14-4727. A53SS_CORE1_ETM_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14258. A53SS_CORE1_ETM_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.612 A53SS_CORE1_ETM_TRCACVR5_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

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Table 14-14259. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 042Ch**

Figure 14-4728. A53SS_CORE1_ETM_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14261. A53SS_CORE1_ETM_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.613 A53SS_CORE1_ETM_TRCACVR6_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

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Table 14-14262. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0430h**

Figure 14-4729. A53SS_CORE1_ETM_TRCACVR6_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14264. A53SS_CORE1_ETM_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.614 A53SS_CORE1_ETM_TRCACVR6_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

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Table 14-14265. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0434h**

Figure 14-4730. A53SS_CORE1_ETM_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14267. A53SS_CORE1_ETM_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.615 A53SS_CORE1_ETM_TRCACVR7_31_0 Register

1 A53SS_CORE1_ETM_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

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Table 14-14268. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0438h**

Figure 14-4731. A53SS_CORE1_ETM_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-14270. A53SS_CORE1_ETM_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.616 A53SS_CORE1_ETM_TRCACVR7_63_32 Register

1 A53SS_CORE1_ETM_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

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Table 14-14271. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 043Ch**

Figure 14-4732. A53SS_CORE1_ETM_TRCACVR7_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14273. A53SS_CORE1_ETM_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.617 A53SS_CORE1_ETM_TRCACATR0 Register

1 A53SS_CORE1_ETM_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-14274. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0480h**

Figure 14-4733. A53SS_CORE1_ETM_TRCACATR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR0_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR0_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR0_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14276. A53SS_CORE1_ETM_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14276. A53SS_CORE1_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14276. A53SS_CORE1_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14276. A53SS_CORE1_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.618 A53SS_CORE1_ETM_TRCACATR1 Register

1 A53SS_CORE1_ETM_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-14277. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0488h**

Figure 14-4734. A53SS_CORE1_ETM_TRCACATR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR1_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR1_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR1_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14279. A53SS_CORE1_ETM_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14279. A53SS_CORE1_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14279. A53SS_CORE1_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14279. A53SS_CORE1_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.619 A53SS_CORE1_ETM_TRCACATR2 Register

1 A53SS_CORE1_ETM_TRCACATR2 Register (Offset = 490h) [reset = 0h]

Address Comparator Access Type Registers 2

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Table 14-14280. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0490h**

Figure 14-4735. A53SS_CORE1_ETM_TRCACATR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR2_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR2_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-14282. A53SS_CORE1_ETM_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14282. A53SS_CORE1_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14282. A53SS_CORE1_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14282. A53SS_CORE1_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.620 A53SS_CORE1_ETM_TRCACATR3 Register

1 A53SS_CORE1_ETM_TRCACATR3 Register (Offset = 498h) [reset = 0h]

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Table 14-14283. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0498h**

Figure 14-4736. A53SS_CORE1_ETM_TRCACATR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR3_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR3_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR3_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14285. A53SS_CORE1_ETM_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14285. A53SS_CORE1_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14285. A53SS_CORE1_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14285. A53SS_CORE1_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.621 A53SS_CORE1_ETM_TRCACATR4 Register

1 A53SS_CORE1_ETM_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-14286. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04A0h**

Figure 14-4737. A53SS_CORE1_ETM_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-14288. A53SS_CORE1_ETM_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14288. A53SS_CORE1_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14288. A53SS_CORE1_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14288. A53SS_CORE1_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.622 A53SS_CORE1_ETM_TRCACATR5 Register

1 A53SS_CORE1_ETM_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-14289. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3013 04A8h**

Figure 14-4738. A53SS_CORE1_ETM_TRCACATR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR5_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR5_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR5_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-14291. A53SS_CORE1_ETM_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14291. A53SS_CORE1_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14291. A53SS_CORE1_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14291. A53SS_CORE1_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.623 A53SS_CORE1_ETM_TRCACATR6 Register

1 A53SS_CORE1_ETM_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

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Table 14-14292. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04B0h**

Figure 14-4739. A53SS_CORE1_ETM_TRCACATR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR6_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR6_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR6_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-14294. A53SS_CORE1_ETM_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14294. A53SS_CORE1_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14294. A53SS_CORE1_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14294. A53SS_CORE1_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.624 A53SS_CORE1_ETM_TRCACATR7 Register

1 A53SS_CORE1_ETM_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

Address Comparator Access Type Registers 7

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Table 14-14295. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04B8h**

Figure 14-4740. A53SS_CORE1_ETM_TRCACATR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR7_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR7_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR7_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14297. A53SS_CORE1_ETM_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-14297. A53SS_CORE1_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-14297. A53SS_CORE1_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-14297. A53SS_CORE1_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.625 A53SS_CORE1_ETM_TRCCIDCVR0 Register

1 A53SS_CORE1_ETM_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-14298. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0600h**

Figure 14-4741. A53SS_CORE1_ETM_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-14300. A53SS_CORE1_ETM_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.626 A53SS_CORE1_ETM_TRCVMIDCVR0 Register

1 A53SS_CORE1_ETM_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-14301. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0640h**

Figure 14-4742. A53SS_CORE1_ETM_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-14303. A53SS_CORE1_ETM_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.627 A53SS_CORE1_ETM_TRCCIDCCTLR0 Register

1 A53SS_CORE1_ETM_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

Return to Summary Table

Table 14-14304. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0680h**

Figure 14-4743. A53SS_CORE1_ETM_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-14306. A53SS_CORE1_ETM_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.628 A53SS_CORE1_ETM_TRCITATBIDR Register

1 A53SS_CORE1_ETM_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

Return to Summary Table

Table 14-14307. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EE4h**

Figure 14-4744. A53SS_CORE1_ETM_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-14309. A53SS_CORE1_ETM_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.629 A53SS_CORE1_ETM_TRCITIDATAR Register

1 A53SS_CORE1_ETM_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

Return to Summary Table

Table 14-14310. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EECh**

Figure 14-4745. A53SS_CORE1_ETM_TRCITIDATAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCITIDATAR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_TRCITIDATAR_31_5</td><td>ATDATAM_31</td><td>ATDATAM_23</td><td>ATDATAM_15</td><td>ATDATAM_7</td><td>ATDATAM_0</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14312. A53SS_CORE1_ETM_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.630 A53SS_CORE1_ETM_TRCITIATBINR Register

1 A53SS_CORE1_ETM_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

Return to Summary Table

Table 14-14313. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EF4h**

Figure 14-4746. A53SS_CORE1_ETM_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-14315. A53SS_CORE1_ETM_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.631 A53SS_CORE1_ETM_TRCITIATBOUTR Register

1 A53SS_CORE1_ETM_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-14316. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EFCh**

Figure 14-4747. A53SS_CORE1_ETM_TRCITIATBOUTR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCITIATBOUTR_31_10						BYTES	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_TRCITIATBOUTR_7_2						AFREADY	ATVALID
R/W						R/W	R/W
0h						0h	0h

Table 14-14318. A53SS_CORE1_ETM_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.632 A53SS_CORE1_ETM_TRCITCTRL Register

1 A53SS_CORE1_ETM_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

Return to Summary Table

Table 14-14319. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0F00h**

Figure 14-4748. A53SS_CORE1_ETM_TRCITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_TRCITCTRL_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCITCTRL_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCITCTRL_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCITCTRL_31_1							ITEN
R/W							R/W
0h							0h

Table 14-14321. A53SS_CORE1_ETM_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.633 A53SS_CORE1_ETM_TRCCLAIMSET Register

1 A53SS_CORE1_ETM_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

Return to Summary Table

Table 14-14322. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA0h**

Figure 14-4749. A53SS_CORE1_ETM_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-14324. A53SS_CORE1_ETM_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.634 A53SS_CORE1_ETM_TRCCLAIMCLR Register

1 A53SS_CORE1_ETM_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

Return to Summary Table

Table 14-14325. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA4h**

Figure 14-4750. A53SS_CORE1_ETM_TRCCLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCCLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCCLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_TRCCLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_TRCCLAIMCLR_31_4</td><td colspan="4">CLR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14327. A53SS_CORE1_ETM_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.635 A53SS_CORE1_ETM_TRCDEVAFF0 Register

1 A53SS_CORE1_ETM_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

Device Affinity Register 0

Return to Summary Table

Table 14-14328. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA8h**

Figure 14-4751. A53SS_CORE1_ETM_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
MPIDR_EL1_31_0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
MPIDR_EL1_31_0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
MPIDR_EL1_31_0							
R/W							
80000001h							

Table 14-14330. A53SS_CORE1_ETM_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000001h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.636 A53SS_CORE1_ETM_TRCDEVAFF1 Register

1 A53SS_CORE1_ETM_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

Return to Summary Table

Table 14-14331. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FACh**

Figure 14-4752. A53SS_CORE1_ETM_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-14333. A53SS_CORE1_ETM_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.637 A53SS_CORE1_ETM_TRCLAR Register

1 A53SS_CORE1_ETM_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

Return to Summary Table

Table 14-14334. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB0h**

Figure 14-4753. A53SS_CORE1_ETM_TRCLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-14336. A53SS_CORE1_ETM_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.638 A53SS_CORE1_ETM_TRCLSR Register

1 A53SS_CORE1_ETM_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

Return to Summary Table

Table 14-14337. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB4h**

Figure 14-4754. A53SS_CORE1_ETM_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14339. A53SS_CORE1_ETM_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.639 A53SS_CORE1_ETM_TRCAUTHSTATUS Register

1 A53SS_CORE1_ETM_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

Return to Summary Table

Table 14-14340. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB8h**

Figure 14-4755. A53SS_CORE1_ETM_TRCAUTHSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">2h</td><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14342. A53SS_CORE1_ETM_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-14342. A53SS_CORE1_ETM_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.640 A53SS_CORE1_ETM_TRCDEVARCH Register

1 A53SS_CORE1_ETM_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

Return to Summary Table

Table 14-14343. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FBCh**

Figure 14-4756. A53SS_CORE1_ETM_TRCDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
</table>

Table 14-14345. A53SS_CORE1_ETM_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.641 A53SS_CORE1_ETM_TRCDEVID Register

1 A53SS_CORE1_ETM_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

Return to Summary Table

Table 14-14346. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FC8h**

Figure 14-4757. A53SS_CORE1_ETM_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DEVID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DEVID							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVID							
R/W							
0h							

Table 14-14348. A53SS_CORE1_ETM_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.642 A53SS_CORE1_ETM_TRCDEVTYPE Register

1 A53SS_CORE1_ETM_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

Return to Summary Table

Table 14-14349. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FCCh**

Figure 14-4758. A53SS_CORE1_ETM_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-14351. A53SS_CORE1_ETM_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.643 A53SS_CORE1_ETM_TRCPIDR4 Register

1 A53SS_CORE1_ETM_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

Peripheral Identification Register 4

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Table 14-14352. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD0h**

Figure 14-4759. A53SS_CORE1_ETM_TRCPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-14354. A53SS_CORE1_ETM_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.644 A53SS_CORE1_ETM_TRCPIDR5 Register

1 A53SS_CORE1_ETM_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register 5

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Table 14-14355. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD4h**

Figure 14-4760. A53SS_CORE1_ETM_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-14357. A53SS_CORE1_ETM_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.645 A53SS_CORE1_ETM_TRCPIDR6 Register

1 A53SS_CORE1_ETM_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register 6

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Table 14-14358. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD8h**

Figure 14-4761. A53SS_CORE1_ETM_TRCPIDR6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR6_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR6_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR6_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_TRCPIDR6_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14360. A53SS_CORE1_ETM_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.646 A53SS_CORE1_ETM_TRCPIDR7 Register

1 A53SS_CORE1_ETM_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

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Table 14-14361. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FDCh**

Figure 14-4762. A53SS_CORE1_ETM_TRCPIDR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR7_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR7_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR7_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCPIDR7_7_0							
R/W							
0h							

Table 14-14363. A53SS_CORE1_ETM_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.647 A53SS_CORE1_ETM_TRCPIDR0 Register

1 A53SS_CORE1_ETM_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

Return to Summary Table

Table 14-14364. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE0h**

Figure 14-4763. A53SS_CORE1_ETM_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
5Dh							

Table 14-14366. A53SS_CORE1_ETM_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.648 A53SS_CORE1_ETM_TRCPIDR1 Register

1 A53SS_CORE1_ETM_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

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Table 14-14367. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE4h**

Figure 14-4764. A53SS_CORE1_ETM_TRCPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-14369. A53SS_CORE1_ETM_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.649 A53SS_CORE1_ETM_TRCPIDR2 Register

1 A53SS_CORE1_ETM_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-14370. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE8h**

Figure 14-4765. A53SS_CORE1_ETM_TRCPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-14372. A53SS_CORE1_ETM_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.650 A53SS_CORE1_ETM_TRCPIDR3 Register

1 A53SS_CORE1_ETM_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

Return to Summary Table

Table 14-14373. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FECh**

Figure 14-4766. A53SS_CORE1_ETM_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-14375. A53SS_CORE1_ETM_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.651 A53SS_CORE1_ETM_TRCCIDR0 Register

1 A53SS_CORE1_ETM_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

Return to Summary Table

Table 14-14376. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF0h**

Figure 14-4767. A53SS_CORE1_ETM_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-14378. A53SS_CORE1_ETM_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.652 A53SS_CORE1_ETM_TRCCIDR1 Register

1 A53SS_CORE1_ETM_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

Return to Summary Table

Table 14-14379. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF4h**

Figure 14-4768. A53SS_CORE1_ETM_TRCCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-14381. A53SS_CORE1_ETM_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.653 A53SS_CORE1_ETM_TRCCIDR2 Register

1 A53SS_CORE1_ETM_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-14382. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF8h**

Figure 14-4769. A53SS_CORE1_ETM_TRCCIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCCIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-14384. A53SS_CORE1_ETM_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.654 A53SS_CORE1_ETM_TRCCIDR3 Register

1 A53SS_CORE1_ETM_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

Return to Summary Table

Table 14-14385. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FFCh**

Figure 14-4770. A53SS_CORE1_ETM_TRCCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-14387. A53SS_CORE1_ETM_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.655 A53SS_CORE1_CTI_CTICONTROL Register

1 A53SS_CORE1_CTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

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Table 14-14388. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0000h**

Figure 14-4771. A53SS_CORE1_CTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICONTROL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICONTROL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-14390. A53SS_CORE1_CTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.656 A53SS_CORE1_CTI_CTIINTACK Register

1 A53SS_CORE1_CTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

Return to Summary Table

Table 14-14391. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0010h**

Figure 14-4772. A53SS_CORE1_CTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ACK_N							
R/W							
0h							

Table 14-14393. A53SS_CORE1_CTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.657 A53SS_CORE1_CTI_CTIAPPSET Register

1 A53SS_CORE1_CTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

Return to Summary Table

Table 14-14394. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0014h**

Figure 14-4773. A53SS_CORE1_CTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-14396. A53SS_CORE1_CTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.658 A53SS_CORE1_CTI_CTIAPPCLEAR Register

1 A53SS_CORE1_CTI_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

Return to Summary Table

Table 14-14397. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0018h**

Figure 14-4774. A53SS_CORE1_CTI_CTIAPPCLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIAPPCLEAR_31_4</td><td colspan="4">CTIAPPCLEARX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14399. A53SS_CORE1_CTI_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.659 A53SS_CORE1_CTI_CTIAPPPULSE Register

1 A53SS_CORE1_CTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

Return to Summary Table

Table 14-14400. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 001Ch**

Figure 14-4775. A53SS_CORE1_CTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPPULSE_31_4				CTIAPPPULSEX			
R/W				R/W			
0h				0h			

Table 14-14402. A53SS_CORE1_CTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.660 A53SS_CORE1_CTI_CTIINEN0 Register

1 A53SS_CORE1_CTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

Return to Summary Table

Table 14-14403. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0020h**

Figure 14-4776. A53SS_CORE1_CTI_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN0_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN0_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN0_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN0_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14405. A53SS_CORE1_CTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.661 A53SS_CORE1_CTI_CTIINEN1 Register

1 A53SS_CORE1_CTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

Return to Summary Table

Table 14-14406. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0024h**

Figure 14-4777. A53SS_CORE1_CTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14408. A53SS_CORE1_CTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.662 A53SS_CORE1_CTI_CTIINEN2 Register

1 A53SS_CORE1_CTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

Return to Summary Table

Table 14-14409. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0028h**

Figure 14-4778. A53SS_CORE1_CTI_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN2_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14411. A53SS_CORE1_CTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.663 A53SS_CORE1_CTI_CTIINEN3 Register

1 A53SS_CORE1_CTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-14412. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 002Ch**

Figure 14-4779. A53SS_CORE1_CTI_CTIINEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN3_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14414. A53SS_CORE1_CTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.664 A53SS_CORE1_CTI_CTIINEN4 Register

1 A53SS_CORE1_CTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

Return to Summary Table

Table 14-14415. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0030h**

Figure 14-4780. A53SS_CORE1_CTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14417. A53SS_CORE1_CTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.665 A53SS_CORE1_CTI_CTIINEN5 Register

1 A53SS_CORE1_CTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-14418. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0034h**

Figure 14-4781. A53SS_CORE1_CTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14420. A53SS_CORE1_CTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.666 A53SS_CORE1_CTI_CTIINEN6 Register

1 A53SS_CORE1_CTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-14421. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0038h**

Figure 14-4782. A53SS_CORE1_CTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN6_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14423. A53SS_CORE1_CTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.667 A53SS_CORE1_CTI_CTIINEN7 Register

1 A53SS_CORE1_CTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-14424. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 003Ch**

Figure 14-4783. A53SS_CORE1_CTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-14426. A53SS_CORE1_CTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.668 A53SS_CORE1_CTI_CTIOUTEN0 Register

1 A53SS_CORE1_CTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-14427. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A0h**

Figure 14-4784. A53SS_CORE1_CTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN0_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14429. A53SS_CORE1_CTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.669 A53SS_CORE1_CTI_CTIOUTEN1 Register

1 A53SS_CORE1_CTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

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Table 14-14430. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A4h**

Figure 14-4785. A53SS_CORE1_CTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN1_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14432. A53SS_CORE1_CTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.670 A53SS_CORE1_CTI_CTIOUTEN2 Register

1 A53SS_CORE1_CTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

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Table 14-14433. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A8h**

Figure 14-4786. A53SS_CORE1_CTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN2_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14435. A53SS_CORE1_CTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.671 A53SS_CORE1_CTI_CTIOUTEN3 Register

1 A53SS_CORE1_CTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

Return to Summary Table

Table 14-14436. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00ACh**

Figure 14-4787. A53SS_CORE1_CTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14438. A53SS_CORE1_CTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.672 A53SS_CORE1_CTI_CTIOUTEN4 Register

1 A53SS_CORE1_CTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

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Table 14-14439. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B0h**

Figure 14-4788. A53SS_CORE1_CTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14441. A53SS_CORE1_CTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.673 A53SS_CORE1_CTI_CTIOUTEN5 Register

1 A53SS_CORE1_CTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

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Table 14-14442. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B4h**

Figure 14-4789. A53SS_CORE1_CTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14444. A53SS_CORE1_CTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.674 A53SS_CORE1_CTI_CTIOUTEN6 Register

1 A53SS_CORE1_CTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

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Table 14-14445. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B8h**

Figure 14-4790. A53SS_CORE1_CTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14447. A53SS_CORE1_CTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.675 A53SS_CORE1_CTI_CTIOUTEN7 Register

1 A53SS_CORE1_CTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

Return to Summary Table

Table 14-14448. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00BCh**

Figure 14-4791. A53SS_CORE1_CTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-14450. A53SS_CORE1_CTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.676 A53SS_CORE1_CTI_CTITRIGINSTATUS Register

1 A53SS_CORE1_CTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-14451. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0130h**

Figure 14-4792. A53SS_CORE1_CTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TRINN							
R/W							
0h							

Table 14-14453. A53SS_CORE1_CTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.677 A53SS_CORE1_CTI_CTITRIGOUTSTATUS Register

1 A53SS_CORE1_CTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

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Table 14-14454. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0134h**

Figure 14-4793. A53SS_CORE1_CTI_CTITRIGOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTITRIGOUTSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTITRIGOUTSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTITRIGOUTSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TROUTN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14456. A53SS_CORE1_CTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.678 A53SS_CORE1_CTI_CTICHINSTATUS Register

1 A53SS_CORE1_CTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-14457. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0138h**

Figure 14-4794. A53SS_CORE1_CTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHINSTATUS_31_4				CHINN			
R/W				R/W			
0h				0h			

Table 14-14459. A53SS_CORE1_CTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.679 A53SS_CORE1_CTI_CTICHOUTSTATUS Register

1 A53SS_CORE1_CTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

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Table 14-14460. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 013Ch**

Figure 14-4795. A53SS_CORE1_CTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-14462. A53SS_CORE1_CTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.680 A53SS_CORE1_CTI_CTIGATE Register

1 A53SS_CORE1_CTI_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

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Table 14-14463. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0140h**

Figure 14-4796. A53SS_CORE1_CTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIGATE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIGATE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIGATE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIGATE_31_4				GATEX			
R/W				R/W			
0h				Fh			

Table 14-14465. A53SS_CORE1_CTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.681 A53SS_CORE1_CTI_ASICCTL Register

1 A53SS_CORE1_CTI_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

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Table 14-14466. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0144h**

Figure 14-4797. A53SS_CORE1_CTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-14468. A53SS_CORE1_CTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.682 A53SS_CORE1_CTI_CTIITCTRL Register

1 A53SS_CORE1_CTI_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

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Table 14-14469. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0F00h**

Figure 14-4798. A53SS_CORE1_CTI_CTIITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_CTIITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14471. A53SS_CORE1_CTI_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.683 A53SS_CORE1_CTI_CTICLAIMSET Register

1 A53SS_CORE1_CTI_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-14472. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FA0h**

Figure 14-4799. A53SS_CORE1_CTI_CTICLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICLAIMSET_31_4				CLAIMX			
R/W				R/W			
0h				Fh			

Table 14-14474. A53SS_CORE1_CTI_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.684 A53SS_CORE1_CTI_CTICLAIMCLR Register

1 A53SS_CORE1_CTI_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

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Table 14-14475. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FA4h**

Figure 14-4800. A53SS_CORE1_CTI_CTICLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTICLAIMCLR_31_4</td><td colspan="4">CLAIMX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14477. A53SS_CORE1_CTI_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.685 A53SS_CORE1_CTI_CTIDEVAFF0 Register

1 A53SS_CORE1_CTI_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

CTI Device Affinity Register 0

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Table 14-14478. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FA8h**

Figure 14-4801. A53SS_CORE1_CTI_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
CTIDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
CTIDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
CTIDEVAFF0							
R/W							
80000001h							

Table 14-14480. A53SS_CORE1_CTI_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.686 A53SS_CORE1_CTI_CTIDEVAFF1 Register

1 A53SS_CORE1_CTI_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-14481. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FACh**

Figure 14-4802. A53SS_CORE1_CTI_CTIDEVAFF1 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
CTIDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
CTIDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
CTIDEVAFF1							
R/W							
0h							

Table 14-14483. A53SS_CORE1_CTI_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.687 A53SS_CORE1_CTI_CTILAR Register

1 A53SS_CORE1_CTI_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

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Table 14-14484. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB0h**

Figure 14-4803. A53SS_CORE1_CTI_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-14486. A53SS_CORE1_CTI_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.688 A53SS_CORE1_CTI_CTILSR Register

1 A53SS_CORE1_CTI_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-14487. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB4h**

Figure 14-4804. A53SS_CORE1_CTI_CTILSR Name Register

31	30	29	28	27	26	25	24
RES0_CTILSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTILSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTILSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTILSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14489. A53SS_CORE1_CTI_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.689 A53SS_CORE1_CTI_CTIAUTHSTATUS Register

1 A53SS_CORE1_CTI_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-14490. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB8h**

Figure 14-4805. A53SS_CORE1_CTI_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-14492. A53SS_CORE1_CTI_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.690 A53SS_CORE1_CTI_CTIDEVARCH Register

1 A53SS_CORE1_CTI_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

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Table 14-14493. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FBCh**

Figure 14-4806. A53SS_CORE1_CTI_CTIDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
1A14h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
1A14h							

Table 14-14495. A53SS_CORE1_CTI_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.691 A53SS_CORE1_CTI_CTIDEVID2 Register

1 A53SS_CORE1_CTI_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

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Table 14-14496. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC0h**

Figure 14-4807. A53SS_CORE1_CTI_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-14498. A53SS_CORE1_CTI_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.692 A53SS_CORE1_CTI_CTIDEVID1 Register

1 A53SS_CORE1_CTI_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

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Table 14-14499. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC4h**

Figure 14-4808. A53SS_CORE1_CTI_CTIDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID1_31_0							
R/W							
0h							

Table 14-14501. A53SS_CORE1_CTI_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.693 A53SS_CORE1_CTI_CTIDEVID Register

1 A53SS_CORE1_CTI_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

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Table 14-14502. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC8h**

Figure 14-4809. A53SS_CORE1_CTI_CTIDEVID Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID_31_26						INOUT	
R/W						R/W	
0h						1h	
23	22	21	20	19	18	17	16
RES0_CTIDEVID_23_22		NUMCHAN					
R/W		R/W					
0h		4h					
15	14	13	12	11	10	9	8
RES0_CTIDEVID_15_14		NUMTRIG					
R/W		R/W					
0h		8h					
7	6	5	4	3	2	1	0
RES0_CTIDEVID_7_5			EXTMUXNUM				
R/W			R/W				
0h			0h				

Table 14-14504. A53SS_CORE1_CTI_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-14504. A53SS_CORE1_CTI_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.694 A53SS_CORE1_CTI_CTIDEVTYPE Register

1 A53SS_CORE1_CTI_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-14505. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FCCh**

Figure 14-4810. A53SS_CORE1_CTI_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-14507. A53SS_CORE1_CTI_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.695 A53SS_CORE1_CTI_CTIPIDR4 Register

1 A53SS_CORE1_CTI_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-14508. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FD0h**

Figure 14-4811. A53SS_CORE1_CTI_CTIPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-14510. A53SS_CORE1_CTI_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.696 A53SS_CORE1_CTI_CTIPIDR5 Register

1 A53SS_CORE1_CTI_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

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Table 14-14511. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FD4h**

Figure 14-4812. A53SS_CORE1_CTI_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-14513. A53SS_CORE1_CTI_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.697 A53SS_CORE1_CTI_CTIPIDR6 Register

1 A53SS_CORE1_CTI_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

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Table 14-14514. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FD8h**

Figure 14-4813. A53SS_CORE1_CTI_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-14516. A53SS_CORE1_CTI_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.698 A53SS_CORE1_CTI_CTIPIDR7 Register

1 A53SS_CORE1_CTI_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

Return to Summary Table

Table 14-14517. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FDCh**

Figure 14-4814. A53SS_CORE1_CTI_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-14519. A53SS_CORE1_CTI_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.699 A53SS_CORE1_CTI_CTIPIDR0 Register

1 A53SS_CORE1_CTI_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

Return to Summary Table

Table 14-14520. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE0h**

Figure 14-4815. A53SS_CORE1_CTI_CTIPIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIPIDR0_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">A8h</td></tr>
</table>

Table 14-14522. A53SS_CORE1_CTI_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.700 A53SS_CORE1_CTI_CTIPIDR1 Register

1 A53SS_CORE1_CTI_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

Return to Summary Table

Table 14-14523. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE4h**

Figure 14-4816. A53SS_CORE1_CTI_CTIPIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DES_0</td><td colspan="4">PART_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Bh</td><td colspan="4">9h</td></tr>
</table>

Table 14-14525. A53SS_CORE1_CTI_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.701 A53SS_CORE1_CTI_CTIPIDR2 Register

1 A53SS_CORE1_CTI_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

Return to Summary Table

Table 14-14526. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE8h**

Figure 14-4817. A53SS_CORE1_CTI_CTIPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-14528. A53SS_CORE1_CTI_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.702 A53SS_CORE1_CTI_CTIPIDR3 Register

1 A53SS_CORE1_CTI_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

Return to Summary Table

Table 14-14529. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FECh**

Figure 14-4818. A53SS_CORE1_CTI_CTIPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-14531. A53SS_CORE1_CTI_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.703 A53SS_CORE1_CTI_CTICIDR0 Register

1 A53SS_CORE1_CTI_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

Return to Summary Table

Table 14-14532. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF0h**

Figure 14-4819. A53SS_CORE1_CTI_CTICIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-14534. A53SS_CORE1_CTI_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.704 A53SS_CORE1_CTI_CTICIDR1 Register

1 A53SS_CORE1_CTI_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

Return to Summary Table

Table 14-14535. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF4h**

Figure 14-4820. A53SS_CORE1_CTI_CTICIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-14537. A53SS_CORE1_CTI_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.705 A53SS_CORE1_CTI_CTICIDR2 Register

1 A53SS_CORE1_CTI_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

Return to Summary Table

Table 14-14538. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF8h**

Figure 14-4821. A53SS_CORE1_CTI_CTICIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTICIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTICIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTICIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-14540. A53SS_CORE1_CTI_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.706 A53SS_CORE1_CTI_CTICIDR3 Register

1 A53SS_CORE1_CTI_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

Return to Summary Table

Table 14-14541. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FFCh**

Figure 14-4822. A53SS_CORE1_CTI_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-14543. A53SS_CORE1_CTI_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.707 A53SS_CORE2_DBG_EDESR Register

1 A53SS_CORE2_DBG_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

Return to Summary Table

Table 14-14544. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0020h**

Figure 14-4823. A53SS_CORE2_DBG_EDESR Name Register

31	30	29	28	27	26	25	24
RES0_EDESR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDESR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDESR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDESR_31_3					SS	RC	OSUC
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14546. A53SS_CORE2_DBG_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.708 A53SS_CORE2_DBG_EDECR Register

1 A53SS_CORE2_DBG_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

Return to Summary Table

Table 14-14547. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0024h**

Figure 14-4824. A53SS_CORE2_DBG_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDECR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDECR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14549. A53SS_CORE2_DBG_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.709 A53SS_CORE2_DBG_EDWAR_31_0 Register

1 A53SS_CORE2_DBG_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

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Table 14-14550. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0030h**

Figure 14-4825. A53SS_CORE2_DBG_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-14552. A53SS_CORE2_DBG_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.710 A53SS_CORE2_DBG_EDWAR_63_32 Register

1 A53SS_CORE2_DBG_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

Return to Summary Table

Table 14-14553. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0034h**

Figure 14-4826. A53SS_CORE2_DBG_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-14555. A53SS_CORE2_DBG_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.711 A53SS_CORE2_DBG_DBGDTRRX_EL0 Register

1 A53SS_CORE2_DBG_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

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Table 14-14556. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0080h**

Figure 14-4827. A53SS_CORE2_DBG_DBGDTRRX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRRX_EL0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGDTRRX_EL0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGDTRRX_EL0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGDTRRX_EL0							
R/W							
0h							

Table 14-14558. A53SS_CORE2_DBG_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.712 A53SS_CORE2_DBG_EDITR Register

1 A53SS_CORE2_DBG_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-14559. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0084h**

Figure 14-4828. A53SS_CORE2_DBG_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-14561. A53SS_CORE2_DBG_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.713 A53SS_CORE2_DBG_EDSCR Register

1 A53SS_CORE2_DBG_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

Return to Summary Table

Table 14-14562. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0088h**

Figure 14-4829. A53SS_CORE2_DBG_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	6	5	4	3	2	1	0
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-14564. A53SS_CORE2_DBG_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-14564. A53SS_CORE2_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-14564. A53SS_CORE2_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-14564. A53SS_CORE2_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.714 A53SS_CORE2_DBG_DBGDTRTX_EL0 Register

1 A53SS_CORE2_DBG_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-14565. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 008Ch**

Figure 14-4830. A53SS_CORE2_DBG_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-14567. A53SS_CORE2_DBG_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.715 A53SS_CORE2_DBG_EDRCR Register

1 A53SS_CORE2_DBG_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-14568. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0090h**

Figure 14-4831. A53SS_CORE2_DBG_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDRCR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDRCR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-14570. A53SS_CORE2_DBG_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-14570. A53SS_CORE2_DBG_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.716 A53SS_CORE2_DBG_EDACR Register

1 A53SS_CORE2_DBG_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-14571. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0094h**

Figure 14-4832. A53SS_CORE2_DBG_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-14573. A53SS_CORE2_DBG_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.717 A53SS_CORE2_DBG_EDECCR Register

1 A53SS_CORE2_DBG_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-14574. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0098h**

Figure 14-4833. A53SS_CORE2_DBG_EDECCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">NSE</td><td colspan="4">SE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14576. A53SS_CORE2_DBG_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-14576. A53SS_CORE2_DBG_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.718 A53SS_CORE2_DBG_EDPCSR_31_0 Register

1 A53SS_CORE2_DBG_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-14577. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 00A0h**

Figure 14-4834. A53SS_CORE2_DBG_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_31_0							
R/W							
0h							

Table 14-14579. A53SS_CORE2_DBG_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31:0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.719 A53SS_CORE2_DBG_EDCIDSR Register

1 A53SS_CORE2_DBG_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-14580. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 00A4h**

Figure 14-4835. A53SS_CORE2_DBG_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXTIDR							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXTIDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXTIDR							
R/W							
0h							

Table 14-14582. A53SS_CORE2_DBG_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.720 A53SS_CORE2_DBG_EDVIDSR Register

1 A53SS_CORE2_DBG_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-14583. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 00A8h**

Figure 14-4836. A53SS_CORE2_DBG_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-14585. A53SS_CORE2_DBG_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63:32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63:32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.721 A53SS_CORE2_DBG_EDPCSR_63_32 Register

1 A53SS_CORE2_DBG_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-14586. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 00ACh**

Figure 14-4837. A53SS_CORE2_DBG_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_63_32							
R/W							
0h							

Table 14-14588. A53SS_CORE2_DBG_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63:32] of the sampled PC.

14.3.1.1.2.722 A53SS_CORE2_DBG_OSLAR_EL1 Register

1 A53SS_CORE2_DBG_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-14589. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0300h**

Figure 14-4838. A53SS_CORE2_DBG_OSLAR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_OSLAR_EL1_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_OSLAR_EL1_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_OSLAR_EL1_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_OSLAR_EL1_31_1							OSLK
R/W							R/W
0h							0h

Table 14-14591. A53SS_CORE2_DBG_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.723 A53SS_CORE2_DBG_EDPRCR Register

1 A53SS_CORE2_DBG_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-14592. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0310h**

Figure 14-4839. A53SS_CORE2_DBG_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-14594. A53SS_CORE2_DBG_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-14594. A53SS_CORE2_DBG_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.724 A53SS_CORE2_DBG_EDPRSR Register

1 A53SS_CORE2_DBG_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-14595. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0314h**

Figure 14-4840. A53SS_CORE2_DBG_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPRSR_31_12							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-14597. A53SS_CORE2_DBG_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-14597. A53SS_CORE2_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-14597. A53SS_CORE2_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.725 A53SS_CORE2_DBG_DBGBVR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14598. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0400h**

Figure 14-4841. A53SS_CORE2_DBG_DBGBVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_31_0							
R/W							
0h							

Table 14-14600. A53SS_CORE2_DBG_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.726 A53SS_CORE2_DBG_DBGBVR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14601. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0404h**

Figure 14-4842. A53SS_CORE2_DBG_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-14603. A53SS_CORE2_DBG_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.727 A53SS_CORE2_DBG_DBGBCR0_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-14604. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0408h**

Figure 14-4843. A53SS_CORE2_DBG_DBGBCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR0_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR0_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR0_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-14606. A53SS_CORE2_DBG_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14606. A53SS_CORE2_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14606. A53SS_CORE2_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.728 A53SS_CORE2_DBG_DBGBVR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14607. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0410h**

Figure 14-4844. A53SS_CORE2_DBG_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-14609. A53SS_CORE2_DBG_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.729 A53SS_CORE2_DBG_DBGBVR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14610. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0414h**

Figure 14-4845. A53SS_CORE2_DBG_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-14612. A53SS_CORE2_DBG_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.730 A53SS_CORE2_DBG_DBGBCR1_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-14613. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0418h**

Figure 14-4846. A53SS_CORE2_DBG_DBGBCR1_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR1_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR1_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR1_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-14615. A53SS_CORE2_DBG_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14615. A53SS_CORE2_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14615. A53SS_CORE2_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.731 A53SS_CORE2_DBG_DBGBVR2_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14616. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0420h**

Figure 14-4847. A53SS_CORE2_DBG_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-14618. A53SS_CORE2_DBG_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.732 A53SS_CORE2_DBG_DBGBVR2_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14619. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0424h**

Figure 14-4848. A53SS_CORE2_DBG_DBGBVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_63_32							
R/W							
0h							

Table 14-14621. A53SS_CORE2_DBG_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.733 A53SS_CORE2_DBG_DBGBCR2_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-14622. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0428h**

Figure 14-4849. A53SS_CORE2_DBG_DBGBCR2_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR2_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR2_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR2_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-14624. A53SS_CORE2_DBG_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14624. A53SS_CORE2_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14624. A53SS_CORE2_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.734 A53SS_CORE2_DBG_DBGBVR3_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14625. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0430h**

Figure 14-4850. A53SS_CORE2_DBG_DBGBVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_31_0							
R/W							
0h							

Table 14-14627. A53SS_CORE2_DBG_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.735 A53SS_CORE2_DBG_DBGBVR3_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14628. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0434h**

Figure 14-4851. A53SS_CORE2_DBG_DBGBVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_63_32							
R/W							
0h							

Table 14-14630. A53SS_CORE2_DBG_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.736 A53SS_CORE2_DBG_DBGBCR3_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-14631. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0438h**

Figure 14-4852. A53SS_CORE2_DBG_DBGBCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR3_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR3_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR3_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-14633. A53SS_CORE2_DBG_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14633. A53SS_CORE2_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14633. A53SS_CORE2_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.737 A53SS_CORE2_DBG_DBGBVR4_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14634. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0440h**

Figure 14-4853. A53SS_CORE2_DBG_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-14636. A53SS_CORE2_DBG_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.738 A53SS_CORE2_DBG_DBGBVR4_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14637. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0444h**

Figure 14-4854. A53SS_CORE2_DBG_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-14639. A53SS_CORE2_DBG_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.739 A53SS_CORE2_DBG_DBGBCR4_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

Debug Breakpoint Control Register 4

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Table 14-14640. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0448h**

Figure 14-4855. A53SS_CORE2_DBG_DBGBCR4_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR4_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR4_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR4_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-14642. A53SS_CORE2_DBG_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14642. A53SS_CORE2_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14642. A53SS_CORE2_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.740 A53SS_CORE2_DBG_DBGBVR5_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14643. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0450h**

Figure 14-4856. A53SS_CORE2_DBG_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-14645. A53SS_CORE2_DBG_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.741 A53SS_CORE2_DBG_DBGBVR5_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-14646. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0454h**

Figure 14-4857. A53SS_CORE2_DBG_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-14648. A53SS_CORE2_DBG_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.742 A53SS_CORE2_DBG_DBGBCR5_EL1 Register

1 A53SS_CORE2_DBG_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

Debug Breakpoint Control Register 5

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Table 14-14649. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0458h**

Figure 14-4858. A53SS_CORE2_DBG_DBGBCR5_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR5_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR5_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR5_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-14651. A53SS_CORE2_DBG_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-14651. A53SS_CORE2_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-14651. A53SS_CORE2_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.743 A53SS_CORE2_DBG_DBGWVR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

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Table 14-14652. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0800h**

Figure 14-4859. A53SS_CORE2_DBG_DBGWVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR0_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-14654. A53SS_CORE2_DBG_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.744 A53SS_CORE2_DBG_DBGWVR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

Return to Summary Table

Table 14-14655. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0804h**

Figure 14-4860. A53SS_CORE2_DBG_DBGWVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-14657. A53SS_CORE2_DBG_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.745 A53SS_CORE2_DBG_DBGWCR0_EL1 Register

1 A53SS_CORE2_DBG_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

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Table 14-14658. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0808h**

Figure 14-4861. A53SS_CORE2_DBG_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-14660. A53SS_CORE2_DBG_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-14660. A53SS_CORE2_DBG_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.746 A53SS_CORE2_DBG_DBGWVR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

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Table 14-14661. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0810h**

Figure 14-4862. A53SS_CORE2_DBG_DBGWVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR1_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-14663. A53SS_CORE2_DBG_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.747 A53SS_CORE2_DBG_DBGWVR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

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Table 14-14664. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0814h**

Figure 14-4863. A53SS_CORE2_DBG_DBGWVR1_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14666. A53SS_CORE2_DBG_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.748 A53SS_CORE2_DBG_DBGWCR1_EL1 Register

1 A53SS_CORE2_DBG_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

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Table 14-14667. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0818h**

Figure 14-4864. A53SS_CORE2_DBG_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-14669. A53SS_CORE2_DBG_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-14669. A53SS_CORE2_DBG_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.749 A53SS_CORE2_DBG_DBGWVR2_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

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Table 14-14670. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0820h**

Figure 14-4865. A53SS_CORE2_DBG_DBGWVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR2_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-14672. A53SS_CORE2_DBG_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.750 A53SS_CORE2_DBG_DBGWVR2_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

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Table 14-14673. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0824h**

Figure 14-4866. A53SS_CORE2_DBG_DBGWVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-14675. A53SS_CORE2_DBG_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.751 A53SS_CORE2_DBG_DBGWCR2_EL1 Register

1 A53SS_CORE2_DBG_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

Return to Summary Table

Table 14-14676. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0828h**

Figure 14-4867. A53SS_CORE2_DBG_DBGWCR2_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RES0_DBGWCR2_EL1_31_29</td><td colspan="5">MASK</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RES0_DBGWCR2_EL1_23_21</td><td>WT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="5">BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">LSC</td><td colspan="2">PAC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-14678. A53SS_CORE2_DBG_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-14678. A53SS_CORE2_DBG_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.752 A53SS_CORE2_DBG_DBGWVR3_EL1_31_0 Register

1 A53SS_CORE2_DBG_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

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Table 14-14679. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0830h**

Figure 14-4868. A53SS_CORE2_DBG_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-14681. A53SS_CORE2_DBG_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.753 A53SS_CORE2_DBG_DBGWVR3_EL1_63_32 Register

1 A53SS_CORE2_DBG_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

Return to Summary Table

Table 14-14682. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0834h**

Figure 14-4869. A53SS_CORE2_DBG_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESS							VA
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA							
R/W							
0h							

Table 14-14684. A53SS_CORE2_DBG_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.754 A53SS_CORE2_DBG_DBGWCR3_EL1 Register

1 A53SS_CORE2_DBG_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

Return to Summary Table

Table 14-14685. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0838h**

Figure 14-4870. A53SS_CORE2_DBG_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-14687. A53SS_CORE2_DBG_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-14687. A53SS_CORE2_DBG_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.755 A53SS_CORE2_DBG_MIDR_EL1 Register

1 A53SS_CORE2_DBG_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-14688. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D00h**

Figure 14-4871. A53SS_CORE2_DBG_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-14690. A53SS_CORE2_DBG_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.756 A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

Return to Summary Table

Table 14-14691. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D20h**

Figure 14-4872. A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
EL3				EL2			
R/W				R/W			
2h				2h			
7	6	5	4	3	2	1	0
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-14693. A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-14693. A53SS_CORE2_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.757 A53SS_CORE2_DBG_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

Return to Summary Table

Table 14-14694. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D24h**

Figure 14-4873. A53SS_CORE2_DBG_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-14696. A53SS_CORE2_DBG_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.758 A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

Return to Summary Table

Table 14-14697. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D28h**

Figure 14-4874. A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	22	21	20	19	18	17	16
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	14	13	12	11	10	9	8
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	6	5	4	3	2	1	0
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-14699. A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-14699. A53SS_CORE2_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.759 A53SS_CORE2_DBG_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

Return to Summary Table

Table 14-14700. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D2Ch**

Figure 14-4875. A53SS_CORE2_DBG_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-14702. A53SS_CORE2_DBG_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.760 A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-14703. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D30h**

Figure 14-4876. A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-14705. A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-14705. A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.761 A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-14706. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D34h**

Figure 14-4877. A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-14708. A53SS_CORE2_DBG_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.762 A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

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Table 14-14709. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D38h**

Figure 14-4878. A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-14711. A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-14711. A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.763 A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

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Table 14-14712. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D3Ch**

Figure 14-4879. A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-14714. A53SS_CORE2_DBG_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.764 A53SS_CORE2_DBG_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

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Table 14-14715. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D40h**

Figure 14-4880. A53SS_CORE2_DBG_ID_AA64PFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-14717. A53SS_CORE2_DBG_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.765 A53SS_CORE2_DBG_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

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Table 14-14718. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D44h**

Figure 14-4881. A53SS_CORE2_DBG_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-14720. A53SS_CORE2_DBG_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.766 A53SS_CORE2_DBG_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

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Table 14-14721. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D48h**

Figure 14-4882. A53SS_CORE2_DBG_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-14723. A53SS_CORE2_DBG_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.767 A53SS_CORE2_DBG_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

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Table 14-14724. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D4Ch**

Figure 14-4883. A53SS_CORE2_DBG_ID_AA64DFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-14726. A53SS_CORE2_DBG_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.768 A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

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Table 14-14727. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D50h**

Figure 14-4884. A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-14729. A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.769 A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

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Table 14-14730. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D54h**

Figure 14-4885. A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-14732. A53SS_CORE2_DBG_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.770 A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-14733. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D58h**

Figure 14-4886. A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-14735. A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.771 A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

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Table 14-14736. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0D5Ch**

Figure 14-4887. A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-14738. A53SS_CORE2_DBG_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.772 A53SS_CORE2_DBG_EDITCTRL Register

1 A53SS_CORE2_DBG_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

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Table 14-14739. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0F00h**

Figure 14-4888. A53SS_CORE2_DBG_EDITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_EDITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14741. A53SS_CORE2_DBG_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.773 A53SS_CORE2_DBG_DBGCLAIMSET_EL1 Register

1 A53SS_CORE2_DBG_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-14742. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FA0h**

Figure 14-4889. A53SS_CORE2_DBG_DBGCLAIMSET_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
FFh							

Table 14-14744. A53SS_CORE2_DBG_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.774 A53SS_CORE2_DBG_DBGCLAIMCLR_EL1 Register

1 A53SS_CORE2_DBG_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-14745. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FA4h**

Figure 14-4890. A53SS_CORE2_DBG_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
0h							

Table 14-14747. A53SS_CORE2_DBG_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.775 A53SS_CORE2_DBG_EDDEVAFF0 Register

1 A53SS_CORE2_DBG_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000002h]

External Debug Device Affinity Register 0

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Table 14-14748. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FA8h**

Figure 14-4891. A53SS_CORE2_DBG_EDDEVAFF0 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF0							
R/W							
80000002h							
23	22	21	20	19	18	17	16
EDDEVAFF0							
R/W							
80000002h							
15	14	13	12	11	10	9	8
EDDEVAFF0							
R/W							
80000002h							
7	6	5	4	3	2	1	0
EDDEVAFF0							
R/W							
80000002h							

Table 14-14750. A53SS_CORE2_DBG_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000002h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.776 A53SS_CORE2_DBG_EDDEVAFF1 Register

1 A53SS_CORE2_DBG_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

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Table 14-14751. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FACh**

Figure 14-4892. A53SS_CORE2_DBG_EDDEVAFF1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14753. A53SS_CORE2_DBG_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.777 A53SS_CORE2_DBG_EDLAR Register

1 A53SS_CORE2_DBG_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

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Table 14-14754. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FB0h**

Figure 14-4893. A53SS_CORE2_DBG_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-14756. A53SS_CORE2_DBG_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.778 A53SS_CORE2_DBG_EDLSR Register

1 A53SS_CORE2_DBG_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

Return to Summary Table

Table 14-14757. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FB4h**

Figure 14-4894. A53SS_CORE2_DBG_EDLSR Name Register

31	30	29	28	27	26	25	24
RES0_EDLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14759. A53SS_CORE2_DBG_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.779 A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1 Register

1 A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

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Table 14-14760. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FB8h**

Figure 14-4895. A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		2h		2h		2h	

Table 14-14762. A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-14762. A53SS_CORE2_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.780 A53SS_CORE2_DBG_EDDEVARCH Register

1 A53SS_CORE2_DBG_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

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Table 14-14763. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FBCh**

Figure 14-4896. A53SS_CORE2_DBG_EDDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
6A15h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
6A15h							

Table 14-14765. A53SS_CORE2_DBG_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.781 A53SS_CORE2_DBG_EDDEVID2 Register

1 A53SS_CORE2_DBG_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

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Table 14-14766. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FC0h**

Figure 14-4897. A53SS_CORE2_DBG_EDDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID2_31_0							
R/W							
0h							

Table 14-14768. A53SS_CORE2_DBG_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.782 A53SS_CORE2_DBG_EDDEVID1 Register

1 A53SS_CORE2_DBG_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

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Table 14-14769. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FC4h**

Figure 14-4898. A53SS_CORE2_DBG_EDDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID1_31_4				PCSROFFSET			
R/W				R/W			
0h				2h			

Table 14-14771. A53SS_CORE2_DBG_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.783 A53SS_CORE2_DBG_EDDEVID Register

1 A53SS_CORE2_DBG_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

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Table 14-14772. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FC8h**

Figure 14-4899. A53SS_CORE2_DBG_EDDEVID Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID_31_28				AUXREGS			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDDEVID_23_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDDEVID_23_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDDEVID_23_4				PCSAMPLE			
R/W				R/W			
0h				3h			

Table 14-14774. A53SS_CORE2_DBG_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.784 A53SS_CORE2_DBG_EDDEVTYPE Register

1 A53SS_CORE2_DBG_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

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Table 14-14775. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FCCh**

Figure 14-4900. A53SS_CORE2_DBG_EDDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				5h			

Table 14-14777. A53SS_CORE2_DBG_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.785 A53SS_CORE2_DBG_EDPIDR4 Register

1 A53SS_CORE2_DBG_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

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Table 14-14778. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FD0h**

Figure 14-4901. A53SS_CORE2_DBG_EDPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-14780. A53SS_CORE2_DBG_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.786 A53SS_CORE2_DBG_EDPIDR0 Register

1 A53SS_CORE2_DBG_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

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Table 14-14781. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FE0h**

Figure 14-4902. A53SS_CORE2_DBG_EDPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
3h							

Table 14-14783. A53SS_CORE2_DBG_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.787 A53SS_CORE2_DBG_EDPIDR1 Register

1 A53SS_CORE2_DBG_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

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Table 14-14784. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FE4h**

Figure 14-4903. A53SS_CORE2_DBG_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-14786. A53SS_CORE2_DBG_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.788 A53SS_CORE2_DBG_EDPIDR2 Register

1 A53SS_CORE2_DBG_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

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Table 14-14787. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FE8h**

Figure 14-4904. A53SS_CORE2_DBG_EDPIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">3h</td></tr>
</table>

Table 14-14789. A53SS_CORE2_DBG_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.789 A53SS_CORE2_DBG_EDPIDR3 Register

1 A53SS_CORE2_DBG_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

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Table 14-14790. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FECh**

Figure 14-4905. A53SS_CORE2_DBG_EDPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-14792. A53SS_CORE2_DBG_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.790 A53SS_CORE2_DBG_EDCIDR0 Register

1 A53SS_CORE2_DBG_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

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Table 14-14793. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FF0h**

Figure 14-4906. A53SS_CORE2_DBG_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-14795. A53SS_CORE2_DBG_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.791 A53SS_CORE2_DBG_EDCIDR1 Register

1 A53SS_CORE2_DBG_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

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Table 14-14796. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FF4h**

Figure 14-4907. A53SS_CORE2_DBG_EDCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-14798. A53SS_CORE2_DBG_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.792 A53SS_CORE2_DBG_EDCIDR2 Register

1 A53SS_CORE2_DBG_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

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Table 14-14799. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FF8h**

Figure 14-4908. A53SS_CORE2_DBG_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-14801. A53SS_CORE2_DBG_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.793 A53SS_CORE2_DBG_EDCIDR3 Register

1 A53SS_CORE2_DBG_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

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Table 14-14802. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3021 0FFCh**

Figure 14-4909. A53SS_CORE2_DBG_EDCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-14804. A53SS_CORE2_DBG_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.794 A53SS_CORE2_PMU_PMEVCNTR0_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

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Table 14-14805. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0000h**

Figure 14-4910. A53SS_CORE2_PMU_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-14807. A53SS_CORE2_PMU_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.795 A53SS_CORE2_PMU_PMEVCNTR1_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

Return to Summary Table

Table 14-14808. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0008h**

Figure 14-4911. A53SS_CORE2_PMU_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-14810. A53SS_CORE2_PMU_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.796 A53SS_CORE2_PMU_PMEVCNTR2_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

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Table 14-14811. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0010h**

Figure 14-4912. A53SS_CORE2_PMU_PMEVCNTR2_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR2_EL0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PMEVCNTR2_EL0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMEVCNTR2_EL0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMEVCNTR2_EL0							
R/W							
0h							

Table 14-14813. A53SS_CORE2_PMU_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.797 A53SS_CORE2_PMU_PMEVCNTR3_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

Return to Summary Table

Table 14-14814. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0018h**

Figure 14-4913. A53SS_CORE2_PMU_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-14816. A53SS_CORE2_PMU_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.798 A53SS_CORE2_PMU_PMEVCNTR4_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

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Table 14-14817. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0020h**

Figure 14-4914. A53SS_CORE2_PMU_PMEVCNTR4_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR4_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR4_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR4_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR4_EL0							
R/W							
0h							

Table 14-14819. A53SS_CORE2_PMU_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.799 A53SS_CORE2_PMU_PMEVCNTR5_EL0 Register

1 A53SS_CORE2_PMU_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

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Table 14-14820. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0028h**

Figure 14-4915. A53SS_CORE2_PMU_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR5_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR5_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-14822. A53SS_CORE2_PMU_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.800 A53SS_CORE2_PMU_PMCCNTR_EL0_31_0 Register

1 A53SS_CORE2_PMU_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

Return to Summary Table

Table 14-14823. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 00F8h**

Figure 14-4916. A53SS_CORE2_PMU_PMCCNTR_EL0_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14825. A53SS_CORE2_PMU_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.801 A53SS_CORE2_PMU_PMCCNTR_EL0_63_32 Register

1 A53SS_CORE2_PMU_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

Return to Summary Table

Table 14-14826. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 00FCh**

Figure 14-4917. A53SS_CORE2_PMU_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-14828. A53SS_CORE2_PMU_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.802 A53SS_CORE2_PMU_PMEVTYPER0_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

Return to Summary Table

Table 14-14829. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0400h**

Figure 14-4918. A53SS_CORE2_PMU_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-14831. A53SS_CORE2_PMU_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14831. A53SS_CORE2_PMU_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.803 A53SS_CORE2_PMU_PMEVTYPER1_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

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Table 14-14832. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0404h**

Figure 14-4919. A53SS_CORE2_PMU_PMEVTYPER1_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER1_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER1_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER1_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-14834. A53SS_CORE2_PMU_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14834. A53SS_CORE2_PMU_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.804 A53SS_CORE2_PMU_PMEVTYPER2_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

Return to Summary Table

Table 14-14835. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0408h**

Figure 14-4920. A53SS_CORE2_PMU_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-14837. A53SS_CORE2_PMU_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14837. A53SS_CORE2_PMU_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.805 A53SS_CORE2_PMU_PMEVTYPER3_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-14838. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 040Ch**

Figure 14-4921. A53SS_CORE2_PMU_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-14840. A53SS_CORE2_PMU_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14840. A53SS_CORE2_PMU_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.806 A53SS_CORE2_PMU_PMEVTYPER4_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

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Table 14-14841. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0410h**

Figure 14-4922. A53SS_CORE2_PMU_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-14843. A53SS_CORE2_PMU_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14843. A53SS_CORE2_PMU_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.807 A53SS_CORE2_PMU_PMEVTYPER5_EL0 Register

1 A53SS_CORE2_PMU_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

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Table 14-14844. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0414h**

Figure 14-4923. A53SS_CORE2_PMU_PMEVTYPER5_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER5_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER5_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER5_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-14846. A53SS_CORE2_PMU_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-14846. A53SS_CORE2_PMU_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.808 A53SS_CORE2_PMU_PMCCFILTR_EL0 Register

1 A53SS_CORE2_PMU_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

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Table 14-14847. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 047Ch**

Figure 14-4924. A53SS_CORE2_PMU_PMCCFILTR_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMCCFILTR_EL0_25_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							

Table 14-14849. A53SS_CORE2_PMU_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-14849. A53SS_CORE2_PMU_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.809 A53SS_CORE2_PMU_PMCNTENSET_EL0 Register

1 A53SS_CORE2_PMU_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

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Table 14-14850. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0C00h**

Figure 14-4925. A53SS_CORE2_PMU_PMCNTENSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-14852. A53SS_CORE2_PMU_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.810 A53SS_CORE2_PMU_PMCNTENCLR_EL0 Register

1 A53SS_CORE2_PMU_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

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Table 14-14853. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0C20h**

Figure 14-4926. A53SS_CORE2_PMU_PMCNTENCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-14855. A53SS_CORE2_PMU_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.811 A53SS_CORE2_PMU_PMINTENSET_EL1 Register

1 A53SS_CORE2_PMU_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

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Table 14-14856. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0C40h**

Figure 14-4927. A53SS_CORE2_PMU_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-14858. A53SS_CORE2_PMU_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.812 A53SS_CORE2_PMU_PMINTENCLR_EL1 Register

1 A53SS_CORE2_PMU_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

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Table 14-14859. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0C60h**

Figure 14-4928. A53SS_CORE2_PMU_PMINTENCLR_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-14861. A53SS_CORE2_PMU_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.813 A53SS_CORE2_PMU_PMOVSCLR_EL0 Register

1 A53SS_CORE2_PMU_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

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Table 14-14862. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0C80h**

Figure 14-4929. A53SS_CORE2_PMU_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-14864. A53SS_CORE2_PMU_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.814 A53SS_CORE2_PMU_PMSWINC_EL0 Register

1 A53SS_CORE2_PMU_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

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Table 14-14865. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0CA0h**

Figure 14-4930. A53SS_CORE2_PMU_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-14867. A53SS_CORE2_PMU_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.815 A53SS_CORE2_PMU_PMOVSSET_EL0 Register

1 A53SS_CORE2_PMU_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

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Table 14-14868. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0CC0h**

Figure 14-4931. A53SS_CORE2_PMU_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-14870. A53SS_CORE2_PMU_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.816 A53SS_CORE2_PMU_PMCFGR Register

1 A53SS_CORE2_PMU_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-14871. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0E00h**

Figure 14-4932. A53SS_CORE2_PMU_PMCFGR Name Register

31	30	29	28	27	26	25	24
RES0_PMCFGR_31_20							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCFGR_31_20				UEN	WT	NA	EX
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	1h
15	14	13	12	11	10	9	8
CCD	CC	SIZE					
R/W	R/W	R/W					
1h	1h	3Fh					
7	6	5	4	3	2	1	0
N							
R/W							
6h							

Table 14-14873. A53SS_CORE2_PMU_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-14873. A53SS_CORE2_PMU_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.817 A53SS_CORE2_PMU_PMCR_EL0 Register

1 A53SS_CORE2_PMU_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-14874. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0E04h**

Figure 14-4933. A53SS_CORE2_PMU_PMCR_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCR_EL0_31_11							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_PMCR_EL0_31_11							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_PMCR_EL0_31_11					RES0_PMCR_EL0_10_7		
R/W					R/W		
0h					0h		

7	6	5	4	3	2	1	0
RES0_PMCR_EL0_10_7	LC	DP	X	D	C	P	E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14876. A53SS_CORE2_PMU_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-14876. A53SS_CORE2_PMU_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.818 A53SS_CORE2_PMU_PMCEID0_EL0 Register

1 A53SS_CORE2_PMU_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-14877. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0E20h**

Figure 14-4934. A53SS_CORE2_PMU_PMCEID0_EL0 Name Register

31	30	29	28	27	26	25	24
CE_31_0							
R/W							
67FFBFFFh							
23	22	21	20	19	18	17	16
CE_31_0							
R/W							
67FFBFFFh							
15	14	13	12	11	10	9	8
CE_31_0							
R/W							
67FFBFFFh							
7	6	5	4	3	2	1	0
CE_31_0							
R/W							
67FFBFFFh							

Table 14-14879. A53SS_CORE2_PMU_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.819 A53SS_CORE2_PMU_PMCEID1_EL0 Register

1 A53SS_CORE2_PMU_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-14880. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0E24h**

Figure 14-4935. A53SS_CORE2_PMU_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-14882. A53SS_CORE2_PMU_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.820 A53SS_CORE2_PMU_PMITCTRL Register

1 A53SS_CORE2_PMU_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-14883. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0F00h**

Figure 14-4936. A53SS_CORE2_PMU_PMITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_PMITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-14885. A53SS_CORE2_PMU_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.821 A53SS_CORE2_PMU_PMDEVAFF0 Register

1 A53SS_CORE2_PMU_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000002h]

Performance Monitors Device Affinity Register 0

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Table 14-14886. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FA8h**

Figure 14-4937. A53SS_CORE2_PMU_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000002h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000002h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000002h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000002h							

Table 14-14888. A53SS_CORE2_PMU_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000002h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.822 A53SS_CORE2_PMU_PMDEVAFF1 Register

1 A53SS_CORE2_PMU_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-14889. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FACh**

Figure 14-4938. A53SS_CORE2_PMU_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
PMDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
PMDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
PMDEVAFF1							
R/W							
0h							

Table 14-14891. A53SS_CORE2_PMU_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.823 A53SS_CORE2_PMU_PMLAR Register

1 A53SS_CORE2_PMU_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

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Table 14-14892. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FB0h**

Figure 14-4939. A53SS_CORE2_PMU_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-14894. A53SS_CORE2_PMU_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.824 A53SS_CORE2_PMU_PMLSR Register

1 A53SS_CORE2_PMU_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

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Table 14-14895. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FB4h**

Figure 14-4940. A53SS_CORE2_PMU_PMLSR Name Register

31	30	29	28	27	26	25	24
RES0_PMLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	1h	1h

Table 14-14897. A53SS_CORE2_PMU_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.825 A53SS_CORE2_PMU_PMAUTHSTATUS Register

1 A53SS_CORE2_PMU_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-14898. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FB8h**

Figure 14-4941. A53SS_CORE2_PMU_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-14900. A53SS_CORE2_PMU_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.826 A53SS_CORE2_PMU_PMDEVARCH Register

1 A53SS_CORE2_PMU_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

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Table 14-14901. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FBCh**

Figure 14-4942. A53SS_CORE2_PMU_PMDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2A16h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2A16h</td></tr>
</table>

Table 14-14903. A53SS_CORE2_PMU_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.827 A53SS_CORE2_PMU_PMDEVTYPE Register

1 A53SS_CORE2_PMU_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

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Table 14-14904. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FCCh**

Figure 14-4943. A53SS_CORE2_PMU_PMDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_PMDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				6h			

Table 14-14906. A53SS_CORE2_PMU_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.828 A53SS_CORE2_PMU_PMPIDR4 Register

1 A53SS_CORE2_PMU_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-14907. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FD0h**

Figure 14-4944. A53SS_CORE2_PMU_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-14909. A53SS_CORE2_PMU_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.829 A53SS_CORE2_PMU_PMPIDR5 Register

1 A53SS_CORE2_PMU_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

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Table 14-14910. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FD4h**

Figure 14-4945. A53SS_CORE2_PMU_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-14912. A53SS_CORE2_PMU_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.830 A53SS_CORE2_PMU_PMPIDR6 Register

1 A53SS_CORE2_PMU_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

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Table 14-14913. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FD8h**

Figure 14-4946. A53SS_CORE2_PMU_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-14915. A53SS_CORE2_PMU_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.831 A53SS_CORE2_PMU_PMPIDR7 Register

1 A53SS_CORE2_PMU_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

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Table 14-14916. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FDCh**

Figure 14-4947. A53SS_CORE2_PMU_PMPIDR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_PMPIDR7_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_PMPIDR7_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_PMPIDR7_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_PMPIDR7_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14918. A53SS_CORE2_PMU_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.832 A53SS_CORE2_PMU_PMPIDR0 Register

1 A53SS_CORE2_PMU_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

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Table 14-14919. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FE0h**

Figure 14-4948. A53SS_CORE2_PMU_PMPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
D3h							

Table 14-14921. A53SS_CORE2_PMU_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.833 A53SS_CORE2_PMU_PMPIDR1 Register

1 A53SS_CORE2_PMU_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-14922. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FE4h**

Figure 14-4949. A53SS_CORE2_PMU_PMPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-14924. A53SS_CORE2_PMU_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.834 A53SS_CORE2_PMU_PMPIDR2 Register

1 A53SS_CORE2_PMU_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

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Table 14-14925. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3022 0FE8h**

Figure 14-4950. A53SS_CORE2_PMU_PMPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-14927. A53SS_CORE2_PMU_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.835 A53SS_CORE2_PMU_PMPIDR3 Register

1 A53SS_CORE2_PMU_PMPIDR3 Register (Offset = FECh) [reset = 0h]

Performance Monitors Peripheral Identification Register 3

Return to Summary Table

Table 14-14928. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FECh**

Figure 14-4951. A53SS_CORE2_PMU_PMPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-14930. A53SS_CORE2_PMU_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.836 A53SS_CORE2_PMU_PMCIDR0 Register

1 A53SS_CORE2_PMU_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

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Table 14-14931. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FF0h**

Figure 14-4952. A53SS_CORE2_PMU_PMCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-14933. A53SS_CORE2_PMU_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.837 A53SS_CORE2_PMU_PMCIDR1 Register

1 A53SS_CORE2_PMU_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

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Table 14-14934. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FF4h**

Figure 14-4953. A53SS_CORE2_PMU_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-14936. A53SS_CORE2_PMU_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.838 A53SS_CORE2_PMU_PMCIDR2 Register

1 A53SS_CORE2_PMU_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-14937. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FF8h**

Figure 14-4954. A53SS_CORE2_PMU_PMCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-14939. A53SS_CORE2_PMU_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.839 A53SS_CORE2_PMU_PMCIDR3 Register

1 A53SS_CORE2_PMU_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

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Table 14-14940. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3022 0FFCh**

Figure 14-4955. A53SS_CORE2_PMU_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-14942. A53SS_CORE2_PMU_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.840 A53SS_CORE2_ETM_TRCPRGCTLR Register

1 A53SS_CORE2_ETM_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

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Table 14-14943. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0004h**

Figure 14-4956. A53SS_CORE2_ETM_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-14945. A53SS_CORE2_ETM_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.841 A53SS_CORE2_ETM_TRCSTATR Register

1 A53SS_CORE2_ETM_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

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Table 14-14946. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 000Ch**

Figure 14-4957. A53SS_CORE2_ETM_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-14948. A53SS_CORE2_ETM_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.842 A53SS_CORE2_ETM_TRCCONFIGR Register

1 A53SS_CORE2_ETM_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

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Table 14-14949. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0010h**

Figure 14-4958. A53SS_CORE2_ETM_TRCCONFIGR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCONFIGR_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCONFIGR_31_18						DV	DA
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCONFIGR_15_15	QE		RS	TS	COND		
R/W	R/W		R/W	R/W	R/W		
0h	0h		0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VMID	CID	RES0_TRCCONFIGR_5_5	CCI	BB	INSTP0		RES1_TRCCONFIGR_0_0
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		1h

Table 14-14951. A53SS_CORE2_ETM_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-14951. A53SS_CORE2_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-14951. A53SS_CORE2_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.843 A53SS_CORE2_ETM_TRCAUXCTLR Register

1 A53SS_CORE2_ETM_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

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Table 14-14952. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0018h**

Figure 14-4959. A53SS_CORE2_ETM_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14954. A53SS_CORE2_ETM_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.844 A53SS_CORE2_ETM_TRCEVENTCTL0R Register

1 A53SS_CORE2_ETM_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

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Table 14-14955. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0020h**

Figure 14-4960. A53SS_CORE2_ETM_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-14957. A53SS_CORE2_ETM_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.845 A53SS_CORE2_ETM_TRCEVENTCTL1R Register

1 A53SS_CORE2_ETM_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

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Table 14-14958. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0024h**

Figure 14-4961. A53SS_CORE2_ETM_TRCEVENTCTL1R Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEVENTCTL1R_31_13			LPOVERRIDE	ATB	RESERVED_TRCEVENTCTL1R_10_4		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEVENTCTL1R_10_4				EN			
R/W				R/W			
0h				0h			

Table 14-14960. A53SS_CORE2_ETM_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.846 A53SS_CORE2_ETM_TRCSTALLCTLR Register

1 A53SS_CORE2_ETM_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

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Table 14-14961. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 002Ch**

Figure 14-4962. A53SS_CORE2_ETM_TRCSTALLCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCSTALLCTLR_31_9							ISTALL
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_TRCSTALLCTLR_7_4				LEVEL		RESERVED_TRCSTALLCTLR_1_0	
R/W				R/W		R/W	
0h				0h		0h	

Table 14-14963. A53SS_CORE2_ETM_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.847 A53SS_CORE2_ETM_TRCTSCTLR Register

1 A53SS_CORE2_ETM_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

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Table 14-14964. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0030h**

Figure 14-4963. A53SS_CORE2_ETM_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-14966. A53SS_CORE2_ETM_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.848 A53SS_CORE2_ETM_TRCSYNCPR Register

1 A53SS_CORE2_ETM_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

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Table 14-14967. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0034h**

Figure 14-4964. A53SS_CORE2_ETM_TRCSYNCPR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSYNCPR_31_5							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSYNCPR_31_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSYNCPR_31_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSYNCPR_31_5			PERIOD				
R/W			R/W				
0h			0h				

Table 14-14969. A53SS_CORE2_ETM_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.849 A53SS_CORE2_ETM_TRCCCCTLR Register

1 A53SS_CORE2_ETM_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

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Table 14-14970. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0038h**

Figure 14-4965. A53SS_CORE2_ETM_TRCCCCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCCCTLR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCCCTLR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCCCTLR_31_12				THRESHOLD			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THRESHOLD							
R/W							
0h							

Table 14-14972. A53SS_CORE2_ETM_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.850 A53SS_CORE2_ETM_TRCBBCTLR Register

1 A53SS_CORE2_ETM_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

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Table 14-14973. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 003Ch**

Figure 14-4966. A53SS_CORE2_ETM_TRCBBCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCBBCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCBBCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCBBCTLR_31_9							MODE
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RANGE							
R/W							
0h							

Table 14-14975. A53SS_CORE2_ETM_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.851 A53SS_CORE2_ETM_TRCTRACEIDR Register

1 A53SS_CORE2_ETM_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-14976. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0040h**

Figure 14-4967. A53SS_CORE2_ETM_TRCTRACEIDR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED_TRCTRACEIDR_31_7</td><td colspan="7">TRACEID</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-14978. A53SS_CORE2_ETM_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.852 A53SS_CORE2_ETM_TRCVICTLR Register

1 A53SS_CORE2_ETM_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-14979. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0080h**

Figure 14-4968. A53SS_CORE2_ETM_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVENT							
R/W							
0h							

Table 14-14981. A53SS_CORE2_ETM_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-14981. A53SS_CORE2_ETM_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.853 A53SS_CORE2_ETM_TRCVIIECTLR Register

1 A53SS_CORE2_ETM_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

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Table 14-14982. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0084h**

Figure 14-4969. A53SS_CORE2_ETM_TRCVIIECTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVIIECTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXCLUDE							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCVIIECTLR_15_8							
R/W							
0h							
7	6	5	4	3	2	1	0
INCLUDE							
R/W							
0h							

Table 14-14984. A53SS_CORE2_ETM_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.854 A53SS_CORE2_ETM_TRCVISSCTLR Register

1 A53SS_CORE2_ETM_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

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Table 14-14985. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0088h**

Figure 14-4970. A53SS_CORE2_ETM_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	22	21	20	19	18	17	16
STOP							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 14-14987. A53SS_CORE2_ETM_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.855 A53SS_CORE2_ETM_TRCSEQEVR0 Register

1 A53SS_CORE2_ETM_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

Return to Summary Table

Table 14-14988. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0100h**

Figure 14-4971. A53SS_CORE2_ETM_TRCSEQEVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-14990. A53SS_CORE2_ETM_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.856 A53SS_CORE2_ETM_TRCSEQEVR1 Register

1 A53SS_CORE2_ETM_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

Return to Summary Table

Table 14-14991. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0104h**

Figure 14-4972. A53SS_CORE2_ETM_TRCSEQEVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-14993. A53SS_CORE2_ETM_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.857 A53SS_CORE2_ETM_TRCSEQEVR2 Register

1 A53SS_CORE2_ETM_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

Return to Summary Table

Table 14-14994. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0108h**

Figure 14-4973. A53SS_CORE2_ETM_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-14996. A53SS_CORE2_ETM_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.858 A53SS_CORE2_ETM_TRCSEQRSTEVR Register

1 A53SS_CORE2_ETM_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

Return to Summary Table

Table 14-14997. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0118h**

Figure 14-4974. A53SS_CORE2_ETM_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RST							
R/W							
0h							

Table 14-14999. A53SS_CORE2_ETM_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.859 A53SS_CORE2_ETM_TRCSEQSTR Register

1 A53SS_CORE2_ETM_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

Return to Summary Table

Table 14-15000. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 011Ch**

Figure 14-4975. A53SS_CORE2_ETM_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-15002. A53SS_CORE2_ETM_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.860 A53SS_CORE2_ETM_TRCEXTINSELR Register

1 A53SS_CORE2_ETM_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

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Table 14-15003. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0120h**

Figure 14-4976. A53SS_CORE2_ETM_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-15005. A53SS_CORE2_ETM_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.861 A53SS_CORE2_ETM_TRCCNTRLDVR0 Register

1 A53SS_CORE2_ETM_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

Return to Summary Table

Table 14-15006. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0140h**

Figure 14-4977. A53SS_CORE2_ETM_TRCCNTRLDVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE_N							
R/W							
0h							

Table 14-15008. A53SS_CORE2_ETM_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.862 A53SS_CORE2_ETM_TRCCNTRLDVR1 Register

1 A53SS_CORE2_ETM_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

Return to Summary Table

Table 14-15009. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0144h**

Figure 14-4978. A53SS_CORE2_ETM_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE_N							
R/W							
0h							

Table 14-15011. A53SS_CORE2_ETM_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.863 A53SS_CORE2_ETM_TRCCNTCTLR0 Register

1 A53SS_CORE2_ETM_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

Return to Summary Table

Table 14-15012. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0150h**

Figure 14-4979. A53SS_CORE2_ETM_TRCCNTCTLR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCNTCTLR0_31_18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RES0_TRCCNTCTLR0_31_18</td><td>CNTCHAIN_N</td><td>RLDSELF_N</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RLDEVENT_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CNTEVENT_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15014. A53SS_CORE2_ETM_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.864 A53SS_CORE2_ETM_TRCCNTCTLR1 Register

1 A53SS_CORE2_ETM_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

Return to Summary Table

Table 14-15015. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0154h**

Figure 14-4980. A53SS_CORE2_ETM_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RLDEVENT_N							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTEVENT_N							
R/W							
0h							

Table 14-15017. A53SS_CORE2_ETM_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.865 A53SS_CORE2_ETM_TRCCNTVR0 Register

1 A53SS_CORE2_ETM_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

Return to Summary Table

Table 14-15018. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0160h**

Figure 14-4981. A53SS_CORE2_ETM_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15020. A53SS_CORE2_ETM_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.866 A53SS_CORE2_ETM_TRCCNTVR1 Register

1 A53SS_CORE2_ETM_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

Return to Summary Table

Table 14-15021. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0164h**

Figure 14-4982. A53SS_CORE2_ETM_TRCCNTVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15023. A53SS_CORE2_ETM_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.867 A53SS_CORE2_ETM_TRCIDR8 Register

1 A53SS_CORE2_ETM_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

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Table 14-15024. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0180h**

Figure 14-4983. A53SS_CORE2_ETM_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							
23	22	21	20	19	18	17	16
MAXSPEC							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXSPEC							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXSPEC							
R/W							
0h							

Table 14-15026. A53SS_CORE2_ETM_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.868 A53SS_CORE2_ETM_TRCIDR9 Register

1 A53SS_CORE2_ETM_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-15027. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0184h**

Figure 14-4984. A53SS_CORE2_ETM_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-15029. A53SS_CORE2_ETM_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.869 A53SS_CORE2_ETM_TRCIDR10 Register

1 A53SS_CORE2_ETM_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-15030. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0188h**

Figure 14-4985. A53SS_CORE2_ETM_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-15032. A53SS_CORE2_ETM_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.870 A53SS_CORE2_ETM_TRCIDR11 Register

1 A53SS_CORE2_ETM_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-15033. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 018Ch**

Figure 14-4986. A53SS_CORE2_ETM_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-15035. A53SS_CORE2_ETM_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.871 A53SS_CORE2_ETM_TRCIDR12 Register

1 A53SS_CORE2_ETM_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-15036. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0190h**

Figure 14-4987. A53SS_CORE2_ETM_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-15038. A53SS_CORE2_ETM_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.872 A53SS_CORE2_ETM_TRCIDR13 Register

1 A53SS_CORE2_ETM_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

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Table 14-15039. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0194h**

Figure 14-4988. A53SS_CORE2_ETM_TRCIDR13 Name Register

31	30	29	28	27	26	25	24
NUMCONDSPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDSPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDSPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDSPC							
R/W							
0h							

Table 14-15041. A53SS_CORE2_ETM_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.873 A53SS_CORE2_ETM_TRCIMSPEC0 Register

1 A53SS_CORE2_ETM_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

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Table 14-15042. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01C0h**

Figure 14-4989. A53SS_CORE2_ETM_TRCIMSPEC0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EN				SUPPORT			
R/W				R/W			
0h				0h			

Table 14-15044. A53SS_CORE2_ETM_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.874 A53SS_CORE2_ETM_TRCIDR0 Register

1 A53SS_CORE2_ETM_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-15045. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01E0h**

Figure 14-4990. A53SS_CORE2_ETM_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	22	21	20	19	18	17	16
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	6	5	4	3	2	1	0
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-15047. A53SS_CORE2_ETM_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-15047. A53SS_CORE2_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-15047. A53SS_CORE2_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.875 A53SS_CORE2_ETM_TRCIDR1 Register

1 A53SS_CORE2_ETM_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

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Table 14-15048. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01E4h**

Figure 14-4991. A53SS_CORE2_ETM_TRCIDR1 Name Register

31	30	29	28	27	26	25	24
DESIGNER							
R/W							
41h							
23	22	21	20	19	18	17	16
RES0_TRCIDR1_23_16							
R/W							
0h							
15	14	13	12	11	10	9	8
RES1_TRCIDR1_15_12				TRCARCHMAJ			
R/W				R/W			
Fh				4h			
7	6	5	4	3	2	1	0
TRCARCHMIN				REVISION			
R/W				R/W			
0h				4h			

Table 14-15050. A53SS_CORE2_ETM_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-15050. A53SS_CORE2_ETM_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.876 A53SS_CORE2_ETM_TRCIDR2 Register

1 A53SS_CORE2_ETM_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

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Table 14-15051. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01E8h**

Figure 14-4992. A53SS_CORE2_ETM_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h
23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	
7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-15053. A53SS_CORE2_ETM_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-15053. A53SS_CORE2_ETM_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.877 A53SS_CORE2_ETM_TRCIDR3 Register

1 A53SS_CORE2_ETM_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

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Table 14-15054. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01ECh**

Figure 14-4993. A53SS_CORE2_ETM_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	14	13	12	11	10	9	8
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	6	5	4	3	2	1	0
CCITMIN							
R/W							
4h							

Table 14-15056. A53SS_CORE2_ETM_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-15056. A53SS_CORE2_ETM_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.878 A53SS_CORE2_ETM_TRCIDR4 Register

1 A53SS_CORE2_ETM_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

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Table 14-15057. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3023 01F0h**

Figure 14-4994. A53SS_CORE2_ETM_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			

23	22	21	20	19	18	17	16
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			

15	14	13	12	11	10	9	8
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h

7	6	5	4	3	2	1	0
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-15059. A53SS_CORE2_ETM_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-15059. A53SS_CORE2_ETM_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.879 A53SS_CORE2_ETM_TRCIDR5 Register

1 A53SS_CORE2_ETM_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-15060. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 01F4h**

Figure 14-4995. A53SS_CORE2_ETM_TRCIDR5 Name Register

31	30	29	28	27	26	25	24
REDFUNCNTR	NUMCNTR			NUMSEQSTATE			RES0_TRCIDR5_24_24
R/W	R/W			R/W			R/W
0h	2h			4h			0h
23	22	21	20	19	18	17	16
LPOVERRIDE	ATBTRIG	TRACEIDSIZE					
R/W	R/W	R/W					
1h	1h	7h					
15	14	13	12	11	10	9	8
RES0_TRCIDR5_15_12				NUMEXTINSEL			NUMEXTIN
R/W				R/W			R/W
0h				4h			1Eh
7	6	5	4	3	2	1	0
NUMEXTIN							
R/W							
1Eh							

Table 14-15062. A53SS_CORE2_ETM_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-15062. A53SS_CORE2_ETM_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.880 A53SS_CORE2_ETM_TRCRSCTLR2 Register

1 A53SS_CORE2_ETM_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

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Table 14-15063. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0208h**

Figure 14-4996. A53SS_CORE2_ETM_TRCRSCTLR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR2_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15065. A53SS_CORE2_ETM_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15065. A53SS_CORE2_ETM_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.881 A53SS_CORE2_ETM_TRCRSCTLR3 Register

1 A53SS_CORE2_ETM_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

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Table 14-15066. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 020Ch**

Figure 14-4997. A53SS_CORE2_ETM_TRCRSCTLR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR3_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR3_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15068. A53SS_CORE2_ETM_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15068. A53SS_CORE2_ETM_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.882 A53SS_CORE2_ETM_TRCRSCTLR4 Register

1 A53SS_CORE2_ETM_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

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Table 14-15069. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0210h**

Figure 14-4998. A53SS_CORE2_ETM_TRCRSCTLR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR4_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR4_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15071. A53SS_CORE2_ETM_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15071. A53SS_CORE2_ETM_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.883 A53SS_CORE2_ETM_TRCRSCTLR5 Register

1 A53SS_CORE2_ETM_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

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Table 14-15072. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0214h**

Figure 14-4999. A53SS_CORE2_ETM_TRCRSCTLR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR5_31_22							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCRSCTLR5_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							

7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15074. A53SS_CORE2_ETM_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15074. A53SS_CORE2_ETM_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.884 A53SS_CORE2_ETM_TRCRSCTLR6 Register

1 A53SS_CORE2_ETM_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

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Table 14-15075. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0218h**

Figure 14-5000. A53SS_CORE2_ETM_TRCRSCTLR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR6_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR6_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15077. A53SS_CORE2_ETM_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15077. A53SS_CORE2_ETM_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.885 A53SS_CORE2_ETM_TRCRSCTLR7 Register

1 A53SS_CORE2_ETM_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

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Table 14-15078. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 021Ch**

Figure 14-5001. A53SS_CORE2_ETM_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15080. A53SS_CORE2_ETM_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15080. A53SS_CORE2_ETM_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.886 A53SS_CORE2_ETM_TRCRSCTLR8 Register

1 A53SS_CORE2_ETM_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-15081. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0220h**

Figure 14-5002. A53SS_CORE2_ETM_TRCRSCTLR8 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR8_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR8_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15083. A53SS_CORE2_ETM_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15083. A53SS_CORE2_ETM_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.887 A53SS_CORE2_ETM_TRCRSCTLR9 Register

1 A53SS_CORE2_ETM_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-15084. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0224h**

Figure 14-5003. A53SS_CORE2_ETM_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15086. A53SS_CORE2_ETM_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15086. A53SS_CORE2_ETM_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.888 A53SS_CORE2_ETM_TRCRSCTLR10 Register

1 A53SS_CORE2_ETM_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-15087. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0228h**

Figure 14-5004. A53SS_CORE2_ETM_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15089. A53SS_CORE2_ETM_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15089. A53SS_CORE2_ETM_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.889 A53SS_CORE2_ETM_TRCRSCTLR11 Register

1 A53SS_CORE2_ETM_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-15090. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 022Ch**

Figure 14-5005. A53SS_CORE2_ETM_TRCRSCTLR11 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR11_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR11_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15092. A53SS_CORE2_ETM_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15092. A53SS_CORE2_ETM_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.890 A53SS_CORE2_ETM_TRCRSCTLR12 Register

1 A53SS_CORE2_ETM_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

Resource Selection Control Registers 12

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Table 14-15093. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0230h**

Figure 14-5006. A53SS_CORE2_ETM_TRCRSCTLR12 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR12_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR12_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15095. A53SS_CORE2_ETM_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15095. A53SS_CORE2_ETM_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.891 A53SS_CORE2_ETM_TRCRSCTLR13 Register

1 A53SS_CORE2_ETM_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

Resource Selection Control Registers 13

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Table 14-15096. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0234h**

Figure 14-5007. A53SS_CORE2_ETM_TRCRSCTLR13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR13_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR13_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15098. A53SS_CORE2_ETM_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15098. A53SS_CORE2_ETM_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.892 A53SS_CORE2_ETM_TRCRSCTLR14 Register

1 A53SS_CORE2_ETM_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

Resource Selection Control Registers 14

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Table 14-15099. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0238h**

Figure 14-5008. A53SS_CORE2_ETM_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15101. A53SS_CORE2_ETM_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15101. A53SS_CORE2_ETM_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.893 A53SS_CORE2_ETM_TRCRSCTLR15 Register

1 A53SS_CORE2_ETM_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

Resource Selection Control Registers 15

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Table 14-15102. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 023Ch**

Figure 14-5009. A53SS_CORE2_ETM_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15104. A53SS_CORE2_ETM_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15104. A53SS_CORE2_ETM_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.894 A53SS_CORE2_ETM_TRCSSCCR0 Register

1 A53SS_CORE2_ETM_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-15105. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0280h**

Figure 14-5010. A53SS_CORE2_ETM_TRCSSCCR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSSCCR0_31_25							RST
R/W							R/W
0h							0h
23	22	21	20	19	18	17	16
ARC							
R/W							
0h							
15	14	13	12	11	10	9	8
SAC							
R/W							
0h							
7	6	5	4	3	2	1	0
SAC							
R/W							
0h							

Table 14-15107. A53SS_CORE2_ETM_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-15107. A53SS_CORE2_ETM_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.895 A53SS_CORE2_ETM_TRCSSCSR0 Register

1 A53SS_CORE2_ETM_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-15108. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 02A0h**

Figure 14-5011. A53SS_CORE2_ETM_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-15110. A53SS_CORE2_ETM_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-15110. A53SS_CORE2_ETM_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.896 A53SS_CORE2_ETM_TRCOSLAR Register

1 A53SS_CORE2_ETM_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-15111. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0300h**

Figure 14-5012. A53SS_CORE2_ETM_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-15113. A53SS_CORE2_ETM_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.897 A53SS_CORE2_ETM_TRCOSLSR Register

1 A53SS_CORE2_ETM_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-15114. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0304h**

Figure 14-5013. A53SS_CORE2_ETM_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-15116. A53SS_CORE2_ETM_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.898 A53SS_CORE2_ETM_TRCPDCR Register

1 A53SS_CORE2_ETM_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-15117. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0310h**

Figure 14-5014. A53SS_CORE2_ETM_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPDCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPDCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-15119. A53SS_CORE2_ETM_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.899 A53SS_CORE2_ETM_TRCPDSR Register

1 A53SS_CORE2_ETM_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

Return to Summary Table

Table 14-15120. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0314h**

Figure 14-5015. A53SS_CORE2_ETM_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDSR_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDSR_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-15122. A53SS_CORE2_ETM_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-15122. A53SS_CORE2_ETM_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.900 A53SS_CORE2_ETM_TRCACVR0_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

Return to Summary Table

Table 14-15123. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0400h**

Figure 14-5016. A53SS_CORE2_ETM_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15125. A53SS_CORE2_ETM_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.901 A53SS_CORE2_ETM_TRCACVR0_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

Return to Summary Table

Table 14-15126. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0404h**

Figure 14-5017. A53SS_CORE2_ETM_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15128. A53SS_CORE2_ETM_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.902 A53SS_CORE2_ETM_TRCACVR1_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-15129. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0408h**

Figure 14-5018. A53SS_CORE2_ETM_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15131. A53SS_CORE2_ETM_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.903 A53SS_CORE2_ETM_TRCACVR1_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-15132. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 040Ch**

Figure 14-5019. A53SS_CORE2_ETM_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15134. A53SS_CORE2_ETM_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.904 A53SS_CORE2_ETM_TRCACVR2_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-15135. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0410h**

Figure 14-5020. A53SS_CORE2_ETM_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15137. A53SS_CORE2_ETM_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.905 A53SS_CORE2_ETM_TRCACVR2_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-15138. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0414h**

Figure 14-5021. A53SS_CORE2_ETM_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15140. A53SS_CORE2_ETM_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.906 A53SS_CORE2_ETM_TRCACVR3_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-15141. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0418h**

Figure 14-5022. A53SS_CORE2_ETM_TRCACVR3_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15143. A53SS_CORE2_ETM_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.907 A53SS_CORE2_ETM_TRCACVR3_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

Return to Summary Table

Table 14-15144. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 041Ch**

Figure 14-5023. A53SS_CORE2_ETM_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15146. A53SS_CORE2_ETM_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.908 A53SS_CORE2_ETM_TRCACVR4_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

Return to Summary Table

Table 14-15147. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0420h**

Figure 14-5024. A53SS_CORE2_ETM_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15149. A53SS_CORE2_ETM_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.909 A53SS_CORE2_ETM_TRCACVR4_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

Return to Summary Table

Table 14-15150. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0424h**

Figure 14-5025. A53SS_CORE2_ETM_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15152. A53SS_CORE2_ETM_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.910 A53SS_CORE2_ETM_TRCACVR5_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

Return to Summary Table

Table 14-15153. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0428h**

Figure 14-5026. A53SS_CORE2_ETM_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15155. A53SS_CORE2_ETM_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.911 A53SS_CORE2_ETM_TRCACVR5_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

Return to Summary Table

Table 14-15156. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 042Ch**

Figure 14-5027. A53SS_CORE2_ETM_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15158. A53SS_CORE2_ETM_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.912 A53SS_CORE2_ETM_TRCACVR6_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

Return to Summary Table

Table 14-15159. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0430h**

Figure 14-5028. A53SS_CORE2_ETM_TRCACVR6_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15161. A53SS_CORE2_ETM_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.913 A53SS_CORE2_ETM_TRCACVR6_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

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Table 14-15162. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0434h**

Figure 14-5029. A53SS_CORE2_ETM_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15164. A53SS_CORE2_ETM_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.914 A53SS_CORE2_ETM_TRCACVR7_31_0 Register

1 A53SS_CORE2_ETM_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

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Table 14-15165. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3023 0438h**

Figure 14-5030. A53SS_CORE2_ETM_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15167. A53SS_CORE2_ETM_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.915 A53SS_CORE2_ETM_TRCACVR7_63_32 Register

1 A53SS_CORE2_ETM_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

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Table 14-15168. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 043Ch**

Figure 14-5031. A53SS_CORE2_ETM_TRCACVR7_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-15170. A53SS_CORE2_ETM_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.916 A53SS_CORE2_ETM_TRCACATR0 Register

1 A53SS_CORE2_ETM_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-15171. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0480h**

Figure 14-5032. A53SS_CORE2_ETM_TRCACATR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR0_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR0_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR0_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15173. A53SS_CORE2_ETM_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15173. A53SS_CORE2_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15173. A53SS_CORE2_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15173. A53SS_CORE2_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.917 A53SS_CORE2_ETM_TRCACATR1 Register

1 A53SS_CORE2_ETM_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-15174. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0488h**

Figure 14-5033. A53SS_CORE2_ETM_TRCACATR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR1_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR1_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR1_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-15176. A53SS_CORE2_ETM_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15176. A53SS_CORE2_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15176. A53SS_CORE2_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15176. A53SS_CORE2_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.918 A53SS_CORE2_ETM_TRCACATR2 Register

1 A53SS_CORE2_ETM_TRCACATR2 Register (Offset = 490h) [reset = 0h]

Address Comparator Access Type Registers 2

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Table 14-15177. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0490h**

Figure 14-5034. A53SS_CORE2_ETM_TRCACATR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR2_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR2_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR2_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15179. A53SS_CORE2_ETM_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15179. A53SS_CORE2_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15179. A53SS_CORE2_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15179. A53SS_CORE2_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.919 A53SS_CORE2_ETM_TRCACATR3 Register

1 A53SS_CORE2_ETM_TRCACATR3 Register (Offset = 498h) [reset = 0h]

Address Comparator Access Type Registers 3

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Table 14-15180. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0498h**

Figure 14-5035. A53SS_CORE2_ETM_TRCACATR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR3_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR3_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-15182. A53SS_CORE2_ETM_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15182. A53SS_CORE2_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15182. A53SS_CORE2_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15182. A53SS_CORE2_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.920 A53SS_CORE2_ETM_TRCACATR4 Register

1 A53SS_CORE2_ETM_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-15183. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 04A0h**

Figure 14-5036. A53SS_CORE2_ETM_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-15185. A53SS_CORE2_ETM_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15185. A53SS_CORE2_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15185. A53SS_CORE2_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15185. A53SS_CORE2_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.921 A53SS_CORE2_ETM_TRCACATR5 Register

1 A53SS_CORE2_ETM_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-15186. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 04A8h**

Figure 14-5037. A53SS_CORE2_ETM_TRCACATR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR5_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR5_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR5_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15188. A53SS_CORE2_ETM_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15188. A53SS_CORE2_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15188. A53SS_CORE2_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15188. A53SS_CORE2_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.922 A53SS_CORE2_ETM_TRCACATR6 Register

1 A53SS_CORE2_ETM_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

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Table 14-15189. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 04B0h**

Figure 14-5038. A53SS_CORE2_ETM_TRCACATR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR6_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR6_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR6_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-15191. A53SS_CORE2_ETM_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15191. A53SS_CORE2_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15191. A53SS_CORE2_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15191. A53SS_CORE2_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.923 A53SS_CORE2_ETM_TRCACATR7 Register

1 A53SS_CORE2_ETM_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

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Table 14-15192. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 04B8h**

Figure 14-5039. A53SS_CORE2_ETM_TRCACATR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR7_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR7_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR7_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-15194. A53SS_CORE2_ETM_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-15194. A53SS_CORE2_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-15194. A53SS_CORE2_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-15194. A53SS_CORE2_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.924 A53SS_CORE2_ETM_TRCCIDCVR0 Register

1 A53SS_CORE2_ETM_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-15195. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0600h**

Figure 14-5040. A53SS_CORE2_ETM_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-15197. A53SS_CORE2_ETM_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.925 A53SS_CORE2_ETM_TRCVMIDCVR0 Register

1 A53SS_CORE2_ETM_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-15198. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0640h**

Figure 14-5041. A53SS_CORE2_ETM_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE							
R/W							
0h							

Table 14-15200. A53SS_CORE2_ETM_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.926 A53SS_CORE2_ETM_TRCCIDCCTLR0 Register

1 A53SS_CORE2_ETM_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

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Table 14-15201. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0680h**

Figure 14-5042. A53SS_CORE2_ETM_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-15203. A53SS_CORE2_ETM_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.927 A53SS_CORE2_ETM_TRCITATBIDR Register

1 A53SS_CORE2_ETM_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

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Table 14-15204. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0EE4h**

Figure 14-5043. A53SS_CORE2_ETM_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-15206. A53SS_CORE2_ETM_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.928 A53SS_CORE2_ETM_TRCITIDATAR Register

1 A53SS_CORE2_ETM_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

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Table 14-15207. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0EECh**

Figure 14-5044. A53SS_CORE2_ETM_TRCITIDATAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITIDATAR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITIDATAR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITIDATAR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITIDATAR_31_5			ATDATAM_31	ATDATAM_23	ATDATAM_15	ATDATAM_7	ATDATAM_0
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-15209. A53SS_CORE2_ETM_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.929 A53SS_CORE2_ETM_TRCITIATBINR Register

1 A53SS_CORE2_ETM_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

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Table 14-15210. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0EF4h**

Figure 14-5045. A53SS_CORE2_ETM_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-15212. A53SS_CORE2_ETM_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.930 A53SS_CORE2_ETM_TRCITIATBOUTR Register

1 A53SS_CORE2_ETM_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-15213. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0EFCh**

Figure 14-5046. A53SS_CORE2_ETM_TRCITIATBOUTR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCITIATBOUTR_31_10						BYTES	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCITIATBOUTR_7_2						AFREADY	ATVALID
R/W						R/W	R/W
0h						0h	0h

Table 14-15215. A53SS_CORE2_ETM_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.931 A53SS_CORE2_ETM_TRCITCTRL Register

1 A53SS_CORE2_ETM_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

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Table 14-15216. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0F00h**

Figure 14-5047. A53SS_CORE2_ETM_TRCITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_TRCITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITCTRL_31_1							ITEN
R/W							R/W
0h							0h

Table 14-15218. A53SS_CORE2_ETM_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.932 A53SS_CORE2_ETM_TRCCLAIMSET Register

1 A53SS_CORE2_ETM_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-15219. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FA0h**

Figure 14-5048. A53SS_CORE2_ETM_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-15221. A53SS_CORE2_ETM_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.933 A53SS_CORE2_ETM_TRCCLAIMCLR Register

1 A53SS_CORE2_ETM_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-15222. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FA4h**

Figure 14-5049. A53SS_CORE2_ETM_TRCCLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMCLR_31_4				CLR			
R/W				R/W			
0h				0h			

Table 14-15224. A53SS_CORE2_ETM_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.934 A53SS_CORE2_ETM_TRCDEVAFF0 Register

1 A53SS_CORE2_ETM_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000002h]

Device Affinity Register 0

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Table 14-15225. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FA8h**

Figure 14-5050. A53SS_CORE2_ETM_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000002h							
23	22	21	20	19	18	17	16
MPIDR_EL1_31_0							
R/W							
80000002h							
15	14	13	12	11	10	9	8
MPIDR_EL1_31_0							
R/W							
80000002h							
7	6	5	4	3	2	1	0
MPIDR_EL1_31_0							
R/W							
80000002h							

Table 14-15227. A53SS_CORE2_ETM_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000002h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.935 A53SS_CORE2_ETM_TRCDEVAFF1 Register

1 A53SS_CORE2_ETM_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

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Table 14-15228. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FACh**

Figure 14-5051. A53SS_CORE2_ETM_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-15230. A53SS_CORE2_ETM_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.936 A53SS_CORE2_ETM_TRCLAR Register

1 A53SS_CORE2_ETM_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

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Table 14-15231. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FB0h**

Figure 14-5052. A53SS_CORE2_ETM_TRCLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-15233. A53SS_CORE2_ETM_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.937 A53SS_CORE2_ETM_TRCLSR Register

1 A53SS_CORE2_ETM_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

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Table 14-15234. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FB4h**

Figure 14-5053. A53SS_CORE2_ETM_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-15236. A53SS_CORE2_ETM_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.938 A53SS_CORE2_ETM_TRCAUTHSTATUS Register

1 A53SS_CORE2_ETM_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

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Table 14-15237. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FB8h**

Figure 14-5054. A53SS_CORE2_ETM_TRCAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-15239. A53SS_CORE2_ETM_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-15239. A53SS_CORE2_ETM_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.939 A53SS_CORE2_ETM_TRCDEVARCH Register

1 A53SS_CORE2_ETM_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

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Table 14-15240. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FBCh**

Figure 14-5055. A53SS_CORE2_ETM_TRCDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
4A13h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
4A13h							

Table 14-15242. A53SS_CORE2_ETM_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.940 A53SS_CORE2_ETM_TRCDEVID Register

1 A53SS_CORE2_ETM_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

Return to Summary Table

Table 14-15243. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FC8h**

Figure 14-5056. A53SS_CORE2_ETM_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVID							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVID							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVID							
R/W							
0h							

Table 14-15245. A53SS_CORE2_ETM_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.941 A53SS_CORE2_ETM_TRCDEVTYPE Register

1 A53SS_CORE2_ETM_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

Return to Summary Table

Table 14-15246. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FCCh**

Figure 14-5057. A53SS_CORE2_ETM_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-15248. A53SS_CORE2_ETM_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.942 A53SS_CORE2_ETM_TRCPIDR4 Register

1 A53SS_CORE2_ETM_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

Peripheral Identification Register 4

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Table 14-15249. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FD0h**

Figure 14-5058. A53SS_CORE2_ETM_TRCPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-15251. A53SS_CORE2_ETM_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.943 A53SS_CORE2_ETM_TRCPIDR5 Register

1 A53SS_CORE2_ETM_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register 5

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Table 14-15252. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FD4h**

Figure 14-5059. A53SS_CORE2_ETM_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-15254. A53SS_CORE2_ETM_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.944 A53SS_CORE2_ETM_TRCPIDR6 Register

1 A53SS_CORE2_ETM_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register 6

Return to Summary Table

Table 14-15255. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FD8h**

Figure 14-5060. A53SS_CORE2_ETM_TRCPIDR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR6_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR6_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR6_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR6_7_0							
R/W							
0h							

Table 14-15257. A53SS_CORE2_ETM_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.945 A53SS_CORE2_ETM_TRCPIDR7 Register

1 A53SS_CORE2_ETM_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

Return to Summary Table

Table 14-15258. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FDCh**

Figure 14-5061. A53SS_CORE2_ETM_TRCPIDR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_TRCPIDR7_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15260. A53SS_CORE2_ETM_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.946 A53SS_CORE2_ETM_TRCPIDR0 Register

1 A53SS_CORE2_ETM_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

Return to Summary Table

Table 14-15261. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FE0h**

Figure 14-5062. A53SS_CORE2_ETM_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
5Dh							

Table 14-15263. A53SS_CORE2_ETM_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.947 A53SS_CORE2_ETM_TRCPIDR1 Register

1 A53SS_CORE2_ETM_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

Return to Summary Table

Table 14-15264. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FE4h**

Figure 14-5063. A53SS_CORE2_ETM_TRCPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-15266. A53SS_CORE2_ETM_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.948 A53SS_CORE2_ETM_TRCPIDR2 Register

1 A53SS_CORE2_ETM_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-15267. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FE8h**

Figure 14-5064. A53SS_CORE2_ETM_TRCPIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">3h</td></tr>
</table>

Table 14-15269. A53SS_CORE2_ETM_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.949 A53SS_CORE2_ETM_TRCPIDR3 Register

1 A53SS_CORE2_ETM_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

Return to Summary Table

Table 14-15270. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FECh**

Figure 14-5065. A53SS_CORE2_ETM_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-15272. A53SS_CORE2_ETM_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.950 A53SS_CORE2_ETM_TRCCIDR0 Register

1 A53SS_CORE2_ETM_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

Return to Summary Table

Table 14-15273. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FF0h**

Figure 14-5066. A53SS_CORE2_ETM_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-15275. A53SS_CORE2_ETM_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.951 A53SS_CORE2_ETM_TRCCIDR1 Register

1 A53SS_CORE2_ETM_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

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Table 14-15276. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FF4h**

Figure 14-5067. A53SS_CORE2_ETM_TRCCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-15278. A53SS_CORE2_ETM_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.952 A53SS_CORE2_ETM_TRCCIDR2 Register

1 A53SS_CORE2_ETM_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-15279. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FF8h**

Figure 14-5068. A53SS_CORE2_ETM_TRCCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_2							
R/W							
5h							

Table 14-15281. A53SS_CORE2_ETM_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.953 A53SS_CORE2_ETM_TRCCIDR3 Register

1 A53SS_CORE2_ETM_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

Return to Summary Table

Table 14-15282. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3023 0FFCh**

Figure 14-5069. A53SS_CORE2_ETM_TRCCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-15284. A53SS_CORE2_ETM_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.954 A53SS_CORE2_CTI_CTICONTROL Register

1 A53SS_CORE2_CTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

Return to Summary Table

Table 14-15285. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0000h**

Figure 14-5070. A53SS_CORE2_CTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICONTROL_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICONTROL_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-15287. A53SS_CORE2_CTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.955 A53SS_CORE2_CTI_CTIINTACK Register

1 A53SS_CORE2_CTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

Return to Summary Table

Table 14-15288. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0010h**

Figure 14-5071. A53SS_CORE2_CTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACK_N							
R/W							
0h							

Table 14-15290. A53SS_CORE2_CTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.956 A53SS_CORE2_CTI_CTIAPPSET Register

1 A53SS_CORE2_CTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

Return to Summary Table

Table 14-15291. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0014h**

Figure 14-5072. A53SS_CORE2_CTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-15293. A53SS_CORE2_CTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.957 A53SS_CORE2_CTI_CTIAPPCLEAR Register

1 A53SS_CORE2_CTI_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

Return to Summary Table

Table 14-15294. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0018h**

Figure 14-5073. A53SS_CORE2_CTI_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIAPPCLEAR_31_4				CTIAPPCLEARX			
R/W				R/W			
0h				0h			

Table 14-15296. A53SS_CORE2_CTI_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.958 A53SS_CORE2_CTI_CTIAPPPULSE Register

1 A53SS_CORE2_CTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

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Table 14-15297. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 001Ch**

Figure 14-5074. A53SS_CORE2_CTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPPULSE_31_4				CTIAPPPULSEX			
R/W				R/W			
0h				0h			

Table 14-15299. A53SS_CORE2_CTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.959 A53SS_CORE2_CTI_CTIINEN0 Register

1 A53SS_CORE2_CTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

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Table 14-15300. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0020h**

Figure 14-5075. A53SS_CORE2_CTI_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN0_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN0_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN0_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN0_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15302. A53SS_CORE2_CTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.960 A53SS_CORE2_CTI_CTIINEN1 Register

1 A53SS_CORE2_CTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

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Table 14-15303. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0024h**

Figure 14-5076. A53SS_CORE2_CTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15305. A53SS_CORE2_CTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.961 A53SS_CORE2_CTI_CTIINEN2 Register

1 A53SS_CORE2_CTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

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Table 14-15306. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0028h**

Figure 14-5077. A53SS_CORE2_CTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN2_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN2_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN2_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN2_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15308. A53SS_CORE2_CTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.962 A53SS_CORE2_CTI_CTIINEN3 Register

1 A53SS_CORE2_CTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-15309. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 002Ch**

Figure 14-5078. A53SS_CORE2_CTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN3_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN3_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN3_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN3_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15311. A53SS_CORE2_CTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.963 A53SS_CORE2_CTI_CTIINEN4 Register

1 A53SS_CORE2_CTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

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Table 14-15312. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0030h**

Figure 14-5079. A53SS_CORE2_CTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15314. A53SS_CORE2_CTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.964 A53SS_CORE2_CTI_CTIINEN5 Register

1 A53SS_CORE2_CTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-15315. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0034h**

Figure 14-5080. A53SS_CORE2_CTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15317. A53SS_CORE2_CTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.965 A53SS_CORE2_CTI_CTIINEN6 Register

1 A53SS_CORE2_CTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-15318. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0038h**

Figure 14-5081. A53SS_CORE2_CTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN6_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15320. A53SS_CORE2_CTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.966 A53SS_CORE2_CTI_CTIINEN7 Register

1 A53SS_CORE2_CTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-15321. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 003Ch**

Figure 14-5082. A53SS_CORE2_CTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-15323. A53SS_CORE2_CTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.967 A53SS_CORE2_CTI_CTIOUTEN0 Register

1 A53SS_CORE2_CTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-15324. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00A0h**

Figure 14-5083. A53SS_CORE2_CTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN0_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15326. A53SS_CORE2_CTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.968 A53SS_CORE2_CTI_CTIOUTEN1 Register

1 A53SS_CORE2_CTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

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Table 14-15327. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00A4h**

Figure 14-5084. A53SS_CORE2_CTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN1_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15329. A53SS_CORE2_CTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.969 A53SS_CORE2_CTI_CTIOUTEN2 Register

1 A53SS_CORE2_CTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

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Table 14-15330. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00A8h**

Figure 14-5085. A53SS_CORE2_CTI_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIOUTEN2_31_4</td><td colspan="4">OUTENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15332. A53SS_CORE2_CTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.970 A53SS_CORE2_CTI_CTIOUTEN3 Register

1 A53SS_CORE2_CTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

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Table 14-15333. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00ACh**

Figure 14-5086. A53SS_CORE2_CTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15335. A53SS_CORE2_CTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.971 A53SS_CORE2_CTI_CTIOUTEN4 Register

1 A53SS_CORE2_CTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

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Table 14-15336. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00B0h**

Figure 14-5087. A53SS_CORE2_CTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15338. A53SS_CORE2_CTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.972 A53SS_CORE2_CTI_CTIOUTEN5 Register

1 A53SS_CORE2_CTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

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Table 14-15339. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00B4h**

Figure 14-5088. A53SS_CORE2_CTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15341. A53SS_CORE2_CTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.973 A53SS_CORE2_CTI_CTIOUTEN6 Register

1 A53SS_CORE2_CTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

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Table 14-15342. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00B8h**

Figure 14-5089. A53SS_CORE2_CTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15344. A53SS_CORE2_CTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.974 A53SS_CORE2_CTI_CTIOUTEN7 Register

1 A53SS_CORE2_CTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

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Table 14-15345. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 00BCh**

Figure 14-5090. A53SS_CORE2_CTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-15347. A53SS_CORE2_CTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.975 A53SS_CORE2_CTI_CTITRIGINSTATUS Register

1 A53SS_CORE2_CTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-15348. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0130h**

Figure 14-5091. A53SS_CORE2_CTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TRINN							
R/W							
0h							

Table 14-15350. A53SS_CORE2_CTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.976 A53SS_CORE2_CTI_CTITRIGOUTSTATUS Register

1 A53SS_CORE2_CTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

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Table 14-15351. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0134h**

Figure 14-5092. A53SS_CORE2_CTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TROUTN							
R/W							
0h							

Table 14-15353. A53SS_CORE2_CTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.977 A53SS_CORE2_CTI_CTICHINSTATUS Register

1 A53SS_CORE2_CTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-15354. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0138h**

Figure 14-5093. A53SS_CORE2_CTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHINSTATUS_31_4				CHINN			
R/W				R/W			
0h				0h			

Table 14-15356. A53SS_CORE2_CTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.978 A53SS_CORE2_CTI_CTICHOUTSTATUS Register

1 A53SS_CORE2_CTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

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Table 14-15357. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 013Ch**

Figure 14-5094. A53SS_CORE2_CTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-15359. A53SS_CORE2_CTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.979 A53SS_CORE2_CTI_CTIGATE Register

1 A53SS_CORE2_CTI_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

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Table 14-15360. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0140h**

Figure 14-5095. A53SS_CORE2_CTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIGATE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIGATE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIGATE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIGATE_31_4				GATEX			
R/W				R/W			
0h				Fh			

Table 14-15362. A53SS_CORE2_CTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.980 A53SS_CORE2_CTI_ASICCTL Register

1 A53SS_CORE2_CTI_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

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Table 14-15363. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0144h**

Figure 14-5096. A53SS_CORE2_CTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-15365. A53SS_CORE2_CTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.981 A53SS_CORE2_CTI_CTIITCTRL Register

1 A53SS_CORE2_CTI_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

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Table 14-15366. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0F00h**

Figure 14-5097. A53SS_CORE2_CTI_CTIITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_CTIITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-15368. A53SS_CORE2_CTI_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.982 A53SS_CORE2_CTI_CTICLAIMSET Register

1 A53SS_CORE2_CTI_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-15369. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FA0h**

Figure 14-5098. A53SS_CORE2_CTI_CTICLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMSET_31_4				CLAIMX			
R/W				R/W			
0h				Fh			

Table 14-15371. A53SS_CORE2_CTI_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.983 A53SS_CORE2_CTI_CTICLAIMCLR Register

1 A53SS_CORE2_CTI_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

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Table 14-15372. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FA4h**

Figure 14-5099. A53SS_CORE2_CTI_CTICLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICLAIMCLR_31_4				CLAIMX			
R/W				R/W			
0h				0h			

Table 14-15374. A53SS_CORE2_CTI_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.984 A53SS_CORE2_CTI_CTIDEVAFF0 Register

1 A53SS_CORE2_CTI_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000002h]

CTI Device Affinity Register 0

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Table 14-15375. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FA8h**

Figure 14-5100. A53SS_CORE2_CTI_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000002h							
23	22	21	20	19	18	17	16
CTIDEVAFF0							
R/W							
80000002h							
15	14	13	12	11	10	9	8
CTIDEVAFF0							
R/W							
80000002h							
7	6	5	4	3	2	1	0
CTIDEVAFF0							
R/W							
80000002h							

Table 14-15377. A53SS_CORE2_CTI_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000002h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.985 A53SS_CORE2_CTI_CTIDEVAFF1 Register

1 A53SS_CORE2_CTI_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-15378. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FACh**

Figure 14-5101. A53SS_CORE2_CTI_CTIDEVAFF1 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
CTIDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
CTIDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
CTIDEVAFF1							
R/W							
0h							

Table 14-15380. A53SS_CORE2_CTI_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.986 A53SS_CORE2_CTI_CTILAR Register

1 A53SS_CORE2_CTI_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

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Table 14-15381. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FB0h**

Figure 14-5102. A53SS_CORE2_CTI_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-15383. A53SS_CORE2_CTI_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.987 A53SS_CORE2_CTI_CTILSR Register

1 A53SS_CORE2_CTI_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-15384. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FB4h**

Figure 14-5103. A53SS_CORE2_CTI_CTILSR Name Register

31	30	29	28	27	26	25	24
RES0_CTILSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTILSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTILSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTILSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-15386. A53SS_CORE2_CTI_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.988 A53SS_CORE2_CTI_CTIAUTHSTATUS Register

1 A53SS_CORE2_CTI_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-15387. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FB8h**

Figure 14-5104. A53SS_CORE2_CTI_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							

7	6	5	4	3	2	1	0
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-15389. A53SS_CORE2_CTI_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.989 A53SS_CORE2_CTI_CTIDEVARCH Register

1 A53SS_CORE2_CTI_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

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Table 14-15390. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FBCh**

Figure 14-5105. A53SS_CORE2_CTI_CTIDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
1A14h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
1A14h							

Table 14-15392. A53SS_CORE2_CTI_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.990 A53SS_CORE2_CTI_CTIDEVID2 Register

1 A53SS_CORE2_CTI_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

Return to Summary Table

Table 14-15393. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FC0h**

Figure 14-5106. A53SS_CORE2_CTI_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-15395. A53SS_CORE2_CTI_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.991 A53SS_CORE2_CTI_CTIDEVID1 Register

1 A53SS_CORE2_CTI_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

Return to Summary Table

Table 14-15396. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FC4h**

Figure 14-5107. A53SS_CORE2_CTI_CTIDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID1_31_0							
R/W							
0h							

Table 14-15398. A53SS_CORE2_CTI_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.992 A53SS_CORE2_CTI_CTIDEVID Register

1 A53SS_CORE2_CTI_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

Return to Summary Table

Table 14-15399. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FC8h**

Figure 14-5108. A53SS_CORE2_CTI_CTIDEVID Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID_31_26						INOUT	
R/W						R/W	
0h						1h	
23	22	21	20	19	18	17	16
RES0_CTIDEVID_23_22		NUMCHAN					
R/W		R/W					
0h		4h					
15	14	13	12	11	10	9	8
RES0_CTIDEVID_15_14		NUMTRIG					
R/W		R/W					
0h		8h					
7	6	5	4	3	2	1	0
RES0_CTIDEVID_7_5			EXTMUXNUM				
R/W			R/W				
0h			0h				

Table 14-15401. A53SS_CORE2_CTI_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-15401. A53SS_CORE2_CTI_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.993 A53SS_CORE2_CTI_CTIDEVTYPE Register

1 A53SS_CORE2_CTI_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-15402. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FCCh**

Figure 14-5109. A53SS_CORE2_CTI_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-15404. A53SS_CORE2_CTI_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.994 A53SS_CORE2_CTI_CTIPIDR4 Register

1 A53SS_CORE2_CTI_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-15405. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FD0h**

Figure 14-5110. A53SS_CORE2_CTI_CTIPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-15407. A53SS_CORE2_CTI_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.995 A53SS_CORE2_CTI_CTIPIDR5 Register

1 A53SS_CORE2_CTI_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

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Table 14-15408. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FD4h**

Figure 14-5111. A53SS_CORE2_CTI_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-15410. A53SS_CORE2_CTI_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.996 A53SS_CORE2_CTI_CTIPIDR6 Register

1 A53SS_CORE2_CTI_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

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Table 14-15411. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FD8h**

Figure 14-5112. A53SS_CORE2_CTI_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-15413. A53SS_CORE2_CTI_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.997 A53SS_CORE2_CTI_CTIPIDR7 Register

1 A53SS_CORE2_CTI_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

Return to Summary Table

Table 14-15414. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FDCh**

Figure 14-5113. A53SS_CORE2_CTI_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-15416. A53SS_CORE2_CTI_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.998 A53SS_CORE2_CTI_CTIPIDR0 Register

1 A53SS_CORE2_CTI_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

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Table 14-15417. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FE0h**

Figure 14-5114. A53SS_CORE2_CTI_CTIPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
A8h							

Table 14-15419. A53SS_CORE2_CTI_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.999 A53SS_CORE2_CTI_CTIPIDR1 Register

1 A53SS_CORE2_CTI_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

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Table 14-15420. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FE4h**

Figure 14-5115. A53SS_CORE2_CTI_CTIPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-15422. A53SS_CORE2_CTI_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.1000 A53SS_CORE2_CTI_CTIPIDR2 Register

1 A53SS_CORE2_CTI_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

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Table 14-15423. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FE8h**

Figure 14-5116. A53SS_CORE2_CTI_CTIPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-15425. A53SS_CORE2_CTI_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.1001 A53SS_CORE2_CTI_CTIPIDR3 Register

1 A53SS_CORE2_CTI_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

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Table 14-15426. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FECh**

Figure 14-5117. A53SS_CORE2_CTI_CTIPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-15428. A53SS_CORE2_CTI_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.1002 A53SS_CORE2_CTI_CTICIDR0 Register

1 A53SS_CORE2_CTI_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

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Table 14-15429. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FF0h**

Figure 14-5118. A53SS_CORE2_CTI_CTICIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-15431. A53SS_CORE2_CTI_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.1003 A53SS_CORE2_CTI_CTICIDR1 Register

1 A53SS_CORE2_CTI_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

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Table 14-15432. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FF4h**

Figure 14-5119. A53SS_CORE2_CTI_CTICIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-15434. A53SS_CORE2_CTI_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.1004 A53SS_CORE2_CTI_CTICIDR2 Register

1 A53SS_CORE2_CTI_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

Return to Summary Table

Table 14-15435. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FF8h**

Figure 14-5120. A53SS_CORE2_CTI_CTICIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-15437. A53SS_CORE2_CTI_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.1005 A53SS_CORE2_CTI_CTICIDR3 Register

1 A53SS_CORE2_CTI_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

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Table 14-15438. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3024 0FFCh**

Figure 14-5121. A53SS_CORE2_CTI_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-15440. A53SS_CORE2_CTI_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.1006 A53SS_CORE3_DBG_EDESR Register

1 A53SS_CORE3_DBG_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

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Table 14-15441. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0020h**

Figure 14-5122. A53SS_CORE3_DBG_EDESR Name Register

31	30	29	28	27	26	25	24
RES0_EDESR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDESR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDESR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDESR_31_3					SS	RC	OSUC
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-15443. A53SS_CORE3_DBG_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.1007 A53SS_CORE3_DBG_EDECR Register

1 A53SS_CORE3_DBG_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

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Table 14-15444. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0024h**

Figure 14-5123. A53SS_CORE3_DBG_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDECR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDECR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-15446. A53SS_CORE3_DBG_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.1008 A53SS_CORE3_DBG_EDWAR_31_0 Register

1 A53SS_CORE3_DBG_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

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Table 14-15447. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0030h**

Figure 14-5124. A53SS_CORE3_DBG_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-15449. A53SS_CORE3_DBG_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.1009 A53SS_CORE3_DBG_EDWAR_63_32 Register

1 A53SS_CORE3_DBG_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

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Table 14-15450. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0034h**

Figure 14-5125. A53SS_CORE3_DBG_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-15452. A53SS_CORE3_DBG_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.1010 A53SS_CORE3_DBG_DBGDTRRX_EL0 Register

1 A53SS_CORE3_DBG_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

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Table 14-15453. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0080h**

Figure 14-5126. A53SS_CORE3_DBG_DBGDTRRX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRRX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRRX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRRX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRRX_EL0							
R/W							
0h							

Table 14-15455. A53SS_CORE3_DBG_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.1011 A53SS_CORE3_DBG_EDITR Register

1 A53SS_CORE3_DBG_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-15456. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0084h**

Figure 14-5127. A53SS_CORE3_DBG_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-15458. A53SS_CORE3_DBG_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.1012 A53SS_CORE3_DBG_EDSCR Register

1 A53SS_CORE3_DBG_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

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Table 14-15459. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0088h**

Figure 14-5128. A53SS_CORE3_DBG_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-15461. A53SS_CORE3_DBG_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-15461. A53SS_CORE3_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-15461. A53SS_CORE3_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-15461. A53SS_CORE3_DBG_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.1013 A53SS_CORE3_DBG_DBGDTRTX_EL0 Register

1 A53SS_CORE3_DBG_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-15462. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 008Ch**

Figure 14-5129. A53SS_CORE3_DBG_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-15464. A53SS_CORE3_DBG_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.1014 A53SS_CORE3_DBG_EDRCR Register

1 A53SS_CORE3_DBG_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-15465. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0090h**

Figure 14-5130. A53SS_CORE3_DBG_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDRCR_31_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDRCR_31_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-15467. A53SS_CORE3_DBG_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-15467. A53SS_CORE3_DBG_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1015 A53SS_CORE3_DBG_EDACR Register

1 A53SS_CORE3_DBG_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-15468. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0094h**

Figure 14-5131. A53SS_CORE3_DBG_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-15470. A53SS_CORE3_DBG_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1016 A53SS_CORE3_DBG_EDECCR Register

1 A53SS_CORE3_DBG_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-15471. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0098h**

Figure 14-5132. A53SS_CORE3_DBG_EDECCR Name Register

31	30	29	28	27	26	25	24
RES0_EDECCR_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDECCR_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDECCR_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NSE				SE			
R/W				R/W			
0h				0h			

Table 14-15473. A53SS_CORE3_DBG_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-15473. A53SS_CORE3_DBG_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.1017 A53SS_CORE3_DBG_EDPCSR_31_0 Register

1 A53SS_CORE3_DBG_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-15474. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 00A0h**

Figure 14-5133. A53SS_CORE3_DBG_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EDPCSR_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EDPCSR_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDPCSR_31_0							
R/W							
0h							

Table 14-15476. A53SS_CORE3_DBG_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31:0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.1018 A53SS_CORE3_DBG_EDCIDSR Register

1 A53SS_CORE3_DBG_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-15477. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 00A4h**

Figure 14-5134. A53SS_CORE3_DBG_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXTIDR							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXTIDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXTIDR							
R/W							
0h							

Table 14-15479. A53SS_CORE3_DBG_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.1019 A53SS_CORE3_DBG_EDVIDSR Register

1 A53SS_CORE3_DBG_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-15480. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 00A8h**

Figure 14-5135. A53SS_CORE3_DBG_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-15482. A53SS_CORE3_DBG_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63:32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63:32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.1020 A53SS_CORE3_DBG_EDPCSR_63_32 Register

1 A53SS_CORE3_DBG_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-15483. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 00ACh**

Figure 14-5136. A53SS_CORE3_DBG_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EDPCSR_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EDPCSR_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDPCSR_63_32							
R/W							
0h							

Table 14-15485. A53SS_CORE3_DBG_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63:32] of the sampled PC.

14.3.1.1.2.1021 A53SS_CORE3_DBG_OSLAR_EL1 Register

1 A53SS_CORE3_DBG_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-15486. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0300h**

Figure 14-5137. A53SS_CORE3_DBG_OSLAR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_OSLAR_EL1_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_OSLAR_EL1_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_OSLAR_EL1_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_OSLAR_EL1_31_1							OSLK
R/W							R/W
0h							0h

Table 14-15488. A53SS_CORE3_DBG_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.1022 A53SS_CORE3_DBG_EDPRCR Register

1 A53SS_CORE3_DBG_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-15489. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0310h**

Figure 14-5138. A53SS_CORE3_DBG_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-15491. A53SS_CORE3_DBG_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-15491. A53SS_CORE3_DBG_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.1023 A53SS_CORE3_DBG_EDPRSR Register

1 A53SS_CORE3_DBG_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-15492. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0314h**

Figure 14-5139. A53SS_CORE3_DBG_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRSR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-15494. A53SS_CORE3_DBG_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-15494. A53SS_CORE3_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-15494. A53SS_CORE3_DBG_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.1024 A53SS_CORE3_DBG_DBGBVR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15495. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0400h**

Figure 14-5140. A53SS_CORE3_DBG_DBGBVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_31_0							
R/W							
0h							

Table 14-15497. A53SS_CORE3_DBG_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1025 A53SS_CORE3_DBG_DBGBVR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15498. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0404h**

Figure 14-5141. A53SS_CORE3_DBG_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-15500. A53SS_CORE3_DBG_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1026 A53SS_CORE3_DBG_DBGBCR0_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-15501. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0408h**

Figure 14-5142. A53SS_CORE3_DBG_DBGBCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR0_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR0_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR0_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15503. A53SS_CORE3_DBG_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15503. A53SS_CORE3_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15503. A53SS_CORE3_DBG_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1027 A53SS_CORE3_DBG_DBGBVR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15504. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0410h**

Figure 14-5143. A53SS_CORE3_DBG_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR1_EL1_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR1_EL1_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-15506. A53SS_CORE3_DBG_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1028 A53SS_CORE3_DBG_DBGBVR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15507. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0414h**

Figure 14-5144. A53SS_CORE3_DBG_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-15509. A53SS_CORE3_DBG_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1029 A53SS_CORE3_DBG_DBGBCR1_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-15510. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0418h**

Figure 14-5145. A53SS_CORE3_DBG_DBGBCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR1_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR1_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR1_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15512. A53SS_CORE3_DBG_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15512. A53SS_CORE3_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15512. A53SS_CORE3_DBG_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1030 A53SS_CORE3_DBG_DBGBVR2_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15513. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0420h**

Figure 14-5146. A53SS_CORE3_DBG_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-15515. A53SS_CORE3_DBG_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1031 A53SS_CORE3_DBG_DBGBVR2_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15516. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0424h**

Figure 14-5147. A53SS_CORE3_DBG_DBGBVR2_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15518. A53SS_CORE3_DBG_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1032 A53SS_CORE3_DBG_DBGBCR2_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-15519. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0428h**

Figure 14-5148. A53SS_CORE3_DBG_DBGBCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR2_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR2_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR2_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15521. A53SS_CORE3_DBG_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15521. A53SS_CORE3_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15521. A53SS_CORE3_DBG_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1033 A53SS_CORE3_DBG_DBGBVR3_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15522. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0430h**

Figure 14-5149. A53SS_CORE3_DBG_DBGBVR3_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15524. A53SS_CORE3_DBG_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1034 A53SS_CORE3_DBG_DBGBVR3_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15525. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0434h**

Figure 14-5150. A53SS_CORE3_DBG_DBGBVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_63_32							
R/W							
0h							

Table 14-15527. A53SS_CORE3_DBG_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1035 A53SS_CORE3_DBG_DBGBCR3_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-15528. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0438h**

Figure 14-5151. A53SS_CORE3_DBG_DBGBCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR3_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR3_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR3_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15530. A53SS_CORE3_DBG_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15530. A53SS_CORE3_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15530. A53SS_CORE3_DBG_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1036 A53SS_CORE3_DBG_DBGBVR4_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15531. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0440h**

Figure 14-5152. A53SS_CORE3_DBG_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBGBVR4_EL1_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBGBVR4_EL1_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-15533. A53SS_CORE3_DBG_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1037 A53SS_CORE3_DBG_DBGBVR4_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15534. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0444h**

Figure 14-5153. A53SS_CORE3_DBG_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-15536. A53SS_CORE3_DBG_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1038 A53SS_CORE3_DBG_DBGBCR4_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

Debug Breakpoint Control Register 4

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Table 14-15537. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0448h**

Figure 14-5154. A53SS_CORE3_DBG_DBGBCR4_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR4_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR4_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR4_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-15539. A53SS_CORE3_DBG_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15539. A53SS_CORE3_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15539. A53SS_CORE3_DBG_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1039 A53SS_CORE3_DBG_DBGBVR5_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15540. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0450h**

Figure 14-5155. A53SS_CORE3_DBG_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-15542. A53SS_CORE3_DBG_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1040 A53SS_CORE3_DBG_DBGBVR5_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-15543. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0454h**

Figure 14-5156. A53SS_CORE3_DBG_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-15545. A53SS_CORE3_DBG_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.1041 A53SS_CORE3_DBG_DBGBCR5_EL1 Register

1 A53SS_CORE3_DBG_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

Debug Breakpoint Control Register 5

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Table 14-15546. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0458h**

Figure 14-5157. A53SS_CORE3_DBG_DBGBCR5_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR5_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR5_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR5_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15548. A53SS_CORE3_DBG_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-15548. A53SS_CORE3_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31:0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31:0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-15548. A53SS_CORE3_DBG_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.1042 A53SS_CORE3_DBG_DBGWVR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

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Table 14-15549. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0800h**

Figure 14-5158. A53SS_CORE3_DBG_DBGWVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR0_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-15551. A53SS_CORE3_DBG_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1043 A53SS_CORE3_DBG_DBGWVR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

Return to Summary Table

Table 14-15552. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0804h**

Figure 14-5159. A53SS_CORE3_DBG_DBGWVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-15554. A53SS_CORE3_DBG_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.1044 A53SS_CORE3_DBG_DBGWCR0_EL1 Register

1 A53SS_CORE3_DBG_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

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Table 14-15555. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0808h**

Figure 14-5160. A53SS_CORE3_DBG_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15557. A53SS_CORE3_DBG_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-15557. A53SS_CORE3_DBG_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.1045 A53SS_CORE3_DBG_DBGWVR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

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Table 14-15558. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0810h**

Figure 14-5161. A53SS_CORE3_DBG_DBGWVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR1_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-15560. A53SS_CORE3_DBG_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1046 A53SS_CORE3_DBG_DBGWVR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

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Table 14-15561. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0814h**

Figure 14-5162. A53SS_CORE3_DBG_DBGWVR1_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15563. A53SS_CORE3_DBG_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.1047 A53SS_CORE3_DBG_DBGWCR1_EL1 Register

1 A53SS_CORE3_DBG_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

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Table 14-15564. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3031 0818h**

Figure 14-5163. A53SS_CORE3_DBG_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15566. A53SS_CORE3_DBG_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-15566. A53SS_CORE3_DBG_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.1048 A53SS_CORE3_DBG_DBGWVR2_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

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Table 14-15567. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0820h**

Figure 14-5164. A53SS_CORE3_DBG_DBGWVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR2_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-15569. A53SS_CORE3_DBG_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1049 A53SS_CORE3_DBG_DBGWVR2_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

Return to Summary Table

Table 14-15570. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0824h**

Figure 14-5165. A53SS_CORE3_DBG_DBGWVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-15572. A53SS_CORE3_DBG_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.1050 A53SS_CORE3_DBG_DBGWCR2_EL1 Register

1 A53SS_CORE3_DBG_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

Return to Summary Table

Table 14-15573. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0828h**

Figure 14-5166. A53SS_CORE3_DBG_DBGWCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR2_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR2_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15575. A53SS_CORE3_DBG_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-15575. A53SS_CORE3_DBG_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.1051 A53SS_CORE3_DBG_DBGWVR3_EL1_31_0 Register

1 A53SS_CORE3_DBG_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

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Table 14-15576. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0830h**

Figure 14-5167. A53SS_CORE3_DBG_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-15578. A53SS_CORE3_DBG_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1052 A53SS_CORE3_DBG_DBGWVR3_EL1_63_32 Register

1 A53SS_CORE3_DBG_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

Return to Summary Table

Table 14-15579. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0834h**

Figure 14-5168. A53SS_CORE3_DBG_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-15581. A53SS_CORE3_DBG_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.1053 A53SS_CORE3_DBG_DBGWCR3_EL1 Register

1 A53SS_CORE3_DBG_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

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Table 14-15582. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0838h**

Figure 14-5169. A53SS_CORE3_DBG_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-15584. A53SS_CORE3_DBG_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-15584. A53SS_CORE3_DBG_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.1054 A53SS_CORE3_DBG_MIDR_EL1 Register

1 A53SS_CORE3_DBG_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-15585. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3031 0D00h**

Figure 14-5170. A53SS_CORE3_DBG_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-15587. A53SS_CORE3_DBG_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.1055 A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

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Table 14-15588. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D20h**

Figure 14-5171. A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
EL3				EL2			
R/W				R/W			
2h				2h			
7	6	5	4	3	2	1	0
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-15590. A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-15590. A53SS_CORE3_DBG_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.1056 A53SS_CORE3_DBG_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

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Table 14-15591. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D24h**

Figure 14-5172. A53SS_CORE3_DBG_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-15593. A53SS_CORE3_DBG_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1057 A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

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Table 14-15594. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D28h**

Figure 14-5173. A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-15596. A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-15596. A53SS_CORE3_DBG_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.1058 A53SS_CORE3_DBG_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

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Table 14-15597. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D2Ch**

Figure 14-5174. A53SS_CORE3_DBG_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-15599. A53SS_CORE3_DBG_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1059 A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-15600. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D30h**

Figure 14-5175. A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-15602. A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-15602. A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1060 A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-15603. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D34h**

Figure 14-5176. A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-15605. A53SS_CORE3_DBG_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1061 A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

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Table 14-15606. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D38h**

Figure 14-5177. A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-15608. A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-15608. A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.1062 A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

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Table 14-15609. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D3Ch**

Figure 14-5178. A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-15611. A53SS_CORE3_DBG_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1063 A53SS_CORE3_DBG_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

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Table 14-15612. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D40h**

Figure 14-5179. A53SS_CORE3_DBG_ID_AA64PFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-15614. A53SS_CORE3_DBG_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1064 A53SS_CORE3_DBG_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

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Table 14-15615. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D44h**

Figure 14-5180. A53SS_CORE3_DBG_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-15617. A53SS_CORE3_DBG_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1065 A53SS_CORE3_DBG_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

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Table 14-15618. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D48h**

Figure 14-5181. A53SS_CORE3_DBG_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-15620. A53SS_CORE3_DBG_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1066 A53SS_CORE3_DBG_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

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Table 14-15621. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D4Ch**

Figure 14-5182. A53SS_CORE3_DBG_ID_AA64DFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-15623. A53SS_CORE3_DBG_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1067 A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

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Table 14-15624. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D50h**

Figure 14-5183. A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-15626. A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1068 A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

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Table 14-15627. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D54h**

Figure 14-5184. A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-15629. A53SS_CORE3_DBG_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1069 A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-15630. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D58h**

Figure 14-5185. A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-15632. A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1070 A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

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Table 14-15633. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0D5Ch**

Figure 14-5186. A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-15635. A53SS_CORE3_DBG_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1071 A53SS_CORE3_DBG_EDITCTRL Register

1 A53SS_CORE3_DBG_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

Return to Summary Table

Table 14-15636. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0F00h**

Figure 14-5187. A53SS_CORE3_DBG_EDITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_EDITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15638. A53SS_CORE3_DBG_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.1072 A53SS_CORE3_DBG_DBGCLAIMSET_EL1 Register

1 A53SS_CORE3_DBG_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-15639. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FA0h**

Figure 14-5188. A53SS_CORE3_DBG_DBGCLAIMSET_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
FFh							

Table 14-15641. A53SS_CORE3_DBG_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.1073 A53SS_CORE3_DBG_DBGCLAIMCLR_EL1 Register

1 A53SS_CORE3_DBG_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-15642. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FA4h**

Figure 14-5189. A53SS_CORE3_DBG_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
0h							

Table 14-15644. A53SS_CORE3_DBG_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.1074 A53SS_CORE3_DBG_EDDEVAFF0 Register

1 A53SS_CORE3_DBG_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000003h]

External Debug Device Affinity Register 0

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Table 14-15645. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FA8h**

Figure 14-5190. A53SS_CORE3_DBG_EDDEVAFF0 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF0							
R/W							
80000003h							
23	22	21	20	19	18	17	16
EDDEVAFF0							
R/W							
80000003h							
15	14	13	12	11	10	9	8
EDDEVAFF0							
R/W							
80000003h							
7	6	5	4	3	2	1	0
EDDEVAFF0							
R/W							
80000003h							

Table 14-15647. A53SS_CORE3_DBG_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000003h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1075 A53SS_CORE3_DBG_EDDEVAFF1 Register

1 A53SS_CORE3_DBG_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

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Table 14-15648. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FACh**

Figure 14-5191. A53SS_CORE3_DBG_EDDEVAFF1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EDDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15650. A53SS_CORE3_DBG_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1076 A53SS_CORE3_DBG_EDLAR Register

1 A53SS_CORE3_DBG_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

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Table 14-15651. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FB0h**

Figure 14-5192. A53SS_CORE3_DBG_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-15653. A53SS_CORE3_DBG_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.1077 A53SS_CORE3_DBG_EDLSR Register

1 A53SS_CORE3_DBG_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

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Table 14-15654. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FB4h**

Figure 14-5193. A53SS_CORE3_DBG_EDLSR Name Register

31	30	29	28	27	26	25	24
RES0_EDLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-15656. A53SS_CORE3_DBG_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.1078 A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1 Register

1 A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

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Table 14-15657. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FB8h**

Figure 14-5194. A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		2h		2h		2h	

Table 14-15659. A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-15659. A53SS_CORE3_DBG_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.1079 A53SS_CORE3_DBG_EDDEVARCH Register

1 A53SS_CORE3_DBG_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

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Table 14-15660. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FBCh**

Figure 14-5195. A53SS_CORE3_DBG_EDDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
</table>

Table 14-15662. A53SS_CORE3_DBG_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.1080 A53SS_CORE3_DBG_EDDEVID2 Register

1 A53SS_CORE3_DBG_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

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Table 14-15663. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FC0h**

Figure 14-5196. A53SS_CORE3_DBG_EDDEVID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDDEVID2_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDDEVID2_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDDEVID2_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_EDDEVID2_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15665. A53SS_CORE3_DBG_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1081 A53SS_CORE3_DBG_EDDEVID1 Register

1 A53SS_CORE3_DBG_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

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Table 14-15666. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FC4h**

Figure 14-5197. A53SS_CORE3_DBG_EDDEVID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDDEVID1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDDEVID1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDDEVID1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RES0_EDDEVID1_31_4</td><td colspan="4">PCSROFFSET</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-15668. A53SS_CORE3_DBG_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.1082 A53SS_CORE3_DBG_EDDEVID Register

1 A53SS_CORE3_DBG_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

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Table 14-15669. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FC8h**

Figure 14-5198. A53SS_CORE3_DBG_EDDEVID Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID_31_28				AUXREGS			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RES0_EDDEVID_23_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID_23_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID_23_4				PCSAMPLE			
R/W				R/W			
0h				3h			

Table 14-15671. A53SS_CORE3_DBG_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.1083 A53SS_CORE3_DBG_EDDEVTYPE Register

1 A53SS_CORE3_DBG_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

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Table 14-15672. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FCCh**

Figure 14-5199. A53SS_CORE3_DBG_EDDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				5h			

Table 14-15674. A53SS_CORE3_DBG_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.1084 A53SS_CORE3_DBG_EDPIDR4 Register

1 A53SS_CORE3_DBG_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

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Table 14-15675. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FD0h**

Figure 14-5200. A53SS_CORE3_DBG_EDPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-15677. A53SS_CORE3_DBG_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.1085 A53SS_CORE3_DBG_EDPIDR0 Register

1 A53SS_CORE3_DBG_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

Return to Summary Table

Table 14-15678. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FE0h**

Figure 14-5201. A53SS_CORE3_DBG_EDPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
3h							

Table 14-15680. A53SS_CORE3_DBG_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.1086 A53SS_CORE3_DBG_EDPIDR1 Register

1 A53SS_CORE3_DBG_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

Return to Summary Table

Table 14-15681. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FE4h**

Figure 14-5202. A53SS_CORE3_DBG_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-15683. A53SS_CORE3_DBG_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.1087 A53SS_CORE3_DBG_EDPIDR2 Register

1 A53SS_CORE3_DBG_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

Return to Summary Table

Table 14-15684. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FE8h**

Figure 14-5203. A53SS_CORE3_DBG_EDPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-15686. A53SS_CORE3_DBG_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.1088 A53SS_CORE3_DBG_EDPIDR3 Register

1 A53SS_CORE3_DBG_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

Return to Summary Table

Table 14-15687. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FECh**

Figure 14-5204. A53SS_CORE3_DBG_EDPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-15689. A53SS_CORE3_DBG_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.1089 A53SS_CORE3_DBG_EDCIDR0 Register

1 A53SS_CORE3_DBG_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

Return to Summary Table

Table 14-15690. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FF0h**

Figure 14-5205. A53SS_CORE3_DBG_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-15692. A53SS_CORE3_DBG_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.1090 A53SS_CORE3_DBG_EDCIDR1 Register

1 A53SS_CORE3_DBG_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

Return to Summary Table

Table 14-15693. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FF4h**

Figure 14-5206. A53SS_CORE3_DBG_EDCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-15695. A53SS_CORE3_DBG_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.1091 A53SS_CORE3_DBG_EDCIDR2 Register

1 A53SS_CORE3_DBG_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

Return to Summary Table

Table 14-15696. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FF8h**

Figure 14-5207. A53SS_CORE3_DBG_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-15698. A53SS_CORE3_DBG_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.1092 A53SS_CORE3_DBG_EDCIDR3 Register

1 A53SS_CORE3_DBG_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

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Table 14-15699. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3031 0FFCh**

Figure 14-5208. A53SS_CORE3_DBG_EDCIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
</table>

Table 14-15701. A53SS_CORE3_DBG_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.1093 A53SS_CORE3_PMU_PMEVCNTR0_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

Return to Summary Table

Table 14-15702. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0000h**

Figure 14-5209. A53SS_CORE3_PMU_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-15704. A53SS_CORE3_PMU_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1094 A53SS_CORE3_PMU_PMEVCNTR1_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

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Table 14-15705. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0008h**

Figure 14-5210. A53SS_CORE3_PMU_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-15707. A53SS_CORE3_PMU_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1095 A53SS_CORE3_PMU_PMEVCNTR2_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

Return to Summary Table

Table 14-15708. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0010h**

Figure 14-5211. A53SS_CORE3_PMU_PMEVCNTR2_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PMEVCNTR2_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PMEVCNTR2_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PMEVCNTR2_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PMEVCNTR2_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15710. A53SS_CORE3_PMU_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1096 A53SS_CORE3_PMU_PMEVCNTR3_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

Return to Summary Table

Table 14-15711. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0018h**

Figure 14-5212. A53SS_CORE3_PMU_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-15713. A53SS_CORE3_PMU_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1097 A53SS_CORE3_PMU_PMEVCNTR4_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

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Table 14-15714. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0020h**

Figure 14-5213. A53SS_CORE3_PMU_PMEVCNTR4_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PMEVCNTR4_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PMEVCNTR4_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PMEVCNTR4_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PMEVCNTR4_EL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15716. A53SS_CORE3_PMU_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1098 A53SS_CORE3_PMU_PMEVCNTR5_EL0 Register

1 A53SS_CORE3_PMU_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

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Table 14-15717. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0028h**

Figure 14-5214. A53SS_CORE3_PMU_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PMEVCNTR5_EL0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMEVCNTR5_EL0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-15719. A53SS_CORE3_PMU_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.1099 A53SS_CORE3_PMU_PMCCNTR_EL0_31_0 Register

1 A53SS_CORE3_PMU_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

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Table 14-15720. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 00F8h**

Figure 14-5215. A53SS_CORE3_PMU_PMCCNTR_EL0_31_0 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-15722. A53SS_CORE3_PMU_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.1100 A53SS_CORE3_PMU_PMCCNTR_EL0_63_32 Register

1 A53SS_CORE3_PMU_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

Return to Summary Table

Table 14-15723. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 00FCh**

Figure 14-5216. A53SS_CORE3_PMU_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-15725. A53SS_CORE3_PMU_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.1101 A53SS_CORE3_PMU_PMEVTYPER0_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

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Table 14-15726. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0400h**

Figure 14-5217. A53SS_CORE3_PMU_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-15728. A53SS_CORE3_PMU_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15728. A53SS_CORE3_PMU_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1102 A53SS_CORE3_PMU_PMEVTYPER1_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

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Table 14-15729. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0404h**

Figure 14-5218. A53SS_CORE3_PMU_PMEVTYPER1_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER1_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER1_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER1_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-15731. A53SS_CORE3_PMU_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15731. A53SS_CORE3_PMU_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1103 A53SS_CORE3_PMU_PMEVTYPER2_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

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Table 14-15732. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0408h**

Figure 14-5219. A53SS_CORE3_PMU_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-15734. A53SS_CORE3_PMU_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15734. A53SS_CORE3_PMU_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1104 A53SS_CORE3_PMU_PMEVTYPER3_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-15735. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 040Ch**

Figure 14-5220. A53SS_CORE3_PMU_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-15737. A53SS_CORE3_PMU_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15737. A53SS_CORE3_PMU_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1105 A53SS_CORE3_PMU_PMEVTYPER4_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

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Table 14-15738. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0410h**

Figure 14-5221. A53SS_CORE3_PMU_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-15740. A53SS_CORE3_PMU_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15740. A53SS_CORE3_PMU_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1106 A53SS_CORE3_PMU_PMEVTYPER5_EL0 Register

1 A53SS_CORE3_PMU_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

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Table 14-15741. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0414h**

Figure 14-5222. A53SS_CORE3_PMU_PMEVTYPER5_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER5_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER5_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER5_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-15743. A53SS_CORE3_PMU_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-15743. A53SS_CORE3_PMU_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.1107 A53SS_CORE3_PMU_PMCCFILTR_EL0 Register

1 A53SS_CORE3_PMU_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

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Table 14-15744. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 047Ch**

Figure 14-5223. A53SS_CORE3_PMU_PMCCFILTR_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMCCFILTR_EL0_25_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							

Table 14-15746. A53SS_CORE3_PMU_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-15746. A53SS_CORE3_PMU_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1108 A53SS_CORE3_PMU_PMCNTENSET_EL0 Register

1 A53SS_CORE3_PMU_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

Return to Summary Table

Table 14-15747. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0C00h**

Figure 14-5224. A53SS_CORE3_PMU_PMCNTENSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-15749. A53SS_CORE3_PMU_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.1109 A53SS_CORE3_PMU_PMCNTENCLR_EL0 Register

1 A53SS_CORE3_PMU_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

Return to Summary Table

Table 14-15750. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0C20h**

Figure 14-5225. A53SS_CORE3_PMU_PMCNTENCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-15752. A53SS_CORE3_PMU_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.1110 A53SS_CORE3_PMU_PMINTENSET_EL1 Register

1 A53SS_CORE3_PMU_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

Return to Summary Table

Table 14-15753. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0C40h**

Figure 14-5226. A53SS_CORE3_PMU_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-15755. A53SS_CORE3_PMU_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.1111 A53SS_CORE3_PMU_PMINTENCLR_EL1 Register

1 A53SS_CORE3_PMU_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

Return to Summary Table

Table 14-15756. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0C60h**

Figure 14-5227. A53SS_CORE3_PMU_PMINTENCLR_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>C</td><td colspan="7">P_X</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P_X</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15758. A53SS_CORE3_PMU_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.1112 A53SS_CORE3_PMU_PMOVSCLR_EL0 Register

1 A53SS_CORE3_PMU_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

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Table 14-15759. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0C80h**

Figure 14-5228. A53SS_CORE3_PMU_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-15761. A53SS_CORE3_PMU_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.1113 A53SS_CORE3_PMU_PMSWINC_EL0 Register

1 A53SS_CORE3_PMU_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

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Table 14-15762. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0CA0h**

Figure 14-5229. A53SS_CORE3_PMU_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-15764. A53SS_CORE3_PMU_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.1114 A53SS_CORE3_PMU_PMOVSSET_EL0 Register

1 A53SS_CORE3_PMU_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

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Table 14-15765. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0CC0h**

Figure 14-5230. A53SS_CORE3_PMU_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-15767. A53SS_CORE3_PMU_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.1115 A53SS_CORE3_PMU_PMCFGR Register

1 A53SS_CORE3_PMU_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-15768. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0E00h**

Figure 14-5231. A53SS_CORE3_PMU_PMCFGR Name Register

31	30	29	28	27	26	25	24
RES0_PMCFGR_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCFGR_31_20				UEN	WT	NA	EX
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CCD	CC	SIZE					
R/W	R/W	R/W					
1h	1h	3Fh					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N							
R/W							
6h							

Table 14-15770. A53SS_CORE3_PMU_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-15770. A53SS_CORE3_PMU_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.1116 A53SS_CORE3_PMU_PMCR_EL0 Register

1 A53SS_CORE3_PMU_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-15771. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0E04h**

Figure 14-5232. A53SS_CORE3_PMU_PMCR_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCR_EL0_31_11							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCR_EL0_31_11							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCR_EL0_31_11					RES0_PMCR_EL0_10_7		
R/W					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RES0_PMCR_EL0_10_7	LC	DP	X	D	C	P	E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-15773. A53SS_CORE3_PMU_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-15773. A53SS_CORE3_PMU_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.1117 A53SS_CORE3_PMU_PMCEID0_EL0 Register

1 A53SS_CORE3_PMU_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-15774. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0E20h**

Figure 14-5233. A53SS_CORE3_PMU_PMCEID0_EL0 Name Register

31	30	29	28	27	26	25	24
CE_31_0							
R/W							
67FFBFFFh							
23	22	21	20	19	18	17	16
CE_31_0							
R/W							
67FFBFFFh							
15	14	13	12	11	10	9	8
CE_31_0							
R/W							
67FFBFFFh							
7	6	5	4	3	2	1	0
CE_31_0							
R/W							
67FFBFFFh							

Table 14-15776. A53SS_CORE3_PMU_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.1118 A53SS_CORE3_PMU_PMCEID1_EL0 Register

1 A53SS_CORE3_PMU_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-15777. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0E24h**

Figure 14-5234. A53SS_CORE3_PMU_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-15779. A53SS_CORE3_PMU_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.1119 A53SS_CORE3_PMU_PMITCTRL Register

1 A53SS_CORE3_PMU_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-15780. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0F00h**

Figure 14-5235. A53SS_CORE3_PMU_PMITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_PMITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15782. A53SS_CORE3_PMU_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.1120 A53SS_CORE3_PMU_PMDEVAFF0 Register

1 A53SS_CORE3_PMU_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000003h]

Performance Monitors Device Affinity Register 0

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Table 14-15783. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FA8h**

Figure 14-5236. A53SS_CORE3_PMU_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000003h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000003h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000003h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000003h							

Table 14-15785. A53SS_CORE3_PMU_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000003h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1121 A53SS_CORE3_PMU_PMDEVAFF1 Register

1 A53SS_CORE3_PMU_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-15786. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FACh**

Figure 14-5237. A53SS_CORE3_PMU_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PMDEVAFF1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMDEVAFF1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMDEVAFF1							
R/W							
0h							

Table 14-15788. A53SS_CORE3_PMU_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1122 A53SS_CORE3_PMU_PMLAR Register

1 A53SS_CORE3_PMU_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

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Table 14-15789. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FB0h**

Figure 14-5238. A53SS_CORE3_PMU_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-15791. A53SS_CORE3_PMU_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.1123 A53SS_CORE3_PMU_PMLSR Register

1 A53SS_CORE3_PMU_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

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Table 14-15792. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FB4h**

Figure 14-5239. A53SS_CORE3_PMU_PMLSR Name Register

31	30	29	28	27	26	25	24
RES0_PMLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	1h	1h

Table 14-15794. A53SS_CORE3_PMU_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.1124 A53SS_CORE3_PMU_PMAUTHSTATUS Register

1 A53SS_CORE3_PMU_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-15795. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FB8h**

Figure 14-5240. A53SS_CORE3_PMU_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-15797. A53SS_CORE3_PMU_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1125 A53SS_CORE3_PMU_PMDEVARCH Register

1 A53SS_CORE3_PMU_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

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Table 14-15798. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FBCh**

Figure 14-5241. A53SS_CORE3_PMU_PMDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
2A16h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
2A16h							

Table 14-15800. A53SS_CORE3_PMU_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.1126 A53SS_CORE3_PMU_PMDEVTYPE Register

1 A53SS_CORE3_PMU_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

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Table 14-15801. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FCCh**

Figure 14-5242. A53SS_CORE3_PMU_PMDEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB</td><td colspan="4">MAJOR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">6h</td></tr>
</table>

Table 14-15803. A53SS_CORE3_PMU_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.1127 A53SS_CORE3_PMU_PMPIDR4 Register

1 A53SS_CORE3_PMU_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-15804. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FD0h**

Figure 14-5243. A53SS_CORE3_PMU_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-15806. A53SS_CORE3_PMU_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.1128 A53SS_CORE3_PMU_PMPIDR5 Register

1 A53SS_CORE3_PMU_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

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Table 14-15807. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FD4h**

Figure 14-5244. A53SS_CORE3_PMU_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-15809. A53SS_CORE3_PMU_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1129 A53SS_CORE3_PMU_PMPIDR6 Register

1 A53SS_CORE3_PMU_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

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Table 14-15810. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FD8h**

Figure 14-5245. A53SS_CORE3_PMU_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-15812. A53SS_CORE3_PMU_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1130 A53SS_CORE3_PMU_PMPIDR7 Register

1 A53SS_CORE3_PMU_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

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Table 14-15813. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FDCh**

Figure 14-5246. A53SS_CORE3_PMU_PMPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR7_31_0							
R/W							
0h							

Table 14-15815. A53SS_CORE3_PMU_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1131 A53SS_CORE3_PMU_PMPIDR0 Register

1 A53SS_CORE3_PMU_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

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Table 14-15816. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FE0h**

Figure 14-5247. A53SS_CORE3_PMU_PMPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
D3h							

Table 14-15818. A53SS_CORE3_PMU_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.1132 A53SS_CORE3_PMU_PMPIDR1 Register

1 A53SS_CORE3_PMU_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-15819. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FE4h**

Figure 14-5248. A53SS_CORE3_PMU_PMPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-15821. A53SS_CORE3_PMU_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.1133 A53SS_CORE3_PMU_PMPIDR2 Register

1 A53SS_CORE3_PMU_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

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Table 14-15822. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FE8h**

Figure 14-5249. A53SS_CORE3_PMU_PMPIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">3h</td></tr>
</table>

Table 14-15824. A53SS_CORE3_PMU_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.1134 A53SS_CORE3_PMU_PMPIDR3 Register

1 A53SS_CORE3_PMU_PMPIDR3 Register (Offset = FECh) [reset = 0h]

Performance Monitors Peripheral Identification Register 3

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Table 14-15825. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FECh**

Figure 14-5250. A53SS_CORE3_PMU_PMPIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15827. A53SS_CORE3_PMU_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.1135 A53SS_CORE3_PMU_PMCIDR0 Register

1 A53SS_CORE3_PMU_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

Return to Summary Table

Table 14-15828. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FF0h**

Figure 14-5251. A53SS_CORE3_PMU_PMCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-15830. A53SS_CORE3_PMU_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.1136 A53SS_CORE3_PMU_PMCIDR1 Register

1 A53SS_CORE3_PMU_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

Return to Summary Table

Table 14-15831. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FF4h**

Figure 14-5252. A53SS_CORE3_PMU_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-15833. A53SS_CORE3_PMU_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.1137 A53SS_CORE3_PMU_PMCIDR2 Register

1 A53SS_CORE3_PMU_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-15834. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FF8h**

Figure 14-5253. A53SS_CORE3_PMU_PMCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-15836. A53SS_CORE3_PMU_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.1138 A53SS_CORE3_PMU_PMCIDR3 Register

1 A53SS_CORE3_PMU_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

Return to Summary Table

Table 14-15837. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3032 0FFCh**

Figure 14-5254. A53SS_CORE3_PMU_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-15839. A53SS_CORE3_PMU_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.1139 A53SS_CORE3_ETM_TRCPRGCTLR Register

1 A53SS_CORE3_ETM_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

Return to Summary Table

Table 14-15840. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0004h**

Figure 14-5255. A53SS_CORE3_ETM_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-15842. A53SS_CORE3_ETM_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.1140 A53SS_CORE3_ETM_TRCSTATR Register

1 A53SS_CORE3_ETM_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

Return to Summary Table

Table 14-15843. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 000Ch**

Figure 14-5256. A53SS_CORE3_ETM_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-15845. A53SS_CORE3_ETM_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.1141 A53SS_CORE3_ETM_TRCCONFIGR Register

1 A53SS_CORE3_ETM_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

Return to Summary Table

Table 14-15846. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0010h**

Figure 14-5257. A53SS_CORE3_ETM_TRCCONFIGR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCONFIGR_31_18							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCONFIGR_31_18						DV	DA
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RES0_TRCCONFIGR_15_15	QE		RS	TS	COND		
R/W	R/W		R/W	R/W	R/W		
0h	0h		0h	0h	0h		
7	6	5	4	3	2	1	0
VMID	CID	RES0_TRCCONFIGR_5_5	CCI	BB	INSTP0		RES1_TRCCONFIGR_0_0
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		1h

Table 14-15848. A53SS_CORE3_ETM_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-15848. A53SS_CORE3_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-15848. A53SS_CORE3_ETM_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.1142 A53SS_CORE3_ETM_TRCAUXCTLR Register

1 A53SS_CORE3_ETM_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

Return to Summary Table

Table 14-15849. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0018h**

Figure 14-5258. A53SS_CORE3_ETM_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-15851. A53SS_CORE3_ETM_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.1143 A53SS_CORE3_ETM_TRCEVENTCTL0R Register

1 A53SS_CORE3_ETM_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

Return to Summary Table

Table 14-15852. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0020h**

Figure 14-5259. A53SS_CORE3_ETM_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	14	13	12	11	10	9	8
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-15854. A53SS_CORE3_ETM_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.1144 A53SS_CORE3_ETM_TRCEVENTCTL1R Register

1 A53SS_CORE3_ETM_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

Return to Summary Table

Table 14-15855. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0024h**

Figure 14-5260. A53SS_CORE3_ETM_TRCEVENTCTL1R Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEVENTCTL1R_31_13			LPOVERRIDE	ATB	RESERVED_TRCEVENTCTL1R_10_4		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEVENTCTL1R_10_4				EN			
R/W				R/W			
0h				0h			

Table 14-15857. A53SS_CORE3_ETM_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.1145 A53SS_CORE3_ETM_TRCSTALLCTLR Register

1 A53SS_CORE3_ETM_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

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Table 14-15858. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 002Ch**

Figure 14-5261. A53SS_CORE3_ETM_TRCSTALLCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCSTALLCTLR_31_9							ISTALL
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCSTALLCTLR_7_4				LEVEL		RESERVED_TRCSTALLCTLR_1_0	
R/W				R/W		R/W	
0h				0h		0h	

Table 14-15860. A53SS_CORE3_ETM_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.1146 A53SS_CORE3_ETM_TRCTSCTLR Register

1 A53SS_CORE3_ETM_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

Return to Summary Table

Table 14-15861. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0030h**

Figure 14-5262. A53SS_CORE3_ETM_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-15863. A53SS_CORE3_ETM_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.1147 A53SS_CORE3_ETM_TRCSYNCPR Register

1 A53SS_CORE3_ETM_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

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Table 14-15864. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0034h**

Figure 14-5263. A53SS_CORE3_ETM_TRCSYNCPR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSYNCPR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSYNCPR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSYNCPR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSYNCPR_31_5			PERIOD				
R/W			R/W				
0h			0h				

Table 14-15866. A53SS_CORE3_ETM_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.1148 A53SS_CORE3_ETM_TRCCCCTLR Register

1 A53SS_CORE3_ETM_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

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Table 14-15867. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0038h**

Figure 14-5264. A53SS_CORE3_ETM_TRCCCCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCCCTLR_31_12							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCCCTLR_31_12							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCCCTLR_31_12				THRESHOLD			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-15869. A53SS_CORE3_ETM_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.1149 A53SS_CORE3_ETM_TRCBBCTLR Register

1 A53SS_CORE3_ETM_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

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Table 14-15870. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 003Ch**

Figure 14-5265. A53SS_CORE3_ETM_TRCBBCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCBBCTLR_31_9							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCBBCTLR_31_9							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCBBCTLR_31_9							MODE
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RANGE							
R/W							
0h							

Table 14-15872. A53SS_CORE3_ETM_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.1150 A53SS_CORE3_ETM_TRCTRACEIDR Register

1 A53SS_CORE3_ETM_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-15873. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0040h**

Figure 14-5266. A53SS_CORE3_ETM_TRCTRACEIDR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCTRACEIDR_31_7	TRACEID						
R/W	R/W						
0h	0h						

Table 14-15875. A53SS_CORE3_ETM_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.1151 A53SS_CORE3_ETM_TRCVICTLR Register

1 A53SS_CORE3_ETM_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-15876. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0080h**

Figure 14-5267. A53SS_CORE3_ETM_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-15878. A53SS_CORE3_ETM_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-15878. A53SS_CORE3_ETM_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.1152 A53SS_CORE3_ETM_TRCVIIECTLR Register

1 A53SS_CORE3_ETM_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

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Table 14-15879. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0084h**

Figure 14-5268. A53SS_CORE3_ETM_TRCVIIECTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCVIIECTLR_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EXCLUDE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCVIIECTLR_15_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INCLUDE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15881. A53SS_CORE3_ETM_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.1153 A53SS_CORE3_ETM_TRCVISSCTLR Register

1 A53SS_CORE3_ETM_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

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Table 14-15882. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0088h**

Figure 14-5269. A53SS_CORE3_ETM_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	22	21	20	19	18	17	16
STOP							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 14-15884. A53SS_CORE3_ETM_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.1154 A53SS_CORE3_ETM_TRCSEQEVR0 Register

1 A53SS_CORE3_ETM_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

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Table 14-15885. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0100h**

Figure 14-5270. A53SS_CORE3_ETM_TRCSEQEVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-15887. A53SS_CORE3_ETM_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.1155 A53SS_CORE3_ETM_TRCSEQEVR1 Register

1 A53SS_CORE3_ETM_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

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Table 14-15888. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0104h**

Figure 14-5271. A53SS_CORE3_ETM_TRCSEQEVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-15890. A53SS_CORE3_ETM_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.1156 A53SS_CORE3_ETM_TRCSEQEVR2 Register

1 A53SS_CORE3_ETM_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

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Table 14-15891. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0108h**

Figure 14-5272. A53SS_CORE3_ETM_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-15893. A53SS_CORE3_ETM_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.1157 A53SS_CORE3_ETM_TRCSEQRSTEVR Register

1 A53SS_CORE3_ETM_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

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Table 14-15894. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0118h**

Figure 14-5273. A53SS_CORE3_ETM_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RST							
R/W							
0h							

Table 14-15896. A53SS_CORE3_ETM_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.1158 A53SS_CORE3_ETM_TRCSEQSTR Register

1 A53SS_CORE3_ETM_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

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Table 14-15897. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 011Ch**

Figure 14-5274. A53SS_CORE3_ETM_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-15899. A53SS_CORE3_ETM_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.1159 A53SS_CORE3_ETM_TRCEXTINSELR Register

1 A53SS_CORE3_ETM_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

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Table 14-15900. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0120h**

Figure 14-5275. A53SS_CORE3_ETM_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-15902. A53SS_CORE3_ETM_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.1160 A53SS_CORE3_ETM_TRCCNTRLDVR0 Register

1 A53SS_CORE3_ETM_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

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Table 14-15903. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0140h**

Figure 14-5276. A53SS_CORE3_ETM_TRCCNTRLDVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15905. A53SS_CORE3_ETM_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.1161 A53SS_CORE3_ETM_TRCCNTRLDVR1 Register

1 A53SS_CORE3_ETM_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

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Table 14-15906. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0144h**

Figure 14-5277. A53SS_CORE3_ETM_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15908. A53SS_CORE3_ETM_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.1162 A53SS_CORE3_ETM_TRCCNTCTLR0 Register

1 A53SS_CORE3_ETM_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

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Table 14-15909. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0150h**

Figure 14-5278. A53SS_CORE3_ETM_TRCCNTCTLR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR0_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTCTLR0_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RLDEVENT_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTEVENT_N							
R/W							
0h							

Table 14-15911. A53SS_CORE3_ETM_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.1163 A53SS_CORE3_ETM_TRCCNTCTLR1 Register

1 A53SS_CORE3_ETM_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

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Table 14-15912. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0154h**

Figure 14-5279. A53SS_CORE3_ETM_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RLDEVENT_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTEVENT_N							
R/W							
0h							

Table 14-15914. A53SS_CORE3_ETM_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.1164 A53SS_CORE3_ETM_TRCCNTVR0 Register

1 A53SS_CORE3_ETM_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

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Table 14-15915. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0160h**

Figure 14-5280. A53SS_CORE3_ETM_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15917. A53SS_CORE3_ETM_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.1165 A53SS_CORE3_ETM_TRCCNTVR1 Register

1 A53SS_CORE3_ETM_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

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Table 14-15918. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0164h**

Figure 14-5281. A53SS_CORE3_ETM_TRCCNTVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-15920. A53SS_CORE3_ETM_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.1166 A53SS_CORE3_ETM_TRCIDR8 Register

1 A53SS_CORE3_ETM_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

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Table 14-15921. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0180h**

Figure 14-5282. A53SS_CORE3_ETM_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							
23	22	21	20	19	18	17	16
MAXSPEC							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXSPEC							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXSPEC							
R/W							
0h							

Table 14-15923. A53SS_CORE3_ETM_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.1167 A53SS_CORE3_ETM_TRCIDR9 Register

1 A53SS_CORE3_ETM_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-15924. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0184h**

Figure 14-5283. A53SS_CORE3_ETM_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-15926. A53SS_CORE3_ETM_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.1168 A53SS_CORE3_ETM_TRCIDR10 Register

1 A53SS_CORE3_ETM_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-15927. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0188h**

Figure 14-5284. A53SS_CORE3_ETM_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-15929. A53SS_CORE3_ETM_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.1169 A53SS_CORE3_ETM_TRCIDR11 Register

1 A53SS_CORE3_ETM_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-15930. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 018Ch**

Figure 14-5285. A53SS_CORE3_ETM_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-15932. A53SS_CORE3_ETM_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.1170 A53SS_CORE3_ETM_TRCIDR12 Register

1 A53SS_CORE3_ETM_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-15933. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0190h**

Figure 14-5286. A53SS_CORE3_ETM_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-15935. A53SS_CORE3_ETM_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.1171 A53SS_CORE3_ETM_TRCIDR13 Register

1 A53SS_CORE3_ETM_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

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Table 14-15936. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0194h**

Figure 14-5287. A53SS_CORE3_ETM_TRCIDR13 Name Register

31	30	29	28	27	26	25	24
NUMCONDSPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDSPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDSPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDSPC							
R/W							
0h							

Table 14-15938. A53SS_CORE3_ETM_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.1172 A53SS_CORE3_ETM_TRCIMSPEC0 Register

1 A53SS_CORE3_ETM_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

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Table 14-15939. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01C0h**

Figure 14-5288. A53SS_CORE3_ETM_TRCIMSPEC0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EN				SUPPORT			
R/W				R/W			
0h				0h			

Table 14-15941. A53SS_CORE3_ETM_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.1173 A53SS_CORE3_ETM_TRCIDR0 Register

1 A53SS_CORE3_ETM_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-15942. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01E0h**

Figure 14-5289. A53SS_CORE3_ETM_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	22	21	20	19	18	17	16
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	6	5	4	3	2	1	0
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-15944. A53SS_CORE3_ETM_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-15944. A53SS_CORE3_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-15944. A53SS_CORE3_ETM_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.1174 A53SS_CORE3_ETM_TRCIDR1 Register

1 A53SS_CORE3_ETM_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

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Table 14-15945. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01E4h**

Figure 14-5290. A53SS_CORE3_ETM_TRCIDR1 Name Register

31	30	29	28	27	26	25	24
DESIGNER							
R/W							
41h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIDR1_23_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES1_TRCIDR1_15_12				TRCARCHMAJ			
R/W				R/W			
Fh				4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRCARCHMIN				REVISION			
R/W				R/W			
0h				4h			

Table 14-15947. A53SS_CORE3_ETM_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-15947. A53SS_CORE3_ETM_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.1175 A53SS_CORE3_ETM_TRCIDR2 Register

1 A53SS_CORE3_ETM_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

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Table 14-15948. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01E8h**

Figure 14-5291. A53SS_CORE3_ETM_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h
23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	
7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-15950. A53SS_CORE3_ETM_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-15950. A53SS_CORE3_ETM_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.1176 A53SS_CORE3_ETM_TRCIDR3 Register

1 A53SS_CORE3_ETM_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

Return to Summary Table

Table 14-15951. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01ECh**

Figure 14-5292. A53SS_CORE3_ETM_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	14	13	12	11	10	9	8
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	6	5	4	3	2	1	0
CCITMIN							
R/W							
4h							

Table 14-15953. A53SS_CORE3_ETM_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-15953. A53SS_CORE3_ETM_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.1177 A53SS_CORE3_ETM_TRCIDR4 Register

1 A53SS_CORE3_ETM_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

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Table 14-15954. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01F0h**

Figure 14-5293. A53SS_CORE3_ETM_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			
23	22	21	20	19	18	17	16
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			
15	14	13	12	11	10	9	8
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-15956. A53SS_CORE3_ETM_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-15956. A53SS_CORE3_ETM_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.1178 A53SS_CORE3_ETM_TRCIDR5 Register

1 A53SS_CORE3_ETM_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-15957. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 01F4h**

Figure 14-5294. A53SS_CORE3_ETM_TRCIDR5 Name Register

31	30	29	28	27	26	25	24
REDFUNCNTR	NUMCNTR			NUMSEQSTATE			RES0_TRCIDR5_24_24
R/W	R/W			R/W			R/W
0h	2h			4h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPOVERRIDE	ATBTRIG	TRACEIDSIZE					
R/W	R/W	R/W					
1h	1h	7h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCIDR5_15_12				NUMEXTINSEL			NUMEXTIN
R/W				R/W			R/W
0h				4h			1Eh
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMEXTIN							
R/W							
1Eh							

Table 14-15959. A53SS_CORE3_ETM_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-15959. A53SS_CORE3_ETM_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.1179 A53SS_CORE3_ETM_TRCRSCTLR2 Register

1 A53SS_CORE3_ETM_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

Resource Selection Control Registers 2

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Table 14-15960. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0208h**

Figure 14-5295. A53SS_CORE3_ETM_TRCRSCTLR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR2_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15962. A53SS_CORE3_ETM_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15962. A53SS_CORE3_ETM_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1180 A53SS_CORE3_ETM_TRCRSCTLR3 Register

1 A53SS_CORE3_ETM_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

Resource Selection Control Registers 3

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Table 14-15963. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 020Ch**

Figure 14-5296. A53SS_CORE3_ETM_TRCRSCTLR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR3_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15965. A53SS_CORE3_ETM_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15965. A53SS_CORE3_ETM_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1181 A53SS_CORE3_ETM_TRCRSCTLR4 Register

1 A53SS_CORE3_ETM_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

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Table 14-15966. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0210h**

Figure 14-5297. A53SS_CORE3_ETM_TRCRSCTLR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR4_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR4_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15968. A53SS_CORE3_ETM_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15968. A53SS_CORE3_ETM_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1182 A53SS_CORE3_ETM_TRCRSCTLR5 Register

1 A53SS_CORE3_ETM_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

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Table 14-15969. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0214h**

Figure 14-5298. A53SS_CORE3_ETM_TRCRSCTLR5 Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">RES0_TRCRSCTLR5_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="2">RES0_TRCRSCTLR5_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15971. A53SS_CORE3_ETM_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15971. A53SS_CORE3_ETM_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1183 A53SS_CORE3_ETM_TRCRSCTLR6 Register

1 A53SS_CORE3_ETM_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

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Table 14-15972. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0218h**

Figure 14-5299. A53SS_CORE3_ETM_TRCRSCTLR6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR6_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR6_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15974. A53SS_CORE3_ETM_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15974. A53SS_CORE3_ETM_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1184 A53SS_CORE3_ETM_TRCRSCTLR7 Register

1 A53SS_CORE3_ETM_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

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Table 14-15975. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 021Ch**

Figure 14-5300. A53SS_CORE3_ETM_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15977. A53SS_CORE3_ETM_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15977. A53SS_CORE3_ETM_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1185 A53SS_CORE3_ETM_TRCRSCTLR8 Register

1 A53SS_CORE3_ETM_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-15978. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0220h**

Figure 14-5301. A53SS_CORE3_ETM_TRCRSCTLR8 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR8_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR8_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15980. A53SS_CORE3_ETM_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15980. A53SS_CORE3_ETM_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1186 A53SS_CORE3_ETM_TRCRSCTLR9 Register

1 A53SS_CORE3_ETM_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-15981. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0224h**

Figure 14-5302. A53SS_CORE3_ETM_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15983. A53SS_CORE3_ETM_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15983. A53SS_CORE3_ETM_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1187 A53SS_CORE3_ETM_TRCRSCTLR10 Register

1 A53SS_CORE3_ETM_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-15984. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0228h**

Figure 14-5303. A53SS_CORE3_ETM_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15986. A53SS_CORE3_ETM_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15986. A53SS_CORE3_ETM_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1188 A53SS_CORE3_ETM_TRCRSCTLR11 Register

1 A53SS_CORE3_ETM_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-15987. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 022Ch**

Figure 14-5304. A53SS_CORE3_ETM_TRCRSCTLR11 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR11_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR11_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15989. A53SS_CORE3_ETM_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15989. A53SS_CORE3_ETM_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1189 A53SS_CORE3_ETM_TRCRSCTLR12 Register

1 A53SS_CORE3_ETM_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

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Table 14-15990. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0230h**

Figure 14-5305. A53SS_CORE3_ETM_TRCRSCTLR12 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR12_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR12_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15992. A53SS_CORE3_ETM_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15992. A53SS_CORE3_ETM_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1190 A53SS_CORE3_ETM_TRCRSCTLR13 Register

1 A53SS_CORE3_ETM_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

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Table 14-15993. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0234h**

Figure 14-5306. A53SS_CORE3_ETM_TRCRSCTLR13 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR13_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR13_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-15995. A53SS_CORE3_ETM_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15995. A53SS_CORE3_ETM_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1191 A53SS_CORE3_ETM_TRCRSCTLR14 Register

1 A53SS_CORE3_ETM_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

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Table 14-15996. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0238h**

Figure 14-5307. A53SS_CORE3_ETM_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-15998. A53SS_CORE3_ETM_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-15998. A53SS_CORE3_ETM_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1192 A53SS_CORE3_ETM_TRCRSCTLR15 Register

1 A53SS_CORE3_ETM_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

Resource Selection Control Registers 15

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Table 14-15999. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 023Ch**

Figure 14-5308. A53SS_CORE3_ETM_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-16001. A53SS_CORE3_ETM_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-16001. A53SS_CORE3_ETM_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.1193 A53SS_CORE3_ETM_TRCSSCCR0 Register

1 A53SS_CORE3_ETM_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-16002. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0280h**

Figure 14-5309. A53SS_CORE3_ETM_TRCSSCCR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSSCCR0_31_25							RST
R/W							R/W
0h							0h
23	22	21	20	19	18	17	16
ARC							
R/W							
0h							
15	14	13	12	11	10	9	8
SAC							
R/W							
0h							
7	6	5	4	3	2	1	0
SAC							
R/W							
0h							

Table 14-16004. A53SS_CORE3_ETM_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-16004. A53SS_CORE3_ETM_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.1194 A53SS_CORE3_ETM_TRCSSCSR0 Register

1 A53SS_CORE3_ETM_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-16005. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 02A0h**

Figure 14-5310. A53SS_CORE3_ETM_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-16007. A53SS_CORE3_ETM_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-16007. A53SS_CORE3_ETM_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.1195 A53SS_CORE3_ETM_TRCOSLAR Register

1 A53SS_CORE3_ETM_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-16008. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0300h**

Figure 14-5311. A53SS_CORE3_ETM_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-16010. A53SS_CORE3_ETM_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.1196 A53SS_CORE3_ETM_TRCOSLSR Register

1 A53SS_CORE3_ETM_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-16011. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0304h**

Figure 14-5312. A53SS_CORE3_ETM_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-16013. A53SS_CORE3_ETM_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1197 A53SS_CORE3_ETM_TRCPDCR Register

1 A53SS_CORE3_ETM_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-16014. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0310h**

Figure 14-5313. A53SS_CORE3_ETM_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-16016. A53SS_CORE3_ETM_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1198 A53SS_CORE3_ETM_TRCPDSR Register

1 A53SS_CORE3_ETM_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

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Table 14-16017. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0314h**

Figure 14-5314. A53SS_CORE3_ETM_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPDSR_31_6							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPDSR_31_6							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-16019. A53SS_CORE3_ETM_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-16019. A53SS_CORE3_ETM_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.1199 A53SS_CORE3_ETM_TRCACVR0_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

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Table 14-16020. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0400h**

Figure 14-5315. A53SS_CORE3_ETM_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16022. A53SS_CORE3_ETM_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1200 A53SS_CORE3_ETM_TRCACVR0_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

Return to Summary Table

Table 14-16023. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0404h**

Figure 14-5316. A53SS_CORE3_ETM_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16025. A53SS_CORE3_ETM_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1201 A53SS_CORE3_ETM_TRCACVR1_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-16026. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0408h**

Figure 14-5317. A53SS_CORE3_ETM_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16028. A53SS_CORE3_ETM_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1202 A53SS_CORE3_ETM_TRCACVR1_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-16029. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 040Ch**

Figure 14-5318. A53SS_CORE3_ETM_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16031. A53SS_CORE3_ETM_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1203 A53SS_CORE3_ETM_TRCACVR2_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-16032. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0410h**

Figure 14-5319. A53SS_CORE3_ETM_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16034. A53SS_CORE3_ETM_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1204 A53SS_CORE3_ETM_TRCACVR2_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-16035. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0414h**

Figure 14-5320. A53SS_CORE3_ETM_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16037. A53SS_CORE3_ETM_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1205 A53SS_CORE3_ETM_TRCACVR3_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-16038. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0418h**

Figure 14-5321. A53SS_CORE3_ETM_TRCACVR3_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16040. A53SS_CORE3_ETM_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1206 A53SS_CORE3_ETM_TRCACVR3_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

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Table 14-16041. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 041Ch**

Figure 14-5322. A53SS_CORE3_ETM_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16043. A53SS_CORE3_ETM_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1207 A53SS_CORE3_ETM_TRCACVR4_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

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Table 14-16044. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0420h**

Figure 14-5323. A53SS_CORE3_ETM_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16046. A53SS_CORE3_ETM_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1208 A53SS_CORE3_ETM_TRCACVR4_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

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Table 14-16047. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0424h**

Figure 14-5324. A53SS_CORE3_ETM_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16049. A53SS_CORE3_ETM_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1209 A53SS_CORE3_ETM_TRCACVR5_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

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Table 14-16050. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0428h**

Figure 14-5325. A53SS_CORE3_ETM_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDRESS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDRESS							
R/W							
0h							

Table 14-16052. A53SS_CORE3_ETM_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1210 A53SS_CORE3_ETM_TRCACVR5_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

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Table 14-16053. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 042Ch**

Figure 14-5326. A53SS_CORE3_ETM_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16055. A53SS_CORE3_ETM_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1211 A53SS_CORE3_ETM_TRCACVR6_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

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Table 14-16056. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0430h**

Figure 14-5327. A53SS_CORE3_ETM_TRCACVR6_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16058. A53SS_CORE3_ETM_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1212 A53SS_CORE3_ETM_TRCACVR6_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

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Table 14-16059. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0434h**

Figure 14-5328. A53SS_CORE3_ETM_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16061. A53SS_CORE3_ETM_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1213 A53SS_CORE3_ETM_TRCACVR7_31_0 Register

1 A53SS_CORE3_ETM_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

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Table 14-16062. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0438h**

Figure 14-5329. A53SS_CORE3_ETM_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16064. A53SS_CORE3_ETM_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1214 A53SS_CORE3_ETM_TRCACVR7_63_32 Register

1 A53SS_CORE3_ETM_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

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Table 14-16065. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 043Ch**

Figure 14-5330. A53SS_CORE3_ETM_TRCACVR7_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-16067. A53SS_CORE3_ETM_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63:32] bits.

14.3.1.1.2.1215 A53SS_CORE3_ETM_TRCACATR0 Register

1 A53SS_CORE3_ETM_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-16068. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0480h**

Figure 14-5331. A53SS_CORE3_ETM_TRCACATR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR0_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR0_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR0_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-16070. A53SS_CORE3_ETM_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16070. A53SS_CORE3_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16070. A53SS_CORE3_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16070. A53SS_CORE3_ETM_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1216 A53SS_CORE3_ETM_TRCACATR1 Register

1 A53SS_CORE3_ETM_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-16071. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0488h**

Figure 14-5332. A53SS_CORE3_ETM_TRCACATR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR1_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR1_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR1_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-16073. A53SS_CORE3_ETM_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16073. A53SS_CORE3_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16073. A53SS_CORE3_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16073. A53SS_CORE3_ETM_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1217 A53SS_CORE3_ETM_TRCACATR2 Register

1 A53SS_CORE3_ETM_TRCACATR2 Register (Offset = 490h) [reset = 0h]

Address Comparator Access Type Registers 2

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Table 14-16074. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0490h**

Figure 14-5333. A53SS_CORE3_ETM_TRCACATR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR2_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR2_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR2_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-16076. A53SS_CORE3_ETM_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16076. A53SS_CORE3_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16076. A53SS_CORE3_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16076. A53SS_CORE3_ETM_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1218 A53SS_CORE3_ETM_TRCACATR3 Register

1 A53SS_CORE3_ETM_TRCACATR3 Register (Offset = 498h) [reset = 0h]

Address Comparator Access Type Registers 3

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Table 14-16077. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0498h**

Figure 14-5334. A53SS_CORE3_ETM_TRCACATR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR3_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR3_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-16079. A53SS_CORE3_ETM_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16079. A53SS_CORE3_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16079. A53SS_CORE3_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16079. A53SS_CORE3_ETM_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1219 A53SS_CORE3_ETM_TRCACATR4 Register

1 A53SS_CORE3_ETM_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-16080. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 04A0h**

Figure 14-5335. A53SS_CORE3_ETM_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-16082. A53SS_CORE3_ETM_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16082. A53SS_CORE3_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16082. A53SS_CORE3_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16082. A53SS_CORE3_ETM_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1220 A53SS_CORE3_ETM_TRCACATR5 Register

1 A53SS_CORE3_ETM_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-16083. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 04A8h**

Figure 14-5336. A53SS_CORE3_ETM_TRCACATR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR5_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR5_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR5_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-16085. A53SS_CORE3_ETM_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16085. A53SS_CORE3_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16085. A53SS_CORE3_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16085. A53SS_CORE3_ETM_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1221 A53SS_CORE3_ETM_TRCACATR6 Register

1 A53SS_CORE3_ETM_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

Address Comparator Access Type Registers 6

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Table 14-16086. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 04B0h**

Figure 14-5337. A53SS_CORE3_ETM_TRCACATR6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCACATR6_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCACATR6_31_22</td><td>DTBM</td><td>DATARANGE</td><td colspan="2">DATASIZE</td><td colspan="2">DATAMATCH</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXLEVEL_NS</td><td colspan="4">EXLEVEL_S</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_TRCACATR6_7_7</td><td colspan="3">CONTEXT</td><td colspan="2">CONTEXTTYPE</td><td colspan="2">TYPE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-16088. A53SS_CORE3_ETM_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16088. A53SS_CORE3_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16088. A53SS_CORE3_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16088. A53SS_CORE3_ETM_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1222 A53SS_CORE3_ETM_TRCACATR7 Register

1 A53SS_CORE3_ETM_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

Address Comparator Access Type Registers 7

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Table 14-16089. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 04B8h**

Figure 14-5338. A53SS_CORE3_ETM_TRCACATR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR7_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR7_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR7_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-16091. A53SS_CORE3_ETM_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-16091. A53SS_CORE3_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-16091. A53SS_CORE3_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-16091. A53SS_CORE3_ETM_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.1223 A53SS_CORE3_ETM_TRCCIDCVR0 Register

1 A53SS_CORE3_ETM_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-16092. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0600h**

Figure 14-5339. A53SS_CORE3_ETM_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-16094. A53SS_CORE3_ETM_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.1224 A53SS_CORE3_ETM_TRCVMIDCVR0 Register

1 A53SS_CORE3_ETM_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-16095. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0640h**

Figure 14-5340. A53SS_CORE3_ETM_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-16097. A53SS_CORE3_ETM_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.1225 A53SS_CORE3_ETM_TRCCIDCCTLR0 Register

1 A53SS_CORE3_ETM_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

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Table 14-16098. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0680h**

Figure 14-5341. A53SS_CORE3_ETM_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-16100. A53SS_CORE3_ETM_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.1226 A53SS_CORE3_ETM_TRCITATBIDR Register

1 A53SS_CORE3_ETM_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

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Table 14-16101. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0EE4h**

Figure 14-5342. A53SS_CORE3_ETM_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-16103. A53SS_CORE3_ETM_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.1227 A53SS_CORE3_ETM_TRCITIDATAR Register

1 A53SS_CORE3_ETM_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

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Table 14-16104. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0EECh**

Figure 14-5343. A53SS_CORE3_ETM_TRCITIDATAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITIDATAR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITIDATAR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITIDATAR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITIDATAR_31_5			ATDATAM_31	ATDATAM_23	ATDATAM_15	ATDATAM_7	ATDATAM_0
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-16106. A53SS_CORE3_ETM_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.1228 A53SS_CORE3_ETM_TRCITIATBINR Register

1 A53SS_CORE3_ETM_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

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Table 14-16107. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0EF4h**

Figure 14-5344. A53SS_CORE3_ETM_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-16109. A53SS_CORE3_ETM_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.1229 A53SS_CORE3_ETM_TRCITIATBOUTR Register

1 A53SS_CORE3_ETM_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-16110. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0EFCh**

Figure 14-5345. A53SS_CORE3_ETM_TRCITIATBOUTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_31_10</td><td colspan="2">BYTES</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_7_2</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-16112. A53SS_CORE3_ETM_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.1230 A53SS_CORE3_ETM_TRCITCTRL Register

1 A53SS_CORE3_ETM_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

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Table 14-16113. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0F00h**

Figure 14-5346. A53SS_CORE3_ETM_TRCITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_TRCITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITCTRL_31_1							ITEN
R/W							R/W
0h							0h

Table 14-16115. A53SS_CORE3_ETM_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.1231 A53SS_CORE3_ETM_TRCCLAIMSET Register

1 A53SS_CORE3_ETM_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-16116. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FA0h**

Figure 14-5347. A53SS_CORE3_ETM_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-16118. A53SS_CORE3_ETM_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.1232 A53SS_CORE3_ETM_TRCCLAIMCLR Register

1 A53SS_CORE3_ETM_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-16119. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FA4h**

Figure 14-5348. A53SS_CORE3_ETM_TRCCLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMCLR_31_4				CLR			
R/W				R/W			
0h				0h			

Table 14-16121. A53SS_CORE3_ETM_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.1233 A53SS_CORE3_ETM_TRCDEVAFF0 Register

1 A53SS_CORE3_ETM_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000003h]

Device Affinity Register 0

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Table 14-16122. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FA8h**

Figure 14-5349. A53SS_CORE3_ETM_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000003h							
23	22	21	20	19	18	17	16
MPIDR_EL1_31_0							
R/W							
80000003h							
15	14	13	12	11	10	9	8
MPIDR_EL1_31_0							
R/W							
80000003h							
7	6	5	4	3	2	1	0
MPIDR_EL1_31_0							
R/W							
80000003h							

Table 14-16124. A53SS_CORE3_ETM_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000003h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1234 A53SS_CORE3_ETM_TRCDEVAFF1 Register

1 A53SS_CORE3_ETM_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

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Table 14-16125. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FACh**

Figure 14-5350. A53SS_CORE3_ETM_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-16127. A53SS_CORE3_ETM_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1235 A53SS_CORE3_ETM_TRCLAR Register

1 A53SS_CORE3_ETM_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

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Table 14-16128. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FB0h**

Figure 14-5351. A53SS_CORE3_ETM_TRCLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-16130. A53SS_CORE3_ETM_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.1236 A53SS_CORE3_ETM_TRCLSR Register

1 A53SS_CORE3_ETM_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

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Table 14-16131. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FB4h**

Figure 14-5352. A53SS_CORE3_ETM_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-16133. A53SS_CORE3_ETM_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.1237 A53SS_CORE3_ETM_TRCAUTHSTATUS Register

1 A53SS_CORE3_ETM_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

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Table 14-16134. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FB8h**

Figure 14-5353. A53SS_CORE3_ETM_TRCAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-16136. A53SS_CORE3_ETM_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-16136. A53SS_CORE3_ETM_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.1238 A53SS_CORE3_ETM_TRCDEVARCH Register

1 A53SS_CORE3_ETM_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

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Table 14-16137. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FBCh**

Figure 14-5354. A53SS_CORE3_ETM_TRCDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
4A13h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
4A13h							

Table 14-16139. A53SS_CORE3_ETM_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.1239 A53SS_CORE3_ETM_TRCDEVID Register

1 A53SS_CORE3_ETM_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-16140. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FC8h**

Figure 14-5355. A53SS_CORE3_ETM_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVID							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVID							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVID							
R/W							
0h							

Table 14-16142. A53SS_CORE3_ETM_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.1240 A53SS_CORE3_ETM_TRCDEVTYPE Register

1 A53SS_CORE3_ETM_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

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Table 14-16143. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FCCh**

Figure 14-5356. A53SS_CORE3_ETM_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-16145. A53SS_CORE3_ETM_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.1241 A53SS_CORE3_ETM_TRCPIDR4 Register

1 A53SS_CORE3_ETM_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

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Table 14-16146. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FD0h**

Figure 14-5357. A53SS_CORE3_ETM_TRCPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-16148. A53SS_CORE3_ETM_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.1242 A53SS_CORE3_ETM_TRCPIDR5 Register

1 A53SS_CORE3_ETM_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

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Table 14-16149. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FD4h**

Figure 14-5358. A53SS_CORE3_ETM_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-16151. A53SS_CORE3_ETM_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.1243 A53SS_CORE3_ETM_TRCPIDR6 Register

1 A53SS_CORE3_ETM_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

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Table 14-16152. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FD8h**

Figure 14-5359. A53SS_CORE3_ETM_TRCPIDR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR6_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR6_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR6_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR6_7_0							
R/W							
0h							

Table 14-16154. A53SS_CORE3_ETM_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.1244 A53SS_CORE3_ETM_TRCPIDR7 Register

1 A53SS_CORE3_ETM_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

Return to Summary Table

Table 14-16155. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FDCh**

Figure 14-5360. A53SS_CORE3_ETM_TRCPIDR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR7_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR7_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR7_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR7_7_0							
R/W							
0h							

Table 14-16157. A53SS_CORE3_ETM_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.1245 A53SS_CORE3_ETM_TRCPIDR0 Register

1 A53SS_CORE3_ETM_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

Return to Summary Table

Table 14-16158. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FE0h**

Figure 14-5361. A53SS_CORE3_ETM_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
5Dh							

Table 14-16160. A53SS_CORE3_ETM_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.1246 A53SS_CORE3_ETM_TRCPIDR1 Register

1 A53SS_CORE3_ETM_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

Return to Summary Table

Table 14-16161. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FE4h**

Figure 14-5362. A53SS_CORE3_ETM_TRCPIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DES_0</td><td colspan="4">PART_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Bh</td><td colspan="4">9h</td></tr>
</table>

Table 14-16163. A53SS_CORE3_ETM_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.1247 A53SS_CORE3_ETM_TRCPIDR2 Register

1 A53SS_CORE3_ETM_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-16164. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FE8h**

Figure 14-5363. A53SS_CORE3_ETM_TRCPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-16166. A53SS_CORE3_ETM_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.1248 A53SS_CORE3_ETM_TRCPIDR3 Register

1 A53SS_CORE3_ETM_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

Return to Summary Table

Table 14-16167. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FECh**

Figure 14-5364. A53SS_CORE3_ETM_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-16169. A53SS_CORE3_ETM_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.1249 A53SS_CORE3_ETM_TRCCIDR0 Register

1 A53SS_CORE3_ETM_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

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Table 14-16170. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FF0h**

Figure 14-5365. A53SS_CORE3_ETM_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_0							
R/W							
Dh							

Table 14-16172. A53SS_CORE3_ETM_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.1250 A53SS_CORE3_ETM_TRCCIDR1 Register

1 A53SS_CORE3_ETM_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

Return to Summary Table

Table 14-16173. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FF4h**

Figure 14-5366. A53SS_CORE3_ETM_TRCCIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16175. A53SS_CORE3_ETM_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.1251 A53SS_CORE3_ETM_TRCCIDR2 Register

1 A53SS_CORE3_ETM_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-16176. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FF8h**

Figure 14-5367. A53SS_CORE3_ETM_TRCCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-16178. A53SS_CORE3_ETM_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.1252 A53SS_CORE3_ETM_TRCCIDR3 Register

1 A53SS_CORE3_ETM_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

Return to Summary Table

Table 14-16179. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3033 0FFCh**

Figure 14-5368. A53SS_CORE3_ETM_TRCCIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
</table>

Table 14-16181. A53SS_CORE3_ETM_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.1253 A53SS_CORE3_CTI_CTICONTROL Register

1 A53SS_CORE3_CTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

Return to Summary Table

Table 14-16182. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0000h**

Figure 14-5369. A53SS_CORE3_CTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICONTROL_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICONTROL_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-16184. A53SS_CORE3_CTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.1254 A53SS_CORE3_CTI_CTIINTACK Register

1 A53SS_CORE3_CTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

Return to Summary Table

Table 14-16185. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0010h**

Figure 14-5370. A53SS_CORE3_CTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ACK_N							
R/W							
0h							

Table 14-16187. A53SS_CORE3_CTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.1255 A53SS_CORE3_CTI_CTIAPPSET Register

1 A53SS_CORE3_CTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

Return to Summary Table

Table 14-16188. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0014h**

Figure 14-5371. A53SS_CORE3_CTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-16190. A53SS_CORE3_CTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.1256 A53SS_CORE3_CTI_CTIAPPCLEAR Register

1 A53SS_CORE3_CTI_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

Return to Summary Table

Table 14-16191. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0018h**

Figure 14-5372. A53SS_CORE3_CTI_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIAPPCLEAR_31_4				CTIAPPCLEARX			
R/W				R/W			
0h				0h			

Table 14-16193. A53SS_CORE3_CTI_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.1257 A53SS_CORE3_CTI_CTIAPPPULSE Register

1 A53SS_CORE3_CTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

Return to Summary Table

Table 14-16194. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 001Ch**

Figure 14-5373. A53SS_CORE3_CTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPPULSE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPPULSE_31_4				CTIAPPPULSEX			
R/W				R/W			
0h				0h			

Table 14-16196. A53SS_CORE3_CTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.1258 A53SS_CORE3_CTI_CTIINEN0 Register

1 A53SS_CORE3_CTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

Return to Summary Table

Table 14-16197. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0020h**

Figure 14-5374. A53SS_CORE3_CTI_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN0_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16199. A53SS_CORE3_CTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.1259 A53SS_CORE3_CTI_CTIINEN1 Register

1 A53SS_CORE3_CTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

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Table 14-16200. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0024h**

Figure 14-5375. A53SS_CORE3_CTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16202. A53SS_CORE3_CTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.1260 A53SS_CORE3_CTI_CTIINEN2 Register

1 A53SS_CORE3_CTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

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Table 14-16203. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0028h**

Figure 14-5376. A53SS_CORE3_CTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN2_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN2_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN2_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN2_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16205. A53SS_CORE3_CTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.1261 A53SS_CORE3_CTI_CTIINEN3 Register

1 A53SS_CORE3_CTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-16206. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 002Ch**

Figure 14-5377. A53SS_CORE3_CTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN3_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16208. A53SS_CORE3_CTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.1262 A53SS_CORE3_CTI_CTIINEN4 Register

1 A53SS_CORE3_CTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

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Table 14-16209. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0030h**

Figure 14-5378. A53SS_CORE3_CTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16211. A53SS_CORE3_CTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.1263 A53SS_CORE3_CTI_CTIINEN5 Register

1 A53SS_CORE3_CTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-16212. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0034h**

Figure 14-5379. A53SS_CORE3_CTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16214. A53SS_CORE3_CTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.1264 A53SS_CORE3_CTI_CTIINEN6 Register

1 A53SS_CORE3_CTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-16215. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0038h**

Figure 14-5380. A53SS_CORE3_CTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN6_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16217. A53SS_CORE3_CTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.1265 A53SS_CORE3_CTI_CTIINEN7 Register

1 A53SS_CORE3_CTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-16218. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 003Ch**

Figure 14-5381. A53SS_CORE3_CTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-16220. A53SS_CORE3_CTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.1266 A53SS_CORE3_CTI_CTIOUTEN0 Register

1 A53SS_CORE3_CTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-16221. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00A0h**

Figure 14-5382. A53SS_CORE3_CTI_CTIOUTEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN0_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIOUTEN0_31_4</td><td colspan="4">OUTENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16223. A53SS_CORE3_CTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.1267 A53SS_CORE3_CTI_CTIOUTEN1 Register

1 A53SS_CORE3_CTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

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Table 14-16224. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3034 00A4h**

Figure 14-5383. A53SS_CORE3_CTI_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN1_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIOUTEN1_31_4</td><td colspan="4">OUTENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16226. A53SS_CORE3_CTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.1268 A53SS_CORE3_CTI_CTIOUTEN2 Register

1 A53SS_CORE3_CTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

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Table 14-16227. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00A8h**

Figure 14-5384. A53SS_CORE3_CTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN2_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16229. A53SS_CORE3_CTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.1269 A53SS_CORE3_CTI_CTIOUTEN3 Register

1 A53SS_CORE3_CTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

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Table 14-16230. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00ACh**

Figure 14-5385. A53SS_CORE3_CTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16232. A53SS_CORE3_CTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.1270 A53SS_CORE3_CTI_CTIOUTEN4 Register

1 A53SS_CORE3_CTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

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Table 14-16233. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00B0h**

Figure 14-5386. A53SS_CORE3_CTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16235. A53SS_CORE3_CTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.1271 A53SS_CORE3_CTI_CTIOUTEN5 Register

1 A53SS_CORE3_CTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

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Table 14-16236. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00B4h**

Figure 14-5387. A53SS_CORE3_CTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16238. A53SS_CORE3_CTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.1272 A53SS_CORE3_CTI_CTIOUTEN6 Register

1 A53SS_CORE3_CTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

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Table 14-16239. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00B8h**

Figure 14-5388. A53SS_CORE3_CTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16241. A53SS_CORE3_CTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.1273 A53SS_CORE3_CTI_CTIOUTEN7 Register

1 A53SS_CORE3_CTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

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Table 14-16242. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 00BCh**

Figure 14-5389. A53SS_CORE3_CTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-16244. A53SS_CORE3_CTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.1274 A53SS_CORE3_CTI_CTITRIGINSTATUS Register

1 A53SS_CORE3_CTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-16245. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0130h**

Figure 14-5390. A53SS_CORE3_CTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TRINN							
R/W							
0h							

Table 14-16247. A53SS_CORE3_CTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.1275 A53SS_CORE3_CTI_CTITRIGOUTSTATUS Register

1 A53SS_CORE3_CTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

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Table 14-16248. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0134h**

Figure 14-5391. A53SS_CORE3_CTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TROUTN							
R/W							
0h							

Table 14-16250. A53SS_CORE3_CTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.1276 A53SS_CORE3_CTI_CTICHINSTATUS Register

1 A53SS_CORE3_CTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

Return to Summary Table

Table 14-16251. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0138h**

Figure 14-5392. A53SS_CORE3_CTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICHINSTATUS_31_4				CHINN			
R/W				R/W			
0h				0h			

Table 14-16253. A53SS_CORE3_CTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.1277 A53SS_CORE3_CTI_CTICHOUTSTATUS Register

1 A53SS_CORE3_CTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-16254. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 013Ch**

Figure 14-5393. A53SS_CORE3_CTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-16256. A53SS_CORE3_CTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.1278 A53SS_CORE3_CTI_CTIGATE Register

1 A53SS_CORE3_CTI_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

Return to Summary Table

Table 14-16257. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0140h**

Figure 14-5394. A53SS_CORE3_CTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIGATE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIGATE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIGATE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIGATE_31_4				GATEX			
R/W				R/W			
0h				Fh			

Table 14-16259. A53SS_CORE3_CTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.1279 A53SS_CORE3_CTI_ASICCTL Register

1 A53SS_CORE3_CTI_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

Return to Summary Table

Table 14-16260. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0144h**

Figure 14-5395. A53SS_CORE3_CTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-16262. A53SS_CORE3_CTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.1280 A53SS_CORE3_CTI_CTIITCTRL Register

1 A53SS_CORE3_CTI_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

Return to Summary Table

Table 14-16263. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0F00h**

Figure 14-5396. A53SS_CORE3_CTI_CTIITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_CTIITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-16265. A53SS_CORE3_CTI_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.1281 A53SS_CORE3_CTI_CTICLAIMSET Register

1 A53SS_CORE3_CTI_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-16266. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FA0h**

Figure 14-5397. A53SS_CORE3_CTI_CTICLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMSET_31_4				CLAIMX			
R/W				R/W			
0h				Fh			

Table 14-16268. A53SS_CORE3_CTI_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.1282 A53SS_CORE3_CTI_CTICLAIMCLR Register

1 A53SS_CORE3_CTI_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

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Table 14-16269. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FA4h**

Figure 14-5398. A53SS_CORE3_CTI_CTICLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICLAIMCLR_31_4				CLAIMX			
R/W				R/W			
0h				0h			

Table 14-16271. A53SS_CORE3_CTI_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.1283 A53SS_CORE3_CTI_CTIDEVAFF0 Register

1 A53SS_CORE3_CTI_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000003h]

CTI Device Affinity Register 0

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Table 14-16272. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FA8h**

Figure 14-5399. A53SS_CORE3_CTI_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000003h							
23	22	21	20	19	18	17	16
CTIDEVAFF0							
R/W							
80000003h							
15	14	13	12	11	10	9	8
CTIDEVAFF0							
R/W							
80000003h							
7	6	5	4	3	2	1	0
CTIDEVAFF0							
R/W							
80000003h							

Table 14-16274. A53SS_CORE3_CTI_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000003h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1284 A53SS_CORE3_CTI_CTIDEVAFF1 Register

1 A53SS_CORE3_CTI_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-16275. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FACh**

Figure 14-5400. A53SS_CORE3_CTI_CTIDEVAFF1 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
CTIDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
CTIDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
CTIDEVAFF1							
R/W							
0h							

Table 14-16277. A53SS_CORE3_CTI_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.1285 A53SS_CORE3_CTI_CTILAR Register

1 A53SS_CORE3_CTI_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

Return to Summary Table

Table 14-16278. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FB0h**

Figure 14-5401. A53SS_CORE3_CTI_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-16280. A53SS_CORE3_CTI_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.1286 A53SS_CORE3_CTI_CTILSR Register

1 A53SS_CORE3_CTI_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-16281. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FB4h**

Figure 14-5402. A53SS_CORE3_CTI_CTILSR Name Register

31	30	29	28	27	26	25	24
RES0_CTILSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTILSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTILSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTILSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-16283. A53SS_CORE3_CTI_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.1287 A53SS_CORE3_CTI_CTIAUTHSTATUS Register

1 A53SS_CORE3_CTI_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-16284. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FB8h**

Figure 14-5403. A53SS_CORE3_CTI_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-16286. A53SS_CORE3_CTI_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.1288 A53SS_CORE3_CTI_CTIDEVARCH Register

1 A53SS_CORE3_CTI_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

Return to Summary Table

Table 14-16287. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FBCh**

Figure 14-5404. A53SS_CORE3_CTI_CTIDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
</table>

Table 14-16289. A53SS_CORE3_CTI_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.1289 A53SS_CORE3_CTI_CTIDEVID2 Register

1 A53SS_CORE3_CTI_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

Return to Summary Table

Table 14-16290. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FC0h**

Figure 14-5405. A53SS_CORE3_CTI_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-16292. A53SS_CORE3_CTI_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1290 A53SS_CORE3_CTI_CTIDEVID1 Register

1 A53SS_CORE3_CTI_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

Return to Summary Table

Table 14-16293. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FC4h**

Figure 14-5406. A53SS_CORE3_CTI_CTIDEVID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIDEVID1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIDEVID1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIDEVID1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RES0_CTIDEVID1_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16295. A53SS_CORE3_CTI_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.1291 A53SS_CORE3_CTI_CTIDEVID Register

1 A53SS_CORE3_CTI_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

Return to Summary Table

Table 14-16296. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FC8h**

Figure 14-5407. A53SS_CORE3_CTI_CTIDEVID Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID_31_26						INOUT	
R/W						R/W	
0h						1h	
23	22	21	20	19	18	17	16
RES0_CTIDEVID_23_22		NUMCHAN					
R/W		R/W					
0h		4h					
15	14	13	12	11	10	9	8
RES0_CTIDEVID_15_14		NUMTRIG					
R/W		R/W					
0h		8h					
7	6	5	4	3	2	1	0
RES0_CTIDEVID_7_5			EXTMUXNUM				
R/W			R/W				
0h			0h				

Table 14-16298. A53SS_CORE3_CTI_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-16298. A53SS_CORE3_CTI_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.1292 A53SS_CORE3_CTI_CTIDEVTYPE Register

1 A53SS_CORE3_CTI_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-16299. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FCCh**

Figure 14-5408. A53SS_CORE3_CTI_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-16301. A53SS_CORE3_CTI_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.1293 A53SS_CORE3_CTI_CTIPIDR4 Register

1 A53SS_CORE3_CTI_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-16302. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FD0h**

Figure 14-5409. A53SS_CORE3_CTI_CTIPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-16304. A53SS_CORE3_CTI_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.1294 A53SS_CORE3_CTI_CTIPIDR5 Register

1 A53SS_CORE3_CTI_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

Return to Summary Table

Table 14-16305. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FD4h**

Figure 14-5410. A53SS_CORE3_CTI_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-16307. A53SS_CORE3_CTI_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1295 A53SS_CORE3_CTI_CTIPIDR6 Register

1 A53SS_CORE3_CTI_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

Return to Summary Table

Table 14-16308. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FD8h**

Figure 14-5411. A53SS_CORE3_CTI_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-16310. A53SS_CORE3_CTI_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1296 A53SS_CORE3_CTI_CTIPIDR7 Register

1 A53SS_CORE3_CTI_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

Return to Summary Table

Table 14-16311. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FDCh**

Figure 14-5412. A53SS_CORE3_CTI_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-16313. A53SS_CORE3_CTI_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.1297 A53SS_CORE3_CTI_CTIPIDR0 Register

1 A53SS_CORE3_CTI_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

Return to Summary Table

Table 14-16314. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FE0h**

Figure 14-5413. A53SS_CORE3_CTI_CTIPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
A8h							

Table 14-16316. A53SS_CORE3_CTI_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.1298 A53SS_CORE3_CTI_CTIPIDR1 Register

1 A53SS_CORE3_CTI_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

Return to Summary Table

Table 14-16317. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FE4h**

Figure 14-5414. A53SS_CORE3_CTI_CTIPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-16319. A53SS_CORE3_CTI_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.1299 A53SS_CORE3_CTI_CTIPIDR2 Register

1 A53SS_CORE3_CTI_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

Return to Summary Table

Table 14-16320. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FE8h**

Figure 14-5415. A53SS_CORE3_CTI_CTIPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-16322. A53SS_CORE3_CTI_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.1300 A53SS_CORE3_CTI_CTIPIDR3 Register

1 A53SS_CORE3_CTI_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

Return to Summary Table

Table 14-16323. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FECh**

Figure 14-5416. A53SS_CORE3_CTI_CTIPIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16325. A53SS_CORE3_CTI_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.1301 A53SS_CORE3_CTI_CTICIDR0 Register

1 A53SS_CORE3_CTI_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

Return to Summary Table

Table 14-16326. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FF0h**

Figure 14-5417. A53SS_CORE3_CTI_CTICIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-16328. A53SS_CORE3_CTI_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.1302 A53SS_CORE3_CTI_CTICIDR1 Register

1 A53SS_CORE3_CTI_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

Return to Summary Table

Table 14-16329. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FF4h**

Figure 14-5418. A53SS_CORE3_CTI_CTICIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-16331. A53SS_CORE3_CTI_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.1303 A53SS_CORE3_CTI_CTICIDR2 Register

1 A53SS_CORE3_CTI_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

Return to Summary Table

Table 14-16332. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FF8h**

Figure 14-5419. A53SS_CORE3_CTI_CTICIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-16334. A53SS_CORE3_CTI_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.1304 A53SS_CORE3_CTI_CTICIDR3 Register

1 A53SS_CORE3_CTI_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

Return to Summary Table

Table 14-16335. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3034 0FFCh**

Figure 14-5420. A53SS_CORE3_CTI_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-16337. A53SS_CORE3_CTI_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.2 a53_rs_bw_limiter

a53_rs_bw_limiter

14.3.1.2.1 a53_rs_bw_limiter Summaries

a53_rs_bw_limiter Summaries

Table 14-16338. RATE_LIMITER Registers, Base Address=3040 3000h, Length=4096

Offset	Length	Register Name	A53_RS_BW_LIMITER0 Physical Address
0h	32	RATE_LIMITER_PID	3040 3000h
4h	32	RATE_LIMITER_CTRL	3040 3004h
100h	32	RATE_LIMITER_RD_BW_CIR	3040 3100h
104h	32	RATE_LIMITER_RD_BW_PIR	3040 3104h
108h	32	RATE_LIMITER_RD_BW_BURST_OFFSET	3040 3108h
10Ch	32	RATE_LIMITER_RD_BW_INFO	3040 310Ch
120h	32	RATE_LIMITER_RD_BW_STATS	3040 3120h
124h	32	RATE_LIMITER_RD_BW_STATS_THRSHLD	3040 3124h
128h	32	RATE_LIMITER_RD_BW_WINDOWS_CNT	3040 3128h
12Ch	32	RATE_LIMITER_RD_BW_STATS_CIR	3040 312Ch
130h	32	RATE_LIMITER_RD_BW_STATS_PIR	3040 3130h
134h	32	RATE_LIMITER_RD_BW_THRSHLD_CNT	3040 3134h
138h	32	RATE_LIMITER_RD_BYTES_MAX	3040 3138h
300h	32	RATE_LIMITER_RD_TXN	3040 3300h
30Ch	32	RATE_LIMITER_RD_TXN_INFO	3040 330Ch
320h	32	RATE_LIMITER_RD_TXN_STATS	3040 3320h
324h	32	RATE_LIMITER_RD_TXN_STATS_THRSHLD	3040 3324h
328h	32	RATE_LIMITER_RD_TXN_WINDOWS_CNT	3040 3328h
32Ch	32	RATE_LIMITER_RD_TXN_LIMIT_CNT	3040 332Ch
330h	32	RATE_LIMITER_RD_TXN_THRESHOLD_CNT	3040 3330h
334h	32	RATE_LIMITER_RD_TXN_LIMIT_TOTAL	3040 3334h
338h	32	RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL	3040 3338h
33Ch	32	RATE_LIMITER_RD_TXN_MAX	3040 333Ch

14.3.1.2.2 a53_rs_bw_limiter Registers

a53_rs_bw_limiter Registers

14.3.1.2.2.1 RATE_LIMITER_PID Register

1 RATE_LIMITER_PID Register (Offset = 0h) [reset = 66602900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-16339. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3000h**

Figure 14-5421. RATE_LIMITER_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		660h			
23	22	21	20	19	18	17	16
FUNC							
R							
660h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
5h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-16341. RATE_LIMITER_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	PID bu identifier Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	660h	PID function identifier Reset Source: rst_mod_g_rst_n
15:11	RTL_VER	R	5h	PID RTL version number Reset Source: rst_mod_g_rst_n
10:8	MAJOR_REV	R	1h	PID Major revision number Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	PID custom Reset Source: rst_mod_g_rst_n
5:0	MINOR_REV	R	0h	PID Minor revision number Reset Source: rst_mod_g_rst_n

14.3.1.2.2.2 RATE_LIMITER_CTRL Register

1 RATE_LIMITER_CTRL Register (Offset = 4h) [reset = 0h]

This register controls the overall behavior of the rate limiter module

Return to Summary Table

Table 14-16342. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3004h**

Figure 14-5422. RATE_LIMITER_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REGION_FILTER_EN	WR_TXN_ENABLE	RD_TXN_ENABLE	WR_BW_ENABLE	RD_BW_ENABLE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-16344. RATE_LIMITER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REGION_FILTER_EN	R/W	0h	Enable the region filter, which will only apply the bandwith and transaction limits to the configured address regions Reset Source: rst_mod_g_rst_n
3	WR_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding write transactions Reset Source: rst_mod_g_rst_n
2	RD_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding read transactions Reset Source: rst_mod_g_rst_n
1	WR_BW_ENABLE	R/W	0h	Enable write bandwidth limiting Reset Source: rst_mod_g_rst_n
0	RD_BW_ENABLE	R/W	0h	Enable read bandwidth limiting Reset Source: rst_mod_g_rst_n

14.3.1.2.2.3 RATE_LIMITER_RD_BW_CIR Register

1 RATE_LIMITER_RD_BW_CIR Register (Offset = 100h) [reset = 0h]

Read Bandwidth Committed Information Rate

Return to Summary Table

Table 14-16345. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3100h**

Figure 14-5423. RATE_LIMITER_RD_BW_CIR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16347. RATE_LIMITER_RD_BW_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR	R/W	0h	Committed Information Rate Reset Source: rst_mod_g_rst_n

14.3.1.2.2.4 RATE_LIMITER_RD_BW_PIR Register

1 RATE_LIMITER_RD_BW_PIR Register (Offset = 104h) [reset = 0h]

Read Bandwidth Peak Information Rate

Return to Summary Table

Table 14-16348. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3104h**

Figure 14-5424. RATE_LIMITER_RD_BW_PIR Name Register

31	30	29	28	27	26	25	24
PIR							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR							
R/W							
0h							

Table 14-16350. RATE_LIMITER_RD_BW_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR	R/W	0h	Peak Information Rate Reset Source: rst_mod_g_rst_n

14.3.1.2.2.5 RATE_LIMITER_RD_BW_BURST_OFFSET Register

1 RATE_LIMITER_RD_BW_BURST_OFFSET Register (Offset = 108h) [reset = 0h]

Read Bandwidth Burst Offset

Return to Summary Table

Table 14-16351. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3108h**

Figure 14-5425. RATE_LIMITER_RD_BW_BURST_OFFSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFFSET							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFSET							
R/W							
0h							

Table 14-16353. RATE_LIMITER_RD_BW_BURST_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFFSET	R/W	0h	Burst Offset - the number of bytes before the Committed Information Rate is applied at startup or after a period of inactivity. Peak Information Rate will still apply Reset Source: rst_mod_g_rst_n

14.3.1.2.2.6 RATE_LIMITER_RD_BW_INFO Register

1 RATE_LIMITER_RD_BW_INFO Register (Offset = 10Ch) [reset = 0h]

Read Bandwidth State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16354. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 310Ch**

Figure 14-5426. RATE_LIMITER_RD_BW_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						COLOR	
NONE						R	
0h						0h	

Table 14-16356. RATE_LIMITER_RD_BW_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	COLOR	R	0h	Read Bandwidth three-color marker output from rategen submodule Reset Source: rst_mod_g_rst_n

14.3.1.2.2.7 RATE_LIMITER_RD_BW_STATS Register

1 RATE_LIMITER_RD_BW_STATS Register (Offset = 120h) [reset = 4000000h]

Read Bandwidth Statistics Control Register

Return to Summary Table

Table 14-16357. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3120h**

Figure 14-5427. RATE_LIMITER_RD_BW_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WINDOW							
R/W							
400h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16359. RATE_LIMITER_RD_BW_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable read bandwidth statistics Reset Source: rst_mod_g_rst_n

14.3.1.2.2.8 RATE_LIMITER_RD_BW_STATS_THRSHLD Register

1 RATE_LIMITER_RD_BW_STATS_THRSHLD Register (Offset = 124h) [reset = 0h]

A statistics threshold separate from the CIR and PIR

Return to Summary Table

Table 14-16360. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3124h**

Figure 14-5428. RATE_LIMITER_RD_BW_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16362. RATE_LIMITER_RD_BW_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	THRESHOLD	R/W	0h	Read bandwidth stats threshold in bytes. Note that this is total bytes, unlike CIR and PIR. CIR and PIR are based on a rolling window, and the statistics threshold is based on a fixed window. This will still take into account DDR bytes used, so can be compared to CIR and PIR directly if the bandwidths are converted via the equations for CIR and PIR. The threshold bandwidth is programmed here as bytes per window Reset Source: rst_mod_g_rst_n

14.3.1.2.2.9 RATE_LIMITER_RD_BW_WINDOWS_CNT Register

1 RATE_LIMITER_RD_BW_WINDOWS_CNT Register (Offset = 128h) [reset = 0h]

Read Bandwidth Statistics - Window Count

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Table 14-16363. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3128h**

Figure 14-5429. RATE_LIMITER_RD_BW_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16365. RATE_LIMITER_RD_BW_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Read bandwidth window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.2.2.10 RATE_LIMITER_RD_BW_STATS_CIR Register

1 RATE_LIMITER_RD_BW_STATS_CIR Register (Offset = 12Ch) [reset = 0h]

Read Bandwidth Statistics - CIR Count

Return to Summary Table

Table 14-16366. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 312Ch**

Figure 14-5430. RATE_LIMITER_RD_BW_STATS_CIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16368. RATE_LIMITER_RD_BW_STATS_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read Commit Information Rate occurred. Note that if PIR is set to a lower value than CIR or if the burst offset feature is used, this will also count times that PIR is reached. Reset Source: rst_mod_g_rst_n

14.3.1.2.2.11 RATE_LIMITER_RD_BW_STATS_PIR Register

1 RATE_LIMITER_RD_BW_STATS_PIR Register (Offset = 130h) [reset = 0h]

Read Bandwidth Statistics - PIR Count

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Table 14-16369. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3130h**

Figure 14-5431. RATE_LIMITER_RD_BW_STATS_PIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16371. RATE_LIMITER_RD_BW_STATS_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read Peak Information Rate occurred Reset Source: rst_mod_g_rst_n

14.3.1.2.2.12 RATE_LIMITER_RD_BW_THRSHLD_CNT Register

1 RATE_LIMITER_RD_BW_THRSHLD_CNT Register (Offset = 134h) [reset = 0h]

Read Bandwidth Statistics - Threshold Count

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Table 14-16372. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3134h**

Figure 14-5432. RATE_LIMITER_RD_BW_THRSHLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16374. RATE_LIMITER_RD_BW_THRSHLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read bytes transferred exceeded the statistics threshold Reset Source: rst_mod_g_rst_n

14.3.1.2.2.13 RATE_LIMITER_RD_BYTES_MAX Register

1 RATE_LIMITER_RD_BYTES_MAX Register (Offset = 138h) [reset = 0h]

The maximum number of bytes seen in a single statitsics window. This can be compared with the window size to calculate the maximum bandwidth seen

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Table 14-16375. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3138h**

Figure 14-5433. RATE_LIMITER_RD_BYTES_MAX Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16377. RATE_LIMITER_RD_BYTES_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Max number of bytes in a single window. This number accounts for DDR bandwidth consumed, not simply the accumulation of the packet bytecnt values across a window. The max bandwidth calculation is the total bytes value in this MMR divided by the windows size in RD_BW_STATS.window and multiplied with the interface frequency: RD_BYTES_MAX * FREQ / RD_BW_STATS.window Reset Source: rst_mod_g_rst_n

14.3.1.2.2.14 RATE_LIMITER_RD_TXN Register

1 RATE_LIMITER_RD_TXN Register (Offset = 300h) [reset = 40h]

The maximum number of outstanding read transactions the rate limiter will allow

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Table 14-16378. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3300h**

Figure 14-5434. RATE_LIMITER_RD_TXN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIMIT							
R/W							
40h							
7	6	5	4	3	2	1	0
LIMIT							
R/W							
40h							

Table 14-16380. RATE_LIMITER_RD_TXN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	LIMIT	R/W	40h	The maximum number of outstanding read transactions allowed. NOTE: This cannot be programmed to a zero. If a zero is written, it will default to the reset value of 16'd64, as a limit of zero outstanding transactions would hang the interface. Reset Source: rst_mod_g_rst_n

14.3.1.2.2.15 RATE_LIMITER_RD_TXN_INFO Register

1 RATE_LIMITER_RD_TXN_INFO Register (Offset = 30Ch) [reset = 0h]

Read Transaction State machine information. Primarly for verification purposes

Return to Summary Table

Table 14-16381. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 330Ch**

Figure 14-5435. RATE_LIMITER_RD_TXN_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	OCC						
NONE	R						
0h	0h						

Table 14-16383. RATE_LIMITER_RD_TXN_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	OCC	R	0h	Read transaction scoreboard occupancy Reset Source: rst_mod_g_rst_n

14.3.1.2.2.16 RATE_LIMITER_RD_TXN_STATS Register

1 RATE_LIMITER_RD_TXN_STATS Register (Offset = 320h) [reset = 4000000h]

Read Transaction Stats Control Register

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Table 14-16384. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3320h**

Figure 14-5436. RATE_LIMITER_RD_TXN_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	22	21	20	19	18	17	16
WINDOW							
R/W							
400h							
15	14	13	12	11	10	9	8
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16386. RATE_LIMITER_RD_TXN_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable read transaction statistics Reset Source: rst_mod_g_rst_n

14.3.1.2.2.17 RATE_LIMITER_RD_TXN_STATS_THRSHLD Register

1 RATE_LIMITER_RD_TXN_STATS_THRSHLD Register (Offset = 324h) [reset = 0h]

A statistics threshold separate from the read transaction limit

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Table 14-16387. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3324h**

Figure 14-5437. RATE_LIMITER_RD_TXN_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16389. RATE_LIMITER_RD_TXN_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THRESHOLD	R/W	0h	Read transaction statistics threshold. The threshold can be set to any value, though it will saturate at the outstanding transaction limit if it is set to a value greater than the programmed outstanding read transaction limit Reset Source: rst_mod_g_rst_n

14.3.1.2.2.18 RATE_LIMITER_RD_TXN_WINDOWS_CNT Register

1 RATE_LIMITER_RD_TXN_WINDOWS_CNT Register (Offset = 328h) [reset = 0h]

Read Transaction Statistics - Window Count

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Table 14-16390. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3328h**

Figure 14-5438. RATE_LIMITER_RD_TXN_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16392. RATE_LIMITER_RD_TXN_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Read transaction window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.2.2.19 RATE_LIMITER_RD_TXN_LIMIT_CNT Register

1 RATE_LIMITER_RD_TXN_LIMIT_CNT Register (Offset = 32Ch) [reset = 0h]

Read Transaction Statistics - number of windows in which the outstanding transaction limit was reached

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Table 14-16393. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 332Ch**

Figure 14-5439. RATE_LIMITER_RD_TXN_LIMIT_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16395. RATE_LIMITER_RD_TXN_LIMIT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the outstanding read transaction limit was reached Reset Source: rst_mod_g_rst_n

14.3.1.2.2.20 RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register

1 RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register (Offset = 330h) [reset = 0h]

Read Transaction Statistics - number of windows in which the statistics threshold was reached

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Table 14-16396. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3330h**

Figure 14-5440. RATE_LIMITER_RD_TXN_THRESHOLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16398. RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the number of outstanding read transactions was greater than or equal to the threshold in RD_TXN_STATS_THRSHLD Reset Source: rst_mod_g_rst_n

14.3.1.2.2.21 RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register

1 RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register (Offset = 334h) [reset = 0h]

Read Transaction Statistics - Cycles at Outstanding Read Transactions Limit

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Table 14-16399. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3334h**

Figure 14-5441. RATE_LIMITER_RD_TXN_LIMIT_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16401. RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with the read transactions outstanding at the programmed limit since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.2.2.22 RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register

1 RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register (Offset = 338h) [reset = 0h]

Read Transaction Statistics - Cycles at the Statistics Threshold

Return to Summary Table

Table 14-16402. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 3338h**

Figure 14-5442. RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16404. RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with read transactions outstanding greater than or equal to the statistics threshold in RD_TXN_STATS_THRSHLD since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.2.2.23 RATE_LIMITER_RD_TXN_MAX Register

1 RATE_LIMITER_RD_TXN_MAX Register (Offset = 33Ch) [reset = 0h]

Read Transaction Statistics - Max Observed Outstanding Read Transactions

Return to Summary Table

Table 14-16405. Instance Table

Instance Name	Physical Address
A53_RS_BW_LIMITER0	**3040 333Ch**

Figure 14-5443. RATE_LIMITER_RD_TXN_MAX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16407. RATE_LIMITER_RD_TXN_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VAL	R	0h	The maximum outstanding read transactions at any point in time, regardless of the programmed limit Reset Source: rst_mod_g_rst_n

14.3.1.3 a53_ws_bw_limiter

a53_ws_bw_limiter

14.3.1.3.1 a53_ws_bw_limiter Summaries

a53_ws_bw_limiter Summaries

Table 14-16408. RATE_LIMITER Registers, Base Address=3040 2000h, Length=4096

Offset	Length	Register Name	A53_WS_BW_LIMITER1 Physical Address
0h	32	RATE_LIMITER_PID	3040 2000h
4h	32	RATE_LIMITER_CTRL	3040 2004h
200h	32	RATE_LIMITER_WR_BW_CIR	3040 2200h
204h	32	RATE_LIMITER_WR_BW_PIR	3040 2204h
208h	32	RATE_LIMITER_WR_BW_BURST_OFFSET	3040 2208h
20Ch	32	RATE_LIMITER_WR_BW_INFO	3040 220Ch
220h	32	RATE_LIMITER_WR_BW_STATS	3040 2220h
224h	32	RATE_LIMITER_WR_BW_STATS_THRSHLD	3040 2224h
228h	32	RATE_LIMITER_WR_BW_WINDOWS_CNT	3040 2228h
22Ch	32	RATE_LIMITER_WR_BW_STATS_CIR	3040 222Ch
230h	32	RATE_LIMITER_WR_BW_STATS_PIR	3040 2230h
234h	32	RATE_LIMITER_WR_BW_THRSHLD_CNT	3040 2234h
238h	32	RATE_LIMITER_WR_BYTES_MAX	3040 2238h
400h	32	RATE_LIMITER_WR_TXN	3040 2400h
40Ch	32	RATE_LIMITER_WR_TXN_INFO	3040 240Ch
420h	32	RATE_LIMITER_WR_TXN_STATS	3040 2420h
424h	32	RATE_LIMITER_WR_TXN_STATS_THRSHLD	3040 2424h
428h	32	RATE_LIMITER_WR_TXN_WINDOWS_CNT	3040 2428h
42Ch	32	RATE_LIMITER_WR_TXN_LIMIT_CNT	3040 242Ch
430h	32	RATE_LIMITER_WR_TXN_THRESHOLD_CNT	3040 2430h
434h	32	RATE_LIMITER_WR_TXN_LIMIT_TOTAL	3040 2434h
438h	32	RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL	3040 2438h
43Ch	32	RATE_LIMITER_WR_TXN_MAX	3040 243Ch

14.3.1.3.2 a53_ws_bw_limiter Registers

a53_ws_bw_limiter Registers

14.3.1.3.2.1 RATE_LIMITER_PID Register

1 RATE_LIMITER_PID Register (Offset = 0h) [reset = 66602900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-16409. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2000h**

Figure 14-5444. RATE_LIMITER_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">660h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">660h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-16411. RATE_LIMITER_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	PID bu identifier Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	660h	PID function identifier Reset Source: rst_mod_g_rst_n
15:11	RTL_VER	R	5h	PID RTL version number Reset Source: rst_mod_g_rst_n
10:8	MAJOR_REV	R	1h	PID Major revision number Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	PID custom Reset Source: rst_mod_g_rst_n
5:0	MINOR_REV	R	0h	PID Minor revision number Reset Source: rst_mod_g_rst_n

14.3.1.3.2.2 RATE_LIMITER_CTRL Register

1 RATE_LIMITER_CTRL Register (Offset = 4h) [reset = 0h]

This register controls the overall behavior of the rate limiter module

Return to Summary Table

Table 14-16412. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2004h**

Figure 14-5445. RATE_LIMITER_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REGION_FILTER_EN	WR_TXN_ENABLE	RD_TXN_ENABLE	WR_BW_ENABLE	RD_BW_ENABLE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-16414. RATE_LIMITER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REGION_FILTER_EN	R/W	0h	Enable the region filter, which will only apply the bandwith and transaction limits to the configured address regions Reset Source: rst_mod_g_rst_n
3	WR_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding write transactions Reset Source: rst_mod_g_rst_n
2	RD_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding read transactions Reset Source: rst_mod_g_rst_n
1	WR_BW_ENABLE	R/W	0h	Enable write bandwidth limiting Reset Source: rst_mod_g_rst_n
0	RD_BW_ENABLE	R/W	0h	Enable read bandwidth limiting Reset Source: rst_mod_g_rst_n

14.3.1.3.2.3 RATE_LIMITER_WR_BW_CIR Register

1 RATE_LIMITER_WR_BW_CIR Register (Offset = 200h) [reset = 0h]

Write Bandwidth Committed Information Rate

Return to Summary Table

Table 14-16415. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2200h**

Figure 14-5446. RATE_LIMITER_WR_BW_CIR Name Register

31	30	29	28	27	26	25	24
CIR							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR							
R/W							
0h							

Table 14-16417. RATE_LIMITER_WR_BW_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR	R/W	0h	Committed Information Rate Reset Source: rst_mod_g_rst_n

14.3.1.3.2.4 RATE_LIMITER_WR_BW_PIR Register

1 RATE_LIMITER_WR_BW_PIR Register (Offset = 204h) [reset = 0h]

Write Bandwidth Peak Information Rate

Return to Summary Table

Table 14-16418. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2204h**

Figure 14-5447. RATE_LIMITER_WR_BW_PIR Name Register

31	30	29	28	27	26	25	24
PIR							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR							
R/W							
0h							

Table 14-16420. RATE_LIMITER_WR_BW_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR	R/W	0h	Peak Information Rate Reset Source: rst_mod_g_rst_n

14.3.1.3.2.5 RATE_LIMITER_WR_BW_BURST_OFFSET Register

1 RATE_LIMITER_WR_BW_BURST_OFFSET Register (Offset = 208h) [reset = 0h]

Write Bandwidth Burst Offset

Return to Summary Table

Table 14-16421. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2208h**

Figure 14-5448. RATE_LIMITER_WR_BW_BURST_OFFSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFFSET							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFSET							
R/W							
0h							

Table 14-16423. RATE_LIMITER_WR_BW_BURST_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFFSET	R/W	0h	Burst Offset - the number of bytes before the Committed Information Rate is applied at startup or after a period of inactivity. Peak Information Rate will still apply Reset Source: rst_mod_g_rst_n

14.3.1.3.2.6 RATE_LIMITER_WR_BW_INFO Register

1 RATE_LIMITER_WR_BW_INFO Register (Offset = 20Ch) [reset = 0h]

Write Bandwidth State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16424. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 220Ch**

Figure 14-5449. RATE_LIMITER_WR_BW_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						COLOR	
NONE						R	
0h						0h	

Table 14-16426. RATE_LIMITER_WR_BW_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	COLOR	R	0h	Write Bandwidth three-color marker output from rategen submodule Reset Source: rst_mod_g_rst_n

14.3.1.3.2.7 RATE_LIMITER_WR_BW_STATS Register

1 RATE_LIMITER_WR_BW_STATS Register (Offset = 220h) [reset = 4000000h]

Write Bandwidth Statistics Control Register

Return to Summary Table

Table 14-16427. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2220h**

Figure 14-5450. RATE_LIMITER_WR_BW_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	22	21	20	19	18	17	16
WINDOW							
R/W							
400h							
15	14	13	12	11	10	9	8
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16429. RATE_LIMITER_WR_BW_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable write bandwidth statistics Reset Source: rst_mod_g_rst_n

14.3.1.3.2.8 RATE_LIMITER_WR_BW_STATS_THRSHLD Register

1 RATE_LIMITER_WR_BW_STATS_THRSHLD Register (Offset = 224h) [reset = 0h]

A statistics threshold separate from the CIR and PIR

Return to Summary Table

Table 14-16430. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2224h**

Figure 14-5451. RATE_LIMITER_WR_BW_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16432. RATE_LIMITER_WR_BW_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	THRESHOLD	R/W	0h	Write bandwidth stats threshold in bytes. Note that this is total bytes, unlike CIR and PIR. CIR and PIR are based on a rolling window, and the statistics threshold is based on a fixed window. This will still take into account DDR bytes used, so can be compared to CIR and PIR directly if the bandwidths are converted via the equations for CIR and PIR. The threshold bandwidth is programmed here as bytes per window Reset Source: rst_mod_g_rst_n

14.3.1.3.2.9 RATE_LIMITER_WR_BW_WINDOWS_CNT Register

1 RATE_LIMITER_WR_BW_WINDOWS_CNT Register (Offset = 228h) [reset = 0h]

Write Bandwidth Statistics - Window Count

Return to Summary Table

Table 14-16433. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2228h**

Figure 14-5452. RATE_LIMITER_WR_BW_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16435. RATE_LIMITER_WR_BW_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Write bandwidth window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.3.2.10 RATE_LIMITER_WR_BW_STATS_CIR Register

1 RATE_LIMITER_WR_BW_STATS_CIR Register (Offset = 22Ch) [reset = 0h]

Write Bandwidth Statistics - CIR Count

Return to Summary Table

Table 14-16436. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 222Ch**

Figure 14-5453. RATE_LIMITER_WR_BW_STATS_CIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16438. RATE_LIMITER_WR_BW_STATS_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write Commit Information Rate occurred. Note that if PIR is set to a lower value than CIR or if the burst offset feature is used, this will also count times that PIR is reached. Reset Source: rst_mod_g_rst_n

14.3.1.3.2.11 RATE_LIMITER_WR_BW_STATS_PIR Register

1 RATE_LIMITER_WR_BW_STATS_PIR Register (Offset = 230h) [reset = 0h]

Write Bandwidth Statistics - PIR Count

Return to Summary Table

Table 14-16439. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2230h**

Figure 14-5454. RATE_LIMITER_WR_BW_STATS_PIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16441. RATE_LIMITER_WR_BW_STATS_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write Peak Information Rate occurred Reset Source: rst_mod_g_rst_n

14.3.1.3.2.12 RATE_LIMITER_WR_BW_THRSHLD_CNT Register

1 RATE_LIMITER_WR_BW_THRSHLD_CNT Register (Offset = 234h) [reset = 0h]

Write Bandwidth Statistics - Threshold Count

Return to Summary Table

Table 14-16442. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2234h**

Figure 14-5455. RATE_LIMITER_WR_BW_THRSHLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16444. RATE_LIMITER_WR_BW_THRSHLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write bytes transferred exceeded the statistics threshold Reset Source: rst_mod_g_rst_n

14.3.1.3.2.13 RATE_LIMITER_WR_BYTES_MAX Register

1 RATE_LIMITER_WR_BYTES_MAX Register (Offset = 238h) [reset = 0h]

The maximum number of bytes seen in a single statitsics window. This can be compared with the window size to calculate the maximum bandwidth seen

Return to Summary Table

Table 14-16445. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2238h**

Figure 14-5456. RATE_LIMITER_WR_BYTES_MAX Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16447. RATE_LIMITER_WR_BYTES_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Max number of bytes in a single window. This number accounts for DDR bandwidth consumed, not simply the accumulation of the packet bytecnt values across a window. The max bandwidth calculation is the total bytes value in this MMR divided by the windows size in WR_BW_STATS.window and multiplied with the interface frequency: WR_BYTES_MAX * FREQ / WR_BW_STATS.window Reset Source: rst_mod_g_rst_n

14.3.1.3.2.14 RATE_LIMITER_WR_TXN Register

1 RATE_LIMITER_WR_TXN Register (Offset = 400h) [reset = 40h]

The maximum number of outstanding write transactions the rate limiter will allow

Return to Summary Table

Table 14-16448. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2400h**

Figure 14-5457. RATE_LIMITER_WR_TXN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIMIT							
R/W							
40h							
7	6	5	4	3	2	1	0
LIMIT							
R/W							
40h							

Table 14-16450. RATE_LIMITER_WR_TXN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	LIMIT	R/W	40h	The maximum number of outstanding write transactions allowed. NOTE: This cannot be programmed to a zero. If a zero is written, it will default to the reset value of 16'd64, as a limit of zero outstanding transactions would hang the interface. Reset Source: rst_mod_g_rst_n

14.3.1.3.2.15 RATE_LIMITER_WR_TXN_INFO Register

1 RATE_LIMITER_WR_TXN_INFO Register (Offset = 40Ch) [reset = 0h]

Write Transaction State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16451. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 240Ch**

Figure 14-5458. RATE_LIMITER_WR_TXN_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	OCC						
NONE	R						
0h	0h						

Table 14-16453. RATE_LIMITER_WR_TXN_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	OCC	R	0h	Write transaction scoreboard occupancy Reset Source: rst_mod_g_rst_n

14.3.1.3.2.16 RATE_LIMITER_WR_TXN_STATS Register

1 RATE_LIMITER_WR_TXN_STATS Register (Offset = 420h) [reset = 4000000h]

Write Transaction Stats Control Register

Return to Summary Table

Table 14-16454. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2420h**

Figure 14-5459. RATE_LIMITER_WR_TXN_STATS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WINDOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">400h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">WINDOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">400h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>OVERFLOW</td><td>CLR</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-16456. RATE_LIMITER_WR_TXN_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable write transaction statistics Reset Source: rst_mod_g_rst_n

14.3.1.3.2.17 RATE_LIMITER_WR_TXN_STATS_THRSHLD Register

1 RATE_LIMITER_WR_TXN_STATS_THRSHLD Register (Offset = 424h) [reset = 0h]

A statistics threshold separate from the write transaction limit

Return to Summary Table

Table 14-16457. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2424h**

Figure 14-5460. RATE_LIMITER_WR_TXN_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16459. RATE_LIMITER_WR_TXN_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THRESHOLD	R/W	0h	Write transaction statistics threshold. The threshold can be set to any value, though it will saturate at the outstanding transaction limit if it is set to a value greater than the programmed outstanding write transaction limit Reset Source: rst_mod_g_rst_n

14.3.1.3.2.18 RATE_LIMITER_WR_TXN_WINDOWS_CNT Register

1 RATE_LIMITER_WR_TXN_WINDOWS_CNT Register (Offset = 428h) [reset = 0h]

Write Transaction Statistics - Window Count

Return to Summary Table

Table 14-16460. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2428h**

Figure 14-5461. RATE_LIMITER_WR_TXN_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16462. RATE_LIMITER_WR_TXN_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Write transaction window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.3.2.19 RATE_LIMITER_WR_TXN_LIMIT_CNT Register

1 RATE_LIMITER_WR_TXN_LIMIT_CNT Register (Offset = 42Ch) [reset = 0h]

Write Transaction Statistics - number of windows in which the outstanding transaction limit was reached

Return to Summary Table

Table 14-16463. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 242Ch**

Figure 14-5462. RATE_LIMITER_WR_TXN_LIMIT_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16465. RATE_LIMITER_WR_TXN_LIMIT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the outstanding write transaction limit was reached Reset Source: rst_mod_g_rst_n

14.3.1.3.2.20 RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register

1 RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register (Offset = 430h) [reset = 0h]

Write Transaction Statistics - number of windows in which the statistics threshold was reached

Return to Summary Table

Table 14-16466. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2430h**

Figure 14-5463. RATE_LIMITER_WR_TXN_THRESHOLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16468. RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the number of outstanding write transactions was greater than or equal to the threshold in WR_TXN_STATS_THRSHLD Reset Source: rst_mod_g_rst_n

14.3.1.3.2.21 RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register

1 RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register (Offset = 434h) [reset = 0h]

Write Transaction Statistics - Cycles at Outstanding Write Transactions Limit

Return to Summary Table

Table 14-16469. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2434h**

Figure 14-5464. RATE_LIMITER_WR_TXN_LIMIT_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16471. RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with the write transactions outstanding at the programmed limit since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.3.2.22 RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register

1 RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register (Offset = 438h) [reset = 0h]

Write Transaction Statistics - Cycles at the Statistics Threshold

Return to Summary Table

Table 14-16472. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 2438h**

Figure 14-5465. RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16474. RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with write transactions outstanding greater than or equal to the statistics threshold in WR_TXN_STATS_THRSHLD since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.1.3.2.23 RATE_LIMITER_WR_TXN_MAX Register

1 RATE_LIMITER_WR_TXN_MAX Register (Offset = 43Ch) [reset = 0h]

Write Transaction Statistics - Max Observed Outstanding Write Transactions

Return to Summary Table

Table 14-16475. Instance Table

Instance Name	Physical Address
A53_WS_BW_LIMITER1	**3040 243Ch**

Figure 14-5466. RATE_LIMITER_WR_TXN_MAX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16477. RATE_LIMITER_WR_TXN_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VAL	R	0h	The maximum outstanding write transactions at any point in time, regardless of the programmed limit Reset Source: rst_mod_g_rst_n

14.3.2 R5FSS Registers

14.3.2.1 R5FSS_COMMON0

R5FSS_COMMON0

14.3.2.1.1 R5FSS_COMMON0 Summaries

R5FSS_COMMON0 Summaries

Table 14-16478. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=3C01 8000h, Length=256

Offset	Length	Register Name	WKUP_R5FSS0_COMMON0 Physical Address
0h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR	3C01 8000h
4h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS	3C01 8004h
8h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS	3C01 8008h
Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS	3C01 800Ch
10h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS	3C01 8010h
14h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS	3C01 8014h
18h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET	3C01 8018h
1Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR	3C01 801Ch
20h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET	3C01 8020h
24h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR	3C01 8024h
40h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID	3C01 8040h

Table 14-16479. ECC_AGGR Registers, Base Address=3F00 D000h, Length=1024

Offset	Length	Register Name	WKUP_R5FSS0_COMMON0 Physical Address
0h	32	ECC_AGGR_REV	3F00 D000h
8h	32	ECC_AGGR_VECTOR	3F00 D008h
Ch	32	ECC_AGGR_STAT	3F00 D00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 D010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 D03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 D040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 D080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 D0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 D13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 D140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 D180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 D1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 D200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 D204h

Table 14-16479. ECC_AGGR Registers, Base Address=3F00 D000h, Length=1024 (continued)

Offset	Length	Register Name	WKUP_R5FSS0_COMMON0 Physical Address
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 D208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 D20Ch

14.3.2.1.2 R5FSS_COMMON0 Registers

R5FSS_COMMON0 Registers

14.3.2.1.2.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register (Offset = 0h) [reset = 0h]

This register contains config bits to enable or disable change requests added to the IP

Return to Summary Table

Table 14-16480. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8000h**

Figure 14-5467. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							COMBINE_TCM_LOCKSTEP_MODE
NONE							R/W
0h							0h

Table 14-16482. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	COMBINE_TCM_LOCKSTEP_MODE	R/W	0h	this bit disables the CR logic to combine TCM in lockstep mode Reset Source: mod_g_rst_n

14.3.2.1.2.2 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 4h) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS single bit error counters

Return to Summary Table

Table 14-16483. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8004h**

Figure 14-5468. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16485. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU0 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU0 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-16485. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.2.1.2.3 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 8h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS single bit error counters

Return to Summary Table

Table 14-16486. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8008h**

Figure 14-5469. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16488. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU1 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU1 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-16488. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.2.1.2.4 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = Ch) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS multi bit error counters

Return to Summary Table

Table 14-16489. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3C01 800Ch

Figure 14-5470. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16491. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-16491. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.2.1.2.5 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = 10h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS multi bit error counters

Return to Summary Table

Table 14-16492. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8010h**

Figure 14-5471. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">EVNT_BUS6</td><td colspan="2">EVNT_BUS5</td><td colspan="2">EVNT_BUS4</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">EVNT_BUS3</td><td colspan="2">EVNT_BUS2</td><td colspan="2">EVNT_BUS1</td><td colspan="2">EVNT_BUS0</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-16494. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-16494. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.2.1.2.6 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register (Offset = 14h) [reset = 0h]

ESM status bits for the PULSAR EVNT BUS

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Table 14-16495. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8014h**

Figure 14-5472. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-16497. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU1 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R	0h	ESM status of CPU1 single bit errors on EVNT BUS Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU0 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R	0h	ESM status of CPU0 single bit errors on EVNT BUS Reset Source: mod_g_rst_n

14.3.2.1.2.7 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register (Offset = 18h) [reset = 0h]

SET the PULSAR EVNT BUS ESM events

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Table 14-16498. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8018h**

Figure 14-5473. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-16500. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.1.2.8 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register (Offset = 1Ch) [reset = 0h]

RESET the PULSAR EVNT BUS ESM events

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Table 14-16501. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 801Ch**

Figure 14-5474. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Name Register

31	30	29	28	27	26	25	24
CPU1_EB6_MULTIPLE_BIT_ERROR	CPU1_EB5_MULTIPLE_BIT_ERROR	CPU1_EB4_MULTIPLE_BIT_ERROR	CPU1_EB3_MULTIPLE_BIT_ERROR	CPU1_EB2_MULTIPLE_BIT_ERROR	CPU1_EB1_MULTIPLE_BIT_ERROR	CPU1_EB0_MULTIPLE_BIT_ERROR	CPU1_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_EB7_SINGLE_BIT_ERROR	CPU1_EB6_SINGLE_BIT_ERROR	CPU1_EB5_SINGLE_BIT_ERROR	CPU1_EB4_SINGLE_BIT_ERROR	CPU1_EB3_SINGLE_BIT_ERROR	CPU1_EB2_SINGLE_BIT_ERROR	CPU1_EB1_SINGLE_BIT_ERROR	CPU1_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_EB6_MULTIPLE_BIT_ERROR	CPU0_EB5_MULTIPLE_BIT_ERROR	CPU0_EB4_MULTIPLE_BIT_ERROR	CPU0_EB3_MULTIPLE_BIT_ERROR	CPU0_EB2_MULTIPLE_BIT_ERROR	CPU0_EB1_MULTIPLE_BIT_ERROR	CPU0_EB0_MULTIPLE_BIT_ERROR	CPU0_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_EB7_SINGLE_BIT_ERROR	CPU0_EB6_SINGLE_BIT_ERROR	CPU0_EB5_SINGLE_BIT_ERROR	CPU0_EB4_SINGLE_BIT_ERROR	CPU0_EB3_SINGLE_BIT_ERROR	CPU0_EB2_SINGLE_BIT_ERROR	CPU0_EB1_SINGLE_BIT_ERROR	CPU0_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16503. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU1_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 31 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
30	CPU1_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 30 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
29	CPU1_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 29 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
28	CPU1_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 28 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
27	CPU1_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 27 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-16503. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CPU1_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 26 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
25	CPU1_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 25 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
24	CPU1_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 24 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
23	CPU1_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 23 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
22	CPU1_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 22 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
21	CPU1_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 21 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
20	CPU1_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 20 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
19	CPU1_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 19 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
18	CPU1_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 18 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
17	CPU1_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 17 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
16	CPU1_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 16 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
15	CPU0_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 15 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
14	CPU0_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 14 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
13	CPU0_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 13 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
12	CPU0_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 12 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
11	CPU0_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 11 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
10	CPU0_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 10 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
9	CPU0_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 9 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
8	CPU0_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 8 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
7	CPU0_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 7 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
6	CPU0_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 6 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-16503. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU0_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 5 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
4	CPU0_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 4 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
3	CPU0_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 3 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
2	CPU0_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 2 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
1	CPU0_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 1 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
0	CPU0_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 0 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

14.3.2.1.2.9 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register (Offset = 20h) [reset = 0h]

MASK the PULSAR EVNT BUS ESM events

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Table 14-16504. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8020h**

Figure 14-5475. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CPU1_MULTIPLE_BIT_ERROR</td><td>CPU1_SINGLE_BIT_ERROR</td><td>CPU0_MULTIPLE_BIT_ERROR</td><td>CPU0_SINGLE_BIT_ERROR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-16506. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.1.2.10 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register (Offset = 24h) [reset = 0h]

UNMASK the PULSAR EVNT BUS ESM events

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Table 14-16507. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8024h**

Figure 14-5476. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-16509. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.1.2.11 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register (Offset = 40h) [reset = 60800200h]

Module ID register

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Table 14-16510. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3C01 8040h**

Figure 14-5477. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6080h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6080h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-16512. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6080h	Module ID field Reset Source: mod_g_rst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release Reset Source: mod_g_rst_n
10:8	REVMAJ	R	2h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: mod_g_rst_n

14.3.2.1.2.12 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-16513. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D000h**

Figure 14-5478. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-16515. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.2.1.2.13 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-16516. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D008h**

Figure 14-5479. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-16518. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.2.1.2.14 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Dh]

Misc Status

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Table 14-16519. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D00Ch**

Figure 14-5480. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Dh							

Table 14-16521. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.2.1.2.15 ECC_AGGR_RESERVED_SVBUS_J Register

1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-16522. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D010h + formula**

Figure 14-5481. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16524. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.2.1.2.16 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-16525. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D03Ch**

Figure 14-5482. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-16527. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.1.2.17 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-16528. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D040h**

Figure 14-5483. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16530. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend

Table 14-16530. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.2.1.2.18 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-16531. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D080h**

Figure 14-5484. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16533. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend

Table 14-16533. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.2.1.2.19 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-16534. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D0C0h**

Figure 14-5485. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16536. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend

Table 14-16536. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.2.1.2.20 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-16537. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D13Ch**

Figure 14-5486. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-16539. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.1.2.21 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-16540. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D140h**

Figure 14-5487. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16542. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend

Table 14-16542. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.2.1.2.22 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-16543. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D180h**

Figure 14-5488. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16545. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend

Table 14-16545. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.2.1.2.23 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-16546. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D1C0h**

Figure 14-5489. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16548. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend

Table 14-16548. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.2.1.2.24 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-16549. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D200h**

Figure 14-5490. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-16551. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.2.1.2.25 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-16552. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D204h**

Figure 14-5491. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-16554. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.2.1.2.26 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-16555. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D208h**

Figure 14-5492. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-16557. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.2.1.2.27 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-16558. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	**3F00 D20Ch**

Figure 14-5493. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-16560. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.2.2 R5FSS_CORE0

R5FSS_CORE0

14.3.2.2.1 R5FSS_CORE0 Summaries

R5FSS_CORE0 Summaries

Table 14-16561. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=0440 0000h, Length=256

Offset	Length	Register Name	MCU_R5FSS0_CORE0 Physical Address
0h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR	0440 0000h
4h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS	0440 0004h
8h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS	0440 0008h
Ch	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS	0440 000Ch
10h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS	0440 0010h
14h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS	0440 0014h
18h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET	0440 0018h
1Ch	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR	0440 001Ch
20h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET	0440 0020h
24h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR	0440 0024h
40h	32	R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID	0440 0040h

Table 14-16562. ECC_AGGR Registers, Base Address=0470 7000h, Length=1024

Offset	Length	Register Name	MCU_R5FSS0_CORE0 Physical Address
0h	32	ECC_AGGR_REV	0470 7000h
8h	32	ECC_AGGR_VECTOR	0470 7008h
Ch	32	ECC_AGGR_STAT	0470 700Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0470 7010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0470 703Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0470 7040h
44h	32	ECC_AGGR_SEC_STATUS_REG1	0470 7044h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0470 7080h
84h	32	ECC_AGGR_SEC_ENABLE_SET_REG1	0470 7084h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0470 70C0h
C4h	32	ECC_AGGR_SEC_ENABLE_CLR_REG1	0470 70C4h
13Ch	32	ECC_AGGR_DED_EOI_REG	0470 713Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0470 7140h
144h	32	ECC_AGGR_DED_STATUS_REG1	0470 7144h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0470 7180h

Table 14-16562. ECC_AGGR Registers, Base Address=0470 7000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_R5FSS0_CORE0 Physical Address
184h	32	ECC_AGGR_DED_ENABLE_SET_REG1	0470 7184h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0470 71C0h
1C4h	32	ECC_AGGR_DED_ENABLE_CLR_REG1	0470 71C4h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0470 7200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0470 7204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0470 7208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0470 720Ch

14.3.2.2.2 R5FSS_CORE0 Registers

R5FSS_CORE0 Registers

14.3.2.2.2.1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register (Offset = 0h) [reset = 0h]

This register contains config bits to enable or disable change requests added to the IP

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Table 14-16563. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0000h**

Figure 14-5494. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							COMBINE_TCM_LOCKSTEP_MODE
NONE							R/W
0h							0h

Table 14-16565. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	COMBINE_TCM_LOCKSTEP_MODE	R/W	0h	this bit disables the CR logic to combine TCM in lockstep mode Reset Source: mod_g_rst_n

14.3.2.2.2.2 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 4h) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS single bit error counters

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Table 14-16566. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0004h**

Figure 14-5495. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16568. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU0 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU0 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-16568. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.2.2.2.3 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 8h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS single bit error counters

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Table 14-16569. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0008h**

Figure 14-5496. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16571. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU1 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU1 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-16571. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.2.2.2.4 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = Ch) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS multi bit error counters

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Table 14-16572. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 000Ch**

Figure 14-5497. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16574. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-16574. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.2.2.2.5 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = 10h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS multi bit error counters

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Table 14-16575. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0010h**

Figure 14-5498. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-16577. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-16577. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.2.2.2.6 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register (Offset = 14h) [reset = 0h]

ESM status bits for the PULSAR EVNT BUS

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Table 14-16578. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0014h**

Figure 14-5499. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-16580. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU1 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R	0h	ESM status of CPU1 single bit errors on EVNT BUS Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU0 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R	0h	ESM status of CPU0 single bit errors on EVNT BUS Reset Source: mod_g_rst_n

14.3.2.2.2.7 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register (Offset = 18h) [reset = 0h]

SET the PULSAR EVNT BUS ESM events

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Table 14-16581. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0018h**

Figure 14-5500. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-16583. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.2.2.8 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register (Offset = 1Ch) [reset = 0h]

RESET the PULSAR EVNT BUS ESM events

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Table 14-16584. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 001Ch**

Figure 14-5501. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Name Register

31	30	29	28	27	26	25	24
CPU1_EB6_MULTIPLE_BIT_ERROR	CPU1_EB5_MULTIPLE_BIT_ERROR	CPU1_EB4_MULTIPLE_BIT_ERROR	CPU1_EB3_MULTIPLE_BIT_ERROR	CPU1_EB2_MULTIPLE_BIT_ERROR	CPU1_EB1_MULTIPLE_BIT_ERROR	CPU1_EB0_MULTIPLE_BIT_ERROR	CPU1_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_EB7_SINGLE_BIT_ERROR	CPU1_EB6_SINGLE_BIT_ERROR	CPU1_EB5_SINGLE_BIT_ERROR	CPU1_EB4_SINGLE_BIT_ERROR	CPU1_EB3_SINGLE_BIT_ERROR	CPU1_EB2_SINGLE_BIT_ERROR	CPU1_EB1_SINGLE_BIT_ERROR	CPU1_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_EB6_MULTIPLE_BIT_ERROR	CPU0_EB5_MULTIPLE_BIT_ERROR	CPU0_EB4_MULTIPLE_BIT_ERROR	CPU0_EB3_MULTIPLE_BIT_ERROR	CPU0_EB2_MULTIPLE_BIT_ERROR	CPU0_EB1_MULTIPLE_BIT_ERROR	CPU0_EB0_MULTIPLE_BIT_ERROR	CPU0_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_EB7_SINGLE_BIT_ERROR	CPU0_EB6_SINGLE_BIT_ERROR	CPU0_EB5_SINGLE_BIT_ERROR	CPU0_EB4_SINGLE_BIT_ERROR	CPU0_EB3_SINGLE_BIT_ERROR	CPU0_EB2_SINGLE_BIT_ERROR	CPU0_EB1_SINGLE_BIT_ERROR	CPU0_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16586. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU1_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 31 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
30	CPU1_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 30 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
29	CPU1_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 29 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
28	CPU1_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 28 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
27	CPU1_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 27 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-16586. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CPU1_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 26 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
25	CPU1_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 25 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
24	CPU1_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 24 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
23	CPU1_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 23 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
22	CPU1_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 22 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
21	CPU1_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 21 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
20	CPU1_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 20 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
19	CPU1_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 19 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
18	CPU1_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 18 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
17	CPU1_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 17 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
16	CPU1_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 16 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
15	CPU0_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 15 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
14	CPU0_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 14 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
13	CPU0_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 13 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
12	CPU0_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 12 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
11	CPU0_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 11 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
10	CPU0_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 10 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
9	CPU0_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 9 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
8	CPU0_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 8 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
7	CPU0_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 7 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
6	CPU0_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 6 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-16586. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU0_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 5 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
4	CPU0_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 4 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
3	CPU0_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 3 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
2	CPU0_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 2 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
1	CPU0_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 1 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
0	CPU0_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 0 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

14.3.2.2.2.9 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register (Offset = 20h) [reset = 0h]

MASK the PULSAR EVNT BUS ESM events

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Table 14-16587. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0020h**

Figure 14-5502. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-16589. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.2.2.10 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register (Offset = 24h) [reset = 0h]

UNMASK the PULSAR EVNT BUS ESM events

Return to Summary Table

Table 14-16590. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0024h**

Figure 14-5503. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-16592. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.2.2.2.11 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register

1 R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register (Offset = 40h) [reset = 60800201h]

Module ID register

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Table 14-16593. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0440 0040h**

Figure 14-5504. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6080h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6080h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-16595. R5FSS_CORE0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6080h	Module ID field Reset Source: mod_g_rst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release Reset Source: mod_g_rst_n
10:8	REVMAJ	R	2h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: mod_g_rst_n

14.3.2.2.2.12 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-16596. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7000h**

Figure 14-5505. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-16598. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.2.2.2.13 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-16599. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7008h**

Figure 14-5506. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-16601. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.2.2.2.14 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 23h]

Misc Status

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Table 14-16602. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 700Ch**

Figure 14-5507. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">23h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">23h</td></tr>
</table>

Table 14-16604. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	23h	Indicates the number of RAMS serviced by the ECC aggregator

14.3.2.2.2.15 ECC_AGGR_RESERVED_SVBUS_J Register

1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-16605. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7010h + formula**

Figure 14-5508. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16607. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.2.2.2.16 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-16608. Instance Table

Instance Name	**Physical Address**
MCU_R5FSS0_CORE0	**0470 703Ch**

Figure 14-5509. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-16610. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.2.2.17 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-16611. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7040h**

Figure 14-5510. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_PEND	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_PEND	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_VBUSM2AXI_EDC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16613. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend

Table 14-16613. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.2.2.2.18 ECC_AGGR_SEC_STATUS_REG1 Register

1 ECC_AGGR_SEC_STATUS_REG1 Register (Offset = 44h) [reset = 0h]

Interrupt Status Register 1

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Table 14-16614. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7044h**

Figure 14-5511. ECC_AGGR_SEC_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_PEND	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_PEND	SCRP_EDC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-16616. ECC_AGGR_SEC_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for scrp_edc_pend

14.3.2.2.2.19 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-16617. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7080h**

Figure 14-5512. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_ENABLE_SET	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_SET	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_VBUSM2AXI_EDC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16619. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend

Table 14-16619. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.2.2.2.20 ECC_AGGR_SEC_ENABLE_SET_REG1 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG1 Register (Offset = 84h) [reset = 0h]

Interrupt Enable Set Register 1

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Table 14-16620. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7084h**

Figure 14-5513. ECC_AGGR_SEC_ENABLE_SET_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_SET	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_SET	SCRP_EDC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-16622. ECC_AGGR_SEC_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for scrp_edc_pend

14.3.2.2.2.21 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-16623. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 70C0h**

Figure 14-5514. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_ENABLE_CLR	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_CLR	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_VBUSM2AXI_EDC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16625. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend

Table 14-16625. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.2.2.2.22 ECC_AGGR_SEC_ENABLE_CLR_REG1 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG1 Register (Offset = C4h) [reset = 0h]

Interrupt Enable Clear Register 1

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Table 14-16626. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 70C4h**

Figure 14-5515. ECC_AGGR_SEC_ENABLE_CLR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_CLR	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	SCRP_EDC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-16628. ECC_AGGR_SEC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for scrp_edc_pend

14.3.2.2.2.23 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-16629. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 713Ch**

Figure 14-5516. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-16631. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.2.2.24 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-16632. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7140h**

Figure 14-5517. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_PEND	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_PEND	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_VBUSM2AXI_EDC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16634. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend

Table 14-16634. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.2.2.2.25 ECC_AGGR_DED_STATUS_REG1 Register

1 ECC_AGGR_DED_STATUS_REG1 Register (Offset = 144h) [reset = 0h]

Interrupt Status Register 1

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Table 14-16635. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7144h**

Figure 14-5518. ECC_AGGR_DED_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_PEND	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_PEND	SCRP_EDC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-16637. ECC_AGGR_DED_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for scrp_edc_pend

14.3.2.2.2.26 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-16638. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7180h**

Figure 14-5519. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_ENABLE_SET	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_SET	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_VBUSM2AXI_EDC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16640. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend

Table 14-16640. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.2.2.2.27 ECC_AGGR_DED_ENABLE_SET_REG1 Register

1 ECC_AGGR_DED_ENABLE_SET_REG1 Register (Offset = 184h) [reset = 0h]

Interrupt Enable Set Register 1

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Table 14-16641. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7184h**

Figure 14-5520. ECC_AGGR_DED_ENABLE_SET_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_SET	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_SET	SCRP_EDC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-16643. ECC_AGGR_DED_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for scrp_edc_pend

14.3.2.2.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-16644. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 71C0h**

Figure 14-5521. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
CPU0_AHB2VBUSP_EDC_ENABLE_CLR	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_CLR	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_VBUSM2AXI_EDC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16646. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU0_AHB2VBUSP_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ahb2vbusp_edc_pend
30	CPU0_AXI2VBUSM_MEM_MST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_edc_ctrl_busecc_pend
29	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
28	CPU0_VBUSM2AXI_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_vbusm2axi_edc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend

Table 14-16646. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.2.2.2.29 ECC_AGGR_DED_ENABLE_CLR_REG1 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG1 Register (Offset = 1C4h) [reset = 0h]

Interrupt Enable Clear Register 1

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Table 14-16647. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 71C4h**

Figure 14-5522. ECC_AGGR_DED_ENABLE_CLR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ECCAGG_ENABLE_CLR	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	SCRP_EDC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-16649. ECC_AGGR_DED_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
1	PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_PULSAR_ULS_CPU0_CFG_SCRP_P_SCR1_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_pulsar_uls_cpu0_cfg_scrp_p_scr1_scr_edc_ctrl_busecc_pend
0	SCRP_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for scrp_edc_pend

14.3.2.2.2.30 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-16650. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7200h**

Figure 14-5523. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-16652. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.2.2.2.31 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-16653. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7204h**

Figure 14-5524. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-16655. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.2.2.2.32 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-16656. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 7208h**

Figure 14-5525. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-16658. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.2.2.2.33 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-16659. Instance Table

Instance Name	Physical Address
MCU_R5FSS0_CORE0	**0470 720Ch**

Figure 14-5526. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-16661. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.3 R5FSS_VIM Registers

14.3.3.1 R5FSS_VIM Registers

Table 14-11137 lists the memory-mapped registers for the R5FSS_VIM module. All register offset addresses not listed in Table 14-11137 should be considered as reserved locations and the register contents should not be modified.

Table 14-16662. R5FSS_VIM Instances

Instance	WKUP Base Address	MCU Base Address
R5FSS_VIC_CFG	2FFF 0000h(1)	07FF 0000h(1)

(1) R5FSS0 private memory-mapped register space. This region is only accessible by its associated R5F core; it is not accessible by any other SoC initiator.

Table 14-16663. R5FSS_VIM Registers

Offset	Acronym	Register Name	WKUP_R5FSS_VIC_CFG Physical Address	MCU_R5FSS_VIC_CFG Physical Address
0h	R5FSS_VIM_PID	Revision register	2FFF 0000h	07FF 0000h
4h	R5FSS_VIM_INFO	Info register	2FFF 0004h	07FF 0004h
8h	R5FSS_VIM_PRIIRQ	Prioritized IRQ register	2FFF 0008h	07FF 0008h
Ch	R5FSS_VIM_PRIFIQ	Prioritized FIQ register	2FFF 000Ch	07FF 000Ch
10h	R5FSS_VIM_IRQGSTS	IRQ group status register	2FFF 0010h	07FF 0010h
14h	R5FSS_VIM_FIQGSTS	FIQ group status register	2FFF 0014h	07FF 0014h
18h	R5FSS_VIM_IRQVEC	IRQ vector address register	2FFF 0018h	07FF 0018h
1Ch	R5FSS_VIM_FIQVEC	FIQ vector address register	2FFF 001Ch	07FF 001Ch
20h	R5FSS_VIM_ACTIRQ	Active IRQ register	2FFF 0020h	07FF 0020h
24h	R5FSS_VIM_ACTFIQ	Active FIQ register	2FFF 0024h	07FF 0024h
30h	R5FSS_VIM_DEDVEC	DED vector address register	2FFF 0030h	07FF 0030h
400h + formula	R5FSS_VIM_RAW_j	Raw status/set register	2FFF 0400h + formula	07FF 0400h + formula
404h + formula	R5FSS_VIM_STS_j	Interrupt enable status/clear register	2FFF 0404h + formula	07FF 0404h + formula
408h + formula	R5FSS_VIM_INTR_EN_SET_j	Interrupt enable set register	2FFF 0408h + formula	07FF 0408h + formula
40Ch + formula	R5FSS_VIM_INTR_EN_CLR_j	Interrupt enabled clear register	2FFF 040Ch + formula	07FF 040Ch + formula
410h + formula	R5FSS_VIM_IRQSTS_j	IRQ interrupt enable status/clear register	2FFF 0410h + formula	07FF 0410h + formula
414h + formula	R5FSS_VIM_FIQSTS_j	FIQ interrupt enable status/clear register	2FFF 0414h + formula	07FF 0414h + formula
418h + formula	R5FSS_VIM_INTMAP_j	Interrupt map register	2FFF 0418h + formula	07FF 0418h + formula
41Ch + formula	R5FSS_VIM_INTTYPE_j	Interrupt type register	2FFF 041Ch + formula	07FF 041Ch + formula
1000h + formula	R5FSS_VIM_PRI_INT_j	Interrupt priority register	2FFF 1000h + formula	07FF 1000h + formula
2000h + formula	R5FSS_VIM_VEC_INT_j	Interrupt vector register	2FFF 2000h + formula	07FF 2000h + formula

1 R5FSS_VIM_PID Register (Offset = 0h) [reset = 60900001h]

R5FSS_VIM_PID is shown in Figure 14-5527 and described in Table 14-11139.

Return to Summary Table.

This register contains the major and minor revisions for the module.

Table 14-16664. R5FSS_VIM_PID Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0000h	07FF 0000h

Figure 14-5527. R5FSS_VIM_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-60900001h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16666. R5FSS_VIM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	60900001h	TI internal data. Identifies revision of peripheral.

2 R5FSS_VIM_INFO Register (Offset = 4h) [reset = 200h]

R5FSS_VIM_INFO is shown in Figure 14-5528 and described in Table 14-11141.

Return to Summary Table.

This contains information about the configuration of the R5FSS_VIM.

Table 14-16667. R5FSS_VIM_INFO Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0004h	07FF 0004h

Figure 14-5528. R5FSS_VIM_INFO Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="21">RESERVED</td><td colspan="11">INTERRUPTS</td></tr>
<tr><td colspan="21">R-0h</td><td colspan="11">R-200h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16669. R5FSS_VIM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
10-0	INTERRUPTS	R	200h	Indicates the number of interrupts supported by the VIM.

3 R5FSS_VIM_PRIIRQ Register (Offset = 8h) [reset = 0h]

R5FSS_VIM_PRIIRQ is shown in Figure 14-5529 and described in Table 14-11143.

Return to Summary Table.

This register contains the number of the highest priority pending IRQ.

Table 14-16670. R5FSS_VIM_PRIIRQ Instances

Instance	WKUP Physical Address	WKUP Physical Address
R5FSS_VIC_CFG	2FFF 0008h	07FF 0008h

Figure 14-5529. R5FSS_VIM_PRIIRQ Register

31	30	29	28	27	26	25	24
VALID	RESERVED						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED				PRI			
R-0h				R-0h			
15	14	13	12	11	10	9	8
RESERVED						NUM	
R-0h						R-0h	
7	6	5	4	3	2	1	0
NUM							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16672. R5FSS_VIM_PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. 0h = NUM field is invalid (no pending IRQ interrupts) 1h = NUM field is valid (pending IRQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the pending IRQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-16672. R5FSS_VIM_PRIIRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the pending IRQ interrupt with the highest priority. 0h = Interrupt 0 1h = Interrupt 1 ... 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

4 R5FSS_VIM_PRIFIQ Register (Offset = Ch) [reset = 0h]

R5FSS_VIM_PRIFIQ is shown in Figure 14-5530 and described in Table 14-11145.

Return to Summary Table.

This register contains the number of the highest priority pending FIQ.

Table 14-16673. R5FSS_VIM_PRIFIQ Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 000Ch	07FF 000Ch

Figure 14-5530. R5FSS_VIM_PRIFIQ Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">NUM</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16675. R5FSS_VIM_PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. 0h = NUM field is invalid (no pending FIQ interrupts) 1h = NUM field is valid (pending FIQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the pending FIQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-16675. R5FSS_VIM_PRIFIQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the pending FIQ interrupt with the highest priority. 0h = Interrupt 0 1h = Interrupt 1 ... 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

5 R5FSS_VIM_IRQGSTS Register (Offset = 10h) [reset = 0h]

R5FSS_VIM_IRQGSTS is shown in Figure 14-5531 and described in Table 14-11147.

Return to Summary Table.

This register indicates which groups of interrupts have pending, unmasked IRQ interrupts.

Table 14-16676. R5FSS_VIM_IRQGSTS Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0010h	07FF 0010h

Figure 14-5531. R5FSS_VIM_IRQGSTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16678. R5FSS_VIM_IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	This field indicates that one or more interrupts in group M are mapped to IRQ, unmasked, and pending. Bit 0 corresponds to group 0, bit 1 corresponds to group 1, etc. The interrupts associated with each group are [(M*32)+31:M*32]

6 R5FSS_VIM_FIQGSTS Register (Offset = 14h) [reset = 0h]

R5FSS_VIM_FIQGSTS is shown in Figure 14-5532 and described in Table 14-11149.

Return to Summary Table.

This register indicates which groups of interrupts have pending, unmasked FIQ interrupts.

Table 14-16679. R5FSS_VIM_FIQGSTS Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0014h	07FF 0014h

Figure 14-5532. R5FSS_VIM_FIQGSTS Register

31-0
STS
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16681. R5FSS_VIM_FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	This field indicates that one or more interrupts in group M are mapped to FIQ, unmasked, and pending. Bit 0 corresponds to group 0, bit 1 corresponds to group 1, etc. The interrupts associated with each group are [(M*32)+31:M*32]

7 R5FSS_VIM_IRQVEC Register (Offset = 18h) [reset = 0h]

R5FSS_VIM_IRQVEC is shown in Figure 14-5533 and described in Table 14-11151.

Return to Summary Table.

This register contains the 32-bit interrupt vector address of the currently pending IRQ.

Table 14-16682. R5FSS_VIM_IRQVEC Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0018h	07FF 0018h

Figure 14-5533. R5FSS_VIM_IRQVEC Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">ADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="30">R-0h</td><td colspan="2">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16684. R5FSS_VIM_IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (addresses must be 32-bit aligned) of the currently pending highest priority IRQ (as indicated by the R5FSS_VIM_PRIIRQ[9-0] NUM field). Reading this register returns the interrupt vector address of the pending IRQ with the highest priority. It also has the following effects: - Mask all IRQ interrupts of an equivalent or lower priority - De-asserts the IRQn signal - De-asserts the coreN_IRQADDRV signal (if set) - Loads R5FSS_VIM_ACTIRQ Writing any value to this register will not alter its contents, but will have the following effect: - Remove the mask on all IRQ priorities This field is only valid if the R5FSS_VIM_PRIIRQ[31] VALID flag is set.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

8 R5FSS_VIM_FIQVEC Register (Offset = 1Ch) [reset = 0h]

R5FSS_VIM_FIQVEC is shown in Figure 14-5534 and described in Table 14-11153.

Return to Summary Table.

This register contains the 32-bit interrupt vector address of the currently pending FIQ.

Table 14-16685. R5FSS_VIM_FIQVEC Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 001Ch	07FF 001Ch

Figure 14-5534. R5FSS_VIM_FIQVEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	
R-0h																														R-0h	

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16687. R5FSS_VIM_FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (addresses must be 32-bit aligned) of the currently pending highest priority FIQ (as indicated by the R5FSS_VIM_PRIFIQ[9-0] NUM field). Reading this register returns the interrupt vector address of the pending FIQ with the highest priority. It also has the following effects: - Mask all FIQ interrupts of an equivalent or lower priority - De-asserts the FIQn signal - Loads R5FSS_VIM_ACTFIQ Writing any value to this register will not alter its contents, but will have the following effect: - Remove the mask on all FIQ priorities This field is only valid if the R5FSS_VIM_PRIFIQ[31] VALID flag is set.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

9 R5FSS_VIM_ACTIRQ Register (Offset = 20h) [reset = 0h]

R5FSS_VIM_ACTIRQ is shown in Figure 14-5535 and described in Table 14-11155.

Return to Summary Table.

This register contains the number of the active IRQ.

Table 14-16688. R5FSS_VIM_ACTIRQ Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0020h	07FF 0020h

Figure 14-5535. R5FSS_VIM_ACTIRQ Register

31	30	29	28	27	26	25	24
VALID	RESERVED						
R-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED				PRI			
R-0h				R-0h			

15	14	13	12	11	10	9	8
RESERVED						NUM	
R-0h						R-0h	

7	6	5	4	3	2	1	0
NUM							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16690. R5FSS_VIM_ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. This field is set whenever the R5FSS_VIM_IRQVEC is read. It is cleared whenever the R5FSS_VIM_IRQVEC is written. 0h = NUM field is invalid (no active IRQ interrupts) 1h = NUM field is valid (active IRQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the active IRQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-16690. R5FSS_VIM_ACTIRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the active IRQ interrupt. This field is loaded with the value from the R5FSS_VIM_PRIIRQ whenever the R5FSS_VIM_IRQVEC is read. 0h = Interrupt 0 1h = Interrupt 1 … 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

10 R5FSS_VIM_ACTFIQ Register (Offset = 24h) [reset = 0h]

R5FSS_VIM_ACTFIQ is shown in Figure 14-5536 and described in Table 14-11157.

Return to Summary Table.

This register contains the number of the active FIQ.

Table 14-16691. R5FSS_VIM_ACTFIQ Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0024h	07FF 0024h

Figure 14-5536. R5FSS_VIM_ACTFIQ Register

31	30	29	28	27	26	25	24
VALID	RESERVED						
R-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED				PRI			
R-0h				R-0h			

15	14	13	12	11	10	9	8
RESERVED						NUM	
R-0h						R-0h	

7	6	5	4	3	2	1	0
NUM							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16693. R5FSS_VIM_ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. This field is set whenever the R5FSS_VIM_PRIFIQ is read. It is cleared whenever the R5FSS_VIM_FIQVEC is written. 0h = NUM field is invalid (no active FIQ interrupts) 1h = NUM field is valid (active FIQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the active FIQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-16693. R5FSS_VIM_ACTFIQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the active FIQ interrupt. This field is loaded with the value from the R5FSS_VIM_PRIFIQ whenever the R5FSS_VIM_FIQVEC is read. 0h = Interrupt 0 1h = Interrupt 1 … 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

11 R5FSS_VIM_DEDVEC Register (Offset = 30h) [reset = 0h]

R5FSS_VIM_DEDVEC is shown in Figure 14-5537 and described in Table 14-11159.

Return to Summary Table.

This register contains the 32-bit interrupt vector address to be used as a default in case of a DED error in any of the vectors.

Table 14-16694. R5FSS_VIM_DEDVEC Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0030h	07FF 0030h

Figure 14-5537. R5FSS_VIM_DEDVEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	
R/W-0h																														R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-16696. R5FSS_VIM_DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (the address must be 32-bit aligned) of an interrupt to be used if an uncorrectable double-bit error (DED) is detected in any of the interrupt vector addresses. If there is a DED, both the R5FSS_VIM_IRQVEC and R5FSS_VIM_FIQVEC registers (along with the VECADDR output) will be populated with the value in this field instead of their normal vector. - ECC Aggregator will indicate where there was a DED. Software may go correct that one location. - Software may keep an ISR at the DED vector which corrects the vectors or otherwise deals with the scenario. - This mechanism is provided because there is no way to indicate on the coreN_IRQADDR to the CPU that the vector is invalid, and it is undesirable to have the CPU jump to a random address.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

12 R5FSS_VIM_RAW_j Register (Offset = 400h + formula) [reset = 0h]

R5FSS_VIM_RAW_j is shown in Figure 14-5538 and described in Table 14-11161.

Return to Summary Table.

This register indicates the raw status of the events in group M.

Offset = 400h + (j * 20h); where j = 0h to Fh.

Table 14-16697. R5FSS_VIM_RAW_j Instances

Instance	**WKUP Physical Address**	**MCU Physical Address**
R5FSS_VIC_CFG	2FFF 0400h + formula	07FF 0400h + formula

Figure 14-5538. R5FSS_VIM_RAW_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-16699. R5FSS_VIM_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R/W1S	0h	This is the raw status of the events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive Read 1h = Active/pending Write 0h = No effect Write 1h = Set to interrupt raw status

13 R5FSS_VIM_STS_j Register (Offset = 404h + formula) [reset = 0h]

R5FSS_VIM_STS_j is shown in Figure 14-5539 and described in Table 14-11163.

Return to Summary Table.

This register indicates the masked status of the events in group M.

Offset = 404h + (j * 20h); where j = 0h to Fh.

Table 14-16700. R5FSS_VIM_STS_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0404h + formula	07FF 0404h + formula

Figure 14-5539. R5FSS_VIM_STS_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-16702. R5FSS_VIM_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive or disabled Read 1h = Active/pending and enabled Write 0h = No effect Write 1h = Clear interrupt raw status

14 R5FSS_VIM_INTR_EN_SET_j Register (Offset = 408h + formula) [reset = 0h]

R5FSS_VIM_INTR_EN_SET_j is shown in Figure 14-5540 and described in Table 14-11165.

Return to Summary Table.

This register is used to enable the mask for the events in group M.

Offset = 408h + (j * 20h); where j = 0h to Fh.

Table 14-16703. R5FSS_VIM_INTR_EN_SET_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0408h + formula	07FF 0408h + formula

Figure 14-5540. R5FSS_VIM_INTR_EN_SET_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W1S-0h</td></tr>
</table>

LEGEND: R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-16705. R5FSS_VIM_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1S	0h	This field is used to enable the mask of events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Disabled Read 1h = Enabled Write 0h = No effect Write 1h = Set enable

15 R5FSS_VIM_INTR_EN_CLR_j Register (Offset = 40Ch + formula) [reset = 0h]

R5FSS_VIM_INTR_EN_CLR_j is shown in Figure 14-5541 and described in Table 14-11167.

Return to Summary Table.

This register is used to disable the mask for the events in group M.

Offset = 40Ch + (j * 20h); where j = 0h to Fh.

Table 14-16706. R5FSS_VIM_INTR_EN_CLR_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 040Ch + formula	07FF 040Ch + formula

Figure 14-5541. R5FSS_VIM_INTR_EN_CLR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-16708. R5FSS_VIM_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This field is used to disable the mask of events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Disabled Read 1h = Enabled Read 0h = No effect Read 1h = Clear enable

16 R5FSS_VIM_IRQSTS_j Register (Offset = 410h + formula) [reset = 0h]

R5FSS_VIM_IRQSTS_j is shown in Figure 14-5542 and described in Table 14-11169.

Return to Summary Table.

This register indicates the masked status of the events in Group M that are also mapped as IRQs.

Offset = 410h + (j * 20h); where j = 0h to Fh.

Table 14-16709. R5FSS_VIM_IRQSTS_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0410h + formula	07FF 0410h + formula

Figure 14-5542. R5FSS_VIM_IRQSTS_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-16711. R5FSS_VIM_IRQSTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M that are mapped to IRQ. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive, disabled, or not an IRQ Read 1h = Active/pending, enabled, and IRQ Write 0h = No effect Write 1h = Clear interrupt raw status (if IRQ)

17 R5FSS_VIM_FIQSTS_j Register (Offset = 414h + formula) [reset = 0h]

R5FSS_VIM_FIQSTS_j is shown in Figure 14-5543 and described in Table 14-11171.

Return to Summary Table.

This register indicates the masked status of the events in group M that are also mapped as FIQs.

Offset = 414h + (j * 20h); where j = 0h to Fh.

Table 14-16712. R5FSS_VIM_FIQSTS_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0414h + formula	07FF 0414h + formula

Figure 14-5543. R5FSS_VIM_FIQSTS_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W1C-0h</td></tr>
</table>

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-16714. R5FSS_VIM_FIQSTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M that are mapped to FIQ. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive, disabled, or not an FIQ Read 1h = Active/pending, enabled, and FIQ Write 0h = No effect Write 1h = Clear interrupt raw status (if FIQ)

18 R5FSS_VIM_INTMAP_j Register (Offset = 418h + formula) [reset = 0h]

R5FSS_VIM_INTMAP_j is shown in Figure 14-5544 and described in Table 14-11173.

Return to Summary Table.

This register is used to map interrupts as IRQ or FIQ.

Offset = 418h + (j * 20h); where j = 0h to Fh.

Table 14-16715. R5FSS_VIM_INTMAP_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 0418h + formula	07FF 0418h + formula

Figure 14-5544. R5FSS_VIM_INTMAP_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-16717. R5FSS_VIM_INTMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). 0h = IRQ interrupt (default) 1h = FIQ interrupt

19 R5FSS_VIM_INTTYPE_j Register (Offset = 41Ch + formula) [reset = 0h]

R5FSS_VIM_INTTYPE_j is shown in Figure 14-5545 and described in Table 14-11175.

Return to Summary Table.

This register indicates whether an interrupt is a pulse or level source.

Offset = 41Ch + (j * 20h); where j = 0h to Fh.

Table 14-16718. R5FSS_VIM_INTTYPE_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 041Ch + formula	07FF 041Ch + formula

Figure 14-5545. R5FSS_VIM_INTTYPE_j Register

31–0
MSK
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-16720. R5FSS_VIM_INTTYPE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). 0h = Level (default) 1h = Pulse Note: This is only informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level.

20 R5FSS_VIM_PRI_INT_j Register (Offset = 1000h + formula) [reset = 0h]

R5FSS_VIM_PRI_INT_j is shown in Figure 14-5546 and described in Table 14-11177.

Return to Summary Table.

This register is used to set the priority of interrupt Q.

Offset = 1000h + (j * 4h); where j = 0h to FFh.

Table 14-16721. R5FSS_VIM_PRI_INT_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 1000h + formula	07FF 1000h + formula

Figure 14-5546. R5FSS_VIM_PRI_INT_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="28">RESERVED</td><td colspan="4">VAL</td></tr>
<tr><td colspan="28">R-0h</td><td colspan="4">R/W-Fh</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-16723. R5FSS_VIM_PRI_INT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
3-0	VAL	R/W	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration. 0h = Highest priority … Fh = Lowest priority (default)

21 R5FSS_VIM_VEC_INT_j Register (Offset = 2000h + formula) [reset = 0h]

R5FSS_VIM_VEC_INT_j is shown in Figure 14-5547 and described in Table 14-11179.

Return to Summary Table.

This register contains the vector address associated with interrupt Q.

Offset = 2000h + (j * 4h); where j = 0h to FFh.

Table 14-16724. R5FSS_VIM_VEC_INT_j Instances

Instance	WKUP Physical Address	MCU Physical Address
R5FSS_VIC_CFG	2FFF 2000h + formula	07FF 2000h + formula

Figure 14-5547. R5FSS_VIM_VEC_INT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																														RESERVED	
R/W-0h																														R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-16726. R5FSS_VIM_VEC_INT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	VAL	R/W	0h	These are the upper 30 bits of the 32-bit vector address associated with interrupt Q. It is the address that will be reflected in the R5FSS_VIM_IRQVEC or R5FSS_VIM_FIQVEC and the VECADDR output when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new vector address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

14.3.4 JPEG Encoder (E5010) Registers

14.3.4.1 jpgenc_rs_bw_limiter

jpgenc_rs_bw_limiter

14.3.4.1.1 jpgenc_rs_bw_limiter Summaries

jpgenc_rs_bw_limiter Summaries

Table 14-16727. RATE_LIMITER Registers, Base Address=3040 4000h, Length=4096

Offset	Length	Register Name	JPGENC_RS_BW_LIMITER4 Physical Address
0h	32	RATE_LIMITER_PID	3040 4000h
4h	32	RATE_LIMITER_CTRL	3040 4004h
100h	32	RATE_LIMITER_RD_BW_CIR	3040 4100h
104h	32	RATE_LIMITER_RD_BW_PIR	3040 4104h
108h	32	RATE_LIMITER_RD_BW_BURST_OFFSET	3040 4108h
10Ch	32	RATE_LIMITER_RD_BW_INFO	3040 410Ch
120h	32	RATE_LIMITER_RD_BW_STATS	3040 4120h
124h	32	RATE_LIMITER_RD_BW_STATS_THRSHLD	3040 4124h
128h	32	RATE_LIMITER_RD_BW_WINDOWS_CNT	3040 4128h
12Ch	32	RATE_LIMITER_RD_BW_STATS_CIR	3040 412Ch
130h	32	RATE_LIMITER_RD_BW_STATS_PIR	3040 4130h
134h	32	RATE_LIMITER_RD_BW_THRSHLD_CNT	3040 4134h
138h	32	RATE_LIMITER_RD_BYTES_MAX	3040 4138h
300h	32	RATE_LIMITER_RD_TXN	3040 4300h
30Ch	32	RATE_LIMITER_RD_TXN_INFO	3040 430Ch
320h	32	RATE_LIMITER_RD_TXN_STATS	3040 4320h
324h	32	RATE_LIMITER_RD_TXN_STATS_THRSHLD	3040 4324h
328h	32	RATE_LIMITER_RD_TXN_WINDOWS_CNT	3040 4328h
32Ch	32	RATE_LIMITER_RD_TXN_LIMIT_CNT	3040 432Ch
330h	32	RATE_LIMITER_RD_TXN_THRESHOLD_CNT	3040 4330h
334h	32	RATE_LIMITER_RD_TXN_LIMIT_TOTAL	3040 4334h
338h	32	RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL	3040 4338h
33Ch	32	RATE_LIMITER_RD_TXN_MAX	3040 433Ch

14.3.4.1.2 jpgenc_rs_bw_limiter Registers

jpgenc_rs_bw_limiter Registers

14.3.4.1.2.1 RATE_LIMITER_PID Register

1 RATE_LIMITER_PID Register (Offset = 0h) [reset = 66602900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-16728. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	3040 4000h

Figure 14-5548. RATE_LIMITER_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		660h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
660h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_REV		
R					R		
5h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-16730. RATE_LIMITER_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	PID bu identifier Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	660h	PID function identifier Reset Source: rst_mod_g_rst_n
15:11	RTL_VER	R	5h	PID RTL version number Reset Source: rst_mod_g_rst_n
10:8	MAJOR_REV	R	1h	PID Major revision number Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	PID custom Reset Source: rst_mod_g_rst_n
5:0	MINOR_REV	R	0h	PID Minor revision number Reset Source: rst_mod_g_rst_n

14.3.4.1.2.2 RATE_LIMITER_CTRL Register

1 RATE_LIMITER_CTRL Register (Offset = 4h) [reset = 0h]

This register controls the overall behavior of the rate limiter module

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Table 14-16731. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4004h**

Figure 14-5549. RATE_LIMITER_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>REGION_FILTER_EN</td><td>WR_TXN_ENABLE</td><td>RD_TXN_ENABLE</td><td>WR_BW_ENABLE</td><td>RD_BW_ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-16733. RATE_LIMITER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REGION_FILTER_EN	R/W	0h	Enable the region filter, which will only apply the bandwith and transaction limits to the configured address regions Reset Source: rst_mod_g_rst_n
3	WR_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding write transactions Reset Source: rst_mod_g_rst_n
2	RD_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding read transactions Reset Source: rst_mod_g_rst_n
1	WR_BW_ENABLE	R/W	0h	Enable write bandwidth limiting Reset Source: rst_mod_g_rst_n
0	RD_BW_ENABLE	R/W	0h	Enable read bandwidth limiting Reset Source: rst_mod_g_rst_n

14.3.4.1.2.3 RATE_LIMITER_RD_BW_CIR Register

1 RATE_LIMITER_RD_BW_CIR Register (Offset = 100h) [reset = 0h]

Read Bandwidth Committed Information Rate

Return to Summary Table

Table 14-16734. Instance Table

Instance Name	**Physical Address**
JPGENC_RS_BW_LIMITER4	**3040 4100h**

Figure 14-5550. RATE_LIMITER_RD_BW_CIR Name Register

31	30	29	28	27	26	25	24
CIR							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR							
R/W							
0h							

Table 14-16736. RATE_LIMITER_RD_BW_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR	R/W	0h	Committed Information Rate Reset Source: rst_mod_g_rst_n

14.3.4.1.2.4 RATE_LIMITER_RD_BW_PIR Register

1 RATE_LIMITER_RD_BW_PIR Register (Offset = 104h) [reset = 0h]

Read Bandwidth Peak Information Rate

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Table 14-16737. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4104h**

Figure 14-5551. RATE_LIMITER_RD_BW_PIR Name Register

31	30	29	28	27	26	25	24
PIR							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR							
R/W							
0h							

Table 14-16739. RATE_LIMITER_RD_BW_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR	R/W	0h	Peak Information Rate Reset Source: rst_mod_g_rst_n

14.3.4.1.2.5 RATE_LIMITER_RD_BW_BURST_OFFSET Register

1 RATE_LIMITER_RD_BW_BURST_OFFSET Register (Offset = 108h) [reset = 0h]

Read Bandwidth Burst Offset

Return to Summary Table

Table 14-16740. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4108h**

Figure 14-5552. RATE_LIMITER_RD_BW_BURST_OFFSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFFSET							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFSET							
R/W							
0h							

Table 14-16742. RATE_LIMITER_RD_BW_BURST_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFFSET	R/W	0h	Burst Offset - the number of bytes before the Committed Information Rate is applied at startup or after a period of inactivity. Peak Information Rate will still apply Reset Source: rst_mod_g_rst_n

14.3.4.1.2.6 RATE_LIMITER_RD_BW_INFO Register

1 RATE_LIMITER_RD_BW_INFO Register (Offset = 10Ch) [reset = 0h]

Read Bandwidth State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16743. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	3040 410Ch

Figure 14-5553. RATE_LIMITER_RD_BW_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						COLOR	
NONE						R	
0h						0h	

Table 14-16745. RATE_LIMITER_RD_BW_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	COLOR	R	0h	Read Bandwidth three-color marker output from rategen submodule Reset Source: rst_mod_g_rst_n

14.3.4.1.2.7 RATE_LIMITER_RD_BW_STATS Register

1 RATE_LIMITER_RD_BW_STATS Register (Offset = 120h) [reset = 4000000h]

Read Bandwidth Statistics Control Register

Return to Summary Table

Table 14-16746. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4120h**

Figure 14-5554. RATE_LIMITER_RD_BW_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	22	21	20	19	18	17	16
WINDOW							
R/W							
400h							
15	14	13	12	11	10	9	8
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16748. RATE_LIMITER_RD_BW_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable read bandwidth statistics Reset Source: rst_mod_g_rst_n

14.3.4.1.2.8 RATE_LIMITER_RD_BW_STATS_THRSHLD Register

1 RATE_LIMITER_RD_BW_STATS_THRSHLD Register (Offset = 124h) [reset = 0h]

A statistics threshold separate from the CIR and PIR

Return to Summary Table

Table 14-16749. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4124h**

Figure 14-5555. RATE_LIMITER_RD_BW_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16751. RATE_LIMITER_RD_BW_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	THRESHOLD	R/W	0h	Read bandwidth stats threshold in bytes. Note that this is total bytes, unlike CIR and PIR. CIR and PIR are based on a rolling window, and the statistics threshold is based on a fixed window. This will still take into account DDR bytes used, so can be compared to CIR and PIR directly if the bandwidths are converted via the equations for CIR and PIR. The threshold bandwidth is programmed here as bytes per window Reset Source: rst_mod_g_rst_n

14.3.4.1.2.9 RATE_LIMITER_RD_BW_WINDOWS_CNT Register

1 RATE_LIMITER_RD_BW_WINDOWS_CNT Register (Offset = 128h) [reset = 0h]

Read Bandwidth Statistics - Window Count

Return to Summary Table

Table 14-16752. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4128h**

Figure 14-5556. RATE_LIMITER_RD_BW_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16754. RATE_LIMITER_RD_BW_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Read bandwidth window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.1.2.10 RATE_LIMITER_RD_BW_STATS_CIR Register

1 RATE_LIMITER_RD_BW_STATS_CIR Register (Offset = 12Ch) [reset = 0h]

Read Bandwidth Statistics - CIR Count

Return to Summary Table

Table 14-16755. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 412Ch**

Figure 14-5557. RATE_LIMITER_RD_BW_STATS_CIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16757. RATE_LIMITER_RD_BW_STATS_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read Commit Information Rate occurred. Note that if PIR is set to a lower value than CIR or if the burst offset feature is used, this will also count times that PIR is reached. Reset Source: rst_mod_g_rst_n

14.3.4.1.2.11 RATE_LIMITER_RD_BW_STATS_PIR Register

1 RATE_LIMITER_RD_BW_STATS_PIR Register (Offset = 130h) [reset = 0h]

Read Bandwidth Statistics - PIR Count

Return to Summary Table

Table 14-16758. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4130h**

Figure 14-5558. RATE_LIMITER_RD_BW_STATS_PIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAL							
R							
0h							

Table 14-16760. RATE_LIMITER_RD_BW_STATS_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read Peak Information Rate occurred Reset Source: rst_mod_g_rst_n

14.3.4.1.2.12 RATE_LIMITER_RD_BW_THRSHLD_CNT Register

1 RATE_LIMITER_RD_BW_THRSHLD_CNT Register (Offset = 134h) [reset = 0h]

Read Bandwidth Statistics - Threshold Count

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Table 14-16761. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4134h**

Figure 14-5559. RATE_LIMITER_RD_BW_THRSHLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16763. RATE_LIMITER_RD_BW_THRSHLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Read bytes transferred exceeded the statistics threshold Reset Source: rst_mod_g_rst_n

14.3.4.1.2.13 RATE_LIMITER_RD_BYTES_MAX Register

1 RATE_LIMITER_RD_BYTES_MAX Register (Offset = 138h) [reset = 0h]

The maximum number of bytes seen in a single statitsics window. This can be compared with the window size to calculate the maximum bandwidth seen

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Table 14-16764. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4138h**

Figure 14-5560. RATE_LIMITER_RD_BYTES_MAX Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAL							
R							
0h							

Table 14-16766. RATE_LIMITER_RD_BYTES_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Max number of bytes in a single window. This number accounts for DDR bandwidth consumed, not simply the accumulation of the packet bytecnt values across a window. The max bandwidth calculation is the total bytes value in this MMR divided by the windows size in RD_BW_STATS.window and multiplied with the interface frequency: RD_BYTES_MAX * FREQ / RD_BW_STATS.window Reset Source: rst_mod_g_rst_n

14.3.4.1.2.14 RATE_LIMITER_RD_TXN Register

1 RATE_LIMITER_RD_TXN Register (Offset = 300h) [reset = 40h]

The maximum number of outstanding read transactions the rate limiter will allow

Return to Summary Table

Table 14-16767. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4300h**

Figure 14-5561. RATE_LIMITER_RD_TXN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIMIT							
R/W							
40h							
7	6	5	4	3	2	1	0
LIMIT							
R/W							
40h							

Table 14-16769. RATE_LIMITER_RD_TXN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	LIMIT	R/W	40h	The maximum number of outstanding read transactions allowed. NOTE: This cannot be programmed to a zero. If a zero is written, it will default to the reset value of 16'd64, as a limit of zero outstanding transactions would hang the interface. Reset Source: rst_mod_g_rst_n

14.3.4.1.2.15 RATE_LIMITER_RD_TXN_INFO Register

1 RATE_LIMITER_RD_TXN_INFO Register (Offset = 30Ch) [reset = 0h]

Read Transaction State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16770. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 430Ch**

Figure 14-5562. RATE_LIMITER_RD_TXN_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	OCC						
NONE	R						
0h	0h						

Table 14-16772. RATE_LIMITER_RD_TXN_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	OCC	R	0h	Read transaction scoreboard occupancy Reset Source: rst_mod_g_rst_n

14.3.4.1.2.16 RATE_LIMITER_RD_TXN_STATS Register

1 RATE_LIMITER_RD_TXN_STATS Register (Offset = 320h) [reset = 4000000h]

Read Transaction Stats Control Register

Return to Summary Table

Table 14-16773. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4320h**

Figure 14-5563. RATE_LIMITER_RD_TXN_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	22	21	20	19	18	17	16
WINDOW							
R/W							
400h							
15	14	13	12	11	10	9	8
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16775. RATE_LIMITER_RD_TXN_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable read transaction statistics Reset Source: rst_mod_g_rst_n

14.3.4.1.2.17 RATE_LIMITER_RD_TXN_STATS_THRSHLD Register

1 RATE_LIMITER_RD_TXN_STATS_THRSHLD Register (Offset = 324h) [reset = 0h]

A statistics threshold separate from the read transaction limit

Return to Summary Table

Table 14-16776. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	3040 4324h

Figure 14-5564. RATE_LIMITER_RD_TXN_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16778. RATE_LIMITER_RD_TXN_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THRESHOLD	R/W	0h	Read transaction statistics threshold. The threshold can be set to any value, though it will saturate at the outstanding transaction limit if it is set to a value greater than the programmed outstanding read transaction limit Reset Source: rst_mod_g_rst_n

14.3.4.1.2.18 RATE_LIMITER_RD_TXN_WINDOWS_CNT Register

1 RATE_LIMITER_RD_TXN_WINDOWS_CNT Register (Offset = 328h) [reset = 0h]

Read Transaction Statistics - Window Count

Return to Summary Table

Table 14-16779. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4328h**

Figure 14-5565. RATE_LIMITER_RD_TXN_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16781. RATE_LIMITER_RD_TXN_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Read transaction window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.1.2.19 RATE_LIMITER_RD_TXN_LIMIT_CNT Register

1 RATE_LIMITER_RD_TXN_LIMIT_CNT Register (Offset = 32Ch) [reset = 0h]

Read Transaction Statistics - number of windows in which the outstanding transaction limit was reached

Return to Summary Table

Table 14-16782. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 432Ch**

Figure 14-5566. RATE_LIMITER_RD_TXN_LIMIT_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16784. RATE_LIMITER_RD_TXN_LIMIT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the outstanding read transaction limit was reached Reset Source: rst_mod_g_rst_n

14.3.4.1.2.20 RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register

1 RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register (Offset = 330h) [reset = 0h]

Read Transaction Statistics - number of windows in which the statistics threshold was reached

Return to Summary Table

Table 14-16785. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4330h**

Figure 14-5567. RATE_LIMITER_RD_TXN_THRESHOLD_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16787. RATE_LIMITER_RD_TXN_THRESHOLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the number of outstanding read transactions was greater than or equal to the threshold in RD_TXN_STATS_THRSHLD Reset Source: rst_mod_g_rst_n

14.3.4.1.2.21 RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register

1 RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register (Offset = 334h) [reset = 0h]

Read Transaction Statistics - Cycles at Outstanding Read Transactions Limit

Return to Summary Table

Table 14-16788. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4334h**

Figure 14-5568. RATE_LIMITER_RD_TXN_LIMIT_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16790. RATE_LIMITER_RD_TXN_LIMIT_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with the read transactions outstanding at the programmed limit since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.1.2.22 RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register

1 RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register (Offset = 338h) [reset = 0h]

Read Transaction Statistics - Cycles at the Statistics Threshold

Return to Summary Table

Table 14-16791. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 4338h**

Figure 14-5569. RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16793. RATE_LIMITER_RD_TXN_THRESHOLD_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with read transactions outstanding greater than or equal to the statistics threshold in RD_TXN_STATS_THRSHLD since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.1.2.23 RATE_LIMITER_RD_TXN_MAX Register

1 RATE_LIMITER_RD_TXN_MAX Register (Offset = 33Ch) [reset = 0h]

Read Transaction Statistics - Max Observed Outstanding Read Transactions

Return to Summary Table

Table 14-16794. Instance Table

Instance Name	Physical Address
JPGENC_RS_BW_LIMITER4	**3040 433Ch**

Figure 14-5570. RATE_LIMITER_RD_TXN_MAX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16796. RATE_LIMITER_RD_TXN_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VAL	R	0h	The maximum outstanding read transactions at any point in time, regardless of the programmed limit Reset Source: rst_mod_g_rst_n

14.3.4.2 jpgenc_ws_bw_limiter

jpgenc_ws_bw_limiter

14.3.4.2.1 jpgenc_ws_bw_limiter Summaries

jpgenc_ws_bw_limiter Summaries

Table 14-16797. RATE_LIMITER Registers, Base Address=3040 5000h, Length=4096

Offset	Length	Register Name	JPGENC_WS_BW_LIMITER5 Physical Address
0h	32	RATE_LIMITER_PID	3040 5000h
4h	32	RATE_LIMITER_CTRL	3040 5004h
200h	32	RATE_LIMITER_WR_BW_CIR	3040 5200h
204h	32	RATE_LIMITER_WR_BW_PIR	3040 5204h
208h	32	RATE_LIMITER_WR_BW_BURST_OFFSET	3040 5208h
20Ch	32	RATE_LIMITER_WR_BW_INFO	3040 520Ch
220h	32	RATE_LIMITER_WR_BW_STATS	3040 5220h
224h	32	RATE_LIMITER_WR_BW_STATS_THRSHLD	3040 5224h
228h	32	RATE_LIMITER_WR_BW_WINDOWS_CNT	3040 5228h
22Ch	32	RATE_LIMITER_WR_BW_STATS_CIR	3040 522Ch
230h	32	RATE_LIMITER_WR_BW_STATS_PIR	3040 5230h
234h	32	RATE_LIMITER_WR_BW_THRSHLD_CNT	3040 5234h
238h	32	RATE_LIMITER_WR_BYTES_MAX	3040 5238h
400h	32	RATE_LIMITER_WR_TXN	3040 5400h
40Ch	32	RATE_LIMITER_WR_TXN_INFO	3040 540Ch
420h	32	RATE_LIMITER_WR_TXN_STATS	3040 5420h
424h	32	RATE_LIMITER_WR_TXN_STATS_THRSHLD	3040 5424h
428h	32	RATE_LIMITER_WR_TXN_WINDOWS_CNT	3040 5428h
42Ch	32	RATE_LIMITER_WR_TXN_LIMIT_CNT	3040 542Ch
430h	32	RATE_LIMITER_WR_TXN_THRESHOLD_CNT	3040 5430h
434h	32	RATE_LIMITER_WR_TXN_LIMIT_TOTAL	3040 5434h
438h	32	RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL	3040 5438h
43Ch	32	RATE_LIMITER_WR_TXN_MAX	3040 543Ch

14.3.4.2.2 jpgenc_ws_bw_limiter Registers

jpgenc_ws_bw_limiter Registers

14.3.4.2.2.1 RATE_LIMITER_PID Register

1 RATE_LIMITER_PID Register (Offset = 0h) [reset = 66602900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-16798. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5000h**

Figure 14-5571. RATE_LIMITER_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		660h			
23	22	21	20	19	18	17	16
FUNC							
R							
660h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
5h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-16800. RATE_LIMITER_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	PID bu identifier Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	660h	PID function identifier Reset Source: rst_mod_g_rst_n
15:11	RTL_VER	R	5h	PID RTL version number Reset Source: rst_mod_g_rst_n
10:8	MAJOR_REV	R	1h	PID Major revision number Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	PID custom Reset Source: rst_mod_g_rst_n
5:0	MINOR_REV	R	0h	PID Minor revision number Reset Source: rst_mod_g_rst_n

14.3.4.2.2.2 RATE_LIMITER_CTRL Register

1 RATE_LIMITER_CTRL Register (Offset = 4h) [reset = 0h]

This register controls the overall behavior of the rate limiter module

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Table 14-16801. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5004h**

Figure 14-5572. RATE_LIMITER_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REGION_FILTER_EN	WR_TXN_ENABLE	RD_TXN_ENABLE	WR_BW_ENABLE	RD_BW_ENABLE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-16803. RATE_LIMITER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REGION_FILTER_EN	R/W	0h	Enable the region filter, which will only apply the bandwith and transaction limits to the configured address regions Reset Source: rst_mod_g_rst_n
3	WR_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding write transactions Reset Source: rst_mod_g_rst_n
2	RD_TXN_ENABLE	R/W	0h	Enable limiting maximum outstanding read transactions Reset Source: rst_mod_g_rst_n
1	WR_BW_ENABLE	R/W	0h	Enable write bandwidth limiting Reset Source: rst_mod_g_rst_n
0	RD_BW_ENABLE	R/W	0h	Enable read bandwidth limiting Reset Source: rst_mod_g_rst_n

14.3.4.2.2.3 RATE_LIMITER_WR_BW_CIR Register

1 RATE_LIMITER_WR_BW_CIR Register (Offset = 200h) [reset = 0h]

Write Bandwidth Committed Information Rate

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Table 14-16804. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5200h**

Figure 14-5573. RATE_LIMITER_WR_BW_CIR Name Register

31	30	29	28	27	26	25	24
CIR							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR							
R/W							
0h							

Table 14-16806. RATE_LIMITER_WR_BW_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR	R/W	0h	Committed Information Rate Reset Source: rst_mod_g_rst_n

14.3.4.2.2.4 RATE_LIMITER_WR_BW_PIR Register

1 RATE_LIMITER_WR_BW_PIR Register (Offset = 204h) [reset = 0h]

Write Bandwidth Peak Information Rate

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Table 14-16807. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5204h**

Figure 14-5574. RATE_LIMITER_WR_BW_PIR Name Register

31	30	29	28	27	26	25	24
PIR							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR							
R/W							
0h							

Table 14-16809. RATE_LIMITER_WR_BW_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR	R/W	0h	Peak Information Rate Reset Source: rst_mod_g_rst_n

14.3.4.2.2.5 RATE_LIMITER_WR_BW_BURST_OFFSET Register

1 RATE_LIMITER_WR_BW_BURST_OFFSET Register (Offset = 208h) [reset = 0h]

Write Bandwidth Burst Offset

Return to Summary Table

Table 14-16810. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5208h**

Figure 14-5575. RATE_LIMITER_WR_BW_BURST_OFFSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFFSET							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFSET							
R/W							
0h							

Table 14-16812. RATE_LIMITER_WR_BW_BURST_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFFSET	R/W	0h	Burst Offset - the number of bytes before the Committed Information Rate is applied at startup or after a period of inactivity. Peak Information Rate will still apply Reset Source: rst_mod_g_rst_n

14.3.4.2.2.6 RATE_LIMITER_WR_BW_INFO Register

1 RATE_LIMITER_WR_BW_INFO Register (Offset = 20Ch) [reset = 0h]

Write Bandwidth State machine information. Primarily for verification purposes

Return to Summary Table

Table 14-16813. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 520Ch**

Figure 14-5576. RATE_LIMITER_WR_BW_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						COLOR	
NONE						R	
0h						0h	

Table 14-16815. RATE_LIMITER_WR_BW_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	COLOR	R	0h	Write Bandwidth three-color marker output from rategen submodule Reset Source: rst_mod_g_rst_n

14.3.4.2.2.7 RATE_LIMITER_WR_BW_STATS Register

1 RATE_LIMITER_WR_BW_STATS Register (Offset = 220h) [reset = 4000000h]

Write Bandwidth Statistics Control Register

Return to Summary Table

Table 14-16816. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5220h**

Figure 14-5577. RATE_LIMITER_WR_BW_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WINDOW							
R/W							
400h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16818. RATE_LIMITER_WR_BW_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable write bandwidth statistics Reset Source: rst_mod_g_rst_n

14.3.4.2.2.8 RATE_LIMITER_WR_BW_STATS_THRSHLD Register

1 RATE_LIMITER_WR_BW_STATS_THRSHLD Register (Offset = 224h) [reset = 0h]

A statistics threshold separate from the CIR and PIR

Return to Summary Table

Table 14-16819. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5224h**

Figure 14-5578. RATE_LIMITER_WR_BW_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16821. RATE_LIMITER_WR_BW_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	THRESHOLD	R/W	0h	Write bandwidth stats threshold in bytes. Note that this is total bytes, unlike CIR and PIR. CIR and PIR are based on a rolling window, and the statistics threshold is based on a fixed window. This will still take into account DDR bytes used, so can be compared to CIR and PIR directly if the bandwidths are converted via the equations for CIR and PIR. The threshold bandwidth is programmed here as bytes per window Reset Source: rst_mod_g_rst_n

14.3.4.2.2.9 RATE_LIMITER_WR_BW_WINDOWS_CNT Register

1 RATE_LIMITER_WR_BW_WINDOWS_CNT Register (Offset = 228h) [reset = 0h]

Write Bandwidth Statistics - Window Count

Return to Summary Table

Table 14-16822. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5228h**

Figure 14-5579. RATE_LIMITER_WR_BW_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16824. RATE_LIMITER_WR_BW_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Write bandwidth window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.2.2.10 RATE_LIMITER_WR_BW_STATS_CIR Register

1 RATE_LIMITER_WR_BW_STATS_CIR Register (Offset = 22Ch) [reset = 0h]

Write Bandwidth Statistics - CIR Count

Return to Summary Table

Table 14-16825. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 522Ch**

Figure 14-5580. RATE_LIMITER_WR_BW_STATS_CIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16827. RATE_LIMITER_WR_BW_STATS_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write Commit Information Rate occurred. Note that if PIR is set to a lower value than CIR or if the burst offset feature is used, this will also count times that PIR is reached. Reset Source: rst_mod_g_rst_n

14.3.4.2.2.11 RATE_LIMITER_WR_BW_STATS_PIR Register

1 RATE_LIMITER_WR_BW_STATS_PIR Register (Offset = 230h) [reset = 0h]

Write Bandwidth Statistics - PIR Count

Return to Summary Table

Table 14-16828. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5230h**

Figure 14-5581. RATE_LIMITER_WR_BW_STATS_PIR Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16830. RATE_LIMITER_WR_BW_STATS_PIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write Peak Information Rate occurred Reset Source: rst_mod_g_rst_n

14.3.4.2.2.12 RATE_LIMITER_WR_BW_THRSHLD_CNT Register

1 RATE_LIMITER_WR_BW_THRSHLD_CNT Register (Offset = 234h) [reset = 0h]

Write Bandwidth Statistics - Threshold Count

Return to Summary Table

Table 14-16831. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5234h**

Figure 14-5582. RATE_LIMITER_WR_BW_THRSHLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16833. RATE_LIMITER_WR_BW_THRSHLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of statistics windows in which Write bytes transferred exceeded the statistics threshold Reset Source: rst_mod_g_rst_n

14.3.4.2.2.13 RATE_LIMITER_WR_BYTES_MAX Register

1 RATE_LIMITER_WR_BYTES_MAX Register (Offset = 238h) [reset = 0h]

The maximum number of bytes seen in a single statitsics window. This can be compared with the window size to calculate the maximum bandwidth seen

Return to Summary Table

Table 14-16834. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5238h**

Figure 14-5583. RATE_LIMITER_WR_BYTES_MAX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16836. RATE_LIMITER_WR_BYTES_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Max number of bytes in a single window. This number accounts for DDR bandwidth consumed, not simply the accumulation of the packet bytecnt values across a window. The max bandwidth calculation is the total bytes value in this MMR divided by the windows size in WR_BW_STATS.window and multiplied with the interface frequency: WR_BYTES_MAX * FREQ / WR_BW_STATS.window Reset Source: rst_mod_g_rst_n

14.3.4.2.2.14 RATE_LIMITER_WR_TXN Register

1 RATE_LIMITER_WR_TXN Register (Offset = 400h) [reset = 40h]

The maximum number of outstanding write transactions the rate limiter will allow

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Table 14-16837. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5400h**

Figure 14-5584. RATE_LIMITER_WR_TXN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMIT							
R/W							
40h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
40h							

Table 14-16839. RATE_LIMITER_WR_TXN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	LIMIT	R/W	40h	The maximum number of outstanding write transactions allowed. NOTE: This cannot be programmed to a zero. If a zero is written, it will default to the reset value of 16'd64, as a limit of zero outstanding transactions would hang the interface. Reset Source: rst_mod_g_rst_n

14.3.4.2.2.15 RATE_LIMITER_WR_TXN_INFO Register

1 RATE_LIMITER_WR_TXN_INFO Register (Offset = 40Ch) [reset = 0h]

Write Transaction State machine information. Primarly for verification purposes

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Table 14-16840. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 540Ch**

Figure 14-5585. RATE_LIMITER_WR_TXN_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	OCC						
NONE	R						
0h	0h						

Table 14-16842. RATE_LIMITER_WR_TXN_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	OCC	R	0h	Write transaction scoreboard occupancy Reset Source: rst_mod_g_rst_n

14.3.4.2.2.16 RATE_LIMITER_WR_TXN_STATS Register

1 RATE_LIMITER_WR_TXN_STATS Register (Offset = 420h) [reset = 4000000h]

Write Transaction Stats Control Register

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Table 14-16843. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5420h**

Figure 14-5586. RATE_LIMITER_WR_TXN_STATS Name Register

31	30	29	28	27	26	25	24
WINDOW							
R/W							
400h							
23	22	21	20	19	18	17	16
WINDOW							
R/W							
400h							
15	14	13	12	11	10	9	8
RESERVED						OVERFLOW	CLR
NONE						R	W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED							EN
NONE							R/W
0h							0h

Table 14-16845. RATE_LIMITER_WR_TXN_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WINDOW	R/W	400h	Statistics window size. This cannot be set to 0. If 16'd0 is written, it will be set to the reset value of 16'd1024 Reset Source: rst_mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	OVERFLOW	R	0h	Statistics overflow error Reset Source: rst_mod_g_rst_n
8	CLR	W	0h	Clear statistics data. Resets statistics counters at 0 Reset Source: rst_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	EN	R/W	0h	Enable write transaction statistics Reset Source: rst_mod_g_rst_n

14.3.4.2.2.17 RATE_LIMITER_WR_TXN_STATS_THRSHLD Register

1 RATE_LIMITER_WR_TXN_STATS_THRSHLD Register (Offset = 424h) [reset = 0h]

A statistics threshold separate from the write transaction limit

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Table 14-16846. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5424h**

Figure 14-5587. RATE_LIMITER_WR_TXN_STATS_THRSHLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-16848. RATE_LIMITER_WR_TXN_STATS_THRSHLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THRESHOLD	R/W	0h	Write transaction statistics threshold. The threshold can be set to any value, though it will saturate at the outstanding transaction limit if it is set to a value greater than the programmed outstanding write transaction limit Reset Source: rst_mod_g_rst_n

14.3.4.2.2.18 RATE_LIMITER_WR_TXN_WINDOWS_CNT Register

1 RATE_LIMITER_WR_TXN_WINDOWS_CNT Register (Offset = 428h) [reset = 0h]

Write Transaction Statistics - Window Count

Return to Summary Table

Table 14-16849. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5428h**

Figure 14-5588. RATE_LIMITER_WR_TXN_WINDOWS_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16851. RATE_LIMITER_WR_TXN_WINDOWS_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	Write transaction window count - the number of windows elapsed since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.2.2.19 RATE_LIMITER_WR_TXN_LIMIT_CNT Register

1 RATE_LIMITER_WR_TXN_LIMIT_CNT Register (Offset = 42Ch) [reset = 0h]

Write Transaction Statistics - number of windows in which the outstanding transaction limit was reached

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Table 14-16852. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 542Ch**

Figure 14-5589. RATE_LIMITER_WR_TXN_LIMIT_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16854. RATE_LIMITER_WR_TXN_LIMIT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the outstanding write transaction limit was reached Reset Source: rst_mod_g_rst_n

14.3.4.2.2.20 RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register

1 RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register (Offset = 430h) [reset = 0h]

Write Transaction Statistics - number of windows in which the statistics threshold was reached

Return to Summary Table

Table 14-16855. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5430h**

Figure 14-5590. RATE_LIMITER_WR_TXN_THRESHOLD_CNT Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16857. RATE_LIMITER_WR_TXN_THRESHOLD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The number of statistics windows in which the number of outstanding write transactions was greater than or equal to the threshold in WR_TXN_STATS_THRSHLD Reset Source: rst_mod_g_rst_n

14.3.4.2.2.21 RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register

1 RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register (Offset = 434h) [reset = 0h]

Write Transaction Statistics - Cycles at Outstanding Write Transactions Limit

Return to Summary Table

Table 14-16858. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5434h**

Figure 14-5591. RATE_LIMITER_WR_TXN_LIMIT_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16860. RATE_LIMITER_WR_TXN_LIMIT_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with the write transactions outstanding at the programmed limit since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.2.2.22 RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register

1 RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register (Offset = 438h) [reset = 0h]

Write Transaction Statistics - Cycles at the Statistics Threshold

Return to Summary Table

Table 14-16861. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 5438h**

Figure 14-5592. RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAL							
R							
0h							

Table 14-16863. RATE_LIMITER_WR_TXN_THRESHOLD_TOTAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	The total number of cycles with write transactions outstanding greater than or equal to the statistics threshold in WR_TXN_STATS_THRSHLD since statistics collection began Reset Source: rst_mod_g_rst_n

14.3.4.2.2.23 RATE_LIMITER_WR_TXN_MAX Register

1 RATE_LIMITER_WR_TXN_MAX Register (Offset = 43Ch) [reset = 0h]

Write Transaction Statistics - Max Observed Outstanding Write Transactions

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Table 14-16864. Instance Table

Instance Name	Physical Address
JPGENC_WS_BW_LIMITER5	**3040 543Ch**

Figure 14-5593. RATE_LIMITER_WR_TXN_MAX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-16866. RATE_LIMITER_WR_TXN_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VAL	R	0h	The maximum outstanding write transactions at any point in time, regardless of the programmed limit Reset Source: rst_mod_g_rst_n

14.4 Interrupt Router Registers

14.4.1 gicss

gicss

14.4.1.1 gicss Summaries

gicss Summaries

Table 14-16867. GIC500_TRANSLATER Registers, Base Address=0100 0000h, Length=4194304

Offset	Length	Register Name	GICSS0 Physical Address
30040h	32	GIC500_TRANSLATER_TRANSLATER	0103 0040h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576

Offset	Length	Register Name	GICSS0 Physical Address
0h	32	GIC500_GICD_CTLR	0180 0000h
4h	32	GIC500_GICD_TYPER	0180 0004h
8h	32	GIC500_GICD_IIDR	0180 0008h
40h	32	GIC500_GICD_SETSPI_NSR	0180 0040h
48h	32	GIC500_GICD_CLRSPI_NSR	0180 0048h
50h	32	GIC500_GICD_SETSPI_SR	0180 0050h
58h	32	GIC500_GICD_CLRSPI_SR	0180 0058h
80h	32	GIC500_GICD_IGROUPR_SGI_PPI	0180 0080h
84h	32	GIC500_GICD_IGROUPR_SPI1	0180 0084h
88h	32	GIC500_GICD_IGROUPR_SPI2	0180 0088h
8Ch	32	GIC500_GICD_IGROUPR_SPI3	0180 008Ch
90h	32	GIC500_GICD_IGROUPR_SPI4	0180 0090h
94h	32	GIC500_GICD_IGROUPR_SPI5	0180 0094h
98h	32	GIC500_GICD_IGROUPR_SPI6	0180 0098h
9Ch	32	GIC500_GICD_IGROUPR_SPI7	0180 009Ch
A0h	32	GIC500_GICD_IGROUPR_SPI8	0180 00A0h
104h	32	GIC500_GICD_ISENABLER_SPI1	0180 0104h
108h	32	GIC500_GICD_ISENABLER_SPI2	0180 0108h
10Ch	32	GIC500_GICD_ISENABLER_SPI3	0180 010Ch
110h	32	GIC500_GICD_ISENABLER_SPI4	0180 0110h
114h	32	GIC500_GICD_ISENABLER_SPI5	0180 0114h
118h	32	GIC500_GICD_ISENABLER_SPI6	0180 0118h
11Ch	32	GIC500_GICD_ISENABLER_SPI7	0180 011Ch
120h	32	GIC500_GICD_ISENABLER_SPI8	0180 0120h
184h	32	GIC500_GICD_ICENABLER_SPI1	0180 0184h
188h	32	GIC500_GICD_ICENABLER_SPI2	0180 0188h
18Ch	32	GIC500_GICD_ICENABLER_SPI3	0180 018Ch
190h	32	GIC500_GICD_ICENABLER_SPI4	0180 0190h
194h	32	GIC500_GICD_ICENABLER_SPI5	0180 0194h
198h	32	GIC500_GICD_ICENABLER_SPI6	0180 0198h
19Ch	32	GIC500_GICD_ICENABLER_SPI7	0180 019Ch
1A0h	32	GIC500_GICD_ICENABLER_SPI8	0180 01A0h
204h	32	GIC500_GICD_ISPENDR_SPI1	0180 0204h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
208h	32	GIC500_GICD_ISPENDR_SPI2	0180 0208h
20Ch	32	GIC500_GICD_ISPENDR_SPI3	0180 020Ch
210h	32	GIC500_GICD_ISPENDR_SPI4	0180 0210h
214h	32	GIC500_GICD_ISPENDR_SPI5	0180 0214h
218h	32	GIC500_GICD_ISPENDR_SPI6	0180 0218h
21Ch	32	GIC500_GICD_ISPENDR_SPI7	0180 021Ch
220h	32	GIC500_GICD_ISPENDR_SPI8	0180 0220h
284h	32	GIC500_GICD_ICPENDR_SPI1	0180 0284h
288h	32	GIC500_GICD_ICPENDR_SPI2	0180 0288h
28Ch	32	GIC500_GICD_ICPENDR_SPI3	0180 028Ch
290h	32	GIC500_GICD_ICPENDR_SPI4	0180 0290h
294h	32	GIC500_GICD_ICPENDR_SPI5	0180 0294h
298h	32	GIC500_GICD_ICPENDR_SPI6	0180 0298h
29Ch	32	GIC500_GICD_ICPENDR_SPI7	0180 029Ch
2A0h	32	GIC500_GICD_ICPENDR_SPI8	0180 02A0h
304h	32	GIC500_GICD_ISACTIVER_SPI1	0180 0304h
308h	32	GIC500_GICD_ISACTIVER_SPI2	0180 0308h
30Ch	32	GIC500_GICD_ISACTIVER_SPI3	0180 030Ch
310h	32	GIC500_GICD_ISACTIVER_SPI4	0180 0310h
314h	32	GIC500_GICD_ISACTIVER_SPI5	0180 0314h
318h	32	GIC500_GICD_ISACTIVER_SPI6	0180 0318h
31Ch	32	GIC500_GICD_ISACTIVER_SPI7	0180 031Ch
320h	32	GIC500_GICD_ISACTIVER_SPI8	0180 0320h
384h	32	GIC500_GICD_ICACTIVER_SPI1	0180 0384h
388h	32	GIC500_GICD_ICACTIVER_SPI2	0180 0388h
38Ch	32	GIC500_GICD_ICACTIVER_SPI3	0180 038Ch
390h	32	GIC500_GICD_ICACTIVER_SPI4	0180 0390h
394h	32	GIC500_GICD_ICACTIVER_SPI5	0180 0394h
398h	32	GIC500_GICD_ICACTIVER_SPI6	0180 0398h
39Ch	32	GIC500_GICD_ICACTIVER_SPI7	0180 039Ch
3A0h	32	GIC500_GICD_ICACTIVER_SPI8	0180 03A0h
420h	32	GIC500_GICD_IPRIORITYR_SPI8	0180 0420h
424h	32	GIC500_GICD_IPRIORITYR_SPI9	0180 0424h
428h	32	GIC500_GICD_IPRIORITYR_SPI10	0180 0428h
42Ch	32	GIC500_GICD_IPRIORITYR_SPI11	0180 042Ch
430h	32	GIC500_GICD_IPRIORITYR_SPI12	0180 0430h
434h	32	GIC500_GICD_IPRIORITYR_SPI13	0180 0434h
438h	32	GIC500_GICD_IPRIORITYR_SPI14	0180 0438h
43Ch	32	GIC500_GICD_IPRIORITYR_SPI15	0180 043Ch
440h	32	GIC500_GICD_IPRIORITYR_SPI16	0180 0440h
444h	32	GIC500_GICD_IPRIORITYR_SPI17	0180 0444h
448h	32	GIC500_GICD_IPRIORITYR_SPI18	0180 0448h
44Ch	32	GIC500_GICD_IPRIORITYR_SPI19	0180 044Ch
450h	32	GIC500_GICD_IPRIORITYR_SPI20	0180 0450h
454h	32	GIC500_GICD_IPRIORITYR_SPI21	0180 0454h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
458h	32	GIC500_GICD_IPRIORITYR_SPI22	0180 0458h
45Ch	32	GIC500_GICD_IPRIORITYR_SPI23	0180 045Ch
460h	32	GIC500_GICD_IPRIORITYR_SPI24	0180 0460h
464h	32	GIC500_GICD_IPRIORITYR_SPI25	0180 0464h
468h	32	GIC500_GICD_IPRIORITYR_SPI26	0180 0468h
46Ch	32	GIC500_GICD_IPRIORITYR_SPI27	0180 046Ch
470h	32	GIC500_GICD_IPRIORITYR_SPI28	0180 0470h
474h	32	GIC500_GICD_IPRIORITYR_SPI29	0180 0474h
478h	32	GIC500_GICD_IPRIORITYR_SPI30	0180 0478h
47Ch	32	GIC500_GICD_IPRIORITYR_SPI31	0180 047Ch
480h	32	GIC500_GICD_IPRIORITYR_SPI32	0180 0480h
484h	32	GIC500_GICD_IPRIORITYR_SPI33	0180 0484h
488h	32	GIC500_GICD_IPRIORITYR_SPI34	0180 0488h
48Ch	32	GIC500_GICD_IPRIORITYR_SPI35	0180 048Ch
490h	32	GIC500_GICD_IPRIORITYR_SPI36	0180 0490h
494h	32	GIC500_GICD_IPRIORITYR_SPI37	0180 0494h
498h	32	GIC500_GICD_IPRIORITYR_SPI38	0180 0498h
49Ch	32	GIC500_GICD_IPRIORITYR_SPI39	0180 049Ch
4A0h	32	GIC500_GICD_IPRIORITYR_SPI40	0180 04A0h
4A4h	32	GIC500_GICD_IPRIORITYR_SPI41	0180 04A4h
4A8h	32	GIC500_GICD_IPRIORITYR_SPI42	0180 04A8h
4ACh	32	GIC500_GICD_IPRIORITYR_SPI43	0180 04ACh
4B0h	32	GIC500_GICD_IPRIORITYR_SPI44	0180 04B0h
4B4h	32	GIC500_GICD_IPRIORITYR_SPI45	0180 04B4h
4B8h	32	GIC500_GICD_IPRIORITYR_SPI46	0180 04B8h
4BCh	32	GIC500_GICD_IPRIORITYR_SPI47	0180 04BCh
4C0h	32	GIC500_GICD_IPRIORITYR_SPI48	0180 04C0h
4C4h	32	GIC500_GICD_IPRIORITYR_SPI49	0180 04C4h
4C8h	32	GIC500_GICD_IPRIORITYR_SPI50	0180 04C8h
4CCh	32	GIC500_GICD_IPRIORITYR_SPI51	0180 04CCh
4D0h	32	GIC500_GICD_IPRIORITYR_SPI52	0180 04D0h
4D4h	32	GIC500_GICD_IPRIORITYR_SPI53	0180 04D4h
4D8h	32	GIC500_GICD_IPRIORITYR_SPI54	0180 04D8h
4DCh	32	GIC500_GICD_IPRIORITYR_SPI55	0180 04DCh
4E0h	32	GIC500_GICD_IPRIORITYR_SPI56	0180 04E0h
4E4h	32	GIC500_GICD_IPRIORITYR_SPI57	0180 04E4h
4E8h	32	GIC500_GICD_IPRIORITYR_SPI58	0180 04E8h
4ECh	32	GIC500_GICD_IPRIORITYR_SPI59	0180 04ECh
4F0h	32	GIC500_GICD_IPRIORITYR_SPI60	0180 04F0h
4F4h	32	GIC500_GICD_IPRIORITYR_SPI61	0180 04F4h
4F8h	32	GIC500_GICD_IPRIORITYR_SPI62	0180 04F8h
4FCh	32	GIC500_GICD_IPRIORITYR_SPI63	0180 04FCh
500h	32	GIC500_GICD_IPRIORITYR_SPI64	0180 0500h
504h	32	GIC500_GICD_IPRIORITYR_SPI65	0180 0504h
508h	32	GIC500_GICD_IPRIORITYR_SPI66	0180 0508h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
50Ch	32	GIC500_GICD_IPRIORITYR_SPI67	0180 050Ch
510h	32	GIC500_GICD_IPRIORITYR_SPI68	0180 0510h
514h	32	GIC500_GICD_IPRIORITYR_SPI69	0180 0514h
518h	32	GIC500_GICD_IPRIORITYR_SPI70	0180 0518h
51Ch	32	GIC500_GICD_IPRIORITYR_SPI71	0180 051Ch
820h	32	GIC500_GICD_ITARGETSR_SPI8	0180 0820h
824h	32	GIC500_GICD_ITARGETSR_SPI9	0180 0824h
828h	32	GIC500_GICD_ITARGETSR_SPI10	0180 0828h
82Ch	32	GIC500_GICD_ITARGETSR_SPI11	0180 082Ch
830h	32	GIC500_GICD_ITARGETSR_SPI12	0180 0830h
834h	32	GIC500_GICD_ITARGETSR_SPI13	0180 0834h
838h	32	GIC500_GICD_ITARGETSR_SPI14	0180 0838h
83Ch	32	GIC500_GICD_ITARGETSR_SPI15	0180 083Ch
840h	32	GIC500_GICD_ITARGETSR_SPI16	0180 0840h
844h	32	GIC500_GICD_ITARGETSR_SPI17	0180 0844h
848h	32	GIC500_GICD_ITARGETSR_SPI18	0180 0848h
84Ch	32	GIC500_GICD_ITARGETSR_SPI19	0180 084Ch
850h	32	GIC500_GICD_ITARGETSR_SPI20	0180 0850h
854h	32	GIC500_GICD_ITARGETSR_SPI21	0180 0854h
858h	32	GIC500_GICD_ITARGETSR_SPI22	0180 0858h
85Ch	32	GIC500_GICD_ITARGETSR_SPI23	0180 085Ch
860h	32	GIC500_GICD_ITARGETSR_SPI24	0180 0860h
864h	32	GIC500_GICD_ITARGETSR_SPI25	0180 0864h
868h	32	GIC500_GICD_ITARGETSR_SPI26	0180 0868h
86Ch	32	GIC500_GICD_ITARGETSR_SPI27	0180 086Ch
870h	32	GIC500_GICD_ITARGETSR_SPI28	0180 0870h
874h	32	GIC500_GICD_ITARGETSR_SPI29	0180 0874h
878h	32	GIC500_GICD_ITARGETSR_SPI30	0180 0878h
87Ch	32	GIC500_GICD_ITARGETSR_SPI31	0180 087Ch
880h	32	GIC500_GICD_ITARGETSR_SPI32	0180 0880h
884h	32	GIC500_GICD_ITARGETSR_SPI33	0180 0884h
888h	32	GIC500_GICD_ITARGETSR_SPI34	0180 0888h
88Ch	32	GIC500_GICD_ITARGETSR_SPI35	0180 088Ch
890h	32	GIC500_GICD_ITARGETSR_SPI36	0180 0890h
894h	32	GIC500_GICD_ITARGETSR_SPI37	0180 0894h
898h	32	GIC500_GICD_ITARGETSR_SPI38	0180 0898h
89Ch	32	GIC500_GICD_ITARGETSR_SPI39	0180 089Ch
8A0h	32	GIC500_GICD_ITARGETSR_SPI40	0180 08A0h
8A4h	32	GIC500_GICD_ITARGETSR_SPI41	0180 08A4h
8A8h	32	GIC500_GICD_ITARGETSR_SPI42	0180 08A8h
8ACh	32	GIC500_GICD_ITARGETSR_SPI43	0180 08ACh
8B0h	32	GIC500_GICD_ITARGETSR_SPI44	0180 08B0h
8B4h	32	GIC500_GICD_ITARGETSR_SPI45	0180 08B4h
8B8h	32	GIC500_GICD_ITARGETSR_SPI46	0180 08B8h
8BCh	32	GIC500_GICD_ITARGETSR_SPI47	0180 08BCh

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
8C0h	32	GIC500_GICD_ITARGETSR_SPI48	0180 08C0h
8C4h	32	GIC500_GICD_ITARGETSR_SPI49	0180 08C4h
8C8h	32	GIC500_GICD_ITARGETSR_SPI50	0180 08C8h
8CCh	32	GIC500_GICD_ITARGETSR_SPI51	0180 08CCh
8D0h	32	GIC500_GICD_ITARGETSR_SPI52	0180 08D0h
8D4h	32	GIC500_GICD_ITARGETSR_SPI53	0180 08D4h
8D8h	32	GIC500_GICD_ITARGETSR_SPI54	0180 08D8h
8DCh	32	GIC500_GICD_ITARGETSR_SPI55	0180 08DCh
8E0h	32	GIC500_GICD_ITARGETSR_SPI56	0180 08E0h
8E4h	32	GIC500_GICD_ITARGETSR_SPI57	0180 08E4h
8E8h	32	GIC500_GICD_ITARGETSR_SPI58	0180 08E8h
8ECh	32	GIC500_GICD_ITARGETSR_SPI59	0180 08ECh
8F0h	32	GIC500_GICD_ITARGETSR_SPI60	0180 08F0h
8F4h	32	GIC500_GICD_ITARGETSR_SPI61	0180 08F4h
8F8h	32	GIC500_GICD_ITARGETSR_SPI62	0180 08F8h
8FCh	32	GIC500_GICD_ITARGETSR_SPI63	0180 08FCh
900h	32	GIC500_GICD_ITARGETSR_SPI64	0180 0900h
904h	32	GIC500_GICD_ITARGETSR_SPI65	0180 0904h
908h	32	GIC500_GICD_ITARGETSR_SPI66	0180 0908h
90Ch	32	GIC500_GICD_ITARGETSR_SPI67	0180 090Ch
910h	32	GIC500_GICD_ITARGETSR_SPI68	0180 0910h
914h	32	GIC500_GICD_ITARGETSR_SPI69	0180 0914h
918h	32	GIC500_GICD_ITARGETSR_SPI70	0180 0918h
91Ch	32	GIC500_GICD_ITARGETSR_SPI71	0180 091Ch
C08h	32	GIC500_GICD_ICFGR_SPI2	0180 0C08h
C0Ch	32	GIC500_GICD_ICFGR_SPI3	0180 0C0Ch
C10h	32	GIC500_GICD_ICFGR_SPI4	0180 0C10h
C14h	32	GIC500_GICD_ICFGR_SPI5	0180 0C14h
C18h	32	GIC500_GICD_ICFGR_SPI6	0180 0C18h
C1Ch	32	GIC500_GICD_ICFGR_SPI7	0180 0C1Ch
C20h	32	GIC500_GICD_ICFGR_SPI8	0180 0C20h
C24h	32	GIC500_GICD_ICFGR_SPI9	0180 0C24h
C28h	32	GIC500_GICD_ICFGR_SPI10	0180 0C28h
C2Ch	32	GIC500_GICD_ICFGR_SPI11	0180 0C2Ch
C30h	32	GIC500_GICD_ICFGR_SPI12	0180 0C30h
C34h	32	GIC500_GICD_ICFGR_SPI13	0180 0C34h
C38h	32	GIC500_GICD_ICFGR_SPI14	0180 0C38h
C3Ch	32	GIC500_GICD_ICFGR_SPI15	0180 0C3Ch
C40h	32	GIC500_GICD_ICFGR_SPI16	0180 0C40h
C44h	32	GIC500_GICD_ICFGR_SPI17	0180 0C44h
D00h	32	GIC500_GICD_IGRPMODR_SGI_PPI	0180 0D00h
D04h	32	GIC500_GICD_IGRPMODR_SPI1	0180 0D04h
D08h	32	GIC500_GICD_IGRPMODR_SPI2	0180 0D08h
D0Ch	32	GIC500_GICD_IGRPMODR_SPI3	0180 0D0Ch
D10h	32	GIC500_GICD_IGRPMODR_SPI4	0180 0D10h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
D14h	32	GIC500_GICD_IGRPMODR_SPI5	0180 0D14h
D18h	32	GIC500_GICD_IGRPMODR_SPI6	0180 0D18h
D1Ch	32	GIC500_GICD_IGRPMODR_SPI7	0180 0D1Ch
D20h	32	GIC500_GICD_IGRPMODR_SPI8	0180 0D20h
E00h	32	GIC500_GICD_NSACR0	0180 0E00h
E04h	32	GIC500_GICD_NSACR1	0180 0E04h
E08h	32	GIC500_GICD_NSACR2	0180 0E08h
E0Ch	32	GIC500_GICD_NSACR3	0180 0E0Ch
E10h	32	GIC500_GICD_NSACR4	0180 0E10h
E14h	32	GIC500_GICD_NSACR5	0180 0E14h
E18h	32	GIC500_GICD_NSACR6	0180 0E18h
E1Ch	32	GIC500_GICD_NSACR7	0180 0E1Ch
E20h	32	GIC500_GICD_NSACR8	0180 0E20h
E24h	32	GIC500_GICD_NSACR9	0180 0E24h
E28h	32	GIC500_GICD_NSACR10	0180 0E28h
E2Ch	32	GIC500_GICD_NSACR11	0180 0E2Ch
E30h	32	GIC500_GICD_NSACR12	0180 0E30h
E34h	32	GIC500_GICD_NSACR13	0180 0E34h
E38h	32	GIC500_GICD_NSACR14	0180 0E38h
E3Ch	32	GIC500_GICD_NSACR15	0180 0E3Ch
E40h	32	GIC500_GICD_NSACR16	0180 0E40h
E44h	32	GIC500_GICD_NSACR17	0180 0E44h
6100h	32	GIC500_GICD_IROUTER_LOWER32	0180 6100h
6104h	32	GIC500_GICD_IROUTER_UPPER32	0180 6104h
6108h	32	GIC500_GICD_IROUTER_LOWER33	0180 6108h
610Ch	32	GIC500_GICD_IROUTER_UPPER33	0180 610Ch
6110h	32	GIC500_GICD_IROUTER_LOWER34	0180 6110h
6114h	32	GIC500_GICD_IROUTER_UPPER34	0180 6114h
6118h	32	GIC500_GICD_IROUTER_LOWER35	0180 6118h
611Ch	32	GIC500_GICD_IROUTER_UPPER35	0180 611Ch
6120h	32	GIC500_GICD_IROUTER_LOWER36	0180 6120h
6124h	32	GIC500_GICD_IROUTER_UPPER36	0180 6124h
6128h	32	GIC500_GICD_IROUTER_LOWER37	0180 6128h
612Ch	32	GIC500_GICD_IROUTER_UPPER37	0180 612Ch
6130h	32	GIC500_GICD_IROUTER_LOWER38	0180 6130h
6134h	32	GIC500_GICD_IROUTER_UPPER38	0180 6134h
6138h	32	GIC500_GICD_IROUTER_LOWER39	0180 6138h
613Ch	32	GIC500_GICD_IROUTER_UPPER39	0180 613Ch
6140h	32	GIC500_GICD_IROUTER_LOWER40	0180 6140h
6144h	32	GIC500_GICD_IROUTER_UPPER40	0180 6144h
6148h	32	GIC500_GICD_IROUTER_LOWER41	0180 6148h
614Ch	32	GIC500_GICD_IROUTER_UPPER41	0180 614Ch
6150h	32	GIC500_GICD_IROUTER_LOWER42	0180 6150h
6154h	32	GIC500_GICD_IROUTER_UPPER42	0180 6154h
6158h	32	GIC500_GICD_IROUTER_LOWER43	0180 6158h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
615Ch	32	GIC500_GICD_IROUTER_UPPER43	0180 615Ch
6160h	32	GIC500_GICD_IROUTER_LOWER44	0180 6160h
6164h	32	GIC500_GICD_IROUTER_UPPER44	0180 6164h
6168h	32	GIC500_GICD_IROUTER_LOWER45	0180 6168h
616Ch	32	GIC500_GICD_IROUTER_UPPER45	0180 616Ch
6170h	32	GIC500_GICD_IROUTER_LOWER46	0180 6170h
6174h	32	GIC500_GICD_IROUTER_UPPER46	0180 6174h
6178h	32	GIC500_GICD_IROUTER_LOWER47	0180 6178h
617Ch	32	GIC500_GICD_IROUTER_UPPER47	0180 617Ch
6180h	32	GIC500_GICD_IROUTER_LOWER48	0180 6180h
6184h	32	GIC500_GICD_IROUTER_UPPER48	0180 6184h
6188h	32	GIC500_GICD_IROUTER_LOWER49	0180 6188h
618Ch	32	GIC500_GICD_IROUTER_UPPER49	0180 618Ch
6190h	32	GIC500_GICD_IROUTER_LOWER50	0180 6190h
6194h	32	GIC500_GICD_IROUTER_UPPER50	0180 6194h
6198h	32	GIC500_GICD_IROUTER_LOWER51	0180 6198h
619Ch	32	GIC500_GICD_IROUTER_UPPER51	0180 619Ch
61A0h	32	GIC500_GICD_IROUTER_LOWER52	0180 61A0h
61A4h	32	GIC500_GICD_IROUTER_UPPER52	0180 61A4h
61A8h	32	GIC500_GICD_IROUTER_LOWER53	0180 61A8h
61ACh	32	GIC500_GICD_IROUTER_UPPER53	0180 61ACh
61B0h	32	GIC500_GICD_IROUTER_LOWER54	0180 61B0h
61B4h	32	GIC500_GICD_IROUTER_UPPER54	0180 61B4h
61B8h	32	GIC500_GICD_IROUTER_LOWER55	0180 61B8h
61BCh	32	GIC500_GICD_IROUTER_UPPER55	0180 61BCh
61C0h	32	GIC500_GICD_IROUTER_LOWER56	0180 61C0h
61C4h	32	GIC500_GICD_IROUTER_UPPER56	0180 61C4h
61C8h	32	GIC500_GICD_IROUTER_LOWER57	0180 61C8h
61CCh	32	GIC500_GICD_IROUTER_UPPER57	0180 61CCh
61D0h	32	GIC500_GICD_IROUTER_LOWER58	0180 61D0h
61D4h	32	GIC500_GICD_IROUTER_UPPER58	0180 61D4h
61D8h	32	GIC500_GICD_IROUTER_LOWER59	0180 61D8h
61DCh	32	GIC500_GICD_IROUTER_UPPER59	0180 61DCh
61E0h	32	GIC500_GICD_IROUTER_LOWER60	0180 61E0h
61E4h	32	GIC500_GICD_IROUTER_UPPER60	0180 61E4h
61E8h	32	GIC500_GICD_IROUTER_LOWER61	0180 61E8h
61ECh	32	GIC500_GICD_IROUTER_UPPER61	0180 61ECh
61F0h	32	GIC500_GICD_IROUTER_LOWER62	0180 61F0h
61F4h	32	GIC500_GICD_IROUTER_UPPER62	0180 61F4h
61F8h	32	GIC500_GICD_IROUTER_LOWER63	0180 61F8h
61FCh	32	GIC500_GICD_IROUTER_UPPER63	0180 61FCh
6200h	32	GIC500_GICD_IROUTER_LOWER64	0180 6200h
6204h	32	GIC500_GICD_IROUTER_UPPER64	0180 6204h
6208h	32	GIC500_GICD_IROUTER_LOWER65	0180 6208h
620Ch	32	GIC500_GICD_IROUTER_UPPER65	0180 620Ch

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
6210h	32	GIC500_GICD_IROUTER_LOWER66	0180 6210h
6214h	32	GIC500_GICD_IROUTER_UPPER66	0180 6214h
6218h	32	GIC500_GICD_IROUTER_LOWER67	0180 6218h
621Ch	32	GIC500_GICD_IROUTER_UPPER67	0180 621Ch
6220h	32	GIC500_GICD_IROUTER_LOWER68	0180 6220h
6224h	32	GIC500_GICD_IROUTER_UPPER68	0180 6224h
6228h	32	GIC500_GICD_IROUTER_LOWER69	0180 6228h
622Ch	32	GIC500_GICD_IROUTER_UPPER69	0180 622Ch
6230h	32	GIC500_GICD_IROUTER_LOWER70	0180 6230h
6234h	32	GIC500_GICD_IROUTER_UPPER70	0180 6234h
6238h	32	GIC500_GICD_IROUTER_LOWER71	0180 6238h
623Ch	32	GIC500_GICD_IROUTER_UPPER71	0180 623Ch
6240h	32	GIC500_GICD_IROUTER_LOWER72	0180 6240h
6244h	32	GIC500_GICD_IROUTER_UPPER72	0180 6244h
6248h	32	GIC500_GICD_IROUTER_LOWER73	0180 6248h
624Ch	32	GIC500_GICD_IROUTER_UPPER73	0180 624Ch
6250h	32	GIC500_GICD_IROUTER_LOWER74	0180 6250h
6254h	32	GIC500_GICD_IROUTER_UPPER74	0180 6254h
6258h	32	GIC500_GICD_IROUTER_LOWER75	0180 6258h
625Ch	32	GIC500_GICD_IROUTER_UPPER75	0180 625Ch
6260h	32	GIC500_GICD_IROUTER_LOWER76	0180 6260h
6264h	32	GIC500_GICD_IROUTER_UPPER76	0180 6264h
6268h	32	GIC500_GICD_IROUTER_LOWER77	0180 6268h
626Ch	32	GIC500_GICD_IROUTER_UPPER77	0180 626Ch
6270h	32	GIC500_GICD_IROUTER_LOWER78	0180 6270h
6274h	32	GIC500_GICD_IROUTER_UPPER78	0180 6274h
6278h	32	GIC500_GICD_IROUTER_LOWER79	0180 6278h
627Ch	32	GIC500_GICD_IROUTER_UPPER79	0180 627Ch
6280h	32	GIC500_GICD_IROUTER_LOWER80	0180 6280h
6284h	32	GIC500_GICD_IROUTER_UPPER80	0180 6284h
6288h	32	GIC500_GICD_IROUTER_LOWER81	0180 6288h
628Ch	32	GIC500_GICD_IROUTER_UPPER81	0180 628Ch
6290h	32	GIC500_GICD_IROUTER_LOWER82	0180 6290h
6294h	32	GIC500_GICD_IROUTER_UPPER82	0180 6294h
6298h	32	GIC500_GICD_IROUTER_LOWER83	0180 6298h
629Ch	32	GIC500_GICD_IROUTER_UPPER83	0180 629Ch
62A0h	32	GIC500_GICD_IROUTER_LOWER84	0180 62A0h
62A4h	32	GIC500_GICD_IROUTER_UPPER84	0180 62A4h
62A8h	32	GIC500_GICD_IROUTER_LOWER85	0180 62A8h
62ACh	32	GIC500_GICD_IROUTER_UPPER85	0180 62ACh
62B0h	32	GIC500_GICD_IROUTER_LOWER86	0180 62B0h
62B4h	32	GIC500_GICD_IROUTER_UPPER86	0180 62B4h
62B8h	32	GIC500_GICD_IROUTER_LOWER87	0180 62B8h
62BCh	32	GIC500_GICD_IROUTER_UPPER87	0180 62BCh
62C0h	32	GIC500_GICD_IROUTER_LOWER88	0180 62C0h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
62C4h	32	GIC500_GICD_IROUTER_UPPER88	0180 62C4h
62C8h	32	GIC500_GICD_IROUTER_LOWER89	0180 62C8h
62CCh	32	GIC500_GICD_IROUTER_UPPER89	0180 62CCh
62D0h	32	GIC500_GICD_IROUTER_LOWER90	0180 62D0h
62D4h	32	GIC500_GICD_IROUTER_UPPER90	0180 62D4h
62D8h	32	GIC500_GICD_IROUTER_LOWER91	0180 62D8h
62DCh	32	GIC500_GICD_IROUTER_UPPER91	0180 62DCh
62E0h	32	GIC500_GICD_IROUTER_LOWER92	0180 62E0h
62E4h	32	GIC500_GICD_IROUTER_UPPER92	0180 62E4h
62E8h	32	GIC500_GICD_IROUTER_LOWER93	0180 62E8h
62ECh	32	GIC500_GICD_IROUTER_UPPER93	0180 62ECh
62F0h	32	GIC500_GICD_IROUTER_LOWER94	0180 62F0h
62F4h	32	GIC500_GICD_IROUTER_UPPER94	0180 62F4h
62F8h	32	GIC500_GICD_IROUTER_LOWER95	0180 62F8h
62FCh	32	GIC500_GICD_IROUTER_UPPER95	0180 62FCh
6300h	32	GIC500_GICD_IROUTER_LOWER96	0180 6300h
6304h	32	GIC500_GICD_IROUTER_UPPER96	0180 6304h
6308h	32	GIC500_GICD_IROUTER_LOWER97	0180 6308h
630Ch	32	GIC500_GICD_IROUTER_UPPER97	0180 630Ch
6310h	32	GIC500_GICD_IROUTER_LOWER98	0180 6310h
6314h	32	GIC500_GICD_IROUTER_UPPER98	0180 6314h
6318h	32	GIC500_GICD_IROUTER_LOWER99	0180 6318h
631Ch	32	GIC500_GICD_IROUTER_UPPER99	0180 631Ch
6320h	32	GIC500_GICD_IROUTER_LOWER100	0180 6320h
6324h	32	GIC500_GICD_IROUTER_UPPER100	0180 6324h
6328h	32	GIC500_GICD_IROUTER_LOWER101	0180 6328h
632Ch	32	GIC500_GICD_IROUTER_UPPER101	0180 632Ch
6330h	32	GIC500_GICD_IROUTER_LOWER102	0180 6330h
6334h	32	GIC500_GICD_IROUTER_UPPER102	0180 6334h
6338h	32	GIC500_GICD_IROUTER_LOWER103	0180 6338h
633Ch	32	GIC500_GICD_IROUTER_UPPER103	0180 633Ch
6340h	32	GIC500_GICD_IROUTER_LOWER104	0180 6340h
6344h	32	GIC500_GICD_IROUTER_UPPER104	0180 6344h
6348h	32	GIC500_GICD_IROUTER_LOWER105	0180 6348h
634Ch	32	GIC500_GICD_IROUTER_UPPER105	0180 634Ch
6350h	32	GIC500_GICD_IROUTER_LOWER106	0180 6350h
6354h	32	GIC500_GICD_IROUTER_UPPER106	0180 6354h
6358h	32	GIC500_GICD_IROUTER_LOWER107	0180 6358h
635Ch	32	GIC500_GICD_IROUTER_UPPER107	0180 635Ch
6360h	32	GIC500_GICD_IROUTER_LOWER108	0180 6360h
6364h	32	GIC500_GICD_IROUTER_UPPER108	0180 6364h
6368h	32	GIC500_GICD_IROUTER_LOWER109	0180 6368h
636Ch	32	GIC500_GICD_IROUTER_UPPER109	0180 636Ch
6370h	32	GIC500_GICD_IROUTER_LOWER110	0180 6370h
6374h	32	GIC500_GICD_IROUTER_UPPER110	0180 6374h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
6378h	32	GIC500_GICD_IROUTER_LOWER111	0180 6378h
637Ch	32	GIC500_GICD_IROUTER_UPPER111	0180 637Ch
6380h	32	GIC500_GICD_IROUTER_LOWER112	0180 6380h
6384h	32	GIC500_GICD_IROUTER_UPPER112	0180 6384h
6388h	32	GIC500_GICD_IROUTER_LOWER113	0180 6388h
638Ch	32	GIC500_GICD_IROUTER_UPPER113	0180 638Ch
6390h	32	GIC500_GICD_IROUTER_LOWER114	0180 6390h
6394h	32	GIC500_GICD_IROUTER_UPPER114	0180 6394h
6398h	32	GIC500_GICD_IROUTER_LOWER115	0180 6398h
639Ch	32	GIC500_GICD_IROUTER_UPPER115	0180 639Ch
63A0h	32	GIC500_GICD_IROUTER_LOWER116	0180 63A0h
63A4h	32	GIC500_GICD_IROUTER_UPPER116	0180 63A4h
63A8h	32	GIC500_GICD_IROUTER_LOWER117	0180 63A8h
63ACh	32	GIC500_GICD_IROUTER_UPPER117	0180 63ACh
63B0h	32	GIC500_GICD_IROUTER_LOWER118	0180 63B0h
63B4h	32	GIC500_GICD_IROUTER_UPPER118	0180 63B4h
63B8h	32	GIC500_GICD_IROUTER_LOWER119	0180 63B8h
63BCh	32	GIC500_GICD_IROUTER_UPPER119	0180 63BCh
63C0h	32	GIC500_GICD_IROUTER_LOWER120	0180 63C0h
63C4h	32	GIC500_GICD_IROUTER_UPPER120	0180 63C4h
63C8h	32	GIC500_GICD_IROUTER_LOWER121	0180 63C8h
63CCh	32	GIC500_GICD_IROUTER_UPPER121	0180 63CCh
63D0h	32	GIC500_GICD_IROUTER_LOWER122	0180 63D0h
63D4h	32	GIC500_GICD_IROUTER_UPPER122	0180 63D4h
63D8h	32	GIC500_GICD_IROUTER_LOWER123	0180 63D8h
63DCh	32	GIC500_GICD_IROUTER_UPPER123	0180 63DCh
63E0h	32	GIC500_GICD_IROUTER_LOWER124	0180 63E0h
63E4h	32	GIC500_GICD_IROUTER_UPPER124	0180 63E4h
63E8h	32	GIC500_GICD_IROUTER_LOWER125	0180 63E8h
63ECh	32	GIC500_GICD_IROUTER_UPPER125	0180 63ECh
63F0h	32	GIC500_GICD_IROUTER_LOWER126	0180 63F0h
63F4h	32	GIC500_GICD_IROUTER_UPPER126	0180 63F4h
63F8h	32	GIC500_GICD_IROUTER_LOWER127	0180 63F8h
63FCh	32	GIC500_GICD_IROUTER_UPPER127	0180 63FCh
6400h	32	GIC500_GICD_IROUTER_LOWER128	0180 6400h
6404h	32	GIC500_GICD_IROUTER_UPPER128	0180 6404h
6408h	32	GIC500_GICD_IROUTER_LOWER129	0180 6408h
640Ch	32	GIC500_GICD_IROUTER_UPPER129	0180 640Ch
6410h	32	GIC500_GICD_IROUTER_LOWER130	0180 6410h
6414h	32	GIC500_GICD_IROUTER_UPPER130	0180 6414h
6418h	32	GIC500_GICD_IROUTER_LOWER131	0180 6418h
641Ch	32	GIC500_GICD_IROUTER_UPPER131	0180 641Ch
6420h	32	GIC500_GICD_IROUTER_LOWER132	0180 6420h
6424h	32	GIC500_GICD_IROUTER_UPPER132	0180 6424h
6428h	32	GIC500_GICD_IROUTER_LOWER133	0180 6428h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
642Ch	32	GIC500_GICD_IROUTER_UPPER133	0180 642Ch
6430h	32	GIC500_GICD_IROUTER_LOWER134	0180 6430h
6434h	32	GIC500_GICD_IROUTER_UPPER134	0180 6434h
6438h	32	GIC500_GICD_IROUTER_LOWER135	0180 6438h
643Ch	32	GIC500_GICD_IROUTER_UPPER135	0180 643Ch
6440h	32	GIC500_GICD_IROUTER_LOWER136	0180 6440h
6444h	32	GIC500_GICD_IROUTER_UPPER136	0180 6444h
6448h	32	GIC500_GICD_IROUTER_LOWER137	0180 6448h
644Ch	32	GIC500_GICD_IROUTER_UPPER137	0180 644Ch
6450h	32	GIC500_GICD_IROUTER_LOWER138	0180 6450h
6454h	32	GIC500_GICD_IROUTER_UPPER138	0180 6454h
6458h	32	GIC500_GICD_IROUTER_LOWER139	0180 6458h
645Ch	32	GIC500_GICD_IROUTER_UPPER139	0180 645Ch
6460h	32	GIC500_GICD_IROUTER_LOWER140	0180 6460h
6464h	32	GIC500_GICD_IROUTER_UPPER140	0180 6464h
6468h	32	GIC500_GICD_IROUTER_LOWER141	0180 6468h
646Ch	32	GIC500_GICD_IROUTER_UPPER141	0180 646Ch
6470h	32	GIC500_GICD_IROUTER_LOWER142	0180 6470h
6474h	32	GIC500_GICD_IROUTER_UPPER142	0180 6474h
6478h	32	GIC500_GICD_IROUTER_LOWER143	0180 6478h
647Ch	32	GIC500_GICD_IROUTER_UPPER143	0180 647Ch
6480h	32	GIC500_GICD_IROUTER_LOWER144	0180 6480h
6484h	32	GIC500_GICD_IROUTER_UPPER144	0180 6484h
6488h	32	GIC500_GICD_IROUTER_LOWER145	0180 6488h
648Ch	32	GIC500_GICD_IROUTER_UPPER145	0180 648Ch
6490h	32	GIC500_GICD_IROUTER_LOWER146	0180 6490h
6494h	32	GIC500_GICD_IROUTER_UPPER146	0180 6494h
6498h	32	GIC500_GICD_IROUTER_LOWER147	0180 6498h
649Ch	32	GIC500_GICD_IROUTER_UPPER147	0180 649Ch
64A0h	32	GIC500_GICD_IROUTER_LOWER148	0180 64A0h
64A4h	32	GIC500_GICD_IROUTER_UPPER148	0180 64A4h
64A8h	32	GIC500_GICD_IROUTER_LOWER149	0180 64A8h
64ACh	32	GIC500_GICD_IROUTER_UPPER149	0180 64ACh
64B0h	32	GIC500_GICD_IROUTER_LOWER150	0180 64B0h
64B4h	32	GIC500_GICD_IROUTER_UPPER150	0180 64B4h
64B8h	32	GIC500_GICD_IROUTER_LOWER151	0180 64B8h
64BCh	32	GIC500_GICD_IROUTER_UPPER151	0180 64BCh
64C0h	32	GIC500_GICD_IROUTER_LOWER152	0180 64C0h
64C4h	32	GIC500_GICD_IROUTER_UPPER152	0180 64C4h
64C8h	32	GIC500_GICD_IROUTER_LOWER153	0180 64C8h
64CCh	32	GIC500_GICD_IROUTER_UPPER153	0180 64CCh
64D0h	32	GIC500_GICD_IROUTER_LOWER154	0180 64D0h
64D4h	32	GIC500_GICD_IROUTER_UPPER154	0180 64D4h
64D8h	32	GIC500_GICD_IROUTER_LOWER155	0180 64D8h
64DCh	32	GIC500_GICD_IROUTER_UPPER155	0180 64DCh

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
64E0h	32	GIC500_GICD_IROUTER_LOWER156	0180 64E0h
64E4h	32	GIC500_GICD_IROUTER_UPPER156	0180 64E4h
64E8h	32	GIC500_GICD_IROUTER_LOWER157	0180 64E8h
64ECh	32	GIC500_GICD_IROUTER_UPPER157	0180 64ECh
64F0h	32	GIC500_GICD_IROUTER_LOWER158	0180 64F0h
64F4h	32	GIC500_GICD_IROUTER_UPPER158	0180 64F4h
64F8h	32	GIC500_GICD_IROUTER_LOWER159	0180 64F8h
64FCh	32	GIC500_GICD_IROUTER_UPPER159	0180 64FCh
6500h	32	GIC500_GICD_IROUTER_LOWER160	0180 6500h
6504h	32	GIC500_GICD_IROUTER_UPPER160	0180 6504h
6508h	32	GIC500_GICD_IROUTER_LOWER161	0180 6508h
650Ch	32	GIC500_GICD_IROUTER_UPPER161	0180 650Ch
6510h	32	GIC500_GICD_IROUTER_LOWER162	0180 6510h
6514h	32	GIC500_GICD_IROUTER_UPPER162	0180 6514h
6518h	32	GIC500_GICD_IROUTER_LOWER163	0180 6518h
651Ch	32	GIC500_GICD_IROUTER_UPPER163	0180 651Ch
6520h	32	GIC500_GICD_IROUTER_LOWER164	0180 6520h
6524h	32	GIC500_GICD_IROUTER_UPPER164	0180 6524h
6528h	32	GIC500_GICD_IROUTER_LOWER165	0180 6528h
652Ch	32	GIC500_GICD_IROUTER_UPPER165	0180 652Ch
6530h	32	GIC500_GICD_IROUTER_LOWER166	0180 6530h
6534h	32	GIC500_GICD_IROUTER_UPPER166	0180 6534h
6538h	32	GIC500_GICD_IROUTER_LOWER167	0180 6538h
653Ch	32	GIC500_GICD_IROUTER_UPPER167	0180 653Ch
6540h	32	GIC500_GICD_IROUTER_LOWER168	0180 6540h
6544h	32	GIC500_GICD_IROUTER_UPPER168	0180 6544h
6548h	32	GIC500_GICD_IROUTER_LOWER169	0180 6548h
654Ch	32	GIC500_GICD_IROUTER_UPPER169	0180 654Ch
6550h	32	GIC500_GICD_IROUTER_LOWER170	0180 6550h
6554h	32	GIC500_GICD_IROUTER_UPPER170	0180 6554h
6558h	32	GIC500_GICD_IROUTER_LOWER171	0180 6558h
655Ch	32	GIC500_GICD_IROUTER_UPPER171	0180 655Ch
6560h	32	GIC500_GICD_IROUTER_LOWER172	0180 6560h
6564h	32	GIC500_GICD_IROUTER_UPPER172	0180 6564h
6568h	32	GIC500_GICD_IROUTER_LOWER173	0180 6568h
656Ch	32	GIC500_GICD_IROUTER_UPPER173	0180 656Ch
6570h	32	GIC500_GICD_IROUTER_LOWER174	0180 6570h
6574h	32	GIC500_GICD_IROUTER_UPPER174	0180 6574h
6578h	32	GIC500_GICD_IROUTER_LOWER175	0180 6578h
657Ch	32	GIC500_GICD_IROUTER_UPPER175	0180 657Ch
6580h	32	GIC500_GICD_IROUTER_LOWER176	0180 6580h
6584h	32	GIC500_GICD_IROUTER_UPPER176	0180 6584h
6588h	32	GIC500_GICD_IROUTER_LOWER177	0180 6588h
658Ch	32	GIC500_GICD_IROUTER_UPPER177	0180 658Ch
6590h	32	GIC500_GICD_IROUTER_LOWER178	0180 6590h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
6594h	32	GIC500_GICD_IROUTER_UPPER178	0180 6594h
6598h	32	GIC500_GICD_IROUTER_LOWER179	0180 6598h
659Ch	32	GIC500_GICD_IROUTER_UPPER179	0180 659Ch
65A0h	32	GIC500_GICD_IROUTER_LOWER180	0180 65A0h
65A4h	32	GIC500_GICD_IROUTER_UPPER180	0180 65A4h
65A8h	32	GIC500_GICD_IROUTER_LOWER181	0180 65A8h
65ACh	32	GIC500_GICD_IROUTER_UPPER181	0180 65ACh
65B0h	32	GIC500_GICD_IROUTER_LOWER182	0180 65B0h
65B4h	32	GIC500_GICD_IROUTER_UPPER182	0180 65B4h
65B8h	32	GIC500_GICD_IROUTER_LOWER183	0180 65B8h
65BCh	32	GIC500_GICD_IROUTER_UPPER183	0180 65BCh
65C0h	32	GIC500_GICD_IROUTER_LOWER184	0180 65C0h
65C4h	32	GIC500_GICD_IROUTER_UPPER184	0180 65C4h
65C8h	32	GIC500_GICD_IROUTER_LOWER185	0180 65C8h
65CCh	32	GIC500_GICD_IROUTER_UPPER185	0180 65CCh
65D0h	32	GIC500_GICD_IROUTER_LOWER186	0180 65D0h
65D4h	32	GIC500_GICD_IROUTER_UPPER186	0180 65D4h
65D8h	32	GIC500_GICD_IROUTER_LOWER187	0180 65D8h
65DCh	32	GIC500_GICD_IROUTER_UPPER187	0180 65DCh
65E0h	32	GIC500_GICD_IROUTER_LOWER188	0180 65E0h
65E4h	32	GIC500_GICD_IROUTER_UPPER188	0180 65E4h
65E8h	32	GIC500_GICD_IROUTER_LOWER189	0180 65E8h
65ECh	32	GIC500_GICD_IROUTER_UPPER189	0180 65ECh
65F0h	32	GIC500_GICD_IROUTER_LOWER190	0180 65F0h
65F4h	32	GIC500_GICD_IROUTER_UPPER190	0180 65F4h
65F8h	32	GIC500_GICD_IROUTER_LOWER191	0180 65F8h
65FCh	32	GIC500_GICD_IROUTER_UPPER191	0180 65FCh
6600h	32	GIC500_GICD_IROUTER_LOWER192	0180 6600h
6604h	32	GIC500_GICD_IROUTER_UPPER192	0180 6604h
6608h	32	GIC500_GICD_IROUTER_LOWER193	0180 6608h
660Ch	32	GIC500_GICD_IROUTER_UPPER193	0180 660Ch
6610h	32	GIC500_GICD_IROUTER_LOWER194	0180 6610h
6614h	32	GIC500_GICD_IROUTER_UPPER194	0180 6614h
6618h	32	GIC500_GICD_IROUTER_LOWER195	0180 6618h
661Ch	32	GIC500_GICD_IROUTER_UPPER195	0180 661Ch
6620h	32	GIC500_GICD_IROUTER_LOWER196	0180 6620h
6624h	32	GIC500_GICD_IROUTER_UPPER196	0180 6624h
6628h	32	GIC500_GICD_IROUTER_LOWER197	0180 6628h
662Ch	32	GIC500_GICD_IROUTER_UPPER197	0180 662Ch
6630h	32	GIC500_GICD_IROUTER_LOWER198	0180 6630h
6634h	32	GIC500_GICD_IROUTER_UPPER198	0180 6634h
6638h	32	GIC500_GICD_IROUTER_LOWER199	0180 6638h
663Ch	32	GIC500_GICD_IROUTER_UPPER199	0180 663Ch
6640h	32	GIC500_GICD_IROUTER_LOWER200	0180 6640h
6644h	32	GIC500_GICD_IROUTER_UPPER200	0180 6644h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
6648h	32	GIC500_GICD_IROUTER_LOWER201	0180 6648h
664Ch	32	GIC500_GICD_IROUTER_UPPER201	0180 664Ch
6650h	32	GIC500_GICD_IROUTER_LOWER202	0180 6650h
6654h	32	GIC500_GICD_IROUTER_UPPER202	0180 6654h
6658h	32	GIC500_GICD_IROUTER_LOWER203	0180 6658h
665Ch	32	GIC500_GICD_IROUTER_UPPER203	0180 665Ch
6660h	32	GIC500_GICD_IROUTER_LOWER204	0180 6660h
6664h	32	GIC500_GICD_IROUTER_UPPER204	0180 6664h
6668h	32	GIC500_GICD_IROUTER_LOWER205	0180 6668h
666Ch	32	GIC500_GICD_IROUTER_UPPER205	0180 666Ch
6670h	32	GIC500_GICD_IROUTER_LOWER206	0180 6670h
6674h	32	GIC500_GICD_IROUTER_UPPER206	0180 6674h
6678h	32	GIC500_GICD_IROUTER_LOWER207	0180 6678h
667Ch	32	GIC500_GICD_IROUTER_UPPER207	0180 667Ch
6680h	32	GIC500_GICD_IROUTER_LOWER208	0180 6680h
6684h	32	GIC500_GICD_IROUTER_UPPER208	0180 6684h
6688h	32	GIC500_GICD_IROUTER_LOWER209	0180 6688h
668Ch	32	GIC500_GICD_IROUTER_UPPER209	0180 668Ch
6690h	32	GIC500_GICD_IROUTER_LOWER210	0180 6690h
6694h	32	GIC500_GICD_IROUTER_UPPER210	0180 6694h
6698h	32	GIC500_GICD_IROUTER_LOWER211	0180 6698h
669Ch	32	GIC500_GICD_IROUTER_UPPER211	0180 669Ch
66A0h	32	GIC500_GICD_IROUTER_LOWER212	0180 66A0h
66A4h	32	GIC500_GICD_IROUTER_UPPER212	0180 66A4h
66A8h	32	GIC500_GICD_IROUTER_LOWER213	0180 66A8h
66ACh	32	GIC500_GICD_IROUTER_UPPER213	0180 66ACh
66B0h	32	GIC500_GICD_IROUTER_LOWER214	0180 66B0h
66B4h	32	GIC500_GICD_IROUTER_UPPER214	0180 66B4h
66B8h	32	GIC500_GICD_IROUTER_LOWER215	0180 66B8h
66BCh	32	GIC500_GICD_IROUTER_UPPER215	0180 66BCh
66C0h	32	GIC500_GICD_IROUTER_LOWER216	0180 66C0h
66C4h	32	GIC500_GICD_IROUTER_UPPER216	0180 66C4h
66C8h	32	GIC500_GICD_IROUTER_LOWER217	0180 66C8h
66CCh	32	GIC500_GICD_IROUTER_UPPER217	0180 66CCh
66D0h	32	GIC500_GICD_IROUTER_LOWER218	0180 66D0h
66D4h	32	GIC500_GICD_IROUTER_UPPER218	0180 66D4h
66D8h	32	GIC500_GICD_IROUTER_LOWER219	0180 66D8h
66DCh	32	GIC500_GICD_IROUTER_UPPER219	0180 66DCh
66E0h	32	GIC500_GICD_IROUTER_LOWER220	0180 66E0h
66E4h	32	GIC500_GICD_IROUTER_UPPER220	0180 66E4h
66E8h	32	GIC500_GICD_IROUTER_LOWER221	0180 66E8h
66ECh	32	GIC500_GICD_IROUTER_UPPER221	0180 66ECh
66F0h	32	GIC500_GICD_IROUTER_LOWER222	0180 66F0h
66F4h	32	GIC500_GICD_IROUTER_UPPER222	0180 66F4h
66F8h	32	GIC500_GICD_IROUTER_LOWER223	0180 66F8h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
66FCh	32	GIC500_GICD_IROUTER_UPPER223	0180 66FCh
6700h	32	GIC500_GICD_IROUTER_LOWER224	0180 6700h
6704h	32	GIC500_GICD_IROUTER_UPPER224	0180 6704h
6708h	32	GIC500_GICD_IROUTER_LOWER225	0180 6708h
670Ch	32	GIC500_GICD_IROUTER_UPPER225	0180 670Ch
6710h	32	GIC500_GICD_IROUTER_LOWER226	0180 6710h
6714h	32	GIC500_GICD_IROUTER_UPPER226	0180 6714h
6718h	32	GIC500_GICD_IROUTER_LOWER227	0180 6718h
671Ch	32	GIC500_GICD_IROUTER_UPPER227	0180 671Ch
6720h	32	GIC500_GICD_IROUTER_LOWER228	0180 6720h
6724h	32	GIC500_GICD_IROUTER_UPPER228	0180 6724h
6728h	32	GIC500_GICD_IROUTER_LOWER229	0180 6728h
672Ch	32	GIC500_GICD_IROUTER_UPPER229	0180 672Ch
6730h	32	GIC500_GICD_IROUTER_LOWER230	0180 6730h
6734h	32	GIC500_GICD_IROUTER_UPPER230	0180 6734h
6738h	32	GIC500_GICD_IROUTER_LOWER231	0180 6738h
673Ch	32	GIC500_GICD_IROUTER_UPPER231	0180 673Ch
6740h	32	GIC500_GICD_IROUTER_LOWER232	0180 6740h
6744h	32	GIC500_GICD_IROUTER_UPPER232	0180 6744h
6748h	32	GIC500_GICD_IROUTER_LOWER233	0180 6748h
674Ch	32	GIC500_GICD_IROUTER_UPPER233	0180 674Ch
6750h	32	GIC500_GICD_IROUTER_LOWER234	0180 6750h
6754h	32	GIC500_GICD_IROUTER_UPPER234	0180 6754h
6758h	32	GIC500_GICD_IROUTER_LOWER235	0180 6758h
675Ch	32	GIC500_GICD_IROUTER_UPPER235	0180 675Ch
6760h	32	GIC500_GICD_IROUTER_LOWER236	0180 6760h
6764h	32	GIC500_GICD_IROUTER_UPPER236	0180 6764h
6768h	32	GIC500_GICD_IROUTER_LOWER237	0180 6768h
676Ch	32	GIC500_GICD_IROUTER_UPPER237	0180 676Ch
6770h	32	GIC500_GICD_IROUTER_LOWER238	0180 6770h
6774h	32	GIC500_GICD_IROUTER_UPPER238	0180 6774h
6778h	32	GIC500_GICD_IROUTER_LOWER239	0180 6778h
677Ch	32	GIC500_GICD_IROUTER_UPPER239	0180 677Ch
6780h	32	GIC500_GICD_IROUTER_LOWER240	0180 6780h
6784h	32	GIC500_GICD_IROUTER_UPPER240	0180 6784h
6788h	32	GIC500_GICD_IROUTER_LOWER241	0180 6788h
678Ch	32	GIC500_GICD_IROUTER_UPPER241	0180 678Ch
6790h	32	GIC500_GICD_IROUTER_LOWER242	0180 6790h
6794h	32	GIC500_GICD_IROUTER_UPPER242	0180 6794h
6798h	32	GIC500_GICD_IROUTER_LOWER243	0180 6798h
679Ch	32	GIC500_GICD_IROUTER_UPPER243	0180 679Ch
67A0h	32	GIC500_GICD_IROUTER_LOWER244	0180 67A0h
67A4h	32	GIC500_GICD_IROUTER_UPPER244	0180 67A4h
67A8h	32	GIC500_GICD_IROUTER_LOWER245	0180 67A8h
67ACh	32	GIC500_GICD_IROUTER_UPPER245	0180 67ACh

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
67B0h	32	GIC500_GICD_IROUTER_LOWER246	0180 67B0h
67B4h	32	GIC500_GICD_IROUTER_UPPER246	0180 67B4h
67B8h	32	GIC500_GICD_IROUTER_LOWER247	0180 67B8h
67BCh	32	GIC500_GICD_IROUTER_UPPER247	0180 67BCh
67C0h	32	GIC500_GICD_IROUTER_LOWER248	0180 67C0h
67C4h	32	GIC500_GICD_IROUTER_UPPER248	0180 67C4h
67C8h	32	GIC500_GICD_IROUTER_LOWER249	0180 67C8h
67CCh	32	GIC500_GICD_IROUTER_UPPER249	0180 67CCh
67D0h	32	GIC500_GICD_IROUTER_LOWER250	0180 67D0h
67D4h	32	GIC500_GICD_IROUTER_UPPER250	0180 67D4h
67D8h	32	GIC500_GICD_IROUTER_LOWER251	0180 67D8h
67DCh	32	GIC500_GICD_IROUTER_UPPER251	0180 67DCh
67E0h	32	GIC500_GICD_IROUTER_LOWER252	0180 67E0h
67E4h	32	GIC500_GICD_IROUTER_UPPER252	0180 67E4h
67E8h	32	GIC500_GICD_IROUTER_LOWER253	0180 67E8h
67ECh	32	GIC500_GICD_IROUTER_UPPER253	0180 67ECh
67F0h	32	GIC500_GICD_IROUTER_LOWER254	0180 67F0h
67F4h	32	GIC500_GICD_IROUTER_UPPER254	0180 67F4h
67F8h	32	GIC500_GICD_IROUTER_LOWER255	0180 67F8h
67FCh	32	GIC500_GICD_IROUTER_UPPER255	0180 67FCh
6800h	32	GIC500_GICD_IROUTER_LOWER256	0180 6800h
6804h	32	GIC500_GICD_IROUTER_UPPER256	0180 6804h
6808h	32	GIC500_GICD_IROUTER_LOWER257	0180 6808h
680Ch	32	GIC500_GICD_IROUTER_UPPER257	0180 680Ch
6810h	32	GIC500_GICD_IROUTER_LOWER258	0180 6810h
6814h	32	GIC500_GICD_IROUTER_UPPER258	0180 6814h
6818h	32	GIC500_GICD_IROUTER_LOWER259	0180 6818h
681Ch	32	GIC500_GICD_IROUTER_UPPER259	0180 681Ch
6820h	32	GIC500_GICD_IROUTER_LOWER260	0180 6820h
6824h	32	GIC500_GICD_IROUTER_UPPER260	0180 6824h
6828h	32	GIC500_GICD_IROUTER_LOWER261	0180 6828h
682Ch	32	GIC500_GICD_IROUTER_UPPER261	0180 682Ch
6830h	32	GIC500_GICD_IROUTER_LOWER262	0180 6830h
6834h	32	GIC500_GICD_IROUTER_UPPER262	0180 6834h
6838h	32	GIC500_GICD_IROUTER_LOWER263	0180 6838h
683Ch	32	GIC500_GICD_IROUTER_UPPER263	0180 683Ch
6840h	32	GIC500_GICD_IROUTER_LOWER264	0180 6840h
6844h	32	GIC500_GICD_IROUTER_UPPER264	0180 6844h
6848h	32	GIC500_GICD_IROUTER_LOWER265	0180 6848h
684Ch	32	GIC500_GICD_IROUTER_UPPER265	0180 684Ch
6850h	32	GIC500_GICD_IROUTER_LOWER266	0180 6850h
6854h	32	GIC500_GICD_IROUTER_UPPER266	0180 6854h
6858h	32	GIC500_GICD_IROUTER_LOWER267	0180 6858h
685Ch	32	GIC500_GICD_IROUTER_UPPER267	0180 685Ch
6860h	32	GIC500_GICD_IROUTER_LOWER268	0180 6860h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
6864h	32	GIC500_GICD_IROUTER_UPPER268	0180 6864h
6868h	32	GIC500_GICD_IROUTER_LOWER269	0180 6868h
686Ch	32	GIC500_GICD_IROUTER_UPPER269	0180 686Ch
6870h	32	GIC500_GICD_IROUTER_LOWER270	0180 6870h
6874h	32	GIC500_GICD_IROUTER_UPPER270	0180 6874h
6878h	32	GIC500_GICD_IROUTER_LOWER271	0180 6878h
687Ch	32	GIC500_GICD_IROUTER_UPPER271	0180 687Ch
6880h	32	GIC500_GICD_IROUTER_LOWER272	0180 6880h
6884h	32	GIC500_GICD_IROUTER_UPPER272	0180 6884h
6888h	32	GIC500_GICD_IROUTER_LOWER273	0180 6888h
688Ch	32	GIC500_GICD_IROUTER_UPPER273	0180 688Ch
6890h	32	GIC500_GICD_IROUTER_LOWER274	0180 6890h
6894h	32	GIC500_GICD_IROUTER_UPPER274	0180 6894h
6898h	32	GIC500_GICD_IROUTER_LOWER275	0180 6898h
689Ch	32	GIC500_GICD_IROUTER_UPPER275	0180 689Ch
68A0h	32	GIC500_GICD_IROUTER_LOWER276	0180 68A0h
68A4h	32	GIC500_GICD_IROUTER_UPPER276	0180 68A4h
68A8h	32	GIC500_GICD_IROUTER_LOWER277	0180 68A8h
68ACh	32	GIC500_GICD_IROUTER_UPPER277	0180 68ACh
68B0h	32	GIC500_GICD_IROUTER_LOWER278	0180 68B0h
68B4h	32	GIC500_GICD_IROUTER_UPPER278	0180 68B4h
68B8h	32	GIC500_GICD_IROUTER_LOWER279	0180 68B8h
68BCh	32	GIC500_GICD_IROUTER_UPPER279	0180 68BCh
68C0h	32	GIC500_GICD_IROUTER_LOWER280	0180 68C0h
68C4h	32	GIC500_GICD_IROUTER_UPPER280	0180 68C4h
68C8h	32	GIC500_GICD_IROUTER_LOWER281	0180 68C8h
68CCh	32	GIC500_GICD_IROUTER_UPPER281	0180 68CCh
68D0h	32	GIC500_GICD_IROUTER_LOWER282	0180 68D0h
68D4h	32	GIC500_GICD_IROUTER_UPPER282	0180 68D4h
68D8h	32	GIC500_GICD_IROUTER_LOWER283	0180 68D8h
68DCh	32	GIC500_GICD_IROUTER_UPPER283	0180 68DCh
68E0h	32	GIC500_GICD_IROUTER_LOWER284	0180 68E0h
68E4h	32	GIC500_GICD_IROUTER_UPPER284	0180 68E4h
68E8h	32	GIC500_GICD_IROUTER_LOWER285	0180 68E8h
68ECh	32	GIC500_GICD_IROUTER_UPPER285	0180 68ECh
68F0h	32	GIC500_GICD_IROUTER_LOWER286	0180 68F0h
68F4h	32	GIC500_GICD_IROUTER_UPPER286	0180 68F4h
68F8h	32	GIC500_GICD_IROUTER_LOWER287	0180 68F8h
68FCh	32	GIC500_GICD_IROUTER_UPPER287	0180 68FCh
C000h	32	GIC500_GICD_ESTATUSR	0180 C000h
C004h	32	GIC500_GICD_ERRTESTR	0180 C004h
C084h	32	GIC500_GICD_SPISR0	0180 C084h
C088h	32	GIC500_GICD_SPISR1	0180 C088h
C08Ch	32	GIC500_GICD_SPISR2	0180 C08Ch
C090h	32	GIC500_GICD_SPISR3	0180 C090h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
C094h	32	GIC500_GICD_SPISR4	0180 C094h
C098h	32	GIC500_GICD_SPISR5	0180 C098h
C09Ch	32	GIC500_GICD_SPISR6	0180 C09Ch
C0A0h	32	GIC500_GICD_SPISR7	0180 C0A0h
FFD0h	32	GIC500_GICD_PIDR4	0180 FFD0h
FFD4h	32	GIC500_GICD_PIDR5	0180 FFD4h
FFD8h	32	GIC500_GICD_PIDR6	0180 FFD8h
FFDCh	32	GIC500_GICD_PIDR7	0180 FFDCh
FFE0h	32	GIC500_GICD_PIDR0	0180 FFE0h
FFE4h	32	GIC500_GICD_PIDR1	0180 FFE4h
FFE8h	32	GIC500_GICD_PIDR2	0180 FFE8h
FFECh	32	GIC500_GICD_PIDR3	0180 FFECh
FFF0h	32	GIC500_GICD_CIDR0	0180 FFF0h
FFF4h	32	GIC500_GICD_CIDR1	0180 FFF4h
FFF8h	32	GIC500_GICD_CIDR2	0180 FFF8h
FFFCh	32	GIC500_GICD_CIDR3	0180 FFFCh
10040h	32	GIC500_MSG_SETSPI_NSR	0181 0040h
10048h	32	GIC500_MSG_CLRSPI_NSR	0181 0048h
10050h	32	GIC500_MSG_SETSPI_SR	0181 0050h
10058h	32	GIC500_MSG_CLRSPI_SR	0181 0058h
20000h	32	GIC500_ITS_CTLR	0182 0000h
20004h	32	GIC500_ITS_IIDR	0182 0004h
20008h	32	GIC500_ITS_TYPER_LOWER	0182 0008h
2000Ch	32	GIC500_ITS_TYPER_UPPER	0182 000Ch
20080h	32	GIC500_ITS_CBASER_LOWER	0182 0080h
20084h	32	GIC500_ITS_CBASER_UPPER	0182 0084h
20088h	32	GIC500_ITS_CWRITER_LOWER	0182 0088h
2008Ch	32	GIC500_ITS_CWRITER_UPPER	0182 008Ch
20090h	32	GIC500_ITS_CREADR_LOWER	0182 0090h
20094h	32	GIC500_ITS_CREADR_UPPER	0182 0094h
20100h	32	GIC500_ITS_BASER0_LOWER	0182 0100h
20104h	32	GIC500_ITS_BASER0_UPPER	0182 0104h
2C000h	32	GIC500_ITS_TRKCTLR	0182 C000h
2C004h	32	GIC500_ITS_TRKR	0182 C004h
2C008h	32	GIC500_ITS_TRKDIDR	0182 C008h
2C00Ch	32	GIC500_ITS_TRKPIDR	0182 C00Ch
2C010h	32	GIC500_ITS_TRKVIDR	0182 C010h
2C014h	32	GIC500_ITS_TRKTGTR	0182 C014h
2C018h	32	GIC500_ITS_TRKICR	0182 C018h
2C01Ch	32	GIC500_ITS_TRKLCR	0182 C01Ch
2FFD0h	32	GIC500_ITS_PIDR4	0182 FFD0h
2FFD4h	32	GIC500_ITS_PIDR5	0182 FFD4h
2FFD8h	32	GIC500_ITS_PIDR6	0182 FFD8h
2FFDCh	32	GIC500_ITS_PIDR7	0182 FFDCh
2FFE0h	32	GIC500_ITS_PIDR0	0182 FFE0h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
2FFE4h	32	GIC500_ITS_PIDR1	0182 FFE4h
2FFE8h	32	GIC500_ITS_PIDR2	0182 FFE8h
2FFECh	32	GIC500_ITS_PIDR3	0182 FFECh
2FFF0h	32	GIC500_ITS_CIDR0	0182 FFF0h
2FFF4h	32	GIC500_ITS_CIDR1	0182 FFF4h
2FFF8h	32	GIC500_ITS_CIDR2	0182 FFF8h
2FFFCh	32	GIC500_ITS_CIDR3	0182 FFFCh
40000h	32	GIC500_GICR_CORE_CONTROL_CTLR_0	0184 0000h
40004h	32	GIC500_GICR_CORE_CONTROL_IIDR_0	0184 0004h
40008h	32	GIC500_GICR_CORE_CONTROL_TYPER_0_LOWER	0184 0008h
4000Ch	32	GIC500_GICR_CORE_CONTROL_TYPER_0_UPPER	0184 000Ch
40014h	32	GIC500_GICR_CORE_CONTROL_WAKER_0	0184 0014h
40070h	32	GIC500_GICR_CORE_CONTROL_PROPBASER_0_LOWER	0184 0070h
40074h	32	GIC500_GICR_CORE_CONTROL_PROPBASER_0_UPPER	0184 0074h
40078h	32	GIC500_GICR_CORE_CONTROL_PENDBASER_0_LOWER	0184 0078h
4007Ch	32	GIC500_GICR_CORE_CONTROL_PENDBASER_0_UPPER	0184 007Ch
4FFD0h	32	GIC500_GICR_CORE_CONTROL_PIDR4_0	0184 FFD0h
4FFD4h	32	GIC500_GICR_CORE_CONTROL_PIDR5_0	0184 FFD4h
4FFD8h	32	GIC500_GICR_CORE_CONTROL_PIDR6_0	0184 FFD8h
4FFDCh	32	GIC500_GICR_CORE_CONTROL_PIDR7_0	0184 FFDCh
4FFE0h	32	GIC500_GICR_CORE_CONTROL_PIDR0_0	0184 FFE0h
4FFE4h	32	GIC500_GICR_CORE_CONTROL_PIDR1_0	0184 FFE4h
4FFE8h	32	GIC500_GICR_CORE_CONTROL_PIDR2_0	0184 FFE8h
4FFECh	32	GIC500_GICR_CORE_CONTROL_PIDR3_0	0184 FFECh
4FFF0h	32	GIC500_GICR_CORE_CONTROL_CIDR0_0	0184 FFF0h
4FFF4h	32	GIC500_GICR_CORE_CONTROL_CIDR1_0	0184 FFF4h
4FFF8h	32	GIC500_GICR_CORE_CONTROL_CIDR2_0	0184 FFF8h
4FFFCh	32	GIC500_GICR_CORE_CONTROL_CIDR3_0	0184 FFFCh
50080h	32	GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0	0185 0080h
50100h	32	GIC500_GICR_CORE_SGI_PPI_ISENABLER00	0185 0100h
50180h	32	GIC500_GICR_CORE_SGI_PPI_ICENABLER00	0185 0180h
50200h	32	GIC500_GICR_CORE_SGI_PPI_ISPENDR00	0185 0200h
50280h	32	GIC500_GICR_CORE_SGI_PPI_ICPENDR00	0185 0280h
50300h	32	GIC500_GICR_CORE_SGI_PPI_ISACTIVER00	0185 0300h
50380h	32	GIC500_GICR_CORE_SGI_PPI_ICACTIVER00	0185 0380h
50400h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR00	0185 0400h
50404h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR10	0185 0404h
50408h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR20	0185 0408h
5040Ch	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR30	0185 040Ch
50410h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR40	0185 0410h
50414h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR50	0185 0414h
50418h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR60	0185 0418h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
5041Ch	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR70	0185 041Ch
50C00h	32	GIC500_GICR_CORE_SGI_PPI_ICFGR00	0185 0C00h
50C04h	32	GIC500_GICR_CORE_SGI_PPI_ICFGR10	0185 0C04h
50D00h	32	GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0	0185 0D00h
50E00h	32	GIC500_GICR_CORE_SGI_PPI_NSACR0	0185 0E00h
5C000h	32	GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR0	0185 C000h
5C080h	32	GIC500_GICR_CORE_SGI_PPI_PPISR0	0185 C080h
60000h	32	GIC500_GICR_CORE_CONTROL_CTLR_1	0186 0000h
60004h	32	GIC500_GICR_CORE_CONTROL_IIDR_1	0186 0004h
60008h	32	GIC500_GICR_CORE_CONTROL_TYPER_1_LOWER	0186 0008h
6000Ch	32	GIC500_GICR_CORE_CONTROL_TYPER_1_UPPER	0186 000Ch
60014h	32	GIC500_GICR_CORE_CONTROL_WAKER_1	0186 0014h
60070h	32	GIC500_GICR_CORE_CONTROL_PROPBASER_1_LOWER	0186 0070h
60074h	32	GIC500_GICR_CORE_CONTROL_PROPBASER_1_UPPER	0186 0074h
60078h	32	GIC500_GICR_CORE_CONTROL_PENDBASER_1_LOWER	0186 0078h
6007Ch	32	GIC500_GICR_CORE_CONTROL_PENDBASER_1_UPPER	0186 007Ch
6FFD0h	32	GIC500_GICR_CORE_CONTROL_PIDR4_1	0186 FFD0h
6FFD4h	32	GIC500_GICR_CORE_CONTROL_PIDR5_1	0186 FFD4h
6FFD8h	32	GIC500_GICR_CORE_CONTROL_PIDR6_1	0186 FFD8h
6FFDCh	32	GIC500_GICR_CORE_CONTROL_PIDR7_1	0186 FFDCh
6FFE0h	32	GIC500_GICR_CORE_CONTROL_PIDR0_1	0186 FFE0h
6FFE4h	32	GIC500_GICR_CORE_CONTROL_PIDR1_1	0186 FFE4h
6FFE8h	32	GIC500_GICR_CORE_CONTROL_PIDR2_1	0186 FFE8h
6FFECh	32	GIC500_GICR_CORE_CONTROL_PIDR3_1	0186 FFECh
6FFF0h	32	GIC500_GICR_CORE_CONTROL_CIDR0_1	0186 FFF0h
6FFF4h	32	GIC500_GICR_CORE_CONTROL_CIDR1_1	0186 FFF4h
6FFF8h	32	GIC500_GICR_CORE_CONTROL_CIDR2_1	0186 FFF8h
6FFFCh	32	GIC500_GICR_CORE_CONTROL_CIDR3_1	0186 FFFCh
70080h	32	GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0	0187 0080h
70100h	32	GIC500_GICR_CORE_SGI_PPI_ISENABLER01	0187 0100h
70180h	32	GIC500_GICR_CORE_SGI_PPI_ICENABLER01	0187 0180h
70200h	32	GIC500_GICR_CORE_SGI_PPI_ISPENDR01	0187 0200h
70280h	32	GIC500_GICR_CORE_SGI_PPI_ICPENDR01	0187 0280h
70300h	32	GIC500_GICR_CORE_SGI_PPI_ISACTIVER01	0187 0300h
70380h	32	GIC500_GICR_CORE_SGI_PPI_ICACTIVER01	0187 0380h
70400h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR01	0187 0400h
70404h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR11	0187 0404h
70408h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR21	0187 0408h
7040Ch	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR31	0187 040Ch
70410h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR41	0187 0410h
70414h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR51	0187 0414h
70418h	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR61	0187 0418h

Table 14-16868. GIC500 Registers, Base Address=0180 0000h, Length=1048576 (continued)

Offset	Length	Register Name	GICSS0 Physical Address
7041Ch	32	GIC500_GICR_CORE_SGI_PPI_IPRIORITYR71	0187 041Ch
70C00h	32	GIC500_GICR_CORE_SGI_PPI_ICFGR01	0187 0C00h
70C04h	32	GIC500_GICR_CORE_SGI_PPI_ICFGR11	0187 0C04h
70D00h	32	GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0	0187 0D00h
70E00h	32	GIC500_GICR_CORE_SGI_PPI_NSACR1	0187 0E00h
7C000h	32	GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR1	0187 C000h
7C080h	32	GIC500_GICR_CORE_SGI_PPI_PPISR1	0187 C080h

Table 14-16869. ECC_AGGR Registers, Base Address=3F00 4000h, Length=1024

Offset	Length	Register Name	GICSS0 Physical Address
0h	32	ECC_AGGR_REV	3F00 4000h
8h	32	ECC_AGGR_VECTOR	3F00 4008h
Ch	32	ECC_AGGR_STAT	3F00 400Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 4010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 403Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 4040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 4080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 40C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 413Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 4140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 4180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 41C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 4200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 4204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 4208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 420Ch

14.4.1.2 gicss Registers

gicss Registers

14.4.1.2.1 GIC500_TRANSLATER_TRANSLATER Register

1 GIC500_TRANSLATER_TRANSLATER Register (Offset = 30040h) [reset = 0h]

GITS_TRANSLATER

Return to Summary Table

Table 14-16870. Instance Table

Instance Name	Physical Address
GICSS0	**0103 0040h**

Figure 14-5594. GIC500_TRANSLATER_TRANSLATER Name Register

31	30	29	28	27	26	25	24
TRANSLATER__1_GITS_TRANSLATER__0_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRANSLATER__1_GITS_TRANSLATER__0_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRANSLATER__1_GITS_TRANSLATER__0_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRANSLATER__1_GITS_TRANSLATER__0_32							
R/W							
0h							

Table 14-16872. GIC500_TRANSLATER_TRANSLATER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANSLATER__1_GITS_TRANSLATER__0_32	R/W	0h	Input ID

14.4.1.2.2 GIC500_GICD_CTLR Register

1 GIC500_GICD_CTLR Register (Offset = 0h) [reset = 30h]

GICD_CTLR

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Table 14-16873. Instance Table

Instance Name	Physical Address
GICSS0	0180 0000h

Figure 14-5595. GIC500_GICD_CTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__1_GICD_CTLR__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DISTRIBUTOR__1_GICD_CTLR__6_1</td><td>DISTRIBUTOR__1_GICD_CTLR__5_1</td><td>DISTRIBUTOR__1_GICD_CTLR__4_1</td><td>RESERVED</td><td>DISTRIBUTOR__1_GICD_CTLR__2_1</td><td>DISTRIBUTOR__1_GICD_CTLR__1_1</td><td>DISTRIBUTOR__1_GICD_CTLR__0_1</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-16875. GIC500_GICD_CTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__1_GICD_CTLR__31_1	R/W	0h	Register Write Pending
30:7	RESERVED	NONE	0h	Reserved
6	DISTRIBUTOR__1_GICD_CTLR__6_1	R/W	0h	S: DS
5	DISTRIBUTOR__1_GICD_CTLR__5_1	R/W	1h	S: ARE_NS
4	DISTRIBUTOR__1_GICD_CTLR__4_1	R/W	1h	NS: ARE_NS S: ARE_S
3	RESERVED	NONE	0h	Reserved
2	DISTRIBUTOR__1_GICD_CTLR__2_1	R/W	0h	S: EnableGrp1_S
1	DISTRIBUTOR__1_GICD_CTLR__1_1	R/W	0h	NS: EnableGrp1A S: EnableGrp1_NS
0	DISTRIBUTOR__1_GICD_CTLR__0_1	R/W	0h	NS: EnableGrp1 S: EnableGrp0

14.4.1.2.3 GIC500_GICD_TYPER Register

1 GIC500_GICD_TYPER Register (Offset = 4h) [reset = 7B0428h]

GICD_TYPER

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Table 14-16876. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0004h**

Figure 14-5596. GIC500_GICD_TYPER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>DISTRIBUTOR__3_GICD_TYPER__24_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">DISTRIBUTOR__3_GICD_TYPER__19_5</td><td>DISTRIBUTOR__3_GICD_TYPER__18_1</td><td>DISTRIBUTOR__3_GICD_TYPER__17_1</td><td>DISTRIBUTOR__3_GICD_TYPER__16_1</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">Fh</td><td>0h</td><td>1h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">DISTRIBUTOR__3_GICD_TYPER__11_5</td><td>DISTRIBUTOR__3_GICD_TYPER__10_1</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">DISTRIBUTOR__3_GICD_TYPER__5_3</td><td colspan="5">DISTRIBUTOR__3_GICD_TYPER__0_5</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">1h</td><td colspan="5">8h</td></tr>
</table>

Table 14-16878. GIC500_GICD_TYPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DISTRIBUTOR__3_GICD_TYPER__24_1	R/W	0h	A3V
23:19	DISTRIBUTOR__3_GICD_TYPER__19_5	R/W	Fh	IDbits
18	DISTRIBUTOR__3_GICD_TYPER__18_1	R/W	0h	DVIS
17	DISTRIBUTOR__3_GICD_TYPER__17_1	R/W	1h	LPIS
16	DISTRIBUTOR__3_GICD_TYPER__16_1	R/W	1h	MBIS
15:11	DISTRIBUTOR__3_GICD_TYPER__11_5	R/W	0h	LSPI
10	DISTRIBUTOR__3_GICD_TYPER__10_1	R/W	1h	SecurityExtn
9:8	RESERVED	NONE	0h	Reserved

Table 14-16878. GIC500_GICD_TYPER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	DISTRIBUTOR__3_GICD_TYPER__5_3	R/W	1h	CPUNumber
4:0	DISTRIBUTOR__3_GICD_TYPER__0_5	R/W	8h	ITLinesNumber

14.4.1.2.4 GIC500_GICD_IIDR Register

1 GIC500_GICD_IIDR Register (Offset = 8h) [reset = 1143Bh]

GICD_IIDR

Return to Summary Table

Table 14-16879. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0008h**

Figure 14-5597. GIC500_GICD_IIDR Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__4_GICD_IIDR__24_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				DISTRIBUTOR__4_GICD_IIDR__16_4			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__4_GICD_IIDR__12_4				DISTRIBUTOR__4_GICD_IIDR__0_12			
R/W				R/W			
1h				43Bh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__4_GICD_IIDR__0_12							
R/W							
43Bh							

Table 14-16881. GIC500_GICD_IIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DISTRIBUTOR__4_GICD_IIDR__24_8	R/W	0h	ProductID
23:20	RESERVED	NONE	0h	Reserved
19:16	DISTRIBUTOR__4_GICD_IIDR__16_4	R/W	1h	Variant
15:12	DISTRIBUTOR__4_GICD_IIDR__12_4	R/W	1h	Revision
11:0	DISTRIBUTOR__4_GICD_IIDR__0_12	R/W	43Bh	Implementer

14.4.1.2.5 GIC500_GICD_SETSPI_NSR Register

1 GIC500_GICD_SETSPI_NSR Register (Offset = 40h) [reset = 0h]

GICD_SETSPI_NSR

Return to Summary Table

Table 14-16882. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0040h**

Figure 14-5598. GIC500_GICD_SETSPI_NSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DISTRIBUTOR__5_GICD_SETSPI_NSR__0_10</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__5_GICD_SETSPI_NSR__0_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16884. GIC500_GICD_SETSPI_NSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	DISTRIBUTOR__5_GICD_SETSPI_NSR__0_10	R/W	0h	SPI ID

14.4.1.2.6 GIC500_GICD_CLRSPI_NSR Register

1 GIC500_GICD_CLRSPI_NSR Register (Offset = 48h) [reset = 0h]

GICD_CLRSPI_NSR

Return to Summary Table

Table 14-16885. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0048h**

Figure 14-5599. GIC500_GICD_CLRSPI_NSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						DISTRIBUTOR__6_GICD_CLRSPI_NSR__0_10	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
DISTRIBUTOR__6_GICD_CLRSPI_NSR__0_10							
R/W							
0h							

Table 14-16887. GIC500_GICD_CLRSPI_NSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	DISTRIBUTOR__6_GICD_CLRSPI_NSR__0_10	R/W	0h	SPI ID

14.4.1.2.7 GIC500_GICD_SETSPI_SR Register

1 GIC500_GICD_SETSPI_SR Register (Offset = 50h) [reset = 0h]

GICD_SETSPI_SR

Return to Summary Table

Table 14-16888. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0050h**

Figure 14-5600. GIC500_GICD_SETSPI_SR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						DISTRIBUTOR__7_GICD_SETSPI_SR__0_10	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
DISTRIBUTOR__7_GICD_SETSPI_SR__0_10							
R/W							
0h							

Table 14-16890. GIC500_GICD_SETSPI_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	DISTRIBUTOR__7_GICD_SETSPI_SR__0_10	R/W	0h	SPI ID

14.4.1.2.8 GIC500_GICD_CLRSPI_SR Register

1 GIC500_GICD_CLRSPI_SR Register (Offset = 58h) [reset = 0h]

GICD_CLRSPI_SR

Return to Summary Table

Table 14-16891. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0058h**

Figure 14-5601. GIC500_GICD_CLRSPI_SR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						DISTRIBUTOR__8_GICD_CLRSPI_SR__0_10	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
DISTRIBUTOR__8_GICD_CLRSPI_SR__0_10							
R/W							
0h							

Table 14-16893. GIC500_GICD_CLRSPI_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	DISTRIBUTOR__8_GICD_CLRSPI_SR__0_10	R/W	0h	SPI ID

14.4.1.2.9 GIC500_GICD_IGROUPR_SGI_PPI Register

1 GIC500_GICD_IGROUPR_SGI_PPI Register (Offset = 80h) [reset = 0h]

GICD_IGROUPR0

Return to Summary Table

Table 14-16894. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0080h**

Figure 14-5602. GIC500_GICD_IGROUPR_SGI_PPI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16896. GIC500_GICD_IGROUPR_SGI_PPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.10 GIC500_GICD_IGROUPR_SPI1 Register

1 GIC500_GICD_IGROUPR_SPI1 Register (Offset = 84h) [reset = 0h]

GICD_IGROUPR1

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Table 14-16897. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0084h**

Figure 14-5603. GIC500_GICD_IGROUPR_SPI1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16899. GIC500_GICD_IGROUPR_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.11 GIC500_GICD_IGROUPR_SPI2 Register

1 GIC500_GICD_IGROUPR_SPI2 Register (Offset = 88h) [reset = 0h]

GICD_IGROUPR2

Return to Summary Table

Table 14-16900. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0088h**

Figure 14-5604. GIC500_GICD_IGROUPR_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16902. GIC500_GICD_IGROUPR_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.12 GIC500_GICD_IGROUPR_SPI3 Register

1 GIC500_GICD_IGROUPR_SPI3 Register (Offset = 8Ch) [reset = 0h]

GICD_IGROUPR3

Return to Summary Table

Table 14-16903. Instance Table

Instance Name	Physical Address
GICSS0	**0180 008Ch**

Figure 14-5605. GIC500_GICD_IGROUPR_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16905. GIC500_GICD_IGROUPR_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.13 GIC500_GICD_IGROUPR_SPI4 Register

1 GIC500_GICD_IGROUPR_SPI4 Register (Offset = 90h) [reset = 0h]

GICD_IGROUPR4

Return to Summary Table

Table 14-16906. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0090h**

Figure 14-5606. GIC500_GICD_IGROUPR_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16908. GIC500_GICD_IGROUPR_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.14 GIC500_GICD_IGROUPR_SPI5 Register

1 GIC500_GICD_IGROUPR_SPI5 Register (Offset = 94h) [reset = 0h]

GICD_IGROUPR5

Return to Summary Table

Table 14-16909. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0094h**

Figure 14-5607. GIC500_GICD_IGROUPR_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16911. GIC500_GICD_IGROUPR_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.15 GIC500_GICD_IGROUPR_SPI6 Register

1 GIC500_GICD_IGROUPR_SPI6 Register (Offset = 98h) [reset = 0h]

GICD_IGROUPR6

Return to Summary Table

Table 14-16912. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0098h**

Figure 14-5608. GIC500_GICD_IGROUPR_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16914. GIC500_GICD_IGROUPR_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.16 GIC500_GICD_IGROUPR_SPI7 Register

1 GIC500_GICD_IGROUPR_SPI7 Register (Offset = 9Ch) [reset = 0h]

GICD_IGROUPR7

Return to Summary Table

Table 14-16915. Instance Table

Instance Name	Physical Address
GICSS0	**0180 009Ch**

Figure 14-5609. GIC500_GICD_IGROUPR_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16917. GIC500_GICD_IGROUPR_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.17 GIC500_GICD_IGROUPR_SPI8 Register

1 GIC500_GICD_IGROUPR_SPI8 Register (Offset = A0h) [reset = 0h]

GICD_IGROUPR8

Return to Summary Table

Table 14-16918. Instance Table

Instance Name	Physical Address
GICSS0	**0180 00A0h**

Figure 14-5610. GIC500_GICD_IGROUPR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16920. GIC500_GICD_IGROUPR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.18 GIC500_GICD_ISENABLER_SPI1 Register

1 GIC500_GICD_ISENABLER_SPI1 Register (Offset = 104h) [reset = 0h]

GICD_ISENABLER1

Return to Summary Table

Table 14-16921. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0104h**

Figure 14-5611. GIC500_GICD_ISENABLER_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16923. GIC500_GICD_ISENABLER_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.19 GIC500_GICD_ISENABLER_SPI2 Register

1 GIC500_GICD_ISENABLER_SPI2 Register (Offset = 108h) [reset = 0h]

GICD_ISENABLER2

Return to Summary Table

Table 14-16924. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0108h**

Figure 14-5612. GIC500_GICD_ISENABLER_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16926. GIC500_GICD_ISENABLER_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.20 GIC500_GICD_ISENABLER_SPI3 Register

1 GIC500_GICD_ISENABLER_SPI3 Register (Offset = 10Ch) [reset = 0h]

GICD_ISENABLER3

Return to Summary Table

Table 14-16927. Instance Table

Instance Name	Physical Address
GICSS0	**0180 010Ch**

Figure 14-5613. GIC500_GICD_ISENABLER_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16929. GIC500_GICD_ISENABLER_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.21 GIC500_GICD_ISENABLER_SPI4 Register

1 GIC500_GICD_ISENABLER_SPI4 Register (Offset = 110h) [reset = 0h]

GICD_ISENABLER4

Return to Summary Table

Table 14-16930. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0110h**

Figure 14-5614. GIC500_GICD_ISENABLER_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16932. GIC500_GICD_ISENABLER_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.22 GIC500_GICD_ISENABLER_SPI5 Register

1 GIC500_GICD_ISENABLER_SPI5 Register (Offset = 114h) [reset = 0h]

GICD_ISENABLER5

Return to Summary Table

Table 14-16933. Instance Table

Instance Name	Physical Address
GICSS0	0180 0114h

Figure 14-5615. GIC500_GICD_ISENABLER_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16935. GIC500_GICD_ISENABLER_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.23 GIC500_GICD_ISENABLER_SPI6 Register

1 GIC500_GICD_ISENABLER_SPI6 Register (Offset = 118h) [reset = 0h]

GICD_ISENABLER6

Return to Summary Table

Table 14-16936. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0118h**

Figure 14-5616. GIC500_GICD_ISENABLER_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16938. GIC500_GICD_ISENABLER_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.24 GIC500_GICD_ISENABLER_SPI7 Register

1 GIC500_GICD_ISENABLER_SPI7 Register (Offset = 11Ch) [reset = 0h]

GICD_ISENABLER7

Return to Summary Table

Table 14-16939. Instance Table

Instance Name	Physical Address
GICSS0	**0180 011Ch**

Figure 14-5617. GIC500_GICD_ISENABLER_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16941. GIC500_GICD_ISENABLER_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.25 GIC500_GICD_ISENABLER_SPI8 Register

1 GIC500_GICD_ISENABLER_SPI8 Register (Offset = 120h) [reset = 0h]

GICD_ISENABLER8

Return to Summary Table

Table 14-16942. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0120h**

Figure 14-5618. GIC500_GICD_ISENABLER_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16944. GIC500_GICD_ISENABLER_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.26 GIC500_GICD_ICENABLER_SPI1 Register

1 GIC500_GICD_ICENABLER_SPI1 Register (Offset = 184h) [reset = 0h]

GICD_ICENABLER1

Return to Summary Table

Table 14-16945. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0184h**

Figure 14-5619. GIC500_GICD_ICENABLER_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16947. GIC500_GICD_ICENABLER_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.27 GIC500_GICD_ICENABLER_SPI2 Register

1 GIC500_GICD_ICENABLER_SPI2 Register (Offset = 188h) [reset = 0h]

GICD_ICENABLER2

Return to Summary Table

Table 14-16948. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0188h**

Figure 14-5620. GIC500_GICD_ICENABLER_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16950. GIC500_GICD_ICENABLER_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.28 GIC500_GICD_ICENABLER_SPI3 Register

1 GIC500_GICD_ICENABLER_SPI3 Register (Offset = 18Ch) [reset = 0h]

GICD_ICENABLER3

Return to Summary Table

Table 14-16951. Instance Table

Instance Name	Physical Address
GICSS0	**0180 018Ch**

Figure 14-5621. GIC500_GICD_ICENABLER_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16953. GIC500_GICD_ICENABLER_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.29 GIC500_GICD_ICENABLER_SPI4 Register

1 GIC500_GICD_ICENABLER_SPI4 Register (Offset = 190h) [reset = 0h]

GICD_ICENABLER4

Return to Summary Table

Table 14-16954. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0190h**

Figure 14-5622. GIC500_GICD_ICENABLER_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16956. GIC500_GICD_ICENABLER_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.30 GIC500_GICD_ICENABLER_SPI5 Register

1 GIC500_GICD_ICENABLER_SPI5 Register (Offset = 194h) [reset = 0h]

GICD_ICENABLER5

Return to Summary Table

Table 14-16957. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0194h**

Figure 14-5623. GIC500_GICD_ICENABLER_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16959. GIC500_GICD_ICENABLER_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.31 GIC500_GICD_ICENABLER_SPI6 Register

1 GIC500_GICD_ICENABLER_SPI6 Register (Offset = 198h) [reset = 0h]

GICD_ICENABLER6

Return to Summary Table

Table 14-16960. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0198h**

Figure 14-5624. GIC500_GICD_ICENABLER_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16962. GIC500_GICD_ICENABLER_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.32 GIC500_GICD_ICENABLER_SPI7 Register

1 GIC500_GICD_ICENABLER_SPI7 Register (Offset = 19Ch) [reset = 0h]

GICD_ICENABLER7

Return to Summary Table

Table 14-16963. Instance Table

Instance Name	Physical Address
GICSS0	**0180 019Ch**

Figure 14-5625. GIC500_GICD_ICENABLER_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16965. GIC500_GICD_ICENABLER_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.33 GIC500_GICD_ICENABLER_SPI8 Register

1 GIC500_GICD_ICENABLER_SPI8 Register (Offset = 1A0h) [reset = 0h]

GICD_ICENABLER8

Return to Summary Table

Table 14-16966. Instance Table

Instance Name	Physical Address
GICSS0	**0180 01A0h**

Figure 14-5626. GIC500_GICD_ICENABLER_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16968. GIC500_GICD_ICENABLER_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.34 GIC500_GICD_ISPENDR_SPI1 Register

1 GIC500_GICD_ISPENDR_SPI1 Register (Offset = 204h) [reset = 0h]

GICD_ISPENDR1

Return to Summary Table

Table 14-16969. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0204h**

Figure 14-5627. GIC500_GICD_ISPENDR_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16971. GIC500_GICD_ISPENDR_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.35 GIC500_GICD_ISPENDR_SPI2 Register

1 GIC500_GICD_ISPENDR_SPI2 Register (Offset = 208h) [reset = 0h]

GICD_ISPENDR2

Return to Summary Table

Table 14-16972. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0208h**

Figure 14-5628. GIC500_GICD_ISPENDR_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16974. GIC500_GICD_ISPENDR_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.36 GIC500_GICD_ISPENDR_SPI3 Register

1 GIC500_GICD_ISPENDR_SPI3 Register (Offset = 20Ch) [reset = 0h]

GICD_ISPENDR3

Return to Summary Table

Table 14-16975. Instance Table

Instance Name	Physical Address
GICSS0	**0180 020Ch**

Figure 14-5629. GIC500_GICD_ISPENDR_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16977. GIC500_GICD_ISPENDR_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.37 GIC500_GICD_ISPENDR_SPI4 Register

1 GIC500_GICD_ISPENDR_SPI4 Register (Offset = 210h) [reset = 0h]

GICD_ISPENDR4

Return to Summary Table

Table 14-16978. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0210h**

Figure 14-5630. GIC500_GICD_ISPENDR_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16980. GIC500_GICD_ISPENDR_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.38 GIC500_GICD_ISPENDR_SPI5 Register

1 GIC500_GICD_ISPENDR_SPI5 Register (Offset = 214h) [reset = 0h]

GICD_ISPENDR5

Return to Summary Table

Table 14-16981. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0214h**

Figure 14-5631. GIC500_GICD_ISPENDR_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16983. GIC500_GICD_ISPENDR_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.39 GIC500_GICD_ISPENDR_SPI6 Register

1 GIC500_GICD_ISPENDR_SPI6 Register (Offset = 218h) [reset = 0h]

GICD_ISPENDR6

Return to Summary Table

Table 14-16984. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0218h**

Figure 14-5632. GIC500_GICD_ISPENDR_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16986. GIC500_GICD_ISPENDR_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.40 GIC500_GICD_ISPENDR_SPI7 Register

1 GIC500_GICD_ISPENDR_SPI7 Register (Offset = 21Ch) [reset = 0h]

GICD_ISPENDR7

Return to Summary Table

Table 14-16987. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 021Ch**

Figure 14-5633. GIC500_GICD_ISPENDR_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16989. GIC500_GICD_ISPENDR_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.41 GIC500_GICD_ISPENDR_SPI8 Register

1 GIC500_GICD_ISPENDR_SPI8 Register (Offset = 220h) [reset = 0h]

GICD_ISPENDR8

Return to Summary Table

Table 14-16990. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0220h**

Figure 14-5634. GIC500_GICD_ISPENDR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16992. GIC500_GICD_ISPENDR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.42 GIC500_GICD_ICPENDR_SPI1 Register

1 GIC500_GICD_ICPENDR_SPI1 Register (Offset = 284h) [reset = 0h]

GICD_ICPENDR1

Return to Summary Table

Table 14-16993. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0284h**

Figure 14-5635. GIC500_GICD_ICPENDR_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16995. GIC500_GICD_ICPENDR_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.43 GIC500_GICD_ICPENDR_SPI2 Register

1 GIC500_GICD_ICPENDR_SPI2 Register (Offset = 288h) [reset = 0h]

GICD_ICPENDR2

Return to Summary Table

Table 14-16996. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0288h**

Figure 14-5636. GIC500_GICD_ICPENDR_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16998. GIC500_GICD_ICPENDR_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.44 GIC500_GICD_ICPENDR_SPI3 Register

1 GIC500_GICD_ICPENDR_SPI3 Register (Offset = 28Ch) [reset = 0h]

GICD_ICPENDR3

Return to Summary Table

Table 14-16999. Instance Table

Instance Name	Physical Address
GICSS0	**0180 028Ch**

Figure 14-5637. GIC500_GICD_ICPENDR_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17001. GIC500_GICD_ICPENDR_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.45 GIC500_GICD_ICPENDR_SPI4 Register

1 GIC500_GICD_ICPENDR_SPI4 Register (Offset = 290h) [reset = 0h]

GICD_ICPENDR4

Return to Summary Table

Table 14-17002. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0290h**

Figure 14-5638. GIC500_GICD_ICPENDR_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17004. GIC500_GICD_ICPENDR_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.46 GIC500_GICD_ICPENDR_SPI5 Register

1 GIC500_GICD_ICPENDR_SPI5 Register (Offset = 294h) [reset = 0h]

GICD_ICPENDR5

Return to Summary Table

Table 14-17005. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0294h**

Figure 14-5639. GIC500_GICD_ICPENDR_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17007. GIC500_GICD_ICPENDR_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.47 GIC500_GICD_ICPENDR_SPI6 Register

1 GIC500_GICD_ICPENDR_SPI6 Register (Offset = 298h) [reset = 0h]

GICD_ICPENDR6

Return to Summary Table

Table 14-17008. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0298h**

Figure 14-5640. GIC500_GICD_ICPENDR_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17010. GIC500_GICD_ICPENDR_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.48 GIC500_GICD_ICPENDR_SPI7 Register

1 GIC500_GICD_ICPENDR_SPI7 Register (Offset = 29Ch) [reset = 0h]

GICD_ICPENDR7

Return to Summary Table

Table 14-17011. Instance Table

Instance Name	Physical Address
GICSS0	**0180 029Ch**

Figure 14-5641. GIC500_GICD_ICPENDR_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17013. GIC500_GICD_ICPENDR_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.49 GIC500_GICD_ICPENDR_SPI8 Register

1 GIC500_GICD_ICPENDR_SPI8 Register (Offset = 2A0h) [reset = 0h]

GICD_ICPENDR8

Return to Summary Table

Table 14-17014. Instance Table

Instance Name	Physical Address
GICSS0	**0180 02A0h**

Figure 14-5642. GIC500_GICD_ICPENDR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17016. GIC500_GICD_ICPENDR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.50 GIC500_GICD_ISACTIVER_SPI1 Register

1 GIC500_GICD_ISACTIVER_SPI1 Register (Offset = 304h) [reset = 0h]

GICD_ISACTIVER1

Return to Summary Table

Table 14-17017. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0304h**

Figure 14-5643. GIC500_GICD_ISACTIVER_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17019. GIC500_GICD_ISACTIVER_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.51 GIC500_GICD_ISACTIVER_SPI2 Register

1 GIC500_GICD_ISACTIVER_SPI2 Register (Offset = 308h) [reset = 0h]

GICD_ISACTIVER2

Return to Summary Table

Table 14-17020. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0308h**

Figure 14-5644. GIC500_GICD_ISACTIVER_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17022. GIC500_GICD_ISACTIVER_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.52 GIC500_GICD_ISACTIVER_SPI3 Register

1 GIC500_GICD_ISACTIVER_SPI3 Register (Offset = 30Ch) [reset = 0h]

GICD_ISACTIVER3

Return to Summary Table

Table 14-17023. Instance Table

Instance Name	Physical Address
GICSS0	**0180 030Ch**

Figure 14-5645. GIC500_GICD_ISACTIVER_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17025. GIC500_GICD_ISACTIVER_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.53 GIC500_GICD_ISACTIVER_SPI4 Register

1 GIC500_GICD_ISACTIVER_SPI4 Register (Offset = 310h) [reset = 0h]

GICD_ISACTIVER4

Return to Summary Table

Table 14-17026. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0310h**

Figure 14-5646. GIC500_GICD_ISACTIVER_SPI4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17028. GIC500_GICD_ISACTIVER_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.54 GIC500_GICD_ISACTIVER_SPI5 Register

1 GIC500_GICD_ISACTIVER_SPI5 Register (Offset = 314h) [reset = 0h]

GICD_ISACTIVER5

Return to Summary Table

Table 14-17029. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 0314h**

Figure 14-5647. GIC500_GICD_ISACTIVER_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17031. GIC500_GICD_ISACTIVER_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.55 GIC500_GICD_ISACTIVER_SPI6 Register

1 GIC500_GICD_ISACTIVER_SPI6 Register (Offset = 318h) [reset = 0h]

GICD_ISACTIVER6

Return to Summary Table

Table 14-17032. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0318h**

Figure 14-5648. GIC500_GICD_ISACTIVER_SPI6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17034. GIC500_GICD_ISACTIVER_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.56 GIC500_GICD_ISACTIVER_SPI7 Register

1 GIC500_GICD_ISACTIVER_SPI7 Register (Offset = 31Ch) [reset = 0h]

GICD_ISACTIVER7

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Table 14-17035. Instance Table

Instance Name	Physical Address
GICSS0	**0180 031Ch**

Figure 14-5649. GIC500_GICD_ISACTIVER_SPI7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17037. GIC500_GICD_ISACTIVER_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.57 GIC500_GICD_ISACTIVER_SPI8 Register

1 GIC500_GICD_ISACTIVER_SPI8 Register (Offset = 320h) [reset = 0h]

GICD_ISACTIVER8

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Table 14-17038. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0320h**

Figure 14-5650. GIC500_GICD_ISACTIVER_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-17040. GIC500_GICD_ISACTIVER_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.58 GIC500_GICD_ICACTIVER_SPI1 Register

1 GIC500_GICD_ICACTIVER_SPI1 Register (Offset = 384h) [reset = 0h]

GICD_ICACTIVER1

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Table 14-17041. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0384h**

Figure 14-5651. GIC500_GICD_ICACTIVER_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17043. GIC500_GICD_ICACTIVER_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.59 GIC500_GICD_ICACTIVER_SPI2 Register

1 GIC500_GICD_ICACTIVER_SPI2 Register (Offset = 388h) [reset = 0h]

GICD_ICACTIVER2

Return to Summary Table

Table 14-17044. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0388h**

Figure 14-5652. GIC500_GICD_ICACTIVER_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17046. GIC500_GICD_ICACTIVER_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.60 GIC500_GICD_ICACTIVER_SPI3 Register

1 GIC500_GICD_ICACTIVER_SPI3 Register (Offset = 38Ch) [reset = 0h]

GICD_ICACTIVER3

Return to Summary Table

Table 14-17047. Instance Table

Instance Name	Physical Address
GICSS0	**0180 038Ch**

Figure 14-5653. GIC500_GICD_ICACTIVER_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17049. GIC500_GICD_ICACTIVER_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.61 GIC500_GICD_ICACTIVER_SPI4 Register

1 GIC500_GICD_ICACTIVER_SPI4 Register (Offset = 390h) [reset = 0h]

GICD_ICACTIVER4

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Table 14-17050. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0390h**

Figure 14-5654. GIC500_GICD_ICACTIVER_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17052. GIC500_GICD_ICACTIVER_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.62 GIC500_GICD_ICACTIVER_SPI5 Register

1 GIC500_GICD_ICACTIVER_SPI5 Register (Offset = 394h) [reset = 0h]

GICD_ICACTIVER5

Return to Summary Table

Table 14-17053. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0394h**

Figure 14-5655. GIC500_GICD_ICACTIVER_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17055. GIC500_GICD_ICACTIVER_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.63 GIC500_GICD_ICACTIVER_SPI6 Register

1 GIC500_GICD_ICACTIVER_SPI6 Register (Offset = 398h) [reset = 0h]

GICD_ICACTIVER6

Return to Summary Table

Table 14-17056. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0398h**

Figure 14-5656. GIC500_GICD_ICACTIVER_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17058. GIC500_GICD_ICACTIVER_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.64 GIC500_GICD_ICACTIVER_SPI7 Register

1 GIC500_GICD_ICACTIVER_SPI7 Register (Offset = 39Ch) [reset = 0h]

GICD_ICACTIVER7

Return to Summary Table

Table 14-17059. Instance Table

Instance Name	Physical Address
GICSS0	**0180 039Ch**

Figure 14-5657. GIC500_GICD_ICACTIVER_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17061. GIC500_GICD_ICACTIVER_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.65 GIC500_GICD_ICACTIVER_SPI8 Register

1 GIC500_GICD_ICACTIVER_SPI8 Register (Offset = 3A0h) [reset = 0h]

GICD_ICACTIVER8

Return to Summary Table

Table 14-17062. Instance Table

Instance Name	Physical Address
GICSS0	**0180 03A0h**

Figure 14-5658. GIC500_GICD_ICACTIVER_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17064. GIC500_GICD_ICACTIVER_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.66 GIC500_GICD_IPRIORITYR_SPI8 Register

1 GIC500_GICD_IPRIORITYR_SPI8 Register (Offset = 420h) [reset = 0h]

GICD_IPRIORITYR8

Return to Summary Table

Table 14-17065. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0420h**

Figure 14-5659. GIC500_GICD_IPRIORITYR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17067. GIC500_GICD_IPRIORITYR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.67 GIC500_GICD_IPRIORITYR_SPI9 Register

1 GIC500_GICD_IPRIORITYR_SPI9 Register (Offset = 424h) [reset = 0h]

GICD_IPRIORITYR9

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Table 14-17068. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0424h**

Figure 14-5660. GIC500_GICD_IPRIORITYR_SPI9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17070. GIC500_GICD_IPRIORITYR_SPI9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.68 GIC500_GICD_IPRIORITYR_SPI10 Register

1 GIC500_GICD_IPRIORITYR_SPI10 Register (Offset = 428h) [reset = 0h]

GICD_IPRIORITYR10

Return to Summary Table

Table 14-17071. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0428h**

Figure 14-5661. GIC500_GICD_IPRIORITYR_SPI10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17073. GIC500_GICD_IPRIORITYR_SPI10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.69 GIC500_GICD_IPRIORITYR_SPI11 Register

1 GIC500_GICD_IPRIORITYR_SPI11 Register (Offset = 42Ch) [reset = 0h]

GICD_IPRIORITYR11

Return to Summary Table

Table 14-17074. Instance Table

Instance Name	Physical Address
GICSS0	**0180 042Ch**

Figure 14-5662. GIC500_GICD_IPRIORITYR_SPI11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17076. GIC500_GICD_IPRIORITYR_SPI11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.70 GIC500_GICD_IPRIORITYR_SPI12 Register

1 GIC500_GICD_IPRIORITYR_SPI12 Register (Offset = 430h) [reset = 0h]

GICD_IPRIORITYR12

Return to Summary Table

Table 14-17077. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0430h**

Figure 14-5663. GIC500_GICD_IPRIORITYR_SPI12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17079. GIC500_GICD_IPRIORITYR_SPI12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.71 GIC500_GICD_IPRIORITYR_SPI13 Register

1 GIC500_GICD_IPRIORITYR_SPI13 Register (Offset = 434h) [reset = 0h]

GICD_IPRIORITYR13

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Table 14-17080. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0434h**

Figure 14-5664. GIC500_GICD_IPRIORITYR_SPI13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17082. GIC500_GICD_IPRIORITYR_SPI13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.72 GIC500_GICD_IPRIORITYR_SPI14 Register

1 GIC500_GICD_IPRIORITYR_SPI14 Register (Offset = 438h) [reset = 0h]

GICD_IPRIORITYR14

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Table 14-17083. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0438h**

Figure 14-5665. GIC500_GICD_IPRIORITYR_SPI14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17085. GIC500_GICD_IPRIORITYR_SPI14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.73 GIC500_GICD_IPRIORITYR_SPI15 Register

1 GIC500_GICD_IPRIORITYR_SPI15 Register (Offset = 43Ch) [reset = 0h]

GICD_IPRIORITYR15

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Table 14-17086. Instance Table

Instance Name	Physical Address
GICSS0	**0180 043Ch**

Figure 14-5666. GIC500_GICD_IPRIORITYR_SPI15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17088. GIC500_GICD_IPRIORITYR_SPI15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.74 GIC500_GICD_IPRIORITYR_SPI16 Register

1 GIC500_GICD_IPRIORITYR_SPI16 Register (Offset = 440h) [reset = 0h]

GICD_IPRIORITYR16

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Table 14-17089. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0440h**

Figure 14-5667. GIC500_GICD_IPRIORITYR_SPI16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17091. GIC500_GICD_IPRIORITYR_SPI16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.75 GIC500_GICD_IPRIORITYR_SPI17 Register

1 GIC500_GICD_IPRIORITYR_SPI17 Register (Offset = 444h) [reset = 0h]

GICD_IPRIORITYR17

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Table 14-17092. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0444h**

Figure 14-5668. GIC500_GICD_IPRIORITYR_SPI17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17094. GIC500_GICD_IPRIORITYR_SPI17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.76 GIC500_GICD_IPRIORITYR_SPI18 Register

1 GIC500_GICD_IPRIORITYR_SPI18 Register (Offset = 448h) [reset = 0h]

GICD_IPRIORITYR18

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Table 14-17095. Instance Table

Instance Name	Physical Address
GICSS0	0180 0448h

Figure 14-5669. GIC500_GICD_IPRIORITYR_SPI18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17097. GIC500_GICD_IPRIORITYR_SPI18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.77 GIC500_GICD_IPRIORITYR_SPI19 Register

1 GIC500_GICD_IPRIORITYR_SPI19 Register (Offset = 44Ch) [reset = 0h]

GICD_IPRIORITYR19

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Table 14-17098. Instance Table

Instance Name	Physical Address
GICSS0	**0180 044Ch**

Figure 14-5670. GIC500_GICD_IPRIORITYR_SPI19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17100. GIC500_GICD_IPRIORITYR_SPI19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.78 GIC500_GICD_IPRIORITYR_SPI20 Register

1 GIC500_GICD_IPRIORITYR_SPI20 Register (Offset = 450h) [reset = 0h]

GICD_IPRIORITYR20

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Table 14-17101. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0450h**

Figure 14-5671. GIC500_GICD_IPRIORITYR_SPI20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17103. GIC500_GICD_IPRIORITYR_SPI20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.79 GIC500_GICD_IPRIORITYR_SPI21 Register

1 GIC500_GICD_IPRIORITYR_SPI21 Register (Offset = 454h) [reset = 0h]

GICD_IPRIORITYR21

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Table 14-17104. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0454h**

Figure 14-5672. GIC500_GICD_IPRIORITYR_SPI21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17106. GIC500_GICD_IPRIORITYR_SPI21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.80 GIC500_GICD_IPRIORITYR_SPI22 Register

1 GIC500_GICD_IPRIORITYR_SPI22 Register (Offset = 458h) [reset = 0h]

GICD_IPRIORITYR22

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Table 14-17107. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0458h**

Figure 14-5673. GIC500_GICD_IPRIORITYR_SPI22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17109. GIC500_GICD_IPRIORITYR_SPI22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.81 GIC500_GICD_IPRIORITYR_SPI23 Register

1 GIC500_GICD_IPRIORITYR_SPI23 Register (Offset = 45Ch) [reset = 0h]

GICD_IPRIORITYR23

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Table 14-17110. Instance Table

Instance Name	Physical Address
GICSS0	**0180 045Ch**

Figure 14-5674. GIC500_GICD_IPRIORITYR_SPI23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17112. GIC500_GICD_IPRIORITYR_SPI23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.82 GIC500_GICD_IPRIORITYR_SPI24 Register

1 GIC500_GICD_IPRIORITYR_SPI24 Register (Offset = 460h) [reset = 0h]

GICD_IPRIORITYR24

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Table 14-17113. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0460h**

Figure 14-5675. GIC500_GICD_IPRIORITYR_SPI24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17115. GIC500_GICD_IPRIORITYR_SPI24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.83 GIC500_GICD_IPRIORITYR_SPI25 Register

1 GIC500_GICD_IPRIORITYR_SPI25 Register (Offset = 464h) [reset = 0h]

GICD_IPRIORITYR25

Return to Summary Table

Table 14-17116. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0464h**

Figure 14-5676. GIC500_GICD_IPRIORITYR_SPI25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17118. GIC500_GICD_IPRIORITYR_SPI25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.84 GIC500_GICD_IPRIORITYR_SPI26 Register

1 GIC500_GICD_IPRIORITYR_SPI26 Register (Offset = 468h) [reset = 0h]

GICD_IPRIORITYR26

Return to Summary Table

Table 14-17119. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0468h**

Figure 14-5677. GIC500_GICD_IPRIORITYR_SPI26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17121. GIC500_GICD_IPRIORITYR_SPI26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.85 GIC500_GICD_IPRIORITYR_SPI27 Register

1 GIC500_GICD_IPRIORITYR_SPI27 Register (Offset = 46Ch) [reset = 0h]

GICD_IPRIORITYR27

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Table 14-17122. Instance Table

Instance Name	Physical Address
GICSS0	**0180 046Ch**

Figure 14-5678. GIC500_GICD_IPRIORITYR_SPI27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17124. GIC500_GICD_IPRIORITYR_SPI27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.86 GIC500_GICD_IPRIORITYR_SPI28 Register

1 GIC500_GICD_IPRIORITYR_SPI28 Register (Offset = 470h) [reset = 0h]

GICD_IPRIORITYR28

Return to Summary Table

Table 14-17125. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0470h**

Figure 14-5679. GIC500_GICD_IPRIORITYR_SPI28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17127. GIC500_GICD_IPRIORITYR_SPI28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.87 GIC500_GICD_IPRIORITYR_SPI29 Register

1 GIC500_GICD_IPRIORITYR_SPI29 Register (Offset = 474h) [reset = 0h]

GICD_IPRIORITYR29

Return to Summary Table

Table 14-17128. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0474h**

Figure 14-5680. GIC500_GICD_IPRIORITYR_SPI29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17130. GIC500_GICD_IPRIORITYR_SPI29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.88 GIC500_GICD_IPRIORITYR_SPI30 Register

1 GIC500_GICD_IPRIORITYR_SPI30 Register (Offset = 478h) [reset = 0h]

GICD_IPRIORITYR30

Return to Summary Table

Table 14-17131. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0478h**

Figure 14-5681. GIC500_GICD_IPRIORITYR_SPI30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17133. GIC500_GICD_IPRIORITYR_SPI30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.89 GIC500_GICD_IPRIORITYR_SPI31 Register

1 GIC500_GICD_IPRIORITYR_SPI31 Register (Offset = 47Ch) [reset = 0h]

GICD_IPRIORITYR31

Return to Summary Table

Table 14-17134. Instance Table

Instance Name	Physical Address
GICSS0	**0180 047Ch**

Figure 14-5682. GIC500_GICD_IPRIORITYR_SPI31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17136. GIC500_GICD_IPRIORITYR_SPI31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.90 GIC500_GICD_IPRIORITYR_SPI32 Register

1 GIC500_GICD_IPRIORITYR_SPI32 Register (Offset = 480h) [reset = 0h]

GICD_IPRIORITYR32

Return to Summary Table

Table 14-17137. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0480h**

Figure 14-5683. GIC500_GICD_IPRIORITYR_SPI32 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17139. GIC500_GICD_IPRIORITYR_SPI32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.91 GIC500_GICD_IPRIORITYR_SPI33 Register

1 GIC500_GICD_IPRIORITYR_SPI33 Register (Offset = 484h) [reset = 0h]

GICD_IPRIORITYR33

Return to Summary Table

Table 14-17140. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0484h**

Figure 14-5684. GIC500_GICD_IPRIORITYR_SPI33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17142. GIC500_GICD_IPRIORITYR_SPI33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.92 GIC500_GICD_IPRIORITYR_SPI34 Register

1 GIC500_GICD_IPRIORITYR_SPI34 Register (Offset = 488h) [reset = 0h]

GICD_IPRIORITYR34

Return to Summary Table

Table 14-17143. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0488h**

Figure 14-5685. GIC500_GICD_IPRIORITYR_SPI34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17145. GIC500_GICD_IPRIORITYR_SPI34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.93 GIC500_GICD_IPRIORITYR_SPI35 Register

1 GIC500_GICD_IPRIORITYR_SPI35 Register (Offset = 48Ch) [reset = 0h]

GICD_IPRIORITYR35

Return to Summary Table

Table 14-17146. Instance Table

Instance Name	Physical Address
GICSS0	0180 048Ch

Figure 14-5686. GIC500_GICD_IPRIORITYR_SPI35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17148. GIC500_GICD_IPRIORITYR_SPI35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.94 GIC500_GICD_IPRIORITYR_SPI36 Register

1 GIC500_GICD_IPRIORITYR_SPI36 Register (Offset = 490h) [reset = 0h]

GICD_IPRIORITYR36

Return to Summary Table

Table 14-17149. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0490h**

Figure 14-5687. GIC500_GICD_IPRIORITYR_SPI36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17151. GIC500_GICD_IPRIORITYR_SPI36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.95 GIC500_GICD_IPRIORITYR_SPI37 Register

1 GIC500_GICD_IPRIORITYR_SPI37 Register (Offset = 494h) [reset = 0h]

GICD_IPRIORITYR37

Return to Summary Table

Table 14-17152. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0494h**

Figure 14-5688. GIC500_GICD_IPRIORITYR_SPI37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17154. GIC500_GICD_IPRIORITYR_SPI37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.96 GIC500_GICD_IPRIORITYR_SPI38 Register

1 GIC500_GICD_IPRIORITYR_SPI38 Register (Offset = 498h) [reset = 0h]

GICD_IPRIORITYR38

Return to Summary Table

Table 14-17155. Instance Table

Instance Name	Physical Address
GICSS0	0180 0498h

Figure 14-5689. GIC500_GICD_IPRIORITYR_SPI38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17157. GIC500_GICD_IPRIORITYR_SPI38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.97 GIC500_GICD_IPRIORITYR_SPI39 Register

1 GIC500_GICD_IPRIORITYR_SPI39 Register (Offset = 49Ch) [reset = 0h]

GICD_IPRIORITYR39

Return to Summary Table

Table 14-17158. Instance Table

Instance Name	Physical Address
GICSS0	**0180 049Ch**

Figure 14-5690. GIC500_GICD_IPRIORITYR_SPI39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17160. GIC500_GICD_IPRIORITYR_SPI39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.98 GIC500_GICD_IPRIORITYR_SPI40 Register

1 GIC500_GICD_IPRIORITYR_SPI40 Register (Offset = 4A0h) [reset = 0h]

GICD_IPRIORITYR40

Return to Summary Table

Table 14-17161. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04A0h**

Figure 14-5691. GIC500_GICD_IPRIORITYR_SPI40 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17163. GIC500_GICD_IPRIORITYR_SPI40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.99 GIC500_GICD_IPRIORITYR_SPI41 Register

1 GIC500_GICD_IPRIORITYR_SPI41 Register (Offset = 4A4h) [reset = 0h]

GICD_IPRIORITYR41

Return to Summary Table

Table 14-17164. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04A4h**

Figure 14-5692. GIC500_GICD_IPRIORITYR_SPI41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17166. GIC500_GICD_IPRIORITYR_SPI41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.100 GIC500_GICD_IPRIORITYR_SPI42 Register

1 GIC500_GICD_IPRIORITYR_SPI42 Register (Offset = 4A8h) [reset = 0h]

GICD_IPRIORITYR42

Return to Summary Table

Table 14-17167. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04A8h**

Figure 14-5693. GIC500_GICD_IPRIORITYR_SPI42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17169. GIC500_GICD_IPRIORITYR_SPI42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.101 GIC500_GICD_IPRIORITYR_SPI43 Register

1 GIC500_GICD_IPRIORITYR_SPI43 Register (Offset = 4ACh) [reset = 0h]

GICD_IPRIORITYR43

Return to Summary Table

Table 14-17170. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04ACh**

Figure 14-5694. GIC500_GICD_IPRIORITYR_SPI43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17172. GIC500_GICD_IPRIORITYR_SPI43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.102 GIC500_GICD_IPRIORITYR_SPI44 Register

1 GIC500_GICD_IPRIORITYR_SPI44 Register (Offset = 4B0h) [reset = 0h]

GICD_IPRIORITYR44

Return to Summary Table

Table 14-17173. Instance Table

Instance Name	Physical Address
GICSS0	0180 04B0h

Figure 14-5695. GIC500_GICD_IPRIORITYR_SPI44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17175. GIC500_GICD_IPRIORITYR_SPI44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.103 GIC500_GICD_IPRIORITYR_SPI45 Register

1 GIC500_GICD_IPRIORITYR_SPI45 Register (Offset = 4B4h) [reset = 0h]

GICD_IPRIORITYR45

Return to Summary Table

Table 14-17176. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04B4h**

Figure 14-5696. GIC500_GICD_IPRIORITYR_SPI45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17178. GIC500_GICD_IPRIORITYR_SPI45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.104 GIC500_GICD_IPRIORITYR_SPI46 Register

1 GIC500_GICD_IPRIORITYR_SPI46 Register (Offset = 4B8h) [reset = 0h]

GICD_IPRIORITYR46

Return to Summary Table

Table 14-17179. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04B8h**

Figure 14-5697. GIC500_GICD_IPRIORITYR_SPI46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17181. GIC500_GICD_IPRIORITYR_SPI46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.105 GIC500_GICD_IPRIORITYR_SPI47 Register

1 GIC500_GICD_IPRIORITYR_SPI47 Register (Offset = 4BCh) [reset = 0h]

GICD_IPRIORITYR47

Return to Summary Table

Table 14-17182. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04BCh**

Figure 14-5698. GIC500_GICD_IPRIORITYR_SPI47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17184. GIC500_GICD_IPRIORITYR_SPI47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.106 GIC500_GICD_IPRIORITYR_SPI48 Register

1 GIC500_GICD_IPRIORITYR_SPI48 Register (Offset = 4C0h) [reset = 0h]

GICD_IPRIORITYR48

Return to Summary Table

Table 14-17185. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 04C0h**

Figure 14-5699. GIC500_GICD_IPRIORITYR_SPI48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17187. GIC500_GICD_IPRIORITYR_SPI48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.107 GIC500_GICD_IPRIORITYR_SPI49 Register

1 GIC500_GICD_IPRIORITYR_SPI49 Register (Offset = 4C4h) [reset = 0h]

GICD_IPRIORITYR49

Return to Summary Table

Table 14-17188. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04C4h**

Figure 14-5700. GIC500_GICD_IPRIORITYR_SPI49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17190. GIC500_GICD_IPRIORITYR_SPI49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.108 GIC500_GICD_IPRIORITYR_SPI50 Register

1 GIC500_GICD_IPRIORITYR_SPI50 Register (Offset = 4C8h) [reset = 0h]

GICD_IPRIORITYR50

Return to Summary Table

Table 14-17191. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04C8h**

Figure 14-5701. GIC500_GICD_IPRIORITYR_SPI50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17193. GIC500_GICD_IPRIORITYR_SPI50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.109 GIC500_GICD_IPRIORITYR_SPI51 Register

1 GIC500_GICD_IPRIORITYR_SPI51 Register (Offset = 4CCh) [reset = 0h]

GICD_IPRIORITYR51

Return to Summary Table

Table 14-17194. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04CCh**

Figure 14-5702. GIC500_GICD_IPRIORITYR_SPI51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17196. GIC500_GICD_IPRIORITYR_SPI51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.110 GIC500_GICD_IPRIORITYR_SPI52 Register

1 GIC500_GICD_IPRIORITYR_SPI52 Register (Offset = 4D0h) [reset = 0h]

GICD_IPRIORITYR52

Return to Summary Table

Table 14-17197. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04D0h**

Figure 14-5703. GIC500_GICD_IPRIORITYR_SPI52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17199. GIC500_GICD_IPRIORITYR_SPI52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.111 GIC500_GICD_IPRIORITYR_SPI53 Register

1 GIC500_GICD_IPRIORITYR_SPI53 Register (Offset = 4D4h) [reset = 0h]

GICD_IPRIORITYR53

Return to Summary Table

Table 14-17200. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04D4h**

Figure 14-5704. GIC500_GICD_IPRIORITYR_SPI53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17202. GIC500_GICD_IPRIORITYR_SPI53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.112 GIC500_GICD_IPRIORITYR_SPI54 Register

1 GIC500_GICD_IPRIORITYR_SPI54 Register (Offset = 4D8h) [reset = 0h]

GICD_IPRIORITYR54

Return to Summary Table

Table 14-17203. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04D8h**

Figure 14-5705. GIC500_GICD_IPRIORITYR_SPI54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17205. GIC500_GICD_IPRIORITYR_SPI54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.113 GIC500_GICD_IPRIORITYR_SPI55 Register

1 GIC500_GICD_IPRIORITYR_SPI55 Register (Offset = 4DCh) [reset = 0h]

GICD_IPRIORITYR55

Return to Summary Table

Table 14-17206. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04DCh**

Figure 14-5706. GIC500_GICD_IPRIORITYR_SPI55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17208. GIC500_GICD_IPRIORITYR_SPI55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.114 GIC500_GICD_IPRIORITYR_SPI56 Register

1 GIC500_GICD_IPRIORITYR_SPI56 Register (Offset = 4E0h) [reset = 0h]

GICD_IPRIORITYR56

Return to Summary Table

Table 14-17209. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04E0h**

Figure 14-5707. GIC500_GICD_IPRIORITYR_SPI56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17211. GIC500_GICD_IPRIORITYR_SPI56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.115 GIC500_GICD_IPRIORITYR_SPI57 Register

1 GIC500_GICD_IPRIORITYR_SPI57 Register (Offset = 4E4h) [reset = 0h]

GICD_IPRIORITYR57

Return to Summary Table

Table 14-17212. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04E4h**

Figure 14-5708. GIC500_GICD_IPRIORITYR_SPI57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17214. GIC500_GICD_IPRIORITYR_SPI57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.116 GIC500_GICD_IPRIORITYR_SPI58 Register

1 GIC500_GICD_IPRIORITYR_SPI58 Register (Offset = 4E8h) [reset = 0h]

GICD_IPRIORITYR58

Return to Summary Table

Table 14-17215. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04E8h**

Figure 14-5709. GIC500_GICD_IPRIORITYR_SPI58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17217. GIC500_GICD_IPRIORITYR_SPI58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.117 GIC500_GICD_IPRIORITYR_SPI59 Register

1 GIC500_GICD_IPRIORITYR_SPI59 Register (Offset = 4ECh) [reset = 0h]

GICD_IPRIORITYR59

Return to Summary Table

Table 14-17218. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04ECh**

Figure 14-5710. GIC500_GICD_IPRIORITYR_SPI59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17220. GIC500_GICD_IPRIORITYR_SPI59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.118 GIC500_GICD_IPRIORITYR_SPI60 Register

1 GIC500_GICD_IPRIORITYR_SPI60 Register (Offset = 4F0h) [reset = 0h]

GICD_IPRIORITYR60

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Table 14-17221. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04F0h**

Figure 14-5711. GIC500_GICD_IPRIORITYR_SPI60 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17223. GIC500_GICD_IPRIORITYR_SPI60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.119 GIC500_GICD_IPRIORITYR_SPI61 Register

1 GIC500_GICD_IPRIORITYR_SPI61 Register (Offset = 4F4h) [reset = 0h]

GICD_IPRIORITYR61

Return to Summary Table

Table 14-17224. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04F4h**

Figure 14-5712. GIC500_GICD_IPRIORITYR_SPI61 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17226. GIC500_GICD_IPRIORITYR_SPI61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.120 GIC500_GICD_IPRIORITYR_SPI62 Register

1 GIC500_GICD_IPRIORITYR_SPI62 Register (Offset = 4F8h) [reset = 0h]

GICD_IPRIORITYR62

Return to Summary Table

Table 14-17227. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04F8h**

Figure 14-5713. GIC500_GICD_IPRIORITYR_SPI62 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17229. GIC500_GICD_IPRIORITYR_SPI62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.121 GIC500_GICD_IPRIORITYR_SPI63 Register

1 GIC500_GICD_IPRIORITYR_SPI63 Register (Offset = 4FCh) [reset = 0h]

GICD_IPRIORITYR63

Return to Summary Table

Table 14-17230. Instance Table

Instance Name	Physical Address
GICSS0	**0180 04FCh**

Figure 14-5714. GIC500_GICD_IPRIORITYR_SPI63 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17232. GIC500_GICD_IPRIORITYR_SPI63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.122 GIC500_GICD_IPRIORITYR_SPI64 Register

1 GIC500_GICD_IPRIORITYR_SPI64 Register (Offset = 500h) [reset = 0h]

GICD_IPRIORITYR64

Return to Summary Table

Table 14-17233. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0500h**

Figure 14-5715. GIC500_GICD_IPRIORITYR_SPI64 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17235. GIC500_GICD_IPRIORITYR_SPI64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.123 GIC500_GICD_IPRIORITYR_SPI65 Register

1 GIC500_GICD_IPRIORITYR_SPI65 Register (Offset = 504h) [reset = 0h]

GICD_IPRIORITYR65

Return to Summary Table

Table 14-17236. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0504h**

Figure 14-5716. GIC500_GICD_IPRIORITYR_SPI65 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17238. GIC500_GICD_IPRIORITYR_SPI65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.124 GIC500_GICD_IPRIORITYR_SPI66 Register

1 GIC500_GICD_IPRIORITYR_SPI66 Register (Offset = 508h) [reset = 0h]

GICD_IPRIORITYR66

Return to Summary Table

Table 14-17239. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0508h**

Figure 14-5717. GIC500_GICD_IPRIORITYR_SPI66 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17241. GIC500_GICD_IPRIORITYR_SPI66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.125 GIC500_GICD_IPRIORITYR_SPI67 Register

1 GIC500_GICD_IPRIORITYR_SPI67 Register (Offset = 50Ch) [reset = 0h]

GICD_IPRIORITYR67

Return to Summary Table

Table 14-17242. Instance Table

Instance Name	Physical Address
GICSS0	**0180 050Ch**

Figure 14-5718. GIC500_GICD_IPRIORITYR_SPI67 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17244. GIC500_GICD_IPRIORITYR_SPI67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.126 GIC500_GICD_IPRIORITYR_SPI68 Register

1 GIC500_GICD_IPRIORITYR_SPI68 Register (Offset = 510h) [reset = 0h]

GICD_IPRIORITYR68

Return to Summary Table

Table 14-17245. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0510h**

Figure 14-5719. GIC500_GICD_IPRIORITYR_SPI68 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17247. GIC500_GICD_IPRIORITYR_SPI68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.127 GIC500_GICD_IPRIORITYR_SPI69 Register

1 GIC500_GICD_IPRIORITYR_SPI69 Register (Offset = 514h) [reset = 0h]

GICD_IPRIORITYR69

Return to Summary Table

Table 14-17248. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0514h**

Figure 14-5720. GIC500_GICD_IPRIORITYR_SPI69 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17250. GIC500_GICD_IPRIORITYR_SPI69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.128 GIC500_GICD_IPRIORITYR_SPI70 Register

1 GIC500_GICD_IPRIORITYR_SPI70 Register (Offset = 518h) [reset = 0h]

GICD_IPRIORITYR70

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Table 14-17251. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0518h**

Figure 14-5721. GIC500_GICD_IPRIORITYR_SPI70 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-17253. GIC500_GICD_IPRIORITYR_SPI70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.129 GIC500_GICD_IPRIORITYR_SPI71 Register

1 GIC500_GICD_IPRIORITYR_SPI71 Register (Offset = 51Ch) [reset = 0h]

GICD_IPRIORITYR71

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Table 14-17254. Instance Table

Instance Name	Physical Address
GICSS0	**0180 051Ch**

Figure 14-5722. GIC500_GICD_IPRIORITYR_SPI71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17256. GIC500_GICD_IPRIORITYR_SPI71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.130 GIC500_GICD_ITARGETSR_SPI8 Register

1 GIC500_GICD_ITARGETSR_SPI8 Register (Offset = 820h) [reset = 0h]

GICD_ITARGETSR8

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Table 14-17257. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0820h**

Figure 14-5723. GIC500_GICD_ITARGETSR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17259. GIC500_GICD_ITARGETSR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.131 GIC500_GICD_ITARGETSR_SPI9 Register

1 GIC500_GICD_ITARGETSR_SPI9 Register (Offset = 824h) [reset = 0h]

GICD_ITARGETSR9

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Table 14-17260. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0824h**

Figure 14-5724. GIC500_GICD_ITARGETSR_SPI9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17262. GIC500_GICD_ITARGETSR_SPI9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.132 GIC500_GICD_ITARGETSR_SPI10 Register

1 GIC500_GICD_ITARGETSR_SPI10 Register (Offset = 828h) [reset = 0h]

GICD_ITARGETSR10

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Table 14-17263. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0828h**

Figure 14-5725. GIC500_GICD_ITARGETSR_SPI10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17265. GIC500_GICD_ITARGETSR_SPI10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.133 GIC500_GICD_ITARGETSR_SPI11 Register

1 GIC500_GICD_ITARGETSR_SPI11 Register (Offset = 82Ch) [reset = 0h]

GICD_ITARGETSR11

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Table 14-17266. Instance Table

Instance Name	Physical Address
GICSS0	**0180 082Ch**

Figure 14-5726. GIC500_GICD_ITARGETSR_SPI11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17268. GIC500_GICD_ITARGETSR_SPI11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.134 GIC500_GICD_ITARGETSR_SPI12 Register

1 GIC500_GICD_ITARGETSR_SPI12 Register (Offset = 830h) [reset = 0h]

GICD_ITARGETSR12

Return to Summary Table

Table 14-17269. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0830h**

Figure 14-5727. GIC500_GICD_ITARGETSR_SPI12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17271. GIC500_GICD_ITARGETSR_SPI12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.135 GIC500_GICD_ITARGETSR_SPI13 Register

1 GIC500_GICD_ITARGETSR_SPI13 Register (Offset = 834h) [reset = 0h]

GICD_ITARGETSR13

Return to Summary Table

Table 14-17272. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0834h**

Figure 14-5728. GIC500_GICD_ITARGETSR_SPI13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17274. GIC500_GICD_ITARGETSR_SPI13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.136 GIC500_GICD_ITARGETSR_SPI14 Register

1 GIC500_GICD_ITARGETSR_SPI14 Register (Offset = 838h) [reset = 0h]

GICD_ITARGETSR14

Return to Summary Table

Table 14-17275. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0838h**

Figure 14-5729. GIC500_GICD_ITARGETSR_SPI14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17277. GIC500_GICD_ITARGETSR_SPI14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.137 GIC500_GICD_ITARGETSR_SPI15 Register

1 GIC500_GICD_ITARGETSR_SPI15 Register (Offset = 83Ch) [reset = 0h]

GICD_ITARGETSR15

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Table 14-17278. Instance Table

Instance Name	Physical Address
GICSS0	**0180 083Ch**

Figure 14-5730. GIC500_GICD_ITARGETSR_SPI15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17280. GIC500_GICD_ITARGETSR_SPI15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.138 GIC500_GICD_ITARGETSR_SPI16 Register

1 GIC500_GICD_ITARGETSR_SPI16 Register (Offset = 840h) [reset = 0h]

GICD_ITARGETSR16

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Table 14-17281. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0840h**

Figure 14-5731. GIC500_GICD_ITARGETSR_SPI16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17283. GIC500_GICD_ITARGETSR_SPI16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.139 GIC500_GICD_ITARGETSR_SPI17 Register

1 GIC500_GICD_ITARGETSR_SPI17 Register (Offset = 844h) [reset = 0h]

GICD_ITARGETSR17

Return to Summary Table

Table 14-17284. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0844h**

Figure 14-5732. GIC500_GICD_ITARGETSR_SPI17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17286. GIC500_GICD_ITARGETSR_SPI17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.140 GIC500_GICD_ITARGETSR_SPI18 Register

1 GIC500_GICD_ITARGETSR_SPI18 Register (Offset = 848h) [reset = 0h]

GICD_ITARGETSR18

Return to Summary Table

Table 14-17287. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0848h**

Figure 14-5733. GIC500_GICD_ITARGETSR_SPI18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17289. GIC500_GICD_ITARGETSR_SPI18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.141 GIC500_GICD_ITARGETSR_SPI19 Register

1 GIC500_GICD_ITARGETSR_SPI19 Register (Offset = 84Ch) [reset = 0h]

GICD_ITARGETSR19

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Table 14-17290. Instance Table

Instance Name	Physical Address
GICSS0	**0180 084Ch**

Figure 14-5734. GIC500_GICD_ITARGETSR_SPI19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17292. GIC500_GICD_ITARGETSR_SPI19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.142 GIC500_GICD_ITARGETSR_SPI20 Register

1 GIC500_GICD_ITARGETSR_SPI20 Register (Offset = 850h) [reset = 0h]

GICD_ITARGETSR20

Return to Summary Table

Table 14-17293. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0850h**

Figure 14-5735. GIC500_GICD_ITARGETSR_SPI20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17295. GIC500_GICD_ITARGETSR_SPI20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.143 GIC500_GICD_ITARGETSR_SPI21 Register

1 GIC500_GICD_ITARGETSR_SPI21 Register (Offset = 854h) [reset = 0h]

GICD_ITARGETSR21

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Table 14-17296. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0854h**

Figure 14-5736. GIC500_GICD_ITARGETSR_SPI21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17298. GIC500_GICD_ITARGETSR_SPI21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.144 GIC500_GICD_ITARGETSR_SPI22 Register

1 GIC500_GICD_ITARGETSR_SPI22 Register (Offset = 858h) [reset = 0h]

GICD_ITARGETSR22

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Table 14-17299. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0858h**

Figure 14-5737. GIC500_GICD_ITARGETSR_SPI22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17301. GIC500_GICD_ITARGETSR_SPI22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.145 GIC500_GICD_ITARGETSR_SPI23 Register

1 GIC500_GICD_ITARGETSR_SPI23 Register (Offset = 85Ch) [reset = 0h]

GICD_ITARGETSR23

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Table 14-17302. Instance Table

Instance Name	Physical Address
GICSS0	**0180 085Ch**

Figure 14-5738. GIC500_GICD_ITARGETSR_SPI23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17304. GIC500_GICD_ITARGETSR_SPI23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.146 GIC500_GICD_ITARGETSR_SPI24 Register

1 GIC500_GICD_ITARGETSR_SPI24 Register (Offset = 860h) [reset = 0h]

GICD_ITARGETSR24

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Table 14-17305. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0860h**

Figure 14-5739. GIC500_GICD_ITARGETSR_SPI24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17307. GIC500_GICD_ITARGETSR_SPI24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.147 GIC500_GICD_ITARGETSR_SPI25 Register

1 GIC500_GICD_ITARGETSR_SPI25 Register (Offset = 864h) [reset = 0h]

GICD_ITARGETSR25

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Table 14-17308. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0864h**

Figure 14-5740. GIC500_GICD_ITARGETSR_SPI25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17310. GIC500_GICD_ITARGETSR_SPI25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.148 GIC500_GICD_ITARGETSR_SPI26 Register

1 GIC500_GICD_ITARGETSR_SPI26 Register (Offset = 868h) [reset = 0h]

GICD_ITARGETSR26

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Table 14-17311. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0868h**

Figure 14-5741. GIC500_GICD_ITARGETSR_SPI26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17313. GIC500_GICD_ITARGETSR_SPI26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.149 GIC500_GICD_ITARGETSR_SPI27 Register

1 GIC500_GICD_ITARGETSR_SPI27 Register (Offset = 86Ch) [reset = 0h]

GICD_ITARGETSR27

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Table 14-17314. Instance Table

Instance Name	Physical Address
GICSS0	0180 086Ch

Figure 14-5742. GIC500_GICD_ITARGETSR_SPI27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17316. GIC500_GICD_ITARGETSR_SPI27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.150 GIC500_GICD_ITARGETSR_SPI28 Register

1 GIC500_GICD_ITARGETSR_SPI28 Register (Offset = 870h) [reset = 0h]

GICD_ITARGETSR28

Return to Summary Table

Table 14-17317. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0870h**

Figure 14-5743. GIC500_GICD_ITARGETSR_SPI28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17319. GIC500_GICD_ITARGETSR_SPI28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.151 GIC500_GICD_ITARGETSR_SPI29 Register

1 GIC500_GICD_ITARGETSR_SPI29 Register (Offset = 874h) [reset = 0h]

GICD_ITARGETSR29

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Table 14-17320. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0874h**

Figure 14-5744. GIC500_GICD_ITARGETSR_SPI29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17322. GIC500_GICD_ITARGETSR_SPI29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.152 GIC500_GICD_ITARGETSR_SPI30 Register

1 GIC500_GICD_ITARGETSR_SPI30 Register (Offset = 878h) [reset = 0h]

GICD_ITARGETSR30

Return to Summary Table

Table 14-17323. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0878h**

Figure 14-5745. GIC500_GICD_ITARGETSR_SPI30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17325. GIC500_GICD_ITARGETSR_SPI30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.153 GIC500_GICD_ITARGETSR_SPI31 Register

1 GIC500_GICD_ITARGETSR_SPI31 Register (Offset = 87Ch) [reset = 0h]

GICD_ITARGETSR31

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Table 14-17326. Instance Table

Instance Name	Physical Address
GICSS0	**0180 087Ch**

Figure 14-5746. GIC500_GICD_ITARGETSR_SPI31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17328. GIC500_GICD_ITARGETSR_SPI31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.154 GIC500_GICD_ITARGETSR_SPI32 Register

1 GIC500_GICD_ITARGETSR_SPI32 Register (Offset = 880h) [reset = 0h]

GICD_ITARGETSR32

Return to Summary Table

Table 14-17329. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0880h**

Figure 14-5747. GIC500_GICD_ITARGETSR_SPI32 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17331. GIC500_GICD_ITARGETSR_SPI32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.155 GIC500_GICD_ITARGETSR_SPI33 Register

1 GIC500_GICD_ITARGETSR_SPI33 Register (Offset = 884h) [reset = 0h]

GICD_ITARGETSR33

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Table 14-17332. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0884h**

Figure 14-5748. GIC500_GICD_ITARGETSR_SPI33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17334. GIC500_GICD_ITARGETSR_SPI33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.156 GIC500_GICD_ITARGETSR_SPI34 Register

1 GIC500_GICD_ITARGETSR_SPI34 Register (Offset = 888h) [reset = 0h]

GICD_ITARGETSR34

Return to Summary Table

Table 14-17335. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0888h**

Figure 14-5749. GIC500_GICD_ITARGETSR_SPI34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17337. GIC500_GICD_ITARGETSR_SPI34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.157 GIC500_GICD_ITARGETSR_SPI35 Register

1 GIC500_GICD_ITARGETSR_SPI35 Register (Offset = 88Ch) [reset = 0h]

GICD_ITARGETSR35

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Table 14-17338. Instance Table

Instance Name	Physical Address
GICSS0	**0180 088Ch**

Figure 14-5750. GIC500_GICD_ITARGETSR_SPI35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17340. GIC500_GICD_ITARGETSR_SPI35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.158 GIC500_GICD_ITARGETSR_SPI36 Register

1 GIC500_GICD_ITARGETSR_SPI36 Register (Offset = 890h) [reset = 0h]

GICD_ITARGETSR36

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Table 14-17341. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0890h**

Figure 14-5751. GIC500_GICD_ITARGETSR_SPI36 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
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<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17343. GIC500_GICD_ITARGETSR_SPI36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.159 GIC500_GICD_ITARGETSR_SPI37 Register

1 GIC500_GICD_ITARGETSR_SPI37 Register (Offset = 894h) [reset = 0h]

GICD_ITARGETSR37

Return to Summary Table

Table 14-17344. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0894h**

Figure 14-5752. GIC500_GICD_ITARGETSR_SPI37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17346. GIC500_GICD_ITARGETSR_SPI37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.160 GIC500_GICD_ITARGETSR_SPI38 Register

1 GIC500_GICD_ITARGETSR_SPI38 Register (Offset = 898h) [reset = 0h]

GICD_ITARGETSR38

Return to Summary Table

Table 14-17347. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0898h**

Figure 14-5753. GIC500_GICD_ITARGETSR_SPI38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17349. GIC500_GICD_ITARGETSR_SPI38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.161 GIC500_GICD_ITARGETSR_SPI39 Register

1 GIC500_GICD_ITARGETSR_SPI39 Register (Offset = 89Ch) [reset = 0h]

GICD_ITARGETSR39

Return to Summary Table

Table 14-17350. Instance Table

Instance Name	Physical Address
GICSS0	**0180 089Ch**

Figure 14-5754. GIC500_GICD_ITARGETSR_SPI39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17352. GIC500_GICD_ITARGETSR_SPI39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.162 GIC500_GICD_ITARGETSR_SPI40 Register

1 GIC500_GICD_ITARGETSR_SPI40 Register (Offset = 8A0h) [reset = 0h]

GICD_ITARGETSR40

Return to Summary Table

Table 14-17353. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08A0h**

Figure 14-5755. GIC500_GICD_ITARGETSR_SPI40 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17355. GIC500_GICD_ITARGETSR_SPI40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.163 GIC500_GICD_ITARGETSR_SPI41 Register

1 GIC500_GICD_ITARGETSR_SPI41 Register (Offset = 8A4h) [reset = 0h]

GICD_ITARGETSR41

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Table 14-17356. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08A4h**

Figure 14-5756. GIC500_GICD_ITARGETSR_SPI41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17358. GIC500_GICD_ITARGETSR_SPI41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.164 GIC500_GICD_ITARGETSR_SPI42 Register

1 GIC500_GICD_ITARGETSR_SPI42 Register (Offset = 8A8h) [reset = 0h]

GICD_ITARGETSR42

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Table 14-17359. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08A8h**

Figure 14-5757. GIC500_GICD_ITARGETSR_SPI42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17361. GIC500_GICD_ITARGETSR_SPI42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.165 GIC500_GICD_ITARGETSR_SPI43 Register

1 GIC500_GICD_ITARGETSR_SPI43 Register (Offset = 8ACh) [reset = 0h]

GICD_ITARGETSR43

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Table 14-17362. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08ACh**

Figure 14-5758. GIC500_GICD_ITARGETSR_SPI43 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17364. GIC500_GICD_ITARGETSR_SPI43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.166 GIC500_GICD_ITARGETSR_SPI44 Register

1 GIC500_GICD_ITARGETSR_SPI44 Register (Offset = 8B0h) [reset = 0h]

GICD_ITARGETSR44

Return to Summary Table

Table 14-17365. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08B0h**

Figure 14-5759. GIC500_GICD_ITARGETSR_SPI44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17367. GIC500_GICD_ITARGETSR_SPI44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.167 GIC500_GICD_ITARGETSR_SPI45 Register

1 GIC500_GICD_ITARGETSR_SPI45 Register (Offset = 8B4h) [reset = 0h]

GICD_ITARGETSR45

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Table 14-17368. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08B4h**

Figure 14-5760. GIC500_GICD_ITARGETSR_SPI45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17370. GIC500_GICD_ITARGETSR_SPI45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.168 GIC500_GICD_ITARGETSR_SPI46 Register

1 GIC500_GICD_ITARGETSR_SPI46 Register (Offset = 8B8h) [reset = 0h]

GICD_ITARGETSR46

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Table 14-17371. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08B8h**

Figure 14-5761. GIC500_GICD_ITARGETSR_SPI46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17373. GIC500_GICD_ITARGETSR_SPI46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.169 GIC500_GICD_ITARGETSR_SPI47 Register

1 GIC500_GICD_ITARGETSR_SPI47 Register (Offset = 8BCh) [reset = 0h]

GICD_ITARGETSR47

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Table 14-17374. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 08BCh**

Figure 14-5762. GIC500_GICD_ITARGETSR_SPI47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17376. GIC500_GICD_ITARGETSR_SPI47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.170 GIC500_GICD_ITARGETSR_SPI48 Register

1 GIC500_GICD_ITARGETSR_SPI48 Register (Offset = 8C0h) [reset = 0h]

GICD_ITARGETSR48

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Table 14-17377. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08C0h**

Figure 14-5763. GIC500_GICD_ITARGETSR_SPI48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17379. GIC500_GICD_ITARGETSR_SPI48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.171 GIC500_GICD_ITARGETSR_SPI49 Register

1 GIC500_GICD_ITARGETSR_SPI49 Register (Offset = 8C4h) [reset = 0h]

GICD_ITARGETSR49

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Table 14-17380. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08C4h**

Figure 14-5764. GIC500_GICD_ITARGETSR_SPI49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17382. GIC500_GICD_ITARGETSR_SPI49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.172 GIC500_GICD_ITARGETSR_SPI50 Register

1 GIC500_GICD_ITARGETSR_SPI50 Register (Offset = 8C8h) [reset = 0h]

GICD_ITARGETSR50

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Table 14-17383. Instance Table

Instance Name	Physical Address
GICSS0	0180 08C8h

Figure 14-5765. GIC500_GICD_ITARGETSR_SPI50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17385. GIC500_GICD_ITARGETSR_SPI50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.173 GIC500_GICD_ITARGETSR_SPI51 Register

1 GIC500_GICD_ITARGETSR_SPI51 Register (Offset = 8CCh) [reset = 0h]

GICD_ITARGETSR51

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Table 14-17386. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08CCh**

Figure 14-5766. GIC500_GICD_ITARGETSR_SPI51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17388. GIC500_GICD_ITARGETSR_SPI51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.174 GIC500_GICD_ITARGETSR_SPI52 Register

1 GIC500_GICD_ITARGETSR_SPI52 Register (Offset = 8D0h) [reset = 0h]

GICD_ITARGETSR52

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Table 14-17389. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08D0h**

Figure 14-5767. GIC500_GICD_ITARGETSR_SPI52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17391. GIC500_GICD_ITARGETSR_SPI52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.175 GIC500_GICD_ITARGETSR_SPI53 Register

1 GIC500_GICD_ITARGETSR_SPI53 Register (Offset = 8D4h) [reset = 0h]

GICD_ITARGETSR53

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Table 14-17392. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08D4h**

Figure 14-5768. GIC500_GICD_ITARGETSR_SPI53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17394. GIC500_GICD_ITARGETSR_SPI53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.176 GIC500_GICD_ITARGETSR_SPI54 Register

1 GIC500_GICD_ITARGETSR_SPI54 Register (Offset = 8D8h) [reset = 0h]

GICD_ITARGETSR54

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Table 14-17395. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08D8h**

Figure 14-5769. GIC500_GICD_ITARGETSR_SPI54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17397. GIC500_GICD_ITARGETSR_SPI54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.177 GIC500_GICD_ITARGETSR_SPI55 Register

1 GIC500_GICD_ITARGETSR_SPI55 Register (Offset = 8DCh) [reset = 0h]

GICD_ITARGETSR55

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Table 14-17398. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08DCh**

Figure 14-5770. GIC500_GICD_ITARGETSR_SPI55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17400. GIC500_GICD_ITARGETSR_SPI55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.178 GIC500_GICD_ITARGETSR_SPI56 Register

1 GIC500_GICD_ITARGETSR_SPI56 Register (Offset = 8E0h) [reset = 0h]

GICD_ITARGETSR56

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Table 14-17401. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08E0h**

Figure 14-5771. GIC500_GICD_ITARGETSR_SPI56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17403. GIC500_GICD_ITARGETSR_SPI56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.179 GIC500_GICD_ITARGETSR_SPI57 Register

1 GIC500_GICD_ITARGETSR_SPI57 Register (Offset = 8E4h) [reset = 0h]

GICD_ITARGETSR57

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Table 14-17404. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08E4h**

Figure 14-5772. GIC500_GICD_ITARGETSR_SPI57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17406. GIC500_GICD_ITARGETSR_SPI57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.180 GIC500_GICD_ITARGETSR_SPI58 Register

1 GIC500_GICD_ITARGETSR_SPI58 Register (Offset = 8E8h) [reset = 0h]

GICD_ITARGETSR58

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Table 14-17407. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08E8h**

Figure 14-5773. GIC500_GICD_ITARGETSR_SPI58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17409. GIC500_GICD_ITARGETSR_SPI58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.181 GIC500_GICD_ITARGETSR_SPI59 Register

1 GIC500_GICD_ITARGETSR_SPI59 Register (Offset = 8ECh) [reset = 0h]

GICD_ITARGETSR59

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Table 14-17410. Instance Table

Instance Name	Physical Address
GICSS0	0180 08ECh

Figure 14-5774. GIC500_GICD_ITARGETSR_SPI59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17412. GIC500_GICD_ITARGETSR_SPI59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.182 GIC500_GICD_ITARGETSR_SPI60 Register

1 GIC500_GICD_ITARGETSR_SPI60 Register (Offset = 8F0h) [reset = 0h]

GICD_ITARGETSR60

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Table 14-17413. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08F0h**

Figure 14-5775. GIC500_GICD_ITARGETSR_SPI60 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17415. GIC500_GICD_ITARGETSR_SPI60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.183 GIC500_GICD_ITARGETSR_SPI61 Register

1 GIC500_GICD_ITARGETSR_SPI61 Register (Offset = 8F4h) [reset = 0h]

GICD_ITARGETSR61

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Table 14-17416. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08F4h**

Figure 14-5776. GIC500_GICD_ITARGETSR_SPI61 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17418. GIC500_GICD_ITARGETSR_SPI61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.184 GIC500_GICD_ITARGETSR_SPI62 Register

1 GIC500_GICD_ITARGETSR_SPI62 Register (Offset = 8F8h) [reset = 0h]

GICD_ITARGETSR62

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Table 14-17419. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08F8h**

Figure 14-5777. GIC500_GICD_ITARGETSR_SPI62 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17421. GIC500_GICD_ITARGETSR_SPI62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.185 GIC500_GICD_ITARGETSR_SPI63 Register

1 GIC500_GICD_ITARGETSR_SPI63 Register (Offset = 8FCh) [reset = 0h]

GICD_ITARGETSR63

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Table 14-17422. Instance Table

Instance Name	Physical Address
GICSS0	**0180 08FCh**

Figure 14-5778. GIC500_GICD_ITARGETSR_SPI63 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17424. GIC500_GICD_ITARGETSR_SPI63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.186 GIC500_GICD_ITARGETSR_SPI64 Register

1 GIC500_GICD_ITARGETSR_SPI64 Register (Offset = 900h) [reset = 0h]

GICD_ITARGETSR64

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Table 14-17425. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0900h**

Figure 14-5779. GIC500_GICD_ITARGETSR_SPI64 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17427. GIC500_GICD_ITARGETSR_SPI64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.187 GIC500_GICD_ITARGETSR_SPI65 Register

1 GIC500_GICD_ITARGETSR_SPI65 Register (Offset = 904h) [reset = 0h]

GICD_ITARGETSR65

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Table 14-17428. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0904h**

Figure 14-5780. GIC500_GICD_ITARGETSR_SPI65 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17430. GIC500_GICD_ITARGETSR_SPI65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.188 GIC500_GICD_ITARGETSR_SPI66 Register

1 GIC500_GICD_ITARGETSR_SPI66 Register (Offset = 908h) [reset = 0h]

GICD_ITARGETSR66

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Table 14-17431. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0908h**

Figure 14-5781. GIC500_GICD_ITARGETSR_SPI66 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17433. GIC500_GICD_ITARGETSR_SPI66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.189 GIC500_GICD_ITARGETSR_SPI67 Register

1 GIC500_GICD_ITARGETSR_SPI67 Register (Offset = 90Ch) [reset = 0h]

GICD_ITARGETSR67

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Table 14-17434. Instance Table

Instance Name	Physical Address
GICSS0	**0180 090Ch**

Figure 14-5782. GIC500_GICD_ITARGETSR_SPI67 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17436. GIC500_GICD_ITARGETSR_SPI67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.190 GIC500_GICD_ITARGETSR_SPI68 Register

1 GIC500_GICD_ITARGETSR_SPI68 Register (Offset = 910h) [reset = 0h]

GICD_ITARGETSR68

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Table 14-17437. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0910h**

Figure 14-5783. GIC500_GICD_ITARGETSR_SPI68 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17439. GIC500_GICD_ITARGETSR_SPI68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.191 GIC500_GICD_ITARGETSR_SPI69 Register

1 GIC500_GICD_ITARGETSR_SPI69 Register (Offset = 914h) [reset = 0h]

GICD_ITARGETSR69

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Table 14-17440. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0914h**

Figure 14-5784. GIC500_GICD_ITARGETSR_SPI69 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17442. GIC500_GICD_ITARGETSR_SPI69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.192 GIC500_GICD_ITARGETSR_SPI70 Register

1 GIC500_GICD_ITARGETSR_SPI70 Register (Offset = 918h) [reset = 0h]

GICD_ITARGETSR70

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Table 14-17443. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0918h**

Figure 14-5785. GIC500_GICD_ITARGETSR_SPI70 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17445. GIC500_GICD_ITARGETSR_SPI70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.193 GIC500_GICD_ITARGETSR_SPI71 Register

1 GIC500_GICD_ITARGETSR_SPI71 Register (Offset = 91Ch) [reset = 0h]

GICD_ITARGETSR71

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Table 14-17446. Instance Table

Instance Name	Physical Address
GICSS0	**0180 091Ch**

Figure 14-5786. GIC500_GICD_ITARGETSR_SPI71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17448. GIC500_GICD_ITARGETSR_SPI71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.194 GIC500_GICD_ICFGR_SPI2 Register

1 GIC500_GICD_ICFGR_SPI2 Register (Offset = C08h) [reset = 0h]

GICD_ICFGR2

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Table 14-17449. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C08h**

Figure 14-5787. GIC500_GICD_ICFGR_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17451. GIC500_GICD_ICFGR_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.195 GIC500_GICD_ICFGR_SPI3 Register

1 GIC500_GICD_ICFGR_SPI3 Register (Offset = C0Ch) [reset = 0h]

GICD_ICFGR3

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Table 14-17452. Instance Table

Instance Name	Physical Address
GICSS0	0180 0C0Ch

Figure 14-5788. GIC500_GICD_ICFGR_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17454. GIC500_GICD_ICFGR_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.196 GIC500_GICD_ICFGR_SPI4 Register

1 GIC500_GICD_ICFGR_SPI4 Register (Offset = C10h) [reset = 0h]

GICD_ICFGR4

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Table 14-17455. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C10h**

Figure 14-5789. GIC500_GICD_ICFGR_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17457. GIC500_GICD_ICFGR_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.197 GIC500_GICD_ICFGR_SPI5 Register

1 GIC500_GICD_ICFGR_SPI5 Register (Offset = C14h) [reset = 0h]

GICD_ICFGR5

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Table 14-17458. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C14h**

Figure 14-5790. GIC500_GICD_ICFGR_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17460. GIC500_GICD_ICFGR_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.198 GIC500_GICD_ICFGR_SPI6 Register

1 GIC500_GICD_ICFGR_SPI6 Register (Offset = C18h) [reset = 0h]

GICD_ICFGR6

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Table 14-17461. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C18h**

Figure 14-5791. GIC500_GICD_ICFGR_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17463. GIC500_GICD_ICFGR_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.199 GIC500_GICD_ICFGR_SPI7 Register

1 GIC500_GICD_ICFGR_SPI7 Register (Offset = C1Ch) [reset = 0h]

GICD_ICFGR7

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Table 14-17464. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C1Ch**

Figure 14-5792. GIC500_GICD_ICFGR_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17466. GIC500_GICD_ICFGR_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.200 GIC500_GICD_ICFGR_SPI8 Register

1 GIC500_GICD_ICFGR_SPI8 Register (Offset = C20h) [reset = 0h]

GICD_ICFGR8

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Table 14-17467. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C20h**

Figure 14-5793. GIC500_GICD_ICFGR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17469. GIC500_GICD_ICFGR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.201 GIC500_GICD_ICFGR_SPI9 Register

1 GIC500_GICD_ICFGR_SPI9 Register (Offset = C24h) [reset = 0h]

GICD_ICFGR9

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Table 14-17470. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 0C24h**

Figure 14-5794. GIC500_GICD_ICFGR_SPI9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17472. GIC500_GICD_ICFGR_SPI9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.202 GIC500_GICD_ICFGR_SPI10 Register

1 GIC500_GICD_ICFGR_SPI10 Register (Offset = C28h) [reset = 0h]

GICD_ICFGR10

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Table 14-17473. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C28h**

Figure 14-5795. GIC500_GICD_ICFGR_SPI10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17475. GIC500_GICD_ICFGR_SPI10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.203 GIC500_GICD_ICFGR_SPI11 Register

1 GIC500_GICD_ICFGR_SPI11 Register (Offset = C2Ch) [reset = 0h]

GICD_ICFGR11

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Table 14-17476. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C2Ch**

Figure 14-5796. GIC500_GICD_ICFGR_SPI11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17478. GIC500_GICD_ICFGR_SPI11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.204 GIC500_GICD_ICFGR_SPI12 Register

1 GIC500_GICD_ICFGR_SPI12 Register (Offset = C30h) [reset = 0h]

GICD_ICFGR12

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Table 14-17479. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C30h**

Figure 14-5797. GIC500_GICD_ICFGR_SPI12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17481. GIC500_GICD_ICFGR_SPI12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.205 GIC500_GICD_ICFGR_SPI13 Register

1 GIC500_GICD_ICFGR_SPI13 Register (Offset = C34h) [reset = 0h]

GICD_ICFGR13

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Table 14-17482. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C34h**

Figure 14-5798. GIC500_GICD_ICFGR_SPI13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17484. GIC500_GICD_ICFGR_SPI13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.206 GIC500_GICD_ICFGR_SPI14 Register

1 GIC500_GICD_ICFGR_SPI14 Register (Offset = C38h) [reset = 0h]

GICD_ICFGR14

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Table 14-17485. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C38h**

Figure 14-5799. GIC500_GICD_ICFGR_SPI14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17487. GIC500_GICD_ICFGR_SPI14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.207 GIC500_GICD_ICFGR_SPI15 Register

1 GIC500_GICD_ICFGR_SPI15 Register (Offset = C3Ch) [reset = 0h]

GICD_ICFGR15

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Table 14-17488. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C3Ch**

Figure 14-5800. GIC500_GICD_ICFGR_SPI15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17490. GIC500_GICD_ICFGR_SPI15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.208 GIC500_GICD_ICFGR_SPI16 Register

1 GIC500_GICD_ICFGR_SPI16 Register (Offset = C40h) [reset = 0h]

GICD_ICFGR16

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Table 14-17491. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C40h**

Figure 14-5801. GIC500_GICD_ICFGR_SPI16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17493. GIC500_GICD_ICFGR_SPI16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.209 GIC500_GICD_ICFGR_SPI17 Register

1 GIC500_GICD_ICFGR_SPI17 Register (Offset = C44h) [reset = 0h]

GICD_ICFGR17

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Table 14-17494. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0C44h**

Figure 14-5802. GIC500_GICD_ICFGR_SPI17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17496. GIC500_GICD_ICFGR_SPI17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.210 GIC500_GICD_IGRPMODR_SGI_PPI Register

1 GIC500_GICD_IGRPMODR_SGI_PPI Register (Offset = D00h) [reset = 0h]

GICD_IGRPMODR0

Return to Summary Table

Table 14-17497. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D00h**

Figure 14-5803. GIC500_GICD_IGRPMODR_SGI_PPI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17499. GIC500_GICD_IGRPMODR_SGI_PPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.211 GIC500_GICD_IGRPMODR_SPI1 Register

1 GIC500_GICD_IGRPMODR_SPI1 Register (Offset = D04h) [reset = 0h]

GICD_IGRPMODR1

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Table 14-17500. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D04h**

Figure 14-5804. GIC500_GICD_IGRPMODR_SPI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17502. GIC500_GICD_IGRPMODR_SPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.212 GIC500_GICD_IGRPMODR_SPI2 Register

1 GIC500_GICD_IGRPMODR_SPI2 Register (Offset = D08h) [reset = 0h]

GICD_IGRPMODR2

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Table 14-17503. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D08h**

Figure 14-5805. GIC500_GICD_IGRPMODR_SPI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17505. GIC500_GICD_IGRPMODR_SPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.213 GIC500_GICD_IGRPMODR_SPI3 Register

1 GIC500_GICD_IGRPMODR_SPI3 Register (Offset = D0Ch) [reset = 0h]

GICD_IGRPMODR3

Return to Summary Table

Table 14-17506. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D0Ch**

Figure 14-5806. GIC500_GICD_IGRPMODR_SPI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17508. GIC500_GICD_IGRPMODR_SPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.214 GIC500_GICD_IGRPMODR_SPI4 Register

1 GIC500_GICD_IGRPMODR_SPI4 Register (Offset = D10h) [reset = 0h]

GICD_IGRPMODR4

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Table 14-17509. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D10h**

Figure 14-5807. GIC500_GICD_IGRPMODR_SPI4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17511. GIC500_GICD_IGRPMODR_SPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.215 GIC500_GICD_IGRPMODR_SPI5 Register

1 GIC500_GICD_IGRPMODR_SPI5 Register (Offset = D14h) [reset = 0h]

GICD_IGRPMODR5

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Table 14-17512. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D14h**

Figure 14-5808. GIC500_GICD_IGRPMODR_SPI5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17514. GIC500_GICD_IGRPMODR_SPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.216 GIC500_GICD_IGRPMODR_SPI6 Register

1 GIC500_GICD_IGRPMODR_SPI6 Register (Offset = D18h) [reset = 0h]

GICD_IGRPMODR6

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Table 14-17515. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D18h**

Figure 14-5809. GIC500_GICD_IGRPMODR_SPI6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17517. GIC500_GICD_IGRPMODR_SPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.217 GIC500_GICD_IGRPMODR_SPI7 Register

1 GIC500_GICD_IGRPMODR_SPI7 Register (Offset = D1Ch) [reset = 0h]

GICD_IGRPMODR7

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Table 14-17518. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D1Ch**

Figure 14-5810. GIC500_GICD_IGRPMODR_SPI7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17520. GIC500_GICD_IGRPMODR_SPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.218 GIC500_GICD_IGRPMODR_SPI8 Register

1 GIC500_GICD_IGRPMODR_SPI8 Register (Offset = D20h) [reset = 0h]

GICD_IGRPMODR8

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Table 14-17521. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0D20h**

Figure 14-5811. GIC500_GICD_IGRPMODR_SPI8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17523. GIC500_GICD_IGRPMODR_SPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.219 GIC500_GICD_NSACR0 Register

1 GIC500_GICD_NSACR0 Register (Offset = E00h) [reset = 0h]

GICD_NSACR0

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Table 14-17524. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E00h**

Figure 14-5812. GIC500_GICD_NSACR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17526. GIC500_GICD_NSACR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.220 GIC500_GICD_NSACR1 Register

1 GIC500_GICD_NSACR1 Register (Offset = E04h) [reset = 0h]

GICD_NSACR1

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Table 14-17527. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E04h**

Figure 14-5813. GIC500_GICD_NSACR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17529. GIC500_GICD_NSACR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.221 GIC500_GICD_NSACR2 Register

1 GIC500_GICD_NSACR2 Register (Offset = E08h) [reset = 0h]

GICD_NSACR2

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Table 14-17530. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E08h**

Figure 14-5814. GIC500_GICD_NSACR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17532. GIC500_GICD_NSACR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.222 GIC500_GICD_NSACR3 Register

1 GIC500_GICD_NSACR3 Register (Offset = E0Ch) [reset = 0h]

GICD_NSACR3

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Table 14-17533. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E0Ch**

Figure 14-5815. GIC500_GICD_NSACR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17535. GIC500_GICD_NSACR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.223 GIC500_GICD_NSACR4 Register

1 GIC500_GICD_NSACR4 Register (Offset = E10h) [reset = 0h]

GICD_NSACR4

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Table 14-17536. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E10h**

Figure 14-5816. GIC500_GICD_NSACR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17538. GIC500_GICD_NSACR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.224 GIC500_GICD_NSACR5 Register

1 GIC500_GICD_NSACR5 Register (Offset = E14h) [reset = 0h]

GICD_NSACR5

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Table 14-17539. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E14h**

Figure 14-5817. GIC500_GICD_NSACR5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17541. GIC500_GICD_NSACR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.225 GIC500_GICD_NSACR6 Register

1 GIC500_GICD_NSACR6 Register (Offset = E18h) [reset = 0h]

GICD_NSACR6

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Table 14-17542. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E18h**

Figure 14-5818. GIC500_GICD_NSACR6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17544. GIC500_GICD_NSACR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.226 GIC500_GICD_NSACR7 Register

1 GIC500_GICD_NSACR7 Register (Offset = E1Ch) [reset = 0h]

GICD_NSACR7

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Table 14-17545. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E1Ch**

Figure 14-5819. GIC500_GICD_NSACR7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17547. GIC500_GICD_NSACR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.227 GIC500_GICD_NSACR8 Register

1 GIC500_GICD_NSACR8 Register (Offset = E20h) [reset = 0h]

GICD_NSACR8

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Table 14-17548. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E20h**

Figure 14-5820. GIC500_GICD_NSACR8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17550. GIC500_GICD_NSACR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.228 GIC500_GICD_NSACR9 Register

1 GIC500_GICD_NSACR9 Register (Offset = E24h) [reset = 0h]

GICD_NSACR9

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Table 14-17551. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E24h**

Figure 14-5821. GIC500_GICD_NSACR9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17553. GIC500_GICD_NSACR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.229 GIC500_GICD_NSACR10 Register

1 GIC500_GICD_NSACR10 Register (Offset = E28h) [reset = 0h]

GICD_NSACR10

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Table 14-17554. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 0E28h**

Figure 14-5822. GIC500_GICD_NSACR10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17556. GIC500_GICD_NSACR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.230 GIC500_GICD_NSACR11 Register

1 GIC500_GICD_NSACR11 Register (Offset = E2Ch) [reset = 0h]

GICD_NSACR11

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Table 14-17557. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E2Ch**

Figure 14-5823. GIC500_GICD_NSACR11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17559. GIC500_GICD_NSACR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.231 GIC500_GICD_NSACR12 Register

1 GIC500_GICD_NSACR12 Register (Offset = E30h) [reset = 0h]

GICD_NSACR12

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Table 14-17560. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E30h**

Figure 14-5824. GIC500_GICD_NSACR12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17562. GIC500_GICD_NSACR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.232 GIC500_GICD_NSACR13 Register

1 GIC500_GICD_NSACR13 Register (Offset = E34h) [reset = 0h]

GICD_NSACR13

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Table 14-17563. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E34h**

Figure 14-5825. GIC500_GICD_NSACR13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17565. GIC500_GICD_NSACR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.233 GIC500_GICD_NSACR14 Register

1 GIC500_GICD_NSACR14 Register (Offset = E38h) [reset = 0h]

GICD_NSACR14

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Table 14-17566. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E38h**

Figure 14-5826. GIC500_GICD_NSACR14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17568. GIC500_GICD_NSACR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.234 GIC500_GICD_NSACR15 Register

1 GIC500_GICD_NSACR15 Register (Offset = E3Ch) [reset = 0h]

GICD_NSACR15

Return to Summary Table

Table 14-17569. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E3Ch**

Figure 14-5827. GIC500_GICD_NSACR15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17571. GIC500_GICD_NSACR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.235 GIC500_GICD_NSACR16 Register

1 GIC500_GICD_NSACR16 Register (Offset = E40h) [reset = 0h]

GICD_NSACR16

Return to Summary Table

Table 14-17572. Instance Table

Instance Name	Physical Address
GICSS0	0180 0E40h

Figure 14-5828. GIC500_GICD_NSACR16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17574. GIC500_GICD_NSACR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.236 GIC500_GICD_NSACR17 Register

1 GIC500_GICD_NSACR17 Register (Offset = E44h) [reset = 0h]

GICD_NSACR17

Return to Summary Table

Table 14-17575. Instance Table

Instance Name	Physical Address
GICSS0	**0180 0E44h**

Figure 14-5829. GIC500_GICD_NSACR17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17577. GIC500_GICD_NSACR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.237 GIC500_GICD_IROUTER_LOWER32 Register

1 GIC500_GICD_IROUTER_LOWER32 Register (Offset = 6100h) [reset = 0h]

GICD_IROUTER32_lower

Return to Summary Table

Table 14-17578. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6100h**

Figure 14-5830. GIC500_GICD_IROUTER_LOWER32 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER32_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER32_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER32_LOWER__0_8							
R/W							
0h							

Table 14-17580. GIC500_GICD_IROUTER_LOWER32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER32_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER32_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER32_LOWER__0_8	R/W	0h	A0

14.4.1.2.238 GIC500_GICD_IROUTER_UPPER32 Register

1 GIC500_GICD_IROUTER_UPPER32 Register (Offset = 6104h) [reset = 0h]

GICD_IROUTER32_upper

Return to Summary Table

Table 14-17581. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6104h**

Figure 14-5831. GIC500_GICD_IROUTER_UPPER32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17583. GIC500_GICD_IROUTER_UPPER32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.239 GIC500_GICD_IROUTER_LOWER33 Register

1 GIC500_GICD_IROUTER_LOWER33 Register (Offset = 6108h) [reset = 0h]

GICD_IROUTER33_lower

Return to Summary Table

Table 14-17584. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6108h**

Figure 14-5832. GIC500_GICD_IROUTER_LOWER33 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER33_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER33_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER33_LOWER__0_8							
R/W							
0h							

Table 14-17586. GIC500_GICD_IROUTER_LOWER33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER33_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER33_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER33_LOWER__0_8	R/W	0h	A0

14.4.1.2.240 GIC500_GICD_IROUTER_UPPER33 Register

1 GIC500_GICD_IROUTER_UPPER33 Register (Offset = 610Ch) [reset = 0h]

GICD_IROUTER33_upper

Return to Summary Table

Table 14-17587. Instance Table

Instance Name	Physical Address
GICSS0	**0180 610Ch**

Figure 14-5833. GIC500_GICD_IROUTER_UPPER33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17589. GIC500_GICD_IROUTER_UPPER33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.241 GIC500_GICD_IROUTER_LOWER34 Register

1 GIC500_GICD_IROUTER_LOWER34 Register (Offset = 6110h) [reset = 0h]

GICD_IROUTER34_lower

Return to Summary Table

Table 14-17590. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6110h**

Figure 14-5834. GIC500_GICD_IROUTER_LOWER34 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER34_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER34_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER34_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17592. GIC500_GICD_IROUTER_LOWER34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER34_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER34_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER34_LOWER__0_8	R/W	0h	A0

14.4.1.2.242 GIC500_GICD_IROUTER_UPPER34 Register

1 GIC500_GICD_IROUTER_UPPER34 Register (Offset = 6114h) [reset = 0h]

GICD_IROUTER34_upper

Return to Summary Table

Table 14-17593. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6114h**

Figure 14-5835. GIC500_GICD_IROUTER_UPPER34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17595. GIC500_GICD_IROUTER_UPPER34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.243 GIC500_GICD_IROUTER_LOWER35 Register

1 GIC500_GICD_IROUTER_LOWER35 Register (Offset = 6118h) [reset = 0h]

GICD_IROUTER35_lower

Return to Summary Table

Table 14-17596. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6118h**

Figure 14-5836. GIC500_GICD_IROUTER_LOWER35 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER35_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER35_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER35_LOWER__0_8							
R/W							
0h							

Table 14-17598. GIC500_GICD_IROUTER_LOWER35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER35_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER35_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER35_LOWER__0_8	R/W	0h	A0

14.4.1.2.244 GIC500_GICD_IROUTER_UPPER35 Register

1 GIC500_GICD_IROUTER_UPPER35 Register (Offset = 611Ch) [reset = 0h]

GICD_IROUTER35_upper

Return to Summary Table

Table 14-17599. Instance Table

Instance Name	Physical Address
GICSS0	**0180 611Ch**

Figure 14-5837. GIC500_GICD_IROUTER_UPPER35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17601. GIC500_GICD_IROUTER_UPPER35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.245 GIC500_GICD_IROUTER_LOWER36 Register

1 GIC500_GICD_IROUTER_LOWER36 Register (Offset = 6120h) [reset = 0h]

GICD_IROUTER36_lower

Return to Summary Table

Table 14-17602. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6120h**

Figure 14-5838. GIC500_GICD_IROUTER_LOWER36 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER36_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER36_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER36_LOWER__0_8							
R/W							
0h							

Table 14-17604. GIC500_GICD_IROUTER_LOWER36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER36_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER36_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER36_LOWER__0_8	R/W	0h	A0

14.4.1.2.246 GIC500_GICD_IROUTER_UPPER36 Register

1 GIC500_GICD_IROUTER_UPPER36 Register (Offset = 6124h) [reset = 0h]

GICD_IROUTER36_upper

Return to Summary Table

Table 14-17605. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 6124h**

Figure 14-5839. GIC500_GICD_IROUTER_UPPER36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17607. GIC500_GICD_IROUTER_UPPER36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.247 GIC500_GICD_IROUTER_LOWER37 Register

1 GIC500_GICD_IROUTER_LOWER37 Register (Offset = 6128h) [reset = 0h]

GICD_IROUTER37_lower

Return to Summary Table

Table 14-17608. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6128h**

Figure 14-5840. GIC500_GICD_IROUTER_LOWER37 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER37_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER37_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER37_LOWER__0_8							
R/W							
0h							

Table 14-17610. GIC500_GICD_IROUTER_LOWER37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER37_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER37_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER37_LOWER__0_8	R/W	0h	A0

14.4.1.2.248 GIC500_GICD_IROUTER_UPPER37 Register

1 GIC500_GICD_IROUTER_UPPER37 Register (Offset = 612Ch) [reset = 0h]

GICD_IROUTER37_upper

Return to Summary Table

Table 14-17611. Instance Table

Instance Name	Physical Address
GICSS0	**0180 612Ch**

Figure 14-5841. GIC500_GICD_IROUTER_UPPER37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17613. GIC500_GICD_IROUTER_UPPER37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.249 GIC500_GICD_IROUTER_LOWER38 Register

1 GIC500_GICD_IROUTER_LOWER38 Register (Offset = 6130h) [reset = 0h]

GICD_IROUTER38_lower

Return to Summary Table

Table 14-17614. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6130h**

Figure 14-5842. GIC500_GICD_IROUTER_LOWER38 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER38_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER38_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER38_LOWER__0_8							
R/W							
0h							

Table 14-17616. GIC500_GICD_IROUTER_LOWER38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER38_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER38_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER38_LOWER__0_8	R/W	0h	A0

14.4.1.2.250 GIC500_GICD_IROUTER_UPPER38 Register

1 GIC500_GICD_IROUTER_UPPER38 Register (Offset = 6134h) [reset = 0h]

GICD_IROUTER38_upper

Return to Summary Table

Table 14-17617. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6134h**

Figure 14-5843. GIC500_GICD_IROUTER_UPPER38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17619. GIC500_GICD_IROUTER_UPPER38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.251 GIC500_GICD_IROUTER_LOWER39 Register

1 GIC500_GICD_IROUTER_LOWER39 Register (Offset = 6138h) [reset = 0h]

GICD_IROUTER39_lower

Return to Summary Table

Table 14-17620. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6138h**

Figure 14-5844. GIC500_GICD_IROUTER_LOWER39 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER39_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER39_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER39_LOWER__0_8							
R/W							
0h							

Table 14-17622. GIC500_GICD_IROUTER_LOWER39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER39_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER39_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER39_LOWER__0_8	R/W	0h	A0

14.4.1.2.252 GIC500_GICD_IROUTER_UPPER39 Register

1 GIC500_GICD_IROUTER_UPPER39 Register (Offset = 613Ch) [reset = 0h]

GICD_IROUTER39_upper

Return to Summary Table

Table 14-17623. Instance Table

Instance Name	Physical Address
GICSS0	**0180 613Ch**

Figure 14-5845. GIC500_GICD_IROUTER_UPPER39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17625. GIC500_GICD_IROUTER_UPPER39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.253 GIC500_GICD_IROUTER_LOWER40 Register

1 GIC500_GICD_IROUTER_LOWER40 Register (Offset = 6140h) [reset = 0h]

GICD_IROUTER40_lower

Return to Summary Table

Table 14-17626. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6140h**

Figure 14-5846. GIC500_GICD_IROUTER_LOWER40 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER40_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER40_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER40_LOWER__0_8							
R/W							
0h							

Table 14-17628. GIC500_GICD_IROUTER_LOWER40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER40_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER40_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER40_LOWER__0_8	R/W	0h	A0

14.4.1.2.254 GIC500_GICD_IROUTER_UPPER40 Register

1 GIC500_GICD_IROUTER_UPPER40 Register (Offset = 6144h) [reset = 0h]

GICD_IROUTER40_upper

Return to Summary Table

Table 14-17629. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6144h**

Figure 14-5847. GIC500_GICD_IROUTER_UPPER40 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17631. GIC500_GICD_IROUTER_UPPER40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.255 GIC500_GICD_IROUTER_LOWER41 Register

1 GIC500_GICD_IROUTER_LOWER41 Register (Offset = 6148h) [reset = 0h]

GICD_IROUTER41_lower

Return to Summary Table

Table 14-17632. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6148h**

Figure 14-5848. GIC500_GICD_IROUTER_LOWER41 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER41_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER41_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER41_LOWER__0_8							
R/W							
0h							

Table 14-17634. GIC500_GICD_IROUTER_LOWER41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER41_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER41_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER41_LOWER__0_8	R/W	0h	A0

14.4.1.2.256 GIC500_GICD_IROUTER_UPPER41 Register

1 GIC500_GICD_IROUTER_UPPER41 Register (Offset = 614Ch) [reset = 0h]

GICD_IROUTER41_upper

Return to Summary Table

Table 14-17635. Instance Table

Instance Name	Physical Address
GICSS0	**0180 614Ch**

Figure 14-5849. GIC500_GICD_IROUTER_UPPER41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17637. GIC500_GICD_IROUTER_UPPER41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.257 GIC500_GICD_IROUTER_LOWER42 Register

1 GIC500_GICD_IROUTER_LOWER42 Register (Offset = 6150h) [reset = 0h]

GICD_IROUTER42_lower

Return to Summary Table

Table 14-17638. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6150h**

Figure 14-5850. GIC500_GICD_IROUTER_LOWER42 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER42_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER42_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER42_LOWER__0_8							
R/W							
0h							

Table 14-17640. GIC500_GICD_IROUTER_LOWER42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER42_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER42_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER42_LOWER__0_8	R/W	0h	A0

14.4.1.2.258 GIC500_GICD_IROUTER_UPPER42 Register

1 GIC500_GICD_IROUTER_UPPER42 Register (Offset = 6154h) [reset = 0h]

GICD_IROUTER42_upper

Return to Summary Table

Table 14-17641. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6154h**

Figure 14-5851. GIC500_GICD_IROUTER_UPPER42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17643. GIC500_GICD_IROUTER_UPPER42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.259 GIC500_GICD_IROUTER_LOWER43 Register

1 GIC500_GICD_IROUTER_LOWER43 Register (Offset = 6158h) [reset = 0h]

GICD_IROUTER43_lower

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Table 14-17644. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6158h**

Figure 14-5852. GIC500_GICD_IROUTER_LOWER43 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER43_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER43_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER43_LOWER__0_8							
R/W							
0h							

Table 14-17646. GIC500_GICD_IROUTER_LOWER43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER43_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER43_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER43_LOWER__0_8	R/W	0h	A0

14.4.1.2.260 GIC500_GICD_IROUTER_UPPER43 Register

1 GIC500_GICD_IROUTER_UPPER43 Register (Offset = 615Ch) [reset = 0h]

GICD_IROUTER43_upper

Return to Summary Table

Table 14-17647. Instance Table

Instance Name	Physical Address
GICSS0	**0180 615Ch**

Figure 14-5853. GIC500_GICD_IROUTER_UPPER43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17649. GIC500_GICD_IROUTER_UPPER43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.261 GIC500_GICD_IROUTER_LOWER44 Register

1 GIC500_GICD_IROUTER_LOWER44 Register (Offset = 6160h) [reset = 0h]

GICD_IROUTER44_lower

Return to Summary Table

Table 14-17650. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6160h**

Figure 14-5854. GIC500_GICD_IROUTER_LOWER44 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER44_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER44_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER44_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17652. GIC500_GICD_IROUTER_LOWER44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER44_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER44_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER44_LOWER__0_8	R/W	0h	A0

14.4.1.2.262 GIC500_GICD_IROUTER_UPPER44 Register

1 GIC500_GICD_IROUTER_UPPER44 Register (Offset = 6164h) [reset = 0h]

GICD_IROUTER44_upper

Return to Summary Table

Table 14-17653. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6164h**

Figure 14-5855. GIC500_GICD_IROUTER_UPPER44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17655. GIC500_GICD_IROUTER_UPPER44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.263 GIC500_GICD_IROUTER_LOWER45 Register

1 GIC500_GICD_IROUTER_LOWER45 Register (Offset = 6168h) [reset = 0h]

GICD_IROUTER45_lower

Return to Summary Table

Table 14-17656. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6168h**

Figure 14-5856. GIC500_GICD_IROUTER_LOWER45 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER45_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER45_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER45_LOWER__0_8							
R/W							
0h							

Table 14-17658. GIC500_GICD_IROUTER_LOWER45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER45_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER45_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER45_LOWER__0_8	R/W	0h	A0

14.4.1.2.264 GIC500_GICD_IROUTER_UPPER45 Register

1 GIC500_GICD_IROUTER_UPPER45 Register (Offset = 616Ch) [reset = 0h]

GICD_IROUTER45_upper

Return to Summary Table

Table 14-17659. Instance Table

Instance Name	Physical Address
GICSS0	**0180 616Ch**

Figure 14-5857. GIC500_GICD_IROUTER_UPPER45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17661. GIC500_GICD_IROUTER_UPPER45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.265 GIC500_GICD_IROUTER_LOWER46 Register

1 GIC500_GICD_IROUTER_LOWER46 Register (Offset = 6170h) [reset = 0h]

GICD_IROUTER46_lower

Return to Summary Table

Table 14-17662. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6170h**

Figure 14-5858. GIC500_GICD_IROUTER_LOWER46 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER46_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER46_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER46_LOWER__0_8							
R/W							
0h							

Table 14-17664. GIC500_GICD_IROUTER_LOWER46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER46_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER46_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER46_LOWER__0_8	R/W	0h	A0

14.4.1.2.266 GIC500_GICD_IROUTER_UPPER46 Register

1 GIC500_GICD_IROUTER_UPPER46 Register (Offset = 6174h) [reset = 0h]

GICD_IROUTER46_upper

Return to Summary Table

Table 14-17665. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6174h**

Figure 14-5859. GIC500_GICD_IROUTER_UPPER46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17667. GIC500_GICD_IROUTER_UPPER46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.267 GIC500_GICD_IROUTER_LOWER47 Register

1 GIC500_GICD_IROUTER_LOWER47 Register (Offset = 6178h) [reset = 0h]

GICD_IROUTER47_lower

Return to Summary Table

Table 14-17668. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6178h**

Figure 14-5860. GIC500_GICD_IROUTER_LOWER47 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER47_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER47_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER47_LOWER__0_8							
R/W							
0h							

Table 14-17670. GIC500_GICD_IROUTER_LOWER47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER47_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER47_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER47_LOWER__0_8	R/W	0h	A0

14.4.1.2.268 GIC500_GICD_IROUTER_UPPER47 Register

1 GIC500_GICD_IROUTER_UPPER47 Register (Offset = 617Ch) [reset = 0h]

GICD_IROUTER47_upper

Return to Summary Table

Table 14-17671. Instance Table

Instance Name	Physical Address
GICSS0	**0180 617Ch**

Figure 14-5861. GIC500_GICD_IROUTER_UPPER47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17673. GIC500_GICD_IROUTER_UPPER47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.269 GIC500_GICD_IROUTER_LOWER48 Register

1 GIC500_GICD_IROUTER_LOWER48 Register (Offset = 6180h) [reset = 0h]

GICD_IROUTER48_lower

Return to Summary Table

Table 14-17674. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6180h**

Figure 14-5862. GIC500_GICD_IROUTER_LOWER48 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER48_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER48_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER48_LOWER__0_8							
R/W							
0h							

Table 14-17676. GIC500_GICD_IROUTER_LOWER48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER48_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER48_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER48_LOWER__0_8	R/W	0h	A0

14.4.1.2.270 GIC500_GICD_IROUTER_UPPER48 Register

1 GIC500_GICD_IROUTER_UPPER48 Register (Offset = 6184h) [reset = 0h]

GICD_IROUTER48_upper

Return to Summary Table

Table 14-17677. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6184h**

Figure 14-5863. GIC500_GICD_IROUTER_UPPER48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17679. GIC500_GICD_IROUTER_UPPER48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.271 GIC500_GICD_IROUTER_LOWER49 Register

1 GIC500_GICD_IROUTER_LOWER49 Register (Offset = 6188h) [reset = 0h]

GICD_IROUTER49_lower

Return to Summary Table

Table 14-17680. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6188h**

Figure 14-5864. GIC500_GICD_IROUTER_LOWER49 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER49_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER49_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER49_LOWER__0_8							
R/W							
0h							

Table 14-17682. GIC500_GICD_IROUTER_LOWER49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER49_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER49_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER49_LOWER__0_8	R/W	0h	A0

14.4.1.2.272 GIC500_GICD_IROUTER_UPPER49 Register

1 GIC500_GICD_IROUTER_UPPER49 Register (Offset = 618Ch) [reset = 0h]

GICD_IROUTER49_upper

Return to Summary Table

Table 14-17683. Instance Table

Instance Name	Physical Address
GICSS0	0180 618Ch

Figure 14-5865. GIC500_GICD_IROUTER_UPPER49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17685. GIC500_GICD_IROUTER_UPPER49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.273 GIC500_GICD_IROUTER_LOWER50 Register

1 GIC500_GICD_IROUTER_LOWER50 Register (Offset = 6190h) [reset = 0h]

GICD_IROUTER50_lower

Return to Summary Table

Table 14-17686. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6190h**

Figure 14-5866. GIC500_GICD_IROUTER_LOWER50 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER50_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER50_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER50_LOWER__0_8							
R/W							
0h							

Table 14-17688. GIC500_GICD_IROUTER_LOWER50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER50_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER50_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER50_LOWER__0_8	R/W	0h	A0

14.4.1.2.274 GIC500_GICD_IROUTER_UPPER50 Register

1 GIC500_GICD_IROUTER_UPPER50 Register (Offset = 6194h) [reset = 0h]

GICD_IROUTER50_upper

Return to Summary Table

Table 14-17689. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6194h**

Figure 14-5867. GIC500_GICD_IROUTER_UPPER50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17691. GIC500_GICD_IROUTER_UPPER50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.275 GIC500_GICD_IROUTER_LOWER51 Register

1 GIC500_GICD_IROUTER_LOWER51 Register (Offset = 6198h) [reset = 0h]

GICD_IROUTER51_lower

Return to Summary Table

Table 14-17692. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6198h**

Figure 14-5868. GIC500_GICD_IROUTER_LOWER51 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER51_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER51_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER51_LOWER__0_8							
R/W							
0h							

Table 14-17694. GIC500_GICD_IROUTER_LOWER51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER51_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER51_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER51_LOWER__0_8	R/W	0h	A0

14.4.1.2.276 GIC500_GICD_IROUTER_UPPER51 Register

1 GIC500_GICD_IROUTER_UPPER51 Register (Offset = 619Ch) [reset = 0h]

GICD_IROUTER51_upper

Return to Summary Table

Table 14-17695. Instance Table

Instance Name	Physical Address
GICSS0	**0180 619Ch**

Figure 14-5869. GIC500_GICD_IROUTER_UPPER51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17697. GIC500_GICD_IROUTER_UPPER51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.277 GIC500_GICD_IROUTER_LOWER52 Register

1 GIC500_GICD_IROUTER_LOWER52 Register (Offset = 61A0h) [reset = 0h]

GICD_IROUTER52_lower

Return to Summary Table

Table 14-17698. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61A0h**

Figure 14-5870. GIC500_GICD_IROUTER_LOWER52 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER52_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER52_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER52_LOWER__0_8							
R/W							
0h							

Table 14-17700. GIC500_GICD_IROUTER_LOWER52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER52_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER52_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER52_LOWER__0_8	R/W	0h	A0

14.4.1.2.278 GIC500_GICD_IROUTER_UPPER52 Register

1 GIC500_GICD_IROUTER_UPPER52 Register (Offset = 61A4h) [reset = 0h]

GICD_IROUTER52_upper

Return to Summary Table

Table 14-17701. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61A4h**

Figure 14-5871. GIC500_GICD_IROUTER_UPPER52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17703. GIC500_GICD_IROUTER_UPPER52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.279 GIC500_GICD_IROUTER_LOWER53 Register

1 GIC500_GICD_IROUTER_LOWER53 Register (Offset = 61A8h) [reset = 0h]

GICD_IROUTER53_lower

Return to Summary Table

Table 14-17704. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61A8h**

Figure 14-5872. GIC500_GICD_IROUTER_LOWER53 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER53_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER53_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER53_LOWER__0_8							
R/W							
0h							

Table 14-17706. GIC500_GICD_IROUTER_LOWER53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER53_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER53_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER53_LOWER__0_8	R/W	0h	A0

14.4.1.2.280 GIC500_GICD_IROUTER_UPPER53 Register

1 GIC500_GICD_IROUTER_UPPER53 Register (Offset = 61ACh) [reset = 0h]

GICD_IROUTER53_upper

Return to Summary Table

Table 14-17707. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61ACh**

Figure 14-5873. GIC500_GICD_IROUTER_UPPER53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17709. GIC500_GICD_IROUTER_UPPER53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.281 GIC500_GICD_IROUTER_LOWER54 Register

1 GIC500_GICD_IROUTER_LOWER54 Register (Offset = 61B0h) [reset = 0h]

GICD_IROUTER54_lower

Return to Summary Table

Table 14-17710. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61B0h**

Figure 14-5874. GIC500_GICD_IROUTER_LOWER54 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER54_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER54_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER54_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17712. GIC500_GICD_IROUTER_LOWER54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER54_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER54_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER54_LOWER__0_8	R/W	0h	A0

14.4.1.2.282 GIC500_GICD_IROUTER_UPPER54 Register

1 GIC500_GICD_IROUTER_UPPER54 Register (Offset = 61B4h) [reset = 0h]

GICD_IROUTER54_upper

Return to Summary Table

Table 14-17713. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61B4h**

Figure 14-5875. GIC500_GICD_IROUTER_UPPER54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17715. GIC500_GICD_IROUTER_UPPER54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.283 GIC500_GICD_IROUTER_LOWER55 Register

1 GIC500_GICD_IROUTER_LOWER55 Register (Offset = 61B8h) [reset = 0h]

GICD_IROUTER55_lower

Return to Summary Table

Table 14-17716. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61B8h**

Figure 14-5876. GIC500_GICD_IROUTER_LOWER55 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER55_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER55_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER55_LOWER__0_8							
R/W							
0h							

Table 14-17718. GIC500_GICD_IROUTER_LOWER55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER55_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER55_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER55_LOWER__0_8	R/W	0h	A0

14.4.1.2.284 GIC500_GICD_IROUTER_UPPER55 Register

1 GIC500_GICD_IROUTER_UPPER55 Register (Offset = 61BCh) [reset = 0h]

GICD_IROUTER55_upper

Return to Summary Table

Table 14-17719. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61BCh**

Figure 14-5877. GIC500_GICD_IROUTER_UPPER55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17721. GIC500_GICD_IROUTER_UPPER55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.285 GIC500_GICD_IROUTER_LOWER56 Register

1 GIC500_GICD_IROUTER_LOWER56 Register (Offset = 61C0h) [reset = 0h]

GICD_IROUTER56_lower

Return to Summary Table

Table 14-17722. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61C0h**

Figure 14-5878. GIC500_GICD_IROUTER_LOWER56 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER56_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER56_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER56_LOWER__0_8							
R/W							
0h							

Table 14-17724. GIC500_GICD_IROUTER_LOWER56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER56_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER56_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER56_LOWER__0_8	R/W	0h	A0

14.4.1.2.286 GIC500_GICD_IROUTER_UPPER56 Register

1 GIC500_GICD_IROUTER_UPPER56 Register (Offset = 61C4h) [reset = 0h]

GICD_IROUTER56_upper

Return to Summary Table

Table 14-17725. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61C4h**

Figure 14-5879. GIC500_GICD_IROUTER_UPPER56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17727. GIC500_GICD_IROUTER_UPPER56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.287 GIC500_GICD_IROUTER_LOWER57 Register

1 GIC500_GICD_IROUTER_LOWER57 Register (Offset = 61C8h) [reset = 0h]

GICD_IROUTER57_lower

Return to Summary Table

Table 14-17728. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61C8h**

Figure 14-5880. GIC500_GICD_IROUTER_LOWER57 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER57_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER57_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER57_LOWER__0_8							
R/W							
0h							

Table 14-17730. GIC500_GICD_IROUTER_LOWER57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER57_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER57_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER57_LOWER__0_8	R/W	0h	A0

14.4.1.2.288 GIC500_GICD_IROUTER_UPPER57 Register

1 GIC500_GICD_IROUTER_UPPER57 Register (Offset = 61CCh) [reset = 0h]

GICD_IROUTER57_upper

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Table 14-17731. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61CCh**

Figure 14-5881. GIC500_GICD_IROUTER_UPPER57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17733. GIC500_GICD_IROUTER_UPPER57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.289 GIC500_GICD_IROUTER_LOWER58 Register

1 GIC500_GICD_IROUTER_LOWER58 Register (Offset = 61D0h) [reset = 0h]

GICD_IROUTER58_lower

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Table 14-17734. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61D0h**

Figure 14-5882. GIC500_GICD_IROUTER_LOWER58 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER58_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER58_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER58_LOWER__0_8							
R/W							
0h							

Table 14-17736. GIC500_GICD_IROUTER_LOWER58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER58_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER58_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER58_LOWER__0_8	R/W	0h	A0

14.4.1.2.290 GIC500_GICD_IROUTER_UPPER58 Register

1 GIC500_GICD_IROUTER_UPPER58 Register (Offset = 61D4h) [reset = 0h]

GICD_IROUTER58_upper

Return to Summary Table

Table 14-17737. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61D4h**

Figure 14-5883. GIC500_GICD_IROUTER_UPPER58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17739. GIC500_GICD_IROUTER_UPPER58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.291 GIC500_GICD_IROUTER_LOWER59 Register

1 GIC500_GICD_IROUTER_LOWER59 Register (Offset = 61D8h) [reset = 0h]

GICD_IROUTER59_lower

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Table 14-17740. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61D8h**

Figure 14-5884. GIC500_GICD_IROUTER_LOWER59 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER59_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER59_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER59_LOWER__0_8							
R/W							
0h							

Table 14-17742. GIC500_GICD_IROUTER_LOWER59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER59_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER59_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER59_LOWER__0_8	R/W	0h	A0

14.4.1.2.292 GIC500_GICD_IROUTER_UPPER59 Register

1 GIC500_GICD_IROUTER_UPPER59 Register (Offset = 61DCh) [reset = 0h]

GICD_IROUTER59_upper

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Table 14-17743. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61DCh**

Figure 14-5885. GIC500_GICD_IROUTER_UPPER59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17745. GIC500_GICD_IROUTER_UPPER59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.293 GIC500_GICD_IROUTER_LOWER60 Register

1 GIC500_GICD_IROUTER_LOWER60 Register (Offset = 61E0h) [reset = 0h]

GICD_IROUTER60_lower

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Table 14-17746. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61E0h**

Figure 14-5886. GIC500_GICD_IROUTER_LOWER60 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER60_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER60_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER60_LOWER__0_8							
R/W							
0h							

Table 14-17748. GIC500_GICD_IROUTER_LOWER60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER60_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER60_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER60_LOWER__0_8	R/W	0h	A0

14.4.1.2.294 GIC500_GICD_IROUTER_UPPER60 Register

1 GIC500_GICD_IROUTER_UPPER60 Register (Offset = 61E4h) [reset = 0h]

GICD_IROUTER60_upper

Return to Summary Table

Table 14-17749. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61E4h**

Figure 14-5887. GIC500_GICD_IROUTER_UPPER60 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17751. GIC500_GICD_IROUTER_UPPER60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.295 GIC500_GICD_IROUTER_LOWER61 Register

1 GIC500_GICD_IROUTER_LOWER61 Register (Offset = 61E8h) [reset = 0h]

GICD_IROUTER61_lower

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Table 14-17752. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61E8h**

Figure 14-5888. GIC500_GICD_IROUTER_LOWER61 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER61_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER61_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER61_LOWER__0_8							
R/W							
0h							

Table 14-17754. GIC500_GICD_IROUTER_LOWER61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER61_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER61_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER61_LOWER__0_8	R/W	0h	A0

14.4.1.2.296 GIC500_GICD_IROUTER_UPPER61 Register

1 GIC500_GICD_IROUTER_UPPER61 Register (Offset = 61ECh) [reset = 0h]

GICD_IROUTER61_upper

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Table 14-17755. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61ECh**

Figure 14-5889. GIC500_GICD_IROUTER_UPPER61 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17757. GIC500_GICD_IROUTER_UPPER61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.297 GIC500_GICD_IROUTER_LOWER62 Register

1 GIC500_GICD_IROUTER_LOWER62 Register (Offset = 61F0h) [reset = 0h]

GICD_IROUTER62_lower

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Table 14-17758. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61F0h**

Figure 14-5890. GIC500_GICD_IROUTER_LOWER62 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER62_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER62_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER62_LOWER__0_8							
R/W							
0h							

Table 14-17760. GIC500_GICD_IROUTER_LOWER62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER62_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER62_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER62_LOWER__0_8	R/W	0h	A0

14.4.1.2.298 GIC500_GICD_IROUTER_UPPER62 Register

1 GIC500_GICD_IROUTER_UPPER62 Register (Offset = 61F4h) [reset = 0h]

GICD_IROUTER62_upper

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Table 14-17761. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61F4h**

Figure 14-5891. GIC500_GICD_IROUTER_UPPER62 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17763. GIC500_GICD_IROUTER_UPPER62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.299 GIC500_GICD_IROUTER_LOWER63 Register

1 GIC500_GICD_IROUTER_LOWER63 Register (Offset = 61F8h) [reset = 0h]

GICD_IROUTER63_lower

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Table 14-17764. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61F8h**

Figure 14-5892. GIC500_GICD_IROUTER_LOWER63 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER63_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER63_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER63_LOWER__0_8							
R/W							
0h							

Table 14-17766. GIC500_GICD_IROUTER_LOWER63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER63_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER63_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER63_LOWER__0_8	R/W	0h	A0

14.4.1.2.300 GIC500_GICD_IROUTER_UPPER63 Register

1 GIC500_GICD_IROUTER_UPPER63 Register (Offset = 61FCh) [reset = 0h]

GICD_IROUTER63_upper

Return to Summary Table

Table 14-17767. Instance Table

Instance Name	Physical Address
GICSS0	**0180 61FCh**

Figure 14-5893. GIC500_GICD_IROUTER_UPPER63 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17769. GIC500_GICD_IROUTER_UPPER63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.301 GIC500_GICD_IROUTER_LOWER64 Register

1 GIC500_GICD_IROUTER_LOWER64 Register (Offset = 6200h) [reset = 0h]

GICD_IROUTER64_lower

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Table 14-17770. Instance Table

Instance Name	Physical Address
GICSS0	0180 6200h

Figure 14-5894. GIC500_GICD_IROUTER_LOWER64 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER64_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER64_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER64_LOWER__0_8							
R/W							
0h							

Table 14-17772. GIC500_GICD_IROUTER_LOWER64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER64_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER64_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER64_LOWER__0_8	R/W	0h	A0

14.4.1.2.302 GIC500_GICD_IROUTER_UPPER64 Register

1 GIC500_GICD_IROUTER_UPPER64 Register (Offset = 6204h) [reset = 0h]

GICD_IROUTER64_upper

Return to Summary Table

Table 14-17773. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6204h**

Figure 14-5895. GIC500_GICD_IROUTER_UPPER64 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17775. GIC500_GICD_IROUTER_UPPER64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.303 GIC500_GICD_IROUTER_LOWER65 Register

1 GIC500_GICD_IROUTER_LOWER65 Register (Offset = 6208h) [reset = 0h]

GICD_IROUTER65_lower

Return to Summary Table

Table 14-17776. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6208h**

Figure 14-5896. GIC500_GICD_IROUTER_LOWER65 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER65_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER65_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER65_LOWER__0_8							
R/W							
0h							

Table 14-17778. GIC500_GICD_IROUTER_LOWER65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER65_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER65_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER65_LOWER__0_8	R/W	0h	A0

14.4.1.2.304 GIC500_GICD_IROUTER_UPPER65 Register

1 GIC500_GICD_IROUTER_UPPER65 Register (Offset = 620Ch) [reset = 0h]

GICD_IROUTER65_upper

Return to Summary Table

Table 14-17779. Instance Table

Instance Name	Physical Address
GICSS0	**0180 620Ch**

Figure 14-5897. GIC500_GICD_IROUTER_UPPER65 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17781. GIC500_GICD_IROUTER_UPPER65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.305 GIC500_GICD_IROUTER_LOWER66 Register

1 GIC500_GICD_IROUTER_LOWER66 Register (Offset = 6210h) [reset = 0h]

GICD_IROUTER66_lower

Return to Summary Table

Table 14-17782. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6210h**

Figure 14-5898. GIC500_GICD_IROUTER_LOWER66 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER66_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER66_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER66_LOWER__0_8							
R/W							
0h							

Table 14-17784. GIC500_GICD_IROUTER_LOWER66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER66_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER66_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER66_LOWER__0_8	R/W	0h	A0

14.4.1.2.306 GIC500_GICD_IROUTER_UPPER66 Register

1 GIC500_GICD_IROUTER_UPPER66 Register (Offset = 6214h) [reset = 0h]

GICD_IROUTER66_upper

Return to Summary Table

Table 14-17785. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6214h**

Figure 14-5899. GIC500_GICD_IROUTER_UPPER66 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17787. GIC500_GICD_IROUTER_UPPER66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.307 GIC500_GICD_IROUTER_LOWER67 Register

1 GIC500_GICD_IROUTER_LOWER67 Register (Offset = 6218h) [reset = 0h]

GICD_IROUTER67_lower

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Table 14-17788. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6218h**

Figure 14-5900. GIC500_GICD_IROUTER_LOWER67 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER67_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER67_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER67_LOWER__0_8							
R/W							
0h							

Table 14-17790. GIC500_GICD_IROUTER_LOWER67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER67_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER67_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER67_LOWER__0_8	R/W	0h	A0

14.4.1.2.308 GIC500_GICD_IROUTER_UPPER67 Register

1 GIC500_GICD_IROUTER_UPPER67 Register (Offset = 621Ch) [reset = 0h]

GICD_IROUTER67_upper

Return to Summary Table

Table 14-17791. Instance Table

Instance Name	Physical Address
GICSS0	**0180 621Ch**

Figure 14-5901. GIC500_GICD_IROUTER_UPPER67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17793. GIC500_GICD_IROUTER_UPPER67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.309 GIC500_GICD_IROUTER_LOWER68 Register

1 GIC500_GICD_IROUTER_LOWER68 Register (Offset = 6220h) [reset = 0h]

GICD_IROUTER68_lower

Return to Summary Table

Table 14-17794. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6220h**

Figure 14-5902. GIC500_GICD_IROUTER_LOWER68 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER68_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER68_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER68_LOWER__0_8							
R/W							
0h							

Table 14-17796. GIC500_GICD_IROUTER_LOWER68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER68_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER68_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER68_LOWER__0_8	R/W	0h	A0

14.4.1.2.310 GIC500_GICD_IROUTER_UPPER68 Register

1 GIC500_GICD_IROUTER_UPPER68 Register (Offset = 6224h) [reset = 0h]

GICD_IROUTER68_upper

Return to Summary Table

Table 14-17797. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6224h**

Figure 14-5903. GIC500_GICD_IROUTER_UPPER68 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17799. GIC500_GICD_IROUTER_UPPER68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.311 GIC500_GICD_IROUTER_LOWER69 Register

1 GIC500_GICD_IROUTER_LOWER69 Register (Offset = 6228h) [reset = 0h]

GICD_IROUTER69_lower

Return to Summary Table

Table 14-17800. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6228h**

Figure 14-5904. GIC500_GICD_IROUTER_LOWER69 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER69_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER69_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER69_LOWER__0_8							
R/W							
0h							

Table 14-17802. GIC500_GICD_IROUTER_LOWER69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER69_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER69_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER69_LOWER__0_8	R/W	0h	A0

14.4.1.2.312 GIC500_GICD_IROUTER_UPPER69 Register

1 GIC500_GICD_IROUTER_UPPER69 Register (Offset = 622Ch) [reset = 0h]

GICD_IROUTER69_upper

Return to Summary Table

Table 14-17803. Instance Table

Instance Name	Physical Address
GICSS0	0180 622Ch

Figure 14-5905. GIC500_GICD_IROUTER_UPPER69 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17805. GIC500_GICD_IROUTER_UPPER69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.313 GIC500_GICD_IROUTER_LOWER70 Register

1 GIC500_GICD_IROUTER_LOWER70 Register (Offset = 6230h) [reset = 0h]

GICD_IROUTER70_lower

Return to Summary Table

Table 14-17806. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6230h**

Figure 14-5906. GIC500_GICD_IROUTER_LOWER70 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER70_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER70_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER70_LOWER__0_8							
R/W							
0h							

Table 14-17808. GIC500_GICD_IROUTER_LOWER70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER70_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER70_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER70_LOWER__0_8	R/W	0h	A0

14.4.1.2.314 GIC500_GICD_IROUTER_UPPER70 Register

1 GIC500_GICD_IROUTER_UPPER70 Register (Offset = 6234h) [reset = 0h]

GICD_IROUTER70_upper

Return to Summary Table

Table 14-17809. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6234h**

Figure 14-5907. GIC500_GICD_IROUTER_UPPER70 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17811. GIC500_GICD_IROUTER_UPPER70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.315 GIC500_GICD_IROUTER_LOWER71 Register

1 GIC500_GICD_IROUTER_LOWER71 Register (Offset = 6238h) [reset = 0h]

GICD_IROUTER71_lower

Return to Summary Table

Table 14-17812. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6238h**

Figure 14-5908. GIC500_GICD_IROUTER_LOWER71 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER71_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER71_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER71_LOWER__0_8							
R/W							
0h							

Table 14-17814. GIC500_GICD_IROUTER_LOWER71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER71_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER71_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER71_LOWER__0_8	R/W	0h	A0

14.4.1.2.316 GIC500_GICD_IROUTER_UPPER71 Register

1 GIC500_GICD_IROUTER_UPPER71 Register (Offset = 623Ch) [reset = 0h]

GICD_IROUTER71_upper

Return to Summary Table

Table 14-17815. Instance Table

Instance Name	Physical Address
GICSS0	**0180 623Ch**

Figure 14-5909. GIC500_GICD_IROUTER_UPPER71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17817. GIC500_GICD_IROUTER_UPPER71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.317 GIC500_GICD_IROUTER_LOWER72 Register

1 GIC500_GICD_IROUTER_LOWER72 Register (Offset = 6240h) [reset = 0h]

GICD_IROUTER72_lower

Return to Summary Table

Table 14-17818. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6240h**

Figure 14-5910. GIC500_GICD_IROUTER_LOWER72 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER72_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER72_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER72_LOWER__0_8							
R/W							
0h							

Table 14-17820. GIC500_GICD_IROUTER_LOWER72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER72_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER72_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER72_LOWER__0_8	R/W	0h	A0

14.4.1.2.318 GIC500_GICD_IROUTER_UPPER72 Register

1 GIC500_GICD_IROUTER_UPPER72 Register (Offset = 6244h) [reset = 0h]

GICD_IROUTER72_upper

Return to Summary Table

Table 14-17821. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6244h**

Figure 14-5911. GIC500_GICD_IROUTER_UPPER72 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17823. GIC500_GICD_IROUTER_UPPER72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.319 GIC500_GICD_IROUTER_LOWER73 Register

1 GIC500_GICD_IROUTER_LOWER73 Register (Offset = 6248h) [reset = 0h]

GICD_IROUTER73_lower

Return to Summary Table

Table 14-17824. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6248h**

Figure 14-5912. GIC500_GICD_IROUTER_LOWER73 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER73_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER73_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER73_LOWER__0_8							
R/W							
0h							

Table 14-17826. GIC500_GICD_IROUTER_LOWER73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER73_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER73_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER73_LOWER__0_8	R/W	0h	A0

14.4.1.2.320 GIC500_GICD_IROUTER_UPPER73 Register

1 GIC500_GICD_IROUTER_UPPER73 Register (Offset = 624Ch) [reset = 0h]

GICD_IROUTER73_upper

Return to Summary Table

Table 14-17827. Instance Table

Instance Name	Physical Address
GICSS0	**0180 624Ch**

Figure 14-5913. GIC500_GICD_IROUTER_UPPER73 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17829. GIC500_GICD_IROUTER_UPPER73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.321 GIC500_GICD_IROUTER_LOWER74 Register

1 GIC500_GICD_IROUTER_LOWER74 Register (Offset = 6250h) [reset = 0h]

GICD_IROUTER74_lower

Return to Summary Table

Table 14-17830. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6250h**

Figure 14-5914. GIC500_GICD_IROUTER_LOWER74 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER74_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER74_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER74_LOWER__0_8							
R/W							
0h							

Table 14-17832. GIC500_GICD_IROUTER_LOWER74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER74_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER74_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER74_LOWER__0_8	R/W	0h	A0

14.4.1.2.322 GIC500_GICD_IROUTER_UPPER74 Register

1 GIC500_GICD_IROUTER_UPPER74 Register (Offset = 6254h) [reset = 0h]

GICD_IROUTER74_upper

Return to Summary Table

Table 14-17833. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6254h**

Figure 14-5915. GIC500_GICD_IROUTER_UPPER74 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17835. GIC500_GICD_IROUTER_UPPER74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.323 GIC500_GICD_IROUTER_LOWER75 Register

1 GIC500_GICD_IROUTER_LOWER75 Register (Offset = 6258h) [reset = 0h]

GICD_IROUTER75_lower

Return to Summary Table

Table 14-17836. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6258h**

Figure 14-5916. GIC500_GICD_IROUTER_LOWER75 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER75_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER75_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER75_LOWER__0_8							
R/W							
0h							

Table 14-17838. GIC500_GICD_IROUTER_LOWER75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER75_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER75_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER75_LOWER__0_8	R/W	0h	A0

14.4.1.2.324 GIC500_GICD_IROUTER_UPPER75 Register

1 GIC500_GICD_IROUTER_UPPER75 Register (Offset = 625Ch) [reset = 0h]

GICD_IROUTER75_upper

Return to Summary Table

Table 14-17839. Instance Table

Instance Name	Physical Address
GICSS0	**0180 625Ch**

Figure 14-5917. GIC500_GICD_IROUTER_UPPER75 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17841. GIC500_GICD_IROUTER_UPPER75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.325 GIC500_GICD_IROUTER_LOWER76 Register

1 GIC500_GICD_IROUTER_LOWER76 Register (Offset = 6260h) [reset = 0h]

GICD_IROUTER76_lower

Return to Summary Table

Table 14-17842. Instance Table

Instance Name	Physical Address
GICSS0	0180 6260h

Figure 14-5918. GIC500_GICD_IROUTER_LOWER76 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER76_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER76_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER76_LOWER__0_8							
R/W							
0h							

Table 14-17844. GIC500_GICD_IROUTER_LOWER76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER76_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER76_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER76_LOWER__0_8	R/W	0h	A0

14.4.1.2.326 GIC500_GICD_IROUTER_UPPER76 Register

1 GIC500_GICD_IROUTER_UPPER76 Register (Offset = 6264h) [reset = 0h]

GICD_IROUTER76_upper

Return to Summary Table

Table 14-17845. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6264h**

Figure 14-5919. GIC500_GICD_IROUTER_UPPER76 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17847. GIC500_GICD_IROUTER_UPPER76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.327 GIC500_GICD_IROUTER_LOWER77 Register

1 GIC500_GICD_IROUTER_LOWER77 Register (Offset = 6268h) [reset = 0h]

GICD_IROUTER77_lower

Return to Summary Table

Table 14-17848. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6268h**

Figure 14-5920. GIC500_GICD_IROUTER_LOWER77 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER77_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER77_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER77_LOWER__0_8							
R/W							
0h							

Table 14-17850. GIC500_GICD_IROUTER_LOWER77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER77_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER77_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER77_LOWER__0_8	R/W	0h	A0

14.4.1.2.328 GIC500_GICD_IROUTER_UPPER77 Register

1 GIC500_GICD_IROUTER_UPPER77 Register (Offset = 626Ch) [reset = 0h]

GICD_IROUTER77_upper

Return to Summary Table

Table 14-17851. Instance Table

Instance Name	Physical Address
GICSS0	**0180 626Ch**

Figure 14-5921. GIC500_GICD_IROUTER_UPPER77 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17853. GIC500_GICD_IROUTER_UPPER77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.329 GIC500_GICD_IROUTER_LOWER78 Register

1 GIC500_GICD_IROUTER_LOWER78 Register (Offset = 6270h) [reset = 0h]

GICD_IROUTER78_lower

Return to Summary Table

Table 14-17854. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6270h**

Figure 14-5922. GIC500_GICD_IROUTER_LOWER78 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER78_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER78_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER78_LOWER__0_8							
R/W							
0h							

Table 14-17856. GIC500_GICD_IROUTER_LOWER78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER78_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER78_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER78_LOWER__0_8	R/W	0h	A0

14.4.1.2.330 GIC500_GICD_IROUTER_UPPER78 Register

1 GIC500_GICD_IROUTER_UPPER78 Register (Offset = 6274h) [reset = 0h]

GICD_IROUTER78_upper

Return to Summary Table

Table 14-17857. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6274h**

Figure 14-5923. GIC500_GICD_IROUTER_UPPER78 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17859. GIC500_GICD_IROUTER_UPPER78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.331 GIC500_GICD_IROUTER_LOWER79 Register

1 GIC500_GICD_IROUTER_LOWER79 Register (Offset = 6278h) [reset = 0h]

GICD_IROUTER79_lower

Return to Summary Table

Table 14-17860. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6278h**

Figure 14-5924. GIC500_GICD_IROUTER_LOWER79 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER79_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER79_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER79_LOWER__0_8							
R/W							
0h							

Table 14-17862. GIC500_GICD_IROUTER_LOWER79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER79_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER79_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER79_LOWER__0_8	R/W	0h	A0

14.4.1.2.332 GIC500_GICD_IROUTER_UPPER79 Register

1 GIC500_GICD_IROUTER_UPPER79 Register (Offset = 627Ch) [reset = 0h]

GICD_IROUTER79_upper

Return to Summary Table

Table 14-17863. Instance Table

Instance Name	Physical Address
GICSS0	**0180 627Ch**

Figure 14-5925. GIC500_GICD_IROUTER_UPPER79 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17865. GIC500_GICD_IROUTER_UPPER79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.333 GIC500_GICD_IROUTER_LOWER80 Register

1 GIC500_GICD_IROUTER_LOWER80 Register (Offset = 6280h) [reset = 0h]

GICD_IROUTER80_lower

Return to Summary Table

Table 14-17866. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6280h**

Figure 14-5926. GIC500_GICD_IROUTER_LOWER80 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER80_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER80_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER80_LOWER__0_8							
R/W							
0h							

Table 14-17868. GIC500_GICD_IROUTER_LOWER80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER80_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER80_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER80_LOWER__0_8	R/W	0h	A0

14.4.1.2.334 GIC500_GICD_IROUTER_UPPER80 Register

1 GIC500_GICD_IROUTER_UPPER80 Register (Offset = 6284h) [reset = 0h]

GICD_IROUTER80_upper

Return to Summary Table

Table 14-17869. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6284h**

Figure 14-5927. GIC500_GICD_IROUTER_UPPER80 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17871. GIC500_GICD_IROUTER_UPPER80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.335 GIC500_GICD_IROUTER_LOWER81 Register

1 GIC500_GICD_IROUTER_LOWER81 Register (Offset = 6288h) [reset = 0h]

GICD_IROUTER81_lower

Return to Summary Table

Table 14-17872. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6288h**

Figure 14-5928. GIC500_GICD_IROUTER_LOWER81 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER81_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER81_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER81_LOWER__0_8							
R/W							
0h							

Table 14-17874. GIC500_GICD_IROUTER_LOWER81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER81_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER81_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER81_LOWER__0_8	R/W	0h	A0

14.4.1.2.336 GIC500_GICD_IROUTER_UPPER81 Register

1 GIC500_GICD_IROUTER_UPPER81 Register (Offset = 628Ch) [reset = 0h]

GICD_IROUTER81_upper

Return to Summary Table

Table 14-17875. Instance Table

Instance Name	Physical Address
GICSS0	**0180 628Ch**

Figure 14-5929. GIC500_GICD_IROUTER_UPPER81 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17877. GIC500_GICD_IROUTER_UPPER81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.337 GIC500_GICD_IROUTER_LOWER82 Register

1 GIC500_GICD_IROUTER_LOWER82 Register (Offset = 6290h) [reset = 0h]

GICD_IROUTER82_lower

Return to Summary Table

Table 14-17878. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6290h**

Figure 14-5930. GIC500_GICD_IROUTER_LOWER82 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER82_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER82_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER82_LOWER__0_8							
R/W							
0h							

Table 14-17880. GIC500_GICD_IROUTER_LOWER82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER82_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER82_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER82_LOWER__0_8	R/W	0h	A0

14.4.1.2.338 GIC500_GICD_IROUTER_UPPER82 Register

1 GIC500_GICD_IROUTER_UPPER82 Register (Offset = 6294h) [reset = 0h]

GICD_IROUTER82_upper

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Table 14-17881. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6294h**

Figure 14-5931. GIC500_GICD_IROUTER_UPPER82 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17883. GIC500_GICD_IROUTER_UPPER82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.339 GIC500_GICD_IROUTER_LOWER83 Register

1 GIC500_GICD_IROUTER_LOWER83 Register (Offset = 6298h) [reset = 0h]

GICD_IROUTER83_lower

Return to Summary Table

Table 14-17884. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6298h**

Figure 14-5932. GIC500_GICD_IROUTER_LOWER83 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER83_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER83_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER83_LOWER__0_8							
R/W							
0h							

Table 14-17886. GIC500_GICD_IROUTER_LOWER83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER83_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER83_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER83_LOWER__0_8	R/W	0h	A0

14.4.1.2.340 GIC500_GICD_IROUTER_UPPER83 Register

1 GIC500_GICD_IROUTER_UPPER83 Register (Offset = 629Ch) [reset = 0h]

GICD_IROUTER83_upper

Return to Summary Table

Table 14-17887. Instance Table

Instance Name	Physical Address
GICSS0	**0180 629Ch**

Figure 14-5933. GIC500_GICD_IROUTER_UPPER83 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17889. GIC500_GICD_IROUTER_UPPER83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.341 GIC500_GICD_IROUTER_LOWER84 Register

1 GIC500_GICD_IROUTER_LOWER84 Register (Offset = 62A0h) [reset = 0h]

GICD_IROUTER84_lower

Return to Summary Table

Table 14-17890. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62A0h**

Figure 14-5934. GIC500_GICD_IROUTER_LOWER84 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER84_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER84_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER84_LOWER__0_8							
R/W							
0h							

Table 14-17892. GIC500_GICD_IROUTER_LOWER84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER84_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER84_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER84_LOWER__0_8	R/W	0h	A0

14.4.1.2.342 GIC500_GICD_IROUTER_UPPER84 Register

1 GIC500_GICD_IROUTER_UPPER84 Register (Offset = 62A4h) [reset = 0h]

GICD_IROUTER84_upper

Return to Summary Table

Table 14-17893. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62A4h**

Figure 14-5935. GIC500_GICD_IROUTER_UPPER84 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17895. GIC500_GICD_IROUTER_UPPER84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.343 GIC500_GICD_IROUTER_LOWER85 Register

1 GIC500_GICD_IROUTER_LOWER85 Register (Offset = 62A8h) [reset = 0h]

GICD_IROUTER85_lower

Return to Summary Table

Table 14-17896. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62A8h**

Figure 14-5936. GIC500_GICD_IROUTER_LOWER85 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER85_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER85_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER85_LOWER__0_8							
R/W							
0h							

Table 14-17898. GIC500_GICD_IROUTER_LOWER85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER85_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER85_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER85_LOWER__0_8	R/W	0h	A0

14.4.1.2.344 GIC500_GICD_IROUTER_UPPER85 Register

1 GIC500_GICD_IROUTER_UPPER85 Register (Offset = 62ACh) [reset = 0h]

GICD_IROUTER85_upper

Return to Summary Table

Table 14-17899. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62ACh**

Figure 14-5937. GIC500_GICD_IROUTER_UPPER85 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17901. GIC500_GICD_IROUTER_UPPER85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.345 GIC500_GICD_IROUTER_LOWER86 Register

1 GIC500_GICD_IROUTER_LOWER86 Register (Offset = 62B0h) [reset = 0h]

GICD_IROUTER86_lower

Return to Summary Table

Table 14-17902. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62B0h**

Figure 14-5938. GIC500_GICD_IROUTER_LOWER86 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER86_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER86_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER86_LOWER__0_8							
R/W							
0h							

Table 14-17904. GIC500_GICD_IROUTER_LOWER86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER86_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER86_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER86_LOWER__0_8	R/W	0h	A0

14.4.1.2.346 GIC500_GICD_IROUTER_UPPER86 Register

1 GIC500_GICD_IROUTER_UPPER86 Register (Offset = 62B4h) [reset = 0h]

GICD_IROUTER86_upper

Return to Summary Table

Table 14-17905. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62B4h**

Figure 14-5939. GIC500_GICD_IROUTER_UPPER86 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17907. GIC500_GICD_IROUTER_UPPER86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.347 GIC500_GICD_IROUTER_LOWER87 Register

1 GIC500_GICD_IROUTER_LOWER87 Register (Offset = 62B8h) [reset = 0h]

GICD_IROUTER87_lower

Return to Summary Table

Table 14-17908. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62B8h**

Figure 14-5940. GIC500_GICD_IROUTER_LOWER87 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER87_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER87_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER87_LOWER__0_8							
R/W							
0h							

Table 14-17910. GIC500_GICD_IROUTER_LOWER87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER87_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER87_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER87_LOWER__0_8	R/W	0h	A0

14.4.1.2.348 GIC500_GICD_IROUTER_UPPER87 Register

1 GIC500_GICD_IROUTER_UPPER87 Register (Offset = 62BCh) [reset = 0h]

GICD_IROUTER87_upper

Return to Summary Table

Table 14-17911. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62BCh**

Figure 14-5941. GIC500_GICD_IROUTER_UPPER87 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17913. GIC500_GICD_IROUTER_UPPER87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.349 GIC500_GICD_IROUTER_LOWER88 Register

1 GIC500_GICD_IROUTER_LOWER88 Register (Offset = 62C0h) [reset = 0h]

GICD_IROUTER88_lower

Return to Summary Table

Table 14-17914. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62C0h**

Figure 14-5942. GIC500_GICD_IROUTER_LOWER88 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER88_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER88_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER88_LOWER__0_8							
R/W							
0h							

Table 14-17916. GIC500_GICD_IROUTER_LOWER88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER88_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER88_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER88_LOWER__0_8	R/W	0h	A0

14.4.1.2.350 GIC500_GICD_IROUTER_UPPER88 Register

1 GIC500_GICD_IROUTER_UPPER88 Register (Offset = 62C4h) [reset = 0h]

GICD_IROUTER88_upper

Return to Summary Table

Table 14-17917. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62C4h**

Figure 14-5943. GIC500_GICD_IROUTER_UPPER88 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17919. GIC500_GICD_IROUTER_UPPER88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.351 GIC500_GICD_IROUTER_LOWER89 Register

1 GIC500_GICD_IROUTER_LOWER89 Register (Offset = 62C8h) [reset = 0h]

GICD_IROUTER89_lower

Return to Summary Table

Table 14-17920. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62C8h**

Figure 14-5944. GIC500_GICD_IROUTER_LOWER89 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER89_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER89_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER89_LOWER__0_8							
R/W							
0h							

Table 14-17922. GIC500_GICD_IROUTER_LOWER89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER89_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER89_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER89_LOWER__0_8	R/W	0h	A0

14.4.1.2.352 GIC500_GICD_IROUTER_UPPER89 Register

1 GIC500_GICD_IROUTER_UPPER89 Register (Offset = 62CCh) [reset = 0h]

GICD_IROUTER89_upper

Return to Summary Table

Table 14-17923. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62CCh**

Figure 14-5945. GIC500_GICD_IROUTER_UPPER89 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17925. GIC500_GICD_IROUTER_UPPER89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.353 GIC500_GICD_IROUTER_LOWER90 Register

1 GIC500_GICD_IROUTER_LOWER90 Register (Offset = 62D0h) [reset = 0h]

GICD_IROUTER90_lower

Return to Summary Table

Table 14-17926. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62D0h**

Figure 14-5946. GIC500_GICD_IROUTER_LOWER90 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER90_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER90_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER90_LOWER__0_8							
R/W							
0h							

Table 14-17928. GIC500_GICD_IROUTER_LOWER90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER90_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER90_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER90_LOWER__0_8	R/W	0h	A0

14.4.1.2.354 GIC500_GICD_IROUTER_UPPER90 Register

1 GIC500_GICD_IROUTER_UPPER90 Register (Offset = 62D4h) [reset = 0h]

GICD_IROUTER90_upper

Return to Summary Table

Table 14-17929. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62D4h**

Figure 14-5947. GIC500_GICD_IROUTER_UPPER90 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17931. GIC500_GICD_IROUTER_UPPER90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.355 GIC500_GICD_IROUTER_LOWER91 Register

1 GIC500_GICD_IROUTER_LOWER91 Register (Offset = 62D8h) [reset = 0h]

GICD_IROUTER91_lower

Return to Summary Table

Table 14-17932. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62D8h**

Figure 14-5948. GIC500_GICD_IROUTER_LOWER91 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER91_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER91_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER91_LOWER__0_8							
R/W							
0h							

Table 14-17934. GIC500_GICD_IROUTER_LOWER91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER91_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER91_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER91_LOWER__0_8	R/W	0h	A0

14.4.1.2.356 GIC500_GICD_IROUTER_UPPER91 Register

1 GIC500_GICD_IROUTER_UPPER91 Register (Offset = 62DCh) [reset = 0h]

GICD_IROUTER91_upper

Return to Summary Table

Table 14-17935. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62DCh**

Figure 14-5949. GIC500_GICD_IROUTER_UPPER91 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17937. GIC500_GICD_IROUTER_UPPER91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.357 GIC500_GICD_IROUTER_LOWER92 Register

1 GIC500_GICD_IROUTER_LOWER92 Register (Offset = 62E0h) [reset = 0h]

GICD_IROUTER92_lower

Return to Summary Table

Table 14-17938. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62E0h**

Figure 14-5950. GIC500_GICD_IROUTER_LOWER92 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER92_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER92_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER92_LOWER__0_8							
R/W							
0h							

Table 14-17940. GIC500_GICD_IROUTER_LOWER92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER92_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER92_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER92_LOWER__0_8	R/W	0h	A0

14.4.1.2.358 GIC500_GICD_IROUTER_UPPER92 Register

1 GIC500_GICD_IROUTER_UPPER92 Register (Offset = 62E4h) [reset = 0h]

GICD_IROUTER92_upper

Return to Summary Table

Table 14-17941. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62E4h**

Figure 14-5951. GIC500_GICD_IROUTER_UPPER92 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17943. GIC500_GICD_IROUTER_UPPER92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.359 GIC500_GICD_IROUTER_LOWER93 Register

1 GIC500_GICD_IROUTER_LOWER93 Register (Offset = 62E8h) [reset = 0h]

GICD_IROUTER93_lower

Return to Summary Table

Table 14-17944. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62E8h**

Figure 14-5952. GIC500_GICD_IROUTER_LOWER93 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER93_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER93_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER93_LOWER__0_8							
R/W							
0h							

Table 14-17946. GIC500_GICD_IROUTER_LOWER93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER93_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER93_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER93_LOWER__0_8	R/W	0h	A0

14.4.1.2.360 GIC500_GICD_IROUTER_UPPER93 Register

1 GIC500_GICD_IROUTER_UPPER93 Register (Offset = 62ECh) [reset = 0h]

GICD_IROUTER93_upper

Return to Summary Table

Table 14-17947. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62ECh**

Figure 14-5953. GIC500_GICD_IROUTER_UPPER93 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17949. GIC500_GICD_IROUTER_UPPER93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.361 GIC500_GICD_IROUTER_LOWER94 Register

1 GIC500_GICD_IROUTER_LOWER94 Register (Offset = 62F0h) [reset = 0h]

GICD_IROUTER94_lower

Return to Summary Table

Table 14-17950. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62F0h**

Figure 14-5954. GIC500_GICD_IROUTER_LOWER94 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER94_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER94_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER94_LOWER__0_8							
R/W							
0h							

Table 14-17952. GIC500_GICD_IROUTER_LOWER94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER94_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER94_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER94_LOWER__0_8	R/W	0h	A0

14.4.1.2.362 GIC500_GICD_IROUTER_UPPER94 Register

1 GIC500_GICD_IROUTER_UPPER94 Register (Offset = 62F4h) [reset = 0h]

GICD_IROUTER94_upper

Return to Summary Table

Table 14-17953. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62F4h**

Figure 14-5955. GIC500_GICD_IROUTER_UPPER94 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17955. GIC500_GICD_IROUTER_UPPER94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.363 GIC500_GICD_IROUTER_LOWER95 Register

1 GIC500_GICD_IROUTER_LOWER95 Register (Offset = 62F8h) [reset = 0h]

GICD_IROUTER95_lower

Return to Summary Table

Table 14-17956. Instance Table

Instance Name	Physical Address
GICSS0	0180 62F8h

Figure 14-5956. GIC500_GICD_IROUTER_LOWER95 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER95_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER95_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER95_LOWER__0_8							
R/W							
0h							

Table 14-17958. GIC500_GICD_IROUTER_LOWER95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER95_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER95_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER95_LOWER__0_8	R/W	0h	A0

14.4.1.2.364 GIC500_GICD_IROUTER_UPPER95 Register

1 GIC500_GICD_IROUTER_UPPER95 Register (Offset = 62FCh) [reset = 0h]

GICD_IROUTER95_upper

Return to Summary Table

Table 14-17959. Instance Table

Instance Name	Physical Address
GICSS0	**0180 62FCh**

Figure 14-5957. GIC500_GICD_IROUTER_UPPER95 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17961. GIC500_GICD_IROUTER_UPPER95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.365 GIC500_GICD_IROUTER_LOWER96 Register

1 GIC500_GICD_IROUTER_LOWER96 Register (Offset = 6300h) [reset = 0h]

GICD_IROUTER96_lower

Return to Summary Table

Table 14-17962. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6300h**

Figure 14-5958. GIC500_GICD_IROUTER_LOWER96 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER96_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER96_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER96_LOWER__0_8							
R/W							
0h							

Table 14-17964. GIC500_GICD_IROUTER_LOWER96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER96_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER96_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER96_LOWER__0_8	R/W	0h	A0

14.4.1.2.366 GIC500_GICD_IROUTER_UPPER96 Register

1 GIC500_GICD_IROUTER_UPPER96 Register (Offset = 6304h) [reset = 0h]

GICD_IROUTER96_upper

Return to Summary Table

Table 14-17965. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6304h**

Figure 14-5959. GIC500_GICD_IROUTER_UPPER96 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17967. GIC500_GICD_IROUTER_UPPER96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.367 GIC500_GICD_IROUTER_LOWER97 Register

1 GIC500_GICD_IROUTER_LOWER97 Register (Offset = 6308h) [reset = 0h]

GICD_IROUTER97_lower

Return to Summary Table

Table 14-17968. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6308h**

Figure 14-5960. GIC500_GICD_IROUTER_LOWER97 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER97_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER97_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER97_LOWER__0_8							
R/W							
0h							

Table 14-17970. GIC500_GICD_IROUTER_LOWER97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER97_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER97_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER97_LOWER__0_8	R/W	0h	A0

14.4.1.2.368 GIC500_GICD_IROUTER_UPPER97 Register

1 GIC500_GICD_IROUTER_UPPER97 Register (Offset = 630Ch) [reset = 0h]

GICD_IROUTER97_upper

Return to Summary Table

Table 14-17971. Instance Table

Instance Name	Physical Address
GICSS0	**0180 630Ch**

Figure 14-5961. GIC500_GICD_IROUTER_UPPER97 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17973. GIC500_GICD_IROUTER_UPPER97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.369 GIC500_GICD_IROUTER_LOWER98 Register

1 GIC500_GICD_IROUTER_LOWER98 Register (Offset = 6310h) [reset = 0h]

GICD_IROUTER98_lower

Return to Summary Table

Table 14-17974. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6310h**

Figure 14-5962. GIC500_GICD_IROUTER_LOWER98 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER98_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER98_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER98_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17976. GIC500_GICD_IROUTER_LOWER98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER98_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER98_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER98_LOWER__0_8	R/W	0h	A0

14.4.1.2.370 GIC500_GICD_IROUTER_UPPER98 Register

1 GIC500_GICD_IROUTER_UPPER98 Register (Offset = 6314h) [reset = 0h]

GICD_IROUTER98_upper

Return to Summary Table

Table 14-17977. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6314h**

Figure 14-5963. GIC500_GICD_IROUTER_UPPER98 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17979. GIC500_GICD_IROUTER_UPPER98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.371 GIC500_GICD_IROUTER_LOWER99 Register

1 GIC500_GICD_IROUTER_LOWER99 Register (Offset = 6318h) [reset = 0h]

GICD_IROUTER99_lower

Return to Summary Table

Table 14-17980. Instance Table

Instance Name	Physical Address
GICSS0	0180 6318h

Figure 14-5964. GIC500_GICD_IROUTER_LOWER99 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER99_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER99_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER99_LOWER__0_8							
R/W							
0h							

Table 14-17982. GIC500_GICD_IROUTER_LOWER99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER99_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER99_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER99_LOWER__0_8	R/W	0h	A0

14.4.1.2.372 GIC500_GICD_IROUTER_UPPER99 Register

1 GIC500_GICD_IROUTER_UPPER99 Register (Offset = 631Ch) [reset = 0h]

GICD_IROUTER99_upper

Return to Summary Table

Table 14-17983. Instance Table

Instance Name	Physical Address
GICSS0	**0180 631Ch**

Figure 14-5965. GIC500_GICD_IROUTER_UPPER99 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17985. GIC500_GICD_IROUTER_UPPER99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.373 GIC500_GICD_IROUTER_LOWER100 Register

1 GIC500_GICD_IROUTER_LOWER100 Register (Offset = 6320h) [reset = 0h]

GICD_IROUTER100_lower

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Table 14-17986. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6320h**

Figure 14-5966. GIC500_GICD_IROUTER_LOWER100 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER100_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER100_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER100_LOWER__0_8							
R/W							
0h							

Table 14-17988. GIC500_GICD_IROUTER_LOWER100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER100_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER100_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER100_LOWER__0_8	R/W	0h	A0

14.4.1.2.374 GIC500_GICD_IROUTER_UPPER100 Register

1 GIC500_GICD_IROUTER_UPPER100 Register (Offset = 6324h) [reset = 0h]

GICD_IROUTER100_upper

Return to Summary Table

Table 14-17989. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6324h**

Figure 14-5967. GIC500_GICD_IROUTER_UPPER100 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17991. GIC500_GICD_IROUTER_UPPER100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.375 GIC500_GICD_IROUTER_LOWER101 Register

1 GIC500_GICD_IROUTER_LOWER101 Register (Offset = 6328h) [reset = 0h]

GICD_IROUTER101_lower

Return to Summary Table

Table 14-17992. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6328h**

Figure 14-5968. GIC500_GICD_IROUTER_LOWER101 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER101_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER101_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER101_LOWER__0_8							
R/W							
0h							

Table 14-17994. GIC500_GICD_IROUTER_LOWER101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER101_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER101_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER101_LOWER__0_8	R/W	0h	A0

14.4.1.2.376 GIC500_GICD_IROUTER_UPPER101 Register

1 GIC500_GICD_IROUTER_UPPER101 Register (Offset = 632Ch) [reset = 0h]

GICD_IROUTER101_upper

Return to Summary Table

Table 14-17995. Instance Table

Instance Name	Physical Address
GICSS0	0180 632Ch

Figure 14-5969. GIC500_GICD_IROUTER_UPPER101 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-17997. GIC500_GICD_IROUTER_UPPER101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.377 GIC500_GICD_IROUTER_LOWER102 Register

1 GIC500_GICD_IROUTER_LOWER102 Register (Offset = 6330h) [reset = 0h]

GICD_IROUTER102_lower

Return to Summary Table

Table 14-17998. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6330h**

Figure 14-5970. GIC500_GICD_IROUTER_LOWER102 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER102_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER102_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER102_LOWER__0_8							
R/W							
0h							

Table 14-18000. GIC500_GICD_IROUTER_LOWER102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER102_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER102_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER102_LOWER__0_8	R/W	0h	A0

14.4.1.2.378 GIC500_GICD_IROUTER_UPPER102 Register

1 GIC500_GICD_IROUTER_UPPER102 Register (Offset = 6334h) [reset = 0h]

GICD_IROUTER102_upper

Return to Summary Table

Table 14-18001. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6334h**

Figure 14-5971. GIC500_GICD_IROUTER_UPPER102 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18003. GIC500_GICD_IROUTER_UPPER102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.379 GIC500_GICD_IROUTER_LOWER103 Register

1 GIC500_GICD_IROUTER_LOWER103 Register (Offset = 6338h) [reset = 0h]

GICD_IROUTER103_lower

Return to Summary Table

Table 14-18004. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6338h**

Figure 14-5972. GIC500_GICD_IROUTER_LOWER103 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER103_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER103_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER103_LOWER__0_8							
R/W							
0h							

Table 14-18006. GIC500_GICD_IROUTER_LOWER103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER103_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER103_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER103_LOWER__0_8	R/W	0h	A0

14.4.1.2.380 GIC500_GICD_IROUTER_UPPER103 Register

1 GIC500_GICD_IROUTER_UPPER103 Register (Offset = 633Ch) [reset = 0h]

GICD_IROUTER103_upper

Return to Summary Table

Table 14-18007. Instance Table

Instance Name	Physical Address
GICSS0	**0180 633Ch**

Figure 14-5973. GIC500_GICD_IROUTER_UPPER103 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18009. GIC500_GICD_IROUTER_UPPER103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.381 GIC500_GICD_IROUTER_LOWER104 Register

1 GIC500_GICD_IROUTER_LOWER104 Register (Offset = 6340h) [reset = 0h]

GICD_IROUTER104_lower

Return to Summary Table

Table 14-18010. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6340h**

Figure 14-5974. GIC500_GICD_IROUTER_LOWER104 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER104_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER104_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER104_LOWER__0_8							
R/W							
0h							

Table 14-18012. GIC500_GICD_IROUTER_LOWER104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER104_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER104_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER104_LOWER__0_8	R/W	0h	A0

14.4.1.2.382 GIC500_GICD_IROUTER_UPPER104 Register

1 GIC500_GICD_IROUTER_UPPER104 Register (Offset = 6344h) [reset = 0h]

GICD_IROUTER104_upper

Return to Summary Table

Table 14-18013. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6344h**

Figure 14-5975. GIC500_GICD_IROUTER_UPPER104 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18015. GIC500_GICD_IROUTER_UPPER104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.383 GIC500_GICD_IROUTER_LOWER105 Register

1 GIC500_GICD_IROUTER_LOWER105 Register (Offset = 6348h) [reset = 0h]

GICD_IROUTER105_lower

Return to Summary Table

Table 14-18016. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6348h**

Figure 14-5976. GIC500_GICD_IROUTER_LOWER105 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER105_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER105_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER105_LOWER__0_8							
R/W							
0h							

Table 14-18018. GIC500_GICD_IROUTER_LOWER105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER105_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER105_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER105_LOWER__0_8	R/W	0h	A0

14.4.1.2.384 GIC500_GICD_IROUTER_UPPER105 Register

1 GIC500_GICD_IROUTER_UPPER105 Register (Offset = 634Ch) [reset = 0h]

GICD_IROUTER105_upper

Return to Summary Table

Table 14-18019. Instance Table

Instance Name	Physical Address
GICSS0	**0180 634Ch**

Figure 14-5977. GIC500_GICD_IROUTER_UPPER105 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18021. GIC500_GICD_IROUTER_UPPER105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.385 GIC500_GICD_IROUTER_LOWER106 Register

1 GIC500_GICD_IROUTER_LOWER106 Register (Offset = 6350h) [reset = 0h]

GICD_IROUTER106_lower

Return to Summary Table

Table 14-18022. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6350h**

Figure 14-5978. GIC500_GICD_IROUTER_LOWER106 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER106_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER106_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER106_LOWER__0_8							
R/W							
0h							

Table 14-18024. GIC500_GICD_IROUTER_LOWER106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER106_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER106_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER106_LOWER__0_8	R/W	0h	A0

14.4.1.2.386 GIC500_GICD_IROUTER_UPPER106 Register

1 GIC500_GICD_IROUTER_UPPER106 Register (Offset = 6354h) [reset = 0h]

GICD_IROUTER106_upper

Return to Summary Table

Table 14-18025. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6354h**

Figure 14-5979. GIC500_GICD_IROUTER_UPPER106 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18027. GIC500_GICD_IROUTER_UPPER106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.387 GIC500_GICD_IROUTER_LOWER107 Register

1 GIC500_GICD_IROUTER_LOWER107 Register (Offset = 6358h) [reset = 0h]

GICD_IROUTER107_lower

Return to Summary Table

Table 14-18028. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6358h**

Figure 14-5980. GIC500_GICD_IROUTER_LOWER107 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER107_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER107_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER107_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18030. GIC500_GICD_IROUTER_LOWER107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER107_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER107_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER107_LOWER__0_8	R/W	0h	A0

14.4.1.2.388 GIC500_GICD_IROUTER_UPPER107 Register

1 GIC500_GICD_IROUTER_UPPER107 Register (Offset = 635Ch) [reset = 0h]

GICD_IROUTER107_upper

Return to Summary Table

Table 14-18031. Instance Table

Instance Name	Physical Address
GICSS0	**0180 635Ch**

Figure 14-5981. GIC500_GICD_IROUTER_UPPER107 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18033. GIC500_GICD_IROUTER_UPPER107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.389 GIC500_GICD_IROUTER_LOWER108 Register

1 GIC500_GICD_IROUTER_LOWER108 Register (Offset = 6360h) [reset = 0h]

GICD_IROUTER108_lower

Return to Summary Table

Table 14-18034. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6360h**

Figure 14-5982. GIC500_GICD_IROUTER_LOWER108 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER108_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER108_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER108_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18036. GIC500_GICD_IROUTER_LOWER108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER108_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER108_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER108_LOWER__0_8	R/W	0h	A0

14.4.1.2.390 GIC500_GICD_IROUTER_UPPER108 Register

1 GIC500_GICD_IROUTER_UPPER108 Register (Offset = 6364h) [reset = 0h]

GICD_IROUTER108_upper

Return to Summary Table

Table 14-18037. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6364h**

Figure 14-5983. GIC500_GICD_IROUTER_UPPER108 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18039. GIC500_GICD_IROUTER_UPPER108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.391 GIC500_GICD_IROUTER_LOWER109 Register

1 GIC500_GICD_IROUTER_LOWER109 Register (Offset = 6368h) [reset = 0h]

GICD_IROUTER109_lower

Return to Summary Table

Table 14-18040. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6368h**

Figure 14-5984. GIC500_GICD_IROUTER_LOWER109 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER109_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER109_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER109_LOWER__0_8							
R/W							
0h							

Table 14-18042. GIC500_GICD_IROUTER_LOWER109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER109_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER109_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER109_LOWER__0_8	R/W	0h	A0

14.4.1.2.392 GIC500_GICD_IROUTER_UPPER109 Register

1 GIC500_GICD_IROUTER_UPPER109 Register (Offset = 636Ch) [reset = 0h]

GICD_IROUTER109_upper

Return to Summary Table

Table 14-18043. Instance Table

Instance Name	Physical Address
GICSS0	**0180 636Ch**

Figure 14-5985. GIC500_GICD_IROUTER_UPPER109 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18045. GIC500_GICD_IROUTER_UPPER109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.393 GIC500_GICD_IROUTER_LOWER110 Register

1 GIC500_GICD_IROUTER_LOWER110 Register (Offset = 6370h) [reset = 0h]

GICD_IROUTER110_lower

Return to Summary Table

Table 14-18046. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6370h**

Figure 14-5986. GIC500_GICD_IROUTER_LOWER110 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER110_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER110_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER110_LOWER__0_8							
R/W							
0h							

Table 14-18048. GIC500_GICD_IROUTER_LOWER110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER110_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER110_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER110_LOWER__0_8	R/W	0h	A0

14.4.1.2.394 GIC500_GICD_IROUTER_UPPER110 Register

1 GIC500_GICD_IROUTER_UPPER110 Register (Offset = 6374h) [reset = 0h]

GICD_IROUTER110_upper

Return to Summary Table

Table 14-18049. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6374h**

Figure 14-5987. GIC500_GICD_IROUTER_UPPER110 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18051. GIC500_GICD_IROUTER_UPPER110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.395 GIC500_GICD_IROUTER_LOWER111 Register

1 GIC500_GICD_IROUTER_LOWER111 Register (Offset = 6378h) [reset = 0h]

GICD_IROUTER111_lower

Return to Summary Table

Table 14-18052. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6378h**

Figure 14-5988. GIC500_GICD_IROUTER_LOWER111 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER111_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER111_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER111_LOWER__0_8							
R/W							
0h							

Table 14-18054. GIC500_GICD_IROUTER_LOWER111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER111_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER111_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER111_LOWER__0_8	R/W	0h	A0

14.4.1.2.396 GIC500_GICD_IROUTER_UPPER111 Register

1 GIC500_GICD_IROUTER_UPPER111 Register (Offset = 637Ch) [reset = 0h]

GICD_IROUTER111_upper

Return to Summary Table

Table 14-18055. Instance Table

Instance Name	Physical Address
GICSS0	**0180 637Ch**

Figure 14-5989. GIC500_GICD_IROUTER_UPPER111 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18057. GIC500_GICD_IROUTER_UPPER111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.397 GIC500_GICD_IROUTER_LOWER112 Register

1 GIC500_GICD_IROUTER_LOWER112 Register (Offset = 6380h) [reset = 0h]

GICD_IROUTER112_lower

Return to Summary Table

Table 14-18058. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6380h**

Figure 14-5990. GIC500_GICD_IROUTER_LOWER112 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER112_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER112_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER112_LOWER__0_8							
R/W							
0h							

Table 14-18060. GIC500_GICD_IROUTER_LOWER112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER112_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER112_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER112_LOWER__0_8	R/W	0h	A0

14.4.1.2.398 GIC500_GICD_IROUTER_UPPER112 Register

1 GIC500_GICD_IROUTER_UPPER112 Register (Offset = 6384h) [reset = 0h]

GICD_IROUTER112_upper

Return to Summary Table

Table 14-18061. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6384h**

Figure 14-5991. GIC500_GICD_IROUTER_UPPER112 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18063. GIC500_GICD_IROUTER_UPPER112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.399 GIC500_GICD_IROUTER_LOWER113 Register

1 GIC500_GICD_IROUTER_LOWER113 Register (Offset = 6388h) [reset = 0h]

GICD_IROUTER113_lower

Return to Summary Table

Table 14-18064. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6388h**

Figure 14-5992. GIC500_GICD_IROUTER_LOWER113 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER113_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER113_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER113_LOWER__0_8							
R/W							
0h							

Table 14-18066. GIC500_GICD_IROUTER_LOWER113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER113_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER113_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER113_LOWER__0_8	R/W	0h	A0

14.4.1.2.400 GIC500_GICD_IROUTER_UPPER113 Register

1 GIC500_GICD_IROUTER_UPPER113 Register (Offset = 638Ch) [reset = 0h]

GICD_IROUTER113_upper

Return to Summary Table

Table 14-18067. Instance Table

Instance Name	Physical Address
GICSS0	**0180 638Ch**

Figure 14-5993. GIC500_GICD_IROUTER_UPPER113 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18069. GIC500_GICD_IROUTER_UPPER113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.401 GIC500_GICD_IROUTER_LOWER114 Register

1 GIC500_GICD_IROUTER_LOWER114 Register (Offset = 6390h) [reset = 0h]

GICD_IROUTER114_lower

Return to Summary Table

Table 14-18070. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6390h**

Figure 14-5994. GIC500_GICD_IROUTER_LOWER114 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER114_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER114_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER114_LOWER__0_8							
R/W							
0h							

Table 14-18072. GIC500_GICD_IROUTER_LOWER114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER114_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER114_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER114_LOWER__0_8	R/W	0h	A0

14.4.1.2.402 GIC500_GICD_IROUTER_UPPER114 Register

1 GIC500_GICD_IROUTER_UPPER114 Register (Offset = 6394h) [reset = 0h]

GICD_IROUTER114_upper

Return to Summary Table

Table 14-18073. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6394h**

Figure 14-5995. GIC500_GICD_IROUTER_UPPER114 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18075. GIC500_GICD_IROUTER_UPPER114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.403 GIC500_GICD_IROUTER_LOWER115 Register

1 GIC500_GICD_IROUTER_LOWER115 Register (Offset = 6398h) [reset = 0h]

GICD_IROUTER115_lower

Return to Summary Table

Table 14-18076. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6398h**

Figure 14-5996. GIC500_GICD_IROUTER_LOWER115 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER115_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER115_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER115_LOWER__0_8							
R/W							
0h							

Table 14-18078. GIC500_GICD_IROUTER_LOWER115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER115_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER115_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER115_LOWER__0_8	R/W	0h	A0

14.4.1.2.404 GIC500_GICD_IROUTER_UPPER115 Register

1 GIC500_GICD_IROUTER_UPPER115 Register (Offset = 639Ch) [reset = 0h]

GICD_IROUTER115_upper

Return to Summary Table

Table 14-18079. Instance Table

Instance Name	Physical Address
GICSS0	**0180 639Ch**

Figure 14-5997. GIC500_GICD_IROUTER_UPPER115 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18081. GIC500_GICD_IROUTER_UPPER115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.405 GIC500_GICD_IROUTER_LOWER116 Register

1 GIC500_GICD_IROUTER_LOWER116 Register (Offset = 63A0h) [reset = 0h]

GICD_IROUTER116_lower

Return to Summary Table

Table 14-18082. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63A0h**

Figure 14-5998. GIC500_GICD_IROUTER_LOWER116 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER116_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER116_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER116_LOWER__0_8							
R/W							
0h							

Table 14-18084. GIC500_GICD_IROUTER_LOWER116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER116_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER116_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER116_LOWER__0_8	R/W	0h	A0

14.4.1.2.406 GIC500_GICD_IROUTER_UPPER116 Register

1 GIC500_GICD_IROUTER_UPPER116 Register (Offset = 63A4h) [reset = 0h]

GICD_IROUTER116_upper

Return to Summary Table

Table 14-18085. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63A4h**

Figure 14-5999. GIC500_GICD_IROUTER_UPPER116 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18087. GIC500_GICD_IROUTER_UPPER116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.407 GIC500_GICD_IROUTER_LOWER117 Register

1 GIC500_GICD_IROUTER_LOWER117 Register (Offset = 63A8h) [reset = 0h]

GICD_IROUTER117_lower

Return to Summary Table

Table 14-18088. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63A8h**

Figure 14-6000. GIC500_GICD_IROUTER_LOWER117 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER117_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER117_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER117_LOWER__0_8							
R/W							
0h							

Table 14-18090. GIC500_GICD_IROUTER_LOWER117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER117_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER117_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER117_LOWER__0_8	R/W	0h	A0

14.4.1.2.408 GIC500_GICD_IROUTER_UPPER117 Register

1 GIC500_GICD_IROUTER_UPPER117 Register (Offset = 63ACh) [reset = 0h]

GICD_IROUTER117_upper

Return to Summary Table

Table 14-18091. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63ACh**

Figure 14-6001. GIC500_GICD_IROUTER_UPPER117 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18093. GIC500_GICD_IROUTER_UPPER117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.409 GIC500_GICD_IROUTER_LOWER118 Register

1 GIC500_GICD_IROUTER_LOWER118 Register (Offset = 63B0h) [reset = 0h]

GICD_IROUTER118_lower

Return to Summary Table

Table 14-18094. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63B0h**

Figure 14-6002. GIC500_GICD_IROUTER_LOWER118 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER118_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER118_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER118_LOWER__0_8							
R/W							
0h							

Table 14-18096. GIC500_GICD_IROUTER_LOWER118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER118_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER118_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER118_LOWER__0_8	R/W	0h	A0

14.4.1.2.410 GIC500_GICD_IROUTER_UPPER118 Register

1 GIC500_GICD_IROUTER_UPPER118 Register (Offset = 63B4h) [reset = 0h]

GICD_IROUTER118_upper

Return to Summary Table

Table 14-18097. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63B4h**

Figure 14-6003. GIC500_GICD_IROUTER_UPPER118 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18099. GIC500_GICD_IROUTER_UPPER118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.411 GIC500_GICD_IROUTER_LOWER119 Register

1 GIC500_GICD_IROUTER_LOWER119 Register (Offset = 63B8h) [reset = 0h]

GICD_IROUTER119_lower

Return to Summary Table

Table 14-18100. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63B8h**

Figure 14-6004. GIC500_GICD_IROUTER_LOWER119 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER119_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER119_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER119_LOWER__0_8							
R/W							
0h							

Table 14-18102. GIC500_GICD_IROUTER_LOWER119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER119_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER119_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER119_LOWER__0_8	R/W	0h	A0

14.4.1.2.412 GIC500_GICD_IROUTER_UPPER119 Register

1 GIC500_GICD_IROUTER_UPPER119 Register (Offset = 63BCh) [reset = 0h]

GICD_IROUTER119_upper

Return to Summary Table

Table 14-18103. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63BCh**

Figure 14-6005. GIC500_GICD_IROUTER_UPPER119 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18105. GIC500_GICD_IROUTER_UPPER119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.413 GIC500_GICD_IROUTER_LOWER120 Register

1 GIC500_GICD_IROUTER_LOWER120 Register (Offset = 63C0h) [reset = 0h]

GICD_IROUTER120_lower

Return to Summary Table

Table 14-18106. Instance Table

Instance Name	Physical Address
GICSS0	0180 63C0h

Figure 14-6006. GIC500_GICD_IROUTER_LOWER120 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER120_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER120_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER120_LOWER__0_8							
R/W							
0h							

Table 14-18108. GIC500_GICD_IROUTER_LOWER120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER120_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER120_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER120_LOWER__0_8	R/W	0h	A0

14.4.1.2.414 GIC500_GICD_IROUTER_UPPER120 Register

1 GIC500_GICD_IROUTER_UPPER120 Register (Offset = 63C4h) [reset = 0h]

GICD_IROUTER120_upper

Return to Summary Table

Table 14-18109. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63C4h**

Figure 14-6007. GIC500_GICD_IROUTER_UPPER120 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18111. GIC500_GICD_IROUTER_UPPER120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.415 GIC500_GICD_IROUTER_LOWER121 Register

1 GIC500_GICD_IROUTER_LOWER121 Register (Offset = 63C8h) [reset = 0h]

GICD_IROUTER121_lower

Return to Summary Table

Table 14-18112. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63C8h**

Figure 14-6008. GIC500_GICD_IROUTER_LOWER121 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER121_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER121_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER121_LOWER__0_8							
R/W							
0h							

Table 14-18114. GIC500_GICD_IROUTER_LOWER121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER121_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER121_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER121_LOWER__0_8	R/W	0h	A0

14.4.1.2.416 GIC500_GICD_IROUTER_UPPER121 Register

1 GIC500_GICD_IROUTER_UPPER121 Register (Offset = 63CCh) [reset = 0h]

GICD_IROUTER121_upper

Return to Summary Table

Table 14-18115. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 63CCh**

Figure 14-6009. GIC500_GICD_IROUTER_UPPER121 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18117. GIC500_GICD_IROUTER_UPPER121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.417 GIC500_GICD_IROUTER_LOWER122 Register

1 GIC500_GICD_IROUTER_LOWER122 Register (Offset = 63D0h) [reset = 0h]

GICD_IROUTER122_lower

Return to Summary Table

Table 14-18118. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63D0h**

Figure 14-6010. GIC500_GICD_IROUTER_LOWER122 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER122_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER122_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER122_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18120. GIC500_GICD_IROUTER_LOWER122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER122_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER122_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER122_LOWER__0_8	R/W	0h	A0

14.4.1.2.418 GIC500_GICD_IROUTER_UPPER122 Register

1 GIC500_GICD_IROUTER_UPPER122 Register (Offset = 63D4h) [reset = 0h]

GICD_IROUTER122_upper

Return to Summary Table

Table 14-18121. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63D4h**

Figure 14-6011. GIC500_GICD_IROUTER_UPPER122 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18123. GIC500_GICD_IROUTER_UPPER122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.419 GIC500_GICD_IROUTER_LOWER123 Register

1 GIC500_GICD_IROUTER_LOWER123 Register (Offset = 63D8h) [reset = 0h]

GICD_IROUTER123_lower

Return to Summary Table

Table 14-18124. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63D8h**

Figure 14-6012. GIC500_GICD_IROUTER_LOWER123 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER123_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER123_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER123_LOWER__0_8							
R/W							
0h							

Table 14-18126. GIC500_GICD_IROUTER_LOWER123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER123_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER123_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER123_LOWER__0_8	R/W	0h	A0

14.4.1.2.420 GIC500_GICD_IROUTER_UPPER123 Register

1 GIC500_GICD_IROUTER_UPPER123 Register (Offset = 63DCh) [reset = 0h]

GICD_IROUTER123_upper

Return to Summary Table

Table 14-18127. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63DCh**

Figure 14-6013. GIC500_GICD_IROUTER_UPPER123 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18129. GIC500_GICD_IROUTER_UPPER123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.421 GIC500_GICD_IROUTER_LOWER124 Register

1 GIC500_GICD_IROUTER_LOWER124 Register (Offset = 63E0h) [reset = 0h]

GICD_IROUTER124_lower

Return to Summary Table

Table 14-18130. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63E0h**

Figure 14-6014. GIC500_GICD_IROUTER_LOWER124 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER124_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER124_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER124_LOWER__0_8							
R/W							
0h							

Table 14-18132. GIC500_GICD_IROUTER_LOWER124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER124_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER124_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER124_LOWER__0_8	R/W	0h	A0

14.4.1.2.422 GIC500_GICD_IROUTER_UPPER124 Register

1 GIC500_GICD_IROUTER_UPPER124 Register (Offset = 63E4h) [reset = 0h]

GICD_IROUTER124_upper

Return to Summary Table

Table 14-18133. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63E4h**

Figure 14-6015. GIC500_GICD_IROUTER_UPPER124 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18135. GIC500_GICD_IROUTER_UPPER124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.423 GIC500_GICD_IROUTER_LOWER125 Register

1 GIC500_GICD_IROUTER_LOWER125 Register (Offset = 63E8h) [reset = 0h]

GICD_IROUTER125_lower

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Table 14-18136. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63E8h**

Figure 14-6016. GIC500_GICD_IROUTER_LOWER125 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER125_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER125_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER125_LOWER__0_8							
R/W							
0h							

Table 14-18138. GIC500_GICD_IROUTER_LOWER125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER125_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER125_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER125_LOWER__0_8	R/W	0h	A0

14.4.1.2.424 GIC500_GICD_IROUTER_UPPER125 Register

1 GIC500_GICD_IROUTER_UPPER125 Register (Offset = 63ECh) [reset = 0h]

GICD_IROUTER125_upper

Return to Summary Table

Table 14-18139. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63ECh**

Figure 14-6017. GIC500_GICD_IROUTER_UPPER125 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18141. GIC500_GICD_IROUTER_UPPER125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.425 GIC500_GICD_IROUTER_LOWER126 Register

1 GIC500_GICD_IROUTER_LOWER126 Register (Offset = 63F0h) [reset = 0h]

GICD_IROUTER126_lower

Return to Summary Table

Table 14-18142. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63F0h**

Figure 14-6018. GIC500_GICD_IROUTER_LOWER126 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER126_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER126_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER126_LOWER__0_8							
R/W							
0h							

Table 14-18144. GIC500_GICD_IROUTER_LOWER126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER126_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER126_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER126_LOWER__0_8	R/W	0h	A0

14.4.1.2.426 GIC500_GICD_IROUTER_UPPER126 Register

1 GIC500_GICD_IROUTER_UPPER126 Register (Offset = 63F4h) [reset = 0h]

GICD_IROUTER126_upper

Return to Summary Table

Table 14-18145. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63F4h**

Figure 14-6019. GIC500_GICD_IROUTER_UPPER126 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18147. GIC500_GICD_IROUTER_UPPER126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.427 GIC500_GICD_IROUTER_LOWER127 Register

1 GIC500_GICD_IROUTER_LOWER127 Register (Offset = 63F8h) [reset = 0h]

GICD_IROUTER127_lower

Return to Summary Table

Table 14-18148. Instance Table

Instance Name	Physical Address
GICSS0	**0180 63F8h**

Figure 14-6020. GIC500_GICD_IROUTER_LOWER127 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER127_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER127_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER127_LOWER__0_8							
R/W							
0h							

Table 14-18150. GIC500_GICD_IROUTER_LOWER127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER127_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER127_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER127_LOWER__0_8	R/W	0h	A0

14.4.1.2.428 GIC500_GICD_IROUTER_UPPER127 Register

1 GIC500_GICD_IROUTER_UPPER127 Register (Offset = 63FCh) [reset = 0h]

GICD_IROUTER127_upper

Return to Summary Table

Table 14-18151. Instance Table

Instance Name	Physical Address
GICSS0	0180 63FCh

Figure 14-6021. GIC500_GICD_IROUTER_UPPER127 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18153. GIC500_GICD_IROUTER_UPPER127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.429 GIC500_GICD_IROUTER_LOWER128 Register

1 GIC500_GICD_IROUTER_LOWER128 Register (Offset = 6400h) [reset = 0h]

GICD_IROUTER128_lower

Return to Summary Table

Table 14-18154. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6400h**

Figure 14-6022. GIC500_GICD_IROUTER_LOWER128 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER128_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER128_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER128_LOWER__0_8							
R/W							
0h							

Table 14-18156. GIC500_GICD_IROUTER_LOWER128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER128_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER128_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER128_LOWER__0_8	R/W	0h	A0

14.4.1.2.430 GIC500_GICD_IROUTER_UPPER128 Register

1 GIC500_GICD_IROUTER_UPPER128 Register (Offset = 6404h) [reset = 0h]

GICD_IROUTER128_upper

Return to Summary Table

Table 14-18157. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6404h**

Figure 14-6023. GIC500_GICD_IROUTER_UPPER128 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18159. GIC500_GICD_IROUTER_UPPER128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.431 GIC500_GICD_IROUTER_LOWER129 Register

1 GIC500_GICD_IROUTER_LOWER129 Register (Offset = 6408h) [reset = 0h]

GICD_IROUTER129_lower

Return to Summary Table

Table 14-18160. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6408h**

Figure 14-6024. GIC500_GICD_IROUTER_LOWER129 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER129_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER129_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER129_LOWER__0_8							
R/W							
0h							

Table 14-18162. GIC500_GICD_IROUTER_LOWER129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER129_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER129_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER129_LOWER__0_8	R/W	0h	A0

14.4.1.2.432 GIC500_GICD_IROUTER_UPPER129 Register

1 GIC500_GICD_IROUTER_UPPER129 Register (Offset = 640Ch) [reset = 0h]

GICD_IROUTER129_upper

Return to Summary Table

Table 14-18163. Instance Table

Instance Name	Physical Address
GICSS0	**0180 640Ch**

Figure 14-6025. GIC500_GICD_IROUTER_UPPER129 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18165. GIC500_GICD_IROUTER_UPPER129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.433 GIC500_GICD_IROUTER_LOWER130 Register

1 GIC500_GICD_IROUTER_LOWER130 Register (Offset = 6410h) [reset = 0h]

GICD_IROUTER130_lower

Return to Summary Table

Table 14-18166. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6410h**

Figure 14-6026. GIC500_GICD_IROUTER_LOWER130 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER130_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER130_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER130_LOWER__0_8							
R/W							
0h							

Table 14-18168. GIC500_GICD_IROUTER_LOWER130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER130_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER130_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER130_LOWER__0_8	R/W	0h	A0

14.4.1.2.434 GIC500_GICD_IROUTER_UPPER130 Register

1 GIC500_GICD_IROUTER_UPPER130 Register (Offset = 6414h) [reset = 0h]

GICD_IROUTER130_upper

Return to Summary Table

Table 14-18169. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6414h**

Figure 14-6027. GIC500_GICD_IROUTER_UPPER130 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18171. GIC500_GICD_IROUTER_UPPER130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.435 GIC500_GICD_IROUTER_LOWER131 Register

1 GIC500_GICD_IROUTER_LOWER131 Register (Offset = 6418h) [reset = 0h]

GICD_IROUTER131_lower

Return to Summary Table

Table 14-18172. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6418h**

Figure 14-6028. GIC500_GICD_IROUTER_LOWER131 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER131_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER131_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER131_LOWER__0_8							
R/W							
0h							

Table 14-18174. GIC500_GICD_IROUTER_LOWER131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER131_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER131_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER131_LOWER__0_8	R/W	0h	A0

14.4.1.2.436 GIC500_GICD_IROUTER_UPPER131 Register

1 GIC500_GICD_IROUTER_UPPER131 Register (Offset = 641Ch) [reset = 0h]

GICD_IROUTER131_upper

Return to Summary Table

Table 14-18175. Instance Table

Instance Name	Physical Address
GICSS0	**0180 641Ch**

Figure 14-6029. GIC500_GICD_IROUTER_UPPER131 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18177. GIC500_GICD_IROUTER_UPPER131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.437 GIC500_GICD_IROUTER_LOWER132 Register

1 GIC500_GICD_IROUTER_LOWER132 Register (Offset = 6420h) [reset = 0h]

GICD_IROUTER132_lower

Return to Summary Table

Table 14-18178. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6420h**

Figure 14-6030. GIC500_GICD_IROUTER_LOWER132 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER132_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER132_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER132_LOWER__0_8							
R/W							
0h							

Table 14-18180. GIC500_GICD_IROUTER_LOWER132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER132_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER132_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER132_LOWER__0_8	R/W	0h	A0

14.4.1.2.438 GIC500_GICD_IROUTER_UPPER132 Register

1 GIC500_GICD_IROUTER_UPPER132 Register (Offset = 6424h) [reset = 0h]

GICD_IROUTER132_upper

Return to Summary Table

Table 14-18181. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6424h**

Figure 14-6031. GIC500_GICD_IROUTER_UPPER132 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18183. GIC500_GICD_IROUTER_UPPER132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.439 GIC500_GICD_IROUTER_LOWER133 Register

1 GIC500_GICD_IROUTER_LOWER133 Register (Offset = 6428h) [reset = 0h]

GICD_IROUTER133_lower

Return to Summary Table

Table 14-18184. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6428h**

Figure 14-6032. GIC500_GICD_IROUTER_LOWER133 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER133_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER133_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER133_LOWER__0_8							
R/W							
0h							

Table 14-18186. GIC500_GICD_IROUTER_LOWER133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER133_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER133_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER133_LOWER__0_8	R/W	0h	A0

14.4.1.2.440 GIC500_GICD_IROUTER_UPPER133 Register

1 GIC500_GICD_IROUTER_UPPER133 Register (Offset = 642Ch) [reset = 0h]

GICD_IROUTER133_upper

Return to Summary Table

Table 14-18187. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 642Ch**

Figure 14-6033. GIC500_GICD_IROUTER_UPPER133 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18189. GIC500_GICD_IROUTER_UPPER133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.441 GIC500_GICD_IROUTER_LOWER134 Register

1 GIC500_GICD_IROUTER_LOWER134 Register (Offset = 6430h) [reset = 0h]

GICD_IROUTER134_lower

Return to Summary Table

Table 14-18190. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6430h**

Figure 14-6034. GIC500_GICD_IROUTER_LOWER134 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER134_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER134_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER134_LOWER__0_8							
R/W							
0h							

Table 14-18192. GIC500_GICD_IROUTER_LOWER134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER134_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER134_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER134_LOWER__0_8	R/W	0h	A0

14.4.1.2.442 GIC500_GICD_IROUTER_UPPER134 Register

1 GIC500_GICD_IROUTER_UPPER134 Register (Offset = 6434h) [reset = 0h]

GICD_IROUTER134_upper

Return to Summary Table

Table 14-18193. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6434h**

Figure 14-6035. GIC500_GICD_IROUTER_UPPER134 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18195. GIC500_GICD_IROUTER_UPPER134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.443 GIC500_GICD_IROUTER_LOWER135 Register

1 GIC500_GICD_IROUTER_LOWER135 Register (Offset = 6438h) [reset = 0h]

GICD_IROUTER135_lower

Return to Summary Table

Table 14-18196. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6438h**

Figure 14-6036. GIC500_GICD_IROUTER_LOWER135 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER135_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER135_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER135_LOWER__0_8							
R/W							
0h							

Table 14-18198. GIC500_GICD_IROUTER_LOWER135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER135_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER135_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER135_LOWER__0_8	R/W	0h	A0

14.4.1.2.444 GIC500_GICD_IROUTER_UPPER135 Register

1 GIC500_GICD_IROUTER_UPPER135 Register (Offset = 643Ch) [reset = 0h]

GICD_IROUTER135_upper

Return to Summary Table

Table 14-18199. Instance Table

Instance Name	Physical Address
GICSS0	**0180 643Ch**

Figure 14-6037. GIC500_GICD_IROUTER_UPPER135 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18201. GIC500_GICD_IROUTER_UPPER135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.445 GIC500_GICD_IROUTER_LOWER136 Register

1 GIC500_GICD_IROUTER_LOWER136 Register (Offset = 6440h) [reset = 0h]

GICD_IROUTER136_lower

Return to Summary Table

Table 14-18202. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6440h**

Figure 14-6038. GIC500_GICD_IROUTER_LOWER136 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER136_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER136_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER136_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18204. GIC500_GICD_IROUTER_LOWER136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER136_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER136_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER136_LOWER__0_8	R/W	0h	A0

14.4.1.2.446 GIC500_GICD_IROUTER_UPPER136 Register

1 GIC500_GICD_IROUTER_UPPER136 Register (Offset = 6444h) [reset = 0h]

GICD_IROUTER136_upper

Return to Summary Table

Table 14-18205. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6444h**

Figure 14-6039. GIC500_GICD_IROUTER_UPPER136 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18207. GIC500_GICD_IROUTER_UPPER136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.447 GIC500_GICD_IROUTER_LOWER137 Register

1 GIC500_GICD_IROUTER_LOWER137 Register (Offset = 6448h) [reset = 0h]

GICD_IROUTER137_lower

Return to Summary Table

Table 14-18208. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6448h**

Figure 14-6040. GIC500_GICD_IROUTER_LOWER137 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER137_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER137_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER137_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18210. GIC500_GICD_IROUTER_LOWER137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER137_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER137_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER137_LOWER__0_8	R/W	0h	A0

14.4.1.2.448 GIC500_GICD_IROUTER_UPPER137 Register

1 GIC500_GICD_IROUTER_UPPER137 Register (Offset = 644Ch) [reset = 0h]

GICD_IROUTER137_upper

Return to Summary Table

Table 14-18211. Instance Table

Instance Name	Physical Address
GICSS0	**0180 644Ch**

Figure 14-6041. GIC500_GICD_IROUTER_UPPER137 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18213. GIC500_GICD_IROUTER_UPPER137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.449 GIC500_GICD_IROUTER_LOWER138 Register

1 GIC500_GICD_IROUTER_LOWER138 Register (Offset = 6450h) [reset = 0h]

GICD_IROUTER138_lower

Return to Summary Table

Table 14-18214. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6450h**

Figure 14-6042. GIC500_GICD_IROUTER_LOWER138 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER138_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER138_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER138_LOWER__0_8							
R/W							
0h							

Table 14-18216. GIC500_GICD_IROUTER_LOWER138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER138_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER138_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER138_LOWER__0_8	R/W	0h	A0

14.4.1.2.450 GIC500_GICD_IROUTER_UPPER138 Register

1 GIC500_GICD_IROUTER_UPPER138 Register (Offset = 6454h) [reset = 0h]

GICD_IROUTER138_upper

Return to Summary Table

Table 14-18217. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6454h**

Figure 14-6043. GIC500_GICD_IROUTER_UPPER138 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18219. GIC500_GICD_IROUTER_UPPER138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.451 GIC500_GICD_IROUTER_LOWER139 Register

1 GIC500_GICD_IROUTER_LOWER139 Register (Offset = 6458h) [reset = 0h]

GICD_IROUTER139_lower

Return to Summary Table

Table 14-18220. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6458h**

Figure 14-6044. GIC500_GICD_IROUTER_LOWER139 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER139_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER139_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER139_LOWER__0_8							
R/W							
0h							

Table 14-18222. GIC500_GICD_IROUTER_LOWER139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER139_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER139_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER139_LOWER__0_8	R/W	0h	A0

14.4.1.2.452 GIC500_GICD_IROUTER_UPPER139 Register

1 GIC500_GICD_IROUTER_UPPER139 Register (Offset = 645Ch) [reset = 0h]

GICD_IROUTER139_upper

Return to Summary Table

Table 14-18223. Instance Table

Instance Name	Physical Address
GICSS0	**0180 645Ch**

Figure 14-6045. GIC500_GICD_IROUTER_UPPER139 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18225. GIC500_GICD_IROUTER_UPPER139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.453 GIC500_GICD_IROUTER_LOWER140 Register

1 GIC500_GICD_IROUTER_LOWER140 Register (Offset = 6460h) [reset = 0h]

GICD_IROUTER140_lower

Return to Summary Table

Table 14-18226. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6460h**

Figure 14-6046. GIC500_GICD_IROUTER_LOWER140 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER140_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER140_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER140_LOWER__0_8							
R/W							
0h							

Table 14-18228. GIC500_GICD_IROUTER_LOWER140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER140_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER140_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER140_LOWER__0_8	R/W	0h	A0

14.4.1.2.454 GIC500_GICD_IROUTER_UPPER140 Register

1 GIC500_GICD_IROUTER_UPPER140 Register (Offset = 6464h) [reset = 0h]

GICD_IROUTER140_upper

Return to Summary Table

Table 14-18229. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6464h**

Figure 14-6047. GIC500_GICD_IROUTER_UPPER140 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18231. GIC500_GICD_IROUTER_UPPER140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.455 GIC500_GICD_IROUTER_LOWER141 Register

1 GIC500_GICD_IROUTER_LOWER141 Register (Offset = 6468h) [reset = 0h]

GICD_IROUTER141_lower

Return to Summary Table

Table 14-18232. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6468h**

Figure 14-6048. GIC500_GICD_IROUTER_LOWER141 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER141_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER141_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER141_LOWER__0_8							
R/W							
0h							

Table 14-18234. GIC500_GICD_IROUTER_LOWER141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER141_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER141_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER141_LOWER__0_8	R/W	0h	A0

14.4.1.2.456 GIC500_GICD_IROUTER_UPPER141 Register

1 GIC500_GICD_IROUTER_UPPER141 Register (Offset = 646Ch) [reset = 0h]

GICD_IROUTER141_upper

Return to Summary Table

Table 14-18235. Instance Table

Instance Name	Physical Address
GICSS0	**0180 646Ch**

Figure 14-6049. GIC500_GICD_IROUTER_UPPER141 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18237. GIC500_GICD_IROUTER_UPPER141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.457 GIC500_GICD_IROUTER_LOWER142 Register

1 GIC500_GICD_IROUTER_LOWER142 Register (Offset = 6470h) [reset = 0h]

GICD_IROUTER142_lower

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Table 14-18238. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6470h**

Figure 14-6050. GIC500_GICD_IROUTER_LOWER142 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER142_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER142_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER142_LOWER__0_8							
R/W							
0h							

Table 14-18240. GIC500_GICD_IROUTER_LOWER142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER142_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER142_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER142_LOWER__0_8	R/W	0h	A0

14.4.1.2.458 GIC500_GICD_IROUTER_UPPER142 Register

1 GIC500_GICD_IROUTER_UPPER142 Register (Offset = 6474h) [reset = 0h]

GICD_IROUTER142_upper

Return to Summary Table

Table 14-18241. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6474h**

Figure 14-6051. GIC500_GICD_IROUTER_UPPER142 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18243. GIC500_GICD_IROUTER_UPPER142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.459 GIC500_GICD_IROUTER_LOWER143 Register

1 GIC500_GICD_IROUTER_LOWER143 Register (Offset = 6478h) [reset = 0h]

GICD_IROUTER143_lower

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Table 14-18244. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6478h**

Figure 14-6052. GIC500_GICD_IROUTER_LOWER143 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER143_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER143_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER143_LOWER__0_8							
R/W							
0h							

Table 14-18246. GIC500_GICD_IROUTER_LOWER143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER143_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER143_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER143_LOWER__0_8	R/W	0h	A0

14.4.1.2.460 GIC500_GICD_IROUTER_UPPER143 Register

1 GIC500_GICD_IROUTER_UPPER143 Register (Offset = 647Ch) [reset = 0h]

GICD_IROUTER143_upper

Return to Summary Table

Table 14-18247. Instance Table

Instance Name	Physical Address
GICSS0	**0180 647Ch**

Figure 14-6053. GIC500_GICD_IROUTER_UPPER143 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18249. GIC500_GICD_IROUTER_UPPER143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.461 GIC500_GICD_IROUTER_LOWER144 Register

1 GIC500_GICD_IROUTER_LOWER144 Register (Offset = 6480h) [reset = 0h]

GICD_IROUTER144_lower

Return to Summary Table

Table 14-18250. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6480h**

Figure 14-6054. GIC500_GICD_IROUTER_LOWER144 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER144_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER144_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER144_LOWER__0_8							
R/W							
0h							

Table 14-18252. GIC500_GICD_IROUTER_LOWER144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER144_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER144_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER144_LOWER__0_8	R/W	0h	A0

14.4.1.2.462 GIC500_GICD_IROUTER_UPPER144 Register

1 GIC500_GICD_IROUTER_UPPER144 Register (Offset = 6484h) [reset = 0h]

GICD_IROUTER144_upper

Return to Summary Table

Table 14-18253. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6484h**

Figure 14-6055. GIC500_GICD_IROUTER_UPPER144 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18255. GIC500_GICD_IROUTER_UPPER144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.463 GIC500_GICD_IROUTER_LOWER145 Register

1 GIC500_GICD_IROUTER_LOWER145 Register (Offset = 6488h) [reset = 0h]

GICD_IROUTER145_lower

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Table 14-18256. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6488h**

Figure 14-6056. GIC500_GICD_IROUTER_LOWER145 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER145_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER145_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER145_LOWER__0_8							
R/W							
0h							

Table 14-18258. GIC500_GICD_IROUTER_LOWER145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER145_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER145_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER145_LOWER__0_8	R/W	0h	A0

14.4.1.2.464 GIC500_GICD_IROUTER_UPPER145 Register

1 GIC500_GICD_IROUTER_UPPER145 Register (Offset = 648Ch) [reset = 0h]

GICD_IROUTER145_upper

Return to Summary Table

Table 14-18259. Instance Table

Instance Name	Physical Address
GICSS0	**0180 648Ch**

Figure 14-6057. GIC500_GICD_IROUTER_UPPER145 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18261. GIC500_GICD_IROUTER_UPPER145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.465 GIC500_GICD_IROUTER_LOWER146 Register

1 GIC500_GICD_IROUTER_LOWER146 Register (Offset = 6490h) [reset = 0h]

GICD_IROUTER146_lower

Return to Summary Table

Table 14-18262. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6490h**

Figure 14-6058. GIC500_GICD_IROUTER_LOWER146 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER146_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER146_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER146_LOWER__0_8							
R/W							
0h							

Table 14-18264. GIC500_GICD_IROUTER_LOWER146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER146_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER146_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER146_LOWER__0_8	R/W	0h	A0

14.4.1.2.466 GIC500_GICD_IROUTER_UPPER146 Register

1 GIC500_GICD_IROUTER_UPPER146 Register (Offset = 6494h) [reset = 0h]

GICD_IROUTER146_upper

Return to Summary Table

Table 14-18265. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6494h**

Figure 14-6059. GIC500_GICD_IROUTER_UPPER146 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18267. GIC500_GICD_IROUTER_UPPER146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.467 GIC500_GICD_IROUTER_LOWER147 Register

1 GIC500_GICD_IROUTER_LOWER147 Register (Offset = 6498h) [reset = 0h]

GICD_IROUTER147_lower

Return to Summary Table

Table 14-18268. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6498h**

Figure 14-6060. GIC500_GICD_IROUTER_LOWER147 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER147_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER147_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER147_LOWER__0_8							
R/W							
0h							

Table 14-18270. GIC500_GICD_IROUTER_LOWER147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER147_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER147_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER147_LOWER__0_8	R/W	0h	A0

14.4.1.2.468 GIC500_GICD_IROUTER_UPPER147 Register

1 GIC500_GICD_IROUTER_UPPER147 Register (Offset = 649Ch) [reset = 0h]

GICD_IROUTER147_upper

Return to Summary Table

Table 14-18271. Instance Table

Instance Name	Physical Address
GICSS0	0180 649Ch

Figure 14-6061. GIC500_GICD_IROUTER_UPPER147 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18273. GIC500_GICD_IROUTER_UPPER147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.469 GIC500_GICD_IROUTER_LOWER148 Register

1 GIC500_GICD_IROUTER_LOWER148 Register (Offset = 64A0h) [reset = 0h]

GICD_IROUTER148_lower

Return to Summary Table

Table 14-18274. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64A0h**

Figure 14-6062. GIC500_GICD_IROUTER_LOWER148 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER148_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER148_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER148_LOWER__0_8							
R/W							
0h							

Table 14-18276. GIC500_GICD_IROUTER_LOWER148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER148_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER148_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER148_LOWER__0_8	R/W	0h	A0

14.4.1.2.470 GIC500_GICD_IROUTER_UPPER148 Register

1 GIC500_GICD_IROUTER_UPPER148 Register (Offset = 64A4h) [reset = 0h]

GICD_IROUTER148_upper

Return to Summary Table

Table 14-18277. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64A4h**

Figure 14-6063. GIC500_GICD_IROUTER_UPPER148 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18279. GIC500_GICD_IROUTER_UPPER148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.471 GIC500_GICD_IROUTER_LOWER149 Register

1 GIC500_GICD_IROUTER_LOWER149 Register (Offset = 64A8h) [reset = 0h]

GICD_IROUTER149_lower

Return to Summary Table

Table 14-18280. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64A8h**

Figure 14-6064. GIC500_GICD_IROUTER_LOWER149 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER149_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER149_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER149_LOWER__0_8							
R/W							
0h							

Table 14-18282. GIC500_GICD_IROUTER_LOWER149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER149_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER149_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER149_LOWER__0_8	R/W	0h	A0

14.4.1.2.472 GIC500_GICD_IROUTER_UPPER149 Register

1 GIC500_GICD_IROUTER_UPPER149 Register (Offset = 64ACh) [reset = 0h]

GICD_IROUTER149_upper

Return to Summary Table

Table 14-18283. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64ACh**

Figure 14-6065. GIC500_GICD_IROUTER_UPPER149 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18285. GIC500_GICD_IROUTER_UPPER149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.473 GIC500_GICD_IROUTER_LOWER150 Register

1 GIC500_GICD_IROUTER_LOWER150 Register (Offset = 64B0h) [reset = 0h]

GICD_IROUTER150_lower

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Table 14-18286. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64B0h**

Figure 14-6066. GIC500_GICD_IROUTER_LOWER150 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER150_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER150_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER150_LOWER__0_8							
R/W							
0h							

Table 14-18288. GIC500_GICD_IROUTER_LOWER150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER150_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER150_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER150_LOWER__0_8	R/W	0h	A0

14.4.1.2.474 GIC500_GICD_IROUTER_UPPER150 Register

1 GIC500_GICD_IROUTER_UPPER150 Register (Offset = 64B4h) [reset = 0h]

GICD_IROUTER150_upper

Return to Summary Table

Table 14-18289. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64B4h**

Figure 14-6067. GIC500_GICD_IROUTER_UPPER150 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18291. GIC500_GICD_IROUTER_UPPER150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.475 GIC500_GICD_IROUTER_LOWER151 Register

1 GIC500_GICD_IROUTER_LOWER151 Register (Offset = 64B8h) [reset = 0h]

GICD_IROUTER151_lower

Return to Summary Table

Table 14-18292. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64B8h**

Figure 14-6068. GIC500_GICD_IROUTER_LOWER151 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER151_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER151_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER151_LOWER__0_8							
R/W							
0h							

Table 14-18294. GIC500_GICD_IROUTER_LOWER151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER151_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER151_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER151_LOWER__0_8	R/W	0h	A0

14.4.1.2.476 GIC500_GICD_IROUTER_UPPER151 Register

1 GIC500_GICD_IROUTER_UPPER151 Register (Offset = 64BCh) [reset = 0h]

GICD_IROUTER151_upper

Return to Summary Table

Table 14-18295. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64BCh**

Figure 14-6069. GIC500_GICD_IROUTER_UPPER151 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18297. GIC500_GICD_IROUTER_UPPER151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.477 GIC500_GICD_IROUTER_LOWER152 Register

1 GIC500_GICD_IROUTER_LOWER152 Register (Offset = 64C0h) [reset = 0h]

GICD_IROUTER152_lower

Return to Summary Table

Table 14-18298. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64C0h**

Figure 14-6070. GIC500_GICD_IROUTER_LOWER152 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER152_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER152_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER152_LOWER__0_8							
R/W							
0h							

Table 14-18300. GIC500_GICD_IROUTER_LOWER152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER152_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER152_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER152_LOWER__0_8	R/W	0h	A0

14.4.1.2.478 GIC500_GICD_IROUTER_UPPER152 Register

1 GIC500_GICD_IROUTER_UPPER152 Register (Offset = 64C4h) [reset = 0h]

GICD_IROUTER152_upper

Return to Summary Table

Table 14-18301. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64C4h**

Figure 14-6071. GIC500_GICD_IROUTER_UPPER152 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18303. GIC500_GICD_IROUTER_UPPER152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.479 GIC500_GICD_IROUTER_LOWER153 Register

1 GIC500_GICD_IROUTER_LOWER153 Register (Offset = 64C8h) [reset = 0h]

GICD_IROUTER153_lower

Return to Summary Table

Table 14-18304. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64C8h**

Figure 14-6072. GIC500_GICD_IROUTER_LOWER153 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER153_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER153_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER153_LOWER__0_8							
R/W							
0h							

Table 14-18306. GIC500_GICD_IROUTER_LOWER153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER153_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER153_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER153_LOWER__0_8	R/W	0h	A0

14.4.1.2.480 GIC500_GICD_IROUTER_UPPER153 Register

1 GIC500_GICD_IROUTER_UPPER153 Register (Offset = 64CCh) [reset = 0h]

GICD_IROUTER153_upper

Return to Summary Table

Table 14-18307. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64CCh**

Figure 14-6073. GIC500_GICD_IROUTER_UPPER153 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18309. GIC500_GICD_IROUTER_UPPER153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.481 GIC500_GICD_IROUTER_LOWER154 Register

1 GIC500_GICD_IROUTER_LOWER154 Register (Offset = 64D0h) [reset = 0h]

GICD_IROUTER154_lower

Return to Summary Table

Table 14-18310. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64D0h**

Figure 14-6074. GIC500_GICD_IROUTER_LOWER154 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER154_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER154_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER154_LOWER__0_8							
R/W							
0h							

Table 14-18312. GIC500_GICD_IROUTER_LOWER154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER154_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER154_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER154_LOWER__0_8	R/W	0h	A0

14.4.1.2.482 GIC500_GICD_IROUTER_UPPER154 Register

1 GIC500_GICD_IROUTER_UPPER154 Register (Offset = 64D4h) [reset = 0h]

GICD_IROUTER154_upper

Return to Summary Table

Table 14-18313. Instance Table

Instance Name	Physical Address
GICSS0	0180 64D4h

Figure 14-6075. GIC500_GICD_IROUTER_UPPER154 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18315. GIC500_GICD_IROUTER_UPPER154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.483 GIC500_GICD_IROUTER_LOWER155 Register

1 GIC500_GICD_IROUTER_LOWER155 Register (Offset = 64D8h) [reset = 0h]

GICD_IROUTER155_lower

Return to Summary Table

Table 14-18316. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64D8h**

Figure 14-6076. GIC500_GICD_IROUTER_LOWER155 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER155_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER155_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER155_LOWER__0_8							
R/W							
0h							

Table 14-18318. GIC500_GICD_IROUTER_LOWER155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER155_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER155_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER155_LOWER__0_8	R/W	0h	A0

14.4.1.2.484 GIC500_GICD_IROUTER_UPPER155 Register

1 GIC500_GICD_IROUTER_UPPER155 Register (Offset = 64DCh) [reset = 0h]

GICD_IROUTER155_upper

Return to Summary Table

Table 14-18319. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64DCh**

Figure 14-6077. GIC500_GICD_IROUTER_UPPER155 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18321. GIC500_GICD_IROUTER_UPPER155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.485 GIC500_GICD_IROUTER_LOWER156 Register

1 GIC500_GICD_IROUTER_LOWER156 Register (Offset = 64E0h) [reset = 0h]

GICD_IROUTER156_lower

Return to Summary Table

Table 14-18322. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64E0h**

Figure 14-6078. GIC500_GICD_IROUTER_LOWER156 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER156_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER156_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER156_LOWER__0_8							
R/W							
0h							

Table 14-18324. GIC500_GICD_IROUTER_LOWER156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER156_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER156_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER156_LOWER__0_8	R/W	0h	A0

14.4.1.2.486 GIC500_GICD_IROUTER_UPPER156 Register

1 GIC500_GICD_IROUTER_UPPER156 Register (Offset = 64E4h) [reset = 0h]

GICD_IROUTER156_upper

Return to Summary Table

Table 14-18325. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64E4h**

Figure 14-6079. GIC500_GICD_IROUTER_UPPER156 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18327. GIC500_GICD_IROUTER_UPPER156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.487 GIC500_GICD_IROUTER_LOWER157 Register

1 GIC500_GICD_IROUTER_LOWER157 Register (Offset = 64E8h) [reset = 0h]

GICD_IROUTER157_lower

Return to Summary Table

Table 14-18328. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64E8h**

Figure 14-6080. GIC500_GICD_IROUTER_LOWER157 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER157_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER157_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER157_LOWER__0_8							
R/W							
0h							

Table 14-18330. GIC500_GICD_IROUTER_LOWER157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER157_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER157_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER157_LOWER__0_8	R/W	0h	A0

14.4.1.2.488 GIC500_GICD_IROUTER_UPPER157 Register

1 GIC500_GICD_IROUTER_UPPER157 Register (Offset = 64ECh) [reset = 0h]

GICD_IROUTER157_upper

Return to Summary Table

Table 14-18331. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64ECh**

Figure 14-6081. GIC500_GICD_IROUTER_UPPER157 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18333. GIC500_GICD_IROUTER_UPPER157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.489 GIC500_GICD_IROUTER_LOWER158 Register

1 GIC500_GICD_IROUTER_LOWER158 Register (Offset = 64F0h) [reset = 0h]

GICD_IROUTER158_lower

Return to Summary Table

Table 14-18334. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64F0h**

Figure 14-6082. GIC500_GICD_IROUTER_LOWER158 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER158_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER158_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER158_LOWER__0_8							
R/W							
0h							

Table 14-18336. GIC500_GICD_IROUTER_LOWER158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER158_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER158_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER158_LOWER__0_8	R/W	0h	A0

14.4.1.2.490 GIC500_GICD_IROUTER_UPPER158 Register

1 GIC500_GICD_IROUTER_UPPER158 Register (Offset = 64F4h) [reset = 0h]

GICD_IROUTER158_upper

Return to Summary Table

Table 14-18337. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64F4h**

Figure 14-6083. GIC500_GICD_IROUTER_UPPER158 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18339. GIC500_GICD_IROUTER_UPPER158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.491 GIC500_GICD_IROUTER_LOWER159 Register

1 GIC500_GICD_IROUTER_LOWER159 Register (Offset = 64F8h) [reset = 0h]

GICD_IROUTER159_lower

Return to Summary Table

Table 14-18340. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64F8h**

Figure 14-6084. GIC500_GICD_IROUTER_LOWER159 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER159_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER159_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER159_LOWER__0_8							
R/W							
0h							

Table 14-18342. GIC500_GICD_IROUTER_LOWER159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER159_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER159_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER159_LOWER__0_8	R/W	0h	A0

14.4.1.2.492 GIC500_GICD_IROUTER_UPPER159 Register

1 GIC500_GICD_IROUTER_UPPER159 Register (Offset = 64FCh) [reset = 0h]

GICD_IROUTER159_upper

Return to Summary Table

Table 14-18343. Instance Table

Instance Name	Physical Address
GICSS0	**0180 64FCh**

Figure 14-6085. GIC500_GICD_IROUTER_UPPER159 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18345. GIC500_GICD_IROUTER_UPPER159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.493 GIC500_GICD_IROUTER_LOWER160 Register

1 GIC500_GICD_IROUTER_LOWER160 Register (Offset = 6500h) [reset = 0h]

GICD_IROUTER160_lower

Return to Summary Table

Table 14-18346. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6500h**

Figure 14-6086. GIC500_GICD_IROUTER_LOWER160 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER160_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER160_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER160_LOWER__0_8							
R/W							
0h							

Table 14-18348. GIC500_GICD_IROUTER_LOWER160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER160_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER160_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER160_LOWER__0_8	R/W	0h	A0

14.4.1.2.494 GIC500_GICD_IROUTER_UPPER160 Register

1 GIC500_GICD_IROUTER_UPPER160 Register (Offset = 6504h) [reset = 0h]

GICD_IROUTER160_upper

Return to Summary Table

Table 14-18349. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6504h**

Figure 14-6087. GIC500_GICD_IROUTER_UPPER160 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18351. GIC500_GICD_IROUTER_UPPER160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.495 GIC500_GICD_IROUTER_LOWER161 Register

1 GIC500_GICD_IROUTER_LOWER161 Register (Offset = 6508h) [reset = 0h]

GICD_IROUTER161_lower

Return to Summary Table

Table 14-18352. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6508h**

Figure 14-6088. GIC500_GICD_IROUTER_LOWER161 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER161_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER161_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER161_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18354. GIC500_GICD_IROUTER_LOWER161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER161_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER161_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER161_LOWER__0_8	R/W	0h	A0

14.4.1.2.496 GIC500_GICD_IROUTER_UPPER161 Register

1 GIC500_GICD_IROUTER_UPPER161 Register (Offset = 650Ch) [reset = 0h]

GICD_IROUTER161_upper

Return to Summary Table

Table 14-18355. Instance Table

Instance Name	Physical Address
GICSS0	**0180 650Ch**

Figure 14-6089. GIC500_GICD_IROUTER_UPPER161 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18357. GIC500_GICD_IROUTER_UPPER161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.497 GIC500_GICD_IROUTER_LOWER162 Register

1 GIC500_GICD_IROUTER_LOWER162 Register (Offset = 6510h) [reset = 0h]

GICD_IROUTER162_lower

Return to Summary Table

Table 14-18358. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6510h**

Figure 14-6090. GIC500_GICD_IROUTER_LOWER162 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER162_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER162_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER162_LOWER__0_8							
R/W							
0h							

Table 14-18360. GIC500_GICD_IROUTER_LOWER162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER162_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER162_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER162_LOWER__0_8	R/W	0h	A0

14.4.1.2.498 GIC500_GICD_IROUTER_UPPER162 Register

1 GIC500_GICD_IROUTER_UPPER162 Register (Offset = 6514h) [reset = 0h]

GICD_IROUTER162_upper

Return to Summary Table

Table 14-18361. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6514h**

Figure 14-6091. GIC500_GICD_IROUTER_UPPER162 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18363. GIC500_GICD_IROUTER_UPPER162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.499 GIC500_GICD_IROUTER_LOWER163 Register

1 GIC500_GICD_IROUTER_LOWER163 Register (Offset = 6518h) [reset = 0h]

GICD_IROUTER163_lower

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Table 14-18364. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6518h**

Figure 14-6092. GIC500_GICD_IROUTER_LOWER163 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER163_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER163_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER163_LOWER__0_8							
R/W							
0h							

Table 14-18366. GIC500_GICD_IROUTER_LOWER163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER163_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER163_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER163_LOWER__0_8	R/W	0h	A0

14.4.1.2.500 GIC500_GICD_IROUTER_UPPER163 Register

1 GIC500_GICD_IROUTER_UPPER163 Register (Offset = 651Ch) [reset = 0h]

GICD_IROUTER163_upper

Return to Summary Table

Table 14-18367. Instance Table

Instance Name	Physical Address
GICSS0	**0180 651Ch**

Figure 14-6093. GIC500_GICD_IROUTER_UPPER163 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18369. GIC500_GICD_IROUTER_UPPER163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.501 GIC500_GICD_IROUTER_LOWER164 Register

1 GIC500_GICD_IROUTER_LOWER164 Register (Offset = 6520h) [reset = 0h]

GICD_IROUTER164_lower

Return to Summary Table

Table 14-18370. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6520h**

Figure 14-6094. GIC500_GICD_IROUTER_LOWER164 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER164_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER164_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER164_LOWER__0_8							
R/W							
0h							

Table 14-18372. GIC500_GICD_IROUTER_LOWER164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER164_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER164_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER164_LOWER__0_8	R/W	0h	A0

14.4.1.2.502 GIC500_GICD_IROUTER_UPPER164 Register

1 GIC500_GICD_IROUTER_UPPER164 Register (Offset = 6524h) [reset = 0h]

GICD_IROUTER164_upper

Return to Summary Table

Table 14-18373. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 6524h**

Figure 14-6095. GIC500_GICD_IROUTER_UPPER164 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18375. GIC500_GICD_IROUTER_UPPER164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.503 GIC500_GICD_IROUTER_LOWER165 Register

1 GIC500_GICD_IROUTER_LOWER165 Register (Offset = 6528h) [reset = 0h]

GICD_IROUTER165_lower

Return to Summary Table

Table 14-18376. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6528h**

Figure 14-6096. GIC500_GICD_IROUTER_LOWER165 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER165_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER165_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER165_LOWER__0_8							
R/W							
0h							

Table 14-18378. GIC500_GICD_IROUTER_LOWER165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER165_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER165_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER165_LOWER__0_8	R/W	0h	A0

14.4.1.2.504 GIC500_GICD_IROUTER_UPPER165 Register

1 GIC500_GICD_IROUTER_UPPER165 Register (Offset = 652Ch) [reset = 0h]

GICD_IROUTER165_upper

Return to Summary Table

Table 14-18379. Instance Table

Instance Name	Physical Address
GICSS0	**0180 652Ch**

Figure 14-6097. GIC500_GICD_IROUTER_UPPER165 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18381. GIC500_GICD_IROUTER_UPPER165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.505 GIC500_GICD_IROUTER_LOWER166 Register

1 GIC500_GICD_IROUTER_LOWER166 Register (Offset = 6530h) [reset = 0h]

GICD_IROUTER166_lower

Return to Summary Table

Table 14-18382. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6530h**

Figure 14-6098. GIC500_GICD_IROUTER_LOWER166 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER166_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER166_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER166_LOWER__0_8							
R/W							
0h							

Table 14-18384. GIC500_GICD_IROUTER_LOWER166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER166_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER166_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER166_LOWER__0_8	R/W	0h	A0

14.4.1.2.506 GIC500_GICD_IROUTER_UPPER166 Register

1 GIC500_GICD_IROUTER_UPPER166 Register (Offset = 6534h) [reset = 0h]

GICD_IROUTER166_upper

Return to Summary Table

Table 14-18385. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6534h**

Figure 14-6099. GIC500_GICD_IROUTER_UPPER166 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18387. GIC500_GICD_IROUTER_UPPER166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.507 GIC500_GICD_IROUTER_LOWER167 Register

1 GIC500_GICD_IROUTER_LOWER167 Register (Offset = 6538h) [reset = 0h]

GICD_IROUTER167_lower

Return to Summary Table

Table 14-18388. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6538h**

Figure 14-6100. GIC500_GICD_IROUTER_LOWER167 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER167_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER167_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER167_LOWER__0_8							
R/W							
0h							

Table 14-18390. GIC500_GICD_IROUTER_LOWER167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER167_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER167_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER167_LOWER__0_8	R/W	0h	A0

14.4.1.2.508 GIC500_GICD_IROUTER_UPPER167 Register

1 GIC500_GICD_IROUTER_UPPER167 Register (Offset = 653Ch) [reset = 0h]

GICD_IROUTER167_upper

Return to Summary Table

Table 14-18391. Instance Table

Instance Name	Physical Address
GICSS0	**0180 653Ch**

Figure 14-6101. GIC500_GICD_IROUTER_UPPER167 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18393. GIC500_GICD_IROUTER_UPPER167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.509 GIC500_GICD_IROUTER_LOWER168 Register

1 GIC500_GICD_IROUTER_LOWER168 Register (Offset = 6540h) [reset = 0h]

GICD_IROUTER168_lower

Return to Summary Table

Table 14-18394. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6540h**

Figure 14-6102. GIC500_GICD_IROUTER_LOWER168 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER168_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER168_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER168_LOWER__0_8							
R/W							
0h							

Table 14-18396. GIC500_GICD_IROUTER_LOWER168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER168_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER168_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER168_LOWER__0_8	R/W	0h	A0

14.4.1.2.510 GIC500_GICD_IROUTER_UPPER168 Register

1 GIC500_GICD_IROUTER_UPPER168 Register (Offset = 6544h) [reset = 0h]

GICD_IROUTER168_upper

Return to Summary Table

Table 14-18397. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6544h**

Figure 14-6103. GIC500_GICD_IROUTER_UPPER168 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18399. GIC500_GICD_IROUTER_UPPER168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.511 GIC500_GICD_IROUTER_LOWER169 Register

1 GIC500_GICD_IROUTER_LOWER169 Register (Offset = 6548h) [reset = 0h]

GICD_IROUTER169_lower

Return to Summary Table

Table 14-18400. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6548h**

Figure 14-6104. GIC500_GICD_IROUTER_LOWER169 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER169_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER169_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER169_LOWER__0_8							
R/W							
0h							

Table 14-18402. GIC500_GICD_IROUTER_LOWER169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER169_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER169_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER169_LOWER__0_8	R/W	0h	A0

14.4.1.2.512 GIC500_GICD_IROUTER_UPPER169 Register

1 GIC500_GICD_IROUTER_UPPER169 Register (Offset = 654Ch) [reset = 0h]

GICD_IROUTER169_upper

Return to Summary Table

Table 14-18403. Instance Table

Instance Name	Physical Address
GICSS0	**0180 654Ch**

Figure 14-6105. GIC500_GICD_IROUTER_UPPER169 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18405. GIC500_GICD_IROUTER_UPPER169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.513 GIC500_GICD_IROUTER_LOWER170 Register

1 GIC500_GICD_IROUTER_LOWER170 Register (Offset = 6550h) [reset = 0h]

GICD_IROUTER170_lower

Return to Summary Table

Table 14-18406. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6550h**

Figure 14-6106. GIC500_GICD_IROUTER_LOWER170 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER170_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER170_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER170_LOWER__0_8							
R/W							
0h							

Table 14-18408. GIC500_GICD_IROUTER_LOWER170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER170_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER170_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER170_LOWER__0_8	R/W	0h	A0

14.4.1.2.514 GIC500_GICD_IROUTER_UPPER170 Register

1 GIC500_GICD_IROUTER_UPPER170 Register (Offset = 6554h) [reset = 0h]

GICD_IROUTER170_upper

Return to Summary Table

Table 14-18409. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6554h**

Figure 14-6107. GIC500_GICD_IROUTER_UPPER170 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18411. GIC500_GICD_IROUTER_UPPER170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.515 GIC500_GICD_IROUTER_LOWER171 Register

1 GIC500_GICD_IROUTER_LOWER171 Register (Offset = 6558h) [reset = 0h]

GICD_IROUTER171_lower

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Table 14-18412. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6558h**

Figure 14-6108. GIC500_GICD_IROUTER_LOWER171 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER171_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER171_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER171_LOWER__0_8							
R/W							
0h							

Table 14-18414. GIC500_GICD_IROUTER_LOWER171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER171_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER171_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER171_LOWER__0_8	R/W	0h	A0

14.4.1.2.516 GIC500_GICD_IROUTER_UPPER171 Register

1 GIC500_GICD_IROUTER_UPPER171 Register (Offset = 655Ch) [reset = 0h]

GICD_IROUTER171_upper

Return to Summary Table

Table 14-18415. Instance Table

Instance Name	Physical Address
GICSS0	**0180 655Ch**

Figure 14-6109. GIC500_GICD_IROUTER_UPPER171 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18417. GIC500_GICD_IROUTER_UPPER171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.517 GIC500_GICD_IROUTER_LOWER172 Register

1 GIC500_GICD_IROUTER_LOWER172 Register (Offset = 6560h) [reset = 0h]

GICD_IROUTER172_lower

Return to Summary Table

Table 14-18418. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6560h**

Figure 14-6110. GIC500_GICD_IROUTER_LOWER172 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER172_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER172_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER172_LOWER__0_8							
R/W							
0h							

Table 14-18420. GIC500_GICD_IROUTER_LOWER172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER172_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER172_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER172_LOWER__0_8	R/W	0h	A0

14.4.1.2.518 GIC500_GICD_IROUTER_UPPER172 Register

1 GIC500_GICD_IROUTER_UPPER172 Register (Offset = 6564h) [reset = 0h]

GICD_IROUTER172_upper

Return to Summary Table

Table 14-18421. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6564h**

Figure 14-6111. GIC500_GICD_IROUTER_UPPER172 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18423. GIC500_GICD_IROUTER_UPPER172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.519 GIC500_GICD_IROUTER_LOWER173 Register

1 GIC500_GICD_IROUTER_LOWER173 Register (Offset = 6568h) [reset = 0h]

GICD_IROUTER173_lower

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Table 14-18424. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6568h**

Figure 14-6112. GIC500_GICD_IROUTER_LOWER173 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER173_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER173_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER173_LOWER__0_8							
R/W							
0h							

Table 14-18426. GIC500_GICD_IROUTER_LOWER173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER173_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER173_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER173_LOWER__0_8	R/W	0h	A0

14.4.1.2.520 GIC500_GICD_IROUTER_UPPER173 Register

1 GIC500_GICD_IROUTER_UPPER173 Register (Offset = 656Ch) [reset = 0h]

GICD_IROUTER173_upper

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Table 14-18427. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 656Ch**

Figure 14-6113. GIC500_GICD_IROUTER_UPPER173 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18429. GIC500_GICD_IROUTER_UPPER173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.521 GIC500_GICD_IROUTER_LOWER174 Register

1 GIC500_GICD_IROUTER_LOWER174 Register (Offset = 6570h) [reset = 0h]

GICD_IROUTER174_lower

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Table 14-18430. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6570h**

Figure 14-6114. GIC500_GICD_IROUTER_LOWER174 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER174_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER174_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER174_LOWER__0_8							
R/W							
0h							

Table 14-18432. GIC500_GICD_IROUTER_LOWER174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER174_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER174_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER174_LOWER__0_8	R/W	0h	A0

14.4.1.2.522 GIC500_GICD_IROUTER_UPPER174 Register

1 GIC500_GICD_IROUTER_UPPER174 Register (Offset = 6574h) [reset = 0h]

GICD_IROUTER174_upper

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Table 14-18433. Instance Table

Instance Name	Physical Address
GICSS0	0180 6574h

Figure 14-6115. GIC500_GICD_IROUTER_UPPER174 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18435. GIC500_GICD_IROUTER_UPPER174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.523 GIC500_GICD_IROUTER_LOWER175 Register

1 GIC500_GICD_IROUTER_LOWER175 Register (Offset = 6578h) [reset = 0h]

GICD_IROUTER175_lower

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Table 14-18436. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6578h**

Figure 14-6116. GIC500_GICD_IROUTER_LOWER175 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER175_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER175_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER175_LOWER__0_8							
R/W							
0h							

Table 14-18438. GIC500_GICD_IROUTER_LOWER175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER175_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER175_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER175_LOWER__0_8	R/W	0h	A0

14.4.1.2.524 GIC500_GICD_IROUTER_UPPER175 Register

1 GIC500_GICD_IROUTER_UPPER175 Register (Offset = 657Ch) [reset = 0h]

GICD_IROUTER175_upper

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Table 14-18439. Instance Table

Instance Name	Physical Address
GICSS0	**0180 657Ch**

Figure 14-6117. GIC500_GICD_IROUTER_UPPER175 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18441. GIC500_GICD_IROUTER_UPPER175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.525 GIC500_GICD_IROUTER_LOWER176 Register

1 GIC500_GICD_IROUTER_LOWER176 Register (Offset = 6580h) [reset = 0h]

GICD_IROUTER176_lower

Return to Summary Table

Table 14-18442. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6580h**

Figure 14-6118. GIC500_GICD_IROUTER_LOWER176 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER176_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER176_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER176_LOWER__0_8							
R/W							
0h							

Table 14-18444. GIC500_GICD_IROUTER_LOWER176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER176_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER176_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER176_LOWER__0_8	R/W	0h	A0

14.4.1.2.526 GIC500_GICD_IROUTER_UPPER176 Register

1 GIC500_GICD_IROUTER_UPPER176 Register (Offset = 6584h) [reset = 0h]

GICD_IROUTER176_upper

Return to Summary Table

Table 14-18445. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6584h**

Figure 14-6119. GIC500_GICD_IROUTER_UPPER176 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18447. GIC500_GICD_IROUTER_UPPER176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.527 GIC500_GICD_IROUTER_LOWER177 Register

1 GIC500_GICD_IROUTER_LOWER177 Register (Offset = 6588h) [reset = 0h]

GICD_IROUTER177_lower

Return to Summary Table

Table 14-18448. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6588h**

Figure 14-6120. GIC500_GICD_IROUTER_LOWER177 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER177_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER177_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER177_LOWER__0_8							
R/W							
0h							

Table 14-18450. GIC500_GICD_IROUTER_LOWER177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER177_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER177_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER177_LOWER__0_8	R/W	0h	A0

14.4.1.2.528 GIC500_GICD_IROUTER_UPPER177 Register

1 GIC500_GICD_IROUTER_UPPER177 Register (Offset = 658Ch) [reset = 0h]

GICD_IROUTER177_upper

Return to Summary Table

Table 14-18451. Instance Table

Instance Name	Physical Address
GICSS0	**0180 658Ch**

Figure 14-6121. GIC500_GICD_IROUTER_UPPER177 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18453. GIC500_GICD_IROUTER_UPPER177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.529 GIC500_GICD_IROUTER_LOWER178 Register

1 GIC500_GICD_IROUTER_LOWER178 Register (Offset = 6590h) [reset = 0h]

GICD_IROUTER178_lower

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Table 14-18454. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6590h**

Figure 14-6122. GIC500_GICD_IROUTER_LOWER178 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER178_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER178_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER178_LOWER__0_8							
R/W							
0h							

Table 14-18456. GIC500_GICD_IROUTER_LOWER178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER178_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER178_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER178_LOWER__0_8	R/W	0h	A0

14.4.1.2.530 GIC500_GICD_IROUTER_UPPER178 Register

1 GIC500_GICD_IROUTER_UPPER178 Register (Offset = 6594h) [reset = 0h]

GICD_IROUTER178_upper

Return to Summary Table

Table 14-18457. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6594h**

Figure 14-6123. GIC500_GICD_IROUTER_UPPER178 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18459. GIC500_GICD_IROUTER_UPPER178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.531 GIC500_GICD_IROUTER_LOWER179 Register

1 GIC500_GICD_IROUTER_LOWER179 Register (Offset = 6598h) [reset = 0h]

GICD_IROUTER179_lower

Return to Summary Table

Table 14-18460. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6598h**

Figure 14-6124. GIC500_GICD_IROUTER_LOWER179 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER179_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER179_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER179_LOWER__0_8							
R/W							
0h							

Table 14-18462. GIC500_GICD_IROUTER_LOWER179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER179_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER179_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER179_LOWER__0_8	R/W	0h	A0

14.4.1.2.532 GIC500_GICD_IROUTER_UPPER179 Register

1 GIC500_GICD_IROUTER_UPPER179 Register (Offset = 659Ch) [reset = 0h]

GICD_IROUTER179_upper

Return to Summary Table

Table 14-18463. Instance Table

Instance Name	Physical Address
GICSS0	**0180 659Ch**

Figure 14-6125. GIC500_GICD_IROUTER_UPPER179 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18465. GIC500_GICD_IROUTER_UPPER179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.533 GIC500_GICD_IROUTER_LOWER180 Register

1 GIC500_GICD_IROUTER_LOWER180 Register (Offset = 65A0h) [reset = 0h]

GICD_IROUTER180_lower

Return to Summary Table

Table 14-18466. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65A0h**

Figure 14-6126. GIC500_GICD_IROUTER_LOWER180 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER180_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER180_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER180_LOWER__0_8							
R/W							
0h							

Table 14-18468. GIC500_GICD_IROUTER_LOWER180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER180_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER180_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER180_LOWER__0_8	R/W	0h	A0

14.4.1.2.534 GIC500_GICD_IROUTER_UPPER180 Register

1 GIC500_GICD_IROUTER_UPPER180 Register (Offset = 65A4h) [reset = 0h]

GICD_IROUTER180_upper

Return to Summary Table

Table 14-18469. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65A4h**

Figure 14-6127. GIC500_GICD_IROUTER_UPPER180 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18471. GIC500_GICD_IROUTER_UPPER180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.535 GIC500_GICD_IROUTER_LOWER181 Register

1 GIC500_GICD_IROUTER_LOWER181 Register (Offset = 65A8h) [reset = 0h]

GICD_IROUTER181_lower

Return to Summary Table

Table 14-18472. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65A8h**

Figure 14-6128. GIC500_GICD_IROUTER_LOWER181 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER181_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER181_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER181_LOWER__0_8							
R/W							
0h							

Table 14-18474. GIC500_GICD_IROUTER_LOWER181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER181_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER181_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER181_LOWER__0_8	R/W	0h	A0

14.4.1.2.536 GIC500_GICD_IROUTER_UPPER181 Register

1 GIC500_GICD_IROUTER_UPPER181 Register (Offset = 65ACh) [reset = 0h]

GICD_IROUTER181_upper

Return to Summary Table

Table 14-18475. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65ACh**

Figure 14-6129. GIC500_GICD_IROUTER_UPPER181 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18477. GIC500_GICD_IROUTER_UPPER181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.537 GIC500_GICD_IROUTER_LOWER182 Register

1 GIC500_GICD_IROUTER_LOWER182 Register (Offset = 65B0h) [reset = 0h]

GICD_IROUTER182_lower

Return to Summary Table

Table 14-18478. Instance Table

Instance Name	Physical Address
GICSS0	0180 65B0h

Figure 14-6130. GIC500_GICD_IROUTER_LOWER182 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER182_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER182_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER182_LOWER__0_8							
R/W							
0h							

Table 14-18480. GIC500_GICD_IROUTER_LOWER182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER182_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER182_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER182_LOWER__0_8	R/W	0h	A0

14.4.1.2.538 GIC500_GICD_IROUTER_UPPER182 Register

1 GIC500_GICD_IROUTER_UPPER182 Register (Offset = 65B4h) [reset = 0h]

GICD_IROUTER182_upper

Return to Summary Table

Table 14-18481. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65B4h**

Figure 14-6131. GIC500_GICD_IROUTER_UPPER182 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18483. GIC500_GICD_IROUTER_UPPER182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.539 GIC500_GICD_IROUTER_LOWER183 Register

1 GIC500_GICD_IROUTER_LOWER183 Register (Offset = 65B8h) [reset = 0h]

GICD_IROUTER183_lower

Return to Summary Table

Table 14-18484. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65B8h**

Figure 14-6132. GIC500_GICD_IROUTER_LOWER183 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER183_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER183_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER183_LOWER__0_8							
R/W							
0h							

Table 14-18486. GIC500_GICD_IROUTER_LOWER183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER183_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER183_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER183_LOWER__0_8	R/W	0h	A0

14.4.1.2.540 GIC500_GICD_IROUTER_UPPER183 Register

1 GIC500_GICD_IROUTER_UPPER183 Register (Offset = 65BCh) [reset = 0h]

GICD_IROUTER183_upper

Return to Summary Table

Table 14-18487. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65BCh**

Figure 14-6133. GIC500_GICD_IROUTER_UPPER183 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18489. GIC500_GICD_IROUTER_UPPER183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.541 GIC500_GICD_IROUTER_LOWER184 Register

1 GIC500_GICD_IROUTER_LOWER184 Register (Offset = 65C0h) [reset = 0h]

GICD_IROUTER184_lower

Return to Summary Table

Table 14-18490. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65C0h**

Figure 14-6134. GIC500_GICD_IROUTER_LOWER184 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER184_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER184_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER184_LOWER__0_8							
R/W							
0h							

Table 14-18492. GIC500_GICD_IROUTER_LOWER184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER184_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER184_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER184_LOWER__0_8	R/W	0h	A0

14.4.1.2.542 GIC500_GICD_IROUTER_UPPER184 Register

1 GIC500_GICD_IROUTER_UPPER184 Register (Offset = 65C4h) [reset = 0h]

GICD_IROUTER184_upper

Return to Summary Table

Table 14-18493. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65C4h**

Figure 14-6135. GIC500_GICD_IROUTER_UPPER184 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18495. GIC500_GICD_IROUTER_UPPER184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.543 GIC500_GICD_IROUTER_LOWER185 Register

1 GIC500_GICD_IROUTER_LOWER185 Register (Offset = 65C8h) [reset = 0h]

GICD_IROUTER185_lower

Return to Summary Table

Table 14-18496. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65C8h**

Figure 14-6136. GIC500_GICD_IROUTER_LOWER185 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER185_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER185_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER185_LOWER__0_8							
R/W							
0h							

Table 14-18498. GIC500_GICD_IROUTER_LOWER185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER185_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER185_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER185_LOWER__0_8	R/W	0h	A0

14.4.1.2.544 GIC500_GICD_IROUTER_UPPER185 Register

1 GIC500_GICD_IROUTER_UPPER185 Register (Offset = 65CCh) [reset = 0h]

GICD_IROUTER185_upper

Return to Summary Table

Table 14-18499. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65CCh**

Figure 14-6137. GIC500_GICD_IROUTER_UPPER185 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18501. GIC500_GICD_IROUTER_UPPER185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.545 GIC500_GICD_IROUTER_LOWER186 Register

1 GIC500_GICD_IROUTER_LOWER186 Register (Offset = 65D0h) [reset = 0h]

GICD_IROUTER186_lower

Return to Summary Table

Table 14-18502. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65D0h**

Figure 14-6138. GIC500_GICD_IROUTER_LOWER186 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER186_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER186_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER186_LOWER__0_8							
R/W							
0h							

Table 14-18504. GIC500_GICD_IROUTER_LOWER186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER186_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER186_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER186_LOWER__0_8	R/W	0h	A0

14.4.1.2.546 GIC500_GICD_IROUTER_UPPER186 Register

1 GIC500_GICD_IROUTER_UPPER186 Register (Offset = 65D4h) [reset = 0h]

GICD_IROUTER186_upper

Return to Summary Table

Table 14-18505. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65D4h**

Figure 14-6139. GIC500_GICD_IROUTER_UPPER186 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18507. GIC500_GICD_IROUTER_UPPER186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.547 GIC500_GICD_IROUTER_LOWER187 Register

1 GIC500_GICD_IROUTER_LOWER187 Register (Offset = 65D8h) [reset = 0h]

GICD_IROUTER187_lower

Return to Summary Table

Table 14-18508. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65D8h**

Figure 14-6140. GIC500_GICD_IROUTER_LOWER187 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER187_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER187_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER187_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18510. GIC500_GICD_IROUTER_LOWER187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER187_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER187_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER187_LOWER__0_8	R/W	0h	A0

14.4.1.2.548 GIC500_GICD_IROUTER_UPPER187 Register

1 GIC500_GICD_IROUTER_UPPER187 Register (Offset = 65DCh) [reset = 0h]

GICD_IROUTER187_upper

Return to Summary Table

Table 14-18511. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65DCh**

Figure 14-6141. GIC500_GICD_IROUTER_UPPER187 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18513. GIC500_GICD_IROUTER_UPPER187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.549 GIC500_GICD_IROUTER_LOWER188 Register

1 GIC500_GICD_IROUTER_LOWER188 Register (Offset = 65E0h) [reset = 0h]

GICD_IROUTER188_lower

Return to Summary Table

Table 14-18514. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65E0h**

Figure 14-6142. GIC500_GICD_IROUTER_LOWER188 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER188_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER188_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER188_LOWER__0_8							
R/W							
0h							

Table 14-18516. GIC500_GICD_IROUTER_LOWER188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER188_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER188_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER188_LOWER__0_8	R/W	0h	A0

14.4.1.2.550 GIC500_GICD_IROUTER_UPPER188 Register

1 GIC500_GICD_IROUTER_UPPER188 Register (Offset = 65E4h) [reset = 0h]

GICD_IROUTER188_upper

Return to Summary Table

Table 14-18517. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65E4h**

Figure 14-6143. GIC500_GICD_IROUTER_UPPER188 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18519. GIC500_GICD_IROUTER_UPPER188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.551 GIC500_GICD_IROUTER_LOWER189 Register

1 GIC500_GICD_IROUTER_LOWER189 Register (Offset = 65E8h) [reset = 0h]

GICD_IROUTER189_lower

Return to Summary Table

Table 14-18520. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65E8h**

Figure 14-6144. GIC500_GICD_IROUTER_LOWER189 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER189_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER189_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER189_LOWER__0_8							
R/W							
0h							

Table 14-18522. GIC500_GICD_IROUTER_LOWER189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER189_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER189_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER189_LOWER__0_8	R/W	0h	A0

14.4.1.2.552 GIC500_GICD_IROUTER_UPPER189 Register

1 GIC500_GICD_IROUTER_UPPER189 Register (Offset = 65ECh) [reset = 0h]

GICD_IROUTER189_upper

Return to Summary Table

Table 14-18523. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65ECh**

Figure 14-6145. GIC500_GICD_IROUTER_UPPER189 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18525. GIC500_GICD_IROUTER_UPPER189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.553 GIC500_GICD_IROUTER_LOWER190 Register

1 GIC500_GICD_IROUTER_LOWER190 Register (Offset = 65F0h) [reset = 0h]

GICD_IROUTER190_lower

Return to Summary Table

Table 14-18526. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65F0h**

Figure 14-6146. GIC500_GICD_IROUTER_LOWER190 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER190_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER190_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER190_LOWER__0_8							
R/W							
0h							

Table 14-18528. GIC500_GICD_IROUTER_LOWER190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER190_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER190_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER190_LOWER__0_8	R/W	0h	A0

14.4.1.2.554 GIC500_GICD_IROUTER_UPPER190 Register

1 GIC500_GICD_IROUTER_UPPER190 Register (Offset = 65F4h) [reset = 0h]

GICD_IROUTER190_upper

Return to Summary Table

Table 14-18529. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65F4h**

Figure 14-6147. GIC500_GICD_IROUTER_UPPER190 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18531. GIC500_GICD_IROUTER_UPPER190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.555 GIC500_GICD_IROUTER_LOWER191 Register

1 GIC500_GICD_IROUTER_LOWER191 Register (Offset = 65F8h) [reset = 0h]

GICD_IROUTER191_lower

Return to Summary Table

Table 14-18532. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65F8h**

Figure 14-6148. GIC500_GICD_IROUTER_LOWER191 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER191_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER191_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER191_LOWER__0_8							
R/W							
0h							

Table 14-18534. GIC500_GICD_IROUTER_LOWER191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER191_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER191_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER191_LOWER__0_8	R/W	0h	A0

14.4.1.2.556 GIC500_GICD_IROUTER_UPPER191 Register

1 GIC500_GICD_IROUTER_UPPER191 Register (Offset = 65FCh) [reset = 0h]

GICD_IROUTER191_upper

Return to Summary Table

Table 14-18535. Instance Table

Instance Name	Physical Address
GICSS0	**0180 65FCh**

Figure 14-6149. GIC500_GICD_IROUTER_UPPER191 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18537. GIC500_GICD_IROUTER_UPPER191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.557 GIC500_GICD_IROUTER_LOWER192 Register

1 GIC500_GICD_IROUTER_LOWER192 Register (Offset = 6600h) [reset = 0h]

GICD_IROUTER192_lower

Return to Summary Table

Table 14-18538. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6600h**

Figure 14-6150. GIC500_GICD_IROUTER_LOWER192 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER192_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER192_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER192_LOWER__0_8							
R/W							
0h							

Table 14-18540. GIC500_GICD_IROUTER_LOWER192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER192_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER192_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER192_LOWER__0_8	R/W	0h	A0

14.4.1.2.558 GIC500_GICD_IROUTER_UPPER192 Register

1 GIC500_GICD_IROUTER_UPPER192 Register (Offset = 6604h) [reset = 0h]

GICD_IROUTER192_upper

Return to Summary Table

Table 14-18541. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6604h**

Figure 14-6151. GIC500_GICD_IROUTER_UPPER192 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18543. GIC500_GICD_IROUTER_UPPER192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.559 GIC500_GICD_IROUTER_LOWER193 Register

1 GIC500_GICD_IROUTER_LOWER193 Register (Offset = 6608h) [reset = 0h]

GICD_IROUTER193_lower

Return to Summary Table

Table 14-18544. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6608h**

Figure 14-6152. GIC500_GICD_IROUTER_LOWER193 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER193_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER193_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER193_LOWER__0_8							
R/W							
0h							

Table 14-18546. GIC500_GICD_IROUTER_LOWER193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER193_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER193_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER193_LOWER__0_8	R/W	0h	A0

14.4.1.2.560 GIC500_GICD_IROUTER_UPPER193 Register

1 GIC500_GICD_IROUTER_UPPER193 Register (Offset = 660Ch) [reset = 0h]

GICD_IROUTER193_upper

Return to Summary Table

Table 14-18547. Instance Table

Instance Name	Physical Address
GICSS0	**0180 660Ch**

Figure 14-6153. GIC500_GICD_IROUTER_UPPER193 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18549. GIC500_GICD_IROUTER_UPPER193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.561 GIC500_GICD_IROUTER_LOWER194 Register

1 GIC500_GICD_IROUTER_LOWER194 Register (Offset = 6610h) [reset = 0h]

GICD_IROUTER194_lower

Return to Summary Table

Table 14-18550. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6610h**

Figure 14-6154. GIC500_GICD_IROUTER_LOWER194 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER194_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER194_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER194_LOWER__0_8							
R/W							
0h							

Table 14-18552. GIC500_GICD_IROUTER_LOWER194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER194_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER194_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER194_LOWER__0_8	R/W	0h	A0

14.4.1.2.562 GIC500_GICD_IROUTER_UPPER194 Register

1 GIC500_GICD_IROUTER_UPPER194 Register (Offset = 6614h) [reset = 0h]

GICD_IROUTER194_upper

Return to Summary Table

Table 14-18553. Instance Table

Instance Name	Physical Address
GICSS0	0180 6614h

Figure 14-6155. GIC500_GICD_IROUTER_UPPER194 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18555. GIC500_GICD_IROUTER_UPPER194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.563 GIC500_GICD_IROUTER_LOWER195 Register

1 GIC500_GICD_IROUTER_LOWER195 Register (Offset = 6618h) [reset = 0h]

GICD_IROUTER195_lower

Return to Summary Table

Table 14-18556. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6618h**

Figure 14-6156. GIC500_GICD_IROUTER_LOWER195 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER195_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER195_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER195_LOWER__0_8							
R/W							
0h							

Table 14-18558. GIC500_GICD_IROUTER_LOWER195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER195_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER195_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER195_LOWER__0_8	R/W	0h	A0

14.4.1.2.564 GIC500_GICD_IROUTER_UPPER195 Register

1 GIC500_GICD_IROUTER_UPPER195 Register (Offset = 661Ch) [reset = 0h]

GICD_IROUTER195_upper

Return to Summary Table

Table 14-18559. Instance Table

Instance Name	Physical Address
GICSS0	**0180 661Ch**

Figure 14-6157. GIC500_GICD_IROUTER_UPPER195 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18561. GIC500_GICD_IROUTER_UPPER195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.565 GIC500_GICD_IROUTER_LOWER196 Register

1 GIC500_GICD_IROUTER_LOWER196 Register (Offset = 6620h) [reset = 0h]

GICD_IROUTER196_lower

Return to Summary Table

Table 14-18562. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6620h**

Figure 14-6158. GIC500_GICD_IROUTER_LOWER196 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER196_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER196_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER196_LOWER__0_8							
R/W							
0h							

Table 14-18564. GIC500_GICD_IROUTER_LOWER196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER196_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER196_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER196_LOWER__0_8	R/W	0h	A0

14.4.1.2.566 GIC500_GICD_IROUTER_UPPER196 Register

1 GIC500_GICD_IROUTER_UPPER196 Register (Offset = 6624h) [reset = 0h]

GICD_IROUTER196_upper

Return to Summary Table

Table 14-18565. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6624h**

Figure 14-6159. GIC500_GICD_IROUTER_UPPER196 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18567. GIC500_GICD_IROUTER_UPPER196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.567 GIC500_GICD_IROUTER_LOWER197 Register

1 GIC500_GICD_IROUTER_LOWER197 Register (Offset = 6628h) [reset = 0h]

GICD_IROUTER197_lower

Return to Summary Table

Table 14-18568. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6628h**

Figure 14-6160. GIC500_GICD_IROUTER_LOWER197 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER197_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER197_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER197_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18570. GIC500_GICD_IROUTER_LOWER197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER197_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER197_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER197_LOWER__0_8	R/W	0h	A0

14.4.1.2.568 GIC500_GICD_IROUTER_UPPER197 Register

1 GIC500_GICD_IROUTER_UPPER197 Register (Offset = 662Ch) [reset = 0h]

GICD_IROUTER197_upper

Return to Summary Table

Table 14-18571. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 662Ch**

Figure 14-6161. GIC500_GICD_IROUTER_UPPER197 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18573. GIC500_GICD_IROUTER_UPPER197 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.569 GIC500_GICD_IROUTER_LOWER198 Register

1 GIC500_GICD_IROUTER_LOWER198 Register (Offset = 6630h) [reset = 0h]

GICD_IROUTER198_lower

Return to Summary Table

Table 14-18574. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6630h**

Figure 14-6162. GIC500_GICD_IROUTER_LOWER198 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER198_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER198_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER198_LOWER__0_8							
R/W							
0h							

Table 14-18576. GIC500_GICD_IROUTER_LOWER198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER198_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER198_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER198_LOWER__0_8	R/W	0h	A0

14.4.1.2.570 GIC500_GICD_IROUTER_UPPER198 Register

1 GIC500_GICD_IROUTER_UPPER198 Register (Offset = 6634h) [reset = 0h]

GICD_IROUTER198_upper

Return to Summary Table

Table 14-18577. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6634h**

Figure 14-6163. GIC500_GICD_IROUTER_UPPER198 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18579. GIC500_GICD_IROUTER_UPPER198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.571 GIC500_GICD_IROUTER_LOWER199 Register

1 GIC500_GICD_IROUTER_LOWER199 Register (Offset = 6638h) [reset = 0h]

GICD_IROUTER199_lower

Return to Summary Table

Table 14-18580. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6638h**

Figure 14-6164. GIC500_GICD_IROUTER_LOWER199 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER199_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER199_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER199_LOWER__0_8							
R/W							
0h							

Table 14-18582. GIC500_GICD_IROUTER_LOWER199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER199_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER199_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER199_LOWER__0_8	R/W	0h	A0

14.4.1.2.572 GIC500_GICD_IROUTER_UPPER199 Register

1 GIC500_GICD_IROUTER_UPPER199 Register (Offset = 663Ch) [reset = 0h]

GICD_IROUTER199_upper

Return to Summary Table

Table 14-18583. Instance Table

Instance Name	Physical Address
GICSS0	**0180 663Ch**

Figure 14-6165. GIC500_GICD_IROUTER_UPPER199 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18585. GIC500_GICD_IROUTER_UPPER199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.573 GIC500_GICD_IROUTER_LOWER200 Register

1 GIC500_GICD_IROUTER_LOWER200 Register (Offset = 6640h) [reset = 0h]

GICD_IROUTER200_lower

Return to Summary Table

Table 14-18586. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6640h**

Figure 14-6166. GIC500_GICD_IROUTER_LOWER200 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER200_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER200_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER200_LOWER__0_8							
R/W							
0h							

Table 14-18588. GIC500_GICD_IROUTER_LOWER200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER200_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER200_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER200_LOWER__0_8	R/W	0h	A0

14.4.1.2.574 GIC500_GICD_IROUTER_UPPER200 Register

1 GIC500_GICD_IROUTER_UPPER200 Register (Offset = 6644h) [reset = 0h]

GICD_IROUTER200_upper

Return to Summary Table

Table 14-18589. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6644h**

Figure 14-6167. GIC500_GICD_IROUTER_UPPER200 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18591. GIC500_GICD_IROUTER_UPPER200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.575 GIC500_GICD_IROUTER_LOWER201 Register

1 GIC500_GICD_IROUTER_LOWER201 Register (Offset = 6648h) [reset = 0h]

GICD_IROUTER201_lower

Return to Summary Table

Table 14-18592. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6648h**

Figure 14-6168. GIC500_GICD_IROUTER_LOWER201 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER201_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER201_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER201_LOWER__0_8							
R/W							
0h							

Table 14-18594. GIC500_GICD_IROUTER_LOWER201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER201_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER201_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER201_LOWER__0_8	R/W	0h	A0

14.4.1.2.576 GIC500_GICD_IROUTER_UPPER201 Register

1 GIC500_GICD_IROUTER_UPPER201 Register (Offset = 664Ch) [reset = 0h]

GICD_IROUTER201_upper

Return to Summary Table

Table 14-18595. Instance Table

Instance Name	Physical Address
GICSS0	**0180 664Ch**

Figure 14-6169. GIC500_GICD_IROUTER_UPPER201 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18597. GIC500_GICD_IROUTER_UPPER201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.577 GIC500_GICD_IROUTER_LOWER202 Register

1 GIC500_GICD_IROUTER_LOWER202 Register (Offset = 6650h) [reset = 0h]

GICD_IROUTER202_lower

Return to Summary Table

Table 14-18598. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6650h**

Figure 14-6170. GIC500_GICD_IROUTER_LOWER202 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER202_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER202_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER202_LOWER__0_8							
R/W							
0h							

Table 14-18600. GIC500_GICD_IROUTER_LOWER202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER202_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER202_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER202_LOWER__0_8	R/W	0h	A0

14.4.1.2.578 GIC500_GICD_IROUTER_UPPER202 Register

1 GIC500_GICD_IROUTER_UPPER202 Register (Offset = 6654h) [reset = 0h]

GICD_IROUTER202_upper

Return to Summary Table

Table 14-18601. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6654h**

Figure 14-6171. GIC500_GICD_IROUTER_UPPER202 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18603. GIC500_GICD_IROUTER_UPPER202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.579 GIC500_GICD_IROUTER_LOWER203 Register

1 GIC500_GICD_IROUTER_LOWER203 Register (Offset = 6658h) [reset = 0h]

GICD_IROUTER203_lower

Return to Summary Table

Table 14-18604. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6658h**

Figure 14-6172. GIC500_GICD_IROUTER_LOWER203 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER203_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER203_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER203_LOWER__0_8							
R/W							
0h							

Table 14-18606. GIC500_GICD_IROUTER_LOWER203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER203_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER203_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER203_LOWER__0_8	R/W	0h	A0

14.4.1.2.580 GIC500_GICD_IROUTER_UPPER203 Register

1 GIC500_GICD_IROUTER_UPPER203 Register (Offset = 665Ch) [reset = 0h]

GICD_IROUTER203_upper

Return to Summary Table

Table 14-18607. Instance Table

Instance Name	Physical Address
GICSS0	0180 665Ch

Figure 14-6173. GIC500_GICD_IROUTER_UPPER203 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18609. GIC500_GICD_IROUTER_UPPER203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.581 GIC500_GICD_IROUTER_LOWER204 Register

1 GIC500_GICD_IROUTER_LOWER204 Register (Offset = 6660h) [reset = 0h]

GICD_IROUTER204_lower

Return to Summary Table

Table 14-18610. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6660h**

Figure 14-6174. GIC500_GICD_IROUTER_LOWER204 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER204_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER204_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER204_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18612. GIC500_GICD_IROUTER_LOWER204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER204_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER204_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER204_LOWER__0_8	R/W	0h	A0

14.4.1.2.582 GIC500_GICD_IROUTER_UPPER204 Register

1 GIC500_GICD_IROUTER_UPPER204 Register (Offset = 6664h) [reset = 0h]

GICD_IROUTER204_upper

Return to Summary Table

Table 14-18613. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6664h**

Figure 14-6175. GIC500_GICD_IROUTER_UPPER204 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18615. GIC500_GICD_IROUTER_UPPER204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.583 GIC500_GICD_IROUTER_LOWER205 Register

1 GIC500_GICD_IROUTER_LOWER205 Register (Offset = 6668h) [reset = 0h]

GICD_IROUTER205_lower

Return to Summary Table

Table 14-18616. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6668h**

Figure 14-6176. GIC500_GICD_IROUTER_LOWER205 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER205_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER205_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER205_LOWER__0_8							
R/W							
0h							

Table 14-18618. GIC500_GICD_IROUTER_LOWER205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER205_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER205_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER205_LOWER__0_8	R/W	0h	A0

14.4.1.2.584 GIC500_GICD_IROUTER_UPPER205 Register

1 GIC500_GICD_IROUTER_UPPER205 Register (Offset = 666Ch) [reset = 0h]

GICD_IROUTER205_upper

Return to Summary Table

Table 14-18619. Instance Table

Instance Name	Physical Address
GICSS0	**0180 666Ch**

Figure 14-6177. GIC500_GICD_IROUTER_UPPER205 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18621. GIC500_GICD_IROUTER_UPPER205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.585 GIC500_GICD_IROUTER_LOWER206 Register

1 GIC500_GICD_IROUTER_LOWER206 Register (Offset = 6670h) [reset = 0h]

GICD_IROUTER206_lower

Return to Summary Table

Table 14-18622. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6670h**

Figure 14-6178. GIC500_GICD_IROUTER_LOWER206 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER206_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER206_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER206_LOWER__0_8							
R/W							
0h							

Table 14-18624. GIC500_GICD_IROUTER_LOWER206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER206_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER206_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER206_LOWER__0_8	R/W	0h	A0

14.4.1.2.586 GIC500_GICD_IROUTER_UPPER206 Register

1 GIC500_GICD_IROUTER_UPPER206 Register (Offset = 6674h) [reset = 0h]

GICD_IROUTER206_upper

Return to Summary Table

Table 14-18625. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6674h**

Figure 14-6179. GIC500_GICD_IROUTER_UPPER206 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18627. GIC500_GICD_IROUTER_UPPER206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.587 GIC500_GICD_IROUTER_LOWER207 Register

1 GIC500_GICD_IROUTER_LOWER207 Register (Offset = 6678h) [reset = 0h]

GICD_IROUTER207_lower

Return to Summary Table

Table 14-18628. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6678h**

Figure 14-6180. GIC500_GICD_IROUTER_LOWER207 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER207_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER207_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER207_LOWER__0_8							
R/W							
0h							

Table 14-18630. GIC500_GICD_IROUTER_LOWER207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER207_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER207_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER207_LOWER__0_8	R/W	0h	A0

14.4.1.2.588 GIC500_GICD_IROUTER_UPPER207 Register

1 GIC500_GICD_IROUTER_UPPER207 Register (Offset = 667Ch) [reset = 0h]

GICD_IROUTER207_upper

Return to Summary Table

Table 14-18631. Instance Table

Instance Name	Physical Address
GICSS0	**0180 667Ch**

Figure 14-6181. GIC500_GICD_IROUTER_UPPER207 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18633. GIC500_GICD_IROUTER_UPPER207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.589 GIC500_GICD_IROUTER_LOWER208 Register

1 GIC500_GICD_IROUTER_LOWER208 Register (Offset = 6680h) [reset = 0h]

GICD_IROUTER208_lower

Return to Summary Table

Table 14-18634. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6680h**

Figure 14-6182. GIC500_GICD_IROUTER_LOWER208 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER208_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER208_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER208_LOWER__0_8							
R/W							
0h							

Table 14-18636. GIC500_GICD_IROUTER_LOWER208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER208_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER208_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER208_LOWER__0_8	R/W	0h	A0

14.4.1.2.590 GIC500_GICD_IROUTER_UPPER208 Register

1 GIC500_GICD_IROUTER_UPPER208 Register (Offset = 6684h) [reset = 0h]

GICD_IROUTER208_upper

Return to Summary Table

Table 14-18637. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6684h**

Figure 14-6183. GIC500_GICD_IROUTER_UPPER208 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18639. GIC500_GICD_IROUTER_UPPER208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.591 GIC500_GICD_IROUTER_LOWER209 Register

1 GIC500_GICD_IROUTER_LOWER209 Register (Offset = 6688h) [reset = 0h]

GICD_IROUTER209_lower

Return to Summary Table

Table 14-18640. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6688h**

Figure 14-6184. GIC500_GICD_IROUTER_LOWER209 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER209_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER209_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER209_LOWER__0_8							
R/W							
0h							

Table 14-18642. GIC500_GICD_IROUTER_LOWER209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER209_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER209_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER209_LOWER__0_8	R/W	0h	A0

14.4.1.2.592 GIC500_GICD_IROUTER_UPPER209 Register

1 GIC500_GICD_IROUTER_UPPER209 Register (Offset = 668Ch) [reset = 0h]

GICD_IROUTER209_upper

Return to Summary Table

Table 14-18643. Instance Table

Instance Name	Physical Address
GICSS0	**0180 668Ch**

Figure 14-6185. GIC500_GICD_IROUTER_UPPER209 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18645. GIC500_GICD_IROUTER_UPPER209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.593 GIC500_GICD_IROUTER_LOWER210 Register

1 GIC500_GICD_IROUTER_LOWER210 Register (Offset = 6690h) [reset = 0h]

GICD_IROUTER210_lower

Return to Summary Table

Table 14-18646. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6690h**

Figure 14-6186. GIC500_GICD_IROUTER_LOWER210 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER210_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER210_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER210_LOWER__0_8							
R/W							
0h							

Table 14-18648. GIC500_GICD_IROUTER_LOWER210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER210_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER210_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER210_LOWER__0_8	R/W	0h	A0

14.4.1.2.594 GIC500_GICD_IROUTER_UPPER210 Register

1 GIC500_GICD_IROUTER_UPPER210 Register (Offset = 6694h) [reset = 0h]

GICD_IROUTER210_upper

Return to Summary Table

Table 14-18649. Instance Table

Instance Name	Physical Address
GICSS0	0180 6694h

Figure 14-6187. GIC500_GICD_IROUTER_UPPER210 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18651. GIC500_GICD_IROUTER_UPPER210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.595 GIC500_GICD_IROUTER_LOWER211 Register

1 GIC500_GICD_IROUTER_LOWER211 Register (Offset = 6698h) [reset = 0h]

GICD_IROUTER211_lower

Return to Summary Table

Table 14-18652. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6698h**

Figure 14-6188. GIC500_GICD_IROUTER_LOWER211 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER211_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER211_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER211_LOWER__0_8							
R/W							
0h							

Table 14-18654. GIC500_GICD_IROUTER_LOWER211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER211_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER211_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER211_LOWER__0_8	R/W	0h	A0

14.4.1.2.596 GIC500_GICD_IROUTER_UPPER211 Register

1 GIC500_GICD_IROUTER_UPPER211 Register (Offset = 669Ch) [reset = 0h]

GICD_IROUTER211_upper

Return to Summary Table

Table 14-18655. Instance Table

Instance Name	Physical Address
GICSS0	**0180 669Ch**

Figure 14-6189. GIC500_GICD_IROUTER_UPPER211 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18657. GIC500_GICD_IROUTER_UPPER211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.597 GIC500_GICD_IROUTER_LOWER212 Register

1 GIC500_GICD_IROUTER_LOWER212 Register (Offset = 66A0h) [reset = 0h]

GICD_IROUTER212_lower

Return to Summary Table

Table 14-18658. Instance Table

Instance Name	Physical Address
GICSS0	0180 66A0h

Figure 14-6190. GIC500_GICD_IROUTER_LOWER212 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER212_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER212_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER212_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18660. GIC500_GICD_IROUTER_LOWER212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER212_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER212_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER212_LOWER__0_8	R/W	0h	A0

14.4.1.2.598 GIC500_GICD_IROUTER_UPPER212 Register

1 GIC500_GICD_IROUTER_UPPER212 Register (Offset = 66A4h) [reset = 0h]

GICD_IROUTER212_upper

Return to Summary Table

Table 14-18661. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66A4h**

Figure 14-6191. GIC500_GICD_IROUTER_UPPER212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18663. GIC500_GICD_IROUTER_UPPER212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.599 GIC500_GICD_IROUTER_LOWER213 Register

1 GIC500_GICD_IROUTER_LOWER213 Register (Offset = 66A8h) [reset = 0h]

GICD_IROUTER213_lower

Return to Summary Table

Table 14-18664. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66A8h**

Figure 14-6192. GIC500_GICD_IROUTER_LOWER213 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER213_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER213_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER213_LOWER__0_8							
R/W							
0h							

Table 14-18666. GIC500_GICD_IROUTER_LOWER213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER213_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER213_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER213_LOWER__0_8	R/W	0h	A0

14.4.1.2.600 GIC500_GICD_IROUTER_UPPER213 Register

1 GIC500_GICD_IROUTER_UPPER213 Register (Offset = 66ACh) [reset = 0h]

GICD_IROUTER213_upper

Return to Summary Table

Table 14-18667. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66ACh**

Figure 14-6193. GIC500_GICD_IROUTER_UPPER213 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18669. GIC500_GICD_IROUTER_UPPER213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.601 GIC500_GICD_IROUTER_LOWER214 Register

1 GIC500_GICD_IROUTER_LOWER214 Register (Offset = 66B0h) [reset = 0h]

GICD_IROUTER214_lower

Return to Summary Table

Table 14-18670. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66B0h**

Figure 14-6194. GIC500_GICD_IROUTER_LOWER214 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER214_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER214_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER214_LOWER__0_8							
R/W							
0h							

Table 14-18672. GIC500_GICD_IROUTER_LOWER214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER214_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER214_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER214_LOWER__0_8	R/W	0h	A0

14.4.1.2.602 GIC500_GICD_IROUTER_UPPER214 Register

1 GIC500_GICD_IROUTER_UPPER214 Register (Offset = 66B4h) [reset = 0h]

GICD_IROUTER214_upper

Return to Summary Table

Table 14-18673. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66B4h**

Figure 14-6195. GIC500_GICD_IROUTER_UPPER214 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18675. GIC500_GICD_IROUTER_UPPER214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.603 GIC500_GICD_IROUTER_LOWER215 Register

1 GIC500_GICD_IROUTER_LOWER215 Register (Offset = 66B8h) [reset = 0h]

GICD_IROUTER215_lower

Return to Summary Table

Table 14-18676. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66B8h**

Figure 14-6196. GIC500_GICD_IROUTER_LOWER215 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER215_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER215_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER215_LOWER__0_8							
R/W							
0h							

Table 14-18678. GIC500_GICD_IROUTER_LOWER215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER215_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER215_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER215_LOWER__0_8	R/W	0h	A0

14.4.1.2.604 GIC500_GICD_IROUTER_UPPER215 Register

1 GIC500_GICD_IROUTER_UPPER215 Register (Offset = 66BCh) [reset = 0h]

GICD_IROUTER215_upper

Return to Summary Table

Table 14-18679. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66BCh**

Figure 14-6197. GIC500_GICD_IROUTER_UPPER215 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18681. GIC500_GICD_IROUTER_UPPER215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.605 GIC500_GICD_IROUTER_LOWER216 Register

1 GIC500_GICD_IROUTER_LOWER216 Register (Offset = 66C0h) [reset = 0h]

GICD_IROUTER216_lower

Return to Summary Table

Table 14-18682. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66C0h**

Figure 14-6198. GIC500_GICD_IROUTER_LOWER216 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER216_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER216_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER216_LOWER__0_8							
R/W							
0h							

Table 14-18684. GIC500_GICD_IROUTER_LOWER216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER216_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER216_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER216_LOWER__0_8	R/W	0h	A0

14.4.1.2.606 GIC500_GICD_IROUTER_UPPER216 Register

1 GIC500_GICD_IROUTER_UPPER216 Register (Offset = 66C4h) [reset = 0h]

GICD_IROUTER216_upper

Return to Summary Table

Table 14-18685. Instance Table

Instance Name	Physical Address
GICSS0	0180 66C4h

Figure 14-6199. GIC500_GICD_IROUTER_UPPER216 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18687. GIC500_GICD_IROUTER_UPPER216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.607 GIC500_GICD_IROUTER_LOWER217 Register

1 GIC500_GICD_IROUTER_LOWER217 Register (Offset = 66C8h) [reset = 0h]

GICD_IROUTER217_lower

Return to Summary Table

Table 14-18688. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66C8h**

Figure 14-6200. GIC500_GICD_IROUTER_LOWER217 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER217_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER217_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER217_LOWER__0_8							
R/W							
0h							

Table 14-18690. GIC500_GICD_IROUTER_LOWER217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER217_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER217_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER217_LOWER__0_8	R/W	0h	A0

14.4.1.2.608 GIC500_GICD_IROUTER_UPPER217 Register

1 GIC500_GICD_IROUTER_UPPER217 Register (Offset = 66CCh) [reset = 0h]

GICD_IROUTER217_upper

Return to Summary Table

Table 14-18691. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66CCh**

Figure 14-6201. GIC500_GICD_IROUTER_UPPER217 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18693. GIC500_GICD_IROUTER_UPPER217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.609 GIC500_GICD_IROUTER_LOWER218 Register

1 GIC500_GICD_IROUTER_LOWER218 Register (Offset = 66D0h) [reset = 0h]

GICD_IROUTER218_lower

Return to Summary Table

Table 14-18694. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66D0h**

Figure 14-6202. GIC500_GICD_IROUTER_LOWER218 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER218_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER218_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER218_LOWER__0_8							
R/W							
0h							

Table 14-18696. GIC500_GICD_IROUTER_LOWER218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER218_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER218_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER218_LOWER__0_8	R/W	0h	A0

14.4.1.2.610 GIC500_GICD_IROUTER_UPPER218 Register

1 GIC500_GICD_IROUTER_UPPER218 Register (Offset = 66D4h) [reset = 0h]

GICD_IROUTER218_upper

Return to Summary Table

Table 14-18697. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66D4h**

Figure 14-6203. GIC500_GICD_IROUTER_UPPER218 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18699. GIC500_GICD_IROUTER_UPPER218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.611 GIC500_GICD_IROUTER_LOWER219 Register

1 GIC500_GICD_IROUTER_LOWER219 Register (Offset = 66D8h) [reset = 0h]

GICD_IROUTER219_lower

Return to Summary Table

Table 14-18700. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66D8h**

Figure 14-6204. GIC500_GICD_IROUTER_LOWER219 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER219_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER219_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER219_LOWER__0_8							
R/W							
0h							

Table 14-18702. GIC500_GICD_IROUTER_LOWER219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER219_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER219_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER219_LOWER__0_8	R/W	0h	A0

14.4.1.2.612 GIC500_GICD_IROUTER_UPPER219 Register

1 GIC500_GICD_IROUTER_UPPER219 Register (Offset = 66DCh) [reset = 0h]

GICD_IROUTER219_upper

Return to Summary Table

Table 14-18703. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66DCh**

Figure 14-6205. GIC500_GICD_IROUTER_UPPER219 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18705. GIC500_GICD_IROUTER_UPPER219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.613 GIC500_GICD_IROUTER_LOWER220 Register

1 GIC500_GICD_IROUTER_LOWER220 Register (Offset = 66E0h) [reset = 0h]

GICD_IROUTER220_lower

Return to Summary Table

Table 14-18706. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66E0h**

Figure 14-6206. GIC500_GICD_IROUTER_LOWER220 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER220_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER220_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER220_LOWER__0_8							
R/W							
0h							

Table 14-18708. GIC500_GICD_IROUTER_LOWER220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER220_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER220_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER220_LOWER__0_8	R/W	0h	A0

14.4.1.2.614 GIC500_GICD_IROUTER_UPPER220 Register

1 GIC500_GICD_IROUTER_UPPER220 Register (Offset = 66E4h) [reset = 0h]

GICD_IROUTER220_upper

Return to Summary Table

Table 14-18709. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66E4h**

Figure 14-6207. GIC500_GICD_IROUTER_UPPER220 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18711. GIC500_GICD_IROUTER_UPPER220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.615 GIC500_GICD_IROUTER_LOWER221 Register

1 GIC500_GICD_IROUTER_LOWER221 Register (Offset = 66E8h) [reset = 0h]

GICD_IROUTER221_lower

Return to Summary Table

Table 14-18712. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 66E8h**

Figure 14-6208. GIC500_GICD_IROUTER_LOWER221 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER221_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER221_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER221_LOWER__0_8							
R/W							
0h							

Table 14-18714. GIC500_GICD_IROUTER_LOWER221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER221_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER221_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER221_LOWER__0_8	R/W	0h	A0

14.4.1.2.616 GIC500_GICD_IROUTER_UPPER221 Register

1 GIC500_GICD_IROUTER_UPPER221 Register (Offset = 66ECh) [reset = 0h]

GICD_IROUTER221_upper

Return to Summary Table

Table 14-18715. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66ECh**

Figure 14-6209. GIC500_GICD_IROUTER_UPPER221 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18717. GIC500_GICD_IROUTER_UPPER221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.617 GIC500_GICD_IROUTER_LOWER222 Register

1 GIC500_GICD_IROUTER_LOWER222 Register (Offset = 66F0h) [reset = 0h]

GICD_IROUTER222_lower

Return to Summary Table

Table 14-18718. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66F0h**

Figure 14-6210. GIC500_GICD_IROUTER_LOWER222 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER222_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER222_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER222_LOWER__0_8							
R/W							
0h							

Table 14-18720. GIC500_GICD_IROUTER_LOWER222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER222_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER222_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER222_LOWER__0_8	R/W	0h	A0

14.4.1.2.618 GIC500_GICD_IROUTER_UPPER222 Register

1 GIC500_GICD_IROUTER_UPPER222 Register (Offset = 66F4h) [reset = 0h]

GICD_IROUTER222_upper

Return to Summary Table

Table 14-18721. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66F4h**

Figure 14-6211. GIC500_GICD_IROUTER_UPPER222 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18723. GIC500_GICD_IROUTER_UPPER222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.619 GIC500_GICD_IROUTER_LOWER223 Register

1 GIC500_GICD_IROUTER_LOWER223 Register (Offset = 66F8h) [reset = 0h]

GICD_IROUTER223_lower

Return to Summary Table

Table 14-18724. Instance Table

Instance Name	Physical Address
GICSS0	0180 66F8h

Figure 14-6212. GIC500_GICD_IROUTER_LOWER223 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER223_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER223_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER223_LOWER__0_8							
R/W							
0h							

Table 14-18726. GIC500_GICD_IROUTER_LOWER223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER223_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER223_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER223_LOWER__0_8	R/W	0h	A0

14.4.1.2.620 GIC500_GICD_IROUTER_UPPER223 Register

1 GIC500_GICD_IROUTER_UPPER223 Register (Offset = 66FCh) [reset = 0h]

GICD_IROUTER223_upper

Return to Summary Table

Table 14-18727. Instance Table

Instance Name	Physical Address
GICSS0	**0180 66FCh**

Figure 14-6213. GIC500_GICD_IROUTER_UPPER223 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18729. GIC500_GICD_IROUTER_UPPER223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.621 GIC500_GICD_IROUTER_LOWER224 Register

1 GIC500_GICD_IROUTER_LOWER224 Register (Offset = 6700h) [reset = 0h]

GICD_IROUTER224_lower

Return to Summary Table

Table 14-18730. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6700h**

Figure 14-6214. GIC500_GICD_IROUTER_LOWER224 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER224_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER224_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER224_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18732. GIC500_GICD_IROUTER_LOWER224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER224_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER224_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER224_LOWER__0_8	R/W	0h	A0

14.4.1.2.622 GIC500_GICD_IROUTER_UPPER224 Register

1 GIC500_GICD_IROUTER_UPPER224 Register (Offset = 6704h) [reset = 0h]

GICD_IROUTER224_upper

Return to Summary Table

Table 14-18733. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6704h**

Figure 14-6215. GIC500_GICD_IROUTER_UPPER224 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18735. GIC500_GICD_IROUTER_UPPER224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.623 GIC500_GICD_IROUTER_LOWER225 Register

1 GIC500_GICD_IROUTER_LOWER225 Register (Offset = 6708h) [reset = 0h]

GICD_IROUTER225_lower

Return to Summary Table

Table 14-18736. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6708h**

Figure 14-6216. GIC500_GICD_IROUTER_LOWER225 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER225_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER225_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER225_LOWER__0_8							
R/W							
0h							

Table 14-18738. GIC500_GICD_IROUTER_LOWER225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER225_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER225_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER225_LOWER__0_8	R/W	0h	A0

14.4.1.2.624 GIC500_GICD_IROUTER_UPPER225 Register

1 GIC500_GICD_IROUTER_UPPER225 Register (Offset = 670Ch) [reset = 0h]

GICD_IROUTER225_upper

Return to Summary Table

Table 14-18739. Instance Table

Instance Name	Physical Address
GICSS0	0180 670Ch

Figure 14-6217. GIC500_GICD_IROUTER_UPPER225 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18741. GIC500_GICD_IROUTER_UPPER225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.625 GIC500_GICD_IROUTER_LOWER226 Register

1 GIC500_GICD_IROUTER_LOWER226 Register (Offset = 6710h) [reset = 0h]

GICD_IROUTER226_lower

Return to Summary Table

Table 14-18742. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6710h**

Figure 14-6218. GIC500_GICD_IROUTER_LOWER226 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER226_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER226_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER226_LOWER__0_8							
R/W							
0h							

Table 14-18744. GIC500_GICD_IROUTER_LOWER226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER226_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER226_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER226_LOWER__0_8	R/W	0h	A0

14.4.1.2.626 GIC500_GICD_IROUTER_UPPER226 Register

1 GIC500_GICD_IROUTER_UPPER226 Register (Offset = 6714h) [reset = 0h]

GICD_IROUTER226_upper

Return to Summary Table

Table 14-18745. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 6714h**

Figure 14-6219. GIC500_GICD_IROUTER_UPPER226 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18747. GIC500_GICD_IROUTER_UPPER226 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.627 GIC500_GICD_IROUTER_LOWER227 Register

1 GIC500_GICD_IROUTER_LOWER227 Register (Offset = 6718h) [reset = 0h]

GICD_IROUTER227_lower

Return to Summary Table

Table 14-18748. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6718h**

Figure 14-6220. GIC500_GICD_IROUTER_LOWER227 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER227_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER227_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER227_LOWER__0_8							
R/W							
0h							

Table 14-18750. GIC500_GICD_IROUTER_LOWER227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER227_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER227_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER227_LOWER__0_8	R/W	0h	A0

14.4.1.2.628 GIC500_GICD_IROUTER_UPPER227 Register

1 GIC500_GICD_IROUTER_UPPER227 Register (Offset = 671Ch) [reset = 0h]

GICD_IROUTER227_upper

Return to Summary Table

Table 14-18751. Instance Table

Instance Name	Physical Address
GICSS0	**0180 671Ch**

Figure 14-6221. GIC500_GICD_IROUTER_UPPER227 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18753. GIC500_GICD_IROUTER_UPPER227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.629 GIC500_GICD_IROUTER_LOWER228 Register

1 GIC500_GICD_IROUTER_LOWER228 Register (Offset = 6720h) [reset = 0h]

GICD_IROUTER228_lower

Return to Summary Table

Table 14-18754. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6720h**

Figure 14-6222. GIC500_GICD_IROUTER_LOWER228 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER228_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER228_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER228_LOWER__0_8							
R/W							
0h							

Table 14-18756. GIC500_GICD_IROUTER_LOWER228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER228_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER228_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER228_LOWER__0_8	R/W	0h	A0

14.4.1.2.630 GIC500_GICD_IROUTER_UPPER228 Register

1 GIC500_GICD_IROUTER_UPPER228 Register (Offset = 6724h) [reset = 0h]

GICD_IROUTER228_upper

Return to Summary Table

Table 14-18757. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6724h**

Figure 14-6223. GIC500_GICD_IROUTER_UPPER228 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18759. GIC500_GICD_IROUTER_UPPER228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.631 GIC500_GICD_IROUTER_LOWER229 Register

1 GIC500_GICD_IROUTER_LOWER229 Register (Offset = 6728h) [reset = 0h]

GICD_IROUTER229_lower

Return to Summary Table

Table 14-18760. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6728h**

Figure 14-6224. GIC500_GICD_IROUTER_LOWER229 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER229_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER229_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER229_LOWER__0_8							
R/W							
0h							

Table 14-18762. GIC500_GICD_IROUTER_LOWER229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER229_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER229_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER229_LOWER__0_8	R/W	0h	A0

14.4.1.2.632 GIC500_GICD_IROUTER_UPPER229 Register

1 GIC500_GICD_IROUTER_UPPER229 Register (Offset = 672Ch) [reset = 0h]

GICD_IROUTER229_upper

Return to Summary Table

Table 14-18763. Instance Table

Instance Name	Physical Address
GICSS0	**0180 672Ch**

Figure 14-6225. GIC500_GICD_IROUTER_UPPER229 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18765. GIC500_GICD_IROUTER_UPPER229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.633 GIC500_GICD_IROUTER_LOWER230 Register

1 GIC500_GICD_IROUTER_LOWER230 Register (Offset = 6730h) [reset = 0h]

GICD_IROUTER230_lower

Return to Summary Table

Table 14-18766. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6730h**

Figure 14-6226. GIC500_GICD_IROUTER_LOWER230 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER230_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER230_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER230_LOWER__0_8							
R/W							
0h							

Table 14-18768. GIC500_GICD_IROUTER_LOWER230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER230_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER230_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER230_LOWER__0_8	R/W	0h	A0

14.4.1.2.634 GIC500_GICD_IROUTER_UPPER230 Register

1 GIC500_GICD_IROUTER_UPPER230 Register (Offset = 6734h) [reset = 0h]

GICD_IROUTER230_upper

Return to Summary Table

Table 14-18769. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6734h**

Figure 14-6227. GIC500_GICD_IROUTER_UPPER230 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18771. GIC500_GICD_IROUTER_UPPER230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.635 GIC500_GICD_IROUTER_LOWER231 Register

1 GIC500_GICD_IROUTER_LOWER231 Register (Offset = 6738h) [reset = 0h]

GICD_IROUTER231_lower

Return to Summary Table

Table 14-18772. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6738h**

Figure 14-6228. GIC500_GICD_IROUTER_LOWER231 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER231_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER231_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER231_LOWER__0_8							
R/W							
0h							

Table 14-18774. GIC500_GICD_IROUTER_LOWER231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER231_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER231_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER231_LOWER__0_8	R/W	0h	A0

14.4.1.2.636 GIC500_GICD_IROUTER_UPPER231 Register

1 GIC500_GICD_IROUTER_UPPER231 Register (Offset = 673Ch) [reset = 0h]

GICD_IROUTER231_upper

Return to Summary Table

Table 14-18775. Instance Table

Instance Name	Physical Address
GICSS0	**0180 673Ch**

Figure 14-6229. GIC500_GICD_IROUTER_UPPER231 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-18777. GIC500_GICD_IROUTER_UPPER231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.637 GIC500_GICD_IROUTER_LOWER232 Register

1 GIC500_GICD_IROUTER_LOWER232 Register (Offset = 6740h) [reset = 0h]

GICD_IROUTER232_lower

Return to Summary Table

Table 14-18778. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6740h**

Figure 14-6230. GIC500_GICD_IROUTER_LOWER232 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER232_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER232_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER232_LOWER__0_8							
R/W							
0h							

Table 14-18780. GIC500_GICD_IROUTER_LOWER232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER232_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER232_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER232_LOWER__0_8	R/W	0h	A0

14.4.1.2.638 GIC500_GICD_IROUTER_UPPER232 Register

1 GIC500_GICD_IROUTER_UPPER232 Register (Offset = 6744h) [reset = 0h]

GICD_IROUTER232_upper

Return to Summary Table

Table 14-18781. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6744h**

Figure 14-6231. GIC500_GICD_IROUTER_UPPER232 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18783. GIC500_GICD_IROUTER_UPPER232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.639 GIC500_GICD_IROUTER_LOWER233 Register

1 GIC500_GICD_IROUTER_LOWER233 Register (Offset = 6748h) [reset = 0h]

GICD_IROUTER233_lower

Return to Summary Table

Table 14-18784. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6748h**

Figure 14-6232. GIC500_GICD_IROUTER_LOWER233 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER233_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER233_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER233_LOWER__0_8							
R/W							
0h							

Table 14-18786. GIC500_GICD_IROUTER_LOWER233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER233_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER233_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER233_LOWER__0_8	R/W	0h	A0

14.4.1.2.640 GIC500_GICD_IROUTER_UPPER233 Register

1 GIC500_GICD_IROUTER_UPPER233 Register (Offset = 674Ch) [reset = 0h]

GICD_IROUTER233_upper

Return to Summary Table

Table 14-18787. Instance Table

Instance Name	Physical Address
GICSS0	0180 674Ch

Figure 14-6233. GIC500_GICD_IROUTER_UPPER233 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18789. GIC500_GICD_IROUTER_UPPER233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.641 GIC500_GICD_IROUTER_LOWER234 Register

1 GIC500_GICD_IROUTER_LOWER234 Register (Offset = 6750h) [reset = 0h]

GICD_IROUTER234_lower

Return to Summary Table

Table 14-18790. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6750h**

Figure 14-6234. GIC500_GICD_IROUTER_LOWER234 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER234_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER234_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER234_LOWER__0_8							
R/W							
0h							

Table 14-18792. GIC500_GICD_IROUTER_LOWER234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER234_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER234_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER234_LOWER__0_8	R/W	0h	A0

14.4.1.2.642 GIC500_GICD_IROUTER_UPPER234 Register

1 GIC500_GICD_IROUTER_UPPER234 Register (Offset = 6754h) [reset = 0h]

GICD_IROUTER234_upper

Return to Summary Table

Table 14-18793. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6754h**

Figure 14-6235. GIC500_GICD_IROUTER_UPPER234 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18795. GIC500_GICD_IROUTER_UPPER234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.643 GIC500_GICD_IROUTER_LOWER235 Register

1 GIC500_GICD_IROUTER_LOWER235 Register (Offset = 6758h) [reset = 0h]

GICD_IROUTER235_lower

Return to Summary Table

Table 14-18796. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6758h**

Figure 14-6236. GIC500_GICD_IROUTER_LOWER235 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER235_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER235_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER235_LOWER__0_8							
R/W							
0h							

Table 14-18798. GIC500_GICD_IROUTER_LOWER235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER235_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER235_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER235_LOWER__0_8	R/W	0h	A0

14.4.1.2.644 GIC500_GICD_IROUTER_UPPER235 Register

1 GIC500_GICD_IROUTER_UPPER235 Register (Offset = 675Ch) [reset = 0h]

GICD_IROUTER235_upper

Return to Summary Table

Table 14-18799. Instance Table

Instance Name	Physical Address
GICSS0	**0180 675Ch**

Figure 14-6237. GIC500_GICD_IROUTER_UPPER235 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18801. GIC500_GICD_IROUTER_UPPER235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.645 GIC500_GICD_IROUTER_LOWER236 Register

1 GIC500_GICD_IROUTER_LOWER236 Register (Offset = 6760h) [reset = 0h]

GICD_IROUTER236_lower

Return to Summary Table

Table 14-18802. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6760h**

Figure 14-6238. GIC500_GICD_IROUTER_LOWER236 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER236_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER236_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER236_LOWER__0_8							
R/W							
0h							

Table 14-18804. GIC500_GICD_IROUTER_LOWER236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER236_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER236_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER236_LOWER__0_8	R/W	0h	A0

14.4.1.2.646 GIC500_GICD_IROUTER_UPPER236 Register

1 GIC500_GICD_IROUTER_UPPER236 Register (Offset = 6764h) [reset = 0h]

GICD_IROUTER236_upper

Return to Summary Table

Table 14-18805. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6764h**

Figure 14-6239. GIC500_GICD_IROUTER_UPPER236 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18807. GIC500_GICD_IROUTER_UPPER236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.647 GIC500_GICD_IROUTER_LOWER237 Register

1 GIC500_GICD_IROUTER_LOWER237 Register (Offset = 6768h) [reset = 0h]

GICD_IROUTER237_lower

Return to Summary Table

Table 14-18808. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6768h**

Figure 14-6240. GIC500_GICD_IROUTER_LOWER237 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER237_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER237_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER237_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18810. GIC500_GICD_IROUTER_LOWER237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER237_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER237_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER237_LOWER__0_8	R/W	0h	A0

14.4.1.2.648 GIC500_GICD_IROUTER_UPPER237 Register

1 GIC500_GICD_IROUTER_UPPER237 Register (Offset = 676Ch) [reset = 0h]

GICD_IROUTER237_upper

Return to Summary Table

Table 14-18811. Instance Table

Instance Name	Physical Address
GICSS0	**0180 676Ch**

Figure 14-6241. GIC500_GICD_IROUTER_UPPER237 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18813. GIC500_GICD_IROUTER_UPPER237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.649 GIC500_GICD_IROUTER_LOWER238 Register

1 GIC500_GICD_IROUTER_LOWER238 Register (Offset = 6770h) [reset = 0h]

GICD_IROUTER238_lower

Return to Summary Table

Table 14-18814. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6770h**

Figure 14-6242. GIC500_GICD_IROUTER_LOWER238 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER238_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER238_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER238_LOWER__0_8							
R/W							
0h							

Table 14-18816. GIC500_GICD_IROUTER_LOWER238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER238_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER238_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER238_LOWER__0_8	R/W	0h	A0

14.4.1.2.650 GIC500_GICD_IROUTER_UPPER238 Register

1 GIC500_GICD_IROUTER_UPPER238 Register (Offset = 6774h) [reset = 0h]

GICD_IROUTER238_upper

Return to Summary Table

Table 14-18817. Instance Table

Instance Name	Physical Address
GICSS0	0180 6774h

Figure 14-6243. GIC500_GICD_IROUTER_UPPER238 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18819. GIC500_GICD_IROUTER_UPPER238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.651 GIC500_GICD_IROUTER_LOWER239 Register

1 GIC500_GICD_IROUTER_LOWER239 Register (Offset = 6778h) [reset = 0h]

GICD_IROUTER239_lower

Return to Summary Table

Table 14-18820. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6778h**

Figure 14-6244. GIC500_GICD_IROUTER_LOWER239 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER239_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER239_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER239_LOWER__0_8							
R/W							
0h							

Table 14-18822. GIC500_GICD_IROUTER_LOWER239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER239_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER239_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER239_LOWER__0_8	R/W	0h	A0

14.4.1.2.652 GIC500_GICD_IROUTER_UPPER239 Register

1 GIC500_GICD_IROUTER_UPPER239 Register (Offset = 677Ch) [reset = 0h]

GICD_IROUTER239_upper

Return to Summary Table

Table 14-18823. Instance Table

Instance Name	Physical Address
GICSS0	**0180 677Ch**

Figure 14-6245. GIC500_GICD_IROUTER_UPPER239 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18825. GIC500_GICD_IROUTER_UPPER239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.653 GIC500_GICD_IROUTER_LOWER240 Register

1 GIC500_GICD_IROUTER_LOWER240 Register (Offset = 6780h) [reset = 0h]

GICD_IROUTER240_lower

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Table 14-18826. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6780h**

Figure 14-6246. GIC500_GICD_IROUTER_LOWER240 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER240_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER240_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER240_LOWER__0_8							
R/W							
0h							

Table 14-18828. GIC500_GICD_IROUTER_LOWER240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER240_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER240_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER240_LOWER__0_8	R/W	0h	A0

14.4.1.2.654 GIC500_GICD_IROUTER_UPPER240 Register

1 GIC500_GICD_IROUTER_UPPER240 Register (Offset = 6784h) [reset = 0h]

GICD_IROUTER240_upper

Return to Summary Table

Table 14-18829. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6784h**

Figure 14-6247. GIC500_GICD_IROUTER_UPPER240 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18831. GIC500_GICD_IROUTER_UPPER240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.655 GIC500_GICD_IROUTER_LOWER241 Register

1 GIC500_GICD_IROUTER_LOWER241 Register (Offset = 6788h) [reset = 0h]

GICD_IROUTER241_lower

Return to Summary Table

Table 14-18832. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6788h**

Figure 14-6248. GIC500_GICD_IROUTER_LOWER241 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER241_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER241_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER241_LOWER__0_8							
R/W							
0h							

Table 14-18834. GIC500_GICD_IROUTER_LOWER241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER241_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER241_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER241_LOWER__0_8	R/W	0h	A0

14.4.1.2.656 GIC500_GICD_IROUTER_UPPER241 Register

1 GIC500_GICD_IROUTER_UPPER241 Register (Offset = 678Ch) [reset = 0h]

GICD_IROUTER241_upper

Return to Summary Table

Table 14-18835. Instance Table

Instance Name	Physical Address
GICSS0	**0180 678Ch**

Figure 14-6249. GIC500_GICD_IROUTER_UPPER241 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18837. GIC500_GICD_IROUTER_UPPER241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.657 GIC500_GICD_IROUTER_LOWER242 Register

1 GIC500_GICD_IROUTER_LOWER242 Register (Offset = 6790h) [reset = 0h]

GICD_IROUTER242_lower

Return to Summary Table

Table 14-18838. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6790h**

Figure 14-6250. GIC500_GICD_IROUTER_LOWER242 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER242_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER242_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER242_LOWER__0_8							
R/W							
0h							

Table 14-18840. GIC500_GICD_IROUTER_LOWER242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER242_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER242_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER242_LOWER__0_8	R/W	0h	A0

14.4.1.2.658 GIC500_GICD_IROUTER_UPPER242 Register

1 GIC500_GICD_IROUTER_UPPER242 Register (Offset = 6794h) [reset = 0h]

GICD_IROUTER242_upper

Return to Summary Table

Table 14-18841. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6794h**

Figure 14-6251. GIC500_GICD_IROUTER_UPPER242 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18843. GIC500_GICD_IROUTER_UPPER242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.659 GIC500_GICD_IROUTER_LOWER243 Register

1 GIC500_GICD_IROUTER_LOWER243 Register (Offset = 6798h) [reset = 0h]

GICD_IROUTER243_lower

Return to Summary Table

Table 14-18844. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6798h**

Figure 14-6252. GIC500_GICD_IROUTER_LOWER243 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER243_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER243_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER243_LOWER__0_8							
R/W							
0h							

Table 14-18846. GIC500_GICD_IROUTER_LOWER243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER243_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER243_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER243_LOWER__0_8	R/W	0h	A0

14.4.1.2.660 GIC500_GICD_IROUTER_UPPER243 Register

1 GIC500_GICD_IROUTER_UPPER243 Register (Offset = 679Ch) [reset = 0h]

GICD_IROUTER243_upper

Return to Summary Table

Table 14-18847. Instance Table

Instance Name	Physical Address
GICSS0	**0180 679Ch**

Figure 14-6253. GIC500_GICD_IROUTER_UPPER243 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18849. GIC500_GICD_IROUTER_UPPER243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.661 GIC500_GICD_IROUTER_LOWER244 Register

1 GIC500_GICD_IROUTER_LOWER244 Register (Offset = 67A0h) [reset = 0h]

GICD_IROUTER244_lower

Return to Summary Table

Table 14-18850. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67A0h**

Figure 14-6254. GIC500_GICD_IROUTER_LOWER244 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER244_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER244_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER244_LOWER__0_8							
R/W							
0h							

Table 14-18852. GIC500_GICD_IROUTER_LOWER244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER244_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER244_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER244_LOWER__0_8	R/W	0h	A0

14.4.1.2.662 GIC500_GICD_IROUTER_UPPER244 Register

1 GIC500_GICD_IROUTER_UPPER244 Register (Offset = 67A4h) [reset = 0h]

GICD_IROUTER244_upper

Return to Summary Table

Table 14-18853. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67A4h**

Figure 14-6255. GIC500_GICD_IROUTER_UPPER244 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18855. GIC500_GICD_IROUTER_UPPER244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.663 GIC500_GICD_IROUTER_LOWER245 Register

1 GIC500_GICD_IROUTER_LOWER245 Register (Offset = 67A8h) [reset = 0h]

GICD_IROUTER245_lower

Return to Summary Table

Table 14-18856. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67A8h**

Figure 14-6256. GIC500_GICD_IROUTER_LOWER245 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER245_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER245_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER245_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18858. GIC500_GICD_IROUTER_LOWER245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER245_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER245_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER245_LOWER__0_8	R/W	0h	A0

14.4.1.2.664 GIC500_GICD_IROUTER_UPPER245 Register

1 GIC500_GICD_IROUTER_UPPER245 Register (Offset = 67ACh) [reset = 0h]

GICD_IROUTER245_upper

Return to Summary Table

Table 14-18859. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67ACh**

Figure 14-6257. GIC500_GICD_IROUTER_UPPER245 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18861. GIC500_GICD_IROUTER_UPPER245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.665 GIC500_GICD_IROUTER_LOWER246 Register

1 GIC500_GICD_IROUTER_LOWER246 Register (Offset = 67B0h) [reset = 0h]

GICD_IROUTER246_lower

Return to Summary Table

Table 14-18862. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67B0h**

Figure 14-6258. GIC500_GICD_IROUTER_LOWER246 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER246_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER246_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER246_LOWER__0_8							
R/W							
0h							

Table 14-18864. GIC500_GICD_IROUTER_LOWER246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER246_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER246_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER246_LOWER__0_8	R/W	0h	A0

14.4.1.2.666 GIC500_GICD_IROUTER_UPPER246 Register

1 GIC500_GICD_IROUTER_UPPER246 Register (Offset = 67B4h) [reset = 0h]

GICD_IROUTER246_upper

Return to Summary Table

Table 14-18865. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 67B4h**

Figure 14-6259. GIC500_GICD_IROUTER_UPPER246 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18867. GIC500_GICD_IROUTER_UPPER246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.667 GIC500_GICD_IROUTER_LOWER247 Register

1 GIC500_GICD_IROUTER_LOWER247 Register (Offset = 67B8h) [reset = 0h]

GICD_IROUTER247_lower

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Table 14-18868. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67B8h**

Figure 14-6260. GIC500_GICD_IROUTER_LOWER247 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER247_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER247_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER247_LOWER__0_8							
R/W							
0h							

Table 14-18870. GIC500_GICD_IROUTER_LOWER247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER247_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER247_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER247_LOWER__0_8	R/W	0h	A0

14.4.1.2.668 GIC500_GICD_IROUTER_UPPER247 Register

1 GIC500_GICD_IROUTER_UPPER247 Register (Offset = 67BCh) [reset = 0h]

GICD_IROUTER247_upper

Return to Summary Table

Table 14-18871. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67BCh**

Figure 14-6261. GIC500_GICD_IROUTER_UPPER247 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18873. GIC500_GICD_IROUTER_UPPER247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.669 GIC500_GICD_IROUTER_LOWER248 Register

1 GIC500_GICD_IROUTER_LOWER248 Register (Offset = 67C0h) [reset = 0h]

GICD_IROUTER248_lower

Return to Summary Table

Table 14-18874. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67C0h**

Figure 14-6262. GIC500_GICD_IROUTER_LOWER248 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER248_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER248_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER248_LOWER__0_8							
R/W							
0h							

Table 14-18876. GIC500_GICD_IROUTER_LOWER248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER248_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER248_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER248_LOWER__0_8	R/W	0h	A0

14.4.1.2.670 GIC500_GICD_IROUTER_UPPER248 Register

1 GIC500_GICD_IROUTER_UPPER248 Register (Offset = 67C4h) [reset = 0h]

GICD_IROUTER248_upper

Return to Summary Table

Table 14-18877. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67C4h**

Figure 14-6263. GIC500_GICD_IROUTER_UPPER248 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18879. GIC500_GICD_IROUTER_UPPER248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.671 GIC500_GICD_IROUTER_LOWER249 Register

1 GIC500_GICD_IROUTER_LOWER249 Register (Offset = 67C8h) [reset = 0h]

GICD_IROUTER249_lower

Return to Summary Table

Table 14-18880. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67C8h**

Figure 14-6264. GIC500_GICD_IROUTER_LOWER249 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER249_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER249_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER249_LOWER__0_8							
R/W							
0h							

Table 14-18882. GIC500_GICD_IROUTER_LOWER249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER249_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER249_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER249_LOWER__0_8	R/W	0h	A0

14.4.1.2.672 GIC500_GICD_IROUTER_UPPER249 Register

1 GIC500_GICD_IROUTER_UPPER249 Register (Offset = 67CCh) [reset = 0h]

GICD_IROUTER249_upper

Return to Summary Table

Table 14-18883. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67CCh**

Figure 14-6265. GIC500_GICD_IROUTER_UPPER249 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18885. GIC500_GICD_IROUTER_UPPER249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.673 GIC500_GICD_IROUTER_LOWER250 Register

1 GIC500_GICD_IROUTER_LOWER250 Register (Offset = 67D0h) [reset = 0h]

GICD_IROUTER250_lower

Return to Summary Table

Table 14-18886. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67D0h**

Figure 14-6266. GIC500_GICD_IROUTER_LOWER250 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER250_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER250_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER250_LOWER__0_8							
R/W							
0h							

Table 14-18888. GIC500_GICD_IROUTER_LOWER250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER250_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER250_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER250_LOWER__0_8	R/W	0h	A0

14.4.1.2.674 GIC500_GICD_IROUTER_UPPER250 Register

1 GIC500_GICD_IROUTER_UPPER250 Register (Offset = 67D4h) [reset = 0h]

GICD_IROUTER250_upper

Return to Summary Table

Table 14-18889. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67D4h**

Figure 14-6267. GIC500_GICD_IROUTER_UPPER250 Name Register

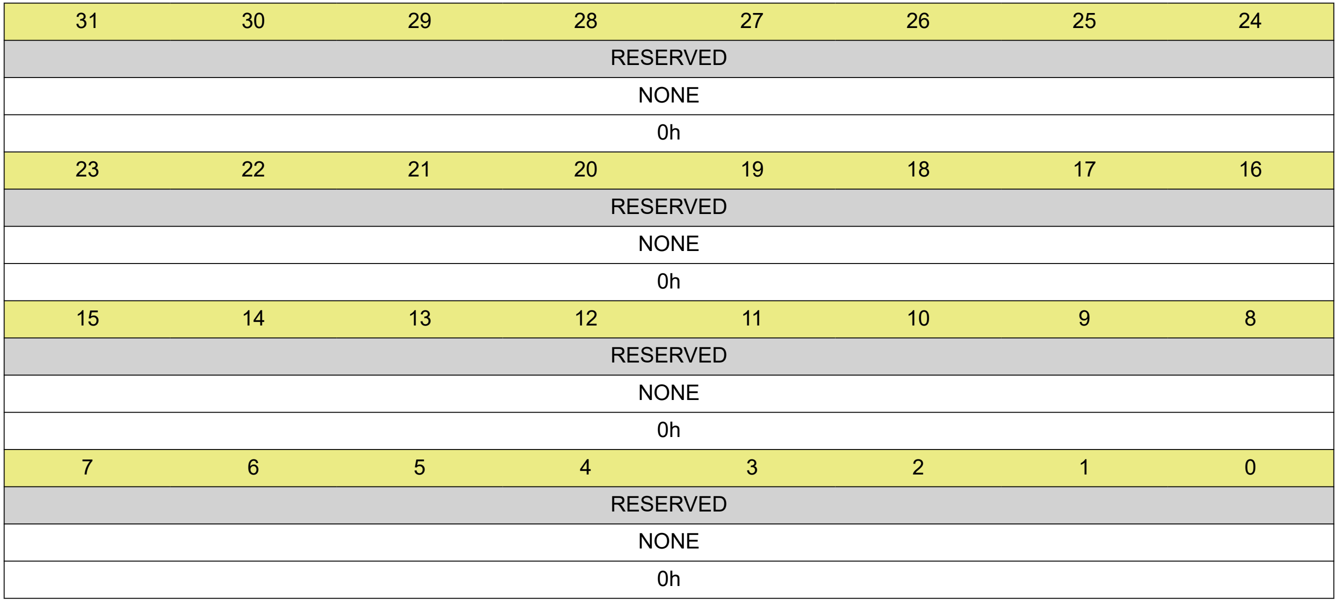

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18891. GIC500_GICD_IROUTER_UPPER250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.675 GIC500_GICD_IROUTER_LOWER251 Register

1 GIC500_GICD_IROUTER_LOWER251 Register (Offset = 67D8h) [reset = 0h]

GICD_IROUTER251_lower

Return to Summary Table

Table 14-18892. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67D8h**

Figure 14-6268. GIC500_GICD_IROUTER_LOWER251 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER251_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER251_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER251_LOWER__0_8							
R/W							
0h							

Table 14-18894. GIC500_GICD_IROUTER_LOWER251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER251_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER251_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER251_LOWER__0_8	R/W	0h	A0

14.4.1.2.676 GIC500_GICD_IROUTER_UPPER251 Register

1 GIC500_GICD_IROUTER_UPPER251 Register (Offset = 67DCh) [reset = 0h]

GICD_IROUTER251_upper

Return to Summary Table

Table 14-18895. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67DCh**

Figure 14-6269. GIC500_GICD_IROUTER_UPPER251 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18897. GIC500_GICD_IROUTER_UPPER251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.677 GIC500_GICD_IROUTER_LOWER252 Register

1 GIC500_GICD_IROUTER_LOWER252 Register (Offset = 67E0h) [reset = 0h]

GICD_IROUTER252_lower

Return to Summary Table

Table 14-18898. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67E0h**

Figure 14-6270. GIC500_GICD_IROUTER_LOWER252 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER252_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER252_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER252_LOWER__0_8							
R/W							
0h							

Table 14-18900. GIC500_GICD_IROUTER_LOWER252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER252_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER252_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER252_LOWER__0_8	R/W	0h	A0

14.4.1.2.678 GIC500_GICD_IROUTER_UPPER252 Register

1 GIC500_GICD_IROUTER_UPPER252 Register (Offset = 67E4h) [reset = 0h]

GICD_IROUTER252_upper

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Table 14-18901. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67E4h**

Figure 14-6271. GIC500_GICD_IROUTER_UPPER252 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18903. GIC500_GICD_IROUTER_UPPER252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.679 GIC500_GICD_IROUTER_LOWER253 Register

1 GIC500_GICD_IROUTER_LOWER253 Register (Offset = 67E8h) [reset = 0h]

GICD_IROUTER253_lower

Return to Summary Table

Table 14-18904. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67E8h**

Figure 14-6272. GIC500_GICD_IROUTER_LOWER253 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER253_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER253_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER253_LOWER__0_8							
R/W							
0h							

Table 14-18906. GIC500_GICD_IROUTER_LOWER253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER253_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER253_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER253_LOWER__0_8	R/W	0h	A0

14.4.1.2.680 GIC500_GICD_IROUTER_UPPER253 Register

1 GIC500_GICD_IROUTER_UPPER253 Register (Offset = 67ECh) [reset = 0h]

GICD_IROUTER253_upper

Return to Summary Table

Table 14-18907. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67ECh**

Figure 14-6273. GIC500_GICD_IROUTER_UPPER253 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18909. GIC500_GICD_IROUTER_UPPER253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.681 GIC500_GICD_IROUTER_LOWER254 Register

1 GIC500_GICD_IROUTER_LOWER254 Register (Offset = 67F0h) [reset = 0h]

GICD_IROUTER254_lower

Return to Summary Table

Table 14-18910. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67F0h**

Figure 14-6274. GIC500_GICD_IROUTER_LOWER254 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER254_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER254_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER254_LOWER__0_8							
R/W							
0h							

Table 14-18912. GIC500_GICD_IROUTER_LOWER254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER254_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER254_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER254_LOWER__0_8	R/W	0h	A0

14.4.1.2.682 GIC500_GICD_IROUTER_UPPER254 Register

1 GIC500_GICD_IROUTER_UPPER254 Register (Offset = 67F4h) [reset = 0h]

GICD_IROUTER254_upper

Return to Summary Table

Table 14-18913. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67F4h**

Figure 14-6275. GIC500_GICD_IROUTER_UPPER254 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18915. GIC500_GICD_IROUTER_UPPER254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.683 GIC500_GICD_IROUTER_LOWER255 Register

1 GIC500_GICD_IROUTER_LOWER255 Register (Offset = 67F8h) [reset = 0h]

GICD_IROUTER255_lower

Return to Summary Table

Table 14-18916. Instance Table

Instance Name	Physical Address
GICSS0	**0180 67F8h**

Figure 14-6276. GIC500_GICD_IROUTER_LOWER255 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER255_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER255_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER255_LOWER__0_8							
R/W							
0h							

Table 14-18918. GIC500_GICD_IROUTER_LOWER255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER255_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER255_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER255_LOWER__0_8	R/W	0h	A0

14.4.1.2.684 GIC500_GICD_IROUTER_UPPER255 Register

1 GIC500_GICD_IROUTER_UPPER255 Register (Offset = 67FCh) [reset = 0h]

GICD_IROUTER255_upper

Return to Summary Table

Table 14-18919. Instance Table

Instance Name	Physical Address
GICSS0	0180 67FCh

Figure 14-6277. GIC500_GICD_IROUTER_UPPER255 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18921. GIC500_GICD_IROUTER_UPPER255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.685 GIC500_GICD_IROUTER_LOWER256 Register

1 GIC500_GICD_IROUTER_LOWER256 Register (Offset = 6800h) [reset = 0h]

GICD_IROUTER256_lower

Return to Summary Table

Table 14-18922. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6800h**

Figure 14-6278. GIC500_GICD_IROUTER_LOWER256 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER256_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER256_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER256_LOWER__0_8							
R/W							
0h							

Table 14-18924. GIC500_GICD_IROUTER_LOWER256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER256_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER256_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER256_LOWER__0_8	R/W	0h	A0

14.4.1.2.686 GIC500_GICD_IROUTER_UPPER256 Register

1 GIC500_GICD_IROUTER_UPPER256 Register (Offset = 6804h) [reset = 0h]

GICD_IROUTER256_upper

Return to Summary Table

Table 14-18925. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6804h**

Figure 14-6279. GIC500_GICD_IROUTER_UPPER256 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18927. GIC500_GICD_IROUTER_UPPER256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.687 GIC500_GICD_IROUTER_LOWER257 Register

1 GIC500_GICD_IROUTER_LOWER257 Register (Offset = 6808h) [reset = 0h]

GICD_IROUTER257_lower

Return to Summary Table

Table 14-18928. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6808h**

Figure 14-6280. GIC500_GICD_IROUTER_LOWER257 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER257_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER257_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER257_LOWER__0_8							
R/W							
0h							

Table 14-18930. GIC500_GICD_IROUTER_LOWER257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER257_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER257_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER257_LOWER__0_8	R/W	0h	A0

14.4.1.2.688 GIC500_GICD_IROUTER_UPPER257 Register

1 GIC500_GICD_IROUTER_UPPER257 Register (Offset = 680Ch) [reset = 0h]

GICD_IROUTER257_upper

Return to Summary Table

Table 14-18931. Instance Table

Instance Name	Physical Address
GICSS0	**0180 680Ch**

Figure 14-6281. GIC500_GICD_IROUTER_UPPER257 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18933. GIC500_GICD_IROUTER_UPPER257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.689 GIC500_GICD_IROUTER_LOWER258 Register

1 GIC500_GICD_IROUTER_LOWER258 Register (Offset = 6810h) [reset = 0h]

GICD_IROUTER258_lower

Return to Summary Table

Table 14-18934. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6810h**

Figure 14-6282. GIC500_GICD_IROUTER_LOWER258 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER258_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER258_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER258_LOWER__0_8							
R/W							
0h							

Table 14-18936. GIC500_GICD_IROUTER_LOWER258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER258_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER258_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER258_LOWER__0_8	R/W	0h	A0

14.4.1.2.690 GIC500_GICD_IROUTER_UPPER258 Register

1 GIC500_GICD_IROUTER_UPPER258 Register (Offset = 6814h) [reset = 0h]

GICD_IROUTER258_upper

Return to Summary Table

Table 14-18937. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6814h**

Figure 14-6283. GIC500_GICD_IROUTER_UPPER258 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18939. GIC500_GICD_IROUTER_UPPER258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.691 GIC500_GICD_IROUTER_LOWER259 Register

1 GIC500_GICD_IROUTER_LOWER259 Register (Offset = 6818h) [reset = 0h]

GICD_IROUTER259_lower

Return to Summary Table

Table 14-18940. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6818h**

Figure 14-6284. GIC500_GICD_IROUTER_LOWER259 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER259_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER259_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER259_LOWER__0_8							
R/W							
0h							

Table 14-18942. GIC500_GICD_IROUTER_LOWER259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER259_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER259_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER259_LOWER__0_8	R/W	0h	A0

14.4.1.2.692 GIC500_GICD_IROUTER_UPPER259 Register

1 GIC500_GICD_IROUTER_UPPER259 Register (Offset = 681Ch) [reset = 0h]

GICD_IROUTER259_upper

Return to Summary Table

Table 14-18943. Instance Table

Instance Name	Physical Address
GICSS0	**0180 681Ch**

Figure 14-6285. GIC500_GICD_IROUTER_UPPER259 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18945. GIC500_GICD_IROUTER_UPPER259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.693 GIC500_GICD_IROUTER_LOWER260 Register

1 GIC500_GICD_IROUTER_LOWER260 Register (Offset = 6820h) [reset = 0h]

GICD_IROUTER260_lower

Return to Summary Table

Table 14-18946. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6820h**

Figure 14-6286. GIC500_GICD_IROUTER_LOWER260 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER260_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER260_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER260_LOWER__0_8							
R/W							
0h							

Table 14-18948. GIC500_GICD_IROUTER_LOWER260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER260_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER260_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER260_LOWER__0_8	R/W	0h	A0

14.4.1.2.694 GIC500_GICD_IROUTER_UPPER260 Register

1 GIC500_GICD_IROUTER_UPPER260 Register (Offset = 6824h) [reset = 0h]

GICD_IROUTER260_upper

Return to Summary Table

Table 14-18949. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6824h**

Figure 14-6287. GIC500_GICD_IROUTER_UPPER260 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18951. GIC500_GICD_IROUTER_UPPER260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.695 GIC500_GICD_IROUTER_LOWER261 Register

1 GIC500_GICD_IROUTER_LOWER261 Register (Offset = 6828h) [reset = 0h]

GICD_IROUTER261_lower

Return to Summary Table

Table 14-18952. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6828h**

Figure 14-6288. GIC500_GICD_IROUTER_LOWER261 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER261_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER261_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER261_LOWER__0_8							
R/W							
0h							

Table 14-18954. GIC500_GICD_IROUTER_LOWER261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER261_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER261_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER261_LOWER__0_8	R/W	0h	A0

14.4.1.2.696 GIC500_GICD_IROUTER_UPPER261 Register

1 GIC500_GICD_IROUTER_UPPER261 Register (Offset = 682Ch) [reset = 0h]

GICD_IROUTER261_upper

Return to Summary Table

Table 14-18955. Instance Table

Instance Name	Physical Address
GICSS0	**0180 682Ch**

Figure 14-6289. GIC500_GICD_IROUTER_UPPER261 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18957. GIC500_GICD_IROUTER_UPPER261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.697 GIC500_GICD_IROUTER_LOWER262 Register

1 GIC500_GICD_IROUTER_LOWER262 Register (Offset = 6830h) [reset = 0h]

GICD_IROUTER262_lower

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Table 14-18958. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6830h**

Figure 14-6290. GIC500_GICD_IROUTER_LOWER262 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER262_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER262_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER262_LOWER__0_8							
R/W							
0h							

Table 14-18960. GIC500_GICD_IROUTER_LOWER262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER262_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER262_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER262_LOWER__0_8	R/W	0h	A0

14.4.1.2.698 GIC500_GICD_IROUTER_UPPER262 Register

1 GIC500_GICD_IROUTER_UPPER262 Register (Offset = 6834h) [reset = 0h]

GICD_IROUTER262_upper

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Table 14-18961. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6834h**

Figure 14-6291. GIC500_GICD_IROUTER_UPPER262 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18963. GIC500_GICD_IROUTER_UPPER262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.699 GIC500_GICD_IROUTER_LOWER263 Register

1 GIC500_GICD_IROUTER_LOWER263 Register (Offset = 6838h) [reset = 0h]

GICD_IROUTER263_lower

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Table 14-18964. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6838h**

Figure 14-6292. GIC500_GICD_IROUTER_LOWER263 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER263_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER263_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER263_LOWER__0_8							
R/W							
0h							

Table 14-18966. GIC500_GICD_IROUTER_LOWER263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER263_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER263_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER263_LOWER__0_8	R/W	0h	A0

14.4.1.2.700 GIC500_GICD_IROUTER_UPPER263 Register

1 GIC500_GICD_IROUTER_UPPER263 Register (Offset = 683Ch) [reset = 0h]

GICD_IROUTER263_upper

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Table 14-18967. Instance Table

Instance Name	Physical Address
GICSS0	**0180 683Ch**

Figure 14-6293. GIC500_GICD_IROUTER_UPPER263 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-18969. GIC500_GICD_IROUTER_UPPER263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.701 GIC500_GICD_IROUTER_LOWER264 Register

1 GIC500_GICD_IROUTER_LOWER264 Register (Offset = 6840h) [reset = 0h]

GICD_IROUTER264_lower

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Table 14-18970. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6840h**

Figure 14-6294. GIC500_GICD_IROUTER_LOWER264 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER264_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER264_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER264_LOWER__0_8							
R/W							
0h							

Table 14-18972. GIC500_GICD_IROUTER_LOWER264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER264_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER264_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER264_LOWER__0_8	R/W	0h	A0

14.4.1.2.702 GIC500_GICD_IROUTER_UPPER264 Register

1 GIC500_GICD_IROUTER_UPPER264 Register (Offset = 6844h) [reset = 0h]

GICD_IROUTER264_upper

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Table 14-18973. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6844h**

Figure 14-6295. GIC500_GICD_IROUTER_UPPER264 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18975. GIC500_GICD_IROUTER_UPPER264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.703 GIC500_GICD_IROUTER_LOWER265 Register

1 GIC500_GICD_IROUTER_LOWER265 Register (Offset = 6848h) [reset = 0h]

GICD_IROUTER265_lower

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Table 14-18976. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6848h**

Figure 14-6296. GIC500_GICD_IROUTER_LOWER265 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER265_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER265_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER265_LOWER__0_8							
R/W							
0h							

Table 14-18978. GIC500_GICD_IROUTER_LOWER265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER265_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER265_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER265_LOWER__0_8	R/W	0h	A0

14.4.1.2.704 GIC500_GICD_IROUTER_UPPER265 Register

1 GIC500_GICD_IROUTER_UPPER265 Register (Offset = 684Ch) [reset = 0h]

GICD_IROUTER265_upper

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Table 14-18979. Instance Table

Instance Name	Physical Address
GICSS0	**0180 684Ch**

Figure 14-6297. GIC500_GICD_IROUTER_UPPER265 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18981. GIC500_GICD_IROUTER_UPPER265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.705 GIC500_GICD_IROUTER_LOWER266 Register

1 GIC500_GICD_IROUTER_LOWER266 Register (Offset = 6850h) [reset = 0h]

GICD_IROUTER266_lower

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Table 14-18982. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6850h**

Figure 14-6298. GIC500_GICD_IROUTER_LOWER266 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER266_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER266_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER266_LOWER__0_8							
R/W							
0h							

Table 14-18984. GIC500_GICD_IROUTER_LOWER266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER266_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER266_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER266_LOWER__0_8	R/W	0h	A0

14.4.1.2.706 GIC500_GICD_IROUTER_UPPER266 Register

1 GIC500_GICD_IROUTER_UPPER266 Register (Offset = 6854h) [reset = 0h]

GICD_IROUTER266_upper

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Table 14-18985. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6854h**

Figure 14-6299. GIC500_GICD_IROUTER_UPPER266 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18987. GIC500_GICD_IROUTER_UPPER266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.707 GIC500_GICD_IROUTER_LOWER267 Register

1 GIC500_GICD_IROUTER_LOWER267 Register (Offset = 6858h) [reset = 0h]

GICD_IROUTER267_lower

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Table 14-18988. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6858h**

Figure 14-6300. GIC500_GICD_IROUTER_LOWER267 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER267_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER267_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER267_LOWER__0_8							
R/W							
0h							

Table 14-18990. GIC500_GICD_IROUTER_LOWER267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER267_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER267_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER267_LOWER__0_8	R/W	0h	A0

14.4.1.2.708 GIC500_GICD_IROUTER_UPPER267 Register

1 GIC500_GICD_IROUTER_UPPER267 Register (Offset = 685Ch) [reset = 0h]

GICD_IROUTER267_upper

Return to Summary Table

Table 14-18991. Instance Table

Instance Name	Physical Address
GICSS0	**0180 685Ch**

Figure 14-6301. GIC500_GICD_IROUTER_UPPER267 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18993. GIC500_GICD_IROUTER_UPPER267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.709 GIC500_GICD_IROUTER_LOWER268 Register

1 GIC500_GICD_IROUTER_LOWER268 Register (Offset = 6860h) [reset = 0h]

GICD_IROUTER268_lower

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Table 14-18994. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6860h**

Figure 14-6302. GIC500_GICD_IROUTER_LOWER268 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER268_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER268_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER268_LOWER__0_8							
R/W							
0h							

Table 14-18996. GIC500_GICD_IROUTER_LOWER268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER268_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER268_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER268_LOWER__0_8	R/W	0h	A0

14.4.1.2.710 GIC500_GICD_IROUTER_UPPER268 Register

1 GIC500_GICD_IROUTER_UPPER268 Register (Offset = 6864h) [reset = 0h]

GICD_IROUTER268_upper

Return to Summary Table

Table 14-18997. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6864h**

Figure 14-6303. GIC500_GICD_IROUTER_UPPER268 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18999. GIC500_GICD_IROUTER_UPPER268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.711 GIC500_GICD_IROUTER_LOWER269 Register

1 GIC500_GICD_IROUTER_LOWER269 Register (Offset = 6868h) [reset = 0h]

GICD_IROUTER269_lower

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Table 14-19000. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 6868h**

Figure 14-6304. GIC500_GICD_IROUTER_LOWER269 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER269_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER269_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER269_LOWER__0_8							
R/W							
0h							

Table 14-19002. GIC500_GICD_IROUTER_LOWER269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER269_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER269_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER269_LOWER__0_8	R/W	0h	A0

14.4.1.2.712 GIC500_GICD_IROUTER_UPPER269 Register

1 GIC500_GICD_IROUTER_UPPER269 Register (Offset = 686Ch) [reset = 0h]

GICD_IROUTER269_upper

Return to Summary Table

Table 14-19003. Instance Table

Instance Name	Physical Address
GICSS0	0180 686Ch

Figure 14-6305. GIC500_GICD_IROUTER_UPPER269 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19005. GIC500_GICD_IROUTER_UPPER269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.713 GIC500_GICD_IROUTER_LOWER270 Register

1 GIC500_GICD_IROUTER_LOWER270 Register (Offset = 6870h) [reset = 0h]

GICD_IROUTER270_lower

Return to Summary Table

Table 14-19006. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6870h**

Figure 14-6306. GIC500_GICD_IROUTER_LOWER270 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER270_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER270_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER270_LOWER__0_8							
R/W							
0h							

Table 14-19008. GIC500_GICD_IROUTER_LOWER270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER270_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER270_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER270_LOWER__0_8	R/W	0h	A0

14.4.1.2.714 GIC500_GICD_IROUTER_UPPER270 Register

1 GIC500_GICD_IROUTER_UPPER270 Register (Offset = 6874h) [reset = 0h]

GICD_IROUTER270_upper

Return to Summary Table

Table 14-19009. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6874h**

Figure 14-6307. GIC500_GICD_IROUTER_UPPER270 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19011. GIC500_GICD_IROUTER_UPPER270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.715 GIC500_GICD_IROUTER_LOWER271 Register

1 GIC500_GICD_IROUTER_LOWER271 Register (Offset = 6878h) [reset = 0h]

GICD_IROUTER271_lower

Return to Summary Table

Table 14-19012. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6878h**

Figure 14-6308. GIC500_GICD_IROUTER_LOWER271 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER271_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER271_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER271_LOWER__0_8							
R/W							
0h							

Table 14-19014. GIC500_GICD_IROUTER_LOWER271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER271_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER271_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER271_LOWER__0_8	R/W	0h	A0

14.4.1.2.716 GIC500_GICD_IROUTER_UPPER271 Register

1 GIC500_GICD_IROUTER_UPPER271 Register (Offset = 687Ch) [reset = 0h]

GICD_IROUTER271_upper

Return to Summary Table

Table 14-19015. Instance Table

Instance Name	Physical Address
GICSS0	**0180 687Ch**

Figure 14-6309. GIC500_GICD_IROUTER_UPPER271 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19017. GIC500_GICD_IROUTER_UPPER271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.717 GIC500_GICD_IROUTER_LOWER272 Register

1 GIC500_GICD_IROUTER_LOWER272 Register (Offset = 6880h) [reset = 0h]

GICD_IROUTER272_lower

Return to Summary Table

Table 14-19018. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6880h**

Figure 14-6310. GIC500_GICD_IROUTER_LOWER272 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER272_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER272_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER272_LOWER__0_8							
R/W							
0h							

Table 14-19020. GIC500_GICD_IROUTER_LOWER272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER272_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER272_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER272_LOWER__0_8	R/W	0h	A0

14.4.1.2.718 GIC500_GICD_IROUTER_UPPER272 Register

1 GIC500_GICD_IROUTER_UPPER272 Register (Offset = 6884h) [reset = 0h]

GICD_IROUTER272_upper

Return to Summary Table

Table 14-19021. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6884h**

Figure 14-6311. GIC500_GICD_IROUTER_UPPER272 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19023. GIC500_GICD_IROUTER_UPPER272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.719 GIC500_GICD_IROUTER_LOWER273 Register

1 GIC500_GICD_IROUTER_LOWER273 Register (Offset = 6888h) [reset = 0h]

GICD_IROUTER273_lower

Return to Summary Table

Table 14-19024. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6888h**

Figure 14-6312. GIC500_GICD_IROUTER_LOWER273 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER273_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER273_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER273_LOWER__0_8							
R/W							
0h							

Table 14-19026. GIC500_GICD_IROUTER_LOWER273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER273_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER273_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER273_LOWER__0_8	R/W	0h	A0

14.4.1.2.720 GIC500_GICD_IROUTER_UPPER273 Register

1 GIC500_GICD_IROUTER_UPPER273 Register (Offset = 688Ch) [reset = 0h]

GICD_IROUTER273_upper

Return to Summary Table

Table 14-19027. Instance Table

Instance Name	Physical Address
GICSS0	**0180 688Ch**

Figure 14-6313. GIC500_GICD_IROUTER_UPPER273 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19029. GIC500_GICD_IROUTER_UPPER273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.721 GIC500_GICD_IROUTER_LOWER274 Register

1 GIC500_GICD_IROUTER_LOWER274 Register (Offset = 6890h) [reset = 0h]

GICD_IROUTER274_lower

Return to Summary Table

Table 14-19030. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6890h**

Figure 14-6314. GIC500_GICD_IROUTER_LOWER274 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER274_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER274_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER274_LOWER__0_8							
R/W							
0h							

Table 14-19032. GIC500_GICD_IROUTER_LOWER274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER274_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER274_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER274_LOWER__0_8	R/W	0h	A0

14.4.1.2.722 GIC500_GICD_IROUTER_UPPER274 Register

1 GIC500_GICD_IROUTER_UPPER274 Register (Offset = 6894h) [reset = 0h]

GICD_IROUTER274_upper

Return to Summary Table

Table 14-19033. Instance Table

Instance Name	Physical Address
GICSS0	0180 6894h

Figure 14-6315. GIC500_GICD_IROUTER_UPPER274 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19035. GIC500_GICD_IROUTER_UPPER274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.723 GIC500_GICD_IROUTER_LOWER275 Register

1 GIC500_GICD_IROUTER_LOWER275 Register (Offset = 6898h) [reset = 0h]

GICD_IROUTER275_lower

Return to Summary Table

Table 14-19036. Instance Table

Instance Name	Physical Address
GICSS0	**0180 6898h**

Figure 14-6316. GIC500_GICD_IROUTER_LOWER275 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER275_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER275_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER275_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19038. GIC500_GICD_IROUTER_LOWER275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER275_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER275_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER275_LOWER__0_8	R/W	0h	A0

14.4.1.2.724 GIC500_GICD_IROUTER_UPPER275 Register

1 GIC500_GICD_IROUTER_UPPER275 Register (Offset = 689Ch) [reset = 0h]

GICD_IROUTER275_upper

Return to Summary Table

Table 14-19039. Instance Table

Instance Name	Physical Address
GICSS0	**0180 689Ch**

Figure 14-6317. GIC500_GICD_IROUTER_UPPER275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19041. GIC500_GICD_IROUTER_UPPER275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.725 GIC500_GICD_IROUTER_LOWER276 Register

1 GIC500_GICD_IROUTER_LOWER276 Register (Offset = 68A0h) [reset = 0h]

GICD_IROUTER276_lower

Return to Summary Table

Table 14-19042. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68A0h**

Figure 14-6318. GIC500_GICD_IROUTER_LOWER276 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER276_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER276_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER276_LOWER__0_8							
R/W							
0h							

Table 14-19044. GIC500_GICD_IROUTER_LOWER276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER276_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER276_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER276_LOWER__0_8	R/W	0h	A0

14.4.1.2.726 GIC500_GICD_IROUTER_UPPER276 Register

1 GIC500_GICD_IROUTER_UPPER276 Register (Offset = 68A4h) [reset = 0h]

GICD_IROUTER276_upper

Return to Summary Table

Table 14-19045. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68A4h**

Figure 14-6319. GIC500_GICD_IROUTER_UPPER276 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19047. GIC500_GICD_IROUTER_UPPER276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.727 GIC500_GICD_IROUTER_LOWER277 Register

1 GIC500_GICD_IROUTER_LOWER277 Register (Offset = 68A8h) [reset = 0h]

GICD_IROUTER277_lower

Return to Summary Table

Table 14-19048. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68A8h**

Figure 14-6320. GIC500_GICD_IROUTER_LOWER277 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER277_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER277_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER277_LOWER__0_8							
R/W							
0h							

Table 14-19050. GIC500_GICD_IROUTER_LOWER277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER277_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER277_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER277_LOWER__0_8	R/W	0h	A0

14.4.1.2.728 GIC500_GICD_IROUTER_UPPER277 Register

1 GIC500_GICD_IROUTER_UPPER277 Register (Offset = 68ACh) [reset = 0h]

GICD_IROUTER277_upper

Return to Summary Table

Table 14-19051. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68ACh**

Figure 14-6321. GIC500_GICD_IROUTER_UPPER277 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19053. GIC500_GICD_IROUTER_UPPER277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.729 GIC500_GICD_IROUTER_LOWER278 Register

1 GIC500_GICD_IROUTER_LOWER278 Register (Offset = 68B0h) [reset = 0h]

GICD_IROUTER278_lower

Return to Summary Table

Table 14-19054. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68B0h**

Figure 14-6322. GIC500_GICD_IROUTER_LOWER278 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER278_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER278_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER278_LOWER__0_8							
R/W							
0h							

Table 14-19056. GIC500_GICD_IROUTER_LOWER278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER278_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER278_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER278_LOWER__0_8	R/W	0h	A0

14.4.1.2.730 GIC500_GICD_IROUTER_UPPER278 Register

1 GIC500_GICD_IROUTER_UPPER278 Register (Offset = 68B4h) [reset = 0h]

GICD_IROUTER278_upper

Return to Summary Table

Table 14-19057. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68B4h**

Figure 14-6323. GIC500_GICD_IROUTER_UPPER278 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19059. GIC500_GICD_IROUTER_UPPER278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.731 GIC500_GICD_IROUTER_LOWER279 Register

1 GIC500_GICD_IROUTER_LOWER279 Register (Offset = 68B8h) [reset = 0h]

GICD_IROUTER279_lower

Return to Summary Table

Table 14-19060. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68B8h**

Figure 14-6324. GIC500_GICD_IROUTER_LOWER279 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER279_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER279_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER279_LOWER__0_8							
R/W							
0h							

Table 14-19062. GIC500_GICD_IROUTER_LOWER279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER279_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER279_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER279_LOWER__0_8	R/W	0h	A0

14.4.1.2.732 GIC500_GICD_IROUTER_UPPER279 Register

1 GIC500_GICD_IROUTER_UPPER279 Register (Offset = 68BCh) [reset = 0h]

GICD_IROUTER279_upper

Return to Summary Table

Table 14-19063. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68BCh**

Figure 14-6325. GIC500_GICD_IROUTER_UPPER279 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19065. GIC500_GICD_IROUTER_UPPER279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.733 GIC500_GICD_IROUTER_LOWER280 Register

1 GIC500_GICD_IROUTER_LOWER280 Register (Offset = 68C0h) [reset = 0h]

GICD_IROUTER280_lower

Return to Summary Table

Table 14-19066. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68C0h**

Figure 14-6326. GIC500_GICD_IROUTER_LOWER280 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER280_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER280_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER280_LOWER__0_8							
R/W							
0h							

Table 14-19068. GIC500_GICD_IROUTER_LOWER280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER280_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER280_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER280_LOWER__0_8	R/W	0h	A0

14.4.1.2.734 GIC500_GICD_IROUTER_UPPER280 Register

1 GIC500_GICD_IROUTER_UPPER280 Register (Offset = 68C4h) [reset = 0h]

GICD_IROUTER280_upper

Return to Summary Table

Table 14-19069. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68C4h**

Figure 14-6327. GIC500_GICD_IROUTER_UPPER280 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19071. GIC500_GICD_IROUTER_UPPER280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.735 GIC500_GICD_IROUTER_LOWER281 Register

1 GIC500_GICD_IROUTER_LOWER281 Register (Offset = 68C8h) [reset = 0h]

GICD_IROUTER281_lower

Return to Summary Table

Table 14-19072. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68C8h**

Figure 14-6328. GIC500_GICD_IROUTER_LOWER281 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER281_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER281_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER281_LOWER__0_8							
R/W							
0h							

Table 14-19074. GIC500_GICD_IROUTER_LOWER281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER281_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER281_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER281_LOWER__0_8	R/W	0h	A0

14.4.1.2.736 GIC500_GICD_IROUTER_UPPER281 Register

1 GIC500_GICD_IROUTER_UPPER281 Register (Offset = 68CCh) [reset = 0h]

GICD_IROUTER281_upper

Return to Summary Table

Table 14-19075. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68CCh**

Figure 14-6329. GIC500_GICD_IROUTER_UPPER281 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19077. GIC500_GICD_IROUTER_UPPER281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.737 GIC500_GICD_IROUTER_LOWER282 Register

1 GIC500_GICD_IROUTER_LOWER282 Register (Offset = 68D0h) [reset = 0h]

GICD_IROUTER282_lower

Return to Summary Table

Table 14-19078. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68D0h**

Figure 14-6330. GIC500_GICD_IROUTER_LOWER282 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER282_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER282_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER282_LOWER__0_8							
R/W							
0h							

Table 14-19080. GIC500_GICD_IROUTER_LOWER282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER282_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER282_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER282_LOWER__0_8	R/W	0h	A0

14.4.1.2.738 GIC500_GICD_IROUTER_UPPER282 Register

1 GIC500_GICD_IROUTER_UPPER282 Register (Offset = 68D4h) [reset = 0h]

GICD_IROUTER282_upper

Return to Summary Table

Table 14-19081. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68D4h**

Figure 14-6331. GIC500_GICD_IROUTER_UPPER282 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19083. GIC500_GICD_IROUTER_UPPER282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.739 GIC500_GICD_IROUTER_LOWER283 Register

1 GIC500_GICD_IROUTER_LOWER283 Register (Offset = 68D8h) [reset = 0h]

GICD_IROUTER283_lower

Return to Summary Table

Table 14-19084. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68D8h**

Figure 14-6332. GIC500_GICD_IROUTER_LOWER283 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DISTRIBUTOR__37_GICD_IROUTER283_LOWER__31_1</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER283_LOWER__8_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DISTRIBUTOR__37_GICD_IROUTER283_LOWER__0_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19086. GIC500_GICD_IROUTER_LOWER283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER283_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER283_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER283_LOWER__0_8	R/W	0h	A0

14.4.1.2.740 GIC500_GICD_IROUTER_UPPER283 Register

1 GIC500_GICD_IROUTER_UPPER283 Register (Offset = 68DCh) [reset = 0h]

GICD_IROUTER283_upper

Return to Summary Table

Table 14-19087. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68DCh**

Figure 14-6333. GIC500_GICD_IROUTER_UPPER283 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19089. GIC500_GICD_IROUTER_UPPER283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.741 GIC500_GICD_IROUTER_LOWER284 Register

1 GIC500_GICD_IROUTER_LOWER284 Register (Offset = 68E0h) [reset = 0h]

GICD_IROUTER284_lower

Return to Summary Table

Table 14-19090. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68E0h**

Figure 14-6334. GIC500_GICD_IROUTER_LOWER284 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER284_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISTRIBUTOR__37_GICD_IROUTER284_LOWER__8_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISTRIBUTOR__37_GICD_IROUTER284_LOWER__0_8							
R/W							
0h							

Table 14-19092. GIC500_GICD_IROUTER_LOWER284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER284_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER284_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER284_LOWER__0_8	R/W	0h	A0

14.4.1.2.742 GIC500_GICD_IROUTER_UPPER284 Register

1 GIC500_GICD_IROUTER_UPPER284 Register (Offset = 68E4h) [reset = 0h]

GICD_IROUTER284_upper

Return to Summary Table

Table 14-19093. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68E4h**

Figure 14-6335. GIC500_GICD_IROUTER_UPPER284 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19095. GIC500_GICD_IROUTER_UPPER284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.743 GIC500_GICD_IROUTER_LOWER285 Register

1 GIC500_GICD_IROUTER_LOWER285 Register (Offset = 68E8h) [reset = 0h]

GICD_IROUTER285_lower

Return to Summary Table

Table 14-19096. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68E8h**

Figure 14-6336. GIC500_GICD_IROUTER_LOWER285 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER285_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER285_LOWER__8_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER285_LOWER__0_8							
R/W							
0h							

Table 14-19098. GIC500_GICD_IROUTER_LOWER285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER285_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER285_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER285_LOWER__0_8	R/W	0h	A0

14.4.1.2.744 GIC500_GICD_IROUTER_UPPER285 Register

1 GIC500_GICD_IROUTER_UPPER285 Register (Offset = 68ECh) [reset = 0h]

GICD_IROUTER285_upper

Return to Summary Table

Table 14-19099. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68ECh**

Figure 14-6337. GIC500_GICD_IROUTER_UPPER285 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19101. GIC500_GICD_IROUTER_UPPER285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.745 GIC500_GICD_IROUTER_LOWER286 Register

1 GIC500_GICD_IROUTER_LOWER286 Register (Offset = 68F0h) [reset = 0h]

GICD_IROUTER286_lower

Return to Summary Table

Table 14-19102. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68F0h**

Figure 14-6338. GIC500_GICD_IROUTER_LOWER286 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER286_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER286_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER286_LOWER__0_8							
R/W							
0h							

Table 14-19104. GIC500_GICD_IROUTER_LOWER286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER286_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER286_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER286_LOWER__0_8	R/W	0h	A0

14.4.1.2.746 GIC500_GICD_IROUTER_UPPER286 Register

1 GIC500_GICD_IROUTER_UPPER286 Register (Offset = 68F4h) [reset = 0h]

GICD_IROUTER286_upper

Return to Summary Table

Table 14-19105. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68F4h**

Figure 14-6339. GIC500_GICD_IROUTER_UPPER286 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19107. GIC500_GICD_IROUTER_UPPER286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.747 GIC500_GICD_IROUTER_LOWER287 Register

1 GIC500_GICD_IROUTER_LOWER287 Register (Offset = 68F8h) [reset = 0h]

GICD_IROUTER287_lower

Return to Summary Table

Table 14-19108. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68F8h**

Figure 14-6340. GIC500_GICD_IROUTER_LOWER287 Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__37_GICD_IROUTER287_LOWER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DISTRIBUTOR__37_GICD_IROUTER287_LOWER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DISTRIBUTOR__37_GICD_IROUTER287_LOWER__0_8							
R/W							
0h							

Table 14-19110. GIC500_GICD_IROUTER_LOWER287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__37_GICD_IROUTER287_LOWER__31_1	R/W	0h	IRM
30:16	RESERVED	NONE	0h	Reserved
15:8	DISTRIBUTOR__37_GICD_IROUTER287_LOWER__8_8	R/W	0h	A1
7:0	DISTRIBUTOR__37_GICD_IROUTER287_LOWER__0_8	R/W	0h	A0

14.4.1.2.748 GIC500_GICD_IROUTER_UPPER287 Register

1 GIC500_GICD_IROUTER_UPPER287 Register (Offset = 68FCh) [reset = 0h]

GICD_IROUTER287_upper

Return to Summary Table

Table 14-19111. Instance Table

Instance Name	Physical Address
GICSS0	**0180 68FCh**

Figure 14-6341. GIC500_GICD_IROUTER_UPPER287 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19113. GIC500_GICD_IROUTER_UPPER287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.749 GIC500_GICD_ESTATUSR Register

1 GIC500_GICD_ESTATUSR Register (Offset = C000h) [reset = 0h]

GICD_ESTATUSR

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Table 14-19114. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C000h**

Figure 14-6342. GIC500_GICD_ESTATUSR Name Register

31	30	29	28	27	26	25	24
DISTRIBUTOR__38_GICD_ESTATUSR__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19116. GIC500_GICD_ESTATUSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISTRIBUTOR__38_GICD_ESTATUSR__31_1	R/W	0h	SWRP
30:0	RESERVED	NONE	0h	Reserved

14.4.1.2.750 GIC500_GICD_ERRTESTR Register

1 GIC500_GICD_ERRTESTR Register (Offset = C004h) [reset = 0h]

GICD_ERRTESTR

Return to Summary Table

Table 14-19117. Instance Table

Instance Name	Physical Address
GICSS0	0180 C004h

Figure 14-6343. GIC500_GICD_ERRTESTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISTRIBUTOR__39_GICD_ERRTESTR__1_1	DISTRIBUTOR__39_GICD_ERRTESTR__0_1
NONE						R/W	R/W
0h						0h	0h

Table 14-19119. GIC500_GICD_ERRTESTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISTRIBUTOR__39_GICD_ERRTESTR__1_1	R/W	0h	AXIM_err
0	DISTRIBUTOR__39_GICD_ERRTESTR__0_1	R/W	0h	ECC_fatal

14.4.1.2.751 GIC500_GICD_SPISR0 Register

1 GIC500_GICD_SPISR0 Register (Offset = C084h) [reset = 0h]

GICD_SPISR0

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Table 14-19120. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C084h**

Figure 14-6344. GIC500_GICD_SPISR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19122. GIC500_GICD_SPISR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.752 GIC500_GICD_SPISR1 Register

1 GIC500_GICD_SPISR1 Register (Offset = C088h) [reset = 0h]

GICD_SPISR1

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Table 14-19123. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C088h**

Figure 14-6345. GIC500_GICD_SPISR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19125. GIC500_GICD_SPISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.753 GIC500_GICD_SPISR2 Register

1 GIC500_GICD_SPISR2 Register (Offset = C08Ch) [reset = 0h]

GICD_SPISR2

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Table 14-19126. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C08Ch**

Figure 14-6346. GIC500_GICD_SPISR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19128. GIC500_GICD_SPISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.754 GIC500_GICD_SPISR3 Register

1 GIC500_GICD_SPISR3 Register (Offset = C090h) [reset = 0h]

GICD_SPISR3

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Table 14-19129. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C090h**

Figure 14-6347. GIC500_GICD_SPISR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19131. GIC500_GICD_SPISR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.755 GIC500_GICD_SPISR4 Register

1 GIC500_GICD_SPISR4 Register (Offset = C094h) [reset = 0h]

GICD_SPISR4

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Table 14-19132. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C094h**

Figure 14-6348. GIC500_GICD_SPISR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19134. GIC500_GICD_SPISR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.756 GIC500_GICD_SPISR5 Register

1 GIC500_GICD_SPISR5 Register (Offset = C098h) [reset = 0h]

GICD_SPISR5

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Table 14-19135. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C098h**

Figure 14-6349. GIC500_GICD_SPISR5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19137. GIC500_GICD_SPISR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.757 GIC500_GICD_SPISR6 Register

1 GIC500_GICD_SPISR6 Register (Offset = C09Ch) [reset = 0h]

GICD_SPISR6

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Table 14-19138. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C09Ch**

Figure 14-6350. GIC500_GICD_SPISR6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19140. GIC500_GICD_SPISR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.758 GIC500_GICD_SPISR7 Register

1 GIC500_GICD_SPISR7 Register (Offset = C0A0h) [reset = 0h]

GICD_SPISR7

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Table 14-19141. Instance Table

Instance Name	Physical Address
GICSS0	**0180 C0A0h**

Figure 14-6351. GIC500_GICD_SPISR7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19143. GIC500_GICD_SPISR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.759 GIC500_GICD_PIDR4 Register

1 GIC500_GICD_PIDR4 Register (Offset = FFD0h) [reset = 0h]

GICD_PIDR4

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Table 14-19144. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFD0h**

Figure 14-6352. GIC500_GICD_PIDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19146. GIC500_GICD_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.760 GIC500_GICD_PIDR5 Register

1 GIC500_GICD_PIDR5 Register (Offset = FFD4h) [reset = 0h]

GICD_PIDR5

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Table 14-19147. Instance Table

Instance Name	**Physical Address**
GICSS0	**0180 FFD4h**

Figure 14-6353. GIC500_GICD_PIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19149. GIC500_GICD_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.761 GIC500_GICD_PIDR6 Register

1 GIC500_GICD_PIDR6 Register (Offset = FFD8h) [reset = 0h]

GICD_PIDR6

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Table 14-19150. Instance Table

Instance Name	Physical Address
GICSS0	0180 FFD8h

Figure 14-6354. GIC500_GICD_PIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19152. GIC500_GICD_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.762 GIC500_GICD_PIDR7 Register

1 GIC500_GICD_PIDR7 Register (Offset = FFDCh) [reset = 0h]

GICD_PIDR7

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Table 14-19153. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFDCh**

Figure 14-6355. GIC500_GICD_PIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19155. GIC500_GICD_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.763 GIC500_GICD_PIDR0 Register

1 GIC500_GICD_PIDR0 Register (Offset = FFE0h) [reset = 0h]

GICD_PIDR0

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Table 14-19156. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFE0h**

Figure 14-6356. GIC500_GICD_PIDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19158. GIC500_GICD_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.764 GIC500_GICD_PIDR1 Register

1 GIC500_GICD_PIDR1 Register (Offset = FFE4h) [reset = 0h]

GICD_PIDR1

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Table 14-19159. Instance Table

Instance Name	Physical Address
GICSS0	0180 FFE4h

Figure 14-6357. GIC500_GICD_PIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19161. GIC500_GICD_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.765 GIC500_GICD_PIDR2 Register

1 GIC500_GICD_PIDR2 Register (Offset = FFE8h) [reset = 0h]

GICD_PIDR2

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Table 14-19162. Instance Table

Instance Name	Physical Address
GICSS0	0180 FFE8h

Figure 14-6358. GIC500_GICD_PIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19164. GIC500_GICD_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.766 GIC500_GICD_PIDR3 Register

1 GIC500_GICD_PIDR3 Register (Offset = FFECh) [reset = 0h]

GICD_PIDR3

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Table 14-19165. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFECh**

Figure 14-6359. GIC500_GICD_PIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19167. GIC500_GICD_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.767 GIC500_GICD_CIDR0 Register

1 GIC500_GICD_CIDR0 Register (Offset = FFF0h) [reset = 0h]

GICD_CIDR0

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Table 14-19168. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFF0h**

Figure 14-6360. GIC500_GICD_CIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19170. GIC500_GICD_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.768 GIC500_GICD_CIDR1 Register

1 GIC500_GICD_CIDR1 Register (Offset = FFF4h) [reset = 0h]

GICD_CIDR1

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Table 14-19171. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFF4h**

Figure 14-6361. GIC500_GICD_CIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19173. GIC500_GICD_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.769 GIC500_GICD_CIDR2 Register

1 GIC500_GICD_CIDR2 Register (Offset = FFF8h) [reset = 0h]

GICD_CIDR2

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Table 14-19174. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFF8h**

Figure 14-6362. GIC500_GICD_CIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19176. GIC500_GICD_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.770 GIC500_GICD_CIDR3 Register

1 GIC500_GICD_CIDR3 Register (Offset = FFFCh) [reset = 0h]

GICD_CIDR3

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Table 14-19177. Instance Table

Instance Name	Physical Address
GICSS0	**0180 FFFCh**

Figure 14-6363. GIC500_GICD_CIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19179. GIC500_GICD_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.771 GIC500_MSG_SETSPI_NSR Register

1 GIC500_MSG_SETSPI_NSR Register (Offset = 10040h) [reset = 0h]

GICD_SETSPI_NSR

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Table 14-19180. Instance Table

Instance Name	Physical Address
GICSS0	**0181 0040h**

Figure 14-6364. GIC500_MSG_SETSPI_NSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						MESSAGE_BASED_SPIS__1_GICD_SETSPI_NSR__0_10	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MESSAGE_BASED_SPIS__1_GICD_SETSPI_NSR__0_10							
R/W							
0h							

Table 14-19182. GIC500_MSG_SETSPI_NSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	MESSAGE_BASED_SPIS__1_GICD_SETSPI_NSR__0_10	R/W	0h	SPI ID

14.4.1.2.772 GIC500_MSG_CLRSPI_NSR Register

1 GIC500_MSG_CLRSPI_NSR Register (Offset = 10048h) [reset = 0h]

GICD_CLRSPI_NSR

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Table 14-19183. Instance Table

Instance Name	Physical Address
GICSS0	**0181 0048h**

Figure 14-6365. GIC500_MSG_CLRSPI_NSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						MESSAGE_BASED_SPIS__2_GICD_CLRSPI_NSR__0_10	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MESSAGE_BASED_SPIS__2_GICD_CLRSPI_NSR__0_10							
R/W							
0h							

Table 14-19185. GIC500_MSG_CLRSPI_NSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	MESSAGE_BASED_SPIS__2_GICD_CLRSPI_NSR__0_10	R/W	0h	SPI ID

14.4.1.2.773 GIC500_MSG_SETSPI_SR Register

1 GIC500_MSG_SETSPI_SR Register (Offset = 10050h) [reset = 0h]

GICD_SETSPI_SR

Return to Summary Table

Table 14-19186. Instance Table

Instance Name	Physical Address
GICSS0	**0181 0050h**

Figure 14-6366. GIC500_MSG_SETSPI_SR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MESSAGE_BASED_SPIS__3_GICD_SETSPI_SR__0_10	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
MESSAGE_BASED_SPIS__3_GICD_SETSPI_SR__0_10							
R/W							
0h							

Table 14-19188. GIC500_MSG_SETSPI_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	MESSAGE_BASED_SPIS__3_GICD_SETSPI_SR__0_10	R/W	0h	SPI ID

14.4.1.2.774 GIC500_MSG_CLRSPI_SR Register

1 GIC500_MSG_CLRSPI_SR Register (Offset = 10058h) [reset = 0h]

GICD_CLRSPI_SR

Return to Summary Table

Table 14-19189. Instance Table

Instance Name	Physical Address
GICSS0	**0181 0058h**

Figure 14-6367. GIC500_MSG_CLRSPI_SR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MESSAGE_BASED_SPIS__4_GICD_CLRSPI_SR__0_10	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
MESSAGE_BASED_SPIS__4_GICD_CLRSPI_SR__0_10							
R/W							
0h							

Table 14-19191. GIC500_MSG_CLRSPI_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	MESSAGE_BASED_SPIS__4_GICD_CLRSPI_SR__0_10	R/W	0h	SPI ID

14.4.1.2.775 GIC500_ITS_CTLR Register

1 GIC500_ITS_CTLR Register (Offset = 20000h) [reset = 80000000h]

GITS_CTLR

Return to Summary Table

Table 14-19192. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0000h**

Figure 14-6368. GIC500_ITS_CTLR Name Register

31	30	29	28	27	26	25	24
ITS__1_GITS_CTLR__31_1	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ITS__1_GITS_CTLR__0_1
NONE							R/W
0h							0h

Table 14-19194. GIC500_ITS_CTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ITS__1_GITS_CTLR__31_1	R/W	1h	Quiescent
30:1	RESERVED	NONE	0h	Reserved
0	ITS__1_GITS_CTLR__0_1	R/W	0h	Enabled

14.4.1.2.776 GIC500_ITS_IIDR Register

1 GIC500_ITS_IIDR Register (Offset = 20004h) [reset = 1143Bh]

GITS_IIDR

Return to Summary Table

Table 14-19195. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0004h**

Figure 14-6369. GIC500_ITS_IIDR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ITS__2_GITS_IIDR__24_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ITS__2_GITS_IIDR__16_4</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">ITS__2_GITS_IIDR__12_4</td><td colspan="4">ITS__2_GITS_IIDR__0_12</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">43Bh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ITS__2_GITS_IIDR__0_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">43Bh</td></tr>
</table>

Table 14-19197. GIC500_ITS_IIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ITS__2_GITS_IIDR__24_8	R/W	0h	ProductID
23:20	RESERVED	NONE	0h	Reserved
19:16	ITS__2_GITS_IIDR__16_4	R/W	1h	Variant
15:12	ITS__2_GITS_IIDR__12_4	R/W	1h	Revision
11:0	ITS__2_GITS_IIDR__0_12	R/W	43Bh	Implementer

14.4.1.2.777 GIC500_ITS_TYPER_LOWER Register

1 GIC500_ITS_TYPER_LOWER Register (Offset = 20008h) [reset = 3028F31h]

GITS_TYPER_lower

Return to Summary Table

Table 14-19198. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0008h**

Figure 14-6370. GIC500_ITS_TYPER_LOWER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ITS__3_GITS_TYPER_LOWER__24_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td>ITS__3_GITS_TYPER_LOWER__19_1</td><td>RESERVED</td><td colspan="2">ITS__3_GITS_TYPER_LOWER__13_5</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td>NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td colspan="2">14h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">ITS__3_GITS_TYPER_LOWER__13_5</td><td colspan="5">ITS__3_GITS_TYPER_LOWER__8_5</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">14h</td><td colspan="5">Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ITS__3_GITS_TYPER_LOWER__4_4</td><td>ITS__3_GITS_TYPER_LOWER__3_1</td><td>RESERVED</td><td>ITS__3_GITS_TYPER_LOWER__1_1</td><td>ITS__3_GITS_TYPER_LOWER__0_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">3h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-19200. GIC500_ITS_TYPER_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ITS__3_GITS_TYPER_LOWER__24_8	R/W	3h	HCC
23:20	RESERVED	NONE	0h	Reserved
19	ITS__3_GITS_TYPER_LOWER__19_1	R/W	0h	PTA
18	RESERVED	NONE	0h	Reserved
17:13	ITS__3_GITS_TYPER_LOWER__13_5	R/W	14h	Devbits
12:8	ITS__3_GITS_TYPER_LOWER__8_5	R/W	Fh	IDbits
7:4	ITS__3_GITS_TYPER_LOWER__4_4	R/W	3h	ITT Entry Size
3	ITS__3_GITS_TYPER_LOWER__3_1	R/W	0h	Distributed
2	RESERVED	NONE	0h	Reserved
1	ITS__3_GITS_TYPER_LOWER__1_1	R/W	0h	VLPIS

Table 14-19200. GIC500_ITS_TYPER_LOWER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ITS__3_GITS_TYPER_LOWER__0_1	R/W	1h	PLPIS

14.4.1.2.778 GIC500_ITS_TYPER_UPPER Register

1 GIC500_ITS_TYPER_UPPER Register (Offset = 2000Ch) [reset = 0h]

GITS_TYPER_upper

Return to Summary Table

Table 14-19201. Instance Table

Instance Name	Physical Address
GICSS0	**0182 000Ch**

Figure 14-6371. GIC500_ITS_TYPER_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19203. GIC500_ITS_TYPER_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.779 GIC500_ITS_CBASER_LOWER Register

1 GIC500_ITS_CBASER_LOWER Register (Offset = 20080h) [reset = 0h]

GITS_CBASER_lower

Return to Summary Table

Table 14-19204. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0080h**

Figure 14-6372. GIC500_ITS_CBASER_LOWER Name Register

31	30	29	28	27	26	25	24
ITS__5_GITS_CBASER_LOWER__12_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITS__5_GITS_CBASER_LOWER__12_20							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITS__5_GITS_CBASER_LOWER__12_20				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITS__5_GITS_CBASER_LOWER__0_8							
R/W							
0h							

Table 14-19206. GIC500_ITS_CBASER_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ITS__5_GITS_CBASER_LOWER__12_20	R/W	0h	Physical Address [31:12]
11:8	RESERVED	NONE	0h	Reserved
7:0	ITS__5_GITS_CBASER_LOWER__0_8	R/W	0h	Size

14.4.1.2.780 GIC500_ITS_CBASER_UPPER Register

1 GIC500_ITS_CBASER_UPPER Register (Offset = 20084h) [reset = 0h]

GITS_CBASER_upper

Return to Summary Table

Table 14-19207. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0084h**

Figure 14-6373. GIC500_ITS_CBASER_UPPER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>ITS__6_GITS_CBASER_UPPER__31_1</td><td>RESERVED</td><td colspan="3">ITS__6_GITS_CBASER_UPPER__27_3</td><td colspan="3">RESERVED</td></tr>
<tr><td>R/W</td><td>NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ITS__6_GITS_CBASER_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ITS__6_GITS_CBASER_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19209. GIC500_ITS_CBASER_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ITS__6_GITS_CBASER_UPPER__31_1	R/W	0h	Valid
30	RESERVED	NONE	0h	Reserved
29:27	ITS__6_GITS_CBASER_UPPER__27_3	R/W	0h	Cacheability
26:16	RESERVED	NONE	0h	Reserved
15:0	ITS__6_GITS_CBASER_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.781 GIC500_ITS_CWRITER_LOWER Register

1 GIC500_ITS_CWRITER_LOWER Register (Offset = 20088h) [reset = 0h]

GITS_CWRITER_lower

Return to Summary Table

Table 14-19210. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0088h**

Figure 14-6374. GIC500_ITS_CWRITER_LOWER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ITS__7_GITS_CWRITER_LOWER__5_15			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ITS__7_GITS_CWRITER_LOWER__5_15							
R/W							
0h							
7	6	5	4	3	2	1	0
ITS__7_GITS_CWRITER_LOWER__5_15			RESERVED				
R/W			NONE				
0h			0h				

Table 14-19212. GIC500_ITS_CWRITER_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:5	ITS__7_GITS_CWRITER_LOWER__5_15	R/W	0h	Offset
4:0	RESERVED	NONE	0h	Reserved

14.4.1.2.782 GIC500_ITS_CWRITER_UPPER Register

1 GIC500_ITS_CWRITER_UPPER Register (Offset = 2008Ch) [reset = 0h]

GITS_CWRITER_upper

Return to Summary Table

Table 14-19213. Instance Table

Instance Name	Physical Address
GICSS0	**0182 008Ch**

Figure 14-6375. GIC500_ITS_CWRITER_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19215. GIC500_ITS_CWRITER_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.783 GIC500_ITS_CREADR_LOWER Register

1 GIC500_ITS_CREADR_LOWER Register (Offset = 20090h) [reset = 0h]

GITS_CREADR_lower

Return to Summary Table

Table 14-19216. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0090h**

Figure 14-6376. GIC500_ITS_CREADR_LOWER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ITS__9_GITS_CREADR_LOWER__5_15			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ITS__9_GITS_CREADR_LOWER__5_15							
R/W							
0h							
7	6	5	4	3	2	1	0
ITS__9_GITS_CREADR_LOWER__5_15			RESERVED				
R/W			NONE				
0h			0h				

Table 14-19218. GIC500_ITS_CREADR_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:5	ITS__9_GITS_CREADR_LOWER__5_15	R/W	0h	Offset
4:0	RESERVED	NONE	0h	Reserved

14.4.1.2.784 GIC500_ITS_CREADR_UPPER Register

1 GIC500_ITS_CREADR_UPPER Register (Offset = 20094h) [reset = 0h]

GITS_CREADR_upper

Return to Summary Table

Table 14-19219. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0094h**

Figure 14-6377. GIC500_ITS_CREADR_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19221. GIC500_ITS_CREADR_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.785 GIC500_ITS_BASER0_LOWER Register

1 GIC500_ITS_BASER0_LOWER Register (Offset = 20100h) [reset = 0h]

GITS_BASER0_lower

Return to Summary Table

Table 14-19222. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0100h**

Figure 14-6378. GIC500_ITS_BASER0_LOWER Name Register

31	30	29	28	27	26	25	24
ITS__11_GITS_BASER0_LOWER__12_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITS__11_GITS_BASER0_LOWER__12_20							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITS__11_GITS_BASER0_LOWER__12_20				RESERVED		ITS__11_GITS_BASER0_LOWER__8_2	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITS__11_GITS_BASER0_LOWER__0_8							
R/W							
0h							

Table 14-19224. GIC500_ITS_BASER0_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ITS__11_GITS_BASER0_LOWER__12_20	R/W	0h	Physical Address [31:12]
11:10	RESERVED	NONE	0h	Reserved
9:8	ITS__11_GITS_BASER0_LOWER__8_2	R/W	0h	Page Size
7:0	ITS__11_GITS_BASER0_LOWER__0_8	R/W	0h	Size

14.4.1.2.786 GIC500_ITS_BASER0_UPPER Register

1 GIC500_ITS_BASER0_UPPER Register (Offset = 20104h) [reset = 1070000h]

GITS_BASER0_upper

Return to Summary Table

Table 14-19225. Instance Table

Instance Name	Physical Address
GICSS0	**0182 0104h**

Figure 14-6379. GIC500_ITS_BASER0_UPPER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ITS__12_GITS_BASER0_UPPER__24_3</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ITS__12_GITS_BASER0_UPPER__16_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ITS__12_GITS_BASER0_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ITS__12_GITS_BASER0_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19227. GIC500_ITS_BASER0_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	ITS__12_GITS_BASER0_UPPER__24_3	R/W	1h	Type
23:16	ITS__12_GITS_BASER0_UPPER__16_8	R/W	7h	Entry Size
15:0	ITS__12_GITS_BASER0_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.787 GIC500_ITS_TRKCTLR Register

1 GIC500_ITS_TRKCTLR Register (Offset = 2C000h) [reset = 0h]

GITS_TRKCTLR

Return to Summary Table

Table 14-19228. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C000h**

Figure 14-6380. GIC500_ITS_TRKCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ITS__13_GITS_TRKCTLR__1_1	ITS__13_GITS_TRKCTLR__0_1
NONE						R/W	R/W
0h						0h	0h

Table 14-19230. GIC500_ITS_TRKCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	ITS__13_GITS_TRKCTLR__1_1	R/W	0h	ITS track
0	ITS__13_GITS_TRKCTLR__0_1	R/W	0h	Cache count reset

14.4.1.2.788 GIC500_ITS_TRKR Register

1 GIC500_ITS_TRKR Register (Offset = 2C004h) [reset = 0h]

GITS_TRKR

Return to Summary Table

Table 14-19231. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C004h**

Figure 14-6381. GIC500_ITS_TRKR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ITS__14_GITS_TRKR__5_1	ITS__14_GITS_TRKR__4_1	ITS__14_GITS_TRKR__3_1	ITS__14_GITS_TRKR__2_1	ITS__14_GITS_TRKR__1_1	ITS__14_GITS_TRKR__0_1
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-19233. GIC500_ITS_TRKR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ITS__14_GITS_TRKR__5_1	R/W	0h	Translated ID out of range
4	ITS__14_GITS_TRKR__4_1	R/W	0h	Target CPU out of range
3	ITS__14_GITS_TRKR__3_1	R/W	0h	DID/ID not mapped
2	ITS__14_GITS_TRKR__2_1	R/W	0h	Input ID out of range
1	ITS__14_GITS_TRKR__1_1	R/W	0h	DID unmapped
0	ITS__14_GITS_TRKR__0_1	R/W	0h	DID out of range

14.4.1.2.789 GIC500_ITS_TRKDIDR Register

1 GIC500_ITS_TRKDIDR Register (Offset = 2C008h) [reset = 0h]

GITS_TRKDIDR

Return to Summary Table

Table 14-19234. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C008h**

Figure 14-6382. GIC500_ITS_TRKDIDR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ITS__15_GITS_TRKDIDR__0_20</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ITS__15_GITS_TRKDIDR__0_20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ITS__15_GITS_TRKDIDR__0_20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19236. GIC500_ITS_TRKDIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	ITS__15_GITS_TRKDIDR__0_20	R/W	0h	DID

14.4.1.2.790 GIC500_ITS_TRKPIDR Register

1 GIC500_ITS_TRKPIDR Register (Offset = 2C00Ch) [reset = 0h]

GITS_TRKPIDR

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Table 14-19237. Instance Table

Instance Name	Physical Address
GICSS0	0182 C00Ch

Figure 14-6383. GIC500_ITS_TRKPIDR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ITS__16_GITS_TRKPIDR__0_16							
R/W							
0h							
7	6	5	4	3	2	1	0
ITS__16_GITS_TRKPIDR__0_16							
R/W							
0h							

Table 14-19239. GIC500_ITS_TRKPIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ITS__16_GITS_TRKPIDR__0_16	R/W	0h	Translated ID

14.4.1.2.791 GIC500_ITS_TRKVIDR Register

1 GIC500_ITS_TRKVIDR Register (Offset = 2C010h) [reset = 0h]

GITS_TRKVIDR

Return to Summary Table

Table 14-19240. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C010h**

Figure 14-6384. GIC500_ITS_TRKVIDR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITS__17_GITS_TRKVIDR__0_16							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITS__17_GITS_TRKVIDR__0_16							
R/W							
0h							

Table 14-19242. GIC500_ITS_TRKVIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ITS__17_GITS_TRKVIDR__0_16	R/W	0h	Input ID

14.4.1.2.792 GIC500_ITS_TRKTGTR Register

1 GIC500_ITS_TRKTGTR Register (Offset = 2C014h) [reset = 0h]

GITS_TRKTGTR

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Table 14-19243. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C014h**

Figure 14-6385. GIC500_ITS_TRKTGTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ITS__18_GITS_TRKTGTR__0_7						
NONE	R/W						
0h	0h						

Table 14-19245. GIC500_ITS_TRKTGTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	ITS__18_GITS_TRKTGTR__0_7	R/W	0h	Target CPU

14.4.1.2.793 GIC500_ITS_TRKICR Register

1 GIC500_ITS_TRKICR Register (Offset = 2C018h) [reset = 0h]

GITS_TRKICR

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Table 14-19246. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C018h**

Figure 14-6386. GIC500_ITS_TRKICR Name Register

31	30	29	28	27	26	25	24
ITS__19_GITS_TRKICR__16_16							
R/W							
0h							
23	22	21	20	19	18	17	16
ITS__19_GITS_TRKICR__16_16							
R/W							
0h							
15	14	13	12	11	10	9	8
ITS__19_GITS_TRKICR__0_16							
R/W							
0h							
7	6	5	4	3	2	1	0
ITS__19_GITS_TRKICR__0_16							
R/W							
0h							

Table 14-19248. GIC500_ITS_TRKICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ITS__19_GITS_TRKICR__16_16	R/W	0h	ITE cache hits
15:0	ITS__19_GITS_TRKICR__0_16	R/W	0h	ITE cache misses

14.4.1.2.794 GIC500_ITS_TRKLCR Register

1 GIC500_ITS_TRKLCR Register (Offset = 2C01Ch) [reset = 0h]

GITS_TRKLCR

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Table 14-19249. Instance Table

Instance Name	Physical Address
GICSS0	**0182 C01Ch**

Figure 14-6387. GIC500_ITS_TRKLCR Name Register

31	30	29	28	27	26	25	24
ITS__20_GITS_TRKLCR__16_16							
R/W							
0h							
23	22	21	20	19	18	17	16
ITS__20_GITS_TRKLCR__16_16							
R/W							
0h							
15	14	13	12	11	10	9	8
ITS__20_GITS_TRKLCR__0_16							
R/W							
0h							
7	6	5	4	3	2	1	0
ITS__20_GITS_TRKLCR__0_16							
R/W							
0h							

Table 14-19251. GIC500_ITS_TRKLCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ITS__20_GITS_TRKLCR__16_16	R/W	0h	LPI cache hits
15:0	ITS__20_GITS_TRKLCR__0_16	R/W	0h	LPI cache misses

14.4.1.2.795 GIC500_ITS_PIDR4 Register

1 GIC500_ITS_PIDR4 Register (Offset = 2FFD0h) [reset = 0h]

GITS_PIDR4

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Table 14-19252. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFD0h**

Figure 14-6388. GIC500_ITS_PIDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19254. GIC500_ITS_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.796 GIC500_ITS_PIDR5 Register

1 GIC500_ITS_PIDR5 Register (Offset = 2FFD4h) [reset = 0h]

GITS_PIDR5

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Table 14-19255. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFD4h**

Figure 14-6389. GIC500_ITS_PIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19257. GIC500_ITS_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.797 GIC500_ITS_PIDR6 Register

1 GIC500_ITS_PIDR6 Register (Offset = 2FFD8h) [reset = 0h]

GITS_PIDR6

Return to Summary Table

Table 14-19258. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFD8h**

Figure 14-6390. GIC500_ITS_PIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19260. GIC500_ITS_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.798 GIC500_ITS_PIDR7 Register

1 GIC500_ITS_PIDR7 Register (Offset = 2FFDCh) [reset = 0h]

GITS_PIDR7

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Table 14-19261. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFDCh**

Figure 14-6391. GIC500_ITS_PIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19263. GIC500_ITS_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.799 GIC500_ITS_PIDR0 Register

1 GIC500_ITS_PIDR0 Register (Offset = 2FFE0h) [reset = 0h]

GITS_PIDR0

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Table 14-19264. Instance Table

Instance Name	Physical Address
GICSS0	0182 FFE0h

Figure 14-6392. GIC500_ITS_PIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19266. GIC500_ITS_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.800 GIC500_ITS_PIDR1 Register

1 GIC500_ITS_PIDR1 Register (Offset = 2FFE4h) [reset = 0h]

GITS_PIDR1

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Table 14-19267. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFE4h**

Figure 14-6393. GIC500_ITS_PIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19269. GIC500_ITS_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.801 GIC500_ITS_PIDR2 Register

1 GIC500_ITS_PIDR2 Register (Offset = 2FFE8h) [reset = 0h]

GITS_PIDR2

Return to Summary Table

Table 14-19270. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFE8h**

Figure 14-6394. GIC500_ITS_PIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19272. GIC500_ITS_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.802 GIC500_ITS_PIDR3 Register

1 GIC500_ITS_PIDR3 Register (Offset = 2FFECh) [reset = 0h]

GITS_PIDR3

Return to Summary Table

Table 14-19273. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFECh**

Figure 14-6395. GIC500_ITS_PIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19275. GIC500_ITS_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.803 GIC500_ITS_CIDR0 Register

1 GIC500_ITS_CIDR0 Register (Offset = 2FFF0h) [reset = 0h]

GITS_CIDR0

Return to Summary Table

Table 14-19276. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFF0h**

Figure 14-6396. GIC500_ITS_CIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19278. GIC500_ITS_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.804 GIC500_ITS_CIDR1 Register

1 GIC500_ITS_CIDR1 Register (Offset = 2FFF4h) [reset = 0h]

GITS_CIDR1

Return to Summary Table

Table 14-19279. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFF4h**

Figure 14-6397. GIC500_ITS_CIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19281. GIC500_ITS_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.805 GIC500_ITS_CIDR2 Register

1 GIC500_ITS_CIDR2 Register (Offset = 2FFF8h) [reset = 0h]

GITS_CIDR2

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Table 14-19282. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFF8h**

Figure 14-6398. GIC500_ITS_CIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19284. GIC500_ITS_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.806 GIC500_ITS_CIDR3 Register

1 GIC500_ITS_CIDR3 Register (Offset = 2FFFCh) [reset = 0h]

GITS_CIDR3

Return to Summary Table

Table 14-19285. Instance Table

Instance Name	Physical Address
GICSS0	**0182 FFFCh**

Figure 14-6399. GIC500_ITS_CIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19287. GIC500_ITS_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.807 GIC500_GICR_CORE_CONTROL_CTLR_0 Register

1 GIC500_GICR_CORE_CONTROL_CTLR_0 Register (Offset = 40000h) [reset = 0h]

GICR_CTLR

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Table 14-19288. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0000h**

Figure 14-6400. GIC500_GICR_CORE_CONTROL_CTLR_0 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__3_1	RESERVED		REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__0_1
NONE				R/W	NONE		R/W
0h				0h	0h		0h

Table 14-19290. GIC500_GICR_CORE_CONTROL_CTLR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__31_1	R/W	0h	Upstream Write Pending
30:4	RESERVED	NONE	0h	Reserved
3	REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__3_1	R/W	0h	Register Write Pending
2:1	RESERVED	NONE	0h	Reserved
0	REDISTRIBUTOR_CONTROL_LPI_0__2_GICR_CTLR__0_1	R/W	0h	Enable LPIs

14.4.1.2.808 GIC500_GICR_CORE_CONTROL_IIDR_0 Register

1 GIC500_GICR_CORE_CONTROL_IIDR_0 Register (Offset = 40004h) [reset = 1143Bh]

GICR_IIDR

Return to Summary Table

Table 14-19291. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0004h**

Figure 14-6401. GIC500_GICR_CORE_CONTROL_IIDR_0 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__24_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__16_4			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__12_4				REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__0_12			
R/W				R/W			
1h				43Bh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__0_12							
R/W							
43Bh							

Table 14-19293. GIC500_GICR_CORE_CONTROL_IIDR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__24_8	R/W	0h	ProductID
23:20	RESERVED	NONE	0h	Reserved
19:16	REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__16_4	R/W	1h	Variant
15:12	REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__12_4	R/W	1h	Revision
11:0	REDISTRIBUTOR_CONTROL_LPI_0__3_GICR_IIDR__0_12	R/W	43Bh	Implementer

14.4.1.2.809 GIC500_GICR_CORE_CONTROL_TYPER_0_LOWER Register

1 GIC500_GICR_CORE_CONTROL_TYPER_0_LOWER Register (Offset = 40008h) [reset = 1h]

GICR_TYPER_lower

Return to Summary Table

Table 14-19294. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0008h**

Figure 14-6402. GIC500_GICR_CORE_CONTROL_TYPER_0_LOWER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__8_16							
R/W							
0h							
15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__8_16							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__4_1	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__3_1	RESERVED	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__1_1	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__0_1
NONE			R/W	R/W	NONE	R/W	R/W
0h			0h	0h	0h	0h	1h

Table 14-19296. GIC500_GICR_CORE_CONTROL_TYPER_0_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__8_16	R/W	0h	Processor Number
7:5	RESERVED	NONE	0h	Reserved
4	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__4_1	R/W	0h	Last
3	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__3_1	R/W	0h	Distributed
2	RESERVED	NONE	0h	Reserved
1	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__1_1	R/W	0h	VLPIS
0	REDISTRIBUTOR_CONTROL_LPI_0__4_GICR_TYPER_LOWER__0_1	R/W	1h	PLPIS

14.4.1.2.810 GIC500_GICR_CORE_CONTROL_TYPER_0_UPPER Register

1 GIC500_GICR_CORE_CONTROL_TYPER_0_UPPER Register (Offset = 4000Ch) [reset = 0h]

GICR_TYPER_upper

Return to Summary Table

Table 14-19297. Instance Table

Instance Name	Physical Address
GICSS0	**0184 000Ch**

Figure 14-6403. GIC500_GICR_CORE_CONTROL_TYPER_0_UPPER Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__24_8							
R/W							
0h							
23	22	21	20	19	18	17	16
REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__16_8							
R/W							
0h							
15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__0_8							
R/W							
0h							

Table 14-19299. GIC500_GICR_CORE_CONTROL_TYPER_0_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__24_8	R/W	0h	A3
23:16	REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__16_8	R/W	0h	A2
15:8	REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__8_8	R/W	0h	A1
7:0	REDISTRIBUTOR_CONTROL_LPI_0__5_GICR_TYPER_UPPER__0_8	R/W	0h	A0

14.4.1.2.811 GIC500_GICR_CORE_CONTROL_WAKER_0 Register

1 GIC500_GICR_CORE_CONTROL_WAKER_0 Register (Offset = 40014h) [reset = 6h]

GICR_WAKER

Return to Summary Table

Table 14-19300. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0014h**

Figure 14-6404. GIC500_GICR_CORE_CONTROL_WAKER_0 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__2_1	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__1_1	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__0_1
NONE					R/W	R/W	R/W
0h					1h	1h	0h

Table 14-19302. GIC500_GICR_CORE_CONTROL_WAKER_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__31_1	R/W	0h	Quiescent
30:3	RESERVED	NONE	0h	Reserved
2	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__2_1	R/W	1h	ChildrenAsleep
1	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__1_1	R/W	1h	ProcessorSleep
0	REDISTRIBUTOR_CONTROL_LPI_0__6_GICR_WAKER__0_1	R/W	0h	Sleep

14.4.1.2.812 GIC500_GICR_CORE_CONTROL_PROPBASER_0_LOWER Register

1 GIC500_GICR_CORE_CONTROL_PROPBASER_0_LOWER Register (Offset = 40070h) [reset = 0h]

GICR_PROPBASER_lower

Return to Summary Table

Table 14-19303. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0070h**

Figure 14-6405. GIC500_GICR_CORE_CONTROL_PROPBASER_0_LOWER Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__12_20							
R/W							
0h							

23	22	21	20	19	18	17	16
REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__12_20							
R/W							
0h							

15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__12_20				RESERVED		REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__7_3	
R/W				NONE		R/W	
0h				0h		0h	

7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__7_3	RESERVED		REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__0_5				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-19305. GIC500_GICR_CORE_CONTROL_PROPBASER_0_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__12_20	R/W	0h	Physical Address [31:12]
11:10	RESERVED	NONE	0h	Reserved
9:7	REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__7_3	R/W	0h	Cacheability
6:5	RESERVED	NONE	0h	Reserved
4:0	REDISTRIBUTOR_CONTROL_LPI_0__7_GICR_PROPBASER_LOWER__0_5	R/W	0h	Idbits

14.4.1.2.813 GIC500_GICR_CORE_CONTROL_PROPBASER_0_UPPER Register

1 GIC500_GICR_CORE_CONTROL_PROPBASER_0_UPPER Register (Offset = 40074h) [reset = 0h]

GICR_PROPBASER_upper

Return to Summary Table

Table 14-19306. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0074h**

Figure 14-6406. GIC500_GICR_CORE_CONTROL_PROPBASER_0_UPPER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_0__8_GICR_PROPBASER_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_0__8_GICR_PROPBASER_UPPER__0_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19308. GIC500_GICR_CORE_CONTROL_PROPBASER_0_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	REDISTRIBUTOR_CONTROL_LPI_0__8_GICR_PROPBASER_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.814 GIC500_GICR_CORE_CONTROL_PENDBASER_0_LOWER Register

1 GIC500_GICR_CORE_CONTROL_PENDBASER_0_LOWER Register (Offset = 40078h) [reset = 0h]

GICR_PENDBASER_lower

Return to Summary Table

Table 14-19309. Instance Table

Instance Name	Physical Address
GICSS0	**0184 0078h**

Figure 14-6407. GIC500_GICR_CORE_CONTROL_PENDBASER_0_LOWER Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__16_16							
R/W							
0h							
23	22	21	20	19	18	17	16
REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__16_16							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__7_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__7_3	RESERVED						
R/W	NONE						
0h	0h						

Table 14-19311. GIC500_GICR_CORE_CONTROL_PENDBASER_0_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__16_16	R/W	0h	Physical Address [31:16]
15:10	RESERVED	NONE	0h	Reserved
9:7	REDISTRIBUTOR_CONTROL_LPI_0__9_GICR_PENDBASER_LOWER__7_3	R/W	0h	Cacheability
6:0	RESERVED	NONE	0h	Reserved

14.4.1.2.815 GIC500_GICR_CORE_CONTROL_PENDBASER_0_UPPER Register

1 GIC500_GICR_CORE_CONTROL_PENDBASER_0_UPPER Register (Offset = 4007Ch) [reset = 0h]

GICR_PENDBASER_upper

Return to Summary Table

Table 14-19312. Instance Table

Instance Name	Physical Address
GICSS0	**0184 007Ch**

Figure 14-6408. GIC500_GICR_CORE_CONTROL_PENDBASER_0_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED	REDISTRIBUTOR_CONTROL_LPI_0__10_GICR_PENDBASER_UPPER__30_1	RESERVED					
NONE	R/W	NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_0__10_GICR_PENDBASER_UPPER__0_16							
R/W							
0h							

7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_0__10_GICR_PENDBASER_UPPER__0_16							
R/W							
0h							

Table 14-19314. GIC500_GICR_CORE_CONTROL_PENDBASER_0_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30	REDISTRIBUTOR_CONTROL_LPI_0__10_GICR_PENDBASER_UPPER__30_1	R/W	0h	Pending Table Zero
29:16	RESERVED	NONE	0h	Reserved
15:0	REDISTRIBUTOR_CONTROL_LPI_0__10_GICR_PENDBASER_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.816 GIC500_GICR_CORE_CONTROL_PIDR4_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR4_0 Register (Offset = 4FFD0h) [reset = 0h]

GICR_PIDR4

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Table 14-19315. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFD0h**

Figure 14-6409. GIC500_GICR_CORE_CONTROL_PIDR4_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19317. GIC500_GICR_CORE_CONTROL_PIDR4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.817 GIC500_GICR_CORE_CONTROL_PIDR5_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR5_0 Register (Offset = 4FFD4h) [reset = 0h]

GICR_PIDR5

Return to Summary Table

Table 14-19318. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFD4h**

Figure 14-6410. GIC500_GICR_CORE_CONTROL_PIDR5_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19320. GIC500_GICR_CORE_CONTROL_PIDR5_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.818 GIC500_GICR_CORE_CONTROL_PIDR6_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR6_0 Register (Offset = 4FFD8h) [reset = 0h]

GICR_PIDR6

Return to Summary Table

Table 14-19321. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFD8h**

Figure 14-6411. GIC500_GICR_CORE_CONTROL_PIDR6_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19323. GIC500_GICR_CORE_CONTROL_PIDR6_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.819 GIC500_GICR_CORE_CONTROL_PIDR7_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR7_0 Register (Offset = 4FFDCh) [reset = 0h]

GICR_PIDR7

Return to Summary Table

Table 14-19324. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFDCh**

Figure 14-6412. GIC500_GICR_CORE_CONTROL_PIDR7_0 Name Register

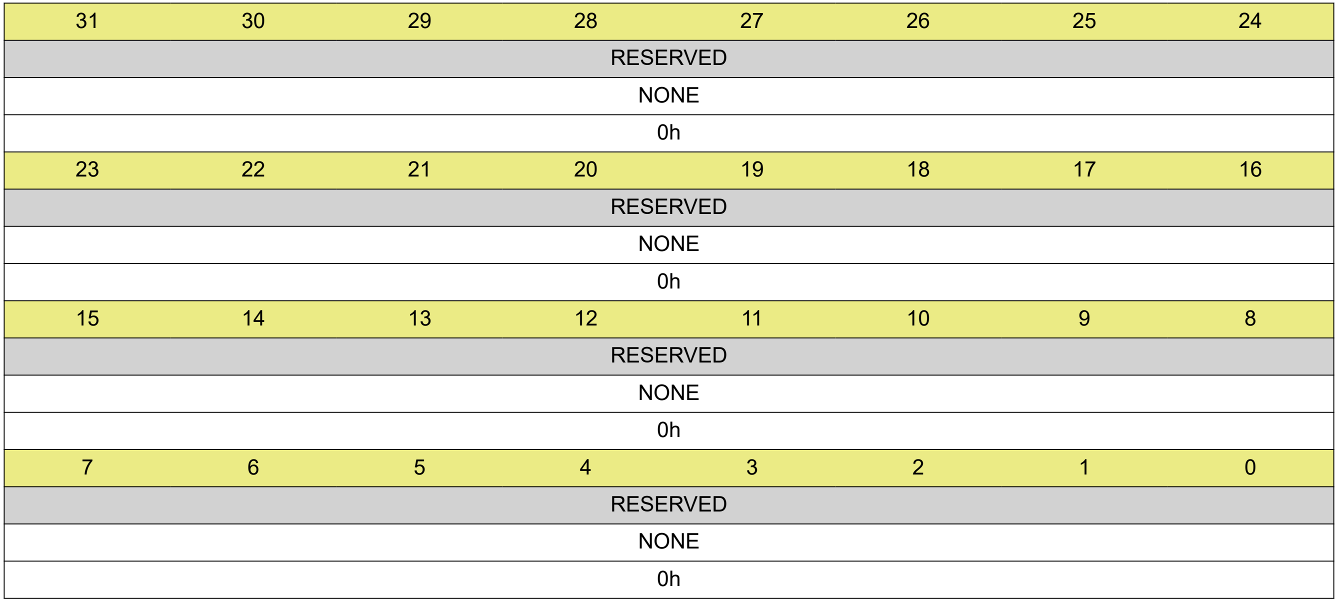

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19326. GIC500_GICR_CORE_CONTROL_PIDR7_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.820 GIC500_GICR_CORE_CONTROL_PIDR0_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR0_0 Register (Offset = 4FFE0h) [reset = 0h]

GICR_PIDR0

Return to Summary Table

Table 14-19327. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFE0h**

Figure 14-6413. GIC500_GICR_CORE_CONTROL_PIDR0_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19329. GIC500_GICR_CORE_CONTROL_PIDR0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.821 GIC500_GICR_CORE_CONTROL_PIDR1_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR1_0 Register (Offset = 4FFE4h) [reset = 0h]

GICR_PIDR1

Return to Summary Table

Table 14-19330. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFE4h**

Figure 14-6414. GIC500_GICR_CORE_CONTROL_PIDR1_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19332. GIC500_GICR_CORE_CONTROL_PIDR1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.822 GIC500_GICR_CORE_CONTROL_PIDR2_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR2_0 Register (Offset = 4FFE8h) [reset = 0h]

GICR_PIDR2

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Table 14-19333. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFE8h**

Figure 14-6415. GIC500_GICR_CORE_CONTROL_PIDR2_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19335. GIC500_GICR_CORE_CONTROL_PIDR2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.823 GIC500_GICR_CORE_CONTROL_PIDR3_0 Register

1 GIC500_GICR_CORE_CONTROL_PIDR3_0 Register (Offset = 4FFECh) [reset = 0h]

GICR_PIDR3

Return to Summary Table

Table 14-19336. Instance Table

Instance Name	Physical Address
GICSS0	0184 FFECh

Figure 14-6416. GIC500_GICR_CORE_CONTROL_PIDR3_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19338. GIC500_GICR_CORE_CONTROL_PIDR3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.824 GIC500_GICR_CORE_CONTROL_CIDR0_0 Register

1 GIC500_GICR_CORE_CONTROL_CIDR0_0 Register (Offset = 4FFF0h) [reset = 0h]

GICR_CIDR0

Return to Summary Table

Table 14-19339. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFF0h**

Figure 14-6417. GIC500_GICR_CORE_CONTROL_CIDR0_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19341. GIC500_GICR_CORE_CONTROL_CIDR0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.825 GIC500_GICR_CORE_CONTROL_CIDR1_0 Register

1 GIC500_GICR_CORE_CONTROL_CIDR1_0 Register (Offset = 4FFF4h) [reset = 0h]

GICR_CIDR1

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Table 14-19342. Instance Table

Instance Name	Physical Address
GICSS0	0184 FFF4h

Figure 14-6418. GIC500_GICR_CORE_CONTROL_CIDR1_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19344. GIC500_GICR_CORE_CONTROL_CIDR1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.826 GIC500_GICR_CORE_CONTROL_CIDR2_0 Register

1 GIC500_GICR_CORE_CONTROL_CIDR2_0 Register (Offset = 4FFF8h) [reset = 0h]

GICR_CIDR2

Return to Summary Table

Table 14-19345. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFF8h**

Figure 14-6419. GIC500_GICR_CORE_CONTROL_CIDR2_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19347. GIC500_GICR_CORE_CONTROL_CIDR2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.827 GIC500_GICR_CORE_CONTROL_CIDR3_0 Register

1 GIC500_GICR_CORE_CONTROL_CIDR3_0 Register (Offset = 4FFFCh) [reset = 0h]

GICR_CIDR3

Return to Summary Table

Table 14-19348. Instance Table

Instance Name	Physical Address
GICSS0	**0184 FFFCh**

Figure 14-6420. GIC500_GICR_CORE_CONTROL_CIDR3_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19350. GIC500_GICR_CORE_CONTROL_CIDR3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.828 GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register

1 GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register (Offset = 70080h) [reset = 0h]

GICR_IGROUPR0

Return to Summary Table

Table 14-19351. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0080h**

Figure 14-6421. GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19353. GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.829 GIC500_GICR_CORE_SGI_PPI_ISENABLER00 Register

1 GIC500_GICR_CORE_SGI_PPI_ISENABLER00 Register (Offset = 50100h) [reset = 0h]

GICR_ISENABLER0

Return to Summary Table

Table 14-19354. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0100h**

Figure 14-6422. GIC500_GICR_CORE_SGI_PPI_ISENABLER00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19356. GIC500_GICR_CORE_SGI_PPI_ISENABLER00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.830 GIC500_GICR_CORE_SGI_PPI_ICENABLER00 Register

1 GIC500_GICR_CORE_SGI_PPI_ICENABLER00 Register (Offset = 50180h) [reset = 0h]

GICR_ICENABLER0

Return to Summary Table

Table 14-19357. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0180h**

Figure 14-6423. GIC500_GICR_CORE_SGI_PPI_ICENABLER00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19359. GIC500_GICR_CORE_SGI_PPI_ICENABLER00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.831 GIC500_GICR_CORE_SGI_PPI_ISPENDR00 Register

1 GIC500_GICR_CORE_SGI_PPI_ISPENDR00 Register (Offset = 50200h) [reset = 0h]

GICR_ISPENDR0

Return to Summary Table

Table 14-19360. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0200h**

Figure 14-6424. GIC500_GICR_CORE_SGI_PPI_ISPENDR00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19362. GIC500_GICR_CORE_SGI_PPI_ISPENDR00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.832 GIC500_GICR_CORE_SGI_PPI_ICPENDR00 Register

1 GIC500_GICR_CORE_SGI_PPI_ICPENDR00 Register (Offset = 50280h) [reset = 0h]

GICR_ICPENDR0

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Table 14-19363. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0280h**

Figure 14-6425. GIC500_GICR_CORE_SGI_PPI_ICPENDR00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19365. GIC500_GICR_CORE_SGI_PPI_ICPENDR00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.833 GIC500_GICR_CORE_SGI_PPI_ISACTIVER00 Register

1 GIC500_GICR_CORE_SGI_PPI_ISACTIVER00 Register (Offset = 50300h) [reset = 0h]

GICR_ISACTIVER0

Return to Summary Table

Table 14-19366. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0300h**

Figure 14-6426. GIC500_GICR_CORE_SGI_PPI_ISACTIVER00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19368. GIC500_GICR_CORE_SGI_PPI_ISACTIVER00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.834 GIC500_GICR_CORE_SGI_PPI_ICACTIVER00 Register

1 GIC500_GICR_CORE_SGI_PPI_ICACTIVER00 Register (Offset = 50380h) [reset = 0h]

GICR_ICACTIVER0

Return to Summary Table

Table 14-19369. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0380h**

Figure 14-6427. GIC500_GICR_CORE_SGI_PPI_ICACTIVER00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19371. GIC500_GICR_CORE_SGI_PPI_ICACTIVER00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.835 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR00 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR00 Register (Offset = 50400h) [reset = 0h]

GICR_IPRIORITYR0

Return to Summary Table

Table 14-19372. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0400h**

Figure 14-6428. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19374. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.836 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR10 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR10 Register (Offset = 50404h) [reset = 0h]

GICR_IPRIORITYR1

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Table 14-19375. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0404h**

Figure 14-6429. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19377. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.837 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR20 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR20 Register (Offset = 50408h) [reset = 0h]

GICR_IPRIORITYR2

Return to Summary Table

Table 14-19378. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0408h**

Figure 14-6430. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19380. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.838 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR30 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR30 Register (Offset = 5040Ch) [reset = 0h]

GICR_IPRIORITYR3

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Table 14-19381. Instance Table

Instance Name	Physical Address
GICSS0	**0185 040Ch**

Figure 14-6431. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19383. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.839 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR40 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR40 Register (Offset = 50410h) [reset = 0h]

GICR_IPRIORITYR4

Return to Summary Table

Table 14-19384. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0410h**

Figure 14-6432. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR40 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19386. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.840 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR50 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR50 Register (Offset = 50414h) [reset = 0h]

GICR_IPRIORITYR5

Return to Summary Table

Table 14-19387. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0414h**

Figure 14-6433. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19389. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.841 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR60 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR60 Register (Offset = 50418h) [reset = 0h]

GICR_IPRIORITYR6

Return to Summary Table

Table 14-19390. Instance Table

Instance Name	Physical Address
GICSS0	0185 0418h

Figure 14-6434. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR60 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19392. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.842 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR70 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR70 Register (Offset = 5041Ch) [reset = 0h]

GICR_IPRIORITYR7

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Table 14-19393. Instance Table

Instance Name	Physical Address
GICSS0	**0185 041Ch**

Figure 14-6435. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR70 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19395. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.843 GIC500_GICR_CORE_SGI_PPI_ICFGR00 Register

1 GIC500_GICR_CORE_SGI_PPI_ICFGR00 Register (Offset = 50C00h) [reset = 0h]

GICR_ICFGR0

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Table 14-19396. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0C00h**

Figure 14-6436. GIC500_GICR_CORE_SGI_PPI_ICFGR00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19398. GIC500_GICR_CORE_SGI_PPI_ICFGR00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.844 GIC500_GICR_CORE_SGI_PPI_ICFGR10 Register

1 GIC500_GICR_CORE_SGI_PPI_ICFGR10 Register (Offset = 50C04h) [reset = 0h]

GICR_ICFGR1

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Table 14-19399. Instance Table

Instance Name	Physical Address
GICSS0	0185 0C04h

Figure 14-6437. GIC500_GICR_CORE_SGI_PPI_ICFGR10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19401. GIC500_GICR_CORE_SGI_PPI_ICFGR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.845 GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register

1 GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register (Offset = 70D00h) [reset = 0h]

GICR_IGRPMODR0

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Table 14-19402. Instance Table

Instance Name	Physical Address
GICSS0	0187 0D00h

Figure 14-6438. GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19404. GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.846 GIC500_GICR_CORE_SGI_PPI_NSACR0 Register

1 GIC500_GICR_CORE_SGI_PPI_NSACR0 Register (Offset = 50E00h) [reset = 0h]

GICR_NSACR

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Table 14-19405. Instance Table

Instance Name	Physical Address
GICSS0	**0185 0E00h**

Figure 14-6439. GIC500_GICR_CORE_SGI_PPI_NSACR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19407. GIC500_GICR_CORE_SGI_PPI_NSACR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.847 GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR0 Register

1 GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR0 Register (Offset = 5C000h) [reset = 0h]

GICR_MISCSTATUSR

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Table 14-19408. Instance Table

Instance Name	Physical Address
GICSS0	**0185 C000h**

Figure 14-6440. GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR0 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__31_1	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__2_1	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__1_1	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__0_1
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-19410. GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__31_1	R/W	0h	cpu_active
30:3	RESERVED	NONE	0h	Reserved
2	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__2_1	R/W	0h	EnableGrp1_S
1	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__1_1	R/W	0h	EnableGrp1_NS
0	REDISTRIBUTOR_SGI_PPI_0__13_GICR_MISCSTATUSR__0_1	R/W	0h	EnableGrp0

14.4.1.2.848 GIC500_GICR_CORE_SGI_PPI_PPISR0 Register

1 GIC500_GICR_CORE_SGI_PPI_PPISR0 Register (Offset = 5C080h) [reset = 0h]

GICR_PPISR

Return to Summary Table

Table 14-19411. Instance Table

Instance Name	Physical Address
GICSS0	**0185 C080h**

Figure 14-6441. GIC500_GICR_CORE_SGI_PPI_PPISR0 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_SGI_PPI_0__14_GICR_PPISR__16_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REDISTRIBUTOR_SGI_PPI_0__14_GICR_PPISR__16_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-19413. GIC500_GICR_CORE_SGI_PPI_PPISR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	REDISTRIBUTOR_SGI_PPI_0__14_GICR_PPISR__16_16	R/W	0h	PPI status
15:0	RESERVED	NONE	0h	Reserved

14.4.1.2.849 GIC500_GICR_CORE_CONTROL_CTLR_1 Register

1 GIC500_GICR_CORE_CONTROL_CTLR_1 Register (Offset = 60000h) [reset = 0h]

GICR_CTLR

Return to Summary Table

Table 14-19414. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0000h**

Figure 14-6442. GIC500_GICR_CORE_CONTROL_CTLR_1 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__3_1	RESERVED		REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__0_1
NONE				R/W	NONE		R/W
0h				0h	0h		0h

Table 14-19416. GIC500_GICR_CORE_CONTROL_CTLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__31_1	R/W	0h	Upstream Write Pending
30:4	RESERVED	NONE	0h	Reserved
3	REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__3_1	R/W	0h	Register Write Pending
2:1	RESERVED	NONE	0h	Reserved
0	REDISTRIBUTOR_CONTROL_LPI_1__2_GICR_CTLR__0_1	R/W	0h	Enable LPIs

14.4.1.2.850 GIC500_GICR_CORE_CONTROL_IIDR_1 Register

1 GIC500_GICR_CORE_CONTROL_IIDR_1 Register (Offset = 60004h) [reset = 1143Bh]

GICR_IIDR

Return to Summary Table

Table 14-19417. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0004h**

Figure 14-6443. GIC500_GICR_CORE_CONTROL_IIDR_1 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__24_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__16_4			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__12_4				REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__0_12			
R/W				R/W			
1h				43Bh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__0_12							
R/W							
43Bh							

Table 14-19419. GIC500_GICR_CORE_CONTROL_IIDR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__24_8	R/W	0h	ProductID
23:20	RESERVED	NONE	0h	Reserved
19:16	REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__16_4	R/W	1h	Variant
15:12	REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__12_4	R/W	1h	Revision
11:0	REDISTRIBUTOR_CONTROL_LPI_1__3_GICR_IIDR__0_12	R/W	43Bh	Implementer

14.4.1.2.851 GIC500_GICR_CORE_CONTROL_TYPER_1_LOWER Register

1 GIC500_GICR_CORE_CONTROL_TYPER_1_LOWER Register (Offset = 60008h) [reset = 1h]

GICR_TYPER_lower

Return to Summary Table

Table 14-19420. Instance Table

Instance Name	Physical Address
GICSS0	0186 0008h

Figure 14-6444. GIC500_GICR_CORE_CONTROL_TYPER_1_LOWER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__8_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__8_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__4_1</td><td>REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__3_1</td><td>RESERVED</td><td>REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__1_1</td><td>REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__0_1</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-19422. GIC500_GICR_CORE_CONTROL_TYPER_1_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__8_16	R/W	0h	Processor Number
7:5	RESERVED	NONE	0h	Reserved
4	REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__4_1	R/W	0h	Last
3	REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__3_1	R/W	0h	Distributed
2	RESERVED	NONE	0h	Reserved
1	REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__1_1	R/W	0h	VLPIS
0	REDISTRIBUTOR_CONTROL_LPI_1__4_GICR_TYPER_LOWER__0_1	R/W	1h	PLPIS

14.4.1.2.852 GIC500_GICR_CORE_CONTROL_TYPER_1_UPPER Register

1 GIC500_GICR_CORE_CONTROL_TYPER_1_UPPER Register (Offset = 6000Ch) [reset = 0h]

GICR_TYPER_upper

Return to Summary Table

Table 14-19423. Instance Table

Instance Name	Physical Address
GICSS0	0186 000Ch

Figure 14-6445. GIC500_GICR_CORE_CONTROL_TYPER_1_UPPER Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__24_8							
R/W							
0h							
23	22	21	20	19	18	17	16
REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__16_8							
R/W							
0h							
15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__8_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__0_8							
R/W							
0h							

Table 14-19425. GIC500_GICR_CORE_CONTROL_TYPER_1_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__24_8	R/W	0h	A3
23:16	REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__16_8	R/W	0h	A2
15:8	REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__8_8	R/W	0h	A1
7:0	REDISTRIBUTOR_CONTROL_LPI_1__5_GICR_TYPER_UPPER__0_8	R/W	0h	A0

14.4.1.2.853 GIC500_GICR_CORE_CONTROL_WAKER_1 Register

1 GIC500_GICR_CORE_CONTROL_WAKER_1 Register (Offset = 60014h) [reset = 6h]

GICR_WAKER

Return to Summary Table

Table 14-19426. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0014h**

Figure 14-6446. GIC500_GICR_CORE_CONTROL_WAKER_1 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__2_1	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__1_1	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__0_1
NONE					R/W	R/W	R/W
0h					1h	1h	0h

Table 14-19428. GIC500_GICR_CORE_CONTROL_WAKER_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__31_1	R/W	0h	Quiescent
30:3	RESERVED	NONE	0h	Reserved
2	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__2_1	R/W	1h	ChildrenAsleep
1	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__1_1	R/W	1h	ProcessorSleep
0	REDISTRIBUTOR_CONTROL_LPI_1__6_GICR_WAKER__0_1	R/W	0h	Sleep

14.4.1.2.854 GIC500_GICR_CORE_CONTROL_PROPBASER_1_LOWER Register

1 GIC500_GICR_CORE_CONTROL_PROPBASER_1_LOWER Register (Offset = 60070h) [reset = 0h]

GICR_PROPBASER_lower

Return to Summary Table

Table 14-19429. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0070h**

Figure 14-6447. GIC500_GICR_CORE_CONTROL_PROPBASER_1_LOWER Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__12_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__12_20							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__12_20				RESERVED		REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__7_3	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__7_3	RESERVED		REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__0_5				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-19431. GIC500_GICR_CORE_CONTROL_PROPBASER_1_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__12_20	R/W	0h	Physical Address [31:12]
11:10	RESERVED	NONE	0h	Reserved
9:7	REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__7_3	R/W	0h	Cacheability
6:5	RESERVED	NONE	0h	Reserved
4:0	REDISTRIBUTOR_CONTROL_LPI_1__7_GICR_PROPBASER_LOWER__0_5	R/W	0h	Idbits

14.4.1.2.855 GIC500_GICR_CORE_CONTROL_PROPBASER_1_UPPER Register

1 GIC500_GICR_CORE_CONTROL_PROPBASER_1_UPPER Register (Offset = 60074h) [reset = 0h]

GICR_PROPBASER_upper

Return to Summary Table

Table 14-19432. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0074h**

Figure 14-6448. GIC500_GICR_CORE_CONTROL_PROPBASER_1_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_1__8_GICR_PROPBASER_UPPER__0_16							
R/W							
0h							
7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_1__8_GICR_PROPBASER_UPPER__0_16							
R/W							
0h							

Table 14-19434. GIC500_GICR_CORE_CONTROL_PROPBASER_1_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	REDISTRIBUTOR_CONTROL_LPI_1__8_GICR_PROPBASER_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.856 GIC500_GICR_CORE_CONTROL_PENDBASER_1_LOWER Register

1 GIC500_GICR_CORE_CONTROL_PENDBASER_1_LOWER Register (Offset = 60078h) [reset = 0h]

GICR_PENDBASER_lower

Return to Summary Table

Table 14-19435. Instance Table

Instance Name	Physical Address
GICSS0	**0186 0078h**

Figure 14-6449. GIC500_GICR_CORE_CONTROL_PENDBASER_1_LOWER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__16_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__16_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__7_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__7_3</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-19437. GIC500_GICR_CORE_CONTROL_PENDBASER_1_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__16_16	R/W	0h	Physical Address [31:16]
15:10	RESERVED	NONE	0h	Reserved
9:7	REDISTRIBUTOR_CONTROL_LPI_1__9_GICR_PENDBASER_LOWER__7_3	R/W	0h	Cacheability
6:0	RESERVED	NONE	0h	Reserved

14.4.1.2.857 GIC500_GICR_CORE_CONTROL_PENDBASER_1_UPPER Register

1 GIC500_GICR_CORE_CONTROL_PENDBASER_1_UPPER Register (Offset = 6007Ch) [reset = 0h]

GICR_PENDBASER_upper

Return to Summary Table

Table 14-19438. Instance Table

Instance Name	Physical Address
GICSS0	**0186 007Ch**

Figure 14-6450. GIC500_GICR_CORE_CONTROL_PENDBASER_1_UPPER Name Register

31	30	29	28	27	26	25	24
RESERVED	REDISTRIBUTOR_CONTROL_LPI_1__10_GICR_PENDBASER_UPPER__30_1	RESERVED					
NONE	R/W	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
REDISTRIBUTOR_CONTROL_LPI_1__10_GICR_PENDBASER_UPPER__0_16							
R/W							
0h							
7	6	5	4	3	2	1	0
REDISTRIBUTOR_CONTROL_LPI_1__10_GICR_PENDBASER_UPPER__0_16							
R/W							
0h							

Table 14-19440. GIC500_GICR_CORE_CONTROL_PENDBASER_1_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30	REDISTRIBUTOR_CONTROL_LPI_1__10_GICR_PENDBASER_UPPER__30_1	R/W	0h	Pending Table Zero
29:16	RESERVED	NONE	0h	Reserved
15:0	REDISTRIBUTOR_CONTROL_LPI_1__10_GICR_PENDBASER_UPPER__0_16	R/W	0h	Physical Address [47:32]

14.4.1.2.858 GIC500_GICR_CORE_CONTROL_PIDR4_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR4_1 Register (Offset = 6FFD0h) [reset = 0h]

GICR_PIDR4

Return to Summary Table

Table 14-19441. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFD0h**

Figure 14-6451. GIC500_GICR_CORE_CONTROL_PIDR4_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19443. GIC500_GICR_CORE_CONTROL_PIDR4_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.859 GIC500_GICR_CORE_CONTROL_PIDR5_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR5_1 Register (Offset = 6FFD4h) [reset = 0h]

GICR_PIDR5

Return to Summary Table

Table 14-19444. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFD4h**

Figure 14-6452. GIC500_GICR_CORE_CONTROL_PIDR5_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19446. GIC500_GICR_CORE_CONTROL_PIDR5_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.860 GIC500_GICR_CORE_CONTROL_PIDR6_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR6_1 Register (Offset = 6FFD8h) [reset = 0h]

GICR_PIDR6

Return to Summary Table

Table 14-19447. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFD8h**

Figure 14-6453. GIC500_GICR_CORE_CONTROL_PIDR6_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19449. GIC500_GICR_CORE_CONTROL_PIDR6_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.861 GIC500_GICR_CORE_CONTROL_PIDR7_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR7_1 Register (Offset = 6FFDCh) [reset = 0h]

GICR_PIDR7

Return to Summary Table

Table 14-19450. Instance Table

Instance Name	Physical Address
GICSS0	0186 FFDCh

Figure 14-6454. GIC500_GICR_CORE_CONTROL_PIDR7_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19452. GIC500_GICR_CORE_CONTROL_PIDR7_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.862 GIC500_GICR_CORE_CONTROL_PIDR0_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR0_1 Register (Offset = 6FFE0h) [reset = 0h]

GICR_PIDR0

Return to Summary Table

Table 14-19453. Instance Table

Instance Name	Physical Address
GICSS0	0186 FFE0h

Figure 14-6455. GIC500_GICR_CORE_CONTROL_PIDR0_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19455. GIC500_GICR_CORE_CONTROL_PIDR0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.863 GIC500_GICR_CORE_CONTROL_PIDR1_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR1_1 Register (Offset = 6FFE4h) [reset = 0h]

GICR_PIDR1

Return to Summary Table

Table 14-19456. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFE4h**

Figure 14-6456. GIC500_GICR_CORE_CONTROL_PIDR1_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19458. GIC500_GICR_CORE_CONTROL_PIDR1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.864 GIC500_GICR_CORE_CONTROL_PIDR2_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR2_1 Register (Offset = 6FFE8h) [reset = 0h]

GICR_PIDR2

Return to Summary Table

Table 14-19459. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFE8h**

Figure 14-6457. GIC500_GICR_CORE_CONTROL_PIDR2_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19461. GIC500_GICR_CORE_CONTROL_PIDR2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.865 GIC500_GICR_CORE_CONTROL_PIDR3_1 Register

1 GIC500_GICR_CORE_CONTROL_PIDR3_1 Register (Offset = 6FFECh) [reset = 0h]

GICR_PIDR3

Return to Summary Table

Table 14-19462. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFECh**

Figure 14-6458. GIC500_GICR_CORE_CONTROL_PIDR3_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19464. GIC500_GICR_CORE_CONTROL_PIDR3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.866 GIC500_GICR_CORE_CONTROL_CIDR0_1 Register

1 GIC500_GICR_CORE_CONTROL_CIDR0_1 Register (Offset = 6FFF0h) [reset = 0h]

GICR_CIDR0

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Table 14-19465. Instance Table

Instance Name	Physical Address
GICSS0	0186 FFF0h

Figure 14-6459. GIC500_GICR_CORE_CONTROL_CIDR0_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19467. GIC500_GICR_CORE_CONTROL_CIDR0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.867 GIC500_GICR_CORE_CONTROL_CIDR1_1 Register

1 GIC500_GICR_CORE_CONTROL_CIDR1_1 Register (Offset = 6FFF4h) [reset = 0h]

GICR_CIDR1

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Table 14-19468. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFF4h**

Figure 14-6460. GIC500_GICR_CORE_CONTROL_CIDR1_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19470. GIC500_GICR_CORE_CONTROL_CIDR1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.868 GIC500_GICR_CORE_CONTROL_CIDR2_1 Register

1 GIC500_GICR_CORE_CONTROL_CIDR2_1 Register (Offset = 6FFF8h) [reset = 0h]

GICR_CIDR2

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Table 14-19471. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFF8h**

Figure 14-6461. GIC500_GICR_CORE_CONTROL_CIDR2_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19473. GIC500_GICR_CORE_CONTROL_CIDR2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.869 GIC500_GICR_CORE_CONTROL_CIDR3_1 Register

1 GIC500_GICR_CORE_CONTROL_CIDR3_1 Register (Offset = 6FFFCh) [reset = 0h]

GICR_CIDR3

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Table 14-19474. Instance Table

Instance Name	Physical Address
GICSS0	**0186 FFFCh**

Figure 14-6462. GIC500_GICR_CORE_CONTROL_CIDR3_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19476. GIC500_GICR_CORE_CONTROL_CIDR3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.870 GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register

1 GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register (Offset = 70080h) [reset = 0h]

GICR_IGROUPR0

Return to Summary Table

Table 14-19477. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0080h**

Figure 14-6463. GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19479. GIC500_GICR_CORE_SGI_PPI_IGROUPR_SGI_PPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.871 GIC500_GICR_CORE_SGI_PPI_ISENABLER01 Register

1 GIC500_GICR_CORE_SGI_PPI_ISENABLER01 Register (Offset = 70100h) [reset = 0h]

GICR_ISENABLER0

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Table 14-19480. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0100h**

Figure 14-6464. GIC500_GICR_CORE_SGI_PPI_ISENABLER01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19482. GIC500_GICR_CORE_SGI_PPI_ISENABLER01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.872 GIC500_GICR_CORE_SGI_PPI_ICENABLER01 Register

1 GIC500_GICR_CORE_SGI_PPI_ICENABLER01 Register (Offset = 70180h) [reset = 0h]

GICR_ICENABLER0

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Table 14-19483. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0180h**

Figure 14-6465. GIC500_GICR_CORE_SGI_PPI_ICENABLER01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19485. GIC500_GICR_CORE_SGI_PPI_ICENABLER01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.873 GIC500_GICR_CORE_SGI_PPI_ISPENDR01 Register

1 GIC500_GICR_CORE_SGI_PPI_ISPENDR01 Register (Offset = 70200h) [reset = 0h]

GICR_ISPENDR0

Return to Summary Table

Table 14-19486. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0200h**

Figure 14-6466. GIC500_GICR_CORE_SGI_PPI_ISPENDR01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19488. GIC500_GICR_CORE_SGI_PPI_ISPENDR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.874 GIC500_GICR_CORE_SGI_PPI_ICPENDR01 Register

1 GIC500_GICR_CORE_SGI_PPI_ICPENDR01 Register (Offset = 70280h) [reset = 0h]

GICR_ICPENDR0

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Table 14-19489. Instance Table

Instance Name	Physical Address
GICSS0	0187 0280h

Figure 14-6467. GIC500_GICR_CORE_SGI_PPI_ICPENDR01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19491. GIC500_GICR_CORE_SGI_PPI_ICPENDR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.875 GIC500_GICR_CORE_SGI_PPI_ISACTIVER01 Register

1 GIC500_GICR_CORE_SGI_PPI_ISACTIVER01 Register (Offset = 70300h) [reset = 0h]

GICR_ISACTIVER0

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Table 14-19492. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0300h**

Figure 14-6468. GIC500_GICR_CORE_SGI_PPI_ISACTIVER01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19494. GIC500_GICR_CORE_SGI_PPI_ISACTIVER01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.876 GIC500_GICR_CORE_SGI_PPI_ICACTIVER01 Register

1 GIC500_GICR_CORE_SGI_PPI_ICACTIVER01 Register (Offset = 70380h) [reset = 0h]

GICR_ICACTIVER0

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Table 14-19495. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0380h**

Figure 14-6469. GIC500_GICR_CORE_SGI_PPI_ICACTIVER01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19497. GIC500_GICR_CORE_SGI_PPI_ICACTIVER01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.877 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR01 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR01 Register (Offset = 70400h) [reset = 0h]

GICR_IPRIORITYR0

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Table 14-19498. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0400h**

Figure 14-6470. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19500. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.878 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR11 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR11 Register (Offset = 70404h) [reset = 0h]

GICR_IPRIORITYR1

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Table 14-19501. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0404h**

Figure 14-6471. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19503. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.879 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR21 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR21 Register (Offset = 70408h) [reset = 0h]

GICR_IPRIORITYR2

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Table 14-19504. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0408h**

Figure 14-6472. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19506. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.880 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR31 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR31 Register (Offset = 7040Ch) [reset = 0h]

GICR_IPRIORITYR3

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Table 14-19507. Instance Table

Instance Name	Physical Address
GICSS0	**0187 040Ch**

Figure 14-6473. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19509. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.881 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR41 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR41 Register (Offset = 70410h) [reset = 0h]

GICR_IPRIORITYR4

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Table 14-19510. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0410h**

Figure 14-6474. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19512. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.882 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR51 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR51 Register (Offset = 70414h) [reset = 0h]

GICR_IPRIORITYR5

Return to Summary Table

Table 14-19513. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0414h**

Figure 14-6475. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19515. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.883 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR61 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR61 Register (Offset = 70418h) [reset = 0h]

GICR_IPRIORITYR6

Return to Summary Table

Table 14-19516. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0418h**

Figure 14-6476. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR61 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19518. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.884 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR71 Register

1 GIC500_GICR_CORE_SGI_PPI_IPRIORITYR71 Register (Offset = 7041Ch) [reset = 0h]

GICR_IPRIORITYR7

Return to Summary Table

Table 14-19519. Instance Table

Instance Name	Physical Address
GICSS0	**0187 041Ch**

Figure 14-6477. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19521. GIC500_GICR_CORE_SGI_PPI_IPRIORITYR71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.885 GIC500_GICR_CORE_SGI_PPI_ICFGR01 Register

1 GIC500_GICR_CORE_SGI_PPI_ICFGR01 Register (Offset = 70C00h) [reset = 0h]

GICR_ICFGR0

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Table 14-19522. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0C00h**

Figure 14-6478. GIC500_GICR_CORE_SGI_PPI_ICFGR01 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19524. GIC500_GICR_CORE_SGI_PPI_ICFGR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.886 GIC500_GICR_CORE_SGI_PPI_ICFGR11 Register

1 GIC500_GICR_CORE_SGI_PPI_ICFGR11 Register (Offset = 70C04h) [reset = 0h]

GICR_ICFGR1

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Table 14-19525. Instance Table

Instance Name	Physical Address
GICSS0	0187 0C04h

Figure 14-6479. GIC500_GICR_CORE_SGI_PPI_ICFGR11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19527. GIC500_GICR_CORE_SGI_PPI_ICFGR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.887 GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register

1 GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register (Offset = 70D00h) [reset = 0h]

GICR_IGRPMODR0

Return to Summary Table

Table 14-19528. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0D00h**

Figure 14-6480. GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19530. GIC500_GICR_CORE_SGI_PPI_IGRPMODR_SGI_PPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.888 GIC500_GICR_CORE_SGI_PPI_NSACR1 Register

1 GIC500_GICR_CORE_SGI_PPI_NSACR1 Register (Offset = 70E00h) [reset = 0h]

GICR_NSACR

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Table 14-19531. Instance Table

Instance Name	Physical Address
GICSS0	**0187 0E00h**

Figure 14-6481. GIC500_GICR_CORE_SGI_PPI_NSACR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19533. GIC500_GICR_CORE_SGI_PPI_NSACR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.4.1.2.889 GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR1 Register

1 GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR1 Register (Offset = 7C000h) [reset = 0h]

GICR_MISCSTATUSR

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Table 14-19534. Instance Table

Instance Name	Physical Address
GICSS0	**0187 C000h**

Figure 14-6482. GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR1 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__31_1	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__2_1	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__1_1	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__0_1
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-19536. GIC500_GICR_CORE_SGI_PPI_MISCSTATUSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__31_1	R/W	0h	cpu_active
30:3	RESERVED	NONE	0h	Reserved
2	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__2_1	R/W	0h	EnableGrp1_S
1	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__1_1	R/W	0h	EnableGrp1_NS
0	REDISTRIBUTOR_SGI_PPI_1__13_GICR_MISCSTATUSR__0_1	R/W	0h	EnableGrp0

14.4.1.2.890 GIC500_GICR_CORE_SGI_PPI_PPISR1 Register

1 GIC500_GICR_CORE_SGI_PPI_PPISR1 Register (Offset = 7C080h) [reset = 0h]

GICR_PPISR

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Table 14-19537. Instance Table

Instance Name	Physical Address
GICSS0	**0187 C080h**

Figure 14-6483. GIC500_GICR_CORE_SGI_PPI_PPISR1 Name Register

31	30	29	28	27	26	25	24
REDISTRIBUTOR_SGI_PPI_1__14_GICR_PPISR__16_16							
R/W							
0h							
23	22	21	20	19	18	17	16
REDISTRIBUTOR_SGI_PPI_1__14_GICR_PPISR__16_16							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19539. GIC500_GICR_CORE_SGI_PPI_PPISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	REDISTRIBUTOR_SGI_PPI_1__14_GICR_PPISR__16_16	R/W	0h	PPI status
15:0	RESERVED	NONE	0h	Reserved

14.4.1.2.891 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-19540. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4000h**

Figure 14-6484. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
5h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19542. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.4.1.2.892 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19543. Instance Table

Instance Name	**Physical Address**
GICSS0	**3F00 4008h**

Figure 14-6485. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-19545. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.4.1.2.893 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 3h]

Misc Status

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Table 14-19546. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 400Ch**

Figure 14-6486. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-19548. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	3h	Indicates the number of RAMS serviced by the ECC aggregator

14.4.1.2.894 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-19549. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4010h + formula**

Figure 14-6487. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19551. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.4.1.2.895 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-19552. Instance Table

Instance Name	Physical Address
GICSS0	3F00 403Ch

Figure 14-6488. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19554. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.4.1.2.896 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19555. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4040h**

Figure 14-6489. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_PEND	ITE_RAMECC_PEND	ICB_RAMECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19557. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for lpi_ramecc_pend
1	ITE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ite_ramecc_pend
0	ICB_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for icb_ramecc_pend

14.4.1.2.897 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19558. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4080h**

Figure 14-6490. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_ENABLE_SET	ITE_RAMECC_ENABLE_SET	ICB_RAMECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19560. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for icb_ramecc_pend

14.4.1.2.898 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19561. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 40C0h**

Figure 14-6491. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_ENABLE_CLR	ITE_RAMECC_ENABLE_CLR	ICB_RAMECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-19563. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for icb_ramecc_pend

14.4.1.2.899 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19564. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 413Ch**

Figure 14-6492. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19566. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.4.1.2.900 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19567. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4140h**

Figure 14-6493. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_PEND	ITE_RAMECC_PEND	ICB_RAMECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19569. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for lpi_ramecc_pend
1	ITE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ite_ramecc_pend
0	ICB_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for icb_ramecc_pend

14.4.1.2.901 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19570. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4180h**

Figure 14-6494. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_ENABLE_SET	ITE_RAMECC_ENABLE_SET	ICB_RAMECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19572. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for icb_ramecc_pend

14.4.1.2.902 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-19573. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 41C0h**

Figure 14-6495. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LPI_RAMECC_ENABLE_CLR	ITE_RAMECC_ENABLE_CLR	ICB_RAMECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-19575. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LPI_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for icb_ramecc_pend

14.4.1.2.903 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-19576. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4200h**

Figure 14-6496. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19578. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.4.1.2.904 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-19579. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4204h**

Figure 14-6497. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-19581. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.4.1.2.905 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-19582. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 4208h**

Figure 14-6498. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19584. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.4.1.2.906 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-19585. Instance Table

Instance Name	Physical Address
GICSS0	**3F00 420Ch**

Figure 14-6499. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-19587. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.5 Interprocessor Communication Registers

14.5.1 Mailbox Registers

14.5.1.1 MAILBOX_MAILBOX_CLUSTER_0

MAILBOX_MAILBOX_CLUSTER_0

14.5.1.1.1 MAILBOX_MAILBOX_CLUSTER_0 Summaries

MAILBOX_MAILBOX_CLUSTER_0 Summaries

Table 14-19588. MAILBOX Registers, Base Address=2900 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_0 Physical Address
0h	32	MAILBOX_REVISION	2900 0000h
10h	32	MAILBOX_SYSCONFIG	2900 0010h
40h	32	MAILBOX_MESSAGE_J	2900 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2900 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2900 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2900 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2900 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2900 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2900 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2900 000Ch + formula

14.5.1.1.2 MAILBOX_MAILBOX_CLUSTER_0 Registers

MAILBOX_MAILBOX_CLUSTER_0 Registers

14.5.1.1.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FCA100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-19589. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0000h**

Figure 14-6500. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
14h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-19591. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	14h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.5.1.1.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-19592. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0010h**

Figure 14-6501. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-19594. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.5.1.1.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = 40h + (j * 4h); where j = 0 to 15d

Table 14-19595. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0040h + formula**

Figure 14-6502. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-19597. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.5.1.1.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = 80h + (j * 4h); where j = 0 to 15d

Table 14-19598. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0080h + formula**

Figure 14-6503. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-19600. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.5.1.1.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = C0h + (j * 4h); where j = 0 to 15d

Table 14-19601. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 00C0h + formula**

Figure 14-6504. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-19603. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.5.1.1.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-19604. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0140h**

Figure 14-6505. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-19606. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.5.1.1.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = 100h + (j * 10h); where j = 0 to 3d

Table 14-19607. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0000h + formula**

Figure 14-6506. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-19609. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-19609. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-19609. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.5.1.1.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = 104h + (j * 10h); where j = 0 to 3d

Table 14-19610. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0004h + formula**

Figure 14-6507. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19612. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-19612. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-19612. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.5.1.1.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 108h + (j * 10h); where j = 0 to 3d

Table 14-19613. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0008h + formula**

Figure 14-6508. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19615. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19615. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19615. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.1.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 10Ch + (j * 10h); where j = 0 to 3d

Table 14-19616. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 000Ch + formula**

Figure 14-6509. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19618. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19618. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19618. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.2 MAILBOX_MAILBOX_CLUSTER_1

MAILBOX_MAILBOX_CLUSTER_1

14.5.1.2.1 MAILBOX_MAILBOX_CLUSTER_1 Summaries

MAILBOX_MAILBOX_CLUSTER_1 Summaries

Table 14-19619. MAILBOX Registers, Base Address=2901 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_1 Physical Address
0h	32	MAILBOX_REVISION	2901 0000h
10h	32	MAILBOX_SYSCONFIG	2901 0010h
40h	32	MAILBOX_MESSAGE_J	2901 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2901 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2901 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2901 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2901 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2901 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2901 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2901 000Ch + formula

14.5.1.2.2 MAILBOX_MAILBOX_CLUSTER_1 Registers

MAILBOX_MAILBOX_CLUSTER_1 Registers

14.5.1.2.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FCA100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-19620. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0000h**

Figure 14-6510. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
6FCh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_REV		
R					R		
14h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-19622. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	14h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.5.1.2.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-19623. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0010h**

Figure 14-6511. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-19625. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.5.1.2.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = 40h + (j * 4h); where j = 0 to 15d

Table 14-19626. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0040h + formula**

Figure 14-6512. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-19628. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.5.1.2.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = 80h + (j * 4h); where j = 0 to 15d

Table 14-19629. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0080h + formula**

Figure 14-6513. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-19631. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.5.1.2.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = C0h + (j * 4h); where j = 0 to 15d

Table 14-19632. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 00C0h + formula**

Figure 14-6514. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-19634. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.5.1.2.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-19635. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0140h**

Figure 14-6515. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-19637. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.5.1.2.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = 100h + (j * 10h); where j = 0 to 3d

Table 14-19638. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0000h + formula**

Figure 14-6516. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-19640. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-19640. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-19640. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.5.1.2.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = 104h + (j * 10h); where j = 0 to 3d

Table 14-19641. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0004h + formula**

Figure 14-6517. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19643. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-19643. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-19643. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.5.1.2.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 108h + (j * 10h); where j = 0 to 3d

Table 14-19644. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0008h + formula**

Figure 14-6518. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19646. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19646. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19646. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.2.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 10Ch + (j * 10h); where j = 0 to 3d

Table 14-19647. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 000Ch + formula**

Figure 14-6519. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19649. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19649. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19649. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.3 MAILBOX_MAILBOX_CLUSTER_2

MAILBOX_MAILBOX_CLUSTER_2

14.5.1.3.1 MAILBOX_MAILBOX_CLUSTER_2 Summaries

MAILBOX_MAILBOX_CLUSTER_2 Summaries

Table 14-19650. MAILBOX Registers, Base Address=2902 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_2 Physical Address
0h	32	MAILBOX_REVISION	2902 0000h
10h	32	MAILBOX_SYSCONFIG	2902 0010h
40h	32	MAILBOX_MESSAGE_J	2902 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2902 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2902 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2902 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2902 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2902 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2902 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2902 000Ch + formula

14.5.1.3.2 MAILBOX_MAILBOX_CLUSTER_2 Registers

MAILBOX_MAILBOX_CLUSTER_2 Registers

14.5.1.3.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FCA100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-19651. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0000h**

Figure 14-6520. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">14h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-19653. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	14h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.5.1.3.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-19654. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0010h**

Figure 14-6521. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-19656. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.5.1.3.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = 40h + (j * 4h); where j = 0 to 15d

Table 14-19657. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0040h + formula**

Figure 14-6522. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-19659. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.5.1.3.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = 80h + (j * 4h); where j = 0 to 15d

Table 14-19660. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0080h + formula**

Figure 14-6523. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-19662. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.5.1.3.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = C0h + (j * 4h); where j = 0 to 15d

Table 14-19663. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 00C0h + formula**

Figure 14-6524. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-19665. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.5.1.3.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-19666. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0140h**

Figure 14-6525. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-19668. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.5.1.3.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = 100h + (j * 10h); where j = 0 to 3d

Table 14-19669. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0000h + formula**

Figure 14-6526. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-19671. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-19671. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-19671. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.5.1.3.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = 104h + (j * 10h); where j = 0 to 3d

Table 14-19672. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0004h + formula**

Figure 14-6527. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19674. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-19674. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-19674. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.5.1.3.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 108h + (j * 10h); where j = 0 to 3d

Table 14-19675. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0008h + formula**

Figure 14-6528. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19677. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19677. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19677. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.3.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 10Ch + (j * 10h); where j = 0 to 3d

Table 14-19678. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 000Ch + formula**

Figure 14-6529. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19680. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19680. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19680. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.4 MAILBOX_MAILBOX_CLUSTER_3

MAILBOX_MAILBOX_CLUSTER_3

14.5.1.4.1 MAILBOX_MAILBOX_CLUSTER_3 Summaries

MAILBOX_MAILBOX_CLUSTER_3 Summaries

Table 14-19681. MAILBOX Registers, Base Address=2903 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_3 Physical Address
0h	32	MAILBOX_REVISION	2903 0000h
10h	32	MAILBOX_SYSCONFIG	2903 0010h
40h	32	MAILBOX_MESSAGE_J	2903 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2903 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2903 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2903 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2903 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2903 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2903 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2903 000Ch + formula

14.5.1.4.2 MAILBOX_MAILBOX_CLUSTER_3 Registers

MAILBOX_MAILBOX_CLUSTER_3 Registers

14.5.1.4.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FCA100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-19682. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0000h**

Figure 14-6530. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">14h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-19684. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	14h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.5.1.4.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-19685. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0010h**

Figure 14-6531. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-19687. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.5.1.4.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = 40h + (j * 4h); where j = 0 to 15d

Table 14-19688. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0040h + formula**

Figure 14-6532. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-19690. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.5.1.4.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = 80h + (j * 4h); where j = 0 to 15d

Table 14-19691. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0080h + formula**

Figure 14-6533. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-19693. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.5.1.4.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = C0h + (j * 4h); where j = 0 to 15d

Table 14-19694. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 00C0h + formula**

Figure 14-6534. MAILBOX_MSG_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_MESSAGES</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-19696. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.5.1.4.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-19697. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0140h**

Figure 14-6535. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-19699. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.5.1.4.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = 100h + (j * 10h); where j = 0 to 3d

Table 14-19700. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0000h + formula**

Figure 14-6536. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-19702. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-19702. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-19702. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.5.1.4.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = 104h + (j * 10h); where j = 0 to 3d

Table 14-19703. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0004h + formula**

Figure 14-6537. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19705. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-19705. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-19705. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.5.1.4.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 108h + (j * 10h); where j = 0 to 3d

Table 14-19706. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0008h + formula**

Figure 14-6538. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19708. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19708. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19708. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.1.4.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = 10Ch + (j * 10h); where j = 0 to 3d

Table 14-19709. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 000Ch + formula**

Figure 14-6539. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19711. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19711. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-19711. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.5.2 Spinlock Registers

14.5.2.1 SPINLOCK

SPINLOCK

14.5.2.1.1 SPINLOCK Summaries

SPINLOCK Summaries

Table 14-19712. SPINLOCK Registers, Base Address=2A00 0000h, Length=32768

Offset	Length	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	2A00 0000h
10h	32	SPINLOCK_SYSCONFIG	2A00 0010h
14h	32	SPINLOCK_SYSTATUS	2A00 0014h
800h	32	SPINLOCK_LOCK_REG_J	2A00 0800h + formula

14.5.2.1.2 SPINLOCK Registers

SPINLOCK Registers

14.5.2.1.2.1 SPINLOCK_REVISION Register

1 SPINLOCK_REVISION Register (Offset = 0h) [reset = 66FA6900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-19713. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0000h**

Figure 14-6540. SPINLOCK_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FAh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FAh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
Dh					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-19715. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: core_srst_n
29:28	BU	R	2h	BU identifier Reset Source: core_srst_n
27:16	FUNCTION	R	6FAh	Module family. Reset Source: core_srst_n
15:11	RTL_VER	R	Dh	RTL version. R of X.Y.R.Z Reset Source: core_srst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: core_srst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: core_srst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: core_srst_n

14.5.2.1.2.2 SPINLOCK_SYSCONFIG Register

1 SPINLOCK_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

Return to Summary Table

Table 14-19716. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0010h**

Figure 14-6541. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SOFT_RESET	RESERVED
NONE						R/W	NONE
0h						0h	0h

Table 14-19718. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks Reset Source: core_srst_n
0	RESERVED	NONE	0h	Reserved

14.5.2.1.2.3 SPINLOCK_SYSTATUS Register

1 SPINLOCK_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Provides information about the Spinlock module

Return to Summary Table

Table 14-19719. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0014h**

Figure 14-6542. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24
NUM_LOCKS							
R							
8h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19721. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NUM_LOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08 Reset Source: core_srst_n
23:8	RESERVED	NONE	0h	Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state Reset Source: core_srst_n
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state Reset Source: core_srst_n

Table 14-19721. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state Reset Source: core_srst_n
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state Reset Source: core_srst_n
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state Reset Source: core_srst_n
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state Reset Source: core_srst_n
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state Reset Source: core_srst_n
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state Reset Source: core_srst_n

14.5.2.1.2.4 SPINLOCK_LOCK_REG_j Register

1 SPINLOCK_LOCK_REG_j Register (Offset = 800h + formula) [reset = 0h]

The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'

Return to Summary Table

Offset = 800h + (j * 4h); where j = 0 to 255d

Table 14-19722. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0800h + formula**

Figure 14-6543. SPINLOCK_LOCK_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TAKEN
NONE							R/W
0h							0h

Table 14-19724. SPINLOCK_LOCK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect Reset Source: core_srst_n

14.6 Memory Controller Registers

14.6.1 ROM

ROM

14.6.1.1 ROM Summaries

ROM Summaries

Table 14-19725. ROM Registers, Base Address=4180 0000h, Length=262144

Offset	Length	Register Name	WKUP_ROM0 Physical Address
0h	32	ROM_ROM_REG_J	4180 0000h + formula

14.6.1.2 ROM Registers

ROM Registers

14.6.1.2.1 ROM_ROM_REG_j Register

1 ROM_ROM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The ROM memory words provide memory mapped random access data storage.

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 49151d

Table 14-19726. Instance Table

Instance Name	Physical Address
WKUP_ROM0	**4180 0000h + formula**

Figure 14-6544. ROM_ROM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R							
0h							

Table 14-19728. ROM_ROM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.6.2 PSRAMECC

PSRAMECC

14.6.2.1 PSRAMECC Summaries

PSRAMECC Summaries

Table 14-19729. PSRAMECC_RAM Registers, Base Address=0000 0000h, Length=1024

Offset	Length	Register Name	PSRAMECC0 Physical Address	PSRAMECC1 Physical Address
0h	32	PSRAMECC_RAM_RAM_REG_J	0000 0000h + formula	0090 0000h + formula

Table 14-19730. ECC_AGGR Registers, Base Address=0070 0000h, Length=1024

Offset	Length	Register Name	PSRAMECC0 Physical Address	PSRAMECC1 Physical Address
0h	32	ECC_AGGR_REV	0070 0000h	0070 1000h
8h	32	ECC_AGGR_VECTOR	0070 0008h	0070 1008h
Ch	32	ECC_AGGR_STAT	0070 000Ch	0070 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 0010h + formula	0070 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 003Ch	0070 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 0040h	0070 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 0080h	0070 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 00C0h	0070 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 013Ch	0070 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 0140h	0070 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 0180h	0070 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 01C0h	0070 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 0200h	0070 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 0204h	0070 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 0208h	0070 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 020Ch	0070 120Ch

14.6.2.2 PSRAMECC Registers

PSRAMECC Registers

14.6.2.2.1 PSRAMECC_RAM_RAM_REG_j Register

1 PSRAMECC_RAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 255d

Table 14-19731. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0000 0000h + formula**
PSRAMECC1	**0090 0000h + formula**

Figure 14-6545. PSRAMECC_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-19733. PSRAMECC_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.6.2.2.2 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

Return to Summary Table

Table 14-19734. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0000h**
PSRAMECC1	**0070 1000h**

Figure 14-6546. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19736. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.2.2.3 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-19737. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0008h**
PSRAMECC1	**0070 1008h**

Figure 14-6547. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-19739. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.2.2.4 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-19740. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 000Ch**
PSRAMECC1	**0070 100Ch**

Figure 14-6548. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-19742. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.2.2.5 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-19743. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0010h + formula**
PSRAMECC1	**0070 1010h + formula**

Figure 14-6549. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19745. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.2.2.6 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-19746. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 003Ch**
PSRAMECC1	**0070 103Ch**

Figure 14-6550. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19748. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.2.2.7 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19749. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0040h**
PSRAMECC1	**0070 1040h**

Figure 14-6551. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-19751. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.6.2.2.8 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19752. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0080h**
PSRAMECC1	**0070 1080h**

Figure 14-6552. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-19754. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.6.2.2.9 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-19755. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 00C0h**
PSRAMECC1	**0070 10C0h**

Figure 14-6553. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19757. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.6.2.2.10 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19758. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 013Ch**
PSRAMECC1	**0070 113Ch**

Figure 14-6554. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19760. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.2.2.11 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19761. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0140h**
PSRAMECC1	**0070 1140h**

Figure 14-6555. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-19763. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.6.2.2.12 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19764. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0180h**
PSRAMECC1	**0070 1180h**

Figure 14-6556. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SRAM_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-19766. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.6.2.2.13 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19767. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 01C0h**
PSRAMECC1	**0070 11C0h**

Figure 14-6557. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19769. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.6.2.2.14 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19770. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0200h**
PSRAMECC1	**0070 1200h**

Figure 14-6558. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19772. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.2.2.15 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19773. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0204h**
PSRAMECC1	**0070 1204h**

Figure 14-6559. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19775. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.2.2.16 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19776. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 0208h**
PSRAMECC1	**0070 1208h**

Figure 14-6560. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19778. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.2.2.17 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19779. Instance Table

Instance Name	Physical Address
PSRAMECC0	**0070 020Ch**
PSRAMECC1	**0070 120Ch**

Figure 14-6561. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-19781. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.3 PSRAMECC_8k

PSRAMECC_8k

14.6.3.1 PSRAMECC_8k Summaries

PSRAMECC_8k Summaries

Table 14-19782. ECC_AGGR Registers, Base Address=2B60 8000h, Length=1024

Offset	Length	Register Name	WKUP_PSRAMECC_8K0 Physical Address
0h	32	ECC_AGGR_REV	2B60 8000h
8h	32	ECC_AGGR_VECTOR	2B60 8008h
Ch	32	ECC_AGGR_STAT	2B60 800Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	2B60 8010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	2B60 803Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2B60 8040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2B60 8080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2B60 80C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2B60 813Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2B60 8140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2B60 8180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2B60 81C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2B60 8200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2B60 8204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2B60 8208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2B60 820Ch

Table 14-19783. PSRAMECC_8K_RAM Registers, Base Address=4188 0000h, Length=32768

Offset	Length	Register Name	WKUP_PSRAMECC_8K0 Physical Address
0h	32	PSRAMECC_8K_RAM_RAM_REG_J	4188 0000h + formula

14.6.3.2 PSRAMECC_8k Registers

PSRAMECC_8k Registers

14.6.3.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-19784. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8000h**

Figure 14-6562. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19786. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.3.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19787. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8008h**

Figure 14-6563. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-19789. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.3.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-19790. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 800Ch**

Figure 14-6564. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-19792. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.3.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-19793. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8010h + formula**

Figure 14-6565. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19795. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.3.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-19796. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 803Ch**

Figure 14-6566. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19798. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19799. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8040h**

Figure 14-6567. ECC_AGGR_SEC_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SRAM_PEND</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-19801. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.6.3.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19802. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8080h**

Figure 14-6568. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-19804. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.6.3.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-19805. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 80C0h**

Figure 14-6569. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19807. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.6.3.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19808. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 813Ch**

Figure 14-6570. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19810. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.3.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19811. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8140h**

Figure 14-6571. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-19813. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.6.3.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19814. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8180h**

Figure 14-6572. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-19816. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.6.3.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19817. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 81C0h**

Figure 14-6573. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19819. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.6.3.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19820. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8200h**

Figure 14-6574. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19822. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.3.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19823. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8204h**

Figure 14-6575. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-19825. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.3.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19826. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 8208h**

Figure 14-6576. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19828. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.3.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19829. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**2B60 820Ch**

Figure 14-6577. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-19831. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.3.2.17 PSRAMECC_8K_RAM_RAM_REG_j Register

1 PSRAMECC_8K_RAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Offset = 0h + (j * 4h); where j = 0 to 8191d

Table 14-19832. Instance Table

Instance Name	Physical Address
WKUP_PSRAMECC_8K0	**4188 0000h + formula**

Figure 14-6578. PSRAMECC_8K_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-19834. PSRAMECC_8K_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.6.4 MSRAM_64k

MSRAM_64k

14.6.4.1 MSRAM_64k Summaries

MSRAM_64k Summaries

Table 14-19835. ECC_AGGR Registers, Base Address=0071 0000h, Length=1024

Offset	Length	Register Name	MSRAM_64K0 Physical Address
0h	32	ECC_AGGR_REV	0071 0000h
8h	32	ECC_AGGR_VECTOR	0071 0008h
Ch	32	ECC_AGGR_STAT	0071 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 020Ch

Table 14-19836. MSRAM_64K_RAM Registers, Base Address=43C4 0000h, Length=65536

Offset	Length	Register Name	MSRAM_64K0 Physical Address
0h	32	MSRAM_64K_RAM_RAM_REG	43C4 0000h

Table 14-19837. MSRAM_64K_RAM Registers, Base Address=7000 0000h, Length=65536

Offset	Length	Register Name	MSRAM_64K0 Physical Address
0h	32	MSRAM_64K_RAM_RAM_REG	7000 0000h

14.6.4.2 MSRAM_64k Registers

MSRAM_64k Registers

14.6.4.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-19838. Instance Table

Instance Name	**Physical Address**
MSRAM_64K0	**0071 0000h**

Figure 14-6579. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19840. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.4.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19841. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0008h**

Figure 14-6580. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-19843. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.4.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-19844. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 000Ch**

Figure 14-6581. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 14-19846. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.4.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-19847. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0010h + formula**

Figure 14-6582. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19849. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.4.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-19850. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 003Ch**

Figure 14-6583. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19852. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.4.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-19853. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0040h**

Figure 14-6584. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC0_PEND
NONE							R/W1TS
0h							0h

Table 14-19855. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.6.4.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19856. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0080h**

Figure 14-6585. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC0_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-19858. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.6.4.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19859. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 00C0h**

Figure 14-6586. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC0_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19861. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.6.4.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19862. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 013Ch**

Figure 14-6587. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19864. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.4.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19865. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0140h**

Figure 14-6588. ECC_AGGR_DED_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RAMECC0_PEND</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-19867. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.6.4.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19868. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0180h**

Figure 14-6589. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC0_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-19870. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.6.4.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19871. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 01C0h**

Figure 14-6590. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC0_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-19873. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.6.4.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19874. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0200h**

Figure 14-6591. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19876. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.4.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19877. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0204h**

Figure 14-6592. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-19879. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.4.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19880. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 0208h**

Figure 14-6593. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-19882. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.4.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19883. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**0071 020Ch**

Figure 14-6594. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-19885. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.4.2.17 MSRAM_64K_RAM_RAM_REG Register

1 MSRAM_64K_RAM_RAM_REG Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Table 14-19886. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**7000 0000h**

Figure 14-6595. MSRAM_64K_RAM_RAM_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BYTE3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BYTE2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BYTE1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19888. MSRAM_64K_RAM_RAM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_n

14.6.4.2.18 MSRAM_64K_RAM_RAM_REG Register

1 MSRAM_64K_RAM_RAM_REG Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Table 14-19889. Instance Table

Instance Name	Physical Address
MSRAM_64K0	**7000 0000h**

Figure 14-6596. MSRAM_64K_RAM_RAM_REG Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-19891. MSRAM_64K_RAM_RAM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_n

14.6.5 MSRAM_256k

MSRAM_256k

14.6.5.1 MSRAM_256k Summaries

MSRAM_256k Summaries

Table 14-19892. ECC_AGGR Registers, Base Address=0470 5000h, Length=1024

Offset	Length	Register Name	MCU_MSRAM_256K0 Physical Address	MCU_MSRAM_256K1 Physical Address
0h	32	ECC_AGGR_REV	0470 5000h	0470 6000h
8h	32	ECC_AGGR_VECTOR	0470 5008h	0470 6008h
Ch	32	ECC_AGGR_STAT	0470 500Ch	0470 600Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0470 5010h + formula	0470 6010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0470 503Ch	0470 603Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0470 5040h	0470 6040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0470 5080h	0470 6080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0470 50C0h	0470 60C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0470 513Ch	0470 613Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0470 5140h	0470 6140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0470 5180h	0470 6180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0470 51C0h	0470 61C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0470 5200h	0470 6200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0470 5204h	0470 6204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0470 5208h	0470 6208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0470 520Ch	0470 620Ch

Table 14-19893. MSRAM_256K_RAM Registers, Base Address=7910 0000h, Length=262144

Offset	Length	Register Name	MCU_MSRAM_256K0 Physical Address	MCU_MSRAM_256K1 Physical Address
0h	32	MSRAM_256K_RAM_RAM_REG	7910 0000h	7914 0000h

14.6.5.2 MSRAM_256k Registers

MSRAM_256k Registers

14.6.5.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-19894. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5000h**
MCU_MSRAM_256K1	**0470 6000h**

Figure 14-6597. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19896. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.5.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19897. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5008h**
MCU_MSRAM_256K1	**0470 6008h**

Figure 14-6598. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-19899. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.5.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 3h]

Misc Status

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Table 14-19900. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 500Ch**
MCU_MSRAM_256K1	**0470 600Ch**

Figure 14-6599. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					3h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
3h							

Table 14-19902. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	3h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.5.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-19903. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5010h + formula**
MCU_MSRAM_256K1	**0470 6010h + formula**

Figure 14-6600. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19905. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.5.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-19906. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 503Ch**
MCU_MSRAM_256K1	**0470 603Ch**

Figure 14-6601. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19908. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.5.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19909. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5040h**
MCU_MSRAM_256K1	**0470 6040h**

Figure 14-6602. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_PEND	BUSECC_PEND	RAMECC0_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19911. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
1	BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for busecc_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.6.5.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19912. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5080h**
MCU_MSRAM_256K1	**0470 6080h**

Figure 14-6603. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_SET	BUSECC_ENABLE_SET	RAMECC0_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19914. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
1	BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for busecc_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.6.5.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19915. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 50C0h**
MCU_MSRAM_256K1	**0470 60C0h**

Figure 14-6604. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_CLR	BUSECC_ENABLE_CLR	RAMECC0_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-19917. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
1	BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for busecc_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.6.5.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19918. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 513Ch**
MCU_MSRAM_256K1	**0470 613Ch**

Figure 14-6605. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19920. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.5.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19921. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5140h**
MCU_MSRAM_256K1	**0470 6140h**

Figure 14-6606. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					ECCAGG_PEND	BUSECC_PEND	RAMECC0_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19923. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
1	BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for busecc_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.6.5.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19924. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5180h**
MCU_MSRAM_256K1	**0470 6180h**

Figure 14-6607. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_SET	BUSECC_ENABLE_SET	RAMECC0_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-19926. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
1	BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for busecc_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.6.5.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19927. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 51C0h**
MCU_MSRAM_256K1	**0470 61C0h**

Figure 14-6608. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECCAGG_ENABLE_CLR	BUSECC_ENABLE_CLR	RAMECC0_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-19929. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
1	BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for busecc_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.6.5.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19930. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5200h**
MCU_MSRAM_256K1	**0470 6200h**

Figure 14-6609. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19932. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.5.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19933. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**0470 5204h**
MCU_MSRAM_256K1	**0470 6204h**

Figure 14-6610. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19935. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.5.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19936. Instance Table

Instance Name	**Physical Address**
MCU_MSRAM_256K0	**0470 5208h**
MCU_MSRAM_256K1	**0470 6208h**

Figure 14-6611. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19938. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.5.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19939. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	0470 520Ch
MCU_MSRAM_256K1	0470 620Ch

Figure 14-6612. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-19941. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.5.2.17 MSRAM_256K_RAM_RAM_REG Register

1 MSRAM_256K_RAM_RAM_REG Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Table 14-19942. Instance Table

Instance Name	Physical Address
MCU_MSRAM_256K0	**7910 0000h**
MCU_MSRAM_256K1	**7914 0000h**

Figure 14-6613. MSRAM_256K_RAM_RAM_REG Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-19944. MSRAM_256K_RAM_RAM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_n

14.6.6 ddr32ss

ddr32ss

14.6.6.1 ddr32ss Summaries

ddr32ss Summaries

Table 14-19945. EMIF_SSCFG Registers, Base Address=0F30 0000h, Length=512

Offset	Length	Register Name	DDR32SS0 Physical Address
0h	32	EMIF_SSCFG_SS_ID_REV_REG	0F30 0000h
4h	32	EMIF_SSCFG_SS_CTL_REG	0F30 0004h
20h	32	EMIF_SSCFG_V2A_CTL_REG	0F30 0020h
24h	32	EMIF_SSCFG_V2A_R1_MAT_REG	0F30 0024h
28h	32	EMIF_SSCFG_V2A_R2_MAT_REG	0F30 0028h
2Ch	32	EMIF_SSCFG_V2A_R3_MAT_REG	0F30 002Ch
30h	32	EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG	0F30 0030h
34h	32	EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG	0F30 0034h
38h	32	EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG	0F30 0038h
3Ch	32	EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG	0F30 003Ch
4Ch	32	EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG	0F30 004Ch
50h	32	EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG	0F30 0050h
54h	32	EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG	0F30 0054h
58h	32	EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG	0F30 0058h
5Ch	32	EMIF_SSCFG_V2A_OLD_CMD_PR_REG	0F30 005Ch
68h	32	EMIF_SSCFG_V2A_LEAKY_THRESH_REG	0F30 0068h
6Ch	32	EMIF_SSCFG_V2A_DRAIN_THRESH_REG	0F30 006Ch
70h	32	EMIF_SSCFG_V2A_AERR_LOG1_REG	0F30 0070h
74h	32	EMIF_SSCFG_V2A_AERR_LOG2_REG	0F30 0074h
9Ch	32	EMIF_SSCFG_V2A_BUS_TO	0F30 009Ch
A0h	32	EMIF_SSCFG_V2A_INT_RAW_REG	0F30 00A0h
A4h	32	EMIF_SSCFG_V2A_INT_STAT_REG	0F30 00A4h
A8h	32	EMIF_SSCFG_V2A_INT_SET_REG	0F30 00A8h
ACh	32	EMIF_SSCFG_V2A_INT_CLR_REG	0F30 00ACh
B0h	32	EMIF_SSCFG_V2A_EOI_REG	0F30 00B0h
100h	32	EMIF_SSCFG_PERF_CNT_SEL_REG	0F30 0100h
104h	32	EMIF_SSCFG_PERF_CNT1_REG	0F30 0104h
108h	32	EMIF_SSCFG_PERF_CNT2_REG	0F30 0108h
10Ch	32	EMIF_SSCFG_PERF_CNT3_REG	0F30 010Ch
110h	32	EMIF_SSCFG_PERF_CNT4_REG	0F30 0110h
120h	32	EMIF_SSCFG_ECC_CTRL_REG	0F30 0120h
124h	32	EMIF_SSCFG_ECC_RID_INDX_REG	0F30 0124h
128h	32	EMIF_SSCFG_ECC_RID_VAL_REG	0F30 0128h
130h	32	EMIF_SSCFG_ECC_R0_STR_ADDR_REG	0F30 0130h
134h	32	EMIF_SSCFG_ECC_R0_END_ADDR_REG	0F30 0134h
138h	32	EMIF_SSCFG_ECC_R1_STR_ADDR_REG	0F30 0138h
13Ch	32	EMIF_SSCFG_ECC_R1_END_ADDR_REG	0F30 013Ch
140h	32	EMIF_SSCFG_ECC_R2_STR_ADDR_REG	0F30 0140h

Table 14-19945. EMIF_SSCFG Registers, Base Address=0F30 0000h, Length=512 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
144h	32	EMIF_SSCFG_ECC_R2_END_ADDR_REG	0F30 0144h
150h	32	EMIF_SSCFG_ECC_1B_ERR_CNT_REG	0F30 0150h
154h	32	EMIF_SSCFG_ECC_1B_ERR_THRSH_REG	0F30 0154h
158h	32	EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG	0F30 0158h
15Ch	32	EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG	0F30 015Ch
160h	32	EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG	0F30 0160h
164h	32	EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG	0F30 0164h
184h	32	EMIF_SSCFG_PHY_TEST_CTRL1_REG	0F30 0184h
188h	32	EMIF_SSCFG_PHY_TEST_CTRL2_REG	0F30 0188h
18Ch	32	EMIF_SSCFG_PHY_TEST_CTRL3_REG	0F30 018Ch
190h	32	EMIF_SSCFG_PHY_TEST_CTRL4_REG	0F30 0190h
194h	32	EMIF_SSCFG_PHY_TEST_CTRL5_REG	0F30 0194h
198h	32	EMIF_SSCFG_PHY_TEST_CTRL6_REG	0F30 0198h
19Ch	32	EMIF_SSCFG_PHY_TEST_CTRL7_REG	0F30 019Ch
1A0h	32	EMIF_SSCFG_PHY_TEST_CTRL8_REG	0F30 01A0h
1A4h	32	EMIF_SSCFG_PHY_TEST_CTRL9_REG	0F30 01A4h
1A8h	32	EMIF_SSCFG_PHY_TEST_CTRL10_REG	0F30 01A8h
1ACh	32	EMIF_SSCFG_PHY_TEST_CTRL11_REG	0F30 01ACh
1B0h	32	EMIF_SSCFG_PHY_TEST_CTRL12_REG	0F30 01B0h
1C0h	32	EMIF_SSCFG_PHY_TEST_STAT1_REG	0F30 01C0h
1C4h	32	EMIF_SSCFG_PHY_TEST_STAT2_REG	0F30 01C4h
1C8h	32	EMIF_SSCFG_PHY_TEST_STAT3_REG	0F30 01C8h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768

Offset	Length	Register Name	DDR32SS0 Physical Address
0h	32	EMIF_CTLCFG_DENALI_CTL_0	0F30 8000h
4h	32	EMIF_CTLCFG_DENALI_CTL_1	0F30 8004h
8h	32	EMIF_CTLCFG_DENALI_CTL_2	0F30 8008h
Ch	32	EMIF_CTLCFG_DENALI_CTL_3	0F30 800Ch
10h	32	EMIF_CTLCFG_DENALI_CTL_4	0F30 8010h
14h	32	EMIF_CTLCFG_DENALI_CTL_5	0F30 8014h
18h	32	EMIF_CTLCFG_DENALI_CTL_6	0F30 8018h
1Ch	32	EMIF_CTLCFG_DENALI_CTL_7	0F30 801Ch
20h	32	EMIF_CTLCFG_DENALI_CTL_8	0F30 8020h
24h	32	EMIF_CTLCFG_DENALI_CTL_9	0F30 8024h
28h	32	EMIF_CTLCFG_DENALI_CTL_10	0F30 8028h
2Ch	32	EMIF_CTLCFG_DENALI_CTL_11	0F30 802Ch
30h	32	EMIF_CTLCFG_DENALI_CTL_12	0F30 8030h
34h	32	EMIF_CTLCFG_DENALI_CTL_13	0F30 8034h
38h	32	EMIF_CTLCFG_DENALI_CTL_14	0F30 8038h
3Ch	32	EMIF_CTLCFG_DENALI_CTL_15	0F30 803Ch
40h	32	EMIF_CTLCFG_DENALI_CTL_16	0F30 8040h
44h	32	EMIF_CTLCFG_DENALI_CTL_17	0F30 8044h
48h	32	EMIF_CTLCFG_DENALI_CTL_18	0F30 8048h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4Ch	32	EMIF_CTLCFG_DENALI_CTL_19	0F30 804Ch
50h	32	EMIF_CTLCFG_DENALI_CTL_20	0F30 8050h
54h	32	EMIF_CTLCFG_DENALI_CTL_21	0F30 8054h
58h	32	EMIF_CTLCFG_DENALI_CTL_22	0F30 8058h
5Ch	32	EMIF_CTLCFG_DENALI_CTL_23	0F30 805Ch
60h	32	EMIF_CTLCFG_DENALI_CTL_24	0F30 8060h
64h	32	EMIF_CTLCFG_DENALI_CTL_25	0F30 8064h
68h	32	EMIF_CTLCFG_DENALI_CTL_26	0F30 8068h
6Ch	32	EMIF_CTLCFG_DENALI_CTL_27	0F30 806Ch
70h	32	EMIF_CTLCFG_DENALI_CTL_28	0F30 8070h
74h	32	EMIF_CTLCFG_DENALI_CTL_29	0F30 8074h
78h	32	EMIF_CTLCFG_DENALI_CTL_30	0F30 8078h
7Ch	32	EMIF_CTLCFG_DENALI_CTL_31	0F30 807Ch
80h	32	EMIF_CTLCFG_DENALI_CTL_32	0F30 8080h
84h	32	EMIF_CTLCFG_DENALI_CTL_33	0F30 8084h
88h	32	EMIF_CTLCFG_DENALI_CTL_34	0F30 8088h
8Ch	32	EMIF_CTLCFG_DENALI_CTL_35	0F30 808Ch
90h	32	EMIF_CTLCFG_DENALI_CTL_36	0F30 8090h
94h	32	EMIF_CTLCFG_DENALI_CTL_37	0F30 8094h
98h	32	EMIF_CTLCFG_DENALI_CTL_38	0F30 8098h
9Ch	32	EMIF_CTLCFG_DENALI_CTL_39	0F30 809Ch
A0h	32	EMIF_CTLCFG_DENALI_CTL_40	0F30 80A0h
A4h	32	EMIF_CTLCFG_DENALI_CTL_41	0F30 80A4h
A8h	32	EMIF_CTLCFG_DENALI_CTL_42	0F30 80A8h
ACh	32	EMIF_CTLCFG_DENALI_CTL_43	0F30 80ACh
B0h	32	EMIF_CTLCFG_DENALI_CTL_44	0F30 80B0h
B4h	32	EMIF_CTLCFG_DENALI_CTL_45	0F30 80B4h
B8h	32	EMIF_CTLCFG_DENALI_CTL_46	0F30 80B8h
BCh	32	EMIF_CTLCFG_DENALI_CTL_47	0F30 80BCh
C0h	32	EMIF_CTLCFG_DENALI_CTL_48	0F30 80C0h
C4h	32	EMIF_CTLCFG_DENALI_CTL_49	0F30 80C4h
C8h	32	EMIF_CTLCFG_DENALI_CTL_50	0F30 80C8h
CCh	32	EMIF_CTLCFG_DENALI_CTL_51	0F30 80CCh
D0h	32	EMIF_CTLCFG_DENALI_CTL_52	0F30 80D0h
D4h	32	EMIF_CTLCFG_DENALI_CTL_53	0F30 80D4h
D8h	32	EMIF_CTLCFG_DENALI_CTL_54	0F30 80D8h
DCh	32	EMIF_CTLCFG_DENALI_CTL_55	0F30 80DCh
E0h	32	EMIF_CTLCFG_DENALI_CTL_56	0F30 80E0h
E4h	32	EMIF_CTLCFG_DENALI_CTL_57	0F30 80E4h
E8h	32	EMIF_CTLCFG_DENALI_CTL_58	0F30 80E8h
ECh	32	EMIF_CTLCFG_DENALI_CTL_59	0F30 80ECh
F0h	32	EMIF_CTLCFG_DENALI_CTL_60	0F30 80F0h
F4h	32	EMIF_CTLCFG_DENALI_CTL_61	0F30 80F4h
F8h	32	EMIF_CTLCFG_DENALI_CTL_62	0F30 80F8h
FCh	32	EMIF_CTLCFG_DENALI_CTL_63	0F30 80FCh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
100h	32	EMIF_CTLCFG_DENALI_CTL_64	0F30 8100h
104h	32	EMIF_CTLCFG_DENALI_CTL_65	0F30 8104h
108h	32	EMIF_CTLCFG_DENALI_CTL_66	0F30 8108h
10Ch	32	EMIF_CTLCFG_DENALI_CTL_67	0F30 810Ch
110h	32	EMIF_CTLCFG_DENALI_CTL_68	0F30 8110h
114h	32	EMIF_CTLCFG_DENALI_CTL_69	0F30 8114h
118h	32	EMIF_CTLCFG_DENALI_CTL_70	0F30 8118h
11Ch	32	EMIF_CTLCFG_DENALI_CTL_71	0F30 811Ch
120h	32	EMIF_CTLCFG_DENALI_CTL_72	0F30 8120h
124h	32	EMIF_CTLCFG_DENALI_CTL_73	0F30 8124h
128h	32	EMIF_CTLCFG_DENALI_CTL_74	0F30 8128h
12Ch	32	EMIF_CTLCFG_DENALI_CTL_75	0F30 812Ch
130h	32	EMIF_CTLCFG_DENALI_CTL_76	0F30 8130h
134h	32	EMIF_CTLCFG_DENALI_CTL_77	0F30 8134h
138h	32	EMIF_CTLCFG_DENALI_CTL_78	0F30 8138h
13Ch	32	EMIF_CTLCFG_DENALI_CTL_79	0F30 813Ch
140h	32	EMIF_CTLCFG_DENALI_CTL_80	0F30 8140h
144h	32	EMIF_CTLCFG_DENALI_CTL_81	0F30 8144h
148h	32	EMIF_CTLCFG_DENALI_CTL_82	0F30 8148h
14Ch	32	EMIF_CTLCFG_DENALI_CTL_83	0F30 814Ch
150h	32	EMIF_CTLCFG_DENALI_CTL_84	0F30 8150h
154h	32	EMIF_CTLCFG_DENALI_CTL_85	0F30 8154h
158h	32	EMIF_CTLCFG_DENALI_CTL_86	0F30 8158h
15Ch	32	EMIF_CTLCFG_DENALI_CTL_87	0F30 815Ch
160h	32	EMIF_CTLCFG_DENALI_CTL_88	0F30 8160h
164h	32	EMIF_CTLCFG_DENALI_CTL_89	0F30 8164h
168h	32	EMIF_CTLCFG_DENALI_CTL_90	0F30 8168h
16Ch	32	EMIF_CTLCFG_DENALI_CTL_91	0F30 816Ch
170h	32	EMIF_CTLCFG_DENALI_CTL_92	0F30 8170h
174h	32	EMIF_CTLCFG_DENALI_CTL_93	0F30 8174h
178h	32	EMIF_CTLCFG_DENALI_CTL_94	0F30 8178h
17Ch	32	EMIF_CTLCFG_DENALI_CTL_95	0F30 817Ch
180h	32	EMIF_CTLCFG_DENALI_CTL_96	0F30 8180h
184h	32	EMIF_CTLCFG_DENALI_CTL_97	0F30 8184h
188h	32	EMIF_CTLCFG_DENALI_CTL_98	0F30 8188h
18Ch	32	EMIF_CTLCFG_DENALI_CTL_99	0F30 818Ch
190h	32	EMIF_CTLCFG_DENALI_CTL_100	0F30 8190h
194h	32	EMIF_CTLCFG_DENALI_CTL_101	0F30 8194h
198h	32	EMIF_CTLCFG_DENALI_CTL_102	0F30 8198h
19Ch	32	EMIF_CTLCFG_DENALI_CTL_103	0F30 819Ch
1A0h	32	EMIF_CTLCFG_DENALI_CTL_104	0F30 81A0h
1A4h	32	EMIF_CTLCFG_DENALI_CTL_105	0F30 81A4h
1A8h	32	EMIF_CTLCFG_DENALI_CTL_106	0F30 81A8h
1ACh	32	EMIF_CTLCFG_DENALI_CTL_107	0F30 81ACh
1B0h	32	EMIF_CTLCFG_DENALI_CTL_108	0F30 81B0h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
1B4h	32	EMIF_CTLCFG_DENALI_CTL_109	0F30 81B4h
1B8h	32	EMIF_CTLCFG_DENALI_CTL_110	0F30 81B8h
1BCh	32	EMIF_CTLCFG_DENALI_CTL_111	0F30 81BCh
1C0h	32	EMIF_CTLCFG_DENALI_CTL_112	0F30 81C0h
1C4h	32	EMIF_CTLCFG_DENALI_CTL_113	0F30 81C4h
1C8h	32	EMIF_CTLCFG_DENALI_CTL_114	0F30 81C8h
1CCh	32	EMIF_CTLCFG_DENALI_CTL_115	0F30 81CCh
1D0h	32	EMIF_CTLCFG_DENALI_CTL_116	0F30 81D0h
1D4h	32	EMIF_CTLCFG_DENALI_CTL_117	0F30 81D4h
1D8h	32	EMIF_CTLCFG_DENALI_CTL_118	0F30 81D8h
1DCh	32	EMIF_CTLCFG_DENALI_CTL_119	0F30 81DCh
1E0h	32	EMIF_CTLCFG_DENALI_CTL_120	0F30 81E0h
1E4h	32	EMIF_CTLCFG_DENALI_CTL_121	0F30 81E4h
1E8h	32	EMIF_CTLCFG_DENALI_CTL_122	0F30 81E8h
1ECh	32	EMIF_CTLCFG_DENALI_CTL_123	0F30 81ECh
1F0h	32	EMIF_CTLCFG_DENALI_CTL_124	0F30 81F0h
1F4h	32	EMIF_CTLCFG_DENALI_CTL_125	0F30 81F4h
1F8h	32	EMIF_CTLCFG_DENALI_CTL_126	0F30 81F8h
1FCh	32	EMIF_CTLCFG_DENALI_CTL_127	0F30 81FCh
200h	32	EMIF_CTLCFG_DENALI_CTL_128	0F30 8200h
204h	32	EMIF_CTLCFG_DENALI_CTL_129	0F30 8204h
208h	32	EMIF_CTLCFG_DENALI_CTL_130	0F30 8208h
20Ch	32	EMIF_CTLCFG_DENALI_CTL_131	0F30 820Ch
210h	32	EMIF_CTLCFG_DENALI_CTL_132	0F30 8210h
214h	32	EMIF_CTLCFG_DENALI_CTL_133	0F30 8214h
218h	32	EMIF_CTLCFG_DENALI_CTL_134	0F30 8218h
21Ch	32	EMIF_CTLCFG_DENALI_CTL_135	0F30 821Ch
220h	32	EMIF_CTLCFG_DENALI_CTL_136	0F30 8220h
224h	32	EMIF_CTLCFG_DENALI_CTL_137	0F30 8224h
228h	32	EMIF_CTLCFG_DENALI_CTL_138	0F30 8228h
22Ch	32	EMIF_CTLCFG_DENALI_CTL_139	0F30 822Ch
230h	32	EMIF_CTLCFG_DENALI_CTL_140	0F30 8230h
234h	32	EMIF_CTLCFG_DENALI_CTL_141	0F30 8234h
238h	32	EMIF_CTLCFG_DENALI_CTL_142	0F30 8238h
23Ch	32	EMIF_CTLCFG_DENALI_CTL_143	0F30 823Ch
240h	32	EMIF_CTLCFG_DENALI_CTL_144	0F30 8240h
244h	32	EMIF_CTLCFG_DENALI_CTL_145	0F30 8244h
248h	32	EMIF_CTLCFG_DENALI_CTL_146	0F30 8248h
24Ch	32	EMIF_CTLCFG_DENALI_CTL_147	0F30 824Ch
250h	32	EMIF_CTLCFG_DENALI_CTL_148	0F30 8250h
254h	32	EMIF_CTLCFG_DENALI_CTL_149	0F30 8254h
258h	32	EMIF_CTLCFG_DENALI_CTL_150	0F30 8258h
25Ch	32	EMIF_CTLCFG_DENALI_CTL_151	0F30 825Ch
260h	32	EMIF_CTLCFG_DENALI_CTL_152	0F30 8260h
264h	32	EMIF_CTLCFG_DENALI_CTL_153	0F30 8264h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
268h	32	EMIF_CTLCFG_DENALI_CTL_154	0F30 8268h
26Ch	32	EMIF_CTLCFG_DENALI_CTL_155	0F30 826Ch
270h	32	EMIF_CTLCFG_DENALI_CTL_156	0F30 8270h
274h	32	EMIF_CTLCFG_DENALI_CTL_157	0F30 8274h
278h	32	EMIF_CTLCFG_DENALI_CTL_158	0F30 8278h
27Ch	32	EMIF_CTLCFG_DENALI_CTL_159	0F30 827Ch
280h	32	EMIF_CTLCFG_DENALI_CTL_160	0F30 8280h
284h	32	EMIF_CTLCFG_DENALI_CTL_161	0F30 8284h
288h	32	EMIF_CTLCFG_DENALI_CTL_162	0F30 8288h
28Ch	32	EMIF_CTLCFG_DENALI_CTL_163	0F30 828Ch
290h	32	EMIF_CTLCFG_DENALI_CTL_164	0F30 8290h
294h	32	EMIF_CTLCFG_DENALI_CTL_165	0F30 8294h
298h	32	EMIF_CTLCFG_DENALI_CTL_166	0F30 8298h
29Ch	32	EMIF_CTLCFG_DENALI_CTL_167	0F30 829Ch
2A0h	32	EMIF_CTLCFG_DENALI_CTL_168	0F30 82A0h
2A4h	32	EMIF_CTLCFG_DENALI_CTL_169	0F30 82A4h
2A8h	32	EMIF_CTLCFG_DENALI_CTL_170	0F30 82A8h
2ACh	32	EMIF_CTLCFG_DENALI_CTL_171	0F30 82ACh
2B0h	32	EMIF_CTLCFG_DENALI_CTL_172	0F30 82B0h
2B4h	32	EMIF_CTLCFG_DENALI_CTL_173	0F30 82B4h
2B8h	32	EMIF_CTLCFG_DENALI_CTL_174	0F30 82B8h
2BCh	32	EMIF_CTLCFG_DENALI_CTL_175	0F30 82BCh
2C0h	32	EMIF_CTLCFG_DENALI_CTL_176	0F30 82C0h
2C4h	32	EMIF_CTLCFG_DENALI_CTL_177	0F30 82C4h
2C8h	32	EMIF_CTLCFG_DENALI_CTL_178	0F30 82C8h
2CCh	32	EMIF_CTLCFG_DENALI_CTL_179	0F30 82CCh
2D0h	32	EMIF_CTLCFG_DENALI_CTL_180	0F30 82D0h
2D4h	32	EMIF_CTLCFG_DENALI_CTL_181	0F30 82D4h
2D8h	32	EMIF_CTLCFG_DENALI_CTL_182	0F30 82D8h
2DCh	32	EMIF_CTLCFG_DENALI_CTL_183	0F30 82DCh
2E0h	32	EMIF_CTLCFG_DENALI_CTL_184	0F30 82E0h
2E4h	32	EMIF_CTLCFG_DENALI_CTL_185	0F30 82E4h
2E8h	32	EMIF_CTLCFG_DENALI_CTL_186	0F30 82E8h
2ECh	32	EMIF_CTLCFG_DENALI_CTL_187	0F30 82ECh
2F0h	32	EMIF_CTLCFG_DENALI_CTL_188	0F30 82F0h
2F4h	32	EMIF_CTLCFG_DENALI_CTL_189	0F30 82F4h
2F8h	32	EMIF_CTLCFG_DENALI_CTL_190	0F30 82F8h
2FCh	32	EMIF_CTLCFG_DENALI_CTL_191	0F30 82FCh
300h	32	EMIF_CTLCFG_DENALI_CTL_192	0F30 8300h
304h	32	EMIF_CTLCFG_DENALI_CTL_193	0F30 8304h
308h	32	EMIF_CTLCFG_DENALI_CTL_194	0F30 8308h
30Ch	32	EMIF_CTLCFG_DENALI_CTL_195	0F30 830Ch
310h	32	EMIF_CTLCFG_DENALI_CTL_196	0F30 8310h
314h	32	EMIF_CTLCFG_DENALI_CTL_197	0F30 8314h
318h	32	EMIF_CTLCFG_DENALI_CTL_198	0F30 8318h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
31Ch	32	EMIF_CTLCFG_DENALI_CTL_199	0F30 831Ch
320h	32	EMIF_CTLCFG_DENALI_CTL_200	0F30 8320h
324h	32	EMIF_CTLCFG_DENALI_CTL_201	0F30 8324h
328h	32	EMIF_CTLCFG_DENALI_CTL_202	0F30 8328h
32Ch	32	EMIF_CTLCFG_DENALI_CTL_203	0F30 832Ch
330h	32	EMIF_CTLCFG_DENALI_CTL_204	0F30 8330h
334h	32	EMIF_CTLCFG_DENALI_CTL_205	0F30 8334h
338h	32	EMIF_CTLCFG_DENALI_CTL_206	0F30 8338h
33Ch	32	EMIF_CTLCFG_DENALI_CTL_207	0F30 833Ch
340h	32	EMIF_CTLCFG_DENALI_CTL_208	0F30 8340h
344h	32	EMIF_CTLCFG_DENALI_CTL_209	0F30 8344h
348h	32	EMIF_CTLCFG_DENALI_CTL_210	0F30 8348h
34Ch	32	EMIF_CTLCFG_DENALI_CTL_211	0F30 834Ch
350h	32	EMIF_CTLCFG_DENALI_CTL_212	0F30 8350h
354h	32	EMIF_CTLCFG_DENALI_CTL_213	0F30 8354h
358h	32	EMIF_CTLCFG_DENALI_CTL_214	0F30 8358h
35Ch	32	EMIF_CTLCFG_DENALI_CTL_215	0F30 835Ch
360h	32	EMIF_CTLCFG_DENALI_CTL_216	0F30 8360h
364h	32	EMIF_CTLCFG_DENALI_CTL_217	0F30 8364h
368h	32	EMIF_CTLCFG_DENALI_CTL_218	0F30 8368h
36Ch	32	EMIF_CTLCFG_DENALI_CTL_219	0F30 836Ch
370h	32	EMIF_CTLCFG_DENALI_CTL_220	0F30 8370h
374h	32	EMIF_CTLCFG_DENALI_CTL_221	0F30 8374h
378h	32	EMIF_CTLCFG_DENALI_CTL_222	0F30 8378h
37Ch	32	EMIF_CTLCFG_DENALI_CTL_223	0F30 837Ch
380h	32	EMIF_CTLCFG_DENALI_CTL_224	0F30 8380h
384h	32	EMIF_CTLCFG_DENALI_CTL_225	0F30 8384h
388h	32	EMIF_CTLCFG_DENALI_CTL_226	0F30 8388h
38Ch	32	EMIF_CTLCFG_DENALI_CTL_227	0F30 838Ch
390h	32	EMIF_CTLCFG_DENALI_CTL_228	0F30 8390h
394h	32	EMIF_CTLCFG_DENALI_CTL_229	0F30 8394h
398h	32	EMIF_CTLCFG_DENALI_CTL_230	0F30 8398h
39Ch	32	EMIF_CTLCFG_DENALI_CTL_231	0F30 839Ch
3A0h	32	EMIF_CTLCFG_DENALI_CTL_232	0F30 83A0h
3A4h	32	EMIF_CTLCFG_DENALI_CTL_233	0F30 83A4h
3A8h	32	EMIF_CTLCFG_DENALI_CTL_234	0F30 83A8h
3ACh	32	EMIF_CTLCFG_DENALI_CTL_235	0F30 83ACh
3B0h	32	EMIF_CTLCFG_DENALI_CTL_236	0F30 83B0h
3B4h	32	EMIF_CTLCFG_DENALI_CTL_237	0F30 83B4h
3B8h	32	EMIF_CTLCFG_DENALI_CTL_238	0F30 83B8h
3BCh	32	EMIF_CTLCFG_DENALI_CTL_239	0F30 83BCh
3C0h	32	EMIF_CTLCFG_DENALI_CTL_240	0F30 83C0h
3C4h	32	EMIF_CTLCFG_DENALI_CTL_241	0F30 83C4h
3C8h	32	EMIF_CTLCFG_DENALI_CTL_242	0F30 83C8h
3CCh	32	EMIF_CTLCFG_DENALI_CTL_243	0F30 83CCh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
3D0h	32	EMIF_CTLCFG_DENALI_CTL_244	0F30 83D0h
3D4h	32	EMIF_CTLCFG_DENALI_CTL_245	0F30 83D4h
3D8h	32	EMIF_CTLCFG_DENALI_CTL_246	0F30 83D8h
3DCh	32	EMIF_CTLCFG_DENALI_CTL_247	0F30 83DCh
3E0h	32	EMIF_CTLCFG_DENALI_CTL_248	0F30 83E0h
3E4h	32	EMIF_CTLCFG_DENALI_CTL_249	0F30 83E4h
3E8h	32	EMIF_CTLCFG_DENALI_CTL_250	0F30 83E8h
3ECh	32	EMIF_CTLCFG_DENALI_CTL_251	0F30 83ECh
3F0h	32	EMIF_CTLCFG_DENALI_CTL_252	0F30 83F0h
3F4h	32	EMIF_CTLCFG_DENALI_CTL_253	0F30 83F4h
3F8h	32	EMIF_CTLCFG_DENALI_CTL_254	0F30 83F8h
3FCh	32	EMIF_CTLCFG_DENALI_CTL_255	0F30 83FCh
400h	32	EMIF_CTLCFG_DENALI_CTL_256	0F30 8400h
404h	32	EMIF_CTLCFG_DENALI_CTL_257	0F30 8404h
408h	32	EMIF_CTLCFG_DENALI_CTL_258	0F30 8408h
40Ch	32	EMIF_CTLCFG_DENALI_CTL_259	0F30 840Ch
410h	32	EMIF_CTLCFG_DENALI_CTL_260	0F30 8410h
414h	32	EMIF_CTLCFG_DENALI_CTL_261	0F30 8414h
418h	32	EMIF_CTLCFG_DENALI_CTL_262	0F30 8418h
41Ch	32	EMIF_CTLCFG_DENALI_CTL_263	0F30 841Ch
420h	32	EMIF_CTLCFG_DENALI_CTL_264	0F30 8420h
424h	32	EMIF_CTLCFG_DENALI_CTL_265	0F30 8424h
428h	32	EMIF_CTLCFG_DENALI_CTL_266	0F30 8428h
42Ch	32	EMIF_CTLCFG_DENALI_CTL_267	0F30 842Ch
430h	32	EMIF_CTLCFG_DENALI_CTL_268	0F30 8430h
434h	32	EMIF_CTLCFG_DENALI_CTL_269	0F30 8434h
438h	32	EMIF_CTLCFG_DENALI_CTL_270	0F30 8438h
43Ch	32	EMIF_CTLCFG_DENALI_CTL_271	0F30 843Ch
440h	32	EMIF_CTLCFG_DENALI_CTL_272	0F30 8440h
444h	32	EMIF_CTLCFG_DENALI_CTL_273	0F30 8444h
448h	32	EMIF_CTLCFG_DENALI_CTL_274	0F30 8448h
44Ch	32	EMIF_CTLCFG_DENALI_CTL_275	0F30 844Ch
450h	32	EMIF_CTLCFG_DENALI_CTL_276	0F30 8450h
454h	32	EMIF_CTLCFG_DENALI_CTL_277	0F30 8454h
458h	32	EMIF_CTLCFG_DENALI_CTL_278	0F30 8458h
45Ch	32	EMIF_CTLCFG_DENALI_CTL_279	0F30 845Ch
460h	32	EMIF_CTLCFG_DENALI_CTL_280	0F30 8460h
464h	32	EMIF_CTLCFG_DENALI_CTL_281	0F30 8464h
468h	32	EMIF_CTLCFG_DENALI_CTL_282	0F30 8468h
46Ch	32	EMIF_CTLCFG_DENALI_CTL_283	0F30 846Ch
470h	32	EMIF_CTLCFG_DENALI_CTL_284	0F30 8470h
474h	32	EMIF_CTLCFG_DENALI_CTL_285	0F30 8474h
478h	32	EMIF_CTLCFG_DENALI_CTL_286	0F30 8478h
47Ch	32	EMIF_CTLCFG_DENALI_CTL_287	0F30 847Ch
480h	32	EMIF_CTLCFG_DENALI_CTL_288	0F30 8480h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
484h	32	EMIF_CTLCFG_DENALI_CTL_289	0F30 8484h
488h	32	EMIF_CTLCFG_DENALI_CTL_290	0F30 8488h
48Ch	32	EMIF_CTLCFG_DENALI_CTL_291	0F30 848Ch
490h	32	EMIF_CTLCFG_DENALI_CTL_292	0F30 8490h
494h	32	EMIF_CTLCFG_DENALI_CTL_293	0F30 8494h
498h	32	EMIF_CTLCFG_DENALI_CTL_294	0F30 8498h
49Ch	32	EMIF_CTLCFG_DENALI_CTL_295	0F30 849Ch
4A0h	32	EMIF_CTLCFG_DENALI_CTL_296	0F30 84A0h
4A4h	32	EMIF_CTLCFG_DENALI_CTL_297	0F30 84A4h
4A8h	32	EMIF_CTLCFG_DENALI_CTL_298	0F30 84A8h
4ACh	32	EMIF_CTLCFG_DENALI_CTL_299	0F30 84ACh
4B0h	32	EMIF_CTLCFG_DENALI_CTL_300	0F30 84B0h
4B4h	32	EMIF_CTLCFG_DENALI_CTL_301	0F30 84B4h
4B8h	32	EMIF_CTLCFG_DENALI_CTL_302	0F30 84B8h
4BCh	32	EMIF_CTLCFG_DENALI_CTL_303	0F30 84BCh
4C0h	32	EMIF_CTLCFG_DENALI_CTL_304	0F30 84C0h
4C4h	32	EMIF_CTLCFG_DENALI_CTL_305	0F30 84C4h
4C8h	32	EMIF_CTLCFG_DENALI_CTL_306	0F30 84C8h
4CCh	32	EMIF_CTLCFG_DENALI_CTL_307	0F30 84CCh
4D0h	32	EMIF_CTLCFG_DENALI_CTL_308	0F30 84D0h
4D4h	32	EMIF_CTLCFG_DENALI_CTL_309	0F30 84D4h
4D8h	32	EMIF_CTLCFG_DENALI_CTL_310	0F30 84D8h
4DCh	32	EMIF_CTLCFG_DENALI_CTL_311	0F30 84DCh
4E0h	32	EMIF_CTLCFG_DENALI_CTL_312	0F30 84E0h
4E4h	32	EMIF_CTLCFG_DENALI_CTL_313	0F30 84E4h
4E8h	32	EMIF_CTLCFG_DENALI_CTL_314	0F30 84E8h
4ECh	32	EMIF_CTLCFG_DENALI_CTL_315	0F30 84ECh
4F0h	32	EMIF_CTLCFG_DENALI_CTL_316	0F30 84F0h
4F4h	32	EMIF_CTLCFG_DENALI_CTL_317	0F30 84F4h
4F8h	32	EMIF_CTLCFG_DENALI_CTL_318	0F30 84F8h
4FCh	32	EMIF_CTLCFG_DENALI_CTL_319	0F30 84FCh
500h	32	EMIF_CTLCFG_DENALI_CTL_320	0F30 8500h
504h	32	EMIF_CTLCFG_DENALI_CTL_321	0F30 8504h
508h	32	EMIF_CTLCFG_DENALI_CTL_322	0F30 8508h
50Ch	32	EMIF_CTLCFG_DENALI_CTL_323	0F30 850Ch
510h	32	EMIF_CTLCFG_DENALI_CTL_324	0F30 8510h
514h	32	EMIF_CTLCFG_DENALI_CTL_325	0F30 8514h
518h	32	EMIF_CTLCFG_DENALI_CTL_326	0F30 8518h
51Ch	32	EMIF_CTLCFG_DENALI_CTL_327	0F30 851Ch
520h	32	EMIF_CTLCFG_DENALI_CTL_328	0F30 8520h
524h	32	EMIF_CTLCFG_DENALI_CTL_329	0F30 8524h
528h	32	EMIF_CTLCFG_DENALI_CTL_330	0F30 8528h
52Ch	32	EMIF_CTLCFG_DENALI_CTL_331	0F30 852Ch
530h	32	EMIF_CTLCFG_DENALI_CTL_332	0F30 8530h
534h	32	EMIF_CTLCFG_DENALI_CTL_333	0F30 8534h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
538h	32	EMIF_CTLCFG_DENALI_CTL_334	0F30 8538h
53Ch	32	EMIF_CTLCFG_DENALI_CTL_335	0F30 853Ch
540h	32	EMIF_CTLCFG_DENALI_CTL_336	0F30 8540h
544h	32	EMIF_CTLCFG_DENALI_CTL_337	0F30 8544h
548h	32	EMIF_CTLCFG_DENALI_CTL_338	0F30 8548h
54Ch	32	EMIF_CTLCFG_DENALI_CTL_339	0F30 854Ch
550h	32	EMIF_CTLCFG_DENALI_CTL_340	0F30 8550h
554h	32	EMIF_CTLCFG_DENALI_CTL_341	0F30 8554h
558h	32	EMIF_CTLCFG_DENALI_CTL_342	0F30 8558h
55Ch	32	EMIF_CTLCFG_DENALI_CTL_343	0F30 855Ch
560h	32	EMIF_CTLCFG_DENALI_CTL_344	0F30 8560h
564h	32	EMIF_CTLCFG_DENALI_CTL_345	0F30 8564h
568h	32	EMIF_CTLCFG_DENALI_CTL_346	0F30 8568h
56Ch	32	EMIF_CTLCFG_DENALI_CTL_347	0F30 856Ch
570h	32	EMIF_CTLCFG_DENALI_CTL_348	0F30 8570h
574h	32	EMIF_CTLCFG_DENALI_CTL_349	0F30 8574h
578h	32	EMIF_CTLCFG_DENALI_CTL_350	0F30 8578h
57Ch	32	EMIF_CTLCFG_DENALI_CTL_351	0F30 857Ch
580h	32	EMIF_CTLCFG_DENALI_CTL_352	0F30 8580h
584h	32	EMIF_CTLCFG_DENALI_CTL_353	0F30 8584h
588h	32	EMIF_CTLCFG_DENALI_CTL_354	0F30 8588h
58Ch	32	EMIF_CTLCFG_DENALI_CTL_355	0F30 858Ch
590h	32	EMIF_CTLCFG_DENALI_CTL_356	0F30 8590h
594h	32	EMIF_CTLCFG_DENALI_CTL_357	0F30 8594h
598h	32	EMIF_CTLCFG_DENALI_CTL_358	0F30 8598h
59Ch	32	EMIF_CTLCFG_DENALI_CTL_359	0F30 859Ch
5A0h	32	EMIF_CTLCFG_DENALI_CTL_360	0F30 85A0h
5A4h	32	EMIF_CTLCFG_DENALI_CTL_361	0F30 85A4h
5A8h	32	EMIF_CTLCFG_DENALI_CTL_362	0F30 85A8h
5ACh	32	EMIF_CTLCFG_DENALI_CTL_363	0F30 85ACh
5B0h	32	EMIF_CTLCFG_DENALI_CTL_364	0F30 85B0h
5B4h	32	EMIF_CTLCFG_DENALI_CTL_365	0F30 85B4h
5B8h	32	EMIF_CTLCFG_DENALI_CTL_366	0F30 85B8h
5BCh	32	EMIF_CTLCFG_DENALI_CTL_367	0F30 85BCh
5C0h	32	EMIF_CTLCFG_DENALI_CTL_368	0F30 85C0h
5C4h	32	EMIF_CTLCFG_DENALI_CTL_369	0F30 85C4h
5C8h	32	EMIF_CTLCFG_DENALI_CTL_370	0F30 85C8h
5CCh	32	EMIF_CTLCFG_DENALI_CTL_371	0F30 85CCh
5D0h	32	EMIF_CTLCFG_DENALI_CTL_372	0F30 85D0h
5D4h	32	EMIF_CTLCFG_DENALI_CTL_373	0F30 85D4h
5D8h	32	EMIF_CTLCFG_DENALI_CTL_374	0F30 85D8h
5DCh	32	EMIF_CTLCFG_DENALI_CTL_375	0F30 85DCh
5E0h	32	EMIF_CTLCFG_DENALI_CTL_376	0F30 85E0h
5E4h	32	EMIF_CTLCFG_DENALI_CTL_377	0F30 85E4h
5E8h	32	EMIF_CTLCFG_DENALI_CTL_378	0F30 85E8h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
5ECh	32	EMIF_CTLCFG_DENALI_CTL_379	0F30 85ECh
5F0h	32	EMIF_CTLCFG_DENALI_CTL_380	0F30 85F0h
5F4h	32	EMIF_CTLCFG_DENALI_CTL_381	0F30 85F4h
5F8h	32	EMIF_CTLCFG_DENALI_CTL_382	0F30 85F8h
5FCh	32	EMIF_CTLCFG_DENALI_CTL_383	0F30 85FCh
600h	32	EMIF_CTLCFG_DENALI_CTL_384	0F30 8600h
604h	32	EMIF_CTLCFG_DENALI_CTL_385	0F30 8604h
608h	32	EMIF_CTLCFG_DENALI_CTL_386	0F30 8608h
60Ch	32	EMIF_CTLCFG_DENALI_CTL_387	0F30 860Ch
610h	32	EMIF_CTLCFG_DENALI_CTL_388	0F30 8610h
614h	32	EMIF_CTLCFG_DENALI_CTL_389	0F30 8614h
618h	32	EMIF_CTLCFG_DENALI_CTL_390	0F30 8618h
61Ch	32	EMIF_CTLCFG_DENALI_CTL_391	0F30 861Ch
620h	32	EMIF_CTLCFG_DENALI_CTL_392	0F30 8620h
624h	32	EMIF_CTLCFG_DENALI_CTL_393	0F30 8624h
628h	32	EMIF_CTLCFG_DENALI_CTL_394	0F30 8628h
62Ch	32	EMIF_CTLCFG_DENALI_CTL_395	0F30 862Ch
630h	32	EMIF_CTLCFG_DENALI_CTL_396	0F30 8630h
634h	32	EMIF_CTLCFG_DENALI_CTL_397	0F30 8634h
638h	32	EMIF_CTLCFG_DENALI_CTL_398	0F30 8638h
63Ch	32	EMIF_CTLCFG_DENALI_CTL_399	0F30 863Ch
640h	32	EMIF_CTLCFG_DENALI_CTL_400	0F30 8640h
644h	32	EMIF_CTLCFG_DENALI_CTL_401	0F30 8644h
648h	32	EMIF_CTLCFG_DENALI_CTL_402	0F30 8648h
64Ch	32	EMIF_CTLCFG_DENALI_CTL_403	0F30 864Ch
650h	32	EMIF_CTLCFG_DENALI_CTL_404	0F30 8650h
654h	32	EMIF_CTLCFG_DENALI_CTL_405	0F30 8654h
658h	32	EMIF_CTLCFG_DENALI_CTL_406	0F30 8658h
65Ch	32	EMIF_CTLCFG_DENALI_CTL_407	0F30 865Ch
660h	32	EMIF_CTLCFG_DENALI_CTL_408	0F30 8660h
664h	32	EMIF_CTLCFG_DENALI_CTL_409	0F30 8664h
668h	32	EMIF_CTLCFG_DENALI_CTL_410	0F30 8668h
66Ch	32	EMIF_CTLCFG_DENALI_CTL_411	0F30 866Ch
670h	32	EMIF_CTLCFG_DENALI_CTL_412	0F30 8670h
674h	32	EMIF_CTLCFG_DENALI_CTL_413	0F30 8674h
678h	32	EMIF_CTLCFG_DENALI_CTL_414	0F30 8678h
67Ch	32	EMIF_CTLCFG_DENALI_CTL_415	0F30 867Ch
680h	32	EMIF_CTLCFG_DENALI_CTL_416	0F30 8680h
684h	32	EMIF_CTLCFG_DENALI_CTL_417	0F30 8684h
688h	32	EMIF_CTLCFG_DENALI_CTL_418	0F30 8688h
68Ch	32	EMIF_CTLCFG_DENALI_CTL_419	0F30 868Ch
690h	32	EMIF_CTLCFG_DENALI_CTL_420	0F30 8690h
694h	32	EMIF_CTLCFG_DENALI_CTL_421	0F30 8694h
698h	32	EMIF_CTLCFG_DENALI_CTL_422	0F30 8698h
69Ch	32	EMIF_CTLCFG_DENALI_CTL_423	0F30 869Ch

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
6A0h	32	EMIF_CTLCFG_DENALI_CTL_424	0F30 86A0h
6A4h	32	EMIF_CTLCFG_DENALI_CTL_425	0F30 86A4h
6A8h	32	EMIF_CTLCFG_DENALI_CTL_426	0F30 86A8h
6ACh	32	EMIF_CTLCFG_DENALI_CTL_427	0F30 86ACh
6B0h	32	EMIF_CTLCFG_DENALI_CTL_428	0F30 86B0h
6B4h	32	EMIF_CTLCFG_DENALI_CTL_429	0F30 86B4h
6B8h	32	EMIF_CTLCFG_DENALI_CTL_430	0F30 86B8h
6BCh	32	EMIF_CTLCFG_DENALI_CTL_431	0F30 86BCh
6C0h	32	EMIF_CTLCFG_DENALI_CTL_432	0F30 86C0h
6C4h	32	EMIF_CTLCFG_DENALI_CTL_433	0F30 86C4h
6C8h	32	EMIF_CTLCFG_DENALI_CTL_434	0F30 86C8h
2000h	32	EMIF_CTLCFG_DENALI_PI_0	0F30 A000h
2004h	32	EMIF_CTLCFG_DENALI_PI_1	0F30 A004h
2008h	32	EMIF_CTLCFG_DENALI_PI_2	0F30 A008h
200Ch	32	EMIF_CTLCFG_DENALI_PI_3	0F30 A00Ch
2010h	32	EMIF_CTLCFG_DENALI_PI_4	0F30 A010h
2014h	32	EMIF_CTLCFG_DENALI_PI_5	0F30 A014h
2018h	32	EMIF_CTLCFG_DENALI_PI_6	0F30 A018h
201Ch	32	EMIF_CTLCFG_DENALI_PI_7	0F30 A01Ch
2020h	32	EMIF_CTLCFG_DENALI_PI_8	0F30 A020h
2024h	32	EMIF_CTLCFG_DENALI_PI_9	0F30 A024h
2028h	32	EMIF_CTLCFG_DENALI_PI_10	0F30 A028h
202Ch	32	EMIF_CTLCFG_DENALI_PI_11	0F30 A02Ch
2030h	32	EMIF_CTLCFG_DENALI_PI_12	0F30 A030h
2034h	32	EMIF_CTLCFG_DENALI_PI_13	0F30 A034h
2038h	32	EMIF_CTLCFG_DENALI_PI_14	0F30 A038h
203Ch	32	EMIF_CTLCFG_DENALI_PI_15	0F30 A03Ch
2040h	32	EMIF_CTLCFG_DENALI_PI_16	0F30 A040h
2044h	32	EMIF_CTLCFG_DENALI_PI_17	0F30 A044h
2048h	32	EMIF_CTLCFG_DENALI_PI_18	0F30 A048h
204Ch	32	EMIF_CTLCFG_DENALI_PI_19	0F30 A04Ch
2050h	32	EMIF_CTLCFG_DENALI_PI_20	0F30 A050h
2054h	32	EMIF_CTLCFG_DENALI_PI_21	0F30 A054h
2058h	32	EMIF_CTLCFG_DENALI_PI_22	0F30 A058h
205Ch	32	EMIF_CTLCFG_DENALI_PI_23	0F30 A05Ch
2060h	32	EMIF_CTLCFG_DENALI_PI_24	0F30 A060h
2064h	32	EMIF_CTLCFG_DENALI_PI_25	0F30 A064h
2068h	32	EMIF_CTLCFG_DENALI_PI_26	0F30 A068h
206Ch	32	EMIF_CTLCFG_DENALI_PI_27	0F30 A06Ch
2070h	32	EMIF_CTLCFG_DENALI_PI_28	0F30 A070h
2074h	32	EMIF_CTLCFG_DENALI_PI_29	0F30 A074h
2078h	32	EMIF_CTLCFG_DENALI_PI_30	0F30 A078h
207Ch	32	EMIF_CTLCFG_DENALI_PI_31	0F30 A07Ch
2080h	32	EMIF_CTLCFG_DENALI_PI_32	0F30 A080h
2084h	32	EMIF_CTLCFG_DENALI_PI_33	0F30 A084h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
2088h	32	EMIF_CTLCFG_DENALI_PI_34	0F30 A088h
208Ch	32	EMIF_CTLCFG_DENALI_PI_35	0F30 A08Ch
2090h	32	EMIF_CTLCFG_DENALI_PI_36	0F30 A090h
2094h	32	EMIF_CTLCFG_DENALI_PI_37	0F30 A094h
2098h	32	EMIF_CTLCFG_DENALI_PI_38	0F30 A098h
209Ch	32	EMIF_CTLCFG_DENALI_PI_39	0F30 A09Ch
20A0h	32	EMIF_CTLCFG_DENALI_PI_40	0F30 A0A0h
20A4h	32	EMIF_CTLCFG_DENALI_PI_41	0F30 A0A4h
20A8h	32	EMIF_CTLCFG_DENALI_PI_42	0F30 A0A8h
20ACh	32	EMIF_CTLCFG_DENALI_PI_43	0F30 A0ACh
20B0h	32	EMIF_CTLCFG_DENALI_PI_44	0F30 A0B0h
20B4h	32	EMIF_CTLCFG_DENALI_PI_45	0F30 A0B4h
20B8h	32	EMIF_CTLCFG_DENALI_PI_46	0F30 A0B8h
20BCh	32	EMIF_CTLCFG_DENALI_PI_47	0F30 A0BCh
20C0h	32	EMIF_CTLCFG_DENALI_PI_48	0F30 A0C0h
20C4h	32	EMIF_CTLCFG_DENALI_PI_49	0F30 A0C4h
20C8h	32	EMIF_CTLCFG_DENALI_PI_50	0F30 A0C8h
20CCh	32	EMIF_CTLCFG_DENALI_PI_51	0F30 A0CCh
20D0h	32	EMIF_CTLCFG_DENALI_PI_52	0F30 A0D0h
20D4h	32	EMIF_CTLCFG_DENALI_PI_53	0F30 A0D4h
20D8h	32	EMIF_CTLCFG_DENALI_PI_54	0F30 A0D8h
20DCh	32	EMIF_CTLCFG_DENALI_PI_55	0F30 A0DCh
20E0h	32	EMIF_CTLCFG_DENALI_PI_56	0F30 A0E0h
20E4h	32	EMIF_CTLCFG_DENALI_PI_57	0F30 A0E4h
20E8h	32	EMIF_CTLCFG_DENALI_PI_58	0F30 A0E8h
20ECh	32	EMIF_CTLCFG_DENALI_PI_59	0F30 A0ECh
20F0h	32	EMIF_CTLCFG_DENALI_PI_60	0F30 A0F0h
20F4h	32	EMIF_CTLCFG_DENALI_PI_61	0F30 A0F4h
20F8h	32	EMIF_CTLCFG_DENALI_PI_62	0F30 A0F8h
20FCh	32	EMIF_CTLCFG_DENALI_PI_63	0F30 A0FCh
2100h	32	EMIF_CTLCFG_DENALI_PI_64	0F30 A100h
2104h	32	EMIF_CTLCFG_DENALI_PI_65	0F30 A104h
2108h	32	EMIF_CTLCFG_DENALI_PI_66	0F30 A108h
210Ch	32	EMIF_CTLCFG_DENALI_PI_67	0F30 A10Ch
2110h	32	EMIF_CTLCFG_DENALI_PI_68	0F30 A110h
2114h	32	EMIF_CTLCFG_DENALI_PI_69	0F30 A114h
2118h	32	EMIF_CTLCFG_DENALI_PI_70	0F30 A118h
211Ch	32	EMIF_CTLCFG_DENALI_PI_71	0F30 A11Ch
2120h	32	EMIF_CTLCFG_DENALI_PI_72	0F30 A120h
2124h	32	EMIF_CTLCFG_DENALI_PI_73	0F30 A124h
2128h	32	EMIF_CTLCFG_DENALI_PI_74	0F30 A128h
212Ch	32	EMIF_CTLCFG_DENALI_PI_75	0F30 A12Ch
2130h	32	EMIF_CTLCFG_DENALI_PI_76	0F30 A130h
2134h	32	EMIF_CTLCFG_DENALI_PI_77	0F30 A134h
2138h	32	EMIF_CTLCFG_DENALI_PI_78	0F30 A138h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
213Ch	32	EMIF_CTLCFG_DENALI_PI_79	0F30 A13Ch
2140h	32	EMIF_CTLCFG_DENALI_PI_80	0F30 A140h
2144h	32	EMIF_CTLCFG_DENALI_PI_81	0F30 A144h
2148h	32	EMIF_CTLCFG_DENALI_PI_82	0F30 A148h
214Ch	32	EMIF_CTLCFG_DENALI_PI_83	0F30 A14Ch
2150h	32	EMIF_CTLCFG_DENALI_PI_84	0F30 A150h
2154h	32	EMIF_CTLCFG_DENALI_PI_85	0F30 A154h
2158h	32	EMIF_CTLCFG_DENALI_PI_86	0F30 A158h
215Ch	32	EMIF_CTLCFG_DENALI_PI_87	0F30 A15Ch
2160h	32	EMIF_CTLCFG_DENALI_PI_88	0F30 A160h
2164h	32	EMIF_CTLCFG_DENALI_PI_89	0F30 A164h
2168h	32	EMIF_CTLCFG_DENALI_PI_90	0F30 A168h
216Ch	32	EMIF_CTLCFG_DENALI_PI_91	0F30 A16Ch
2170h	32	EMIF_CTLCFG_DENALI_PI_92	0F30 A170h
2174h	32	EMIF_CTLCFG_DENALI_PI_93	0F30 A174h
2178h	32	EMIF_CTLCFG_DENALI_PI_94	0F30 A178h
217Ch	32	EMIF_CTLCFG_DENALI_PI_95	0F30 A17Ch
2180h	32	EMIF_CTLCFG_DENALI_PI_96	0F30 A180h
2184h	32	EMIF_CTLCFG_DENALI_PI_97	0F30 A184h
2188h	32	EMIF_CTLCFG_DENALI_PI_98	0F30 A188h
218Ch	32	EMIF_CTLCFG_DENALI_PI_99	0F30 A18Ch
2190h	32	EMIF_CTLCFG_DENALI_PI_100	0F30 A190h
2194h	32	EMIF_CTLCFG_DENALI_PI_101	0F30 A194h
2198h	32	EMIF_CTLCFG_DENALI_PI_102	0F30 A198h
219Ch	32	EMIF_CTLCFG_DENALI_PI_103	0F30 A19Ch
21A0h	32	EMIF_CTLCFG_DENALI_PI_104	0F30 A1A0h
21A4h	32	EMIF_CTLCFG_DENALI_PI_105	0F30 A1A4h
21A8h	32	EMIF_CTLCFG_DENALI_PI_106	0F30 A1A8h
21ACh	32	EMIF_CTLCFG_DENALI_PI_107	0F30 A1ACh
21B0h	32	EMIF_CTLCFG_DENALI_PI_108	0F30 A1B0h
21B4h	32	EMIF_CTLCFG_DENALI_PI_109	0F30 A1B4h
21B8h	32	EMIF_CTLCFG_DENALI_PI_110	0F30 A1B8h
21BCh	32	EMIF_CTLCFG_DENALI_PI_111	0F30 A1BCh
21C0h	32	EMIF_CTLCFG_DENALI_PI_112	0F30 A1C0h
21C4h	32	EMIF_CTLCFG_DENALI_PI_113	0F30 A1C4h
21C8h	32	EMIF_CTLCFG_DENALI_PI_114	0F30 A1C8h
21CCh	32	EMIF_CTLCFG_DENALI_PI_115	0F30 A1CCh
21D0h	32	EMIF_CTLCFG_DENALI_PI_116	0F30 A1D0h
21D4h	32	EMIF_CTLCFG_DENALI_PI_117	0F30 A1D4h
21D8h	32	EMIF_CTLCFG_DENALI_PI_118	0F30 A1D8h
21DCh	32	EMIF_CTLCFG_DENALI_PI_119	0F30 A1DCh
21E0h	32	EMIF_CTLCFG_DENALI_PI_120	0F30 A1E0h
21E4h	32	EMIF_CTLCFG_DENALI_PI_121	0F30 A1E4h
21E8h	32	EMIF_CTLCFG_DENALI_PI_122	0F30 A1E8h
21ECh	32	EMIF_CTLCFG_DENALI_PI_123	0F30 A1ECh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
21F0h	32	EMIF_CTLCFG_DENALI_PI_124	0F30 A1F0h
21F4h	32	EMIF_CTLCFG_DENALI_PI_125	0F30 A1F4h
21F8h	32	EMIF_CTLCFG_DENALI_PI_126	0F30 A1F8h
21FCh	32	EMIF_CTLCFG_DENALI_PI_127	0F30 A1FCh
2200h	32	EMIF_CTLCFG_DENALI_PI_128	0F30 A200h
2204h	32	EMIF_CTLCFG_DENALI_PI_129	0F30 A204h
2208h	32	EMIF_CTLCFG_DENALI_PI_130	0F30 A208h
220Ch	32	EMIF_CTLCFG_DENALI_PI_131	0F30 A20Ch
2210h	32	EMIF_CTLCFG_DENALI_PI_132	0F30 A210h
2214h	32	EMIF_CTLCFG_DENALI_PI_133	0F30 A214h
2218h	32	EMIF_CTLCFG_DENALI_PI_134	0F30 A218h
221Ch	32	EMIF_CTLCFG_DENALI_PI_135	0F30 A21Ch
2220h	32	EMIF_CTLCFG_DENALI_PI_136	0F30 A220h
2224h	32	EMIF_CTLCFG_DENALI_PI_137	0F30 A224h
2228h	32	EMIF_CTLCFG_DENALI_PI_138	0F30 A228h
222Ch	32	EMIF_CTLCFG_DENALI_PI_139	0F30 A22Ch
2230h	32	EMIF_CTLCFG_DENALI_PI_140	0F30 A230h
2234h	32	EMIF_CTLCFG_DENALI_PI_141	0F30 A234h
2238h	32	EMIF_CTLCFG_DENALI_PI_142	0F30 A238h
223Ch	32	EMIF_CTLCFG_DENALI_PI_143	0F30 A23Ch
2240h	32	EMIF_CTLCFG_DENALI_PI_144	0F30 A240h
2244h	32	EMIF_CTLCFG_DENALI_PI_145	0F30 A244h
2248h	32	EMIF_CTLCFG_DENALI_PI_146	0F30 A248h
224Ch	32	EMIF_CTLCFG_DENALI_PI_147	0F30 A24Ch
2250h	32	EMIF_CTLCFG_DENALI_PI_148	0F30 A250h
2254h	32	EMIF_CTLCFG_DENALI_PI_149	0F30 A254h
2258h	32	EMIF_CTLCFG_DENALI_PI_150	0F30 A258h
225Ch	32	EMIF_CTLCFG_DENALI_PI_151	0F30 A25Ch
2260h	32	EMIF_CTLCFG_DENALI_PI_152	0F30 A260h
2264h	32	EMIF_CTLCFG_DENALI_PI_153	0F30 A264h
2268h	32	EMIF_CTLCFG_DENALI_PI_154	0F30 A268h
226Ch	32	EMIF_CTLCFG_DENALI_PI_155	0F30 A26Ch
2270h	32	EMIF_CTLCFG_DENALI_PI_156	0F30 A270h
2274h	32	EMIF_CTLCFG_DENALI_PI_157	0F30 A274h
2278h	32	EMIF_CTLCFG_DENALI_PI_158	0F30 A278h
227Ch	32	EMIF_CTLCFG_DENALI_PI_159	0F30 A27Ch
2280h	32	EMIF_CTLCFG_DENALI_PI_160	0F30 A280h
2284h	32	EMIF_CTLCFG_DENALI_PI_161	0F30 A284h
2288h	32	EMIF_CTLCFG_DENALI_PI_162	0F30 A288h
228Ch	32	EMIF_CTLCFG_DENALI_PI_163	0F30 A28Ch
2290h	32	EMIF_CTLCFG_DENALI_PI_164	0F30 A290h
2294h	32	EMIF_CTLCFG_DENALI_PI_165	0F30 A294h
2298h	32	EMIF_CTLCFG_DENALI_PI_166	0F30 A298h
229Ch	32	EMIF_CTLCFG_DENALI_PI_167	0F30 A29Ch
22A0h	32	EMIF_CTLCFG_DENALI_PI_168	0F30 A2A0h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
22A4h	32	EMIF_CTLCFG_DENALI_PI_169	0F30 A2A4h
22A8h	32	EMIF_CTLCFG_DENALI_PI_170	0F30 A2A8h
22ACh	32	EMIF_CTLCFG_DENALI_PI_171	0F30 A2ACh
22B0h	32	EMIF_CTLCFG_DENALI_PI_172	0F30 A2B0h
22B4h	32	EMIF_CTLCFG_DENALI_PI_173	0F30 A2B4h
22B8h	32	EMIF_CTLCFG_DENALI_PI_174	0F30 A2B8h
22BCh	32	EMIF_CTLCFG_DENALI_PI_175	0F30 A2BCh
22C0h	32	EMIF_CTLCFG_DENALI_PI_176	0F30 A2C0h
22C4h	32	EMIF_CTLCFG_DENALI_PI_177	0F30 A2C4h
22C8h	32	EMIF_CTLCFG_DENALI_PI_178	0F30 A2C8h
22CCh	32	EMIF_CTLCFG_DENALI_PI_179	0F30 A2CCh
22D0h	32	EMIF_CTLCFG_DENALI_PI_180	0F30 A2D0h
22D4h	32	EMIF_CTLCFG_DENALI_PI_181	0F30 A2D4h
22D8h	32	EMIF_CTLCFG_DENALI_PI_182	0F30 A2D8h
22DCh	32	EMIF_CTLCFG_DENALI_PI_183	0F30 A2DCh
22E0h	32	EMIF_CTLCFG_DENALI_PI_184	0F30 A2E0h
22E4h	32	EMIF_CTLCFG_DENALI_PI_185	0F30 A2E4h
22E8h	32	EMIF_CTLCFG_DENALI_PI_186	0F30 A2E8h
22ECh	32	EMIF_CTLCFG_DENALI_PI_187	0F30 A2ECh
22F0h	32	EMIF_CTLCFG_DENALI_PI_188	0F30 A2F0h
22F4h	32	EMIF_CTLCFG_DENALI_PI_189	0F30 A2F4h
22F8h	32	EMIF_CTLCFG_DENALI_PI_190	0F30 A2F8h
22FCh	32	EMIF_CTLCFG_DENALI_PI_191	0F30 A2FCh
2300h	32	EMIF_CTLCFG_DENALI_PI_192	0F30 A300h
2304h	32	EMIF_CTLCFG_DENALI_PI_193	0F30 A304h
2308h	32	EMIF_CTLCFG_DENALI_PI_194	0F30 A308h
230Ch	32	EMIF_CTLCFG_DENALI_PI_195	0F30 A30Ch
2310h	32	EMIF_CTLCFG_DENALI_PI_196	0F30 A310h
2314h	32	EMIF_CTLCFG_DENALI_PI_197	0F30 A314h
2318h	32	EMIF_CTLCFG_DENALI_PI_198	0F30 A318h
231Ch	32	EMIF_CTLCFG_DENALI_PI_199	0F30 A31Ch
2320h	32	EMIF_CTLCFG_DENALI_PI_200	0F30 A320h
2324h	32	EMIF_CTLCFG_DENALI_PI_201	0F30 A324h
2328h	32	EMIF_CTLCFG_DENALI_PI_202	0F30 A328h
232Ch	32	EMIF_CTLCFG_DENALI_PI_203	0F30 A32Ch
2330h	32	EMIF_CTLCFG_DENALI_PI_204	0F30 A330h
2334h	32	EMIF_CTLCFG_DENALI_PI_205	0F30 A334h
2338h	32	EMIF_CTLCFG_DENALI_PI_206	0F30 A338h
233Ch	32	EMIF_CTLCFG_DENALI_PI_207	0F30 A33Ch
2340h	32	EMIF_CTLCFG_DENALI_PI_208	0F30 A340h
2344h	32	EMIF_CTLCFG_DENALI_PI_209	0F30 A344h
2348h	32	EMIF_CTLCFG_DENALI_PI_210	0F30 A348h
234Ch	32	EMIF_CTLCFG_DENALI_PI_211	0F30 A34Ch
2350h	32	EMIF_CTLCFG_DENALI_PI_212	0F30 A350h
2354h	32	EMIF_CTLCFG_DENALI_PI_213	0F30 A354h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
2358h	32	EMIF_CTLCFG_DENALI_PI_214	0F30 A358h
235Ch	32	EMIF_CTLCFG_DENALI_PI_215	0F30 A35Ch
2360h	32	EMIF_CTLCFG_DENALI_PI_216	0F30 A360h
2364h	32	EMIF_CTLCFG_DENALI_PI_217	0F30 A364h
2368h	32	EMIF_CTLCFG_DENALI_PI_218	0F30 A368h
236Ch	32	EMIF_CTLCFG_DENALI_PI_219	0F30 A36Ch
2370h	32	EMIF_CTLCFG_DENALI_PI_220	0F30 A370h
2374h	32	EMIF_CTLCFG_DENALI_PI_221	0F30 A374h
2378h	32	EMIF_CTLCFG_DENALI_PI_222	0F30 A378h
237Ch	32	EMIF_CTLCFG_DENALI_PI_223	0F30 A37Ch
2380h	32	EMIF_CTLCFG_DENALI_PI_224	0F30 A380h
2384h	32	EMIF_CTLCFG_DENALI_PI_225	0F30 A384h
2388h	32	EMIF_CTLCFG_DENALI_PI_226	0F30 A388h
238Ch	32	EMIF_CTLCFG_DENALI_PI_227	0F30 A38Ch
2390h	32	EMIF_CTLCFG_DENALI_PI_228	0F30 A390h
2394h	32	EMIF_CTLCFG_DENALI_PI_229	0F30 A394h
2398h	32	EMIF_CTLCFG_DENALI_PI_230	0F30 A398h
239Ch	32	EMIF_CTLCFG_DENALI_PI_231	0F30 A39Ch
23A0h	32	EMIF_CTLCFG_DENALI_PI_232	0F30 A3A0h
23A4h	32	EMIF_CTLCFG_DENALI_PI_233	0F30 A3A4h
23A8h	32	EMIF_CTLCFG_DENALI_PI_234	0F30 A3A8h
23ACh	32	EMIF_CTLCFG_DENALI_PI_235	0F30 A3ACh
23B0h	32	EMIF_CTLCFG_DENALI_PI_236	0F30 A3B0h
23B4h	32	EMIF_CTLCFG_DENALI_PI_237	0F30 A3B4h
23B8h	32	EMIF_CTLCFG_DENALI_PI_238	0F30 A3B8h
23BCh	32	EMIF_CTLCFG_DENALI_PI_239	0F30 A3BCh
23C0h	32	EMIF_CTLCFG_DENALI_PI_240	0F30 A3C0h
23C4h	32	EMIF_CTLCFG_DENALI_PI_241	0F30 A3C4h
23C8h	32	EMIF_CTLCFG_DENALI_PI_242	0F30 A3C8h
23CCh	32	EMIF_CTLCFG_DENALI_PI_243	0F30 A3CCh
23D0h	32	EMIF_CTLCFG_DENALI_PI_244	0F30 A3D0h
23D4h	32	EMIF_CTLCFG_DENALI_PI_245	0F30 A3D4h
23D8h	32	EMIF_CTLCFG_DENALI_PI_246	0F30 A3D8h
23DCh	32	EMIF_CTLCFG_DENALI_PI_247	0F30 A3DCh
23E0h	32	EMIF_CTLCFG_DENALI_PI_248	0F30 A3E0h
23E4h	32	EMIF_CTLCFG_DENALI_PI_249	0F30 A3E4h
23E8h	32	EMIF_CTLCFG_DENALI_PI_250	0F30 A3E8h
23ECh	32	EMIF_CTLCFG_DENALI_PI_251	0F30 A3ECh
23F0h	32	EMIF_CTLCFG_DENALI_PI_252	0F30 A3F0h
23F4h	32	EMIF_CTLCFG_DENALI_PI_253	0F30 A3F4h
23F8h	32	EMIF_CTLCFG_DENALI_PI_254	0F30 A3F8h
23FCh	32	EMIF_CTLCFG_DENALI_PI_255	0F30 A3FCh
2400h	32	EMIF_CTLCFG_DENALI_PI_256	0F30 A400h
2404h	32	EMIF_CTLCFG_DENALI_PI_257	0F30 A404h
2408h	32	EMIF_CTLCFG_DENALI_PI_258	0F30 A408h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
240Ch	32	EMIF_CTLCFG_DENALI_PI_259	0F30 A40Ch
2410h	32	EMIF_CTLCFG_DENALI_PI_260	0F30 A410h
2414h	32	EMIF_CTLCFG_DENALI_PI_261	0F30 A414h
2418h	32	EMIF_CTLCFG_DENALI_PI_262	0F30 A418h
241Ch	32	EMIF_CTLCFG_DENALI_PI_263	0F30 A41Ch
2420h	32	EMIF_CTLCFG_DENALI_PI_264	0F30 A420h
2424h	32	EMIF_CTLCFG_DENALI_PI_265	0F30 A424h
2428h	32	EMIF_CTLCFG_DENALI_PI_266	0F30 A428h
242Ch	32	EMIF_CTLCFG_DENALI_PI_267	0F30 A42Ch
2430h	32	EMIF_CTLCFG_DENALI_PI_268	0F30 A430h
2434h	32	EMIF_CTLCFG_DENALI_PI_269	0F30 A434h
2438h	32	EMIF_CTLCFG_DENALI_PI_270	0F30 A438h
243Ch	32	EMIF_CTLCFG_DENALI_PI_271	0F30 A43Ch
2440h	32	EMIF_CTLCFG_DENALI_PI_272	0F30 A440h
2444h	32	EMIF_CTLCFG_DENALI_PI_273	0F30 A444h
2448h	32	EMIF_CTLCFG_DENALI_PI_274	0F30 A448h
244Ch	32	EMIF_CTLCFG_DENALI_PI_275	0F30 A44Ch
2450h	32	EMIF_CTLCFG_DENALI_PI_276	0F30 A450h
2454h	32	EMIF_CTLCFG_DENALI_PI_277	0F30 A454h
2458h	32	EMIF_CTLCFG_DENALI_PI_278	0F30 A458h
245Ch	32	EMIF_CTLCFG_DENALI_PI_279	0F30 A45Ch
2460h	32	EMIF_CTLCFG_DENALI_PI_280	0F30 A460h
2464h	32	EMIF_CTLCFG_DENALI_PI_281	0F30 A464h
2468h	32	EMIF_CTLCFG_DENALI_PI_282	0F30 A468h
246Ch	32	EMIF_CTLCFG_DENALI_PI_283	0F30 A46Ch
2470h	32	EMIF_CTLCFG_DENALI_PI_284	0F30 A470h
2474h	32	EMIF_CTLCFG_DENALI_PI_285	0F30 A474h
2478h	32	EMIF_CTLCFG_DENALI_PI_286	0F30 A478h
247Ch	32	EMIF_CTLCFG_DENALI_PI_287	0F30 A47Ch
2480h	32	EMIF_CTLCFG_DENALI_PI_288	0F30 A480h
2484h	32	EMIF_CTLCFG_DENALI_PI_289	0F30 A484h
2488h	32	EMIF_CTLCFG_DENALI_PI_290	0F30 A488h
248Ch	32	EMIF_CTLCFG_DENALI_PI_291	0F30 A48Ch
2490h	32	EMIF_CTLCFG_DENALI_PI_292	0F30 A490h
2494h	32	EMIF_CTLCFG_DENALI_PI_293	0F30 A494h
2498h	32	EMIF_CTLCFG_DENALI_PI_294	0F30 A498h
249Ch	32	EMIF_CTLCFG_DENALI_PI_295	0F30 A49Ch
24A0h	32	EMIF_CTLCFG_DENALI_PI_296	0F30 A4A0h
24A4h	32	EMIF_CTLCFG_DENALI_PI_297	0F30 A4A4h
24A8h	32	EMIF_CTLCFG_DENALI_PI_298	0F30 A4A8h
24ACh	32	EMIF_CTLCFG_DENALI_PI_299	0F30 A4ACh
24B0h	32	EMIF_CTLCFG_DENALI_PI_300	0F30 A4B0h
24B4h	32	EMIF_CTLCFG_DENALI_PI_301	0F30 A4B4h
24B8h	32	EMIF_CTLCFG_DENALI_PI_302	0F30 A4B8h
24BCh	32	EMIF_CTLCFG_DENALI_PI_303	0F30 A4BCh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
24C0h	32	EMIF_CTLCFG_DENALI_PI_304	0F30 A4C0h
24C4h	32	EMIF_CTLCFG_DENALI_PI_305	0F30 A4C4h
24C8h	32	EMIF_CTLCFG_DENALI_PI_306	0F30 A4C8h
24CCh	32	EMIF_CTLCFG_DENALI_PI_307	0F30 A4CCh
24D0h	32	EMIF_CTLCFG_DENALI_PI_308	0F30 A4D0h
24D4h	32	EMIF_CTLCFG_DENALI_PI_309	0F30 A4D4h
24D8h	32	EMIF_CTLCFG_DENALI_PI_310	0F30 A4D8h
24DCh	32	EMIF_CTLCFG_DENALI_PI_311	0F30 A4DCh
24E0h	32	EMIF_CTLCFG_DENALI_PI_312	0F30 A4E0h
24E4h	32	EMIF_CTLCFG_DENALI_PI_313	0F30 A4E4h
24E8h	32	EMIF_CTLCFG_DENALI_PI_314	0F30 A4E8h
24ECh	32	EMIF_CTLCFG_DENALI_PI_315	0F30 A4ECh
24F0h	32	EMIF_CTLCFG_DENALI_PI_316	0F30 A4F0h
24F4h	32	EMIF_CTLCFG_DENALI_PI_317	0F30 A4F4h
24F8h	32	EMIF_CTLCFG_DENALI_PI_318	0F30 A4F8h
24FCh	32	EMIF_CTLCFG_DENALI_PI_319	0F30 A4FCh
2500h	32	EMIF_CTLCFG_DENALI_PI_320	0F30 A500h
2504h	32	EMIF_CTLCFG_DENALI_PI_321	0F30 A504h
2508h	32	EMIF_CTLCFG_DENALI_PI_322	0F30 A508h
250Ch	32	EMIF_CTLCFG_DENALI_PI_323	0F30 A50Ch
2510h	32	EMIF_CTLCFG_DENALI_PI_324	0F30 A510h
2514h	32	EMIF_CTLCFG_DENALI_PI_325	0F30 A514h
2518h	32	EMIF_CTLCFG_DENALI_PI_326	0F30 A518h
251Ch	32	EMIF_CTLCFG_DENALI_PI_327	0F30 A51Ch
2520h	32	EMIF_CTLCFG_DENALI_PI_328	0F30 A520h
2524h	32	EMIF_CTLCFG_DENALI_PI_329	0F30 A524h
2528h	32	EMIF_CTLCFG_DENALI_PI_330	0F30 A528h
252Ch	32	EMIF_CTLCFG_DENALI_PI_331	0F30 A52Ch
2530h	32	EMIF_CTLCFG_DENALI_PI_332	0F30 A530h
2534h	32	EMIF_CTLCFG_DENALI_PI_333	0F30 A534h
2538h	32	EMIF_CTLCFG_DENALI_PI_334	0F30 A538h
253Ch	32	EMIF_CTLCFG_DENALI_PI_335	0F30 A53Ch
2540h	32	EMIF_CTLCFG_DENALI_PI_336	0F30 A540h
2544h	32	EMIF_CTLCFG_DENALI_PI_337	0F30 A544h
2548h	32	EMIF_CTLCFG_DENALI_PI_338	0F30 A548h
254Ch	32	EMIF_CTLCFG_DENALI_PI_339	0F30 A54Ch
2550h	32	EMIF_CTLCFG_DENALI_PI_340	0F30 A550h
2554h	32	EMIF_CTLCFG_DENALI_PI_341	0F30 A554h
2558h	32	EMIF_CTLCFG_DENALI_PI_342	0F30 A558h
255Ch	32	EMIF_CTLCFG_DENALI_PI_343	0F30 A55Ch
2560h	32	EMIF_CTLCFG_DENALI_PI_344	0F30 A560h
2564h	32	EMIF_CTLCFG_DENALI_PI_345	0F30 A564h
2568h	32	EMIF_CTLCFG_DENALI_PI_346	0F30 A568h
256Ch	32	EMIF_CTLCFG_DENALI_PI_347	0F30 A56Ch
2570h	32	EMIF_CTLCFG_DENALI_PI_348	0F30 A570h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
2574h	32	EMIF_CTLCFG_DENALI_PI_349	0F30 A574h
2578h	32	EMIF_CTLCFG_DENALI_PI_350	0F30 A578h
257Ch	32	EMIF_CTLCFG_DENALI_PI_351	0F30 A57Ch
2580h	32	EMIF_CTLCFG_DENALI_PI_352	0F30 A580h
2584h	32	EMIF_CTLCFG_DENALI_PI_353	0F30 A584h
2588h	32	EMIF_CTLCFG_DENALI_PI_354	0F30 A588h
258Ch	32	EMIF_CTLCFG_DENALI_PI_355	0F30 A58Ch
2590h	32	EMIF_CTLCFG_DENALI_PI_356	0F30 A590h
2594h	32	EMIF_CTLCFG_DENALI_PI_357	0F30 A594h
2598h	32	EMIF_CTLCFG_DENALI_PI_358	0F30 A598h
259Ch	32	EMIF_CTLCFG_DENALI_PI_359	0F30 A59Ch
25A0h	32	EMIF_CTLCFG_DENALI_PI_360	0F30 A5A0h
25A4h	32	EMIF_CTLCFG_DENALI_PI_361	0F30 A5A4h
25A8h	32	EMIF_CTLCFG_DENALI_PI_362	0F30 A5A8h
25ACh	32	EMIF_CTLCFG_DENALI_PI_363	0F30 A5ACh
25B0h	32	EMIF_CTLCFG_DENALI_PI_364	0F30 A5B0h
25B4h	32	EMIF_CTLCFG_DENALI_PI_365	0F30 A5B4h
25B8h	32	EMIF_CTLCFG_DENALI_PI_366	0F30 A5B8h
25BCh	32	EMIF_CTLCFG_DENALI_PI_367	0F30 A5BCh
25C0h	32	EMIF_CTLCFG_DENALI_PI_368	0F30 A5C0h
25C4h	32	EMIF_CTLCFG_DENALI_PI_369	0F30 A5C4h
25C8h	32	EMIF_CTLCFG_DENALI_PI_370	0F30 A5C8h
25CCh	32	EMIF_CTLCFG_DENALI_PI_371	0F30 A5CCh
25D0h	32	EMIF_CTLCFG_DENALI_PI_372	0F30 A5D0h
25D4h	32	EMIF_CTLCFG_DENALI_PI_373	0F30 A5D4h
25D8h	32	EMIF_CTLCFG_DENALI_PI_374	0F30 A5D8h
25DCh	32	EMIF_CTLCFG_DENALI_PI_375	0F30 A5DCh
25E0h	32	EMIF_CTLCFG_DENALI_PI_376	0F30 A5E0h
25E4h	32	EMIF_CTLCFG_DENALI_PI_377	0F30 A5E4h
25E8h	32	EMIF_CTLCFG_DENALI_PI_378	0F30 A5E8h
25ECh	32	EMIF_CTLCFG_DENALI_PI_379	0F30 A5ECh
25F0h	32	EMIF_CTLCFG_DENALI_PI_380	0F30 A5F0h
25F4h	32	EMIF_CTLCFG_DENALI_PI_381	0F30 A5F4h
25F8h	32	EMIF_CTLCFG_DENALI_PI_382	0F30 A5F8h
25FCh	32	EMIF_CTLCFG_DENALI_PI_383	0F30 A5FCh
2600h	32	EMIF_CTLCFG_DENALI_PI_384	0F30 A600h
2604h	32	EMIF_CTLCFG_DENALI_PI_385	0F30 A604h
2608h	32	EMIF_CTLCFG_DENALI_PI_386	0F30 A608h
260Ch	32	EMIF_CTLCFG_DENALI_PI_387	0F30 A60Ch
2610h	32	EMIF_CTLCFG_DENALI_PI_388	0F30 A610h
2614h	32	EMIF_CTLCFG_DENALI_PI_389	0F30 A614h
2618h	32	EMIF_CTLCFG_DENALI_PI_390	0F30 A618h
261Ch	32	EMIF_CTLCFG_DENALI_PI_391	0F30 A61Ch
2620h	32	EMIF_CTLCFG_DENALI_PI_392	0F30 A620h
2624h	32	EMIF_CTLCFG_DENALI_PI_393	0F30 A624h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
2628h	32	EMIF_CTLCFG_DENALI_PI_394	0F30 A628h
262Ch	32	EMIF_CTLCFG_DENALI_PI_395	0F30 A62Ch
2630h	32	EMIF_CTLCFG_DENALI_PI_396	0F30 A630h
2634h	32	EMIF_CTLCFG_DENALI_PI_397	0F30 A634h
2638h	32	EMIF_CTLCFG_DENALI_PI_398	0F30 A638h
263Ch	32	EMIF_CTLCFG_DENALI_PI_399	0F30 A63Ch
2640h	32	EMIF_CTLCFG_DENALI_PI_400	0F30 A640h
2644h	32	EMIF_CTLCFG_DENALI_PI_401	0F30 A644h
2648h	32	EMIF_CTLCFG_DENALI_PI_402	0F30 A648h
264Ch	32	EMIF_CTLCFG_DENALI_PI_403	0F30 A64Ch
2650h	32	EMIF_CTLCFG_DENALI_PI_404	0F30 A650h
2654h	32	EMIF_CTLCFG_DENALI_PI_405	0F30 A654h
2658h	32	EMIF_CTLCFG_DENALI_PI_406	0F30 A658h
265Ch	32	EMIF_CTLCFG_DENALI_PI_407	0F30 A65Ch
2660h	32	EMIF_CTLCFG_DENALI_PI_408	0F30 A660h
2664h	32	EMIF_CTLCFG_DENALI_PI_409	0F30 A664h
2668h	32	EMIF_CTLCFG_DENALI_PI_410	0F30 A668h
266Ch	32	EMIF_CTLCFG_DENALI_PI_411	0F30 A66Ch
2670h	32	EMIF_CTLCFG_DENALI_PI_412	0F30 A670h
2674h	32	EMIF_CTLCFG_DENALI_PI_413	0F30 A674h
2678h	32	EMIF_CTLCFG_DENALI_PI_414	0F30 A678h
267Ch	32	EMIF_CTLCFG_DENALI_PI_415	0F30 A67Ch
2680h	32	EMIF_CTLCFG_DENALI_PI_416	0F30 A680h
2684h	32	EMIF_CTLCFG_DENALI_PI_417	0F30 A684h
2688h	32	EMIF_CTLCFG_DENALI_PI_418	0F30 A688h
268Ch	32	EMIF_CTLCFG_DENALI_PI_419	0F30 A68Ch
2690h	32	EMIF_CTLCFG_DENALI_PI_420	0F30 A690h
2694h	32	EMIF_CTLCFG_DENALI_PI_421	0F30 A694h
2698h	32	EMIF_CTLCFG_DENALI_PI_422	0F30 A698h
269Ch	32	EMIF_CTLCFG_DENALI_PI_423	0F30 A69Ch
4000h	32	EMIF_CTLCFG_DENALI_PHY_0	0F30 C000h
4004h	32	EMIF_CTLCFG_DENALI_PHY_1	0F30 C004h
4008h	32	EMIF_CTLCFG_DENALI_PHY_2	0F30 C008h
400Ch	32	EMIF_CTLCFG_DENALI_PHY_3	0F30 C00Ch
4010h	32	EMIF_CTLCFG_DENALI_PHY_4	0F30 C010h
4014h	32	EMIF_CTLCFG_DENALI_PHY_5	0F30 C014h
4018h	32	EMIF_CTLCFG_DENALI_PHY_6	0F30 C018h
401Ch	32	EMIF_CTLCFG_DENALI_PHY_7	0F30 C01Ch
4020h	32	EMIF_CTLCFG_DENALI_PHY_8	0F30 C020h
4024h	32	EMIF_CTLCFG_DENALI_PHY_9	0F30 C024h
4028h	32	EMIF_CTLCFG_DENALI_PHY_10	0F30 C028h
402Ch	32	EMIF_CTLCFG_DENALI_PHY_11	0F30 C02Ch
4030h	32	EMIF_CTLCFG_DENALI_PHY_12	0F30 C030h
4034h	32	EMIF_CTLCFG_DENALI_PHY_13	0F30 C034h
4038h	32	EMIF_CTLCFG_DENALI_PHY_14	0F30 C038h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
403Ch	32	EMIF_CTLCFG_DENALI_PHY_15	0F30 C03Ch
4040h	32	EMIF_CTLCFG_DENALI_PHY_16	0F30 C040h
4044h	32	EMIF_CTLCFG_DENALI_PHY_17	0F30 C044h
4048h	32	EMIF_CTLCFG_DENALI_PHY_18	0F30 C048h
404Ch	32	EMIF_CTLCFG_DENALI_PHY_19	0F30 C04Ch
4050h	32	EMIF_CTLCFG_DENALI_PHY_20	0F30 C050h
4054h	32	EMIF_CTLCFG_DENALI_PHY_21	0F30 C054h
4058h	32	EMIF_CTLCFG_DENALI_PHY_22	0F30 C058h
405Ch	32	EMIF_CTLCFG_DENALI_PHY_23	0F30 C05Ch
4060h	32	EMIF_CTLCFG_DENALI_PHY_24	0F30 C060h
4064h	32	EMIF_CTLCFG_DENALI_PHY_25	0F30 C064h
4068h	32	EMIF_CTLCFG_DENALI_PHY_26	0F30 C068h
406Ch	32	EMIF_CTLCFG_DENALI_PHY_27	0F30 C06Ch
4070h	32	EMIF_CTLCFG_DENALI_PHY_28	0F30 C070h
4074h	32	EMIF_CTLCFG_DENALI_PHY_29	0F30 C074h
4078h	32	EMIF_CTLCFG_DENALI_PHY_30	0F30 C078h
407Ch	32	EMIF_CTLCFG_DENALI_PHY_31	0F30 C07Ch
4080h	32	EMIF_CTLCFG_DENALI_PHY_32	0F30 C080h
4084h	32	EMIF_CTLCFG_DENALI_PHY_33	0F30 C084h
4088h	32	EMIF_CTLCFG_DENALI_PHY_34	0F30 C088h
408Ch	32	EMIF_CTLCFG_DENALI_PHY_35	0F30 C08Ch
4090h	32	EMIF_CTLCFG_DENALI_PHY_36	0F30 C090h
4094h	32	EMIF_CTLCFG_DENALI_PHY_37	0F30 C094h
4098h	32	EMIF_CTLCFG_DENALI_PHY_38	0F30 C098h
409Ch	32	EMIF_CTLCFG_DENALI_PHY_39	0F30 C09Ch
40A0h	32	EMIF_CTLCFG_DENALI_PHY_40	0F30 C0A0h
40A4h	32	EMIF_CTLCFG_DENALI_PHY_41	0F30 C0A4h
40A8h	32	EMIF_CTLCFG_DENALI_PHY_42	0F30 C0A8h
40ACh	32	EMIF_CTLCFG_DENALI_PHY_43	0F30 C0ACh
40B0h	32	EMIF_CTLCFG_DENALI_PHY_44	0F30 C0B0h
40B4h	32	EMIF_CTLCFG_DENALI_PHY_45	0F30 C0B4h
40B8h	32	EMIF_CTLCFG_DENALI_PHY_46	0F30 C0B8h
40BCh	32	EMIF_CTLCFG_DENALI_PHY_47	0F30 C0BCh
40C0h	32	EMIF_CTLCFG_DENALI_PHY_48	0F30 C0C0h
40C4h	32	EMIF_CTLCFG_DENALI_PHY_49	0F30 C0C4h
40C8h	32	EMIF_CTLCFG_DENALI_PHY_50	0F30 C0C8h
40CCh	32	EMIF_CTLCFG_DENALI_PHY_51	0F30 C0CCh
40D0h	32	EMIF_CTLCFG_DENALI_PHY_52	0F30 C0D0h
40D4h	32	EMIF_CTLCFG_DENALI_PHY_53	0F30 C0D4h
40D8h	32	EMIF_CTLCFG_DENALI_PHY_54	0F30 C0D8h
40DCh	32	EMIF_CTLCFG_DENALI_PHY_55	0F30 C0DCh
40E0h	32	EMIF_CTLCFG_DENALI_PHY_56	0F30 C0E0h
40E4h	32	EMIF_CTLCFG_DENALI_PHY_57	0F30 C0E4h
40E8h	32	EMIF_CTLCFG_DENALI_PHY_58	0F30 C0E8h
40ECh	32	EMIF_CTLCFG_DENALI_PHY_59	0F30 C0ECh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
40F0h	32	EMIF_CTLCFG_DENALI_PHY_60	0F30 C0F0h
40F4h	32	EMIF_CTLCFG_DENALI_PHY_61	0F30 C0F4h
40F8h	32	EMIF_CTLCFG_DENALI_PHY_62	0F30 C0F8h
40FCh	32	EMIF_CTLCFG_DENALI_PHY_63	0F30 C0FCh
4100h	32	EMIF_CTLCFG_DENALI_PHY_64	0F30 C100h
4104h	32	EMIF_CTLCFG_DENALI_PHY_65	0F30 C104h
4108h	32	EMIF_CTLCFG_DENALI_PHY_66	0F30 C108h
410Ch	32	EMIF_CTLCFG_DENALI_PHY_67	0F30 C10Ch
4110h	32	EMIF_CTLCFG_DENALI_PHY_68	0F30 C110h
4114h	32	EMIF_CTLCFG_DENALI_PHY_69	0F30 C114h
4118h	32	EMIF_CTLCFG_DENALI_PHY_70	0F30 C118h
411Ch	32	EMIF_CTLCFG_DENALI_PHY_71	0F30 C11Ch
4120h	32	EMIF_CTLCFG_DENALI_PHY_72	0F30 C120h
4124h	32	EMIF_CTLCFG_DENALI_PHY_73	0F30 C124h
4128h	32	EMIF_CTLCFG_DENALI_PHY_74	0F30 C128h
412Ch	32	EMIF_CTLCFG_DENALI_PHY_75	0F30 C12Ch
4130h	32	EMIF_CTLCFG_DENALI_PHY_76	0F30 C130h
4134h	32	EMIF_CTLCFG_DENALI_PHY_77	0F30 C134h
4138h	32	EMIF_CTLCFG_DENALI_PHY_78	0F30 C138h
413Ch	32	EMIF_CTLCFG_DENALI_PHY_79	0F30 C13Ch
4140h	32	EMIF_CTLCFG_DENALI_PHY_80	0F30 C140h
4144h	32	EMIF_CTLCFG_DENALI_PHY_81	0F30 C144h
4148h	32	EMIF_CTLCFG_DENALI_PHY_82	0F30 C148h
414Ch	32	EMIF_CTLCFG_DENALI_PHY_83	0F30 C14Ch
4150h	32	EMIF_CTLCFG_DENALI_PHY_84	0F30 C150h
4154h	32	EMIF_CTLCFG_DENALI_PHY_85	0F30 C154h
4158h	32	EMIF_CTLCFG_DENALI_PHY_86	0F30 C158h
415Ch	32	EMIF_CTLCFG_DENALI_PHY_87	0F30 C15Ch
4160h	32	EMIF_CTLCFG_DENALI_PHY_88	0F30 C160h
4164h	32	EMIF_CTLCFG_DENALI_PHY_89	0F30 C164h
4168h	32	EMIF_CTLCFG_DENALI_PHY_90	0F30 C168h
416Ch	32	EMIF_CTLCFG_DENALI_PHY_91	0F30 C16Ch
4170h	32	EMIF_CTLCFG_DENALI_PHY_92	0F30 C170h
4174h	32	EMIF_CTLCFG_DENALI_PHY_93	0F30 C174h
4178h	32	EMIF_CTLCFG_DENALI_PHY_94	0F30 C178h
417Ch	32	EMIF_CTLCFG_DENALI_PHY_95	0F30 C17Ch
4180h	32	EMIF_CTLCFG_DENALI_PHY_96	0F30 C180h
4184h	32	EMIF_CTLCFG_DENALI_PHY_97	0F30 C184h
4188h	32	EMIF_CTLCFG_DENALI_PHY_98	0F30 C188h
418Ch	32	EMIF_CTLCFG_DENALI_PHY_99	0F30 C18Ch
4190h	32	EMIF_CTLCFG_DENALI_PHY_100	0F30 C190h
4194h	32	EMIF_CTLCFG_DENALI_PHY_101	0F30 C194h
4198h	32	EMIF_CTLCFG_DENALI_PHY_102	0F30 C198h
419Ch	32	EMIF_CTLCFG_DENALI_PHY_103	0F30 C19Ch
41A0h	32	EMIF_CTLCFG_DENALI_PHY_104	0F30 C1A0h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
41A4h	32	EMIF_CTLCFG_DENALI_PHY_105	0F30 C1A4h
41A8h	32	EMIF_CTLCFG_DENALI_PHY_106	0F30 C1A8h
41ACh	32	EMIF_CTLCFG_DENALI_PHY_107	0F30 C1ACh
41B0h	32	EMIF_CTLCFG_DENALI_PHY_108	0F30 C1B0h
41B4h	32	EMIF_CTLCFG_DENALI_PHY_109	0F30 C1B4h
41B8h	32	EMIF_CTLCFG_DENALI_PHY_110	0F30 C1B8h
41BCh	32	EMIF_CTLCFG_DENALI_PHY_111	0F30 C1BCh
41C0h	32	EMIF_CTLCFG_DENALI_PHY_112	0F30 C1C0h
41C4h	32	EMIF_CTLCFG_DENALI_PHY_113	0F30 C1C4h
41C8h	32	EMIF_CTLCFG_DENALI_PHY_114	0F30 C1C8h
41CCh	32	EMIF_CTLCFG_DENALI_PHY_115	0F30 C1CCh
41D0h	32	EMIF_CTLCFG_DENALI_PHY_116	0F30 C1D0h
41D4h	32	EMIF_CTLCFG_DENALI_PHY_117	0F30 C1D4h
41D8h	32	EMIF_CTLCFG_DENALI_PHY_118	0F30 C1D8h
41DCh	32	EMIF_CTLCFG_DENALI_PHY_119	0F30 C1DCh
41E0h	32	EMIF_CTLCFG_DENALI_PHY_120	0F30 C1E0h
41E4h	32	EMIF_CTLCFG_DENALI_PHY_121	0F30 C1E4h
41E8h	32	EMIF_CTLCFG_DENALI_PHY_122	0F30 C1E8h
41ECh	32	EMIF_CTLCFG_DENALI_PHY_123	0F30 C1ECh
41F0h	32	EMIF_CTLCFG_DENALI_PHY_124	0F30 C1F0h
41F4h	32	EMIF_CTLCFG_DENALI_PHY_125	0F30 C1F4h
41F8h	32	EMIF_CTLCFG_DENALI_PHY_126	0F30 C1F8h
41FCh	32	EMIF_CTLCFG_DENALI_PHY_127	0F30 C1FCh
4200h	32	EMIF_CTLCFG_DENALI_PHY_128	0F30 C200h
4204h	32	EMIF_CTLCFG_DENALI_PHY_129	0F30 C204h
4208h	32	EMIF_CTLCFG_DENALI_PHY_130	0F30 C208h
420Ch	32	EMIF_CTLCFG_DENALI_PHY_131	0F30 C20Ch
4210h	32	EMIF_CTLCFG_DENALI_PHY_132	0F30 C210h
4214h	32	EMIF_CTLCFG_DENALI_PHY_133	0F30 C214h
4218h	32	EMIF_CTLCFG_DENALI_PHY_134	0F30 C218h
421Ch	32	EMIF_CTLCFG_DENALI_PHY_135	0F30 C21Ch
4220h	32	EMIF_CTLCFG_DENALI_PHY_136	0F30 C220h
4400h	32	EMIF_CTLCFG_DENALI_PHY_256	0F30 C400h
4404h	32	EMIF_CTLCFG_DENALI_PHY_257	0F30 C404h
4408h	32	EMIF_CTLCFG_DENALI_PHY_258	0F30 C408h
440Ch	32	EMIF_CTLCFG_DENALI_PHY_259	0F30 C40Ch
4410h	32	EMIF_CTLCFG_DENALI_PHY_260	0F30 C410h
4414h	32	EMIF_CTLCFG_DENALI_PHY_261	0F30 C414h
4418h	32	EMIF_CTLCFG_DENALI_PHY_262	0F30 C418h
441Ch	32	EMIF_CTLCFG_DENALI_PHY_263	0F30 C41Ch
4420h	32	EMIF_CTLCFG_DENALI_PHY_264	0F30 C420h
4424h	32	EMIF_CTLCFG_DENALI_PHY_265	0F30 C424h
4428h	32	EMIF_CTLCFG_DENALI_PHY_266	0F30 C428h
442Ch	32	EMIF_CTLCFG_DENALI_PHY_267	0F30 C42Ch
4430h	32	EMIF_CTLCFG_DENALI_PHY_268	0F30 C430h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4434h	32	EMIF_CTLCFG_DENALI_PHY_269	0F30 C434h
4438h	32	EMIF_CTLCFG_DENALI_PHY_270	0F30 C438h
443Ch	32	EMIF_CTLCFG_DENALI_PHY_271	0F30 C43Ch
4440h	32	EMIF_CTLCFG_DENALI_PHY_272	0F30 C440h
4444h	32	EMIF_CTLCFG_DENALI_PHY_273	0F30 C444h
4448h	32	EMIF_CTLCFG_DENALI_PHY_274	0F30 C448h
444Ch	32	EMIF_CTLCFG_DENALI_PHY_275	0F30 C44Ch
4450h	32	EMIF_CTLCFG_DENALI_PHY_276	0F30 C450h
4454h	32	EMIF_CTLCFG_DENALI_PHY_277	0F30 C454h
4458h	32	EMIF_CTLCFG_DENALI_PHY_278	0F30 C458h
445Ch	32	EMIF_CTLCFG_DENALI_PHY_279	0F30 C45Ch
4460h	32	EMIF_CTLCFG_DENALI_PHY_280	0F30 C460h
4464h	32	EMIF_CTLCFG_DENALI_PHY_281	0F30 C464h
4468h	32	EMIF_CTLCFG_DENALI_PHY_282	0F30 C468h
446Ch	32	EMIF_CTLCFG_DENALI_PHY_283	0F30 C46Ch
4470h	32	EMIF_CTLCFG_DENALI_PHY_284	0F30 C470h
4474h	32	EMIF_CTLCFG_DENALI_PHY_285	0F30 C474h
4478h	32	EMIF_CTLCFG_DENALI_PHY_286	0F30 C478h
447Ch	32	EMIF_CTLCFG_DENALI_PHY_287	0F30 C47Ch
4480h	32	EMIF_CTLCFG_DENALI_PHY_288	0F30 C480h
4484h	32	EMIF_CTLCFG_DENALI_PHY_289	0F30 C484h
4488h	32	EMIF_CTLCFG_DENALI_PHY_290	0F30 C488h
448Ch	32	EMIF_CTLCFG_DENALI_PHY_291	0F30 C48Ch
4490h	32	EMIF_CTLCFG_DENALI_PHY_292	0F30 C490h
4494h	32	EMIF_CTLCFG_DENALI_PHY_293	0F30 C494h
4498h	32	EMIF_CTLCFG_DENALI_PHY_294	0F30 C498h
449Ch	32	EMIF_CTLCFG_DENALI_PHY_295	0F30 C49Ch
44A0h	32	EMIF_CTLCFG_DENALI_PHY_296	0F30 C4A0h
44A4h	32	EMIF_CTLCFG_DENALI_PHY_297	0F30 C4A4h
44A8h	32	EMIF_CTLCFG_DENALI_PHY_298	0F30 C4A8h
44ACh	32	EMIF_CTLCFG_DENALI_PHY_299	0F30 C4ACh
44B0h	32	EMIF_CTLCFG_DENALI_PHY_300	0F30 C4B0h
44B4h	32	EMIF_CTLCFG_DENALI_PHY_301	0F30 C4B4h
44B8h	32	EMIF_CTLCFG_DENALI_PHY_302	0F30 C4B8h
44BCh	32	EMIF_CTLCFG_DENALI_PHY_303	0F30 C4BCh
44C0h	32	EMIF_CTLCFG_DENALI_PHY_304	0F30 C4C0h
44C4h	32	EMIF_CTLCFG_DENALI_PHY_305	0F30 C4C4h
44C8h	32	EMIF_CTLCFG_DENALI_PHY_306	0F30 C4C8h
44CCh	32	EMIF_CTLCFG_DENALI_PHY_307	0F30 C4CCh
44D0h	32	EMIF_CTLCFG_DENALI_PHY_308	0F30 C4D0h
44D4h	32	EMIF_CTLCFG_DENALI_PHY_309	0F30 C4D4h
44D8h	32	EMIF_CTLCFG_DENALI_PHY_310	0F30 C4D8h
44DCh	32	EMIF_CTLCFG_DENALI_PHY_311	0F30 C4DCh
44E0h	32	EMIF_CTLCFG_DENALI_PHY_312	0F30 C4E0h
44E4h	32	EMIF_CTLCFG_DENALI_PHY_313	0F30 C4E4h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
44E8h	32	EMIF_CTLCFG_DENALI_PHY_314	0F30 C4E8h
44ECh	32	EMIF_CTLCFG_DENALI_PHY_315	0F30 C4ECh
44F0h	32	EMIF_CTLCFG_DENALI_PHY_316	0F30 C4F0h
44F4h	32	EMIF_CTLCFG_DENALI_PHY_317	0F30 C4F4h
44F8h	32	EMIF_CTLCFG_DENALI_PHY_318	0F30 C4F8h
44FCh	32	EMIF_CTLCFG_DENALI_PHY_319	0F30 C4FCh
4500h	32	EMIF_CTLCFG_DENALI_PHY_320	0F30 C500h
4504h	32	EMIF_CTLCFG_DENALI_PHY_321	0F30 C504h
4508h	32	EMIF_CTLCFG_DENALI_PHY_322	0F30 C508h
450Ch	32	EMIF_CTLCFG_DENALI_PHY_323	0F30 C50Ch
4510h	32	EMIF_CTLCFG_DENALI_PHY_324	0F30 C510h
4514h	32	EMIF_CTLCFG_DENALI_PHY_325	0F30 C514h
4518h	32	EMIF_CTLCFG_DENALI_PHY_326	0F30 C518h
451Ch	32	EMIF_CTLCFG_DENALI_PHY_327	0F30 C51Ch
4520h	32	EMIF_CTLCFG_DENALI_PHY_328	0F30 C520h
4524h	32	EMIF_CTLCFG_DENALI_PHY_329	0F30 C524h
4528h	32	EMIF_CTLCFG_DENALI_PHY_330	0F30 C528h
452Ch	32	EMIF_CTLCFG_DENALI_PHY_331	0F30 C52Ch
4530h	32	EMIF_CTLCFG_DENALI_PHY_332	0F30 C530h
4534h	32	EMIF_CTLCFG_DENALI_PHY_333	0F30 C534h
4538h	32	EMIF_CTLCFG_DENALI_PHY_334	0F30 C538h
453Ch	32	EMIF_CTLCFG_DENALI_PHY_335	0F30 C53Ch
4540h	32	EMIF_CTLCFG_DENALI_PHY_336	0F30 C540h
4544h	32	EMIF_CTLCFG_DENALI_PHY_337	0F30 C544h
4548h	32	EMIF_CTLCFG_DENALI_PHY_338	0F30 C548h
454Ch	32	EMIF_CTLCFG_DENALI_PHY_339	0F30 C54Ch
4550h	32	EMIF_CTLCFG_DENALI_PHY_340	0F30 C550h
4554h	32	EMIF_CTLCFG_DENALI_PHY_341	0F30 C554h
4558h	32	EMIF_CTLCFG_DENALI_PHY_342	0F30 C558h
455Ch	32	EMIF_CTLCFG_DENALI_PHY_343	0F30 C55Ch
4560h	32	EMIF_CTLCFG_DENALI_PHY_344	0F30 C560h
4564h	32	EMIF_CTLCFG_DENALI_PHY_345	0F30 C564h
4568h	32	EMIF_CTLCFG_DENALI_PHY_346	0F30 C568h
456Ch	32	EMIF_CTLCFG_DENALI_PHY_347	0F30 C56Ch
4570h	32	EMIF_CTLCFG_DENALI_PHY_348	0F30 C570h
4574h	32	EMIF_CTLCFG_DENALI_PHY_349	0F30 C574h
4578h	32	EMIF_CTLCFG_DENALI_PHY_350	0F30 C578h
457Ch	32	EMIF_CTLCFG_DENALI_PHY_351	0F30 C57Ch
4580h	32	EMIF_CTLCFG_DENALI_PHY_352	0F30 C580h
4584h	32	EMIF_CTLCFG_DENALI_PHY_353	0F30 C584h
4588h	32	EMIF_CTLCFG_DENALI_PHY_354	0F30 C588h
458Ch	32	EMIF_CTLCFG_DENALI_PHY_355	0F30 C58Ch
4590h	32	EMIF_CTLCFG_DENALI_PHY_356	0F30 C590h
4594h	32	EMIF_CTLCFG_DENALI_PHY_357	0F30 C594h
4598h	32	EMIF_CTLCFG_DENALI_PHY_358	0F30 C598h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
459Ch	32	EMIF_CTLCFG_DENALI_PHY_359	0F30 C59Ch
45A0h	32	EMIF_CTLCFG_DENALI_PHY_360	0F30 C5A0h
45A4h	32	EMIF_CTLCFG_DENALI_PHY_361	0F30 C5A4h
45A8h	32	EMIF_CTLCFG_DENALI_PHY_362	0F30 C5A8h
45ACh	32	EMIF_CTLCFG_DENALI_PHY_363	0F30 C5ACh
45B0h	32	EMIF_CTLCFG_DENALI_PHY_364	0F30 C5B0h
45B4h	32	EMIF_CTLCFG_DENALI_PHY_365	0F30 C5B4h
45B8h	32	EMIF_CTLCFG_DENALI_PHY_366	0F30 C5B8h
45BCh	32	EMIF_CTLCFG_DENALI_PHY_367	0F30 C5BCh
45C0h	32	EMIF_CTLCFG_DENALI_PHY_368	0F30 C5C0h
45C4h	32	EMIF_CTLCFG_DENALI_PHY_369	0F30 C5C4h
45C8h	32	EMIF_CTLCFG_DENALI_PHY_370	0F30 C5C8h
45CCh	32	EMIF_CTLCFG_DENALI_PHY_371	0F30 C5CCh
45D0h	32	EMIF_CTLCFG_DENALI_PHY_372	0F30 C5D0h
45D4h	32	EMIF_CTLCFG_DENALI_PHY_373	0F30 C5D4h
45D8h	32	EMIF_CTLCFG_DENALI_PHY_374	0F30 C5D8h
45DCh	32	EMIF_CTLCFG_DENALI_PHY_375	0F30 C5DCh
45E0h	32	EMIF_CTLCFG_DENALI_PHY_376	0F30 C5E0h
45E4h	32	EMIF_CTLCFG_DENALI_PHY_377	0F30 C5E4h
45E8h	32	EMIF_CTLCFG_DENALI_PHY_378	0F30 C5E8h
45ECh	32	EMIF_CTLCFG_DENALI_PHY_379	0F30 C5ECh
45F0h	32	EMIF_CTLCFG_DENALI_PHY_380	0F30 C5F0h
45F4h	32	EMIF_CTLCFG_DENALI_PHY_381	0F30 C5F4h
45F8h	32	EMIF_CTLCFG_DENALI_PHY_382	0F30 C5F8h
45FCh	32	EMIF_CTLCFG_DENALI_PHY_383	0F30 C5FCh
4600h	32	EMIF_CTLCFG_DENALI_PHY_384	0F30 C600h
4604h	32	EMIF_CTLCFG_DENALI_PHY_385	0F30 C604h
4608h	32	EMIF_CTLCFG_DENALI_PHY_386	0F30 C608h
460Ch	32	EMIF_CTLCFG_DENALI_PHY_387	0F30 C60Ch
4610h	32	EMIF_CTLCFG_DENALI_PHY_388	0F30 C610h
4614h	32	EMIF_CTLCFG_DENALI_PHY_389	0F30 C614h
4618h	32	EMIF_CTLCFG_DENALI_PHY_390	0F30 C618h
461Ch	32	EMIF_CTLCFG_DENALI_PHY_391	0F30 C61Ch
4620h	32	EMIF_CTLCFG_DENALI_PHY_392	0F30 C620h
4800h	32	EMIF_CTLCFG_DENALI_PHY_512	0F30 C800h
4804h	32	EMIF_CTLCFG_DENALI_PHY_513	0F30 C804h
4808h	32	EMIF_CTLCFG_DENALI_PHY_514	0F30 C808h
480Ch	32	EMIF_CTLCFG_DENALI_PHY_515	0F30 C80Ch
4810h	32	EMIF_CTLCFG_DENALI_PHY_516	0F30 C810h
4814h	32	EMIF_CTLCFG_DENALI_PHY_517	0F30 C814h
4818h	32	EMIF_CTLCFG_DENALI_PHY_518	0F30 C818h
481Ch	32	EMIF_CTLCFG_DENALI_PHY_519	0F30 C81Ch
4820h	32	EMIF_CTLCFG_DENALI_PHY_520	0F30 C820h
4824h	32	EMIF_CTLCFG_DENALI_PHY_521	0F30 C824h
4828h	32	EMIF_CTLCFG_DENALI_PHY_522	0F30 C828h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
482Ch	32	EMIF_CTLCFG_DENALI_PHY_523	0F30 C82Ch
4830h	32	EMIF_CTLCFG_DENALI_PHY_524	0F30 C830h
4834h	32	EMIF_CTLCFG_DENALI_PHY_525	0F30 C834h
4838h	32	EMIF_CTLCFG_DENALI_PHY_526	0F30 C838h
483Ch	32	EMIF_CTLCFG_DENALI_PHY_527	0F30 C83Ch
4840h	32	EMIF_CTLCFG_DENALI_PHY_528	0F30 C840h
4844h	32	EMIF_CTLCFG_DENALI_PHY_529	0F30 C844h
4848h	32	EMIF_CTLCFG_DENALI_PHY_530	0F30 C848h
484Ch	32	EMIF_CTLCFG_DENALI_PHY_531	0F30 C84Ch
4850h	32	EMIF_CTLCFG_DENALI_PHY_532	0F30 C850h
4854h	32	EMIF_CTLCFG_DENALI_PHY_533	0F30 C854h
4858h	32	EMIF_CTLCFG_DENALI_PHY_534	0F30 C858h
485Ch	32	EMIF_CTLCFG_DENALI_PHY_535	0F30 C85Ch
4860h	32	EMIF_CTLCFG_DENALI_PHY_536	0F30 C860h
4864h	32	EMIF_CTLCFG_DENALI_PHY_537	0F30 C864h
4868h	32	EMIF_CTLCFG_DENALI_PHY_538	0F30 C868h
486Ch	32	EMIF_CTLCFG_DENALI_PHY_539	0F30 C86Ch
4870h	32	EMIF_CTLCFG_DENALI_PHY_540	0F30 C870h
4874h	32	EMIF_CTLCFG_DENALI_PHY_541	0F30 C874h
4878h	32	EMIF_CTLCFG_DENALI_PHY_542	0F30 C878h
487Ch	32	EMIF_CTLCFG_DENALI_PHY_543	0F30 C87Ch
4880h	32	EMIF_CTLCFG_DENALI_PHY_544	0F30 C880h
4884h	32	EMIF_CTLCFG_DENALI_PHY_545	0F30 C884h
4888h	32	EMIF_CTLCFG_DENALI_PHY_546	0F30 C888h
488Ch	32	EMIF_CTLCFG_DENALI_PHY_547	0F30 C88Ch
4890h	32	EMIF_CTLCFG_DENALI_PHY_548	0F30 C890h
4894h	32	EMIF_CTLCFG_DENALI_PHY_549	0F30 C894h
4898h	32	EMIF_CTLCFG_DENALI_PHY_550	0F30 C898h
489Ch	32	EMIF_CTLCFG_DENALI_PHY_551	0F30 C89Ch
48A0h	32	EMIF_CTLCFG_DENALI_PHY_552	0F30 C8A0h
48A4h	32	EMIF_CTLCFG_DENALI_PHY_553	0F30 C8A4h
48A8h	32	EMIF_CTLCFG_DENALI_PHY_554	0F30 C8A8h
48ACh	32	EMIF_CTLCFG_DENALI_PHY_555	0F30 C8ACh
48B0h	32	EMIF_CTLCFG_DENALI_PHY_556	0F30 C8B0h
48B4h	32	EMIF_CTLCFG_DENALI_PHY_557	0F30 C8B4h
48B8h	32	EMIF_CTLCFG_DENALI_PHY_558	0F30 C8B8h
48BCh	32	EMIF_CTLCFG_DENALI_PHY_559	0F30 C8BCh
48C0h	32	EMIF_CTLCFG_DENALI_PHY_560	0F30 C8C0h
48C4h	32	EMIF_CTLCFG_DENALI_PHY_561	0F30 C8C4h
48C8h	32	EMIF_CTLCFG_DENALI_PHY_562	0F30 C8C8h
48CCh	32	EMIF_CTLCFG_DENALI_PHY_563	0F30 C8CCh
48D0h	32	EMIF_CTLCFG_DENALI_PHY_564	0F30 C8D0h
48D4h	32	EMIF_CTLCFG_DENALI_PHY_565	0F30 C8D4h
48D8h	32	EMIF_CTLCFG_DENALI_PHY_566	0F30 C8D8h
48DCh	32	EMIF_CTLCFG_DENALI_PHY_567	0F30 C8DCh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
48E0h	32	EMIF_CTLCFG_DENALI_PHY_568	0F30 C8E0h
48E4h	32	EMIF_CTLCFG_DENALI_PHY_569	0F30 C8E4h
48E8h	32	EMIF_CTLCFG_DENALI_PHY_570	0F30 C8E8h
48ECh	32	EMIF_CTLCFG_DENALI_PHY_571	0F30 C8ECh
48F0h	32	EMIF_CTLCFG_DENALI_PHY_572	0F30 C8F0h
48F4h	32	EMIF_CTLCFG_DENALI_PHY_573	0F30 C8F4h
48F8h	32	EMIF_CTLCFG_DENALI_PHY_574	0F30 C8F8h
48FCh	32	EMIF_CTLCFG_DENALI_PHY_575	0F30 C8FCh
4900h	32	EMIF_CTLCFG_DENALI_PHY_576	0F30 C900h
4904h	32	EMIF_CTLCFG_DENALI_PHY_577	0F30 C904h
4908h	32	EMIF_CTLCFG_DENALI_PHY_578	0F30 C908h
490Ch	32	EMIF_CTLCFG_DENALI_PHY_579	0F30 C90Ch
4910h	32	EMIF_CTLCFG_DENALI_PHY_580	0F30 C910h
4914h	32	EMIF_CTLCFG_DENALI_PHY_581	0F30 C914h
4918h	32	EMIF_CTLCFG_DENALI_PHY_582	0F30 C918h
491Ch	32	EMIF_CTLCFG_DENALI_PHY_583	0F30 C91Ch
4920h	32	EMIF_CTLCFG_DENALI_PHY_584	0F30 C920h
4924h	32	EMIF_CTLCFG_DENALI_PHY_585	0F30 C924h
4928h	32	EMIF_CTLCFG_DENALI_PHY_586	0F30 C928h
492Ch	32	EMIF_CTLCFG_DENALI_PHY_587	0F30 C92Ch
4930h	32	EMIF_CTLCFG_DENALI_PHY_588	0F30 C930h
4934h	32	EMIF_CTLCFG_DENALI_PHY_589	0F30 C934h
4938h	32	EMIF_CTLCFG_DENALI_PHY_590	0F30 C938h
493Ch	32	EMIF_CTLCFG_DENALI_PHY_591	0F30 C93Ch
4940h	32	EMIF_CTLCFG_DENALI_PHY_592	0F30 C940h
4944h	32	EMIF_CTLCFG_DENALI_PHY_593	0F30 C944h
4948h	32	EMIF_CTLCFG_DENALI_PHY_594	0F30 C948h
494Ch	32	EMIF_CTLCFG_DENALI_PHY_595	0F30 C94Ch
4950h	32	EMIF_CTLCFG_DENALI_PHY_596	0F30 C950h
4954h	32	EMIF_CTLCFG_DENALI_PHY_597	0F30 C954h
4958h	32	EMIF_CTLCFG_DENALI_PHY_598	0F30 C958h
495Ch	32	EMIF_CTLCFG_DENALI_PHY_599	0F30 C95Ch
4960h	32	EMIF_CTLCFG_DENALI_PHY_600	0F30 C960h
4964h	32	EMIF_CTLCFG_DENALI_PHY_601	0F30 C964h
4968h	32	EMIF_CTLCFG_DENALI_PHY_602	0F30 C968h
496Ch	32	EMIF_CTLCFG_DENALI_PHY_603	0F30 C96Ch
4970h	32	EMIF_CTLCFG_DENALI_PHY_604	0F30 C970h
4974h	32	EMIF_CTLCFG_DENALI_PHY_605	0F30 C974h
4978h	32	EMIF_CTLCFG_DENALI_PHY_606	0F30 C978h
497Ch	32	EMIF_CTLCFG_DENALI_PHY_607	0F30 C97Ch
4980h	32	EMIF_CTLCFG_DENALI_PHY_608	0F30 C980h
4984h	32	EMIF_CTLCFG_DENALI_PHY_609	0F30 C984h
4988h	32	EMIF_CTLCFG_DENALI_PHY_610	0F30 C988h
498Ch	32	EMIF_CTLCFG_DENALI_PHY_611	0F30 C98Ch
4990h	32	EMIF_CTLCFG_DENALI_PHY_612	0F30 C990h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4994h	32	EMIF_CTLCFG_DENALI_PHY_613	0F30 C994h
4998h	32	EMIF_CTLCFG_DENALI_PHY_614	0F30 C998h
499Ch	32	EMIF_CTLCFG_DENALI_PHY_615	0F30 C99Ch
49A0h	32	EMIF_CTLCFG_DENALI_PHY_616	0F30 C9A0h
49A4h	32	EMIF_CTLCFG_DENALI_PHY_617	0F30 C9A4h
49A8h	32	EMIF_CTLCFG_DENALI_PHY_618	0F30 C9A8h
49ACh	32	EMIF_CTLCFG_DENALI_PHY_619	0F30 C9ACh
49B0h	32	EMIF_CTLCFG_DENALI_PHY_620	0F30 C9B0h
49B4h	32	EMIF_CTLCFG_DENALI_PHY_621	0F30 C9B4h
49B8h	32	EMIF_CTLCFG_DENALI_PHY_622	0F30 C9B8h
49BCh	32	EMIF_CTLCFG_DENALI_PHY_623	0F30 C9BCh
49C0h	32	EMIF_CTLCFG_DENALI_PHY_624	0F30 C9C0h
49C4h	32	EMIF_CTLCFG_DENALI_PHY_625	0F30 C9C4h
49C8h	32	EMIF_CTLCFG_DENALI_PHY_626	0F30 C9C8h
49CCh	32	EMIF_CTLCFG_DENALI_PHY_627	0F30 C9CCh
49D0h	32	EMIF_CTLCFG_DENALI_PHY_628	0F30 C9D0h
49D4h	32	EMIF_CTLCFG_DENALI_PHY_629	0F30 C9D4h
49D8h	32	EMIF_CTLCFG_DENALI_PHY_630	0F30 C9D8h
49DCh	32	EMIF_CTLCFG_DENALI_PHY_631	0F30 C9DCh
49E0h	32	EMIF_CTLCFG_DENALI_PHY_632	0F30 C9E0h
49E4h	32	EMIF_CTLCFG_DENALI_PHY_633	0F30 C9E4h
49E8h	32	EMIF_CTLCFG_DENALI_PHY_634	0F30 C9E8h
49ECh	32	EMIF_CTLCFG_DENALI_PHY_635	0F30 C9ECh
49F0h	32	EMIF_CTLCFG_DENALI_PHY_636	0F30 C9F0h
49F4h	32	EMIF_CTLCFG_DENALI_PHY_637	0F30 C9F4h
49F8h	32	EMIF_CTLCFG_DENALI_PHY_638	0F30 C9F8h
49FCh	32	EMIF_CTLCFG_DENALI_PHY_639	0F30 C9FCh
4A00h	32	EMIF_CTLCFG_DENALI_PHY_640	0F30 CA00h
4A04h	32	EMIF_CTLCFG_DENALI_PHY_641	0F30 CA04h
4A08h	32	EMIF_CTLCFG_DENALI_PHY_642	0F30 CA08h
4A0Ch	32	EMIF_CTLCFG_DENALI_PHY_643	0F30 CA0Ch
4A10h	32	EMIF_CTLCFG_DENALI_PHY_644	0F30 CA10h
4A14h	32	EMIF_CTLCFG_DENALI_PHY_645	0F30 CA14h
4A18h	32	EMIF_CTLCFG_DENALI_PHY_646	0F30 CA18h
4A1Ch	32	EMIF_CTLCFG_DENALI_PHY_647	0F30 CA1Ch
4A20h	32	EMIF_CTLCFG_DENALI_PHY_648	0F30 CA20h
4C00h	32	EMIF_CTLCFG_DENALI_PHY_768	0F30 CC00h
4C04h	32	EMIF_CTLCFG_DENALI_PHY_769	0F30 CC04h
4C08h	32	EMIF_CTLCFG_DENALI_PHY_770	0F30 CC08h
4C0Ch	32	EMIF_CTLCFG_DENALI_PHY_771	0F30 CC0Ch
4C10h	32	EMIF_CTLCFG_DENALI_PHY_772	0F30 CC10h
4C14h	32	EMIF_CTLCFG_DENALI_PHY_773	0F30 CC14h
4C18h	32	EMIF_CTLCFG_DENALI_PHY_774	0F30 CC18h
4C1Ch	32	EMIF_CTLCFG_DENALI_PHY_775	0F30 CC1Ch
4C20h	32	EMIF_CTLCFG_DENALI_PHY_776	0F30 CC20h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4C24h	32	EMIF_CTLCFG_DENALI_PHY_777	0F30 CC24h
4C28h	32	EMIF_CTLCFG_DENALI_PHY_778	0F30 CC28h
4C2Ch	32	EMIF_CTLCFG_DENALI_PHY_779	0F30 CC2Ch
4C30h	32	EMIF_CTLCFG_DENALI_PHY_780	0F30 CC30h
4C34h	32	EMIF_CTLCFG_DENALI_PHY_781	0F30 CC34h
4C38h	32	EMIF_CTLCFG_DENALI_PHY_782	0F30 CC38h
4C3Ch	32	EMIF_CTLCFG_DENALI_PHY_783	0F30 CC3Ch
4C40h	32	EMIF_CTLCFG_DENALI_PHY_784	0F30 CC40h
4C44h	32	EMIF_CTLCFG_DENALI_PHY_785	0F30 CC44h
4C48h	32	EMIF_CTLCFG_DENALI_PHY_786	0F30 CC48h
4C4Ch	32	EMIF_CTLCFG_DENALI_PHY_787	0F30 CC4Ch
4C50h	32	EMIF_CTLCFG_DENALI_PHY_788	0F30 CC50h
4C54h	32	EMIF_CTLCFG_DENALI_PHY_789	0F30 CC54h
4C58h	32	EMIF_CTLCFG_DENALI_PHY_790	0F30 CC58h
4C5Ch	32	EMIF_CTLCFG_DENALI_PHY_791	0F30 CC5Ch
4C60h	32	EMIF_CTLCFG_DENALI_PHY_792	0F30 CC60h
4C64h	32	EMIF_CTLCFG_DENALI_PHY_793	0F30 CC64h
4C68h	32	EMIF_CTLCFG_DENALI_PHY_794	0F30 CC68h
4C6Ch	32	EMIF_CTLCFG_DENALI_PHY_795	0F30 CC6Ch
4C70h	32	EMIF_CTLCFG_DENALI_PHY_796	0F30 CC70h
4C74h	32	EMIF_CTLCFG_DENALI_PHY_797	0F30 CC74h
4C78h	32	EMIF_CTLCFG_DENALI_PHY_798	0F30 CC78h
4C7Ch	32	EMIF_CTLCFG_DENALI_PHY_799	0F30 CC7Ch
4C80h	32	EMIF_CTLCFG_DENALI_PHY_800	0F30 CC80h
4C84h	32	EMIF_CTLCFG_DENALI_PHY_801	0F30 CC84h
4C88h	32	EMIF_CTLCFG_DENALI_PHY_802	0F30 CC88h
4C8Ch	32	EMIF_CTLCFG_DENALI_PHY_803	0F30 CC8Ch
4C90h	32	EMIF_CTLCFG_DENALI_PHY_804	0F30 CC90h
4C94h	32	EMIF_CTLCFG_DENALI_PHY_805	0F30 CC94h
4C98h	32	EMIF_CTLCFG_DENALI_PHY_806	0F30 CC98h
4C9Ch	32	EMIF_CTLCFG_DENALI_PHY_807	0F30 CC9Ch
4CA0h	32	EMIF_CTLCFG_DENALI_PHY_808	0F30 CCA0h
4CA4h	32	EMIF_CTLCFG_DENALI_PHY_809	0F30 CCA4h
4CA8h	32	EMIF_CTLCFG_DENALI_PHY_810	0F30 CCA8h
4CACh	32	EMIF_CTLCFG_DENALI_PHY_811	0F30 CCACh
4CB0h	32	EMIF_CTLCFG_DENALI_PHY_812	0F30 CCB0h
4CB4h	32	EMIF_CTLCFG_DENALI_PHY_813	0F30 CCB4h
4CB8h	32	EMIF_CTLCFG_DENALI_PHY_814	0F30 CCB8h
4CBCh	32	EMIF_CTLCFG_DENALI_PHY_815	0F30 CCBCh
4CC0h	32	EMIF_CTLCFG_DENALI_PHY_816	0F30 CCC0h
4CC4h	32	EMIF_CTLCFG_DENALI_PHY_817	0F30 CCC4h
4CC8h	32	EMIF_CTLCFG_DENALI_PHY_818	0F30 CCC8h
4CCCh	32	EMIF_CTLCFG_DENALI_PHY_819	0F30 CCCCh
4CD0h	32	EMIF_CTLCFG_DENALI_PHY_820	0F30 CCD0h
4CD4h	32	EMIF_CTLCFG_DENALI_PHY_821	0F30 CCD4h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4CD8h	32	EMIF_CTLCFG_DENALI_PHY_822	0F30 CCD8h
4CDCh	32	EMIF_CTLCFG_DENALI_PHY_823	0F30 CCDCh
4CE0h	32	EMIF_CTLCFG_DENALI_PHY_824	0F30 CCE0h
4CE4h	32	EMIF_CTLCFG_DENALI_PHY_825	0F30 CCE4h
4CE8h	32	EMIF_CTLCFG_DENALI_PHY_826	0F30 CCE8h
4CECh	32	EMIF_CTLCFG_DENALI_PHY_827	0F30 CCECh
4CF0h	32	EMIF_CTLCFG_DENALI_PHY_828	0F30 CCF0h
4CF4h	32	EMIF_CTLCFG_DENALI_PHY_829	0F30 CCF4h
4CF8h	32	EMIF_CTLCFG_DENALI_PHY_830	0F30 CCF8h
4CFCh	32	EMIF_CTLCFG_DENALI_PHY_831	0F30 CCFCh
4D00h	32	EMIF_CTLCFG_DENALI_PHY_832	0F30 CD00h
4D04h	32	EMIF_CTLCFG_DENALI_PHY_833	0F30 CD04h
4D08h	32	EMIF_CTLCFG_DENALI_PHY_834	0F30 CD08h
4D0Ch	32	EMIF_CTLCFG_DENALI_PHY_835	0F30 CD0Ch
4D10h	32	EMIF_CTLCFG_DENALI_PHY_836	0F30 CD10h
4D14h	32	EMIF_CTLCFG_DENALI_PHY_837	0F30 CD14h
4D18h	32	EMIF_CTLCFG_DENALI_PHY_838	0F30 CD18h
4D1Ch	32	EMIF_CTLCFG_DENALI_PHY_839	0F30 CD1Ch
4D20h	32	EMIF_CTLCFG_DENALI_PHY_840	0F30 CD20h
4D24h	32	EMIF_CTLCFG_DENALI_PHY_841	0F30 CD24h
4D28h	32	EMIF_CTLCFG_DENALI_PHY_842	0F30 CD28h
4D2Ch	32	EMIF_CTLCFG_DENALI_PHY_843	0F30 CD2Ch
4D30h	32	EMIF_CTLCFG_DENALI_PHY_844	0F30 CD30h
4D34h	32	EMIF_CTLCFG_DENALI_PHY_845	0F30 CD34h
4D38h	32	EMIF_CTLCFG_DENALI_PHY_846	0F30 CD38h
4D3Ch	32	EMIF_CTLCFG_DENALI_PHY_847	0F30 CD3Ch
4D40h	32	EMIF_CTLCFG_DENALI_PHY_848	0F30 CD40h
4D44h	32	EMIF_CTLCFG_DENALI_PHY_849	0F30 CD44h
4D48h	32	EMIF_CTLCFG_DENALI_PHY_850	0F30 CD48h
4D4Ch	32	EMIF_CTLCFG_DENALI_PHY_851	0F30 CD4Ch
4D50h	32	EMIF_CTLCFG_DENALI_PHY_852	0F30 CD50h
4D54h	32	EMIF_CTLCFG_DENALI_PHY_853	0F30 CD54h
4D58h	32	EMIF_CTLCFG_DENALI_PHY_854	0F30 CD58h
4D5Ch	32	EMIF_CTLCFG_DENALI_PHY_855	0F30 CD5Ch
4D60h	32	EMIF_CTLCFG_DENALI_PHY_856	0F30 CD60h
4D64h	32	EMIF_CTLCFG_DENALI_PHY_857	0F30 CD64h
4D68h	32	EMIF_CTLCFG_DENALI_PHY_858	0F30 CD68h
4D6Ch	32	EMIF_CTLCFG_DENALI_PHY_859	0F30 CD6Ch
4D70h	32	EMIF_CTLCFG_DENALI_PHY_860	0F30 CD70h
4D74h	32	EMIF_CTLCFG_DENALI_PHY_861	0F30 CD74h
4D78h	32	EMIF_CTLCFG_DENALI_PHY_862	0F30 CD78h
4D7Ch	32	EMIF_CTLCFG_DENALI_PHY_863	0F30 CD7Ch
4D80h	32	EMIF_CTLCFG_DENALI_PHY_864	0F30 CD80h
4D84h	32	EMIF_CTLCFG_DENALI_PHY_865	0F30 CD84h
4D88h	32	EMIF_CTLCFG_DENALI_PHY_866	0F30 CD88h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
4D8Ch	32	EMIF_CTLCFG_DENALI_PHY_867	0F30 CD8Ch
4D90h	32	EMIF_CTLCFG_DENALI_PHY_868	0F30 CD90h
4D94h	32	EMIF_CTLCFG_DENALI_PHY_869	0F30 CD94h
4D98h	32	EMIF_CTLCFG_DENALI_PHY_870	0F30 CD98h
4D9Ch	32	EMIF_CTLCFG_DENALI_PHY_871	0F30 CD9Ch
4DA0h	32	EMIF_CTLCFG_DENALI_PHY_872	0F30 CDA0h
4DA4h	32	EMIF_CTLCFG_DENALI_PHY_873	0F30 CDA4h
4DA8h	32	EMIF_CTLCFG_DENALI_PHY_874	0F30 CDA8h
4DACh	32	EMIF_CTLCFG_DENALI_PHY_875	0F30 CDACh
4DB0h	32	EMIF_CTLCFG_DENALI_PHY_876	0F30 CDB0h
4DB4h	32	EMIF_CTLCFG_DENALI_PHY_877	0F30 CDB4h
4DB8h	32	EMIF_CTLCFG_DENALI_PHY_878	0F30 CDB8h
4DBCh	32	EMIF_CTLCFG_DENALI_PHY_879	0F30 CDBCh
4DC0h	32	EMIF_CTLCFG_DENALI_PHY_880	0F30 CDC0h
4DC4h	32	EMIF_CTLCFG_DENALI_PHY_881	0F30 CDC4h
4DC8h	32	EMIF_CTLCFG_DENALI_PHY_882	0F30 CDC8h
4DCCh	32	EMIF_CTLCFG_DENALI_PHY_883	0F30 CDCCh
4DD0h	32	EMIF_CTLCFG_DENALI_PHY_884	0F30 CDD0h
4DD4h	32	EMIF_CTLCFG_DENALI_PHY_885	0F30 CDD4h
4DD8h	32	EMIF_CTLCFG_DENALI_PHY_886	0F30 CDD8h
4DDCh	32	EMIF_CTLCFG_DENALI_PHY_887	0F30 CDDCh
4DE0h	32	EMIF_CTLCFG_DENALI_PHY_888	0F30 CDE0h
4DE4h	32	EMIF_CTLCFG_DENALI_PHY_889	0F30 CDE4h
4DE8h	32	EMIF_CTLCFG_DENALI_PHY_890	0F30 CDE8h
4DECh	32	EMIF_CTLCFG_DENALI_PHY_891	0F30 CDECh
4DF0h	32	EMIF_CTLCFG_DENALI_PHY_892	0F30 CDF0h
4DF4h	32	EMIF_CTLCFG_DENALI_PHY_893	0F30 CDF4h
4DF8h	32	EMIF_CTLCFG_DENALI_PHY_894	0F30 CDF8h
4DFCh	32	EMIF_CTLCFG_DENALI_PHY_895	0F30 CDFCh
4E00h	32	EMIF_CTLCFG_DENALI_PHY_896	0F30 CE00h
4E04h	32	EMIF_CTLCFG_DENALI_PHY_897	0F30 CE04h
4E08h	32	EMIF_CTLCFG_DENALI_PHY_898	0F30 CE08h
4E0Ch	32	EMIF_CTLCFG_DENALI_PHY_899	0F30 CE0Ch
4E10h	32	EMIF_CTLCFG_DENALI_PHY_900	0F30 CE10h
4E14h	32	EMIF_CTLCFG_DENALI_PHY_901	0F30 CE14h
4E18h	32	EMIF_CTLCFG_DENALI_PHY_902	0F30 CE18h
4E1Ch	32	EMIF_CTLCFG_DENALI_PHY_903	0F30 CE1Ch
4E20h	32	EMIF_CTLCFG_DENALI_PHY_904	0F30 CE20h
5000h	32	EMIF_CTLCFG_DENALI_PHY_1024	0F30 D000h
5004h	32	EMIF_CTLCFG_DENALI_PHY_1025	0F30 D004h
5008h	32	EMIF_CTLCFG_DENALI_PHY_1026	0F30 D008h
500Ch	32	EMIF_CTLCFG_DENALI_PHY_1027	0F30 D00Ch
5010h	32	EMIF_CTLCFG_DENALI_PHY_1028	0F30 D010h
5014h	32	EMIF_CTLCFG_DENALI_PHY_1029	0F30 D014h
5018h	32	EMIF_CTLCFG_DENALI_PHY_1030	0F30 D018h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
501Ch	32	EMIF_CTLCFG_DENALI_PHY_1031	0F30 D01Ch
5020h	32	EMIF_CTLCFG_DENALI_PHY_1032	0F30 D020h
5024h	32	EMIF_CTLCFG_DENALI_PHY_1033	0F30 D024h
5028h	32	EMIF_CTLCFG_DENALI_PHY_1034	0F30 D028h
502Ch	32	EMIF_CTLCFG_DENALI_PHY_1035	0F30 D02Ch
5030h	32	EMIF_CTLCFG_DENALI_PHY_1036	0F30 D030h
5034h	32	EMIF_CTLCFG_DENALI_PHY_1037	0F30 D034h
5038h	32	EMIF_CTLCFG_DENALI_PHY_1038	0F30 D038h
503Ch	32	EMIF_CTLCFG_DENALI_PHY_1039	0F30 D03Ch
5040h	32	EMIF_CTLCFG_DENALI_PHY_1040	0F30 D040h
5044h	32	EMIF_CTLCFG_DENALI_PHY_1041	0F30 D044h
5048h	32	EMIF_CTLCFG_DENALI_PHY_1042	0F30 D048h
504Ch	32	EMIF_CTLCFG_DENALI_PHY_1043	0F30 D04Ch
5050h	32	EMIF_CTLCFG_DENALI_PHY_1044	0F30 D050h
5054h	32	EMIF_CTLCFG_DENALI_PHY_1045	0F30 D054h
5058h	32	EMIF_CTLCFG_DENALI_PHY_1046	0F30 D058h
505Ch	32	EMIF_CTLCFG_DENALI_PHY_1047	0F30 D05Ch
5060h	32	EMIF_CTLCFG_DENALI_PHY_1048	0F30 D060h
5064h	32	EMIF_CTLCFG_DENALI_PHY_1049	0F30 D064h
5068h	32	EMIF_CTLCFG_DENALI_PHY_1050	0F30 D068h
506Ch	32	EMIF_CTLCFG_DENALI_PHY_1051	0F30 D06Ch
5070h	32	EMIF_CTLCFG_DENALI_PHY_1052	0F30 D070h
5074h	32	EMIF_CTLCFG_DENALI_PHY_1053	0F30 D074h
5078h	32	EMIF_CTLCFG_DENALI_PHY_1054	0F30 D078h
507Ch	32	EMIF_CTLCFG_DENALI_PHY_1055	0F30 D07Ch
5080h	32	EMIF_CTLCFG_DENALI_PHY_1056	0F30 D080h
5084h	32	EMIF_CTLCFG_DENALI_PHY_1057	0F30 D084h
5088h	32	EMIF_CTLCFG_DENALI_PHY_1058	0F30 D088h
508Ch	32	EMIF_CTLCFG_DENALI_PHY_1059	0F30 D08Ch
5090h	32	EMIF_CTLCFG_DENALI_PHY_1060	0F30 D090h
5094h	32	EMIF_CTLCFG_DENALI_PHY_1061	0F30 D094h
5098h	32	EMIF_CTLCFG_DENALI_PHY_1062	0F30 D098h
509Ch	32	EMIF_CTLCFG_DENALI_PHY_1063	0F30 D09Ch
50A0h	32	EMIF_CTLCFG_DENALI_PHY_1064	0F30 D0A0h
50A4h	32	EMIF_CTLCFG_DENALI_PHY_1065	0F30 D0A4h
50A8h	32	EMIF_CTLCFG_DENALI_PHY_1066	0F30 D0A8h
50ACh	32	EMIF_CTLCFG_DENALI_PHY_1067	0F30 D0ACh
50B0h	32	EMIF_CTLCFG_DENALI_PHY_1068	0F30 D0B0h
50B4h	32	EMIF_CTLCFG_DENALI_PHY_1069	0F30 D0B4h
50B8h	32	EMIF_CTLCFG_DENALI_PHY_1070	0F30 D0B8h
50BCh	32	EMIF_CTLCFG_DENALI_PHY_1071	0F30 D0BCh
50C0h	32	EMIF_CTLCFG_DENALI_PHY_1072	0F30 D0C0h
5400h	32	EMIF_CTLCFG_DENALI_PHY_1280	0F30 D400h
5404h	32	EMIF_CTLCFG_DENALI_PHY_1281	0F30 D404h
5408h	32	EMIF_CTLCFG_DENALI_PHY_1282	0F30 D408h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
540Ch	32	EMIF_CTLCFG_DENALI_PHY_1283	0F30 D40Ch
5410h	32	EMIF_CTLCFG_DENALI_PHY_1284	0F30 D410h
5414h	32	EMIF_CTLCFG_DENALI_PHY_1285	0F30 D414h
5418h	32	EMIF_CTLCFG_DENALI_PHY_1286	0F30 D418h
541Ch	32	EMIF_CTLCFG_DENALI_PHY_1287	0F30 D41Ch
5420h	32	EMIF_CTLCFG_DENALI_PHY_1288	0F30 D420h
5424h	32	EMIF_CTLCFG_DENALI_PHY_1289	0F30 D424h
5428h	32	EMIF_CTLCFG_DENALI_PHY_1290	0F30 D428h
542Ch	32	EMIF_CTLCFG_DENALI_PHY_1291	0F30 D42Ch
5430h	32	EMIF_CTLCFG_DENALI_PHY_1292	0F30 D430h
5434h	32	EMIF_CTLCFG_DENALI_PHY_1293	0F30 D434h
5438h	32	EMIF_CTLCFG_DENALI_PHY_1294	0F30 D438h
543Ch	32	EMIF_CTLCFG_DENALI_PHY_1295	0F30 D43Ch
5440h	32	EMIF_CTLCFG_DENALI_PHY_1296	0F30 D440h
5444h	32	EMIF_CTLCFG_DENALI_PHY_1297	0F30 D444h
5448h	32	EMIF_CTLCFG_DENALI_PHY_1298	0F30 D448h
544Ch	32	EMIF_CTLCFG_DENALI_PHY_1299	0F30 D44Ch
5450h	32	EMIF_CTLCFG_DENALI_PHY_1300	0F30 D450h
5454h	32	EMIF_CTLCFG_DENALI_PHY_1301	0F30 D454h
5458h	32	EMIF_CTLCFG_DENALI_PHY_1302	0F30 D458h
545Ch	32	EMIF_CTLCFG_DENALI_PHY_1303	0F30 D45Ch
5460h	32	EMIF_CTLCFG_DENALI_PHY_1304	0F30 D460h
5464h	32	EMIF_CTLCFG_DENALI_PHY_1305	0F30 D464h
5468h	32	EMIF_CTLCFG_DENALI_PHY_1306	0F30 D468h
546Ch	32	EMIF_CTLCFG_DENALI_PHY_1307	0F30 D46Ch
5470h	32	EMIF_CTLCFG_DENALI_PHY_1308	0F30 D470h
5474h	32	EMIF_CTLCFG_DENALI_PHY_1309	0F30 D474h
5478h	32	EMIF_CTLCFG_DENALI_PHY_1310	0F30 D478h
547Ch	32	EMIF_CTLCFG_DENALI_PHY_1311	0F30 D47Ch
5480h	32	EMIF_CTLCFG_DENALI_PHY_1312	0F30 D480h
5484h	32	EMIF_CTLCFG_DENALI_PHY_1313	0F30 D484h
5488h	32	EMIF_CTLCFG_DENALI_PHY_1314	0F30 D488h
548Ch	32	EMIF_CTLCFG_DENALI_PHY_1315	0F30 D48Ch
5490h	32	EMIF_CTLCFG_DENALI_PHY_1316	0F30 D490h
5494h	32	EMIF_CTLCFG_DENALI_PHY_1317	0F30 D494h
5498h	32	EMIF_CTLCFG_DENALI_PHY_1318	0F30 D498h
549Ch	32	EMIF_CTLCFG_DENALI_PHY_1319	0F30 D49Ch
54A0h	32	EMIF_CTLCFG_DENALI_PHY_1320	0F30 D4A0h
54A4h	32	EMIF_CTLCFG_DENALI_PHY_1321	0F30 D4A4h
54A8h	32	EMIF_CTLCFG_DENALI_PHY_1322	0F30 D4A8h
54ACh	32	EMIF_CTLCFG_DENALI_PHY_1323	0F30 D4ACh
54B0h	32	EMIF_CTLCFG_DENALI_PHY_1324	0F30 D4B0h
54B4h	32	EMIF_CTLCFG_DENALI_PHY_1325	0F30 D4B4h
54B8h	32	EMIF_CTLCFG_DENALI_PHY_1326	0F30 D4B8h
54BCh	32	EMIF_CTLCFG_DENALI_PHY_1327	0F30 D4BCh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
54C0h	32	EMIF_CTLCFG_DENALI_PHY_1328	0F30 D4C0h
5800h	32	EMIF_CTLCFG_DENALI_PHY_1536	0F30 D800h
5804h	32	EMIF_CTLCFG_DENALI_PHY_1537	0F30 D804h
5808h	32	EMIF_CTLCFG_DENALI_PHY_1538	0F30 D808h
580Ch	32	EMIF_CTLCFG_DENALI_PHY_1539	0F30 D80Ch
5810h	32	EMIF_CTLCFG_DENALI_PHY_1540	0F30 D810h
5814h	32	EMIF_CTLCFG_DENALI_PHY_1541	0F30 D814h
5818h	32	EMIF_CTLCFG_DENALI_PHY_1542	0F30 D818h
581Ch	32	EMIF_CTLCFG_DENALI_PHY_1543	0F30 D81Ch
5820h	32	EMIF_CTLCFG_DENALI_PHY_1544	0F30 D820h
5824h	32	EMIF_CTLCFG_DENALI_PHY_1545	0F30 D824h
5828h	32	EMIF_CTLCFG_DENALI_PHY_1546	0F30 D828h
582Ch	32	EMIF_CTLCFG_DENALI_PHY_1547	0F30 D82Ch
5830h	32	EMIF_CTLCFG_DENALI_PHY_1548	0F30 D830h
5834h	32	EMIF_CTLCFG_DENALI_PHY_1549	0F30 D834h
5838h	32	EMIF_CTLCFG_DENALI_PHY_1550	0F30 D838h
583Ch	32	EMIF_CTLCFG_DENALI_PHY_1551	0F30 D83Ch
5840h	32	EMIF_CTLCFG_DENALI_PHY_1552	0F30 D840h
5844h	32	EMIF_CTLCFG_DENALI_PHY_1553	0F30 D844h
5848h	32	EMIF_CTLCFG_DENALI_PHY_1554	0F30 D848h
584Ch	32	EMIF_CTLCFG_DENALI_PHY_1555	0F30 D84Ch
5850h	32	EMIF_CTLCFG_DENALI_PHY_1556	0F30 D850h
5854h	32	EMIF_CTLCFG_DENALI_PHY_1557	0F30 D854h
5858h	32	EMIF_CTLCFG_DENALI_PHY_1558	0F30 D858h
585Ch	32	EMIF_CTLCFG_DENALI_PHY_1559	0F30 D85Ch
5860h	32	EMIF_CTLCFG_DENALI_PHY_1560	0F30 D860h
5864h	32	EMIF_CTLCFG_DENALI_PHY_1561	0F30 D864h
5868h	32	EMIF_CTLCFG_DENALI_PHY_1562	0F30 D868h
586Ch	32	EMIF_CTLCFG_DENALI_PHY_1563	0F30 D86Ch
5870h	32	EMIF_CTLCFG_DENALI_PHY_1564	0F30 D870h
5874h	32	EMIF_CTLCFG_DENALI_PHY_1565	0F30 D874h
5878h	32	EMIF_CTLCFG_DENALI_PHY_1566	0F30 D878h
587Ch	32	EMIF_CTLCFG_DENALI_PHY_1567	0F30 D87Ch
5880h	32	EMIF_CTLCFG_DENALI_PHY_1568	0F30 D880h
5884h	32	EMIF_CTLCFG_DENALI_PHY_1569	0F30 D884h
5888h	32	EMIF_CTLCFG_DENALI_PHY_1570	0F30 D888h
588Ch	32	EMIF_CTLCFG_DENALI_PHY_1571	0F30 D88Ch
5890h	32	EMIF_CTLCFG_DENALI_PHY_1572	0F30 D890h
5894h	32	EMIF_CTLCFG_DENALI_PHY_1573	0F30 D894h
5898h	32	EMIF_CTLCFG_DENALI_PHY_1574	0F30 D898h
589Ch	32	EMIF_CTLCFG_DENALI_PHY_1575	0F30 D89Ch
58A0h	32	EMIF_CTLCFG_DENALI_PHY_1576	0F30 D8A0h
58A4h	32	EMIF_CTLCFG_DENALI_PHY_1577	0F30 D8A4h
58A8h	32	EMIF_CTLCFG_DENALI_PHY_1578	0F30 D8A8h
58ACh	32	EMIF_CTLCFG_DENALI_PHY_1579	0F30 D8ACh

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
58B0h	32	EMIF_CTLCFG_DENALI_PHY_1580	0F30 D8B0h
58B4h	32	EMIF_CTLCFG_DENALI_PHY_1581	0F30 D8B4h
58B8h	32	EMIF_CTLCFG_DENALI_PHY_1582	0F30 D8B8h
58BCh	32	EMIF_CTLCFG_DENALI_PHY_1583	0F30 D8BCh
58C0h	32	EMIF_CTLCFG_DENALI_PHY_1584	0F30 D8C0h
5C00h	32	EMIF_CTLCFG_DENALI_PHY_1792	0F30 DC00h
5C04h	32	EMIF_CTLCFG_DENALI_PHY_1793	0F30 DC04h
5C08h	32	EMIF_CTLCFG_DENALI_PHY_1794	0F30 DC08h
5C0Ch	32	EMIF_CTLCFG_DENALI_PHY_1795	0F30 DC0Ch
5C10h	32	EMIF_CTLCFG_DENALI_PHY_1796	0F30 DC10h
5C14h	32	EMIF_CTLCFG_DENALI_PHY_1797	0F30 DC14h
5C18h	32	EMIF_CTLCFG_DENALI_PHY_1798	0F30 DC18h
5C1Ch	32	EMIF_CTLCFG_DENALI_PHY_1799	0F30 DC1Ch
5C20h	32	EMIF_CTLCFG_DENALI_PHY_1800	0F30 DC20h
5C24h	32	EMIF_CTLCFG_DENALI_PHY_1801	0F30 DC24h
5C28h	32	EMIF_CTLCFG_DENALI_PHY_1802	0F30 DC28h
5C2Ch	32	EMIF_CTLCFG_DENALI_PHY_1803	0F30 DC2Ch
5C30h	32	EMIF_CTLCFG_DENALI_PHY_1804	0F30 DC30h
5C34h	32	EMIF_CTLCFG_DENALI_PHY_1805	0F30 DC34h
5C38h	32	EMIF_CTLCFG_DENALI_PHY_1806	0F30 DC38h
5C3Ch	32	EMIF_CTLCFG_DENALI_PHY_1807	0F30 DC3Ch
5C40h	32	EMIF_CTLCFG_DENALI_PHY_1808	0F30 DC40h
5C44h	32	EMIF_CTLCFG_DENALI_PHY_1809	0F30 DC44h
5C48h	32	EMIF_CTLCFG_DENALI_PHY_1810	0F30 DC48h
5C4Ch	32	EMIF_CTLCFG_DENALI_PHY_1811	0F30 DC4Ch
5C50h	32	EMIF_CTLCFG_DENALI_PHY_1812	0F30 DC50h
5C54h	32	EMIF_CTLCFG_DENALI_PHY_1813	0F30 DC54h
5C58h	32	EMIF_CTLCFG_DENALI_PHY_1814	0F30 DC58h
5C5Ch	32	EMIF_CTLCFG_DENALI_PHY_1815	0F30 DC5Ch
5C60h	32	EMIF_CTLCFG_DENALI_PHY_1816	0F30 DC60h
5C64h	32	EMIF_CTLCFG_DENALI_PHY_1817	0F30 DC64h
5C68h	32	EMIF_CTLCFG_DENALI_PHY_1818	0F30 DC68h
5C6Ch	32	EMIF_CTLCFG_DENALI_PHY_1819	0F30 DC6Ch
5C70h	32	EMIF_CTLCFG_DENALI_PHY_1820	0F30 DC70h
5C74h	32	EMIF_CTLCFG_DENALI_PHY_1821	0F30 DC74h
5C78h	32	EMIF_CTLCFG_DENALI_PHY_1822	0F30 DC78h
5C7Ch	32	EMIF_CTLCFG_DENALI_PHY_1823	0F30 DC7Ch
5C80h	32	EMIF_CTLCFG_DENALI_PHY_1824	0F30 DC80h
5C84h	32	EMIF_CTLCFG_DENALI_PHY_1825	0F30 DC84h
5C88h	32	EMIF_CTLCFG_DENALI_PHY_1826	0F30 DC88h
5C8Ch	32	EMIF_CTLCFG_DENALI_PHY_1827	0F30 DC8Ch
5C90h	32	EMIF_CTLCFG_DENALI_PHY_1828	0F30 DC90h
5C94h	32	EMIF_CTLCFG_DENALI_PHY_1829	0F30 DC94h
5C98h	32	EMIF_CTLCFG_DENALI_PHY_1830	0F30 DC98h
5C9Ch	32	EMIF_CTLCFG_DENALI_PHY_1831	0F30 DC9Ch

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
5CA0h	32	EMIF_CTLCFG_DENALI_PHY_1832	0F30 DCA0h
5CA4h	32	EMIF_CTLCFG_DENALI_PHY_1833	0F30 DCA4h
5CA8h	32	EMIF_CTLCFG_DENALI_PHY_1834	0F30 DCA8h
5CACh	32	EMIF_CTLCFG_DENALI_PHY_1835	0F30 DCACh
5CB0h	32	EMIF_CTLCFG_DENALI_PHY_1836	0F30 DCB0h
5CB4h	32	EMIF_CTLCFG_DENALI_PHY_1837	0F30 DCB4h
5CB8h	32	EMIF_CTLCFG_DENALI_PHY_1838	0F30 DCB8h
5CBCh	32	EMIF_CTLCFG_DENALI_PHY_1839	0F30 DCBCh
5CC0h	32	EMIF_CTLCFG_DENALI_PHY_1840	0F30 DCC0h
5CC4h	32	EMIF_CTLCFG_DENALI_PHY_1841	0F30 DCC4h
5CC8h	32	EMIF_CTLCFG_DENALI_PHY_1842	0F30 DCC8h
5CCCh	32	EMIF_CTLCFG_DENALI_PHY_1843	0F30 DCCCh
5CD0h	32	EMIF_CTLCFG_DENALI_PHY_1844	0F30 DCD0h
5CD4h	32	EMIF_CTLCFG_DENALI_PHY_1845	0F30 DCD4h
5CD8h	32	EMIF_CTLCFG_DENALI_PHY_1846	0F30 DCD8h
5CDCh	32	EMIF_CTLCFG_DENALI_PHY_1847	0F30 DCDCh
5CE0h	32	EMIF_CTLCFG_DENALI_PHY_1848	0F30 DCE0h
5CE4h	32	EMIF_CTLCFG_DENALI_PHY_1849	0F30 DCE4h
5CE8h	32	EMIF_CTLCFG_DENALI_PHY_1850	0F30 DCE8h
5CECh	32	EMIF_CTLCFG_DENALI_PHY_1851	0F30 DCECh
5CF0h	32	EMIF_CTLCFG_DENALI_PHY_1852	0F30 DCF0h
5CF4h	32	EMIF_CTLCFG_DENALI_PHY_1853	0F30 DCF4h
5CF8h	32	EMIF_CTLCFG_DENALI_PHY_1854	0F30 DCF8h
5CFCh	32	EMIF_CTLCFG_DENALI_PHY_1855	0F30 DCFCh
5D00h	32	EMIF_CTLCFG_DENALI_PHY_1856	0F30 DD00h
5D04h	32	EMIF_CTLCFG_DENALI_PHY_1857	0F30 DD04h
5D08h	32	EMIF_CTLCFG_DENALI_PHY_1858	0F30 DD08h
5D0Ch	32	EMIF_CTLCFG_DENALI_PHY_1859	0F30 DD0Ch
5D10h	32	EMIF_CTLCFG_DENALI_PHY_1860	0F30 DD10h
5D14h	32	EMIF_CTLCFG_DENALI_PHY_1861	0F30 DD14h
5D18h	32	EMIF_CTLCFG_DENALI_PHY_1862	0F30 DD18h
5D1Ch	32	EMIF_CTLCFG_DENALI_PHY_1863	0F30 DD1Ch
5D20h	32	EMIF_CTLCFG_DENALI_PHY_1864	0F30 DD20h
5D24h	32	EMIF_CTLCFG_DENALI_PHY_1865	0F30 DD24h
5D28h	32	EMIF_CTLCFG_DENALI_PHY_1866	0F30 DD28h
5D2Ch	32	EMIF_CTLCFG_DENALI_PHY_1867	0F30 DD2Ch
5D30h	32	EMIF_CTLCFG_DENALI_PHY_1868	0F30 DD30h
5D34h	32	EMIF_CTLCFG_DENALI_PHY_1869	0F30 DD34h
5D38h	32	EMIF_CTLCFG_DENALI_PHY_1870	0F30 DD38h
5D3Ch	32	EMIF_CTLCFG_DENALI_PHY_1871	0F30 DD3Ch
5D40h	32	EMIF_CTLCFG_DENALI_PHY_1872	0F30 DD40h
5D44h	32	EMIF_CTLCFG_DENALI_PHY_1873	0F30 DD44h
5D48h	32	EMIF_CTLCFG_DENALI_PHY_1874	0F30 DD48h
5D4Ch	32	EMIF_CTLCFG_DENALI_PHY_1875	0F30 DD4Ch
5D50h	32	EMIF_CTLCFG_DENALI_PHY_1876	0F30 DD50h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
5D54h	32	EMIF_CTLCFG_DENALI_PHY_1877	0F30 DD54h
5D58h	32	EMIF_CTLCFG_DENALI_PHY_1878	0F30 DD58h
5D5Ch	32	EMIF_CTLCFG_DENALI_PHY_1879	0F30 DD5Ch
5D60h	32	EMIF_CTLCFG_DENALI_PHY_1880	0F30 DD60h
5D64h	32	EMIF_CTLCFG_DENALI_PHY_1881	0F30 DD64h
5D68h	32	EMIF_CTLCFG_DENALI_PHY_1882	0F30 DD68h
5D6Ch	32	EMIF_CTLCFG_DENALI_PHY_1883	0F30 DD6Ch
5D70h	32	EMIF_CTLCFG_DENALI_PHY_1884	0F30 DD70h
5D74h	32	EMIF_CTLCFG_DENALI_PHY_1885	0F30 DD74h
5D78h	32	EMIF_CTLCFG_DENALI_PHY_1886	0F30 DD78h
5D7Ch	32	EMIF_CTLCFG_DENALI_PHY_1887	0F30 DD7Ch
5D80h	32	EMIF_CTLCFG_DENALI_PHY_1888	0F30 DD80h
5D84h	32	EMIF_CTLCFG_DENALI_PHY_1889	0F30 DD84h
5D88h	32	EMIF_CTLCFG_DENALI_PHY_1890	0F30 DD88h
5D8Ch	32	EMIF_CTLCFG_DENALI_PHY_1891	0F30 DD8Ch
5D90h	32	EMIF_CTLCFG_DENALI_PHY_1892	0F30 DD90h
5D94h	32	EMIF_CTLCFG_DENALI_PHY_1893	0F30 DD94h
5D98h	32	EMIF_CTLCFG_DENALI_PHY_1894	0F30 DD98h
5D9Ch	32	EMIF_CTLCFG_DENALI_PHY_1895	0F30 DD9Ch
5DA0h	32	EMIF_CTLCFG_DENALI_PHY_1896	0F30 DDA0h
5DA4h	32	EMIF_CTLCFG_DENALI_PHY_1897	0F30 DDA4h
5DA8h	32	EMIF_CTLCFG_DENALI_PHY_1898	0F30 DDA8h
5DACh	32	EMIF_CTLCFG_DENALI_PHY_1899	0F30 DDACh
5DB0h	32	EMIF_CTLCFG_DENALI_PHY_1900	0F30 DDB0h
5DB4h	32	EMIF_CTLCFG_DENALI_PHY_1901	0F30 DDB4h
5DB8h	32	EMIF_CTLCFG_DENALI_PHY_1902	0F30 DDB8h
5DBCh	32	EMIF_CTLCFG_DENALI_PHY_1903	0F30 DDBCh
5DC0h	32	EMIF_CTLCFG_DENALI_PHY_1904	0F30 DDC0h
5DC4h	32	EMIF_CTLCFG_DENALI_PHY_1905	0F30 DDC4h
5DC8h	32	EMIF_CTLCFG_DENALI_PHY_1906	0F30 DDC8h
5DCCh	32	EMIF_CTLCFG_DENALI_PHY_1907	0F30 DDCCh
5DD0h	32	EMIF_CTLCFG_DENALI_PHY_1908	0F30 DDD0h
5DD4h	32	EMIF_CTLCFG_DENALI_PHY_1909	0F30 DDD4h
5DD8h	32	EMIF_CTLCFG_DENALI_PHY_1910	0F30 DDD8h
5DDCh	32	EMIF_CTLCFG_DENALI_PHY_1911	0F30 DDDCh
5DE0h	32	EMIF_CTLCFG_DENALI_PHY_1912	0F30 DDE0h
5DE4h	32	EMIF_CTLCFG_DENALI_PHY_1913	0F30 DDE4h
5DE8h	32	EMIF_CTLCFG_DENALI_PHY_1914	0F30 DDE8h
5DECh	32	EMIF_CTLCFG_DENALI_PHY_1915	0F30 DDECh
5DF0h	32	EMIF_CTLCFG_DENALI_PHY_1916	0F30 DDF0h
5DF4h	32	EMIF_CTLCFG_DENALI_PHY_1917	0F30 DDF4h
5DF8h	32	EMIF_CTLCFG_DENALI_PHY_1918	0F30 DDF8h
5DFCh	32	EMIF_CTLCFG_DENALI_PHY_1919	0F30 DDFCh
5E00h	32	EMIF_CTLCFG_DENALI_PHY_1920	0F30 DE00h
5E04h	32	EMIF_CTLCFG_DENALI_PHY_1921	0F30 DE04h

Table 14-19946. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR32SS0 Physical Address
5E08h	32	EMIF_CTLCFG_DENALI_PHY_1922	0F30 DE08h
5E0Ch	32	EMIF_CTLCFG_DENALI_PHY_1923	0F30 DE0Ch

14.6.6.2 ddr32ss Registers

ddr32ss Registers

14.6.6.2.1 EMIF_SSCFG_SS_ID_REV_REG Register

1 EMIF_SSCFG_SS_ID_REV_REG Register (Offset = 0h) [reset = 68052900h]

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

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Table 14-19947. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0000h**

Figure 14-6614. EMIF_SSCFG_SS_ID_REV_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6805h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6805h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJ_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MIN_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-19949. EMIF_SSCFG_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MOD_ID	R	6805h	Module ID Reset Source: ctl_smod_g_rst_n
15:11	RTL_VER	R	5h	RTL version Reset Source: ctl_smod_g_rst_n
10:8	MAJ_REV	R	1h	Major revision Reset Source: ctl_smod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: ctl_smod_g_rst_n
5:0	MIN_REV	R	0h	Minor revision Reset Source: ctl_smod_g_rst_n

14.6.6.2.2 EMIF_SSCFG_SS_CTL_REG Register

1 EMIF_SSCFG_SS_CTL_REG Register (Offset = 4h) [reset = 0h]

The Subsystem Control Register contains fields for control functions required for submodules in the subsystem.

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Table 14-19950. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0004h**

Figure 14-6615. EMIF_SSCFG_SS_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-19952. EMIF_SSCFG_SS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_BYPASS	R/W	0h	Cadence PHY De-Skew PLL bypass. Write 1 to bypass PLL. Reset Source: ctl_smod_g_rst_n

14.6.6.2.3 EMIF_SSCFG_V2A_CTL_REG Register

1 EMIF_SSCFG_V2A_CTL_REG Register (Offset = 20h) [reset = FF18273h]

The VBUSM2AXI Control register contains control functions required for the VBUSM2AXI submodule.

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Table 14-19953. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0020h**

Figure 14-6616. EMIF_SSCFG_V2A_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				TOTAL_CMD_THRESH			
NONE				R/W			
0h				3Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TOTAL_CMD_THRESH		WR_LO_BLK_THR					CRIT_THRESH
R/W		R/W					R/W
3Fh		18h					18h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRIT_THRESH				RESERVED	SDRAM_3QT	SDRAM_IDX	
R/W				NONE	R/W	R/W	
18h				0h	0h	13h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDRAM_IDX			REGION_IDX				
R/W			R/W				
13h			13h				

Table 14-19955. EMIF_SSCFG_V2A_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:22	TOTAL_CMD_THRESH	R/W	3Fh	Total command threshold. The VBUSM2AXI bridge will block all commands to DDR when the total number of commands sent to the Cadence controller is greater than this value. The reset value of this field is optimal; however, it can be changed for better traffic shaping. Reset Source: ctl_smod_g_rst_n
21:17	WR_LO_BLK_THR	R/W	18h	Write data threshold in 32 byte quantas. The VBUSM2AXI bridge will block all Low Priority Thread writes to DDR when the total number of write data bytes sent to the Cadence controller is greater than this value. The reset value of this field is optimal; however, it can be changed for better traffic shaping. Reset Source: ctl_smod_g_rst_n
16:12	CRIT_THRESH	R/W	18h	Critical threshold. The VBUSM2AXI bridge will block all Low Priority Thread traffic to DDR when the total number of commands sent to the Cadence controller is greater than this value. The reset value of this field is optimal; however, it can be changed for better traffic shaping. This value must always be programmed less than total_cmd_thresh Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved

Table 14-19955. EMIF_SSCFG_V2A_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SDRAM_3QT	R/W	0h	Setting this field to a 1 will modify SDRAM Index to be 3/4 its programmed value to support 3, 6, 12 and 24 GB sizes. Reset Source: ctl_smod_g_rst_n
9:5	SDRAM_IDX	R/W	13h	SDRAM Index = log2(connected SDRAM size) - 16. The sdram_idx describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues. Max size supported is 32GB. A programmed value greater than 0x13 will result in this field being reset to 0x13. Reset Source: ctl_smod_g_rst_n
4:0	REGION_IDX	R/W	13h	Region Index = log2(CBA region size) - 16. The region_idx describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues. Max size supported is 32GB. A programmed value greater than 0x13 will result in this field being reset to 0x13. Reset Source: ctl_smod_g_rst_n

14.6.6.2.4 EMIF_SSCFG_V2A_R1_MAT_REG Register

1 EMIF_SSCFG_V2A_R1_MAT_REG Register (Offset = 24h) [reset = 0h]

The Range 1 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 1 Match Register uses the associated Range 1 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-19956. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0024h**

Figure 14-6617. EMIF_SSCFG_V2A_R1_MAT_REG Name Register

31	30	29	28	27	26	25	24
RANGE1_RANGEEN_A	RANGE1_MASK_A			RANGE1_ROUTEID_A			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
RANGE1_ROUTEID_A							
R/W							
0h							
15	14	13	12	11	10	9	8
RANGE1_RANGEEN_B	RANGE1_MASK_B			RANGE1_ROUTEID_B			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
RANGE1_ROUTEID_B							
R/W							
0h							

Table 14-19958. EMIF_SSCFG_V2A_R1_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE1_RANGEEN_A	R/W	0h	The range1_rangeen_a enables the RouteID AND'd with range1_mask_a to match the range1_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE1_MASK_A	R/W	0h	The range1_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE1_ROUTEID_A	R/W	0h	The range1_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE1_RANGEEN_B	R/W	0h	The range1_rangeen_b enables the RouteID AND'd with range1_mask_b to match the range1_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE1_MASK_B	R/W	0h	The range1_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-19958. EMIF_SSCFG_V2A_R1_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE1_ROUTEID_B	R/W	0h	The range1_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.6.6.2.5 EMIF_SSCFG_V2A_R2_MAT_REG Register

1 EMIF_SSCFG_V2A_R2_MAT_REG Register (Offset = 28h) [reset = 0h]

The Range 2 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 2 Match Register uses the associated Range 2 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-19959. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0028h**

Figure 14-6618. EMIF_SSCFG_V2A_R2_MAT_REG Name Register

31	30	29	28	27	26	25	24
RANGE2_RANGEEN_A	RANGE2_MASK_A			RANGE2_ROUTEID_A			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
RANGE2_ROUTEID_A							
R/W							
0h							
15	14	13	12	11	10	9	8
RANGE2_RANGEEN_B	RANGE2_MASK_B			RANGE2_ROUTEID_B			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
RANGE2_ROUTEID_B							
R/W							
0h							

Table 14-19961. EMIF_SSCFG_V2A_R2_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE2_RANGEEN_A	R/W	0h	The range2_rangeen_a enables the RouteID AND'd with range2_mask_a to match the range2_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE2_MASK_A	R/W	0h	The range2_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE2_ROUTEID_A	R/W	0h	The range2_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE2_RANGEEN_B	R/W	0h	The range2_rangeen_b enables the RouteID AND'd with range2_mask_b to match the range2_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE2_MASK_B	R/W	0h	The range2_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-19961. EMIF_SSCFG_V2A_R2_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE2_ROUTEID_B	R/W	0h	The range2_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.6.6.2.6 EMIF_SSCFG_V2A_R3_MAT_REG Register

1 EMIF_SSCFG_V2A_R3_MAT_REG Register (Offset = 2Ch) [reset = 0h]

The Range 3 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 3 Match Register uses the associated Range 3 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-19962. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 002Ch**

Figure 14-6619. EMIF_SSCFG_V2A_R3_MAT_REG Name Register

31	30	29	28	27	26	25	24
RANGE3_RANGEEN_A	RANGE3_MASK_A			RANGE3_ROUTEID_A			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
RANGE3_ROUTEID_A							
R/W							
0h							
15	14	13	12	11	10	9	8
RANGE3_RANGEEN_B	RANGE3_MASK_B			RANGE3_ROUTEID_B			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
RANGE3_ROUTEID_B							
R/W							
0h							

Table 14-19964. EMIF_SSCFG_V2A_R3_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE3_RANGEEN_A	R/W	0h	The range3_rangeen_a enables the RouteID AND'd with range3_mask_a to match the range3_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE3_MASK_A	R/W	0h	The range3_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE3_ROUTEID_A	R/W	0h	The range3_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE3_RANGEEN_B	R/W	0h	The range3_rangeen_b enables the RouteID AND'd with range3_mask_b to match the range3_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE3_MASK_B	R/W	0h	The range3_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-19964. EMIF_SSCFG_V2A_R3_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE3_ROUTEID_B	R/W	0h	The range3_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.6.6.2.7 EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG Register (Offset = 30h) [reset = 0h]

The LPT Default Priority Mapping Register is the default map for the inbound VBUSM priority on the Low Priority Thread to the AXI priority.

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Table 14-19965. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 0030h

Figure 14-6620. EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	LPT_PRIMAP0			RESERVED	LPT_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	LPT_PRIMAP2			RESERVED	LPT_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	LPT_PRIMAP4			RESERVED	LPT_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	LPT_PRIMAP6			RESERVED	LPT_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19967. EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	LPT_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	LPT_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	LPT_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LPT_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19967. EMIF_SSCFG_V2A_LPT_DEF_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	LPT_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	LPT_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	LPT_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	LPT_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.8 EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG Register (Offset = 34h) [reset = 0h]

The LPT Range 1 Priority Mapping Register is used to map the inbound VBUSM priority on the Low Priority Thread to AXI priority when a RouteID match 1 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

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Table 14-19968. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0034h**

Figure 14-6621. EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE1_PRIMAP0			RESERVED	LPT_RANGE1_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	LPT_RANGE1_PRIMAP2			RESERVED	LPT_RANGE1_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	LPT_RANGE1_PRIMAP4			RESERVED	LPT_RANGE1_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	LPT_RANGE1_PRIMAP6			RESERVED	LPT_RANGE1_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19970. EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	LPT_RANGE1_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	LPT_RANGE1_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	LPT_RANGE1_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LPT_RANGE1_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19970. EMIF_SSCFG_V2A_LPT_R1_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	LPT_RANGE1_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	LPT_RANGE1_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	LPT_RANGE1_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	LPT_RANGE1_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.9 EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG Register (Offset = 38h) [reset = 0h]

The LPT Range 2 Priority Mapping Register is used to map the inbound VBUSM priority on the Low Priority Thread to AXI priority when a RouteID match 2 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

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Table 14-19971. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0038h**

Figure 14-6622. EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE2_PRIMAP0			RESERVED	LPT_RANGE2_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	LPT_RANGE2_PRIMAP2			RESERVED	LPT_RANGE2_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	LPT_RANGE2_PRIMAP4			RESERVED	LPT_RANGE2_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	LPT_RANGE2_PRIMAP6			RESERVED	LPT_RANGE2_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19973. EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	LPT_RANGE2_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	LPT_RANGE2_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	LPT_RANGE2_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LPT_RANGE2_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19973. EMIF_SSCFG_V2A_LPT_R2_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	LPT_RANGE2_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	LPT_RANGE2_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	LPT_RANGE2_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	LPT_RANGE2_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.10 EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG Register (Offset = 3Ch) [reset = 0h]

The LPT Range 3 Priority Mapping Register is used to map the inbound VBUSM priority on the Low Priority Thread to AXI priority when a RouteID match 3 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

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Table 14-19974. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 003Ch**

Figure 14-6623. EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE3_PRIMAP0			RESERVED	LPT_RANGE3_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	LPT_RANGE3_PRIMAP2			RESERVED	LPT_RANGE3_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	LPT_RANGE3_PRIMAP4			RESERVED	LPT_RANGE3_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	LPT_RANGE3_PRIMAP6			RESERVED	LPT_RANGE3_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19976. EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	LPT_RANGE3_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	LPT_RANGE3_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	LPT_RANGE3_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	LPT_RANGE3_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19976. EMIF_SSCFG_V2A_LPT_R3_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	LPT_RANGE3_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	LPT_RANGE3_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	LPT_RANGE3_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	LPT_RANGE3_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.11 EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG Register (Offset = 4Ch) [reset = 0h]

The HPT Default Priority Mapping Register is the default map for the inbound VBUSM priority on the High Priority Thread to the AXI priority.

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Table 14-19977. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 004Ch

Figure 14-6624. EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	HPT_PRIMAP0			RESERVED	HPT_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	HPT_PRIMAP2			RESERVED	HPT_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	HPT_PRIMAP4			RESERVED	HPT_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HPT_PRIMAP6			RESERVED	HPT_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19979. EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	HPT_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	HPT_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	HPT_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HPT_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19979. EMIF_SSCFG_V2A_HPT_DEF_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	HPT_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	HPT_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	HPT_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	HPT_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.12 EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG Register (Offset = 50h) [reset = 0h]

The HPT Range 1 Priority Mapping Register is used to map the inbound VBUSM priority on the High Priority Thread to AXI priority when a RouteID match 1 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

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Table 14-19980. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0050h**

Figure 14-6625. EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE1_PRIMAP0			RESERVED	HPT_RANGE1_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_RANGE1_PRIMAP2			RESERVED	HPT_RANGE1_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	HPT_RANGE1_PRIMAP4			RESERVED	HPT_RANGE1_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	HPT_RANGE1_PRIMAP6			RESERVED	HPT_RANGE1_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19982. EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	HPT_RANGE1_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	HPT_RANGE1_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	HPT_RANGE1_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HPT_RANGE1_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19982. EMIF_SSCFG_V2A_HPT_R1_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	HPT_RANGE1_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	HPT_RANGE1_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	HPT_RANGE1_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	HPT_RANGE1_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.13 EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG Register (Offset = 54h) [reset = 0h]

The HPT Range 2 Priority Mapping Register is used to map the inbound VBUSM priority on the High Priority Thread to AXI priority when a RouteID match 2 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

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Table 14-19983. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0054h**

Figure 14-6626. EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE2_PRIMAP0			RESERVED	HPT_RANGE2_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	HPT_RANGE2_PRIMAP2			RESERVED	HPT_RANGE2_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	HPT_RANGE2_PRIMAP4			RESERVED	HPT_RANGE2_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HPT_RANGE2_PRIMAP6			RESERVED	HPT_RANGE2_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19985. EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	HPT_RANGE2_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	HPT_RANGE2_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	HPT_RANGE2_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HPT_RANGE2_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19985. EMIF_SSCFG_V2A_HPT_R2_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	HPT_RANGE2_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	HPT_RANGE2_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	HPT_RANGE2_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	HPT_RANGE2_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.14 EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG Register (Offset = 58h) [reset = 0h]

The HPT Range 3 Priority Mapping Register is used to map the inbound VBUSM priority on the High Priority Thread to AXI priority when a RouteID match 3 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

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Table 14-19986. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 0058h

Figure 14-6627. EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE3_PRIMAP0			RESERVED	HPT_RANGE3_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_RANGE3_PRIMAP2			RESERVED	HPT_RANGE3_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	HPT_RANGE3_PRIMAP4			RESERVED	HPT_RANGE3_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	HPT_RANGE3_PRIMAP6			RESERVED	HPT_RANGE3_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-19988. EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	HPT_RANGE3_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	HPT_RANGE3_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	HPT_RANGE3_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HPT_RANGE3_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-19988. EMIF_SSCFG_V2A_HPT_R3_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	HPT_RANGE3_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	HPT_RANGE3_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	HPT_RANGE3_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	HPT_RANGE3_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.6.6.2.15 EMIF_SSCFG_V2A_OLD_CMD_PR_REG Register

1 EMIF_SSCFG_V2A_OLD_CMD_PR_REG Register (Offset = 5Ch) [reset = 3FFh]

VBUSM2AXI Oldest Command Priority Raise Register

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Table 14-19989. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 005Ch**

Figure 14-6628. EMIF_SSCFG_V2A_OLD_CMD_PR_REG Name Register

31	30	29	28	27	26	25	24
HPT_PRI_EQUAL	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							OLD_CMD_PR_MODE
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						OLD_CMD_PR_THRESH	
NONE						R/W	
0h						3FFh	

7	6	5	4	3	2	1	0
OLD_CMD_PR_THRESH							
R/W							
3FFh							

Table 14-19991. EMIF_SSCFG_V2A_OLD_CMD_PR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HPT_PRI_EQUAL	R/W	0h	Setting to 1 will disable priority-based arbitration among the HPT commands. Reset Source: ctl_smod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	OLD_CMD_PR_MODE	R/W	0h	Oldest Command Priority Raise mode. Setting to 0 will count LPT commands sent while oldest command is waiting. Setting to 1 will count all commands sent while oldest command is waiting. Reset Source: ctl_smod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	OLD_CMD_PR_THRESH	R/W	3FFh	Oldest Command Priority Raise threshold. Number of commands sent in a row before the oldest command in the command FIFO is forwarded. This value must always be programmed greater than leaky thresholds. Reset Source: ctl_smod_g_rst_n

14.6.6.2.16 EMIF_SSCFG_V2A_LEAKY_THRESH_REG Register

1 EMIF_SSCFG_V2A_LEAKY_THRESH_REG Register (Offset = 68h) [reset = FFh]

VBUSM2AXI Leaky Bucket Threshold Register

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Table 14-19992. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0068h**

Figure 14-6629. EMIF_SSCFG_V2A_LEAKY_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SYS_LEAKY_THRESH							
R/W							
FFh							

Table 14-19994. EMIF_SSCFG_V2A_LEAKY_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SYS_LEAKY_THRESH	R/W	FFh	System Leaky Bucket threshold. Number of HPT commands sent in a row before a single LPT command is forwarded. A programmed value less than 0x4 will result in this field being reset to 0xFF. Reset Source: ctl_smod_g_rst_n

14.6.6.2.17 EMIF_SSCFG_V2A_DRAIN_THRESH_REG Register

1 EMIF_SSCFG_V2A_DRAIN_THRESH_REG Register (Offset = 6Ch) [reset = 3FFh]

VBUSM2AXI Drain Threshold Register

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Table 14-19995. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 006Ch**

Figure 14-6630. EMIF_SSCFG_V2A_DRAIN_THRESH_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">SYS_DRAIN_THRESH</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYS_DRAIN_THRESH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3FFh</td></tr>
</table>

Table 14-19997. EMIF_SSCFG_V2A_DRAIN_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	SYS_DRAIN_THRESH	R/W	3FFh	System Drain threshold. Number of commands sent to the Cadence controller after which controller drain will be enabled. A programmed value less than 0x020 will result in this field being reset to 0x3FF. Reset Source: ctl_smod_g_rst_n

14.6.6.2.18 EMIF_SSCFG_V2A_AERR_LOG1_REG Register

1 EMIF_SSCFG_V2A_AERR_LOG1_REG Register (Offset = 70h) [reset = 0h]

The Address Error Log 1 register displays the RouteID and lsb of the address for the first VBUSM command that was outside the programmed addressing range. Writing a 0x1 will clear all fields. Writing any other value has no effect. The Address Error Log 2 register will also be cleared upon writing this register.

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Table 14-19998. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0070h**

Figure 14-6631. EMIF_SSCFG_V2A_AERR_LOG1_REG Name Register

31	30	29	28	27	26	25	24
AERR_ADDR_LSB							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
AERR_ADDR_LSB							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RESERVED				AERR_ROUTE_ID			
NONE				R/W1TC			
0h				0h			
7	6	5	4	3	2	1	0
AERR_ROUTE_ID							
R/W1TC							
0h							

Table 14-20000. EMIF_SSCFG_V2A_AERR_LOG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	AERR_ADDR_LSB	R/W1TC	0h	Address[15:0] of the VBUSM command Reset Source: ctl_smod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	AERR_ROUTE_ID	R/W1TC	0h	RouteID of the VBUSM write command Reset Source: ctl_smod_g_rst_n

14.6.6.2.19 EMIF_SSCFG_V2A_AERR_LOG2_REG Register

1 EMIF_SSCFG_V2A_AERR_LOG2_REG Register (Offset = 74h) [reset = 0h]

The Address Error Log 2 registers displays the msb of the address for the first VBUSM command that was outside the programmed addressing range. This register will be cleared upon writing the Address Error Log 1 register.

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Table 14-20001. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0074h**

Figure 14-6632. EMIF_SSCFG_V2A_AERR_LOG2_REG Name Register

31	30	29	28	27	26	25	24
AERR_ADDR_MSB							
R							
0h							
23	22	21	20	19	18	17	16
AERR_ADDR_MSB							
R							
0h							
15	14	13	12	11	10	9	8
AERR_ADDR_MSB							
R							
0h							
7	6	5	4	3	2	1	0
AERR_ADDR_MSB							
R							
0h							

Table 14-20003. EMIF_SSCFG_V2A_AERR_LOG2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AERR_ADDR_MSB	R	0h	Address[34:16] of the VBUSM command Reset Source: ctl_smod_g_rst_n

14.6.6.2.20 EMIF_SSCFG_V2A_BUS_TO Register

1 EMIF_SSCFG_V2A_BUS_TO Register (Offset = 9Ch) [reset = FFFFFFh]

VBUSM2AXI Bus Timeout Register

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Table 14-20004. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 009Ch**

Figure 14-6633. EMIF_SSCFG_V2A_BUS_TO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
BUS_TIMER							
R/W							
FFFFFFh							
15	14	13	12	11	10	9	8
BUS_TIMER							
R/W							
FFFFFFh							
7	6	5	4	3	2	1	0
BUS_TIMER							
R/W							
FFFFFFh							

Table 14-20006. EMIF_SSCFG_V2A_BUS_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	BUS_TIMER	R/W	FFFFFFh	AXI bus timeout value. Number of DDR clock cycles after which the VBUSM2AXI bridge times out if a hang on the controller AXI interface is detected. A value of N will be equal to N x 16 clocks. Writing a 0 will disable the timeout feature. Reset Source: ctl_smod_g_rst_n

14.6.6.2.21 EMIF_SSCFG_V2A_INT_RAW_REG Register

1 EMIF_SSCFG_V2A_INT_RAW_REG Register (Offset = A0h) [reset = 0h]

VBUSM2AXI Interrupt Raw Status Register

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Table 14-20007. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 00A0h**

Figure 14-6634. EMIF_SSCFG_V2A_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	RESERVED
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-20009. EMIF_SSCFG_V2A_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR	R/W1TS	0h	Raw status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR	R/W1TS	0h	Raw status of SDRAM ECC 2-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR	R/W1TS	0h	Raw status of SDRAM ECC 1-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR	R/W1TS	0h	Raw status of VBUSM2AXI interrupt for controller AXI interface timeout. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
1	AERR	R/W1TS	0h	Raw status of VBUSM2AXI interrupt for VBUSM address outside the programmed range. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.6.6.2.22 EMIF_SSCFG_V2A_INT_STAT_REG Register

1 EMIF_SSCFG_V2A_INT_STAT_REG Register (Offset = A4h) [reset = 0h]

VBUSM2AXI Interrupt Status Register

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Table 14-20010. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 00A4h**

Figure 14-6635. EMIF_SSCFG_V2A_INT_STAT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	RESERVED
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-20012. EMIF_SSCFG_V2A_INT_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR	R/W1TC	0h	Enabled status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR	R/W1TC	0h	Enabled status of SDRAM ECC 2-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR	R/W1TC	0h	Enabled status of SDRAM ECC 1-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR	R/W1TC	0h	Enabled status of VBUSM2AXI interrupt for controller AXI interface timeout. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-20012. EMIF_SSCFG_V2A_INT_STAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR	R/W1TC	0h	Enabled status of VBUSM2AXI interrupt for VBUSM address outside the programmed range. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.6.6.2.23 EMIF_SSCFG_V2A_INT_SET_REG Register

1 EMIF_SSCFG_V2A_INT_SET_REG Register (Offset = A8h) [reset = 0h]

VBUSM2AXI Interrupt Enable Set Register

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Table 14-20013. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 00A8h

Figure 14-6636. EMIF_SSCFG_V2A_INT_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	RESERVED
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-20015. EMIF_SSCFG_V2A_INT_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC 2-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC 1-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR_EN	R/W1TS	0h	Enable set for VBUSM2AXI interrupt for controller AXI interface timeout. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-20015. EMIF_SSCFG_V2A_INT_SET_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1TS	0h	Enable set for VBUSM2AXI interrupt for VBUSM address outside the programmed range. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.6.6.2.24 EMIF_SSCFG_V2A_INT_CLR_REG Register

1 EMIF_SSCFG_V2A_INT_CLR_REG Register (Offset = ACh) [reset = 0h]

VBUSM2AXI Interrupt Enable Clear Register

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Table 14-20016. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 00ACh**

Figure 14-6637. EMIF_SSCFG_V2A_INT_CLR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	RESERVED
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-20018. EMIF_SSCFG_V2A_INT_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC 2-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC 1-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR_EN	R/W1TC	0h	Enable clear for VBUSM2AXI interrupt for controller AXI interface timeout. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-20018. EMIF_SSCFG_V2A_INT_CLR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1TC	0h	Enable clear for VBUSM2AXI interrupt for VBUSM address outside the programmed range. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.6.6.2.25 EMIF_SSCFG_V2A_EOI_REG Register

1 EMIF_SSCFG_V2A_EOI_REG Register (Offset = B0h) [reset = 0h]

VBUSM2AXI End of Interrupt Register

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Table 14-20019. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 00B0h**

Figure 14-6638. EMIF_SSCFG_V2A_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EOI	
NONE						W	
0h						0h	

Table 14-20021. EMIF_SSCFG_V2A_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	EOI	W	0h	Software End Of Interrupt (EOI) control. Write 0 for aerr/toerr interrupt. Write 1 for ecc1b interrupt. Write 2 for ecc2b interrupt. This field always reads 0 (no EOI memory). Reset Source: ctl_smod_g_rst_n

14.6.6.2.26 EMIF_SSCFG_PERF_CNT_SEL_REG Register

1 EMIF_SSCFG_PERF_CNT_SEL_REG Register (Offset = 100h) [reset = 3020100h]

The Performance Counter Select register is used to select the statistic type to be counted in the corresponding Performance Counter register.

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Table 14-20022. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0100h**

Figure 14-6639. EMIF_SSCFG_PERF_CNT_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		CNT4_SEL					
NONE		R/W					
0h		3h					
23	22	21	20	19	18	17	16
RESERVED		CNT3_SEL					
NONE		R/W					
0h		2h					
15	14	13	12	11	10	9	8
RESERVED		CNT2_SEL					
NONE		R/W					
0h		1h					
7	6	5	4	3	2	1	0
RESERVED		CNT1_SEL					
NONE		R/W					
0h		0h					

Table 14-20024. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

Table 14-20024. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29:24	CNT4_SEL	R/W	3h	Statistic select for Performance Counter 4 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-20024. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	CNT3_SEL	R/W	2h	Statistic select for Performance Counter 3 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-20024. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	CNT2_SEL	R/W	1h	Statistic select for Performance Counter 2 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-20024. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	CNT1_SEL	R/W	0h	Statistic select for Performance Counter 1 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n

14.6.6.2.27 EMIF_SSCFG_PERF_CNT1_REG Register

1 EMIF_SSCFG_PERF_CNT1_REG Register (Offset = 104h) [reset = 0h]

Performance Counter 1 Register

Return to Summary Table

Table 14-20025. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0104h**

Figure 14-6640. EMIF_SSCFG_PERF_CNT1_REG Name Register

31	30	29	28	27	26	25	24
CNT1							
R							
0h							
23	22	21	20	19	18	17	16
CNT1							
R							
0h							
15	14	13	12	11	10	9	8
CNT1							
R							
0h							
7	6	5	4	3	2	1	0
CNT1							
R							
0h							

Table 14-20027. EMIF_SSCFG_PERF_CNT1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT1	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.6.6.2.28 EMIF_SSCFG_PERF_CNT2_REG Register

1 EMIF_SSCFG_PERF_CNT2_REG Register (Offset = 108h) [reset = 0h]

Performance Counter 2 Register

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Table 14-20028. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0108h**

Figure 14-6641. EMIF_SSCFG_PERF_CNT2_REG Name Register

31	30	29	28	27	26	25	24
CNT2							
R							
0h							
23	22	21	20	19	18	17	16
CNT2							
R							
0h							
15	14	13	12	11	10	9	8
CNT2							
R							
0h							
7	6	5	4	3	2	1	0
CNT2							
R							
0h							

Table 14-20030. EMIF_SSCFG_PERF_CNT2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT2	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.6.6.2.29 EMIF_SSCFG_PERF_CNT3_REG Register

1 EMIF_SSCFG_PERF_CNT3_REG Register (Offset = 10Ch) [reset = 0h]

Performance Counter 3 Register

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Table 14-20031. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 010Ch**

Figure 14-6642. EMIF_SSCFG_PERF_CNT3_REG Name Register

31	30	29	28	27	26	25	24
CNT3							
R							
0h							
23	22	21	20	19	18	17	16
CNT3							
R							
0h							
15	14	13	12	11	10	9	8
CNT3							
R							
0h							
7	6	5	4	3	2	1	0
CNT3							
R							
0h							

Table 14-20033. EMIF_SSCFG_PERF_CNT3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT3	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.6.6.2.30 EMIF_SSCFG_PERF_CNT4_REG Register

1 EMIF_SSCFG_PERF_CNT4_REG Register (Offset = 110h) [reset = 0h]

Performance Counter 4 Register

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Table 14-20034. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0110h**

Figure 14-6643. EMIF_SSCFG_PERF_CNT4_REG Name Register

31	30	29	28	27	26	25	24
CNT4							
R							
0h							
23	22	21	20	19	18	17	16
CNT4							
R							
0h							
15	14	13	12	11	10	9	8
CNT4							
R							
0h							
7	6	5	4	3	2	1	0
CNT4							
R							
0h							

Table 14-20036. EMIF_SSCFG_PERF_CNT4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT4	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.6.6.2.31 EMIF_SSCFG_ECC_CTRL_REG Register

1 EMIF_SSCFG_ECC_CTRL_REG Register (Offset = 120h) [reset = 0h]

ECC Control Register

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Table 14-20037. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0120h**

Figure 14-6644. EMIF_SSCFG_ECC_CTRL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">COR_ECC_THRESH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>WR_ALLOC</td><td>RESERVED</td><td>ECC_CK</td><td>RMW_EN</td><td>ECC_EN</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-20039. EMIF_SSCFG_ECC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	COR_ECC_THRESH	R/W	0h	Threshold for 1-bit ECC errors in multiple data words in an SDRAM burst that create an uncorrected error fault indication. Value of 0/1 means 2 or more 1-bit errors in multiple data words will result in an uncorrected error fault indication, value of 2 means 3 or more 1-bit errors will result in an uncorrected error fault indication, and so on. Value of 8 or greater disables this feature. This field must always be kept at default, and only changed for debug. Reset Source: ctl_smod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	WR_ALLOC	R/W	0h	When set to 1, an unassigned ECC cache-line will be allocated for a write with routeID that do not match any of the mapped routeID's. Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	ECC_CK	R/W	0h	Set 1 to enable ECC verification for read accesses when ecc_en=1. The value of this field is ignored when ecc_en=0. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

Table 14-20039. EMIF_SSCFG_ECC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RMW_EN	R/W	0h	Read modify write enable. Set 1 to enable RMW functionality for sub-quanta accesses when ecc_en=1. This bit must be set to 1 if ecc_en is set to a 1 to ensure subquanta accesses to DRAM do not result in ECC errors. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n
0	ECC_EN	R/W	0h	DRAM ECC enable. Setting a 1 causes ECC to be written to DRAM. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.32 EMIF_SSCFG_ECC_RID_INDX_REG Register

1 EMIF_SSCFG_ECC_RID_INDX_REG Register (Offset = 124h) [reset = 0h]

ECC Cache RouteID Index Register

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Table 14-20040. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0124h**

Figure 14-6645. EMIF_SSCFG_ECC_RID_INDX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		ECCRID_ADR					
NONE		R/W					
0h		0h					

Table 14-20042. EMIF_SSCFG_ECC_RID_INDX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ECCRID_ADR	R/W	0h	This index specifies the ECC cache entry number that the eccrid_val is mapped to. Reset Source: ctl_smod_g_rst_n

14.6.6.2.33 EMIF_SSCFG_ECC_RID_VAL_REG Register

1 EMIF_SSCFG_ECC_RID_VAL_REG Register (Offset = 128h) [reset = 0h]

ECC Cache RouteID Write Value Register

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Table 14-20043. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 0128h**

Figure 14-6646. EMIF_SSCFG_ECC_RID_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ECCRID_VAL_VLD	RESERVED			ECCRID_VAL			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
ECCRID_VAL							
R/W							
0h							

Table 14-20045. EMIF_SSCFG_ECC_RID_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ECCRID_VAL_VLD	R/W	0h	A 1 in this field indicates that value in eccrid_val is valid. Reset Source: ctl_smod_g_rst_n
14:12	RESERVED	NONE	0h	Reserved
11:0	ECCRID_VAL	R/W	0h	RouteID value written or read. Reset Source: ctl_smod_g_rst_n

14.6.6.2.34 EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register (Offset = 130h) [reset = FFFFh]

ECC Range 0 Start Address Register

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Table 14-20046. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0130h**

Figure 14-6647. EMIF_SSCFG_ECC_R0_STR_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ECC_STR_ADR_0		
NONE					R/W		
0h					FFFFh		
15	14	13	12	11	10	9	8
ECC_STR_ADR_0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ECC_STR_ADR_0							
R/W							
FFFFh							

Table 14-20048. EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_STR_ADR_0	R/W	FFFFh	Start caddress[34:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.35 EMIF_SSCFG_ECC_R0_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R0_END_ADDR_REG Register (Offset = 134h) [reset = 0h]

ECC Range 0 End Address Register

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Table 14-20049. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0134h**

Figure 14-6648. EMIF_SSCFG_ECC_R0_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					ECC_END_ADR_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECC_END_ADR_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_END_ADR_0							
R/W							
0h							

Table 14-20051. EMIF_SSCFG_ECC_R0_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_END_ADR_0	R/W	0h	End caddress[34:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.36 EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register (Offset = 138h) [reset = FFFFh]

ECC Range 1 Start Address Register

Return to Summary Table

Table 14-20052. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0138h**

Figure 14-6649. EMIF_SSCFG_ECC_R1_STR_ADDR_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ECC_STR_ADR_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ECC_STR_ADR_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_STR_ADR_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-20054. EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_STR_ADR_1	R/W	FFFFh	Start caddress[34:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.37 EMIF_SSCFG_ECC_R1_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R1_END_ADDR_REG Register (Offset = 13Ch) [reset = 0h]

ECC Range 1 End Address Register

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Table 14-20055. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 013Ch

Figure 14-6650. EMIF_SSCFG_ECC_R1_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					ECC_END_ADR_1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECC_END_ADR_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_END_ADR_1							
R/W							
0h							

Table 14-20057. EMIF_SSCFG_ECC_R1_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_END_ADR_1	R/W	0h	End caddress[34:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.38 EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register (Offset = 140h) [reset = FFFFh]

ECC Range 2 Start Address Register

Return to Summary Table

Table 14-20058. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0140h**

Figure 14-6651. EMIF_SSCFG_ECC_R2_STR_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					ECC_STR_ADR_2		
NONE					R/W		
0h					FFFFh		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECC_STR_ADR_2							
R/W							
FFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_STR_ADR_2							
R/W							
FFFFh							

Table 14-20060. EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_STR_ADR_2	R/W	FFFFh	Start caddress[34:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.39 EMIF_SSCFG_ECC_R2_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R2_END_ADDR_REG Register (Offset = 144h) [reset = 0h]

ECC Range 2 End Address Register

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Table 14-20061. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0144h**

Figure 14-6652. EMIF_SSCFG_ECC_R2_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ECC_END_ADR_2		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
ECC_END_ADR_2							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_END_ADR_2							
R/W							
0h							

Table 14-20063. EMIF_SSCFG_ECC_R2_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	ECC_END_ADR_2	R/W	0h	End caddress[34:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.6.6.2.40 EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register (Offset = 150h) [reset = 0h]

ECC 1-Bit Error Count Register

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Table 14-20064. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 0150h

Figure 14-6653. EMIF_SSCFG_ECC_1B_ERR_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ECC_1B_ERR_CNT							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_CNT							
R/W1TC							
0h							

Table 14-20066. EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ECC_1B_ERR_CNT	R/W1TC	0h	16-bit counter that displays number of 1-bit ECC errors on SDRAM data. Writing a 0x1 will clear this count. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.6.6.2.41 EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register (Offset = 154h) [reset = 0h]

ECC 1-Bit Error Threshold Register

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Table 14-20067. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0154h**

Figure 14-6654. EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ECC_1B_ERR_THRSH							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_THRSH							
R/W							
0h							

Table 14-20069. EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ECC_1B_ERR_THRSH	R/W	0h	ECC 1-bit error threshold. The bridge will generate an interrupt when the ECC 1-bit error count is equal to or greater than this threshold. A value of 0 will disable the generation of interrupt. Reset Source: ctl_smod_g_rst_n

14.6.6.2.42 EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register (Offset = 158h) [reset = 0h]

ECC 1-Bit Error Address Log Register

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Table 14-20070. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0158h**

Figure 14-6655. EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	ECC_1B_ERR_ADR						
NONE	R/W1TC						
0h	0h						
23	22	21	20	19	18	17	16
ECC_1B_ERR_ADR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
ECC_1B_ERR_ADR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_ADR							
R/W1TC							
0h							

Table 14-20072. EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	ECC_1B_ERR_ADR	R/W1TC	0h	ECC 1-bit error address. 32-byte aligned address that had the 1-bit ECC error. This field displays the first address logged in the 2 deep logging FIFO. Writing a 0x1 will pop the top element of the FIFO. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.6.6.2.43 EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register (Offset = 15Ch) [reset = 0h]

ECC 1-Bit Error Mask Log Register

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Table 14-20073. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 015Ch**

Figure 14-6656. EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_MSK							
R							
0h							

Table 14-20075. EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ECC_1B_ERR_MSK	R	0h	ECC 1-bit error mask. Mask for the 64-byte data block that had the 1-bit ECC errors. Each bit represents an ECC quanta (8 bytes) in the 64-byte data block starting at address specified by ecc_1b_err_adr. Value of 1 on the bit represents an error in that particular 8 bytes. This field displays the first mask logged in the 2 deep logging FIFO along with the ecc_1b_err_adr. The same mechanism used to pop ecc_1b_err_adr is used to pop this field. Reset Source: ctl_smod_g_rst_n

14.6.6.2.44 EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register

1 EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register (Offset = 160h) [reset = 0h]

ECC 2-Bit Error Address Log Register

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Table 14-20076. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0160h**

Figure 14-6657. EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	ECC_2B_ERR_ADR						
NONE	R/W1TC						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECC_2B_ERR_ADR							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECC_2B_ERR_ADR							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_2B_ERR_ADR							
R/W1TC							
0h							

Table 14-20078. EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	ECC_2B_ERR_ADR	R/W1TC	0h	ECC 2-bit error address. 32-byte aligned address that had the 2-bit ECC error. Writing a 0x1 will clear this field and the ecc_2b_err_msk field. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.6.6.2.45 EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register

1 EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register (Offset = 164h) [reset = 0h]

ECC 2-Bit Error Mask Log Register

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Table 14-20079. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0164h**

Figure 14-6658. EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ECC_2B_ERR_MSK							
R							
0h							

Table 14-20081. EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ECC_2B_ERR_MSK	R	0h	ECC 2-bit error mask. Mask for the 64-byte data block that had the 2-bit ECC errors. Each bit represents an ECC quanta (8 bytes) in the 64-byte data block starting at address specified by ecc_2b_err_adr. Value of 1 on the bit represents an error in that particular 8 bytes. Reset Source: ctl_smod_g_rst_n

14.6.6.2.46 EMIF_SSCFG_PHY_TEST_CTRL1_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL1_REG Register (Offset = 184h) [reset = FFFFFFC0h]

PHY Test Control 1 Register

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Table 14-20082. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0184h**

Figure 14-6659. EMIF_SSCFG_PHY_TEST_CTRL1_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_TSEL_RD_SEL							
R/W							
FFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_TSEL_WR_SEL							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_TSEL_ADDR_SEL							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_TSEL_ADDR_EN	JTAG_DATAOUT_TSEL_EN	JTAG_ENABLE_TERM	JTAG_ENABLE_OE	JTAG_ENABLE_IE	JTAG_ENABLE_DRIVE	JTAG_ENABLE	HVM_TEST_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	0h	0h	0h	0h	0h	0h

Table 14-20084. EMIF_SSCFG_PHY_TEST_CTRL1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	JTAG_DATAOUT_TSEL_RD_SEL	R/W	FFh	Controls jtag_dataout_tsel_rd_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
23:16	JTAG_DATAOUT_TSEL_WR_SEL	R/W	FFh	Controls jtag_dataout_tsel_wr_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:8	JTAG_DATAOUT_TSEL_ADDR_SEL	R/W	FFh	Controls jtag_dataout_tsel_addr_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_TSEL_ADDR_EN	R/W	1h	Controls jtag_dataout_tsel_addr_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_TSEL_EN	R/W	1h	Controls jtag_dataout_tsel_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5	JTAG_ENABLE_TERM	R/W	0h	Controls jtag_enable_term port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20084. EMIF_SSCFG_PHY_TEST_CTRL1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	JTAG_ENABLE_OE	R/W	0h	Controls jtag_enable_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_ENABLE_IE	R/W	0h	Controls jtag_enable_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2	JTAG_ENABLE_DRIVE	R/W	0h	Controls jtag_enable_drive port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
1	JTAG_ENABLE	R/W	0h	Controls jtag_enable port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	HVM_TEST_EN	R/W	0h	1=Enable HVM test functionality. 0=Disable HVM test functionality. Setting a 1 will enable control of PHY ports using PHY Test Control registers, and will enable 50 MHz clock to the jtag_dataout_pad_dslice_io_cfg[1], jtag_dataout_pad_acs_io_cfg[1], and jtag_dataout_pad_adr_io_cfg[1] ports on the PHY. Reset Source: ctl_smod_g_rst_n

14.6.6.2.47 EMIF_SSCFG_PHY_TEST_CTRL2_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL2_REG Register (Offset = 188h) [reset = 215FC000h]

PHY Test Control 2 Register

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Table 14-20085. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0188h**

Figure 14-6660. EMIF_SSCFG_PHY_TEST_CTRL2_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_PAD_ADR_IO_CFG0	JTAG_DATAOUT_PAD_ACS_IO_CFG0	JTAG_DATAOUT_PAD_DSLICE_IO_CFG2	JTAG_DATAOUT_PAD_DSLICE_IO_CFG0	JTAG_DATAOUT_ATB_EN	JTAG_DATAOUT_VREF_CTRL_DQ		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	1h	0h	0h	2BFh		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_VREF_CTRL_DQ							
R/W							
2BFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_VREF_CTRL_DQ	JTAG_DATAOUT_PHY_RX_CAL_CODE						
R/W	R/W						
2BFh	100h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_PHY_RX_CAL_CODE		JTAG_DATAOUT_PHY_DSLICE_PAD_RX_CTLE_SETTING					
R/W		R/W					
100h		0h					

Table 14-20087. EMIF_SSCFG_PHY_TEST_CTRL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_PAD_ADR_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_adr_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PAD_ACS_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_acs_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29	JTAG_DATAOUT_PAD_DSLICE_IO_CFG2	R/W	1h	Controls jtag_dataout_pad_dslice_io_cfg[2] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
28	JTAG_DATAOUT_PAD_DSLICE_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_dslice_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27	JTAG_DATAOUT_ATB_EN	R/W	0h	Controls jtag_dataout_atb_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20087. EMIF_SSCFG_PHY_TEST_CTRL2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:15	JTAG_DATAOUT_VREF_CTRL_DQ	R/W	2BFh	Controls jtag_dataout_vref_ctrl_dq port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
14:6	JTAG_DATAOUT_PHY_RX_CAL_CODE	R/W	100h	Controls jtag_dataout_phy_rx_cal_code port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:0	JTAG_DATAOUT_PHY_DSLICE_PAD_RX_CTLE_SETTING	R/W	0h	Controls jtag_dataout_phy_dslice_pad_rx_ctle_setting port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.48 EMIF_SSCFG_PHY_TEST_CTRL3_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL3_REG Register (Offset = 18Ch) [reset = 0h]

PHY Test Control 3 Register

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Table 14-20088. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 018Ch**

Figure 14-6661. EMIF_SSCFG_PHY_TEST_CTRL3_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ATB_CTRL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_ATB_CTRL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_PAD_ATB_CTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_PAD_ATB_CTRL							
R/W							
0h							

Table 14-20090. EMIF_SSCFG_PHY_TEST_CTRL3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	JTAG_DATAOUT_ATB_CTRL	R/W	0h	Controls jtag_dataout_atb_ctrl port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAOUT_PAD_ATB_CTRL	R/W	0h	Controls jtag_dataout_pad_atb_ctrl port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.49 EMIF_SSCFG_PHY_TEST_CTRL4_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL4_REG Register (Offset = 190h) [reset = 0h]

PHY Test Control 4 Register

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Table 14-20091. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0190h**

Figure 14-6662. EMIF_SSCFG_PHY_TEST_CTRL4_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>JTAG_DATAOUT_ERROR_N_OE</td><td>JTAG_DATAOUT_PARITY_IN_OE</td><td colspan="2">JTAG_DATAOUT_ODT_OE</td><td colspan="4">JTAG_DATAOUT_ADDRESS_OE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_ADDRESS_OE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">JTAG_DATAOUT_ADDRESS_OE</td><td colspan="2">JTAG_DATAOUT_BANK_OE</td><td colspan="2">JTAG_DATAOUT_BG_OE</td><td>JTAG_DATAOUT_WE_N_OE</td><td>JTAG_DATAOUT_CAS_N_OE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>JTAG_DATAOUT_RAS_N_OE</td><td>JTAG_DATAOUT_ACT_N_OE</td><td colspan="2">JTAG_DATAOUT_CS_N_OE</td><td>JTAG_DATAOUT_MEM_CLK_0_OE</td><td colspan="2">JTAG_DATAOUT_CKE_OE</td><td>JTAG_DATAOUT_RESET_N_OE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-20093. EMIF_SSCFG_PHY_TEST_CTRL4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N_OE	R/W	0h	Controls jtag_dataout_error_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN_OE	R/W	0h	Controls jtag_dataout_parity_in_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT_OE	R/W	0h	Controls jtag_dataout_odt_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS_OE	R/W	0h	Controls jtag_dataout_address_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK_OE	R/W	0h	Controls jtag_dataout_bank_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20093. EMIF_SSCFG_PHY_TEST_CTRL4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	JTAG_DATAOUT_BG_OE	R/W	0h	Controls jtag_dataout_bg_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAOUT_WE_N_OE	R/W	0h	Controls jtag_dataout_we_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N_OE	R/W	0h	Controls jtag_dataout_cas_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N_OE	R/W	0h	Controls jtag_dataout_ras_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N_OE	R/W	0h	Controls jtag_dataout_act_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N_OE	R/W	0h	Controls jtag_dataout_cs_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0_OE	R/W	0h	Controls jtag_dataout_mem_clk_0_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE_OE	R/W	0h	Controls jtag_dataout_cke_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N_OE	R/W	0h	Controls jtag_dataout_reset_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.50 EMIF_SSCFG_PHY_TEST_CTRL5_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL5_REG Register (Offset = 194h) [reset = 0h]

PHY Test Control 5 Register

Return to Summary Table

Table 14-20094. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0194h**

Figure 14-6663. EMIF_SSCFG_PHY_TEST_CTRL5_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_DATA_OE							
R/W							
0h							
23	22	21	20	19	18	17	16
JTAG_DATAOUT_DATA_OE							
R/W							
0h							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_DATA_OE							
R/W							
0h							
7	6	5	4	3	2	1	0
JTAG_DATAOUT_DATA_OE							
R/W							
0h							

Table 14-20096. EMIF_SSCFG_PHY_TEST_CTRL5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_DATAOUT_DATA_OE	R/W	0h	Controls jtag_dataout_data_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.51 EMIF_SSCFG_PHY_TEST_CTRL6_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL6_REG Register (Offset = 198h) [reset = 0h]

PHY Test Control 6 Register

Return to Summary Table

Table 14-20097. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 0198h**

Figure 14-6664. EMIF_SSCFG_PHY_TEST_CTRL6_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ERROR_N	JTAG_DATAOUT_PARITY_IN	JTAG_DATAOUT_ODT		JTAG_DATAOUT_ADDRESS			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_ADDRESS		JTAG_DATAOUT_BANK		JTAG_DATAOUT_BG		JTAG_DATAOUT_WE_N	JTAG_DATAOUT_CAS_N
R/W		R/W		R/W		R/W	R/W
0h		0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_RAS_N	JTAG_DATAOUT_ACT_N	JTAG_DATAOUT_CS_N		JTAG_DATAOUT_MEM_CLK_0	JTAG_DATAOUT_CKE		JTAG_DATAOUT_RESET_N
R/W	R/W	R/W		R/W	R/W		R/W
0h	0h	0h		0h	0h		0h

Table 14-20099. EMIF_SSCFG_PHY_TEST_CTRL6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N	R/W	0h	Controls jtag_dataout_error_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN	R/W	0h	Controls jtag_dataout_parity_in port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT	R/W	0h	Controls jtag_dataout_odt port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS	R/W	0h	Controls jtag_dataout_address port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK	R/W	0h	Controls jtag_dataout_bank port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
11:10	JTAG_DATAOUT_BG	R/W	0h	Controls jtag_dataout_bg port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20099. EMIF_SSCFG_PHY_TEST_CTRL6_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	JTAG_DATAOUT_WE_N	R/W	0h	Controls jtag_dataout_we_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N	R/W	0h	Controls jtag_dataout_cas_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N	R/W	0h	Controls jtag_dataout_ras_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N	R/W	0h	Controls jtag_dataout_act_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N	R/W	0h	Controls jtag_dataout_cs_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0	R/W	0h	Controls jtag_dataout_mem_clk_0 port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE	R/W	0h	Controls jtag_dataout_cke port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N	R/W	0h	Controls jtag_dataout_reset_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.52 EMIF_SSCFG_PHY_TEST_CTRL7_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL7_REG Register (Offset = 19Ch) [reset = 0h]

PHY Test Control 7 Register

Return to Summary Table

Table 14-20100. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 019Ch**

Figure 14-6665. EMIF_SSCFG_PHY_TEST_CTRL7_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20102. EMIF_SSCFG_PHY_TEST_CTRL7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_DATAOUT_DATA	R/W	0h	Controls jtag_dataout_data port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.53 EMIF_SSCFG_PHY_TEST_CTRL8_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL8_REG Register (Offset = 1A0h) [reset = FFFFFFFFh]

PHY Test Control 8 Register

Return to Summary Table

Table 14-20103. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01A0h**

Figure 14-6666. EMIF_SSCFG_PHY_TEST_CTRL8_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ERROR_N_IE	JTAG_DATAOUT_PARITY_IN_IE	JTAG_DATAOUT_ODT_IE		JTAG_DATAOUT_ADDRESS_IE			
R/W	R/W	R/W		R/W			
1h	1h	3h		3FFFh			

23	22	21	20	19	18	17	16
JTAG_DATAOUT_ADDRESS_IE							
R/W							
3FFFh							

15	14	13	12	11	10	9	8
JTAG_DATAOUT_ADDRESS_IE		JTAG_DATAOUT_BANK_IE		JTAG_DATAOUT_BG_IE		JTAG_DATAOUT_WE_N_IE	JTAG_DATAOUT_CAS_N_IE
R/W		R/W		R/W		R/W	R/W
3FFFh		3h		3h		1h	1h

7	6	5	4	3	2	1	0
JTAG_DATAOUT_RAS_N_IE	JTAG_DATAOUT_ACT_N_IE	JTAG_DATAOUT_CS_N_IE		JTAG_DATAOUT_MEM_CLK_0_IE	JTAG_DATAOUT_CKE_IE		JTAG_DATAOUT_RESET_N_IE
R/W	R/W	R/W		R/W	R/W		R/W
1h	1h	3h		1h	3h		1h

Table 14-20105. EMIF_SSCFG_PHY_TEST_CTRL8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N_IE	R/W	1h	Controls jtag_dataout_error_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN_IE	R/W	1h	Controls jtag_dataout_parity_in_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT_IE	R/W	3h	Controls jtag_dataout_odt_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS_IE	R/W	3FFFh	Controls jtag_dataout_address_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK_IE	R/W	3h	Controls jtag_dataout_bank_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20105. EMIF_SSCFG_PHY_TEST_CTRL8_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	JTAG_DATAOUT_BG_IE	R/W	3h	Controls jtag_dataout_bg_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAOUT_WE_N_IE	R/W	1h	Controls jtag_dataout_we_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N_IE	R/W	1h	Controls jtag_dataout_cas_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N_IE	R/W	1h	Controls jtag_dataout_ras_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N_IE	R/W	1h	Controls jtag_dataout_act_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N_IE	R/W	3h	Controls jtag_dataout_cs_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0_IE	R/W	1h	Controls jtag_dataout_mem_clk_0_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE_IE	R/W	3h	Controls jtag_dataout_cke_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N_IE	R/W	1h	Controls jtag_dataout_reset_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.54 EMIF_SSCFG_PHY_TEST_CTRL9_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL9_REG Register (Offset = 1A4h) [reset = FFFFFFFFh]

PHY Test Control 9 Register

Return to Summary Table

Table 14-20106. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01A4h**

Figure 14-6667. EMIF_SSCFG_PHY_TEST_CTRL9_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_DATA_IE							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
JTAG_DATAOUT_DATA_IE							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_DATA_IE							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
JTAG_DATAOUT_DATA_IE							
R/W							
FFFFFFFFh							

Table 14-20108. EMIF_SSCFG_PHY_TEST_CTRL9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_DATAOUT_DATA_IE	R/W	FFFFFFFFh	Controls jtag_dataout_data_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.55 EMIF_SSCFG_PHY_TEST_CTRL10_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL10_REG Register (Offset = 1A8h) [reset = Fh]

PHY Test Control 10 Register

Return to Summary Table

Table 14-20109. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01A8h**

Figure 14-6668. EMIF_SSCFG_PHY_TEST_CTRL10_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HVM_CLK_DIV							
R/W							
Fh							

Table 14-20111. EMIF_SSCFG_PHY_TEST_CTRL10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HVM_CLK_DIV	R/W	Fh	Divfactor to divide ddrss_ddr_pll_clk to generate PCLK for HVM tests when ddrss_bs_mode=0 and hvm_test_en=1. 0=div by 1, 1=div by 2, and so on. Reset Source: ctl_smod_g_rst_n

14.6.6.2.56 EMIF_SSCFG_PHY_TEST_CTRL11_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL11_REG Register (Offset = 1ACh) [reset = F000F00h]

PHY Test Control 11 Register

Return to Summary Table

Table 14-20112. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01ACh**

Figure 14-6669. EMIF_SSCFG_PHY_TEST_CTRL11_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				JTAG_DATAOUT_DQS_IE			
NONE				R/W			
0h				Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_DQS				JTAG_DATAOUT_DQS_OE			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				JTAG_DATAOUT_DM_IE			
NONE				R/W			
0h				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_DM				JTAG_DATAOUT_DM_OE			
R/W				R/W			
0h				0h			

Table 14-20114. EMIF_SSCFG_PHY_TEST_CTRL11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	JTAG_DATAOUT_DQS_IE	R/W	Fh	Controls jtag_dataout_dqs_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
23:20	JTAG_DATAOUT_DQS	R/W	0h	Controls jtag_dataout_dqs port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
19:16	JTAG_DATAOUT_DQS_OE	R/W	0h	Controls jtag_dataout_dqs_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	JTAG_DATAOUT_DM_IE	R/W	Fh	Controls jtag_dataout_dm_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7:4	JTAG_DATAOUT_DM	R/W	0h	Controls jtag_dataout_dm port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-20114. EMIF_SSCFG_PHY_TEST_CTRL11_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	JTAG_DATAOUT_DM_OE	R/W	0h	Controls jtag_dataout_dm_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.57 EMIF_SSCFG_PHY_TEST_CTRL12_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL12_REG Register (Offset = 1B0h) [reset = 0h]

PHY Test Control 12 Register

Return to Summary Table

Table 14-20115. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01B0h**

Figure 14-6670. EMIF_SSCFG_PHY_TEST_CTRL12_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_PHY_DSLICE_PAD_BOOSTPN_SETTING							
R/W							
0h							
7	6	5	4	3	2	1	0
JTAG_DATAOUT_PHY_DSLICE_PAD_BOOSTPN_SETTING							
R/W							
0h							

Table 14-20117. EMIF_SSCFG_PHY_TEST_CTRL12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	JTAG_DATAOUT_PHY_DSLICE_PAD_BOOSTPN_SETTING	R/W	0h	Controls jtag_dataout_phy_dslice_pad_boostpn_setting port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.6.6.2.58 EMIF_SSCFG_PHY_TEST_STAT1_REG Register

1 EMIF_SSCFG_PHY_TEST_STAT1_REG Register (Offset = 1C0h) [reset = 0h]

PHY Test Status 1 Register

Return to Summary Table

Table 14-20118. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01C0h**

Figure 14-6671. EMIF_SSCFG_PHY_TEST_STAT1_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAIN_ERROR_N	JTAG_DATAIN_PARITY_IN	JTAG_DATAIN_ODT		JTAG_DATAIN_ADDRESS			
R	R	R		R			
0h	0h	0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAIN_ADDRESS							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAIN_ADDRESS		JTAG_DATAIN_BANK		JTAG_DATAIN_BG		JTAG_DATAIN_WE_N	JTAG_DATAIN_CAS_N
R		R		R		R	R
0h		0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAIN_RAS_N	JTAG_DATAIN_ACT_N	JTAG_DATAIN_CS_N		JTAG_DATAIN_MEM_CLK_0	JTAG_DATAIN_CKE		JTAG_DATAIN_RESET_N
R	R	R		R	R		R
0h	0h	0h		0h	0h		0h

Table 14-20120. EMIF_SSCFG_PHY_TEST_STAT1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAIN_ERROR_N	R	0h	Displays value of jtag_datain_error_n port on the PHY. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAIN_PARITY_IN	R	0h	Displays value of jtag_datain_parity_in port on the PHY. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAIN_ODT	R	0h	Displays value of jtag_datain_odt port on the PHY. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAIN_ADDRESS	R	0h	Displays value of jtag_datain_address port on the PHY. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAIN_BANK	R	0h	Displays value of jtag_datain_bank port on the PHY. Reset Source: ctl_smod_g_rst_n
11:10	JTAG_DATAIN_BG	R	0h	Displays value of jtag_datain_bg port on the PHY. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAIN_WE_N	R	0h	Displays value of jtag_datain_we_n port on the PHY. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAIN_CAS_N	R	0h	Displays value of jtag_datain_cas_n port on the PHY. Reset Source: ctl_smod_g_rst_n

Table 14-20120. EMIF_SSCFG_PHY_TEST_STAT1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	JTAG_DATAIN_RAS_N	R	0h	Displays value of jtag_datain_ras_n port on the PHY. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAIN_ACT_N	R	0h	Displays value of jtag_datain_act_n port on the PHY. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAIN_CS_N	R	0h	Displays value of jtag_datain_cs_n port on the PHY. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAIN_MEM_CLK_0	R	0h	Displays value of jtag_datain_mem_clk_0 port on the PHY. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAIN_CKE	R	0h	Displays value of jtag_datain_cke port on the PHY. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAIN_RESET_N	R	0h	Displays value of jtag_datain_reset_n port on the PHY. Reset Source: ctl_smod_g_rst_n

14.6.6.2.59 EMIF_SSCFG_PHY_TEST_STAT2_REG Register

1 EMIF_SSCFG_PHY_TEST_STAT2_REG Register (Offset = 1C4h) [reset = 0h]

PHY Test Status 2 Register

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Table 14-20121. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01C4h**

Figure 14-6672. EMIF_SSCFG_PHY_TEST_STAT2_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">JTAG_DATAIN_DATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">JTAG_DATAIN_DATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">JTAG_DATAIN_DATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">JTAG_DATAIN_DATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20123. EMIF_SSCFG_PHY_TEST_STAT2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_DATAIN_DATA	R	0h	Displays value of jtag_datain_data port on the PHY. Reset Source: ctl_smod_g_rst_n

14.6.6.2.60 EMIF_SSCFG_PHY_TEST_STAT3_REG Register

1 EMIF_SSCFG_PHY_TEST_STAT3_REG Register (Offset = 1C8h) [reset = 0h]

PHY Test Status 3 Register

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Table 14-20124. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 01C8h**

Figure 14-6673. EMIF_SSCFG_PHY_TEST_STAT3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				JTAG_DATAIN_DQS			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				JTAG_DATAIN_DM			
NONE				R			
0h				0h			

Table 14-20126. EMIF_SSCFG_PHY_TEST_STAT3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	JTAG_DATAIN_DQS	R	0h	Displays value of jtag_datain_dqs port on the PHY. Reset Source: ctl_smod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	JTAG_DATAIN_DM	R	0h	Displays value of jtag_datain_dm port on the PHY. Reset Source: ctl_smod_g_rst_n

14.6.6.2.61 EMIF_CTLCFG_DENALI_CTL_0 Register

1 EMIF_CTLCFG_DENALI_CTL_0 Register (Offset = 0h) [reset = 10460000h]

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Table 14-20127. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8000h**

Figure 14-6674. EMIF_CTLCFG_DENALI_CTL_0 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_ID							
R							
1046h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CONTROLLER_ID							
R							
1046h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				DRAM_CLASS			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							START
NONE							R/W
0h							0h

Table 14-20129. EMIF_CTLCFG_DENALI_CTL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CONTROLLER_ID	R	1046h	Holds the controller product id number. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	DRAM_CLASS	R/W	0h	Defines the class of DRAM memory which is connected to the controller. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	START	R/W	0h	Initiate command processing in the controller. Set to 1 to initiate. Reset Source: ctl_amod_g_rst_n

14.6.6.2.62 EMIF_CTLCFG_DENALI_CTL_1 Register

1 EMIF_CTLCFG_DENALI_CTL_1 Register (Offset = 4h) [reset = 617AD652h]

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Table 14-20130. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8004h**

Figure 14-6675. EMIF_CTLCFG_DENALI_CTL_1 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_VERSION_0							
R							
617AD652h							
23	22	21	20	19	18	17	16
CONTROLLER_VERSION_0							
R							
617AD652h							
15	14	13	12	11	10	9	8
CONTROLLER_VERSION_0							
R							
617AD652h							
7	6	5	4	3	2	1	0
CONTROLLER_VERSION_0							
R							
617AD652h							

Table 14-20132. EMIF_CTLCFG_DENALI_CTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLLER_VERSION_0	R	617AD652h	Holds the controller version id. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.63 EMIF_CTLCFG_DENALI_CTL_2 Register

1 EMIF_CTLCFG_DENALI_CTL_2 Register (Offset = 8h) [reset = 409E81h]

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Table 14-20133. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8008h**

Figure 14-6676. EMIF_CTLCFG_DENALI_CTL_2 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_VERSION_1							
R							
409E81h							
23	22	21	20	19	18	17	16
CONTROLLER_VERSION_1							
R							
409E81h							
15	14	13	12	11	10	9	8
CONTROLLER_VERSION_1							
R							
409E81h							
7	6	5	4	3	2	1	0
CONTROLLER_VERSION_1							
R							
409E81h							

Table 14-20135. EMIF_CTLCFG_DENALI_CTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLLER_VERSION_1	R	409E81h	Holds the controller version id. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.64 EMIF_CTLCFG_DENALI_CTL_3 Register

1 EMIF_CTLCFG_DENALI_CTL_3 Register (Offset = Ch) [reset = 40020A12h]

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Table 14-20136. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 800Ch**

Figure 14-6677. EMIF_CTLCFG_DENALI_CTL_3 Name Register

31	30	29	28	27	26	25	24
READ_DATA_FIFO_DEPTH							
R							
40h							
23	22	21	20	19	18	17	16
RESERVED						MAX_CS_REG	
NONE						R	
0h						2h	
15	14	13	12	11	10	9	8
RESERVED				MAX_COL_REG			
NONE				R			
0h				Ah			
7	6	5	4	3	2	1	0
RESERVED			MAX_ROW_REG				
NONE			R				
0h			12h				

Table 14-20138. EMIF_CTLCFG_DENALI_CTL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	READ_DATA_FIFO_DEPTH	R	40h	Reports the depth of the controller core read data queue. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	MAX_CS_REG	R	2h	Holds the maximum number of chip selects available. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MAX_COL_REG	R	Ah	Holds the maximum width of column address in DRAMs. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	MAX_ROW_REG	R	12h	Holds the maximum width of memory address bus. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.65 EMIF_CTLCFG_DENALI_CTL_4 Register

1 EMIF_CTLCFG_DENALI_CTL_4 Register (Offset = 10h) [reset = 52006h]

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Table 14-20139. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8010h**

Figure 14-6678. EMIF_CTLCFG_DENALI_CTL_4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
WRITE_DATA_FIFO_PTR_WIDTH							
R							
5h							
15	14	13	12	11	10	9	8
WRITE_DATA_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
READ_DATA_FIFO_PTR_WIDTH							
R							
6h							

Table 14-20141. EMIF_CTLCFG_DENALI_CTL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	WRITE_DATA_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core write data latency queue pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	WRITE_DATA_FIFO_DEPTH	R	20h	Reports the depth of the controller core write data latency queue. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	READ_DATA_FIFO_PTR_WIDTH	R	6h	Reports the width of the controller core read data queue pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.66 EMIF_CTLCFG_DENALI_CTL_5 Register

1 EMIF_CTLCFG_DENALI_CTL_5 Register (Offset = 14h) [reset = 2050020h]

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Table 14-20142. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8014h**

Figure 14-6679. EMIF_CTLCFG_DENALI_CTL_5 Name Register

31	30	29	28	27	26	25	24
ASYNC_CDC_STAGES							
R							
2h							
23	22	21	20	19	18	17	16
MEMCD_RMODW_FIFO_PTR_WIDTH							
R							
5h							
15	14	13	12	11	10	9	8
MEMCD_RMODW_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
MEMCD_RMODW_FIFO_DEPTH							
R							
20h							

Table 14-20144. EMIF_CTLCFG_DENALI_CTL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ASYNC_CDC_STAGES	R	2h	Reports the number of synchronizer delays specified for the asynchronous boundary crossings. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	MEMCD_RMODW_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core read/modify/write FIFO pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MEMCD_RMODW_FIFO_DEPTH	R	20h	Reports the depth of the controller core read/modify/write FIFO. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.67 EMIF_CTLCFG_DENALI_CTL_6 Register

1 EMIF_CTLCFG_DENALI_CTL_6 Register (Offset = 18h) [reset = 3070101h]

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Table 14-20145. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8018h**

Figure 14-6680. EMIF_CTLCFG_DENALI_CTL_6 Name Register

31	30	29	28	27	26	25	24
AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH							
R							
3h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AXI0_WR_ARRAY_LOG2_DEPTH							
R							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AXI0_RDFIFO_LOG2_DEPTH							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AXI0_CMDFIFO_LOG2_DEPTH							
R							
1h							

Table 14-20147. EMIF_CTLCFG_DENALI_CTL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH	R	3h	Reports the depth of the AXI port 0 write command processing FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	AXI0_WR_ARRAY_LOG2_DEPTH	R	7h	Reports the depth of the AXI port 0 write data array. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	AXI0_RDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 read data FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	AXI0_CMDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 command FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.68 EMIF_CTLCFG_DENALI_CTL_7 Register

1 EMIF_CTLCFG_DENALI_CTL_7 Register (Offset = 1Ch) [reset = 0h]

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Table 14-20148. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 801Ch**

Figure 14-6681. EMIF_CTLCFG_DENALI_CTL_7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F0							
R/W							
0h							

Table 14-20150. EMIF_CTLCFG_DENALI_CTL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F0	R/W	0h	DRAM TINIT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.69 EMIF_CTLCFG_DENALI_CTL_8 Register

1 EMIF_CTLCFG_DENALI_CTL_8 Register (Offset = 20h) [reset = 0h]

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Table 14-20151. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8020h**

Figure 14-6682. EMIF_CTLCFG_DENALI_CTL_8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TINIT3_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TINIT3_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TINIT3_F0							
R/W							
0h							

Table 14-20153. EMIF_CTLCFG_DENALI_CTL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F0	R/W	0h	DRAM TINIT3 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.70 EMIF_CTLCFG_DENALI_CTL_9 Register

1 EMIF_CTLCFG_DENALI_CTL_9 Register (Offset = 24h) [reset = 0h]

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Table 14-20154. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8024h**

Figure 14-6683. EMIF_CTLCFG_DENALI_CTL_9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20156. EMIF_CTLCFG_DENALI_CTL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F0	R/W	0h	DRAM TINIT4 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.71 EMIF_CTLCFG_DENALI_CTL_10 Register

1 EMIF_CTLCFG_DENALI_CTL_10 Register (Offset = 28h) [reset = 0h]

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Table 14-20157. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8028h**

Figure 14-6684. EMIF_CTLCFG_DENALI_CTL_10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT5_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT5_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT5_F0							
R/W							
0h							

Table 14-20159. EMIF_CTLCFG_DENALI_CTL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT5_F0	R/W	0h	DRAM TINIT5 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.72 EMIF_CTLCFG_DENALI_CTL_11 Register

1 EMIF_CTLCFG_DENALI_CTL_11 Register (Offset = 2Ch) [reset = 0h]

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Table 14-20160. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 802Ch**

Figure 14-6685. EMIF_CTLCFG_DENALI_CTL_11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F1							
R/W							
0h							

Table 14-20162. EMIF_CTLCFG_DENALI_CTL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F1	R/W	0h	DRAM TINIT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.73 EMIF_CTLCFG_DENALI_CTL_12 Register

1 EMIF_CTLCFG_DENALI_CTL_12 Register (Offset = 30h) [reset = 0h]

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Table 14-20163. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8030h**

Figure 14-6686. EMIF_CTLCFG_DENALI_CTL_12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT3_F1							
R/W							
0h							

Table 14-20165. EMIF_CTLCFG_DENALI_CTL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F1	R/W	0h	DRAM TINIT3 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.74 EMIF_CTLCFG_DENALI_CTL_13 Register

1 EMIF_CTLCFG_DENALI_CTL_13 Register (Offset = 34h) [reset = 0h]

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Table 14-20166. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8034h**

Figure 14-6687. EMIF_CTLCFG_DENALI_CTL_13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TINIT4_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TINIT4_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TINIT4_F1							
R/W							
0h							

Table 14-20168. EMIF_CTLCFG_DENALI_CTL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F1	R/W	0h	DRAM TINIT4 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.75 EMIF_CTLCFG_DENALI_CTL_14 Register

1 EMIF_CTLCFG_DENALI_CTL_14 Register (Offset = 38h) [reset = 0h]

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Table 14-20169. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8038h**

Figure 14-6688. EMIF_CTLCFG_DENALI_CTL_14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TINIT5_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TINIT5_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TINIT5_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20171. EMIF_CTLCFG_DENALI_CTL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT5_F1	R/W	0h	DRAM TINIT5 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.76 EMIF_CTLCFG_DENALI_CTL_15 Register

1 EMIF_CTLCFG_DENALI_CTL_15 Register (Offset = 3Ch) [reset = 0h]

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Table 14-20172. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 803Ch**

Figure 14-6689. EMIF_CTLCFG_DENALI_CTL_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F2							
R/W							
0h							

Table 14-20174. EMIF_CTLCFG_DENALI_CTL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F2	R/W	0h	DRAM TINIT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.77 EMIF_CTLCFG_DENALI_CTL_16 Register

1 EMIF_CTLCFG_DENALI_CTL_16 Register (Offset = 40h) [reset = 0h]

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Table 14-20175. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8040h**

Figure 14-6690. EMIF_CTLCFG_DENALI_CTL_16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT3_F2							
R/W							
0h							

Table 14-20177. EMIF_CTLCFG_DENALI_CTL_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F2	R/W	0h	DRAM TINIT3 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.78 EMIF_CTLCFG_DENALI_CTL_17 Register

1 EMIF_CTLCFG_DENALI_CTL_17 Register (Offset = 44h) [reset = 0h]

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Table 14-20178. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8044h**

Figure 14-6691. EMIF_CTLCFG_DENALI_CTL_17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT4_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT4_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT4_F2							
R/W							
0h							

Table 14-20180. EMIF_CTLCFG_DENALI_CTL_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F2	R/W	0h	DRAM TINIT4 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.79 EMIF_CTLCFG_DENALI_CTL_18 Register

1 EMIF_CTLCFG_DENALI_CTL_18 Register (Offset = 48h) [reset = 0h]

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Table 14-20181. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8048h**

Figure 14-6692. EMIF_CTLCFG_DENALI_CTL_18 Name Register

31	30	29	28	27	26	25	24
RESERVED							NO_AUTO_MRR_INIT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TINIT5_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT5_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT5_F2							
R/W							
0h							

Table 14-20183. EMIF_CTLCFG_DENALI_CTL_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:0	TINIT5_F2	R/W	0h	DRAM TINIT5 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.80 EMIF_CTLCFG_DENALI_CTL_19 Register

1 EMIF_CTLCFG_DENALI_CTL_19 Register (Offset = 4Ch) [reset = 0h]

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Table 14-20184. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 804Ch**

Figure 14-6693. EMIF_CTLCFG_DENALI_CTL_19 Name Register

31	30	29	28	27	26	25	24
RESERVED						DFI_FREQ_RATIO_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						DFI_FREQ_RATIO_F1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						DFI_FREQ_RATIO_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							MRR_ERROR_STATUS
NONE							R
0h							0h

Table 14-20186. EMIF_CTLCFG_DENALI_CTL_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DFI_FREQ_RATIO_F2	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=2 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	DFI_FREQ_RATIO_F1	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	DFI_FREQ_RATIO_F0	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-20186. EMIF_CTLCFG_DENALI_CTL_19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MRR_ERROR_STATUS	R	0h	Indicates that an MRR was issued while in self-refresh. Value of 1 indicates a violation. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.81 EMIF_CTLCFG_DENALI_CTL_20 Register

1 EMIF_CTLCFG_DENALI_CTL_20 Register (Offset = 50h) [reset = 1h]

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Table 14-20187. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8050h**

Figure 14-6694. EMIF_CTLCFG_DENALI_CTL_20 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_INDEP_TRAIN_MODE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						ODT_VALUE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							NO_MRW_INIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							DFI_CMD_RATIO
NONE							R
0h							1h

Table 14-20189. EMIF_CTLCFG_DENALI_CTL_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_INDEP_TRAIN_MODE	R/W	0h	Enable PHY independent training mode commands during initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	NO_MRW_INIT	R/W	0h	Disable MRW commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DFI_CMD_RATIO	R	1h	Indicates the controller clock to DFI PHY clock ratio for the DFI command interface. For LPDDR5, this is always a 1:1 ratio. For all other memory classes, this will be the same as the dfi_freq_ratio. Zero specifies a 1:1 ratio and one specifies a 1:2 ratio. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.82 EMIF_CTLCFG_DENALI_CTL_21 Register

1 EMIF_CTLCFG_DENALI_CTL_21 Register (Offset = 54h) [reset = 0h]

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Table 14-20190. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8054h**

Figure 14-6695. EMIF_CTLCFG_DENALI_CTL_21 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DFIBUS_FREQ_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DFIBUS_FREQ_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_INDEP_INIT_MODE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TSREF2PHYMSTR</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20192. EMIF_CTLCFG_DENALI_CTL_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	DFIBUS_FREQ_F1	R/W	0h	Defines the DFI bus frequency. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	DFIBUS_FREQ_F0	R/W	0h	Defines the DFI bus frequency. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_INDEP_INIT_MODE	R/W	0h	Enable PHY independent initailization mode commands during initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	TSREF2PHYMSTR	R/W	0h	Specifies the minimum time after a self-refresh exit command on the DFI bus that the Controller will wait for the PHY to assert the dfi_phymstr_req signal, before completing other commands. Used when the low power control logic is expected to pass control to the PHY for training when exiting SREF. Reset Source: ctl_amod_g_rst_n

14.6.6.2.83 EMIF_CTLCFG_DENALI_CTL_22 Register

1 EMIF_CTLCFG_DENALI_CTL_22 Register (Offset = 58h) [reset = 0h]

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Table 14-20193. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8058h**

Figure 14-6696. EMIF_CTLCFG_DENALI_CTL_22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">FREQ_CHANGE_TYPE_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">FREQ_CHANGE_TYPE_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">FREQ_CHANGE_TYPE_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DFIBUS_FREQ_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-20195. EMIF_CTLCFG_DENALI_CTL_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	FREQ_CHANGE_TYPE_F2	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=2 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	FREQ_CHANGE_TYPE_F1	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	FREQ_CHANGE_TYPE_F0	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	DFIBUS_FREQ_F2	R/W	0h	Defines the DFI bus frequency. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.84 EMIF_CTLCFG_DENALI_CTL_23 Register

1 EMIF_CTLCFG_DENALI_CTL_23 Register (Offset = 5Ch) [reset = 0h]

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Table 14-20196. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 805Ch**

Figure 14-6697. EMIF_CTLCFG_DENALI_CTL_23 Name Register

31	30	29	28	27	26	25	24
TRST_PWRON							
R/W							
0h							
23	22	21	20	19	18	17	16
TRST_PWRON							
R/W							
0h							
15	14	13	12	11	10	9	8
TRST_PWRON							
R/W							
0h							
7	6	5	4	3	2	1	0
TRST_PWRON							
R/W							
0h							

Table 14-20198. EMIF_CTLCFG_DENALI_CTL_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.85 EMIF_CTLCFG_DENALI_CTL_24 Register

1 EMIF_CTLCFG_DENALI_CTL_24 Register (Offset = 60h) [reset = 0h]

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Table 14-20199. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8060h**

Figure 14-6698. EMIF_CTLCFG_DENALI_CTL_24 Name Register

31	30	29	28	27	26	25	24
CKE_INACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
CKE_INACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
CKE_INACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
CKE_INACTIVE							
R/W							
0h							

Table 14-20201. EMIF_CTLCFG_DENALI_CTL_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active. Reset Source: ctl_amod_g_rst_n

14.6.6.2.86 EMIF_CTLCFG_DENALI_CTL_25 Register

1 EMIF_CTLCFG_DENALI_CTL_25 Register (Offset = 64h) [reset = 0h]

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Table 14-20202. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8064h**

Figure 14-6699. EMIF_CTLCFG_DENALI_CTL_25 Name Register

31	30	29	28	27	26	25	24
TDLL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDLL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDLL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDLL_F0							
R/W							
0h							

Table 14-20204. EMIF_CTLCFG_DENALI_CTL_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TDLL_F1	R/W	0h	DRAM TDLL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TDLL_F0	R/W	0h	DRAM TDLL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.87 EMIF_CTLCFG_DENALI_CTL_26 Register

1 EMIF_CTLCFG_DENALI_CTL_26 Register (Offset = 68h) [reset = 0h]

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Table 14-20205. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8068h

Figure 14-6700. EMIF_CTLCFG_DENALI_CTL_26 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DQS_OSC_PER_CS_OOV_TRAINING_STATUS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>LPC_SW_ENTER_DQS_OSC_IN_PROGRESS_ERR_STATUS</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDLL_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDLL_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20207. EMIF_CTLCFG_DENALI_CTL_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DQS_OSC_PER_CS_OOV_TRAINING_STATUS	R	0h	Set the CS information for which DQS oscillator is having out of variance value. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	LPC_SW_ENTER_DQS_OSC_IN_PROGRESS_ERR_STATUS	R	0h	Error response for Software issued Low power command while DQS Oscillator is in progress. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	TDLL_F2	R/W	0h	DRAM TDLL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.88 EMIF_CTLCFG_DENALI_CTL_27 Register

1 EMIF_CTLCFG_DENALI_CTL_27 Register (Offset = 6Ch) [reset = 0h]

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Table 14-20208. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 806Ch**

Figure 14-6701. EMIF_CTLCFG_DENALI_CTL_27 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_MPC_CMD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_MPC_CMD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_MPC_CMD							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							DQS_OSC_TST
NONE							R/W
0h							0h

Table 14-20210. EMIF_CTLCFG_DENALI_CTL_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DQS_OSC_MPC_CMD	R/W	0h	Set MPC encoding for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DQS_OSC_TST	R/W	0h	Enable DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.89 EMIF_CTLCFG_DENALI_CTL_28 Register

1 EMIF_CTLCFG_DENALI_CTL_28 Register (Offset = 70h) [reset = 0h]

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Table 14-20211. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8070h**

Figure 14-6702. EMIF_CTLCFG_DENALI_CTL_28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DQS_OSC_ENABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MRR_MSB_REG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRR_LSB_REG							
R/W							
0h							

Table 14-20213. EMIF_CTLCFG_DENALI_CTL_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DQS_OSC_ENABLE	R/W	0h	Enable DQS oscillator measurement function in DRAM. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	MRR_MSB_REG	R/W	0h	Set MSB MRR register number for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n
7:0	MRR_LSB_REG	R/W	0h	Set LSB MRR register number for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.90 EMIF_CTLCFG_DENALI_CTL_29 Register

1 EMIF_CTLCFG_DENALI_CTL_29 Register (Offset = 74h) [reset = 0h]

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Table 14-20214. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8074h**

Figure 14-6703. EMIF_CTLCFG_DENALI_CTL_29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FUNC_VALID_CYCLES</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">DQS_OSC_PERIOD</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DQS_OSC_PERIOD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20216. EMIF_CTLCFG_DENALI_CTL_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	FUNC_VALID_CYCLES	R/W	0h	Number of cycles to hold dfi_function_valid asserted. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:0	DQS_OSC_PERIOD	R/W	0h	Number of cycles to run the oscillator measurement. Must reflect cycles programmed into mode register. Reset Source: ctl_amod_g_rst_n

14.6.6.2.91 EMIF_CTLCFG_DENALI_CTL_30 Register

1 EMIF_CTLCFG_DENALI_CTL_30 Register (Offset = 78h) [reset = 0h]

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Table 14-20217. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8078h**

Figure 14-6704. EMIF_CTLCFG_DENALI_CTL_30 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							

Table 14-20219. EMIF_CTLCFG_DENALI_CTL_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_NORM_THRESHOLD	R/W	0h	Number of long counts until the normal priority request is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.6.6.2.92 EMIF_CTLCFG_DENALI_CTL_31 Register

1 EMIF_CTLCFG_DENALI_CTL_31 Register (Offset = 7Ch) [reset = 0h]

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Table 14-20220. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 807Ch

Figure 14-6705. EMIF_CTLCFG_DENALI_CTL_31 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							

Table 14-20222. EMIF_CTLCFG_DENALI_CTL_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_HIGH_THRESHOLD	R/W	0h	Number of long counts until the high priority request is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.6.6.2.93 EMIF_CTLCFG_DENALI_CTL_32 Register

1 EMIF_CTLCFG_DENALI_CTL_32 Register (Offset = 80h) [reset = 0h]

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Table 14-20223. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8080h**

Figure 14-6706. EMIF_CTLCFG_DENALI_CTL_32 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_TIMEOUT							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_TIMEOUT							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_TIMEOUT							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_TIMEOUT							
R/W							
0h							

Table 14-20225. EMIF_CTLCFG_DENALI_CTL_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_TIMEOUT	R/W	0h	Number of long counts until the timeout is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.6.6.2.94 EMIF_CTLCFG_DENALI_CTL_33 Register

1 EMIF_CTLCFG_DENALI_CTL_33 Register (Offset = 84h) [reset = 0h]

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Table 14-20226. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8084h**

Figure 14-6707. EMIF_CTLCFG_DENALI_CTL_33 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							

Table 14-20228. EMIF_CTLCFG_DENALI_CTL_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_PROMOTE_THRESHOLD	R/W	0h	Number of long counts until a software request for the DQS Oscillator is promoted to high priority. Reset Source: ctl_amod_g_rst_n

14.6.6.2.95 EMIF_CTLCFG_DENALI_CTL_34 Register

1 EMIF_CTLCFG_DENALI_CTL_34 Register (Offset = 88h) [reset = 0h]

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Table 14-20229. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8088h

Figure 14-6708. EMIF_CTLCFG_DENALI_CTL_34 Name Register

31	30	29	28	27	26	25	24
TOSCO_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DQS_OSC_REQUEST
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OSC_VARIANCE_LIMIT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OSC_VARIANCE_LIMIT							
R/W							
0h							

Table 14-20231. EMIF_CTLCFG_DENALI_CTL_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TOSCO_F0	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DQS_OSC_REQUEST	W	0h	Software request for DQS Oscillator measurement function in DRAM. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	OSC_VARIANCE_LIMIT	R/W	0h	Allowed difference between base value and DQS Oscillator measurement. Reset Source: ctl_amod_g_rst_n

14.6.6.2.96 EMIF_CTLCFG_DENALI_CTL_35 Register

1 EMIF_CTLCFG_DENALI_CTL_35 Register (Offset = 8Ch) [reset = 0h]

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Table 14-20232. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 808Ch**

Figure 14-6709. EMIF_CTLCFG_DENALI_CTL_35 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_BASE_VALUE_0_CS0							
R							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_BASE_VALUE_0_CS0							
R							
0h							
15	14	13	12	11	10	9	8
TOSCO_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TOSCO_F1							
R/W							
0h							

Table 14-20234. EMIF_CTLCFG_DENALI_CTL_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_0_CS0	R	0h	Base value for device 0 on chip 0. READ-ONLY DEV=0 Reset Source: ctl_amod_g_rst_n
15:8	TOSCO_F2	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TOSCO_F1	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.97 EMIF_CTLCFG_DENALI_CTL_36 Register

1 EMIF_CTLCFG_DENALI_CTL_36 Register (Offset = 90h) [reset = 0h]

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Table 14-20235. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8090h**

Figure 14-6710. EMIF_CTLCFG_DENALI_CTL_36 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_2_CS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_2_CS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_1_CS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_1_CS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20237. EMIF_CTLCFG_DENALI_CTL_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_2_CS0	R	0h	Base value for device 2 on chip 0. READ-ONLY DEV=2 Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_1_CS0	R	0h	Base value for device 1 on chip 0. READ-ONLY DEV=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.98 EMIF_CTLCFG_DENALI_CTL_37 Register

1 EMIF_CTLCFG_DENALI_CTL_37 Register (Offset = 94h) [reset = 0h]

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Table 14-20238. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8094h

Figure 14-6711. EMIF_CTLCFG_DENALI_CTL_37 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_BASE_VALUE_0_CS1							
R							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_BASE_VALUE_0_CS1							
R							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_BASE_VALUE_3_CS0							
R							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_BASE_VALUE_3_CS0							
R							
0h							

Table 14-20240. EMIF_CTLCFG_DENALI_CTL_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_0_CS1	R	0h	Base value for device 0 on chip 1. READ-ONLY DEV=0 Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_3_CS0	R	0h	Base value for device 3 on chip 0. READ-ONLY DEV=3 Reset Source: ctl_amod_g_rst_n

14.6.6.2.99 EMIF_CTLCFG_DENALI_CTL_38 Register

1 EMIF_CTLCFG_DENALI_CTL_38 Register (Offset = 98h) [reset = 0h]

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Table 14-20241. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8098h

Figure 14-6712. EMIF_CTLCFG_DENALI_CTL_38 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_BASE_VALUE_2_CS1							
R							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_BASE_VALUE_2_CS1							
R							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_BASE_VALUE_1_CS1							
R							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_BASE_VALUE_1_CS1							
R							
0h							

Table 14-20243. EMIF_CTLCFG_DENALI_CTL_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_2_CS1	R	0h	Base value for device 2 on chip 1. READ-ONLY DEV=2 Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_1_CS1	R	0h	Base value for device 1 on chip 1. READ-ONLY DEV=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.100 EMIF_CTLCFG_DENALI_CTL_39 Register

1 EMIF_CTLCFG_DENALI_CTL_39 Register (Offset = 9Ch) [reset = 0h]

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Table 14-20244. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 809Ch**

Figure 14-6713. EMIF_CTLCFG_DENALI_CTL_39 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>DQS_OSC_IN_PROGRESS_STATUS</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DQS_OSC_STATUS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_3_CS1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DQS_OSC_BASE_VALUE_3_CS1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20246. EMIF_CTLCFG_DENALI_CTL_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DQS_OSC_IN_PROGRESS_STATUS	R	0h	DQS Oscillator is in progress.Set '1' DQS OSC is in progress READ-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	DQS_OSC_STATUS	R	0h	Holds the overflow and out of variance status associated with the resp. interrupts. Bit [0] set indicates overflow of DQS oscillator,bit [1] set indicates overflow of WCKO oscillator,bit [2] set indicates oov of DQS oscillator,bit [3] set indicates oov of WCKO oscillator. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_3_CS1	R	0h	Base value for device 3 on chip 1. READ-ONLY DEV=3 Reset Source: ctl_amod_g_rst_n

14.6.6.2.101 EMIF_CTLCFG_DENALI_CTL_40 Register

1 EMIF_CTLCFG_DENALI_CTL_40 Register (Offset = A0h) [reset = 0h]

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Table 14-20247. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80A0h**

Figure 14-6714. EMIF_CTLCFG_DENALI_CTL_40 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		ADDITIVE_LAT_F0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F0						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F0						
NONE	R/W						
0h	0h						

Table 14-20249. EMIF_CTLCFG_DENALI_CTL_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F0	R/W	0h	DRAM CA parity latency value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F0	R/W	0h	DRAM additive latency value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F0	R/W	0h	DRAM WRLAT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F0	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.102 EMIF_CTLCFG_DENALI_CTL_41 Register

1 EMIF_CTLCFG_DENALI_CTL_41 Register (Offset = A4h) [reset = 0h]

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Table 14-20250. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 80A4h

Figure 14-6715. EMIF_CTLCFG_DENALI_CTL_41 Name Register

31	30	29	28	27	26	25	24
TMRD_PAR_MAX_PL_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TMOD_PAR_MAX_PL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_PAR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TMOD_PAR_F0							
R/W							
0h							

Table 14-20252. EMIF_CTLCFG_DENALI_CTL_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F0	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F0	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F0	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F0	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.103 EMIF_CTLCFG_DENALI_CTL_42 Register

1 EMIF_CTLCFG_DENALI_CTL_42 Register (Offset = A8h) [reset = 0h]

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Table 14-20253. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80A8h**

Figure 14-6716. EMIF_CTLCFG_DENALI_CTL_42 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		ADDITIVE_LAT_F1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F1						
NONE	R/W						
0h	0h						

Table 14-20255. EMIF_CTLCFG_DENALI_CTL_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F1	R/W	0h	DRAM CA parity latency value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F1	R/W	0h	DRAM additive latency value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F1	R/W	0h	DRAM WRLAT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F1	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.104 EMIF_CTLCFG_DENALI_CTL_43 Register

1 EMIF_CTLCFG_DENALI_CTL_43 Register (Offset = ACh) [reset = 0h]

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Table 14-20256. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 80ACh

Figure 14-6717. EMIF_CTLCFG_DENALI_CTL_43 Name Register

31	30	29	28	27	26	25	24
TMRD_PAR_MAX_PL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TMOD_PAR_MAX_PL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_PAR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TMOD_PAR_F1							
R/W							
0h							

Table 14-20258. EMIF_CTLCFG_DENALI_CTL_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F1	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F1	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F1	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F1	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.105 EMIF_CTLCFG_DENALI_CTL_44 Register

1 EMIF_CTLCFG_DENALI_CTL_44 Register (Offset = B0h) [reset = 0h]

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Table 14-20259. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80B0h**

Figure 14-6718. EMIF_CTLCFG_DENALI_CTL_44 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		ADDITIVE_LAT_F2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	WRLAT_F2						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	CASLAT_LIN_F2						
NONE	R/W						
0h	0h						

Table 14-20261. EMIF_CTLCFG_DENALI_CTL_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F2	R/W	0h	DRAM CA parity latency value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F2	R/W	0h	DRAM additive latency value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F2	R/W	0h	DRAM WRLAT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F2	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.106 EMIF_CTLCFG_DENALI_CTL_45 Register

1 EMIF_CTLCFG_DENALI_CTL_45 Register (Offset = B4h) [reset = 0h]

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Table 14-20262. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80B4h**

Figure 14-6719. EMIF_CTLCFG_DENALI_CTL_45 Name Register

31	30	29	28	27	26	25	24
TMRD_PAR_MAX_PL_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TMOD_PAR_MAX_PL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_PAR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TMOD_PAR_F2							
R/W							
0h							

Table 14-20264. EMIF_CTLCFG_DENALI_CTL_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F2	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F2	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 4 in cycles. Used during changes of CA parity latency value in DRAM. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F2	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F2	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.107 EMIF_CTLCFG_DENALI_CTL_46 Register

1 EMIF_CTLCFG_DENALI_CTL_46 Register (Offset = B8h) [reset = 0h]

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Table 14-20265. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80B8h**

Figure 14-6720. EMIF_CTLCFG_DENALI_CTL_46 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TRRD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCCD_L_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCCD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TBST_INT_INTERVAL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-20267. EMIF_CTLCFG_DENALI_CTL_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRRD_F0	R/W	0h	DRAM TRRD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCCD_L_F0	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TBST_INT_INTERVAL	R/W	0h	DRAM burst interrupt interval value in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.108 EMIF_CTLCFG_DENALI_CTL_47 Register

1 EMIF_CTLCFG_DENALI_CTL_47 Register (Offset = BCh) [reset = 0h]

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Table 14-20268. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80BCh**

Figure 14-6721. EMIF_CTLCFG_DENALI_CTL_47 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>TRC_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TRC_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRRD_L_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20270. EMIF_CTLCFG_DENALI_CTL_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:8	TRC_F0	R/W	0h	DRAM TRC value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_L_F0	R/W	0h	DRAM TRRD_L value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.109 EMIF_CTLCFG_DENALI_CTL_48 Register

1 EMIF_CTLCFG_DENALI_CTL_48 Register (Offset = C0h) [reset = 0h]

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Table 14-20271. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 80C0h

Figure 14-6722. EMIF_CTLCFG_DENALI_CTL_48 Name Register

31	30	29	28	27	26	25	24
RESERVED		TWTR_L_F0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		TWTR_F0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							TRAS_MIN_F0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TRAS_MIN_F0							
R/W							
0h							

Table 14-20273. EMIF_CTLCFG_DENALI_CTL_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F0	R/W	0h	DRAM TWTR_L value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F0	R/W	0h	DRAM TWTR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F0	R/W	0h	DRAM TRAS_MIN value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.110 EMIF_CTLCFG_DENALI_CTL_49 Register

1 EMIF_CTLCFG_DENALI_CTL_49 Register (Offset = C4h) [reset = 0h]

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Table 14-20274. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80C4h**

Figure 14-6723. EMIF_CTLCFG_DENALI_CTL_49 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCCD_L_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							TFAW_F0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
TFAW_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRP_F0							
R/W							
0h							

Table 14-20276. EMIF_CTLCFG_DENALI_CTL_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCCD_L_F1	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F0	R/W	0h	DRAM TFAW value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F0	R/W	0h	DRAM TRP value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.111 EMIF_CTLCFG_DENALI_CTL_50 Register

1 EMIF_CTLCFG_DENALI_CTL_50 Register (Offset = C8h) [reset = 0h]

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Table 14-20277. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80C8h**

Figure 14-6724. EMIF_CTLCFG_DENALI_CTL_50 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRC_F1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TRC_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TRRD_L_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TRRD_F1							
R/W							
0h							

Table 14-20279. EMIF_CTLCFG_DENALI_CTL_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	TRC_F1	R/W	0h	DRAM TRC value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TRRD_L_F1	R/W	0h	DRAM TRRD_L value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_F1	R/W	0h	DRAM TRRD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.112 EMIF_CTLCFG_DENALI_CTL_51 Register

1 EMIF_CTLCFG_DENALI_CTL_51 Register (Offset = CCh) [reset = 0h]

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Table 14-20280. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80CCh**

Figure 14-6725. EMIF_CTLCFG_DENALI_CTL_51 Name Register

31	30	29	28	27	26	25	24
RESERVED		TWTR_L_F1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TWTR_F1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TRAS_MIN_F1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRAS_MIN_F1							
R/W							
0h							

Table 14-20282. EMIF_CTLCFG_DENALI_CTL_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F1	R/W	0h	DRAM TWTR_L value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F1	R/W	0h	DRAM TWTR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F1	R/W	0h	DRAM TRAS_MIN value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.113 EMIF_CTLCFG_DENALI_CTL_52 Register

1 EMIF_CTLCFG_DENALI_CTL_52 Register (Offset = D0h) [reset = 0h]

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Table 14-20283. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80D0h**

Figure 14-6726. EMIF_CTLCFG_DENALI_CTL_52 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCCD_L_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>TFAW_F1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TFAW_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRP_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20285. EMIF_CTLCFG_DENALI_CTL_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCCD_L_F2	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F1	R/W	0h	DRAM TFAW value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F1	R/W	0h	DRAM TRP value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.114 EMIF_CTLCFG_DENALI_CTL_53 Register

1 EMIF_CTLCFG_DENALI_CTL_53 Register (Offset = D4h) [reset = 0h]

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Table 14-20286. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80D4h**

Figure 14-6727. EMIF_CTLCFG_DENALI_CTL_53 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRC_F2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRC_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRRD_L_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRRD_F2							
R/W							
0h							

Table 14-20288. EMIF_CTLCFG_DENALI_CTL_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	TRC_F2	R/W	0h	DRAM TRC value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TRRD_L_F2	R/W	0h	DRAM TRRD_L value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_F2	R/W	0h	DRAM TRRD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.115 EMIF_CTLCFG_DENALI_CTL_54 Register

1 EMIF_CTLCFG_DENALI_CTL_54 Register (Offset = D8h) [reset = 0h]

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Table 14-20289. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80D8h**

Figure 14-6728. EMIF_CTLCFG_DENALI_CTL_54 Name Register

31	30	29	28	27	26	25	24
RESERVED		TWTR_L_F2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		TWTR_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							TRAS_MIN_F2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TRAS_MIN_F2							
R/W							
0h							

Table 14-20291. EMIF_CTLCFG_DENALI_CTL_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F2	R/W	0h	DRAM TWTR_L value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F2	R/W	0h	DRAM TWTR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F2	R/W	0h	DRAM TRAS_MIN value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.116 EMIF_CTLCFG_DENALI_CTL_55 Register

1 EMIF_CTLCFG_DENALI_CTL_55 Register (Offset = DCh) [reset = 0h]

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Table 14-20292. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 80DCh

Figure 14-6729. EMIF_CTLCFG_DENALI_CTL_55 Name Register

31	30	29	28	27	26	25	24
TRTP_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							TFAW_F2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
TFAW_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TRP_F2							
R/W							
0h							

Table 14-20294. EMIF_CTLCFG_DENALI_CTL_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_F0	R/W	0h	DRAM TRTP value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F2	R/W	0h	DRAM TFAW value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F2	R/W	0h	DRAM TRP value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.117 EMIF_CTLCFG_DENALI_CTL_56 Register

1 EMIF_CTLCFG_DENALI_CTL_56 Register (Offset = E0h) [reset = 0h]

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Table 14-20295. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80E0h**

Figure 14-6730. EMIF_CTLCFG_DENALI_CTL_56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TMOD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRTP_AP_F0							
R/W							
0h							

Table 14-20297. EMIF_CTLCFG_DENALI_CTL_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TMOD_F0	R/W	0h	Number of cycles after MRS command and before any other command. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_F0	R/W	0h	DRAM TMRD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRTP_AP_F0	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.118 EMIF_CTLCFG_DENALI_CTL_57 Register

1 EMIF_CTLCFG_DENALI_CTL_57 Register (Offset = E4h) [reset = 0h]

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Table 14-20298. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80E4h**

Figure 14-6731. EMIF_CTLCFG_DENALI_CTL_57 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKE_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TRAS_MAX_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRAS_MAX_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRAS_MAX_F0							
R/W							
0h							

Table 14-20300. EMIF_CTLCFG_DENALI_CTL_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F0	R/W	0h	Minimum CKE pulse width. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F0	R/W	0h	DRAM TRAS_MAX value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.119 EMIF_CTLCFG_DENALI_CTL_58 Register

1 EMIF_CTLCFG_DENALI_CTL_58 Register (Offset = E8h) [reset = 0h]

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Table 14-20301. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80E8h**

Figure 14-6732. EMIF_CTLCFG_DENALI_CTL_58 Name Register

31	30	29	28	27	26	25	24
TRTP_AP_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRTP_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TCCDMW_F0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TCKESR_F0							
R/W							
0h							

Table 14-20303. EMIF_CTLCFG_DENALI_CTL_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_AP_F1	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TRTP_F1	R/W	0h	DRAM TRTP value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F0	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F0	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.120 EMIF_CTLCFG_DENALI_CTL_59 Register

1 EMIF_CTLCFG_DENALI_CTL_59 Register (Offset = ECh) [reset = 0h]

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Table 14-20304. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 80ECh

Figure 14-6733. EMIF_CTLCFG_DENALI_CTL_59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TMOD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TMRD_F1							
R/W							
0h							

Table 14-20306. EMIF_CTLCFG_DENALI_CTL_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TMOD_F1	R/W	0h	Number of cycles after MRS command and before any other command. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TMRD_F1	R/W	0h	DRAM TMRD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.121 EMIF_CTLCFG_DENALI_CTL_60 Register

1 EMIF_CTLCFG_DENALI_CTL_60 Register (Offset = F0h) [reset = 0h]

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Table 14-20307. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80F0h**

Figure 14-6734. EMIF_CTLCFG_DENALI_CTL_60 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKE_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TRAS_MAX_F1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRAS_MAX_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRAS_MAX_F1							
R/W							
0h							

Table 14-20309. EMIF_CTLCFG_DENALI_CTL_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F1	R/W	0h	Minimum CKE pulse width. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F1	R/W	0h	DRAM TRAS_MAX value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.122 EMIF_CTLCFG_DENALI_CTL_61 Register

1 EMIF_CTLCFG_DENALI_CTL_61 Register (Offset = F4h) [reset = 0h]

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Table 14-20310. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80F4h**

Figure 14-6735. EMIF_CTLCFG_DENALI_CTL_61 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TRTP_AP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TRTP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TCCDMW_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TCKESR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20312. EMIF_CTLCFG_DENALI_CTL_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_AP_F2	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TRTP_F2	R/W	0h	DRAM TRTP value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F1	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F1	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.123 EMIF_CTLCFG_DENALI_CTL_62 Register

1 EMIF_CTLCFG_DENALI_CTL_62 Register (Offset = F8h) [reset = 0h]

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Table 14-20313. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80F8h**

Figure 14-6736. EMIF_CTLCFG_DENALI_CTL_62 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TMOD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TMRD_F2							
R/W							
0h							

Table 14-20315. EMIF_CTLCFG_DENALI_CTL_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TMOD_F2	R/W	0h	Number of cycles after MRS command and before any other command. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TMRD_F2	R/W	0h	DRAM TMRD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.124 EMIF_CTLCFG_DENALI_CTL_63 Register

1 EMIF_CTLCFG_DENALI_CTL_63 Register (Offset = FCh) [reset = 0h]

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Table 14-20316. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 80FCh**

Figure 14-6737. EMIF_CTLCFG_DENALI_CTL_63 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKE_F2				
NONE			R/W				
0h			0h				

23	22	21	20	19	18	17	16
RESERVED				TRAS_MAX_F2			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
TRAS_MAX_F2							
R/W							
0h							

7	6	5	4	3	2	1	0
TRAS_MAX_F2							
R/W							
0h							

Table 14-20318. EMIF_CTLCFG_DENALI_CTL_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F2	R/W	0h	Minimum CKE pulse width. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F2	R/W	0h	DRAM TRAS_MAX value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.125 EMIF_CTLCFG_DENALI_CTL_64 Register

1 EMIF_CTLCFG_DENALI_CTL_64 Register (Offset = 100h) [reset = 40000h]

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Table 14-20319. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8100h**

Figure 14-6738. EMIF_CTLCFG_DENALI_CTL_64 Name Register

31	30	29	28	27	26	25	24
RESERVED					MC_RESERVED0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED					TPPD		
NONE					R/W		
0h					4h		
15	14	13	12	11	10	9	8
RESERVED		TCCDMW_F2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
TCKESR_F2							
R/W							
0h							

Table 14-20321. EMIF_CTLCFG_DENALI_CTL_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	MC_RESERVED0	R/W	0h	Reserved
23:19	RESERVED	NONE	0h	Reserved
18:16	TPPD	R/W	4h	DRAM TPPD value in cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F2	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F2	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.126 EMIF_CTLCFG_DENALI_CTL_65 Register

1 EMIF_CTLCFG_DENALI_CTL_65 Register (Offset = 104h) [reset = 0h]

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Table 14-20322. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8104h**

Figure 14-6739. EMIF_CTLCFG_DENALI_CTL_65 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TWR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TRCD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>WRITEINTERP</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MC_RESERVED1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-20324. EMIF_CTLCFG_DENALI_CTL_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TWR_F0	R/W	0h	DRAM TWR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TRCD_F0	R/W	0h	DRAM TRCD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	WRITEINTERP	R/W	0h	Allow controller to interrupt a write burst to the DRAMs with a read command. Set to 1 to allow interruption. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MC_RESERVED1	R/W	0h	Reserved

14.6.6.2.127 EMIF_CTLCFG_DENALI_CTL_66 Register

1 EMIF_CTLCFG_DENALI_CTL_66 Register (Offset = 108h) [reset = 0h]

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Table 14-20325. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8108h**

Figure 14-6740. EMIF_CTLCFG_DENALI_CTL_66 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TWR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TRCD_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TWR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRCD_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20327. EMIF_CTLCFG_DENALI_CTL_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TWR_F2	R/W	0h	DRAM TWR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TRCD_F2	R/W	0h	DRAM TRCD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TWR_F1	R/W	0h	DRAM TWR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRCD_F1	R/W	0h	DRAM TRCD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.128 EMIF_CTLCFG_DENALI_CTL_67 Register

1 EMIF_CTLCFG_DENALI_CTL_67 Register (Offset = 10Ch) [reset = 0h]

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Table 14-20328. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 810Ch**

Figure 14-6741. EMIF_CTLCFG_DENALI_CTL_67 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRAS_LOCKOUT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CONCURRENTAP
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							AP
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				TMRR			
NONE				R/W			
0h				0h			

Table 14-20330. EMIF_CTLCFG_DENALI_CTL_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRAS_LOCKOUT	R/W	0h	IF the DRAM supports it, this allows the controller to execute auto pre-charge commands before the TRAS_MIN parameter expires. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CONCURRENTAP	R/W	0h	IF the DRAM supports it, this allows the controller to issue commands to other banks while a bank is in auto pre-charge. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AP	R/W	0h	Enable auto pre-charge mode of controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TMRR	R/W	0h	DRAM TMRR value in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.129 EMIF_CTLCFG_DENALI_CTL_68 Register

1 EMIF_CTLCFG_DENALI_CTL_68 Register (Offset = 110h) [reset = 2000000h]

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Table 14-20331. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8110h**

Figure 14-6742. EMIF_CTLCFG_DENALI_CTL_68 Name Register

31	30	29	28	27	26	25	24
RESERVED		BSTLEN					
NONE		R/W					
0h		2h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDAL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDAL_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDAL_F0							
R/W							
0h							

Table 14-20333. EMIF_CTLCFG_DENALI_CTL_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization. Program to 1 for BL2, program to 2 for BL4, program to 3 for BL8, program to 4 for BL16, or program to 5 for BL32. All other settings are reserved. Reset Source: ctl_amod_g_rst_n
23:16	TDAL_F2	R/W	0h	DRAM TDAL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TDAL_F1	R/W	0h	DRAM TDAL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TDAL_F0	R/W	0h	DRAM TDAL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.130 EMIF_CTLCFG_DENALI_CTL_69 Register

1 EMIF_CTLCFG_DENALI_CTL_69 Register (Offset = 114h) [reset = 0h]

Return to Summary Table

Table 14-20334. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8114h**

Figure 14-6743. EMIF_CTLCFG_DENALI_CTL_69 Name Register

31	30	29	28	27	26	25	24
TRP_AB_F0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
TRP_AB_F2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
TRP_AB_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRP_AB_F0_0							
R/W							
0h							

Table 14-20336. EMIF_CTLCFG_DENALI_CTL_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRP_AB_F0_1	R/W	0h	DRAM TRP all bank value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TRP_AB_F2_0	R/W	0h	DRAM TRP all bank value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TRP_AB_F1_0	R/W	0h	DRAM TRP all bank value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRP_AB_F0_0	R/W	0h	DRAM TRP all bank value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.131 EMIF_CTLCFG_DENALI_CTL_70 Register

1 EMIF_CTLCFG_DENALI_CTL_70 Register (Offset = 118h) [reset = 0h]

Return to Summary Table

Table 14-20337. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8118h**

Figure 14-6744. EMIF_CTLCFG_DENALI_CTL_70 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ADDRESS_MIRRORING</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>REG_DIMM_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TRP_AB_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRP_AB_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20339. EMIF_CTLCFG_DENALI_CTL_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ADDRESS_MIRRORING	R/W	0h	Indicates which chip selects support address mirroring. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation of the controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	TRP_AB_F2_1	R/W	0h	DRAM TRP all bank value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRP_AB_F1_1	R/W	0h	DRAM TRP all bank value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.132 EMIF_CTLCFG_DENALI_CTL_71 Register

1 EMIF_CTLCFG_DENALI_CTL_71 Register (Offset = 11Ch) [reset = 0h]

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Table 14-20340. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 811Ch

Figure 14-6745. EMIF_CTLCFG_DENALI_CTL_71 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>NO_MEMORY_DM</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>MC_RESERVED2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>OPTIMAL_RMODW_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20342. EMIF_CTLCFG_DENALI_CTL_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	NO_MEMORY_DM	R/W	0h	Indicates that the external DRAM does not support DM masking. Set to 1 for no DM masking at the DRAM. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	MC_RESERVED2	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	OPTIMAL_RMODW_EN	R/W	0h	Enables optimized RMODW logic in the controller. A value of 1 enables optimized RMODW operation. All RMODW operations are still supported in a non-optimal manner when the value is 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.133 EMIF_CTLCFG_DENALI_CTL_72 Register

1 EMIF_CTLCFG_DENALI_CTL_72 Register (Offset = 120h) [reset = 0h]

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Table 14-20343. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8120h**

Figure 14-6746. EMIF_CTLCFG_DENALI_CTL_72 Name Register

31	30	29	28	27	26	25	24
RESERVED						CA_PARITY_ERROR_INJECT	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
CA_PARITY_ERROR_INJECT							
R/W							
0h							
15	14	13	12	11	10	9	8
CA_PARITY_ERROR_INJECT							
R/W							
0h							
7	6	5	4	3	2	1	0
CA_PARITY_ERROR_INJECT							
R/W							
0h							

Table 14-20345. EMIF_CTLCFG_DENALI_CTL_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	CA_PARITY_ERROR_INJECT	R/W	0h	Selects bit to corrupt on the CA bus for CA parity error injection. Reset Source: ctl_amod_g_rst_n

14.6.6.2.134 EMIF_CTLCFG_DENALI_CTL_73 Register

1 EMIF_CTLCFG_DENALI_CTL_73 Register (Offset = 124h) [reset = 0h]

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Table 14-20346. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8124h**

Figure 14-6747. EMIF_CTLCFG_DENALI_CTL_73 Name Register

31	30	29	28	27	26	25	24
RESERVED							TREF_ENABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							AREF_STATUS
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							AREFRESH
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CA_PARITY_ERROR
NONE							R
0h							0h

Table 14-20348. EMIF_CTLCFG_DENALI_CTL_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TREF_ENABLE	R/W	0h	Issue auto-refresh commands to the DRAMs at the interval defined in the TREF parameter. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	AREF_STATUS	R	0h	Indicates a SR error associated with the AREF interrupt. Value of 1 indicates a violation. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AREFRESH	W	0h	Initiate auto-refresh at the end of the current burst boundary. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	CA_PARITY_ERROR	R	0h	Contains one hot indication of registered DIMM parity errors. Value of 1 indicates an error on that DIMM. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.135 EMIF_CTLCFG_DENALI_CTL_74 Register

1 EMIF_CTLCFG_DENALI_CTL_74 Register (Offset = 128h) [reset = 0h]

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Table 14-20349. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8128h**

Figure 14-6748. EMIF_CTLCFG_DENALI_CTL_74 Name Register

31	30	29	28	27	26	25	24
RESERVED						TRFC_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TRFC_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED		CS_COMPARISON_FOR_REFRESH_DEPTH					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED					TRFC_OPT_THRESHOLD		
NONE					R/W		
0h					0h		

Table 14-20351. EMIF_CTLCFG_DENALI_CTL_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TRFC_F0	R/W	0h	DRAM TRFC value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	CS_COMPARISON_FOR_REFRESH_DEPTH	R/W	0h	Defines the number of entries of the command queue that the refresh logic will consider for sending a refresh command. A non-zero value limits the decode to a subset of the full command pipeline. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TRFC_OPT_THRESHOLD	R/W	0h	Number of clocks before TRFC expires when the refresh task will deassert its request for optimal command to command turn-around timing. Reset Source: ctl_amod_g_rst_n

14.6.6.2.136 EMIF_CTLCFG_DENALI_CTL_75 Register

1 EMIF_CTLCFG_DENALI_CTL_75 Register (Offset = 12Ch) [reset = 0h]

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Table 14-20352. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 812Ch**

Figure 14-6749. EMIF_CTLCFG_DENALI_CTL_75 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREF_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREF_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TREF_F0							
R/W							
0h							

Table 14-20354. EMIF_CTLCFG_DENALI_CTL_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F0	R/W	0h	DRAM TREF value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.137 EMIF_CTLCFG_DENALI_CTL_76 Register

1 EMIF_CTLCFG_DENALI_CTL_76 Register (Offset = 130h) [reset = 0h]

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Table 14-20355. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8130h**

Figure 14-6750. EMIF_CTLCFG_DENALI_CTL_76 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TRFC_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRFC_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20357. EMIF_CTLCFG_DENALI_CTL_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_F1	R/W	0h	DRAM TRFC value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.138 EMIF_CTLCFG_DENALI_CTL_77 Register

1 EMIF_CTLCFG_DENALI_CTL_77 Register (Offset = 134h) [reset = 0h]

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Table 14-20358. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8134h**

Figure 14-6751. EMIF_CTLCFG_DENALI_CTL_77 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TREF_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TREF_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TREF_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20360. EMIF_CTLCFG_DENALI_CTL_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F1	R/W	0h	DRAM TREF value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.139 EMIF_CTLCFG_DENALI_CTL_78 Register

1 EMIF_CTLCFG_DENALI_CTL_78 Register (Offset = 138h) [reset = 0h]

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Table 14-20361. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8138h**

Figure 14-6752. EMIF_CTLCFG_DENALI_CTL_78 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_F2							
R/W							
0h							

Table 14-20363. EMIF_CTLCFG_DENALI_CTL_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_F2	R/W	0h	DRAM TRFC value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.140 EMIF_CTLCFG_DENALI_CTL_79 Register

1 EMIF_CTLCFG_DENALI_CTL_79 Register (Offset = 13Ch) [reset = 0h]

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Table 14-20364. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 813Ch**

Figure 14-6753. EMIF_CTLCFG_DENALI_CTL_79 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TREF_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TREF_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TREF_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20366. EMIF_CTLCFG_DENALI_CTL_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F2	R/W	0h	DRAM TREF value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.141 EMIF_CTLCFG_DENALI_CTL_80 Register

1 EMIF_CTLCFG_DENALI_CTL_80 Register (Offset = 140h) [reset = 0h]

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Table 14-20367. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8140h**

Figure 14-6754. EMIF_CTLCFG_DENALI_CTL_80 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TREF_INTERVAL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TREF_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TREF_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20369. EMIF_CTLCFG_DENALI_CTL_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects. Reset Source: ctl_amod_g_rst_n

14.6.6.2.142 EMIF_CTLCFG_DENALI_CTL_81 Register

1 EMIF_CTLCFG_DENALI_CTL_81 Register (Offset = 144h) [reset = 0h]

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Table 14-20370. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8144h

Figure 14-6755. EMIF_CTLCFG_DENALI_CTL_81 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_PB_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_PB_F0							
R/W							
0h							

Table 14-20372. EMIF_CTLCFG_DENALI_CTL_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F0	R/W	0h	DRAM TRFC_PB value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.143 EMIF_CTLCFG_DENALI_CTL_82 Register

1 EMIF_CTLCFG_DENALI_CTL_82 Register (Offset = 148h) [reset = 0h]

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Table 14-20373. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8148h**

Figure 14-6756. EMIF_CTLCFG_DENALI_CTL_82 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TREFI_PB_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TREFI_PB_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TREFI_PB_F0							
R/W							
0h							

Table 14-20375. EMIF_CTLCFG_DENALI_CTL_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F0	R/W	0h	DRAM TREFI_PB value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.144 EMIF_CTLCFG_DENALI_CTL_83 Register

1 EMIF_CTLCFG_DENALI_CTL_83 Register (Offset = 14Ch) [reset = 0h]

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Table 14-20376. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 814Ch**

Figure 14-6757. EMIF_CTLCFG_DENALI_CTL_83 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_PB_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_PB_F1							
R/W							
0h							

Table 14-20378. EMIF_CTLCFG_DENALI_CTL_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F1	R/W	0h	DRAM TRFC_PB value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.145 EMIF_CTLCFG_DENALI_CTL_84 Register

1 EMIF_CTLCFG_DENALI_CTL_84 Register (Offset = 150h) [reset = 0h]

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Table 14-20379. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8150h**

Figure 14-6758. EMIF_CTLCFG_DENALI_CTL_84 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TREFI_PB_F1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TREFI_PB_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TREFI_PB_F1							
R/W							
0h							

Table 14-20381. EMIF_CTLCFG_DENALI_CTL_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F1	R/W	0h	DRAM TREFI_PB value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.146 EMIF_CTLCFG_DENALI_CTL_85 Register

1 EMIF_CTLCFG_DENALI_CTL_85 Register (Offset = 154h) [reset = 0h]

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Table 14-20382. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8154h**

Figure 14-6759. EMIF_CTLCFG_DENALI_CTL_85 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TRFC_PB_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRFC_PB_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20384. EMIF_CTLCFG_DENALI_CTL_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F2	R/W	0h	DRAM TRFC_PB value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.147 EMIF_CTLCFG_DENALI_CTL_86 Register

1 EMIF_CTLCFG_DENALI_CTL_86 Register (Offset = 158h) [reset = 0h]

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Table 14-20385. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8158h**

Figure 14-6760. EMIF_CTLCFG_DENALI_CTL_86 Name Register

31	30	29	28	27	26	25	24
RESERVED							PBR_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TREFI_PB_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TREFI_PB_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TREFI_PB_F2							
R/W							
0h							

Table 14-20387. EMIF_CTLCFG_DENALI_CTL_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PBR_EN	R/W	0h	Enables the per-bank refresh feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F2	R/W	0h	DRAM TREFI_PB value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.148 EMIF_CTLCFG_DENALI_CTL_87 Register

1 EMIF_CTLCFG_DENALI_CTL_87 Register (Offset = 15Ch) [reset = 0h]

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Table 14-20388. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 815Ch**

Figure 14-6761. EMIF_CTLCFG_DENALI_CTL_87 Name Register

31	30	29	28	27	26	25	24
RESERVED				PBR_BANK_SELECT_DELAY			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PBR_MAX_BANK_WAIT							
R/W							
0h							
15	14	13	12	11	10	9	8
PBR_MAX_BANK_WAIT							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PBR_NUMERIC_ORDER
NONE							R/W
0h							0h

Table 14-20390. EMIF_CTLCFG_DENALI_CTL_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PBR_BANK_SELECT_DELAY	R/W	0h	Defines the PBR bank select to command delay, the time from bank selection to when the command queue bank selection logic is guaranteed to have blocked the bank. Reset Source: ctl_amod_g_rst_n
23:8	PBR_MAX_BANK_WAIT	R/W	0h	Defines the maximum number of cycles that the PBR module will wait for Strategy to release the target bank until the PBR will assert the inhibit and close the target bank. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PBR_NUMERIC_ORDER	R/W	0h	Enables the PBR to run REFpb commands in numeric bank order [0,1,2,3, etc.] When disabled, the order may be modified if supported by the memory type. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.149 EMIF_CTLCFG_DENALI_CTL_88 Register

1 EMIF_CTLCFG_DENALI_CTL_88 Register (Offset = 160h) [reset = 0h]

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Table 14-20391. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8160h

Figure 14-6762. EMIF_CTLCFG_DENALI_CTL_88 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			AREF_PBR_CONT_DIS_THRESHOLD				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			AREF_PBR_CONT_EN_THRESHOLD				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							PBR_CONT_REQ_EN
NONE							R/W
0h							0h

Table 14-20393. EMIF_CTLCFG_DENALI_CTL_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	AREF_PBR_CONT_DIS_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be deasserted. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	AREF_PBR_CONT_EN_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be asserted. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PBR_CONT_REQ_EN	R/W	0h	Enables the per-bank refresh continuous request feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.150 EMIF_CTLCFG_DENALI_CTL_89 Register

1 EMIF_CTLCFG_DENALI_CTL_89 Register (Offset = 164h) [reset = 0h]

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Table 14-20394. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8164h**

Figure 14-6763. EMIF_CTLCFG_DENALI_CTL_89 Name Register

31	30	29	28	27	26	25	24
TPDEX_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TPDEX_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TPDEX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TPDEX_F0							
R/W							
0h							

Table 14-20396. EMIF_CTLCFG_DENALI_CTL_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TPDEX_F1	R/W	0h	DRAM TPDEX value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TPDEX_F0	R/W	0h	DRAM TPDEX value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.151 EMIF_CTLCFG_DENALI_CTL_90 Register

1 EMIF_CTLCFG_DENALI_CTL_90 Register (Offset = 168h) [reset = 0h]

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Table 14-20397. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8168h**

Figure 14-6764. EMIF_CTLCFG_DENALI_CTL_90 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TMRRI_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TMRRI_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TPDEX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TPDEX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20399. EMIF_CTLCFG_DENALI_CTL_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRRI_F1	R/W	0h	DRAM TMRRI value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TMRRI_F0	R/W	0h	DRAM TMRRI value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	TPDEX_F2	R/W	0h	DRAM TPDEX value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.152 EMIF_CTLCFG_DENALI_CTL_91 Register

1 EMIF_CTLCFG_DENALI_CTL_91 Register (Offset = 16Ch) [reset = 0h]

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Table 14-20400. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 816Ch**

Figure 14-6765. EMIF_CTLCFG_DENALI_CTL_91 Name Register

31	30	29	28	27	26	25	24
RESERVED			TMRWCKEL_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKEHCS_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCKELCS_F0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMRRI_F2							
R/W							
0h							

Table 14-20402. EMIF_CTLCFG_DENALI_CTL_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TMRWCKEL_F0	R/W	0h	DRAM TMRWCKEL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKEHCS_F0	R/W	0h	DRAM TCKEHCS value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELCS_F0	R/W	0h	DRAM TCKELCS value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TMRRI_F2	R/W	0h	DRAM TMRRI value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.153 EMIF_CTLCFG_DENALI_CTL_92 Register

1 EMIF_CTLCFG_DENALI_CTL_92 Register (Offset = 170h) [reset = 0h]

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Table 14-20403. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8170h

Figure 14-6766. EMIF_CTLCFG_DENALI_CTL_92 Name Register

31	30	29	28	27	26	25	24
RESERVED			TMRWCKEL_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKEHCS_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCKELCS_F1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TZQCKE_F0			
NONE				R/W			
0h				0h			

Table 14-20405. EMIF_CTLCFG_DENALI_CTL_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TMRWCKEL_F1	R/W	0h	DRAM TMRWCKEL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKEHCS_F1	R/W	0h	DRAM TCKEHCS value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELCS_F1	R/W	0h	DRAM TCKELCS value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TZQCKE_F0	R/W	0h	DRAM TZQCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.154 EMIF_CTLCFG_DENALI_CTL_93 Register

1 EMIF_CTLCFG_DENALI_CTL_93 Register (Offset = 174h) [reset = 0h]

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Table 14-20406. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8174h

Figure 14-6767. EMIF_CTLCFG_DENALI_CTL_93 Name Register

31	30	29	28	27	26	25	24
RESERVED			TMRWCKEL_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKEHCS_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCKELCS_F2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TZQCKE_F1			
NONE				R/W			
0h				0h			

Table 14-20408. EMIF_CTLCFG_DENALI_CTL_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TMRWCKEL_F2	R/W	0h	DRAM TMRWCKEL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKEHCS_F2	R/W	0h	DRAM TCKEHCS value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELCS_F2	R/W	0h	DRAM TCKELCS value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TZQCKE_F1	R/W	0h	DRAM TZQCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.155 EMIF_CTLCFG_DENALI_CTL_94 Register

1 EMIF_CTLCFG_DENALI_CTL_94 Register (Offset = 178h) [reset = 0h]

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Table 14-20409. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8178h

Figure 14-6768. EMIF_CTLCFG_DENALI_CTL_94 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCSCKE_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							CA_DEFAULT_VAL_F0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			TCSCKE_F0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED				TZQCKE_F2			
NONE				R/W			
0h				0h			

Table 14-20411. EMIF_CTLCFG_DENALI_CTL_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCSCKE_F1	R/W	0h	DRAM TCSCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CA_DEFAULT_VAL_F0	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCSCKE_F0	R/W	0h	DRAM TCSCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TZQCKE_F2	R/W	0h	DRAM TZQCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.156 EMIF_CTLCFG_DENALI_CTL_95 Register

1 EMIF_CTLCFG_DENALI_CTL_95 Register (Offset = 17Ch) [reset = 0h]

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Table 14-20412. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 817Ch**

Figure 14-6769. EMIF_CTLCFG_DENALI_CTL_95 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>CA_DEFAULT_VAL_F2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCSCKE_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CA_DEFAULT_VAL_F1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20414. EMIF_CTLCFG_DENALI_CTL_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	CA_DEFAULT_VAL_F2	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCSCKE_F2	R/W	0h	DRAM TCSCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	CA_DEFAULT_VAL_F1	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.157 EMIF_CTLCFG_DENALI_CTL_96 Register

1 EMIF_CTLCFG_DENALI_CTL_96 Register (Offset = 180h) [reset = 0h]

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Table 14-20415. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8180h**

Figure 14-6770. EMIF_CTLCFG_DENALI_CTL_96 Name Register

31	30	29	28	27	26	25	24
TXSNR_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXSNR_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXSR_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXSR_F0							
R/W							
0h							

Table 14-20417. EMIF_CTLCFG_DENALI_CTL_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXSNR_F0	R/W	0h	DRAM TXSNR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	TXSR_F0	R/W	0h	DRAM TXSR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.158 EMIF_CTLCFG_DENALI_CTL_97 Register

1 EMIF_CTLCFG_DENALI_CTL_97 Register (Offset = 184h) [reset = 0h]

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Table 14-20418. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8184h**

Figure 14-6771. EMIF_CTLCFG_DENALI_CTL_97 Name Register

31	30	29	28	27	26	25	24
TXSNR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TXSNR_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TXSR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TXSR_F1							
R/W							
0h							

Table 14-20420. EMIF_CTLCFG_DENALI_CTL_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXSNR_F1	R/W	0h	DRAM TXSNR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TXSR_F1	R/W	0h	DRAM TXSR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.159 EMIF_CTLCFG_DENALI_CTL_98 Register

1 EMIF_CTLCFG_DENALI_CTL_98 Register (Offset = 188h) [reset = 0h]

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Table 14-20421. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8188h**

Figure 14-6772. EMIF_CTLCFG_DENALI_CTL_98 Name Register

31	30	29	28	27	26	25	24
TXSNR_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TXSNR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TXSR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TXSR_F2							
R/W							
0h							

Table 14-20423. EMIF_CTLCFG_DENALI_CTL_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXSNR_F2	R/W	0h	DRAM TXSNR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	TXSR_F2	R/W	0h	DRAM TXSR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.160 EMIF_CTLCFG_DENALI_CTL_99 Register

1 EMIF_CTLCFG_DENALI_CTL_99 Register (Offset = 18Ch) [reset = 0h]

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Table 14-20424. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 818Ch**

Figure 14-6773. EMIF_CTLCFG_DENALI_CTL_99 Name Register

31	30	29	28	27	26	25	24
TXPR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TXPR_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TXPR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TXPR_F0							
R/W							
0h							

Table 14-20426. EMIF_CTLCFG_DENALI_CTL_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXPR_F1	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TXPR_F0	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.161 EMIF_CTLCFG_DENALI_CTL_100 Register

1 EMIF_CTLCFG_DENALI_CTL_100 Register (Offset = 190h) [reset = 0h]

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Table 14-20427. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8190h**

Figure 14-6774. EMIF_CTLCFG_DENALI_CTL_100 Name Register

31	30	29	28	27	26	25	24
RESERVED					TESCKE_F0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TSR_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXPR_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXPR_F2							
R/W							
0h							

Table 14-20429. EMIF_CTLCFG_DENALI_CTL_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	TESCKE_F0	R/W	0h	DRAM TESCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TSR_F0	R/W	0h	DRAM TSR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	TXPR_F2	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.162 EMIF_CTLCFG_DENALI_CTL_101 Register

1 EMIF_CTLCFG_DENALI_CTL_101 Register (Offset = 194h) [reset = 0h]

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Table 14-20430. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8194h

Figure 14-6775. EMIF_CTLCFG_DENALI_CTL_101 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKCKEL_F0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			TCKEHCMD_F0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			TCKELCMD_F0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCSCKEH_F0				
NONE			R/W				
0h			0h				

Table 14-20432. EMIF_CTLCFG_DENALI_CTL_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKCKEL_F0	R/W	0h	DRAM TCKCKEL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKEHCMD_F0	R/W	0h	DRAM TCKEHCMD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELCMD_F0	R/W	0h	DRAM TCKELCMD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCSCKEH_F0	R/W	0h	DRAM TCSCKEH value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.163 EMIF_CTLCFG_DENALI_CTL_102 Register

1 EMIF_CTLCFG_DENALI_CTL_102 Register (Offset = 198h) [reset = 0h]

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Table 14-20433. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8198h**

Figure 14-6776. EMIF_CTLCFG_DENALI_CTL_102 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCSCKEH_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					TESCKE_F1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TSR_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TCKELPD_F0				
NONE			R/W				
0h			0h				

Table 14-20435. EMIF_CTLCFG_DENALI_CTL_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCSCKEH_F1	R/W	0h	DRAM TCSCKEH value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	TESCKE_F1	R/W	0h	DRAM TESCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TSR_F1	R/W	0h	DRAM TSR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKELPD_F0	R/W	0h	DRAM TCKELPD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.164 EMIF_CTLCFG_DENALI_CTL_103 Register

1 EMIF_CTLCFG_DENALI_CTL_103 Register (Offset = 19Ch) [reset = 0h]

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Table 14-20436. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 819Ch**

Figure 14-6777. EMIF_CTLCFG_DENALI_CTL_103 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKELPD_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			TCKCKEL_F1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			TCKEHCMD_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCKELCMD_F1				
NONE			R/W				
0h			0h				

Table 14-20438. EMIF_CTLCFG_DENALI_CTL_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELPD_F1	R/W	0h	DRAM TCKELPD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKCKEL_F1	R/W	0h	DRAM TCKCKEL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKEHCMD_F1	R/W	0h	DRAM TCKEHCMD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKELCMD_F1	R/W	0h	DRAM TCKELCMD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.165 EMIF_CTLCFG_DENALI_CTL_104 Register

1 EMIF_CTLCFG_DENALI_CTL_104 Register (Offset = 1A0h) [reset = 0h]

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Table 14-20439. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81A0h**

Figure 14-6778. EMIF_CTLCFG_DENALI_CTL_104 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKELCMD_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCSCKEH_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TESCKE_F2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TSR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20441. EMIF_CTLCFG_DENALI_CTL_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELCMD_F2	R/W	0h	DRAM TCKELCMD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCSCKEH_F2	R/W	0h	DRAM TCSCKEH value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TESCKE_F2	R/W	0h	DRAM TESCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TSR_F2	R/W	0h	DRAM TSR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.166 EMIF_CTLCFG_DENALI_CTL_105 Register

1 EMIF_CTLCFG_DENALI_CTL_105 Register (Offset = 1A4h) [reset = 0h]

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Table 14-20442. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 81A4h

Figure 14-6779. EMIF_CTLCFG_DENALI_CTL_105 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCMDCKE_F0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			TCKELPD_F2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			TCKCKEL_F2				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCKEHCMD_F2				
NONE			R/W				
0h			0h				

Table 14-20444. EMIF_CTLCFG_DENALI_CTL_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCMDCKE_F0	R/W	0h	DRAM TCMDCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKELPD_F2	R/W	0h	DRAM TCKELPD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKCKEL_F2	R/W	0h	DRAM TCKCKEL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKEHCMD_F2	R/W	0h	DRAM TCKEHCMD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.167 EMIF_CTLCFG_DENALI_CTL_106 Register

1 EMIF_CTLCFG_DENALI_CTL_106 Register (Offset = 1A8h) [reset = 0h]

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Table 14-20445. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81A8h**

Figure 14-6780. EMIF_CTLCFG_DENALI_CTL_106 Name Register

31	30	29	28	27	26	25	24
RESERVED							SREFRESH_EXIT_NO_REFRESH
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			TCMDCKE_F2				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCMDCKE_F1				
NONE			R/W				
0h			0h				

Table 14-20447. EMIF_CTLCFG_DENALI_CTL_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SREFRESH_EXIT_NO_REFRESH	R/W	0h	Disables the automatic refresh request associated with self-refresh exit. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PWRUP_SREFRESH_EXIT	R/W	0h	Allow powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCMDCKE_F2	R/W	0h	DRAM TCMDCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCMDCKE_F1	R/W	0h	DRAM TCMDCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.168 EMIF_CTLCFG_DENALI_CTL_107 Register

1 EMIF_CTLCFG_DENALI_CTL_107 Register (Offset = 1ACh) [reset = 0h]

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Table 14-20448. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81ACh**

Figure 14-6781. EMIF_CTLCFG_DENALI_CTL_107 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">DFS_STATUS</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DFS_CMD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CKE_DELAY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ENABLE_QUICK_SREFRESH</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20450. EMIF_CTLCFG_DENALI_CTL_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	DFS_STATUS	R/W	0h	Contains status and interrupt information related to DFS. Bit [0] set indicates that the DFS request from the hardware interface was ignored because param_dfs_enable was zero or because another HWI-initiated DFS operation was already in progress. Bit [1] set indicates that a DFS operation initiated by the hardware interface was terminated because the PHY did not deassert dfi_init_complete within tDFI_INIT_START after the controller asserted dfi_init_start. Bit [2] set indicates that a hardware interface initiated DFS operation completed successfully. Bit [3] set indicates that the DFS command on the software interface was ignored either because param_dfs_enable was zero or because another SW-initiated DFS operation was already in progress. Bit [4] set indicates that a DFS operation initiated by the software interface was terminated because the PHY did not deassert dfi_init_complete within tDFI_INIT_START after the controller asserted dfi_init_start. Bit [5] set indicates that a software initiated DFS operation completed successfully. Bit [6] set indicates that the DFS logic entered the software wait state after a DFS operation completed. Clear this bit to allow the logic to exit this wait state. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved

Table 14-20450. EMIF_CTLCFG_DENALI_CTL_107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:16	DFS_CMD	W	0h	It Currently not supported gt DFS software command request interface. Bit [0] sends the DFS exit request when set. Bit [1] sends the DFS enter request when set. Bit [2] tells the controller to gate the memory clock before handing control to the PHY during a DFS operation. Bits [4 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	CKE_DELAY	R/W	0h	Additional cycles to delay CKE for status reporting. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	ENABLE_QUICK_SREFRESH	R/W	0h	Allow user to interrupt memory initialization to enter self-refresh mode. Set to 1 to allow interruption. Reset Source: ctl_amod_g_rst_n

14.6.6.2.169 EMIF_CTLCFG_DENALI_CTL_108 Register

1 EMIF_CTLCFG_DENALI_CTL_108 Register (Offset = 1B0h) [reset = 0h]

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Table 14-20451. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 81B0h

Figure 14-6782. EMIF_CTLCFG_DENALI_CTL_108 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DFS_PROMOTE_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DFS_PROMOTE_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>DFS_ZQ_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20453. EMIF_CTLCFG_DENALI_CTL_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	DFS_PROMOTE_THRESHOLD_F0	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW and HW DFS commands. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DFS_ZQ_EN	R/W	0h	Enables ZQ calibration across all ranks during a DFS exit. Set to 1 to enable. Not valid when operating in ZQ background mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.170 EMIF_CTLCFG_DENALI_CTL_109 Register

1 EMIF_CTLCFG_DENALI_CTL_109 Register (Offset = 1B4h) [reset = 0h]

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Table 14-20454. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81B4h**

Figure 14-6783. EMIF_CTLCFG_DENALI_CTL_109 Name Register

31	30	29	28	27	26	25	24
DFS_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-20456. EMIF_CTLCFG_DENALI_CTL_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DFS_PROMOTE_THRESHOLD_F2	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and HW DFS commands. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	DFS_PROMOTE_THRESHOLD_F1	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW and HW DFS commands. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.171 EMIF_CTLCFG_DENALI_CTL_110 Register

1 EMIF_CTLCFG_DENALI_CTL_110 Register (Offset = 1B8h) [reset = 0h]

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Table 14-20457. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81B8h**

Figure 14-6784. EMIF_CTLCFG_DENALI_CTL_110 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED5							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED					MC_RESERVED4		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED					MC_RESERVED3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					ZQ_STATUS_LOG		
NONE					R		
0h					0h		

Table 14-20459. EMIF_CTLCFG_DENALI_CTL_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED5	R/W	0h	Reserved
23:19	RESERVED	NONE	0h	Reserved
18:16	MC_RESERVED4	R/W	0h	Reserved
15:11	RESERVED	NONE	0h	Reserved
10:8	MC_RESERVED3	R/W	0h	Reserved
7:3	RESERVED	NONE	0h	Reserved
2:0	ZQ_STATUS_LOG	R	0h	Indicates what kind of ZQ command was terminated without execution that caused the ZQ status interrupt to assert. Bit [0] correlates to a ZQ cal init, reset, short or long command. Bit [1] correlates to a ZQ cal start command. Bit [2] correlates to a ZQ cal latch command. Value of 1 indicates that that type of command was received, but terminated without execution. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.172 EMIF_CTLCFG_DENALI_CTL_111 Register

1 EMIF_CTLCFG_DENALI_CTL_111 Register (Offset = 1BCh) [reset = 0h]

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Table 14-20460. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81BCh**

Figure 14-6785. EMIF_CTLCFG_DENALI_CTL_111 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_NORM_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_NORM_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED7							
R/W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED6							
R/W							
0h							

Table 14-20462. EMIF_CTLCFG_DENALI_CTL_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_NORM_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED7	R/W	0h	Reserved
7:0	MC_RESERVED6	R/W	0h	Reserved

14.6.6.2.173 EMIF_CTLCFG_DENALI_CTL_112 Register

1 EMIF_CTLCFG_DENALI_CTL_112 Register (Offset = 1C0h) [reset = 0h]

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Table 14-20463. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81C0h**

Figure 14-6786. EMIF_CTLCFG_DENALI_CTL_112 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_TIMEOUT_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_TIMEOUT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_HIGH_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_HIGH_THRESHOLD_F0							
R/W							
0h							

Table 14-20465. EMIF_CTLCFG_DENALI_CTL_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_TIMEOUT_F0	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_HIGH_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.174 EMIF_CTLCFG_DENALI_CTL_113 Register

1 EMIF_CTLCFG_DENALI_CTL_113 Register (Offset = 1C4h) [reset = 0h]

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Table 14-20466. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81C4h**

Figure 14-6787. EMIF_CTLCFG_DENALI_CTL_113 Name Register

31	30	29	28	27	26	25	24
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-20468. EMIF_CTLCFG_DENALI_CTL_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.175 EMIF_CTLCFG_DENALI_CTL_114 Register

1 EMIF_CTLCFG_DENALI_CTL_114 Register (Offset = 1C8h) [reset = 0h]

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Table 14-20469. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81C8h**

Figure 14-6788. EMIF_CTLCFG_DENALI_CTL_114 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_HIGH_THRESHOLD_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_CTRLUPD_HIGH_THRESHOLD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_CTRLUPD_NORM_THRESHOLD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPD_CTRLUPD_NORM_THRESHOLD_F1							
R/W							
0h							

Table 14-20471. EMIF_CTLCFG_DENALI_CTL_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_HIGH_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_NORM_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.176 EMIF_CTLCFG_DENALI_CTL_115 Register

1 EMIF_CTLCFG_DENALI_CTL_115 Register (Offset = 1CCh) [reset = 0h]

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Table 14-20472. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81CCh**

Figure 14-6789. EMIF_CTLCFG_DENALI_CTL_115 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_TIMEOUT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_TIMEOUT_F1							
R/W							
0h							

Table 14-20474. EMIF_CTLCFG_DENALI_CTL_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_TIMEOUT_F1	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.177 EMIF_CTLCFG_DENALI_CTL_116 Register

1 EMIF_CTLCFG_DENALI_CTL_116 Register (Offset = 1D0h) [reset = 0h]

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Table 14-20475. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81D0h**

Figure 14-6790. EMIF_CTLCFG_DENALI_CTL_116 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_NORM_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_CTRLUPD_NORM_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-20477. EMIF_CTLCFG_DENALI_CTL_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_NORM_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.178 EMIF_CTLCFG_DENALI_CTL_117 Register

1 EMIF_CTLCFG_DENALI_CTL_117 Register (Offset = 1D4h) [reset = 0h]

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Table 14-20478. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81D4h**

Figure 14-6791. EMIF_CTLCFG_DENALI_CTL_117 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_TIMEOUT_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_CTRLUPD_TIMEOUT_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_CTRLUPD_HIGH_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPD_CTRLUPD_HIGH_THRESHOLD_F2							
R/W							
0h							

Table 14-20480. EMIF_CTLCFG_DENALI_CTL_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_TIMEOUT_F2	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_HIGH_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.179 EMIF_CTLCFG_DENALI_CTL_118 Register

1 EMIF_CTLCFG_DENALI_CTL_118 Register (Offset = 1D8h) [reset = 0h]

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Table 14-20481. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81D8h**

Figure 14-6792. EMIF_CTLCFG_DENALI_CTL_118 Name Register

31	30	29	28	27	26	25	24
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-20483. EMIF_CTLCFG_DENALI_CTL_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.180 EMIF_CTLCFG_DENALI_CTL_119 Register

1 EMIF_CTLCFG_DENALI_CTL_119 Register (Offset = 1DCh) [reset = 0h]

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Table 14-20484. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81DCh**

Figure 14-6793. EMIF_CTLCFG_DENALI_CTL_119 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							

Table 14-20486. EMIF_CTLCFG_DENALI_CTL_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F0	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.181 EMIF_CTLCFG_DENALI_CTL_120 Register

1 EMIF_CTLCFG_DENALI_CTL_120 Register (Offset = 1E0h) [reset = 0h]

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Table 14-20487. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 81E0h

Figure 14-6794. EMIF_CTLCFG_DENALI_CTL_120 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							

Table 14-20489. EMIF_CTLCFG_DENALI_CTL_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.182 EMIF_CTLCFG_DENALI_CTL_121 Register

1 EMIF_CTLCFG_DENALI_CTL_121 Register (Offset = 1E4h) [reset = 0h]

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Table 14-20490. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81E4h**

Figure 14-6795. EMIF_CTLCFG_DENALI_CTL_121 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							

Table 14-20492. EMIF_CTLCFG_DENALI_CTL_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.183 EMIF_CTLCFG_DENALI_CTL_122 Register

1 EMIF_CTLCFG_DENALI_CTL_122 Register (Offset = 1E8h) [reset = 0h]

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Table 14-20493. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81E8h**

Figure 14-6796. EMIF_CTLCFG_DENALI_CTL_122 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							

Table 14-20495. EMIF_CTLCFG_DENALI_CTL_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.184 EMIF_CTLCFG_DENALI_CTL_123 Register

1 EMIF_CTLCFG_DENALI_CTL_123 Register (Offset = 1ECh) [reset = 0h]

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Table 14-20496. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 81ECh

Figure 14-6797. EMIF_CTLCFG_DENALI_CTL_123 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							

Table 14-20498. EMIF_CTLCFG_DENALI_CTL_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.185 EMIF_CTLCFG_DENALI_CTL_124 Register

1 EMIF_CTLCFG_DENALI_CTL_124 Register (Offset = 1F0h) [reset = 0h]

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Table 14-20499. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81F0h**

Figure 14-6798. EMIF_CTLCFG_DENALI_CTL_124 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-20501. EMIF_CTLCFG_DENALI_CTL_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.186 EMIF_CTLCFG_DENALI_CTL_125 Register

1 EMIF_CTLCFG_DENALI_CTL_125 Register (Offset = 1F4h) [reset = 0h]

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Table 14-20502. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81F4h**

Figure 14-6799. EMIF_CTLCFG_DENALI_CTL_125 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TDFI_PHYMSTR_RESP_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_RESP_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_RESP_F0							
R/W							
0h							

Table 14-20504. EMIF_CTLCFG_DENALI_CTL_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F0	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.187 EMIF_CTLCFG_DENALI_CTL_126 Register

1 EMIF_CTLCFG_DENALI_CTL_126 Register (Offset = 1F8h) [reset = 0h]

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Table 14-20505. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81F8h**

Figure 14-6800. EMIF_CTLCFG_DENALI_CTL_126 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F1							
R/W							
0h							

Table 14-20507. EMIF_CTLCFG_DENALI_CTL_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F1	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.188 EMIF_CTLCFG_DENALI_CTL_127 Register

1 EMIF_CTLCFG_DENALI_CTL_127 Register (Offset = 1FCh) [reset = 0h]

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Table 14-20508. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 81FCh**

Figure 14-6801. EMIF_CTLCFG_DENALI_CTL_127 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							

Table 14-20510. EMIF_CTLCFG_DENALI_CTL_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.189 EMIF_CTLCFG_DENALI_CTL_128 Register

1 EMIF_CTLCFG_DENALI_CTL_128 Register (Offset = 200h) [reset = 0h]

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Table 14-20511. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8200h**

Figure 14-6802. EMIF_CTLCFG_DENALI_CTL_128 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							

Table 14-20513. EMIF_CTLCFG_DENALI_CTL_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.190 EMIF_CTLCFG_DENALI_CTL_129 Register

1 EMIF_CTLCFG_DENALI_CTL_129 Register (Offset = 204h) [reset = 0h]

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Table 14-20514. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8204h**

Figure 14-6803. EMIF_CTLCFG_DENALI_CTL_129 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							

Table 14-20516. EMIF_CTLCFG_DENALI_CTL_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.191 EMIF_CTLCFG_DENALI_CTL_130 Register

1 EMIF_CTLCFG_DENALI_CTL_130 Register (Offset = 208h) [reset = 0h]

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Table 14-20517. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8208h

Figure 14-6804. EMIF_CTLCFG_DENALI_CTL_130 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							

Table 14-20519. EMIF_CTLCFG_DENALI_CTL_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.192 EMIF_CTLCFG_DENALI_CTL_131 Register

1 EMIF_CTLCFG_DENALI_CTL_131 Register (Offset = 20Ch) [reset = 0h]

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Table 14-20520. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 820Ch**

Figure 14-6805. EMIF_CTLCFG_DENALI_CTL_131 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-20522. EMIF_CTLCFG_DENALI_CTL_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.193 EMIF_CTLCFG_DENALI_CTL_132 Register

1 EMIF_CTLCFG_DENALI_CTL_132 Register (Offset = 210h) [reset = 0h]

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Table 14-20523. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8210h**

Figure 14-6806. EMIF_CTLCFG_DENALI_CTL_132 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TDFI_PHYMSTR_RESP_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_RESP_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_RESP_F1							
R/W							
0h							

Table 14-20525. EMIF_CTLCFG_DENALI_CTL_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F1	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.194 EMIF_CTLCFG_DENALI_CTL_133 Register

1 EMIF_CTLCFG_DENALI_CTL_133 Register (Offset = 214h) [reset = 0h]

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Table 14-20526. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8214h**

Figure 14-6807. EMIF_CTLCFG_DENALI_CTL_133 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							

Table 14-20528. EMIF_CTLCFG_DENALI_CTL_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F2	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.195 EMIF_CTLCFG_DENALI_CTL_134 Register

1 EMIF_CTLCFG_DENALI_CTL_134 Register (Offset = 218h) [reset = 0h]

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Table 14-20529. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8218h**

Figure 14-6808. EMIF_CTLCFG_DENALI_CTL_134 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							

Table 14-20531. EMIF_CTLCFG_DENALI_CTL_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.196 EMIF_CTLCFG_DENALI_CTL_135 Register

1 EMIF_CTLCFG_DENALI_CTL_135 Register (Offset = 21Ch) [reset = 0h]

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Table 14-20532. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 821Ch**

Figure 14-6809. EMIF_CTLCFG_DENALI_CTL_135 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							

Table 14-20534. EMIF_CTLCFG_DENALI_CTL_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.197 EMIF_CTLCFG_DENALI_CTL_136 Register

1 EMIF_CTLCFG_DENALI_CTL_136 Register (Offset = 220h) [reset = 0h]

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Table 14-20535. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8220h**

Figure 14-6810. EMIF_CTLCFG_DENALI_CTL_136 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							

Table 14-20537. EMIF_CTLCFG_DENALI_CTL_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.198 EMIF_CTLCFG_DENALI_CTL_137 Register

1 EMIF_CTLCFG_DENALI_CTL_137 Register (Offset = 224h) [reset = 0h]

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Table 14-20538. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8224h**

Figure 14-6811. EMIF_CTLCFG_DENALI_CTL_137 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							

Table 14-20540. EMIF_CTLCFG_DENALI_CTL_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.199 EMIF_CTLCFG_DENALI_CTL_138 Register

1 EMIF_CTLCFG_DENALI_CTL_138 Register (Offset = 228h) [reset = 0h]

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Table 14-20541. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8228h**

Figure 14-6812. EMIF_CTLCFG_DENALI_CTL_138 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-20543. EMIF_CTLCFG_DENALI_CTL_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.200 EMIF_CTLCFG_DENALI_CTL_139 Register

1 EMIF_CTLCFG_DENALI_CTL_139 Register (Offset = 22Ch) [reset = 0h]

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Table 14-20544. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 822Ch**

Figure 14-6813. EMIF_CTLCFG_DENALI_CTL_139 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHYMSTR_NO_AREF</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20546. EMIF_CTLCFG_DENALI_CTL_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHYMSTR_NO_AREF	R/W	0h	isables refreshes during the PHY controller interface sequence. Set to 1 to disable. Refreshes during reset are only supported for DFI 4.0 and this parameter may be set or cleared for DFI 4.0. For all other DFI versions, this parameter must be set to 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F2	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.201 EMIF_CTLCFG_DENALI_CTL_140 Register

1 EMIF_CTLCFG_DENALI_CTL_140 Register (Offset = 230h) [reset = 0h]

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Table 14-20547. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8230h**

Figure 14-6814. EMIF_CTLCFG_DENALI_CTL_140 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHYMSTR_TRAIN_AFTER_INIT_COMPLETE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHYMSTR_DFI_VERSION_4P0V1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PHYMSTR_ERROR_STATUS	
NONE						R	
0h						0h	

Table 14-20549. EMIF_CTLCFG_DENALI_CTL_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHYMSTR_TRAIN_AFTER_INIT_COMPLETE	R/W	0h	Defines how the PHY will use the PHY Controller Interface for training. Clear to 0 to perform training without the PHY Controller Interface, or set to 1 to use the PHY Controller Interface to gain control over the DFI bus after the dfi_init_complete signal assertion for the initial training. Default is cleared to 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHYMSTR_DFI_VERSION_4P0V1	R/W	0h	Defines the version of the DFI 4.0 specification supported. Clear to 0 for DFI 4.0 version 2 PHY Controller Interface, or set to 1 for DFI 4.0 version 1 PHY Controller Interface. Default is cleared to 0 for version 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-20549. EMIF_CTLCFG_DENALI_CTL_140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PHYMSTR_ERROR_STATUS	R	0h	Identifies the source of any DFI PHY Controller Interface errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit [0] set indicates a TDFI_PHYMSTR_MAX or TDFI_PHYMSTR_TYPEn_MAX parmaeter violation and bit [1] set indicates a TDFI_PHYMSTR_RESP parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.202 EMIF_CTLCFG_DENALI_CTL_141 Register

1 EMIF_CTLCFG_DENALI_CTL_141 Register (Offset = 234h) [reset = 0h]

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Table 14-20550. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8234h**

Figure 14-6815. EMIF_CTLCFG_DENALI_CTL_141 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							

Table 14-20552. EMIF_CTLCFG_DENALI_CTL_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.203 EMIF_CTLCFG_DENALI_CTL_142 Register

1 EMIF_CTLCFG_DENALI_CTL_142 Register (Offset = 238h) [reset = 0h]

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Table 14-20553. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8238h**

Figure 14-6816. EMIF_CTLCFG_DENALI_CTL_142 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							

Table 14-20555. EMIF_CTLCFG_DENALI_CTL_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.204 EMIF_CTLCFG_DENALI_CTL_143 Register

1 EMIF_CTLCFG_DENALI_CTL_143 Register (Offset = 23Ch) [reset = 0h]

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Table 14-20556. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 823Ch**

Figure 14-6817. EMIF_CTLCFG_DENALI_CTL_143 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							

Table 14-20558. EMIF_CTLCFG_DENALI_CTL_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_TIMEOUT_F0	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.205 EMIF_CTLCFG_DENALI_CTL_144 Register

1 EMIF_CTLCFG_DENALI_CTL_144 Register (Offset = 240h) [reset = 0h]

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Table 14-20559. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8240h**

Figure 14-6818. EMIF_CTLCFG_DENALI_CTL_144 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							

Table 14-20561. EMIF_CTLCFG_DENALI_CTL_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.206 EMIF_CTLCFG_DENALI_CTL_145 Register

1 EMIF_CTLCFG_DENALI_CTL_145 Register (Offset = 244h) [reset = 0h]

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Table 14-20562. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8244h**

Figure 14-6819. EMIF_CTLCFG_DENALI_CTL_145 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-20564. EMIF_CTLCFG_DENALI_CTL_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.207 EMIF_CTLCFG_DENALI_CTL_146 Register

1 EMIF_CTLCFG_DENALI_CTL_146 Register (Offset = 248h) [reset = 0h]

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Table 14-20565. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8248h**

Figure 14-6820. EMIF_CTLCFG_DENALI_CTL_146 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							

Table 14-20567. EMIF_CTLCFG_DENALI_CTL_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_TIMEOUT_F1	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.208 EMIF_CTLCFG_DENALI_CTL_147 Register

1 EMIF_CTLCFG_DENALI_CTL_147 Register (Offset = 24Ch) [reset = 0h]

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Table 14-20568. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 824Ch**

Figure 14-6821. EMIF_CTLCFG_DENALI_CTL_147 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							

Table 14-20570. EMIF_CTLCFG_DENALI_CTL_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.209 EMIF_CTLCFG_DENALI_CTL_148 Register

1 EMIF_CTLCFG_DENALI_CTL_148 Register (Offset = 250h) [reset = 0h]

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Table 14-20571. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8250h**

Figure 14-6822. EMIF_CTLCFG_DENALI_CTL_148 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							

Table 14-20573. EMIF_CTLCFG_DENALI_CTL_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.210 EMIF_CTLCFG_DENALI_CTL_149 Register

1 EMIF_CTLCFG_DENALI_CTL_149 Register (Offset = 254h) [reset = 0h]

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Table 14-20574. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8254h**

Figure 14-6823. EMIF_CTLCFG_DENALI_CTL_149 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PPR_CONTROL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MRR_TEMPCHK_TIMEOUT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MRR_TEMPCHK_TIMEOUT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MRR_TEMPCHK_TIMEOUT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20576. EMIF_CTLCFG_DENALI_CTL_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PPR_CONTROL	R/W	0h	Enables the post-package repair feature. Set to 1 to enable. This parameter may only be programmed before initialization begins. Reset Source: ctl_amod_g_rst_n
23:0	MRR_TEMPCHK_TIMEOUT_F2	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.211 EMIF_CTLCFG_DENALI_CTL_150 Register

1 EMIF_CTLCFG_DENALI_CTL_150 Register (Offset = 258h) [reset = 0h]

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Table 14-20577. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8258h**

Figure 14-6824. EMIF_CTLCFG_DENALI_CTL_150 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PPR_COMMAND_MRW_REGNUM							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PPR_COMMAND		
NONE					W		
0h					0h		

Table 14-20579. EMIF_CTLCFG_DENALI_CTL_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PPR_COMMAND_MRW_REGNUM	R/W	0h	Specifies the mode register to be used. Clear to 0 for MRW0 or program to 4 for MRW4. All other values are reserved.. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PPR_COMMAND	W	0h	Specifies the type of PPR command. Program to 1 for pre-charge all, program to 2 for MRW, program to 3 for activate, or program to 5 for write. All other values are reserved. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.212 EMIF_CTLCFG_DENALI_CTL_151 Register

1 EMIF_CTLCFG_DENALI_CTL_151 Register (Offset = 25Ch) [reset = 0h]

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Table 14-20580. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 825Ch**

Figure 14-6825. EMIF_CTLCFG_DENALI_CTL_151 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PPR_COMMAND_MRW_DATA
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PPR_COMMAND_MRW_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPR_COMMAND_MRW_DATA							
R/W							
0h							

Table 14-20582. EMIF_CTLCFG_DENALI_CTL_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PPR_COMMAND_MRW_DATA	R/W	0h	Specifies the data for the mode register write. Reset Source: ctl_amod_g_rst_n

14.6.6.2.213 EMIF_CTLCFG_DENALI_CTL_152 Register

1 EMIF_CTLCFG_DENALI_CTL_152 Register (Offset = 260h) [reset = 0h]

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Table 14-20583. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8260h**

Figure 14-6826. EMIF_CTLCFG_DENALI_CTL_152 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PPR_BANK_ADDRESS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PPR_ROW_ADDRESS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PPR_ROW_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PPR_ROW_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20585. EMIF_CTLCFG_DENALI_CTL_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PPR_BANK_ADDRESS	R/W	0h	Specifies the bank for the row to be repaired. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:0	PPR_ROW_ADDRESS	R/W	0h	Specifies the encoded row address to be repaired. Reset Source: ctl_amod_g_rst_n

14.6.6.2.214 EMIF_CTLCFG_DENALI_CTL_153 Register

1 EMIF_CTLCFG_DENALI_CTL_153 Register (Offset = 264h) [reset = 0h]

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Table 14-20586. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8264h**

Figure 14-6827. EMIF_CTLCFG_DENALI_CTL_153 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PPR_CS_ADDRESS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20588. EMIF_CTLCFG_DENALI_CTL_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PPR_CS_ADDRESS	R/W	0h	Specifies the chip select for the row to be repaired. Reset Source: ctl_amod_g_rst_n

14.6.6.2.215 EMIF_CTLCFG_DENALI_CTL_154 Register

1 EMIF_CTLCFG_DENALI_CTL_154 Register (Offset = 268h) [reset = 0h]

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Table 14-20589. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8268h**

Figure 14-6828. EMIF_CTLCFG_DENALI_CTL_154 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_0							
R/W							
0h							

Table 14-20591. EMIF_CTLCFG_DENALI_CTL_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_0	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.6.6.2.216 EMIF_CTLCFG_DENALI_CTL_155 Register

1 EMIF_CTLCFG_DENALI_CTL_155 Register (Offset = 26Ch) [reset = 0h]

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Table 14-20592. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 826Ch**

Figure 14-6829. EMIF_CTLCFG_DENALI_CTL_155 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_1							
R/W							
0h							

Table 14-20594. EMIF_CTLCFG_DENALI_CTL_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_1	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.6.6.2.217 EMIF_CTLCFG_DENALI_CTL_156 Register

1 EMIF_CTLCFG_DENALI_CTL_156 Register (Offset = 270h) [reset = 0h]

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Table 14-20595. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8270h**

Figure 14-6830. EMIF_CTLCFG_DENALI_CTL_156 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_2							
R/W							
0h							

Table 14-20597. EMIF_CTLCFG_DENALI_CTL_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_2	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.6.6.2.218 EMIF_CTLCFG_DENALI_CTL_157 Register

1 EMIF_CTLCFG_DENALI_CTL_157 Register (Offset = 274h) [reset = 0h]

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Table 14-20598. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8274h**

Figure 14-6831. EMIF_CTLCFG_DENALI_CTL_157 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_3							
R/W							
0h							

Table 14-20600. EMIF_CTLCFG_DENALI_CTL_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_3	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.6.6.2.219 EMIF_CTLCFG_DENALI_CTL_158 Register

1 EMIF_CTLCFG_DENALI_CTL_158 Register (Offset = 278h) [reset = 0h]

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Table 14-20601. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8278h**

Figure 14-6832. EMIF_CTLCFG_DENALI_CTL_158 Name Register

31	30	29	28	27	26	25	24
CKSRX_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CKSRE_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							FM_OVRIDE_CONTROL
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PPR_STATUS	
NONE						R	
0h						0h	

Table 14-20603. EMIF_CTLCFG_DENALI_CTL_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CKSRX_F0	R/W	0h	Clock stable delay on self-refresh exit. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	CKSRE_F0	R/W	0h	Clock hold delay on self-refresh entry. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	FM_OVRIDE_CONTROL	R/W	0h	Enables the FM Override feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PPR_STATUS	R	0h	Reports the status of the PPR operation. Bit [0] set indicates that PPR operations are now allowed and bit [1] set indicates if the last PPR command is complete. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.220 EMIF_CTLCFG_DENALI_CTL_159 Register

1 EMIF_CTLCFG_DENALI_CTL_159 Register (Offset = 27Ch) [reset = 0h]

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Table 14-20604. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 827Ch**

Figure 14-6833. EMIF_CTLCFG_DENALI_CTL_159 Name Register

31	30	29	28	27	26	25	24
CKSRX_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
CKSRE_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
CKSRX_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
CKSRE_F1							
R/W							
0h							

Table 14-20606. EMIF_CTLCFG_DENALI_CTL_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CKSRX_F2	R/W	0h	Clock stable delay on self-refresh exit. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	CKSRE_F2	R/W	0h	Clock hold delay on self-refresh entry. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	CKSRX_F1	R/W	0h	Clock stable delay on self-refresh exit. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	CKSRE_F1	R/W	0h	Clock hold delay on self-refresh entry. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.221 EMIF_CTLCFG_DENALI_CTL_160 Register

1 EMIF_CTLCFG_DENALI_CTL_160 Register (Offset = 280h) [reset = 0h]

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Table 14-20607. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8280h**

Figure 14-6834. EMIF_CTLCFG_DENALI_CTL_160 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_SHORT_WAKEUP_F0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_IDLE_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	LP_CMD						
NONE	W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LOWPOWER_REFRESH_ENABLE	
NONE						R/W	
0h						0h	

Table 14-20609. EMIF_CTLCFG_DENALI_CTL_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SR_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_IDLE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=0 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	LP_CMD	W	0h	Low power software command request interface. Bit [0] controls exit, bit [1] controls entry, bits [4:2] define the low power state, bit [5] controls memory clock gating, bit [6] controls controller clock gating, and bit [7] controls lock. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-20609. EMIF_CTLCFG_DENALI_CTL_160 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	LOWPOWER_REFRESH_ENABLE	R/W	0h	Enable refreshes while in low power mode. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.222 EMIF_CTLCFG_DENALI_CTL_161 Register

1 EMIF_CTLCFG_DENALI_CTL_161 Register (Offset = 284h) [reset = 0h]

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Table 14-20610. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8284h**

Figure 14-6835. EMIF_CTLCFG_DENALI_CTL_161 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_SHORT_WAKEUP_F0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_PD_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LPI_SR_LONG_WAKEUP_F0			
NONE				R/W			
0h				0h			

Table 14-20612. EMIF_CTLCFG_DENALI_CTL_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SRPD_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_PD_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SR_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.223 EMIF_CTLCFG_DENALI_CTL_162 Register

1 EMIF_CTLCFG_DENALI_CTL_162 Register (Offset = 288h) [reset = 0h]

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Table 14-20613. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8288h**

Figure 14-6836. EMIF_CTLCFG_DENALI_CTL_162 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_IDLE_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_TIMER_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LPI_SRPD_LONG_WAKEUP_F0			
NONE				R/W			
0h				0h			

Table 14-20615. EMIF_CTLCFG_DENALI_CTL_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_IDLE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_TIMER_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SRPD_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.224 EMIF_CTLCFG_DENALI_CTL_163 Register

1 EMIF_CTLCFG_DENALI_CTL_163 Register (Offset = 28Ch) [reset = 0h]

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Table 14-20616. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 828Ch**

Figure 14-6837. EMIF_CTLCFG_DENALI_CTL_163 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_PD_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_LONG_WAKEUP_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SR_SHORT_WAKEUP_F1			
NONE				R/W			
0h				0h			

Table 14-20618. EMIF_CTLCFG_DENALI_CTL_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_PD_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-20618. EMIF_CTLCFG_DENALI_CTL_163 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	LPI_SR_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.225 EMIF_CTLCFG_DENALI_CTL_164 Register

1 EMIF_CTLCFG_DENALI_CTL_164 Register (Offset = 290h) [reset = 0h]

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Table 14-20619. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8290h**

Figure 14-6838. EMIF_CTLCFG_DENALI_CTL_164 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_TIMER_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_SRPD_LONG_WAKEUP_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LPI_SRPD_SHORT_WAKEUP_F1			
NONE				R/W			
0h				0h			

Table 14-20621. EMIF_CTLCFG_DENALI_CTL_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_TIMER_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SRPD_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.226 EMIF_CTLCFG_DENALI_CTL_165 Register

1 EMIF_CTLCFG_DENALI_CTL_165 Register (Offset = 294h) [reset = 0h]

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Table 14-20622. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8294h**

Figure 14-6839. EMIF_CTLCFG_DENALI_CTL_165 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_LONG_WAKEUP_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_SHORT_WAKEUP_F2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_IDLE_WAKEUP_F2			
NONE				R/W			
0h				0h			

Table 14-20624. EMIF_CTLCFG_DENALI_CTL_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SR_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_IDLE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.227 EMIF_CTLCFG_DENALI_CTL_166 Register

1 EMIF_CTLCFG_DENALI_CTL_166 Register (Offset = 298h) [reset = 0h]

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Table 14-20625. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8298h**

Figure 14-6840. EMIF_CTLCFG_DENALI_CTL_166 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SRPD_LONG_WAKEUP_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SRPD_SHORT_WAKEUP_F2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_PD_WAKEUP_F2			
NONE				R/W			
0h				0h			

Table 14-20627. EMIF_CTLCFG_DENALI_CTL_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SRPD_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_PD_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.228 EMIF_CTLCFG_DENALI_CTL_167 Register

1 EMIF_CTLCFG_DENALI_CTL_167 Register (Offset = 29Ch) [reset = 0h]

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Table 14-20628. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 829Ch**

Figure 14-6841. EMIF_CTLCFG_DENALI_CTL_167 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							LPI_CTRL_REQ_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		LPI_WAKEUP_EN					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LPI_TIMER_WAKEUP_F2			
NONE				R/W			
0h				0h			

Table 14-20630. EMIF_CTLCFG_DENALI_CTL_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	LPI_CTRL_REQ_EN	R/W	0h	Enables the dfi_lpi_ctrl_req signal for the LPI. This signal is only relevant for DFI versions 3.1 and beyond. Set to 1 to enable or clear to 0 to disable. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	LPI_WAKEUP_EN	R/W	0h	Enables the various low power state wakeup parameters for LPI request uses. Bit [0] enables controller idle wakeup, bit [1] enables power-down wakeup, bit [2] enables either self-refresh short, self-refresh long with or without mem clk gating, either self-refresh power-down short, or self-refresh power-down long with or without mem clk gating, bit [3] enables self-refresh long with mem and ctlr clk gating or self-refresh power-down long with mem and ctlr clk gating, bit [4] enables the LPI timer expire wakeup, and bit [5] is reserved. Set each bit to 1 to enable the respective LP_WAKEUP value for the LPI request. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_TIMER_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.229 EMIF_CTLCFG_DENALI_CTL_168 Register

1 EMIF_CTLCFG_DENALI_CTL_168 Register (Offset = 2A0h) [reset = 0h]

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Table 14-20631. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82A0h**

Figure 14-6842. EMIF_CTLCFG_DENALI_CTL_168 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_WAKEUP_TIMEOUT			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPI_WAKEUP_TIMEOUT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_TIMER_COUNT			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LPI_TIMER_COUNT							
R/W							
0h							

Table 14-20633. EMIF_CTLCFG_DENALI_CTL_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	LPI_WAKEUP_TIMEOUT	R/W	0h	Defines the LPI timeout time, the maximum cycles between a dfi_lp_req de-assertion and a dfi_lp_ack de-assertion. If this value is exceeded, an interrupt will occur. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	LPI_TIMER_COUNT	R/W	0h	Defines the LPI timer count. Reset Source: ctl_amod_g_rst_n

14.6.6.2.230 EMIF_CTLCFG_DENALI_CTL_169 Register

1 EMIF_CTLCFG_DENALI_CTL_169 Register (Offset = 2A4h) [reset = 4000h]

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Table 14-20634. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 82A4h

Figure 14-6843. EMIF_CTLCFG_DENALI_CTL_169 Name Register

31	30	29	28	27	26	25	24
RESERVED				LP_AUTO_EXIT_EN			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LP_AUTO_ENTRY_EN			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	LP_STATE						
NONE	R						
0h	40h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TDFI_LP_RESP		
NONE					R/W		
0h					0h		

Table 14-20636. EMIF_CTLCFG_DENALI_CTL_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LP_AUTO_EXIT_EN	R/W	0h	Enable auto exit from each of the low power states when a read or write command enters the command queue. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, bit [2] controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit [3] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LP_AUTO_ENTRY_EN	R/W	0h	Enable auto entry into each of the low power states when the associated idle timer expires. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, bit [2] controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit [3] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	LP_STATE	R	40h	Low power state status parameter. Bits [5:0] indicate the current low power state and bit [6] set indicates that status bits are valid. READ-ONLY Reset Source: ctl_amod_g_rst_n

Table 14-20636. EMIF_CTLCFG_DENALI_CTL_169 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2:0	TDFI_LP_RESP	R/W	0h	Defines the DFI tLP_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_lp_req assertion and a dfi_lp_ack assertion. Reset Source: ctl_amod_g_rst_n

14.6.6.2.231 EMIF_CTLCFG_DENALI_CTL_170 Register

1 EMIF_CTLCFG_DENALI_CTL_170 Register (Offset = 2A8h) [reset = 0h]

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Table 14-20637. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82A8h**

Figure 14-6844. EMIF_CTLCFG_DENALI_CTL_170 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LP_AUTO_PD_IDLE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LP_AUTO_PD_IDLE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					LP_AUTO_MEM_GATE_EN		
NONE					R/W		
0h					0h		

Table 14-20639. EMIF_CTLCFG_DENALI_CTL_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	LP_AUTO_PD_IDLE	R/W	0h	Defines the idle time [in controller clocks] until the controller will automatically issue an entry into one of the power-down low power states. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	LP_AUTO_MEM_GATE_EN	R/W	0h	Enable memory clock gating when entering a low power state via the auto low power counters. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, and bit [2] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.232 EMIF_CTLCFG_DENALI_CTL_171 Register

1 EMIF_CTLCFG_DENALI_CTL_171 Register (Offset = 2ACh) [reset = 0h]

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Table 14-20640. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82ACh**

Figure 14-6845. EMIF_CTLCFG_DENALI_CTL_171 Name Register

31	30	29	28	27	26	25	24
LP_AUTO_SR_LONG_MC_GATE_IDLE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LP_AUTO_SR_LONG_IDLE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LP_AUTO_SR_SHORT_IDLE			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LP_AUTO_SR_SHORT_IDLE							
R/W							
0h							

Table 14-20642. EMIF_CTLCFG_DENALI_CTL_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	LP_AUTO_SR_LONG_MC_GATE_IDLE	R/W	0h	Defines the idle time [in long counts] until the controller will automatically issue an entry into the self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating low power states. Reset Source: ctl_amod_g_rst_n
23:16	LP_AUTO_SR_LONG_IDLE	R/W	0h	Defines the idle time [in long counts] until the controller will automatically issue an entry into the self-refresh long or self-refresh power-down long [with or without memory clock gating] low power states. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	LP_AUTO_SR_SHORT_IDLE	R/W	0h	Defines the idle time [in controller clocks] until the controller will automatically issue an entry into the self-refresh short or self-refresh power-down short [with or without memory clock gating] low power states. Reset Source: ctl_amod_g_rst_n

14.6.6.2.233 EMIF_CTLCFG_DENALI_CTL_172 Register

1 EMIF_CTLCFG_DENALI_CTL_172 Register (Offset = 2B0h) [reset = 0h]

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Table 14-20643. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82B0h**

Figure 14-6846. EMIF_CTLCFG_DENALI_CTL_172 Name Register

31	30	29	28	27	26	25	24
HW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-20645. EMIF_CTLCFG_DENALI_CTL_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HW_PROMOTE_THRESHOLD_F1	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	HW_PROMOTE_THRESHOLD_F0	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.234 EMIF_CTLCFG_DENALI_CTL_173 Register

1 EMIF_CTLCFG_DENALI_CTL_173 Register (Offset = 2B4h) [reset = 0h]

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Table 14-20646. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82B4h**

Figure 14-6847. EMIF_CTLCFG_DENALI_CTL_173 Name Register

31	30	29	28	27	26	25	24
LPC_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPC_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HW_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-20648. EMIF_CTLCFG_DENALI_CTL_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LPC_PROMOTE_THRESHOLD_F0	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 4. Applies to SW and auto low power commands. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	HW_PROMOTE_THRESHOLD_F2	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.235 EMIF_CTLCFG_DENALI_CTL_174 Register

1 EMIF_CTLCFG_DENALI_CTL_174 Register (Offset = 2B8h) [reset = 0h]

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Table 14-20649. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82B8h**

Figure 14-6848. EMIF_CTLCFG_DENALI_CTL_174 Name Register

31	30	29	28	27	26	25	24
LPC_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
LPC_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
LPC_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
LPC_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-20651. EMIF_CTLCFG_DENALI_CTL_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LPC_PROMOTE_THRESHOLD_F2	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 4. Applies to SW and auto low power commands. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	LPC_PROMOTE_THRESHOLD_F1	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 4. Applies to SW and auto low power commands. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.236 EMIF_CTLCFG_DENALI_CTL_175 Register

1 EMIF_CTLCFG_DENALI_CTL_175 Register (Offset = 2BCh) [reset = 0h]

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Table 14-20652. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82BCh**

Figure 14-6849. EMIF_CTLCFG_DENALI_CTL_175 Name Register

31	30	29	28	27	26	25	24
RESERVED							LPC_SR_EXIT_CMD_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							LPC_SR_PHYMSTR_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							LPC_SR_PHYUPD_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							LPC_SR_CTRLUPD_EN
NONE							R/W
0h							0h

Table 14-20654. EMIF_CTLCFG_DENALI_CTL_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	LPC_SR_EXIT_CMD_EN	R/W	0h	Enable LPC to execute any of the commands on self-refresh exit while exiting. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	LPC_SR_PHYMSTR_EN	R/W	0h	Enable LPC to execute a DFI PHY Controller request on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	LPC_SR_PHYUPD_EN	R/W	0h	Enable LPC to execute a DFI PHY update on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	LPC_SR_CTRLUPD_EN	R/W	0h	Enable LPC to execute a DFI control update on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.237 EMIF_CTLCFG_DENALI_CTL_176 Register

1 EMIF_CTLCFG_DENALI_CTL_176 Register (Offset = 2C0h) [reset = 0h]

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Table 14-20655. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82C0h**

Figure 14-6850. EMIF_CTLCFG_DENALI_CTL_176 Name Register

31	30	29	28	27	26	25	24
RESERVED							DFS_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PWRDN_SHIFT_DELAY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PWRDN_SHIFT_DELAY							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							LPC_SR_ZQ_EN
NONE							R/W
0h							0h

Table 14-20657. EMIF_CTLCFG_DENALI_CTL_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DFS_ENABLE	R/W	0h	Enable hardware dynamic frequency scaling. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PWRDN_SHIFT_DELAY	R/W	0h	This parameter should be programmed to zero. Manual adjustment of inhibit_pwrdn_shift in memcd_strategy_data_delay. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	LPC_SR_ZQ_EN	R/W	0h	Enable LPC to execute a ZQ calibration on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.238 EMIF_CTLCFG_DENALI_CTL_177 Register

1 EMIF_CTLCFG_DENALI_CTL_177 Register (Offset = 2C4h) [reset = 0h]

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Table 14-20658. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82C4h**

Figure 14-6851. EMIF_CTLCFG_DENALI_CTL_177 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							DFS_PHY_REG_WRITE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					DFS_DLL_OFF		
NONE					R/W		
0h					0h		

Table 14-20660. EMIF_CTLCFG_DENALI_CTL_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	DFS_PHY_REG_WRITE_EN	R/W	0h	Enable a register write to the PHY during a frequency change. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	DFS_DLL_OFF	R/W	0h	Defines if the memory DLL must be off for the associated frequency set. Bit [0] corresponds to frequency set 0, bit [1] corresponds to frequency set 1, etc. Set each bit to 1 to require DLL off. Reset Source: ctl_amod_g_rst_n

14.6.6.2.239 EMIF_CTLCFG_DENALI_CTL_178 Register

1 EMIF_CTLCFG_DENALI_CTL_178 Register (Offset = 2C8h) [reset = 0h]

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Table 14-20661. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82C8h**

Figure 14-6852. EMIF_CTLCFG_DENALI_CTL_178 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							

Table 14-20663. EMIF_CTLCFG_DENALI_CTL_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_ADDR	R/W	0h	Register address which will be written during a frequency change. Must be a PHY register address. Reset Source: ctl_amod_g_rst_n

14.6.6.2.240 EMIF_CTLCFG_DENALI_CTL_179 Register

1 EMIF_CTLCFG_DENALI_CTL_179 Register (Offset = 2CCh) [reset = 0h]

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Table 14-20664. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82CCh**

Figure 14-6853. EMIF_CTLCFG_DENALI_CTL_179 Name Register

31	30	29	28	27	26	25	24
RESERVED						CURRENT_REG_COPY	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DFS_PHY_REG_WRITE_WAIT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DFS_PHY_REG_WRITE_WAIT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DFS_PHY_REG_WRITE_MASK			
NONE				R/W			
0h				0h			

Table 14-20666. EMIF_CTLCFG_DENALI_CTL_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CURRENT_REG_COPY	R	0h	Indicates the current copy of timing parameters that is in use by the controller. Reset Source: ctl_amod_g_rst_n
23:8	DFS_PHY_REG_WRITE_WAIT	R/W	0h	Defines the number of DFI PHY clocks that the controller will wait after issuing the register write to the PHY during a frequency change. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	DFS_PHY_REG_WRITE_MASK	R/W	0h	Register mask which will be written during a frequency change. Reset Source: ctl_amod_g_rst_n

14.6.6.2.241 EMIF_CTLCFG_DENALI_CTL_180 Register

1 EMIF_CTLCFG_DENALI_CTL_180 Register (Offset = 2D0h) [reset = 0h]

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Table 14-20667. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82D0h**

Figure 14-6854. EMIF_CTLCFG_DENALI_CTL_180 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						DFIBUS_BOOT_FREQ	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						INIT_FREQ	
NONE						R/W	
0h						0h	

Table 14-20669. EMIF_CTLCFG_DENALI_CTL_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	DFIBUS_BOOT_FREQ	R/W	0h	Defines the DFI bus boot frequency register copy Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	INIT_FREQ	R/W	0h	Specifies what frequency register copy will be in use by the memory after initialization completes. Reset Source: ctl_amod_g_rst_n

14.6.6.2.242 EMIF_CTLCFG_DENALI_CTL_181 Register

1 EMIF_CTLCFG_DENALI_CTL_181 Register (Offset = 2D4h) [reset = 0h]

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Table 14-20670. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82D4h**

Figure 14-6855. EMIF_CTLCFG_DENALI_CTL_181 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							

Table 14-20672. EMIF_CTLCFG_DENALI_CTL_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F0	R/W	0h	Register data which will be written during a frequency change. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.243 EMIF_CTLCFG_DENALI_CTL_182 Register

1 EMIF_CTLCFG_DENALI_CTL_182 Register (Offset = 2D8h) [reset = 0h]

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Table 14-20673. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 82D8h

Figure 14-6856. EMIF_CTLCFG_DENALI_CTL_182 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							

Table 14-20675. EMIF_CTLCFG_DENALI_CTL_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F1	R/W	0h	Register data which will be written during a frequency change. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.244 EMIF_CTLCFG_DENALI_CTL_183 Register

1 EMIF_CTLCFG_DENALI_CTL_183 Register (Offset = 2DCh) [reset = 0h]

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Table 14-20676. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 82DCh

Figure 14-6857. EMIF_CTLCFG_DENALI_CTL_183 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							

Table 14-20678. EMIF_CTLCFG_DENALI_CTL_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F2	R/W	0h	Register data which will be written during a frequency change. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.245 EMIF_CTLCFG_DENALI_CTL_184 Register

1 EMIF_CTLCFG_DENALI_CTL_184 Register (Offset = 2E0h) [reset = 0h]

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Table 14-20679. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82E0h**

Figure 14-6858. EMIF_CTLCFG_DENALI_CTL_184 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_INIT_START_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_INIT_START_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_INIT_START_F0							
R/W							
0h							

Table 14-20681. EMIF_CTLCFG_DENALI_CTL_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.246 EMIF_CTLCFG_DENALI_CTL_185 Register

1 EMIF_CTLCFG_DENALI_CTL_185 Register (Offset = 2E4h) [reset = 0h]

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Table 14-20682. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 82E4h

Figure 14-6859. EMIF_CTLCFG_DENALI_CTL_185 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_INIT_COMPLETE_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_INIT_COMPLETE_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_INIT_COMPLETE_F0							
R/W							
0h							

Table 14-20684. EMIF_CTLCFG_DENALI_CTL_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.247 EMIF_CTLCFG_DENALI_CTL_186 Register

1 EMIF_CTLCFG_DENALI_CTL_186 Register (Offset = 2E8h) [reset = 0h]

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Table 14-20685. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82E8h**

Figure 14-6860. EMIF_CTLCFG_DENALI_CTL_186 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_START_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_START_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_START_F1							
R/W							
0h							

Table 14-20687. EMIF_CTLCFG_DENALI_CTL_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.248 EMIF_CTLCFG_DENALI_CTL_187 Register

1 EMIF_CTLCFG_DENALI_CTL_187 Register (Offset = 2ECh) [reset = 0h]

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Table 14-20688. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 82ECh

Figure 14-6861. EMIF_CTLCFG_DENALI_CTL_187 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_COMPLETE_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_COMPLETE_F1							
R/W							
0h							

Table 14-20690. EMIF_CTLCFG_DENALI_CTL_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.249 EMIF_CTLCFG_DENALI_CTL_188 Register

1 EMIF_CTLCFG_DENALI_CTL_188 Register (Offset = 2F0h) [reset = 0h]

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Table 14-20691. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82F0h**

Figure 14-6862. EMIF_CTLCFG_DENALI_CTL_188 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_START_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_START_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_START_F2							
R/W							
0h							

Table 14-20693. EMIF_CTLCFG_DENALI_CTL_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.250 EMIF_CTLCFG_DENALI_CTL_189 Register

1 EMIF_CTLCFG_DENALI_CTL_189 Register (Offset = 2F4h) [reset = 0h]

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Table 14-20694. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82F4h**

Figure 14-6863. EMIF_CTLCFG_DENALI_CTL_189 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_COMPLETE_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_COMPLETE_F2							
R/W							
0h							

Table 14-20696. EMIF_CTLCFG_DENALI_CTL_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.251 EMIF_CTLCFG_DENALI_CTL_190 Register

1 EMIF_CTLCFG_DENALI_CTL_190 Register (Offset = 2F8h) [reset = 0h]

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Table 14-20697. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82F8h**

Figure 14-6864. EMIF_CTLCFG_DENALI_CTL_190 Name Register

31	30	29	28	27	26	25	24
RESERVED					WRITE_MODEREG		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WRITE_MODEREG							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WRITE_MODEREG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRITE_MODEREG							
R/W							
0h							

Table 14-20699. EMIF_CTLCFG_DENALI_CTL_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits [7:0] define the memory mode register number if bit [23] is set, bits [15:8] define the chip select if bit [24] is clear, bits [23:16] define which memory mode register/s to write, bit [24] defines whether all chip selects will be written, and bit [25] triggers the write. Reset Source: ctl_amod_g_rst_n

14.6.6.2.252 EMIF_CTLCFG_DENALI_CTL_191 Register

1 EMIF_CTLCFG_DENALI_CTL_191 Register (Offset = 2FCh) [reset = 0h]

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Table 14-20700. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 82FCh**

Figure 14-6865. EMIF_CTLCFG_DENALI_CTL_191 Name Register

31	30	29	28	27	26	25	24
RESERVED							READ_MODEREG
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
READ_MODEREG							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
READ_MODEREG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRW_STATUS							
R							
0h							

Table 14-20702. EMIF_CTLCFG_DENALI_CTL_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits [7:0] define the memory mode register and bits [15:8] define the chip select. Set bit [16] to 1 to trigger. Reset Source: ctl_amod_g_rst_n
7:0	MRW_STATUS	R	0h	Write memory mode register status. Bit [0] set indicates a WRITE_MODEREG parameter programming error. Bit [1] set indicates a PASR error. Bit [2] is Reserved. Bit [3] set indicates a self-refresh or deep power-down error. Bit [4] set indicates that a write to MR3 or MR11 was attempted [WRITE_MODEREG bit [25] was asserted with bit [17] set, or bit [23] was asserted with bits [7:0] defining MR3 or MR11] during tZQCAL after a ZQ calibration start command. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.253 EMIF_CTLCFG_DENALI_CTL_192 Register

1 EMIF_CTLCFG_DENALI_CTL_192 Register (Offset = 300h) [reset = 0h]

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Table 14-20703. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8300h

Figure 14-6866. EMIF_CTLCFG_DENALI_CTL_192 Name Register

31	30	29	28	27	26	25	24
PERIPHERAL_MRR_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
PERIPHERAL_MRR_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
PERIPHERAL_MRR_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
PERIPHERAL_MRR_DATA_0							
R							
0h							

Table 14-20705. EMIF_CTLCFG_DENALI_CTL_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PERIPHERAL_MRR_DATA_0	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits [7:0] indicate the read data and bits [15:8] indicate the chip. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.254 EMIF_CTLCFG_DENALI_CTL_193 Register

1 EMIF_CTLCFG_DENALI_CTL_193 Register (Offset = 304h) [reset = 0h]

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Table 14-20706. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8304h**

Figure 14-6867. EMIF_CTLCFG_DENALI_CTL_193 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AUTO_TEMPCHK_VAL_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUTO_TEMPCHK_VAL_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPHERAL_MRR_DATA_1							
R							
0h							

Table 14-20708. EMIF_CTLCFG_DENALI_CTL_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	AUTO_TEMPCHK_VAL_0	R	0h	MR4 data for all devices accessed by automatic MRR commands. Bits [3:0] correlate to the device on the lower byte, bits [7:4] correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:0	PERIPHERAL_MRR_DATA_1	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits [7:0] indicate the read data and bits [15:8] indicate the chip. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.255 EMIF_CTLCFG_DENALI_CTL_194 Register

1 EMIF_CTLCFG_DENALI_CTL_194 Register (Offset = 308h) [reset = 0h]

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Table 14-20709. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8308h**

Figure 14-6868. EMIF_CTLCFG_DENALI_CTL_194 Name Register

31	30	29	28	27	26	25	24
RESERVED						MRW_DFS_UPDATE_FRC	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DISABLE_UPDATE_TVRCG
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUTO_TEMPCHK_VAL_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AUTO_TEMPCHK_VAL_1							
R							
0h							

Table 14-20711. EMIF_CTLCFG_DENALI_CTL_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	MRW_DFS_UPDATE_FRC	R/W	0h	Defines the frequency register set to use when doing a software MRW with WRITE_MODEREG bit [26]. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DISABLE_UPDATE_TVRCG	R/W	0h	Bypass changing for TVRCG during a DFS operation. Set to 1 to skip TVRCG. Reset Source: ctl_amod_g_rst_n
15:0	AUTO_TEMPCHK_VAL_1	R	0h	MR4 data for all devices accessed by automatic MRR commands. Bits [3:0] correlate to the device on the lower byte, bits [7:4] correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.256 EMIF_CTLCFG_DENALI_CTL_195 Register

1 EMIF_CTLCFG_DENALI_CTL_195 Register (Offset = 30Ch) [reset = 0h]

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Table 14-20712. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 830Ch**

Figure 14-6869. EMIF_CTLCFG_DENALI_CTL_195 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TVRCG_DISABLE_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TVRCG_ENABLE_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TVRCG_ENABLE_F0							
R/W							
0h							

Table 14-20714. EMIF_CTLCFG_DENALI_CTL_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F0	R/W	0h	JEDEC TVRCG_DISABLE time. FC=0 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F0	R/W	0h	JEDEC TVRCG_ENABLE time. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.257 EMIF_CTLCFG_DENALI_CTL_196 Register

1 EMIF_CTLCFG_DENALI_CTL_196 Register (Offset = 310h) [reset = 0h]

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Table 14-20715. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8310h**

Figure 14-6870. EMIF_CTLCFG_DENALI_CTL_196 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKFSPX_F0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			TCKFSPE_F0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED						TFC_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TFC_F0							
R/W							
0h							

Table 14-20717. EMIF_CTLCFG_DENALI_CTL_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F0	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F0	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F0	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.258 EMIF_CTLCFG_DENALI_CTL_197 Register

1 EMIF_CTLCFG_DENALI_CTL_197 Register (Offset = 314h) [reset = 0h]

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Table 14-20718. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8314h**

Figure 14-6871. EMIF_CTLCFG_DENALI_CTL_197 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TVREF_LONG_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TVREF_LONG_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TVREF_LONG_F0							
R/W							
0h							

Table 14-20720. EMIF_CTLCFG_DENALI_CTL_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F0	R/W	0h	JEDEC TVREF, design will always use the long value. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.259 EMIF_CTLCFG_DENALI_CTL_198 Register

1 EMIF_CTLCFG_DENALI_CTL_198 Register (Offset = 318h) [reset = 0h]

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Table 14-20721. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8318h**

Figure 14-6872. EMIF_CTLCFG_DENALI_CTL_198 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TVRCG_DISABLE_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TVRCG_ENABLE_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVRCG_ENABLE_F1							
R/W							
0h							

Table 14-20723. EMIF_CTLCFG_DENALI_CTL_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F1	R/W	0h	JEDEC TVRCG_DISABLE time. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F1	R/W	0h	JEDEC TVRCG_ENABLE time. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.260 EMIF_CTLCFG_DENALI_CTL_199 Register

1 EMIF_CTLCFG_DENALI_CTL_199 Register (Offset = 31Ch) [reset = 0h]

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Table 14-20724. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 831Ch**

Figure 14-6873. EMIF_CTLCFG_DENALI_CTL_199 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKFSPX_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKFSPE_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TFC_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TFC_F1							
R/W							
0h							

Table 14-20726. EMIF_CTLCFG_DENALI_CTL_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F1	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F1	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F1	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.261 EMIF_CTLCFG_DENALI_CTL_200 Register

1 EMIF_CTLCFG_DENALI_CTL_200 Register (Offset = 320h) [reset = 0h]

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Table 14-20727. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8320h**

Figure 14-6874. EMIF_CTLCFG_DENALI_CTL_200 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TVREF_LONG_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TVREF_LONG_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TVREF_LONG_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20729. EMIF_CTLCFG_DENALI_CTL_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F1	R/W	0h	JEDEC TVREF, design will always use the long value. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.262 EMIF_CTLCFG_DENALI_CTL_201 Register

1 EMIF_CTLCFG_DENALI_CTL_201 Register (Offset = 324h) [reset = 0h]

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Table 14-20730. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8324h**

Figure 14-6875. EMIF_CTLCFG_DENALI_CTL_201 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TVRCG_DISABLE_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TVRCG_ENABLE_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TVRCG_ENABLE_F2							
R/W							
0h							

Table 14-20732. EMIF_CTLCFG_DENALI_CTL_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F2	R/W	0h	JEDEC TVRCG_DISABLE time. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F2	R/W	0h	JEDEC TVRCG_ENABLE time. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.263 EMIF_CTLCFG_DENALI_CTL_202 Register

1 EMIF_CTLCFG_DENALI_CTL_202 Register (Offset = 328h) [reset = 0h]

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Table 14-20733. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8328h**

Figure 14-6876. EMIF_CTLCFG_DENALI_CTL_202 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKFSPX_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKFSPE_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TFC_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TFC_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20735. EMIF_CTLCFG_DENALI_CTL_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F2	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F2	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F2	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.264 EMIF_CTLCFG_DENALI_CTL_203 Register

1 EMIF_CTLCFG_DENALI_CTL_203 Register (Offset = 32Ch) [reset = 0h]

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Table 14-20736. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 832Ch**

Figure 14-6877. EMIF_CTLCFG_DENALI_CTL_203 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TVREF_LONG_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TVREF_LONG_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVREF_LONG_F2							
R/W							
0h							

Table 14-20738. EMIF_CTLCFG_DENALI_CTL_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F2	R/W	0h	JEDEC TVREF, design will always use the long value. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.265 EMIF_CTLCFG_DENALI_CTL_204 Register

1 EMIF_CTLCFG_DENALI_CTL_204 Register (Offset = 330h) [reset = 0h]

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Table 14-20739. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8330h**

Figure 14-6878. EMIF_CTLCFG_DENALI_CTL_204 Name Register

31	30	29	28	27	26	25	24
MRR_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
MRR_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-20741. EMIF_CTLCFG_DENALI_CTL_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRR_PROMOTE_THRESHOLD_F1	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	MRR_PROMOTE_THRESHOLD_F0	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.266 EMIF_CTLCFG_DENALI_CTL_205 Register

1 EMIF_CTLCFG_DENALI_CTL_205 Register (Offset = 334h) [reset = 0h]

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Table 14-20742. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8334h**

Figure 14-6879. EMIF_CTLCFG_DENALI_CTL_205 Name Register

31	30	29	28	27	26	25	24
MRW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MRW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MRR_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRR_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-20744. EMIF_CTLCFG_DENALI_CTL_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRW_PROMOTE_THRESHOLD_F0	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	MRR_PROMOTE_THRESHOLD_F2	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.267 EMIF_CTLCFG_DENALI_CTL_206 Register

1 EMIF_CTLCFG_DENALI_CTL_206 Register (Offset = 338h) [reset = 0h]

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Table 14-20745. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8338h

Figure 14-6880. EMIF_CTLCFG_DENALI_CTL_206 Name Register

31	30	29	28	27	26	25	24
MRW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
MRW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRW_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-20747. EMIF_CTLCFG_DENALI_CTL_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRW_PROMOTE_THRESHOLD_F2	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	MRW_PROMOTE_THRESHOLD_F1	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.268 EMIF_CTLCFG_DENALI_CTL_207 Register

1 EMIF_CTLCFG_DENALI_CTL_207 Register (Offset = 33Ch) [reset = 0h]

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Table 14-20748. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 833Ch**

Figure 14-6881. EMIF_CTLCFG_DENALI_CTL_207 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR0_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MR0_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR0_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR4_DLL_RST</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20750. EMIF_CTLCFG_DENALI_CTL_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR0_DATA_F0_0	R/W	0h	Data to program into memory mode register 0. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	MR4_DLL_RST	R/W	0h	Asserted if DRAM DLL Reset bit resides in MR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.269 EMIF_CTLCFG_DENALI_CTL_208 Register

1 EMIF_CTLCFG_DENALI_CTL_208 Register (Offset = 340h) [reset = 0h]

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Table 14-20751. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8340h**

Figure 14-6882. EMIF_CTLCFG_DENALI_CTL_208 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F0_0							
R/W							
0h							

Table 14-20753. EMIF_CTLCFG_DENALI_CTL_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.270 EMIF_CTLCFG_DENALI_CTL_209 Register

1 EMIF_CTLCFG_DENALI_CTL_209 Register (Offset = 344h) [reset = 0h]

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Table 14-20754. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8344h

Figure 14-6883. EMIF_CTLCFG_DENALI_CTL_209 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR2_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR2_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR2_DATA_F0_0							
R/W							
0h							

Table 14-20756. EMIF_CTLCFG_DENALI_CTL_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.271 EMIF_CTLCFG_DENALI_CTL_210 Register

1 EMIF_CTLCFG_DENALI_CTL_210 Register (Offset = 348h) [reset = 0h]

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Table 14-20757. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8348h**

Figure 14-6884. EMIF_CTLCFG_DENALI_CTL_210 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR0_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR0_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR0_DATA_F1_0							
R/W							
0h							

Table 14-20759. EMIF_CTLCFG_DENALI_CTL_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F1_0	R/W	0h	Data to program into memory mode register 0. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.272 EMIF_CTLCFG_DENALI_CTL_211 Register

1 EMIF_CTLCFG_DENALI_CTL_211 Register (Offset = 34Ch) [reset = 0h]

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Table 14-20760. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 834Ch

Figure 14-6885. EMIF_CTLCFG_DENALI_CTL_211 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR1_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR1_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR1_DATA_F1_0							
R/W							
0h							

Table 14-20762. EMIF_CTLCFG_DENALI_CTL_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.273 EMIF_CTLCFG_DENALI_CTL_212 Register

1 EMIF_CTLCFG_DENALI_CTL_212 Register (Offset = 350h) [reset = 0h]

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Table 14-20763. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8350h**

Figure 14-6886. EMIF_CTLCFG_DENALI_CTL_212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F1_0							
R/W							
0h							

Table 14-20765. EMIF_CTLCFG_DENALI_CTL_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.274 EMIF_CTLCFG_DENALI_CTL_213 Register

1 EMIF_CTLCFG_DENALI_CTL_213 Register (Offset = 354h) [reset = 0h]

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Table 14-20766. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8354h**

Figure 14-6887. EMIF_CTLCFG_DENALI_CTL_213 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR0_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR0_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR0_DATA_F2_0							
R/W							
0h							

Table 14-20768. EMIF_CTLCFG_DENALI_CTL_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F2_0	R/W	0h	Data to program into memory mode register 0. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.275 EMIF_CTLCFG_DENALI_CTL_214 Register

1 EMIF_CTLCFG_DENALI_CTL_214 Register (Offset = 358h) [reset = 0h]

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Table 14-20769. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8358h**

Figure 14-6888. EMIF_CTLCFG_DENALI_CTL_214 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F2_0
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
MR1_DATA_F2_0							
R/W							
0h							

7	6	5	4	3	2	1	0
MR1_DATA_F2_0							
R/W							
0h							

Table 14-20771. EMIF_CTLCFG_DENALI_CTL_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.276 EMIF_CTLCFG_DENALI_CTL_215 Register

1 EMIF_CTLCFG_DENALI_CTL_215 Register (Offset = 35Ch) [reset = 0h]

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Table 14-20772. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 835Ch**

Figure 14-6889. EMIF_CTLCFG_DENALI_CTL_215 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR2_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR2_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR2_DATA_F2_0							
R/W							
0h							

Table 14-20774. EMIF_CTLCFG_DENALI_CTL_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.277 EMIF_CTLCFG_DENALI_CTL_216 Register

1 EMIF_CTLCFG_DENALI_CTL_216 Register (Offset = 360h) [reset = 0h]

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Table 14-20775. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8360h**

Figure 14-6890. EMIF_CTLCFG_DENALI_CTL_216 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR0_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR0_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR0_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20777. EMIF_CTLCFG_DENALI_CTL_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F0_1	R/W	0h	Data to program into memory mode register 0. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.278 EMIF_CTLCFG_DENALI_CTL_217 Register

1 EMIF_CTLCFG_DENALI_CTL_217 Register (Offset = 364h) [reset = 0h]

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Table 14-20778. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8364h

Figure 14-6891. EMIF_CTLCFG_DENALI_CTL_217 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F0_1							
R/W							
0h							

Table 14-20780. EMIF_CTLCFG_DENALI_CTL_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.279 EMIF_CTLCFG_DENALI_CTL_218 Register

1 EMIF_CTLCFG_DENALI_CTL_218 Register (Offset = 368h) [reset = 0h]

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Table 14-20781. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8368h**

Figure 14-6892. EMIF_CTLCFG_DENALI_CTL_218 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR2_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR2_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR2_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20783. EMIF_CTLCFG_DENALI_CTL_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.280 EMIF_CTLCFG_DENALI_CTL_219 Register

1 EMIF_CTLCFG_DENALI_CTL_219 Register (Offset = 36Ch) [reset = 0h]

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Table 14-20784. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 836Ch**

Figure 14-6893. EMIF_CTLCFG_DENALI_CTL_219 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR0_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR0_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR0_DATA_F1_1							
R/W							
0h							

Table 14-20786. EMIF_CTLCFG_DENALI_CTL_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F1_1	R/W	0h	Data to program into memory mode register 0. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.281 EMIF_CTLCFG_DENALI_CTL_220 Register

1 EMIF_CTLCFG_DENALI_CTL_220 Register (Offset = 370h) [reset = 0h]

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Table 14-20787. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8370h**

Figure 14-6894. EMIF_CTLCFG_DENALI_CTL_220 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F1_1							
R/W							
0h							

Table 14-20789. EMIF_CTLCFG_DENALI_CTL_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.282 EMIF_CTLCFG_DENALI_CTL_221 Register

1 EMIF_CTLCFG_DENALI_CTL_221 Register (Offset = 374h) [reset = 0h]

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Table 14-20790. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8374h

Figure 14-6895. EMIF_CTLCFG_DENALI_CTL_221 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F1_1							
R/W							
0h							

Table 14-20792. EMIF_CTLCFG_DENALI_CTL_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.283 EMIF_CTLCFG_DENALI_CTL_222 Register

1 EMIF_CTLCFG_DENALI_CTL_222 Register (Offset = 378h) [reset = 0h]

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Table 14-20793. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8378h**

Figure 14-6896. EMIF_CTLCFG_DENALI_CTL_222 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR0_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR0_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR0_DATA_F2_1							
R/W							
0h							

Table 14-20795. EMIF_CTLCFG_DENALI_CTL_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F2_1	R/W	0h	Data to program into memory mode register 0. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.284 EMIF_CTLCFG_DENALI_CTL_223 Register

1 EMIF_CTLCFG_DENALI_CTL_223 Register (Offset = 37Ch) [reset = 0h]

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Table 14-20796. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 837Ch**

Figure 14-6897. EMIF_CTLCFG_DENALI_CTL_223 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F2_1							
R/W							
0h							

Table 14-20798. EMIF_CTLCFG_DENALI_CTL_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.285 EMIF_CTLCFG_DENALI_CTL_224 Register

1 EMIF_CTLCFG_DENALI_CTL_224 Register (Offset = 380h) [reset = 0h]

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Table 14-20799. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8380h**

Figure 14-6898. EMIF_CTLCFG_DENALI_CTL_224 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F2_1							
R/W							
0h							

Table 14-20801. EMIF_CTLCFG_DENALI_CTL_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.286 EMIF_CTLCFG_DENALI_CTL_225 Register

1 EMIF_CTLCFG_DENALI_CTL_225 Register (Offset = 384h) [reset = 0h]

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Table 14-20802. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8384h**

Figure 14-6899. EMIF_CTLCFG_DENALI_CTL_225 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MRSINGLE_DATA_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20804. EMIF_CTLCFG_DENALI_CTL_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write. Reset Source: ctl_amod_g_rst_n

14.6.6.2.287 EMIF_CTLCFG_DENALI_CTL_226 Register

1 EMIF_CTLCFG_DENALI_CTL_226 Register (Offset = 388h) [reset = 0h]

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Table 14-20805. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8388h**

Figure 14-6900. EMIF_CTLCFG_DENALI_CTL_226 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MRSINGLE_DATA_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20807. EMIF_CTLCFG_DENALI_CTL_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write. Reset Source: ctl_amod_g_rst_n

14.6.6.2.288 EMIF_CTLCFG_DENALI_CTL_227 Register

1 EMIF_CTLCFG_DENALI_CTL_227 Register (Offset = 38Ch) [reset = 0h]

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Table 14-20808. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 838Ch

Figure 14-6901. EMIF_CTLCFG_DENALI_CTL_227 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR3_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20810. EMIF_CTLCFG_DENALI_CTL_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.289 EMIF_CTLCFG_DENALI_CTL_228 Register

1 EMIF_CTLCFG_DENALI_CTL_228 Register (Offset = 390h) [reset = 0h]

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Table 14-20811. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8390h**

Figure 14-6902. EMIF_CTLCFG_DENALI_CTL_228 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR3_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR3_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR3_DATA_F1_0							
R/W							
0h							

Table 14-20813. EMIF_CTLCFG_DENALI_CTL_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.290 EMIF_CTLCFG_DENALI_CTL_229 Register

1 EMIF_CTLCFG_DENALI_CTL_229 Register (Offset = 394h) [reset = 0h]

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Table 14-20814. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8394h**

Figure 14-6903. EMIF_CTLCFG_DENALI_CTL_229 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR3_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR3_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR3_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20816. EMIF_CTLCFG_DENALI_CTL_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.291 EMIF_CTLCFG_DENALI_CTL_230 Register

1 EMIF_CTLCFG_DENALI_CTL_230 Register (Offset = 398h) [reset = 0h]

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Table 14-20817. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8398h**

Figure 14-6904. EMIF_CTLCFG_DENALI_CTL_230 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR3_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR3_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR3_DATA_F0_1							
R/W							
0h							

Table 14-20819. EMIF_CTLCFG_DENALI_CTL_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.292 EMIF_CTLCFG_DENALI_CTL_231 Register

1 EMIF_CTLCFG_DENALI_CTL_231 Register (Offset = 39Ch) [reset = 0h]

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Table 14-20820. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 839Ch**

Figure 14-6905. EMIF_CTLCFG_DENALI_CTL_231 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR3_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR3_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR3_DATA_F1_1							
R/W							
0h							

Table 14-20822. EMIF_CTLCFG_DENALI_CTL_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.293 EMIF_CTLCFG_DENALI_CTL_232 Register

1 EMIF_CTLCFG_DENALI_CTL_232 Register (Offset = 3A0h) [reset = 0h]

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Table 14-20823. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83A0h

Figure 14-6906. EMIF_CTLCFG_DENALI_CTL_232 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR3_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR3_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR3_DATA_F2_1							
R/W							
0h							

Table 14-20825. EMIF_CTLCFG_DENALI_CTL_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.294 EMIF_CTLCFG_DENALI_CTL_233 Register

1 EMIF_CTLCFG_DENALI_CTL_233 Register (Offset = 3A4h) [reset = 0h]

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Table 14-20826. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83A4h

Figure 14-6907. EMIF_CTLCFG_DENALI_CTL_233 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR4_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR4_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR4_DATA_F0_0							
R/W							
0h							

Table 14-20828. EMIF_CTLCFG_DENALI_CTL_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F0_0	R/W	0h	Data to program into memory mode register 4. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.295 EMIF_CTLCFG_DENALI_CTL_234 Register

1 EMIF_CTLCFG_DENALI_CTL_234 Register (Offset = 3A8h) [reset = 0h]

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Table 14-20829. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83A8h**

Figure 14-6908. EMIF_CTLCFG_DENALI_CTL_234 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR4_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR4_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR4_DATA_F1_0							
R/W							
0h							

Table 14-20831. EMIF_CTLCFG_DENALI_CTL_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F1_0	R/W	0h	Data to program into memory mode register 4. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.296 EMIF_CTLCFG_DENALI_CTL_235 Register

1 EMIF_CTLCFG_DENALI_CTL_235 Register (Offset = 3ACh) [reset = 0h]

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Table 14-20832. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83ACh

Figure 14-6909. EMIF_CTLCFG_DENALI_CTL_235 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR4_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR4_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR4_DATA_F2_0							
R/W							
0h							

Table 14-20834. EMIF_CTLCFG_DENALI_CTL_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F2_0	R/W	0h	Data to program into memory mode register 4. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.297 EMIF_CTLCFG_DENALI_CTL_236 Register

1 EMIF_CTLCFG_DENALI_CTL_236 Register (Offset = 3B0h) [reset = 0h]

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Table 14-20835. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83B0h**

Figure 14-6910. EMIF_CTLCFG_DENALI_CTL_236 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F0_1							
R/W							
0h							

Table 14-20837. EMIF_CTLCFG_DENALI_CTL_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F0_1	R/W	0h	Data to program into memory mode register 4. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.298 EMIF_CTLCFG_DENALI_CTL_237 Register

1 EMIF_CTLCFG_DENALI_CTL_237 Register (Offset = 3B4h) [reset = 0h]

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Table 14-20838. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83B4h

Figure 14-6911. EMIF_CTLCFG_DENALI_CTL_237 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR4_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR4_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR4_DATA_F1_1							
R/W							
0h							

Table 14-20840. EMIF_CTLCFG_DENALI_CTL_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F1_1	R/W	0h	Data to program into memory mode register 4. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.299 EMIF_CTLCFG_DENALI_CTL_238 Register

1 EMIF_CTLCFG_DENALI_CTL_238 Register (Offset = 3B8h) [reset = 0h]

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Table 14-20841. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83B8h

Figure 14-6912. EMIF_CTLCFG_DENALI_CTL_238 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F2_1							
R/W							
0h							

Table 14-20843. EMIF_CTLCFG_DENALI_CTL_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F2_1	R/W	0h	Data to program into memory mode register 4. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.300 EMIF_CTLCFG_DENALI_CTL_239 Register

1 EMIF_CTLCFG_DENALI_CTL_239 Register (Offset = 3BCh) [reset = 0h]

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Table 14-20844. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83BCh**

Figure 14-6913. EMIF_CTLCFG_DENALI_CTL_239 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F0_0
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
MR5_DATA_F0_0							
R/W							
0h							

7	6	5	4	3	2	1	0
MR5_DATA_F0_0							
R/W							
0h							

Table 14-20846. EMIF_CTLCFG_DENALI_CTL_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F0_0	R/W	0h	Data to program into memory mode register 5. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.301 EMIF_CTLCFG_DENALI_CTL_240 Register

1 EMIF_CTLCFG_DENALI_CTL_240 Register (Offset = 3C0h) [reset = 0h]

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Table 14-20847. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83C0h**

Figure 14-6914. EMIF_CTLCFG_DENALI_CTL_240 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR5_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR5_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR5_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20849. EMIF_CTLCFG_DENALI_CTL_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F1_0	R/W	0h	Data to program into memory mode register 5. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.302 EMIF_CTLCFG_DENALI_CTL_241 Register

1 EMIF_CTLCFG_DENALI_CTL_241 Register (Offset = 3C4h) [reset = 0h]

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Table 14-20850. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83C4h

Figure 14-6915. EMIF_CTLCFG_DENALI_CTL_241 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F2_0							
R/W							
0h							

Table 14-20852. EMIF_CTLCFG_DENALI_CTL_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F2_0	R/W	0h	Data to program into memory mode register 5. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.303 EMIF_CTLCFG_DENALI_CTL_242 Register

1 EMIF_CTLCFG_DENALI_CTL_242 Register (Offset = 3C8h) [reset = 0h]

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Table 14-20853. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83C8h**

Figure 14-6916. EMIF_CTLCFG_DENALI_CTL_242 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR5_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR5_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR5_DATA_F0_1							
R/W							
0h							

Table 14-20855. EMIF_CTLCFG_DENALI_CTL_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F0_1	R/W	0h	Data to program into memory mode register 5. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.304 EMIF_CTLCFG_DENALI_CTL_243 Register

1 EMIF_CTLCFG_DENALI_CTL_243 Register (Offset = 3CCh) [reset = 0h]

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Table 14-20856. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83CCh

Figure 14-6917. EMIF_CTLCFG_DENALI_CTL_243 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F1_1							
R/W							
0h							

Table 14-20858. EMIF_CTLCFG_DENALI_CTL_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F1_1	R/W	0h	Data to program into memory mode register 5. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.305 EMIF_CTLCFG_DENALI_CTL_244 Register

1 EMIF_CTLCFG_DENALI_CTL_244 Register (Offset = 3D0h) [reset = 0h]

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Table 14-20859. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83D0h

Figure 14-6918. EMIF_CTLCFG_DENALI_CTL_244 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR5_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR5_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR5_DATA_F2_1							
R/W							
0h							

Table 14-20861. EMIF_CTLCFG_DENALI_CTL_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F2_1	R/W	0h	Data to program into memory mode register 5. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.306 EMIF_CTLCFG_DENALI_CTL_245 Register

1 EMIF_CTLCFG_DENALI_CTL_245 Register (Offset = 3D4h) [reset = 0h]

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Table 14-20862. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83D4h

Figure 14-6919. EMIF_CTLCFG_DENALI_CTL_245 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR6_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR6_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR6_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20864. EMIF_CTLCFG_DENALI_CTL_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F0_0	R/W	0h	Data to program into memory mode register 6. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.307 EMIF_CTLCFG_DENALI_CTL_246 Register

1 EMIF_CTLCFG_DENALI_CTL_246 Register (Offset = 3D8h) [reset = 0h]

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Table 14-20865. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 83D8h

Figure 14-6920. EMIF_CTLCFG_DENALI_CTL_246 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR6_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR6_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR6_DATA_F1_0							
R/W							
0h							

Table 14-20867. EMIF_CTLCFG_DENALI_CTL_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F1_0	R/W	0h	Data to program into memory mode register 6. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.308 EMIF_CTLCFG_DENALI_CTL_247 Register

1 EMIF_CTLCFG_DENALI_CTL_247 Register (Offset = 3DCh) [reset = 0h]

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Table 14-20868. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83DCh**

Figure 14-6921. EMIF_CTLCFG_DENALI_CTL_247 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR6_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR6_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR6_DATA_F2_0							
R/W							
0h							

Table 14-20870. EMIF_CTLCFG_DENALI_CTL_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F2_0	R/W	0h	Data to program into memory mode register 6. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.309 EMIF_CTLCFG_DENALI_CTL_248 Register

1 EMIF_CTLCFG_DENALI_CTL_248 Register (Offset = 3E0h) [reset = 0h]

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Table 14-20871. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83E0h**

Figure 14-6922. EMIF_CTLCFG_DENALI_CTL_248 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR6_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR6_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR6_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20873. EMIF_CTLCFG_DENALI_CTL_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F0_1	R/W	0h	Data to program into memory mode register 6. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.310 EMIF_CTLCFG_DENALI_CTL_249 Register

1 EMIF_CTLCFG_DENALI_CTL_249 Register (Offset = 3E4h) [reset = 0h]

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Table 14-20874. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83E4h**

Figure 14-6923. EMIF_CTLCFG_DENALI_CTL_249 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR6_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR6_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR6_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20876. EMIF_CTLCFG_DENALI_CTL_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F1_1	R/W	0h	Data to program into memory mode register 6. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.311 EMIF_CTLCFG_DENALI_CTL_250 Register

1 EMIF_CTLCFG_DENALI_CTL_250 Register (Offset = 3E8h) [reset = 0h]

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Table 14-20877. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83E8h**

Figure 14-6924. EMIF_CTLCFG_DENALI_CTL_250 Name Register

31	30	29	28	27	26	25	24
MR8_DATA_0							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							MR6_DATA_F2_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
MR6_DATA_F2_1							
R/W							
0h							

7	6	5	4	3	2	1	0
MR6_DATA_F2_1							
R/W							
0h							

Table 14-20879. EMIF_CTLCFG_DENALI_CTL_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR8_DATA_0	R	0h	Data to program into memory mode register 8 for each chip select. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F2_1	R/W	0h	Data to program into memory mode register 6. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.312 EMIF_CTLCFG_DENALI_CTL_251 Register

1 EMIF_CTLCFG_DENALI_CTL_251 Register (Offset = 3ECh) [reset = 0h]

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Table 14-20880. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83ECh**

Figure 14-6925. EMIF_CTLCFG_DENALI_CTL_251 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR10_DATA_F0_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MR10_DATA_F0_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR10_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR8_DATA_1							
R							
0h							

Table 14-20882. EMIF_CTLCFG_DENALI_CTL_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR10_DATA_F0_0	R/W	0h	Data to program into memory mode register 10. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR8_DATA_1	R	0h	Data to program into memory mode register 8 for each chip select. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.313 EMIF_CTLCFG_DENALI_CTL_252 Register

1 EMIF_CTLCFG_DENALI_CTL_252 Register (Offset = 3F0h) [reset = 0h]

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Table 14-20883. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83F0h**

Figure 14-6926. EMIF_CTLCFG_DENALI_CTL_252 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR10_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR10_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR10_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20885. EMIF_CTLCFG_DENALI_CTL_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F1_0	R/W	0h	Data to program into memory mode register 10. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.314 EMIF_CTLCFG_DENALI_CTL_253 Register

1 EMIF_CTLCFG_DENALI_CTL_253 Register (Offset = 3F4h) [reset = 0h]

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Table 14-20886. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 83F4h**

Figure 14-6927. EMIF_CTLCFG_DENALI_CTL_253 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F2_0							
R/W							
0h							

Table 14-20888. EMIF_CTLCFG_DENALI_CTL_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F2_0	R/W	0h	Data to program into memory mode register 10. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.315 EMIF_CTLCFG_DENALI_CTL_254 Register

1 EMIF_CTLCFG_DENALI_CTL_254 Register (Offset = 3F8h) [reset = 0h]

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Table 14-20889. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83F8h**

Figure 14-6928. EMIF_CTLCFG_DENALI_CTL_254 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F0_1							
R/W							
0h							

Table 14-20891. EMIF_CTLCFG_DENALI_CTL_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F0_1	R/W	0h	Data to program into memory mode register 10. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.316 EMIF_CTLCFG_DENALI_CTL_255 Register

1 EMIF_CTLCFG_DENALI_CTL_255 Register (Offset = 3FCh) [reset = 0h]

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Table 14-20892. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 83FCh**

Figure 14-6929. EMIF_CTLCFG_DENALI_CTL_255 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F1_1							
R/W							
0h							

Table 14-20894. EMIF_CTLCFG_DENALI_CTL_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F1_1	R/W	0h	Data to program into memory mode register 10. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.317 EMIF_CTLCFG_DENALI_CTL_256 Register

1 EMIF_CTLCFG_DENALI_CTL_256 Register (Offset = 400h) [reset = 0h]

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Table 14-20895. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8400h**

Figure 14-6930. EMIF_CTLCFG_DENALI_CTL_256 Name Register

31	30	29	28	27	26	25	24
MR11_DATA_F0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F2_1							
R/W							
0h							

Table 14-20897. EMIF_CTLCFG_DENALI_CTL_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F2_1	R/W	0h	Data to program into memory mode register 10. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.318 EMIF_CTLCFG_DENALI_CTL_257 Register

1 EMIF_CTLCFG_DENALI_CTL_257 Register (Offset = 404h) [reset = 0h]

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Table 14-20898. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8404h**

Figure 14-6931. EMIF_CTLCFG_DENALI_CTL_257 Name Register

31	30	29	28	27	26	25	24
MR11_DATA_F1_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MR11_DATA_F0_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR11_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR11_DATA_F1_0							
R/W							
0h							

Table 14-20900. EMIF_CTLCFG_DENALI_CTL_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.319 EMIF_CTLCFG_DENALI_CTL_258 Register

1 EMIF_CTLCFG_DENALI_CTL_258 Register (Offset = 408h) [reset = 0h]

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Table 14-20901. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8408h**

Figure 14-6932. EMIF_CTLCFG_DENALI_CTL_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR12_DATA_F0_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
MR12_DATA_F0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
MR12_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR11_DATA_F2_1							
R/W							
0h							

Table 14-20903. EMIF_CTLCFG_DENALI_CTL_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.320 EMIF_CTLCFG_DENALI_CTL_259 Register

1 EMIF_CTLCFG_DENALI_CTL_259 Register (Offset = 40Ch) [reset = 0h]

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Table 14-20904. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 840Ch

Figure 14-6933. EMIF_CTLCFG_DENALI_CTL_259 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR12_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR12_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR12_DATA_F1_0							
R/W							
0h							

Table 14-20906. EMIF_CTLCFG_DENALI_CTL_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.321 EMIF_CTLCFG_DENALI_CTL_260 Register

1 EMIF_CTLCFG_DENALI_CTL_260 Register (Offset = 410h) [reset = 0h]

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Table 14-20907. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8410h**

Figure 14-6934. EMIF_CTLCFG_DENALI_CTL_260 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F2_0							
R/W							
0h							

Table 14-20909. EMIF_CTLCFG_DENALI_CTL_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.322 EMIF_CTLCFG_DENALI_CTL_261 Register

1 EMIF_CTLCFG_DENALI_CTL_261 Register (Offset = 414h) [reset = 0h]

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Table 14-20910. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8414h**

Figure 14-6935. EMIF_CTLCFG_DENALI_CTL_261 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR12_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR12_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR12_DATA_F0_1							
R/W							
0h							

Table 14-20912. EMIF_CTLCFG_DENALI_CTL_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.323 EMIF_CTLCFG_DENALI_CTL_262 Register

1 EMIF_CTLCFG_DENALI_CTL_262 Register (Offset = 418h) [reset = 0h]

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Table 14-20913. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8418h**

Figure 14-6936. EMIF_CTLCFG_DENALI_CTL_262 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F1_1							
R/W							
0h							

Table 14-20915. EMIF_CTLCFG_DENALI_CTL_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.324 EMIF_CTLCFG_DENALI_CTL_263 Register

1 EMIF_CTLCFG_DENALI_CTL_263 Register (Offset = 41Ch) [reset = 0h]

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Table 14-20916. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 841Ch**

Figure 14-6937. EMIF_CTLCFG_DENALI_CTL_263 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F2_1							
R/W							
0h							

Table 14-20918. EMIF_CTLCFG_DENALI_CTL_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.325 EMIF_CTLCFG_DENALI_CTL_264 Register

1 EMIF_CTLCFG_DENALI_CTL_264 Register (Offset = 420h) [reset = 0h]

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Table 14-20919. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8420h

Figure 14-6938. EMIF_CTLCFG_DENALI_CTL_264 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR13_DATA_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR13_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR13_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20921. EMIF_CTLCFG_DENALI_CTL_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR13_DATA_0	R/W	0h	Data to program into memory mode register 13. Reset Source: ctl_amod_g_rst_n

14.6.6.2.326 EMIF_CTLCFG_DENALI_CTL_265 Register

1 EMIF_CTLCFG_DENALI_CTL_265 Register (Offset = 424h) [reset = 0h]

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Table 14-20922. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8424h

Figure 14-6939. EMIF_CTLCFG_DENALI_CTL_265 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR13_DATA_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR13_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR13_DATA_1							
R/W							
0h							

Table 14-20924. EMIF_CTLCFG_DENALI_CTL_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR13_DATA_1	R/W	0h	Data to program into memory mode register 13. Reset Source: ctl_amod_g_rst_n

14.6.6.2.327 EMIF_CTLCFG_DENALI_CTL_266 Register

1 EMIF_CTLCFG_DENALI_CTL_266 Register (Offset = 428h) [reset = 0h]

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Table 14-20925. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8428h**

Figure 14-6940. EMIF_CTLCFG_DENALI_CTL_266 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR14_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR14_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR14_DATA_F0_0							
R/W							
0h							

Table 14-20927. EMIF_CTLCFG_DENALI_CTL_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.328 EMIF_CTLCFG_DENALI_CTL_267 Register

1 EMIF_CTLCFG_DENALI_CTL_267 Register (Offset = 42Ch) [reset = 0h]

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Table 14-20928. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 842Ch**

Figure 14-6941. EMIF_CTLCFG_DENALI_CTL_267 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR14_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR14_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR14_DATA_F1_0							
R/W							
0h							

Table 14-20930. EMIF_CTLCFG_DENALI_CTL_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.329 EMIF_CTLCFG_DENALI_CTL_268 Register

1 EMIF_CTLCFG_DENALI_CTL_268 Register (Offset = 430h) [reset = 0h]

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Table 14-20931. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8430h**

Figure 14-6942. EMIF_CTLCFG_DENALI_CTL_268 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR14_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR14_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR14_DATA_F2_0							
R/W							
0h							

Table 14-20933. EMIF_CTLCFG_DENALI_CTL_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.330 EMIF_CTLCFG_DENALI_CTL_269 Register

1 EMIF_CTLCFG_DENALI_CTL_269 Register (Offset = 434h) [reset = 0h]

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Table 14-20934. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8434h**

Figure 14-6943. EMIF_CTLCFG_DENALI_CTL_269 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR14_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR14_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR14_DATA_F0_1							
R/W							
0h							

Table 14-20936. EMIF_CTLCFG_DENALI_CTL_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.331 EMIF_CTLCFG_DENALI_CTL_270 Register

1 EMIF_CTLCFG_DENALI_CTL_270 Register (Offset = 438h) [reset = 0h]

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Table 14-20937. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8438h**

Figure 14-6944. EMIF_CTLCFG_DENALI_CTL_270 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR14_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR14_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR14_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20939. EMIF_CTLCFG_DENALI_CTL_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.332 EMIF_CTLCFG_DENALI_CTL_271 Register

1 EMIF_CTLCFG_DENALI_CTL_271 Register (Offset = 43Ch) [reset = 0h]

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Table 14-20940. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 843Ch

Figure 14-6945. EMIF_CTLCFG_DENALI_CTL_271 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MR16_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR14_DATA_F2_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR14_DATA_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR14_DATA_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20942. EMIF_CTLCFG_DENALI_CTL_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR16_DATA_0	R/W	0h	Data to program into memory mode register 16. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.333 EMIF_CTLCFG_DENALI_CTL_272 Register

1 EMIF_CTLCFG_DENALI_CTL_272 Register (Offset = 440h) [reset = 0h]

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Table 14-20943. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8440h**

Figure 14-6946. EMIF_CTLCFG_DENALI_CTL_272 Name Register

31	30	29	28	27	26	25	24
MR20_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
MR17_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
MR17_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR16_DATA_1							
R/W							
0h							

Table 14-20945. EMIF_CTLCFG_DENALI_CTL_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR20_DATA_0	R/W	0h	Data to program into memory mode register 20. Reset Source: ctl_amod_g_rst_n
23:16	MR17_DATA_1	R/W	0h	Data to program into memory mode register 17. Reset Source: ctl_amod_g_rst_n
15:8	MR17_DATA_0	R/W	0h	Data to program into memory mode register 17. Reset Source: ctl_amod_g_rst_n
7:0	MR16_DATA_1	R/W	0h	Data to program into memory mode register 16. Reset Source: ctl_amod_g_rst_n

14.6.6.2.334 EMIF_CTLCFG_DENALI_CTL_273 Register

1 EMIF_CTLCFG_DENALI_CTL_273 Register (Offset = 444h) [reset = 0h]

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Table 14-20946. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8444h**

Figure 14-6947. EMIF_CTLCFG_DENALI_CTL_273 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR22_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MR22_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR22_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR20_DATA_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20948. EMIF_CTLCFG_DENALI_CTL_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR20_DATA_1	R/W	0h	Data to program into memory mode register 20. Reset Source: ctl_amod_g_rst_n

14.6.6.2.335 EMIF_CTLCFG_DENALI_CTL_274 Register

1 EMIF_CTLCFG_DENALI_CTL_274 Register (Offset = 448h) [reset = 0h]

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Table 14-20949. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8448h**

Figure 14-6948. EMIF_CTLCFG_DENALI_CTL_274 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR22_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR22_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR22_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20951. EMIF_CTLCFG_DENALI_CTL_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.336 EMIF_CTLCFG_DENALI_CTL_275 Register

1 EMIF_CTLCFG_DENALI_CTL_275 Register (Offset = 44Ch) [reset = 0h]

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Table 14-20952. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 844Ch

Figure 14-6949. EMIF_CTLCFG_DENALI_CTL_275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR22_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR22_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR22_DATA_F2_0							
R/W							
0h							

Table 14-20954. EMIF_CTLCFG_DENALI_CTL_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.337 EMIF_CTLCFG_DENALI_CTL_276 Register

1 EMIF_CTLCFG_DENALI_CTL_276 Register (Offset = 450h) [reset = 0h]

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Table 14-20955. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8450h**

Figure 14-6950. EMIF_CTLCFG_DENALI_CTL_276 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR22_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR22_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR22_DATA_F0_1							
R/W							
0h							

Table 14-20957. EMIF_CTLCFG_DENALI_CTL_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.338 EMIF_CTLCFG_DENALI_CTL_277 Register

1 EMIF_CTLCFG_DENALI_CTL_277 Register (Offset = 454h) [reset = 0h]

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Table 14-20958. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8454h**

Figure 14-6951. EMIF_CTLCFG_DENALI_CTL_277 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR22_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR22_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR22_DATA_F1_1							
R/W							
0h							

Table 14-20960. EMIF_CTLCFG_DENALI_CTL_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.339 EMIF_CTLCFG_DENALI_CTL_278 Register

1 EMIF_CTLCFG_DENALI_CTL_278 Register (Offset = 458h) [reset = 0h]

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Table 14-20961. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8458h

Figure 14-6952. EMIF_CTLCFG_DENALI_CTL_278 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR22_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR22_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR22_DATA_F2_1							
R/W							
0h							

Table 14-20963. EMIF_CTLCFG_DENALI_CTL_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.340 EMIF_CTLCFG_DENALI_CTL_279 Register

1 EMIF_CTLCFG_DENALI_CTL_279 Register (Offset = 45Ch) [reset = 0h]

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Table 14-20964. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 845Ch**

Figure 14-6953. EMIF_CTLCFG_DENALI_CTL_279 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR_FSP_DATA_VALID_F0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR23_DATA
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR23_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR23_DATA							
R/W							
0h							

Table 14-20966. EMIF_CTLCFG_DENALI_CTL_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MR_FSP_DATA_VALID_F0	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR23_DATA	R/W	0h	Data to program into memory mode register 23. Reset Source: ctl_amod_g_rst_n

14.6.6.2.341 EMIF_CTLCFG_DENALI_CTL_280 Register

1 EMIF_CTLCFG_DENALI_CTL_280 Register (Offset = 460h) [reset = 10000h]

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Table 14-20967. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8460h**

Figure 14-6954. EMIF_CTLCFG_DENALI_CTL_280 Name Register

31	30	29	28	27	26	25	24
RESERVED							DFS_FSP_INSYNC_INACTIVE
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							DFS_FSP_INSYNC_ACTIVE
NONE							R
0h							1h
15	14	13	12	11	10	9	8
RESERVED							MR_FSP_DATA_VALID_F2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							MR_FSP_DATA_VALID_F1
NONE							R/W
0h							0h

Table 14-20969. EMIF_CTLCFG_DENALI_CTL_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DFS_FSP_INSYNC_INACTIVE	R	0h	When cleared, this indicates that the contents in memcd_param is new that the values in memory's MRx FSP reg and if a dfs occurs, they need to be updated. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DFS_FSP_INSYNC_ACTIVE	R	1h	When cleared, this indicates that the contents in memcd_param is new that the values in memory's MRx FSP reg and if a dfs occurs, they need to be updated. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	MR_FSP_DATA_VALID_F2	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=2 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-20969. EMIF_CTLCFG_DENALI_CTL_280 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MR_FSP_DATA_VALID_F1	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.342 EMIF_CTLCFG_DENALI_CTL_281 Register

1 EMIF_CTLCFG_DENALI_CTL_281 Register (Offset = 464h) [reset = 0h]

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Table 14-20970. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8464h

Figure 14-6955. EMIF_CTLCFG_DENALI_CTL_281 Name Register

31	30	29	28	27	26	25	24
RESERVED							FSP_OP_CURRENT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							FSP_STATUS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							DFS_ALWAYS_WRITE_FSP
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							FSP_PHY_UPDATE_MRW
NONE							R/W
0h							0h

Table 14-20972. EMIF_CTLCFG_DENALI_CTL_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	FSP_OP_CURRENT	R/W	0h	Reports which FSP set the memory is currently using. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	FSP_STATUS	R/W	0h	Indicates that a DFS event caused the FSP mode registers to be updated. Value of 1 means that the FSP mode registers were changed. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	DFS_ALWAYS_WRITE_FSP	R/W	0h	Forces all FSP mode registers to be written by the controller during a DFS event. Set to 1 to force the write. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	FSP_PHY_UPDATE_MRW	R/W	0h	Identifies the logic responsible for updating MR12 and MR14 in memory. Clear to 0 for the controller, or set to 1 for the PHY or PI. Reset Source: ctl_amod_g_rst_n

14.6.6.2.343 EMIF_CTLCFG_DENALI_CTL_282 Register

1 EMIF_CTLCFG_DENALI_CTL_282 Register (Offset = 468h) [reset = 0h]

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Table 14-20973. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8468h

Figure 14-6956. EMIF_CTLCFG_DENALI_CTL_282 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">FSP0_FRC</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSP1_FRC_VALID</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSP0_FRC_VALID</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSP_WR_CURRENT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20975. EMIF_CTLCFG_DENALI_CTL_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	FSP0_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	FSP1_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP1_FRC parameter reflects the frequency used to program the FSP1 registers. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	FSP0_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP0_FRC parameter reflects the frequency used to program the FSP0 registers. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	FSP_WR_CURRENT	R/W	0h	Reports which FSP set the memory will target with write commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.344 EMIF_CTLCFG_DENALI_CTL_283 Register

1 EMIF_CTLCFG_DENALI_CTL_283 Register (Offset = 46Ch) [reset = 0h]

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Table 14-20976. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 846Ch**

Figure 14-6957. EMIF_CTLCFG_DENALI_CTL_283 Name Register

31	30	29	28	27	26	25	24
RESERVED		ADDR_SPACE					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						BIST_RESULT	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							BIST_GO
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						FSP1_FRC	
NONE						R/W	
0h						0h	

Table 14-20978. EMIF_CTLCFG_DENALI_CTL_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	BIST_RESULT	R	0h	BIST operation status [pass/fail]. Bit [0] indicates data check status and bit [1] indicates address check status. Value of 1 is a passing result. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	BIST_GO	W	0h	Initiate a BIST operation. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	FSP1_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.345 EMIF_CTLCFG_DENALI_CTL_284 Register

1 EMIF_CTLCFG_DENALI_CTL_284 Register (Offset = 470h) [reset = 0h]

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Table 14-20979. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8470h**

Figure 14-6958. EMIF_CTLCFG_DENALI_CTL_284 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>BIST_ADDR_CHECK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>BIST_DATA_CHECK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20981. EMIF_CTLCFG_DENALI_CTL_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.346 EMIF_CTLCFG_DENALI_CTL_285 Register

1 EMIF_CTLCFG_DENALI_CTL_285 Register (Offset = 474h) [reset = 0h]

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Table 14-20982. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8474h**

Figure 14-6959. EMIF_CTLCFG_DENALI_CTL_285 Name Register

31	30	29	28	27	26	25	24
BIST_START_ADDRESS_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIST_START_ADDRESS_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_START_ADDRESS_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_START_ADDRESS_0							
R/W							
0h							

Table 14-20984. EMIF_CTLCFG_DENALI_CTL_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_START_ADDRESS_0	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.6.6.2.347 EMIF_CTLCFG_DENALI_CTL_286 Register

1 EMIF_CTLCFG_DENALI_CTL_286 Register (Offset = 478h) [reset = 0h]

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Table 14-20985. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8478h**

Figure 14-6960. EMIF_CTLCFG_DENALI_CTL_286 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					BIST_START_ADDRESS_1		
NONE					R/W		
0h					0h		

Table 14-20987. EMIF_CTLCFG_DENALI_CTL_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.6.6.2.348 EMIF_CTLCFG_DENALI_CTL_287 Register

1 EMIF_CTLCFG_DENALI_CTL_287 Register (Offset = 47Ch) [reset = 0h]

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Table 14-20988. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 847Ch**

Figure 14-6961. EMIF_CTLCFG_DENALI_CTL_287 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_MASK_0							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_MASK_0							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_MASK_0							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_MASK_0							
R/W							
0h							

Table 14-20990. EMIF_CTLCFG_DENALI_CTL_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_MASK_0	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.6.6.2.349 EMIF_CTLCFG_DENALI_CTL_288 Register

1 EMIF_CTLCFG_DENALI_CTL_288 Register (Offset = 480h) [reset = 0h]

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Table 14-20991. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8480h**

Figure 14-6962. EMIF_CTLCFG_DENALI_CTL_288 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_MASK_1							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_MASK_1							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_MASK_1							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_MASK_1							
R/W							
0h							

Table 14-20993. EMIF_CTLCFG_DENALI_CTL_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_MASK_1	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.6.6.2.350 EMIF_CTLCFG_DENALI_CTL_289 Register

1 EMIF_CTLCFG_DENALI_CTL_289 Register (Offset = 484h) [reset = 0h]

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Table 14-20994. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8484h**

Figure 14-6963. EMIF_CTLCFG_DENALI_CTL_289 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					BIST_TEST_MODE		
NONE					R/W		
0h					0h		

Table 14-20996. EMIF_CTLCFG_DENALI_CTL_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	BIST_TEST_MODE	R/W	0h	Sets the BIST test mode. Value of 0 specifies standard BIST operation, value of 1 specifies a reduced BIST operation, value of 2 specifies a self-refresh retention test, value of 3 specifies an idle retention test, and value of 4 specifies memory initalization function. All other values are reserved. Reset Source: ctl_amod_g_rst_n

14.6.6.2.351 EMIF_CTLCFG_DENALI_CTL_290 Register

1 EMIF_CTLCFG_DENALI_CTL_290 Register (Offset = 488h) [reset = 0h]

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Table 14-20997. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8488h

Figure 14-6964. EMIF_CTLCFG_DENALI_CTL_290 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_0							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_PATTERN_0							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_PATTERN_0							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_0							
R/W							
0h							

Table 14-20999. EMIF_CTLCFG_DENALI_CTL_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_0	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.6.6.2.352 EMIF_CTLCFG_DENALI_CTL_291 Register

1 EMIF_CTLCFG_DENALI_CTL_291 Register (Offset = 48Ch) [reset = 0h]

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Table 14-21000. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 848Ch**

Figure 14-6965. EMIF_CTLCFG_DENALI_CTL_291 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIST_DATA_PATTERN_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_DATA_PATTERN_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_DATA_PATTERN_1							
R/W							
0h							

Table 14-21002. EMIF_CTLCFG_DENALI_CTL_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_1	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.6.6.2.353 EMIF_CTLCFG_DENALI_CTL_292 Register

1 EMIF_CTLCFG_DENALI_CTL_292 Register (Offset = 490h) [reset = 0h]

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Table 14-21003. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8490h

Figure 14-6966. EMIF_CTLCFG_DENALI_CTL_292 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_2							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_PATTERN_2							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_PATTERN_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_2							
R/W							
0h							

Table 14-21005. EMIF_CTLCFG_DENALI_CTL_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_2	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.6.6.2.354 EMIF_CTLCFG_DENALI_CTL_293 Register

1 EMIF_CTLCFG_DENALI_CTL_293 Register (Offset = 494h) [reset = 0h]

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Table 14-21006. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8494h**

Figure 14-6967. EMIF_CTLCFG_DENALI_CTL_293 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_3							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_PATTERN_3							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_PATTERN_3							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_3							
R/W							
0h							

Table 14-21008. EMIF_CTLCFG_DENALI_CTL_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_3	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.6.6.2.355 EMIF_CTLCFG_DENALI_CTL_294 Register

1 EMIF_CTLCFG_DENALI_CTL_294 Register (Offset = 498h) [reset = 0h]

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Table 14-21009. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8498h**

Figure 14-6968. EMIF_CTLCFG_DENALI_CTL_294 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				BIST_ERR_STOP			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
BIST_ERR_STOP							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							BIST_RET_STATE
NONE							R
0h							0h

Table 14-21011. EMIF_CTLCFG_DENALI_CTL_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. A value of 0 will allow the test to run to completion. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BIST_RET_STATE	R	0h	Indicates if BIST is in a retention wait state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Value of 1 indicates BIST is waiting. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.356 EMIF_CTLCFG_DENALI_CTL_295 Register

1 EMIF_CTLCFG_DENALI_CTL_295 Register (Offset = 49Ch) [reset = 0h]

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Table 14-21012. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 849Ch**

Figure 14-6969. EMIF_CTLCFG_DENALI_CTL_295 Name Register

31	30	29	28	27	26	25	24
RESERVED			LONG_COUNT_MASK				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							BIST_RET_STATE_EXIT
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				BIST_ERR_COUNT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
BIST_ERR_COUNT							
R							
0h							

Table 14-21014. EMIF_CTLCFG_DENALI_CTL_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles. The only supported values are 0x00 [1024 cycles], 0x10 [512 clocks], 0x18 [256 clocks], 0x1C [128 clocks], 0x1E [64 clocks] and 0x1F [32 clocks]. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	BIST_RET_STATE_EXIT	W	0h	Exit self-refresh or idle retention state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.357 EMIF_CTLCFG_DENALI_CTL_296 Register

1 EMIF_CTLCFG_DENALI_CTL_296 Register (Offset = 4A0h) [reset = 0h]

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Table 14-21015. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84A0h

Figure 14-6970. EMIF_CTLCFG_DENALI_CTL_296 Name Register

31	30	29	28	27	26	25	24
RESERVED			AREF_MAX_CREDIT				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			AREF_MAX_DEFICIT				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			AREF_HIGH_THRESHOLD				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			AREF_NORM_THRESHOLD				
NONE			R/W				
0h			0h				

Table 14-21017. EMIF_CTLCFG_DENALI_CTL_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	AREF_MAX_CREDIT	R/W	0h	AREF number of posted refreshes until the maximum number of refresh credits has been reached. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	AREF_MAX_DEFICIT	R/W	0h	AREF number of pending refreshes until the maximum number of refreshes has been exceeded. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	AREF_HIGH_THRESHOLD	R/W	0h	AREF number of pending refreshes until the high priority request is asserted. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	AREF_NORM_THRESHOLD	R/W	0h	AREF number of pending refreshes until the normal priority request is asserted. Reset Source: ctl_amod_g_rst_n

14.6.6.2.358 EMIF_CTLCFG_DENALI_CTL_297 Register

1 EMIF_CTLCFG_DENALI_CTL_297 Register (Offset = 4A4h) [reset = 0h]

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Table 14-21018. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84A4h**

Figure 14-6971. EMIF_CTLCFG_DENALI_CTL_297 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ZQ_CALSTART_NORM_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ZQ_CALSTART_NORM_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ZQCS_OPT_THRESHOLD</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AREF_CMD_MAX_PER_TREFI</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21020. EMIF_CTLCFG_DENALI_CTL_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_NORM_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=0 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	ZQCS_OPT_THRESHOLD	R/W	0h	Number of clocks before ZQCS expires when the ZQ task will deassert its request for optimal command to command turn-around timing. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	AREF_CMD_MAX_PER_TREFI	R/W	0h	Sets the maximum number of auto-refreshes that will be executed in a TREFI period - both normal and high priority. This does not prevent refreshes generated by sub-task requests such as a self-refresh exit and enter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.359 EMIF_CTLCFG_DENALI_CTL_298 Register

1 EMIF_CTLCFG_DENALI_CTL_298 Register (Offset = 4A8h) [reset = 0h]

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Table 14-21021. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84A8h

Figure 14-6972. EMIF_CTLCFG_DENALI_CTL_298 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_HIGH_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_HIGH_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_HIGH_THRESHOLD_F0							
R/W							
0h							

Table 14-21023. EMIF_CTLCFG_DENALI_CTL_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_HIGH_THRESHOLD_F0	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_HIGH_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.360 EMIF_CTLCFG_DENALI_CTL_299 Register

1 EMIF_CTLCFG_DENALI_CTL_299 Register (Offset = 4ACh) [reset = 0h]

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Table 14-21024. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84ACh**

Figure 14-6973. EMIF_CTLCFG_DENALI_CTL_299 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_HIGH_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CS_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_NORM_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_NORM_THRESHOLD_F0							
R/W							
0h							

Table 14-21026. EMIF_CTLCFG_DENALI_CTL_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_HIGH_THRESHOLD_F0	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_NORM_THRESHOLD_F0	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.361 EMIF_CTLCFG_DENALI_CTL_300 Register

1 EMIF_CTLCFG_DENALI_CTL_300 Register (Offset = 4B0h) [reset = 0h]

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Table 14-21027. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84B0h**

Figure 14-6974. EMIF_CTLCFG_DENALI_CTL_300 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_TIMEOUT_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_TIMEOUT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_TIMEOUT_F0							
R/W							
0h							

Table 14-21029. EMIF_CTLCFG_DENALI_CTL_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_TIMEOUT_F0	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_TIMEOUT_F0	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.362 EMIF_CTLCFG_DENALI_CTL_301 Register

1 EMIF_CTLCFG_DENALI_CTL_301 Register (Offset = 4B4h) [reset = 0h]

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Table 14-21030. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84B4h

Figure 14-6975. EMIF_CTLCFG_DENALI_CTL_301 Name Register

31	30	29	28	27	26	25	24
ZQ_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_TIMEOUT_F0							
R/W							
0h							

Table 14-21032. EMIF_CTLCFG_DENALI_CTL_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_PROMOTE_THRESHOLD_F0	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_TIMEOUT_F0	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.363 EMIF_CTLCFG_DENALI_CTL_302 Register

1 EMIF_CTLCFG_DENALI_CTL_302 Register (Offset = 4B8h) [reset = 0h]

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Table 14-21033. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84B8h

Figure 14-6976. EMIF_CTLCFG_DENALI_CTL_302 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_HIGH_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_HIGH_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_NORM_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_NORM_THRESHOLD_F1							
R/W							
0h							

Table 14-21035. EMIF_CTLCFG_DENALI_CTL_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_HIGH_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_NORM_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.364 EMIF_CTLCFG_DENALI_CTL_303 Register

1 EMIF_CTLCFG_DENALI_CTL_303 Register (Offset = 4BCh) [reset = 0h]

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Table 14-21036. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84BCh**

Figure 14-6977. EMIF_CTLCFG_DENALI_CTL_303 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_NORM_THRESHOLD_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQ_CS_NORM_THRESHOLD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ZQ_CALLATCH_HIGH_THRESHOLD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQ_CALLATCH_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-21038. EMIF_CTLCFG_DENALI_CTL_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_NORM_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALLATCH_HIGH_THRESHOLD_F1	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.365 EMIF_CTLCFG_DENALI_CTL_304 Register

1 EMIF_CTLCFG_DENALI_CTL_304 Register (Offset = 4C0h) [reset = 0h]

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Table 14-21039. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84C0h

Figure 14-6978. EMIF_CTLCFG_DENALI_CTL_304 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_TIMEOUT_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_HIGH_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-21041. EMIF_CTLCFG_DENALI_CTL_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_TIMEOUT_F1	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_HIGH_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.366 EMIF_CTLCFG_DENALI_CTL_305 Register

1 EMIF_CTLCFG_DENALI_CTL_305 Register (Offset = 4C4h) [reset = 0h]

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Table 14-21042. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84C4h

Figure 14-6979. EMIF_CTLCFG_DENALI_CTL_305 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_TIMEOUT_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CS_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALLATCH_TIMEOUT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALLATCH_TIMEOUT_F1							
R/W							
0h							

Table 14-21044. EMIF_CTLCFG_DENALI_CTL_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_TIMEOUT_F1	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALLATCH_TIMEOUT_F1	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.367 EMIF_CTLCFG_DENALI_CTL_306 Register

1 EMIF_CTLCFG_DENALI_CTL_306 Register (Offset = 4C8h) [reset = 0h]

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Table 14-21045. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84C8h**

Figure 14-6980. EMIF_CTLCFG_DENALI_CTL_306 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_NORM_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_NORM_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-21047. EMIF_CTLCFG_DENALI_CTL_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_NORM_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_PROMOTE_THRESHOLD_F1	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.368 EMIF_CTLCFG_DENALI_CTL_307 Register

1 EMIF_CTLCFG_DENALI_CTL_307 Register (Offset = 4CCh) [reset = 0h]

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Table 14-21048. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84CCh**

Figure 14-6981. EMIF_CTLCFG_DENALI_CTL_307 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_HIGH_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_HIGH_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_HIGH_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_HIGH_THRESHOLD_F2							
R/W							
0h							

Table 14-21050. EMIF_CTLCFG_DENALI_CTL_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_HIGH_THRESHOLD_F2	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_HIGH_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.369 EMIF_CTLCFG_DENALI_CTL_308 Register

1 EMIF_CTLCFG_DENALI_CTL_308 Register (Offset = 4D0h) [reset = 0h]

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Table 14-21051. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84D0h**

Figure 14-6982. EMIF_CTLCFG_DENALI_CTL_308 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_HIGH_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CS_HIGH_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_NORM_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_NORM_THRESHOLD_F2							
R/W							
0h							

Table 14-21053. EMIF_CTLCFG_DENALI_CTL_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_HIGH_THRESHOLD_F2	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_NORM_THRESHOLD_F2	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.370 EMIF_CTLCFG_DENALI_CTL_309 Register

1 EMIF_CTLCFG_DENALI_CTL_309 Register (Offset = 4D4h) [reset = 0h]

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Table 14-21054. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84D4h

Figure 14-6983. EMIF_CTLCFG_DENALI_CTL_309 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_TIMEOUT_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_TIMEOUT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_TIMEOUT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_TIMEOUT_F2							
R/W							
0h							

Table 14-21056. EMIF_CTLCFG_DENALI_CTL_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_TIMEOUT_F2	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_TIMEOUT_F2	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.371 EMIF_CTLCFG_DENALI_CTL_310 Register

1 EMIF_CTLCFG_DENALI_CTL_310 Register (Offset = 4D8h) [reset = 0h]

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Table 14-21057. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84D8h**

Figure 14-6984. EMIF_CTLCFG_DENALI_CTL_310 Name Register

31	30	29	28	27	26	25	24
ZQ_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQ_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ZQ_CS_TIMEOUT_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQ_CS_TIMEOUT_F2							
R/W							
0h							

Table 14-21059. EMIF_CTLCFG_DENALI_CTL_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_PROMOTE_THRESHOLD_F2	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_TIMEOUT_F2	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.372 EMIF_CTLCFG_DENALI_CTL_311 Register

1 EMIF_CTLCFG_DENALI_CTL_311 Register (Offset = 4DCh) [reset = 0h]

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Table 14-21060. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84DCh**

Figure 14-6985. EMIF_CTLCFG_DENALI_CTL_311 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQINIT_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ZQINIT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIMEOUT_TIMER_LOG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21062. EMIF_CTLCFG_DENALI_CTL_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TIMEOUT_TIMER_LOG	R	0h	Reflects which timers experienced a timeout error [or had an uncleared error] when the timeout interrupt fired. Bit [0] correlates to a ZQ cal init, cs, cl, or reset FM timeout. Bit [1] correlates to the ZQ calstart FM timeout. Bit [2] correlates to the ZQ callatch FM timeout. Bit [3] correlates to the MRR temperature check FM timeout. Bit [4] correlates to the DQS oscillator FM timeout. Bit [5] correlates to the DFI update FM timeout. Bit [6] correlates to the low power interface wakeup timeout. Bit [7] correlates to the auto refresh max deficit timeout. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.373 EMIF_CTLCFG_DENALI_CTL_312 Register

1 EMIF_CTLCFG_DENALI_CTL_312 Register (Offset = 4E0h) [reset = 0h]

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Table 14-21063. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84E0h**

Figure 14-6986. EMIF_CTLCFG_DENALI_CTL_312 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQCS_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ZQCS_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				ZQCL_F0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ZQCL_F0							
R/W							
0h							

Table 14-21065. EMIF_CTLCFG_DENALI_CTL_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCS_F0	R/W	0h	Number of cycles needed for a ZQCS command. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCL_F0	R/W	0h	Number of cycles needed for a ZQCL command. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.374 EMIF_CTLCFG_DENALI_CTL_313 Register

1 EMIF_CTLCFG_DENALI_CTL_313 Register (Offset = 4E4h) [reset = 0h]

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Table 14-21066. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84E4h**

Figure 14-6987. EMIF_CTLCFG_DENALI_CTL_313 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TZQLAT_F0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED				TZQCAL_F0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TZQCAL_F0							
R/W							
0h							

Table 14-21068. EMIF_CTLCFG_DENALI_CTL_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.375 EMIF_CTLCFG_DENALI_CTL_314 Register

1 EMIF_CTLCFG_DENALI_CTL_314 Register (Offset = 4E8h) [reset = 0h]

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Table 14-21069. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84E8h**

Figure 14-6988. EMIF_CTLCFG_DENALI_CTL_314 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQCL_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQCL_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ZQINIT_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQINIT_F1							
R/W							
0h							

Table 14-21071. EMIF_CTLCFG_DENALI_CTL_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCL_F1	R/W	0h	Number of cycles needed for a ZQCL command. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.376 EMIF_CTLCFG_DENALI_CTL_315 Register

1 EMIF_CTLCFG_DENALI_CTL_315 Register (Offset = 4ECh) [reset = 0h]

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Table 14-21072. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84ECh**

Figure 14-6989. EMIF_CTLCFG_DENALI_CTL_315 Name Register

31	30	29	28	27	26	25	24
RESERVED				TZQCAL_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TZQCAL_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ZQCS_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQCS_F1							
R/W							
0h							

Table 14-21074. EMIF_CTLCFG_DENALI_CTL_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCS_F1	R/W	0h	Number of cycles needed for a ZQCS command. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.377 EMIF_CTLCFG_DENALI_CTL_316 Register

1 EMIF_CTLCFG_DENALI_CTL_316 Register (Offset = 4F0h) [reset = 0h]

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Table 14-21075. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84F0h**

Figure 14-6990. EMIF_CTLCFG_DENALI_CTL_316 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQINIT_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ZQINIT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">TZQLAT_F1</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-21077. EMIF_CTLCFG_DENALI_CTL_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command. FC=2 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.378 EMIF_CTLCFG_DENALI_CTL_317 Register

1 EMIF_CTLCFG_DENALI_CTL_317 Register (Offset = 4F4h) [reset = 0h]

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Table 14-21078. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84F4h**

Figure 14-6991. EMIF_CTLCFG_DENALI_CTL_317 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQCS_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQCS_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ZQCL_F2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQCL_F2							
R/W							
0h							

Table 14-21080. EMIF_CTLCFG_DENALI_CTL_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCS_F2	R/W	0h	Number of cycles needed for a ZQCS command. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCL_F2	R/W	0h	Number of cycles needed for a ZQCL command. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.379 EMIF_CTLCFG_DENALI_CTL_318 Register

1 EMIF_CTLCFG_DENALI_CTL_318 Register (Offset = 4F8h) [reset = 0h]

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Table 14-21081. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 84F8h

Figure 14-6992. EMIF_CTLCFG_DENALI_CTL_318 Name Register

31	30	29	28	27	26	25	24
RESERVED						ZQ_SW_REQ_START_LATCH_MAP	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED	TZQLAT_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED				TZQCAL_F2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TZQCAL_F2							
R/W							
0h							

Table 14-21083. EMIF_CTLCFG_DENALI_CTL_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ZQ_SW_REQ_START_LATCH_MAP	R/W	0h	Specifies which chip selects will simultaneously receive a ZQ start or latch command once the ZQ_REQ parameter is written with a ZQ Start or ZQ Latch command. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.380 EMIF_CTLCFG_DENALI_CTL_319 Register

1 EMIF_CTLCFG_DENALI_CTL_319 Register (Offset = 4FCh) [reset = 0h]

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Table 14-21084. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 84FCh**

Figure 14-6993. EMIF_CTLCFG_DENALI_CTL_319 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQRESET_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ZQRESET_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							ZQ_REQ_PENDING
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED				ZQ_REQ			
NONE				W			
0h				0h			

Table 14-21086. EMIF_CTLCFG_DENALI_CTL_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQRESET_F0	R/W	0h	Number of cycles needed for a ZQRESET command. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. Value of 1 indicates command in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	ZQ_REQ	W	0h	User request to initiate a ZQ calibration. Program to 3 for ZQ Start, program to 4 for ZQ Initialization [ZQINIT], program to 5 for ZQ Latch, or program to 8 for ZQ Reset. Clearing to 0 will not trigger any ZQ command. This parameter should only be written when the ZQ_REQ_PENDING parameter is cleared to 0. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.381 EMIF_CTLCFG_DENALI_CTL_320 Register

1 EMIF_CTLCFG_DENALI_CTL_320 Register (Offset = 500h) [reset = 0h]

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Table 14-21087. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8500h**

Figure 14-6994. EMIF_CTLCFG_DENALI_CTL_320 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQRESET_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ZQRESET_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQRESET_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ZQRESET_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21089. EMIF_CTLCFG_DENALI_CTL_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQRESET_F2	R/W	0h	Number of cycles needed for a ZQRESET command. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQRESET_F1	R/W	0h	Number of cycles needed for a ZQRESET command. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.382 EMIF_CTLCFG_DENALI_CTL_321 Register

1 EMIF_CTLCFG_DENALI_CTL_321 Register (Offset = 504h) [reset = 0h]

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Table 14-21090. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8504h**

Figure 14-6995. EMIF_CTLCFG_DENALI_CTL_321 Name Register

31	30	29	28	27	26	25	24
RESERVED						ZQ_CAL_LATCH_MAP_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						ZQ_CAL_START_MAP_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ZQCS_ROTATE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							NO_ZQ_INIT
NONE							R/W
0h							0h

Table 14-21092. EMIF_CTLCFG_DENALI_CTL_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ZQ_CAL_LATCH_MAP_0	R/W	0h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. CS=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ZQ_CAL_START_MAP_0	R/W	0h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. CS=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ZQCS_ROTATE	R/W	0h	For memories that perform ZQ short commands [ZQCS], selects whether a ZQCS command will calibrate just one chip select or all chip selects. When rotation is off, all chip selects will be calibrated, requiring a longer time frame, but ZQ calibration will need to be performed less frequently. Set to 1 for rotating CS. For ZQ start/latch memories, this parameter is ignored. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21092. EMIF_CTLCFG_DENALI_CTL_321 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.383 EMIF_CTLCFG_DENALI_CTL_322 Register

1 EMIF_CTLCFG_DENALI_CTL_322 Register (Offset = 508h) [reset = 0h]

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Table 14-21093. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8508h**

Figure 14-6996. EMIF_CTLCFG_DENALI_CTL_322 Name Register

31	30	29	28	27	26	25	24
RESERVED						BANK_DIFF_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						BANK_DIFF_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						ZQ_CAL_LATCH_MAP_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						ZQ_CAL_START_MAP_1	
NONE						R/W	
0h						0h	

Table 14-21095. EMIF_CTLCFG_DENALI_CTL_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	BANK_DIFF_1	R/W	0h	Encoded number of banks on the DRAM[s]. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	BANK_DIFF_0	R/W	0h	Encoded number of banks on the DRAM[s]. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	ZQ_CAL_LATCH_MAP_1	R/W	0h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. CS=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ZQ_CAL_START_MAP_1	R/W	0h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. CS=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.384 EMIF_CTLCFG_DENALI_CTL_323 Register

1 EMIF_CTLCFG_DENALI_CTL_323 Register (Offset = 50Ch) [reset = 0h]

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Table 14-21096. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 850Ch

Figure 14-6997. EMIF_CTLCFG_DENALI_CTL_323 Name Register

31	30	29	28	27	26	25	24
RESERVED				COL_DIFF_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COL_DIFF_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					ROW_DIFF_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ROW_DIFF_0		
NONE					R/W		
0h					0h		

Table 14-21098. EMIF_CTLCFG_DENALI_CTL_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	COL_DIFF_1	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	COL_DIFF_0	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	ROW_DIFF_1	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	ROW_DIFF_0	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n

14.6.6.2.385 EMIF_CTLCFG_DENALI_CTL_324 Register

1 EMIF_CTLCFG_DENALI_CTL_324 Register (Offset = 510h) [reset = 0h]

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Table 14-21099. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8510h**

Figure 14-6998. EMIF_CTLCFG_DENALI_CTL_324 Name Register

31	30	29	28	27	26	25	24
CS_VAL_UPPER_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CS_VAL_UPPER_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_VAL_LOWER_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CS_VAL_LOWER_0							
R/W							
0h							

Table 14-21101. EMIF_CTLCFG_DENALI_CTL_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CS_VAL_UPPER_0	R/W	0h	Upper bound address for chip select 0. Reset Source: ctl_amod_g_rst_n
15:0	CS_VAL_LOWER_0	R/W	0h	Lower bound address for chip select 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.386 EMIF_CTLCFG_DENALI_CTL_325 Register

1 EMIF_CTLCFG_DENALI_CTL_325 Register (Offset = 514h) [reset = 0h]

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Table 14-21102. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8514h**

Figure 14-6999. EMIF_CTLCFG_DENALI_CTL_325 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CS_MSK_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CS_MSK_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ROW_START_VAL_0	
NONE						R/W	
0h						0h	

Table 14-21104. EMIF_CTLCFG_DENALI_CTL_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	CS_MSK_0	R/W	0h	Mask applied to the address decode for chip select 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ROW_START_VAL_0	R/W	0h	Row start value for chip select 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.387 EMIF_CTLCFG_DENALI_CTL_326 Register

1 EMIF_CTLCFG_DENALI_CTL_326 Register (Offset = 518h) [reset = 0h]

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Table 14-21105. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8518h

Figure 14-7000. EMIF_CTLCFG_DENALI_CTL_326 Name Register

31	30	29	28	27	26	25	24
CS_VAL_UPPER_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CS_VAL_UPPER_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_VAL_LOWER_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CS_VAL_LOWER_1							
R/W							
0h							

Table 14-21107. EMIF_CTLCFG_DENALI_CTL_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CS_VAL_UPPER_1	R/W	0h	Upper bound address for chip select 1. Reset Source: ctl_amod_g_rst_n
15:0	CS_VAL_LOWER_1	R/W	0h	Lower bound address for chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.388 EMIF_CTLCFG_DENALI_CTL_327 Register

1 EMIF_CTLCFG_DENALI_CTL_327 Register (Offset = 51Ch) [reset = 0h]

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Table 14-21108. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 851Ch**

Figure 14-7001. EMIF_CTLCFG_DENALI_CTL_327 Name Register

31	30	29	28	27	26	25	24
RESERVED						CS_MAP_NON_POW2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
CS_MSK_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_MSK_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROW_START_VAL_1	
NONE						R/W	
0h						0h	

Table 14-21110. EMIF_CTLCFG_DENALI_CTL_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CS_MAP_NON_POW2	R/W	0h	Defines which chip selects are non-power-of-2 memory sizes. Reset Source: ctl_amod_g_rst_n
23:8	CS_MSK_1	R/W	0h	Mask applied to the address decode for chip select 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ROW_START_VAL_1	R/W	0h	Row start value for chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.389 EMIF_CTLCFG_DENALI_CTL_328 Register

1 EMIF_CTLCFG_DENALI_CTL_328 Register (Offset = 520h) [reset = A000000h]

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Table 14-21111. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8520h**

Figure 14-7002. EMIF_CTLCFG_DENALI_CTL_328 Name Register

31	30	29	28	27	26	25	24
RESERVED			APREBIT				
NONE			R/W				
0h			Ah				
23	22	21	20	19	18	17	16
RESERVED							MC_RESERVED9
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			MC_RESERVED8				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							CS_LOWER_ADDR_EN
NONE							R/W
0h							0h

Table 14-21113. EMIF_CTLCFG_DENALI_CTL_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	APREBIT	R/W	Ah	Location of the auto pre-charge bit in the DRAM address. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MC_RESERVED9	R/W	0h	Reserved
15:13	RESERVED	NONE	0h	Reserved
12:8	MC_RESERVED8	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	CS_LOWER_ADDR_EN	R/W	0h	Enables moving the CS field to lower in the address map. When set to 1, the memory address map will be changed to ROW__CS__BANK. Please refer to the limitations before setting this bit. Reset Source: ctl_amod_g_rst_n

14.6.6.2.390 EMIF_CTLCFG_DENALI_CTL_329 Register

1 EMIF_CTLCFG_DENALI_CTL_329 Register (Offset = 524h) [reset = 0h]

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Table 14-21114. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8524h**

Figure 14-7003. EMIF_CTLCFG_DENALI_CTL_329 Name Register

31	30	29	28	27	26	25	24
RESERVED							ADDR_COLLISION_MPM_DIS
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							ADDR_CMP_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
COMMAND_AGE_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
AGE_COUNT							
R/W							
0h							

Table 14-21116. EMIF_CTLCFG_DENALI_CTL_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ADDR_COLLISION_MPM_DIS	R/W	0h	Disable address collision detection extension using micro page mask for command queue placement and selection. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	ADDR_CMP_EN	R/W	0h	Enable address collision detection as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	COMMAND_AGE_COUNT	R/W	0h	Initial value of individual command aging counters for command aging. Reset Source: ctl_amod_g_rst_n
7:0	AGE_COUNT	R/W	0h	Initial value of controller aging-rate counter for command aging. Reset Source: ctl_amod_g_rst_n

14.6.6.2.391 EMIF_CTLCFG_DENALI_CTL_330 Register

1 EMIF_CTLCFG_DENALI_CTL_330 Register (Offset = 528h) [reset = 0h]

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Table 14-21117. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8528h

Figure 14-7004. EMIF_CTLCFG_DENALI_CTL_330 Name Register

31	30	29	28	27	26	25	24
RESERVED							RW_SAME_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PRIORITY_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PLACEMENT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							BANK_SPLIT_EN
NONE							R/W
0h							0h

Table 14-21119. EMIF_CTLCFG_DENALI_CTL_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RW_SAME_EN	R/W	0h	Enable read/write grouping as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PRIORITY_EN	R/W	0h	Enable priority as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PLACEMENT_EN	R/W	0h	Enable placement logic for command queue. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BANK_SPLIT_EN	R/W	0h	Enable bank splitting as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.392 EMIF_CTLCFG_DENALI_CTL_331 Register

1 EMIF_CTLCFG_DENALI_CTL_331 Register (Offset = 52Ch) [reset = 0h]

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Table 14-21120. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 852Ch**

Figure 14-7005. EMIF_CTLCFG_DENALI_CTL_331 Name Register

31	30	29	28	27	26	25	24
RESERVED						DISABLE_RW_GROUP_W_BNK_CONFLICT	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							W2R_SPLIT_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CS_SAME_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RW_SAME_PAGE_EN
NONE							R/W
0h							0h

Table 14-21122. EMIF_CTLCFG_DENALI_CTL_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DISABLE_RW_GROUP_W_BNK_CONFLICT	R/W	0h	Disables placement to read/write group when grouping creates a bank collision. Bit [0] controls placement next to bank conflict command and bit [1] controls placement 2 away from bank conflict command. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	W2R_SPLIT_EN	R/W	0h	Enable splitting of commands to the same chip select from a write to a read command as a rule for command queue placement. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	CS_SAME_EN	R/W	0h	Enable chip select grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21122. EMIF_CTLCFG_DENALI_CTL_331 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RW_SAME_PAGE_EN	R/W	0h	Enable page grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.393 EMIF_CTLCFG_DENALI_CTL_332 Register

1 EMIF_CTLCFG_DENALI_CTL_332 Register (Offset = 530h) [reset = 0h]

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Table 14-21123. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8530h**

Figure 14-7006. EMIF_CTLCFG_DENALI_CTL_332 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">INHIBIT_DRAM_CMD</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>DISABLE_RD_INTERLEAVE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>SWAP_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">NUM_Q_ENTRIES_ACT_DISABLE</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-21125. EMIF_CTLCFG_DENALI_CTL_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	INHIBIT_DRAM_CMD	R/W	0h	Inhibit command types from being executed from the command queue. Clear to 0 to enable any command, program to 1 to inhibit read/write and bank commands, program to 2 to inhibit MRR and peripheral MRR commands, or program to 3 to inhibit MRR and read/write commands. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DISABLE_RD_INTERLEAVE	R/W	0h	Disable read data interleaving for commands from the same port, regardless of the requestor ID. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SWAP_EN	R/W	0h	Enable command swapping logic in execution unit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	NUM_Q_ENTRIES_ACT_DISABLE	R/W	0h	Number of queue entries in which ACT requests will be disabled. Programming to X will disable ACT requests from the X entries lowest in the command queue. Reset Source: ctl_amod_g_rst_n

14.6.6.2.394 EMIF_CTLCFG_DENALI_CTL_333 Register

1 EMIF_CTLCFG_DENALI_CTL_333 Register (Offset = 534h) [reset = 0h]

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Table 14-21126. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8534h**

Figure 14-7007. EMIF_CTLCFG_DENALI_CTL_333 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MEMDATA_RATIO_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MEM_DP_REDUCTION</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">BURST_ON_FLY_BIT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CS_MAP</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-21128. EMIF_CTLCFG_DENALI_CTL_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	MEMDATA_RATIO_0	R/W	0h	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. CS=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MEM_DP_REDUCTION	R/W	0h	Enable the half datapath feature of the controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	BURST_ON_FLY_BIT	R/W	0h	Identifies the burst-on-fly bit in the memory mode registers. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CS_MAP	R/W	0h	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n

14.6.6.2.395 EMIF_CTLCFG_DENALI_CTL_334 Register

1 EMIF_CTLCFG_DENALI_CTL_334 Register (Offset = 538h) [reset = 0h]

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Table 14-21129. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8538h**

Figure 14-7008. EMIF_CTLCFG_DENALI_CTL_334 Name Register

31	30	29	28	27	26	25	24
RESERVED				DEVICE2_BYTE0_CS0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				DEVICE1_BYTE0_CS0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				DEVICE0_BYTE0_CS0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MEMDATA_RATIO_1		
NONE					R/W		
0h					0h		

Table 14-21131. EMIF_CTLCFG_DENALI_CTL_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	DEVICE2_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 2 on chip 0. Used for MRRs to identify where data will be returned. DEV=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	DEVICE1_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 0. Used for MRRs to identify where data will be returned. DEV=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	DEVICE0_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 0. Used for MRRs to identify where data will be returned. DEV=0 Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MEMDATA_RATIO_1	R/W	0h	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. CS=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.396 EMIF_CTLCFG_DENALI_CTL_335 Register

1 EMIF_CTLCFG_DENALI_CTL_335 Register (Offset = 53Ch) [reset = 0h]

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Table 14-21132. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 853Ch

Figure 14-7009. EMIF_CTLCFG_DENALI_CTL_335 Name Register

31	30	29	28	27	26	25	24
RESERVED				DEVICE2_BYTE0_CS1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				DEVICE1_BYTE0_CS1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				DEVICE0_BYTE0_CS1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				DEVICE3_BYTE0_CS0			
NONE				R/W			
0h				0h			

Table 14-21134. EMIF_CTLCFG_DENALI_CTL_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	DEVICE2_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 2 on chip 1. Used for MRRs to identify where data will be returned. DEV=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	DEVICE1_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 1. Used for MRRs to identify where data will be returned. DEV=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	DEVICE0_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 1. Used for MRRs to identify where data will be returned. DEV=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	DEVICE3_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 3 on chip 0. Used for MRRs to identify where data will be returned. DEV=3 Reset Source: ctl_amod_g_rst_n

14.6.6.2.397 EMIF_CTLCFG_DENALI_CTL_336 Register

1 EMIF_CTLCFG_DENALI_CTL_336 Register (Offset = 540h) [reset = 0h]

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Table 14-21135. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8540h**

Figure 14-7010. EMIF_CTLCFG_DENALI_CTL_336 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">WR_ORDER_REQ</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>IN_ORDER_ACCEPT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">Q_FULLNESS</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DEVICE3_BYTE0_CS1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21137. EMIF_CTLCFG_DENALI_CTL_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	WR_ORDER_REQ	R/W	0h	Determines if the controller can re-order write commands from the same source ID and/or the same port. Bit [0] controls source ID usage and bit [1] controls port ID usage. Set each bit to 1 to enable usage in placement logic. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	IN_ORDER_ACCEPT	R/W	0h	Forces the controller to accept commands in the order in which they are placed in the command queue. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	Q_FULLNESS	R/W	0h	Quantity that determines when the command queue almost full signal will assert [q_almost_full]. When cleared to 0, the q_almost_full signal will be driven to 0 irrespective of number of entries in the command queue. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-21137. EMIF_CTLCFG_DENALI_CTL_336 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	DEVICE3_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 3 on chip 1. Used for MRRs to identify where data will be returned. DEV=3 Reset Source: ctl_amod_g_rst_n

14.6.6.2.398 EMIF_CTLCFG_DENALI_CTL_337 Register

1 EMIF_CTLCFG_DENALI_CTL_337 Register (Offset = 544h) [reset = 0h]

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Table 14-21138. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8544h

Figure 14-7011. EMIF_CTLCFG_DENALI_CTL_337 Name Register

31	30	29	28	27	26	25	24
RESERVED							CTRLUPD_AREF_HP_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CTRLUPD_REQ_PER_AREF_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CTRLUPD_REQ
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CONTROLLER_BUSY
NONE							R
0h							0h

Table 14-21140. EMIF_CTLCFG_DENALI_CTL_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CTRLUPD_AREF_HP_ENABLE	R/W	0h	Enable an automatic controller-initiated update [dfi_ctrlupd_req] after every high priority refresh when executing as a subtask request. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic controller-initiated update [dfi_ctrlupd_req] after every refresh. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	CTRLUPD_REQ	W	0h	Assert the DFI controller-initiated update request signal dfi_ctrlupd_req. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21140. EMIF_CTLCFG_DENALI_CTL_337 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CONTROLLER_BUSY	R	0h	Indicator that the controller is processing a command. Evaluates all ports for outstanding transactions. Value of 1 indicates controller busy. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.399 EMIF_CTLCFG_DENALI_CTL_338 Register

1 EMIF_CTLCFG_DENALI_CTL_338 Register (Offset = 548h) [reset = 0h]

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Table 14-21141. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8548h**

Figure 14-7012. EMIF_CTLCFG_DENALI_CTL_338 Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_PREAMBLE_TRAINING_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PREAMBLE_SUPPORT_F2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PREAMBLE_SUPPORT_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PREAMBLE_SUPPORT_F0	
NONE						R/W	
0h						0h	

Table 14-21143. EMIF_CTLCFG_DENALI_CTL_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PREAMBLE_SUPPORT_F2	R/W	0h	Selection the preamble for read and write burst transfers. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PREAMBLE_SUPPORT_F1	R/W	0h	Selection the preamble for read and write burst transfers. FC=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PREAMBLE_SUPPORT_F0	R/W	0h	Selection the preamble for read and write burst transfers. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.400 EMIF_CTLCFG_DENALI_CTL_339 Register

1 EMIF_CTLCFG_DENALI_CTL_339 Register (Offset = 54Ch) [reset = 0h]

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Table 14-21144. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 854Ch**

Figure 14-7013. EMIF_CTLCFG_DENALI_CTL_339 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			DFI_ERROR				
NONE			R				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							RD_DBI_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							WR_DBI_EN
NONE							R/W
0h							0h

Table 14-21146. EMIF_CTLCFG_DENALI_CTL_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	DFI_ERROR	R	0h	Indicates that the DFI error flag has been asserted. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	RD_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for read data with DDR4 devices. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	WR_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for write data with DDR4 devices. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.401 EMIF_CTLCFG_DENALI_CTL_340 Register

1 EMIF_CTLCFG_DENALI_CTL_340 Register (Offset = 550h) [reset = 0h]

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Table 14-21147. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8550h**

Figure 14-7014. EMIF_CTLCFG_DENALI_CTL_340 Name Register

31	30	29	28	27	26	25	24
RESERVED							BG_ROTATE_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				DFI_ERROR_INFO			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
DFI_ERROR_INFO							
R							
0h							
7	6	5	4	3	2	1	0
DFI_ERROR_INFO							
R							
0h							

Table 14-21149. EMIF_CTLCFG_DENALI_CTL_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	BG_ROTATE_EN	R/W	0h	Enable bank group rotation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	DFI_ERROR_INFO	R	0h	Holds the encoded DFI error type associated with the DFI_ERROR parameter assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.402 EMIF_CTLCFG_DENALI_CTL_341 Register

1 EMIF_CTLCFG_DENALI_CTL_341 Register (Offset = 554h) [reset = 0h]

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Table 14-21150. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8554h

Figure 14-7015. EMIF_CTLCFG_DENALI_CTL_341 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							MC_RESERVED10
NONE							W
0h							0h

Table 14-21152. EMIF_CTLCFG_DENALI_CTL_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MC_RESERVED10	W	0h	Reserved

14.6.6.2.403 EMIF_CTLCFG_DENALI_CTL_342 Register

1 EMIF_CTLCFG_DENALI_CTL_342 Register (Offset = 558h) [reset = 0h]

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Table 14-21153. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8558h**

Figure 14-7016. EMIF_CTLCFG_DENALI_CTL_342 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_MASTER							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INT_STATUS_MASTER							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INT_STATUS_MASTER							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT_STATUS_MASTER							
R							
0h							

Table 14-21155. EMIF_CTLCFG_DENALI_CTL_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_MASTER	R	0h	Controller status reporting register for interrupt status groups. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.404 EMIF_CTLCFG_DENALI_CTL_343 Register

1 EMIF_CTLCFG_DENALI_CTL_343 Register (Offset = 55Ch) [reset = 0h]

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Table 14-21156. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 855Ch

Figure 14-7017. EMIF_CTLCFG_DENALI_CTL_343 Name Register

31	30	29	28	27	26	25	24
INT_MASK_MASTER							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_MASTER							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_MASTER							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MASTER							
R/W							
0h							

Table 14-21158. EMIF_CTLCFG_DENALI_CTL_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_MASTER	R/W	0h	Controller mask register for interrupt status groups. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.405 EMIF_CTLCFG_DENALI_CTL_344 Register

1 EMIF_CTLCFG_DENALI_CTL_344 Register (Offset = 560h) [reset = 0h]

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Table 14-21159. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8560h**

Figure 14-7018. EMIF_CTLCFG_DENALI_CTL_344 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_TIMEOUT							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_TIMEOUT							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_TIMEOUT							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_TIMEOUT							
R							
0h							

Table 14-21161. EMIF_CTLCFG_DENALI_CTL_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_TIMEOUT	R	0h	Status of interrupts in the controller related to Timeout monitors. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.406 EMIF_CTLCFG_DENALI_CTL_345 Register

1 EMIF_CTLCFG_DENALI_CTL_345 Register (Offset = 564h) [reset = 0h]

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Table 14-21162. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8564h**

Figure 14-7019. EMIF_CTLCFG_DENALI_CTL_345 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_LOWPOWER							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INT_STATUS_LOWPOWER							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MC_RESERVED11							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MC_RESERVED11							
R							
0h							

Table 14-21164. EMIF_CTLCFG_DENALI_CTL_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_STATUS_LOWPOWER	R	0h	Status of interrupts in the controller related to Low Power. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED11	R	0h	Reserved

14.6.6.2.407 EMIF_CTLCFG_DENALI_CTL_346 Register

1 EMIF_CTLCFG_DENALI_CTL_346 Register (Offset = 568h) [reset = 0h]

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Table 14-21165. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8568h**

Figure 14-7020. EMIF_CTLCFG_DENALI_CTL_346 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED13							
R							
0h							
23	22	21	20	19	18	17	16
MC_RESERVED13							
R							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED12							
R							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED12							
R							
0h							

Table 14-21167. EMIF_CTLCFG_DENALI_CTL_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED13	R	0h	Reserved
15:0	MC_RESERVED12	R	0h	Reserved

14.6.6.2.408 EMIF_CTLCFG_DENALI_CTL_347 Register

1 EMIF_CTLCFG_DENALI_CTL_347 Register (Offset = 56Ch) [reset = 0h]

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Table 14-21168. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 856Ch

Figure 14-7021. EMIF_CTLCFG_DENALI_CTL_347 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_TRAINING							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_TRAINING							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_TRAINING							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_TRAINING							
R							
0h							

Table 14-21170. EMIF_CTLCFG_DENALI_CTL_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_TRAINING	R	0h	Status of interrupts in the controller related to Training/Calibration. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.409 EMIF_CTLCFG_DENALI_CTL_348 Register

1 EMIF_CTLCFG_DENALI_CTL_348 Register (Offset = 570h) [reset = 0h]

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Table 14-21171. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8570h**

Figure 14-7022. EMIF_CTLCFG_DENALI_CTL_348 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_USERIF							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_USERIF							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_USERIF							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_USERIF							
R							
0h							

Table 14-21173. EMIF_CTLCFG_DENALI_CTL_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_USERIF	R	0h	Status of interrupts in the controller related to ASIC to Controller Interface. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.410 EMIF_CTLCFG_DENALI_CTL_349 Register

1 EMIF_CTLCFG_DENALI_CTL_349 Register (Offset = 574h) [reset = 0h]

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Table 14-21174. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8574h**

Figure 14-7023. EMIF_CTLCFG_DENALI_CTL_349 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED14							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_BIST							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_MISC							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_MISC							
R							
0h							

Table 14-21176. EMIF_CTLCFG_DENALI_CTL_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED14	R	0h	Reserved
23:16	INT_STATUS_BIST	R	0h	Status of interrupts in the controller related to BIST. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	INT_STATUS_MISC	R	0h	Status of interrupts in the controller related to Miscellaneous features. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.411 EMIF_CTLCFG_DENALI_CTL_350 Register

1 EMIF_CTLCFG_DENALI_CTL_350 Register (Offset = 578h) [reset = 0h]

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Table 14-21177. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8578h**

Figure 14-7024. EMIF_CTLCFG_DENALI_CTL_350 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_INIT							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_FREQ							
R							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED15							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_DFI							
R							
0h							

Table 14-21179. EMIF_CTLCFG_DENALI_CTL_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_STATUS_INIT	R	0h	Status of interrupts in the controller related to Initialization. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	INT_STATUS_FREQ	R	0h	Status of interrupts in the controller related to Frequency Scaling. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED15	R	0h	Reserved
7:0	INT_STATUS_DFI	R	0h	Status of interrupts in the controller related to DFI. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.412 EMIF_CTLCFG_DENALI_CTL_351 Register

1 EMIF_CTLCFG_DENALI_CTL_351 Register (Offset = 57Ch) [reset = 0h]

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Table 14-21180. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 857Ch**

Figure 14-7025. EMIF_CTLCFG_DENALI_CTL_351 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_PARITY							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_MODE							
R							
0h							

Table 14-21182. EMIF_CTLCFG_DENALI_CTL_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_STATUS_PARITY	R	0h	Status of interrupts in the controller related to Parity. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	INT_STATUS_MODE	R	0h	Status of interrupts in the controller related to Memory Mode Settings. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.413 EMIF_CTLCFG_DENALI_CTL_352 Register

1 EMIF_CTLCFG_DENALI_CTL_352 Register (Offset = 580h) [reset = 0h]

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Table 14-21183. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8580h**

Figure 14-7026. EMIF_CTLCFG_DENALI_CTL_352 Name Register

31	30	29	28	27	26	25	24
INT_ACK_TIMEOUT							
W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INT_ACK_TIMEOUT							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INT_ACK_TIMEOUT							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT_ACK_TIMEOUT							
W							
0h							

Table 14-21185. EMIF_CTLCFG_DENALI_CTL_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_TIMEOUT	W	0h	Clear status of the INT_STATUS_TIMEOUT parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.414 EMIF_CTLCFG_DENALI_CTL_353 Register

1 EMIF_CTLCFG_DENALI_CTL_353 Register (Offset = 584h) [reset = 0h]

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Table 14-21186. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8584h**

Figure 14-7027. EMIF_CTLCFG_DENALI_CTL_353 Name Register

31	30	29	28	27	26	25	24
INT_ACK_LOWPOWER							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_LOWPOWER							
W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED16							
W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED16							
W							
0h							

Table 14-21188. EMIF_CTLCFG_DENALI_CTL_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_ACK_LOWPOWER	W	0h	Clear status of the INT_STATUS_LOWPOWER parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED16	W	0h	Reserved

14.6.6.2.415 EMIF_CTLCFG_DENALI_CTL_354 Register

1 EMIF_CTLCFG_DENALI_CTL_354 Register (Offset = 588h) [reset = 0h]

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Table 14-21189. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8588h**

Figure 14-7028. EMIF_CTLCFG_DENALI_CTL_354 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MC_RESERVED18</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MC_RESERVED18</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MC_RESERVED17</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MC_RESERVED17</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21191. EMIF_CTLCFG_DENALI_CTL_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED18	W	0h	Reserved
15:0	MC_RESERVED17	W	0h	Reserved

14.6.6.2.416 EMIF_CTLCFG_DENALI_CTL_355 Register

1 EMIF_CTLCFG_DENALI_CTL_355 Register (Offset = 58Ch) [reset = 0h]

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Table 14-21192. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 858Ch**

Figure 14-7029. EMIF_CTLCFG_DENALI_CTL_355 Name Register

31	30	29	28	27	26	25	24
INT_ACK_TRAINING							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_TRAINING							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_TRAINING							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_TRAINING							
W							
0h							

Table 14-21194. EMIF_CTLCFG_DENALI_CTL_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_TRAINING	W	0h	Clear status of the INT_STATUS_TRAINING parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.417 EMIF_CTLCFG_DENALI_CTL_356 Register

1 EMIF_CTLCFG_DENALI_CTL_356 Register (Offset = 590h) [reset = 0h]

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Table 14-21195. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8590h

Figure 14-7030. EMIF_CTLCFG_DENALI_CTL_356 Name Register

31	30	29	28	27	26	25	24
INT_ACK_USERIF							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_USERIF							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_USERIF							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_USERIF							
W							
0h							

Table 14-21197. EMIF_CTLCFG_DENALI_CTL_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_USERIF	W	0h	Clear status of the INT_STATUS_USERIF parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.418 EMIF_CTLCFG_DENALI_CTL_357 Register

1 EMIF_CTLCFG_DENALI_CTL_357 Register (Offset = 594h) [reset = 0h]

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Table 14-21198. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8594h**

Figure 14-7031. EMIF_CTLCFG_DENALI_CTL_357 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED19							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_BIST							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_MISC							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_MISC							
W							
0h							

Table 14-21200. EMIF_CTLCFG_DENALI_CTL_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED19	W	0h	Reserved
23:16	INT_ACK_BIST	W	0h	Clear status of the INT_STATUS_BIST parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	INT_ACK_MISC	W	0h	Clear status of the INT_STATUS_MISC parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.419 EMIF_CTLCFG_DENALI_CTL_358 Register

1 EMIF_CTLCFG_DENALI_CTL_358 Register (Offset = 598h) [reset = 0h]

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Table 14-21201. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8598h**

Figure 14-7032. EMIF_CTLCFG_DENALI_CTL_358 Name Register

31	30	29	28	27	26	25	24
INT_ACK_INIT							
W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INT_ACK_FREQ							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MC_RESERVED20							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT_ACK_DFI							
W							
0h							

Table 14-21203. EMIF_CTLCFG_DENALI_CTL_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_ACK_INIT	W	0h	Clear status of the INT_STATUS_INIT parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:16	INT_ACK_FREQ	W	0h	Clear status of the INT_STATUS_FREQ parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED20	W	0h	Reserved
7:0	INT_ACK_DFI	W	0h	Clear status of the INT_STATUS_DFI parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.420 EMIF_CTLCFG_DENALI_CTL_359 Register

1 EMIF_CTLCFG_DENALI_CTL_359 Register (Offset = 59Ch) [reset = 0h]

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Table 14-21204. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 859Ch**

Figure 14-7033. EMIF_CTLCFG_DENALI_CTL_359 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INT_ACK_PARITY							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_MODE							
W							
0h							

Table 14-21206. EMIF_CTLCFG_DENALI_CTL_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_ACK_PARITY	W	0h	Clear status of the INT_STATUS_PARITY parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:0	INT_ACK_MODE	W	0h	Clear status of the INT_STATUS_MODE parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.421 EMIF_CTLCFG_DENALI_CTL_360 Register

1 EMIF_CTLCFG_DENALI_CTL_360 Register (Offset = 5A0h) [reset = 0h]

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Table 14-21207. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 85A0h

Figure 14-7034. EMIF_CTLCFG_DENALI_CTL_360 Name Register

31	30	29	28	27	26	25	24
INT_MASK_TIMEOUT							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_TIMEOUT							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_TIMEOUT							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_TIMEOUT							
R/W							
0h							

Table 14-21209. EMIF_CTLCFG_DENALI_CTL_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_TIMEOUT	R/W	0h	Mask for the controller_int signal from the INT_MASK_TIMEOUT parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.422 EMIF_CTLCFG_DENALI_CTL_361 Register

1 EMIF_CTLCFG_DENALI_CTL_361 Register (Offset = 5A4h) [reset = 0h]

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Table 14-21210. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85A4h**

Figure 14-7035. EMIF_CTLCFG_DENALI_CTL_361 Name Register

31	30	29	28	27	26	25	24
INT_MASK_LOWPOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_LOWPOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED21							
R/W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED21							
R/W							
0h							

Table 14-21212. EMIF_CTLCFG_DENALI_CTL_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_MASK_LOWPOWER	R/W	0h	Mask for the controller_int signal from the INT_MASK_LOWPOWER parameter Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED21	R/W	0h	Reserved

14.6.6.2.423 EMIF_CTLCFG_DENALI_CTL_362 Register

1 EMIF_CTLCFG_DENALI_CTL_362 Register (Offset = 5A8h) [reset = 0h]

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Table 14-21213. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85A8h**

Figure 14-7036. EMIF_CTLCFG_DENALI_CTL_362 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED23							
R/W							
0h							
23	22	21	20	19	18	17	16
MC_RESERVED23							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED22							
R/W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED22							
R/W							
0h							

Table 14-21215. EMIF_CTLCFG_DENALI_CTL_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED23	R/W	0h	Reserved
15:0	MC_RESERVED22	R/W	0h	Reserved

14.6.6.2.424 EMIF_CTLCFG_DENALI_CTL_363 Register

1 EMIF_CTLCFG_DENALI_CTL_363 Register (Offset = 5ACh) [reset = 0h]

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Table 14-21216. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85ACh**

Figure 14-7037. EMIF_CTLCFG_DENALI_CTL_363 Name Register

31	30	29	28	27	26	25	24
INT_MASK_TRAINING							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_TRAINING							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_TRAINING							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_TRAINING							
R/W							
0h							

Table 14-21218. EMIF_CTLCFG_DENALI_CTL_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_TRAINING	R/W	0h	Mask for the controller_int signal from the INT_MASK_TRAINING parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.425 EMIF_CTLCFG_DENALI_CTL_364 Register

1 EMIF_CTLCFG_DENALI_CTL_364 Register (Offset = 5B0h) [reset = 0h]

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Table 14-21219. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85B0h**

Figure 14-7038. EMIF_CTLCFG_DENALI_CTL_364 Name Register

31	30	29	28	27	26	25	24
INT_MASK_USERIF							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_USERIF							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_USERIF							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_USERIF							
R/W							
0h							

Table 14-21221. EMIF_CTLCFG_DENALI_CTL_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_USERIF	R/W	0h	Mask for the controller_int signal from the INT_MASK_USERIF parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.426 EMIF_CTLCFG_DENALI_CTL_365 Register

1 EMIF_CTLCFG_DENALI_CTL_365 Register (Offset = 5B4h) [reset = 0h]

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Table 14-21222. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85B4h**

Figure 14-7039. EMIF_CTLCFG_DENALI_CTL_365 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED24							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_BIST							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_MISC							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MISC							
R/W							
0h							

Table 14-21224. EMIF_CTLCFG_DENALI_CTL_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED24	R/W	0h	Reserved
23:16	INT_MASK_BIST	R/W	0h	Mask for the controller_int signal from the INT_MASK_BIST parameter Reset Source: ctl_amod_g_rst_n
15:0	INT_MASK_MISC	R/W	0h	Mask for the controller_int signal from the INT_MASK_MISC parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.427 EMIF_CTLCFG_DENALI_CTL_366 Register

1 EMIF_CTLCFG_DENALI_CTL_366 Register (Offset = 5B8h) [reset = 0h]

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Table 14-21225. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85B8h**

Figure 14-7040. EMIF_CTLCFG_DENALI_CTL_366 Name Register

31	30	29	28	27	26	25	24
INT_MASK_INIT							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_FREQ							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED25							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_DFI							
R/W							
0h							

Table 14-21227. EMIF_CTLCFG_DENALI_CTL_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_MASK_INIT	R/W	0h	Mask for the controller_int signal from the INT_MASK_INIT parameter Reset Source: ctl_amod_g_rst_n
23:16	INT_MASK_FREQ	R/W	0h	Mask for the controller_int signal from the INT_MASK_FREQ parameter Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED25	R/W	0h	Reserved
7:0	INT_MASK_DFI	R/W	0h	Mask for the controller_int signal from the INT_MASK_DFI parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.428 EMIF_CTLCFG_DENALI_CTL_367 Register

1 EMIF_CTLCFG_DENALI_CTL_367 Register (Offset = 5BCh) [reset = 0h]

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Table 14-21228. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85BCh**

Figure 14-7041. EMIF_CTLCFG_DENALI_CTL_367 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INT_MASK_PARITY							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MODE							
R/W							
0h							

Table 14-21230. EMIF_CTLCFG_DENALI_CTL_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_MASK_PARITY	R/W	0h	Mask for the controller_int signal from the INT_MASK_PARITY parameter Reset Source: ctl_amod_g_rst_n
7:0	INT_MASK_MODE	R/W	0h	Mask for the controller_int signal from the INT_MASK_MODE parameter Reset Source: ctl_amod_g_rst_n

14.6.6.2.429 EMIF_CTLCFG_DENALI_CTL_368 Register

1 EMIF_CTLCFG_DENALI_CTL_368 Register (Offset = 5C0h) [reset = 0h]

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Table 14-21231. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85C0h**

Figure 14-7042. EMIF_CTLCFG_DENALI_CTL_368 Name Register

31	30	29	28	27	26	25	24
OUT_OF_RANGE_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
OUT_OF_RANGE_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
OUT_OF_RANGE_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
OUT_OF_RANGE_ADDR_0							
R							
0h							

Table 14-21233. EMIF_CTLCFG_DENALI_CTL_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_OF_RANGE_ADDR_0	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.430 EMIF_CTLCFG_DENALI_CTL_369 Register

1 EMIF_CTLCFG_DENALI_CTL_369 Register (Offset = 5C4h) [reset = 0h]

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Table 14-21234. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85C4h**

Figure 14-7043. EMIF_CTLCFG_DENALI_CTL_369 Name Register

31	30	29	28	27	26	25	24
RESERVED	OUT_OF_RANGE_TYPE						
NONE	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUT_OF_RANGE_LENGTH			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUT_OF_RANGE_LENGTH							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OUT_OF_RANGE_ADDR_1		
NONE					R		
0h					0h		

Table 14-21236. EMIF_CTLCFG_DENALI_CTL_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	OUT_OF_RANGE_TYPE	R	0h	Type of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:8	OUT_OF_RANGE_LENGTH	R	0h	Length of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	OUT_OF_RANGE_ADDR_1	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.431 EMIF_CTLCFG_DENALI_CTL_370 Register

1 EMIF_CTLCFG_DENALI_CTL_370 Register (Offset = 5C8h) [reset = 0h]

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Table 14-21237. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85C8h**

Figure 14-7044. EMIF_CTLCFG_DENALI_CTL_370 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		OUT_OF_RANGE_SOURCE_ID					
NONE		R					
0h		0h					

Table 14-21239. EMIF_CTLCFG_DENALI_CTL_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	OUT_OF_RANGE_SOURCE_ID	R	0h	Source ID of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.432 EMIF_CTLCFG_DENALI_CTL_371 Register

1 EMIF_CTLCFG_DENALI_CTL_371 Register (Offset = 5CCh) [reset = 0h]

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Table 14-21240. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85CCh**

Figure 14-7045. EMIF_CTLCFG_DENALI_CTL_371 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_0							
R							
0h							

Table 14-21242. EMIF_CTLCFG_DENALI_CTL_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.433 EMIF_CTLCFG_DENALI_CTL_372 Register

1 EMIF_CTLCFG_DENALI_CTL_372 Register (Offset = 5D0h) [reset = 0h]

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Table 14-21243. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85D0h**

Figure 14-7046. EMIF_CTLCFG_DENALI_CTL_372 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_1							
R							
0h							

Table 14-21245. EMIF_CTLCFG_DENALI_CTL_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.434 EMIF_CTLCFG_DENALI_CTL_373 Register

1 EMIF_CTLCFG_DENALI_CTL_373 Register (Offset = 5D4h) [reset = 0h]

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Table 14-21246. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85D4h**

Figure 14-7047. EMIF_CTLCFG_DENALI_CTL_373 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_2							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_2							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_2							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_2							
R							
0h							

Table 14-21248. EMIF_CTLCFG_DENALI_CTL_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_2	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.435 EMIF_CTLCFG_DENALI_CTL_374 Register

1 EMIF_CTLCFG_DENALI_CTL_374 Register (Offset = 5D8h) [reset = 0h]

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Table 14-21249. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85D8h**

Figure 14-7048. EMIF_CTLCFG_DENALI_CTL_374 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_3							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_3							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_3							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_3							
R							
0h							

Table 14-21251. EMIF_CTLCFG_DENALI_CTL_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_3	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.436 EMIF_CTLCFG_DENALI_CTL_375 Register

1 EMIF_CTLCFG_DENALI_CTL_375 Register (Offset = 5DCh) [reset = 0h]

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Table 14-21252. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85DCh**

Figure 14-7049. EMIF_CTLCFG_DENALI_CTL_375 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_DATA_0							
R							
0h							

Table 14-21254. EMIF_CTLCFG_DENALI_CTL_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.437 EMIF_CTLCFG_DENALI_CTL_376 Register

1 EMIF_CTLCFG_DENALI_CTL_376 Register (Offset = 5E0h) [reset = 0h]

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Table 14-21255. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 85E0h

Figure 14-7050. EMIF_CTLCFG_DENALI_CTL_376 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_DATA_1							
R							
0h							

Table 14-21257. EMIF_CTLCFG_DENALI_CTL_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.438 EMIF_CTLCFG_DENALI_CTL_377 Register

1 EMIF_CTLCFG_DENALI_CTL_377 Register (Offset = 5E4h) [reset = 0h]

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Table 14-21258. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 85E4h

Figure 14-7051. EMIF_CTLCFG_DENALI_CTL_377 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIST_FAIL_DATA_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_FAIL_DATA_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_FAIL_DATA_2							
R							
0h							

Table 14-21260. EMIF_CTLCFG_DENALI_CTL_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_2	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.439 EMIF_CTLCFG_DENALI_CTL_378 Register

1 EMIF_CTLCFG_DENALI_CTL_378 Register (Offset = 5E8h) [reset = 0h]

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Table 14-21261. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85E8h**

Figure 14-7052. EMIF_CTLCFG_DENALI_CTL_378 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_3							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_DATA_3							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_DATA_3							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_DATA_3							
R							
0h							

Table 14-21263. EMIF_CTLCFG_DENALI_CTL_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_3	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.440 EMIF_CTLCFG_DENALI_CTL_379 Register

1 EMIF_CTLCFG_DENALI_CTL_379 Register (Offset = 5ECh) [reset = 0h]

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Table 14-21264. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 85ECh

Figure 14-7053. EMIF_CTLCFG_DENALI_CTL_379 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_ADDR_0							
R							
0h							

Table 14-21266. EMIF_CTLCFG_DENALI_CTL_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_ADDR_0	R	0h	Address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.441 EMIF_CTLCFG_DENALI_CTL_380 Register

1 EMIF_CTLCFG_DENALI_CTL_380 Register (Offset = 5F0h) [reset = 0h]

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Table 14-21267. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85F0h**

Figure 14-7054. EMIF_CTLCFG_DENALI_CTL_380 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					BIST_FAIL_ADDR_1		
NONE					R		
0h					0h		

Table 14-21269. EMIF_CTLCFG_DENALI_CTL_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	BIST_FAIL_ADDR_1	R	0h	Address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.442 EMIF_CTLCFG_DENALI_CTL_381 Register

1 EMIF_CTLCFG_DENALI_CTL_381 Register (Offset = 5F4h) [reset = 0h]

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Table 14-21270. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85F4h**

Figure 14-7055. EMIF_CTLCFG_DENALI_CTL_381 Name Register

31	30	29	28	27	26	25	24
PORT_CMD_ERROR_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
PORT_CMD_ERROR_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
PORT_CMD_ERROR_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
PORT_CMD_ERROR_ADDR_0							
R							
0h							

Table 14-21272. EMIF_CTLCFG_DENALI_CTL_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_CMD_ERROR_ADDR_0	R	0h	Address of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.443 EMIF_CTLCFG_DENALI_CTL_382 Register

1 EMIF_CTLCFG_DENALI_CTL_382 Register (Offset = 5F8h) [reset = 0h]

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Table 14-21273. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85F8h**

Figure 14-7056. EMIF_CTLCFG_DENALI_CTL_382 Name Register

31	30	29	28	27	26	25	24
TODTL_2CMD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED						PORT_CMD_ERROR_TYPE	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED		PORT_CMD_ERROR_ID					
NONE		R					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED					PORT_CMD_ERROR_ADDR_1		
NONE					R		
0h					0h		

Table 14-21275. EMIF_CTLCFG_DENALI_CTL_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PORT_CMD_ERROR_TYPE	R	0h	Type of error and access type that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PORT_CMD_ERROR_ID	R	0h	Source ID of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PORT_CMD_ERROR_ADDR_1	R	0h	Address of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.444 EMIF_CTLCFG_DENALI_CTL_383 Register

1 EMIF_CTLCFG_DENALI_CTL_383 Register (Offset = 5FCh) [reset = 0h]

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Table 14-21276. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 85FCh**

Figure 14-7057. EMIF_CTLCFG_DENALI_CTL_383 Name Register

31	30	29	28	27	26	25	24
RESERVED				TODTH_WR_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TODTL_2CMD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TODTH_RD_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TODTH_WR_F0			
NONE				R/W			
0h				0h			

Table 14-21278. EMIF_CTLCFG_DENALI_CTL_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TODTH_WR_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TODTH_RD_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TODTH_WR_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.445 EMIF_CTLCFG_DENALI_CTL_384 Register

1 EMIF_CTLCFG_DENALI_CTL_384 Register (Offset = 600h) [reset = 0h]

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Table 14-21279. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8600h**

Figure 14-7058. EMIF_CTLCFG_DENALI_CTL_384 Name Register

31	30	29	28	27	26	25	24
RESERVED				TODTH_RD_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TODTH_WR_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TODTL_2CMD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TODTH_RD_F1			
NONE				R/W			
0h				0h			

Table 14-21281. EMIF_CTLCFG_DENALI_CTL_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TODTH_RD_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TODTH_WR_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TODTH_RD_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.446 EMIF_CTLCFG_DENALI_CTL_385 Register

1 EMIF_CTLCFG_DENALI_CTL_385 Register (Offset = 604h) [reset = 0h]

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Table 14-21282. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8604h**

Figure 14-7059. EMIF_CTLCFG_DENALI_CTL_385 Name Register

31	30	29	28	27	26	25	24
RESERVED							EN_ODT_ASSERT_EXCEPT_RD
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							ODT_EN_F2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							ODT_EN_F1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							ODT_EN_F0
NONE							R/W
0h							0h

Table 14-21284. EMIF_CTLCFG_DENALI_CTL_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	EN_ODT_ASSERT_EXCEPT_RD	R/W	0h	Enable controller to assert ODT at all times except during reads. Assumes single ODT pin connected. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=2 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=1 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.447 EMIF_CTLCFG_DENALI_CTL_386 Register

1 EMIF_CTLCFG_DENALI_CTL_386 Register (Offset = 608h) [reset = 0h]

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Table 14-21285. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8608h**

Figure 14-7060. EMIF_CTLCFG_DENALI_CTL_386 Name Register

31	30	29	28	27	26	25	24
RESERVED						ODT_RD_MAP_CS0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED		WR_TO_ODTH_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		WR_TO_ODTH_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		WR_TO_ODTH_F0					
NONE		R/W					
0h		0h					

Table 14-21287. EMIF_CTLCFG_DENALI_CTL_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ODT_RD_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a read occurs. Set bit X to enable termination on csX when a read is performed. CS=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	WR_TO_ODTH_F2	R/W	0h	Defines the delay from a write command to ODT assertion. FC=2 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	WR_TO_ODTH_F1	R/W	0h	Defines the delay from a write command to ODT assertion. FC=1 Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	WR_TO_ODTH_F0	R/W	0h	Defines the delay from a write command to ODT assertion. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.448 EMIF_CTLCFG_DENALI_CTL_387 Register

1 EMIF_CTLCFG_DENALI_CTL_387 Register (Offset = 60Ch) [reset = 0h]

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Table 14-21288. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 860Ch**

Figure 14-7061. EMIF_CTLCFG_DENALI_CTL_387 Name Register

31	30	29	28	27	26	25	24
RESERVED		RD_TO_ODTH_F0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						ODT_WR_MAP_CS1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						ODT_RD_MAP_CS1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						ODT_WR_MAP_CS0	
NONE						R/W	
0h						0h	

Table 14-21290. EMIF_CTLCFG_DENALI_CTL_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	RD_TO_ODTH_F0	R/W	0h	Defines the delay from a read command to ODT assertion. FC=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ODT_WR_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a write occurs. Set bit X to enable termination on csX when a write is performed. CS=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	ODT_RD_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a read occurs. Set bit X to enable termination on csX when a read is performed. CS=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ODT_WR_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a write occurs. Set bit X to enable termination on csX when a write is performed. CS=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.449 EMIF_CTLCFG_DENALI_CTL_388 Register

1 EMIF_CTLCFG_DENALI_CTL_388 Register (Offset = 610h) [reset = 8080000h]

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Table 14-21291. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8610h

Figure 14-7062. EMIF_CTLCFG_DENALI_CTL_388 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RW2MRW_DLY_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">8h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RW2MRW_DLY_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RD_TO_ODTH_F2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RD_TO_ODTH_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-21293. EMIF_CTLCFG_DENALI_CTL_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RW2MRW_DLY_F1	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	RW2MRW_DLY_F0	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=0 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	RD_TO_ODTH_F2	R/W	0h	Defines the delay from a read command to ODT assertion. FC=2 Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	RD_TO_ODTH_F1	R/W	0h	Defines the delay from a read command to ODT assertion. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.450 EMIF_CTLCFG_DENALI_CTL_389 Register

1 EMIF_CTLCFG_DENALI_CTL_389 Register (Offset = 614h) [reset = 1010108h]

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Table 14-21294. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8614h

Figure 14-7063. EMIF_CTLCFG_DENALI_CTL_389 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R2W_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R2R_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RW2MRW_DLY_F2				
NONE			R/W				
0h			8h				

Table 14-21296. EMIF_CTLCFG_DENALI_CTL_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	RW2MRW_DLY_F2	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.451 EMIF_CTLCFG_DENALI_CTL_390 Register

1 EMIF_CTLCFG_DENALI_CTL_390 Register (Offset = 618h) [reset = 1010101h]

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Table 14-21297. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8618h**

Figure 14-7064. EMIF_CTLCFG_DENALI_CTL_390 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R2W_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R2R_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			W2W_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				

Table 14-21299. EMIF_CTLCFG_DENALI_CTL_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.452 EMIF_CTLCFG_DENALI_CTL_391 Register

1 EMIF_CTLCFG_DENALI_CTL_391 Register (Offset = 61Ch) [reset = 1010101h]

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Table 14-21300. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 861Ch

Figure 14-7065. EMIF_CTLCFG_DENALI_CTL_391 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
23	22	21	20	19	18	17	16
RESERVED			R2W_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
15	14	13	12	11	10	9	8
RESERVED			R2R_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
7	6	5	4	3	2	1	0
RESERVED			W2W_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				

Table 14-21302. EMIF_CTLCFG_DENALI_CTL_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.453 EMIF_CTLCFG_DENALI_CTL_392 Register

1 EMIF_CTLCFG_DENALI_CTL_392 Register (Offset = 620h) [reset = 2020201h]

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Table 14-21303. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8620h**

Figure 14-7066. EMIF_CTLCFG_DENALI_CTL_392 Name Register

31	30	29	28	27	26	25	24
RESERVED			R2W_SAMECS_DLY_F2				
NONE			R/W				
0h			2h				
23	22	21	20	19	18	17	16
RESERVED			R2W_SAMECS_DLY_F1				
NONE			R/W				
0h			2h				
15	14	13	12	11	10	9	8
RESERVED			R2W_SAMECS_DLY_F0				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
RESERVED			W2W_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				

Table 14-21305. EMIF_CTLCFG_DENALI_CTL_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	R2W_SAMECS_DLY_F2	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_SAMECS_DLY_F1	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2W_SAMECS_DLY_F0	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.454 EMIF_CTLCFG_DENALI_CTL_393 Register

1 EMIF_CTLCFG_DENALI_CTL_393 Register (Offset = 624h) [reset = 0h]

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Table 14-21306. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8624h**

Figure 14-7067. EMIF_CTLCFG_DENALI_CTL_393 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED			W2W_SAMECS_DLY				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			W2R_SAMECS_DLY				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			R2R_SAMECS_DLY				
NONE			R/W				
0h			0h				

Table 14-21308. EMIF_CTLCFG_DENALI_CTL_393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	W2W_SAMECS_DLY	R/W	0h	Additional delay to insert between two writes to the same chip select. Any value including 0 supported. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	W2R_SAMECS_DLY	R/W	0h	Additional delay to insert between writes and reads to the same chip select. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	R2R_SAMECS_DLY	R/W	0h	Additional delay to insert between two reads to the same chip select. Any value including 0 supported. Reset Source: ctl_amod_g_rst_n

14.6.6.2.455 EMIF_CTLCFG_DENALI_CTL_394 Register

1 EMIF_CTLCFG_DENALI_CTL_394 Register (Offset = 628h) [reset = 0h]

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Table 14-21309. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8628h**

Figure 14-7068. EMIF_CTLCFG_DENALI_CTL_394 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED					TDQSCK_MIN_F1		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED				TDQSCK_MAX_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED					TDQSCK_MIN_F0		
NONE					R/W		
0h					0h		

Table 14-21311. EMIF_CTLCFG_DENALI_CTL_394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK. FC=2 Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	TDQSCK_MIN_F1	R/W	0h	Additional delay needed for tDQSCK. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK. FC=1 Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TDQSCK_MIN_F0	R/W	0h	Additional delay needed for tDQSCK. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.456 EMIF_CTLCFG_DENALI_CTL_395 Register

1 EMIF_CTLCFG_DENALI_CTL_395 Register (Offset = 62Ch) [reset = 0h]

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Table 14-21312. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 862Ch

Figure 14-7069. EMIF_CTLCFG_DENALI_CTL_395 Name Register

31	30	29	28	27	26	25	24
RESERVED					AXI0_R_PRIORITY		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							AXI0_FIXED_PORT_PRIORITY_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							AXI0_ALL_STROBES_USED_ENABLE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TDQSCK_MIN_F2		
NONE					R/W		
0h					0h		

Table 14-21314. EMIF_CTLCFG_DENALI_CTL_395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	AXI0_R_PRIORITY	R/W	0h	Priority of read commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	AXI0_FIXED_PORT_PRIORITY_ENABLE	R/W	0h	Defines the priority control for AXI port 0 as per-port or per-command. Set to 1 for per-port with priority defined through the AXI.0._R_PRIORITY and AXI.0._W_PRIORITY parameters. Clear to 0 for per-command. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AXI0_ALL_STROBES_USED_ENABLE	R/W	0h	Enables use of the AWALLSTRB signal for AXI port 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved

Table 14-21314. EMIF_CTLCFG_DENALI_CTL_395 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TDQSCK_MIN_F2	R/W	0h	Additional delay needed for tDQSCK. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.457 EMIF_CTLCFG_DENALI_CTL_396 Register

1 EMIF_CTLCFG_DENALI_CTL_396 Register (Offset = 630h) [reset = 6000000h]

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Table 14-21315. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8630h**

Figure 14-7070. EMIF_CTLCFG_DENALI_CTL_396 Name Register

31	30	29	28	27	26	25	24
TDFI_PHY_RDLAT_F0							
R/W							
6h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MEM_RST_VALID
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CKE_STATUS	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					AXI0_W_PRIORITY		
NONE					R/W		
0h					0h		

Table 14-21317. EMIF_CTLCFG_DENALI_CTL_396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_PHY_RDLAT_F0	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MEM_RST_VALID	R	0h	Register access to mem_rst_valid signal. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	CKE_STATUS	R	0h	Register access to cke_status signal. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	AXI0_W_PRIORITY	R/W	0h	Priority of write commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low. Reset Source: ctl_amod_g_rst_n

14.6.6.2.458 EMIF_CTLCFG_DENALI_CTL_397 Register

1 EMIF_CTLCFG_DENALI_CTL_397 Register (Offset = 634h) [reset = 0h]

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Table 14-21318. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8634h

Figure 14-7071. EMIF_CTLCFG_DENALI_CTL_397 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			TDFI_CTRLUPD_MAX_F0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_MAX_F0							
R/W							
0h							

Table 14-21320. EMIF_CTLCFG_DENALI_CTL_397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.459 EMIF_CTLCFG_DENALI_CTL_398 Register

1 EMIF_CTLCFG_DENALI_CTL_398 Register (Offset = 638h) [reset = 0h]

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Table 14-21321. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8638h**

Figure 14-7072. EMIF_CTLCFG_DENALI_CTL_398 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							

Table 14-21323. EMIF_CTLCFG_DENALI_CTL_398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.460 EMIF_CTLCFG_DENALI_CTL_399 Register

1 EMIF_CTLCFG_DENALI_CTL_399 Register (Offset = 63Ch) [reset = 0h]

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Table 14-21324. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 863Ch**

Figure 14-7073. EMIF_CTLCFG_DENALI_CTL_399 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							

Table 14-21326. EMIF_CTLCFG_DENALI_CTL_399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.461 EMIF_CTLCFG_DENALI_CTL_400 Register

1 EMIF_CTLCFG_DENALI_CTL_400 Register (Offset = 640h) [reset = 0h]

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Table 14-21327. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8640h**

Figure 14-7074. EMIF_CTLCFG_DENALI_CTL_400 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							

Table 14-21329. EMIF_CTLCFG_DENALI_CTL_400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.462 EMIF_CTLCFG_DENALI_CTL_401 Register

1 EMIF_CTLCFG_DENALI_CTL_401 Register (Offset = 644h) [reset = 0h]

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Table 14-21330. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8644h**

Figure 14-7075. EMIF_CTLCFG_DENALI_CTL_401 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							

Table 14-21332. EMIF_CTLCFG_DENALI_CTL_401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.463 EMIF_CTLCFG_DENALI_CTL_402 Register

1 EMIF_CTLCFG_DENALI_CTL_402 Register (Offset = 648h) [reset = 0h]

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Table 14-21333. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 8648h**

Figure 14-7076. EMIF_CTLCFG_DENALI_CTL_402 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDFI_PHYUPD_RESP_F0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
TDFI_PHYUPD_RESP_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_RESP_F0							
R/W							
0h							

Table 14-21335. EMIF_CTLCFG_DENALI_CTL_402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F0	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.464 EMIF_CTLCFG_DENALI_CTL_403 Register

1 EMIF_CTLCFG_DENALI_CTL_403 Register (Offset = 64Ch) [reset = 0h]

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Table 14-21336. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 864Ch

Figure 14-7077. EMIF_CTLCFG_DENALI_CTL_403 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							

Table 14-21338. EMIF_CTLCFG_DENALI_CTL_403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.465 EMIF_CTLCFG_DENALI_CTL_404 Register

1 EMIF_CTLCFG_DENALI_CTL_404 Register (Offset = 650h) [reset = 2h]

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Table 14-21339. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8650h**

Figure 14-7078. EMIF_CTLCFG_DENALI_CTL_404 Name Register

31	30	29	28	27	26	25	24
TDFI_RDDATA_EN_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_RDCSLAT_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TDFI_PHY_WRDATA_F0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TDFI_CTRL_DELAY_F0			
NONE				R/W			
0h				2h			

Table 14-21341. EMIF_CTLCFG_DENALI_CTL_404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F0	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F0	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=0 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F0	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.466 EMIF_CTLCFG_DENALI_CTL_405 Register

1 EMIF_CTLCFG_DENALI_CTL_405 Register (Offset = 654h) [reset = 6000000h]

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Table 14-21342. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8654h**

Figure 14-7079. EMIF_CTLCFG_DENALI_CTL_405 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TDFI_PHY_RDLAT_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">TDFI_CTRLMSG_RESP_F0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHY_WRLAT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_WRCSLAT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21344. EMIF_CTLCFG_DENALI_CTL_405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_PHY_RDLAT_F1	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=1 Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	TDFI_CTRLMSG_RESP_F0	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F0	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F0	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.467 EMIF_CTLCFG_DENALI_CTL_406 Register

1 EMIF_CTLCFG_DENALI_CTL_406 Register (Offset = 658h) [reset = 0h]

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Table 14-21345. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8658h**

Figure 14-7080. EMIF_CTLCFG_DENALI_CTL_406 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TDFI_CTRLUPD_MAX_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_CTRLUPD_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_CTRLUPD_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21347. EMIF_CTLCFG_DENALI_CTL_406 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.468 EMIF_CTLCFG_DENALI_CTL_407 Register

1 EMIF_CTLCFG_DENALI_CTL_407 Register (Offset = 65Ch) [reset = 0h]

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Table 14-21348. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 865Ch**

Figure 14-7081. EMIF_CTLCFG_DENALI_CTL_407 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							

Table 14-21350. EMIF_CTLCFG_DENALI_CTL_407 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.469 EMIF_CTLCFG_DENALI_CTL_408 Register

1 EMIF_CTLCFG_DENALI_CTL_408 Register (Offset = 660h) [reset = 0h]

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Table 14-21351. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8660h**

Figure 14-7082. EMIF_CTLCFG_DENALI_CTL_408 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							

Table 14-21353. EMIF_CTLCFG_DENALI_CTL_408 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.470 EMIF_CTLCFG_DENALI_CTL_409 Register

1 EMIF_CTLCFG_DENALI_CTL_409 Register (Offset = 664h) [reset = 0h]

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Table 14-21354. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8664h**

Figure 14-7083. EMIF_CTLCFG_DENALI_CTL_409 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							

Table 14-21356. EMIF_CTLCFG_DENALI_CTL_409 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.471 EMIF_CTLCFG_DENALI_CTL_410 Register

1 EMIF_CTLCFG_DENALI_CTL_410 Register (Offset = 668h) [reset = 0h]

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Table 14-21357. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8668h**

Figure 14-7084. EMIF_CTLCFG_DENALI_CTL_410 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							

Table 14-21359. EMIF_CTLCFG_DENALI_CTL_410 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.472 EMIF_CTLCFG_DENALI_CTL_411 Register

1 EMIF_CTLCFG_DENALI_CTL_411 Register (Offset = 66Ch) [reset = 0h]

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Table 14-21360. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 866Ch**

Figure 14-7085. EMIF_CTLCFG_DENALI_CTL_411 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDFI_PHYUPD_RESP_F1						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
TDFI_PHYUPD_RESP_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_RESP_F1							
R/W							
0h							

Table 14-21362. EMIF_CTLCFG_DENALI_CTL_411 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F1	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.473 EMIF_CTLCFG_DENALI_CTL_412 Register

1 EMIF_CTLCFG_DENALI_CTL_412 Register (Offset = 670h) [reset = 0h]

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Table 14-21363. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8670h**

Figure 14-7086. EMIF_CTLCFG_DENALI_CTL_412 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							

Table 14-21365. EMIF_CTLCFG_DENALI_CTL_412 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.474 EMIF_CTLCFG_DENALI_CTL_413 Register

1 EMIF_CTLCFG_DENALI_CTL_413 Register (Offset = 674h) [reset = 2h]

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Table 14-21366. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8674h**

Figure 14-7087. EMIF_CTLCFG_DENALI_CTL_413 Name Register

31	30	29	28	27	26	25	24
TDFI_RDDATA_EN_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_RDCSLAT_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TDFI_PHY_WRDATA_F1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TDFI_CTRL_DELAY_F1			
NONE				R/W			
0h				2h			

Table 14-21368. EMIF_CTLCFG_DENALI_CTL_413 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F1	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F1	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=1 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F1	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.475 EMIF_CTLCFG_DENALI_CTL_414 Register

1 EMIF_CTLCFG_DENALI_CTL_414 Register (Offset = 678h) [reset = 6000000h]

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Table 14-21369. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8678h**

Figure 14-7088. EMIF_CTLCFG_DENALI_CTL_414 Name Register

31	30	29	28	27	26	25	24
TDFI_PHY_RDLAT_F2							
R/W							
6h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TDFI_CTRLMSG_RESP_F1						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHY_WRLAT_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_WRCSLAT_F1							
R/W							
0h							

Table 14-21371. EMIF_CTLCFG_DENALI_CTL_414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_PHY_RDLAT_F2	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=2 Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	TDFI_CTRLMSG_RESP_F1	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F1	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F1	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.476 EMIF_CTLCFG_DENALI_CTL_415 Register

1 EMIF_CTLCFG_DENALI_CTL_415 Register (Offset = 67Ch) [reset = 0h]

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Table 14-21372. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 867Ch**

Figure 14-7089. EMIF_CTLCFG_DENALI_CTL_415 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21374. EMIF_CTLCFG_DENALI_CTL_415 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.477 EMIF_CTLCFG_DENALI_CTL_416 Register

1 EMIF_CTLCFG_DENALI_CTL_416 Register (Offset = 680h) [reset = 0h]

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Table 14-21375. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8680h**

Figure 14-7090. EMIF_CTLCFG_DENALI_CTL_416 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							

Table 14-21377. EMIF_CTLCFG_DENALI_CTL_416 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.478 EMIF_CTLCFG_DENALI_CTL_417 Register

1 EMIF_CTLCFG_DENALI_CTL_417 Register (Offset = 684h) [reset = 0h]

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Table 14-21378. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 8684h

Figure 14-7091. EMIF_CTLCFG_DENALI_CTL_417 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							

Table 14-21380. EMIF_CTLCFG_DENALI_CTL_417 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.479 EMIF_CTLCFG_DENALI_CTL_418 Register

1 EMIF_CTLCFG_DENALI_CTL_418 Register (Offset = 688h) [reset = 0h]

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Table 14-21381. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8688h**

Figure 14-7092. EMIF_CTLCFG_DENALI_CTL_418 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							

Table 14-21383. EMIF_CTLCFG_DENALI_CTL_418 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.480 EMIF_CTLCFG_DENALI_CTL_419 Register

1 EMIF_CTLCFG_DENALI_CTL_419 Register (Offset = 68Ch) [reset = 0h]

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Table 14-21384. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 868Ch**

Figure 14-7093. EMIF_CTLCFG_DENALI_CTL_419 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							

Table 14-21386. EMIF_CTLCFG_DENALI_CTL_419 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.481 EMIF_CTLCFG_DENALI_CTL_420 Register

1 EMIF_CTLCFG_DENALI_CTL_420 Register (Offset = 690h) [reset = 0h]

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Table 14-21387. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8690h**

Figure 14-7094. EMIF_CTLCFG_DENALI_CTL_420 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">TDFI_PHYUPD_RESP_F2</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHYUPD_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_PHYUPD_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21389. EMIF_CTLCFG_DENALI_CTL_420 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F2	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.482 EMIF_CTLCFG_DENALI_CTL_421 Register

1 EMIF_CTLCFG_DENALI_CTL_421 Register (Offset = 694h) [reset = 0h]

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Table 14-21390. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8694h**

Figure 14-7095. EMIF_CTLCFG_DENALI_CTL_421 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							

Table 14-21392. EMIF_CTLCFG_DENALI_CTL_421 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.483 EMIF_CTLCFG_DENALI_CTL_422 Register

1 EMIF_CTLCFG_DENALI_CTL_422 Register (Offset = 698h) [reset = 2h]

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Table 14-21393. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 8698h**

Figure 14-7096. EMIF_CTLCFG_DENALI_CTL_422 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TDFI_RDDATA_EN_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TDFI_RDCSLAT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TDFI_PHY_WRDATA_F2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TDFI_CTRL_DELAY_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-21395. EMIF_CTLCFG_DENALI_CTL_422 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F2	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F2	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=2 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F2	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.484 EMIF_CTLCFG_DENALI_CTL_423 Register

1 EMIF_CTLCFG_DENALI_CTL_423 Register (Offset = 69Ch) [reset = 0h]

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Table 14-21396. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 869Ch**

Figure 14-7097. EMIF_CTLCFG_DENALI_CTL_423 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">TDFI_CTRLMSG_RESP_F2</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHY_WRLAT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_WRCSLAT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21398. EMIF_CTLCFG_DENALI_CTL_423 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TDFI_CTRLMSG_RESP_F2	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F2	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F2	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.485 EMIF_CTLCFG_DENALI_CTL_424 Register

1 EMIF_CTLCFG_DENALI_CTL_424 Register (Offset = 6A0h) [reset = 0h]

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Table 14-21399. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86A0h**

Figure 14-7098. EMIF_CTLCFG_DENALI_CTL_424 Name Register

31	30	29	28	27	26	25	24
RESERVED	UPDATE_ERROR_STATUS						
NONE	R						
0h	0h						
23	22	21	20	19	18	17	16
DLL_RST_ADJ_DLY							
R/W							
0h							
15	14	13	12	11	10	9	8
DLL_RST_DELAY							
R/W							
0h							
7	6	5	4	3	2	1	0
DLL_RST_DELAY							
R/W							
0h							

Table 14-21401. EMIF_CTLCFG_DENALI_CTL_424 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI MC-initiated or PHY-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting controller delay in DLL until the DLL reset signal dll_rst_n may be asserted. If this signal is not being used by the PHY, this parameter may be ignored. Reset Source: ctl_amod_g_rst_n
15:0	DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held. If this signal is not being used by the PHY, this parameter may be ignored. Reset Source: ctl_amod_g_rst_n

14.6.6.2.486 EMIF_CTLCFG_DENALI_CTL_425 Register

1 EMIF_CTLCFG_DENALI_CTL_425 Register (Offset = 6A4h) [reset = 0h]

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Table 14-21402. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86A4h**

Figure 14-7099. EMIF_CTLCFG_DENALI_CTL_425 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDFI_DRAM_CLK_DISABLE			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_CTRLUPD_MIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_CTRLUPD_MIN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						DRAM_CLK_DISABLE	
NONE						R/W	
0h						0h	

Table 14-21404. EMIF_CTLCFG_DENALI_CTL_425 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDFI_DRAM_CLK_DISABLE	R/W	0h	Defines the DFI tDRAM_CLK_DISABLE timing parameter [in DFI clocks], the delay between a dfi_dram_clock_disable assertion and the memory clock disable. Reset Source: ctl_amod_g_rst_n
23:8	TDFI_CTRLUPD_MIN	R/W	0h	Defines the DFI tCTRLUPD_MIN timing parameter [in DFI clocks], the minimum cycles that dfi_ctrlupd_req must be asserted. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	DRAM_CLK_DISABLE	R/W	0h	Set value for the dfi_dram_clk_disable signal. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.487 EMIF_CTLCFG_DENALI_CTL_426 Register

1 EMIF_CTLCFG_DENALI_CTL_426 Register (Offset = 6A8h) [reset = 0h]

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Table 14-21405. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86A8h**

Figure 14-7100. EMIF_CTLCFG_DENALI_CTL_426 Name Register

31	30	29	28	27	26	25	24
RESERVED							DISABLE_MEMORY_MASKED_WRITE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_WRDATA_DELAY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TDFI_PARIN_LAT		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TDFI_DRAM_CLK_ENABLE			
NONE				R/W			
0h				0h			

Table 14-21407. EMIF_CTLCFG_DENALI_CTL_426 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DISABLE_MEMORY_MASKED_WRITE	R/W	0h	Restricts the controller from masked write commands. Set to 1 to not issue these commands. Only used if connected to an LPDDR4 device. Reset Source: ctl_amod_g_rst_n
23:16	TDFI_WRDATA_DELAY	R/W	0h	Defines the tWRDATA_DELAY timing parameter [in DFI PHY clocks], the maximum cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PARIN_LAT	R/W	0h	Defines the DFI tPARIN_LAT timing parameter [in DFI PHY clocks], the maximum cycles between a DFI command and a dfi_parity_in signal assertion. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_DRAM_CLK_ENABLE	R/W	0h	Defines the DFI tDRAM_CLK_ENABLE timing parameter [in DFI clocks], the delay between a dfi_dram_clk_disable de-assertion and the memory clock enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.488 EMIF_CTLCFG_DENALI_CTL_427 Register

1 EMIF_CTLCFG_DENALI_CTL_427 Register (Offset = 6ACh) [reset = 0h]

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Table 14-21408. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 86ACh**

Figure 14-7101. EMIF_CTLCFG_DENALI_CTL_427 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PRE_2TICK_COUNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">BANK_ACTIVATE_2TICK_COUNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">STRATEGY_2TICK_COUNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>MULTI_CHANNEL_ZQ_CAL_MASTER</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21410. EMIF_CTLCFG_DENALI_CTL_427 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PRE_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	BANK_ACTIVATE_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	STRATEGY_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	MULTI_CHANNEL_ZQ_CAL_MASTER	R/W	0h	In a two controller scenario, defines if this controller will issue ZQ calibration start commands when neither controller is in a low power mode. Set to 1 to define this controller as the controller that issues ZQ calibration start commands or clear to 0 to define this controller as the target. This parameter should only be programmed once during initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.489 EMIF_CTLCFG_DENALI_CTL_428 Register

1 EMIF_CTLCFG_DENALI_CTL_428 Register (Offset = 6B0h) [reset = 10101h]

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Table 14-21411. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86B0h**

Figure 14-7102. EMIF_CTLCFG_DENALI_CTL_428 Name Register

31	30	29	28	27	26	25	24
RESERVED				TMP_2X4_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PRE_4TICK_COUNT		
NONE					R/W		
0h					1h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					BANK_ACTIVATE_4TICK_COUNT		
NONE					R/W		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					STRATEGY_4TICK_COUNT		
NONE					R/W		
0h					1h		

Table 14-21413. EMIF_CTLCFG_DENALI_CTL_428 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TMP_2X4_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PRE_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	BANK_ACTIVATE_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	STRATEGY_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.490 EMIF_CTLCFG_DENALI_CTL_429 Register

1 EMIF_CTLCFG_DENALI_CTL_429 Register (Offset = 6B4h) [reset = 10001h]

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Table 14-21414. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86B4h**

Figure 14-7103. EMIF_CTLCFG_DENALI_CTL_429 Name Register

31	30	29	28	27	26	25	24
RESERVED				ODT_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				TMP_NXN_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED				TMP_NXN_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				TMP_2X4_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			

Table 14-21416. EMIF_CTLCFG_DENALI_CTL_429 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	ODT_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TMP_NXN_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TMP_NXN_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TMP_2X4_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.491 EMIF_CTLCFG_DENALI_CTL_430 Register

1 EMIF_CTLCFG_DENALI_CTL_430 Register (Offset = 6B8h) [reset = 1000101h]

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Table 14-21417. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86B8h**

Figure 14-7104. EMIF_CTLCFG_DENALI_CTL_430 Name Register

31	30	29	28	27	26	25	24
RESERVED				TRP_TICK_PLUS_ADJ			
NONE				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TRAS_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TRAS_TICK_PLUS_ADJ			
NONE				R/W			
0h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ODT_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			

Table 14-21419. EMIF_CTLCFG_DENALI_CTL_430 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TRP_TICK_PLUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TRAS_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TRAS_TICK_PLUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	ODT_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.492 EMIF_CTLCFG_DENALI_CTL_431 Register

1 EMIF_CTLCFG_DENALI_CTL_431 Register (Offset = 6BCh) [reset = 2000200h]

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Table 14-21420. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86BCh**

Figure 14-7105. EMIF_CTLCFG_DENALI_CTL_431 Name Register

31	30	29	28	27	26	25	24
RESERVED				TMP_4X2_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TWR_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TWR_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRP_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-21422. EMIF_CTLCFG_DENALI_CTL_431 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TMP_4X2_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TWR_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TWR_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TRP_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.493 EMIF_CTLCFG_DENALI_CTL_432 Register

1 EMIF_CTLCFG_DENALI_CTL_432 Register (Offset = 6C0h) [reset = 2010000h]

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Table 14-21423. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86C0h**

Figure 14-7106. EMIF_CTLCFG_DENALI_CTL_432 Name Register

31	30	29	28	27	26	25	24
RESERVED				RL_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				TRFC_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED				TRFC_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				TMP_4X2_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-21425. EMIF_CTLCFG_DENALI_CTL_432 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	RL_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TRFC_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TRFC_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TMP_4X2_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.494 EMIF_CTLCFG_DENALI_CTL_433 Register

1 EMIF_CTLCFG_DENALI_CTL_433 Register (Offset = 6C4h) [reset = 28000200h]

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Table 14-21426. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 86C4h**

Figure 14-7107. EMIF_CTLCFG_DENALI_CTL_433 Name Register

31	30	29	28	27	26	25	24
NWR_F0							
R/W							
28h							
23	22	21	20	19	18	17	16
RESERVED				WL_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				WL_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				RL_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-21428. EMIF_CTLCFG_DENALI_CTL_433 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NWR_F0	R/W	28h	DRAM NWR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	WL_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	WL_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	RL_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.6.6.2.495 EMIF_CTLCFG_DENALI_CTL_434 Register

1 EMIF_CTLCFG_DENALI_CTL_434 Register (Offset = 6C8h) [reset = 2828h]

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Table 14-21429. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 86C8h

Figure 14-7108. EMIF_CTLCFG_DENALI_CTL_434 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NWR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">28h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NWR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">28h</td></tr>
</table>

Table 14-21431. EMIF_CTLCFG_DENALI_CTL_434 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	NWR_F2	R/W	28h	DRAM NWR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	NWR_F1	R/W	28h	DRAM NWR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.496 EMIF_CTLCFG_DENALI_PI_0 Register

1 EMIF_CTLCFG_DENALI_PI_0 Register (Offset = 2000h) [reset = 0h]

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Table 14-21432. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A000h

Figure 14-7109. EMIF_CTLCFG_DENALI_PI_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_DRAM_CLASS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_START</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21434. EMIF_CTLCFG_DENALI_PI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PI_DRAM_CLASS	R/W	0h	Defines the memory class for the PI. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_START	R/W	0h	Initiate command processing in the PI. Set to 1 to initiate. Reset Source: ctl_amod_g_rst_n

14.6.6.2.497 EMIF_CTLCFG_DENALI_PI_1 Register

1 EMIF_CTLCFG_DENALI_PI_1 Register (Offset = 2004h) [reset = 30BD08BAh]

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Table 14-21435. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A004h**

Figure 14-7110. EMIF_CTLCFG_DENALI_PI_1 Name Register

31	30	29	28	27	26	25	24
PI_VERSION_0							
R							
30BD08BAh							
23	22	21	20	19	18	17	16
PI_VERSION_0							
R							
30BD08BAh							
15	14	13	12	11	10	9	8
PI_VERSION_0							
R							
30BD08BAh							
7	6	5	4	3	2	1	0
PI_VERSION_0							
R							
30BD08BAh							

Table 14-21437. EMIF_CTLCFG_DENALI_PI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_VERSION_0	R	30BD08BAh	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.498 EMIF_CTLCFG_DENALI_PI_2 Register

1 EMIF_CTLCFG_DENALI_PI_2 Register (Offset = 2008h) [reset = 453CB5Ch]

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Table 14-21438. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A008h**

Figure 14-7111. EMIF_CTLCFG_DENALI_PI_2 Name Register

31	30	29	28	27	26	25	24
PI_VERSION_1							
R							
453CB5Ch							
23	22	21	20	19	18	17	16
PI_VERSION_1							
R							
453CB5Ch							
15	14	13	12	11	10	9	8
PI_VERSION_1							
R							
453CB5Ch							
7	6	5	4	3	2	1	0
PI_VERSION_1							
R							
453CB5Ch							

Table 14-21440. EMIF_CTLCFG_DENALI_PI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_VERSION_1	R	453CB5Ch	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.499 EMIF_CTLCFG_DENALI_PI_3 Register

1 EMIF_CTLCFG_DENALI_PI_3 Register (Offset = 200Ch) [reset = 11387h]

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Table 14-21441. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A00Ch

Figure 14-7112. EMIF_CTLCFG_DENALI_PI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NORMAL_LVL_SEQ
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RELEASE_DFI
NONE							R
0h							1h
15	14	13	12	11	10	9	8
PI_ID							
R							
1387h							
7	6	5	4	3	2	1	0
PI_ID							
R							
1387h							

Table 14-21443. EMIF_CTLCFG_DENALI_PI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NORMAL_LVL_SEQ	R/W	0h	Enable the PI to finish all the pending leveling before releasing the DFI bus. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RELEASE_DFI	R	1h	This is a status whether PI has release DFI. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:0	PI_ID	R	1387h	Holds the PI ID number. This is a Cadence DDR PHY IP identifier. It is set to 0x1387. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.500 EMIF_CTLCFG_DENALI_PI_4 Register

1 EMIF_CTLCFG_DENALI_PI_4 Register (Offset = 2010h) [reset = 0h]

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Table 14-21444. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A010h**

Figure 14-7113. EMIF_CTLCFG_DENALI_PI_4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TCMD_GAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TCMD_GAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_NOTCARE_PHYUPD</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_INIT_LVL_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21446. EMIF_CTLCFG_DENALI_PI_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TCMD_GAP	R/W	0h	Specifies the minimum gap in DFI clocks between two commands. Used to guard the timing from the last command of MC and the first command of PI when MC hand over the control of DFI to PI. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_NOTCARE_PHYUPD	R/W	0h	Allow the PI to issue a controller request to the controller if a phyupd_req from the PHY has been detected.bit[1] represents supports in normal state;bit[0] represents supports in initialization state. Set to 1 to issue the controller request. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_INIT_LVL_EN	R/W	0h	Enables the initial leveling sequence after PI initialization procedure. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.501 EMIF_CTLCFG_DENALI_PI_5 Register

1 EMIF_CTLCFG_DENALI_PI_5 Register (Offset = 2014h) [reset = 64h]

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Table 14-21447. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A014h**

Figure 14-7114. EMIF_CTLCFG_DENALI_PI_5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_DFI_PHYMSTR_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_DFI_VERSION</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_TRAIN_ALL_FREQ_REQ</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_RESERVED0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">64h</td></tr>
</table>

Table 14-21449. EMIF_CTLCFG_DENALI_PI_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_DFI_PHYMSTR_TYPE	R/W	0h	DFI Controller Request Type used for dfi 4.1 verision: This signal indicates the required state of DRAM when PHY becomes the controller. Each memory rank uses one bit. 1'b0: IDLE. The MC should close all the pages. 1'b1: IDLE or Self Refresh. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DFI_VERSION	R/W	0h	Define the DFI controller version, set 1 for DFI4.1, set 0 for DFI4.0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_TRAIN_ALL_FREQ_REQ	W	0h	Triggers training for all supported frequencies in PI_FREQ_MAP. Applies to LPDDR4 devices onlyh. Set to 1 to trigger. Only applicable after memory initialization has been completed. Can be used to train new frequencies that were not available at initialization time. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PI_RESERVED0	R/W	64h	Reserved

14.6.6.2.502 EMIF_CTLCFG_DENALI_PI_6 Register

1 EMIF_CTLCFG_DENALI_PI_6 Register (Offset = 2018h) [reset = 0h]

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Table 14-21450. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A018h

Figure 14-7115. EMIF_CTLCFG_DENALI_PI_6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_DFI_PHYMSTR_STATE_SEL_R
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_DFI_PHYMSTR_CS_STATE_R
NONE							R/W
0h							0h

Table 14-21452. EMIF_CTLCFG_DENALI_PI_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_DFI_PHYMSTR_STATE_SEL_R	R/W	0h	DFI PHY Controller State Select: Indication from the PHY to the MC whether the requested memory state is IDLE or Self refresh. 'b0: indicates that the corresponding CS must be put into the IDLE state. 'b1: indicates that the corresponding CS must be put into the Self refresh state. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DFI_PHYMSTR_CS_STATE_R	R/W	0h	This signal indicates the state of the DRAM when the PHY becomes the controller. 'b0: The PHY specifies the required state, using the dfi_phymstr_state_sel signal. 'b1: is reserved. Reset Source: ctl_amod_g_rst_n

14.6.6.2.503 EMIF_CTLCFG_DENALI_PI_7 Register

1 EMIF_CTLCFG_DENALI_PI_7 Register (Offset = 201Ch) [reset = 0h]

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Table 14-21453. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A01Ch**

Figure 14-7116. EMIF_CTLCFG_DENALI_PI_7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TDFI_PHYMSTR_MAX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_PHYMSTR_MAX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_PHYMSTR_MAX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_PHYMSTR_MAX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21455. EMIF_CTLCFG_DENALI_PI_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_PHYMSTR_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phymstr_req signal is asserted and the dfi_phymstr_ack signal is asserted. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.504 EMIF_CTLCFG_DENALI_PI_8 Register

1 EMIF_CTLCFG_DENALI_PI_8 Register (Offset = 2020h) [reset = 0h]

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Table 14-21456. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A020h**

Figure 14-7117. EMIF_CTLCFG_DENALI_PI_8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TDFI_PHYMSTR_RESP			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
PI_TDFI_PHYMSTR_RESP							
R							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_PHYMSTR_RESP							
R							
0h							

Table 14-21458. EMIF_CTLCFG_DENALI_PI_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TDFI_PHYMSTR_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phymstr_req signal assertion and a dfi_phymstr_ack signal assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.505 EMIF_CTLCFG_DENALI_PI_9 Register

1 EMIF_CTLCFG_DENALI_PI_9 Register (Offset = 2024h) [reset = 0h]

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Table 14-21459. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A024h**

Figure 14-7118. EMIF_CTLCFG_DENALI_PI_9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21461. EMIF_CTLCFG_DENALI_PI_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TDFI_PHYUPD_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phyupd_req signal assertion and a dfi_phyupd_ack signal assertion. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.506 EMIF_CTLCFG_DENALI_PI_10 Register

1 EMIF_CTLCFG_DENALI_PI_10 Register (Offset = 2028h) [reset = 0h]

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Table 14-21462. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A028h**

Figure 14-7119. EMIF_CTLCFG_DENALI_PI_10 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_PHYUPD_MAX							
R							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_PHYUPD_MAX							
R							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_PHYUPD_MAX							
R							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_PHYUPD_MAX							
R							
0h							

Table 14-21464. EMIF_CTLCFG_DENALI_PI_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_PHYUPD_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phyupd_req signal is asserted and the dfi_phy_ack signal is asserted. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.507 EMIF_CTLCFG_DENALI_PI_11 Register

1 EMIF_CTLCFG_DENALI_PI_11 Register (Offset = 202Ch) [reset = 0h]

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Table 14-21465. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A02Ch

Figure 14-7120. EMIF_CTLCFG_DENALI_PI_11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_INIT_DFS_CALVL_ONLY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED			PI_INIT_WORK_FREQ				
NONE			R/W				
0h			0h				

Table 14-21467. EMIF_CTLCFG_DENALI_PI_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_INIT_DFS_CALVL_ONLY	R/W	0h	Enables frequency training for CA leveling only. Other trainings are not performed. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_INIT_WORK_FREQ	R/W	0h	Indicates the initial work frequency after initialization and initial leveling sequence. Reset Source: ctl_amod_g_rst_n

14.6.6.2.508 EMIF_CTLCFG_DENALI_PI_12 Register

1 EMIF_CTLCFG_DENALI_PI_12 Register (Offset = 2030h) [reset = 0h]

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Table 14-21468. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A030h**

Figure 14-7121. EMIF_CTLCFG_DENALI_PI_12 Name Register

31	30	29	28	27	26	25	24
PI_FREQ_MAP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_FREQ_MAP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_FREQ_MAP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_FREQ_MAP							
R/W							
0h							

Table 14-21470. EMIF_CTLCFG_DENALI_PI_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_FREQ_MAP	R/W	0h	Frequency map for supported working frequencies. Each bit represents one supported frequency. Reset Source: ctl_amod_g_rst_n

14.6.6.2.509 EMIF_CTLCFG_DENALI_PI_13 Register

1 EMIF_CTLCFG_DENALI_PI_13 Register (Offset = 2034h) [reset = F0001h]

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Table 14-21471. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A034h**

Figure 14-7122. EMIF_CTLCFG_DENALI_PI_13 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_CS_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PI_CS_MAP			
NONE				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SW_RST_N
NONE							R/W
0h							1h

Table 14-21473. EMIF_CTLCFG_DENALI_PI_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_CS_SEL	R/W	0h	Defines which chip selects are active in swlvl, 0 for binary, 1 for one-hot. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CS_MAP	R/W	Fh	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED1	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_SW_RST_N	R/W	1h	User request to reset the whole PI except the parameter modules. Set 0 to reset, set to 1 to release. Reset Source: ctl_amod_g_rst_n

14.6.6.2.510 EMIF_CTLCFG_DENALI_PI_14 Register

1 EMIF_CTLCFG_DENALI_PI_14 Register (Offset = 2038h) [reset = 0h]

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Table 14-21474. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A038h**

Figure 14-7123. EMIF_CTLCFG_DENALI_PI_14 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TMRR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PI_SRX_LVL_TARGET_CS_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PI_RANK_NUM_PER_CKE				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED				PI_CS_MASK			
NONE				R/W			
0h				0h			

Table 14-21476. EMIF_CTLCFG_DENALI_PI_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TMRR	R/W	0h	DRAM tMRR value in memory clock cycles. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SRX_LVL_TARGET_CS_EN	R/W	0h	Defines self refresh exit trigger target rank/ranks training or all ranks training. 1: The rank/ranks exit from self refresh will trigger the corresponding rank/ranks training. Note: If multiple ranks exit from self refresh, current design only support the multiple ranks srx command issues at the same time. 0: Any rank/ranks exit from self refresh will trigger all ranks training Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RANK_NUM_PER_CKE	R/W	0h	Defines the number of chip selects share one cke Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CS_MASK	R/W	0h	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n

14.6.6.2.511 EMIF_CTLCFG_DENALI_PI_15 Register

1 EMIF_CTLCFG_DENALI_PI_15 Register (Offset = 203Ch) [reset = 0h]

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Table 14-21477. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A03Ch

Figure 14-7124. EMIF_CTLCFG_DENALI_PI_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_MCAREF_FORWARD_ONLY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED					PI_VRCG_EN		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				PI_TMPRR			
NONE				R/W			
0h				0h			

Table 14-21479. EMIF_CTLCFG_DENALI_PI_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED2	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_MCAREF_FORWARD_ONLY	R/W	0h	Controls the generation of AREF from the PI module or forward the MC received value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_VRCG_EN	R/W	0h	Whether enable VRCG mode in two cases: bit0 - when DFS. bit1-when setting DQ Vref. bit2-when setting CBT. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_TMPRR	R/W	0h	DRAM tMPRR value in memory clock cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.512 EMIF_CTLCFG_DENALI_PI_16 Register

1 EMIF_CTLCFG_DENALI_PI_16 Register (Offset = 2040h) [reset = 0h]

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Table 14-21480. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A040h**

Figure 14-7125. EMIF_CTLCFG_DENALI_PI_16 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_ON_DFIBUS
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_INTERVAL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TREF_INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TREF_INTERVAL							
R/W							
0h							

Table 14-21482. EMIF_CTLCFG_DENALI_PI_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_ON_DFIBUS	R	0h	Monitors the state of the PI controlling the DFI bus. 1 means PI is in control. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects. Reset Source: ctl_amod_g_rst_n

14.6.6.2.513 EMIF_CTLCFG_DENALI_PI_17 Register

1 EMIF_CTLCFG_DENALI_PI_17 Register (Offset = 2044h) [reset = 0h]

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Table 14-21483. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A044h**

Figure 14-7126. EMIF_CTLCFG_DENALI_PI_17 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SW_WRLVL_RESP_0
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_OP_DONE
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_LOAD
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_DATA_RETENTION
NONE							R
0h							0h

Table 14-21485. EMIF_CTLCFG_DENALI_PI_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SW_WRLVL_RESP_0	R	0h	Write leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_OP_DONE	R	0h	Reports the status of the software leveling operation. Value of 1 indicates operation complete. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_LOAD	W	0h	User request to load delays and execute software leveling. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DATA_RETENTION	R	0h	Monitors the readiness for the PHY to be put into data retention mode after pi_sref_entry req parameter has been written. 1 means ready for data retention. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.514 EMIF_CTLCFG_DENALI_PI_18 Register

1 EMIF_CTLCFG_DENALI_PI_18 Register (Offset = 2048h) [reset = 0h]

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Table 14-21486. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A048h

Figure 14-7127. EMIF_CTLCFG_DENALI_PI_18 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_SW_RDLVL_RESP_0	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED							PI_SW_WRLVL_RESP_3
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SW_WRLVL_RESP_2
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SW_WRLVL_RESP_1
NONE							R
0h							0h

Table 14-21488. EMIF_CTLCFG_DENALI_PI_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_SW_RDLVL_RESP_0	R	0h	Read leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SW_WRLVL_RESP_3	R	0h	Write leveling response for data slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SW_WRLVL_RESP_2	R	0h	Write leveling response for data slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SW_WRLVL_RESP_1	R	0h	Write leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.515 EMIF_CTLCFG_DENALI_PI_19 Register

1 EMIF_CTLCFG_DENALI_PI_19 Register (Offset = 204Ch) [reset = 0h]

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Table 14-21489. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A04Ch

Figure 14-7128. EMIF_CTLCFG_DENALI_PI_19 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_SW_CALVL_RESP_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_SW_RDLVL_RESP_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_SW_RDLVL_RESP_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_SW_RDLVL_RESP_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-21491. EMIF_CTLCFG_DENALI_PI_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_SW_CALVL_RESP_0	R	0h	CA leveling response for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_RDLVL_RESP_3	R	0h	Read leveling response for data slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_SW_RDLVL_RESP_2	R	0h	Read leveling response for data slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_SW_RDLVL_RESP_1	R	0h	Read leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.516 EMIF_CTLCFG_DENALI_PI_20 Register

1 EMIF_CTLCFG_DENALI_PI_20 Register (Offset = 2050h) [reset = 0h]

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Table 14-21492. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A050h**

Figure 14-7129. EMIF_CTLCFG_DENALI_PI_20 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_0
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_EXIT
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_START
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					PI_SW_LEVELING_MODE		
NONE					R/W		
0h					0h		

Table 14-21494. EMIF_CTLCFG_DENALI_PI_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_0	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_EXIT	W	0h	User request to exit software leveling. Set to 1 to exit. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_START	W	0h	User request to initiate software leveling of type in the SW_LEVELING_MODE parameter. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_SW_LEVELING_MODE	R/W	0h	Defines the leveling operation for software leveling. Set to 'b111 for DDR4 VREF training, set to b001 for write leveling, set to b010 for read data eye training, or set to b011 for read gate training, set to b100 for ca training, set to b101 for wdq training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.517 EMIF_CTLCFG_DENALI_PI_21 Register

1 EMIF_CTLCFG_DENALI_PI_21 Register (Offset = 2054h) [reset = 0h]

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Table 14-21495. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A054h

Figure 14-7130. EMIF_CTLCFG_DENALI_PI_21 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_1
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_0	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_0
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_0
NONE							W
0h							0h

Table 14-21497. EMIF_CTLCFG_DENALI_PI_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_1	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_0	R	0h	Leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_0	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_0	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.518 EMIF_CTLCFG_DENALI_PI_22 Register

1 EMIF_CTLCFG_DENALI_PI_22 Register (Offset = 2058h) [reset = 0h]

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Table 14-21498. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A058h**

Figure 14-7131. EMIF_CTLCFG_DENALI_PI_22 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_2
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_1	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_1
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_1
NONE							W
0h							0h

Table 14-21500. EMIF_CTLCFG_DENALI_PI_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_2	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_1	R	0h	Leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_1	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_1	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.519 EMIF_CTLCFG_DENALI_PI_23 Register

1 EMIF_CTLCFG_DENALI_PI_23 Register (Offset = 205Ch) [reset = 0h]

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Table 14-21501. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A05Ch

Figure 14-7132. EMIF_CTLCFG_DENALI_PI_23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SWLVL_WR_SLICE_3</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_SW_WDQLVL_RESP_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SWLVL_VREF_UPDATE_SLICE_2</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SWLVL_RD_SLICE_2</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21503. EMIF_CTLCFG_DENALI_PI_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_3	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_2	R	0h	Leveling response for data slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_2	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_2	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.520 EMIF_CTLCFG_DENALI_PI_24 Register

1 EMIF_CTLCFG_DENALI_PI_24 Register (Offset = 2060h) [reset = 0h]

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Table 14-21504. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A060h**

Figure 14-7133. EMIF_CTLCFG_DENALI_PI_24 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_SM2_START
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_SW_WDQLVL_RESP_3	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_3
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_SWLVL_RD_SLICE_3
NONE							W
0h							0h

Table 14-21506. EMIF_CTLCFG_DENALI_PI_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_SM2_START	W	0h	SW leveling start command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_3	R	0h	Leveling response for data slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_3	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_3	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.521 EMIF_CTLCFG_DENALI_PI_25 Register

1 EMIF_CTLCFG_DENALI_PI_25 Register (Offset = 2064h) [reset = 0h]

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Table 14-21507. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A064h**

Figure 14-7134. EMIF_CTLCFG_DENALI_PI_25 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_DFS_PERIOD_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SEQUENTIAL_LVL_REQ
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_SM2_RD
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_SM2_WR
NONE							W
0h							0h

Table 14-21509. EMIF_CTLCFG_DENALI_PI_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_DFS_PERIOD_EN	R/W	0h	Enable the DFS triggered periodic leveling. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SEQUENTIAL_LVL_REQ	W	0h	User request to initiate all possible leveling sequences. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_SM2_RD	W	0h	SW leveling read command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_SM2_WR	W	0h	SW leveling write command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.522 EMIF_CTLCFG_DENALI_PI_26 Register

1 EMIF_CTLCFG_DENALI_PI_26 Register (Offset = 2068h) [reset = 1000000h]

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Table 14-21510. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A068h**

Figure 14-7135. EMIF_CTLCFG_DENALI_PI_26 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_16BIT_DRAM_CONNECT
NONE							R/W
0h							1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_DFI40_POLARITY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_MPD_PERIOD_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_SRE_PERIOD_EN
NONE							R/W
0h							0h

Table 14-21512. EMIF_CTLCFG_DENALI_PI_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_16BIT_DRAM_CONNECT	R/W	1h	Enable 16/32 bit DRAM configuration. 0: 16bit DRAM. 1: 32 bit DRAM. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DFI40_POLARITY	R/W	0h	Defines the polarity of the dfi_wrdata_cs_n/dfi_rddata_cs_n signals. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MPD_PERIOD_EN	R/W	0h	Enable the max power saving mode exit triggered periodic leveling. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SRE_PERIOD_EN	R/W	0h	Enable the self refresh exit triggered periodic leveling. Reset Source: ctl_amod_g_rst_n

14.6.6.2.523 EMIF_CTLCFG_DENALI_PI_27 Register

1 EMIF_CTLCFG_DENALI_PI_27 Register (Offset = 206Ch) [reset = 0h]

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Table 14-21513. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A06Ch**

Figure 14-7136. EMIF_CTLCFG_DENALI_PI_27 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_WLDQSEN					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						PI_WRLVL_CS	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PI_WRLVL_CS_SW			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_REQ
NONE							W
0h							0h

Table 14-21515. EMIF_CTLCFG_DENALI_PI_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_WLDQSEN	R/W	0h	Delay from issuing MRS to first DQS strobe for write leveling. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_WRLVL_CS	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_WRLVL_CS_SW	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WRLVL_REQ	W	0h	User request to initiate write leveling. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.524 EMIF_CTLCFG_DENALI_PI_28 Register

1 EMIF_CTLCFG_DENALI_PI_28 Register (Offset = 2070h) [reset = 0h]

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Table 14-21516. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A070h**

Figure 14-7137. EMIF_CTLCFG_DENALI_PI_28 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_ON_SREF_EXIT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_WRLVL_INTERVAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WRLVL_INTERVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_WLMRD					
NONE		R/W					
0h		0h					

Table 14-21518. EMIF_CTLCFG_DENALI_PI_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WRLVL_ON_SREF_EXIT	R/W	0h	Enables automatic write leveling on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PI_WRLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic write leveling commands. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_WLMRD	R/W	0h	Delay from issuing MRS to first write leveling strobe. Reset Source: ctl_amod_g_rst_n

14.6.6.2.525 EMIF_CTLCFG_DENALI_PI_29 Register

1 EMIF_CTLCFG_DENALI_PI_29 Register (Offset = 2074h) [reset = 0h]

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Table 14-21519. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A074h**

Figure 14-7138. EMIF_CTLCFG_DENALI_PI_29 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_WRLVL_CS_MAP			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PI_WRLVL_ROTATE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PI_WRLVL_RESP_MASK			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_DISABLE_DFS
NONE							R/W
0h							0h

Table 14-21521. EMIF_CTLCFG_DENALI_PI_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_WRLVL_CS_MAP	R/W	0h	Defines the chip select map for write leveling operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for write leveling. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WRLVL_ROTATE	R/W	0h	Enables rotational CS for counter triggered automatic write leveling. Set to 1, only one rank's write levling will process, the rank number is rotational for each time that write leveling been triggered by counter expiring. Set to 0 or not a short pattern leveling [indicated by dfi_lvl_periodic], the counter expired write leveling will process all the ranks. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_WRLVL_RESP_MASK	R/W	0h	Mask for the dfi_wrlvl_resp signal during write leveling. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21521. EMIF_CTLCFG_DENALI_PI_29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PI_WRLVL_DISABLE_DFS	R/W	0h	Disable automatic write leveling on freq change. Set to 1 to disable wrlvl on dfs,set 0 enable wrlvl on dfs. Reset Source: ctl_amod_g_rst_n

14.6.6.2.526 EMIF_CTLCFG_DENALI_PI_30 Register

1 EMIF_CTLCFG_DENALI_PI_30 Register (Offset = 2078h) [reset = 0h]

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Table 14-21522. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A078h**

Figure 14-7139. EMIF_CTLCFG_DENALI_PI_30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_WRLVL_ERROR_STATUS
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_ON_MPD_EXIT
NONE							R/W
0h							0h

Table 14-21524. EMIF_CTLCFG_DENALI_PI_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_TDFI_WRLVL_EN	R/W	0h	Defines the DFI tWRLVL_EN timing parameter [in DFI clocks], the minimum cycles from a dfi_wrlvl_en assertion to the first dfi_wrlvl_strobe assertion. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WRLVL_ERROR_STATUS	R	0h	Holds the error associated with the write level error interrupt. Bit [0] set indicates a TDFI_WRLVL_MAX parameter violation and bit [1] set indicates a TDFI_WRLVL_RESP parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WRLVL_ON_MPD_EXIT	R/W	0h	Enables automatic write leveling on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.527 EMIF_CTLCFG_DENALI_PI_31 Register

1 EMIF_CTLCFG_DENALI_PI_31 Register (Offset = 207Ch) [reset = 0h]

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Table 14-21525. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A07Ch**

Figure 14-7140. EMIF_CTLCFG_DENALI_PI_31 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WRLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_RESP							
R/W							
0h							

Table 14-21527. EMIF_CTLCFG_DENALI_PI_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WRLVL_RESP	R/W	0h	Defines the DFI tWRLVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_wrlvl_req assertion and a dfi_wrlvl_en assertion. Reset Source: ctl_amod_g_rst_n

14.6.6.2.528 EMIF_CTLCFG_DENALI_PI_32 Register

1 EMIF_CTLCFG_DENALI_PI_32 Register (Offset = 2080h) [reset = 0h]

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Table 14-21528. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A080h

Figure 14-7141. EMIF_CTLCFG_DENALI_PI_32 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WRLVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_MAX							
R/W							
0h							

Table 14-21530. EMIF_CTLCFG_DENALI_PI_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WRLVL_MAX	R/W	0h	Defines the DFI tWRLVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_wrlvl_en assertion and a valid dfi_wrlvl_resp. Reset Source: ctl_amod_g_rst_n

14.6.6.2.529 EMIF_CTLCFG_DENALI_PI_33 Register

1 EMIF_CTLCFG_DENALI_PI_33 Register (Offset = 2084h) [reset = 0h]

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Table 14-21531. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A084h**

Figure 14-7142. EMIF_CTLCFG_DENALI_PI_33 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ODT_VALUE			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TODTH_RD			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TODTH_WR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_WRLVL_STROBE_NUM				
NONE			R/W				
0h			0h				

Table 14-21533. EMIF_CTLCFG_DENALI_PI_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TODTH_RD	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a read command, in memory clocks. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TODTH_WR	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a write command, in memory clocks. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_WRLVL_STROBE_NUM	R/W	0h	Defines the number of write leveling strobes generated. Reset Source: ctl_amod_g_rst_n

14.6.6.2.530 EMIF_CTLCFG_DENALI_PI_34 Register

1 EMIF_CTLCFG_DENALI_PI_34 Register (Offset = 2088h) [reset = 0h]

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Table 14-21534. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A088h**

Figure 14-7143. EMIF_CTLCFG_DENALI_PI_34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_ADDRESS_MIRRORING			
NONE				R/W			
0h				0h			

Table 14-21536. EMIF_CTLCFG_DENALI_PI_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_ADDRESS_MIRRORING	R/W	0h	Indicates which chip selects support address mirroring. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.531 EMIF_CTLCFG_DENALI_PI_35 Register

1 EMIF_CTLCFG_DENALI_PI_35 Register (Offset = 208Ch) [reset = 0h]

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Table 14-21537. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A08Ch

Figure 14-7144. EMIF_CTLCFG_DENALI_PI_35 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_CA_PARITY_ERROR_INJECT	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							

Table 14-21539. EMIF_CTLCFG_DENALI_PI_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PI_CA_PARITY_ERROR_INJECT	R/W	0h	Selects bit to corrupt on the CA bus for CA parity error injection. Reset Source: ctl_amod_g_rst_n

14.6.6.2.532 EMIF_CTLCFG_DENALI_PI_36 Register

1 EMIF_CTLCFG_DENALI_PI_36 Register (Offset = 2090h) [reset = 0h]

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Table 14-21540. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A090h**

Figure 14-7145. EMIF_CTLCFG_DENALI_PI_36 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_GATE_REQ
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_REQ
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED4			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED					PI_RESERVED3		
NONE					R/W		
0h					0h		

Table 14-21542. EMIF_CTLCFG_DENALI_PI_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_GATE_REQ	W	0h	User request to initiate gate training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_REQ	W	0h	User request to initiate data eye training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED4	R/W	0h	Reserved
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_RESERVED3	R/W	0h	Reserved

14.6.6.2.533 EMIF_CTLCFG_DENALI_PI_37 Register

1 EMIF_CTLCFG_DENALI_PI_37 Register (Offset = 2094h) [reset = 0h]

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Table 14-21543. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A094h

Figure 14-7146. EMIF_CTLCFG_DENALI_PI_37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_RDLVL_CS	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_RDLVL_CS_SW			
NONE				R/W			
0h				0h			

Table 14-21545. EMIF_CTLCFG_DENALI_PI_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_CS	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RDLVL_CS_SW	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.534 EMIF_CTLCFG_DENALI_PI_38 Register

1 EMIF_CTLCFG_DENALI_PI_38 Register (Offset = 2098h) [reset = 0h]

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Table 14-21546. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A098h**

Figure 14-7147. EMIF_CTLCFG_DENALI_PI_38 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_0							
R/W							
0h							

Table 14-21548. EMIF_CTLCFG_DENALI_PI_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_0	R/W	0h	Non-default pattern 0 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.535 EMIF_CTLCFG_DENALI_PI_39 Register

1 EMIF_CTLCFG_DENALI_PI_39 Register (Offset = 209Ch) [reset = 0h]

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Table 14-21549. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A09Ch**

Figure 14-7148. EMIF_CTLCFG_DENALI_PI_39 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_1							
R/W							
0h							

Table 14-21551. EMIF_CTLCFG_DENALI_PI_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_1	R/W	0h	Non-default pattern 1 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.536 EMIF_CTLCFG_DENALI_PI_40 Register

1 EMIF_CTLCFG_DENALI_PI_40 Register (Offset = 20A0h) [reset = 0h]

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Table 14-21552. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0A0h**

Figure 14-7149. EMIF_CTLCFG_DENALI_PI_40 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_RDLVL_PAT_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_RDLVL_PAT_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_RDLVL_PAT_2							
R/W							
0h							

Table 14-21554. EMIF_CTLCFG_DENALI_PI_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_2	R/W	0h	Non-default pattern 2 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.537 EMIF_CTLCFG_DENALI_PI_41 Register

1 EMIF_CTLCFG_DENALI_PI_41 Register (Offset = 20A4h) [reset = 0h]

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Table 14-21555. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0A4h**

Figure 14-7150. EMIF_CTLCFG_DENALI_PI_41 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_3							
R/W							
0h							

Table 14-21557. EMIF_CTLCFG_DENALI_PI_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_3	R/W	0h	Non-default pattern 3 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.538 EMIF_CTLCFG_DENALI_PI_42 Register

1 EMIF_CTLCFG_DENALI_PI_42 Register (Offset = 20A8h) [reset = 0h]

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Table 14-21558. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0A8h**

Figure 14-7151. EMIF_CTLCFG_DENALI_PI_42 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_4							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_4							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_4							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_4							
R/W							
0h							

Table 14-21560. EMIF_CTLCFG_DENALI_PI_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_4	R/W	0h	Non-default pattern 4 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.539 EMIF_CTLCFG_DENALI_PI_43 Register

1 EMIF_CTLCFG_DENALI_PI_43 Register (Offset = 20ACh) [reset = 0h]

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Table 14-21561. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0ACh**

Figure 14-7152. EMIF_CTLCFG_DENALI_PI_43 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_5							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_5							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_5							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_5							
R/W							
0h							

Table 14-21563. EMIF_CTLCFG_DENALI_PI_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_5	R/W	0h	Non-default pattern 5 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.540 EMIF_CTLCFG_DENALI_PI_44 Register

1 EMIF_CTLCFG_DENALI_PI_44 Register (Offset = 20B0h) [reset = 0h]

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Table 14-21564. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0B0h**

Figure 14-7153. EMIF_CTLCFG_DENALI_PI_44 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_6							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_6							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_6							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_6							
R/W							
0h							

Table 14-21566. EMIF_CTLCFG_DENALI_PI_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_6	R/W	0h	Non-default pattern 6 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.541 EMIF_CTLCFG_DENALI_PI_45 Register

1 EMIF_CTLCFG_DENALI_PI_45 Register (Offset = 20B4h) [reset = 0h]

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Table 14-21567. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0B4h**

Figure 14-7154. EMIF_CTLCFG_DENALI_PI_45 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_RDLVL_PAT_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_RDLVL_PAT_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_RDLVL_PAT_7							
R/W							
0h							

Table 14-21569. EMIF_CTLCFG_DENALI_PI_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_7	R/W	0h	Non-default pattern 7 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.542 EMIF_CTLCFG_DENALI_PI_46 Register

1 EMIF_CTLCFG_DENALI_PI_46 Register (Offset = 20B8h) [reset = 0h]

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Table 14-21570. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A0B8h

Figure 14-7155. EMIF_CTLCFG_DENALI_PI_46 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RDLVL_GATE_ON_SREF_EXIT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RDLVL_DISABLE_DFS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RDLVL_ON_SREF_EXIT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RDLVL_SEQ_EN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21572. EMIF_CTLCFG_DENALI_PI_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_GATE_ON_SREF_EXIT	R/W	0h	Enables automatic gate training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_DISABLE_DFS	R/W	0h	Disables automatic data eye training on freq change. Set to 1 to disable rdlvl on dfs,Set to 0 to enable rdlvl on dfs. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RDLVL_ON_SREF_EXIT	R/W	0h	Enables automatic data eye training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RDLVL_SEQ_EN	R/W	0h	Specifies the pattern, format and MPR for data eye training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.543 EMIF_CTLCFG_DENALI_PI_47 Register

1 EMIF_CTLCFG_DENALI_PI_47 Register (Offset = 20BCh) [reset = 0h]

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Table 14-21573. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A0BCh

Figure 14-7156. EMIF_CTLCFG_DENALI_PI_47 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_ROTATE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_GATE_ON_MPD_EXIT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_ON_MPD_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_GATE_DISABLE_DFS
NONE							R/W
0h							0h

Table 14-21575. EMIF_CTLCFG_DENALI_PI_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_ROTATE	R/W	0h	Enables rotational CS for interval data eye training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_GATE_ON_MPD_EXIT	R/W	0h	Enables automatic gate training on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RDLVL_ON_MPD_EXIT	R/W	0h	Enables automatic data eye training on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21575. EMIF_CTLCFG_DENALI_PI_47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PI_RDLVL_GATE_DISABLE_DFS	R/W	0h	Disables automatic gate training on freq change. Set to 1 to disable rdlvl_gate on dfs,Set to 0 to enable rdlvl_gate on dfs. Reset Source: ctl_amod_g_rst_n

14.6.6.2.544 EMIF_CTLCFG_DENALI_PI_48 Register

1 EMIF_CTLCFG_DENALI_PI_48 Register (Offset = 20C0h) [reset = 0h]

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Table 14-21576. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0C0h**

Figure 14-7157. EMIF_CTLCFG_DENALI_PI_48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_RDLVL_GATE_CS_MAP			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_RDLVL_CS_MAP			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_RDLVL_GATE_ROTATE
NONE							R/W
0h							0h

Table 14-21578. EMIF_CTLCFG_DENALI_PI_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PI_RDLVL_GATE_CS_MAP	R/W	0h	Defines the chip select map for gate training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for gate training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RDLVL_CS_MAP	R/W	0h	Defines the chip select map for data eye training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for data eye training. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_RDLVL_GATE_ROTATE	R/W	0h	Enables rotational CS for interval gate training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n

14.6.6.2.545 EMIF_CTLCFG_DENALI_PI_49 Register

1 EMIF_CTLCFG_DENALI_PI_49 Register (Offset = 20C4h) [reset = 0h]

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Table 14-21579. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0C4h**

Figure 14-7158. EMIF_CTLCFG_DENALI_PI_49 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_RDLVL_RR</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_RR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21581. EMIF_CTLCFG_DENALI_PI_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_RDLVL_RR	R/W	0h	Defines the DFI tRDLVL_RR timing parameter [in DFI clocks], the minimum cycles between read commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.546 EMIF_CTLCFG_DENALI_PI_50 Register

1 EMIF_CTLCFG_DENALI_PI_50 Register (Offset = 20C8h) [reset = 0h]

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Table 14-21582. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0C8h**

Figure 14-7159. EMIF_CTLCFG_DENALI_PI_50 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_RDLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_RDLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_RDLVL_RESP							
R/W							
0h							

Table 14-21584. EMIF_CTLCFG_DENALI_PI_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_RDLVL_RESP	R/W	0h	Defines the DFI tRDLVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_rdlvl_req or dfi_rdlvl_gate_req assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion. Reset Source: ctl_amod_g_rst_n

14.6.6.2.547 EMIF_CTLCFG_DENALI_PI_51 Register

1 EMIF_CTLCFG_DENALI_PI_51 Register (Offset = 20CCh) [reset = 0h]

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Table 14-21585. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A0CCh

Figure 14-7160. EMIF_CTLCFG_DENALI_PI_51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_RDLVL_RESP_MASK			
NONE				R/W			
0h				0h			

Table 14-21587. EMIF_CTLCFG_DENALI_PI_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TDFI_RDLVL_EN	R/W	0h	Defines the DFI tRDLVL_EN timing parameter [in DFI clocks], the minimum cycles from a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion to the first read or MRR. Set to 1 means the minium value[1 cycle], set to 0 means the maxium value Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RDLVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during data eye training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.548 EMIF_CTLCFG_DENALI_PI_52 Register

1 EMIF_CTLCFG_DENALI_PI_52 Register (Offset = 20D0h) [reset = 0h]

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Table 14-21588. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0D0h**

Figure 14-7161. EMIF_CTLCFG_DENALI_PI_52 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_RDLVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_RDLVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_RDLVL_MAX							
R/W							
0h							

Table 14-21590. EMIF_CTLCFG_DENALI_PI_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_RDLVL_MAX	R/W	0h	Defines the DFI tRDLVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion and a valid dfi_rdlvl_resp. Reset Source: ctl_amod_g_rst_n

14.6.6.2.549 EMIF_CTLCFG_DENALI_PI_53 Register

1 EMIF_CTLCFG_DENALI_PI_53 Register (Offset = 20D4h) [reset = 0h]

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Table 14-21591. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0D4h**

Figure 14-7162. EMIF_CTLCFG_DENALI_PI_53 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_RDLVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_RDLVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RDLVL_ERROR_STATUS</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21593. EMIF_CTLCFG_DENALI_PI_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	PI_RDLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic data eye training commands. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_RDLVL_ERROR_STATUS	R	0h	Holds the error associated with the data eye training error or gate training error interrupt. Uppermost bit set indicates a TDFI_RDLVL_RESP parameter violation. Next uppermost bit set indicates a TDFI_RDLVL_MAX parameter violation. Lower bits are reserved. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.550 EMIF_CTLCFG_DENALI_PI_54 Register

1 EMIF_CTLCFG_DENALI_PI_54 Register (Offset = 20D8h) [reset = 0h]

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Table 14-21594. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0D8h**

Figure 14-7163. EMIF_CTLCFG_DENALI_PI_54 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RDLVL_PATTERN_NUM			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RDLVL_PATTERN_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RDLVL_GATE_INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_GATE_INTERVAL							
R/W							
0h							

Table 14-21596. EMIF_CTLCFG_DENALI_PI_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RDLVL_PATTERN_NUM	R/W	0h	Defines the number of pattern supported in read leveling. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RDLVL_PATTERN_START	R/W	0h	Defines the start pattern in read leveling. Reset Source: ctl_amod_g_rst_n
15:0	PI_RDLVL_GATE_INTERVAL	R/W	0h	Number of long count sequences counted between automatic gate training commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.551 EMIF_CTLCFG_DENALI_PI_55 Register

1 EMIF_CTLCFG_DENALI_PI_55 Register (Offset = 20DCh) [reset = 0h]

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Table 14-21597. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A0DCh

Figure 14-7164. EMIF_CTLCFG_DENALI_PI_55 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_REG_DIMM_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RD_PREAMBLE_TRAINING_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PI_RDLVL_GATE_STROBE_NUM				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_RDLVL_STROBE_NUM				
NONE			R/W				
0h			0h				

Table 14-21599. EMIF_CTLCFG_DENALI_PI_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RDLVL_GATE_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read gate training. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RDLVL_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read eye training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.552 EMIF_CTLCFG_DENALI_PI_56 Register

1 EMIF_CTLCFG_DENALI_PI_56 Register (Offset = 20E0h) [reset = 0h]

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Table 14-21600. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0E0h**

Figure 14-7165. EMIF_CTLCFG_DENALI_PI_56 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CALVL_CS_SW</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_CALVL_REQ</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_PHY_WRLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_RDDATA_EN</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21602. EMIF_CTLCFG_DENALI_PI_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CALVL_CS_SW	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CALVL_REQ	W	0h	User request to initiate CA training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PI_TDFI_PHY_WRLAT	R	0h	Holds the calculated DFI tPHY_WRLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_en assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PI_TDFI_RDDATA_EN	R	0h	Holds the calculated DFI tRDDATA_EN timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_en assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.553 EMIF_CTLCFG_DENALI_PI_57 Register

1 EMIF_CTLCFG_DENALI_PI_57 Register (Offset = 20E4h) [reset = 0h]

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Table 14-21603. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0E4h**

Figure 14-7166. EMIF_CTLCFG_DENALI_PI_57 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_CALVL_SEQ_EN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED6</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RESERVED5</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_CALVL_CS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-21605. EMIF_CTLCFG_DENALI_PI_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_CALVL_SEQ_EN	R/W	0h	Specifies which CA training patterns will be used. Set to 0 for pattern 0 only, set to 1 for patterns 0 and 1, set to 2 for patterns 0, 1 and 2, or set to 3 for all patterns. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED6	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED5	R/W	0h	Reserved
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_CALVL_CS	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.554 EMIF_CTLCFG_DENALI_PI_58 Register

1 EMIF_CTLCFG_DENALI_PI_58 Register (Offset = 20E8h) [reset = 0h]

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Table 14-21606. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0E8h**

Figure 14-7167. EMIF_CTLCFG_DENALI_PI_58 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_CALVL_ROTATE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_CALVL_DISABLE_DFS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_CALVL_ON_SREF_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_CALVL_PERIODIC
NONE							R/W
0h							0h

Table 14-21608. EMIF_CTLCFG_DENALI_PI_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_CALVL_ROTATE	R/W	0h	Enables rotational CS for interval CA training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CALVL_DISABLE_DFS	R/W	0h	Disables automatic CA training on freq change. Set to 1 to disable CA training on dfs, Set to 0 to enable CA training . Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_CALVL_ON_SREF_EXIT	R/W	0h	Enables automatic CA training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CALVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during CA training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.555 EMIF_CTLCFG_DENALI_PI_59 Register

1 EMIF_CTLCFG_DENALI_PI_59 Register (Offset = 20ECh) [reset = 0h]

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Table 14-21609. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0ECh**

Figure 14-7168. EMIF_CTLCFG_DENALI_PI_59 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_CALVL_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CALVL_CS_MAP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21611. EMIF_CTLCFG_DENALI_PI_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TDFI_CALVL_EN	R/W	0h	Defines the DFI tCALVL_EN timing parameter [in DFI clocks], the minimum cycles between a dfi_calvl_en assertion and a dfi_cke de-assertion. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CALVL_CS_MAP	R/W	0h	Defines the chip select map for CA training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.556 EMIF_CTLCFG_DENALI_PI_60 Register

1 EMIF_CTLCFG_DENALI_PI_60 Register (Offset = 20F0h) [reset = 0h]

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Table 14-21612. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0F0h**

Figure 14-7169. EMIF_CTLCFG_DENALI_PI_60 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CALVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CALVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CALVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CALVL_RESP							
R/W							
0h							

Table 14-21614. EMIF_CTLCFG_DENALI_PI_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CALVL_RESP	R/W	0h	Defines the DFI tCALVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_calvl_req assertion and a dfi_calvl_en assertion. Reset Source: ctl_amod_g_rst_n

14.6.6.2.557 EMIF_CTLCFG_DENALI_PI_61 Register

1 EMIF_CTLCFG_DENALI_PI_61 Register (Offset = 20F4h) [reset = 0h]

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Table 14-21615. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0F4h**

Figure 14-7170. EMIF_CTLCFG_DENALI_PI_61 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CALVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CALVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CALVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CALVL_MAX							
R/W							
0h							

Table 14-21617. EMIF_CTLCFG_DENALI_PI_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CALVL_MAX	R/W	0h	Defines the DFI tCALVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_calvl_en assertion and a valid dfi_calvl_resp. Reset Source: ctl_amod_g_rst_n

14.6.6.2.558 EMIF_CTLCFG_DENALI_PI_62 Register

1 EMIF_CTLCFG_DENALI_PI_62 Register (Offset = 20F8h) [reset = 0h]

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Table 14-21618. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A0F8h**

Figure 14-7171. EMIF_CTLCFG_DENALI_PI_62 Name Register

31	30	29	28	27	26	25	24
PI_CALVL_INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_CALVL_INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_CALVL_ERROR_STATUS	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PI_CALVL_RESP_MASK
NONE							R/W
0h							0h

Table 14-21620. EMIF_CTLCFG_DENALI_PI_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_CALVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic CA training commands. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_CALVL_ERROR_STATUS	R	0h	Holds the error associated with the CA training error interrupt. Bit [0] set indicates a TDFI_CALVL_RESP parameter violation and bit [1] set indicates a TDFI_CALVL_MAX parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CALVL_RESP_MASK	R/W	0h	Mask for the dfi_calvl_resp signal during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.559 EMIF_CTLCFG_DENALI_PI_63 Register

1 EMIF_CTLCFG_DENALI_PI_63 Register (Offset = 20FCh) [reset = 0h]

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Table 14-21621. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A0FCh

Figure 14-7172. EMIF_CTLCFG_DENALI_PI_63 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TCAEXT				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_TCACKEH				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED		PI_TCAMRD					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED			PI_TCACKEL				
NONE			R/W				
0h			0h				

Table 14-21623. EMIF_CTLCFG_DENALI_PI_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TCAEXT	R/W	0h	DRAM tCAEXT value in memory cycles. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TCACKEH	R/W	0h	DRAM tCACKEH value in memory cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_TCAMRD	R/W	0h	DRAM tCAMRD value in memory cycles. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCACKEL	R/W	0h	DRAM tCACKEL value in memory cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.560 EMIF_CTLCFG_DENALI_PI_64 Register

1 EMIF_CTLCFG_DENALI_PI_64 Register (Offset = 2100h) [reset = 0h]

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Table 14-21624. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A100h**

Figure 14-7173. EMIF_CTLCFG_DENALI_PI_64 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_START_MIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CALVL_VREF_NORMAL_STEPSIZE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CALVL_VREF_INITIAL_STEPSIZE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_CA_TRAIN_VREF_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21626. EMIF_CTLCFG_DENALI_PI_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TDFI_INIT_START_MIN	R/W	0h	Minimum number of DFI clocks before dfi_init_start can be driven after a previous command/training event. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CALVL_VREF_NORMAL_STEPSIZE	R/W	0h	The adjust step for the post-initial Vref[ca] training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_CALVL_VREF_INITIAL_STEPSIZE	R/W	0h	The adjust step for the initial Vref[ca] training. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CA_TRAIN_VREF_EN	R/W	0h	Control for VREF training during CA training post power-on initialization. Set to enable VREF training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.561 EMIF_CTLCFG_DENALI_PI_65 Register

1 EMIF_CTLCFG_DENALI_PI_65 Register (Offset = 2104h) [reset = 1000000h]

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Table 14-21627. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A104h**

Figure 14-7174. EMIF_CTLCFG_DENALI_PI_65 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_REFRESH_BETWEEN_SEGMENT_DISABLE
NONE							R/W
0h							1h
23	22	21	20	19	18	17	16
RESERVED	PI_SW_CA_TRAIN_VREF						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED			PI_CALVL_STROBE_NUM				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PI_TCKCKEH							
R/W							
0h							

Table 14-21629. EMIF_CTLCFG_DENALI_PI_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_REFRESH_BETWEEN_SEGMENT_DISABLE	R/W	1h	Disable the refresh between CA first and second segment training. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_SW_CA_TRAIN_VREF	R/W	0h	The Vref value which is set for SW step by step CA training. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CALVL_STROBE_NUM	R/W	0h	The consecutive dfi_calvl_strobe number when updating the CA vref data. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKCKEH	R/W	0h	DRAM tCKELCK Clock and command valid before CKE HIGH. Reset Source: ctl_amod_g_rst_n

14.6.6.2.562 EMIF_CTLCFG_DENALI_PI_66 Register

1 EMIF_CTLCFG_DENALI_PI_66 Register (Offset = 2108h) [reset = 0h]

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Table 14-21630. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A108h**

Figure 14-7175. EMIF_CTLCFG_DENALI_PI_66 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_INIT_COMPLETE_MIN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_DRAM_CLK_DISABLE_DEASSERT_SEL
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_INIT_STARTORCOMPLETE_2_CLKDISABLE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_CLKDISABLE_2_INIT_START							
R/W							
0h							

Table 14-21632. EMIF_CTLCFG_DENALI_PI_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TDFI_INIT_COMPLETE_MIN	R/W	0h	Minimum number of DFI clocks from dfi_init_complete to a command/training event. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DRAM_CLK_DISABLE_DEASSERT_SEL	R/W	0h	Indicate dfi_dram_clk_disable deassert following dfi_init_start deassert or dfi_init_complete assert. Set to 0: dfi_dram_clk_disable deassert following dfi_init_start deassert. Set to 1: dfi_dram_clk_disable deassert following dfi_init_complete assert. Reset Source: ctl_amod_g_rst_n
15:8	PI_INIT_STARTORCOMPLETE_2_CLKDISABLE	R/W	0h	Defines the delay from deasserting of dfi_init_start or asserting of dfi_init_complete to deasserting of dfi_dram_clk_disable in DFI clock. Reset Source: ctl_amod_g_rst_n
7:0	PI_CLKDISABLE_2_INIT_START	R/W	0h	Defines the delay from the asserting of dfi_dram_clk_disable to the asserting of dfi_init_start in DFI clock. Reset Source: ctl_amod_g_rst_n

14.6.6.2.563 EMIF_CTLCFG_DENALI_PI_67 Register

1 EMIF_CTLCFG_DENALI_PI_67 Register (Offset = 210Ch) [reset = 0h]

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Table 14-21633. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A10Ch

Figure 14-7176. EMIF_CTLCFG_DENALI_PI_67 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MC_DFS_PI_SET_VREF_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_VREFLVL_DISABLE_DFS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_VREF_PDA_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PI_VREF_CS	
NONE						R/W	
0h						0h	

Table 14-21635. EMIF_CTLCFG_DENALI_PI_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MC_DFS_PI_SET_VREF_ENABLE	R/W	0h	Enable the PI to set VREF value after DFS issued by MC. MR12 and MR14 for LPDDR4. MR6 for DDR4. 1 means disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_VREFLVL_DISABLE_DFS	R/W	0h	Disables automatic VREF training on freq change. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_VREF_PDA_EN	R/W	0h	Enable per-DRAM addressability during VREF training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_VREF_CS	R/W	0h	Specifies the target chip select for the VREF training operation. Reset Source: ctl_amod_g_rst_n

14.6.6.2.564 EMIF_CTLCFG_DENALI_PI_68 Register

1 EMIF_CTLCFG_DENALI_PI_68 Register (Offset = 2110h) [reset = 0h]

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Table 14-21636. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A110h**

Figure 14-7177. EMIF_CTLCFG_DENALI_PI_68 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_WDQLVL_RESP_MASK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PI_WDQLVL_BST_NUM</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_WDQLVL_VREF_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_INIT_COMPLETE_TO_MC_DELAY_COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21638. EMIF_CTLCFG_DENALI_PI_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_WDQLVL_RESP_MASK	R/W	0h	Write DQ training response mask. When set to 1, the dfi_wdqlvl_en of the slice is not asserted. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_WDQLVL_BST_NUM	R/W	0h	Defines the number of write/read bursts issued at each step in write DQ training. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_VREF_EN	R/W	0h	Control for VREF training as part of non-initialization write DQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_INIT_COMPLETE_TO_MC_DELAY_COUNT	R/W	0h	It controls the time PI bypass CKE at the beginning of PI mask dfi_init_complete to controller. Reset Source: ctl_amod_g_rst_n

14.6.6.2.565 EMIF_CTLCFG_DENALI_PI_69 Register

1 EMIF_CTLCFG_DENALI_PI_69 Register (Offset = 2114h) [reset = 0h]

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Table 14-21639. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A114h**

Figure 14-7178. EMIF_CTLCFG_DENALI_PI_69 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_WDQLVL_VREF_NORMAL_STEPSIZE				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_WDQLVL_VREF_INITIAL_STEPSIZE				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_WDQLVL_CS_MAP			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_WDQLVL_ROTATE
NONE							R/W
0h							0h

Table 14-21641. EMIF_CTLCFG_DENALI_PI_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_VREF_NORMAL_STEPSIZE	R/W	0h	Write DQ training vref step size for post_initial training. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_WDQLVL_VREF_INITIAL_STEPSIZE	R/W	0h	Write DQ training vref step size for initial training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_WDQLVL_CS_MAP	R/W	0h	Map of CS's included in write DQ training sequence. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_ROTATE	R/W	0h	Enables write DQ training rotate for interval training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.566 EMIF_CTLCFG_DENALI_PI_70 Register

1 EMIF_CTLCFG_DENALI_PI_70 Register (Offset = 2118h) [reset = 0h]

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Table 14-21642. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A118h**

Figure 14-7179. EMIF_CTLCFG_DENALI_PI_70 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WDQLVL_CS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_WDQLVL_CS_SW</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_WDQLVL_REQ</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_WDQLVL_PERIODIC</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21644. EMIF_CTLCFG_DENALI_PI_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_WDQLVL_CS	R/W	0h	Write DQ training target chip select. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_WDQLVL_CS_SW	R/W	0h	Write DQ training target chip select. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_REQ	W	0h	SW write to initiate Write DQ training request. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_PERIODIC	R/W	0h	Enables periodic write DQ training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.567 EMIF_CTLCFG_DENALI_PI_71 Register

1 EMIF_CTLCFG_DENALI_PI_71 Register (Offset = 211Ch) [reset = 0h]

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Table 14-21645. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A11Ch**

Figure 14-7180. EMIF_CTLCFG_DENALI_PI_71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_WDQLVL_EN							
R/W							
0h							

Table 14-21647. EMIF_CTLCFG_DENALI_PI_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDFI_WDQLVL_EN	R/W	0h	DFI timing param tWDQLVL_EN. Minimum number of DFI clocks required after the write DQ training enable signal is asserted until the first write command may be asserted. Reset Source: ctl_amod_g_rst_n

14.6.6.2.568 EMIF_CTLCFG_DENALI_PI_72 Register

1 EMIF_CTLCFG_DENALI_PI_72 Register (Offset = 2120h) [reset = 0h]

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Table 14-21648. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A120h**

Figure 14-7181. EMIF_CTLCFG_DENALI_PI_72 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RESP							
R/W							
0h							

Table 14-21650. EMIF_CTLCFG_DENALI_PI_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WDQLVL_RESP	R/W	0h	DFI timing param tWDQLVL_RESP. Maximum number of DFI clocks that may occur between a write DQ training request and the associated mode enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.569 EMIF_CTLCFG_DENALI_PI_73 Register

1 EMIF_CTLCFG_DENALI_PI_73 Register (Offset = 2124h) [reset = 0h]

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Table 14-21651. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A124h**

Figure 14-7182. EMIF_CTLCFG_DENALI_PI_73 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_MAX							
R/W							
0h							

Table 14-21653. EMIF_CTLCFG_DENALI_PI_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WDQLVL_MAX	R/W	0h	DFI timing param tWDQLVL_MAX. Maximum number of DFI clocks that the PI will wait for a response from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.570 EMIF_CTLCFG_DENALI_PI_74 Register

1 EMIF_CTLCFG_DENALI_PI_74 Register (Offset = 2128h) [reset = 0h]

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Table 14-21654. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A128h**

Figure 14-7183. EMIF_CTLCFG_DENALI_PI_74 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_ON_MPD_EXIT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_WDQLVL_ON_SREF_EXIT
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WDQLVL_INTERVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WDQLVL_INTERVAL							
R/W							
0h							

Table 14-21656. EMIF_CTLCFG_DENALI_PI_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_ON_MPD_EXIT	R/W	0h	Issue a write DQ training command on maximum power saving mode exit. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WDQLVL_ON_SREF_EXIT	R/W	0h	Issue a write DQ training command on self-refresh exit. Reset Source: ctl_amod_g_rst_n
15:0	PI_WDQLVL_INTERVAL	R/W	0h	Sets the maximum number of long count sequences allowed between automatic write DQ training operations. Reset Source: ctl_amod_g_rst_n

14.6.6.2.571 EMIF_CTLCFG_DENALI_PI_75 Register

1 EMIF_CTLCFG_DENALI_PI_75 Register (Offset = 212Ch) [reset = 0h]

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Table 14-21657. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A12Ch

Figure 14-7184. EMIF_CTLCFG_DENALI_PI_75 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_WDQLVL_NEED_SAVE_RESTORE	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_WDQLVL_ERROR_STATUS	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_WDQLVL_DISABLE_DFS
NONE							R/W
0h							0h

Table 14-21659. EMIF_CTLCFG_DENALI_PI_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PI_WDQLVL_NEED_SAVE_RESTORE	R/W	0h	Enables the use of functional DRAM address space for write DQ training, 1 = enable, not for LPDDR4. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_ERROR_STATUS	R	0h	Holds the error associated with the write dq level error interrupt. Bit [0] set indicates a PI_TDFI_WDQLVL_MAX parameter violation and bit [1] set indicates a PI_TDFI_WDQLVL_RESP parameter violation. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_DISABLE_DFS	R/W	0h	Disable automatic write DQ training on freq change. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.572 EMIF_CTLCFG_DENALI_PI_76 Register

1 EMIF_CTLCFG_DENALI_PI_76 Register (Offset = 2130h) [reset = 0h]

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Table 14-21660. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A130h**

Figure 14-7185. EMIF_CTLCFG_DENALI_PI_76 Name Register

31	30	29	28	27	26	25	24
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							

Table 14-21662. EMIF_CTLCFG_DENALI_PI_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_WDQLVL_DRAM_LVL_START_ADDR_0	R/W	0h	Start address of WDQ leveling, not for LPDDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.573 EMIF_CTLCFG_DENALI_PI_77 Register

1 EMIF_CTLCFG_DENALI_PI_77 Register (Offset = 2134h) [reset = 0h]

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Table 14-21663. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 A134h**

Figure 14-7186. EMIF_CTLCFG_DENALI_PI_77 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_NO_MEMORY_DM
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_WDQLVL_DM_LEVEL_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PI_WDQLVL_DRAM_LVL_START_ADDR_1		
NONE					R/W		
0h					0h		

Table 14-21665. EMIF_CTLCFG_DENALI_PI_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PI_NO_MEMORY_DM	R/W	0h	Defines if the attached memory supports the Data Mask function, 1 = not supported. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_DM_LEVEL_EN	R/W	0h	Enable for write DM training as part of the write DQ training, not for LPDDR4. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_WDQLVL_DRAM_LVL_START_ADDR_1	R/W	0h	Start address of WDQ leveling, not for LPDDR4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.574 EMIF_CTLCFG_DENALI_PI_78 Register

1 EMIF_CTLCFG_DENALI_PI_78 Register (Offset = 2138h) [reset = 0h]

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Table 14-21666. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A138h**

Figure 14-7187. EMIF_CTLCFG_DENALI_PI_78 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_NIBBLE_MODE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_SWLVL_SM2_DM_NIBBLE_START
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TDFI_WDQLVL_WW	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_WDQLVL_WW							
R/W							
0h							

Table 14-21668. EMIF_CTLCFG_DENALI_PI_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_NIBBLE_MODE	R/W	0h	WDQ Training Nibble mode indication. When set to 1, nibble mode is enabled, and the training timing is doubled. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_SM2_DM_NIBBLE_START	W	0h	Start command for stage 2, when in the process of DM leveling or nibble mode. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_WW	R/W	0h	Minimum number of DFI clocks to be inserted between write commands during the DM portion of write DQ training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.575 EMIF_CTLCFG_DENALI_PI_79 Register

1 EMIF_CTLCFG_DENALI_PI_79 Register (Offset = 213Ch) [reset = 0h]

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Table 14-21669. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A13Ch**

Figure 14-7188. EMIF_CTLCFG_DENALI_PI_79 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_PDA_VREF_TRAIN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_WDQLVL_PDA_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_DQS_OSC_PERIOD_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_OSC_EN
NONE							R/W
0h							0h

Table 14-21671. EMIF_CTLCFG_DENALI_PI_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_PDA_VREF_TRAIN	R/W	0h	Enable for the use of PDA to set the VREF during write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WDQLVL_PDA_EN	R/W	0h	Enable for the use of write DQ training for PDA mode, 1 = enabled. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DQS_OSC_PERIOD_EN	R/W	0h	Enable for DQS oscillator triggered periodic write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_OSC_EN	R/W	0h	Enable for DQS oscillator triggered write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n

14.6.6.2.576 EMIF_CTLCFG_DENALI_PI_80 Register

1 EMIF_CTLCFG_DENALI_PI_80 Register (Offset = 2140h) [reset = 0h]

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Table 14-21672. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A140h**

Figure 14-7189. EMIF_CTLCFG_DENALI_PI_80 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PI_ROW_DIFF</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_BANK_DIFF</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_DBILVL_RESP_MASK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_PARALLEL_WDQLVL_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21674. EMIF_CTLCFG_DENALI_PI_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_ROW_DIFF	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_BANK_DIFF	R/W	0h	Difference between number of bank pins available and number being used. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_DBILVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during read dbi training. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_PARALLEL_WDQLVL_EN	R/W	0h	Enable per rank parallel Write DQ training for LPDDR4, 1 = enabled. Reset Source: ctl_amod_g_rst_n

14.6.6.2.577 EMIF_CTLCFG_DENALI_PI_81 Register

1 EMIF_CTLCFG_DENALI_PI_81 Register (Offset = 2144h) [reset = 2000000h]

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Table 14-21675. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A144h**

Figure 14-7190. EMIF_CTLCFG_DENALI_PI_81 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED9			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED8			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED7			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			PI_TCCD				
NONE			R/W				
0h			0h				

Table 14-21677. EMIF_CTLCFG_DENALI_PI_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED9	R/W	2h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED8	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED7	R/W	0h	Reserved
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.578 EMIF_CTLCFG_DENALI_PI_82 Register

1 EMIF_CTLCFG_DENALI_PI_82 Register (Offset = 2148h) [reset = 1000200h]

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Table 14-21678. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A148h**

Figure 14-7191. EMIF_CTLCFG_DENALI_PI_82 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED13			
NONE				R/W			
0h				1h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED12			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED11			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED10			
NONE				R/W			
0h				0h			

Table 14-21680. EMIF_CTLCFG_DENALI_PI_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED13	R/W	1h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED12	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED11	R/W	2h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED10	R/W	0h	Reserved

14.6.6.2.579 EMIF_CTLCFG_DENALI_PI_83 Register

1 EMIF_CTLCFG_DENALI_PI_83 Register (Offset = 214Ch) [reset = 100h]

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Table 14-21681. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A14Ch**

Figure 14-7192. EMIF_CTLCFG_DENALI_PI_83 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED17			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED16			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED15			
NONE				R/W			
0h				1h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED14			
NONE				R/W			
0h				0h			

Table 14-21683. EMIF_CTLCFG_DENALI_PI_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED17	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED16	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED15	R/W	1h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED14	R/W	0h	Reserved

14.6.6.2.580 EMIF_CTLCFG_DENALI_PI_84 Register

1 EMIF_CTLCFG_DENALI_PI_84 Register (Offset = 2150h) [reset = 2000100h]

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Table 14-21684. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A150h**

Figure 14-7193. EMIF_CTLCFG_DENALI_PI_84 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED21			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED20			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED19			
NONE				R/W			
0h				1h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED18			
NONE				R/W			
0h				0h			

Table 14-21686. EMIF_CTLCFG_DENALI_PI_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED21	R/W	2h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED20	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED19	R/W	1h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED18	R/W	0h	Reserved

14.6.6.2.581 EMIF_CTLCFG_DENALI_PI_85 Register

1 EMIF_CTLCFG_DENALI_PI_85 Register (Offset = 2154h) [reset = 2000200h]

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Table 14-21687. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A154h**

Figure 14-7194. EMIF_CTLCFG_DENALI_PI_85 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED25			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED24			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED23			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED22			
NONE				R/W			
0h				0h			

Table 14-21689. EMIF_CTLCFG_DENALI_PI_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED25	R/W	2h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED24	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED23	R/W	2h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED22	R/W	0h	Reserved

14.6.6.2.582 EMIF_CTLCFG_DENALI_PI_86 Register

1 EMIF_CTLCFG_DENALI_PI_86 Register (Offset = 2158h) [reset = 0h]

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Table 14-21690. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A158h**

Figure 14-7195. EMIF_CTLCFG_DENALI_PI_86 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED26</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21692. EMIF_CTLCFG_DENALI_PI_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED26	R/W	0h	Reserved

14.6.6.2.583 EMIF_CTLCFG_DENALI_PI_87 Register

1 EMIF_CTLCFG_DENALI_PI_87 Register (Offset = 215Ch) [reset = 0h]

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Table 14-21693. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A15Ch**

Figure 14-7196. EMIF_CTLCFG_DENALI_PI_87 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_INT_STATUS					
NONE		R					
0h		0h					
23	22	21	20	19	18	17	16
PI_INT_STATUS							
R							
0h							
15	14	13	12	11	10	9	8
PI_INT_STATUS							
R							
0h							
7	6	5	4	3	2	1	0
PI_INT_STATUS							
R							
0h							

Table 14-21695. EMIF_CTLCFG_DENALI_PI_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_INT_STATUS	R	0h	Status of interrupt features in the PI. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.584 EMIF_CTLCFG_DENALI_PI_88 Register

1 EMIF_CTLCFG_DENALI_PI_88 Register (Offset = 2160h) [reset = 0h]

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Table 14-21696. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A160h

Figure 14-7197. EMIF_CTLCFG_DENALI_PI_88 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_INT_ACK				
NONE			W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_INT_ACK							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_INT_ACK							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_INT_ACK							
W							
0h							

Table 14-21698. EMIF_CTLCFG_DENALI_PI_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	PI_INT_ACK	W	0h	Clear the corresponding interrupt bit of the PI_INT_STATUS parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.585 EMIF_CTLCFG_DENALI_PI_89 Register

1 EMIF_CTLCFG_DENALI_PI_89 Register (Offset = 2164h) [reset = 0h]

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Table 14-21699. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A164h**

Figure 14-7198. EMIF_CTLCFG_DENALI_PI_89 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_INT_MASK					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_INT_MASK							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_INT_MASK							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_INT_MASK							
R/W							
0h							

Table 14-21701. EMIF_CTLCFG_DENALI_PI_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_INT_MASK	R/W	0h	Mask for PI_int signals from the PI_INT_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.586 EMIF_CTLCFG_DENALI_PI_90 Register

1 EMIF_CTLCFG_DENALI_PI_90 Register (Offset = 2168h) [reset = 0h]

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Table 14-21702. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A168h**

Figure 14-7199. EMIF_CTLCFG_DENALI_PI_90 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_0							
R							
0h							

Table 14-21704. EMIF_CTLCFG_DENALI_PI_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.587 EMIF_CTLCFG_DENALI_PI_91 Register

1 EMIF_CTLCFG_DENALI_PI_91 Register (Offset = 216Ch) [reset = 0h]

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Table 14-21705. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A16Ch**

Figure 14-7200. EMIF_CTLCFG_DENALI_PI_91 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_1							
R							
0h							

Table 14-21707. EMIF_CTLCFG_DENALI_PI_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.588 EMIF_CTLCFG_DENALI_PI_92 Register

1 EMIF_CTLCFG_DENALI_PI_92 Register (Offset = 2170h) [reset = 0h]

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Table 14-21708. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A170h**

Figure 14-7201. EMIF_CTLCFG_DENALI_PI_92 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_2							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_2							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_2							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_2							
R							
0h							

Table 14-21710. EMIF_CTLCFG_DENALI_PI_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_2	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.589 EMIF_CTLCFG_DENALI_PI_93 Register

1 EMIF_CTLCFG_DENALI_PI_93 Register (Offset = 2174h) [reset = 0h]

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Table 14-21711. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A174h**

Figure 14-7202. EMIF_CTLCFG_DENALI_PI_93 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_3							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_3							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_3							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_3							
R							
0h							

Table 14-21713. EMIF_CTLCFG_DENALI_PI_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_3	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.590 EMIF_CTLCFG_DENALI_PI_94 Register

1 EMIF_CTLCFG_DENALI_PI_94 Register (Offset = 2178h) [reset = 0h]

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Table 14-21714. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A178h**

Figure 14-7203. EMIF_CTLCFG_DENALI_PI_94 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_FAIL_DATA_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_FAIL_DATA_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_FAIL_DATA_0							
R							
0h							

Table 14-21716. EMIF_CTLCFG_DENALI_PI_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.591 EMIF_CTLCFG_DENALI_PI_95 Register

1 EMIF_CTLCFG_DENALI_PI_95 Register (Offset = 217Ch) [reset = 0h]

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Table 14-21717. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A17Ch**

Figure 14-7204. EMIF_CTLCFG_DENALI_PI_95 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_1							
R							
0h							

Table 14-21719. EMIF_CTLCFG_DENALI_PI_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.592 EMIF_CTLCFG_DENALI_PI_96 Register

1 EMIF_CTLCFG_DENALI_PI_96 Register (Offset = 2180h) [reset = 0h]

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Table 14-21720. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A180h**

Figure 14-7205. EMIF_CTLCFG_DENALI_PI_96 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_2							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_DATA_2							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_DATA_2							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_2							
R							
0h							

Table 14-21722. EMIF_CTLCFG_DENALI_PI_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_2	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.593 EMIF_CTLCFG_DENALI_PI_97 Register

1 EMIF_CTLCFG_DENALI_PI_97 Register (Offset = 2184h) [reset = 0h]

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Table 14-21723. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A184h**

Figure 14-7206. EMIF_CTLCFG_DENALI_PI_97 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_3							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_DATA_3							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_DATA_3							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_3							
R							
0h							

Table 14-21725. EMIF_CTLCFG_DENALI_PI_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_3	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.594 EMIF_CTLCFG_DENALI_PI_98 Register

1 EMIF_CTLCFG_DENALI_PI_98 Register (Offset = 2188h) [reset = 0h]

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Table 14-21726. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A188h**

Figure 14-7207. EMIF_CTLCFG_DENALI_PI_98 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_ADDR_0							
R							
0h							

Table 14-21728. EMIF_CTLCFG_DENALI_PI_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_ADDR_0	R	0h	The burst aligned address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.595 EMIF_CTLCFG_DENALI_PI_99 Register

1 EMIF_CTLCFG_DENALI_PI_99 Register (Offset = 218Ch) [reset = 200h]

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Table 14-21729. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A18Ch**

Figure 14-7208. EMIF_CTLCFG_DENALI_PI_99 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_CMD_SWAP_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_LONG_COUNT_MASK</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_BSTLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PI_BIST_FAIL_ADDR_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-21731. EMIF_CTLCFG_DENALI_PI_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_CMD_SWAP_EN	R/W	0h	Command pin swap function enable Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_BIST_FAIL_ADDR_1	R	0h	The burst aligned address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.596 EMIF_CTLCFG_DENALI_PI_100 Register

1 EMIF_CTLCFG_DENALI_PI_100 Register (Offset = 2190h) [reset = 0h]

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Table 14-21732. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A190h

Figure 14-7209. EMIF_CTLCFG_DENALI_PI_100 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_BG_MUX_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_BG_MUX_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_ACT_N_MUX				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_PARITY_IN_MUX				
NONE			R/W				
0h			0h				

Table 14-21734. EMIF_CTLCFG_DENALI_PI_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_BG_MUX_1	R/W	0h	Command pin BG_1 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_BG_MUX_0	R/W	0h	Command pin BG_0 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_ACT_N_MUX	R/W	0h	Command pin ACT_N mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_PARITY_IN_MUX	R/W	0h	Command pin parity mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.597 EMIF_CTLCFG_DENALI_PI_101 Register

1 EMIF_CTLCFG_DENALI_PI_101 Register (Offset = 2194h) [reset = 0h]

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Table 14-21735. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A194h**

Figure 14-7210. EMIF_CTLCFG_DENALI_PI_101 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_BANK_MUX_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_WE_N_MUX				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_CAS_N_MUX				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_RAS_N_MUX				
NONE			R/W				
0h			0h				

Table 14-21737. EMIF_CTLCFG_DENALI_PI_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_BANK_MUX_0	R/W	0h	Command pin BANK_0 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_WE_N_MUX	R/W	0h	Command pin WE_N mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CAS_N_MUX	R/W	0h	Command pin CAS_N mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RAS_N_MUX	R/W	0h	Command pin RAS_N mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.598 EMIF_CTLCFG_DENALI_PI_102 Register

1 EMIF_CTLCFG_DENALI_PI_102 Register (Offset = 2198h) [reset = 0h]

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Table 14-21738. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A198h

Figure 14-7211. EMIF_CTLCFG_DENALI_PI_102 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_DATA_BYTE_SWAP_SLICE1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_DATA_BYTE_SWAP_SLICE0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_DATA_BYTE_SWAP_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_BANK_MUX_1				
NONE			R/W				
0h			0h				

Table 14-21740. EMIF_CTLCFG_DENALI_PI_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_DATA_BYTE_SWAP_SLICE1	R/W	0h	DATA pin 1 mux selector Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_DATA_BYTE_SWAP_SLICE0	R/W	0h	DATA pin 0 mux selector Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DATA_BYTE_SWAP_EN	R/W	0h	DATA pin swap function enable Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_BANK_MUX_1	R/W	0h	Command pin BANK_1 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.599 EMIF_CTLCFG_DENALI_PI_103 Register

1 EMIF_CTLCFG_DENALI_PI_103 Register (Offset = 219Ch) [reset = 0h]

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Table 14-21741. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A19Ch**

Figure 14-7212. EMIF_CTLCFG_DENALI_PI_103 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_CTRLUPD_REQ_PER_AREF_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_DATA_BYTE_SWAP_SLICE3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_DATA_BYTE_SWAP_SLICE2	
NONE						R/W	
0h						0h	

Table 14-21743. EMIF_CTLCFG_DENALI_PI_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PI_CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic PI initiated update [dfi_ctrlupd_req] after every refresh. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_DATA_BYTE_SWAP_SLICE3	R/W	0h	DATA pin 3 mux selector Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_DATA_BYTE_SWAP_SLICE2	R/W	0h	DATA pin 2 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.600 EMIF_CTLCFG_DENALI_PI_104 Register

1 EMIF_CTLCFG_DENALI_PI_104 Register (Offset = 21A0h) [reset = 0h]

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Table 14-21744. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1A0h

Figure 14-7213. EMIF_CTLCFG_DENALI_PI_104 Name Register

31	30	29	28	27	26	25	24
RESERVED					PI_TDFI_PARIN_LAT		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						PI_UPDATE_ERROR_STATUS	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_MIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MIN							
R/W							
0h							

Table 14-21746. EMIF_CTLCFG_DENALI_PI_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_TDFI_PARIN_LAT	R/W	0h	Defines the DFI tPARIN_LAT timing parameter [in DFI PHY clocks], the maximum cycles between a DFI command and a dfi_parity_in signal assertion. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI PI-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit 1-0: ctrlupd_max_error, ctrlupd_interval_error. Bit 6-2: reserved. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PI_TDFI_CTRLUPD_MIN	R/W	0h	Reports the DFI tCTRLUPD_MIN timing parameter [in DFI clocks], the minimum cycles that dfi_ctrlupd_req must be asserted. Reset Source: ctl_amod_g_rst_n

14.6.6.2.601 EMIF_CTLCFG_DENALI_PI_105 Register

1 EMIF_CTLCFG_DENALI_PI_105 Register (Offset = 21A4h) [reset = 0h]

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Table 14-21747. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1A4h**

Figure 14-7214. EMIF_CTLCFG_DENALI_PI_105 Name Register

31	30	29	28	27	26	25	24
PI_ADDR_SPACE							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_BIST_LFSR_PATTERN_DONE
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PI_BIST_RESULT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PI_BIST_GO
NONE							R/W
0h							0h

Table 14-21749. EMIF_CTLCFG_DENALI_PI_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation. The end address of BIST is start_address+[1 shifted up by PI_ADDR_SPACE]-1. The end address should not beyond the actual memory address range. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_BIST_LFSR_PATTERN_DONE	R	0h	BIST operation lfsr pattern, data pattern 1'b0 means the data is useful,1'b1 means next pattern sequence can ingore. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_BIST_RESULT	R	0h	BIST operation status [pass/fail]. Bit [0] indicates data check status and bit [1] indicates address check status. Value of 1 is a passing result. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_BIST_GO	R/W	0h	Initiate a BIST operation. Set to 1 to trigger. Reset Source: ctl_amod_g_rst_n

14.6.6.2.602 EMIF_CTLCFG_DENALI_PI_106 Register

1 EMIF_CTLCFG_DENALI_PI_106 Register (Offset = 21A8h) [reset = 0h]

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Table 14-21750. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1A8h**

Figure 14-7215. EMIF_CTLCFG_DENALI_PI_106 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_BIST_ADDR_CHECK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_BIST_DATA_CHECK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21752. EMIF_CTLCFG_DENALI_PI_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.603 EMIF_CTLCFG_DENALI_PI_107 Register

1 EMIF_CTLCFG_DENALI_PI_107 Register (Offset = 21ACh) [reset = 0h]

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Table 14-21753. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1ACh

Figure 14-7216. EMIF_CTLCFG_DENALI_PI_107 Name Register

31	30	29	28	27	26	25	24
PI_BIST_START_ADDRESS_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_START_ADDRESS_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_START_ADDRESS_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_START_ADDRESS_0							
R/W							
0h							

Table 14-21755. EMIF_CTLCFG_DENALI_PI_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_START_ADDRESS_0	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.6.6.2.604 EMIF_CTLCFG_DENALI_PI_108 Register

1 EMIF_CTLCFG_DENALI_PI_108 Register (Offset = 21B0h) [reset = 0h]

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Table 14-21756. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1B0h**

Figure 14-7217. EMIF_CTLCFG_DENALI_PI_108 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_MBIST_INIT_PATTERN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PI_BIST_START_ADDRESS_1		
NONE					R/W		
0h					0h		

Table 14-21758. EMIF_CTLCFG_DENALI_PI_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_MBIST_INIT_PATTERN	R/W	0h	PI mbist data check, random lfsr pattern mode init pattern seed. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.6.6.2.605 EMIF_CTLCFG_DENALI_PI_109 Register

1 EMIF_CTLCFG_DENALI_PI_109 Register (Offset = 21B4h) [reset = 0h]

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Table 14-21759. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1B4h**

Figure 14-7218. EMIF_CTLCFG_DENALI_PI_109 Name Register

31	30	29	28	27	26	25	24
PI_BIST_DATA_MASK_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_DATA_MASK_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_DATA_MASK_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_DATA_MASK_0							
R/W							
0h							

Table 14-21761. EMIF_CTLCFG_DENALI_PI_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_DATA_MASK_0	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. The mask range is the data transfer size in each memory clock cycle [The data on a rising edge and a failing edge]. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.6.6.2.606 EMIF_CTLCFG_DENALI_PI_110 Register

1 EMIF_CTLCFG_DENALI_PI_110 Register (Offset = 21B8h) [reset = 0h]

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Table 14-21762. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1B8h**

Figure 14-7219. EMIF_CTLCFG_DENALI_PI_110 Name Register

31	30	29	28	27	26	25	24
PI_BIST_DATA_MASK_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_DATA_MASK_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_DATA_MASK_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_DATA_MASK_1							
R/W							
0h							

Table 14-21764. EMIF_CTLCFG_DENALI_PI_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_DATA_MASK_1	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. The mask range is the data transfer size in each memory clock cycle [The data on a rising edge and a failing edge]. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.6.6.2.607 EMIF_CTLCFG_DENALI_PI_111 Register

1 EMIF_CTLCFG_DENALI_PI_111 Register (Offset = 21BCh) [reset = 0h]

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Table 14-21765. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1BCh**

Figure 14-7220. EMIF_CTLCFG_DENALI_PI_111 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_BIST_ERR_STOP			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_ERR_STOP							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_BIST_ERR_COUNT			
NONE				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_ERR_COUNT							
R							
0h							

Table 14-21767. EMIF_CTLCFG_DENALI_PI_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is set to 1, 2 or 3. A value of 0 will allow the test to run to completion. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is set to 1, 2 or 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.608 EMIF_CTLCFG_DENALI_PI_112 Register

1 EMIF_CTLCFG_DENALI_PI_112 Register (Offset = 21C0h) [reset = 0h]

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Table 14-21768. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1C0h**

Figure 14-7221. EMIF_CTLCFG_DENALI_PI_112 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							

Table 14-21770. EMIF_CTLCFG_DENALI_PI_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_0_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.609 EMIF_CTLCFG_DENALI_PI_113 Register

1 EMIF_CTLCFG_DENALI_PI_113 Register (Offset = 21C4h) [reset = 0h]

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Table 14-21771. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1C4h**

Figure 14-7222. EMIF_CTLCFG_DENALI_PI_113 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_0_1			
NONE				R/W			
0h				0h			

Table 14-21773. EMIF_CTLCFG_DENALI_PI_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_0_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.610 EMIF_CTLCFG_DENALI_PI_114 Register

1 EMIF_CTLCFG_DENALI_PI_114 Register (Offset = 21C8h) [reset = 0h]

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Table 14-21774. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1C8h

Figure 14-7223. EMIF_CTLCFG_DENALI_PI_114 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							

Table 14-21776. EMIF_CTLCFG_DENALI_PI_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_1_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.611 EMIF_CTLCFG_DENALI_PI_115 Register

1 EMIF_CTLCFG_DENALI_PI_115 Register (Offset = 21CCh) [reset = 0h]

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Table 14-21777. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1CCh

Figure 14-7224. EMIF_CTLCFG_DENALI_PI_115 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_BIST_ADDR_MASK_1_1			
NONE				R/W			
0h				0h			

Table 14-21779. EMIF_CTLCFG_DENALI_PI_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_1_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.612 EMIF_CTLCFG_DENALI_PI_116 Register

1 EMIF_CTLCFG_DENALI_PI_116 Register (Offset = 21D0h) [reset = 0h]

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Table 14-21780. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1D0h**

Figure 14-7225. EMIF_CTLCFG_DENALI_PI_116 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							

Table 14-21782. EMIF_CTLCFG_DENALI_PI_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_2_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.613 EMIF_CTLCFG_DENALI_PI_117 Register

1 EMIF_CTLCFG_DENALI_PI_117 Register (Offset = 21D4h) [reset = 0h]

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Table 14-21783. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1D4h**

Figure 14-7226. EMIF_CTLCFG_DENALI_PI_117 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_2_1			
NONE				R/W			
0h				0h			

Table 14-21785. EMIF_CTLCFG_DENALI_PI_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_2_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.614 EMIF_CTLCFG_DENALI_PI_118 Register

1 EMIF_CTLCFG_DENALI_PI_118 Register (Offset = 21D8h) [reset = 0h]

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Table 14-21786. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1D8h**

Figure 14-7227. EMIF_CTLCFG_DENALI_PI_118 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							

Table 14-21788. EMIF_CTLCFG_DENALI_PI_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_3_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.615 EMIF_CTLCFG_DENALI_PI_119 Register

1 EMIF_CTLCFG_DENALI_PI_119 Register (Offset = 21DCh) [reset = 0h]

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Table 14-21789. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1DCh

Figure 14-7228. EMIF_CTLCFG_DENALI_PI_119 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_BIST_ADDR_MASK_3_1			
NONE				R/W			
0h				0h			

Table 14-21791. EMIF_CTLCFG_DENALI_PI_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_3_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.616 EMIF_CTLCFG_DENALI_PI_120 Register

1 EMIF_CTLCFG_DENALI_PI_120 Register (Offset = 21E0h) [reset = 0h]

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Table 14-21792. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1E0h**

Figure 14-7229. EMIF_CTLCFG_DENALI_PI_120 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							

Table 14-21794. EMIF_CTLCFG_DENALI_PI_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_4_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.617 EMIF_CTLCFG_DENALI_PI_121 Register

1 EMIF_CTLCFG_DENALI_PI_121 Register (Offset = 21E4h) [reset = 0h]

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Table 14-21795. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1E4h

Figure 14-7230. EMIF_CTLCFG_DENALI_PI_121 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_4_1			
NONE				R/W			
0h				0h			

Table 14-21797. EMIF_CTLCFG_DENALI_PI_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_4_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.618 EMIF_CTLCFG_DENALI_PI_122 Register

1 EMIF_CTLCFG_DENALI_PI_122 Register (Offset = 21E8h) [reset = 0h]

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Table 14-21798. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1E8h**

Figure 14-7231. EMIF_CTLCFG_DENALI_PI_122 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							

Table 14-21800. EMIF_CTLCFG_DENALI_PI_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_5_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.619 EMIF_CTLCFG_DENALI_PI_123 Register

1 EMIF_CTLCFG_DENALI_PI_123 Register (Offset = 21ECh) [reset = 0h]

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Table 14-21801. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1ECh**

Figure 14-7232. EMIF_CTLCFG_DENALI_PI_123 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_5_1			
NONE				R/W			
0h				0h			

Table 14-21803. EMIF_CTLCFG_DENALI_PI_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_5_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.620 EMIF_CTLCFG_DENALI_PI_124 Register

1 EMIF_CTLCFG_DENALI_PI_124 Register (Offset = 21F0h) [reset = 0h]

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Table 14-21804. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1F0h**

Figure 14-7233. EMIF_CTLCFG_DENALI_PI_124 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							

Table 14-21806. EMIF_CTLCFG_DENALI_PI_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_6_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.621 EMIF_CTLCFG_DENALI_PI_125 Register

1 EMIF_CTLCFG_DENALI_PI_125 Register (Offset = 21F4h) [reset = 0h]

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Table 14-21807. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1F4h

Figure 14-7234. EMIF_CTLCFG_DENALI_PI_125 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_6_1			
NONE				R/W			
0h				0h			

Table 14-21809. EMIF_CTLCFG_DENALI_PI_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_6_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.622 EMIF_CTLCFG_DENALI_PI_126 Register

1 EMIF_CTLCFG_DENALI_PI_126 Register (Offset = 21F8h) [reset = 0h]

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Table 14-21810. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A1F8h**

Figure 14-7235. EMIF_CTLCFG_DENALI_PI_126 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_BIST_ADDR_MASK_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_BIST_ADDR_MASK_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_BIST_ADDR_MASK_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_BIST_ADDR_MASK_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21812. EMIF_CTLCFG_DENALI_PI_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_7_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.623 EMIF_CTLCFG_DENALI_PI_127 Register

1 EMIF_CTLCFG_DENALI_PI_127 Register (Offset = 21FCh) [reset = 0h]

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Table 14-21813. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A1FCh

Figure 14-7236. EMIF_CTLCFG_DENALI_PI_127 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_7_1			
NONE				R/W			
0h				0h			

Table 14-21815. EMIF_CTLCFG_DENALI_PI_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_7_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.624 EMIF_CTLCFG_DENALI_PI_128 Register

1 EMIF_CTLCFG_DENALI_PI_128 Register (Offset = 2200h) [reset = 0h]

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Table 14-21816. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A200h**

Figure 14-7237. EMIF_CTLCFG_DENALI_PI_128 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							

Table 14-21818. EMIF_CTLCFG_DENALI_PI_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_8_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.625 EMIF_CTLCFG_DENALI_PI_129 Register

1 EMIF_CTLCFG_DENALI_PI_129 Register (Offset = 2204h) [reset = 0h]

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Table 14-21819. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A204h**

Figure 14-7238. EMIF_CTLCFG_DENALI_PI_129 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_8_1			
NONE				R/W			
0h				0h			

Table 14-21821. EMIF_CTLCFG_DENALI_PI_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PI_BIST_ADDR_MASK_8_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.626 EMIF_CTLCFG_DENALI_PI_130 Register

1 EMIF_CTLCFG_DENALI_PI_130 Register (Offset = 2208h) [reset = 0h]

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Table 14-21822. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A208h

Figure 14-7239. EMIF_CTLCFG_DENALI_PI_130 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							

Table 14-21824. EMIF_CTLCFG_DENALI_PI_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_9_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.627 EMIF_CTLCFG_DENALI_PI_131 Register

1 EMIF_CTLCFG_DENALI_PI_131 Register (Offset = 220Ch) [reset = 0h]

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Table 14-21825. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A20Ch**

Figure 14-7240. EMIF_CTLCFG_DENALI_PI_131 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_BIST_PAT_MODE	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_BIST_ADDR_MODE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED					PI_BIST_MODE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_9_1			
NONE				R/W			
0h				0h			

Table 14-21827. EMIF_CTLCFG_DENALI_PI_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_BIST_PAT_MODE	R/W	0h	Sets the pattern mode of BIST. 'b00 indicates using built-in pattern. 'b01 indicates checkerboard pattern, each data transfer inverts the last data transfer based on the built-in pattern. 'b10 indicates using both user pattern and built-in pattern. 'b11 indicates using pi lfsr random pattern. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_BIST_ADDR_MODE	R/W	0h	Sets the address traversing order of BIST. 'b00 indicates fast column order [burst-column-bank-row-rank]. 'b01 indicates fast row order [burst-row-column-bank-rank]. 'b10 indicates fast bank order [burst-bank-column-row-rank]. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_BIST_MODE	R/W	0h	Sets the BIST data checking mode. 'b00 indicates MOVI13N mode. 'b01 indicates March C mode. 'b10 indicates GALPAT mode. 'b11 indicates PRBS mode. 'b100 indicates programmable March data check mode. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-21827. EMIF_CTLCFG_DENALI_PI_131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PI_BIST_ADDR_MASK_9_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.6.6.2.628 EMIF_CTLCFG_DENALI_PI_132 Register

1 EMIF_CTLCFG_DENALI_PI_132 Register (Offset = 2210h) [reset = 0h]

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Table 14-21828. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A210h**

Figure 14-7241. EMIF_CTLCFG_DENALI_PI_132 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_USER_PAT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_USER_PAT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_0							
R/W							
0h							

Table 14-21830. EMIF_CTLCFG_DENALI_PI_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_0	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.6.6.2.629 EMIF_CTLCFG_DENALI_PI_133 Register

1 EMIF_CTLCFG_DENALI_PI_133 Register (Offset = 2214h) [reset = 0h]

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Table 14-21831. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A214h**

Figure 14-7242. EMIF_CTLCFG_DENALI_PI_133 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_USER_PAT_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_USER_PAT_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_USER_PAT_1							
R/W							
0h							

Table 14-21833. EMIF_CTLCFG_DENALI_PI_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_1	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.6.6.2.630 EMIF_CTLCFG_DENALI_PI_134 Register

1 EMIF_CTLCFG_DENALI_PI_134 Register (Offset = 2218h) [reset = 0h]

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Table 14-21834. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A218h**

Figure 14-7243. EMIF_CTLCFG_DENALI_PI_134 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_USER_PAT_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_USER_PAT_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_2							
R/W							
0h							

Table 14-21836. EMIF_CTLCFG_DENALI_PI_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_2	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.6.6.2.631 EMIF_CTLCFG_DENALI_PI_135 Register

1 EMIF_CTLCFG_DENALI_PI_135 Register (Offset = 221Ch) [reset = 0h]

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Table 14-21837. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A21Ch

Figure 14-7244. EMIF_CTLCFG_DENALI_PI_135 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_USER_PAT_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_USER_PAT_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_3							
R/W							
0h							

Table 14-21839. EMIF_CTLCFG_DENALI_PI_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_3	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.6.6.2.632 EMIF_CTLCFG_DENALI_PI_136 Register

1 EMIF_CTLCFG_DENALI_PI_136 Register (Offset = 2220h) [reset = 0h]

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Table 14-21840. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A220h**

Figure 14-7245. EMIF_CTLCFG_DENALI_PI_136 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PI_BIST_PAT_NUM						
NONE	R/W						
0h	0h						

Table 14-21842. EMIF_CTLCFG_DENALI_PI_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PI_BIST_PAT_NUM	R/W	0h	Sets the max used pattern number of BIST from a total of 8 built-in patterns. Ex. set to 3, The BIST would use pattern 1, 2 and 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.633 EMIF_CTLCFG_DENALI_PI_137 Register

1 EMIF_CTLCFG_DENALI_PI_137 Register (Offset = 2224h) [reset = 0h]

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Table 14-21843. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A224h**

Figure 14-7246. EMIF_CTLCFG_DENALI_PI_137 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_0							
R/W							
0h							

Table 14-21845. EMIF_CTLCFG_DENALI_PI_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_0	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.634 EMIF_CTLCFG_DENALI_PI_138 Register

1 EMIF_CTLCFG_DENALI_PI_138 Register (Offset = 2228h) [reset = 0h]

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Table 14-21846. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A228h**

Figure 14-7247. EMIF_CTLCFG_DENALI_PI_138 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_STAGE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_STAGE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_STAGE_1							
R/W							
0h							

Table 14-21848. EMIF_CTLCFG_DENALI_PI_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_1	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.635 EMIF_CTLCFG_DENALI_PI_139 Register

1 EMIF_CTLCFG_DENALI_PI_139 Register (Offset = 222Ch) [reset = 0h]

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Table 14-21849. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A22Ch

Figure 14-7248. EMIF_CTLCFG_DENALI_PI_139 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_2							
R/W							
0h							

Table 14-21851. EMIF_CTLCFG_DENALI_PI_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_2	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.636 EMIF_CTLCFG_DENALI_PI_140 Register

1 EMIF_CTLCFG_DENALI_PI_140 Register (Offset = 2230h) [reset = 0h]

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Table 14-21852. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A230h**

Figure 14-7249. EMIF_CTLCFG_DENALI_PI_140 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_3					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_3							
R/W							
0h							

Table 14-21854. EMIF_CTLCFG_DENALI_PI_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_3	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.637 EMIF_CTLCFG_DENALI_PI_141 Register

1 EMIF_CTLCFG_DENALI_PI_141 Register (Offset = 2234h) [reset = 0h]

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Table 14-21855. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A234h**

Figure 14-7250. EMIF_CTLCFG_DENALI_PI_141 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_4					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_4							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_4							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_4							
R/W							
0h							

Table 14-21857. EMIF_CTLCFG_DENALI_PI_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_4	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.638 EMIF_CTLCFG_DENALI_PI_142 Register

1 EMIF_CTLCFG_DENALI_PI_142 Register (Offset = 2238h) [reset = 0h]

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Table 14-21858. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A238h**

Figure 14-7251. EMIF_CTLCFG_DENALI_PI_142 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_5					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_STAGE_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_STAGE_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_STAGE_5							
R/W							
0h							

Table 14-21860. EMIF_CTLCFG_DENALI_PI_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_5	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.639 EMIF_CTLCFG_DENALI_PI_143 Register

1 EMIF_CTLCFG_DENALI_PI_143 Register (Offset = 223Ch) [reset = 0h]

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Table 14-21861. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A23Ch**

Figure 14-7252. EMIF_CTLCFG_DENALI_PI_143 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_6					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_6							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_6							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_6							
R/W							
0h							

Table 14-21863. EMIF_CTLCFG_DENALI_PI_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_6	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.640 EMIF_CTLCFG_DENALI_PI_144 Register

1 EMIF_CTLCFG_DENALI_PI_144 Register (Offset = 2240h) [reset = 0h]

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Table 14-21864. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A240h**

Figure 14-7253. EMIF_CTLCFG_DENALI_PI_144 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_7					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_7							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_7							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_7							
R/W							
0h							

Table 14-21866. EMIF_CTLCFG_DENALI_PI_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_7	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.641 EMIF_CTLCFG_DENALI_PI_145 Register

1 EMIF_CTLCFG_DENALI_PI_145 Register (Offset = 2244h) [reset = 0h]

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Table 14-21867. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A244h**

Figure 14-7254. EMIF_CTLCFG_DENALI_PI_145 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SELF_REFRESH_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_CRC_CALC
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_BG_ROTATE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PI_COL_DIFF			
NONE				R/W			
0h				0h			

Table 14-21869. EMIF_CTLCFG_DENALI_PI_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SELF_REFRESH_EN	R/W	0h	Control for PI to enable self refresh mode. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CRC_CALC	R/W	0h	Defines where CRC is performed; set to 1 for PI responsibility or clear to 0 for PHY responsibility. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_BG_ROTATE_EN	R/W	0h	Enable bank group rotation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_COL_DIFF	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n

14.6.6.2.642 EMIF_CTLCFG_DENALI_PI_146 Register

1 EMIF_CTLCFG_DENALI_PI_146 Register (Offset = 2248h) [reset = 0h]

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Table 14-21870. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A248h

Figure 14-7255. EMIF_CTLCFG_DENALI_PI_146 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SREF_ENTRY_REQ
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SREFRESH_EXIT_NO_REFRESH
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_MC_PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h

Table 14-21872. EMIF_CTLCFG_DENALI_PI_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SREF_ENTRY_REQ	W	0h	In PI power up data retention, PI can issued sref entry command. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SREFRESH_EXIT_NO_REFRESH	R/W	0h	Disables the automatic refresh request associated with self-refresh exit. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_PWRUP_SREFRESH_EXIT	R/W	0h	PI control powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-21872. EMIF_CTLCFG_DENALI_PI_146 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PI_MC_PWRUP_SREFRESH_EXIT	R/W	0h	It indicates MC control powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.643 EMIF_CTLCFG_DENALI_PI_147 Register

1 EMIF_CTLCFG_DENALI_PI_147 Register (Offset = 224Ch) [reset = 0h]

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Table 14-21873. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A24Ch

Figure 14-7256. EMIF_CTLCFG_DENALI_PI_147 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_AUTO_MRR_INIT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_NO_PHY_IND_TRAIN_INIT
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_NO_MRW_INIT
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_NO_MRW_BT_INIT
NONE							R/W
0h							0h

Table 14-21875. EMIF_CTLCFG_DENALI_PI_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_NO_PHY_IND_TRAIN_INIT	R/W	0h	Disable PHY Independent Training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_NO_MRW_INIT	R/W	0h	Disable MRW commands after training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_NO_MRW_BT_INIT	R/W	0h	Disable MRW commands before training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.644 EMIF_CTLCFG_DENALI_PI_148 Register

1 EMIF_CTLCFG_DENALI_PI_148 Register (Offset = 2250h) [reset = 0h]

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Table 14-21876. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A250h**

Figure 14-7257. EMIF_CTLCFG_DENALI_PI_148 Name Register

31	30	29	28	27	26	25	24
PI_TRST_PWRON							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TRST_PWRON							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TRST_PWRON							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TRST_PWRON							
R/W							
0h							

Table 14-21878. EMIF_CTLCFG_DENALI_PI_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.645 EMIF_CTLCFG_DENALI_PI_149 Register

1 EMIF_CTLCFG_DENALI_PI_149 Register (Offset = 2254h) [reset = 0h]

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Table 14-21879. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A254h**

Figure 14-7258. EMIF_CTLCFG_DENALI_PI_149 Name Register

31	30	29	28	27	26	25	24
PI_CKE_INACTIVE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_CKE_INACTIVE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_CKE_INACTIVE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_CKE_INACTIVE							
R/W							
0h							

Table 14-21881. EMIF_CTLCFG_DENALI_PI_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active. Reset Source: ctl_amod_g_rst_n

14.6.6.2.646 EMIF_CTLCFG_DENALI_PI_150 Register

1 EMIF_CTLCFG_DENALI_PI_150 Register (Offset = 2258h) [reset = 0h]

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Table 14-21882. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A258h**

Figure 14-7259. EMIF_CTLCFG_DENALI_PI_150 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_DLL_RST_DELAY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_DLL_RST_DELAY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_DRAM_INIT_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_DLL_RST</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21884. EMIF_CTLCFG_DENALI_PI_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DRAM_INIT_EN	R/W	0h	Control for the initialization of DRAM by the PI. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DLL_RST	R/W	0h	Enables use of the DLL reset [dll_rst_n]. Reset Source: ctl_amod_g_rst_n

14.6.6.2.647 EMIF_CTLCFG_DENALI_PI_151 Register

1 EMIF_CTLCFG_DENALI_PI_151 Register (Offset = 225Ch) [reset = 0h]

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Table 14-21885. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A25Ch

Figure 14-7260. EMIF_CTLCFG_DENALI_PI_151 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_DLL_RST_ADJ_DLY							
R/W							
0h							

Table 14-21887. EMIF_CTLCFG_DENALI_PI_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting controller delay in DLL until the DLL reset signal dll_rst_n may be asserted. Reset Source: ctl_amod_g_rst_n

14.6.6.2.648 EMIF_CTLCFG_DENALI_PI_152 Register

1 EMIF_CTLCFG_DENALI_PI_152 Register (Offset = 2260h) [reset = 0h]

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Table 14-21888. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A260h**

Figure 14-7261. EMIF_CTLCFG_DENALI_PI_152 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_WRITE_MODEREG	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_WRITE_MODEREG							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_WRITE_MODEREG							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WRITE_MODEREG							
R/W							
0h							

Table 14-21890. EMIF_CTLCFG_DENALI_PI_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PI_WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits [7:0] define the memory mode register number if bit [23] is set, bits [15:8] define the chip select if bit [24] is clear, bits [23:16] define which memory mode register/s to write, bit [24] defines whether all chip selects will be written, and bit [25] triggers the write. Reset Source: ctl_amod_g_rst_n

14.6.6.2.649 EMIF_CTLCFG_DENALI_PI_153 Register

1 EMIF_CTLCFG_DENALI_PI_153 Register (Offset = 2264h) [reset = 0h]

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Table 14-21891. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A264h**

Figure 14-7262. EMIF_CTLCFG_DENALI_PI_153 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED 27
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_MRW_STATUS							
R							
0h							

Table 14-21893. EMIF_CTLCFG_DENALI_PI_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED27	R/W	0h	Reserved
7:0	PI_MRW_STATUS	R	0h	Write memory mode register status. Bit [0] set indicates a WRITE_MODEREG parameter programming error. Bit [1] set indicates a PASR error. Bit [2] is Reserved. Bit [3] set indicates a self refresh or deep power down error. Bit [4] set indicates that a write to MR3 or MR11 was attempted [write_modereg bit [25] was asserted with bit [17] set, or bit [23] was asserted with bits [7:0] defining MR3 or MR11] during tZQCAL after a ZQ calibration start command. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.650 EMIF_CTLCFG_DENALI_PI_154 Register

1 EMIF_CTLCFG_DENALI_PI_154 Register (Offset = 2268h) [reset = 0h]

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Table 14-21894. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A268h**

Figure 14-7263. EMIF_CTLCFG_DENALI_PI_154 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_READ_MODEREG
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_READ_MODEREG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_READ_MODEREG							
R/W							
0h							

Table 14-21896. EMIF_CTLCFG_DENALI_PI_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits [7:0] define the memory mode register and bits [15:8] define the chip select. Set bit [16] to 1 to trigger. Reset Source: ctl_amod_g_rst_n

14.6.6.2.651 EMIF_CTLCFG_DENALI_PI_155 Register

1 EMIF_CTLCFG_DENALI_PI_155 Register (Offset = 226Ch) [reset = 0h]

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Table 14-21897. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A26Ch

Figure 14-7264. EMIF_CTLCFG_DENALI_PI_155 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_ZQ_INIT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_PERIPHERAL_MRR_DATA_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_PERIPHERAL_MRR_DATA_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_PERIPHERAL_MRR_DATA_0							
R							
0h							

Table 14-21899. EMIF_CTLCFG_DENALI_PI_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:0	PI_PERIPHERAL_MRR_DATA_0	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter, Bits [15:0] define MRR data, [23:16] define the chip select. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.652 EMIF_CTLCFG_DENALI_PI_156 Register

1 EMIF_CTLCFG_DENALI_PI_156 Register (Offset = 2270h) [reset = 0h]

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Table 14-21900. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A270h**

Figure 14-7265. EMIF_CTLCFG_DENALI_PI_156 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RESERVED30</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_ZQ_REQ_PENDING</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED29</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED28</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-21902. EMIF_CTLCFG_DENALI_PI_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED30	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED29	W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED28	R/W	0h	Reserved

14.6.6.2.653 EMIF_CTLCFG_DENALI_PI_157 Register

1 EMIF_CTLCFG_DENALI_PI_157 Register (Offset = 2274h) [reset = 0h]

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Table 14-21903. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A274h**

Figure 14-7266. EMIF_CTLCFG_DENALI_PI_157 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MONITOR_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MONITOR_CAP_SEL_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_MONITOR_SRC_SEL_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PI_RESERVED31</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-21905. EMIF_CTLCFG_DENALI_PI_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MONITOR_0	R	0h	Monitor register 0. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_MONITOR_CAP_SEL_0	R/W	0h	Selection of captures for pi_monitor_0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_MONITOR_SRC_SEL_0	R/W	0h	Selection of sources for pi_monitor_0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_RESERVED31	R/W	0h	Reserved

14.6.6.2.654 EMIF_CTLCFG_DENALI_PI_158 Register

1 EMIF_CTLCFG_DENALI_PI_158 Register (Offset = 2278h) [reset = 0h]

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Table 14-21906. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A278h

Figure 14-7267. EMIF_CTLCFG_DENALI_PI_158 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_2			
NONE				R/W			
0h				0h			

23	22	21	20	19	18	17	16
PI_MONITOR_1							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							PI_MONITOR_CAP_SEL_1
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED				PI_MONITOR_SRC_SEL_1			
NONE				R/W			
0h				0h			

Table 14-21908. EMIF_CTLCFG_DENALI_PI_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_MONITOR_SRC_SEL_2	R/W	0h	Selection of sources for pi_monitor_2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MONITOR_1	R	0h	Monitor register 1. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MONITOR_CAP_SEL_1	R/W	0h	Selection of captures for pi_monitor_1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_MONITOR_SRC_SEL_1	R/W	0h	Selection of sources for pi_monitor_1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.655 EMIF_CTLCFG_DENALI_PI_159 Register

1 EMIF_CTLCFG_DENALI_PI_159 Register (Offset = 227Ch) [reset = 0h]

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Table 14-21909. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A27Ch**

Figure 14-7268. EMIF_CTLCFG_DENALI_PI_159 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MONITOR_CAP_SEL_3
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PI_MONITOR_SRC_SEL_3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_MONITOR_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							PI_MONITOR_CAP_SEL_2
NONE							R/W
0h							0h

Table 14-21911. EMIF_CTLCFG_DENALI_PI_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MONITOR_CAP_SEL_3	R/W	0h	Selection of captures for pi_monitor_3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_MONITOR_SRC_SEL_3	R/W	0h	Selection of sources for pi_monitor_3. Reset Source: ctl_amod_g_rst_n
15:8	PI_MONITOR_2	R	0h	Monitor register 2. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_MONITOR_CAP_SEL_2	R/W	0h	Selection of captures for pi_monitor_2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.656 EMIF_CTLCFG_DENALI_PI_160 Register

1 EMIF_CTLCFG_DENALI_PI_160 Register (Offset = 2280h) [reset = 0h]

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Table 14-21912. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A280h**

Figure 14-7269. EMIF_CTLCFG_DENALI_PI_160 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MONITOR_4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MONITOR_CAP_SEL_4</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_MONITOR_SRC_SEL_4</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MONITOR_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21914. EMIF_CTLCFG_DENALI_PI_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MONITOR_4	R	0h	Monitor register 4. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_MONITOR_CAP_SEL_4	R/W	0h	Selection of captures for pi_monitor_4. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_MONITOR_SRC_SEL_4	R/W	0h	Selection of sources for pi_monitor_4. Reset Source: ctl_amod_g_rst_n
7:0	PI_MONITOR_3	R	0h	Monitor register 3. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.657 EMIF_CTLCFG_DENALI_PI_161 Register

1 EMIF_CTLCFG_DENALI_PI_161 Register (Offset = 2284h) [reset = 0h]

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Table 14-21915. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A284h

Figure 14-7270. EMIF_CTLCFG_DENALI_PI_161 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_6			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MONITOR_5							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_MONITOR_CAP_SEL_5
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_MONITOR_SRC_SEL_5			
NONE				R/W			
0h				0h			

Table 14-21917. EMIF_CTLCFG_DENALI_PI_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_MONITOR_SRC_SEL_6	R/W	0h	Selection of sources for pi_monitor_6. Reset Source: ctl_amod_g_rst_n
23:16	PI_MONITOR_5	R	0h	Monitor register 5. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MONITOR_CAP_SEL_5	R/W	0h	Selection of captures for pi_monitor_5. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_MONITOR_SRC_SEL_5	R/W	0h	Selection of sources for pi_monitor_5. Reset Source: ctl_amod_g_rst_n

14.6.6.2.658 EMIF_CTLCFG_DENALI_PI_162 Register

1 EMIF_CTLCFG_DENALI_PI_162 Register (Offset = 2288h) [reset = 0h]

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Table 14-21918. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A288h**

Figure 14-7271. EMIF_CTLCFG_DENALI_PI_162 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MONITOR_CAP_SEL_7
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PI_MONITOR_SRC_SEL_7			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_MONITOR_6							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							PI_MONITOR_CAP_SEL_6
NONE							R/W
0h							0h

Table 14-21920. EMIF_CTLCFG_DENALI_PI_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MONITOR_CAP_SEL_7	R/W	0h	Selection of captures for pi_monitor_7. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_MONITOR_SRC_SEL_7	R/W	0h	Selection of sources for pi_monitor_7. Reset Source: ctl_amod_g_rst_n
15:8	PI_MONITOR_6	R	0h	Monitor register 6. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_MONITOR_CAP_SEL_6	R/W	0h	Selection of captures for pi_monitor_6. Reset Source: ctl_amod_g_rst_n

14.6.6.2.659 EMIF_CTLCFG_DENALI_PI_163 Register

1 EMIF_CTLCFG_DENALI_PI_163 Register (Offset = 228Ch) [reset = 0h]

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Table 14-21921. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A28Ch

Figure 14-7272. EMIF_CTLCFG_DENALI_PI_163 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_MONITOR_7							
R							
0h							

Table 14-21923. EMIF_CTLCFG_DENALI_PI_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_MONITOR_7	R	0h	Monitor register 7. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.660 EMIF_CTLCFG_DENALI_PI_164 Register

1 EMIF_CTLCFG_DENALI_PI_164 Register (Offset = 2290h) [reset = 0h]

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Table 14-21924. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A290h**

Figure 14-7273. EMIF_CTLCFG_DENALI_PI_164 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_MONITOR_STROBE							
W							
0h							

Table 14-21926. EMIF_CTLCFG_DENALI_PI_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_MONITOR_STROBE	W	0h	Strobe the pi_monitor once. Every bit corresponds respectively with a pi_monitor. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.661 EMIF_CTLCFG_DENALI_PI_165 Register

1 EMIF_CTLCFG_DENALI_PI_165 Register (Offset = 2294h) [reset = 0h]

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Table 14-21927. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A294h**

Figure 14-7274. EMIF_CTLCFG_DENALI_PI_165 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED32
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_FREQ_RETENTION_NUM				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_FREQ_NUMBER_STATUS				
NONE			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_DLL_LOCK
NONE							R
0h							0h

Table 14-21929. EMIF_CTLCFG_DENALI_PI_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED32	R/W	0h	Reserved
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_FREQ_RETENTION_NUM	R/W	0h	Monitor active freq number in PI for data_retention Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_FREQ_NUMBER_STATUS	R	0h	Monitor active freq number in PI. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DLL_LOCK	R	0h	Monitor dfi_init_complete from PHY. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.662 EMIF_CTLCFG_DENALI_PI_166 Register

1 EMIF_CTLCFG_DENALI_PI_166 Register (Offset = 2298h) [reset = 0h]

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Table 14-21930. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A298h**

Figure 14-7275. EMIF_CTLCFG_DENALI_PI_166 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED34
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_POWER_REDUC_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_RESERVED33
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_PHYMSTR_TYPE	
NONE						R/W	
0h						0h	

Table 14-21932. EMIF_CTLCFG_DENALI_PI_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED34	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_POWER_REDUC_EN	R/W	0h	PI Power reduction enable, 1 = enabled. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED33	R/W	0h	Reserved
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_PHYMSTR_TYPE	R/W	0h	Defines how the controller should set the state of DRAM before turning control of the DFI bus over to the PI. Reset Source: ctl_amod_g_rst_n

14.6.6.2.663 EMIF_CTLCFG_DENALI_PI_167 Register

1 EMIF_CTLCFG_DENALI_PI_167 Register (Offset = 229Ch) [reset = 0h]

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Table 14-21933. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A29Ch**

Figure 14-7276. EMIF_CTLCFG_DENALI_PI_167 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED38
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED37
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED36
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED35
NONE							R/W
0h							0h

Table 14-21935. EMIF_CTLCFG_DENALI_PI_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED38	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED37	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED36	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED35	R/W	0h	Reserved

14.6.6.2.664 EMIF_CTLCFG_DENALI_PI_168 Register

1 EMIF_CTLCFG_DENALI_PI_168 Register (Offset = 22A0h) [reset = 0h]

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Table 14-21936. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2A0h**

Figure 14-7277. EMIF_CTLCFG_DENALI_PI_168 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED42
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_RESERVED41
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_RESERVED40
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_RESERVED39
NONE							R/W
0h							0h

Table 14-21938. EMIF_CTLCFG_DENALI_PI_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED42	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED41	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED40	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED39	R/W	0h	Reserved

14.6.6.2.665 EMIF_CTLCFG_DENALI_PI_169 Register

1 EMIF_CTLCFG_DENALI_PI_169 Register (Offset = 22A4h) [reset = 0h]

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Table 14-21939. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2A4h

Figure 14-7278. EMIF_CTLCFG_DENALI_PI_169 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED46
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED45
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED44
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED43
NONE							R/W
0h							0h

Table 14-21941. EMIF_CTLCFG_DENALI_PI_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED46	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED45	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED44	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED43	R/W	0h	Reserved

14.6.6.2.666 EMIF_CTLCFG_DENALI_PI_170 Register

1 EMIF_CTLCFG_DENALI_PI_170 Register (Offset = 22A8h) [reset = 0h]

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Table 14-21942. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2A8h**

Figure 14-7279. EMIF_CTLCFG_DENALI_PI_170 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED50
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED49
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED48
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED47
NONE							R/W
0h							0h

Table 14-21944. EMIF_CTLCFG_DENALI_PI_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED50	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED49	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED48	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED47	R/W	0h	Reserved

14.6.6.2.667 EMIF_CTLCFG_DENALI_PI_171 Register

1 EMIF_CTLCFG_DENALI_PI_171 Register (Offset = 22ACh) [reset = 0h]

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Table 14-21945. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2ACh

Figure 14-7280. EMIF_CTLCFG_DENALI_PI_171 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_WRLVL_MAX_STROBE_PEND							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_RESERVED52
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_RESERVED51
NONE							R/W
0h							0h

Table 14-21947. EMIF_CTLCFG_DENALI_PI_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_WRLVL_MAX_STROBE_PEND	R/W	0h	Defines the maximum number of wrlvl_strobes that be accumulated before an AREF is prevented from being generated. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED52	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED51	R/W	0h	Reserved

14.6.6.2.668 EMIF_CTLCFG_DENALI_PI_172 Register

1 EMIF_CTLCFG_DENALI_PI_172 Register (Offset = 22B0h) [reset = 0h]

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Table 14-21948. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2B0h**

Figure 14-7281. EMIF_CTLCFG_DENALI_PI_172 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_TREFBW_THR
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_TREFBW_THR							
R/W							
0h							

Table 14-21950. EMIF_CTLCFG_DENALI_PI_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PI_TREFBW_THR	R/W	0h	Threshold value to control the AREF command interval. When the number of pending AREF is over this value, the interval is expanded to be tREF/8. Reset Source: ctl_amod_g_rst_n

14.6.6.2.669 EMIF_CTLCFG_DENALI_PI_173 Register

1 EMIF_CTLCFG_DENALI_PI_173 Register (Offset = 22B4h) [reset = 0h]

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Table 14-21951. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2B4h**

Figure 14-7282. EMIF_CTLCFG_DENALI_PI_173 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_FREQ_CHANGE_REG_COPY				
NONE			R/W				
0h			0h				

Table 14-21953. EMIF_CTLCFG_DENALI_PI_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PI_FREQ_CHANGE_REG_COPY	R/W	0h	In non-DFI 4.0 mode, contains the frequency copy value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.670 EMIF_CTLCFG_DENALI_PI_174 Register

1 EMIF_CTLCFG_DENALI_PI_174 Register (Offset = 22B8h) [reset = 0h]

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Table 14-21954. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2B8h

Figure 14-7283. EMIF_CTLCFG_DENALI_PI_174 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_CATR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PI_PARALLEL_CALVL_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PI_RESERVED53				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							PI_FREQ_SEL_FROM_REGIF
NONE							R/W
0h							0h

Table 14-21956. EMIF_CTLCFG_DENALI_PI_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CATR	R/W	0h	It indicates LP4 DRAM CA terminition ON/OFF state. Each bit corresponds to each chip select. 1:ON 0:OFF. This parameter is active when PI_NO_CATR_READ==1. When PI_NO_CATR_READ==0, this param is inactive Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_PARALLEL_CALVL_EN	R/W	0h	Enable parallel channel CA training for LPDDR4. 1: All the channels in one rank do CA Training in parallel. 0: Each channel does CA Training in sequence Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RESERVED53	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_FREQ_SEL_FROM_REGIF	R/W	0h	In non-DFI 4.0 mode, user select the frequency copies from pi_freq_change_reg_copy. Reset Source: ctl_amod_g_rst_n

14.6.6.2.671 EMIF_CTLCFG_DENALI_PI_175 Register

1 EMIF_CTLCFG_DENALI_PI_175 Register (Offset = 22BCh) [reset = 0h]

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Table 14-21957. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2BCh

Figure 14-7284. EMIF_CTLCFG_DENALI_PI_175 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_DISABLE_PHYMSTR_REQ
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_DISCONNECT_MC
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_MASK_INIT_COMPLETE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_NO_CATR_READ
NONE							R/W
0h							0h

Table 14-21959. EMIF_CTLCFG_DENALI_PI_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_DISABLE_PHYMSTR_REQ	R/W	0h	PI mask dfi_phymstr_req to the controller and get dfi bus without dfi_phymstr_ack, 1: disconnect Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DISCONNECT_MC	R/W	0h	PI disconnects the controller from the PHY, 1: disconnect Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MASK_INIT_COMPLETE	R/W	0h	Enable the masking of the dfi_init_complete signal back to the controller, 1: mask. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_NO_CATR_READ	R/W	0h	Defines how the LPDDR4 termination status is determined. 1: PI use PI_CATR to get DRAM CA Termination status. 0: PI reads DRAM MR0.OP7 to get DRAM CA Termination status. Reset Source: ctl_amod_g_rst_n

14.6.6.2.672 EMIF_CTLCFG_DENALI_PI_176 Register

1 EMIF_CTLCFG_DENALI_PI_176 Register (Offset = 22C0h) [reset = 0h]

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Table 14-21960. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2C0h**

Figure 14-7285. EMIF_CTLCFG_DENALI_PI_176 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TVREF_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TVREF_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PI_PHYMSTR_REQ_ACK_LOOP_DELAY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_NOTCARE_MC_INIT_START</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-21962. EMIF_CTLCFG_DENALI_PI_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TVREF_F0	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_PHYMSTR_REQ_ACK_LOOP_DELAY	R/W	0h	The delay between phymstr_req and inner phymstr_ack when PI_DISABLE_PHYMSTR_REQ set 1 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_NOTCARE_MC_INIT_START	R/W	0h	Defines whether PI waits for the controller to initiate dfi_init_start before PI memory initialization, 1: wait for dfi_init_start Reset Source: ctl_amod_g_rst_n

14.6.6.2.673 EMIF_CTLCFG_DENALI_PI_177 Register

1 EMIF_CTLCFG_DENALI_PI_177 Register (Offset = 22C4h) [reset = 0h]

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Table 14-21963. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2C4h**

Figure 14-7286. EMIF_CTLCFG_DENALI_PI_177 Name Register

31	30	29	28	27	26	25	24
PI_TVREF_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TVREF_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TVREF_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TVREF_F1							
R/W							
0h							

Table 14-21965. EMIF_CTLCFG_DENALI_PI_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TVREF_F2	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:0	PI_TVREF_F1	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.674 EMIF_CTLCFG_DENALI_PI_178 Register

1 EMIF_CTLCFG_DENALI_PI_178 Register (Offset = 22C8h) [reset = 0h]

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Table 14-21966. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2C8h**

Figure 14-7287. EMIF_CTLCFG_DENALI_PI_178 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TSDO_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TSDO_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TSDO_F0							
R/W							
0h							

Table 14-21968. EMIF_CTLCFG_DENALI_PI_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_TSDO_F2	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 2, in PI clocks Reset Source: ctl_amod_g_rst_n
15:8	PI_TSDO_F1	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 1, in PI clocks Reset Source: ctl_amod_g_rst_n
7:0	PI_TSDO_F0	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 0, in PI clocks Reset Source: ctl_amod_g_rst_n

14.6.6.2.675 EMIF_CTLCFG_DENALI_PI_179 Register

1 EMIF_CTLCFG_DENALI_PI_179 Register (Offset = 22CCh) [reset = 0h]

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Table 14-21969. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2CCh**

Figure 14-7288. EMIF_CTLCFG_DENALI_PI_179 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F0							
R/W							
0h							

Table 14-21971. EMIF_CTLCFG_DENALI_PI_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F0	R/W	0h	The delay from read or write to bus idle for frequency set 0. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.6.6.2.676 EMIF_CTLCFG_DENALI_PI_180 Register

1 EMIF_CTLCFG_DENALI_PI_180 Register (Offset = 22D0h) [reset = 0h]

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Table 14-21972. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2D0h**

Figure 14-7289. EMIF_CTLCFG_DENALI_PI_180 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F1							
R/W							
0h							

Table 14-21974. EMIF_CTLCFG_DENALI_PI_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F1	R/W	0h	The delay from read or write to bus idle for frequency set 1. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.6.6.2.677 EMIF_CTLCFG_DENALI_PI_181 Register

1 EMIF_CTLCFG_DENALI_PI_181 Register (Offset = 22D4h) [reset = 0h]

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Table 14-21975. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2D4h**

Figure 14-7290. EMIF_CTLCFG_DENALI_PI_181 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_ZQINIT_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_ZQINIT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDELAY_RDWR_2_BUS_IDLE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21977. EMIF_CTLCFG_DENALI_PI_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F2	R/W	0h	The delay from read or write to bus idle for frequency set 2. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.6.6.2.678 EMIF_CTLCFG_DENALI_PI_182 Register

1 EMIF_CTLCFG_DENALI_PI_182 Register (Offset = 22D8h) [reset = 0h]

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Table 14-21978. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2D8h**

Figure 14-7291. EMIF_CTLCFG_DENALI_PI_182 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQINIT_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_ZQINIT_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_ZQINIT_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_ZQINIT_F1							
R/W							
0h							

Table 14-21980. EMIF_CTLCFG_DENALI_PI_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.679 EMIF_CTLCFG_DENALI_PI_183 Register

1 EMIF_CTLCFG_DENALI_PI_183 Register (Offset = 22DCh) [reset = 0h]

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Table 14-21981. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2DCh**

Figure 14-7292. EMIF_CTLCFG_DENALI_PI_183 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TPARITY_ERROR_CMD_INHIBIT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CA_PARITY_LAT_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_ADDITIVE_LAT_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_WRLAT_F0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-21983. EMIF_CTLCFG_DENALI_PI_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TPARITY_ERROR_CMD_INHIBIT_F0	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CA_PARITY_LAT_F0	R/W	0h	DRAM CA parity latency value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_ADDITIVE_LAT_F0	R/W	0h	DRAM additive latency value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_WRLAT_F0	R/W	0h	DRAM WRLAT value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.680 EMIF_CTLCFG_DENALI_PI_184 Register

1 EMIF_CTLCFG_DENALI_PI_184 Register (Offset = 22E0h) [reset = 0h]

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Table 14-21984. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2E0h

Figure 14-7293. EMIF_CTLCFG_DENALI_PI_184 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_CA_PARITY_LAT_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_ADDITIVE_LAT_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_WRLAT_F1</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_CASLAT_LIN_F0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-21986. EMIF_CTLCFG_DENALI_PI_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CA_PARITY_LAT_F1	R/W	0h	DRAM CA parity latency value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_ADDITIVE_LAT_F1	R/W	0h	DRAM additive latency value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_WRLAT_F1	R/W	0h	DRAM WRLAT value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CASLAT_LIN_F0	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 0. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n

14.6.6.2.681 EMIF_CTLCFG_DENALI_PI_185 Register

1 EMIF_CTLCFG_DENALI_PI_185 Register (Offset = 22E4h) [reset = 0h]

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Table 14-21987. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2E4h**

Figure 14-7294. EMIF_CTLCFG_DENALI_PI_185 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_ADDITIVE_LAT_F2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED	PI_WRLAT_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_CASLAT_LIN_F1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
PI_TPARITY_ERROR_CMD_INHIBIT_F1							
R/W							
0h							

Table 14-21989. EMIF_CTLCFG_DENALI_PI_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_ADDITIVE_LAT_F2	R/W	0h	DRAM additive latency value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WRLAT_F2	R/W	0h	DRAM WRLAT value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CASLAT_LIN_F1	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 1. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n
7:0	PI_TPARITY_ERROR_CMD_INHIBIT_F1	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.682 EMIF_CTLCFG_DENALI_PI_186 Register

1 EMIF_CTLCFG_DENALI_PI_186 Register (Offset = 22E8h) [reset = 0h]

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Table 14-21990. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2E8h**

Figure 14-7295. EMIF_CTLCFG_DENALI_PI_186 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PI_CASLAT_LIN_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
PI_TPARITY_ERROR_CMD_INHIBIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_CA_PARITY_LAT_F2			
NONE				R/W			
0h				0h			

Table 14-21992. EMIF_CTLCFG_DENALI_PI_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PI_CASLAT_LIN_F2	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 2. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n
15:8	PI_TPARITY_ERROR_CMD_INHIBIT_F2	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CA_PARITY_LAT_F2	R/W	0h	DRAM CA parity latency value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.683 EMIF_CTLCFG_DENALI_PI_187 Register

1 EMIF_CTLCFG_DENALI_PI_187 Register (Offset = 22ECh) [reset = 0h]

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Table 14-21993. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 A2ECh**

Figure 14-7296. EMIF_CTLCFG_DENALI_PI_187 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TRFC_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TRFC_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21995. EMIF_CTLCFG_DENALI_PI_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F0	R/W	0h	DRAM tRFC value in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.684 EMIF_CTLCFG_DENALI_PI_188 Register

1 EMIF_CTLCFG_DENALI_PI_188 Register (Offset = 22F0h) [reset = 0h]

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Table 14-21996. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2F0h**

Figure 14-7297. EMIF_CTLCFG_DENALI_PI_188 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TREF_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TREF_F0							
R/W							
0h							

Table 14-21998. EMIF_CTLCFG_DENALI_PI_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F0	R/W	0h	DRAM tREF value in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.685 EMIF_CTLCFG_DENALI_PI_189 Register

1 EMIF_CTLCFG_DENALI_PI_189 Register (Offset = 22F4h) [reset = 0h]

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Table 14-21999. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A2F4h

Figure 14-7298. EMIF_CTLCFG_DENALI_PI_189 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TRFC_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TRFC_F1							
R/W							
0h							

Table 14-22001. EMIF_CTLCFG_DENALI_PI_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F1	R/W	0h	DRAM tRFC value in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.686 EMIF_CTLCFG_DENALI_PI_190 Register

1 EMIF_CTLCFG_DENALI_PI_190 Register (Offset = 22F8h) [reset = 0h]

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Table 14-22002. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2F8h**

Figure 14-7299. EMIF_CTLCFG_DENALI_PI_190 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TREF_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TREF_F1							
R/W							
0h							

Table 14-22004. EMIF_CTLCFG_DENALI_PI_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F1	R/W	0h	DRAM tREF value in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.687 EMIF_CTLCFG_DENALI_PI_191 Register

1 EMIF_CTLCFG_DENALI_PI_191 Register (Offset = 22FCh) [reset = 0h]

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Table 14-22005. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A2FCh**

Figure 14-7300. EMIF_CTLCFG_DENALI_PI_191 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TRFC_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TRFC_F2							
R/W							
0h							

Table 14-22007. EMIF_CTLCFG_DENALI_PI_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F2	R/W	0h	DRAM tRFC value in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.688 EMIF_CTLCFG_DENALI_PI_192 Register

1 EMIF_CTLCFG_DENALI_PI_192 Register (Offset = 2300h) [reset = 2000000h]

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Table 14-22008. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A300h**

Figure 14-7301. EMIF_CTLCFG_DENALI_PI_192 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TDFI_CTRL_DELAY_F0			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TREF_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TREF_F2							
R/W							
0h							

Table 14-22010. EMIF_CTLCFG_DENALI_PI_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 0, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F2	R/W	0h	DRAM tREF value in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.689 EMIF_CTLCFG_DENALI_PI_193 Register

1 EMIF_CTLCFG_DENALI_PI_193 Register (Offset = 2304h) [reset = 202h]

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Table 14-22011. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A304h**

Figure 14-7302. EMIF_CTLCFG_DENALI_PI_193 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_WRLVL_EN_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_WRLVL_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CTRL_DELAY_F2			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				PI_TDFI_CTRL_DELAY_F1			
NONE				R/W			
0h				2h			

Table 14-22013. EMIF_CTLCFG_DENALI_PI_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_WRLVL_EN_F1	R/W	0h	Enable the PI write leveling module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_WRLVL_EN_F0	R/W	0h	Enable the PI write leveling module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 2, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 1, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n

14.6.6.2.690 EMIF_CTLCFG_DENALI_PI_194 Register

1 EMIF_CTLCFG_DENALI_PI_194 Register (Offset = 2308h) [reset = 0h]

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Table 14-22014. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A308h**

Figure 14-7303. EMIF_CTLCFG_DENALI_PI_194 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WRLVL_WW_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_WW_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_WRLVL_EN_F2	
NONE						R/W	
0h						0h	

Table 14-22016. EMIF_CTLCFG_DENALI_PI_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PI_TDFI_WRLVL_WW_F0	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_WRLVL_EN_F2	R/W	0h	Enable the PI write leveling module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.691 EMIF_CTLCFG_DENALI_PI_195 Register

1 EMIF_CTLCFG_DENALI_PI_195 Register (Offset = 230Ch) [reset = 0h]

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Table 14-22017. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A30Ch**

Figure 14-7304. EMIF_CTLCFG_DENALI_PI_195 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_WRLVL_WW_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_WW_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WRLVL_WW_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_WW_F1							
R/W							
0h							

Table 14-22019. EMIF_CTLCFG_DENALI_PI_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WRLVL_WW_F2	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WRLVL_WW_F1	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n

14.6.6.2.692 EMIF_CTLCFG_DENALI_PI_196 Register

1 EMIF_CTLCFG_DENALI_PI_196 Register (Offset = 2310h) [reset = 0h]

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Table 14-22020. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A310h**

Figure 14-7305. EMIF_CTLCFG_DENALI_PI_196 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_ODT_EN_F1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PI_TODTL_2CMD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_ODT_EN_F0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_TODTL_2CMD_F0							
R/W							
0h							

Table 14-22022. EMIF_CTLCFG_DENALI_PI_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.693 EMIF_CTLCFG_DENALI_PI_197 Register

1 EMIF_CTLCFG_DENALI_PI_197 Register (Offset = 2314h) [reset = 0h]

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Table 14-22023. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A314h

Figure 14-7306. EMIF_CTLCFG_DENALI_PI_197 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TODTON_MIN_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_ODTLON_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_ODT_EN_F2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TODTL_2CMD_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22025. EMIF_CTLCFG_DENALI_PI_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TODTON_MIN_F0	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODTLON_F0	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.694 EMIF_CTLCFG_DENALI_PI_198 Register

1 EMIF_CTLCFG_DENALI_PI_198 Register (Offset = 2318h) [reset = 0h]

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Table 14-22026. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A318h

Figure 14-7307. EMIF_CTLCFG_DENALI_PI_198 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TODTON_MIN_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODTLON_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TODTON_MIN_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_ODTLON_F1			
NONE				R/W			
0h				0h			

Table 14-22028. EMIF_CTLCFG_DENALI_PI_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TODTON_MIN_F2	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODTLON_F2	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TODTON_MIN_F1	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_ODTLON_F1	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.695 EMIF_CTLCFG_DENALI_PI_199 Register

1 EMIF_CTLCFG_DENALI_PI_199 Register (Offset = 231Ch) [reset = 0h]

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Table 14-22029. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A31Ch

Figure 14-7308. EMIF_CTLCFG_DENALI_PI_199 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_RD_TO_ODTH_F0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PI_WR_TO_ODTH_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		PI_WR_TO_ODTH_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PI_WR_TO_ODTH_F0					
NONE		R/W					
0h		0h					

Table 14-22031. EMIF_CTLCFG_DENALI_PI_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_RD_TO_ODTH_F0	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_WR_TO_ODTH_F2	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_WR_TO_ODTH_F1	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_WR_TO_ODTH_F0	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.696 EMIF_CTLCFG_DENALI_PI_200 Register

1 EMIF_CTLCFG_DENALI_PI_200 Register (Offset = 2320h) [reset = 0h]

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Table 14-22032. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A320h**

Figure 14-7309. EMIF_CTLCFG_DENALI_PI_200 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_GATE_EN_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED		PI_RD_TO_ODTH_F2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PI_RD_TO_ODTH_F1					
NONE		R/W					
0h		0h					

Table 14-22034. EMIF_CTLCFG_DENALI_PI_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_GATE_EN_F0	R/W	0h	Enable the PI gate training module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_EN_F0	R/W	0h	Enable the PI data eye training module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_RD_TO_ODTH_F2	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_RD_TO_ODTH_F1	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.697 EMIF_CTLCFG_DENALI_PI_201 Register

1 EMIF_CTLCFG_DENALI_PI_201 Register (Offset = 2324h) [reset = 0h]

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Table 14-22035. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A324h**

Figure 14-7310. EMIF_CTLCFG_DENALI_PI_201 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_GATE_EN_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_EN_F2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_GATE_EN_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_EN_F1	
NONE						R/W	
0h						0h	

Table 14-22037. EMIF_CTLCFG_DENALI_PI_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_GATE_EN_F2	R/W	0h	Enable the PI gate training module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_EN_F2	R/W	0h	Enable the PI data eye training module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_GATE_EN_F1	R/W	0h	Enable the PI gate training module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_EN_F1	R/W	0h	Enable the PI data eye training module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.698 EMIF_CTLCFG_DENALI_PI_202 Register

1 EMIF_CTLCFG_DENALI_PI_202 Register (Offset = 2328h) [reset = 0h]

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Table 14-22038. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A328h**

Figure 14-7311. EMIF_CTLCFG_DENALI_PI_202 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TWR_MPR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TWR_MPR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TWR_MPR_F0							
R/W							
0h							

Table 14-22040. EMIF_CTLCFG_DENALI_PI_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F0	R/W	0h	Enable PATTERN-0 for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:16	PI_TWR_MPR_F2	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TWR_MPR_F1	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TWR_MPR_F0	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.699 EMIF_CTLCFG_DENALI_PI_203 Register

1 EMIF_CTLCFG_DENALI_PI_203 Register (Offset = 232Ch) [reset = 0h]

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Table 14-22041. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A32Ch

Figure 14-7312. EMIF_CTLCFG_DENALI_PI_203 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_MULTI_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_DFE_EN_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_RXCAL_EN_F0	
NONE						R/W	
0h						0h	

Table 14-22043. EMIF_CTLCFG_DENALI_PI_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F1	R/W	0h	Enable PATTERN-0 for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F0	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F0	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F0	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.700 EMIF_CTLCFG_DENALI_PI_204 Register

1 EMIF_CTLCFG_DENALI_PI_204 Register (Offset = 2330h) [reset = 0h]

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Table 14-22044. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A330h**

Figure 14-7313. EMIF_CTLCFG_DENALI_PI_204 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_RDLVL_MULTI_EN_F1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_RDLVL_DFE_EN_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_RDLVL_RXCAL_EN_F1	
NONE						R/W	
0h						0h	

Table 14-22046. EMIF_CTLCFG_DENALI_PI_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F2	R/W	0h	Enable PATTERN-0 for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F1	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F1	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F1	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.701 EMIF_CTLCFG_DENALI_PI_205 Register

1 EMIF_CTLCFG_DENALI_PI_205 Register (Offset = 2334h) [reset = 0h]

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Table 14-22047. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A334h**

Figure 14-7314. EMIF_CTLCFG_DENALI_PI_205 Name Register

31	30	29	28	27	26	25	24
PI_RDLAT_ADJ_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_MULTI_EN_F2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_DFE_EN_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_RXCAL_EN_F2	
NONE						R/W	
0h						0h	

Table 14-22049. EMIF_CTLCFG_DENALI_PI_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_RDLAT_ADJ_F0	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F2	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F2	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F2	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.702 EMIF_CTLCFG_DENALI_PI_206 Register

1 EMIF_CTLCFG_DENALI_PI_206 Register (Offset = 2338h) [reset = 0h]

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Table 14-22050. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A338h

Figure 14-7315. EMIF_CTLCFG_DENALI_PI_206 Name Register

31	30	29	28	27	26	25	24
PI_WRLAT_ADJ_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_WRLAT_ADJ_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_RDLAT_ADJ_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_RDLAT_ADJ_F1							
R/W							
0h							

Table 14-22052. EMIF_CTLCFG_DENALI_PI_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_WRLAT_ADJ_F1	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_WRLAT_ADJ_F0	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_RDLAT_ADJ_F2	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_RDLAT_ADJ_F1	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.703 EMIF_CTLCFG_DENALI_PI_207 Register

1 EMIF_CTLCFG_DENALI_PI_207 Register (Offset = 233Ch) [reset = 0h]

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Table 14-22053. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A33Ch**

Figure 14-7316. EMIF_CTLCFG_DENALI_PI_207 Name Register

31	30	29	28	27	26	25	24
RESERVED					PI_TDFI_PHY_WRDATA_F2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PI_TDFI_PHY_WRDATA_F1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PI_TDFI_PHY_WRDATA_F0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WRLAT_ADJ_F2							
R/W							
0h							

Table 14-22055. EMIF_CTLCFG_DENALI_PI_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_TDFI_PHY_WRDATA_F2	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 2, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_TDFI_PHY_WRDATA_F1	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 1, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_TDFI_PHY_WRDATA_F0	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 0, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
7:0	PI_WRLAT_ADJ_F2	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.704 EMIF_CTLCFG_DENALI_PI_208 Register

1 EMIF_CTLCFG_DENALI_PI_208 Register (Offset = 2340h) [reset = 0h]

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Table 14-22056. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A340h**

Figure 14-7317. EMIF_CTLCFG_DENALI_PI_208 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_CALVL_CAPTURE_F0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_CALVL_CAPTURE_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TDFI_CALVL_CC_F0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CALVL_CC_F0							
R/W							
0h							

Table 14-22058. EMIF_CTLCFG_DENALI_PI_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F0	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F0	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.705 EMIF_CTLCFG_DENALI_PI_209 Register

1 EMIF_CTLCFG_DENALI_PI_209 Register (Offset = 2344h) [reset = 0h]

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Table 14-22059. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A344h

Figure 14-7318. EMIF_CTLCFG_DENALI_PI_209 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_CALVL_CAPTURE_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_CALVL_CAPTURE_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_CALVL_CC_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_CALVL_CC_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22061. EMIF_CTLCFG_DENALI_PI_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F1	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F1	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.706 EMIF_CTLCFG_DENALI_PI_210 Register

1 EMIF_CTLCFG_DENALI_PI_210 Register (Offset = 2348h) [reset = 0h]

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Table 14-22062. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A348h**

Figure 14-7319. EMIF_CTLCFG_DENALI_PI_210 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_CALVL_CAPTURE_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TDFI_CALVL_CAPTURE_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_CALVL_CC_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TDFI_CALVL_CC_F2							
R/W							
0h							

Table 14-22064. EMIF_CTLCFG_DENALI_PI_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F2	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F2	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.707 EMIF_CTLCFG_DENALI_PI_211 Register

1 EMIF_CTLCFG_DENALI_PI_211 Register (Offset = 234Ch) [reset = 0h]

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Table 14-22065. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A34Ch**

Figure 14-7320. EMIF_CTLCFG_DENALI_PI_211 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TMRZ_F0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PI_CALVL_EN_F2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_CALVL_EN_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_CALVL_EN_F0	
NONE						R/W	
0h						0h	

Table 14-22067. EMIF_CTLCFG_DENALI_PI_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TMRZ_F0	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_CALVL_EN_F2	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 2. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_CALVL_EN_F1	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 1. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_CALVL_EN_F0	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 0. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.708 EMIF_CTLCFG_DENALI_PI_212 Register

1 EMIF_CTLCFG_DENALI_PI_212 Register (Offset = 2350h) [reset = 0h]

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Table 14-22068. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A350h**

Figure 14-7321. EMIF_CTLCFG_DENALI_PI_212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PI_TMRZ_F1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED		PI_TCAENT_F0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PI_TCAENT_F0							
R/W							
0h							

Table 14-22070. EMIF_CTLCFG_DENALI_PI_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PI_TMRZ_F1	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F0	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.709 EMIF_CTLCFG_DENALI_PI_213 Register

1 EMIF_CTLCFG_DENALI_PI_213 Register (Offset = 2354h) [reset = 0h]

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Table 14-22071. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A354h**

Figure 14-7322. EMIF_CTLCFG_DENALI_PI_213 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PI_TMRZ_F2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED		PI_TCAENT_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PI_TCAENT_F1							
R/W							
0h							

Table 14-22073. EMIF_CTLCFG_DENALI_PI_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PI_TMRZ_F2	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F1	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.710 EMIF_CTLCFG_DENALI_PI_214 Register

1 EMIF_CTLCFG_DENALI_PI_214 Register (Offset = 2358h) [reset = 0h]

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Table 14-22074. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A358h**

Figure 14-7323. EMIF_CTLCFG_DENALI_PI_214 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TDFI_CASEL_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TDFI_CACSCA_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_TCAENT_F2					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TCAENT_F2							
R/W							
0h							

Table 14-22076. EMIF_CTLCFG_DENALI_PI_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TDFI_CASEL_F0	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TDFI_CACSCA_F0	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F2	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.711 EMIF_CTLCFG_DENALI_PI_215 Register

1 EMIF_CTLCFG_DENALI_PI_215 Register (Offset = 235Ch) [reset = 0h]

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Table 14-22077. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A35Ch**

Figure 14-7324. EMIF_CTLCFG_DENALI_PI_215 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TVREF_LONG_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TVREF_LONG_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TVREF_SHORT_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TVREF_SHORT_F0							
R/W							
0h							

Table 14-22079. EMIF_CTLCFG_DENALI_PI_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_LONG_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_SHORT_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.712 EMIF_CTLCFG_DENALI_PI_216 Register

1 EMIF_CTLCFG_DENALI_PI_216 Register (Offset = 2360h) [reset = 0h]

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Table 14-22080. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A360h**

Figure 14-7325. EMIF_CTLCFG_DENALI_PI_216 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TVREF_SHORT_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TVREF_SHORT_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TDFI_CASEL_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TDFI_CACSCA_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-22082. EMIF_CTLCFG_DENALI_PI_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_SHORT_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TDFI_CASEL_F1	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TDFI_CACSCA_F1	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.713 EMIF_CTLCFG_DENALI_PI_217 Register

1 EMIF_CTLCFG_DENALI_PI_217 Register (Offset = 2364h) [reset = 0h]

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Table 14-22083. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A364h**

Figure 14-7326. EMIF_CTLCFG_DENALI_PI_217 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TDFI_CASEL_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TDFI_CACSCA_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TVREF_LONG_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TVREF_LONG_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22085. EMIF_CTLCFG_DENALI_PI_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TDFI_CASEL_F2	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TDFI_CACSCA_F2	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_LONG_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.714 EMIF_CTLCFG_DENALI_PI_218 Register

1 EMIF_CTLCFG_DENALI_PI_218 Register (Offset = 2368h) [reset = 0h]

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Table 14-22086. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A368h**

Figure 14-7327. EMIF_CTLCFG_DENALI_PI_218 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TVREF_LONG_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TVREF_LONG_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TVREF_SHORT_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TVREF_SHORT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22088. EMIF_CTLCFG_DENALI_PI_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_LONG_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_SHORT_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.715 EMIF_CTLCFG_DENALI_PI_219 Register

1 EMIF_CTLCFG_DENALI_PI_219 Register (Offset = 236Ch) [reset = 0h]

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Table 14-22089. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A36Ch**

Figure 14-7328. EMIF_CTLCFG_DENALI_PI_219 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F1						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F0						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F0						
NONE	R/W						
0h	0h						

Table 14-22091. EMIF_CTLCFG_DENALI_PI_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_CALVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_CALVL_VREF_INITIAL_START_POINT_F1	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CALVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CALVL_VREF_INITIAL_START_POINT_F0	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n

14.6.6.2.716 EMIF_CTLCFG_DENALI_PI_220 Register

1 EMIF_CTLCFG_DENALI_PI_220 Register (Offset = 2370h) [reset = 0h]

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Table 14-22092. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A370h**

Figure 14-7329. EMIF_CTLCFG_DENALI_PI_220 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_CALVL_VREF_DELTA_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_CALVL_VREF_DELTA_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F2						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F2						
NONE	R/W						
0h	0h						

Table 14-22094. EMIF_CTLCFG_DENALI_PI_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CALVL_VREF_DELTA_F1	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CALVL_VREF_DELTA_F0	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CALVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CALVL_VREF_INITIAL_START_POINT_F2	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n

14.6.6.2.717 EMIF_CTLCFG_DENALI_PI_221 Register

1 EMIF_CTLCFG_DENALI_PI_221 Register (Offset = 2374h) [reset = 0h]

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Table 14-22095. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A374h**

Figure 14-7330. EMIF_CTLCFG_DENALI_PI_221 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TXP_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TDFI_CALVL_STROBE_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_CALVL_VREF_DELTA_F2			
NONE				R/W			
0h				0h			

Table 14-22097. EMIF_CTLCFG_DENALI_PI_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F0	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F0	R/W	0h	CKE assert to next valid command delay for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F0	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CALVL_VREF_DELTA_F2	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.718 EMIF_CTLCFG_DENALI_PI_222 Register

1 EMIF_CTLCFG_DENALI_PI_222 Register (Offset = 2378h) [reset = 0h]

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Table 14-22098. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A378h**

Figure 14-7331. EMIF_CTLCFG_DENALI_PI_222 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TXP_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TDFI_CALVL_STROBE_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_TCKELCK_F0				
NONE			R/W				
0h			0h				

Table 14-22100. EMIF_CTLCFG_DENALI_PI_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F1	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F1	R/W	0h	CKE assert to next valid command delay for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F1	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F0	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.719 EMIF_CTLCFG_DENALI_PI_223 Register

1 EMIF_CTLCFG_DENALI_PI_223 Register (Offset = 237Ch) [reset = 0h]

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Table 14-22101. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A37Ch

Figure 14-7332. EMIF_CTLCFG_DENALI_PI_223 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TXP_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TDFI_CALVL_STROBE_F2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_TCKELCK_F1				
NONE			R/W				
0h			0h				

Table 14-22103. EMIF_CTLCFG_DENALI_PI_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F2	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F2	R/W	0h	CKE assert to next valid command delay for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F2	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F1	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.720 EMIF_CTLCFG_DENALI_PI_224 Register

1 EMIF_CTLCFG_DENALI_PI_224 Register (Offset = 2380h) [reset = 0h]

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Table 14-22104. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A380h**

Figure 14-7333. EMIF_CTLCFG_DENALI_PI_224 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_INIT_START_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_START_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_START_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			PI_TCKELCK_F2				
NONE			R/W				
0h			0h				

Table 14-22106. EMIF_CTLCFG_DENALI_PI_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	PI_TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 0, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F2	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.721 EMIF_CTLCFG_DENALI_PI_225 Register

1 EMIF_CTLCFG_DENALI_PI_225 Register (Offset = 2384h) [reset = 0h]

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Table 14-22107. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A384h

Figure 14-7334. EMIF_CTLCFG_DENALI_PI_225 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							

Table 14-22109. EMIF_CTLCFG_DENALI_PI_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 0, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.722 EMIF_CTLCFG_DENALI_PI_226 Register

1 EMIF_CTLCFG_DENALI_PI_226 Register (Offset = 2388h) [reset = 0h]

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Table 14-22110. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A388h

Figure 14-7335. EMIF_CTLCFG_DENALI_PI_226 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_START_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_START_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_START_F1							
R/W							
0h							

Table 14-22112. EMIF_CTLCFG_DENALI_PI_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 1, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.723 EMIF_CTLCFG_DENALI_PI_227 Register

1 EMIF_CTLCFG_DENALI_PI_227 Register (Offset = 238Ch) [reset = 0h]

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Table 14-22113. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A38Ch

Figure 14-7336. EMIF_CTLCFG_DENALI_PI_227 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							

Table 14-22115. EMIF_CTLCFG_DENALI_PI_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 1, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.724 EMIF_CTLCFG_DENALI_PI_228 Register

1 EMIF_CTLCFG_DENALI_PI_228 Register (Offset = 2390h) [reset = 0h]

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Table 14-22116. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A390h**

Figure 14-7337. EMIF_CTLCFG_DENALI_PI_228 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_START_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_START_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_START_F2							
R/W							
0h							

Table 14-22118. EMIF_CTLCFG_DENALI_PI_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 2, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.725 EMIF_CTLCFG_DENALI_PI_229 Register

1 EMIF_CTLCFG_DENALI_PI_229 Register (Offset = 2394h) [reset = 0h]

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Table 14-22119. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A394h**

Figure 14-7338. EMIF_CTLCFG_DENALI_PI_229 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCKEHDQS_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22121. EMIF_CTLCFG_DENALI_PI_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCKEHDQS_F0	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:0	PI_TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 2, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.726 EMIF_CTLCFG_DENALI_PI_230 Register

1 EMIF_CTLCFG_DENALI_PI_230 Register (Offset = 2398h) [reset = 0h]

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Table 14-22122. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A398h**

Figure 14-7339. EMIF_CTLCFG_DENALI_PI_230 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_TCKEHDQS_F1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TFC_F0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TFC_F0							
R/W							
0h							

Table 14-22124. EMIF_CTLCFG_DENALI_PI_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PI_TCKEHDQS_F1	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F0	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.727 EMIF_CTLCFG_DENALI_PI_231 Register

1 EMIF_CTLCFG_DENALI_PI_231 Register (Offset = 239Ch) [reset = 0h]

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Table 14-22125. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A39Ch**

Figure 14-7340. EMIF_CTLCFG_DENALI_PI_231 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCKEHDQS_F2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TFC_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TFC_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22127. EMIF_CTLCFG_DENALI_PI_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PI_TCKEHDQS_F2	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F1	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.728 EMIF_CTLCFG_DENALI_PI_232 Register

1 EMIF_CTLCFG_DENALI_PI_232 Register (Offset = 23A0h) [reset = 0h]

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Table 14-22128. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3A0h**

Figure 14-7341. EMIF_CTLCFG_DENALI_PI_232 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_VREF_EN_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_VREF_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TFC_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TFC_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22130. EMIF_CTLCFG_DENALI_PI_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_VREF_EN_F1	R/W	0h	Enable VREF training during power-up initialization for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_VREF_EN_F0	R/W	0h	Enable VREF training during power-up initialization for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F2	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.729 EMIF_CTLCFG_DENALI_PI_233 Register

1 EMIF_CTLCFG_DENALI_PI_233 Register (Offset = 23A4h) [reset = 0h]

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Table 14-22131. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3A4h**

Figure 14-7342. EMIF_CTLCFG_DENALI_PI_233 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WDQLVL_WR_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_WR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_VREF_EN_F2	
NONE						R/W	
0h						0h	

Table 14-22133. EMIF_CTLCFG_DENALI_PI_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PI_TDFI_WDQLVL_WR_F0	R/W	0h	Switch time from write to read for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_VREF_EN_F2	R/W	0h	Enable VREF training during power-up initialization for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.730 EMIF_CTLCFG_DENALI_PI_234 Register

1 EMIF_CTLCFG_DENALI_PI_234 Register (Offset = 23A8h) [reset = 0h]

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Table 14-22134. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3A8h

Figure 14-7343. EMIF_CTLCFG_DENALI_PI_234 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_WDQLVL_VREF_INITIAL_START_POINT_F0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WDQLVL_RW_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_WDQLVL_RW_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22136. EMIF_CTLCFG_DENALI_PI_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	Write DQ training vref initial training stop value for frequency set 0. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F0	R/W	0h	Write DQ training vref initial training start value for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F0	R/W	0h	Switch time from read to write for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.731 EMIF_CTLCFG_DENALI_PI_235 Register

1 EMIF_CTLCFG_DENALI_PI_235 Register (Offset = 23ACh) [reset = 0h]

Return to Summary Table

Table 14-22137. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3ACh**

Figure 14-7344. EMIF_CTLCFG_DENALI_PI_235 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_WDQLVL_CL_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_NTP_TRAIN_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WDQLVL_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_WDQLVL_VREF_DELTA_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-22139. EMIF_CTLCFG_DENALI_PI_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F0	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F0	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F0	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F0	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.732 EMIF_CTLCFG_DENALI_PI_236 Register

1 EMIF_CTLCFG_DENALI_PI_236 Register (Offset = 23B0h) [reset = 0h]

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Table 14-22140. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3B0h**

Figure 14-7345. EMIF_CTLCFG_DENALI_PI_236 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_WDQLVL_WR_F1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_WDQLVL_WR_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WDQLVL_WRLAT_ADJ_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WDQLVL_RDLAT_ADJ_F0							
R/W							
0h							

Table 14-22142. EMIF_CTLCFG_DENALI_PI_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WDQLVL_WR_F1	R/W	0h	Switch time from write to read for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F0	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 0, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F0	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 0, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.733 EMIF_CTLCFG_DENALI_PI_237 Register

1 EMIF_CTLCFG_DENALI_PI_237 Register (Offset = 23B4h) [reset = 0h]

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Table 14-22143. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3B4h**

Figure 14-7346. EMIF_CTLCFG_DENALI_PI_237 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F1						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TDFI_WDQLVL_RW_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_WDQLVL_RW_F1							
R/W							
0h							

Table 14-22145. EMIF_CTLCFG_DENALI_PI_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	Write DQ training vref initial training stop value for frequency set 1. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F1	R/W	0h	Write DQ training vref initial training start value for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F1	R/W	0h	Switch time from read to write for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.734 EMIF_CTLCFG_DENALI_PI_238 Register

1 EMIF_CTLCFG_DENALI_PI_238 Register (Offset = 23B8h) [reset = 0h]

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Table 14-22146. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3B8h**

Figure 14-7347. EMIF_CTLCFG_DENALI_PI_238 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_WDQLVL_CL_F1				
NONE			R/W				
0h			0h				

23	22	21	20	19	18	17	16
RESERVED						PI_NTP_TRAIN_EN_F1	
NONE						R/W	
0h						0h	

15	14	13	12	11	10	9	8
RESERVED						PI_WDQLVL_EN_F1	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED				PI_WDQLVL_VREF_DELTA_F1			
NONE				R/W			
0h				0h			

Table 14-22148. EMIF_CTLCFG_DENALI_PI_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F1	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F1	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F1	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F1	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.735 EMIF_CTLCFG_DENALI_PI_239 Register

1 EMIF_CTLCFG_DENALI_PI_239 Register (Offset = 23BCh) [reset = 0h]

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Table 14-22149. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3BCh**

Figure 14-7348. EMIF_CTLCFG_DENALI_PI_239 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_WDQLVL_WR_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_WR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_WDQLVL_WRLAT_ADJ_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_RDLAT_ADJ_F1							
R/W							
0h							

Table 14-22151. EMIF_CTLCFG_DENALI_PI_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WDQLVL_WR_F2	R/W	0h	Switch time from write to read for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F1	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 1, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F1	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 1, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.736 EMIF_CTLCFG_DENALI_PI_240 Register

1 EMIF_CTLCFG_DENALI_PI_240 Register (Offset = 23C0h) [reset = 0h]

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Table 14-22152. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3C0h

Figure 14-7349. EMIF_CTLCFG_DENALI_PI_240 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F2							
R/W							
0h							

Table 14-22154. EMIF_CTLCFG_DENALI_PI_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	Write DQ training vref initial training stop value for frequency set 2. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F2	R/W	0h	Write DQ training vref initial training start value for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F2	R/W	0h	Switch time from read to write for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.737 EMIF_CTLCFG_DENALI_PI_241 Register

1 EMIF_CTLCFG_DENALI_PI_241 Register (Offset = 23C4h) [reset = 0h]

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Table 14-22155. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3C4h**

Figure 14-7350. EMIF_CTLCFG_DENALI_PI_241 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_WDQLVL_CL_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_NTP_TRAIN_EN_F2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_WDQLVL_EN_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_WDQLVL_VREF_DELTA_F2			
NONE				R/W			
0h				0h			

Table 14-22157. EMIF_CTLCFG_DENALI_PI_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F2	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F2	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F2	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F2	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.738 EMIF_CTLCFG_DENALI_PI_242 Register

1 EMIF_CTLCFG_DENALI_PI_242 Register (Offset = 23C8h) [reset = 0h]

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Table 14-22158. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3C8h**

Figure 14-7351. EMIF_CTLCFG_DENALI_PI_242 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RD_DBI_LEVEL_EN_F1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_RD_DBI_LEVEL_EN_F0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WDQLVL_WRLAT_ADJ_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WDQLVL_RDLAT_ADJ_F2							
R/W							
0h							

Table 14-22160. EMIF_CTLCFG_DENALI_PI_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RD_DBI_LEVEL_EN_F1	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RD_DBI_LEVEL_EN_F0	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F2	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 2, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F2	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 2, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.739 EMIF_CTLCFG_DENALI_PI_243 Register

1 EMIF_CTLCFG_DENALI_PI_243 Register (Offset = 23CCh) [reset = 0h]

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Table 14-22161. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3CCh

Figure 14-7352. EMIF_CTLCFG_DENALI_PI_243 Name Register

31	30	29	28	27	26	25	24
PI_TRCD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TRP_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TRTP_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_RD_DBI_LEVEL_EN_F2	
NONE						R/W	
0h						0h	

Table 14-22163. EMIF_CTLCFG_DENALI_PI_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRCD_F0	R/W	0h	DRAM tRCD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRP_F0	R/W	0h	DRAM tRP value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_TRTP_F0	R/W	0h	DRAM tRTP value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RD_DBI_LEVEL_EN_F2	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n

14.6.6.2.740 EMIF_CTLCFG_DENALI_PI_244 Register

1 EMIF_CTLCFG_DENALI_PI_244 Register (Offset = 23D0h) [reset = 0h]

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Table 14-22164. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3D0h**

Figure 14-7353. EMIF_CTLCFG_DENALI_PI_244 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TWR_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED		PI_TWTR_F0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED			PI_TCCD_L_F0				
NONE			R/W				
0h			0h				

Table 14-22166. EMIF_CTLCFG_DENALI_PI_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_TWR_F0	R/W	0h	DRAM tWR value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_TWTR_F0	R/W	0h	DRAM tWTR value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCCD_L_F0	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.741 EMIF_CTLCFG_DENALI_PI_245 Register

1 EMIF_CTLCFG_DENALI_PI_245 Register (Offset = 23D4h) [reset = 0h]

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Table 14-22167. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3D4h**

Figure 14-7354. EMIF_CTLCFG_DENALI_PI_245 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TRAS_MAX_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TRAS_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TRAS_MAX_F0							
R/W							
0h							

Table 14-22169. EMIF_CTLCFG_DENALI_PI_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F0	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.742 EMIF_CTLCFG_DENALI_PI_246 Register

1 EMIF_CTLCFG_DENALI_PI_246 Register (Offset = 23D8h) [reset = 0h]

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Table 14-22170. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3D8h**

Figure 14-7355. EMIF_CTLCFG_DENALI_PI_246 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCCDMW_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDQSCK_MAX_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_TRAS_MIN_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TRAS_MIN_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22172. EMIF_CTLCFG_DENALI_PI_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F0	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F0	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.743 EMIF_CTLCFG_DENALI_PI_247 Register

1 EMIF_CTLCFG_DENALI_PI_247 Register (Offset = 23DCh) [reset = 0h]

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Table 14-22173. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3DCh**

Figure 14-7356. EMIF_CTLCFG_DENALI_PI_247 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F0							
R/W							
0h							

Table 14-22175. EMIF_CTLCFG_DENALI_PI_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F0	R/W	0h	DRAM tMOD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F0	R/W	0h	DRAM tMRW value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F0	R/W	0h	DRAM tMRD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F0	R/W	0h	Min cycles from sref entry to sref exit for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.744 EMIF_CTLCFG_DENALI_PI_248 Register

1 EMIF_CTLCFG_DENALI_PI_248 Register (Offset = 23E0h) [reset = 0h]

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Table 14-22176. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3E0h

Figure 14-7357. EMIF_CTLCFG_DENALI_PI_248 Name Register

31	30	29	28	27	26	25	24
PI_TRP_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TRTP_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_PAR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TMOD_PAR_F0							
R/W							
0h							

Table 14-22178. EMIF_CTLCFG_DENALI_PI_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRP_F1	R/W	0h	DRAM tRP value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRTP_F1	R/W	0h	DRAM tRTP value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_PAR_F0	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F0	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.745 EMIF_CTLCFG_DENALI_PI_249 Register

1 EMIF_CTLCFG_DENALI_PI_249 Register (Offset = 23E4h) [reset = 0h]

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Table 14-22179. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3E4h**

Figure 14-7358. EMIF_CTLCFG_DENALI_PI_249 Name Register

31	30	29	28	27	26	25	24
PI_TWR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PI_TWTR_F1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			PI_TCCD_L_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PI_TRCD_F1							
R/W							
0h							

Table 14-22181. EMIF_CTLCFG_DENALI_PI_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TWR_F1	R/W	0h	DRAM tWR value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TWTR_F1	R/W	0h	DRAM tWTR value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TCCD_L_F1	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TRCD_F1	R/W	0h	DRAM tRCD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.746 EMIF_CTLCFG_DENALI_PI_250 Register

1 EMIF_CTLCFG_DENALI_PI_250 Register (Offset = 23E8h) [reset = 0h]

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Table 14-22182. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3E8h**

Figure 14-7359. EMIF_CTLCFG_DENALI_PI_250 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				PI_TRAS_MAX_F1			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
PI_TRAS_MAX_F1							
R/W							
0h							

7	6	5	4	3	2	1	0
PI_TRAS_MAX_F1							
R/W							
0h							

Table 14-22184. EMIF_CTLCFG_DENALI_PI_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F1	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.747 EMIF_CTLCFG_DENALI_PI_251 Register

1 EMIF_CTLCFG_DENALI_PI_251 Register (Offset = 23ECh) [reset = 0h]

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Table 14-22185. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3ECh

Figure 14-7360. EMIF_CTLCFG_DENALI_PI_251 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TCCDMW_F1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TDQSCK_MAX_F1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_TRAS_MIN_F1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TRAS_MIN_F1							
R/W							
0h							

Table 14-22187. EMIF_CTLCFG_DENALI_PI_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F1	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F1	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.748 EMIF_CTLCFG_DENALI_PI_252 Register

1 EMIF_CTLCFG_DENALI_PI_252 Register (Offset = 23F0h) [reset = 0h]

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Table 14-22188. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3F0h

Figure 14-7361. EMIF_CTLCFG_DENALI_PI_252 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F1							
R/W							
0h							

Table 14-22190. EMIF_CTLCFG_DENALI_PI_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F1	R/W	0h	DRAM tMOD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F1	R/W	0h	DRAM tMRW value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F1	R/W	0h	DRAM tMRD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F1	R/W	0h	Min cycles from sref entry to sref exit for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.749 EMIF_CTLCFG_DENALI_PI_253 Register

1 EMIF_CTLCFG_DENALI_PI_253 Register (Offset = 23F4h) [reset = 0h]

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Table 14-22191. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A3F4h

Figure 14-7362. EMIF_CTLCFG_DENALI_PI_253 Name Register

31	30	29	28	27	26	25	24
PI_TRP_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TRTP_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_PAR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TMOD_PAR_F1							
R/W							
0h							

Table 14-22193. EMIF_CTLCFG_DENALI_PI_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRP_F2	R/W	0h	DRAM tRP value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRTP_F2	R/W	0h	DRAM tRTP value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_PAR_F1	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F1	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.750 EMIF_CTLCFG_DENALI_PI_254 Register

1 EMIF_CTLCFG_DENALI_PI_254 Register (Offset = 23F8h) [reset = 0h]

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Table 14-22194. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3F8h**

Figure 14-7363. EMIF_CTLCFG_DENALI_PI_254 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TWR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TWTR_F2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TCCD_L_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TRCD_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22196. EMIF_CTLCFG_DENALI_PI_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TWR_F2	R/W	0h	DRAM tWR value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TWTR_F2	R/W	0h	DRAM tWTR value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TCCD_L_F2	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TRCD_F2	R/W	0h	DRAM tRCD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.751 EMIF_CTLCFG_DENALI_PI_255 Register

1 EMIF_CTLCFG_DENALI_PI_255 Register (Offset = 23FCh) [reset = 0h]

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Table 14-22197. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A3FCh**

Figure 14-7364. EMIF_CTLCFG_DENALI_PI_255 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TRAS_MAX_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TRAS_MAX_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TRAS_MAX_F2							
R/W							
0h							

Table 14-22199. EMIF_CTLCFG_DENALI_PI_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F2	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.752 EMIF_CTLCFG_DENALI_PI_256 Register

1 EMIF_CTLCFG_DENALI_PI_256 Register (Offset = 2400h) [reset = 0h]

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Table 14-22200. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A400h

Figure 14-7365. EMIF_CTLCFG_DENALI_PI_256 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TCCDMW_F2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TDQSCK_MAX_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_TRAS_MIN_F2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TRAS_MIN_F2							
R/W							
0h							

Table 14-22202. EMIF_CTLCFG_DENALI_PI_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F2	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F2	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.753 EMIF_CTLCFG_DENALI_PI_257 Register

1 EMIF_CTLCFG_DENALI_PI_257 Register (Offset = 2404h) [reset = 0h]

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Table 14-22203. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A404h**

Figure 14-7366. EMIF_CTLCFG_DENALI_PI_257 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F2							
R/W							
0h							

Table 14-22205. EMIF_CTLCFG_DENALI_PI_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F2	R/W	0h	DRAM tMOD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F2	R/W	0h	DRAM tMRW value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F2	R/W	0h	DRAM tMRD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F2	R/W	0h	Min cycles from sref entry to sref exit for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.754 EMIF_CTLCFG_DENALI_PI_258 Register

1 EMIF_CTLCFG_DENALI_PI_258 Register (Offset = 2408h) [reset = 0h]

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Table 14-22206. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A408h

Figure 14-7367. EMIF_CTLCFG_DENALI_PI_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_PAR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TMOD_PAR_F2							
R/W							
0h							

Table 14-22208. EMIF_CTLCFG_DENALI_PI_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TMRD_PAR_F2	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F2	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.755 EMIF_CTLCFG_DENALI_PI_259 Register

1 EMIF_CTLCFG_DENALI_PI_259 Register (Offset = 240Ch) [reset = 0h]

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Table 14-22209. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A40Ch

Figure 14-7368. EMIF_CTLCFG_DENALI_PI_259 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PI_TDFI_CTRLUPD_MAX_F0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F0							
R/W							
0h							

Table 14-22211. EMIF_CTLCFG_DENALI_PI_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 0, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.756 EMIF_CTLCFG_DENALI_PI_260 Register

1 EMIF_CTLCFG_DENALI_PI_260 Register (Offset = 2410h) [reset = 0h]

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Table 14-22212. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A410h**

Figure 14-7369. EMIF_CTLCFG_DENALI_PI_260 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							

Table 14-22214. EMIF_CTLCFG_DENALI_PI_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 0, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.757 EMIF_CTLCFG_DENALI_PI_261 Register

1 EMIF_CTLCFG_DENALI_PI_261 Register (Offset = 2414h) [reset = 0h]

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Table 14-22215. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A414h

Figure 14-7370. EMIF_CTLCFG_DENALI_PI_261 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TDFI_CTRLUPD_MAX_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_CTRLUPD_MAX_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CTRLUPD_MAX_F1							
R/W							
0h							

Table 14-22217. EMIF_CTLCFG_DENALI_PI_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 1, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.758 EMIF_CTLCFG_DENALI_PI_262 Register

1 EMIF_CTLCFG_DENALI_PI_262 Register (Offset = 2418h) [reset = 0h]

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Table 14-22218. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A418h**

Figure 14-7371. EMIF_CTLCFG_DENALI_PI_262 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							

Table 14-22220. EMIF_CTLCFG_DENALI_PI_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 1, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.759 EMIF_CTLCFG_DENALI_PI_263 Register

1 EMIF_CTLCFG_DENALI_PI_263 Register (Offset = 241Ch) [reset = 0h]

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Table 14-22221. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A41Ch**

Figure 14-7372. EMIF_CTLCFG_DENALI_PI_263 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_CTRLUPD_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22223. EMIF_CTLCFG_DENALI_PI_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 2, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.760 EMIF_CTLCFG_DENALI_PI_264 Register

1 EMIF_CTLCFG_DENALI_PI_264 Register (Offset = 2420h) [reset = 0h]

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Table 14-22224. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A420h**

Figure 14-7373. EMIF_CTLCFG_DENALI_PI_264 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							

Table 14-22226. EMIF_CTLCFG_DENALI_PI_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 2, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.761 EMIF_CTLCFG_DENALI_PI_265 Register

1 EMIF_CTLCFG_DENALI_PI_265 Register (Offset = 2424h) [reset = 0h]

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Table 14-22227. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A424h**

Figure 14-7374. EMIF_CTLCFG_DENALI_PI_265 Name Register

31	30	29	28	27	26	25	24
PI_TXSR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TXSR_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TXSR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSR_F0							
R/W							
0h							

Table 14-22229. EMIF_CTLCFG_DENALI_PI_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TXSR_F1	R/W	0h	DRAM TXSR value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n
15:0	PI_TXSR_F0	R/W	0h	DRAM TXSR value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.762 EMIF_CTLCFG_DENALI_PI_266 Register

1 EMIF_CTLCFG_DENALI_PI_266 Register (Offset = 2428h) [reset = 0h]

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Table 14-22230. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A428h**

Figure 14-7375. EMIF_CTLCFG_DENALI_PI_266 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TEXCKE_F1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_TEXCKE_F0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TXSR_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TXSR_F2							
R/W							
0h							

Table 14-22232. EMIF_CTLCFG_DENALI_PI_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TEXCKE_F1	R/W	0h	DRAM CKE low after SREF command timing for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TEXCKE_F0	R/W	0h	DRAM CKE low after SREF command timing for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:0	PI_TXSR_F2	R/W	0h	DRAM TXSR value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.763 EMIF_CTLCFG_DENALI_PI_267 Register

1 EMIF_CTLCFG_DENALI_PI_267 Register (Offset = 242Ch) [reset = 0h]

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Table 14-22233. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A42Ch**

Figure 14-7376. EMIF_CTLCFG_DENALI_PI_267 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDLL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDLL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		PI_TEXCKE_F2					
NONE		R/W					
0h		0h					

Table 14-22235. EMIF_CTLCFG_DENALI_PI_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	PI_TDLL_F0	R/W	0h	DRAM tDLL value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_TEXCKE_F2	R/W	0h	DRAM CKE low after SREF command timing for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.764 EMIF_CTLCFG_DENALI_PI_268 Register

1 EMIF_CTLCFG_DENALI_PI_268 Register (Offset = 2430h) [reset = 0h]

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Table 14-22236. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A430h

Figure 14-7377. EMIF_CTLCFG_DENALI_PI_268 Name Register

31	30	29	28	27	26	25	24
PI_TDLL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDLL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDLL_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDLL_F1							
R/W							
0h							

Table 14-22238. EMIF_CTLCFG_DENALI_PI_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TDLL_F2	R/W	0h	DRAM tDLL value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n
15:0	PI_TDLL_F1	R/W	0h	DRAM tDLL value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.765 EMIF_CTLCFG_DENALI_PI_269 Register

1 EMIF_CTLCFG_DENALI_PI_269 Register (Offset = 2434h) [reset = 0h]

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Table 14-22239. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A434h

Figure 14-7378. EMIF_CTLCFG_DENALI_PI_269 Name Register

31	30	29	28	27	26	25	24
PI_TCKSRE_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TCKSRX_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TCKSRE_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TCKSRX_F0							
R/W							
0h							

Table 14-22241. EMIF_CTLCFG_DENALI_PI_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TCKSRE_F1	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
23:16	PI_TCKSRX_F1	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n
15:8	PI_TCKSRE_F0	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKSRX_F0	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.766 EMIF_CTLCFG_DENALI_PI_270 Register

1 EMIF_CTLCFG_DENALI_PI_270 Register (Offset = 2438h) [reset = 0h]

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Table 14-22242. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A438h**

Figure 14-7379. EMIF_CTLCFG_DENALI_PI_270 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TCKSRE_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TCKSRX_F2							
R/W							
0h							

Table 14-22244. EMIF_CTLCFG_DENALI_PI_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TCKSRE_F2	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKSRX_F2	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.767 EMIF_CTLCFG_DENALI_PI_271 Register

1 EMIF_CTLCFG_DENALI_PI_271 Register (Offset = 243Ch) [reset = 0h]

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Table 14-22245. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A43Ch

Figure 14-7380. EMIF_CTLCFG_DENALI_PI_271 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT_F0							
R/W							
0h							

Table 14-22247. EMIF_CTLCFG_DENALI_PI_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F0	R/W	0h	DRAM tINIT value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.768 EMIF_CTLCFG_DENALI_PI_272 Register

1 EMIF_CTLCFG_DENALI_PI_272 Register (Offset = 2440h) [reset = 0h]

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Table 14-22248. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A440h

Figure 14-7381. EMIF_CTLCFG_DENALI_PI_272 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT3_F0							
R/W							
0h							

Table 14-22250. EMIF_CTLCFG_DENALI_PI_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F0	R/W	0h	DRAM tINIT3 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.769 EMIF_CTLCFG_DENALI_PI_273 Register

1 EMIF_CTLCFG_DENALI_PI_273 Register (Offset = 2444h) [reset = 0h]

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Table 14-22251. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A444h**

Figure 14-7382. EMIF_CTLCFG_DENALI_PI_273 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TINIT4_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22253. EMIF_CTLCFG_DENALI_PI_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F0	R/W	0h	DRAM tINIT4 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.770 EMIF_CTLCFG_DENALI_PI_274 Register

1 EMIF_CTLCFG_DENALI_PI_274 Register (Offset = 2448h) [reset = 0h]

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Table 14-22254. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A448h**

Figure 14-7383. EMIF_CTLCFG_DENALI_PI_274 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F0							
R/W							
0h							

Table 14-22256. EMIF_CTLCFG_DENALI_PI_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F0	R/W	0h	DRAM tINIT5 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.771 EMIF_CTLCFG_DENALI_PI_275 Register

1 EMIF_CTLCFG_DENALI_PI_275 Register (Offset = 244Ch) [reset = 0h]

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Table 14-22257. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A44Ch

Figure 14-7384. EMIF_CTLCFG_DENALI_PI_275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TXSNR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSNR_F0							
R/W							
0h							

Table 14-22259. EMIF_CTLCFG_DENALI_PI_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PI_TXSNR_F0	R/W	0h	DRAM tXSNR value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.772 EMIF_CTLCFG_DENALI_PI_276 Register

1 EMIF_CTLCFG_DENALI_PI_276 Register (Offset = 2450h) [reset = 0h]

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Table 14-22260. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A450h**

Figure 14-7385. EMIF_CTLCFG_DENALI_PI_276 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT_F1							
R/W							
0h							

Table 14-22262. EMIF_CTLCFG_DENALI_PI_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F1	R/W	0h	DRAM tINIT value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.773 EMIF_CTLCFG_DENALI_PI_277 Register

1 EMIF_CTLCFG_DENALI_PI_277 Register (Offset = 2454h) [reset = 0h]

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Table 14-22263. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A454h**

Figure 14-7386. EMIF_CTLCFG_DENALI_PI_277 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT3_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT3_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT3_F1							
R/W							
0h							

Table 14-22265. EMIF_CTLCFG_DENALI_PI_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F1	R/W	0h	DRAM tINIT3 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.774 EMIF_CTLCFG_DENALI_PI_278 Register

1 EMIF_CTLCFG_DENALI_PI_278 Register (Offset = 2458h) [reset = 0h]

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Table 14-22266. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A458h**

Figure 14-7387. EMIF_CTLCFG_DENALI_PI_278 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT4_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT4_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT4_F1							
R/W							
0h							

Table 14-22268. EMIF_CTLCFG_DENALI_PI_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F1	R/W	0h	DRAM tINIT4 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.775 EMIF_CTLCFG_DENALI_PI_279 Register

1 EMIF_CTLCFG_DENALI_PI_279 Register (Offset = 245Ch) [reset = 0h]

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Table 14-22269. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A45Ch

Figure 14-7388. EMIF_CTLCFG_DENALI_PI_279 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F1							
R/W							
0h							

Table 14-22271. EMIF_CTLCFG_DENALI_PI_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F1	R/W	0h	DRAM tINIT5 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.776 EMIF_CTLCFG_DENALI_PI_280 Register

1 EMIF_CTLCFG_DENALI_PI_280 Register (Offset = 2460h) [reset = 0h]

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Table 14-22272. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A460h**

Figure 14-7389. EMIF_CTLCFG_DENALI_PI_280 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TXSNR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSNR_F1							
R/W							
0h							

Table 14-22274. EMIF_CTLCFG_DENALI_PI_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PI_TXSNR_F1	R/W	0h	DRAM tXSNR value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.777 EMIF_CTLCFG_DENALI_PI_281 Register

1 EMIF_CTLCFG_DENALI_PI_281 Register (Offset = 2464h) [reset = 0h]

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Table 14-22275. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A464h**

Figure 14-7390. EMIF_CTLCFG_DENALI_PI_281 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT_F2							
R/W							
0h							

Table 14-22277. EMIF_CTLCFG_DENALI_PI_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F2	R/W	0h	DRAM tINIT value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.778 EMIF_CTLCFG_DENALI_PI_282 Register

1 EMIF_CTLCFG_DENALI_PI_282 Register (Offset = 2468h) [reset = 0h]

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Table 14-22278. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A468h**

Figure 14-7391. EMIF_CTLCFG_DENALI_PI_282 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT3_F2							
R/W							
0h							

Table 14-22280. EMIF_CTLCFG_DENALI_PI_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F2	R/W	0h	DRAM tINIT3 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.779 EMIF_CTLCFG_DENALI_PI_283 Register

1 EMIF_CTLCFG_DENALI_PI_283 Register (Offset = 246Ch) [reset = 0h]

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Table 14-22281. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A46Ch**

Figure 14-7392. EMIF_CTLCFG_DENALI_PI_283 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT4_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT4_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT4_F2							
R/W							
0h							

Table 14-22283. EMIF_CTLCFG_DENALI_PI_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F2	R/W	0h	DRAM tINIT4 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.780 EMIF_CTLCFG_DENALI_PI_284 Register

1 EMIF_CTLCFG_DENALI_PI_284 Register (Offset = 2470h) [reset = 0h]

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Table 14-22284. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A470h**

Figure 14-7393. EMIF_CTLCFG_DENALI_PI_284 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F2							
R/W							
0h							

Table 14-22286. EMIF_CTLCFG_DENALI_PI_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F2	R/W	0h	DRAM tINIT5 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.781 EMIF_CTLCFG_DENALI_PI_285 Register

1 EMIF_CTLCFG_DENALI_PI_285 Register (Offset = 2474h) [reset = 0h]

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Table 14-22287. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A474h**

Figure 14-7394. EMIF_CTLCFG_DENALI_PI_285 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED54			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_RESERVED54							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TXSNR_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TXSNR_F2							
R/W							
0h							

Table 14-22289. EMIF_CTLCFG_DENALI_PI_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_RESERVED54	R/W	0h	Reserved
15:0	PI_TXSNR_F2	R/W	0h	DRAM tXSNR value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.782 EMIF_CTLCFG_DENALI_PI_286 Register

1 EMIF_CTLCFG_DENALI_PI_286 Register (Offset = 2478h) [reset = 0h]

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Table 14-22290. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A478h**

Figure 14-7395. EMIF_CTLCFG_DENALI_PI_286 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TZQCAL_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_TZQCAL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED55			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_RESERVED55							
R/W							
0h							

Table 14-22292. EMIF_CTLCFG_DENALI_PI_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED55	R/W	0h	Reserved

14.6.6.2.783 EMIF_CTLCFG_DENALI_PI_287 Register

1 EMIF_CTLCFG_DENALI_PI_287 Register (Offset = 247Ch) [reset = 0h]

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Table 14-22293. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A47Ch**

Figure 14-7396. EMIF_CTLCFG_DENALI_PI_287 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED56			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RESERVED56							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F0						
NONE	R/W						
0h	0h						

Table 14-22295. EMIF_CTLCFG_DENALI_PI_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED56	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.784 EMIF_CTLCFG_DENALI_PI_288 Register

1 EMIF_CTLCFG_DENALI_PI_288 Register (Offset = 2480h) [reset = 0h]

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Table 14-22296. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A480h**

Figure 14-7397. EMIF_CTLCFG_DENALI_PI_288 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TZQCAL_F1			
NONE				R/W			
0h				0h			

23	22	21	20	19	18	17	16
PI_TZQCAL_F1							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED57			
NONE				R/W			
0h				0h			

7	6	5	4	3	2	1	0
PI_RESERVED57							
R/W							
0h							

Table 14-22298. EMIF_CTLCFG_DENALI_PI_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED57	R/W	0h	Reserved

14.6.6.2.785 EMIF_CTLCFG_DENALI_PI_289 Register

1 EMIF_CTLCFG_DENALI_PI_289 Register (Offset = 2484h) [reset = 0h]

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Table 14-22299. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A484h**

Figure 14-7398. EMIF_CTLCFG_DENALI_PI_289 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED58</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_RESERVED58</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_TZQLAT_F1</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-22301. EMIF_CTLCFG_DENALI_PI_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED58	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.786 EMIF_CTLCFG_DENALI_PI_290 Register

1 EMIF_CTLCFG_DENALI_PI_290 Register (Offset = 2488h) [reset = 0h]

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Table 14-22302. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A488h**

Figure 14-7399. EMIF_CTLCFG_DENALI_PI_290 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TZQCAL_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TZQCAL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_RESERVED59			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_RESERVED59							
R/W							
0h							

Table 14-22304. EMIF_CTLCFG_DENALI_PI_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED59	R/W	0h	Reserved

14.6.6.2.787 EMIF_CTLCFG_DENALI_PI_291 Register

1 EMIF_CTLCFG_DENALI_PI_291 Register (Offset = 248Ch) [reset = 0h]

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Table 14-22305. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A48Ch**

Figure 14-7400. EMIF_CTLCFG_DENALI_PI_291 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED60			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RESERVED60							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F2						
NONE	R/W						
0h	0h						

Table 14-22307. EMIF_CTLCFG_DENALI_PI_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED60	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.788 EMIF_CTLCFG_DENALI_PI_292 Register

1 EMIF_CTLCFG_DENALI_PI_292 Register (Offset = 2490h) [reset = 0h]

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Table 14-22308. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A490h**

Figure 14-7401. EMIF_CTLCFG_DENALI_PI_292 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED62			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_RESERVED62							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED61			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_RESERVED61							
R/W							
0h							

Table 14-22310. EMIF_CTLCFG_DENALI_PI_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_RESERVED62	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED61	R/W	0h	Reserved

14.6.6.2.789 EMIF_CTLCFG_DENALI_PI_293 Register

1 EMIF_CTLCFG_DENALI_PI_293 Register (Offset = 2494h) [reset = 0h]

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Table 14-22311. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A494h**

Figure 14-7402. EMIF_CTLCFG_DENALI_PI_293 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_PREAMBLE_SUPPORT_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F0			
NONE				R/W			
0h				0h			

Table 14-22313. EMIF_CTLCFG_DENALI_PI_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_PREAMBLE_SUPPORT_F0	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_WDQ_OSC_DELTA_INDEX_F2	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 2. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_WDQ_OSC_DELTA_INDEX_F1	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 1. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQ_OSC_DELTA_INDEX_F0	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 0. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n

14.6.6.2.790 EMIF_CTLCFG_DENALI_PI_294 Register

1 EMIF_CTLCFG_DENALI_PI_294 Register (Offset = 2498h) [reset = 0h]

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Table 14-22314. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A498h**

Figure 14-7403. EMIF_CTLCFG_DENALI_PI_294 Name Register

31	30	29	28	27	26	25	24
RESERVED					PI_MEMDATA_RATIO_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PI_MEMDATA_RATIO_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_PREAMBLE_SUPPORT_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_PREAMBLE_SUPPORT_F1	
NONE						R/W	
0h						0h	

Table 14-22316. EMIF_CTLCFG_DENALI_PI_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_MEMDATA_RATIO_1	R/W	0h	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_MEMDATA_RATIO_0	R/W	0h	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_PREAMBLE_SUPPORT_F2	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_PREAMBLE_SUPPORT_F1	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n

14.6.6.2.791 EMIF_CTLCFG_DENALI_PI_295 Register

1 EMIF_CTLCFG_DENALI_PI_295 Register (Offset = 249Ch) [reset = 0h]

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Table 14-22317. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A49Ch**

Figure 14-7404. EMIF_CTLCFG_DENALI_PI_295 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ODT_WR_MAP_CS0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODT_RD_MAP_CS0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PI_MEMDATA_RATIO_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					PI_MEMDATA_RATIO_2		
NONE					R/W		
0h					0h		

Table 14-22319. EMIF_CTLCFG_DENALI_PI_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_ODT_WR_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a write. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODT_RD_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a read. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_MEMDATA_RATIO_3	R/W	0h	Defines the ratio of the DRAM device size on chip select 3 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_MEMDATA_RATIO_2	R/W	0h	Defines the ratio of the DRAM device size on chip select 2 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n

14.6.6.2.792 EMIF_CTLCFG_DENALI_PI_296 Register

1 EMIF_CTLCFG_DENALI_PI_296 Register (Offset = 24A0h) [reset = 0h]

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Table 14-22320. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4A0h**

Figure 14-7405. EMIF_CTLCFG_DENALI_PI_296 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ODT_WR_MAP_CS2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODT_RD_MAP_CS2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_ODT_WR_MAP_CS1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_ODT_RD_MAP_CS1			
NONE				R/W			
0h				0h			

Table 14-22322. EMIF_CTLCFG_DENALI_PI_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_ODT_WR_MAP_CS2	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 2. Set bit X to enable termination on csX when cs2 is performing a write. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODT_RD_MAP_CS2	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 2. Set bit X to enable termination on csX when cs2 is performing a read. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_ODT_WR_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a write. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_ODT_RD_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a read. Reset Source: ctl_amod_g_rst_n

14.6.6.2.793 EMIF_CTLCFG_DENALI_PI_297 Register

1 EMIF_CTLCFG_DENALI_PI_297 Register (Offset = 24A4h) [reset = 0h]

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Table 14-22323. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 A4A4h**

Figure 14-7406. EMIF_CTLCFG_DENALI_PI_297 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_VREF_VAL_DEV0_1						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PI_VREF_VAL_DEV0_0						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_ODT_WR_MAP_CS3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_ODT_RD_MAP_CS3			
NONE				R/W			
0h				0h			

Table 14-22325. EMIF_CTLCFG_DENALI_PI_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_VREF_VAL_DEV0_1	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_VREF_VAL_DEV0_0	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_ODT_WR_MAP_CS3	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 3. Set bit X to enable termination on csX when cs3 is performing a write. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_ODT_RD_MAP_CS3	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 3. Set bit X to enable termination on csX when cs3 is performing a read. Reset Source: ctl_amod_g_rst_n

14.6.6.2.794 EMIF_CTLCFG_DENALI_PI_298 Register

1 EMIF_CTLCFG_DENALI_PI_298 Register (Offset = 24A8h) [reset = 0h]

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Table 14-22326. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4A8h

Figure 14-7407. EMIF_CTLCFG_DENALI_PI_298 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_VREF_VAL_DEV1_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_VREF_VAL_DEV1_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_VREF_VAL_DEV0_3						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_VREF_VAL_DEV0_2						
NONE	R/W						
0h	0h						

Table 14-22328. EMIF_CTLCFG_DENALI_PI_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_VREF_VAL_DEV1_1	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_VREF_VAL_DEV1_0	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_VREF_VAL_DEV0_3	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 3. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_VREF_VAL_DEV0_2	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 2. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.795 EMIF_CTLCFG_DENALI_PI_299 Register

1 EMIF_CTLCFG_DENALI_PI_299 Register (Offset = 24ACh) [reset = 0h]

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Table 14-22329. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4ACh

Figure 14-7408. EMIF_CTLCFG_DENALI_PI_299 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_VREF_VAL_DEV2_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_VREF_VAL_DEV2_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_VREF_VAL_DEV1_3						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_VREF_VAL_DEV1_2						
NONE	R/W						
0h	0h						

Table 14-22331. EMIF_CTLCFG_DENALI_PI_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_VREF_VAL_DEV2_1	R/W	0h	Defines the range and value for VREF training for DRAM 2 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_VREF_VAL_DEV2_0	R/W	0h	Defines the range and value for VREF training for DRAM 2 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_VREF_VAL_DEV1_3	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 3. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_VREF_VAL_DEV1_2	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 2. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.796 *EMIF_CTLCFG_DENALI_PI_300 Register*

1 EMIF_CTLCFG_DENALI_PI_300 Register (Offset = 24B0h) [reset = 0h]

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Table 14-22332. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4B0h**

Figure 14-7409. EMIF_CTLCFG_DENALI_PI_300 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_VREF_VAL_DEV3_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_VREF_VAL_DEV3_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_VREF_VAL_DEV2_3						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_VREF_VAL_DEV2_2						
NONE	R/W						
0h	0h						

Table 14-22334. EMIF_CTLCFG_DENALI_PI_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_VREF_VAL_DEV3_1	R/W	0h	Defines the range and value for VREF training for DRAM 3 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_VREF_VAL_DEV3_0	R/W	0h	Defines the range and value for VREF training for DRAM 3 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_VREF_VAL_DEV2_3	R/W	0h	Defines the range and value for VREF training for DRAM 2 for CS 3. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_VREF_VAL_DEV2_2	R/W	0h	Defines the range and value for VREF training for DRAM 2 for CS 2. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.797 EMIF_CTLCFG_DENALI_PI_301 Register

1 EMIF_CTLCFG_DENALI_PI_301 Register (Offset = 24B4h) [reset = 0h]

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Table 14-22335. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4B4h

Figure 14-7410. EMIF_CTLCFG_DENALI_PI_301 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_SLICE_PER_DEV_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_SLICE_PER_DEV_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PI_VREF_VAL_DEV3_3						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PI_VREF_VAL_DEV3_2						
NONE	R/W						
0h	0h						

Table 14-22337. EMIF_CTLCFG_DENALI_PI_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_SLICE_PER_DEV_1	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SLICE_PER_DEV_0	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_VREF_VAL_DEV3_3	R/W	0h	Defines the range and value for VREF training for DRAM 3 for CS 3. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_VREF_VAL_DEV3_2	R/W	0h	Defines the range and value for VREF training for DRAM 3 for CS 2. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.798 EMIF_CTLCFG_DENALI_PI_302 Register

1 EMIF_CTLCFG_DENALI_PI_302 Register (Offset = 24B8h) [reset = 0h]

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Table 14-22338. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4B8h**

Figure 14-7411. EMIF_CTLCFG_DENALI_PI_302 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_MR6_VREF_0_1					
NONE		R					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PI_MR6_VREF_0_0					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED						PI_SLICE_PER_DEV_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_SLICE_PER_DEV_2	
NONE						R/W	
0h						0h	

Table 14-22340. EMIF_CTLCFG_DENALI_PI_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_MR6_VREF_0_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_MR6_VREF_0_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_SLICE_PER_DEV_3	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_SLICE_PER_DEV_2	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n

14.6.6.2.799 EMIF_CTLCFG_DENALI_PI_303 Register

1 EMIF_CTLCFG_DENALI_PI_303 Register (Offset = 24BCh) [reset = 0h]

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Table 14-22341. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4BCh

Figure 14-7412. EMIF_CTLCFG_DENALI_PI_303 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_MR6_VREF_1_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_MR6_VREF_1_0					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_MR6_VREF_0_3					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_MR6_VREF_0_2					
NONE		R					
0h		0h					

Table 14-22343. EMIF_CTLCFG_DENALI_PI_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_MR6_VREF_1_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_MR6_VREF_1_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_MR6_VREF_0_3	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_MR6_VREF_0_2	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.800 EMIF_CTLCFG_DENALI_PI_304 Register

1 EMIF_CTLCFG_DENALI_PI_304 Register (Offset = 24C0h) [reset = 0h]

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Table 14-22344. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4C0h

Figure 14-7413. EMIF_CTLCFG_DENALI_PI_304 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_MR6_VREF_2_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_MR6_VREF_2_0					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_MR6_VREF_1_3					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_MR6_VREF_1_2					
NONE		R					
0h		0h					

Table 14-22346. EMIF_CTLCFG_DENALI_PI_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_MR6_VREF_2_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_MR6_VREF_2_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_MR6_VREF_1_3	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_MR6_VREF_1_2	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.801 EMIF_CTLCFG_DENALI_PI_305 Register

1 EMIF_CTLCFG_DENALI_PI_305 Register (Offset = 24C4h) [reset = 0h]

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Table 14-22347. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4C4h**

Figure 14-7414. EMIF_CTLCFG_DENALI_PI_305 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_MR6_VREF_3_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_MR6_VREF_3_0					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_MR6_VREF_2_3					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_MR6_VREF_2_2					
NONE		R					
0h		0h					

Table 14-22349. EMIF_CTLCFG_DENALI_PI_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_MR6_VREF_3_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_MR6_VREF_3_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_MR6_VREF_2_3	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_MR6_VREF_2_2	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.802 EMIF_CTLCFG_DENALI_PI_306 Register

1 EMIF_CTLCFG_DENALI_PI_306 Register (Offset = 24C8h) [reset = 0h]

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Table 14-22350. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4C8h**

Figure 14-7415. EMIF_CTLCFG_DENALI_PI_306 Name Register

31	30	29	28	27	26	25	24
PI_MR15_DATA_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR13_DATA_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_MR6_VREF_3_3					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_MR6_VREF_3_2					
NONE		R					
0h		0h					

Table 14-22352. EMIF_CTLCFG_DENALI_PI_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR15_DATA_0	R/W	0h	Data to program into memory mode register 15 for chip select 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR13_DATA_0	R/W	0h	Data to program into memory mode register 13 for chip select 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_MR6_VREF_3_3	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_MR6_VREF_3_2	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.803 EMIF_CTLCFG_DENALI_PI_307 Register

1 EMIF_CTLCFG_DENALI_PI_307 Register (Offset = 24CCh) [reset = 0h]

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Table 14-22353. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4CCh

Figure 14-7416. EMIF_CTLCFG_DENALI_PI_307 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_MR20_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR17_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR16_DATA_0							
R/W							
0h							

Table 14-22355. EMIF_CTLCFG_DENALI_PI_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_MR20_DATA_0	R/W	0h	Data to program into memory mode register 20 for chip select 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR17_DATA_0	R/W	0h	Data to program into memory mode register 17 for chip select 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR16_DATA_0	R/W	0h	Data to program into memory mode register 16 for chip select 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.804 EMIF_CTLCFG_DENALI_PI_308 Register

1 EMIF_CTLCFG_DENALI_PI_308 Register (Offset = 24D0h) [reset = 0h]

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Table 14-22356. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4D0h

Figure 14-7417. EMIF_CTLCFG_DENALI_PI_308 Name Register

31	30	29	28	27	26	25	24
PI_MR40_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR32_DATA_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR32_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR32_DATA_0							
R/W							
0h							

Table 14-22358. EMIF_CTLCFG_DENALI_PI_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR40_DATA_0	R/W	0h	Data to program into memory mode register 40 for chip select 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR32_DATA_0	R/W	0h	Data to program into memory mode register 32 for chip select 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.805 EMIF_CTLCFG_DENALI_PI_309 Register

1 EMIF_CTLCFG_DENALI_PI_309 Register (Offset = 24D4h) [reset = 0h]

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Table 14-22359. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4D4h**

Figure 14-7418. EMIF_CTLCFG_DENALI_PI_309 Name Register

31	30	29	28	27	26	25	24
PI_MR17_DATA_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR16_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR15_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR13_DATA_1							
R/W							
0h							

Table 14-22361. EMIF_CTLCFG_DENALI_PI_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR17_DATA_1	R/W	0h	Data to program into memory mode register 17 for chip select 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR16_DATA_1	R/W	0h	Data to program into memory mode register 16 for chip select 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR15_DATA_1	R/W	0h	Data to program into memory mode register 15 for chip select 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR13_DATA_1	R/W	0h	Data to program into memory mode register 13 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.806 EMIF_CTLCFG_DENALI_PI_310 Register

1 EMIF_CTLCFG_DENALI_PI_310 Register (Offset = 24D8h) [reset = 0h]

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Table 14-22362. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4D8h**

Figure 14-7419. EMIF_CTLCFG_DENALI_PI_310 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MR32_DATA_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PI_MR32_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR32_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR20_DATA_1							
R/W							
0h							

Table 14-22364. EMIF_CTLCFG_DENALI_PI_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	PI_MR32_DATA_1	R/W	0h	Data to program into memory mode register 32 for chip select 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR20_DATA_1	R/W	0h	Data to program into memory mode register 20 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.807 EMIF_CTLCFG_DENALI_PI_311 Register

1 EMIF_CTLCFG_DENALI_PI_311 Register (Offset = 24DCh) [reset = 0h]

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Table 14-22365. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4DCh**

Figure 14-7420. EMIF_CTLCFG_DENALI_PI_311 Name Register

31	30	29	28	27	26	25	24
PI_MR16_DATA_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR15_DATA_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR13_DATA_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR40_DATA_1							
R/W							
0h							

Table 14-22367. EMIF_CTLCFG_DENALI_PI_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR16_DATA_2	R/W	0h	Data to program into memory mode register 16 for chip select 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR15_DATA_2	R/W	0h	Data to program into memory mode register 15 for chip select 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR13_DATA_2	R/W	0h	Data to program into memory mode register 13 for chip select 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR40_DATA_1	R/W	0h	Data to program into memory mode register 40 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.808 EMIF_CTLCFG_DENALI_PI_312 Register

1 EMIF_CTLCFG_DENALI_PI_312 Register (Offset = 24E0h) [reset = 0h]

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Table 14-22368. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4E0h**

Figure 14-7421. EMIF_CTLCFG_DENALI_PI_312 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_MR20_DATA_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR17_DATA_2							
R/W							
0h							

Table 14-22370. EMIF_CTLCFG_DENALI_PI_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_MR20_DATA_2	R/W	0h	Data to program into memory mode register 20 for chip select 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR17_DATA_2	R/W	0h	Data to program into memory mode register 17 for chip select 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.809 EMIF_CTLCFG_DENALI_PI_313 Register

1 EMIF_CTLCFG_DENALI_PI_313 Register (Offset = 24E4h) [reset = 0h]

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Table 14-22371. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4E4h**

Figure 14-7422. EMIF_CTLCFG_DENALI_PI_313 Name Register

31	30	29	28	27	26	25	24
PI_MR40_DATA_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR32_DATA_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR32_DATA_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR32_DATA_2							
R/W							
0h							

Table 14-22373. EMIF_CTLCFG_DENALI_PI_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR40_DATA_2	R/W	0h	Data to program into memory mode register 40 for chip select 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR32_DATA_2	R/W	0h	Data to program into memory mode register 32 for chip select 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.810 EMIF_CTLCFG_DENALI_PI_314 Register

1 EMIF_CTLCFG_DENALI_PI_314 Register (Offset = 24E8h) [reset = 0h]

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Table 14-22374. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4E8h

Figure 14-7423. EMIF_CTLCFG_DENALI_PI_314 Name Register

31	30	29	28	27	26	25	24
PI_MR17_DATA_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR16_DATA_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR15_DATA_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR13_DATA_3							
R/W							
0h							

Table 14-22376. EMIF_CTLCFG_DENALI_PI_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR17_DATA_3	R/W	0h	Data to program into memory mode register 17 for chip select 3. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR16_DATA_3	R/W	0h	Data to program into memory mode register 16 for chip select 3. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR15_DATA_3	R/W	0h	Data to program into memory mode register 15 for chip select 3. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR13_DATA_3	R/W	0h	Data to program into memory mode register 13 for chip select 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.811 EMIF_CTLCFG_DENALI_PI_315 Register

1 EMIF_CTLCFG_DENALI_PI_315 Register (Offset = 24ECh) [reset = 0h]

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Table 14-22377. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4ECh**

Figure 14-7424. EMIF_CTLCFG_DENALI_PI_315 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MR32_DATA_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR32_DATA_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR32_DATA_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR20_DATA_3							
R/W							
0h							

Table 14-22379. EMIF_CTLCFG_DENALI_PI_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	PI_MR32_DATA_3	R/W	0h	Data to program into memory mode register 32 for chip select 3. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR20_DATA_3	R/W	0h	Data to program into memory mode register 20 for chip select 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.812 EMIF_CTLCFG_DENALI_PI_316 Register

1 EMIF_CTLCFG_DENALI_PI_316 Register (Offset = 24F0h) [reset = 0h]

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Table 14-22380. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4F0h**

Figure 14-7425. EMIF_CTLCFG_DENALI_PI_316 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_CKE_MUX_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_CKE_MUX_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_CKE_MUX_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PI_MR40_DATA_3							
R/W							
0h							

Table 14-22382. EMIF_CTLCFG_DENALI_PI_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_CKE_MUX_2	R/W	0h	Command pin CKE_2 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_CKE_MUX_1	R/W	0h	Command pin CKE_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CKE_MUX_0	R/W	0h	Command pin CKE_0 mux selector Reset Source: ctl_amod_g_rst_n
7:0	PI_MR40_DATA_3	R/W	0h	Data to program into memory mode register 40 for chip select 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.813 EMIF_CTLCFG_DENALI_PI_317 Register

1 EMIF_CTLCFG_DENALI_PI_317 Register (Offset = 24F4h) [reset = 0h]

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Table 14-22383. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4F4h

Figure 14-7426. EMIF_CTLCFG_DENALI_PI_317 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_CS_MUX_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_CS_MUX_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_CS_MUX_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_CKE_MUX_3				
NONE			R/W				
0h			0h				

Table 14-22385. EMIF_CTLCFG_DENALI_PI_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_CS_MUX_2	R/W	0h	Command pin CS_2 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_CS_MUX_1	R/W	0h	Command pin CS_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CS_MUX_0	R/W	0h	Command pin CS_0 mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_CKE_MUX_3	R/W	0h	Command pin CKE_3 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.814 EMIF_CTLCFG_DENALI_PI_318 Register

1 EMIF_CTLCFG_DENALI_PI_318 Register (Offset = 24F8h) [reset = 0h]

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Table 14-22386. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A4F8h**

Figure 14-7427. EMIF_CTLCFG_DENALI_PI_318 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_ODT_MUX_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_ODT_MUX_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_ODT_MUX_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_CS_MUX_3				
NONE			R/W				
0h			0h				

Table 14-22388. EMIF_CTLCFG_DENALI_PI_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_ODT_MUX_2	R/W	0h	Command pin ODT_2 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_ODT_MUX_1	R/W	0h	Command pin ODT_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_ODT_MUX_0	R/W	0h	Command pin ODT_0 mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_CS_MUX_3	R/W	0h	Command pin CS_3 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.815 EMIF_CTLCFG_DENALI_PI_319 Register

1 EMIF_CTLCFG_DENALI_PI_319 Register (Offset = 24FCh) [reset = 0h]

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Table 14-22389. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A4FCh

Figure 14-7428. EMIF_CTLCFG_DENALI_PI_319 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_RESET_N_MUX_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_RESET_N_MUX_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_RESET_N_MUX_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_ODT_MUX_3				
NONE			R/W				
0h			0h				

Table 14-22391. EMIF_CTLCFG_DENALI_PI_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_RESET_N_MUX_2	R/W	0h	Command pin RESET_N_2 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_RESET_N_MUX_1	R/W	0h	Command pin RESET_N_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RESET_N_MUX_0	R/W	0h	Command pin RESET_N_0 mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_ODT_MUX_3	R/W	0h	Command pin ODT_3 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.816 EMIF_CTLCFG_DENALI_PI_320 Register

1 EMIF_CTLCFG_DENALI_PI_320 Register (Offset = 2500h) [reset = 0h]

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Table 14-22392. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A500h**

Figure 14-7429. EMIF_CTLCFG_DENALI_PI_320 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MRSINGLE_DATA_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PI_MRSINGLE_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MRSINGLE_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			PI_RESET_N_MUX_3				
NONE			R/W				
0h			0h				

Table 14-22394. EMIF_CTLCFG_DENALI_PI_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	PI_MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write to chip select 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RESET_N_MUX_3	R/W	0h	Command pin RESET_N_3 mux selector Reset Source: ctl_amod_g_rst_n

14.6.6.2.817 EMIF_CTLCFG_DENALI_PI_321 Register

1 EMIF_CTLCFG_DENALI_PI_321 Register (Offset = 2504h) [reset = 0h]

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Table 14-22395. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A504h**

Figure 14-7430. EMIF_CTLCFG_DENALI_PI_321 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MRSINGLE_DATA_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MRSINGLE_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MRSINGLE_DATA_1							
R/W							
0h							

Table 14-22397. EMIF_CTLCFG_DENALI_PI_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write to chip select 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.818 EMIF_CTLCFG_DENALI_PI_322 Register

1 EMIF_CTLCFG_DENALI_PI_322 Register (Offset = 2508h) [reset = 0h]

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Table 14-22398. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A508h**

Figure 14-7431. EMIF_CTLCFG_DENALI_PI_322 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MRSINGLE_DATA_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MRSINGLE_DATA_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MRSINGLE_DATA_2							
R/W							
0h							

Table 14-22400. EMIF_CTLCFG_DENALI_PI_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MRSINGLE_DATA_2	R/W	0h	Data to program into memory mode register single write to chip select 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.819 EMIF_CTLCFG_DENALI_PI_323 Register

1 EMIF_CTLCFG_DENALI_PI_323 Register (Offset = 250Ch) [reset = 1000000h]

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Table 14-22401. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A50Ch

Figure 14-7432. EMIF_CTLCFG_DENALI_PI_323 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQ_CAL_START_MAP_0			
NONE				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MRSINGLE_DATA_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MRSINGLE_DATA_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MRSINGLE_DATA_3							
R/W							
0h							

Table 14-22403. EMIF_CTLCFG_DENALI_PI_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_ZQ_CAL_START_MAP_0	R/W	1h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MRSINGLE_DATA_3	R/W	0h	Data to program into memory mode register single write to chip select 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.820 EMIF_CTLCFG_DENALI_PI_324 Register

1 EMIF_CTLCFG_DENALI_PI_324 Register (Offset = 2510h) [reset = 4020201h]

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Table 14-22404. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A510h**

Figure 14-7433. EMIF_CTLCFG_DENALI_PI_324 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQ_CAL_START_MAP_2			
NONE				R/W			
0h				4h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_ZQ_CAL_LATCH_MAP_1			
NONE				R/W			
0h				2h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_ZQ_CAL_START_MAP_1			
NONE				R/W			
0h				2h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_ZQ_CAL_LATCH_MAP_0			
NONE				R/W			
0h				1h			

Table 14-22406. EMIF_CTLCFG_DENALI_PI_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_ZQ_CAL_START_MAP_2	R/W	4h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 2 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ZQ_CAL_LATCH_MAP_1	R/W	2h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_ZQ_CAL_START_MAP_1	R/W	2h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-22406. EMIF_CTLCFG_DENALI_PI_324 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PI_ZQ_CAL_LATCH_MAP_0	R/W	1h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.821 EMIF_CTLCFG_DENALI_PI_325 Register

1 EMIF_CTLCFG_DENALI_PI_325 Register (Offset = 2514h) [reset = 80804h]

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Table 14-22407. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A514h

Figure 14-7434. EMIF_CTLCFG_DENALI_PI_325 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_ZQ_CAL_LATCH_MAP_3			
NONE				R/W			
0h				8h			
15	14	13	12	11	10	9	8
RESERVED				PI_ZQ_CAL_START_MAP_3			
NONE				R/W			
0h				8h			
7	6	5	4	3	2	1	0
RESERVED				PI_ZQ_CAL_LATCH_MAP_2			
NONE				R/W			
0h				4h			

Table 14-22409. EMIF_CTLCFG_DENALI_PI_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PI_ZQ_CAL_LATCH_MAP_3	R/W	8h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 3 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_ZQ_CAL_START_MAP_3	R/W	8h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 3 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_ZQ_CAL_LATCH_MAP_2	R/W	4h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 2 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n

14.6.6.2.822 EMIF_CTLCFG_DENALI_PI_326 Register

1 EMIF_CTLCFG_DENALI_PI_326 Register (Offset = 2518h) [reset = 0h]

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Table 14-22410. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A518h**

Figure 14-7435. EMIF_CTLCFG_DENALI_PI_326 Name Register

31	30	29	28	27	26	25	24
PI_DQS_OSC_BASE_VALUE_1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_DQS_OSC_BASE_VALUE_1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_DQS_OSC_BASE_VALUE_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_DQS_OSC_BASE_VALUE_0_0							
R/W							
0h							

Table 14-22412. EMIF_CTLCFG_DENALI_PI_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_DQS_OSC_BASE_VALUE_1_0	R/W	0h	Base value for comparison of oscillator measurement for device 1 of rank 0 Reset Source: ctl_amod_g_rst_n
15:0	PI_DQS_OSC_BASE_VALUE_0_0	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.823 EMIF_CTLCFG_DENALI_PI_327 Register

1 EMIF_CTLCFG_DENALI_PI_327 Register (Offset = 251Ch) [reset = 0h]

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Table 14-22413. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A51Ch**

Figure 14-7436. EMIF_CTLCFG_DENALI_PI_327 Name Register

31	30	29	28	27	26	25	24
PI_DQS_OSC_BASE_VALUE_1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_DQS_OSC_BASE_VALUE_1_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_DQS_OSC_BASE_VALUE_0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_DQS_OSC_BASE_VALUE_0_1							
R/W							
0h							

Table 14-22415. EMIF_CTLCFG_DENALI_PI_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_DQS_OSC_BASE_VALUE_1_1	R/W	0h	Base value for comparison of oscillator measurement for device 1 of rank 1 Reset Source: ctl_amod_g_rst_n
15:0	PI_DQS_OSC_BASE_VALUE_0_1	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.824 EMIF_CTLCFG_DENALI_PI_328 Register

1 EMIF_CTLCFG_DENALI_PI_328 Register (Offset = 2520h) [reset = 0h]

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Table 14-22416. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A520h

Figure 14-7437. EMIF_CTLCFG_DENALI_PI_328 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F0_0							
R/W							
0h							

Table 14-22418. EMIF_CTLCFG_DENALI_PI_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.825 EMIF_CTLCFG_DENALI_PI_329 Register

1 EMIF_CTLCFG_DENALI_PI_329 Register (Offset = 2524h) [reset = 0h]

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Table 14-22419. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A524h**

Figure 14-7438. EMIF_CTLCFG_DENALI_PI_329 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F0_0							
R/W							
0h							

Table 14-22421. EMIF_CTLCFG_DENALI_PI_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.826 EMIF_CTLCFG_DENALI_PI_330 Register

1 EMIF_CTLCFG_DENALI_PI_330 Register (Offset = 2528h) [reset = 0h]

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Table 14-22422. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A528h**

Figure 14-7439. EMIF_CTLCFG_DENALI_PI_330 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_0							
R/W							
0h							

Table 14-22424. EMIF_CTLCFG_DENALI_PI_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.827 EMIF_CTLCFG_DENALI_PI_331 Register

1 EMIF_CTLCFG_DENALI_PI_331 Register (Offset = 252Ch) [reset = 0h]

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Table 14-22425. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A52Ch**

Figure 14-7440. EMIF_CTLCFG_DENALI_PI_331 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22427. EMIF_CTLCFG_DENALI_PI_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.828 EMIF_CTLCFG_DENALI_PI_332 Register

1 EMIF_CTLCFG_DENALI_PI_332 Register (Offset = 2530h) [reset = 0h]

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Table 14-22428. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A530h**

Figure 14-7441. EMIF_CTLCFG_DENALI_PI_332 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F0_0							
R/W							
0h							

Table 14-22430. EMIF_CTLCFG_DENALI_PI_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.829 EMIF_CTLCFG_DENALI_PI_333 Register

1 EMIF_CTLCFG_DENALI_PI_333 Register (Offset = 2534h) [reset = 0h]

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Table 14-22431. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A534h

Figure 14-7442. EMIF_CTLCFG_DENALI_PI_333 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F0_0							
R/W							
0h							

Table 14-22433. EMIF_CTLCFG_DENALI_PI_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.830 EMIF_CTLCFG_DENALI_PI_334 Register

1 EMIF_CTLCFG_DENALI_PI_334 Register (Offset = 2538h) [reset = 0h]

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Table 14-22434. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A538h

Figure 14-7443. EMIF_CTLCFG_DENALI_PI_334 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F0_0							
R/W							
0h							

Table 14-22436. EMIF_CTLCFG_DENALI_PI_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.831 EMIF_CTLCFG_DENALI_PI_335 Register

1 EMIF_CTLCFG_DENALI_PI_335 Register (Offset = 253Ch) [reset = 0h]

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Table 14-22437. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A53Ch

Figure 14-7444. EMIF_CTLCFG_DENALI_PI_335 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F0_0							
R/W							
0h							

Table 14-22439. EMIF_CTLCFG_DENALI_PI_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.832 EMIF_CTLCFG_DENALI_PI_336 Register

1 EMIF_CTLCFG_DENALI_PI_336 Register (Offset = 2540h) [reset = 0h]

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Table 14-22440. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A540h**

Figure 14-7445. EMIF_CTLCFG_DENALI_PI_336 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR0_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR0_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR0_DATA_F1_0							
R/W							
0h							

Table 14-22442. EMIF_CTLCFG_DENALI_PI_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.833 EMIF_CTLCFG_DENALI_PI_337 Register

1 EMIF_CTLCFG_DENALI_PI_337 Register (Offset = 2544h) [reset = 0h]

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Table 14-22443. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A544h**

Figure 14-7446. EMIF_CTLCFG_DENALI_PI_337 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F1_0							
R/W							
0h							

Table 14-22445. EMIF_CTLCFG_DENALI_PI_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.834 EMIF_CTLCFG_DENALI_PI_338 Register

1 EMIF_CTLCFG_DENALI_PI_338 Register (Offset = 2548h) [reset = 0h]

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Table 14-22446. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A548h**

Figure 14-7447. EMIF_CTLCFG_DENALI_PI_338 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F1_0							
R/W							
0h							

Table 14-22448. EMIF_CTLCFG_DENALI_PI_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.835 EMIF_CTLCFG_DENALI_PI_339 Register

1 EMIF_CTLCFG_DENALI_PI_339 Register (Offset = 254Ch) [reset = 0h]

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Table 14-22449. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A54Ch**

Figure 14-7448. EMIF_CTLCFG_DENALI_PI_339 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_0							
R/W							
0h							

Table 14-22451. EMIF_CTLCFG_DENALI_PI_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.836 EMIF_CTLCFG_DENALI_PI_340 Register

1 EMIF_CTLCFG_DENALI_PI_340 Register (Offset = 2550h) [reset = 0h]

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Table 14-22452. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A550h

Figure 14-7449. EMIF_CTLCFG_DENALI_PI_340 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F1_0							
R/W							
0h							

Table 14-22454. EMIF_CTLCFG_DENALI_PI_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.837 EMIF_CTLCFG_DENALI_PI_341 Register

1 EMIF_CTLCFG_DENALI_PI_341 Register (Offset = 2554h) [reset = 0h]

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Table 14-22455. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A554h**

Figure 14-7450. EMIF_CTLCFG_DENALI_PI_341 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR5_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR5_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR5_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22457. EMIF_CTLCFG_DENALI_PI_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.838 EMIF_CTLCFG_DENALI_PI_342 Register

1 EMIF_CTLCFG_DENALI_PI_342 Register (Offset = 2558h) [reset = 0h]

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Table 14-22458. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A558h**

Figure 14-7451. EMIF_CTLCFG_DENALI_PI_342 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MR11_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22460. EMIF_CTLCFG_DENALI_PI_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.839 EMIF_CTLCFG_DENALI_PI_343 Register

1 EMIF_CTLCFG_DENALI_PI_343 Register (Offset = 255Ch) [reset = 0h]

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Table 14-22461. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A55Ch

Figure 14-7452. EMIF_CTLCFG_DENALI_PI_343 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F1_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F1_0							
R/W							
0h							

Table 14-22463. EMIF_CTLCFG_DENALI_PI_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.840 EMIF_CTLCFG_DENALI_PI_344 Register

1 EMIF_CTLCFG_DENALI_PI_344 Register (Offset = 2560h) [reset = 0h]

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Table 14-22464. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A560h**

Figure 14-7453. EMIF_CTLCFG_DENALI_PI_344 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR0_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22466. EMIF_CTLCFG_DENALI_PI_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.841 EMIF_CTLCFG_DENALI_PI_345 Register

1 EMIF_CTLCFG_DENALI_PI_345 Register (Offset = 2564h) [reset = 0h]

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Table 14-22467. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A564h**

Figure 14-7454. EMIF_CTLCFG_DENALI_PI_345 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F2_0							
R/W							
0h							

Table 14-22469. EMIF_CTLCFG_DENALI_PI_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.842 EMIF_CTLCFG_DENALI_PI_346 Register

1 EMIF_CTLCFG_DENALI_PI_346 Register (Offset = 2568h) [reset = 0h]

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Table 14-22470. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A568h**

Figure 14-7455. EMIF_CTLCFG_DENALI_PI_346 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_0							
R/W							
0h							

Table 14-22472. EMIF_CTLCFG_DENALI_PI_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.843 EMIF_CTLCFG_DENALI_PI_347 Register

1 EMIF_CTLCFG_DENALI_PI_347 Register (Offset = 256Ch) [reset = 0h]

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Table 14-22473. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A56Ch

Figure 14-7456. EMIF_CTLCFG_DENALI_PI_347 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F2_0							
R/W							
0h							

Table 14-22475. EMIF_CTLCFG_DENALI_PI_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.844 EMIF_CTLCFG_DENALI_PI_348 Register

1 EMIF_CTLCFG_DENALI_PI_348 Register (Offset = 2570h) [reset = 0h]

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Table 14-22476. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A570h**

Figure 14-7457. EMIF_CTLCFG_DENALI_PI_348 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22478. EMIF_CTLCFG_DENALI_PI_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.845 EMIF_CTLCFG_DENALI_PI_349 Register

1 EMIF_CTLCFG_DENALI_PI_349 Register (Offset = 2574h) [reset = 0h]

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Table 14-22479. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A574h**

Figure 14-7458. EMIF_CTLCFG_DENALI_PI_349 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR5_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR5_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR5_DATA_F2_0							
R/W							
0h							

Table 14-22481. EMIF_CTLCFG_DENALI_PI_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.846 EMIF_CTLCFG_DENALI_PI_350 Register

1 EMIF_CTLCFG_DENALI_PI_350 Register (Offset = 2578h) [reset = 0h]

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Table 14-22482. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A578h**

Figure 14-7459. EMIF_CTLCFG_DENALI_PI_350 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F2_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F2_0							
R/W							
0h							

Table 14-22484. EMIF_CTLCFG_DENALI_PI_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.847 EMIF_CTLCFG_DENALI_PI_351 Register

1 EMIF_CTLCFG_DENALI_PI_351 Register (Offset = 257Ch) [reset = 0h]

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Table 14-22485. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A57Ch

Figure 14-7460. EMIF_CTLCFG_DENALI_PI_351 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F2_0							
R/W							
0h							

Table 14-22487. EMIF_CTLCFG_DENALI_PI_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.848 EMIF_CTLCFG_DENALI_PI_352 Register

1 EMIF_CTLCFG_DENALI_PI_352 Register (Offset = 2580h) [reset = 0h]

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Table 14-22488. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A580h**

Figure 14-7461. EMIF_CTLCFG_DENALI_PI_352 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F0_1							
R/W							
0h							

Table 14-22490. EMIF_CTLCFG_DENALI_PI_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.849 EMIF_CTLCFG_DENALI_PI_353 Register

1 EMIF_CTLCFG_DENALI_PI_353 Register (Offset = 2584h) [reset = 0h]

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Table 14-22491. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A584h**

Figure 14-7462. EMIF_CTLCFG_DENALI_PI_353 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F0_1							
R/W							
0h							

Table 14-22493. EMIF_CTLCFG_DENALI_PI_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.850 EMIF_CTLCFG_DENALI_PI_354 Register

1 EMIF_CTLCFG_DENALI_PI_354 Register (Offset = 2588h) [reset = 0h]

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Table 14-22494. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A588h**

Figure 14-7463. EMIF_CTLCFG_DENALI_PI_354 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_1							
R/W							
0h							

Table 14-22496. EMIF_CTLCFG_DENALI_PI_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.851 EMIF_CTLCFG_DENALI_PI_355 Register

1 EMIF_CTLCFG_DENALI_PI_355 Register (Offset = 258Ch) [reset = 0h]

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Table 14-22497. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A58Ch

Figure 14-7464. EMIF_CTLCFG_DENALI_PI_355 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F0_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
PI_MR3_DATA_F0_1							
R/W							
0h							

7	6	5	4	3	2	1	0
PI_MR3_DATA_F0_1							
R/W							
0h							

Table 14-22499. EMIF_CTLCFG_DENALI_PI_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.852 EMIF_CTLCFG_DENALI_PI_356 Register

1 EMIF_CTLCFG_DENALI_PI_356 Register (Offset = 2590h) [reset = 0h]

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Table 14-22500. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A590h**

Figure 14-7465. EMIF_CTLCFG_DENALI_PI_356 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22502. EMIF_CTLCFG_DENALI_PI_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.853 EMIF_CTLCFG_DENALI_PI_357 Register

1 EMIF_CTLCFG_DENALI_PI_357 Register (Offset = 2594h) [reset = 0h]

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Table 14-22503. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A594h**

Figure 14-7466. EMIF_CTLCFG_DENALI_PI_357 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR5_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR5_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR5_DATA_F0_1							
R/W							
0h							

Table 14-22505. EMIF_CTLCFG_DENALI_PI_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.854 EMIF_CTLCFG_DENALI_PI_358 Register

1 EMIF_CTLCFG_DENALI_PI_358 Register (Offset = 2598h) [reset = 0h]

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Table 14-22506. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A598h**

Figure 14-7467. EMIF_CTLCFG_DENALI_PI_358 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F0_1							
R/W							
0h							

Table 14-22508. EMIF_CTLCFG_DENALI_PI_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.855 EMIF_CTLCFG_DENALI_PI_359 Register

1 EMIF_CTLCFG_DENALI_PI_359 Register (Offset = 259Ch) [reset = 0h]

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Table 14-22509. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A59Ch

Figure 14-7468. EMIF_CTLCFG_DENALI_PI_359 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F0_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F0_1							
R/W							
0h							

Table 14-22511. EMIF_CTLCFG_DENALI_PI_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.856 EMIF_CTLCFG_DENALI_PI_360 Register

1 EMIF_CTLCFG_DENALI_PI_360 Register (Offset = 25A0h) [reset = 0h]

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Table 14-22512. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5A0h**

Figure 14-7469. EMIF_CTLCFG_DENALI_PI_360 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR0_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22514. EMIF_CTLCFG_DENALI_PI_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.857 EMIF_CTLCFG_DENALI_PI_361 Register

1 EMIF_CTLCFG_DENALI_PI_361 Register (Offset = 25A4h) [reset = 0h]

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Table 14-22515. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5A4h**

Figure 14-7470. EMIF_CTLCFG_DENALI_PI_361 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR1_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22517. EMIF_CTLCFG_DENALI_PI_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.858 EMIF_CTLCFG_DENALI_PI_362 Register

1 EMIF_CTLCFG_DENALI_PI_362 Register (Offset = 25A8h) [reset = 0h]

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Table 14-22518. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5A8h**

Figure 14-7471. EMIF_CTLCFG_DENALI_PI_362 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F1_1							
R/W							
0h							

Table 14-22520. EMIF_CTLCFG_DENALI_PI_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.859 EMIF_CTLCFG_DENALI_PI_363 Register

1 EMIF_CTLCFG_DENALI_PI_363 Register (Offset = 25ACh) [reset = 0h]

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Table 14-22521. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5ACh**

Figure 14-7472. EMIF_CTLCFG_DENALI_PI_363 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_1							
R/W							
0h							

Table 14-22523. EMIF_CTLCFG_DENALI_PI_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.860 EMIF_CTLCFG_DENALI_PI_364 Register

1 EMIF_CTLCFG_DENALI_PI_364 Register (Offset = 25B0h) [reset = 0h]

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Table 14-22524. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5B0h

Figure 14-7473. EMIF_CTLCFG_DENALI_PI_364 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F1_1							
R/W							
0h							

Table 14-22526. EMIF_CTLCFG_DENALI_PI_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.861 EMIF_CTLCFG_DENALI_PI_365 Register

1 EMIF_CTLCFG_DENALI_PI_365 Register (Offset = 25B4h) [reset = 0h]

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Table 14-22527. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5B4h**

Figure 14-7474. EMIF_CTLCFG_DENALI_PI_365 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F1_1							
R/W							
0h							

Table 14-22529. EMIF_CTLCFG_DENALI_PI_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.862 EMIF_CTLCFG_DENALI_PI_366 Register

1 EMIF_CTLCFG_DENALI_PI_366 Register (Offset = 25B8h) [reset = 0h]

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Table 14-22530. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5B8h**

Figure 14-7475. EMIF_CTLCFG_DENALI_PI_366 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F1_1							
R/W							
0h							

Table 14-22532. EMIF_CTLCFG_DENALI_PI_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.863 EMIF_CTLCFG_DENALI_PI_367 Register

1 EMIF_CTLCFG_DENALI_PI_367 Register (Offset = 25BCh) [reset = 0h]

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Table 14-22533. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5BCh

Figure 14-7476. EMIF_CTLCFG_DENALI_PI_367 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F1_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F1_1							
R/W							
0h							

Table 14-22535. EMIF_CTLCFG_DENALI_PI_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.864 EMIF_CTLCFG_DENALI_PI_368 Register

1 EMIF_CTLCFG_DENALI_PI_368 Register (Offset = 25C0h) [reset = 0h]

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Table 14-22536. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5C0h**

Figure 14-7477. EMIF_CTLCFG_DENALI_PI_368 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F2_1							
R/W							
0h							

Table 14-22538. EMIF_CTLCFG_DENALI_PI_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.865 EMIF_CTLCFG_DENALI_PI_369 Register

1 EMIF_CTLCFG_DENALI_PI_369 Register (Offset = 25C4h) [reset = 0h]

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Table 14-22539. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5C4h**

Figure 14-7478. EMIF_CTLCFG_DENALI_PI_369 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F2_1							
R/W							
0h							

Table 14-22541. EMIF_CTLCFG_DENALI_PI_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.866 EMIF_CTLCFG_DENALI_PI_370 Register

1 EMIF_CTLCFG_DENALI_PI_370 Register (Offset = 25C8h) [reset = 0h]

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Table 14-22542. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5C8h

Figure 14-7479. EMIF_CTLCFG_DENALI_PI_370 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F2_1							
R/W							
0h							

Table 14-22544. EMIF_CTLCFG_DENALI_PI_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.867 EMIF_CTLCFG_DENALI_PI_371 Register

1 EMIF_CTLCFG_DENALI_PI_371 Register (Offset = 25CCh) [reset = 0h]

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Table 14-22545. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5CCh**

Figure 14-7480. EMIF_CTLCFG_DENALI_PI_371 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F2_1							
R/W							
0h							

Table 14-22547. EMIF_CTLCFG_DENALI_PI_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.868 EMIF_CTLCFG_DENALI_PI_372 Register

1 EMIF_CTLCFG_DENALI_PI_372 Register (Offset = 25D0h) [reset = 0h]

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Table 14-22548. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5D0h**

Figure 14-7481. EMIF_CTLCFG_DENALI_PI_372 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F2_1							
R/W							
0h							

Table 14-22550. EMIF_CTLCFG_DENALI_PI_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.869 EMIF_CTLCFG_DENALI_PI_373 Register

1 EMIF_CTLCFG_DENALI_PI_373 Register (Offset = 25D4h) [reset = 0h]

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Table 14-22551. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5D4h

Figure 14-7482. EMIF_CTLCFG_DENALI_PI_373 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F2_1							
R/W							
0h							

Table 14-22553. EMIF_CTLCFG_DENALI_PI_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.870 EMIF_CTLCFG_DENALI_PI_374 Register

1 EMIF_CTLCFG_DENALI_PI_374 Register (Offset = 25D8h) [reset = 0h]

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Table 14-22554. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 A5D8h**

Figure 14-7483. EMIF_CTLCFG_DENALI_PI_374 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F2_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F2_1							
R/W							
0h							

Table 14-22556. EMIF_CTLCFG_DENALI_PI_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.871 EMIF_CTLCFG_DENALI_PI_375 Register

1 EMIF_CTLCFG_DENALI_PI_375 Register (Offset = 25DCh) [reset = 0h]

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Table 14-22557. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5DCh**

Figure 14-7484. EMIF_CTLCFG_DENALI_PI_375 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F2_1							
R/W							
0h							

Table 14-22559. EMIF_CTLCFG_DENALI_PI_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.872 EMIF_CTLCFG_DENALI_PI_376 Register

1 EMIF_CTLCFG_DENALI_PI_376 Register (Offset = 25E0h) [reset = 0h]

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Table 14-22560. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5E0h

Figure 14-7485. EMIF_CTLCFG_DENALI_PI_376 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F0_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F0_2							
R/W							
0h							

Table 14-22562. EMIF_CTLCFG_DENALI_PI_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_2	R/W	0h	Data to program into memory mode register 0 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.873 EMIF_CTLCFG_DENALI_PI_377 Register

1 EMIF_CTLCFG_DENALI_PI_377 Register (Offset = 25E4h) [reset = 0h]

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Table 14-22563. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5E4h

Figure 14-7486. EMIF_CTLCFG_DENALI_PI_377 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F0_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F0_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F0_2							
R/W							
0h							

Table 14-22565. EMIF_CTLCFG_DENALI_PI_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.874 EMIF_CTLCFG_DENALI_PI_378 Register

1 EMIF_CTLCFG_DENALI_PI_378 Register (Offset = 25E8h) [reset = 0h]

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Table 14-22566. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5E8h**

Figure 14-7487. EMIF_CTLCFG_DENALI_PI_378 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F0_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_2							
R/W							
0h							

Table 14-22568. EMIF_CTLCFG_DENALI_PI_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.875 EMIF_CTLCFG_DENALI_PI_379 Register

1 EMIF_CTLCFG_DENALI_PI_379 Register (Offset = 25ECh) [reset = 0h]

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Table 14-22569. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5ECh**

Figure 14-7488. EMIF_CTLCFG_DENALI_PI_379 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F0_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F0_2							
R/W							
0h							

Table 14-22571. EMIF_CTLCFG_DENALI_PI_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.876 EMIF_CTLCFG_DENALI_PI_380 Register

1 EMIF_CTLCFG_DENALI_PI_380 Register (Offset = 25F0h) [reset = 0h]

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Table 14-22572. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5F0h

Figure 14-7489. EMIF_CTLCFG_DENALI_PI_380 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR4_DATA_F0_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22574. EMIF_CTLCFG_DENALI_PI_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_2	R/W	0h	Data to program into memory mode register 4 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.877 EMIF_CTLCFG_DENALI_PI_381 Register

1 EMIF_CTLCFG_DENALI_PI_381 Register (Offset = 25F4h) [reset = 0h]

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Table 14-22575. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5F4h**

Figure 14-7490. EMIF_CTLCFG_DENALI_PI_381 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR5_DATA_F0_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR5_DATA_F0_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR5_DATA_F0_2							
R/W							
0h							

Table 14-22577. EMIF_CTLCFG_DENALI_PI_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_2	R/W	0h	Data to program into memory mode register 5 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.878 EMIF_CTLCFG_DENALI_PI_382 Register

1 EMIF_CTLCFG_DENALI_PI_382 Register (Offset = 25F8h) [reset = 0h]

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Table 14-22578. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A5F8h**

Figure 14-7491. EMIF_CTLCFG_DENALI_PI_382 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F0_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F0_2							
R/W							
0h							

Table 14-22580. EMIF_CTLCFG_DENALI_PI_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_2	R/W	0h	Data to program into memory mode register 6 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.879 EMIF_CTLCFG_DENALI_PI_383 Register

1 EMIF_CTLCFG_DENALI_PI_383 Register (Offset = 25FCh) [reset = 0h]

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Table 14-22581. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A5FCh

Figure 14-7492. EMIF_CTLCFG_DENALI_PI_383 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F0_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F0_2							
R/W							
0h							

Table 14-22583. EMIF_CTLCFG_DENALI_PI_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.880 EMIF_CTLCFG_DENALI_PI_384 Register

1 EMIF_CTLCFG_DENALI_PI_384 Register (Offset = 2600h) [reset = 0h]

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Table 14-22584. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A600h**

Figure 14-7493. EMIF_CTLCFG_DENALI_PI_384 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F1_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F1_2							
R/W							
0h							

Table 14-22586. EMIF_CTLCFG_DENALI_PI_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_2	R/W	0h	Data to program into memory mode register 0 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.881 EMIF_CTLCFG_DENALI_PI_385 Register

1 EMIF_CTLCFG_DENALI_PI_385 Register (Offset = 2604h) [reset = 0h]

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Table 14-22587. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A604h

Figure 14-7494. EMIF_CTLCFG_DENALI_PI_385 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F1_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F1_2							
R/W							
0h							

Table 14-22589. EMIF_CTLCFG_DENALI_PI_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.882 EMIF_CTLCFG_DENALI_PI_386 Register

1 EMIF_CTLCFG_DENALI_PI_386 Register (Offset = 2608h) [reset = 0h]

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Table 14-22590. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A608h

Figure 14-7495. EMIF_CTLCFG_DENALI_PI_386 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F1_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F1_2							
R/W							
0h							

Table 14-22592. EMIF_CTLCFG_DENALI_PI_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.883 EMIF_CTLCFG_DENALI_PI_387 Register

1 EMIF_CTLCFG_DENALI_PI_387 Register (Offset = 260Ch) [reset = 0h]

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Table 14-22593. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A60Ch**

Figure 14-7496. EMIF_CTLCFG_DENALI_PI_387 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_2							
R/W							
0h							

Table 14-22595. EMIF_CTLCFG_DENALI_PI_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.884 EMIF_CTLCFG_DENALI_PI_388 Register

1 EMIF_CTLCFG_DENALI_PI_388 Register (Offset = 2610h) [reset = 0h]

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Table 14-22596. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A610h

Figure 14-7497. EMIF_CTLCFG_DENALI_PI_388 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F1_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F1_2							
R/W							
0h							

Table 14-22598. EMIF_CTLCFG_DENALI_PI_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_2	R/W	0h	Data to program into memory mode register 4 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.885 EMIF_CTLCFG_DENALI_PI_389 Register

1 EMIF_CTLCFG_DENALI_PI_389 Register (Offset = 2614h) [reset = 0h]

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Table 14-22599. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A614h**

Figure 14-7498. EMIF_CTLCFG_DENALI_PI_389 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F1_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F1_2							
R/W							
0h							

Table 14-22601. EMIF_CTLCFG_DENALI_PI_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_2	R/W	0h	Data to program into memory mode register 5 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.886 EMIF_CTLCFG_DENALI_PI_390 Register

1 EMIF_CTLCFG_DENALI_PI_390 Register (Offset = 2618h) [reset = 0h]

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Table 14-22602. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A618h**

Figure 14-7499. EMIF_CTLCFG_DENALI_PI_390 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F1_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F1_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F1_2							
R/W							
0h							

Table 14-22604. EMIF_CTLCFG_DENALI_PI_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_2	R/W	0h	Data to program into memory mode register 6 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.887 EMIF_CTLCFG_DENALI_PI_391 Register

1 EMIF_CTLCFG_DENALI_PI_391 Register (Offset = 261Ch) [reset = 0h]

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Table 14-22605. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A61Ch

Figure 14-7500. EMIF_CTLCFG_DENALI_PI_391 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F1_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F1_2							
R/W							
0h							

Table 14-22607. EMIF_CTLCFG_DENALI_PI_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.888 EMIF_CTLCFG_DENALI_PI_392 Register

1 EMIF_CTLCFG_DENALI_PI_392 Register (Offset = 2620h) [reset = 0h]

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Table 14-22608. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A620h

Figure 14-7501. EMIF_CTLCFG_DENALI_PI_392 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F2_2							
R/W							
0h							

Table 14-22610. EMIF_CTLCFG_DENALI_PI_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_2	R/W	0h	Data to program into memory mode register 0 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.889 EMIF_CTLCFG_DENALI_PI_393 Register

1 EMIF_CTLCFG_DENALI_PI_393 Register (Offset = 2624h) [reset = 0h]

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Table 14-22611. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A624h**

Figure 14-7502. EMIF_CTLCFG_DENALI_PI_393 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR1_DATA_F2_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F2_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F2_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22613. EMIF_CTLCFG_DENALI_PI_393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.890 EMIF_CTLCFG_DENALI_PI_394 Register

1 EMIF_CTLCFG_DENALI_PI_394 Register (Offset = 2628h) [reset = 0h]

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Table 14-22614. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A628h**

Figure 14-7503. EMIF_CTLCFG_DENALI_PI_394 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_2							
R/W							
0h							

Table 14-22616. EMIF_CTLCFG_DENALI_PI_394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.891 EMIF_CTLCFG_DENALI_PI_395 Register

1 EMIF_CTLCFG_DENALI_PI_395 Register (Offset = 262Ch) [reset = 0h]

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Table 14-22617. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A62Ch**

Figure 14-7504. EMIF_CTLCFG_DENALI_PI_395 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F2_2							
R/W							
0h							

Table 14-22619. EMIF_CTLCFG_DENALI_PI_395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.892 EMIF_CTLCFG_DENALI_PI_396 Register

1 EMIF_CTLCFG_DENALI_PI_396 Register (Offset = 2630h) [reset = 0h]

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Table 14-22620. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A630h**

Figure 14-7505. EMIF_CTLCFG_DENALI_PI_396 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F2_2							
R/W							
0h							

Table 14-22622. EMIF_CTLCFG_DENALI_PI_396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_2	R/W	0h	Data to program into memory mode register 4 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.893 EMIF_CTLCFG_DENALI_PI_397 Register

1 EMIF_CTLCFG_DENALI_PI_397 Register (Offset = 2634h) [reset = 0h]

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Table 14-22623. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A634h**

Figure 14-7506. EMIF_CTLCFG_DENALI_PI_397 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F2_2							
R/W							
0h							

Table 14-22625. EMIF_CTLCFG_DENALI_PI_397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_2	R/W	0h	Data to program into memory mode register 5 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.894 EMIF_CTLCFG_DENALI_PI_398 Register

1 EMIF_CTLCFG_DENALI_PI_398 Register (Offset = 2638h) [reset = 0h]

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Table 14-22626. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A638h

Figure 14-7507. EMIF_CTLCFG_DENALI_PI_398 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F2_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F2_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F2_2							
R/W							
0h							

Table 14-22628. EMIF_CTLCFG_DENALI_PI_398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_2	R/W	0h	Data to program into memory mode register 6 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.895 EMIF_CTLCFG_DENALI_PI_399 Register

1 EMIF_CTLCFG_DENALI_PI_399 Register (Offset = 263Ch) [reset = 0h]

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Table 14-22629. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A63Ch

Figure 14-7508. EMIF_CTLCFG_DENALI_PI_399 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F2_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F2_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F2_2							
R/W							
0h							

Table 14-22631. EMIF_CTLCFG_DENALI_PI_399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.896 EMIF_CTLCFG_DENALI_PI_400 Register

1 EMIF_CTLCFG_DENALI_PI_400 Register (Offset = 2640h) [reset = 0h]

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Table 14-22632. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A640h

Figure 14-7509. EMIF_CTLCFG_DENALI_PI_400 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR0_DATA_F0_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR0_DATA_F0_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR0_DATA_F0_3							
R/W							
0h							

Table 14-22634. EMIF_CTLCFG_DENALI_PI_400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_3	R/W	0h	Data to program into memory mode register 0 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.897 EMIF_CTLCFG_DENALI_PI_401 Register

1 EMIF_CTLCFG_DENALI_PI_401 Register (Offset = 2644h) [reset = 0h]

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Table 14-22635. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 A644h**

Figure 14-7510. EMIF_CTLCFG_DENALI_PI_401 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F0_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F0_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F0_3							
R/W							
0h							

Table 14-22637. EMIF_CTLCFG_DENALI_PI_401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.898 EMIF_CTLCFG_DENALI_PI_402 Register

1 EMIF_CTLCFG_DENALI_PI_402 Register (Offset = 2648h) [reset = 0h]

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Table 14-22638. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A648h**

Figure 14-7511. EMIF_CTLCFG_DENALI_PI_402 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F0_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F0_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F0_3							
R/W							
0h							

Table 14-22640. EMIF_CTLCFG_DENALI_PI_402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.899 EMIF_CTLCFG_DENALI_PI_403 Register

1 EMIF_CTLCFG_DENALI_PI_403 Register (Offset = 264Ch) [reset = 0h]

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Table 14-22641. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A64Ch**

Figure 14-7512. EMIF_CTLCFG_DENALI_PI_403 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR3_DATA_F0_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22643. EMIF_CTLCFG_DENALI_PI_403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.900 EMIF_CTLCFG_DENALI_PI_404 Register

1 EMIF_CTLCFG_DENALI_PI_404 Register (Offset = 2650h) [reset = 0h]

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Table 14-22644. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A650h**

Figure 14-7513. EMIF_CTLCFG_DENALI_PI_404 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F0_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F0_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F0_3							
R/W							
0h							

Table 14-22646. EMIF_CTLCFG_DENALI_PI_404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_3	R/W	0h	Data to program into memory mode register 4 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.901 EMIF_CTLCFG_DENALI_PI_405 Register

1 EMIF_CTLCFG_DENALI_PI_405 Register (Offset = 2654h) [reset = 0h]

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Table 14-22647. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A654h**

Figure 14-7514. EMIF_CTLCFG_DENALI_PI_405 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F0_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F0_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F0_3							
R/W							
0h							

Table 14-22649. EMIF_CTLCFG_DENALI_PI_405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_3	R/W	0h	Data to program into memory mode register 5 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.902 EMIF_CTLCFG_DENALI_PI_406 Register

1 EMIF_CTLCFG_DENALI_PI_406 Register (Offset = 2658h) [reset = 0h]

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Table 14-22650. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A658h**

Figure 14-7515. EMIF_CTLCFG_DENALI_PI_406 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F0_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F0_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F0_3							
R/W							
0h							

Table 14-22652. EMIF_CTLCFG_DENALI_PI_406 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_3	R/W	0h	Data to program into memory mode register 6 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.903 EMIF_CTLCFG_DENALI_PI_407 Register

1 EMIF_CTLCFG_DENALI_PI_407 Register (Offset = 265Ch) [reset = 0h]

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Table 14-22653. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A65Ch

Figure 14-7516. EMIF_CTLCFG_DENALI_PI_407 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F0_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F0_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F0_3							
R/W							
0h							

Table 14-22655. EMIF_CTLCFG_DENALI_PI_407 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.904 EMIF_CTLCFG_DENALI_PI_408 Register

1 EMIF_CTLCFG_DENALI_PI_408 Register (Offset = 2660h) [reset = 0h]

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Table 14-22656. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A660h**

Figure 14-7517. EMIF_CTLCFG_DENALI_PI_408 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F1_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F1_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F1_3							
R/W							
0h							

Table 14-22658. EMIF_CTLCFG_DENALI_PI_408 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_3	R/W	0h	Data to program into memory mode register 0 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.905 EMIF_CTLCFG_DENALI_PI_409 Register

1 EMIF_CTLCFG_DENALI_PI_409 Register (Offset = 2664h) [reset = 0h]

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Table 14-22659. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A664h**

Figure 14-7518. EMIF_CTLCFG_DENALI_PI_409 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR1_DATA_F1_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR1_DATA_F1_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR1_DATA_F1_3							
R/W							
0h							

Table 14-22661. EMIF_CTLCFG_DENALI_PI_409 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.906 EMIF_CTLCFG_DENALI_PI_410 Register

1 EMIF_CTLCFG_DENALI_PI_410 Register (Offset = 2668h) [reset = 0h]

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Table 14-22662. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A668h

Figure 14-7519. EMIF_CTLCFG_DENALI_PI_410 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR2_DATA_F1_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR2_DATA_F1_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR2_DATA_F1_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22664. EMIF_CTLCFG_DENALI_PI_410 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.907 EMIF_CTLCFG_DENALI_PI_411 Register

1 EMIF_CTLCFG_DENALI_PI_411 Register (Offset = 266Ch) [reset = 0h]

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Table 14-22665. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A66Ch**

Figure 14-7520. EMIF_CTLCFG_DENALI_PI_411 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_3							
R/W							
0h							

Table 14-22667. EMIF_CTLCFG_DENALI_PI_411 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.908 EMIF_CTLCFG_DENALI_PI_412 Register

1 EMIF_CTLCFG_DENALI_PI_412 Register (Offset = 2670h) [reset = 0h]

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Table 14-22668. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A670h**

Figure 14-7521. EMIF_CTLCFG_DENALI_PI_412 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F1_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F1_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F1_3							
R/W							
0h							

Table 14-22670. EMIF_CTLCFG_DENALI_PI_412 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_3	R/W	0h	Data to program into memory mode register 4 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.909 EMIF_CTLCFG_DENALI_PI_413 Register

1 EMIF_CTLCFG_DENALI_PI_413 Register (Offset = 2674h) [reset = 0h]

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Table 14-22671. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A674h**

Figure 14-7522. EMIF_CTLCFG_DENALI_PI_413 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F1_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F1_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F1_3							
R/W							
0h							

Table 14-22673. EMIF_CTLCFG_DENALI_PI_413 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_3	R/W	0h	Data to program into memory mode register 5 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.910 EMIF_CTLCFG_DENALI_PI_414 Register

1 EMIF_CTLCFG_DENALI_PI_414 Register (Offset = 2678h) [reset = 0h]

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Table 14-22674. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A678h**

Figure 14-7523. EMIF_CTLCFG_DENALI_PI_414 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MR11_DATA_F1_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR6_DATA_F1_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22676. EMIF_CTLCFG_DENALI_PI_414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_3	R/W	0h	Data to program into memory mode register 6 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.911 EMIF_CTLCFG_DENALI_PI_415 Register

1 EMIF_CTLCFG_DENALI_PI_415 Register (Offset = 267Ch) [reset = 0h]

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Table 14-22677. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A67Ch**

Figure 14-7524. EMIF_CTLCFG_DENALI_PI_415 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F1_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F1_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F1_3							
R/W							
0h							

Table 14-22679. EMIF_CTLCFG_DENALI_PI_415 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.912 EMIF_CTLCFG_DENALI_PI_416 Register

1 EMIF_CTLCFG_DENALI_PI_416 Register (Offset = 2680h) [reset = 0h]

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Table 14-22680. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A680h

Figure 14-7525. EMIF_CTLCFG_DENALI_PI_416 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR0_DATA_F2_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR0_DATA_F2_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR0_DATA_F2_3							
R/W							
0h							

Table 14-22682. EMIF_CTLCFG_DENALI_PI_416 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_3	R/W	0h	Data to program into memory mode register 0 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.913 EMIF_CTLCFG_DENALI_PI_417 Register

1 EMIF_CTLCFG_DENALI_PI_417 Register (Offset = 2684h) [reset = 0h]

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Table 14-22683. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A684h**

Figure 14-7526. EMIF_CTLCFG_DENALI_PI_417 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F2_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F2_3							
R/W							
0h							

Table 14-22685. EMIF_CTLCFG_DENALI_PI_417 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.914 EMIF_CTLCFG_DENALI_PI_418 Register

1 EMIF_CTLCFG_DENALI_PI_418 Register (Offset = 2688h) [reset = 0h]

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Table 14-22686. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A688h**

Figure 14-7527. EMIF_CTLCFG_DENALI_PI_418 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F2_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_3							
R/W							
0h							

Table 14-22688. EMIF_CTLCFG_DENALI_PI_418 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.915 EMIF_CTLCFG_DENALI_PI_419 Register

1 EMIF_CTLCFG_DENALI_PI_419 Register (Offset = 268Ch) [reset = 0h]

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Table 14-22689. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A68Ch**

Figure 14-7528. EMIF_CTLCFG_DENALI_PI_419 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F2_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F2_3							
R/W							
0h							

Table 14-22691. EMIF_CTLCFG_DENALI_PI_419 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.916 EMIF_CTLCFG_DENALI_PI_420 Register

1 EMIF_CTLCFG_DENALI_PI_420 Register (Offset = 2690h) [reset = 0h]

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Table 14-22692. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A690h**

Figure 14-7529. EMIF_CTLCFG_DENALI_PI_420 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F2_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F2_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F2_3							
R/W							
0h							

Table 14-22694. EMIF_CTLCFG_DENALI_PI_420 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_3	R/W	0h	Data to program into memory mode register 4 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.917 EMIF_CTLCFG_DENALI_PI_421 Register

1 EMIF_CTLCFG_DENALI_PI_421 Register (Offset = 2694h) [reset = 0h]

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Table 14-22695. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A694h**

Figure 14-7530. EMIF_CTLCFG_DENALI_PI_421 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F2_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F2_3							
R/W							
0h							

Table 14-22697. EMIF_CTLCFG_DENALI_PI_421 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_3	R/W	0h	Data to program into memory mode register 5 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.918 EMIF_CTLCFG_DENALI_PI_422 Register

1 EMIF_CTLCFG_DENALI_PI_422 Register (Offset = 2698h) [reset = 0h]

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Table 14-22698. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 A698h**

Figure 14-7531. EMIF_CTLCFG_DENALI_PI_422 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F2_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F2_3
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F2_3							
R/W							
0h							

Table 14-22700. EMIF_CTLCFG_DENALI_PI_422 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_3	R/W	0h	Data to program into memory mode register 6 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.919 EMIF_CTLCFG_DENALI_PI_423 Register

1 EMIF_CTLCFG_DENALI_PI_423 Register (Offset = 269Ch) [reset = 0h]

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Table 14-22701. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 A69Ch

Figure 14-7532. EMIF_CTLCFG_DENALI_PI_423 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F2_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F2_3							
R/W							
0h							

Table 14-22703. EMIF_CTLCFG_DENALI_PI_423 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.920 EMIF_CTLCFG_DENALI_PHY_0 Register

1 EMIF_CTLCFG_DENALI_PHY_0 Register (Offset = 4000h) [reset = 0h]

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Table 14-22704. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C000h

Figure 14-7533. EMIF_CTLCFG_DENALI_PHY_0 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WR_BYPASS_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_0						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		

Table 14-22706. EMIF_CTLCFG_DENALI_PHY_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Write data clock bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_0	R/W	0h	Controls PCLK/PARK pin for pad for slice 0 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_0	R/W	0h	RX_PCLK boot clock frequency selection for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.921 EMIF_CTLCFG_DENALI_PHY_1 Register

1 EMIF_CTLCFG_DENALI_PHY_1 Register (Offset = 4004h) [reset = 0h]

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Table 14-22707. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C004h

Figure 14-7534. EMIF_CTLCFG_DENALI_PHY_1 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_0			
NONE				R/W			
0h				0h			

Table 14-22709. EMIF_CTLCFG_DENALI_PHY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_0	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	R/W	0h	Write DQS bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.922 EMIF_CTLCFG_DENALI_PHY_2 Register

1 EMIF_CTLCFG_DENALI_PHY_2 Register (Offset = 4008h) [reset = 0h]

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Table 14-22710. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C008h**

Figure 14-7535. EMIF_CTLCFG_DENALI_PHY_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22712. EMIF_CTLCFG_DENALI_PHY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_0	R/W	0h	Two_cycle_preamble for bypass mode for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.923 EMIF_CTLCFG_DENALI_PHY_3 Register

1 EMIF_CTLCFG_DENALI_PHY_3 Register (Offset = 400Ch) [reset = 0h]

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Table 14-22713. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C00Ch

Figure 14-7536. EMIF_CTLCFG_DENALI_PHY_3 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_0					
NONE		R/W					
0h		0h					

Table 14-22715. EMIF_CTLCFG_DENALI_PHY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-22715. EMIF_CTLCFG_DENALI_PHY_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.924 EMIF_CTLCFG_DENALI_PHY_4 Register

1 EMIF_CTLCFG_DENALI_PHY_4 Register (Offset = 4010h) [reset = 0h]

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Table 14-22716. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C010h**

Figure 14-7537. EMIF_CTLCFG_DENALI_PHY_4 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ6_SHIFT_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ5_SHIFT_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ4_SHIFT_0					
NONE		R/W					
0h		0h					

Table 14-22718. EMIF_CTLCFG_DENALI_PHY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-22718. EMIF_CTLCFG_DENALI_PHY_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.925 EMIF_CTLCFG_DENALI_PHY_5 Register

1 EMIF_CTLCFG_DENALI_PHY_5 Register (Offset = 4014h) [reset = 1000000h]

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Table 14-22719. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C014h**

Figure 14-7538. EMIF_CTLCFG_DENALI_PHY_5 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_0
NONE							R/W
0h							1h
23	22	21	20	19	18	17	16
RESERVED						PHY_PER_RANK_CS_MAP_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_0					
NONE		R/W					
0h		0h					

Table 14-22721. EMIF_CTLCFG_DENALI_PHY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_PER_CS_TRAINING_MULTICAST_EN_0	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_PER_RANK_CS_MAP_0	R/W	0h	Per-rank CS map for slice 0. Setting a bit uses that CS for the rank, bit [0] uses CS0, bit [1] uses CS1, etc. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-22721. EMIF_CTLCFG_DENALI_PHY_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.926 EMIF_CTLCFG_DENALI_PHY_6 Register

1 EMIF_CTLCFG_DENALI_PHY_6 Register (Offset = 4018h) [reset = 0h]

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Table 14-22722. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C018h**

Figure 14-7539. EMIF_CTLCFG_DENALI_PHY_6 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_LP4_BOOT_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_PER_CS_TRAINING_INDEX_0
NONE							R/W
0h							0h

Table 14-22724. EMIF_CTLCFG_DENALI_PHY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_LP4_BOOT_RDDATA_EN_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_INDEX_0	R/W	0h	For per-rank training, indicates which rank's paramters are read/ written for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.927 EMIF_CTLCFG_DENALI_PHY_7 Register

1 EMIF_CTLCFG_DENALI_PHY_7 Register (Offset = 401Ch) [reset = 0h]

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Table 14-22725. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C01Ch

Figure 14-7540. EMIF_CTLCFG_DENALI_PHY_7 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_0			
NONE				R/W			
0h				0h			

Table 14-22727. EMIF_CTLCFG_DENALI_PHY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 0. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_LP4_BOOT_RPTR_UPDATE_0	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.928 EMIF_CTLCFG_DENALI_PHY_8 Register

1 EMIF_CTLCFG_DENALI_PHY_8 Register (Offset = 4020h) [reset = 0h]

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Table 14-22728. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C020h**

Figure 14-7541. EMIF_CTLCFG_DENALI_PHY_8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_LPBK_DFX_TIMEOUT_EN_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_LPBK_CONTROL_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_LPBK_CONTROL_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_CTRL_LPBK_EN_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-22730. EMIF_CTLCFG_DENALI_PHY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LPBK_DFX_TIMEOUT_EN_0	R/W	0h	Loopback read only test timeout mechanism enable for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_LPBK_CONTROL_0	R/W	0h	Loopback control bits for slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CTRL_LPBK_EN_0	R/W	0h	Loopback control en for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.929 EMIF_CTLCFG_DENALI_PHY_9 Register

1 EMIF_CTLCFG_DENALI_PHY_9 Register (Offset = 4024h) [reset = 0h]

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Table 14-22731. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C024h**

Figure 14-7542. EMIF_CTLCFG_DENALI_PHY_9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_GATE_DELAY_COMP_DISABLE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-22733. EMIF_CTLCFG_DENALI_PHY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_GATE_DELAY_COMP_DISABLE_0	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.930 EMIF_CTLCFG_DENALI_PHY_10 Register

1 EMIF_CTLCFG_DENALI_PHY_10 Register (Offset = 4028h) [reset = 0h]

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Table 14-22734. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C028h**

Figure 14-7543. EMIF_CTLCFG_DENALI_PHY_10 Name Register

31	30	29	28	27	26	25	24
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							

Table 14-22736. EMIF_CTLCFG_DENALI_PHY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_0	R/W	0h	Auto timing marging control bits for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.931 EMIF_CTLCFG_DENALI_PHY_11 Register

1 EMIF_CTLCFG_DENALI_PHY_11 Register (Offset = 402Ch) [reset = 0h]

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Table 14-22737. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C02Ch**

Figure 14-7544. EMIF_CTLCFG_DENALI_PHY_11 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_0			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							

Table 14-22739. EMIF_CTLCFG_DENALI_PHY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_0	R	0h	Observation register for the auto_timing_margin for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.932 EMIF_CTLCFG_DENALI_PHY_12 Register

1 EMIF_CTLCFG_DENALI_PHY_12 Register (Offset = 4030h) [reset = 1000000h]

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Table 14-22740. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C030h**

Figure 14-7545. EMIF_CTLCFG_DENALI_PHY_12 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_0						
NONE	R/W						
0h	1h						
23	22	21	20	19	18	17	16
RESERVED							PHY_PDA_MODE_EN_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_DQ_IDLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DQ_IDLE_0							
R/W							
0h							

Table 14-22742. EMIF_CTLCFG_DENALI_PHY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_0	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_0	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.933 EMIF_CTLCFG_DENALI_PHY_13 Register

1 EMIF_CTLCFG_DENALI_PHY_13 Register (Offset = 4034h) [reset = 0h]

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Table 14-22743. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C034h

Figure 14-7546. EMIF_CTLCFG_DENALI_PHY_13 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTI_PATT_RST_DISABLE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_RDLVL_MULTI_PATT_ENABLE_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_PRBS_PATTERN_MASK_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PRBS_PATTERN_MASK_0							
R/W							
0h							

Table 14-22745. EMIF_CTLCFG_DENALI_PHY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_0	R/W	0h	Read Leveling read level windows disable reset for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_0	R/W	0h	Read Leveling Multi-pattern enable for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.934 EMIF_CTLCFG_DENALI_PHY_14 Register

1 EMIF_CTLCFG_DENALI_PHY_14 Register (Offset = 4038h) [reset = 0h]

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Table 14-22746. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C038h**

Figure 14-7547. EMIF_CTLCFG_DENALI_PHY_14 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	

23	22	21	20	19	18	17	16
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED	PHY_VREF_TRAIN_OBS_0						
NONE	R						
0h	0h						

7	6	5	4	3	2	1	0
RESERVED		PHY_VREF_INITIAL_STEPSIZE_0					
NONE		R/W					
0h		0h					

Table 14-22748. EMIF_CTLCFG_DENALI_PHY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_0	R	0h	Observation register for best vref value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_0	R/W	0h	Data slice initial VREF training step size for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.935 EMIF_CTLCFG_DENALI_PHY_15 Register

1 EMIF_CTLCFG_DENALI_PHY_15 Register (Offset = 403Ch) [reset = 0h]

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Table 14-22749. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C03Ch**

Figure 14-7548. EMIF_CTLCFG_DENALI_PHY_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_GATE_SMPL1_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_SNAP_OBS_REGS_0
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_0			
NONE				R/W			
0h				0h			

Table 14-22751. EMIF_CTLCFG_DENALI_PHY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_0	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.936 EMIF_CTLCFG_DENALI_PHY_16 Register

1 EMIF_CTLCFG_DENALI_PHY_16 Register (Offset = 4040h) [reset = 0h]

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Table 14-22752. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C040h**

Figure 14-7549. EMIF_CTLCFG_DENALI_PHY_16 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MEM_CLASS_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LPDDR_0
NONE							R/W
0h							0h

Table 14-22754. EMIF_CTLCFG_DENALI_PHY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_0	R/W	0h	Indicates the type of DRAM for slice 0. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_0	R/W	0h	Adds a cycle of delay for the slice 0 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.6.6.2.937 EMIF_CTLCFG_DENALI_PHY_17 Register

1 EMIF_CTLCFG_DENALI_PHY_17 Register (Offset = 4044h) [reset = 0h]

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Table 14-22755. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C044h

Figure 14-7550. EMIF_CTLCFG_DENALI_PHY_17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ON_FLY_GATE_ADJUST_EN_0	
NONE						R/W	
0h						0h	

Table 14-22757. EMIF_CTLCFG_DENALI_PHY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_0	R/W	0h	Control the on-the-fly gate adjustment for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.938 EMIF_CTLCFG_DENALI_PHY_18 Register

1 EMIF_CTLCFG_DENALI_PHY_18 Register (Offset = 4048h) [reset = 0h]

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Table 14-22758. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C048h**

Figure 14-7551. EMIF_CTLCFG_DENALI_PHY_18 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_0							
R							
0h							

Table 14-22760. EMIF_CTLCFG_DENALI_PHY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_0	R	0h	Report the on-the-fly gate measurement result for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.939 EMIF_CTLCFG_DENALI_PHY_19 Register

1 EMIF_CTLCFG_DENALI_PHY_19 Register (Offset = 404Ch) [reset = 0h]

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Table 14-22761. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C04Ch**

Figure 14-7552. EMIF_CTLCFG_DENALI_PHY_19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_0
NONE							R/W
0h							0h

Table 14-22763. EMIF_CTLCFG_DENALI_PHY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_PST_AMBLE_0	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DFI40_POLARITY_0	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.940 EMIF_CTLCFG_DENALI_PHY_20 Register

1 EMIF_CTLCFG_DENALI_PHY_20 Register (Offset = 4050h) [reset = 0h]

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Table 14-22764. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C050h**

Figure 14-7553. EMIF_CTLCFG_DENALI_PHY_20 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_0							
R/W							
0h							

Table 14-22766. EMIF_CTLCFG_DENALI_PHY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_0	R/W	0h	Read leveling pattern 8 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.941 EMIF_CTLCFG_DENALI_PHY_21 Register

1 EMIF_CTLCFG_DENALI_PHY_21 Register (Offset = 4054h) [reset = 0h]

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Table 14-22767. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C054h**

Figure 14-7554. EMIF_CTLCFG_DENALI_PHY_21 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_PATT9_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_PATT9_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_PATT9_0							
R/W							
0h							

Table 14-22769. EMIF_CTLCFG_DENALI_PHY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_0	R/W	0h	Read leveling pattern 9 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.942 EMIF_CTLCFG_DENALI_PHY_22 Register

1 EMIF_CTLCFG_DENALI_PHY_22 Register (Offset = 4058h) [reset = 0h]

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Table 14-22770. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C058h**

Figure 14-7555. EMIF_CTLCFG_DENALI_PHY_22 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT10_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT10_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_0							
R/W							
0h							

Table 14-22772. EMIF_CTLCFG_DENALI_PHY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_0	R/W	0h	Read leveling pattern 10 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.943 EMIF_CTLCFG_DENALI_PHY_23 Register

1 EMIF_CTLCFG_DENALI_PHY_23 Register (Offset = 405Ch) [reset = 0h]

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Table 14-22773. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C05Ch**

Figure 14-7556. EMIF_CTLCFG_DENALI_PHY_23 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_0							
R/W							
0h							

Table 14-22775. EMIF_CTLCFG_DENALI_PHY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_0	R/W	0h	Read leveling pattern 11 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.944 EMIF_CTLCFG_DENALI_PHY_24 Register

1 EMIF_CTLCFG_DENALI_PHY_24 Register (Offset = 4060h) [reset = 0h]

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Table 14-22776. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C060h**

Figure 14-7557. EMIF_CTLCFG_DENALI_PHY_24 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_0							
R/W							
0h							

Table 14-22778. EMIF_CTLCFG_DENALI_PHY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_0	R/W	0h	Read leveling pattern 12 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.945 EMIF_CTLCFG_DENALI_PHY_25 Register

1 EMIF_CTLCFG_DENALI_PHY_25 Register (Offset = 4064h) [reset = 0h]

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Table 14-22779. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C064h**

Figure 14-7558. EMIF_CTLCFG_DENALI_PHY_25 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT13_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT13_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_0							
R/W							
0h							

Table 14-22781. EMIF_CTLCFG_DENALI_PHY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_0	R/W	0h	Read leveling pattern 13 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.946 EMIF_CTLCFG_DENALI_PHY_26 Register

1 EMIF_CTLCFG_DENALI_PHY_26 Register (Offset = 4068h) [reset = 0h]

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Table 14-22782. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C068h**

Figure 14-7559. EMIF_CTLCFG_DENALI_PHY_26 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_0							
R/W							
0h							

Table 14-22784. EMIF_CTLCFG_DENALI_PHY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_0	R/W	0h	Read leveling pattern 14 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.947 EMIF_CTLCFG_DENALI_PHY_27 Register

1 EMIF_CTLCFG_DENALI_PHY_27 Register (Offset = 406Ch) [reset = 0h]

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Table 14-22785. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C06Ch

Figure 14-7560. EMIF_CTLCFG_DENALI_PHY_27 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_0							
R/W							
0h							

Table 14-22787. EMIF_CTLCFG_DENALI_PHY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_0	R/W	0h	Read leveling pattern 15 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.948 EMIF_CTLCFG_DENALI_PHY_28 Register

1 EMIF_CTLCFG_DENALI_PHY_28 Register (Offset = 4070h) [reset = 0h]

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Table 14-22788. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C070h**

Figure 14-7561. EMIF_CTLCFG_DENALI_PHY_28 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_MASTER_DLY_LOCK_OBS_SELECT_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_0		
NONE					R/W		
0h					0h		

Table 14-22790. EMIF_CTLCFG_DENALI_PHY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_0	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 0. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for future use for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.949 EMIF_CTLCFG_DENALI_PHY_29 Register

1 EMIF_CTLCFG_DENALI_PHY_29 Register (Offset = 4074h) [reset = 0h]

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Table 14-22791. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C074h**

Figure 14-7562. EMIF_CTLCFG_DENALI_PHY_29 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_0			
NONE				R/W			
0h				0h			

Table 14-22793. EMIF_CTLCFG_DENALI_PHY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_0	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.950 EMIF_CTLCFG_DENALI_PHY_30 Register

1 EMIF_CTLCFG_DENALI_PHY_30 Register (Offset = 4078h) [reset = 0h]

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Table 14-22794. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C078h**

Figure 14-7563. EMIF_CTLCFG_DENALI_PHY_30 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WRLVL_ALGO_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_LVL_DEBUG_CONT_0
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LVL_DEBUG_MODE_0
NONE							R/W
0h							0h

Table 14-22796. EMIF_CTLCFG_DENALI_PHY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_0	R/W	0h	Write leveling algorithm selection for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_0	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_0	R/W	0h	Enables leveling debug mode for slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.951 EMIF_CTLCFG_DENALI_PHY_31 Register

1 EMIF_CTLCFG_DENALI_PHY_31 Register (Offset = 407Ch) [reset = 0h]

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Table 14-22797. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C07Ch

Figure 14-7564. EMIF_CTLCFG_DENALI_PHY_31 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_GTLVL_CAPTURE_CNT_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_MASK_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			

Table 14-22799. EMIF_CTLCFG_DENALI_PHY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 0. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_0	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.952 EMIF_CTLCFG_DENALI_PHY_32 Register

1 EMIF_CTLCFG_DENALI_PHY_32 Register (Offset = 4080h) [reset = 0h]

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Table 14-22800. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C080h**

Figure 14-7565. EMIF_CTLCFG_DENALI_PHY_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDLVL_OP_MODE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_RDLVL_UPDT_WAIT_CNT_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_RDLVL_CAPTURE_CNT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-22802. EMIF_CTLCFG_DENALI_PHY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_0	R/W	0h	Read leveling algorithm select for slice 0. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.953 EMIF_CTLCFG_DENALI_PHY_33 Register

1 EMIF_CTLCFG_DENALI_PHY_33 Register (Offset = 4084h) [reset = 0h]

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Table 14-22803. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C084h

Figure 14-7566. EMIF_CTLCFG_DENALI_PHY_33 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_DATA_SWIZZLE_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_SWIZZLE_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_DATA_MASK_0							
R/W							
0h							

Table 14-22805. EMIF_CTLCFG_DENALI_PHY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_0	R/W	0h	Read level bit swizzling for DDR4 operation for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_0	R/W	0h	Per-bit mask for read leveling for slice 0. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.954 EMIF_CTLCFG_DENALI_PHY_34 Register

1 EMIF_CTLCFG_DENALI_PHY_34 Register (Offset = 4088h) [reset = 0h]

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Table 14-22806. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C088h

Figure 14-7567. EMIF_CTLCFG_DENALI_PHY_34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_PATT_0		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED		PHY_WDQLVL_BURST_CNT_0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PHY_WDQLVL_CLK_JITTER_TOLERANCE_0							
R/W							
0h							

Table 14-22808. EMIF_CTLCFG_DENALI_PHY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_0	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 0. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_0	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_0	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.955 EMIF_CTLCFG_DENALI_PHY_35 Register

1 EMIF_CTLCFG_DENALI_PHY_35 Register (Offset = 408Ch) [reset = 0h]

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Table 14-22809. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C08Ch**

Figure 14-7568. EMIF_CTLCFG_DENALI_PHY_35 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0							
R/W							
0h							

Table 14-22811. EMIF_CTLCFG_DENALI_PHY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.956 EMIF_CTLCFG_DENALI_PHY_36 Register

1 EMIF_CTLCFG_DENALI_PHY_36 Register (Offset = 4090h) [reset = 0h]

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Table 14-22812. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C090h**

Figure 14-7569. EMIF_CTLCFG_DENALI_PHY_36 Name Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_WDQLVL_CLR_PREV_RESULTS_0
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_DM_DLY_STEP_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DQ_SLV_DELTA_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_SELECT_0							
R/W							
0h							

Table 14-22814. EMIF_CTLCFG_DENALI_PHY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_0	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_0	R/W	0h	The target delay line step for DM training for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_0	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_0	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.957 EMIF_CTLCFG_DENALI_PHY_37 Register

1 EMIF_CTLCFG_DENALI_PHY_37 Register (Offset = 4094h) [reset = 0h]

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Table 14-22815. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C094h**

Figure 14-7570. EMIF_CTLCFG_DENALI_PHY_37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_WDQLVL_DATADM_MASK_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_WDQLVL_DATADM_MASK_0							
R/W							
0h							

Table 14-22817. EMIF_CTLCFG_DENALI_PHY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_0	R/W	0h	Per-bit mask for write data leveling for slice 0. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.6.6.2.958 EMIF_CTLCFG_DENALI_PHY_38 Register

1 EMIF_CTLCFG_DENALI_PHY_38 Register (Offset = 4098h) [reset = 0h]

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Table 14-22818. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C098h**

Figure 14-7571. EMIF_CTLCFG_DENALI_PHY_38 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT0_0							
R/W							
0h							

Table 14-22820. EMIF_CTLCFG_DENALI_PHY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.959 EMIF_CTLCFG_DENALI_PHY_39 Register

1 EMIF_CTLCFG_DENALI_PHY_39 Register (Offset = 409Ch) [reset = 0h]

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Table 14-22821. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C09Ch**

Figure 14-7572. EMIF_CTLCFG_DENALI_PHY_39 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT1_0							
R/W							
0h							

Table 14-22823. EMIF_CTLCFG_DENALI_PHY_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.960 EMIF_CTLCFG_DENALI_PHY_40 Register

1 EMIF_CTLCFG_DENALI_PHY_40 Register (Offset = 40A0h) [reset = 0h]

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Table 14-22824. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0A0h**

Figure 14-7573. EMIF_CTLCFG_DENALI_PHY_40 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_USER_PATT2_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT2_0							
R/W							
0h							

Table 14-22826. EMIF_CTLCFG_DENALI_PHY_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.961 EMIF_CTLCFG_DENALI_PHY_41 Register

1 EMIF_CTLCFG_DENALI_PHY_41 Register (Offset = 40A4h) [reset = 0h]

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Table 14-22827. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0A4h**

Figure 14-7574. EMIF_CTLCFG_DENALI_PHY_41 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT3_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT3_0							
R/W							
0h							

Table 14-22829. EMIF_CTLCFG_DENALI_PHY_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.962 EMIF_CTLCFG_DENALI_PHY_42 Register

1 EMIF_CTLCFG_DENALI_PHY_42 Register (Offset = 40A8h) [reset = 0h]

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Table 14-22830. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0A8h

Figure 14-7575. EMIF_CTLCFG_DENALI_PHY_42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_NTP_MULT_TRAIN_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT4_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT4_0							
R/W							
0h							

Table 14-22832. EMIF_CTLCFG_DENALI_PHY_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_0	R/W	0h	Control for single pass only No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.963 EMIF_CTLCFG_DENALI_PHY_43 Register

1 EMIF_CTLCFG_DENALI_PHY_43 Register (Offset = 40ACh) [reset = 0h]

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Table 14-22833. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0ACh**

Figure 14-7576. EMIF_CTLCFG_DENALI_PHY_43 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_EARLY_THRESHOLD_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_EARLY_THRESHOLD_0							
R/W							
0h							

Table 14-22835. EMIF_CTLCFG_DENALI_PHY_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_0	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_0	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.964 EMIF_CTLCFG_DENALI_PHY_44 Register

1 EMIF_CTLCFG_DENALI_PHY_44 Register (Offset = 40B0h) [reset = 0h]

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Table 14-22836. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0B0h**

Figure 14-7577. EMIF_CTLCFG_DENALI_PHY_44 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_MAX_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_PERIOD_THRESHOLD_MIN_0							
R/W							
0h							

Table 14-22838. EMIF_CTLCFG_DENALI_PHY_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_0	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_0	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.965 EMIF_CTLCFG_DENALI_PHY_45 Register

1 EMIF_CTLCFG_DENALI_PHY_45 Register (Offset = 40B4h) [reset = 0h]

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Table 14-22839. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0B4h**

Figure 14-7578. EMIF_CTLCFG_DENALI_PHY_45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_0					
NONE		W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_0
NONE							R/W
0h							0h

Table 14-22841. EMIF_CTLCFG_DENALI_PHY_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_0	R	0h	Observation register containing read entry FIFO pointers for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for slice 0. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_0	R/W	0h	Indicates if slice 0 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.966 EMIF_CTLCFG_DENALI_PHY_46 Register

1 EMIF_CTLCFG_DENALI_PHY_46 Register (Offset = 40B8h) [reset = 100000h]

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Table 14-22842. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0B8h

Figure 14-7579. EMIF_CTLCFG_DENALI_PHY_46 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_0							
R							
100000h							

Table 14-22844. EMIF_CTLCFG_DENALI_PHY_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_0	R	100000h	Observation register containing loopback status/results for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.967 EMIF_CTLCFG_DENALI_PHY_47 Register

1 EMIF_CTLCFG_DENALI_PHY_47 Register (Offset = 40BCh) [reset = 0h]

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Table 14-22845. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0BCh**

Figure 14-7580. EMIF_CTLCFG_DENALI_PHY_47 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_MASTER_DLY_LOCK_OBS_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_MASTER_DLY_LOCK_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_LPBK_ERROR_COUNT_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_LPBK_ERROR_COUNT_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22847. EMIF_CTLCFG_DENALI_PHY_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing controller delay results for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.968 EMIF_CTLCFG_DENALI_PHY_48 Register

1 EMIF_CTLCFG_DENALI_PHY_48 Register (Offset = 40C0h) [reset = 0h]

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Table 14-22848. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0C0h**

Figure 14-7581. EMIF_CTLCFG_DENALI_PHY_48 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MEAS_DLY_STEP_VALUE_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						

Table 14-22850. EMIF_CTLCFG_DENALI_PHY_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_0	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQ target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.969 EMIF_CTLCFG_DENALI_PHY_49 Register

1 EMIF_CTLCFG_DENALI_PHY_49 Register (Offset = 40C4h) [reset = 0h]

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Table 14-22851. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0C4h

Figure 14-7582. EMIF_CTLCFG_DENALI_PHY_49 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							

Table 14-22853. EMIF_CTLCFG_DENALI_PHY_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQS base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS gate target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.970 EMIF_CTLCFG_DENALI_PHY_50 Register

1 EMIF_CTLCFG_DENALI_PHY_50 Register (Offset = 40C8h) [reset = 0h]

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Table 14-22854. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0C8h**

Figure 14-7583. EMIF_CTLCFG_DENALI_PHY_50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_WR_SHIFT_OBS_0		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WR_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0							
R							
0h							

Table 14-22856. EMIF_CTLCFG_DENALI_PHY_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQ base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.971 EMIF_CTLCFG_DENALI_PHY_51 Register

1 EMIF_CTLCFG_DENALI_PHY_51 Register (Offset = 40CCh) [reset = 0h]

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Table 14-22857. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0CCh

Figure 14-7584. EMIF_CTLCFG_DENALI_PHY_51 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_0	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_HARD1_DELAY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_HARD0_DELAY_OBS_0							
R							
0h							

Table 14-22859. EMIF_CTLCFG_DENALI_PHY_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.972 EMIF_CTLCFG_DENALI_PHY_52 Register

1 EMIF_CTLCFG_DENALI_PHY_52 Register (Offset = 40D0h) [reset = 0h]

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Table 14-22860. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0D0h

Figure 14-7585. EMIF_CTLCFG_DENALI_PHY_52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_WRLVL_STATUS_OBS_0				
NONE			R				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_STATUS_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_STATUS_OBS_0							
R							
0h							

Table 14-22862. EMIF_CTLCFG_DENALI_PHY_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_0	R	0h	Observation register containing write leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.973 EMIF_CTLCFG_DENALI_PHY_53 Register

1 EMIF_CTLCFG_DENALI_PHY_53 Register (Offset = 40D4h) [reset = 0h]

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Table 14-22863. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0D4h**

Figure 14-7586. EMIF_CTLCFG_DENALI_PHY_53 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0							
R							
0h							

Table 14-22865. EMIF_CTLCFG_DENALI_PHY_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample2 target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample1 target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.974 EMIF_CTLCFG_DENALI_PHY_54 Register

1 EMIF_CTLCFG_DENALI_PHY_54 Register (Offset = 40D8h) [reset = 0h]

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Table 14-22866. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0D8h**

Figure 14-7587. EMIF_CTLCFG_DENALI_PHY_54 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_0					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD0_DELAY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_ERROR_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_ERROR_OBS_0							
R							
0h							

Table 14-22868. EMIF_CTLCFG_DENALI_PHY_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_WRLVL_ERROR_OBS_0	R	0h	Observation register containing write leveling error status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.975 EMIF_CTLCFG_DENALI_PHY_55 Register

1 EMIF_CTLCFG_DENALI_PHY_55 Register (Offset = 40DCh) [reset = 0h]

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Table 14-22869. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0DCh**

Figure 14-7588. EMIF_CTLCFG_DENALI_PHY_55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_0					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_HARD1_DELAY_OBS_0							
R							
0h							

Table 14-22871. EMIF_CTLCFG_DENALI_PHY_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.976 EMIF_CTLCFG_DENALI_PHY_56 Register

1 EMIF_CTLCFG_DENALI_PHY_56 Register (Offset = 40E0h) [reset = 0h]

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Table 14-22872. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0E0h**

Figure 14-7589. EMIF_CTLCFG_DENALI_PHY_56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_GTLVL_STATUS_OBS_0	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_GTLVL_STATUS_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_STATUS_OBS_0							
R							
0h							

Table 14-22874. EMIF_CTLCFG_DENALI_PHY_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_0	R	0h	Observation register containing gate training status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.977 EMIF_CTLCFG_DENALI_PHY_57 Register

1 EMIF_CTLCFG_DENALI_PHY_57 Register (Offset = 40E4h) [reset = 0h]

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Table 14-22875. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0E4h**

Figure 14-7590. EMIF_CTLCFG_DENALI_PHY_57 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0							
R							
0h							

Table 14-22877. EMIF_CTLCFG_DENALI_PHY_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.978 EMIF_CTLCFG_DENALI_PHY_58 Register

1 EMIF_CTLCFG_DENALI_PHY_58 Register (Offset = 40E8h) [reset = 0h]

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Table 14-22878. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0E8h**

Figure 14-7591. EMIF_CTLCFG_DENALI_PHY_58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	
NONE						R	
0h						0h	

Table 14-22880. EMIF_CTLCFG_DENALI_PHY_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	R	0h	Observation register containing read leveling number of windows found for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.979 EMIF_CTLCFG_DENALI_PHY_59 Register

1 EMIF_CTLCFG_DENALI_PHY_59 Register (Offset = 40ECh) [reset = 0h]

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Table 14-22881. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0ECh

Figure 14-7592. EMIF_CTLCFG_DENALI_PHY_59 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_0							
R							
0h							

Table 14-22883. EMIF_CTLCFG_DENALI_PHY_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_0	R	0h	Observation register containing read leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.980 EMIF_CTLCFG_DENALI_PHY_60 Register

1 EMIF_CTLCFG_DENALI_PHY_60 Register (Offset = 40F0h) [reset = 7FF0000h]

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Table 14-22884. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C0F0h

Figure 14-7593. EMIF_CTLCFG_DENALI_PHY_60 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_0		
NONE					R		
0h					7FFh		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DQDM_TE_DLY_OBS_0							
R							
7FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_0		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_LE_DLY_OBS_0							
R							
0h							

Table 14-22886. EMIF_CTLCFG_DENALI_PHY_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_0	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_0	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.981 EMIF_CTLCFG_DENALI_PHY_61 Register

1 EMIF_CTLCFG_DENALI_PHY_61 Register (Offset = 40F4h) [reset = 0h]

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Table 14-22887. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0F4h**

Figure 14-7594. EMIF_CTLCFG_DENALI_PHY_61 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							

Table 14-22889. EMIF_CTLCFG_DENALI_PHY_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_0	R	0h	Observation register containing write data leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.982 EMIF_CTLCFG_DENALI_PHY_62 Register

1 EMIF_CTLCFG_DENALI_PHY_62 Register (Offset = 40F8h) [reset = 0h]

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Table 14-22890. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0F8h**

Figure 14-7595. EMIF_CTLCFG_DENALI_PHY_62 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							

Table 14-22892. EMIF_CTLCFG_DENALI_PHY_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_0	R	0h	Observation register containing periodic write data leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.983 EMIF_CTLCFG_DENALI_PHY_63 Register

1 EMIF_CTLCFG_DENALI_PHY_63 Register (Offset = 40FCh) [reset = 0h]

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Table 14-22893. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C0FCh**

Figure 14-7596. EMIF_CTLCFG_DENALI_PHY_63 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_DDL_MODE_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_MODE_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_MODE_0							
R/W							
0h							

Table 14-22895. EMIF_CTLCFG_DENALI_PHY_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_0	R/W	0h	DDL mode for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.984 EMIF_CTLCFG_DENALI_PHY_64 Register

1 EMIF_CTLCFG_DENALI_PHY_64 Register (Offset = 4100h) [reset = 0h]

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Table 14-22896. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C100h**

Figure 14-7597. EMIF_CTLCFG_DENALI_PHY_64 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_MASK_0					
NONE		R/W					
0h		0h					

Table 14-22898. EMIF_CTLCFG_DENALI_PHY_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_0	R/W	0h	DDL mask for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.985 EMIF_CTLCFG_DENALI_PHY_65 Register

1 EMIF_CTLCFG_DENALI_PHY_65 Register (Offset = 4104h) [reset = 0h]

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Table 14-22899. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C104h**

Figure 14-7598. EMIF_CTLCFG_DENALI_PHY_65 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_0							
R							
0h							

Table 14-22901. EMIF_CTLCFG_DENALI_PHY_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_0	R	0h	DDL test observation for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.986 EMIF_CTLCFG_DENALI_PHY_66 Register

1 EMIF_CTLCFG_DENALI_PHY_66 Register (Offset = 4108h) [reset = 0h]

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Table 14-22902. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C108h**

Figure 14-7599. EMIF_CTLCFG_DENALI_PHY_66 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							

Table 14-22904. EMIF_CTLCFG_DENALI_PHY_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_0	R	0h	DDL test observation delays for slice 0 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.987 EMIF_CTLCFG_DENALI_PHY_67 Register

1 EMIF_CTLCFG_DENALI_PHY_67 Register (Offset = 410Ch) [reset = 0h]

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Table 14-22905. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C10Ch**

Figure 14-7600. EMIF_CTLCFG_DENALI_PHY_67 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_0							
R/W							
0h							

Table 14-22907. EMIF_CTLCFG_DENALI_PHY_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_0	R/W	0h	RX Calibration codes for DQ0 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_0	R/W	0h	LPDDR4 write preamble extension enable for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_0	R/W	0h	Specify threshold value for PHY init update tracking for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.988 EMIF_CTLCFG_DENALI_PHY_68 Register

1 EMIF_CTLCFG_DENALI_PHY_68 Register (Offset = 4110h) [reset = 0h]

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Table 14-22908. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C110h**

Figure 14-7601. EMIF_CTLCFG_DENALI_PHY_68 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ2_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ1_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ1_0							
R/W							
0h							

Table 14-22910. EMIF_CTLCFG_DENALI_PHY_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_0	R/W	0h	RX Calibration codes for DQ2 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_0	R/W	0h	RX Calibration codes for DQ1 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.989 EMIF_CTLCFG_DENALI_PHY_69 Register

1 EMIF_CTLCFG_DENALI_PHY_69 Register (Offset = 4114h) [reset = 0h]

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Table 14-22911. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C114h**

Figure 14-7602. EMIF_CTLCFG_DENALI_PHY_69 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ4_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ4_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ3_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ3_0							
R/W							
0h							

Table 14-22913. EMIF_CTLCFG_DENALI_PHY_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_0	R/W	0h	RX Calibration codes for DQ4 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_0	R/W	0h	RX Calibration codes for DQ3 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.990 EMIF_CTLCFG_DENALI_PHY_70 Register

1 EMIF_CTLCFG_DENALI_PHY_70 Register (Offset = 4118h) [reset = 0h]

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Table 14-22914. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C118h**

Figure 14-7603. EMIF_CTLCFG_DENALI_PHY_70 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ6_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ5_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ5_0							
R/W							
0h							

Table 14-22916. EMIF_CTLCFG_DENALI_PHY_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_0	R/W	0h	RX Calibration codes for DQ6 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_0	R/W	0h	RX Calibration codes for DQ5 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.991 EMIF_CTLCFG_DENALI_PHY_71 Register

1 EMIF_CTLCFG_DENALI_PHY_71 Register (Offset = 411Ch) [reset = 0h]

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Table 14-22917. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C11Ch

Figure 14-7604. EMIF_CTLCFG_DENALI_PHY_71 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ7_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ7_0							
R/W							
0h							

Table 14-22919. EMIF_CTLCFG_DENALI_PHY_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_0	R/W	0h	RX Calibration codes for DQ7 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.992 EMIF_CTLCFG_DENALI_PHY_72 Register

1 EMIF_CTLCFG_DENALI_PHY_72 Register (Offset = 4120h) [reset = 0h]

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Table 14-22920. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C120h

Figure 14-7605. EMIF_CTLCFG_DENALI_PHY_72 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RX_CAL_DM_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RX_CAL_DM_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DM_0							
R/W							
0h							

Table 14-22922. EMIF_CTLCFG_DENALI_PHY_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_0	R/W	0h	RX Calibration codes for DM for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.993 EMIF_CTLCFG_DENALI_PHY_73 Register

1 EMIF_CTLCFG_DENALI_PHY_73 Register (Offset = 4124h) [reset = 0h]

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Table 14-22923. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C124h**

Figure 14-7606. EMIF_CTLCFG_DENALI_PHY_73 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_FDBK_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQS_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQS_0							
R/W							
0h							

Table 14-22925. EMIF_CTLCFG_DENALI_PHY_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_0	R/W	0h	RX Calibration codes for FDBK for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_0	R/W	0h	RX Calibration codes for DQS for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.994 EMIF_CTLCFG_DENALI_PHY_74 Register

1 EMIF_CTLCFG_DENALI_PHY_74 Register (Offset = 4128h) [reset = 0h]

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Table 14-22926. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C128h**

Figure 14-7607. EMIF_CTLCFG_DENALI_PHY_74 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_CAL_SAMPLE_WAIT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_STATIC_TOG_DISABLE_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_PAD_RX_BIAS_EN_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_PAD_RX_BIAS_EN_0							
R/W							
0h							

Table 14-22928. EMIF_CTLCFG_DENALI_PHY_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_CAL_SAMPLE_WAIT_0	R/W	0h	Determines number of cycles to wait for each sample for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_0	R/W	0h	Control to disable toggle during static activity for slice 0. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_0	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.995 EMIF_CTLCFG_DENALI_PHY_75 Register

1 EMIF_CTLCFG_DENALI_PHY_75 Register (Offset = 412Ch) [reset = 0h]

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Table 14-22929. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C12Ch**

Figure 14-7608. EMIF_CTLCFG_DENALI_PHY_75 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_ADJUST_SAMPLE_CNT_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_DATA_DC_ADJUST_START_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DATA_DC_WEIGHT_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_CAL_TIMEOUT_0							
R/W							
0h							

Table 14-22931. EMIF_CTLCFG_DENALI_PHY_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_ADJUST_SAMPLE_CNT_0	R/W	0h	Duty cycle adjust sample count for slice 0. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DATA_DC_ADJUST_START_0	R/W	0h	Duty cycle adjust starting value for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DATA_DC_WEIGHT_0	R/W	0h	Determines weight of average calculating for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_CAL_TIMEOUT_0	R/W	0h	Determines timeout number of iteration for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.996 EMIF_CTLCFG_DENALI_PHY_76 Register

1 EMIF_CTLCFG_DENALI_PHY_76 Register (Offset = 4130h) [reset = 0h]

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Table 14-22932. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C130h**

Figure 14-7609. EMIF_CTLCFG_DENALI_PHY_76 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_CAL_START_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_DATA_DC_CAL_POLARITY_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_ADJUST_THRSHLD_0							
R/W							
0h							

Table 14-22934. EMIF_CTLCFG_DENALI_PHY_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_DATA_DC_CAL_START_0	R/W	0h	Manual trigger for DCC for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DATA_DC_CAL_POLARITY_0	R/W	0h	Calibration polarity for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_ADJUST_DIRECT_0	R/W	0h	Adjust direction for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_ADJUST_THRSHLD_0	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.997 EMIF_CTLCFG_DENALI_PHY_77 Register

1 EMIF_CTLCFG_DENALI_PHY_77 Register (Offset = 4134h) [reset = 1h]

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Table 14-22935. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C134h**

Figure 14-7610. EMIF_CTLCFG_DENALI_PHY_77 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDPATH_GATE_DISABLE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_FDBK_PWR_CTRL_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DATA_DC_SW_RANK_0	
NONE						R/W	
0h						1h	

Table 14-22937. EMIF_CTLCFG_DENALI_PHY_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDPATH_GATE_DISABLE_0	R/W	0h	Data slice read path power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_FDBK_PWR_CTRL_0	R/W	0h	Shutoff gate feedback IO to reduce power for slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DATA_DC_SW_RANK_0	R/W	1h	Rank selection for software based duty cycle correction for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.998 EMIF_CTLCFG_DENALI_PHY_78 Register

1 EMIF_CTLCFG_DENALI_PHY_78 Register (Offset = 4138h) [reset = 0h]

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Table 14-22938. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C138h**

Figure 14-7611. EMIF_CTLCFG_DENALI_PHY_78 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h

Table 14-22940. EMIF_CTLCFG_DENALI_PHY_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_SLICE_PWR_RDC_DISABLE_0	R/W	0h	Data slice power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.999 EMIF_CTLCFG_DENALI_PHY_79 Register

1 EMIF_CTLCFG_DENALI_PHY_79 Register (Offset = 413Ch) [reset = 0h]

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Table 14-22941. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C13Ch

Figure 14-7612. EMIF_CTLCFG_DENALI_PHY_79 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_SELECT_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_SELECT_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DQ_TSEL_ENABLE_0		
NONE					R/W		
0h					0h		

Table 14-22943. EMIF_CTLCFG_DENALI_PHY_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQS signals for slice 0. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 0. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1000 EMIF_CTLCFG_DENALI_PHY_80 Register

1 EMIF_CTLCFG_DENALI_PHY_80 Register (Offset = 4140h) [reset = 0h]

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Table 14-22944. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C140h**

Figure 14-7613. EMIF_CTLCFG_DENALI_PHY_80 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_INITIAL_START_POINT_0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_TWO_CYC_PREAMBLE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_SELECT_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_SELECT_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22946. EMIF_CTLCFG_DENALI_PHY_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_0	R/W	0h	Data slice initial VREF training start value for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_0	R/W	0h	2 cycle preamble support for slice 0. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQS signals for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1001 EMIF_CTLCFG_DENALI_PHY_81 Register

1 EMIF_CTLCFG_DENALI_PHY_81 Register (Offset = 4144h) [reset = 0h]

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Table 14-22947. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C144h**

Figure 14-7614. EMIF_CTLCFG_DENALI_PHY_81 Name Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_NTP_TRAIN_EN_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_VREF_TRAINING_CTRL_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_VREF_INITIAL_STOP_POINT_0						
NONE	R/W						
0h	0h						

Table 14-22949. EMIF_CTLCFG_DENALI_PHY_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_0	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_0	R/W	0h	Enable for No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_0	R/W	0h	Data slice vref training enable control for slice 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_0	R/W	0h	Data slice initial VREF training stop value for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1002 EMIF_CTLCFG_DENALI_PHY_82 Register

1 EMIF_CTLCFG_DENALI_PHY_82 Register (Offset = 4148h) [reset = 0h]

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Table 14-22950. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C148h**

Figure 14-7615. EMIF_CTLCFG_DENALI_PHY_82 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_WDQ_STOP_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_NTP_WDQ_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_START_0							
R/W							
0h							

Table 14-22952. EMIF_CTLCFG_DENALI_PHY_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_0	R/W	0h	End of WR DQ target delay in No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_0	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1003 EMIF_CTLCFG_DENALI_PHY_83 Register

1 EMIF_CTLCFG_DENALI_PHY_83 Register (Offset = 414Ch) [reset = 0h]

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Table 14-22953. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C14Ch**

Figure 14-7616. EMIF_CTLCFG_DENALI_PHY_83 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WDQLVL_DVW_MIN_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DVW_MIN_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_BIT_EN_0							
R/W							
0h							

Table 14-22955. EMIF_CTLCFG_DENALI_PHY_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_0	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_0	R/W	0h	Minimum data valid window across DQs and ranks for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_0	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1004 EMIF_CTLCFG_DENALI_PHY_84 Register

1 EMIF_CTLCFG_DENALI_PHY_84 Register (Offset = 4150h) [reset = 0h]

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Table 14-22956. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C150h**

Figure 14-7617. EMIF_CTLCFG_DENALI_PHY_84 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_TX_DCD_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_0					
NONE		R/W					
0h		0h					

Table 14-22958. EMIF_CTLCFG_DENALI_PHY_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_0	R/W	0h	Controls TX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_0	R/W	0h	Enable for fast multi-pattern window search for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_0	R/W	0h	Peridic training start point offset for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1005 EMIF_CTLCFG_DENALI_PHY_85 Register

1 EMIF_CTLCFG_DENALI_PHY_85 Register (Offset = 4154h) [reset = 0h]

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Table 14-22959. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C154h**

Figure 14-7618. EMIF_CTLCFG_DENALI_PHY_85 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_3_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_2_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_1_0				
NONE			R/W				
0h			0h				

Table 14-22961. EMIF_CTLCFG_DENALI_PHY_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1006 EMIF_CTLCFG_DENALI_PHY_86 Register

1 EMIF_CTLCFG_DENALI_PHY_86 Register (Offset = 4158h) [reset = 0h]

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Table 14-22962. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C158h**

Figure 14-7619. EMIF_CTLCFG_DENALI_PHY_86 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_7_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_6_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_5_0				
NONE			R/W				
0h			0h				

Table 14-22964. EMIF_CTLCFG_DENALI_PHY_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dm pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1007 EMIF_CTLCFG_DENALI_PHY_87 Register

1 EMIF_CTLCFG_DENALI_PHY_87 Register (Offset = 415Ch) [reset = 0h]

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Table 14-22965. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C15Ch**

Figure 14-7620. EMIF_CTLCFG_DENALI_PHY_87 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_PAD_DSLICE_IO_CFG_0						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_FDBK_RX_DCD_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_DQS_RX_DCD_0				
NONE			R/W				
0h			0h				

Table 14-22967. EMIF_CTLCFG_DENALI_PHY_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_0	R/W	0h	Controls PCLK/PARK pin for pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_0	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dqs pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1008 EMIF_CTLCFG_DENALI_PHY_88 Register

1 EMIF_CTLCFG_DENALI_PHY_88 Register (Offset = 4160h) [reset = 0h]

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Table 14-22968. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C160h**

Figure 14-7621. EMIF_CTLCFG_DENALI_PHY_88 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ1_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ0_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22970. EMIF_CTLCFG_DENALI_PHY_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_0	R/W	0h	Read DQ1 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_0	R/W	0h	Read DQ0 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1009 EMIF_CTLCFG_DENALI_PHY_89 Register

1 EMIF_CTLCFG_DENALI_PHY_89 Register (Offset = 4164h) [reset = 0h]

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Table 14-22971. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C164h**

Figure 14-7622. EMIF_CTLCFG_DENALI_PHY_89 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ3_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ2_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22973. EMIF_CTLCFG_DENALI_PHY_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_0	R/W	0h	Read DQ3 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_0	R/W	0h	Read DQ2 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1010 EMIF_CTLCFG_DENALI_PHY_90 Register

1 EMIF_CTLCFG_DENALI_PHY_90 Register (Offset = 4168h) [reset = 0h]

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Table 14-22974. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C168h**

Figure 14-7623. EMIF_CTLCFG_DENALI_PHY_90 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ5_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ4_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ4_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22976. EMIF_CTLCFG_DENALI_PHY_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_0	R/W	0h	Read DQ5 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_0	R/W	0h	Read DQ4 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1011 EMIF_CTLCFG_DENALI_PHY_91 Register

1 EMIF_CTLCFG_DENALI_PHY_91 Register (Offset = 416Ch) [reset = 0h]

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Table 14-22977. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C16Ch**

Figure 14-7624. EMIF_CTLCFG_DENALI_PHY_91 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ7_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ7_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ6_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ6_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22979. EMIF_CTLCFG_DENALI_PHY_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_0	R/W	0h	Read DQ7 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_0	R/W	0h	Read DQ6 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1012 EMIF_CTLCFG_DENALI_PHY_92 Register

1 EMIF_CTLCFG_DENALI_PHY_92 Register (Offset = 4170h) [reset = 0h]

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Table 14-22980. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C170h**

Figure 14-7625. EMIF_CTLCFG_DENALI_PHY_92 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED					PHY_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_0							
R/W							
0h							

Table 14-22982. EMIF_CTLCFG_DENALI_PHY_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_0	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 0. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_0	R/W	0h	RX_PCLK clock frequency selection for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_0	R/W	0h	Read DM/DBI target delay setting for slice 0. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1013 EMIF_CTLCFG_DENALI_PHY_93 Register

1 EMIF_CTLCFG_DENALI_PHY_93 Register (Offset = 4174h) [reset = 0h]

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Table 14-22983. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C174h

Figure 14-7626. EMIF_CTLCFG_DENALI_PHY_93 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_0		
NONE					R/W		
0h					0h		

Table 14-22985. EMIF_CTLCFG_DENALI_PHY_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DATA_DC_CAL_CLK_SEL_0	R/W	0h	Determines DCC CAL clock for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1014 EMIF_CTLCFG_DENALI_PHY_94 Register

1 EMIF_CTLCFG_DENALI_PHY_94 Register (Offset = 4178h) [reset = 0h]

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Table 14-22986. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C178h**

Figure 14-7627. EMIF_CTLCFG_DENALI_PHY_94 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_OE_TIMING_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_TSEL_WR_TIMING_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_TSEL_RD_TIMING_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_OE_TIMING_0							
R/W							
0h							

Table 14-22988. EMIF_CTLCFG_DENALI_PHY_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_0	R/W	0h	Start/end timing values for DQS output enable signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1015 EMIF_CTLCFG_DENALI_PHY_95 Register

1 EMIF_CTLCFG_DENALI_PHY_95 Register (Offset = 417Ch) [reset = 0h]

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Table 14-22989. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C17Ch

Figure 14-7628. EMIF_CTLCFG_DENALI_PHY_95 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQS_OE_RD_TIMING_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQS_TSEL_RD_TIMING_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_0			
NONE				R/W			
0h				0h			

Table 14-22991. EMIF_CTLCFG_DENALI_PHY_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based OE extension for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1016 EMIF_CTLCFG_DENALI_PHY_96 Register

1 EMIF_CTLCFG_DENALI_PHY_96 Register (Offset = 4180h) [reset = 0h]

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Table 14-22992. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C180h**

Figure 14-7629. EMIF_CTLCFG_DENALI_PHY_96 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_VREF_CTRL_DQ_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_VREF_SETTING_TIME_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_VREF_SETTING_TIME_0							
R/W							
0h							

Table 14-22994. EMIF_CTLCFG_DENALI_PHY_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_0	R/W	0h	Pad VREF control settings for DQ slice 0. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_0	R/W	0h	Number of cycles for vref settle after setting is changed for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1017 EMIF_CTLCFG_DENALI_PHY_97 Register

1 EMIF_CTLCFG_DENALI_PHY_97 Register (Offset = 4184h) [reset = 0h]

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Table 14-22995. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C184h**

Figure 14-7630. EMIF_CTLCFG_DENALI_PHY_97 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDATA_EN_IE_DLY_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DQS_IE_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQ_IE_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PER_CS_TRAINING_EN_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-22997. EMIF_CTLCFG_DENALI_PHY_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_RDDATA_EN_IE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_IE_TIMING_0	R/W	0h	Start/end timing values for DQS input enable signals for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_IE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_EN_0	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 0. Must have same value in all slices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1018 EMIF_CTLCFG_DENALI_PHY_98 Register

1 EMIF_CTLCFG_DENALI_PHY_98 Register (Offset = 4188h) [reset = 0h]

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Table 14-22998. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C188h**

Figure 14-7631. EMIF_CTLCFG_DENALI_PHY_98 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_WDQLVL_IE_ON_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DBI_MODE_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_IE_MODE_0	
NONE						R/W	
0h						0h	

Table 14-23000. EMIF_CTLCFG_DENALI_PHY_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_DLY_0	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_WDQLVL_IE_ON_0	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DBI_MODE_0	R/W	0h	DBI mode for slice 0. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_IE_MODE_0	R/W	0h	Input enable mode bits for slice 0. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1019 EMIF_CTLCFG_DENALI_PHY_99 Register

1 EMIF_CTLCFG_DENALI_PHY_99 Register (Offset = 418Ch) [reset = 0h]

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Table 14-23001. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C18Ch**

Figure 14-7632. EMIF_CTLCFG_DENALI_PHY_99 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_MASTER_MODE_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_RDDATA_EN_OE_DLY_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				

Table 14-23003. EMIF_CTLCFG_DENALI_PHY_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_MASTER_MODE_0	R/W	0h	Controller delay line override settings for slice 0. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_OE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_TSEL_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_0	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1020 EMIF_CTLCFG_DENALI_PHY_100 Register

1 EMIF_CTLCFG_DENALI_PHY_100 Register (Offset = 4190h) [reset = 0h]

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Table 14-23004. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C190h

Figure 14-7633. EMIF_CTLCFG_DENALI_PHY_100 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_WAIT_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_MASTER_DELAY_STEP_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_MASTER_DELAY_START_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_START_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23006. EMIF_CTLCFG_DENALI_PHY_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 0. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_0	R/W	0h	Start value for controller delay line locking algorithm for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1021 EMIF_CTLCFG_DENALI_PHY_101 Register

1 EMIF_CTLCFG_DENALI_PHY_101 Register (Offset = 4194h) [reset = 0h]

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Table 14-23007. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C194h**

Figure 14-7634. EMIF_CTLCFG_DENALI_PHY_101 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PHY_WRLVL_DLY_STEP_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RPTR_UPDATE_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_HALF_MEASURE_0							
R/W							
0h							

Table 14-23009. EMIF_CTLCFG_DENALI_PHY_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_0	R/W	0h	DQS target delay fine step size during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_0	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1022 EMIF_CTLCFG_DENALI_PHY_102 Register

1 EMIF_CTLCFG_DENALI_PHY_102 Register (Offset = 4198h) [reset = 0h]

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Table 14-23010. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C198h**

Figure 14-7635. EMIF_CTLCFG_DENALI_PHY_102 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_GTLVL_RESP_WAIT_CNT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_GTLVL_DLY_STEP_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_RESP_WAIT_CNT_0					
NONE		R/W					
0h		0h					

Table 14-23012. EMIF_CTLCFG_DENALI_PHY_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 0. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1023 EMIF_CTLCFG_DENALI_PHY_103 Register

1 EMIF_CTLCFG_DENALI_PHY_103 Register (Offset = 419Ch) [reset = 0h]

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Table 14-23013. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C19Ch**

Figure 14-7636. EMIF_CTLCFG_DENALI_PHY_103 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GTLVL_FINAL_STEP_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_GTLVL_FINAL_STEP_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_BACK_STEP_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_BACK_STEP_0							
R/W							
0h							

Table 14-23015. EMIF_CTLCFG_DENALI_PHY_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_0	R/W	0h	Final backup step delay used in gate training algorithm for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_0	R/W	0h	Interim backup step delay used in gate training algorithm for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1024 EMIF_CTLCFG_DENALI_PHY_104 Register

1 EMIF_CTLCFG_DENALI_PHY_104 Register (Offset = 41A0h) [reset = 0h]

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Table 14-23016. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1A0h**

Figure 14-7637. EMIF_CTLCFG_DENALI_PHY_104 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_WDQLVL_DM_SEARCH_RANGE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DM_SEARCH_RANGE_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DLY_STEP_0							
R/W							
0h							

Table 14-23018. EMIF_CTLCFG_DENALI_PHY_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_0	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_0	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 0. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_0	R/W	0h	DQ target delay step size during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1025 EMIF_CTLCFG_DENALI_PHY_105 Register

1 EMIF_CTLCFG_DENALI_PHY_105 Register (Offset = 41A4h) [reset = 0h]

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Table 14-23019. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1A4h**

Figure 14-7638. EMIF_CTLCFG_DENALI_PHY_105 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_DLY_STEP_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_TOGGLE_PRE_SUPPORT_0
NONE							R/W
0h							0h

Table 14-23021. EMIF_CTLCFG_DENALI_PHY_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_0	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1026 EMIF_CTLCFG_DENALI_PHY_106 Register

1 EMIF_CTLCFG_DENALI_PHY_106 Register (Offset = 41A8h) [reset = 0h]

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Table 14-23022. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1A8h

Figure 14-7639. EMIF_CTLCFG_DENALI_PHY_106 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_MAX_EDGE_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_MAX_EDGE_0							
R/W							
0h							

Table 14-23024. EMIF_CTLCFG_DENALI_PHY_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_0	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1027 EMIF_CTLCFG_DENALI_PHY_107 Register

1 EMIF_CTLCFG_DENALI_PHY_107 Register (Offset = 41ACh) [reset = 30000h]

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Table 14-23025. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1ACh**

Figure 14-7640. EMIF_CTLCFG_DENALI_PHY_107 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_0	
NONE						R/W	
0h						3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_0	
NONE						R/W	
0h						0h	

Table 14-23027. EMIF_CTLCFG_DENALI_PHY_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DATA_DC_INIT_DISABLE_0	R/W	3h	Disable duty cycle adjust at initialization for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_0	R/W	0h	Write path clock gating timing for slice 0. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_0	R/W	0h	Write path clock gating disable for slice 0. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.6.6.2.1028 EMIF_CTLCFG_DENALI_PHY_108 Register

1 EMIF_CTLCFG_DENALI_PHY_108 Register (Offset = 41B0h) [reset = 0h]

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Table 14-23028. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1B0h**

Figure 14-7641. EMIF_CTLCFG_DENALI_PHY_108 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ_INIT_SLV_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQS_INIT_SLV_DELAY_0							
R/W							
0h							

Table 14-23030. EMIF_CTLCFG_DENALI_PHY_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_0	R/W	0h	Initial value of write DQ target delay for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_0	R/W	0h	Initial value of write DQS target delay for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1029 EMIF_CTLCFG_DENALI_PHY_109 Register

1 EMIF_CTLCFG_DENALI_PHY_109 Register (Offset = 41B4h) [reset = 0h]

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Table 14-23031. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1B4h

Figure 14-7642. EMIF_CTLCFG_DENALI_PHY_109 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_0
NONE							R/W
0h							0h

Table 14-23033. EMIF_CTLCFG_DENALI_PHY_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_0	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_0	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_WDQLVL_ENABLE_0	R/W	0h	Enable duty cycle adjust during write DQ training for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DATA_DC_WRLVL_ENABLE_0	R/W	0h	Enable duty cycle adjust during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1030 EMIF_CTLCFG_DENALI_PHY_110 Register

1 EMIF_CTLCFG_DENALI_PHY_110 Register (Offset = 41B8h) [reset = 0h]

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Table 14-23034. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1B8h**

Figure 14-7643. EMIF_CTLCFG_DENALI_PHY_110 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED	PHY_MEAS_DLY_STEP_ENABLE_0						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_WDQ_OSC_DELTA_0						
NONE	R/W						
0h	0h						

Table 14-23036. EMIF_CTLCFG_DENALI_PHY_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_WDQ_OSC_DELTA_0	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1031 EMIF_CTLCFG_DENALI_PHY_111 Register

1 EMIF_CTLCFG_DENALI_PHY_111 Register (Offset = 41BCh) [reset = 0h]

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Table 14-23037. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1BCh**

Figure 14-7644. EMIF_CTLCFG_DENALI_PHY_111 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							

Table 14-23039. EMIF_CTLCFG_DENALI_PHY_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_0	R/W	0h	DQ/DM bit swizzling 0 for slice 0. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1032 EMIF_CTLCFG_DENALI_PHY_112 Register

1 EMIF_CTLCFG_DENALI_PHY_112 Register (Offset = 41C0h) [reset = 0h]

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Table 14-23040. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1C0h

Figure 14-7645. EMIF_CTLCFG_DENALI_PHY_112 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_DQ_DM_SWIZZLE1_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-23042. EMIF_CTLCFG_DENALI_PHY_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_0	R/W	0h	DQ/DM bit swizzling 1 for slice 0. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1033 EMIF_CTLCFG_DENALI_PHY_113 Register

1 EMIF_CTLCFG_DENALI_PHY_113 Register (Offset = 41C4h) [reset = 0h]

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Table 14-23043. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1C4h**

Figure 14-7646. EMIF_CTLCFG_DENALI_PHY_113 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ1_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23045. EMIF_CTLCFG_DENALI_PHY_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1034 EMIF_CTLCFG_DENALI_PHY_114 Register

1 EMIF_CTLCFG_DENALI_PHY_114 Register (Offset = 41C8h) [reset = 0h]

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Table 14-23046. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1C8h**

Figure 14-7647. EMIF_CTLCFG_DENALI_PHY_114 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ3_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23048. EMIF_CTLCFG_DENALI_PHY_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1035 EMIF_CTLCFG_DENALI_PHY_115 Register

1 EMIF_CTLCFG_DENALI_PHY_115 Register (Offset = 41CCh) [reset = 0h]

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Table 14-23049. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1CCh**

Figure 14-7648. EMIF_CTLCFG_DENALI_PHY_115 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_CLK_WRDQ5_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_CLK_WRDQ5_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_CLK_WRDQ4_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CLK_WRDQ4_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23051. EMIF_CTLCFG_DENALI_PHY_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1036 EMIF_CTLCFG_DENALI_PHY_116 Register

1 EMIF_CTLCFG_DENALI_PHY_116 Register (Offset = 41D0h) [reset = 0h]

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Table 14-23052. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1D0h**

Figure 14-7649. EMIF_CTLCFG_DENALI_PHY_116 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ7_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ6_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23054. EMIF_CTLCFG_DENALI_PHY_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1037 EMIF_CTLCFG_DENALI_PHY_117 Register

1 EMIF_CTLCFG_DENALI_PHY_117 Register (Offset = 41D4h) [reset = 0h]

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Table 14-23055. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1D4h**

Figure 14-7650. EMIF_CTLCFG_DENALI_PHY_117 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQS_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDM_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23057. EMIF_CTLCFG_DENALI_PHY_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQS for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1038 EMIF_CTLCFG_DENALI_PHY_118 Register

1 EMIF_CTLCFG_DENALI_PHY_118 Register (Offset = 41D8h) [reset = 0h]

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Table 14-23058. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1D8h

Figure 14-7651. EMIF_CTLCFG_DENALI_PHY_118 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_0	
NONE						R/W	
0h						0h	

Table 14-23060. EMIF_CTLCFG_DENALI_PHY_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_0	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1039 EMIF_CTLCFG_DENALI_PHY_119 Register

1 EMIF_CTLCFG_DENALI_PHY_119 Register (Offset = 41DCh) [reset = 0h]

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Table 14-23061. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1DCh**

Figure 14-7652. EMIF_CTLCFG_DENALI_PHY_119 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23063. EMIF_CTLCFG_DENALI_PHY_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1040 EMIF_CTLCFG_DENALI_PHY_120 Register

1 EMIF_CTLCFG_DENALI_PHY_120 Register (Offset = 41E0h) [reset = 0h]

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Table 14-23064. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1E0h**

Figure 14-7653. EMIF_CTLCFG_DENALI_PHY_120 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23066. EMIF_CTLCFG_DENALI_PHY_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1041 EMIF_CTLCFG_DENALI_PHY_121 Register

1 EMIF_CTLCFG_DENALI_PHY_121 Register (Offset = 41E4h) [reset = 0h]

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Table 14-23067. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1E4h**

Figure 14-7654. EMIF_CTLCFG_DENALI_PHY_121 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23069. EMIF_CTLCFG_DENALI_PHY_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1042 EMIF_CTLCFG_DENALI_PHY_122 Register

1 EMIF_CTLCFG_DENALI_PHY_122 Register (Offset = 41E8h) [reset = 0h]

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Table 14-23070. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1E8h**

Figure 14-7655. EMIF_CTLCFG_DENALI_PHY_122 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23072. EMIF_CTLCFG_DENALI_PHY_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1043 EMIF_CTLCFG_DENALI_PHY_123 Register

1 EMIF_CTLCFG_DENALI_PHY_123 Register (Offset = 41ECh) [reset = 0h]

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Table 14-23073. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1ECh**

Figure 14-7656. EMIF_CTLCFG_DENALI_PHY_123 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23075. EMIF_CTLCFG_DENALI_PHY_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1044 EMIF_CTLCFG_DENALI_PHY_124 Register

1 EMIF_CTLCFG_DENALI_PHY_124 Register (Offset = 41F0h) [reset = 0h]

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Table 14-23076. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1F0h

Figure 14-7657. EMIF_CTLCFG_DENALI_PHY_124 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23078. EMIF_CTLCFG_DENALI_PHY_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1045 EMIF_CTLCFG_DENALI_PHY_125 Register

1 EMIF_CTLCFG_DENALI_PHY_125 Register (Offset = 41F4h) [reset = 0h]

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Table 14-23079. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1F4h

Figure 14-7658. EMIF_CTLCFG_DENALI_PHY_125 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23081. EMIF_CTLCFG_DENALI_PHY_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1046 EMIF_CTLCFG_DENALI_PHY_126 Register

1 EMIF_CTLCFG_DENALI_PHY_126 Register (Offset = 41F8h) [reset = 0h]

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Table 14-23082. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C1F8h**

Figure 14-7659. EMIF_CTLCFG_DENALI_PHY_126 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DM_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23084. EMIF_CTLCFG_DENALI_PHY_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1047 EMIF_CTLCFG_DENALI_PHY_127 Register

1 EMIF_CTLCFG_DENALI_PHY_127 Register (Offset = 41FCh) [reset = 0h]

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Table 14-23085. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C1FCh

Figure 14-7660. EMIF_CTLCFG_DENALI_PHY_127 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_GATE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DM_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-23087. EMIF_CTLCFG_DENALI_PHY_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_0	R/W	0h	Read DQS target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1048 EMIF_CTLCFG_DENALI_PHY_128 Register

1 EMIF_CTLCFG_DENALI_PHY_128 Register (Offset = 4200h) [reset = 0h]

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Table 14-23088. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C200h**

Figure 14-7661. EMIF_CTLCFG_DENALI_PHY_128 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_DELAY_EARLY_THRESHOLD_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_WRITE_PATH_LAT_ADD_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_LATENCY_ADJUST_0			
NONE				R/W			
0h				0h			

Table 14-23090. EMIF_CTLCFG_DENALI_PHY_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_0	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_0	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1049 EMIF_CTLCFG_DENALI_PHY_129 Register

1 EMIF_CTLCFG_DENALI_PHY_129 Register (Offset = 4204h) [reset = 0h]

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Table 14-23091. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C204h**

Figure 14-7662. EMIF_CTLCFG_DENALI_PHY_129 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_EARLY_FORCE_ZERO_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0							
R/W							
0h							

Table 14-23093. EMIF_CTLCFG_DENALI_PHY_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_0	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1050 EMIF_CTLCFG_DENALI_PHY_130 Register

1 EMIF_CTLCFG_DENALI_PHY_130 Register (Offset = 4208h) [reset = 0h]

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Table 14-23094. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C208h**

Figure 14-7663. EMIF_CTLCFG_DENALI_PHY_130 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_0							
R/W							
0h							

Table 14-23096. EMIF_CTLCFG_DENALI_PHY_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_0	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_0	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1051 EMIF_CTLCFG_DENALI_PHY_131 Register

1 EMIF_CTLCFG_DENALI_PHY_131 Register (Offset = 420Ch) [reset = 0h]

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Table 14-23097. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C20Ch**

Figure 14-7664. EMIF_CTLCFG_DENALI_PHY_131 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PASS_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_NTP_WRLAT_START_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_START_0							
R/W							
0h							

Table 14-23099. EMIF_CTLCFG_DENALI_PHY_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_0	R/W	0h	Indicates if No-topology training found a passing result for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_0	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_0	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1052 EMIF_CTLCFG_DENALI_PHY_132 Register

1 EMIF_CTLCFG_DENALI_PHY_132 Register (Offset = 4210h) [reset = 0h]

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Table 14-23100. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C210h

Figure 14-7665. EMIF_CTLCFG_DENALI_PHY_132 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0							
R/W							
0h							

Table 14-23102. EMIF_CTLCFG_DENALI_PHY_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1053 EMIF_CTLCFG_DENALI_PHY_133 Register

1 EMIF_CTLCFG_DENALI_PHY_133 Register (Offset = 4214h) [reset = 20202020h]

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Table 14-23103. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C214h**

Figure 14-7666. EMIF_CTLCFG_DENALI_PHY_133 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_0							
R/W							
20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_0							
R/W							
20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_0							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_0							
R/W							
20h							

Table 14-23105. EMIF_CTLCFG_DENALI_PHY_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ2_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ1_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ0_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQS_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1054 EMIF_CTLCFG_DENALI_PHY_134 Register

1 EMIF_CTLCFG_DENALI_PHY_134 Register (Offset = 4218h) [reset = 20202020h]

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Table 14-23106. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C218h**

Figure 14-7667. EMIF_CTLCFG_DENALI_PHY_134 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ6_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ5_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ4_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ3_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-23108. EMIF_CTLCFG_DENALI_PHY_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ6_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ5_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ4_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ3_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1055 EMIF_CTLCFG_DENALI_PHY_135 Register

1 EMIF_CTLCFG_DENALI_PHY_135 Register (Offset = 421Ch) [reset = 2020h]

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Table 14-23109. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C21Ch**

Figure 14-7668. EMIF_CTLCFG_DENALI_PHY_135 Name Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DATA_DC_DM_CLK_ADJUST_0							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQ7_CLK_ADJUST_0							
R/W							
20h							

Table 14-23111. EMIF_CTLCFG_DENALI_PHY_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_DSLICE_PAD_BOOSTPN_SETTING_0	R/W	0h	Setting for boost P/N of pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DM_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ7_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1056 EMIF_CTLCFG_DENALI_PHY_136 Register

1 EMIF_CTLCFG_DENALI_PHY_136 Register (Offset = 4220h) [reset = 0h]

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Table 14-23112. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C220h

Figure 14-7669. EMIF_CTLCFG_DENALI_PHY_136 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTLE_SETTING_0					
NONE		R/W					
0h		0h					

Table 14-23114. EMIF_CTLCFG_DENALI_PHY_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DQS_FFE_0	R/W	0h	TX_FFE setting for DQS pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DQ_FFE_0	R/W	0h	TX_FFE setting for DQ/DM pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DSLICE_PAD_RX_CTLE_SETTING_0	R/W	0h	Setting for RX ctle P/N of pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1057 EMIF_CTLCFG_DENALI_PHY_256 Register

1 EMIF_CTLCFG_DENALI_PHY_256 Register (Offset = 4400h) [reset = 0h]

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Table 14-23115. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C400h

Figure 14-7670. EMIF_CTLCFG_DENALI_PHY_256 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WR_BYPASS_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_1						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		

Table 14-23117. EMIF_CTLCFG_DENALI_PHY_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_1	R/W	0h	Write data clock bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_1	R/W	0h	Controls PCLK/PARK pin for pad for slice 1 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_1	R/W	0h	RX_PCLK boot clock frequency selection for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1058 EMIF_CTLCFG_DENALI_PHY_257 Register

1 EMIF_CTLCFG_DENALI_PHY_257 Register (Offset = 4404h) [reset = 0h]

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Table 14-23118. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C404h**

Figure 14-7671. EMIF_CTLCFG_DENALI_PHY_257 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_1			
NONE				R/W			
0h				0h			

Table 14-23120. EMIF_CTLCFG_DENALI_PHY_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_1	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	R/W	0h	Write DQS bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1059 EMIF_CTLCFG_DENALI_PHY_258 Register

1 EMIF_CTLCFG_DENALI_PHY_258 Register (Offset = 4408h) [reset = 0h]

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Table 14-23121. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C408h**

Figure 14-7672. EMIF_CTLCFG_DENALI_PHY_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23123. EMIF_CTLCFG_DENALI_PHY_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_1	R/W	0h	Bypass mode override setting for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_1	R/W	0h	Two_cycle_preamble for bypass mode for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1060 EMIF_CTLCFG_DENALI_PHY_259 Register

1 EMIF_CTLCFG_DENALI_PHY_259 Register (Offset = 440Ch) [reset = 0h]

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Table 14-23124. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C40Ch

Figure 14-7673. EMIF_CTLCFG_DENALI_PHY_259 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_1					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-23126. EMIF_CTLCFG_DENALI_PHY_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23126. EMIF_CTLCFG_DENALI_PHY_259 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1061 EMIF_CTLCFG_DENALI_PHY_260 Register

1 EMIF_CTLCFG_DENALI_PHY_260 Register (Offset = 4410h) [reset = 0h]

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Table 14-23127. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C410h**

Figure 14-7674. EMIF_CTLCFG_DENALI_PHY_260 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-23129. EMIF_CTLCFG_DENALI_PHY_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23129. EMIF_CTLCFG_DENALI_PHY_260 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1062 EMIF_CTLCFG_DENALI_PHY_261 Register

1 EMIF_CTLCFG_DENALI_PHY_261 Register (Offset = 4414h) [reset = 1000000h]

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Table 14-23130. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C414h**

Figure 14-7675. EMIF_CTLCFG_DENALI_PHY_261 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_1
NONE							R/W
0h							1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PER_RANK_CS_MAP_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_SW_WRDQS_SHIFT_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDM_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-23132. EMIF_CTLCFG_DENALI_PHY_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_PER_CS_TRAINING_MULTICAST_EN_1	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_PER_RANK_CS_MAP_1	R/W	0h	Per-rank CS map for slice 1. Setting a bit uses that CS for the rank, bit [0] uses CS0, bit [1] uses CS1, etc. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23132. EMIF_CTLCFG_DENALI_PHY_261 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1063 EMIF_CTLCFG_DENALI_PHY_262 Register

1 EMIF_CTLCFG_DENALI_PHY_262 Register (Offset = 4418h) [reset = 0h]

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Table 14-23133. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C418h**

Figure 14-7676. EMIF_CTLCFG_DENALI_PHY_262 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_LP4_BOOT_RDDATA_EN_DLY_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PER_CS_TRAINING_INDEX_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-23135. EMIF_CTLCFG_DENALI_PHY_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_LP4_BOOT_RDDATA_EN_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_INDEX_1	R/W	0h	For per-rank training, indicates which rank's paramters are read/written for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1064 EMIF_CTLCFG_DENALI_PHY_263 Register

1 EMIF_CTLCFG_DENALI_PHY_263 Register (Offset = 441Ch) [reset = 0h]

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Table 14-23136. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C41Ch

Figure 14-7677. EMIF_CTLCFG_DENALI_PHY_263 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_1			
NONE				R/W			
0h				0h			

Table 14-23138. EMIF_CTLCFG_DENALI_PHY_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 1. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_LP4_BOOT_RPTR_UPDATE_1	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1065 EMIF_CTLCFG_DENALI_PHY_264 Register

1 EMIF_CTLCFG_DENALI_PHY_264 Register (Offset = 4420h) [reset = 0h]

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Table 14-23139. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C420h

Figure 14-7678. EMIF_CTLCFG_DENALI_PHY_264 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_1	
NONE						R/W	
0h						0h	

Table 14-23141. EMIF_CTLCFG_DENALI_PHY_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LPBK_DFX_TIMEOUT_EN_1	R/W	0h	Loopback read only test timeout mechanism enable for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_LPBK_CONTROL_1	R/W	0h	Loopback control bits for slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CTRL_LPBK_EN_1	R/W	0h	Loopback control en for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1066 EMIF_CTLCFG_DENALI_PHY_265 Register

1 EMIF_CTLCFG_DENALI_PHY_265 Register (Offset = 4424h) [reset = 0h]

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Table 14-23142. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C424h

Figure 14-7679. EMIF_CTLCFG_DENALI_PHY_265 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_GATE_DELAY_COMP_DISABLE_1
NONE							R/W
0h							0h

Table 14-23144. EMIF_CTLCFG_DENALI_PHY_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_GATE_DELAY_COMP_DISABLE_1	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1067 EMIF_CTLCFG_DENALI_PHY_266 Register

1 EMIF_CTLCFG_DENALI_PHY_266 Register (Offset = 4428h) [reset = 0h]

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Table 14-23145. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C428h**

Figure 14-7680. EMIF_CTLCFG_DENALI_PHY_266 Name Register

31	30	29	28	27	26	25	24
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							

Table 14-23147. EMIF_CTLCFG_DENALI_PHY_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_1	R/W	0h	Auto timing marging control bits for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1068 EMIF_CTLCFG_DENALI_PHY_267 Register

1 EMIF_CTLCFG_DENALI_PHY_267 Register (Offset = 442Ch) [reset = 0h]

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Table 14-23148. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C42Ch**

Figure 14-7681. EMIF_CTLCFG_DENALI_PHY_267 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_1			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							

Table 14-23150. EMIF_CTLCFG_DENALI_PHY_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_1	R	0h	Observation register for the auto_timing_margin for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1069 EMIF_CTLCFG_DENALI_PHY_268 Register

1 EMIF_CTLCFG_DENALI_PHY_268 Register (Offset = 4430h) [reset = 1000000h]

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Table 14-23151. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C430h**

Figure 14-7682. EMIF_CTLCFG_DENALI_PHY_268 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_1						
NONE	R/W						
0h	1h						
23	22	21	20	19	18	17	16
RESERVED							PHY_PDA_MODE_EN_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_DQ_IDLE_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DQ_IDLE_1							
R/W							
0h							

Table 14-23153. EMIF_CTLCFG_DENALI_PHY_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_1	R/W	1h	PRBS7 start pattern for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_1	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_1	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1070 EMIF_CTLCFG_DENALI_PHY_269 Register

1 EMIF_CTLCFG_DENALI_PHY_269 Register (Offset = 4434h) [reset = 0h]

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Table 14-23154. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C434h**

Figure 14-7683. EMIF_CTLCFG_DENALI_PHY_269 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTI_PATT_RST_DISABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_RDLVL_MULTI_PATT_ENABLE_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_PRBS_PATTERN_MASK_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PRBS_PATTERN_MASK_1							
R/W							
0h							

Table 14-23156. EMIF_CTLCFG_DENALI_PHY_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_1	R/W	0h	Read Leveling read level windows disable reset for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_1	R/W	0h	Read Leveling Multi-pattern enable for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_1	R/W	0h	PRBS7 mask signal for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1071 EMIF_CTLCFG_DENALI_PHY_270 Register

1 EMIF_CTLCFG_DENALI_PHY_270 Register (Offset = 4438h) [reset = 0h]

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Table 14-23157. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C438h**

Figure 14-7684. EMIF_CTLCFG_DENALI_PHY_270 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_VREF_TRAIN_OBS_1						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_VREF_INITIAL_STEPSIZE_1					
NONE		R/W					
0h		0h					

Table 14-23159. EMIF_CTLCFG_DENALI_PHY_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_1	R	0h	Observation register for best vref value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_1	R/W	0h	Data slice initial VREF training step size for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1072 EMIF_CTLCFG_DENALI_PHY_271 Register

1 EMIF_CTLCFG_DENALI_PHY_271 Register (Offset = 443Ch) [reset = 0h]

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Table 14-23160. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C43Ch**

Figure 14-7685. EMIF_CTLCFG_DENALI_PHY_271 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_1
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
PHY_GATE_SMPL1_SLAVE_DELAY_1							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED							SC_PHY_SNAP_OBS_REGS_1
NONE							W
0h							0h

7	6	5	4	3	2	1	0
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_1			
NONE				R/W			
0h				0h			

Table 14-23162. EMIF_CTLCFG_DENALI_PHY_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_1	W	0h	Initiates a snapshot of the internal observation registers for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_1	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1073 EMIF_CTLCFG_DENALI_PHY_272 Register

1 EMIF_CTLCFG_DENALI_PHY_272 Register (Offset = 4440h) [reset = 0h]

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Table 14-23163. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C440h**

Figure 14-7686. EMIF_CTLCFG_DENALI_PHY_272 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MEM_CLASS_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LPDDR_1
NONE							R/W
0h							0h

Table 14-23165. EMIF_CTLCFG_DENALI_PHY_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_1	R/W	0h	Indicates the type of DRAM for slice 1. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_1	R/W	0h	Adds a cycle of delay for the slice 1 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.6.6.2.1074 EMIF_CTLCFG_DENALI_PHY_273 Register

1 EMIF_CTLCFG_DENALI_PHY_273 Register (Offset = 4444h) [reset = 0h]

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Table 14-23166. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C444h**

Figure 14-7687. EMIF_CTLCFG_DENALI_PHY_273 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ON_FLY_GATE_ADJUST_EN_1	
NONE						R/W	
0h						0h	

Table 14-23168. EMIF_CTLCFG_DENALI_PHY_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_1	R/W	0h	Control the on-the-fly gate adjustment for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1075 EMIF_CTLCFG_DENALI_PHY_274 Register

1 EMIF_CTLCFG_DENALI_PHY_274 Register (Offset = 4448h) [reset = 0h]

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Table 14-23169. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C448h**

Figure 14-7688. EMIF_CTLCFG_DENALI_PHY_274 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_1							
R							
0h							

Table 14-23171. EMIF_CTLCFG_DENALI_PHY_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_1	R	0h	Report the on-the-fly gate measurement result for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1076 EMIF_CTLCFG_DENALI_PHY_275 Register

1 EMIF_CTLCFG_DENALI_PHY_275 Register (Offset = 444Ch) [reset = 0h]

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Table 14-23172. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C44Ch**

Figure 14-7689. EMIF_CTLCFG_DENALI_PHY_275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_1
NONE							R/W
0h							0h

Table 14-23174. EMIF_CTLCFG_DENALI_PHY_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_PST_AMBLE_1	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DFI40_POLARITY_1	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1077 EMIF_CTLCFG_DENALI_PHY_276 Register

1 EMIF_CTLCFG_DENALI_PHY_276 Register (Offset = 4450h) [reset = 0h]

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Table 14-23175. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C450h**

Figure 14-7690. EMIF_CTLCFG_DENALI_PHY_276 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_1							
R/W							
0h							

Table 14-23177. EMIF_CTLCFG_DENALI_PHY_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_1	R/W	0h	Read leveling pattern 8 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1078 EMIF_CTLCFG_DENALI_PHY_277 Register

1 EMIF_CTLCFG_DENALI_PHY_277 Register (Offset = 4454h) [reset = 0h]

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Table 14-23178. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C454h**

Figure 14-7691. EMIF_CTLCFG_DENALI_PHY_277 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT9_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT9_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_1							
R/W							
0h							

Table 14-23180. EMIF_CTLCFG_DENALI_PHY_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_1	R/W	0h	Read leveling pattern 9 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1079 EMIF_CTLCFG_DENALI_PHY_278 Register

1 EMIF_CTLCFG_DENALI_PHY_278 Register (Offset = 4458h) [reset = 0h]

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Table 14-23181. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C458h**

Figure 14-7692. EMIF_CTLCFG_DENALI_PHY_278 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT10_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT10_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_1							
R/W							
0h							

Table 14-23183. EMIF_CTLCFG_DENALI_PHY_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_1	R/W	0h	Read leveling pattern 10 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1080 EMIF_CTLCFG_DENALI_PHY_279 Register

1 EMIF_CTLCFG_DENALI_PHY_279 Register (Offset = 445Ch) [reset = 0h]

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Table 14-23184. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C45Ch

Figure 14-7693. EMIF_CTLCFG_DENALI_PHY_279 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_1							
R/W							
0h							

Table 14-23186. EMIF_CTLCFG_DENALI_PHY_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_1	R/W	0h	Read leveling pattern 11 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1081 EMIF_CTLCFG_DENALI_PHY_280 Register

1 EMIF_CTLCFG_DENALI_PHY_280 Register (Offset = 4460h) [reset = 0h]

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Table 14-23187. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C460h**

Figure 14-7694. EMIF_CTLCFG_DENALI_PHY_280 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_1							
R/W							
0h							

Table 14-23189. EMIF_CTLCFG_DENALI_PHY_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_1	R/W	0h	Read leveling pattern 12 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1082 EMIF_CTLCFG_DENALI_PHY_281 Register

1 EMIF_CTLCFG_DENALI_PHY_281 Register (Offset = 4464h) [reset = 0h]

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Table 14-23190. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C464h**

Figure 14-7695. EMIF_CTLCFG_DENALI_PHY_281 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT13_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT13_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_1							
R/W							
0h							

Table 14-23192. EMIF_CTLCFG_DENALI_PHY_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_1	R/W	0h	Read leveling pattern 13 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1083 EMIF_CTLCFG_DENALI_PHY_282 Register

1 EMIF_CTLCFG_DENALI_PHY_282 Register (Offset = 4468h) [reset = 0h]

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Table 14-23193. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C468h**

Figure 14-7696. EMIF_CTLCFG_DENALI_PHY_282 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_1							
R/W							
0h							

Table 14-23195. EMIF_CTLCFG_DENALI_PHY_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_1	R/W	0h	Read leveling pattern 14 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1084 EMIF_CTLCFG_DENALI_PHY_283 Register

1 EMIF_CTLCFG_DENALI_PHY_283 Register (Offset = 446Ch) [reset = 0h]

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Table 14-23196. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C46Ch**

Figure 14-7697. EMIF_CTLCFG_DENALI_PHY_283 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_1							
R/W							
0h							

Table 14-23198. EMIF_CTLCFG_DENALI_PHY_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_1	R/W	0h	Read leveling pattern 15 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1085 EMIF_CTLCFG_DENALI_PHY_284 Register

1 EMIF_CTLCFG_DENALI_PHY_284 Register (Offset = 4470h) [reset = 0h]

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Table 14-23199. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C470h**

Figure 14-7698. EMIF_CTLCFG_DENALI_PHY_284 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_MASTER_DLY_LOCK_OBS_SELECT_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_1		
NONE					R/W		
0h					0h		

Table 14-23201. EMIF_CTLCFG_DENALI_PHY_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_1	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_1	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 1. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_1	R/W	0h	Reserved for future use for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1086 EMIF_CTLCFG_DENALI_PHY_285 Register

1 EMIF_CTLCFG_DENALI_PHY_285 Register (Offset = 4474h) [reset = 0h]

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Table 14-23202. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C474h**

Figure 14-7699. EMIF_CTLCFG_DENALI_PHY_285 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_1			
NONE				R/W			
0h				0h			

Table 14-23204. EMIF_CTLCFG_DENALI_PHY_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_1	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1087 EMIF_CTLCFG_DENALI_PHY_286 Register

1 EMIF_CTLCFG_DENALI_PHY_286 Register (Offset = 4478h) [reset = 0h]

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Table 14-23205. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C478h**

Figure 14-7700. EMIF_CTLCFG_DENALI_PHY_286 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_1
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_1
NONE							R/W
0h							0h

Table 14-23207. EMIF_CTLCFG_DENALI_PHY_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_1	R/W	0h	Write leveling algorithm selection for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_1	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_1	R/W	0h	Enables leveling debug mode for slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1088 EMIF_CTLCFG_DENALI_PHY_287 Register

1 EMIF_CTLCFG_DENALI_PHY_287 Register (Offset = 447Ch) [reset = 0h]

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Table 14-23208. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C47Ch**

Figure 14-7701. EMIF_CTLCFG_DENALI_PHY_287 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_GTLVL_UPDT_WAIT_CNT_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_GTLVL_CAPTURE_CNT_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQ_MASK_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_WRLVL_UPDT_WAIT_CNT_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-23210. EMIF_CTLCFG_DENALI_PHY_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 1. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_1	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1089 EMIF_CTLCFG_DENALI_PHY_288 Register

1 EMIF_CTLCFG_DENALI_PHY_288 Register (Offset = 4480h) [reset = 0h]

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Table 14-23211. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C480h**

Figure 14-7702. EMIF_CTLCFG_DENALI_PHY_288 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PHY_RDLVL_OP_MODE_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_RDLVL_CAPTURE_CNT_1					
NONE		R/W					
0h		0h					

Table 14-23213. EMIF_CTLCFG_DENALI_PHY_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_1	R/W	0h	Read leveling algorithm select for slice 1. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1090 EMIF_CTLCFG_DENALI_PHY_289 Register

1 EMIF_CTLCFG_DENALI_PHY_289 Register (Offset = 4484h) [reset = 0h]

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Table 14-23214. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C484h**

Figure 14-7703. EMIF_CTLCFG_DENALI_PHY_289 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_DATA_SWIZZLE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_DATA_SWIZZLE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_DATA_MASK_1							
R/W							
0h							

Table 14-23216. EMIF_CTLCFG_DENALI_PHY_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_1	R/W	0h	Read level bit swizzling for DDR4 operation for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_1	R/W	0h	Per-bit mask for read leveling for slice 1. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1091 EMIF_CTLCFG_DENALI_PHY_290 Register

1 EMIF_CTLCFG_DENALI_PHY_290 Register (Offset = 4488h) [reset = 0h]

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Table 14-23217. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C488h**

Figure 14-7704. EMIF_CTLCFG_DENALI_PHY_290 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WDQLVL_PATT_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_WDQLVL_BURST_CNT_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_CLK_JITTER_TOLERANCE_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23219. EMIF_CTLCFG_DENALI_PHY_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_1	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 1. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_1	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_1	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1092 EMIF_CTLCFG_DENALI_PHY_291 Register

1 EMIF_CTLCFG_DENALI_PHY_291 Register (Offset = 448Ch) [reset = 0h]

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Table 14-23220. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C48Ch

Figure 14-7705. EMIF_CTLCFG_DENALI_PHY_291 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1							
R/W							
0h							

Table 14-23222. EMIF_CTLCFG_DENALI_PHY_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1093 EMIF_CTLCFG_DENALI_PHY_292 Register

1 EMIF_CTLCFG_DENALI_PHY_292 Register (Offset = 4490h) [reset = 0h]

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Table 14-23223. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C490h**

Figure 14-7706. EMIF_CTLCFG_DENALI_PHY_292 Name Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_WDQLVL_CLR_PREV_RESULTS_1
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_DM_DLY_STEP_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DQ_SLV_DELTA_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_SELECT_1							
R/W							
0h							

Table 14-23225. EMIF_CTLCFG_DENALI_PHY_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_1	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_1	R/W	0h	The target delay line step for DM training for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_1	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_1	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1094 EMIF_CTLCFG_DENALI_PHY_293 Register

1 EMIF_CTLCFG_DENALI_PHY_293 Register (Offset = 4494h) [reset = 0h]

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Table 14-23226. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C494h**

Figure 14-7707. EMIF_CTLCFG_DENALI_PHY_293 Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_WDQLVL_DATADM_MASK_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DATADM_MASK_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23228. EMIF_CTLCFG_DENALI_PHY_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_1	R/W	0h	Per-bit mask for write data leveling for slice 1. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1095 EMIF_CTLCFG_DENALI_PHY_294 Register

1 EMIF_CTLCFG_DENALI_PHY_294 Register (Offset = 4498h) [reset = 0h]

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Table 14-23229. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C498h**

Figure 14-7708. EMIF_CTLCFG_DENALI_PHY_294 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT0_1							
R/W							
0h							

Table 14-23231. EMIF_CTLCFG_DENALI_PHY_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1096 EMIF_CTLCFG_DENALI_PHY_295 Register

1 EMIF_CTLCFG_DENALI_PHY_295 Register (Offset = 449Ch) [reset = 0h]

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Table 14-23232. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C49Ch**

Figure 14-7709. EMIF_CTLCFG_DENALI_PHY_295 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT1_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT1_1							
R/W							
0h							

Table 14-23234. EMIF_CTLCFG_DENALI_PHY_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1097 EMIF_CTLCFG_DENALI_PHY_296 Register

1 EMIF_CTLCFG_DENALI_PHY_296 Register (Offset = 44A0h) [reset = 0h]

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Table 14-23235. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4A0h**

Figure 14-7710. EMIF_CTLCFG_DENALI_PHY_296 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT2_1							
R/W							
0h							

Table 14-23237. EMIF_CTLCFG_DENALI_PHY_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1098 EMIF_CTLCFG_DENALI_PHY_297 Register

1 EMIF_CTLCFG_DENALI_PHY_297 Register (Offset = 44A4h) [reset = 0h]

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Table 14-23238. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4A4h**

Figure 14-7711. EMIF_CTLCFG_DENALI_PHY_297 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_1							
R/W							
0h							

23	22	21	20	19	18	17	16
PHY_USER_PATT3_1							
R/W							
0h							

15	14	13	12	11	10	9	8
PHY_USER_PATT3_1							
R/W							
0h							

7	6	5	4	3	2	1	0
PHY_USER_PATT3_1							
R/W							
0h							

Table 14-23240. EMIF_CTLCFG_DENALI_PHY_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1099 EMIF_CTLCFG_DENALI_PHY_298 Register

1 EMIF_CTLCFG_DENALI_PHY_298 Register (Offset = 44A8h) [reset = 0h]

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Table 14-23241. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4A8h**

Figure 14-7712. EMIF_CTLCFG_DENALI_PHY_298 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_NTP_MULT_TRAIN_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_USER_PATT4_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_USER_PATT4_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23243. EMIF_CTLCFG_DENALI_PHY_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_1	R/W	0h	Control for single pass only No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1100 EMIF_CTLCFG_DENALI_PHY_299 Register

1 EMIF_CTLCFG_DENALI_PHY_299 Register (Offset = 44ACh) [reset = 0h]

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Table 14-23244. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4ACh**

Figure 14-7713. EMIF_CTLCFG_DENALI_PHY_299 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_PERIOD_THRESHOLD_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_NTP_EARLY_THRESHOLD_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_EARLY_THRESHOLD_1							
R/W							
0h							

Table 14-23246. EMIF_CTLCFG_DENALI_PHY_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_1	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_1	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1101 EMIF_CTLCFG_DENALI_PHY_300 Register

1 EMIF_CTLCFG_DENALI_PHY_300 Register (Offset = 44B0h) [reset = 0h]

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Table 14-23247. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4B0h

Figure 14-7714. EMIF_CTLCFG_DENALI_PHY_300 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_MAX_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_PERIOD_THRESHOLD_MIN_1							
R/W							
0h							

Table 14-23249. EMIF_CTLCFG_DENALI_PHY_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_1	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_1	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1102 EMIF_CTLCFG_DENALI_PHY_301 Register

1 EMIF_CTLCFG_DENALI_PHY_301 Register (Offset = 44B4h) [reset = 0h]

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Table 14-23250. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4B4h**

Figure 14-7715. EMIF_CTLCFG_DENALI_PHY_301 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_FIFO_PTR_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		SC_PHY_MANUAL_CLEAR_1					
NONE		W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_1
NONE							R/W
0h							0h

Table 14-23252. EMIF_CTLCFG_DENALI_PHY_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_1	R	0h	Observation register containing read entry FIFO pointers for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_1	W	0h	Manual reset/clear of internal logic for slice 1. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_1	R/W	0h	Indicates if slice 1 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1103 EMIF_CTLCFG_DENALI_PHY_302 Register

1 EMIF_CTLCFG_DENALI_PHY_302 Register (Offset = 44B8h) [reset = 100000h]

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Table 14-23253. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4B8h

Figure 14-7716. EMIF_CTLCFG_DENALI_PHY_302 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_1							
R							
100000h							

Table 14-23255. EMIF_CTLCFG_DENALI_PHY_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_1	R	100000h	Observation register containing loopback status/results for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1104 EMIF_CTLCFG_DENALI_PHY_303 Register

1 EMIF_CTLCFG_DENALI_PHY_303 Register (Offset = 44BCh) [reset = 0h]

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Table 14-23256. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4BCh**

Figure 14-7717. EMIF_CTLCFG_DENALI_PHY_303 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MASTER_DLY_LOCK_OBS_1		
NONE					R		
0h					0h		
23	22	21	20	19	18	17	16
PHY_MASTER_DLY_LOCK_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_LPBK_ERROR_COUNT_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_1							
R							
0h							

Table 14-23258. EMIF_CTLCFG_DENALI_PHY_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_1	R	0h	Observation register containing controller delay results for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_1	R	0h	Observation register containing total number of loopback error data for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1105 EMIF_CTLCFG_DENALI_PHY_304 Register

1 EMIF_CTLCFG_DENALI_PHY_304 Register (Offset = 44C0h) [reset = 0h]

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Table 14-23259. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4C0h**

Figure 14-7718. EMIF_CTLCFG_DENALI_PHY_304 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MEAS_DLY_STEP_VALUE_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						

Table 14-23261. EMIF_CTLCFG_DENALI_PHY_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_1	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQ target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1106 EMIF_CTLCFG_DENALI_PHY_305 Register

1 EMIF_CTLCFG_DENALI_PHY_305 Register (Offset = 44C4h) [reset = 0h]

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Table 14-23262. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4C4h

Figure 14-7719. EMIF_CTLCFG_DENALI_PHY_305 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							

Table 14-23264. EMIF_CTLCFG_DENALI_PHY_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQS base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS gate target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1107 EMIF_CTLCFG_DENALI_PHY_306 Register

1 EMIF_CTLCFG_DENALI_PHY_306 Register (Offset = 44C8h) [reset = 0h]

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Table 14-23265. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4C8h**

Figure 14-7720. EMIF_CTLCFG_DENALI_PHY_306 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_1		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1							
R							
0h							

Table 14-23267. EMIF_CTLCFG_DENALI_PHY_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_1	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQ base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1108 EMIF_CTLCFG_DENALI_PHY_307 Register

1 EMIF_CTLCFG_DENALI_PHY_307 Register (Offset = 44CCh) [reset = 0h]

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Table 14-23268. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4CCh

Figure 14-7721. EMIF_CTLCFG_DENALI_PHY_307 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_1	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_HARD1_DELAY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_1	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_HARD0_DELAY_OBS_1							
R							
0h							

Table 14-23270. EMIF_CTLCFG_DENALI_PHY_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1109 EMIF_CTLCFG_DENALI_PHY_308 Register

1 EMIF_CTLCFG_DENALI_PHY_308 Register (Offset = 44D0h) [reset = 0h]

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Table 14-23271. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4D0h

Figure 14-7722. EMIF_CTLCFG_DENALI_PHY_308 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_WRLVL_STATUS_OBS_1				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
PHY_WRLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_1							
R							
0h							

Table 14-23273. EMIF_CTLCFG_DENALI_PHY_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_1	R	0h	Observation register containing write leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1110 EMIF_CTLCFG_DENALI_PHY_309 Register

1 EMIF_CTLCFG_DENALI_PHY_309 Register (Offset = 44D4h) [reset = 0h]

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Table 14-23274. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4D4h**

Figure 14-7723. EMIF_CTLCFG_DENALI_PHY_309 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1							
R							
0h							

Table 14-23276. EMIF_CTLCFG_DENALI_PHY_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample2 target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample1 target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1111 EMIF_CTLCFG_DENALI_PHY_310 Register

1 EMIF_CTLCFG_DENALI_PHY_310 Register (Offset = 44D8h) [reset = 0h]

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Table 14-23277. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C4D8h

Figure 14-7724. EMIF_CTLCFG_DENALI_PHY_310 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD0_DELAY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_ERROR_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_ERROR_OBS_1							
R							
0h							

Table 14-23279. EMIF_CTLCFG_DENALI_PHY_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_WRLVL_ERROR_OBS_1	R	0h	Observation register containing write leveling error status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1112 EMIF_CTLCFG_DENALI_PHY_311 Register

1 EMIF_CTLCFG_DENALI_PHY_311 Register (Offset = 44DCh) [reset = 0h]

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Table 14-23280. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4DCh**

Figure 14-7725. EMIF_CTLCFG_DENALI_PHY_311 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_1					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_HARD1_DELAY_OBS_1							
R							
0h							

Table 14-23282. EMIF_CTLCFG_DENALI_PHY_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1113 EMIF_CTLCFG_DENALI_PHY_312 Register

1 EMIF_CTLCFG_DENALI_PHY_312 Register (Offset = 44E0h) [reset = 0h]

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Table 14-23283. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4E0h**

Figure 14-7726. EMIF_CTLCFG_DENALI_PHY_312 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_GTLVL_STATUS_OBS_1	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_GTLVL_STATUS_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_STATUS_OBS_1							
R							
0h							

Table 14-23285. EMIF_CTLCFG_DENALI_PHY_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_1	R	0h	Observation register containing gate training status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1114 EMIF_CTLCFG_DENALI_PHY_313 Register

1 EMIF_CTLCFG_DENALI_PHY_313 Register (Offset = 44E4h) [reset = 0h]

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Table 14-23286. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4E4h**

Figure 14-7727. EMIF_CTLCFG_DENALI_PHY_313 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1							
R							
0h							

Table 14-23288. EMIF_CTLCFG_DENALI_PHY_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1115 EMIF_CTLCFG_DENALI_PHY_314 Register

1 EMIF_CTLCFG_DENALI_PHY_314 Register (Offset = 44E8h) [reset = 0h]

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Table 14-23289. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4E8h**

Figure 14-7728. EMIF_CTLCFG_DENALI_PHY_314 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	
NONE						R	
0h						0h	

Table 14-23291. EMIF_CTLCFG_DENALI_PHY_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	R	0h	Observation register containing read leveling number of windows found for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1116 EMIF_CTLCFG_DENALI_PHY_315 Register

1 EMIF_CTLCFG_DENALI_PHY_315 Register (Offset = 44ECh) [reset = 0h]

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Table 14-23292. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4ECh**

Figure 14-7729. EMIF_CTLCFG_DENALI_PHY_315 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_1							
R							
0h							

Table 14-23294. EMIF_CTLCFG_DENALI_PHY_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_1	R	0h	Observation register containing read leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1117 EMIF_CTLCFG_DENALI_PHY_316 Register

1 EMIF_CTLCFG_DENALI_PHY_316 Register (Offset = 44F0h) [reset = 7FF0000h]

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Table 14-23295. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4F0h**

Figure 14-7730. EMIF_CTLCFG_DENALI_PHY_316 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WDQLVL_DQDM_TE_DLY_OBS_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">7FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DQDM_TE_DLY_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WDQLVL_DQDM_LE_DLY_OBS_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DQDM_LE_DLY_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23297. EMIF_CTLCFG_DENALI_PHY_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_1	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_1	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1118 EMIF_CTLCFG_DENALI_PHY_317 Register

1 EMIF_CTLCFG_DENALI_PHY_317 Register (Offset = 44F4h) [reset = 0h]

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Table 14-23298. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4F4h**

Figure 14-7731. EMIF_CTLCFG_DENALI_PHY_317 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							

Table 14-23300. EMIF_CTLCFG_DENALI_PHY_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_1	R	0h	Observation register containing write data leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1119 EMIF_CTLCFG_DENALI_PHY_318 Register

1 EMIF_CTLCFG_DENALI_PHY_318 Register (Offset = 44F8h) [reset = 0h]

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Table 14-23301. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4F8h**

Figure 14-7732. EMIF_CTLCFG_DENALI_PHY_318 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							

Table 14-23303. EMIF_CTLCFG_DENALI_PHY_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_1	R	0h	Observation register containing periodic write data leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1120 EMIF_CTLCFG_DENALI_PHY_319 Register

1 EMIF_CTLCFG_DENALI_PHY_319 Register (Offset = 44FCh) [reset = 0h]

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Table 14-23304. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C4FCh**

Figure 14-7733. EMIF_CTLCFG_DENALI_PHY_319 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_DDL_MODE_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_MODE_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_MODE_1							
R/W							
0h							

Table 14-23306. EMIF_CTLCFG_DENALI_PHY_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_1	R/W	0h	DDL mode for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1121 EMIF_CTLCFG_DENALI_PHY_320 Register

1 EMIF_CTLCFG_DENALI_PHY_320 Register (Offset = 4500h) [reset = 0h]

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Table 14-23307. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C500h**

Figure 14-7734. EMIF_CTLCFG_DENALI_PHY_320 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_MASK_1					
NONE		R/W					
0h		0h					

Table 14-23309. EMIF_CTLCFG_DENALI_PHY_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_1	R/W	0h	DDL mask for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1122 EMIF_CTLCFG_DENALI_PHY_321 Register

1 EMIF_CTLCFG_DENALI_PHY_321 Register (Offset = 4504h) [reset = 0h]

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Table 14-23310. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C504h**

Figure 14-7735. EMIF_CTLCFG_DENALI_PHY_321 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_1							
R							
0h							

Table 14-23312. EMIF_CTLCFG_DENALI_PHY_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_1	R	0h	DDL test observation for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1123 EMIF_CTLCFG_DENALI_PHY_322 Register

1 EMIF_CTLCFG_DENALI_PHY_322 Register (Offset = 4508h) [reset = 0h]

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Table 14-23313. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C508h**

Figure 14-7736. EMIF_CTLCFG_DENALI_PHY_322 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							

Table 14-23315. EMIF_CTLCFG_DENALI_PHY_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_1	R	0h	DDL test observation delays for slice 1 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1124 EMIF_CTLCFG_DENALI_PHY_323 Register

1 EMIF_CTLCFG_DENALI_PHY_323 Register (Offset = 450Ch) [reset = 0h]

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Table 14-23316. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C50Ch**

Figure 14-7737. EMIF_CTLCFG_DENALI_PHY_323 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_1							
R/W							
0h							

Table 14-23318. EMIF_CTLCFG_DENALI_PHY_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_1	R/W	0h	RX Calibration codes for DQ0 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_1	R/W	0h	LPDDR4 write preamble extension enable for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_1	R/W	0h	Specify threshold value for PHY init update tracking for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1125 EMIF_CTLCFG_DENALI_PHY_324 Register

1 EMIF_CTLCFG_DENALI_PHY_324 Register (Offset = 4510h) [reset = 0h]

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Table 14-23319. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 C510h**

Figure 14-7738. EMIF_CTLCFG_DENALI_PHY_324 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ1_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ1_1							
R/W							
0h							

Table 14-23321. EMIF_CTLCFG_DENALI_PHY_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_1	R/W	0h	RX Calibration codes for DQ2 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_1	R/W	0h	RX Calibration codes for DQ1 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1126 EMIF_CTLCFG_DENALI_PHY_325 Register

1 EMIF_CTLCFG_DENALI_PHY_325 Register (Offset = 4514h) [reset = 0h]

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Table 14-23322. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C514h**

Figure 14-7739. EMIF_CTLCFG_DENALI_PHY_325 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_RX_CAL_DQ4_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RX_CAL_DQ4_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_RX_CAL_DQ3_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RX_CAL_DQ3_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23324. EMIF_CTLCFG_DENALI_PHY_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_1	R/W	0h	RX Calibration codes for DQ4 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_1	R/W	0h	RX Calibration codes for DQ3 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1127 EMIF_CTLCFG_DENALI_PHY_326 Register

1 EMIF_CTLCFG_DENALI_PHY_326 Register (Offset = 4518h) [reset = 0h]

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Table 14-23325. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C518h**

Figure 14-7740. EMIF_CTLCFG_DENALI_PHY_326 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ6_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ5_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ5_1							
R/W							
0h							

Table 14-23327. EMIF_CTLCFG_DENALI_PHY_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_1	R/W	0h	RX Calibration codes for DQ6 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_1	R/W	0h	RX Calibration codes for DQ5 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1128 EMIF_CTLCFG_DENALI_PHY_327 Register

1 EMIF_CTLCFG_DENALI_PHY_327 Register (Offset = 451Ch) [reset = 0h]

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Table 14-23328. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C51Ch**

Figure 14-7741. EMIF_CTLCFG_DENALI_PHY_327 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ7_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ7_1							
R/W							
0h							

Table 14-23330. EMIF_CTLCFG_DENALI_PHY_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_1	R/W	0h	RX Calibration codes for DQ7 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1129 EMIF_CTLCFG_DENALI_PHY_328 Register

1 EMIF_CTLCFG_DENALI_PHY_328 Register (Offset = 4520h) [reset = 0h]

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Table 14-23331. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C520h**

Figure 14-7742. EMIF_CTLCFG_DENALI_PHY_328 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RX_CAL_DM_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RX_CAL_DM_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RX_CAL_DM_1							
R/W							
0h							

Table 14-23333. EMIF_CTLCFG_DENALI_PHY_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_1	R/W	0h	RX Calibration codes for DM for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1130 EMIF_CTLCFG_DENALI_PHY_329 Register

1 EMIF_CTLCFG_DENALI_PHY_329 Register (Offset = 4524h) [reset = 0h]

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Table 14-23334. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C524h

Figure 14-7743. EMIF_CTLCFG_DENALI_PHY_329 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_FDBK_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQS_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQS_1							
R/W							
0h							

Table 14-23336. EMIF_CTLCFG_DENALI_PHY_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_1	R/W	0h	RX Calibration codes for FDBK for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_1	R/W	0h	RX Calibration codes for DQS for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1131 EMIF_CTLCFG_DENALI_PHY_330 Register

1 EMIF_CTLCFG_DENALI_PHY_330 Register (Offset = 4528h) [reset = 0h]

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Table 14-23337. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C528h

Figure 14-7744. EMIF_CTLCFG_DENALI_PHY_330 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_CAL_SAMPLE_WAIT_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_STATIC_TOG_DISABLE_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_PAD_RX_BIAS_EN_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_PAD_RX_BIAS_EN_1							
R/W							
0h							

Table 14-23339. EMIF_CTLCFG_DENALI_PHY_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_CAL_SAMPLE_WAIT_1	R/W	0h	Determines number of cycles to wait for each sample for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_1	R/W	0h	Control to disable toggle during static activity for slice 1. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_1	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1132 EMIF_CTLCFG_DENALI_PHY_331 Register

1 EMIF_CTLCFG_DENALI_PHY_331 Register (Offset = 452Ch) [reset = 0h]

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Table 14-23340. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C52Ch**

Figure 14-7745. EMIF_CTLCFG_DENALI_PHY_331 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DATA_DC_ADJUST_SAMPLE_CNT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_DATA_DC_ADJUST_START_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DATA_DC_WEIGHT_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_DC_CAL_TIMEOUT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23342. EMIF_CTLCFG_DENALI_PHY_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_ADJUST_SAMPLE_CNT_1	R/W	0h	Duty cycle adjust sample count for slice 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DATA_DC_ADJUST_START_1	R/W	0h	Duty cycle adjust starting value for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DATA_DC_WEIGHT_1	R/W	0h	Determines weight of average calculating for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_CAL_TIMEOUT_1	R/W	0h	Determines timeout number of iteration for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1133 EMIF_CTLCFG_DENALI_PHY_332 Register

1 EMIF_CTLCFG_DENALI_PHY_332 Register (Offset = 4530h) [reset = 0h]

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Table 14-23343. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C530h**

Figure 14-7746. EMIF_CTLCFG_DENALI_PHY_332 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_CAL_START_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DATA_DC_CAL_POLARITY_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DATA_DC_ADJUST_THRSHLD_1							
R/W							
0h							

Table 14-23345. EMIF_CTLCFG_DENALI_PHY_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_DATA_DC_CAL_START_1	R/W	0h	Manual trigger for DCC for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DATA_DC_CAL_POLARITY_1	R/W	0h	Calibration polarity for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_ADJUST_DIRECT_1	R/W	0h	Adjust direction for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_ADJUST_THRSHLD_1	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1134 EMIF_CTLCFG_DENALI_PHY_333 Register

1 EMIF_CTLCFG_DENALI_PHY_333 Register (Offset = 4534h) [reset = 1h]

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Table 14-23346. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C534h**

Figure 14-7747. EMIF_CTLCFG_DENALI_PHY_333 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDPATH_GATE_DISABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_FDBK_PWR_CTRL_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DATA_DC_SW_RANK_1	
NONE						R/W	
0h						1h	

Table 14-23348. EMIF_CTLCFG_DENALI_PHY_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDPATH_GATE_DISABLE_1	R/W	0h	Data slice read path power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SLV_DLY_CTRL_GATE_DISABLE_1	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_FDBK_PWR_CTRL_1	R/W	0h	Shutoff gate feedback IO to reduce power for slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DATA_DC_SW_RANK_1	R/W	1h	Rank selection for software based duty cycle correction for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1135 EMIF_CTLCFG_DENALI_PHY_334 Register

1 EMIF_CTLCFG_DENALI_PHY_334 Register (Offset = 4538h) [reset = 0h]

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Table 14-23349. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C538h**

Figure 14-7748. EMIF_CTLCFG_DENALI_PHY_334 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h

Table 14-23351. EMIF_CTLCFG_DENALI_PHY_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_SLICE_PWR_RDC_DISABLE_1	R/W	0h	Data slice power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1136 EMIF_CTLCFG_DENALI_PHY_335 Register

1 EMIF_CTLCFG_DENALI_PHY_335 Register (Offset = 453Ch) [reset = 0h]

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Table 14-23352. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C53Ch

Figure 14-7749. EMIF_CTLCFG_DENALI_PHY_335 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_SELECT_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_SELECT_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DQ_TSEL_ENABLE_1		
NONE					R/W		
0h					0h		

Table 14-23354. EMIF_CTLCFG_DENALI_PHY_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQS signals for slice 1. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 1. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1137 EMIF_CTLCFG_DENALI_PHY_336 Register

1 EMIF_CTLCFG_DENALI_PHY_336 Register (Offset = 4540h) [reset = 0h]

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Table 14-23355. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C540h**

Figure 14-7750. EMIF_CTLCFG_DENALI_PHY_336 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_1							
R/W							
0h							

Table 14-23357. EMIF_CTLCFG_DENALI_PHY_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_1	R/W	0h	Data slice initial VREF training start value for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_1	R/W	0h	2 cycle preamble support for slice 1. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQS signals for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1138 EMIF_CTLCFG_DENALI_PHY_337 Register

1 EMIF_CTLCFG_DENALI_PHY_337 Register (Offset = 4544h) [reset = 0h]

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Table 14-23358. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C544h**

Figure 14-7751. EMIF_CTLCFG_DENALI_PHY_337 Name Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_1						
NONE	R/W						
0h	0h						

Table 14-23360. EMIF_CTLCFG_DENALI_PHY_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_1	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_1	R/W	0h	Enable for No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_1	R/W	0h	Data slice vref training enable control for slice 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_1	R/W	0h	Data slice initial VREF training stop value for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1139 EMIF_CTLCFG_DENALI_PHY_338 Register

1 EMIF_CTLCFG_DENALI_PHY_338 Register (Offset = 4548h) [reset = 0h]

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Table 14-23361. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C548h**

Figure 14-7752. EMIF_CTLCFG_DENALI_PHY_338 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_NTP_WDQ_STOP_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_NTP_WDQ_START_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_START_1							
R/W							
0h							

Table 14-23363. EMIF_CTLCFG_DENALI_PHY_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_1	R/W	0h	End of WR DQ target delay in No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_1	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1140 EMIF_CTLCFG_DENALI_PHY_339 Register

1 EMIF_CTLCFG_DENALI_PHY_339 Register (Offset = 454Ch) [reset = 0h]

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Table 14-23364. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C54Ch

Figure 14-7753. EMIF_CTLCFG_DENALI_PHY_339 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_1							
R/W							
0h							

Table 14-23366. EMIF_CTLCFG_DENALI_PHY_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_1	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_1	R/W	0h	Minimum data valid window across DQs and ranks for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_1	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1141 EMIF_CTLCFG_DENALI_PHY_340 Register

1 EMIF_CTLCFG_DENALI_PHY_340 Register (Offset = 4550h) [reset = 0h]

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Table 14-23367. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C550h**

Figure 14-7754. EMIF_CTLCFG_DENALI_PHY_340 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_TX_DCD_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_1					
NONE		R/W					
0h		0h					

Table 14-23369. EMIF_CTLCFG_DENALI_PHY_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_1	R/W	0h	Controls TX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_1	R/W	0h	Enable for fast multi-pattern window search for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_1	R/W	0h	Peridic training start point offset for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1142 EMIF_CTLCFG_DENALI_PHY_341 Register

1 EMIF_CTLCFG_DENALI_PHY_341 Register (Offset = 4554h) [reset = 0h]

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Table 14-23370. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C554h**

Figure 14-7755. EMIF_CTLCFG_DENALI_PHY_341 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_3_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_2_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_1_1				
NONE			R/W				
0h			0h				

Table 14-23372. EMIF_CTLCFG_DENALI_PHY_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1143 EMIF_CTLCFG_DENALI_PHY_342 Register

1 EMIF_CTLCFG_DENALI_PHY_342 Register (Offset = 4558h) [reset = 0h]

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Table 14-23373. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C558h**

Figure 14-7756. EMIF_CTLCFG_DENALI_PHY_342 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_7_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_6_1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_5_1				
NONE			R/W				
0h			0h				

Table 14-23375. EMIF_CTLCFG_DENALI_PHY_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dm pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1144 EMIF_CTLCFG_DENALI_PHY_343 Register

1 EMIF_CTLCFG_DENALI_PHY_343 Register (Offset = 455Ch) [reset = 0h]

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Table 14-23376. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C55Ch**

Figure 14-7757. EMIF_CTLCFG_DENALI_PHY_343 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_PAD_DSLICE_IO_CFG_1						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_1				
NONE			R/W				
0h			0h				

Table 14-23378. EMIF_CTLCFG_DENALI_PHY_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_1	R/W	0h	Controls PCLK/PARK pin for pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_1	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dqs pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1145 EMIF_CTLCFG_DENALI_PHY_344 Register

1 EMIF_CTLCFG_DENALI_PHY_344 Register (Offset = 4560h) [reset = 0h]

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Table 14-23379. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 C560h**

Figure 14-7758. EMIF_CTLCFG_DENALI_PHY_344 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ1_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ0_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23381. EMIF_CTLCFG_DENALI_PHY_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_1	R/W	0h	Read DQ1 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_1	R/W	0h	Read DQ0 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1146 EMIF_CTLCFG_DENALI_PHY_345 Register

1 EMIF_CTLCFG_DENALI_PHY_345 Register (Offset = 4564h) [reset = 0h]

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Table 14-23382. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C564h**

Figure 14-7759. EMIF_CTLCFG_DENALI_PHY_345 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ3_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ2_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23384. EMIF_CTLCFG_DENALI_PHY_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_1	R/W	0h	Read DQ3 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_1	R/W	0h	Read DQ2 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1147 EMIF_CTLCFG_DENALI_PHY_346 Register

1 EMIF_CTLCFG_DENALI_PHY_346 Register (Offset = 4568h) [reset = 0h]

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Table 14-23385. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C568h**

Figure 14-7760. EMIF_CTLCFG_DENALI_PHY_346 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ5_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ4_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ4_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23387. EMIF_CTLCFG_DENALI_PHY_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_1	R/W	0h	Read DQ5 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_1	R/W	0h	Read DQ4 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1148 EMIF_CTLCFG_DENALI_PHY_347 Register

1 EMIF_CTLCFG_DENALI_PHY_347 Register (Offset = 456Ch) [reset = 0h]

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Table 14-23388. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C56Ch**

Figure 14-7761. EMIF_CTLCFG_DENALI_PHY_347 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDDQ7_SLAVE_DELAY_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RDDQ7_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RDDQ6_SLAVE_DELAY_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RDDQ6_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23390. EMIF_CTLCFG_DENALI_PHY_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_1	R/W	0h	Read DQ7 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_1	R/W	0h	Read DQ6 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1149 EMIF_CTLCFG_DENALI_PHY_348 Register

1 EMIF_CTLCFG_DENALI_PHY_348 Register (Offset = 4570h) [reset = 0h]

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Table 14-23391. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C570h**

Figure 14-7762. EMIF_CTLCFG_DENALI_PHY_348 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED					PHY_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23393. EMIF_CTLCFG_DENALI_PHY_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_1	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 1. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_1	R/W	0h	RX_PCLK clock frequency selection for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_1	R/W	0h	Read DM/DBI target delay setting for slice 1. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1150 EMIF_CTLCFG_DENALI_PHY_349 Register

1 EMIF_CTLCFG_DENALI_PHY_349 Register (Offset = 4574h) [reset = 0h]

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Table 14-23394. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C574h**

Figure 14-7763. EMIF_CTLCFG_DENALI_PHY_349 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_1		
NONE					R/W		
0h					0h		

Table 14-23396. EMIF_CTLCFG_DENALI_PHY_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DATA_DC_CAL_CLK_SEL_1	R/W	0h	Determines DCC CAL clock for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1151 EMIF_CTLCFG_DENALI_PHY_350 Register

1 EMIF_CTLCFG_DENALI_PHY_350 Register (Offset = 4578h) [reset = 0h]

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Table 14-23397. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C578h

Figure 14-7764. EMIF_CTLCFG_DENALI_PHY_350 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_OE_TIMING_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_WR_TIMING_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_RD_TIMING_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_OE_TIMING_1							
R/W							
0h							

Table 14-23399. EMIF_CTLCFG_DENALI_PHY_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_1	R/W	0h	Start/end timing values for DQS output enable signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1152 EMIF_CTLCFG_DENALI_PHY_351 Register

1 EMIF_CTLCFG_DENALI_PHY_351 Register (Offset = 457Ch) [reset = 0h]

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Table 14-23400. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C57Ch**

Figure 14-7765. EMIF_CTLCFG_DENALI_PHY_351 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_WR_TIMING_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DQS_OE_RD_TIMING_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_RD_TIMING_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_IO_PAD_DELAY_TIMING_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-23402. EMIF_CTLCFG_DENALI_PHY_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based OE extension for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1153 EMIF_CTLCFG_DENALI_PHY_352 Register

1 EMIF_CTLCFG_DENALI_PHY_352 Register (Offset = 4580h) [reset = 0h]

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Table 14-23403. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C580h**

Figure 14-7766. EMIF_CTLCFG_DENALI_PHY_352 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PHY_PAD_VREF_CTRL_DQ_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_VREF_SETTING_TIME_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_1							
R/W							
0h							

Table 14-23405. EMIF_CTLCFG_DENALI_PHY_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_1	R/W	0h	Pad VREF control settings for DQ slice 1. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_1	R/W	0h	Number of cycles for vref settle after setting is changed for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1154 EMIF_CTLCFG_DENALI_PHY_353 Register

1 EMIF_CTLCFG_DENALI_PHY_353 Register (Offset = 4584h) [reset = 0h]

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Table 14-23406. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C584h

Figure 14-7767. EMIF_CTLCFG_DENALI_PHY_353 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQS_IE_TIMING_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_IE_TIMING_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_PER_CS_TRAINING_EN_1
NONE							R/W
0h							0h

Table 14-23408. EMIF_CTLCFG_DENALI_PHY_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_RDDATA_EN_IE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_IE_TIMING_1	R/W	0h	Start/end timing values for DQS input enable signals for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_IE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_EN_1	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 1. Must have same value in all slices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1155 EMIF_CTLCFG_DENALI_PHY_354 Register

1 EMIF_CTLCFG_DENALI_PHY_354 Register (Offset = 4588h) [reset = 0h]

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Table 14-23409. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C588h**

Figure 14-7768. EMIF_CTLCFG_DENALI_PHY_354 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							PHY_WDQLVL_IE_ON_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_DBI_MODE_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PHY_IE_MODE_1	
NONE						R/W	
0h						0h	

Table 14-23411. EMIF_CTLCFG_DENALI_PHY_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_DLY_1	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_WDQLVL_IE_ON_1	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DBI_MODE_1	R/W	0h	DBI mode for slice 1. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_IE_MODE_1	R/W	0h	Input enable mode bits for slice 1. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1156 EMIF_CTLCFG_DENALI_PHY_355 Register

1 EMIF_CTLCFG_DENALI_PHY_355 Register (Offset = 458Ch) [reset = 0h]

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Table 14-23412. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C58Ch

Figure 14-7769. EMIF_CTLCFG_DENALI_PHY_355 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_MASTER_MODE_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_RDDATA_EN_OE_DLY_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_RDDATA_EN_TSEL_DLY_1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_1				
NONE			R/W				
0h			0h				

Table 14-23414. EMIF_CTLCFG_DENALI_PHY_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_MASTER_MODE_1	R/W	0h	Controller delay line override settings for slice 1. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_OE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_TSEL_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_1	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1157 EMIF_CTLCFG_DENALI_PHY_356 Register

1 EMIF_CTLCFG_DENALI_PHY_356 Register (Offset = 4590h) [reset = 0h]

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Table 14-23415. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 C590h**

Figure 14-7770. EMIF_CTLCFG_DENALI_PHY_356 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_WAIT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_MASTER_DELAY_STEP_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_MASTER_DELAY_START_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_START_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23417. EMIF_CTLCFG_DENALI_PHY_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_1	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 1. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_1	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_1	R/W	0h	Start value for controller delay line locking algorithm for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1158 EMIF_CTLCFG_DENALI_PHY_357 Register

1 EMIF_CTLCFG_DENALI_PHY_357 Register (Offset = 4594h) [reset = 0h]

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Table 14-23418. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C594h**

Figure 14-7771. EMIF_CTLCFG_DENALI_PHY_357 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DLY_STEP_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RPTR_UPDATE_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_HALF_MEASURE_1							
R/W							
0h							

Table 14-23420. EMIF_CTLCFG_DENALI_PHY_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_1	R/W	0h	DQS target delay fine step size during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_1	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_1	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1159 EMIF_CTLCFG_DENALI_PHY_358 Register

1 EMIF_CTLCFG_DENALI_PHY_358 Register (Offset = 4598h) [reset = 0h]

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Table 14-23421. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C598h**

Figure 14-7772. EMIF_CTLCFG_DENALI_PHY_358 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_GTLVL_RESP_WAIT_CNT_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_GTLVL_DLY_STEP_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_WRLVL_RESP_WAIT_CNT_1					
NONE		R/W					
0h		0h					

Table 14-23423. EMIF_CTLCFG_DENALI_PHY_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 1. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1160 EMIF_CTLCFG_DENALI_PHY_359 Register

1 EMIF_CTLCFG_DENALI_PHY_359 Register (Offset = 459Ch) [reset = 0h]

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Table 14-23424. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C59Ch**

Figure 14-7773. EMIF_CTLCFG_DENALI_PHY_359 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GTLVL_FINAL_STEP_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_GTLVL_FINAL_STEP_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_BACK_STEP_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_BACK_STEP_1							
R/W							
0h							

Table 14-23426. EMIF_CTLCFG_DENALI_PHY_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_1	R/W	0h	Final backup step delay used in gate training algorithm for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_1	R/W	0h	Interim backup step delay used in gate training algorithm for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1161 EMIF_CTLCFG_DENALI_PHY_360 Register

1 EMIF_CTLCFG_DENALI_PHY_360 Register (Offset = 45A0h) [reset = 0h]

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Table 14-23427. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5A0h**

Figure 14-7774. EMIF_CTLCFG_DENALI_PHY_360 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_WDQLVL_DM_SEARCH_RANGE_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_WDQLVL_DM_SEARCH_RANGE_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_1							
R/W							
0h							

Table 14-23429. EMIF_CTLCFG_DENALI_PHY_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_1	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_1	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 1. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_1	R/W	0h	DQ target delay step size during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1162 EMIF_CTLCFG_DENALI_PHY_361 Register

1 EMIF_CTLCFG_DENALI_PHY_361 Register (Offset = 45A4h) [reset = 0h]

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Table 14-23430. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5A4h**

Figure 14-7775. EMIF_CTLCFG_DENALI_PHY_361 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RDLVL_DLY_STEP_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_TOGGLE_PRE_SUPPORT_1
NONE							R/W
0h							0h

Table 14-23432. EMIF_CTLCFG_DENALI_PHY_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_1	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1163 EMIF_CTLCFG_DENALI_PHY_362 Register

1 EMIF_CTLCFG_DENALI_PHY_362 Register (Offset = 45A8h) [reset = 0h]

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Table 14-23433. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5A8h**

Figure 14-7776. EMIF_CTLCFG_DENALI_PHY_362 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_MAX_EDGE_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_MAX_EDGE_1							
R/W							
0h							

Table 14-23435. EMIF_CTLCFG_DENALI_PHY_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_1	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1164 EMIF_CTLCFG_DENALI_PHY_363 Register

1 EMIF_CTLCFG_DENALI_PHY_363 Register (Offset = 45ACh) [reset = 30000h]

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Table 14-23436. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C5ACh

Figure 14-7777. EMIF_CTLCFG_DENALI_PHY_363 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_1	
NONE						R/W	
0h						3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_1	
NONE						R/W	
0h						0h	

Table 14-23438. EMIF_CTLCFG_DENALI_PHY_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DATA_DC_INIT_DISABLE_1	R/W	3h	Disable duty cycle adjust at initialization for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_1	R/W	0h	Write path clock gating timing for slice 1. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_1	R/W	0h	Write path clock gating disable for slice 1. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.6.6.2.1165 EMIF_CTLCFG_DENALI_PHY_364 Register

1 EMIF_CTLCFG_DENALI_PHY_364 Register (Offset = 45B0h) [reset = 0h]

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Table 14-23439. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5B0h**

Figure 14-7778. EMIF_CTLCFG_DENALI_PHY_364 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ_INIT_SLV_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY_1							
R/W							
0h							

Table 14-23441. EMIF_CTLCFG_DENALI_PHY_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_1	R/W	0h	Initial value of write DQ target delay for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_1	R/W	0h	Initial value of write DQS target delay for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1166 EMIF_CTLCFG_DENALI_PHY_365 Register

1 EMIF_CTLCFG_DENALI_PHY_365 Register (Offset = 45B4h) [reset = 0h]

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Table 14-23442. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5B4h**

Figure 14-7779. EMIF_CTLCFG_DENALI_PHY_365 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DM_CLK_SE_THRSHLD_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_1
NONE							R/W
0h							0h

Table 14-23444. EMIF_CTLCFG_DENALI_PHY_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_1	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_1	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_WDQLVL_ENABLE_1	R/W	0h	Enable duty cycle adjust during write DQ training for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DATA_DC_WRLVL_ENABLE_1	R/W	0h	Enable duty cycle adjust during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1167 EMIF_CTLCFG_DENALI_PHY_366 Register

1 EMIF_CTLCFG_DENALI_PHY_366 Register (Offset = 45B8h) [reset = 0h]

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Table 14-23445. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5B8h**

Figure 14-7780. EMIF_CTLCFG_DENALI_PHY_366 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_RDDATA_EN_DLY_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED	PHY_MEAS_DLY_STEP_ENABLE_1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_WDQ_OSC_DELTA_1						
NONE	R/W						
0h	0h						

Table 14-23447. EMIF_CTLCFG_DENALI_PHY_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_MEAS_DLY_STEP_ENABLE_1	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_WDQ_OSC_DELTA_1	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1168 EMIF_CTLCFG_DENALI_PHY_367 Register

1 EMIF_CTLCFG_DENALI_PHY_367 Register (Offset = 45BCh) [reset = 0h]

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Table 14-23448. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C5BCh

Figure 14-7781. EMIF_CTLCFG_DENALI_PHY_367 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							

Table 14-23450. EMIF_CTLCFG_DENALI_PHY_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_1	R/W	0h	DQ/DM bit swizzling 0 for slice 1. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1169 EMIF_CTLCFG_DENALI_PHY_368 Register

1 EMIF_CTLCFG_DENALI_PHY_368 Register (Offset = 45C0h) [reset = 0h]

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Table 14-23451. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5C0h**

Figure 14-7782. EMIF_CTLCFG_DENALI_PHY_368 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_1			
NONE				R/W			
0h				0h			

Table 14-23453. EMIF_CTLCFG_DENALI_PHY_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_1	R/W	0h	DQ/DM bit swizzling 1 for slice 1. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1170 EMIF_CTLCFG_DENALI_PHY_369 Register

1 EMIF_CTLCFG_DENALI_PHY_369 Register (Offset = 45C4h) [reset = 0h]

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Table 14-23454. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5C4h**

Figure 14-7783. EMIF_CTLCFG_DENALI_PHY_369 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ1_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23456. EMIF_CTLCFG_DENALI_PHY_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1171 EMIF_CTLCFG_DENALI_PHY_370 Register

1 EMIF_CTLCFG_DENALI_PHY_370 Register (Offset = 45C8h) [reset = 0h]

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Table 14-23457. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5C8h**

Figure 14-7784. EMIF_CTLCFG_DENALI_PHY_370 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ3_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23459. EMIF_CTLCFG_DENALI_PHY_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1172 EMIF_CTLCFG_DENALI_PHY_371 Register

1 EMIF_CTLCFG_DENALI_PHY_371 Register (Offset = 45CCh) [reset = 0h]

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Table 14-23460. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5CCh**

Figure 14-7785. EMIF_CTLCFG_DENALI_PHY_371 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ5_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ4_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23462. EMIF_CTLCFG_DENALI_PHY_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1173 EMIF_CTLCFG_DENALI_PHY_372 Register

1 EMIF_CTLCFG_DENALI_PHY_372 Register (Offset = 45D0h) [reset = 0h]

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Table 14-23463. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5D0h**

Figure 14-7786. EMIF_CTLCFG_DENALI_PHY_372 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ7_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ6_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23465. EMIF_CTLCFG_DENALI_PHY_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1174 EMIF_CTLCFG_DENALI_PHY_373 Register

1 EMIF_CTLCFG_DENALI_PHY_373 Register (Offset = 45D4h) [reset = 0h]

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Table 14-23466. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5D4h**

Figure 14-7787. EMIF_CTLCFG_DENALI_PHY_373 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_CLK_WRDQS_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDM_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23468. EMIF_CTLCFG_DENALI_PHY_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQS for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1175 EMIF_CTLCFG_DENALI_PHY_374 Register

1 EMIF_CTLCFG_DENALI_PHY_374 Register (Offset = 45D8h) [reset = 0h]

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Table 14-23469. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5D8h**

Figure 14-7788. EMIF_CTLCFG_DENALI_PHY_374 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_1	
NONE						R/W	
0h						0h	

Table 14-23471. EMIF_CTLCFG_DENALI_PHY_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_1	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1176 EMIF_CTLCFG_DENALI_PHY_375 Register

1 EMIF_CTLCFG_DENALI_PHY_375 Register (Offset = 45DCh) [reset = 0h]

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Table 14-23472. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5DCh**

Figure 14-7789. EMIF_CTLCFG_DENALI_PHY_375 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23474. EMIF_CTLCFG_DENALI_PHY_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1177 EMIF_CTLCFG_DENALI_PHY_376 Register

1 EMIF_CTLCFG_DENALI_PHY_376 Register (Offset = 45E0h) [reset = 0h]

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Table 14-23475. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C5E0h

Figure 14-7790. EMIF_CTLCFG_DENALI_PHY_376 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23477. EMIF_CTLCFG_DENALI_PHY_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1178 EMIF_CTLCFG_DENALI_PHY_377 Register

1 EMIF_CTLCFG_DENALI_PHY_377 Register (Offset = 45E4h) [reset = 0h]

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Table 14-23478. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5E4h**

Figure 14-7791. EMIF_CTLCFG_DENALI_PHY_377 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23480. EMIF_CTLCFG_DENALI_PHY_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1179 EMIF_CTLCFG_DENALI_PHY_378 Register

1 EMIF_CTLCFG_DENALI_PHY_378 Register (Offset = 45E8h) [reset = 0h]

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Table 14-23481. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5E8h**

Figure 14-7792. EMIF_CTLCFG_DENALI_PHY_378 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23483. EMIF_CTLCFG_DENALI_PHY_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1180 EMIF_CTLCFG_DENALI_PHY_379 Register

1 EMIF_CTLCFG_DENALI_PHY_379 Register (Offset = 45ECh) [reset = 0h]

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Table 14-23484. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5ECh**

Figure 14-7793. EMIF_CTLCFG_DENALI_PHY_379 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23486. EMIF_CTLCFG_DENALI_PHY_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1181 EMIF_CTLCFG_DENALI_PHY_380 Register

1 EMIF_CTLCFG_DENALI_PHY_380 Register (Offset = 45F0h) [reset = 0h]

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Table 14-23487. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5F0h**

Figure 14-7794. EMIF_CTLCFG_DENALI_PHY_380 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23489. EMIF_CTLCFG_DENALI_PHY_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1182 EMIF_CTLCFG_DENALI_PHY_381 Register

1 EMIF_CTLCFG_DENALI_PHY_381 Register (Offset = 45F4h) [reset = 0h]

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Table 14-23490. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5F4h**

Figure 14-7795. EMIF_CTLCFG_DENALI_PHY_381 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23492. EMIF_CTLCFG_DENALI_PHY_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1183 EMIF_CTLCFG_DENALI_PHY_382 Register

1 EMIF_CTLCFG_DENALI_PHY_382 Register (Offset = 45F8h) [reset = 0h]

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Table 14-23493. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5F8h**

Figure 14-7796. EMIF_CTLCFG_DENALI_PHY_382 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DM_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-23495. EMIF_CTLCFG_DENALI_PHY_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1184 EMIF_CTLCFG_DENALI_PHY_383 Register

1 EMIF_CTLCFG_DENALI_PHY_383 Register (Offset = 45FCh) [reset = 0h]

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Table 14-23496. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C5FCh**

Figure 14-7797. EMIF_CTLCFG_DENALI_PHY_383 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_GATE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_GATE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DM_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DM_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23498. EMIF_CTLCFG_DENALI_PHY_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_1	R/W	0h	Read DQS target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1185 EMIF_CTLCFG_DENALI_PHY_384 Register

1 EMIF_CTLCFG_DENALI_PHY_384 Register (Offset = 4600h) [reset = 0h]

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Table 14-23499. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C600h**

Figure 14-7798. EMIF_CTLCFG_DENALI_PHY_384 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_WRLVL_DELAY_EARLY_THRESHOLD_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_WRLVL_DELAY_EARLY_THRESHOLD_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WRITE_PATH_LAT_ADD_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_RDDQS_LATENCY_ADJUST_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-23501. EMIF_CTLCFG_DENALI_PHY_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_1	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_1	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1186 EMIF_CTLCFG_DENALI_PHY_385 Register

1 EMIF_CTLCFG_DENALI_PHY_385 Register (Offset = 4604h) [reset = 0h]

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Table 14-23502. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C604h**

Figure 14-7799. EMIF_CTLCFG_DENALI_PHY_385 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_EARLY_FORCE_ZERO_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1							
R/W							
0h							

Table 14-23504. EMIF_CTLCFG_DENALI_PHY_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_1	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1187 EMIF_CTLCFG_DENALI_PHY_386 Register

1 EMIF_CTLCFG_DENALI_PHY_386 Register (Offset = 4608h) [reset = 0h]

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Table 14-23505. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C608h**

Figure 14-7800. EMIF_CTLCFG_DENALI_PHY_386 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_1							
R/W							
0h							

Table 14-23507. EMIF_CTLCFG_DENALI_PHY_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_1	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_1	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1188 EMIF_CTLCFG_DENALI_PHY_387 Register

1 EMIF_CTLCFG_DENALI_PHY_387 Register (Offset = 460Ch) [reset = 0h]

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Table 14-23508. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C60Ch

Figure 14-7801. EMIF_CTLCFG_DENALI_PHY_387 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PASS_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_1							
R/W							
0h							

Table 14-23510. EMIF_CTLCFG_DENALI_PHY_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_1	R/W	0h	Indicates if No-topology training found a passing result for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_1	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_1	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1189 EMIF_CTLCFG_DENALI_PHY_388 Register

1 EMIF_CTLCFG_DENALI_PHY_388 Register (Offset = 4610h) [reset = 0h]

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Table 14-23511. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C610h**

Figure 14-7802. EMIF_CTLCFG_DENALI_PHY_388 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1							
R/W							
0h							

Table 14-23513. EMIF_CTLCFG_DENALI_PHY_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1190 EMIF_CTLCFG_DENALI_PHY_389 Register

1 EMIF_CTLCFG_DENALI_PHY_389 Register (Offset = 4614h) [reset = 20202020h]

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Table 14-23514. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C614h**

Figure 14-7803. EMIF_CTLCFG_DENALI_PHY_389 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_1							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ1_CLK_ADJUST_1							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DATA_DC_DQ0_CLK_ADJUST_1							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQS_CLK_ADJUST_1							
R/W							
20h							

Table 14-23516. EMIF_CTLCFG_DENALI_PHY_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ2_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ1_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ0_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQS_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1191 EMIF_CTLCFG_DENALI_PHY_390 Register

1 EMIF_CTLCFG_DENALI_PHY_390 Register (Offset = 4618h) [reset = 20202020h]

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Table 14-23517. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C618h**

Figure 14-7804. EMIF_CTLCFG_DENALI_PHY_390 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_1							
R/W							
20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ5_CLK_ADJUST_1							
R/W							
20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ4_CLK_ADJUST_1							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ3_CLK_ADJUST_1							
R/W							
20h							

Table 14-23519. EMIF_CTLCFG_DENALI_PHY_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ6_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ5_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ4_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ3_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1192 EMIF_CTLCFG_DENALI_PHY_391 Register

1 EMIF_CTLCFG_DENALI_PHY_391 Register (Offset = 461Ch) [reset = 2020h]

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Table 14-23520. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C61Ch**

Figure 14-7805. EMIF_CTLCFG_DENALI_PHY_391 Name Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_1							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_1							
R/W							
20h							

Table 14-23522. EMIF_CTLCFG_DENALI_PHY_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_DSLICE_PAD_BOOSTPN_SETTING_1	R/W	0h	Setting for boost P/N of pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DM_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ7_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1193 EMIF_CTLCFG_DENALI_PHY_392 Register

1 EMIF_CTLCFG_DENALI_PHY_392 Register (Offset = 4620h) [reset = 0h]

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Table 14-23523. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 C620h**

Figure 14-7806. EMIF_CTLCFG_DENALI_PHY_392 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DQS_FFE_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DQ_FFE_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_DSLICE_PAD_RX_CTLE_SETTING_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-23525. EMIF_CTLCFG_DENALI_PHY_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DQS_FFE_1	R/W	0h	TX_FFE setting for DQS pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DQ_FFE_1	R/W	0h	TX_FFE setting for DQ/DM pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DSLICE_PAD_RX_CTLE_SETTING_1	R/W	0h	Setting for RX ctle P/N of pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1194 EMIF_CTLCFG_DENALI_PHY_512 Register

1 EMIF_CTLCFG_DENALI_PHY_512 Register (Offset = 4800h) [reset = 0h]

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Table 14-23526. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C800h**

Figure 14-7807. EMIF_CTLCFG_DENALI_PHY_512 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WR_BYPASS_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_2						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_2		
NONE					R/W		
0h					0h		

Table 14-23528. EMIF_CTLCFG_DENALI_PHY_512 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_2	R/W	0h	Write data clock bypass mode target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_2	R/W	0h	Controls PCLK/PARK pin for pad for slice 2 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_2	R/W	0h	RX_PCLK boot clock frequency selection for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1195 EMIF_CTLCFG_DENALI_PHY_513 Register

1 EMIF_CTLCFG_DENALI_PHY_513 Register (Offset = 4804h) [reset = 0h]

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Table 14-23529. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C804h

Figure 14-7808. EMIF_CTLCFG_DENALI_PHY_513 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_2			
NONE				R/W			
0h				0h			

Table 14-23531. EMIF_CTLCFG_DENALI_PHY_513 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_2	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2	R/W	0h	Write DQS bypass mode target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_2	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1196 EMIF_CTLCFG_DENALI_PHY_514 Register

1 EMIF_CTLCFG_DENALI_PHY_514 Register (Offset = 4808h) [reset = 0h]

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Table 14-23532. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C808h**

Figure 14-7809. EMIF_CTLCFG_DENALI_PHY_514 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_2
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_2	
NONE						R/W	
0h						0h	

15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23534. EMIF_CTLCFG_DENALI_PHY_514 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_2	R/W	0h	Bypass mode override setting for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_2	R/W	0h	Two_cycle_preamble for bypass mode for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2	R/W	0h	Read DQS bypass mode target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1197 EMIF_CTLCFG_DENALI_PHY_515 Register

1 EMIF_CTLCFG_DENALI_PHY_515 Register (Offset = 480Ch) [reset = 0h]

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Table 14-23535. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C80Ch

Figure 14-7810. EMIF_CTLCFG_DENALI_PHY_515 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_2					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_2					
NONE		R/W					
0h		0h					

Table 14-23537. EMIF_CTLCFG_DENALI_PHY_515 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23537. EMIF_CTLCFG_DENALI_PHY_515 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1198 EMIF_CTLCFG_DENALI_PHY_516 Register

1 EMIF_CTLCFG_DENALI_PHY_516 Register (Offset = 4810h) [reset = 0h]

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Table 14-23538. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C810h**

Figure 14-7811. EMIF_CTLCFG_DENALI_PHY_516 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_2					
NONE		R/W					
0h		0h					

Table 14-23540. EMIF_CTLCFG_DENALI_PHY_516 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23540. EMIF_CTLCFG_DENALI_PHY_516 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1199 EMIF_CTLCFG_DENALI_PHY_517 Register

1 EMIF_CTLCFG_DENALI_PHY_517 Register (Offset = 4814h) [reset = 1000000h]

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Table 14-23541. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C814h**

Figure 14-7812. EMIF_CTLCFG_DENALI_PHY_517 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_2
NONE							R/W
0h							1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PER_RANK_CS_MAP_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_SW_WRDQS_SHIFT_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDM_SHIFT_2					
NONE		R/W					
0h		0h					

Table 14-23543. EMIF_CTLCFG_DENALI_PHY_517 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_PER_CS_TRAINING_MULTICAST_EN_2	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_PER_RANK_CS_MAP_2	R/W	0h	Per-rank CS map for slice 2. Setting a bit uses that CS for the rank, bit [0] uses CS0, bit [1] uses CS1, etc. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23543. EMIF_CTLCFG_DENALI_PHY_517 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1200 EMIF_CTLCFG_DENALI_PHY_518 Register

1 EMIF_CTLCFG_DENALI_PHY_518 Register (Offset = 4818h) [reset = 0h]

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Table 14-23544. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C818h**

Figure 14-7813. EMIF_CTLCFG_DENALI_PHY_518 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_LP4_BOOT_RDDATA_EN_DLY_2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_LP4_BOOT_RDDATA_EN_IE_DLY_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PER_CS_TRAINING_INDEX_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-23546. EMIF_CTLCFG_DENALI_PHY_518 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_LP4_BOOT_RDDATA_EN_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_INDEX_2	R/W	0h	For per-rank training, indicates which rank's paramters are read/ written for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1201 EMIF_CTLCFG_DENALI_PHY_519 Register

1 EMIF_CTLCFG_DENALI_PHY_519 Register (Offset = 481Ch) [reset = 0h]

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Table 14-23547. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C81Ch

Figure 14-7814. EMIF_CTLCFG_DENALI_PHY_519 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_2			
NONE				R/W			
0h				0h			

Table 14-23549. EMIF_CTLCFG_DENALI_PHY_519 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_2	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 2. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_LP4_BOOT_RPTR_UPDATE_2	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1202 EMIF_CTLCFG_DENALI_PHY_520 Register

1 EMIF_CTLCFG_DENALI_PHY_520 Register (Offset = 4820h) [reset = 0h]

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Table 14-23550. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C820h**

Figure 14-7815. EMIF_CTLCFG_DENALI_PHY_520 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_2	
NONE						R/W	
0h						0h	

Table 14-23552. EMIF_CTLCFG_DENALI_PHY_520 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LPBK_DFX_TIMEOUT_EN_2	R/W	0h	Loopback read only test timeout mechanism enable for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_LPBK_CONTROL_2	R/W	0h	Loopback control bits for slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CTRL_LPBK_EN_2	R/W	0h	Loopback control en for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1203 EMIF_CTLCFG_DENALI_PHY_521 Register

1 EMIF_CTLCFG_DENALI_PHY_521 Register (Offset = 4824h) [reset = 0h]

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Table 14-23553. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C824h**

Figure 14-7816. EMIF_CTLCFG_DENALI_PHY_521 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_GATE_DELAY_COMP_DISABLE_2
NONE							R/W
0h							0h

Table 14-23555. EMIF_CTLCFG_DENALI_PHY_521 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_GATE_DELAY_COMP_DISABLE_2	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1204 EMIF_CTLCFG_DENALI_PHY_522 Register

1 EMIF_CTLCFG_DENALI_PHY_522 Register (Offset = 4828h) [reset = 0h]

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Table 14-23556. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C828h**

Figure 14-7817. EMIF_CTLCFG_DENALI_PHY_522 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_CONTROL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_CONTROL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_CONTROL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_CONTROL_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23558. EMIF_CTLCFG_DENALI_PHY_522 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_2	R/W	0h	Auto timing marging control bits for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1205 EMIF_CTLCFG_DENALI_PHY_523 Register

1 EMIF_CTLCFG_DENALI_PHY_523 Register (Offset = 482Ch) [reset = 0h]

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Table 14-23559. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C82Ch

Figure 14-7818. EMIF_CTLCFG_DENALI_PHY_523 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_AUTO_TIMING_MARGIN_OBS_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_OBS_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_OBS_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_AUTO_TIMING_MARGIN_OBS_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23561. EMIF_CTLCFG_DENALI_PHY_523 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_2	R	0h	Observation register for the auto_timing_margin for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1206 EMIF_CTLCFG_DENALI_PHY_524 Register

1 EMIF_CTLCFG_DENALI_PHY_524 Register (Offset = 4830h) [reset = 1000000h]

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Table 14-23562. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C830h**

Figure 14-7819. EMIF_CTLCFG_DENALI_PHY_524 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_2						
NONE	R/W						
0h	1h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PDA_MODE_EN_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DQ_IDLE_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_IDLE_2							
R/W							
0h							

Table 14-23564. EMIF_CTLCFG_DENALI_PHY_524 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_2	R/W	1h	PRBS7 start pattern for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_2	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_2	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1207 EMIF_CTLCFG_DENALI_PHY_525 Register

1 EMIF_CTLCFG_DENALI_PHY_525 Register (Offset = 4834h) [reset = 0h]

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Table 14-23565. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C834h

Figure 14-7820. EMIF_CTLCFG_DENALI_PHY_525 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTI_PATT_RST_DISABLE_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_RDLVL_MULTI_PATT_ENABLE_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_PRBS_PATTERN_MASK_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PRBS_PATTERN_MASK_2							
R/W							
0h							

Table 14-23567. EMIF_CTLCFG_DENALI_PHY_525 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_2	R/W	0h	Read Leveling read level windows disable reset for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_2	R/W	0h	Read Leveling Multi-pattern enable for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_2	R/W	0h	PRBS7 mask signal for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1208 EMIF_CTLCFG_DENALI_PHY_526 Register

1 EMIF_CTLCFG_DENALI_PHY_526 Register (Offset = 4838h) [reset = 0h]

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Table 14-23568. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C838h**

Figure 14-7821. EMIF_CTLCFG_DENALI_PHY_526 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_TRAIN_OBS_2</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_VREF_INITIAL_STEPSIZE_2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-23570. EMIF_CTLCFG_DENALI_PHY_526 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_2	R	0h	Observation register for best vref value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_2	R/W	0h	Data slice initial VREF training step size for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1209 EMIF_CTLCFG_DENALI_PHY_527 Register

1 EMIF_CTLCFG_DENALI_PHY_527 Register (Offset = 483Ch) [reset = 0h]

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Table 14-23571. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C83Ch**

Figure 14-7822. EMIF_CTLCFG_DENALI_PHY_527 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL1_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_SNAP_OBS_REGS_2
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_2			
NONE				R/W			
0h				0h			

Table 14-23573. EMIF_CTLCFG_DENALI_PHY_527 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_2	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_2	W	0h	Initiates a snapshot of the internal observation registers for slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_2	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1210 EMIF_CTLCFG_DENALI_PHY_528 Register

1 EMIF_CTLCFG_DENALI_PHY_528 Register (Offset = 4840h) [reset = 0h]

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Table 14-23574. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C840h**

Figure 14-7823. EMIF_CTLCFG_DENALI_PHY_528 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_MEM_CLASS_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							PHY_LPDDR_2
NONE							R/W
0h							0h

Table 14-23576. EMIF_CTLCFG_DENALI_PHY_528 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_2	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_2	R/W	0h	Indicates the type of DRAM for slice 2. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_2	R/W	0h	Adds a cycle of delay for the slice 2 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.6.6.2.1211 EMIF_CTLCFG_DENALI_PHY_529 Register

1 EMIF_CTLCFG_DENALI_PHY_529 Register (Offset = 4844h) [reset = 0h]

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Table 14-23577. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C844h

Figure 14-7824. EMIF_CTLCFG_DENALI_PHY_529 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ON_FLY_GATE_ADJUST_EN_2	
NONE						R/W	
0h						0h	

Table 14-23579. EMIF_CTLCFG_DENALI_PHY_529 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_2	R/W	0h	Control the on-the-fly gate adjustment for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1212 EMIF_CTLCFG_DENALI_PHY_530 Register

1 EMIF_CTLCFG_DENALI_PHY_530 Register (Offset = 4848h) [reset = 0h]

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Table 14-23580. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C848h**

Figure 14-7825. EMIF_CTLCFG_DENALI_PHY_530 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_2							
R							
0h							

Table 14-23582. EMIF_CTLCFG_DENALI_PHY_530 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_2	R	0h	Report the on-the-fly gate measurement result for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1213 EMIF_CTLCFG_DENALI_PHY_531 Register

1 EMIF_CTLCFG_DENALI_PHY_531 Register (Offset = 484Ch) [reset = 0h]

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Table 14-23583. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C84Ch**

Figure 14-7826. EMIF_CTLCFG_DENALI_PHY_531 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_2
NONE							R/W
0h							0h

Table 14-23585. EMIF_CTLCFG_DENALI_PHY_531 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_PST_AMBLE_2	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DFI40_POLARITY_2	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1214 EMIF_CTLCFG_DENALI_PHY_532 Register

1 EMIF_CTLCFG_DENALI_PHY_532 Register (Offset = 4850h) [reset = 0h]

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Table 14-23586. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C850h**

Figure 14-7827. EMIF_CTLCFG_DENALI_PHY_532 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_2							
R/W							
0h							

Table 14-23588. EMIF_CTLCFG_DENALI_PHY_532 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_2	R/W	0h	Read leveling pattern 8 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1215 EMIF_CTLCFG_DENALI_PHY_533 Register

1 EMIF_CTLCFG_DENALI_PHY_533 Register (Offset = 4854h) [reset = 0h]

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Table 14-23589. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C854h**

Figure 14-7828. EMIF_CTLCFG_DENALI_PHY_533 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT9_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT9_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_2							
R/W							
0h							

Table 14-23591. EMIF_CTLCFG_DENALI_PHY_533 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_2	R/W	0h	Read leveling pattern 9 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1216 EMIF_CTLCFG_DENALI_PHY_534 Register

1 EMIF_CTLCFG_DENALI_PHY_534 Register (Offset = 4858h) [reset = 0h]

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Table 14-23592. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C858h**

Figure 14-7829. EMIF_CTLCFG_DENALI_PHY_534 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_PATT10_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_PATT10_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_PATT10_2							
R/W							
0h							

Table 14-23594. EMIF_CTLCFG_DENALI_PHY_534 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_2	R/W	0h	Read leveling pattern 10 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1217 EMIF_CTLCFG_DENALI_PHY_535 Register

1 EMIF_CTLCFG_DENALI_PHY_535 Register (Offset = 485Ch) [reset = 0h]

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Table 14-23595. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C85Ch**

Figure 14-7830. EMIF_CTLCFG_DENALI_PHY_535 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_2							
R/W							
0h							

Table 14-23597. EMIF_CTLCFG_DENALI_PHY_535 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_2	R/W	0h	Read leveling pattern 11 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1218 EMIF_CTLCFG_DENALI_PHY_536 Register

1 EMIF_CTLCFG_DENALI_PHY_536 Register (Offset = 4860h) [reset = 0h]

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Table 14-23598. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C860h**

Figure 14-7831. EMIF_CTLCFG_DENALI_PHY_536 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_2							
R/W							
0h							

Table 14-23600. EMIF_CTLCFG_DENALI_PHY_536 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_2	R/W	0h	Read leveling pattern 12 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1219 EMIF_CTLCFG_DENALI_PHY_537 Register

1 EMIF_CTLCFG_DENALI_PHY_537 Register (Offset = 4864h) [reset = 0h]

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Table 14-23601. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C864h**

Figure 14-7832. EMIF_CTLCFG_DENALI_PHY_537 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_PATT13_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_PATT13_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_PATT13_2							
R/W							
0h							

Table 14-23603. EMIF_CTLCFG_DENALI_PHY_537 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_2	R/W	0h	Read leveling pattern 13 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1220 EMIF_CTLCFG_DENALI_PHY_538 Register

1 EMIF_CTLCFG_DENALI_PHY_538 Register (Offset = 4868h) [reset = 0h]

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Table 14-23604. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C868h**

Figure 14-7833. EMIF_CTLCFG_DENALI_PHY_538 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_2							
R/W							
0h							

Table 14-23606. EMIF_CTLCFG_DENALI_PHY_538 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_2	R/W	0h	Read leveling pattern 14 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1221 EMIF_CTLCFG_DENALI_PHY_539 Register

1 EMIF_CTLCFG_DENALI_PHY_539 Register (Offset = 486Ch) [reset = 0h]

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Table 14-23607. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C86Ch**

Figure 14-7834. EMIF_CTLCFG_DENALI_PHY_539 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_2							
R/W							
0h							

Table 14-23609. EMIF_CTLCFG_DENALI_PHY_539 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_2	R/W	0h	Read leveling pattern 15 data for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1222 EMIF_CTLCFG_DENALI_PHY_540 Register

1 EMIF_CTLCFG_DENALI_PHY_540 Register (Offset = 4870h) [reset = 0h]

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Table 14-23610. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C870h**

Figure 14-7835. EMIF_CTLCFG_DENALI_PHY_540 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED				PHY_MASTER_DLY_LOCK_OBS_SELECT_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_2		
NONE					R/W		
0h					0h		

Table 14-23612. EMIF_CTLCFG_DENALI_PHY_540 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_2	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_2	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 2. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_2	R/W	0h	Reserved for future use for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1223 EMIF_CTLCFG_DENALI_PHY_541 Register

1 EMIF_CTLCFG_DENALI_PHY_541 Register (Offset = 4874h) [reset = 0h]

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Table 14-23613. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C874h**

Figure 14-7836. EMIF_CTLCFG_DENALI_PHY_541 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WR_SHIFT_OBS_SELECT_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_WR_ENC_OBS_SELECT_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_2			
NONE				R/W			
0h				0h			

Table 14-23615. EMIF_CTLCFG_DENALI_PHY_541 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_2	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_2	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/ half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1224 EMIF_CTLCFG_DENALI_PHY_542 Register

1 EMIF_CTLCFG_DENALI_PHY_542 Register (Offset = 4878h) [reset = 0h]

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Table 14-23616. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C878h

Figure 14-7837. EMIF_CTLCFG_DENALI_PHY_542 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WRLVL_ALGO_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_LVL_DEBUG_CONT_2
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LVL_DEBUG_MODE_2
NONE							R/W
0h							0h

Table 14-23618. EMIF_CTLCFG_DENALI_PHY_542 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_2	R/W	0h	Write leveling algorithm selection for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_2	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_2	R/W	0h	Enables leveling debug mode for slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1225 EMIF_CTLCFG_DENALI_PHY_543 Register

1 EMIF_CTLCFG_DENALI_PHY_543 Register (Offset = 487Ch) [reset = 0h]

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Table 14-23619. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C87Ch**

Figure 14-7838. EMIF_CTLCFG_DENALI_PHY_543 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_GTLVL_CAPTURE_CNT_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_MASK_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_2			
NONE				R/W			
0h				0h			

Table 14-23621. EMIF_CTLCFG_DENALI_PHY_543 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 2. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_2	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1226 EMIF_CTLCFG_DENALI_PHY_544 Register

1 EMIF_CTLCFG_DENALI_PHY_544 Register (Offset = 4880h) [reset = 0h]

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Table 14-23622. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C880h**

Figure 14-7839. EMIF_CTLCFG_DENALI_PHY_544 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RDLVL_RDDQS_DQ_OBS_SELECT_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDLVL_OP_MODE_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_RDLVL_CAPTURE_CNT_2					
NONE		R/W					
0h		0h					

Table 14-23624. EMIF_CTLCFG_DENALI_PHY_544 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_2	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_2	R/W	0h	Read leveling algorithm select for slice 2. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1227 EMIF_CTLCFG_DENALI_PHY_545 Register

1 EMIF_CTLCFG_DENALI_PHY_545 Register (Offset = 4884h) [reset = 0h]

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Table 14-23625. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C884h**

Figure 14-7840. EMIF_CTLCFG_DENALI_PHY_545 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_DATA_SWIZZLE_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_DATA_SWIZZLE_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_DATA_MASK_2							
R/W							
0h							

Table 14-23627. EMIF_CTLCFG_DENALI_PHY_545 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_2	R/W	0h	Read level bit swizzling for DDR4 operation for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_2	R/W	0h	Per-bit mask for read leveling for slice 2. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1228 EMIF_CTLCFG_DENALI_PHY_546 Register

1 EMIF_CTLCFG_DENALI_PHY_546 Register (Offset = 4888h) [reset = 0h]

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Table 14-23628. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C888h**

Figure 14-7841. EMIF_CTLCFG_DENALI_PHY_546 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WDQLVL_PATT_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_WDQLVL_BURST_CNT_2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_CLK_JITTER_TOLERANCE_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23630. EMIF_CTLCFG_DENALI_PHY_546 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_2	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 2. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_2	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_2	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1229 EMIF_CTLCFG_DENALI_PHY_547 Register

1 EMIF_CTLCFG_DENALI_PHY_547 Register (Offset = 488Ch) [reset = 0h]

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Table 14-23631. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C88Ch

Figure 14-7842. EMIF_CTLCFG_DENALI_PHY_547 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2							
R/W							
0h							

Table 14-23633. EMIF_CTLCFG_DENALI_PHY_547 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_2	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1230 EMIF_CTLCFG_DENALI_PHY_548 Register

1 EMIF_CTLCFG_DENALI_PHY_548 Register (Offset = 4890h) [reset = 0h]

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Table 14-23634. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C890h**

Figure 14-7843. EMIF_CTLCFG_DENALI_PHY_548 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>SC_PHY_WDQLVL_CLR_PREV_RESULTS_2</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_WDQLVL_DM_DLY_STEP_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DQ_SLV_DELTA_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_PERIODIC_OBS_SELECT_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23636. EMIF_CTLCFG_DENALI_PHY_548 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_2	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_2	R/W	0h	The target delay line step for DM training for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_2	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_2	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1231 EMIF_CTLCFG_DENALI_PHY_549 Register

1 EMIF_CTLCFG_DENALI_PHY_549 Register (Offset = 4894h) [reset = 0h]

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Table 14-23637. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C894h**

Figure 14-7844. EMIF_CTLCFG_DENALI_PHY_549 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_WDQLVL_DATADM_MASK_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_WDQLVL_DATADM_MASK_2							
R/W							
0h							

Table 14-23639. EMIF_CTLCFG_DENALI_PHY_549 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_2	R/W	0h	Per-bit mask for write data leveling for slice 2. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1232 EMIF_CTLCFG_DENALI_PHY_550 Register

1 EMIF_CTLCFG_DENALI_PHY_550 Register (Offset = 4898h) [reset = 0h]

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Table 14-23640. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C898h**

Figure 14-7845. EMIF_CTLCFG_DENALI_PHY_550 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_USER_PATT0_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT0_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT0_2							
R/W							
0h							

Table 14-23642. EMIF_CTLCFG_DENALI_PHY_550 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1233 EMIF_CTLCFG_DENALI_PHY_551 Register

1 EMIF_CTLCFG_DENALI_PHY_551 Register (Offset = 489Ch) [reset = 0h]

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Table 14-23643. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C89Ch

Figure 14-7846. EMIF_CTLCFG_DENALI_PHY_551 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT1_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT1_2							
R/W							
0h							

Table 14-23645. EMIF_CTLCFG_DENALI_PHY_551 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1234 EMIF_CTLCFG_DENALI_PHY_552 Register

1 EMIF_CTLCFG_DENALI_PHY_552 Register (Offset = 48A0h) [reset = 0h]

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Table 14-23646. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8A0h**

Figure 14-7847. EMIF_CTLCFG_DENALI_PHY_552 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT2_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT2_2							
R/W							
0h							

Table 14-23648. EMIF_CTLCFG_DENALI_PHY_552 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1235 EMIF_CTLCFG_DENALI_PHY_553 Register

1 EMIF_CTLCFG_DENALI_PHY_553 Register (Offset = 48A4h) [reset = 0h]

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Table 14-23649. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8A4h**

Figure 14-7848. EMIF_CTLCFG_DENALI_PHY_553 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_USER_PATT3_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT3_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT3_2							
R/W							
0h							

Table 14-23651. EMIF_CTLCFG_DENALI_PHY_553 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1236 EMIF_CTLCFG_DENALI_PHY_554 Register

1 EMIF_CTLCFG_DENALI_PHY_554 Register (Offset = 48A8h) [reset = 0h]

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Table 14-23652. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8A8h**

Figure 14-7849. EMIF_CTLCFG_DENALI_PHY_554 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_NTP_MULT_TRAIN_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT4_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT4_2							
R/W							
0h							

Table 14-23654. EMIF_CTLCFG_DENALI_PHY_554 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_2	R/W	0h	Control for single pass only No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1237 EMIF_CTLCFG_DENALI_PHY_555 Register

1 EMIF_CTLCFG_DENALI_PHY_555 Register (Offset = 48ACh) [reset = 0h]

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Table 14-23655. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8ACh**

Figure 14-7850. EMIF_CTLCFG_DENALI_PHY_555 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_EARLY_THRESHOLD_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_EARLY_THRESHOLD_2							
R/W							
0h							

Table 14-23657. EMIF_CTLCFG_DENALI_PHY_555 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_2	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_2	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1238 EMIF_CTLCFG_DENALI_PHY_556 Register

1 EMIF_CTLCFG_DENALI_PHY_556 Register (Offset = 48B0h) [reset = 0h]

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Table 14-23658. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8B0h**

Figure 14-7851. EMIF_CTLCFG_DENALI_PHY_556 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_PERIOD_THRESHOLD_MAX_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_PERIOD_THRESHOLD_MIN_2							
R/W							
0h							

Table 14-23660. EMIF_CTLCFG_DENALI_PHY_556 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_2	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_2	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1239 EMIF_CTLCFG_DENALI_PHY_557 Register

1 EMIF_CTLCFG_DENALI_PHY_557 Register (Offset = 48B4h) [reset = 0h]

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Table 14-23661. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8B4h**

Figure 14-7852. EMIF_CTLCFG_DENALI_PHY_557 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_2					
NONE		W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_2
NONE							R/W
0h							0h

Table 14-23663. EMIF_CTLCFG_DENALI_PHY_557 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_2	R	0h	Observation register containing read entry FIFO pointers for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_2	W	0h	Manual reset/clear of internal logic for slice 2. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_2	R/W	0h	Indicates if slice 2 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1240 EMIF_CTLCFG_DENALI_PHY_558 Register

1 EMIF_CTLCFG_DENALI_PHY_558 Register (Offset = 48B8h) [reset = 100000h]

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Table 14-23664. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8B8h**

Figure 14-7853. EMIF_CTLCFG_DENALI_PHY_558 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_2							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_2							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_2							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_2							
R							
100000h							

Table 14-23666. EMIF_CTLCFG_DENALI_PHY_558 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_2	R	100000h	Observation register containing loopback status/results for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1241 EMIF_CTLCFG_DENALI_PHY_559 Register

1 EMIF_CTLCFG_DENALI_PHY_559 Register (Offset = 48BCh) [reset = 0h]

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Table 14-23667. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8BCh

Figure 14-7854. EMIF_CTLCFG_DENALI_PHY_559 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MASTER_DLY_LOCK_OBS_2		
NONE					R		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MASTER_DLY_LOCK_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_LPBK_ERROR_COUNT_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_LPBK_ERROR_COUNT_OBS_2							
R							
0h							

Table 14-23669. EMIF_CTLCFG_DENALI_PHY_559 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_2	R	0h	Observation register containing controller delay results for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_2	R	0h	Observation register containing total number of loopback error data for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1242 EMIF_CTLCFG_DENALI_PHY_560 Register

1 EMIF_CTLCFG_DENALI_PHY_560 Register (Offset = 48C0h) [reset = 0h]

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Table 14-23670. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8C0h**

Figure 14-7855. EMIF_CTLCFG_DENALI_PHY_560 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MEAS_DLY_STEP_VALUE_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_2						
NONE	R						
0h	0h						

Table 14-23672. EMIF_CTLCFG_DENALI_PHY_560 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_2	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS base target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQ target delay encoded values for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1243 EMIF_CTLCFG_DENALI_PHY_561 Register

1 EMIF_CTLCFG_DENALI_PHY_561 Register (Offset = 48C4h) [reset = 0h]

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Table 14-23673. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8C4h

Figure 14-7856. EMIF_CTLCFG_DENALI_PHY_561 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2						
NONE	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_2							
R							
0h							

Table 14-23675. EMIF_CTLCFG_DENALI_PHY_561 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write DQS base target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS gate target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1244 EMIF_CTLCFG_DENALI_PHY_562 Register

1 EMIF_CTLCFG_DENALI_PHY_562 Register (Offset = 48C8h) [reset = 0h]

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Table 14-23676. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8C8h**

Figure 14-7857. EMIF_CTLCFG_DENALI_PHY_562 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_WR_SHIFT_OBS_2		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WR_ADDER_SLV_DLY_ENC_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2							
R							
0h							

Table 14-23678. EMIF_CTLCFG_DENALI_PHY_562 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_2	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write adder target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write DQ base target delay encoded value for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1245 EMIF_CTLCFG_DENALI_PHY_563 Register

1 EMIF_CTLCFG_DENALI_PHY_563 Register (Offset = 48CCh) [reset = 0h]

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Table 14-23679. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8CCh

Figure 14-7858. EMIF_CTLCFG_DENALI_PHY_563 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_2	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_HARD1_DELAY_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_2	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_HARD0_DELAY_OBS_2							
R							
0h							

Table 14-23681. EMIF_CTLCFG_DENALI_PHY_563 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_2	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_2	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1246 EMIF_CTLCFG_DENALI_PHY_564 Register

1 EMIF_CTLCFG_DENALI_PHY_564 Register (Offset = 48D0h) [reset = 0h]

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Table 14-23682. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8D0h**

Figure 14-7859. EMIF_CTLCFG_DENALI_PHY_564 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_WRLVL_STATUS_OBS_2				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
PHY_WRLVL_STATUS_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_2							
R							
0h							

Table 14-23684. EMIF_CTLCFG_DENALI_PHY_564 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_2	R	0h	Observation register containing write leveling status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1247 EMIF_CTLCFG_DENALI_PHY_565 Register

1 EMIF_CTLCFG_DENALI_PHY_565 Register (Offset = 48D4h) [reset = 0h]

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Table 14-23685. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8D4h**

Figure 14-7860. EMIF_CTLCFG_DENALI_PHY_565 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2							
R							
0h							

Table 14-23687. EMIF_CTLCFG_DENALI_PHY_565 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing gate sample2 target delay encoded values for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing gate sample1 target delay encoded values for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1248 EMIF_CTLCFG_DENALI_PHY_566 Register

1 EMIF_CTLCFG_DENALI_PHY_566 Register (Offset = 48D8h) [reset = 0h]

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Table 14-23688. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8D8h**

Figure 14-7861. EMIF_CTLCFG_DENALI_PHY_566 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_2					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD0_DELAY_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_ERROR_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_ERROR_OBS_2							
R							
0h							

Table 14-23690. EMIF_CTLCFG_DENALI_PHY_566 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD0_DELAY_OBS_2	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_WRLVL_ERROR_OBS_2	R	0h	Observation register containing write leveling error status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1249 EMIF_CTLCFG_DENALI_PHY_567 Register

1 EMIF_CTLCFG_DENALI_PHY_567 Register (Offset = 48DCh) [reset = 0h]

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Table 14-23691. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8DCh

Figure 14-7862. EMIF_CTLCFG_DENALI_PHY_567 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_2					
NONE		R					
0h		0h					
7	6	5	4	3	2	1	0
PHY_GTLVL_HARD1_DELAY_OBS_2							
R							
0h							

Table 14-23693. EMIF_CTLCFG_DENALI_PHY_567 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD1_DELAY_OBS_2	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1250 EMIF_CTLCFG_DENALI_PHY_568 Register

1 EMIF_CTLCFG_DENALI_PHY_568 Register (Offset = 48E0h) [reset = 0h]

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Table 14-23694. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8E0h**

Figure 14-7863. EMIF_CTLCFG_DENALI_PHY_568 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_STATUS_OBS_2	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
PHY_GTLVL_STATUS_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_2							
R							
0h							

Table 14-23696. EMIF_CTLCFG_DENALI_PHY_568 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_2	R	0h	Observation register containing gate training status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1251 EMIF_CTLCFG_DENALI_PHY_569 Register

1 EMIF_CTLCFG_DENALI_PHY_569 Register (Offset = 48E4h) [reset = 0h]

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Table 14-23697. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8E4h

Figure 14-7864. EMIF_CTLCFG_DENALI_PHY_569 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2							
R							
0h							

Table 14-23699. EMIF_CTLCFG_DENALI_PHY_569 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1252 EMIF_CTLCFG_DENALI_PHY_570 Register

1 EMIF_CTLCFG_DENALI_PHY_570 Register (Offset = 48E8h) [reset = 0h]

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Table 14-23700. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8E8h

Figure 14-7865. EMIF_CTLCFG_DENALI_PHY_570 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_2	
NONE						R	
0h						0h	

Table 14-23702. EMIF_CTLCFG_DENALI_PHY_570 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_2	R	0h	Observation register containing read leveling number of windows found for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1253 EMIF_CTLCFG_DENALI_PHY_571 Register

1 EMIF_CTLCFG_DENALI_PHY_571 Register (Offset = 48ECh) [reset = 0h]

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Table 14-23703. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8ECh**

Figure 14-7866. EMIF_CTLCFG_DENALI_PHY_571 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_2							
R							
0h							

Table 14-23705. EMIF_CTLCFG_DENALI_PHY_571 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_2	R	0h	Observation register containing read leveling status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1254 EMIF_CTLCFG_DENALI_PHY_572 Register

1 EMIF_CTLCFG_DENALI_PHY_572 Register (Offset = 48F0h) [reset = 7FF0000h]

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Table 14-23706. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8F0h**

Figure 14-7867. EMIF_CTLCFG_DENALI_PHY_572 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_2		
NONE					R		
0h					7FFh		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DQDM_TE_DLY_OBS_2							
R							
7FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_2		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_LE_DLY_OBS_2							
R							
0h							

Table 14-23708. EMIF_CTLCFG_DENALI_PHY_572 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_2	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_2	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1255 EMIF_CTLCFG_DENALI_PHY_573 Register

1 EMIF_CTLCFG_DENALI_PHY_573 Register (Offset = 48F4h) [reset = 0h]

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Table 14-23709. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8F4h**

Figure 14-7868. EMIF_CTLCFG_DENALI_PHY_573 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_2							
R							
0h							

Table 14-23711. EMIF_CTLCFG_DENALI_PHY_573 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_2	R	0h	Observation register containing write data leveling status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1256 EMIF_CTLCFG_DENALI_PHY_574 Register

1 EMIF_CTLCFG_DENALI_PHY_574 Register (Offset = 48F8h) [reset = 0h]

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Table 14-23712. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C8F8h

Figure 14-7869. EMIF_CTLCFG_DENALI_PHY_574 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_PERIODIC_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_PERIODIC_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_2							
R							
0h							

Table 14-23714. EMIF_CTLCFG_DENALI_PHY_574 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_2	R	0h	Observation register containing periodic write data leveling status for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1257 EMIF_CTLCFG_DENALI_PHY_575 Register

1 EMIF_CTLCFG_DENALI_PHY_575 Register (Offset = 48FCh) [reset = 0h]

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Table 14-23715. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C8FCh**

Figure 14-7870. EMIF_CTLCFG_DENALI_PHY_575 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_2						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_MODE_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_MODE_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_MODE_2							
R/W							
0h							

Table 14-23717. EMIF_CTLCFG_DENALI_PHY_575 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_2	R/W	0h	DDL mode for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1258 EMIF_CTLCFG_DENALI_PHY_576 Register

1 EMIF_CTLCFG_DENALI_PHY_576 Register (Offset = 4900h) [reset = 0h]

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Table 14-23718. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C900h**

Figure 14-7871. EMIF_CTLCFG_DENALI_PHY_576 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_DDL_MASK_2					
NONE		R/W					
0h		0h					

Table 14-23720. EMIF_CTLCFG_DENALI_PHY_576 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_2	R/W	0h	DDL mask for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1259 EMIF_CTLCFG_DENALI_PHY_577 Register

1 EMIF_CTLCFG_DENALI_PHY_577 Register (Offset = 4904h) [reset = 0h]

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Table 14-23721. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C904h**

Figure 14-7872. EMIF_CTLCFG_DENALI_PHY_577 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_2							
R							
0h							

Table 14-23723. EMIF_CTLCFG_DENALI_PHY_577 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_2	R	0h	DDL test observation for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1260 EMIF_CTLCFG_DENALI_PHY_578 Register

1 EMIF_CTLCFG_DENALI_PHY_578 Register (Offset = 4908h) [reset = 0h]

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Table 14-23724. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C908h**

Figure 14-7873. EMIF_CTLCFG_DENALI_PHY_578 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							

Table 14-23726. EMIF_CTLCFG_DENALI_PHY_578 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_2	R	0h	DDL test observation delays for slice 2 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1261 EMIF_CTLCFG_DENALI_PHY_579 Register

1 EMIF_CTLCFG_DENALI_PHY_579 Register (Offset = 490Ch) [reset = 0h]

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Table 14-23727. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C90Ch**

Figure 14-7874. EMIF_CTLCFG_DENALI_PHY_579 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ0_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_LP4_WDQS_OE_EXTEND_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_TRACK_UPD_THRESHOLD_2							
R/W							
0h							

Table 14-23729. EMIF_CTLCFG_DENALI_PHY_579 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_2	R/W	0h	RX Calibration codes for DQ0 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_2	R/W	0h	LPDDR4 write preamble extension enable for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_2	R/W	0h	Specify threshold value for PHY init update tracking for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1262 EMIF_CTLCFG_DENALI_PHY_580 Register

1 EMIF_CTLCFG_DENALI_PHY_580 Register (Offset = 4910h) [reset = 0h]

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Table 14-23730. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C910h**

Figure 14-7875. EMIF_CTLCFG_DENALI_PHY_580 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ2_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ1_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ1_2							
R/W							
0h							

Table 14-23732. EMIF_CTLCFG_DENALI_PHY_580 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_2	R/W	0h	RX Calibration codes for DQ2 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_2	R/W	0h	RX Calibration codes for DQ1 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1263 EMIF_CTLCFG_DENALI_PHY_581 Register

1 EMIF_CTLCFG_DENALI_PHY_581 Register (Offset = 4914h) [reset = 0h]

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Table 14-23733. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C914h**

Figure 14-7876. EMIF_CTLCFG_DENALI_PHY_581 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ4_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ4_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ3_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ3_2							
R/W							
0h							

Table 14-23735. EMIF_CTLCFG_DENALI_PHY_581 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_2	R/W	0h	RX Calibration codes for DQ4 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_2	R/W	0h	RX Calibration codes for DQ3 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1264 EMIF_CTLCFG_DENALI_PHY_582 Register

1 EMIF_CTLCFG_DENALI_PHY_582 Register (Offset = 4918h) [reset = 0h]

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Table 14-23736. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C918h**

Figure 14-7877. EMIF_CTLCFG_DENALI_PHY_582 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ6_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ5_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ5_2							
R/W							
0h							

Table 14-23738. EMIF_CTLCFG_DENALI_PHY_582 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_2	R/W	0h	RX Calibration codes for DQ6 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_2	R/W	0h	RX Calibration codes for DQ5 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1265 EMIF_CTLCFG_DENALI_PHY_583 Register

1 EMIF_CTLCFG_DENALI_PHY_583 Register (Offset = 491Ch) [reset = 0h]

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Table 14-23739. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C91Ch**

Figure 14-7878. EMIF_CTLCFG_DENALI_PHY_583 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ7_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ7_2							
R/W							
0h							

Table 14-23741. EMIF_CTLCFG_DENALI_PHY_583 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_2	R/W	0h	RX Calibration codes for DQ7 for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1266 EMIF_CTLCFG_DENALI_PHY_584 Register

1 EMIF_CTLCFG_DENALI_PHY_584 Register (Offset = 4920h) [reset = 0h]

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Table 14-23742. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C920h**

Figure 14-7879. EMIF_CTLCFG_DENALI_PHY_584 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RX_CAL_DM_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RX_CAL_DM_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DM_2							
R/W							
0h							

Table 14-23744. EMIF_CTLCFG_DENALI_PHY_584 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_2	R/W	0h	RX Calibration codes for DM for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1267 EMIF_CTLCFG_DENALI_PHY_585 Register

1 EMIF_CTLCFG_DENALI_PHY_585 Register (Offset = 4924h) [reset = 0h]

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Table 14-23745. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C924h**

Figure 14-7880. EMIF_CTLCFG_DENALI_PHY_585 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_FDBK_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQS_2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQS_2							
R/W							
0h							

Table 14-23747. EMIF_CTLCFG_DENALI_PHY_585 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_2	R/W	0h	RX Calibration codes for FDBK for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_2	R/W	0h	RX Calibration codes for DQS for slice 2. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1268 EMIF_CTLCFG_DENALI_PHY_586 Register

1 EMIF_CTLCFG_DENALI_PHY_586 Register (Offset = 4928h) [reset = 0h]

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Table 14-23748. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C928h**

Figure 14-7881. EMIF_CTLCFG_DENALI_PHY_586 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_CAL_SAMPLE_WAIT_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_STATIC_TOG_DISABLE_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_PAD_RX_BIAS_EN_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_PAD_RX_BIAS_EN_2							
R/W							
0h							

Table 14-23750. EMIF_CTLCFG_DENALI_PHY_586 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_CAL_SAMPLE_WAIT_2	R/W	0h	Determines number of cycles to wait for each sample for slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_2	R/W	0h	Control to disable toggle during static activity for slice 2. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_2	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1269 EMIF_CTLCFG_DENALI_PHY_587 Register

1 EMIF_CTLCFG_DENALI_PHY_587 Register (Offset = 492Ch) [reset = 0h]

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Table 14-23751. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C92Ch**

Figure 14-7882. EMIF_CTLCFG_DENALI_PHY_587 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DATA_DC_ADJUST_SAMPLE_CNT_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_DATA_DC_ADJUST_START_2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DATA_DC_WEIGHT_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_DC_CAL_TIMEOUT_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23753. EMIF_CTLCFG_DENALI_PHY_587 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_ADJUST_SAMPLE_CNT_2	R/W	0h	Duty cycle adjust sample count for slice 2. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DATA_DC_ADJUST_START_2	R/W	0h	Duty cycle adjust starting value for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DATA_DC_WEIGHT_2	R/W	0h	Determines weight of average calculating for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_CAL_TIMEOUT_2	R/W	0h	Determines timeout number of iteration for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1270 EMIF_CTLCFG_DENALI_PHY_588 Register

1 EMIF_CTLCFG_DENALI_PHY_588 Register (Offset = 4930h) [reset = 0h]

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Table 14-23754. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C930h**

Figure 14-7883. EMIF_CTLCFG_DENALI_PHY_588 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_CAL_START_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DATA_DC_CAL_POLARITY_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DATA_DC_ADJUST_THRSHLD_2							
R/W							
0h							

Table 14-23756. EMIF_CTLCFG_DENALI_PHY_588 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_DATA_DC_CAL_START_2	R/W	0h	Manual trigger for DCC for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DATA_DC_CAL_POLARITY_2	R/W	0h	Calibration polarity for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_ADJUST_DIRECT_2	R/W	0h	Adjust direction for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_ADJUST_THRSHLD_2	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1271 EMIF_CTLCFG_DENALI_PHY_589 Register

1 EMIF_CTLCFG_DENALI_PHY_589 Register (Offset = 4934h) [reset = 1h]

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Table 14-23757. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C934h**

Figure 14-7884. EMIF_CTLCFG_DENALI_PHY_589 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDPATH_GATE_DISABLE_2
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_2
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED					PHY_FDBK_PWR_CTRL_2		
NONE					R/W		
0h					0h		

7	6	5	4	3	2	1	0
RESERVED						PHY_DATA_DC_SW_RANK_2	
NONE						R/W	
0h						1h	

Table 14-23759. EMIF_CTLCFG_DENALI_PHY_589 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDPATH_GATE_DISABLE_2	R/W	0h	Data slice read path power reduction disable for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SLV_DLY_CTRL_GATE_DISABLE_2	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_FDBK_PWR_CTRL_2	R/W	0h	Shutoff gate feedback IO to reduce power for slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DATA_DC_SW_RANK_2	R/W	1h	Rank selection for software based duty cycle correction for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1272 EMIF_CTLCFG_DENALI_PHY_590 Register

1 EMIF_CTLCFG_DENALI_PHY_590 Register (Offset = 4938h) [reset = 0h]

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Table 14-23760. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C938h

Figure 14-7885. EMIF_CTLCFG_DENALI_PHY_590 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_2
NONE							R/W
0h							0h

Table 14-23762. EMIF_CTLCFG_DENALI_PHY_590 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_SLICE_PWR_RDC_DISABLE_2	R/W	0h	Data slice power reduction disable for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_2	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1273 EMIF_CTLCFG_DENALI_PHY_591 Register

1 EMIF_CTLCFG_DENALI_PHY_591 Register (Offset = 493Ch) [reset = 0h]

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Table 14-23763. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C93Ch**

Figure 14-7886. EMIF_CTLCFG_DENALI_PHY_591 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_SELECT_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_SELECT_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DQ_TSEL_ENABLE_2		
NONE					R/W		
0h					0h		

Table 14-23765. EMIF_CTLCFG_DENALI_PHY_591 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_2	R/W	0h	Operation type tsel enables for DQS signals for slice 2. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_2	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 2. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_2	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 2. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1274 EMIF_CTLCFG_DENALI_PHY_592 Register

1 EMIF_CTLCFG_DENALI_PHY_592 Register (Offset = 4940h) [reset = 0h]

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Table 14-23766. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C940h**

Figure 14-7887. EMIF_CTLCFG_DENALI_PHY_592 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_2						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_TWO_CYC_PREAMBLE_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQS_TSEL_SELECT_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQS_TSEL_SELECT_2							
R/W							
0h							

Table 14-23768. EMIF_CTLCFG_DENALI_PHY_592 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_2	R/W	0h	Data slice initial VREF training start value for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_2	R/W	0h	2 cycle preamble support for slice 2. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_2	R/W	0h	Operation type tsel select values for DQS signals for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1275 EMIF_CTLCFG_DENALI_PHY_593 Register

1 EMIF_CTLCFG_DENALI_PHY_593 Register (Offset = 4944h) [reset = 0h]

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Table 14-23769. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C944h**

Figure 14-7888. EMIF_CTLCFG_DENALI_PHY_593 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_NTP_WDQ_STEP_SIZE_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_NTP_TRAIN_EN_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_VREF_TRAINING_CTRL_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_INITIAL_STOP_POINT_2</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-23771. EMIF_CTLCFG_DENALI_PHY_593 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_2	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_2	R/W	0h	Enable for No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_2	R/W	0h	Data slice vref training enable control for slice 2. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_2	R/W	0h	Data slice initial VREF training stop value for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1276 EMIF_CTLCFG_DENALI_PHY_594 Register

1 EMIF_CTLCFG_DENALI_PHY_594 Register (Offset = 4948h) [reset = 0h]

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Table 14-23772. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C948h**

Figure 14-7889. EMIF_CTLCFG_DENALI_PHY_594 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_NTP_WDQ_STOP_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_NTP_WDQ_START_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_START_2							
R/W							
0h							

Table 14-23774. EMIF_CTLCFG_DENALI_PHY_594 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_2	R/W	0h	End of WR DQ target delay in No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_2	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1277 EMIF_CTLCFG_DENALI_PHY_595 Register

1 EMIF_CTLCFG_DENALI_PHY_595 Register (Offset = 494Ch) [reset = 0h]

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Table 14-23775. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C94Ch**

Figure 14-7890. EMIF_CTLCFG_DENALI_PHY_595 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WDQLVL_DVW_MIN_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DVW_MIN_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_BIT_EN_2							
R/W							
0h							

Table 14-23777. EMIF_CTLCFG_DENALI_PHY_595 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_2	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_2	R/W	0h	Minimum data valid window across DQs and ranks for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_2	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1278 EMIF_CTLCFG_DENALI_PHY_596 Register

1 EMIF_CTLCFG_DENALI_PHY_596 Register (Offset = 4950h) [reset = 0h]

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Table 14-23778. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C950h

Figure 14-7891. EMIF_CTLCFG_DENALI_PHY_596 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_TX_DCD_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_FAST_LVL_EN_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_WDQLVL_PER_START_OFFSET_2					
NONE		R/W					
0h		0h					

Table 14-23780. EMIF_CTLCFG_DENALI_PHY_596 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_2	R/W	0h	Controls TX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_2	R/W	0h	Enable for fast multi-pattern window search for slice 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_2	R/W	0h	Peridic training start point offset for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1279 EMIF_CTLCFG_DENALI_PHY_597 Register

1 EMIF_CTLCFG_DENALI_PHY_597 Register (Offset = 4954h) [reset = 0h]

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Table 14-23781. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C954h

Figure 14-7892. EMIF_CTLCFG_DENALI_PHY_597 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_3_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_2_2				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_1_2				
NONE			R/W				
0h			0h				

Table 14-23783. EMIF_CTLCFG_DENALI_PHY_597 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1280 EMIF_CTLCFG_DENALI_PHY_598 Register

1 EMIF_CTLCFG_DENALI_PHY_598 Register (Offset = 4958h) [reset = 0h]

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Table 14-23784. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C958h

Figure 14-7893. EMIF_CTLCFG_DENALI_PHY_598 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_7_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_6_2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_5_2				
NONE			R/W				
0h			0h				

Table 14-23786. EMIF_CTLCFG_DENALI_PHY_598 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_2	R/W	0h	Controls RX_DCD pin for dm pad for slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1281 EMIF_CTLCFG_DENALI_PHY_599 Register

1 EMIF_CTLCFG_DENALI_PHY_599 Register (Offset = 495Ch) [reset = 0h]

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Table 14-23787. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C95Ch**

Figure 14-7894. EMIF_CTLCFG_DENALI_PHY_599 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_PAD_DSLICE_IO_CFG_2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_2				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_2				
NONE			R/W				
0h			0h				

Table 14-23789. EMIF_CTLCFG_DENALI_PHY_599 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_2	R/W	0h	Controls PCLK/PARK pin for pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_2	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_2	R/W	0h	Controls RX_DCD pin for dqs pad for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1282 EMIF_CTLCFG_DENALI_PHY_600 Register

1 EMIF_CTLCFG_DENALI_PHY_600 Register (Offset = 4960h) [reset = 0h]

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Table 14-23790. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C960h**

Figure 14-7895. EMIF_CTLCFG_DENALI_PHY_600 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ1_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ0_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ0_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23792. EMIF_CTLCFG_DENALI_PHY_600 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_2	R/W	0h	Read DQ1 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_2	R/W	0h	Read DQ0 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1283 EMIF_CTLCFG_DENALI_PHY_601 Register

1 EMIF_CTLCFG_DENALI_PHY_601 Register (Offset = 4964h) [reset = 0h]

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Table 14-23793. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C964h**

Figure 14-7896. EMIF_CTLCFG_DENALI_PHY_601 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ3_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ2_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ2_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23795. EMIF_CTLCFG_DENALI_PHY_601 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_2	R/W	0h	Read DQ3 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_2	R/W	0h	Read DQ2 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1284 EMIF_CTLCFG_DENALI_PHY_602 Register

1 EMIF_CTLCFG_DENALI_PHY_602 Register (Offset = 4968h) [reset = 0h]

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Table 14-23796. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C968h**

Figure 14-7897. EMIF_CTLCFG_DENALI_PHY_602 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ5_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ4_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ4_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23798. EMIF_CTLCFG_DENALI_PHY_602 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_2	R/W	0h	Read DQ5 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_2	R/W	0h	Read DQ4 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1285 EMIF_CTLCFG_DENALI_PHY_603 Register

1 EMIF_CTLCFG_DENALI_PHY_603 Register (Offset = 496Ch) [reset = 0h]

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Table 14-23799. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C96Ch**

Figure 14-7898. EMIF_CTLCFG_DENALI_PHY_603 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ7_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ7_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ6_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ6_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23801. EMIF_CTLCFG_DENALI_PHY_603 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_2	R/W	0h	Read DQ7 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_2	R/W	0h	Read DQ6 target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1286 EMIF_CTLCFG_DENALI_PHY_604 Register

1 EMIF_CTLCFG_DENALI_PHY_604 Register (Offset = 4970h) [reset = 0h]

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Table 14-23802. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C970h

Figure 14-7899. EMIF_CTLCFG_DENALI_PHY_604 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_RX_PCLK_CLK_SEL_2		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDM_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDM_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23804. EMIF_CTLCFG_DENALI_PHY_604 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_2	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 2. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_2	R/W	0h	RX_PCLK clock frequency selection for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_2	R/W	0h	Read DM/DBI target delay setting for slice 2. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1287 EMIF_CTLCFG_DENALI_PHY_605 Register

1 EMIF_CTLCFG_DENALI_PHY_605 Register (Offset = 4974h) [reset = 0h]

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Table 14-23805. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C974h

Figure 14-7900. EMIF_CTLCFG_DENALI_PHY_605 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_DATA_DC_CAL_CLK_SEL_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-23807. EMIF_CTLCFG_DENALI_PHY_605 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DATA_DC_CAL_CLK_SEL_2	R/W	0h	Determines DCC CAL clock for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1288 EMIF_CTLCFG_DENALI_PHY_606 Register

1 EMIF_CTLCFG_DENALI_PHY_606 Register (Offset = 4978h) [reset = 0h]

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Table 14-23808. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C978h**

Figure 14-7901. EMIF_CTLCFG_DENALI_PHY_606 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_OE_TIMING_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_WR_TIMING_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_RD_TIMING_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_OE_TIMING_2							
R/W							
0h							

Table 14-23810. EMIF_CTLCFG_DENALI_PHY_606 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_2	R/W	0h	Start/end timing values for DQS output enable signals for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_2	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_2	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_2	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1289 EMIF_CTLCFG_DENALI_PHY_607 Register

1 EMIF_CTLCFG_DENALI_PHY_607 Register (Offset = 497Ch) [reset = 0h]

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Table 14-23811. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C97Ch

Figure 14-7902. EMIF_CTLCFG_DENALI_PHY_607 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_2							
R/W							
0h							

23	22	21	20	19	18	17	16
PHY_DQS_OE_RD_TIMING_2							
R/W							
0h							

15	14	13	12	11	10	9	8
PHY_DQS_TSEL_RD_TIMING_2							
R/W							
0h							

7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_2			
NONE				R/W			
0h				0h			

Table 14-23813. EMIF_CTLCFG_DENALI_PHY_607 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_2	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_2	R/W	0h	Start/end timing values for DQS read based OE extension for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_2	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_2	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1290 EMIF_CTLCFG_DENALI_PHY_608 Register

1 EMIF_CTLCFG_DENALI_PHY_608 Register (Offset = 4980h) [reset = 0h]

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Table 14-23814. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C980h**

Figure 14-7903. EMIF_CTLCFG_DENALI_PHY_608 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_VREF_CTRL_DQ_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_VREF_SETTING_TIME_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_VREF_SETTING_TIME_2							
R/W							
0h							

Table 14-23816. EMIF_CTLCFG_DENALI_PHY_608 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_2	R/W	0h	Pad VREF control settings for DQ slice 2. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_2	R/W	0h	Number of cycles for vref settle after setting is changed for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1291 EMIF_CTLCFG_DENALI_PHY_609 Register

1 EMIF_CTLCFG_DENALI_PHY_609 Register (Offset = 4984h) [reset = 0h]

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Table 14-23817. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C984h**

Figure 14-7904. EMIF_CTLCFG_DENALI_PHY_609 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQS_IE_TIMING_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_IE_TIMING_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_PER_CS_TRAINING_EN_2
NONE							R/W
0h							0h

Table 14-23819. EMIF_CTLCFG_DENALI_PHY_609 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_RDDATA_EN_IE_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_IE_TIMING_2	R/W	0h	Start/end timing values for DQS input enable signals for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_IE_TIMING_2	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_EN_2	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 2. Must have same value in all slices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1292 EMIF_CTLCFG_DENALI_PHY_610 Register

1 EMIF_CTLCFG_DENALI_PHY_610 Register (Offset = 4988h) [reset = 0h]

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Table 14-23820. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C988h**

Figure 14-7905. EMIF_CTLCFG_DENALI_PHY_610 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_WDQLVL_IE_ON_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DBI_MODE_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_IE_MODE_2	
NONE						R/W	
0h						0h	

Table 14-23822. EMIF_CTLCFG_DENALI_PHY_610 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_DLY_2	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_WDQLVL_IE_ON_2	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DBI_MODE_2	R/W	0h	DBI mode for slice 2. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_IE_MODE_2	R/W	0h	Input enable mode bits for slice 2. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1293 EMIF_CTLCFG_DENALI_PHY_611 Register

1 EMIF_CTLCFG_DENALI_PHY_611 Register (Offset = 498Ch) [reset = 0h]

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Table 14-23823. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C98Ch**

Figure 14-7906. EMIF_CTLCFG_DENALI_PHY_611 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_MASTER_MODE_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_RDDATA_EN_OE_DLY_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_RDDATA_EN_TSEL_DLY_2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_2				
NONE			R/W				
0h			0h				

Table 14-23825. EMIF_CTLCFG_DENALI_PHY_611 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_MASTER_MODE_2	R/W	0h	Controller delay line override settings for slice 2. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_OE_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_TSEL_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_2	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1294 EMIF_CTLCFG_DENALI_PHY_612 Register

1 EMIF_CTLCFG_DENALI_PHY_612 Register (Offset = 4990h) [reset = 0h]

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Table 14-23826. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C990h

Figure 14-7907. EMIF_CTLCFG_DENALI_PHY_612 Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_DELAY_WAIT_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_MASTER_DELAY_STEP_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MASTER_DELAY_START_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_START_2							
R/W							
0h							

Table 14-23828. EMIF_CTLCFG_DENALI_PHY_612 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_2	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 2. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_2	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_2	R/W	0h	Start value for controller delay line locking algorithm for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1295 EMIF_CTLCFG_DENALI_PHY_613 Register

1 EMIF_CTLCFG_DENALI_PHY_613 Register (Offset = 4994h) [reset = 0h]

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Table 14-23829. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C994h**

Figure 14-7908. EMIF_CTLCFG_DENALI_PHY_613 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DLY_STEP_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RPTR_UPDATE_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_HALF_MEASURE_2							
R/W							
0h							

Table 14-23831. EMIF_CTLCFG_DENALI_PHY_613 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_2	R/W	0h	DQS target delay fine step size during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_2	R/W	0h	DQS target delay step size during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_2	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_2	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1296 EMIF_CTLCFG_DENALI_PHY_614 Register

1 EMIF_CTLCFG_DENALI_PHY_614 Register (Offset = 4998h) [reset = 0h]

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Table 14-23832. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C998h**

Figure 14-7909. EMIF_CTLCFG_DENALI_PHY_614 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_GTLVL_RESP_WAIT_CNT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_GTLVL_DLY_STEP_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_WRLVL_RESP_WAIT_CNT_2					
NONE		R/W					
0h		0h					

Table 14-23834. EMIF_CTLCFG_DENALI_PHY_614 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_2	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 2. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_2	R/W	0h	DQS target delay step size during gate training for slice 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_2	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1297 EMIF_CTLCFG_DENALI_PHY_615 Register

1 EMIF_CTLCFG_DENALI_PHY_615 Register (Offset = 499Ch) [reset = 0h]

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Table 14-23835. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C99Ch**

Figure 14-7910. EMIF_CTLCFG_DENALI_PHY_615 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GTLVL_FINAL_STEP_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_GTLVL_FINAL_STEP_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_BACK_STEP_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_BACK_STEP_2							
R/W							
0h							

Table 14-23837. EMIF_CTLCFG_DENALI_PHY_615 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_2	R/W	0h	Final backup step delay used in gate training algorithm for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_2	R/W	0h	Interim backup step delay used in gate training algorithm for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1298 EMIF_CTLCFG_DENALI_PHY_616 Register

1 EMIF_CTLCFG_DENALI_PHY_616 Register (Offset = 49A0h) [reset = 0h]

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Table 14-23838. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9A0h**

Figure 14-7911. EMIF_CTLCFG_DENALI_PHY_616 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_WDQLVL_DM_SEARCH_RANGE_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DM_SEARCH_RANGE_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_WDQLVL_QTR_DLY_STEP_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DLY_STEP_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23840. EMIF_CTLCFG_DENALI_PHY_616 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_2	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_2	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 2. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_2	R/W	0h	DQ target delay step size during write data leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1299 EMIF_CTLCFG_DENALI_PHY_617 Register

1 EMIF_CTLCFG_DENALI_PHY_617 Register (Offset = 49A4h) [reset = 0h]

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Table 14-23841. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9A4h**

Figure 14-7912. EMIF_CTLCFG_DENALI_PHY_617 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_DLY_STEP_2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_TOGGLE_PRE_SUPPORT_2
NONE							R/W
0h							0h

Table 14-23843. EMIF_CTLCFG_DENALI_PHY_617 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_2	R/W	0h	DQS target delay step size during read leveling for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_2	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1300 EMIF_CTLCFG_DENALI_PHY_618 Register

1 EMIF_CTLCFG_DENALI_PHY_618 Register (Offset = 49A8h) [reset = 0h]

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Table 14-23844. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9A8h**

Figure 14-7913. EMIF_CTLCFG_DENALI_PHY_618 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_MAX_EDGE_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_MAX_EDGE_2							
R/W							
0h							

Table 14-23846. EMIF_CTLCFG_DENALI_PHY_618 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_2	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1301 EMIF_CTLCFG_DENALI_PHY_619 Register

1 EMIF_CTLCFG_DENALI_PHY_619 Register (Offset = 49ACh) [reset = 30000h]

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Table 14-23847. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C9ACh

Figure 14-7914. EMIF_CTLCFG_DENALI_PHY_619 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_DATA_DC_INIT_DISABLE_2	
NONE						R/W	
0h						3h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRPATH_GATE_TIMING_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_WRPATH_GATE_DISABLE_2	
NONE						R/W	
0h						0h	

Table 14-23849. EMIF_CTLCFG_DENALI_PHY_619 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DATA_DC_INIT_DISABLE_2	R/W	3h	Disable duty cycle adjust at initialization for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_2	R/W	0h	Write path clock gating timing for slice 2. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_2	R/W	0h	Write path clock gating disable for slice 2. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.6.6.2.1302 EMIF_CTLCFG_DENALI_PHY_620 Register

1 EMIF_CTLCFG_DENALI_PHY_620 Register (Offset = 49B0h) [reset = 0h]

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Table 14-23850. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9B0h**

Figure 14-7915. EMIF_CTLCFG_DENALI_PHY_620 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ_INIT_SLV_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQS_INIT_SLV_DELAY_2							
R/W							
0h							

Table 14-23852. EMIF_CTLCFG_DENALI_PHY_620 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_2	R/W	0h	Initial value of write DQ target delay for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_2	R/W	0h	Initial value of write DQS target delay for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1303 EMIF_CTLCFG_DENALI_PHY_621 Register

1 EMIF_CTLCFG_DENALI_PHY_621 Register (Offset = 49B4h) [reset = 0h]

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Table 14-23853. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C9B4h

Figure 14-7916. EMIF_CTLCFG_DENALI_PHY_621 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_2
NONE							R/W
0h							0h

Table 14-23855. EMIF_CTLCFG_DENALI_PHY_621 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_2	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_2	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_WDQLVL_ENABLE_2	R/W	0h	Enable duty cycle adjust during write DQ training for slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DATA_DC_WRLVL_ENABLE_2	R/W	0h	Enable duty cycle adjust during write leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1304 EMIF_CTLCFG_DENALI_PHY_622 Register

1 EMIF_CTLCFG_DENALI_PHY_622 Register (Offset = 49B8h) [reset = 0h]

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Table 14-23856. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9B8h**

Figure 14-7917. EMIF_CTLCFG_DENALI_PHY_622 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_RDDATA_EN_DLY_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED	PHY_MEAS_DLY_STEP_ENABLE_2						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_WDQ_OSC_DELTA_2						
NONE	R/W						
0h	0h						

Table 14-23858. EMIF_CTLCFG_DENALI_PHY_622 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_MEAS_DLY_STEP_ENABLE_2	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 2. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_WDQ_OSC_DELTA_2	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1305 EMIF_CTLCFG_DENALI_PHY_623 Register

1 EMIF_CTLCFG_DENALI_PHY_623 Register (Offset = 49BCh) [reset = 0h]

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Table 14-23859. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9BCh**

Figure 14-7918. EMIF_CTLCFG_DENALI_PHY_623 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_DM_SWIZZLE0_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_DM_SWIZZLE0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_2							
R/W							
0h							

Table 14-23861. EMIF_CTLCFG_DENALI_PHY_623 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_2	R/W	0h	DQ/DM bit swizzling 0 for slice 2. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1306 EMIF_CTLCFG_DENALI_PHY_624 Register

1 EMIF_CTLCFG_DENALI_PHY_624 Register (Offset = 49C0h) [reset = 0h]

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Table 14-23862. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C9C0h

Figure 14-7919. EMIF_CTLCFG_DENALI_PHY_624 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_2			
NONE				R/W			
0h				0h			

Table 14-23864. EMIF_CTLCFG_DENALI_PHY_624 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_2	R/W	0h	DQ/DM bit swizzling 1 for slice 2. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1307 EMIF_CTLCFG_DENALI_PHY_625 Register

1 EMIF_CTLCFG_DENALI_PHY_625 Register (Offset = 49C4h) [reset = 0h]

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Table 14-23865. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9C4h**

Figure 14-7920. EMIF_CTLCFG_DENALI_PHY_625 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ1_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ0_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23867. EMIF_CTLCFG_DENALI_PHY_625 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ1 for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ0 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1308 EMIF_CTLCFG_DENALI_PHY_626 Register

1 EMIF_CTLCFG_DENALI_PHY_626 Register (Offset = 49C8h) [reset = 0h]

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Table 14-23868. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9C8h**

Figure 14-7921. EMIF_CTLCFG_DENALI_PHY_626 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ3_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ2_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23870. EMIF_CTLCFG_DENALI_PHY_626 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ3 for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ2 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1309 EMIF_CTLCFG_DENALI_PHY_627 Register

1 EMIF_CTLCFG_DENALI_PHY_627 Register (Offset = 49CCh) [reset = 0h]

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Table 14-23871. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9CCh**

Figure 14-7922. EMIF_CTLCFG_DENALI_PHY_627 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ5_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ4_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23873. EMIF_CTLCFG_DENALI_PHY_627 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ5 for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ4 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1310 EMIF_CTLCFG_DENALI_PHY_628 Register

1 EMIF_CTLCFG_DENALI_PHY_628 Register (Offset = 49D0h) [reset = 0h]

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Table 14-23874. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9D0h**

Figure 14-7923. EMIF_CTLCFG_DENALI_PHY_628 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ7_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ6_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23876. EMIF_CTLCFG_DENALI_PHY_628 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ7 for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQ6 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1311 EMIF_CTLCFG_DENALI_PHY_629 Register

1 EMIF_CTLCFG_DENALI_PHY_629 Register (Offset = 49D4h) [reset = 0h]

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Table 14-23877. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9D4h**

Figure 14-7924. EMIF_CTLCFG_DENALI_PHY_629 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_CLK_WRDQS_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDM_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23879. EMIF_CTLCFG_DENALI_PHY_629 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DQS for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_2	R/W	0h	Write clock target delay setting for DM for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1312 EMIF_CTLCFG_DENALI_PHY_630 Register

1 EMIF_CTLCFG_DENALI_PHY_630 Register (Offset = 49D8h) [reset = 0h]

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Table 14-23880. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C9D8h

Figure 14-7925. EMIF_CTLCFG_DENALI_PHY_630 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_2	
NONE						R/W	
0h						0h	

Table 14-23882. EMIF_CTLCFG_DENALI_PHY_630 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_2	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1313 EMIF_CTLCFG_DENALI_PHY_631 Register

1 EMIF_CTLCFG_DENALI_PHY_631 Register (Offset = 49DCh) [reset = 0h]

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Table 14-23883. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9DCh**

Figure 14-7926. EMIF_CTLCFG_DENALI_PHY_631 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23885. EMIF_CTLCFG_DENALI_PHY_631 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1314 EMIF_CTLCFG_DENALI_PHY_632 Register

1 EMIF_CTLCFG_DENALI_PHY_632 Register (Offset = 49E0h) [reset = 0h]

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Table 14-23886. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9E0h**

Figure 14-7927. EMIF_CTLCFG_DENALI_PHY_632 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23888. EMIF_CTLCFG_DENALI_PHY_632 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1315 EMIF_CTLCFG_DENALI_PHY_633 Register

1 EMIF_CTLCFG_DENALI_PHY_633 Register (Offset = 49E4h) [reset = 0h]

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Table 14-23889. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 C9E4h

Figure 14-7928. EMIF_CTLCFG_DENALI_PHY_633 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23891. EMIF_CTLCFG_DENALI_PHY_633 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1316 EMIF_CTLCFG_DENALI_PHY_634 Register

1 EMIF_CTLCFG_DENALI_PHY_634 Register (Offset = 49E8h) [reset = 0h]

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Table 14-23892. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9E8h**

Figure 14-7929. EMIF_CTLCFG_DENALI_PHY_634 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23894. EMIF_CTLCFG_DENALI_PHY_634 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1317 EMIF_CTLCFG_DENALI_PHY_635 Register

1 EMIF_CTLCFG_DENALI_PHY_635 Register (Offset = 49ECh) [reset = 0h]

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Table 14-23895. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9ECh**

Figure 14-7930. EMIF_CTLCFG_DENALI_PHY_635 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23897. EMIF_CTLCFG_DENALI_PHY_635 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1318 EMIF_CTLCFG_DENALI_PHY_636 Register

1 EMIF_CTLCFG_DENALI_PHY_636 Register (Offset = 49F0h) [reset = 0h]

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Table 14-23898. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9F0h**

Figure 14-7931. EMIF_CTLCFG_DENALI_PHY_636 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23900. EMIF_CTLCFG_DENALI_PHY_636 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1319 EMIF_CTLCFG_DENALI_PHY_637 Register

1 EMIF_CTLCFG_DENALI_PHY_637 Register (Offset = 49F4h) [reset = 0h]

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Table 14-23901. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9F4h**

Figure 14-7932. EMIF_CTLCFG_DENALI_PHY_637 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23903. EMIF_CTLCFG_DENALI_PHY_637 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1320 EMIF_CTLCFG_DENALI_PHY_638 Register

1 EMIF_CTLCFG_DENALI_PHY_638 Register (Offset = 49F8h) [reset = 0h]

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Table 14-23904. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9F8h**

Figure 14-7933. EMIF_CTLCFG_DENALI_PHY_638 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DM_RISE_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23906. EMIF_CTLCFG_DENALI_PHY_638 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS target delay setting for DM for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1321 EMIF_CTLCFG_DENALI_PHY_639 Register

1 EMIF_CTLCFG_DENALI_PHY_639 Register (Offset = 49FCh) [reset = 0h]

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Table 14-23907. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 C9FCh**

Figure 14-7934. EMIF_CTLCFG_DENALI_PHY_639 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_2							
R/W							
0h							

Table 14-23909. EMIF_CTLCFG_DENALI_PHY_639 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_2	R/W	0h	Read DQS target delay setting for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS target delay setting for DM for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1322 EMIF_CTLCFG_DENALI_PHY_640 Register

1 EMIF_CTLCFG_DENALI_PHY_640 Register (Offset = 4A00h) [reset = 0h]

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Table 14-23910. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CA00h

Figure 14-7935. EMIF_CTLCFG_DENALI_PHY_640 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DELAY_EARLY_THRESHOLD_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRITE_PATH_LAT_ADD_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_LATENCY_ADJUST_2			
NONE				R/W			
0h				0h			

Table 14-23912. EMIF_CTLCFG_DENALI_PHY_640 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_2	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_2	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1323 EMIF_CTLCFG_DENALI_PHY_641 Register

1 EMIF_CTLCFG_DENALI_PHY_641 Register (Offset = 4A04h) [reset = 0h]

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Table 14-23913. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA04h**

Figure 14-7936. EMIF_CTLCFG_DENALI_PHY_641 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_EARLY_FORCE_ZERO_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2							
R/W							
0h							

Table 14-23915. EMIF_CTLCFG_DENALI_PHY_641 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_2	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1324 EMIF_CTLCFG_DENALI_PHY_642 Register

1 EMIF_CTLCFG_DENALI_PHY_642 Register (Offset = 4A08h) [reset = 0h]

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Table 14-23916. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA08h**

Figure 14-7937. EMIF_CTLCFG_DENALI_PHY_642 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_GTLVL_LAT_ADJ_START_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_RDDQS_SLV_DLY_START_2							
R/W							
0h							

Table 14-23918. EMIF_CTLCFG_DENALI_PHY_642 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_2	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_2	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1325 EMIF_CTLCFG_DENALI_PHY_643 Register

1 EMIF_CTLCFG_DENALI_PHY_643 Register (Offset = 4A0Ch) [reset = 0h]

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Table 14-23919. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA0Ch**

Figure 14-7938. EMIF_CTLCFG_DENALI_PHY_643 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_NTP_PASS_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_NTP_WRLAT_START_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WDQLVL_DQDM_SLV_DLY_START_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DQDM_SLV_DLY_START_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23921. EMIF_CTLCFG_DENALI_PHY_643 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_2	R/W	0h	Indicates if No-topology training found a passing result for slice 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_2	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_2	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1326 EMIF_CTLCFG_DENALI_PHY_644 Register

1 EMIF_CTLCFG_DENALI_PHY_644 Register (Offset = 4A10h) [reset = 0h]

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Table 14-23922. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CA10h

Figure 14-7939. EMIF_CTLCFG_DENALI_PHY_644 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2							
R/W							
0h							

Table 14-23924. EMIF_CTLCFG_DENALI_PHY_644 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1327 EMIF_CTLCFG_DENALI_PHY_645 Register

1 EMIF_CTLCFG_DENALI_PHY_645 Register (Offset = 4A14h) [reset = 20202020h]

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Table 14-23925. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA14h**

Figure 14-7940. EMIF_CTLCFG_DENALI_PHY_645 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_2							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ1_CLK_ADJUST_2							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DATA_DC_DQ0_CLK_ADJUST_2							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQS_CLK_ADJUST_2							
R/W							
20h							

Table 14-23927. EMIF_CTLCFG_DENALI_PHY_645 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ2_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ1_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ0_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQS_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1328 EMIF_CTLCFG_DENALI_PHY_646 Register

1 EMIF_CTLCFG_DENALI_PHY_646 Register (Offset = 4A18h) [reset = 20202020h]

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Table 14-23928. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CA18h

Figure 14-7941. EMIF_CTLCFG_DENALI_PHY_646 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ6_CLK_ADJUST_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ5_CLK_ADJUST_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ4_CLK_ADJUST_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_DC_DQ3_CLK_ADJUST_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-23930. EMIF_CTLCFG_DENALI_PHY_646 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ6_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ5_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ4_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ3_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1329 EMIF_CTLCFG_DENALI_PHY_647 Register

1 EMIF_CTLCFG_DENALI_PHY_647 Register (Offset = 4A1Ch) [reset = 2020h]

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Table 14-23931. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA1Ch**

Figure 14-7942. EMIF_CTLCFG_DENALI_PHY_647 Name Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_2							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_2							
R/W							
20h							

Table 14-23933. EMIF_CTLCFG_DENALI_PHY_647 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_DSLICE_PAD_BOOSTPN_SETTING_2	R/W	0h	Setting for boost P/N of pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DM_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ7_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1330 EMIF_CTLCFG_DENALI_PHY_648 Register

1 EMIF_CTLCFG_DENALI_PHY_648 Register (Offset = 4A20h) [reset = 0h]

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Table 14-23934. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CA20h**

Figure 14-7943. EMIF_CTLCFG_DENALI_PHY_648 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTLE_SETTING_2					
NONE		R/W					
0h		0h					

Table 14-23936. EMIF_CTLCFG_DENALI_PHY_648 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DQS_FFE_2	R/W	0h	TX_FFE setting for DQS pad for slice 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DQ_FFE_2	R/W	0h	TX_FFE setting for DQ/DM pad for slice 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DSLICE_PAD_RX_CTLE_SETTING_2	R/W	0h	Setting for RX ctle P/N of pad for slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1331 EMIF_CTLCFG_DENALI_PHY_768 Register

1 EMIF_CTLCFG_DENALI_PHY_768 Register (Offset = 4C00h) [reset = 0h]

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Table 14-23937. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC00h**

Figure 14-7944. EMIF_CTLCFG_DENALI_PHY_768 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WR_BYPASS_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_3						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_3		
NONE					R/W		
0h					0h		

Table 14-23939. EMIF_CTLCFG_DENALI_PHY_768 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_3	R/W	0h	Write data clock bypass mode target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_3	R/W	0h	Controls PCLK/PARK pin for pad for slice 3 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_3	R/W	0h	RX_PCLK boot clock frequency selection for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1332 EMIF_CTLCFG_DENALI_PHY_769 Register

1 EMIF_CTLCFG_DENALI_PHY_769 Register (Offset = 4C04h) [reset = 0h]

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Table 14-23940. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC04h**

Figure 14-7945. EMIF_CTLCFG_DENALI_PHY_769 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_3			
NONE				R/W			
0h				0h			

Table 14-23942. EMIF_CTLCFG_DENALI_PHY_769 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_3	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3	R/W	0h	Write DQS bypass mode target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_3	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1333 EMIF_CTLCFG_DENALI_PHY_770 Register

1 EMIF_CTLCFG_DENALI_PHY_770 Register (Offset = 4C08h) [reset = 0h]

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Table 14-23943. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC08h**

Figure 14-7946. EMIF_CTLCFG_DENALI_PHY_770 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3							
R/W							
0h							

Table 14-23945. EMIF_CTLCFG_DENALI_PHY_770 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_3	R/W	0h	Bypass mode override setting for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_3	R/W	0h	Two_cycle_preamble for bypass mode for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3	R/W	0h	Read DQS bypass mode target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1334 EMIF_CTLCFG_DENALI_PHY_771 Register

1 EMIF_CTLCFG_DENALI_PHY_771 Register (Offset = 4C0Ch) [reset = 0h]

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Table 14-23946. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC0Ch**

Figure 14-7947. EMIF_CTLCFG_DENALI_PHY_771 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_3					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_3					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_3					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_3					
NONE		R/W					
0h		0h					

Table 14-23948. EMIF_CTLCFG_DENALI_PHY_771 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23948. EMIF_CTLCFG_DENALI_PHY_771 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1335 EMIF_CTLCFG_DENALI_PHY_772 Register

1 EMIF_CTLCFG_DENALI_PHY_772 Register (Offset = 4C10h) [reset = 0h]

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Table 14-23949. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC10h**

Figure 14-7948. EMIF_CTLCFG_DENALI_PHY_772 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_3					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ6_SHIFT_3					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ5_SHIFT_3					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ4_SHIFT_3					
NONE		R/W					
0h		0h					

Table 14-23951. EMIF_CTLCFG_DENALI_PHY_772 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23951. EMIF_CTLCFG_DENALI_PHY_772 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1336 EMIF_CTLCFG_DENALI_PHY_773 Register

1 EMIF_CTLCFG_DENALI_PHY_773 Register (Offset = 4C14h) [reset = 1000000h]

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Table 14-23952. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC14h**

Figure 14-7949. EMIF_CTLCFG_DENALI_PHY_773 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PER_CS_TRAINING_MULTICAST_EN_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PER_RANK_CS_MAP_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_SW_WRDQS_SHIFT_3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_SW_WRDM_SHIFT_3</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-23954. EMIF_CTLCFG_DENALI_PHY_773 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_PER_CS_TRAINING_MULTICAST_EN_3	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 3. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_PER_RANK_CS_MAP_3	R/W	0h	Per-rank CS map for slice 3. Setting a bit uses that CS for the rank, bit [0] uses CS0, bit [1] uses CS1, etc. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-23954. EMIF_CTLCFG_DENALI_PHY_773 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 3. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1337 EMIF_CTLCFG_DENALI_PHY_774 Register

1 EMIF_CTLCFG_DENALI_PHY_774 Register (Offset = 4C18h) [reset = 0h]

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Table 14-23955. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC18h**

Figure 14-7950. EMIF_CTLCFG_DENALI_PHY_774 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_LP4_BOOT_RDDATA_EN_DLY_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_PER_CS_TRAINING_INDEX_3
NONE							R/W
0h							0h

Table 14-23957. EMIF_CTLCFG_DENALI_PHY_774 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 3. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_LP4_BOOT_RDDATA_EN_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_INDEX_3	R/W	0h	For per-rank training, indicates which rank's paramters are read/ written for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1338 EMIF_CTLCFG_DENALI_PHY_775 Register

1 EMIF_CTLCFG_DENALI_PHY_775 Register (Offset = 4C1Ch) [reset = 0h]

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Table 14-23958. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC1Ch**

Figure 14-7951. EMIF_CTLCFG_DENALI_PHY_775 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_3			
NONE				R/W			
0h				0h			

Table 14-23960. EMIF_CTLCFG_DENALI_PHY_775 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_3	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 3. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_LP4_BOOT_RPTR_UPDATE_3	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1339 EMIF_CTLCFG_DENALI_PHY_776 Register

1 EMIF_CTLCFG_DENALI_PHY_776 Register (Offset = 4C20h) [reset = 0h]

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Table 14-23961. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC20h**

Figure 14-7952. EMIF_CTLCFG_DENALI_PHY_776 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_LPBK_CONTROL_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_LPBK_CONTROL_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_CTRL_LPBK_EN_3	
NONE						R/W	
0h						0h	

Table 14-23963. EMIF_CTLCFG_DENALI_PHY_776 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LPBK_DFX_TIMEOUT_EN_3	R/W	0h	Loopback read only test timeout mechanism enable for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_LPBK_CONTROL_3	R/W	0h	Loopback control bits for slice 3. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CTRL_LPBK_EN_3	R/W	0h	Loopback control en for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1340 EMIF_CTLCFG_DENALI_PHY_777 Register

1 EMIF_CTLCFG_DENALI_PHY_777 Register (Offset = 4C24h) [reset = 0h]

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Table 14-23964. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 CC24h**

Figure 14-7953. EMIF_CTLCFG_DENALI_PHY_777 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_GATE_DELAY_COMP_DISABLE_3
NONE							R/W
0h							0h

Table 14-23966. EMIF_CTLCFG_DENALI_PHY_777 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_GATE_DELAY_COMP_DISABLE_3	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1341 EMIF_CTLCFG_DENALI_PHY_778 Register

1 EMIF_CTLCFG_DENALI_PHY_778 Register (Offset = 4C28h) [reset = 0h]

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Table 14-23967. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC28h**

Figure 14-7954. EMIF_CTLCFG_DENALI_PHY_778 Name Register

31	30	29	28	27	26	25	24
PHY_AUTO_TIMING_MARGIN_CONTROL_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_AUTO_TIMING_MARGIN_CONTROL_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_AUTO_TIMING_MARGIN_CONTROL_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_3							
R/W							
0h							

Table 14-23969. EMIF_CTLCFG_DENALI_PHY_778 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_3	R/W	0h	Auto timing marging control bits for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1342 EMIF_CTLCFG_DENALI_PHY_779 Register

1 EMIF_CTLCFG_DENALI_PHY_779 Register (Offset = 4C2Ch) [reset = 0h]

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Table 14-23970. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC2Ch

Figure 14-7955. EMIF_CTLCFG_DENALI_PHY_779 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_3			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_OBS_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_OBS_3							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_OBS_3							
R							
0h							

Table 14-23972. EMIF_CTLCFG_DENALI_PHY_779 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_3	R	0h	Observation register for the auto_timing_margin for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1343 EMIF_CTLCFG_DENALI_PHY_780 Register

1 EMIF_CTLCFG_DENALI_PHY_780 Register (Offset = 4C30h) [reset = 1000000h]

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Table 14-23973. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC30h**

Figure 14-7956. EMIF_CTLCFG_DENALI_PHY_780 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_3						
NONE	R/W						
0h	1h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PDA_MODE_EN_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DQ_IDLE_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_IDLE_3							
R/W							
0h							

Table 14-23975. EMIF_CTLCFG_DENALI_PHY_780 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_3	R/W	1h	PRBS7 start pattern for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_3	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_3	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1344 EMIF_CTLCFG_DENALI_PHY_781 Register

1 EMIF_CTLCFG_DENALI_PHY_781 Register (Offset = 4C34h) [reset = 0h]

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Table 14-23976. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC34h**

Figure 14-7957. EMIF_CTLCFG_DENALI_PHY_781 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTI_PATT_RST_DISABLE_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_RDLVL_MULTI_PATT_ENABLE_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_PRBS_PATTERN_MASK_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PRBS_PATTERN_MASK_3							
R/W							
0h							

Table 14-23978. EMIF_CTLCFG_DENALI_PHY_781 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_3	R/W	0h	Read Leveling read level windows disable reset for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_3	R/W	0h	Read Leveling Multi-pattern enable for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_3	R/W	0h	PRBS7 mask signal for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1345 EMIF_CTLCFG_DENALI_PHY_782 Register

1 EMIF_CTLCFG_DENALI_PHY_782 Register (Offset = 4C38h) [reset = 0h]

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Table 14-23979. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC38h**

Figure 14-7958. EMIF_CTLCFG_DENALI_PHY_782 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_TRAIN_OBS_3</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_VREF_INITIAL_STEPSIZE_3</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-23981. EMIF_CTLCFG_DENALI_PHY_782 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_3	R	0h	Observation register for best vref value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_3	R/W	0h	Data slice initial VREF training step size for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1346 EMIF_CTLCFG_DENALI_PHY_783 Register

1 EMIF_CTLCFG_DENALI_PHY_783 Register (Offset = 4C3Ch) [reset = 0h]

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Table 14-23982. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC3Ch**

Figure 14-7959. EMIF_CTLCFG_DENALI_PHY_783 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_3
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_GATE_SMPL1_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_SNAP_OBS_REGS_3
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_3			
NONE				R/W			
0h				0h			

Table 14-23984. EMIF_CTLCFG_DENALI_PHY_783 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_3	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_3	W	0h	Initiates a snapshot of the internal observation registers for slice 3. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_3	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1347 EMIF_CTLCFG_DENALI_PHY_784 Register

1 EMIF_CTLCFG_DENALI_PHY_784 Register (Offset = 4C40h) [reset = 0h]

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Table 14-23985. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC40h**

Figure 14-7960. EMIF_CTLCFG_DENALI_PHY_784 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_3
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_MEM_CLASS_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							PHY_LPDDR_3
NONE							R/W
0h							0h

Table 14-23987. EMIF_CTLCFG_DENALI_PHY_784 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_3	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_3	R/W	0h	Indicates the type of DRAM for slice 3. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_3	R/W	0h	Adds a cycle of delay for the slice 3 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.6.6.2.1348 EMIF_CTLCFG_DENALI_PHY_785 Register

1 EMIF_CTLCFG_DENALI_PHY_785 Register (Offset = 4C44h) [reset = 0h]

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Table 14-23988. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC44h

Figure 14-7961. EMIF_CTLCFG_DENALI_PHY_785 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ON_FLY_GATE_ADJUST_EN_3	
NONE						R/W	
0h						0h	

Table 14-23990. EMIF_CTLCFG_DENALI_PHY_785 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_3	R/W	0h	Control the on-the-fly gate adjustment for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1349 EMIF_CTLCFG_DENALI_PHY_786 Register

1 EMIF_CTLCFG_DENALI_PHY_786 Register (Offset = 4C48h) [reset = 0h]

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Table 14-23991. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC48h**

Figure 14-7962. EMIF_CTLCFG_DENALI_PHY_786 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_3							
R							
0h							

Table 14-23993. EMIF_CTLCFG_DENALI_PHY_786 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_3	R	0h	Report the on-the-fly gate measurement result for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1350 EMIF_CTLCFG_DENALI_PHY_787 Register

1 EMIF_CTLCFG_DENALI_PHY_787 Register (Offset = 4C4Ch) [reset = 0h]

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Table 14-23994. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC4Ch**

Figure 14-7963. EMIF_CTLCFG_DENALI_PHY_787 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_3
NONE							R/W
0h							0h

Table 14-23996. EMIF_CTLCFG_DENALI_PHY_787 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	PHY_LP4_PST_AMBLE_3	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DFI40_POLARITY_3	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1351 EMIF_CTLCFG_DENALI_PHY_788 Register

1 EMIF_CTLCFG_DENALI_PHY_788 Register (Offset = 4C50h) [reset = 0h]

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Table 14-23997. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC50h

Figure 14-7964. EMIF_CTLCFG_DENALI_PHY_788 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_3							
R/W							
0h							

Table 14-23999. EMIF_CTLCFG_DENALI_PHY_788 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_3	R/W	0h	Read leveling pattern 8 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1352 EMIF_CTLCFG_DENALI_PHY_789 Register

1 EMIF_CTLCFG_DENALI_PHY_789 Register (Offset = 4C54h) [reset = 0h]

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Table 14-24000. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC54h**

Figure 14-7965. EMIF_CTLCFG_DENALI_PHY_789 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT9_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT9_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_3							
R/W							
0h							

Table 14-24002. EMIF_CTLCFG_DENALI_PHY_789 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_3	R/W	0h	Read leveling pattern 9 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1353 EMIF_CTLCFG_DENALI_PHY_790 Register

1 EMIF_CTLCFG_DENALI_PHY_790 Register (Offset = 4C58h) [reset = 0h]

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Table 14-24003. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC58h**

Figure 14-7966. EMIF_CTLCFG_DENALI_PHY_790 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_PATT10_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_PATT10_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_PATT10_3							
R/W							
0h							

Table 14-24005. EMIF_CTLCFG_DENALI_PHY_790 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_3	R/W	0h	Read leveling pattern 10 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1354 EMIF_CTLCFG_DENALI_PHY_791 Register

1 EMIF_CTLCFG_DENALI_PHY_791 Register (Offset = 4C5Ch) [reset = 0h]

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Table 14-24006. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC5Ch

Figure 14-7967. EMIF_CTLCFG_DENALI_PHY_791 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_3							
R/W							
0h							

Table 14-24008. EMIF_CTLCFG_DENALI_PHY_791 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_3	R/W	0h	Read leveling pattern 11 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1355 EMIF_CTLCFG_DENALI_PHY_792 Register

1 EMIF_CTLCFG_DENALI_PHY_792 Register (Offset = 4C60h) [reset = 0h]

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Table 14-24009. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC60h**

Figure 14-7968. EMIF_CTLCFG_DENALI_PHY_792 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_3							
R/W							
0h							

Table 14-24011. EMIF_CTLCFG_DENALI_PHY_792 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_3	R/W	0h	Read leveling pattern 12 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1356 EMIF_CTLCFG_DENALI_PHY_793 Register

1 EMIF_CTLCFG_DENALI_PHY_793 Register (Offset = 4C64h) [reset = 0h]

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Table 14-24012. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC64h**

Figure 14-7969. EMIF_CTLCFG_DENALI_PHY_793 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_PATT13_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_PATT13_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_PATT13_3							
R/W							
0h							

Table 14-24014. EMIF_CTLCFG_DENALI_PHY_793 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_3	R/W	0h	Read leveling pattern 13 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1357 EMIF_CTLCFG_DENALI_PHY_794 Register

1 EMIF_CTLCFG_DENALI_PHY_794 Register (Offset = 4C68h) [reset = 0h]

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Table 14-24015. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC68h**

Figure 14-7970. EMIF_CTLCFG_DENALI_PHY_794 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_3							
R/W							
0h							

Table 14-24017. EMIF_CTLCFG_DENALI_PHY_794 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_3	R/W	0h	Read leveling pattern 14 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1358 EMIF_CTLCFG_DENALI_PHY_795 Register

1 EMIF_CTLCFG_DENALI_PHY_795 Register (Offset = 4C6Ch) [reset = 0h]

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Table 14-24018. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC6Ch**

Figure 14-7971. EMIF_CTLCFG_DENALI_PHY_795 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_3							
R/W							
0h							

Table 14-24020. EMIF_CTLCFG_DENALI_PHY_795 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_3	R/W	0h	Read leveling pattern 15 data for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1359 EMIF_CTLCFG_DENALI_PHY_796 Register

1 EMIF_CTLCFG_DENALI_PHY_796 Register (Offset = 4C70h) [reset = 0h]

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Table 14-24021. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC70h**

Figure 14-7972. EMIF_CTLCFG_DENALI_PHY_796 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_3		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED				PHY_MASTER_DLY_LOCK_OBS_SELECT_3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_3
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_3		
NONE					R/W		
0h					0h		

Table 14-24023. EMIF_CTLCFG_DENALI_PHY_796 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_3	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_3	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 3. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_3	R/W	0h	Reserved for future use for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1360 EMIF_CTLCFG_DENALI_PHY_797 Register

1 EMIF_CTLCFG_DENALI_PHY_797 Register (Offset = 4C74h) [reset = 0h]

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Table 14-24024. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC74h**

Figure 14-7973. EMIF_CTLCFG_DENALI_PHY_797 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_3			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WR_SHIFT_OBS_SELECT_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_WR_ENC_OBS_SELECT_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_3			
NONE				R/W			
0h				0h			

Table 14-24026. EMIF_CTLCFG_DENALI_PHY_797 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_3	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_3	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 3. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1361 EMIF_CTLCFG_DENALI_PHY_798 Register

1 EMIF_CTLCFG_DENALI_PHY_798 Register (Offset = 4C78h) [reset = 0h]

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Table 14-24027. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC78h**

Figure 14-7974. EMIF_CTLCFG_DENALI_PHY_798 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_3					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_3	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_3
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_3
NONE							R/W
0h							0h

Table 14-24029. EMIF_CTLCFG_DENALI_PHY_798 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_3	R/W	0h	Write leveling algorithm selection for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_3	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 3. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_3	R/W	0h	Enables leveling debug mode for slice 3. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1362 EMIF_CTLCFG_DENALI_PHY_799 Register

1 EMIF_CTLCFG_DENALI_PHY_799 Register (Offset = 4C7Ch) [reset = 0h]

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Table 14-24030. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC7Ch**

Figure 14-7975. EMIF_CTLCFG_DENALI_PHY_799 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_3			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_GTLVL_CAPTURE_CNT_3					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_MASK_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_3			
NONE				R/W			
0h				0h			

Table 14-24032. EMIF_CTLCFG_DENALI_PHY_799 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 3. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_3	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1363 EMIF_CTLCFG_DENALI_PHY_800 Register

1 EMIF_CTLCFG_DENALI_PHY_800 Register (Offset = 4C80h) [reset = 0h]

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Table 14-24033. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC80h**

Figure 14-7976. EMIF_CTLCFG_DENALI_PHY_800 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RDLVL_RDDQS_DQ_OBS_SELECT_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDLVL_OP_MODE_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_RDLVL_CAPTURE_CNT_3					
NONE		R/W					
0h		0h					

Table 14-24035. EMIF_CTLCFG_DENALI_PHY_800 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_3	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_3	R/W	0h	Read leveling algorithm select for slice 3. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 3. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1364 EMIF_CTLCFG_DENALI_PHY_801 Register

1 EMIF_CTLCFG_DENALI_PHY_801 Register (Offset = 4C84h) [reset = 0h]

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Table 14-24036. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC84h**

Figure 14-7977. EMIF_CTLCFG_DENALI_PHY_801 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_DATA_SWIZZLE_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_DATA_SWIZZLE_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_DATA_MASK_3							
R/W							
0h							

Table 14-24038. EMIF_CTLCFG_DENALI_PHY_801 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_3	R/W	0h	Read level bit swizzling for DDR4 operation for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_3	R/W	0h	Per-bit mask for read leveling for slice 3. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1365 EMIF_CTLCFG_DENALI_PHY_802 Register

1 EMIF_CTLCFG_DENALI_PHY_802 Register (Offset = 4C88h) [reset = 0h]

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Table 14-24039. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC88h

Figure 14-7978. EMIF_CTLCFG_DENALI_PHY_802 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_WDQLVL_PATT_3		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_WDQLVL_BURST_CNT_3					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_CLK_JITTER_TOLERANCE_3							
R/W							
0h							

Table 14-24041. EMIF_CTLCFG_DENALI_PHY_802 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_3	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 3. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_3	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_3	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1366 EMIF_CTLCFG_DENALI_PHY_803 Register

1 EMIF_CTLCFG_DENALI_PHY_803 Register (Offset = 4C8Ch) [reset = 0h]

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Table 14-24042. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 CC8Ch**

Figure 14-7979. EMIF_CTLCFG_DENALI_PHY_803 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_3			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3							
R/W							
0h							

Table 14-24044. EMIF_CTLCFG_DENALI_PHY_803 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_3	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1367 EMIF_CTLCFG_DENALI_PHY_804 Register

1 EMIF_CTLCFG_DENALI_PHY_804 Register (Offset = 4C90h) [reset = 0h]

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Table 14-24045. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC90h**

Figure 14-7980. EMIF_CTLCFG_DENALI_PHY_804 Name Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_WDQLVL_CLR_PREV_RESULTS_3
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_DM_DLY_STEP_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DQ_SLV_DELTA_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_SELECT_3							
R/W							
0h							

Table 14-24047. EMIF_CTLCFG_DENALI_PHY_804 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_3	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 3. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_3	R/W	0h	The target delay line step for DM training for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_3	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_3	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1368 EMIF_CTLCFG_DENALI_PHY_805 Register

1 EMIF_CTLCFG_DENALI_PHY_805 Register (Offset = 4C94h) [reset = 0h]

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Table 14-24048. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC94h**

Figure 14-7981. EMIF_CTLCFG_DENALI_PHY_805 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_WDQLVL_DATADM_MASK_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WDQLVL_DATADM_MASK_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24050. EMIF_CTLCFG_DENALI_PHY_805 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_3	R/W	0h	Per-bit mask for write data leveling for slice 3. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1369 EMIF_CTLCFG_DENALI_PHY_806 Register

1 EMIF_CTLCFG_DENALI_PHY_806 Register (Offset = 4C98h) [reset = 0h]

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Table 14-24051. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CC98h

Figure 14-7982. EMIF_CTLCFG_DENALI_PHY_806 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT0_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT0_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT0_3							
R/W							
0h							

Table 14-24053. EMIF_CTLCFG_DENALI_PHY_806 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1370 EMIF_CTLCFG_DENALI_PHY_807 Register

1 EMIF_CTLCFG_DENALI_PHY_807 Register (Offset = 4C9Ch) [reset = 0h]

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Table 14-24054. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CC9Ch**

Figure 14-7983. EMIF_CTLCFG_DENALI_PHY_807 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_USER_PATT1_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT1_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT1_3							
R/W							
0h							

Table 14-24056. EMIF_CTLCFG_DENALI_PHY_807 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1371 EMIF_CTLCFG_DENALI_PHY_808 Register

1 EMIF_CTLCFG_DENALI_PHY_808 Register (Offset = 4CA0h) [reset = 0h]

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Table 14-24057. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCA0h**

Figure 14-7984. EMIF_CTLCFG_DENALI_PHY_808 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT2_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT2_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT2_3							
R/W							
0h							

Table 14-24059. EMIF_CTLCFG_DENALI_PHY_808 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1372 EMIF_CTLCFG_DENALI_PHY_809 Register

1 EMIF_CTLCFG_DENALI_PHY_809 Register (Offset = 4CA4h) [reset = 0h]

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Table 14-24060. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCA4h

Figure 14-7985. EMIF_CTLCFG_DENALI_PHY_809 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT3_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT3_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT3_3							
R/W							
0h							

Table 14-24062. EMIF_CTLCFG_DENALI_PHY_809 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1373 EMIF_CTLCFG_DENALI_PHY_810 Register

1 EMIF_CTLCFG_DENALI_PHY_810 Register (Offset = 4CA8h) [reset = 0h]

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Table 14-24063. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCA8h

Figure 14-7986. EMIF_CTLCFG_DENALI_PHY_810 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_NTP_MULT_TRAIN_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_USER_PATT4_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_USER_PATT4_3							
R/W							
0h							

Table 14-24065. EMIF_CTLCFG_DENALI_PHY_810 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_3	R/W	0h	Control for single pass only No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1374 EMIF_CTLCFG_DENALI_PHY_811 Register

1 EMIF_CTLCFG_DENALI_PHY_811 Register (Offset = 4CACh) [reset = 0h]

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Table 14-24066. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCACh

Figure 14-7987. EMIF_CTLCFG_DENALI_PHY_811 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_PERIOD_THRESHOLD_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_NTP_EARLY_THRESHOLD_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_EARLY_THRESHOLD_3							
R/W							
0h							

Table 14-24068. EMIF_CTLCFG_DENALI_PHY_811 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_3	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_3	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1375 EMIF_CTLCFG_DENALI_PHY_812 Register

1 EMIF_CTLCFG_DENALI_PHY_812 Register (Offset = 4CB0h) [reset = 0h]

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Table 14-24069. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCB0h**

Figure 14-7988. EMIF_CTLCFG_DENALI_PHY_812 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_MAX_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_PERIOD_THRESHOLD_MIN_3							
R/W							
0h							

Table 14-24071. EMIF_CTLCFG_DENALI_PHY_812 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_3	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_3	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1376 EMIF_CTLCFG_DENALI_PHY_813 Register

1 EMIF_CTLCFG_DENALI_PHY_813 Register (Offset = 4CB4h) [reset = 0h]

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Table 14-24072. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCB4h**

Figure 14-7989. EMIF_CTLCFG_DENALI_PHY_813 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_3					
NONE		W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_3
NONE							R/W
0h							0h

Table 14-24074. EMIF_CTLCFG_DENALI_PHY_813 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_3	R	0h	Observation register containing read entry FIFO pointers for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_3	W	0h	Manual reset/clear of internal logic for slice 3. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_3	R/W	0h	Indicates if slice 3 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1377 EMIF_CTLCFG_DENALI_PHY_814 Register

1 EMIF_CTLCFG_DENALI_PHY_814 Register (Offset = 4CB8h) [reset = 100000h]

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Table 14-24075. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCB8h

Figure 14-7990. EMIF_CTLCFG_DENALI_PHY_814 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_3							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_3							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_3							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_3							
R							
100000h							

Table 14-24077. EMIF_CTLCFG_DENALI_PHY_814 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_3	R	100000h	Observation register containing loopback status/results for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1378 EMIF_CTLCFG_DENALI_PHY_815 Register

1 EMIF_CTLCFG_DENALI_PHY_815 Register (Offset = 4CBCh) [reset = 0h]

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Table 14-24078. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCBCh**

Figure 14-7991. EMIF_CTLCFG_DENALI_PHY_815 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MASTER_DLY_LOCK_OBS_3		
NONE					R		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MASTER_DLY_LOCK_OBS_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_LPBK_ERROR_COUNT_OBS_3							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_LPBK_ERROR_COUNT_OBS_3							
R							
0h							

Table 14-24080. EMIF_CTLCFG_DENALI_PHY_815 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_3	R	0h	Observation register containing controller delay results for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_3	R	0h	Observation register containing total number of loopback error data for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1379 EMIF_CTLCFG_DENALI_PHY_816 Register

1 EMIF_CTLCFG_DENALI_PHY_816 Register (Offset = 4CC0h) [reset = 0h]

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Table 14-24081. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCC0h**

Figure 14-7992. EMIF_CTLCFG_DENALI_PHY_816 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MEAS_DLY_STEP_VALUE_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_3						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_3						
NONE	R						
0h	0h						

Table 14-24083. EMIF_CTLCFG_DENALI_PHY_816 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_3	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS base target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQ target delay encoded values for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1380 EMIF_CTLCFG_DENALI_PHY_817 Register

1 EMIF_CTLCFG_DENALI_PHY_817 Register (Offset = 4CC4h) [reset = 0h]

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Table 14-24084. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCC4h

Figure 14-7993. EMIF_CTLCFG_DENALI_PHY_817 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_3						
NONE	R						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3		
NONE					R		
0h					0h		

15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3							
R							
0h							

7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_3							
R							
0h							

Table 14-24086. EMIF_CTLCFG_DENALI_PHY_817 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write DQS base target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS gate target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1381 EMIF_CTLCFG_DENALI_PHY_818 Register

1 EMIF_CTLCFG_DENALI_PHY_818 Register (Offset = 4CC8h) [reset = 0h]

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Table 14-24087. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCC8h**

Figure 14-7994. EMIF_CTLCFG_DENALI_PHY_818 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_3		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_3							
R							
0h							

Table 14-24089. EMIF_CTLCFG_DENALI_PHY_818 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_3	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write adder target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write DQ base target delay encoded value for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1382 EMIF_CTLCFG_DENALI_PHY_819 Register

1 EMIF_CTLCFG_DENALI_PHY_819 Register (Offset = 4CCCh) [reset = 0h]

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Table 14-24090. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCCCh

Figure 14-7995. EMIF_CTLCFG_DENALI_PHY_819 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_WRLVL_HARD1_DELAY_OBS_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_WRLVL_HARD1_DELAY_OBS_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_WRLVL_HARD0_DELAY_OBS_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WRLVL_HARD0_DELAY_OBS_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24092. EMIF_CTLCFG_DENALI_PHY_819 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_3	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_3	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1383 EMIF_CTLCFG_DENALI_PHY_820 Register

1 EMIF_CTLCFG_DENALI_PHY_820 Register (Offset = 4CD0h) [reset = 0h]

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Table 14-24093. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCD0h**

Figure 14-7996. EMIF_CTLCFG_DENALI_PHY_820 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_WRLVL_STATUS_OBS_3</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_WRLVL_STATUS_OBS_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WRLVL_STATUS_OBS_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24095. EMIF_CTLCFG_DENALI_PHY_820 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_3	R	0h	Observation register containing write leveling status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1384 EMIF_CTLCFG_DENALI_PHY_821 Register

1 EMIF_CTLCFG_DENALI_PHY_821 Register (Offset = 4CD4h) [reset = 0h]

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Table 14-24096. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCD4h

Figure 14-7997. EMIF_CTLCFG_DENALI_PHY_821 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3							
R							
0h							

Table 14-24098. EMIF_CTLCFG_DENALI_PHY_821 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing gate sample2 target delay encoded values for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing gate sample1 target delay encoded values for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1385 EMIF_CTLCFG_DENALI_PHY_822 Register

1 EMIF_CTLCFG_DENALI_PHY_822 Register (Offset = 4CD8h) [reset = 0h]

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Table 14-24099. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCD8h**

Figure 14-7998. EMIF_CTLCFG_DENALI_PHY_822 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_3					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD0_DELAY_OBS_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_ERROR_OBS_3							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_ERROR_OBS_3							
R							
0h							

Table 14-24101. EMIF_CTLCFG_DENALI_PHY_822 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD0_DELAY_OBS_3	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_WRLVL_ERROR_OBS_3	R	0h	Observation register containing write leveling error status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1386 EMIF_CTLCFG_DENALI_PHY_823 Register

1 EMIF_CTLCFG_DENALI_PHY_823 Register (Offset = 4CDCh) [reset = 0h]

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Table 14-24102. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCDCh

Figure 14-7999. EMIF_CTLCFG_DENALI_PHY_823 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_3					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_HARD1_DELAY_OBS_3							
R							
0h							

Table 14-24104. EMIF_CTLCFG_DENALI_PHY_823 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD1_DELAY_OBS_3	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1387 EMIF_CTLCFG_DENALI_PHY_824 Register

1 EMIF_CTLCFG_DENALI_PHY_824 Register (Offset = 4CE0h) [reset = 0h]

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Table 14-24105. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCE0h**

Figure 14-8000. EMIF_CTLCFG_DENALI_PHY_824 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_STATUS_OBS_3	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
PHY_GTLVL_STATUS_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_3							
R							
0h							

Table 14-24107. EMIF_CTLCFG_DENALI_PHY_824 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_3	R	0h	Observation register containing gate training status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1388 EMIF_CTLCFG_DENALI_PHY_825 Register

1 EMIF_CTLCFG_DENALI_PHY_825 Register (Offset = 4CE4h) [reset = 0h]

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Table 14-24108. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCE4h**

Figure 14-8001. EMIF_CTLCFG_DENALI_PHY_825 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3							
R							
0h							

Table 14-24110. EMIF_CTLCFG_DENALI_PHY_825 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1389 EMIF_CTLCFG_DENALI_PHY_826 Register

1 EMIF_CTLCFG_DENALI_PHY_826 Register (Offset = 4CE8h) [reset = 0h]

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Table 14-24111. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCE8h**

Figure 14-8002. EMIF_CTLCFG_DENALI_PHY_826 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3	
NONE						R	
0h						0h	

Table 14-24113. EMIF_CTLCFG_DENALI_PHY_826 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3	R	0h	Observation register containing read leveling number of windows found for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1390 EMIF_CTLCFG_DENALI_PHY_827 Register

1 EMIF_CTLCFG_DENALI_PHY_827 Register (Offset = 4CECh) [reset = 0h]

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Table 14-24114. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCECh

Figure 14-8003. EMIF_CTLCFG_DENALI_PHY_827 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_3							
R							
0h							

Table 14-24116. EMIF_CTLCFG_DENALI_PHY_827 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_3	R	0h	Observation register containing read leveling status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1391 EMIF_CTLCFG_DENALI_PHY_828 Register

1 EMIF_CTLCFG_DENALI_PHY_828 Register (Offset = 4CF0h) [reset = 7FF0000h]

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Table 14-24117. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCF0h

Figure 14-8004. EMIF_CTLCFG_DENALI_PHY_828 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_3		
NONE					R		
0h					7FFh		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DQDM_TE_DLY_OBS_3							
R							
7FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_3		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_LE_DLY_OBS_3							
R							
0h							

Table 14-24119. EMIF_CTLCFG_DENALI_PHY_828 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_3	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_3	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1392 EMIF_CTLCFG_DENALI_PHY_829 Register

1 EMIF_CTLCFG_DENALI_PHY_829 Register (Offset = 4CF4h) [reset = 0h]

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Table 14-24120. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCF4h

Figure 14-8005. EMIF_CTLCFG_DENALI_PHY_829 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_3							
R							
0h							

Table 14-24122. EMIF_CTLCFG_DENALI_PHY_829 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_3	R	0h	Observation register containing write data leveling status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1393 EMIF_CTLCFG_DENALI_PHY_830 Register

1 EMIF_CTLCFG_DENALI_PHY_830 Register (Offset = 4CF8h) [reset = 0h]

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Table 14-24123. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CCF8h

Figure 14-8006. EMIF_CTLCFG_DENALI_PHY_830 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_PERIODIC_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_3							
R							
0h							

Table 14-24125. EMIF_CTLCFG_DENALI_PHY_830 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_3	R	0h	Observation register containing periodic write data leveling status for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1394 EMIF_CTLCFG_DENALI_PHY_831 Register

1 EMIF_CTLCFG_DENALI_PHY_831 Register (Offset = 4CFCh) [reset = 0h]

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Table 14-24126. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CCFCh**

Figure 14-8007. EMIF_CTLCFG_DENALI_PHY_831 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_3						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_MODE_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_MODE_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_MODE_3							
R/W							
0h							

Table 14-24128. EMIF_CTLCFG_DENALI_PHY_831 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_3	R/W	0h	DDL mode for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1395 EMIF_CTLCFG_DENALI_PHY_832 Register

1 EMIF_CTLCFG_DENALI_PHY_832 Register (Offset = 4D00h) [reset = 0h]

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Table 14-24129. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD00h

Figure 14-8008. EMIF_CTLCFG_DENALI_PHY_832 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_MASK_3					
NONE		R/W					
0h		0h					

Table 14-24131. EMIF_CTLCFG_DENALI_PHY_832 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_3	R/W	0h	DDL mask for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1396 EMIF_CTLCFG_DENALI_PHY_833 Register

1 EMIF_CTLCFG_DENALI_PHY_833 Register (Offset = 4D04h) [reset = 0h]

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Table 14-24132. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD04h**

Figure 14-8009. EMIF_CTLCFG_DENALI_PHY_833 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_3							
R							
0h							

Table 14-24134. EMIF_CTLCFG_DENALI_PHY_833 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_3	R	0h	DDL test observation for slice 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1397 EMIF_CTLCFG_DENALI_PHY_834 Register

1 EMIF_CTLCFG_DENALI_PHY_834 Register (Offset = 4D08h) [reset = 0h]

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Table 14-24135. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD08h**

Figure 14-8010. EMIF_CTLCFG_DENALI_PHY_834 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_3							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_MSTR_DLY_OBS_3							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_MSTR_DLY_OBS_3							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_3							
R							
0h							

Table 14-24137. EMIF_CTLCFG_DENALI_PHY_834 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_3	R	0h	DDL test observation delays for slice 3 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1398 EMIF_CTLCFG_DENALI_PHY_835 Register

1 EMIF_CTLCFG_DENALI_PHY_835 Register (Offset = 4D0Ch) [reset = 0h]

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Table 14-24138. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD0Ch**

Figure 14-8011. EMIF_CTLCFG_DENALI_PHY_835 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ0_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_LP4_WDQS_OE_EXTEND_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_TRACK_UPD_THRESHOLD_3							
R/W							
0h							

Table 14-24140. EMIF_CTLCFG_DENALI_PHY_835 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_3	R/W	0h	RX Calibration codes for DQ0 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_3	R/W	0h	LPDDR4 write preamble extension enable for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_3	R/W	0h	Specify threshold value for PHY init update tracking for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1399 EMIF_CTLCFG_DENALI_PHY_836 Register

1 EMIF_CTLCFG_DENALI_PHY_836 Register (Offset = 4D10h) [reset = 0h]

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Table 14-24141. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD10h**

Figure 14-8012. EMIF_CTLCFG_DENALI_PHY_836 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_3
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ2_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ1_3
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ1_3							
R/W							
0h							

Table 14-24143. EMIF_CTLCFG_DENALI_PHY_836 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_3	R/W	0h	RX Calibration codes for DQ2 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_3	R/W	0h	RX Calibration codes for DQ1 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1400 EMIF_CTLCFG_DENALI_PHY_837 Register

1 EMIF_CTLCFG_DENALI_PHY_837 Register (Offset = 4D14h) [reset = 0h]

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Table 14-24144. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD14h**

Figure 14-8013. EMIF_CTLCFG_DENALI_PHY_837 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ4_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ4_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ3_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ3_3							
R/W							
0h							

Table 14-24146. EMIF_CTLCFG_DENALI_PHY_837 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_3	R/W	0h	RX Calibration codes for DQ4 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_3	R/W	0h	RX Calibration codes for DQ3 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1401 EMIF_CTLCFG_DENALI_PHY_838 Register

1 EMIF_CTLCFG_DENALI_PHY_838 Register (Offset = 4D18h) [reset = 0h]

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Table 14-24147. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD18h

Figure 14-8014. EMIF_CTLCFG_DENALI_PHY_838 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ6_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ5_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ5_3							
R/W							
0h							

Table 14-24149. EMIF_CTLCFG_DENALI_PHY_838 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_3	R/W	0h	RX Calibration codes for DQ6 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_3	R/W	0h	RX Calibration codes for DQ5 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1402 EMIF_CTLCFG_DENALI_PHY_839 Register

1 EMIF_CTLCFG_DENALI_PHY_839 Register (Offset = 4D1Ch) [reset = 0h]

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Table 14-24150. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD1Ch**

Figure 14-8015. EMIF_CTLCFG_DENALI_PHY_839 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ7_3
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ7_3							
R/W							
0h							

Table 14-24152. EMIF_CTLCFG_DENALI_PHY_839 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_3	R/W	0h	RX Calibration codes for DQ7 for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1403 EMIF_CTLCFG_DENALI_PHY_840 Register

1 EMIF_CTLCFG_DENALI_PHY_840 Register (Offset = 4D20h) [reset = 0h]

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Table 14-24153. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD20h**

Figure 14-8016. EMIF_CTLCFG_DENALI_PHY_840 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RX_CAL_DM_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_RX_CAL_DM_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RX_CAL_DM_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24155. EMIF_CTLCFG_DENALI_PHY_840 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_3	R/W	0h	RX Calibration codes for DM for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1404 EMIF_CTLCFG_DENALI_PHY_841 Register

1 EMIF_CTLCFG_DENALI_PHY_841 Register (Offset = 4D24h) [reset = 0h]

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Table 14-24156. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD24h**

Figure 14-8017. EMIF_CTLCFG_DENALI_PHY_841 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_FDBK_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQS_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQS_3							
R/W							
0h							

Table 14-24158. EMIF_CTLCFG_DENALI_PHY_841 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_3	R/W	0h	RX Calibration codes for FDBK for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_3	R/W	0h	RX Calibration codes for DQS for slice 3. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1405 EMIF_CTLCFG_DENALI_PHY_842 Register

1 EMIF_CTLCFG_DENALI_PHY_842 Register (Offset = 4D28h) [reset = 0h]

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Table 14-24159. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD28h**

Figure 14-8018. EMIF_CTLCFG_DENALI_PHY_842 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_CAL_SAMPLE_WAIT_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_STATIC_TOG_DISABLE_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_PAD_RX_BIAS_EN_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_RX_BIAS_EN_3							
R/W							
0h							

Table 14-24161. EMIF_CTLCFG_DENALI_PHY_842 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_CAL_SAMPLE_WAIT_3	R/W	0h	Determines number of cycles to wait for each sample for slice 3. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_3	R/W	0h	Control to disable toggle during static activity for slice 3. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_3	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1406 EMIF_CTLCFG_DENALI_PHY_843 Register

1 EMIF_CTLCFG_DENALI_PHY_843 Register (Offset = 4D2Ch) [reset = 0h]

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Table 14-24162. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD2Ch**

Figure 14-8019. EMIF_CTLCFG_DENALI_PHY_843 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DATA_DC_ADJUST_SAMPLE_CNT_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_DATA_DC_ADJUST_START_3</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DATA_DC_WEIGHT_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_DC_CAL_TIMEOUT_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24164. EMIF_CTLCFG_DENALI_PHY_843 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_ADJUST_SAMPLE_CNT_3	R/W	0h	Duty cycle adjust sample count for slice 3. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DATA_DC_ADJUST_START_3	R/W	0h	Duty cycle adjust starting value for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DATA_DC_WEIGHT_3	R/W	0h	Determines weight of average calculating for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_CAL_TIMEOUT_3	R/W	0h	Determines timeout number of iteration for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1407 EMIF_CTLCFG_DENALI_PHY_844 Register

1 EMIF_CTLCFG_DENALI_PHY_844 Register (Offset = 4D30h) [reset = 0h]

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Table 14-24165. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD30h

Figure 14-8020. EMIF_CTLCFG_DENALI_PHY_844 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_CAL_START_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_DATA_DC_CAL_POLARITY_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_ADJUST_THRSHLD_3							
R/W							
0h							

Table 14-24167. EMIF_CTLCFG_DENALI_PHY_844 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_DATA_DC_CAL_START_3	R/W	0h	Manual trigger for DCC for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DATA_DC_CAL_POLARITY_3	R/W	0h	Calibration polarity for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_ADJUST_DIRECT_3	R/W	0h	Adjust direction for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_ADJUST_THRSHLD_3	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1408 EMIF_CTLCFG_DENALI_PHY_845 Register

1 EMIF_CTLCFG_DENALI_PHY_845 Register (Offset = 4D34h) [reset = 1h]

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Table 14-24168. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD34h**

Figure 14-8021. EMIF_CTLCFG_DENALI_PHY_845 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDPATH_GATE_DISABLE_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_FDBK_PWR_CTRL_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DATA_DC_SW_RANK_3	
NONE						R/W	
0h						1h	

Table 14-24170. EMIF_CTLCFG_DENALI_PHY_845 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDPATH_GATE_DISABLE_3	R/W	0h	Data slice read path power reduction disable for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SLV_DLY_CTRL_GATE_DISABLE_3	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_FDBK_PWR_CTRL_3	R/W	0h	Shutoff gate feedback IO to reduce power for slice 3. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DATA_DC_SW_RANK_3	R/W	1h	Rank selection for software based duty cycle correction for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1409 EMIF_CTLCFG_DENALI_PHY_846 Register

1 EMIF_CTLCFG_DENALI_PHY_846 Register (Offset = 4D38h) [reset = 0h]

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Table 14-24171. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD38h**

Figure 14-8022. EMIF_CTLCFG_DENALI_PHY_846 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_3
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_3
NONE							R/W
0h							0h

Table 14-24173. EMIF_CTLCFG_DENALI_PHY_846 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_SLICE_PWR_RDC_DISABLE_3	R/W	0h	Data slice power reduction disable for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_3	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1410 EMIF_CTLCFG_DENALI_PHY_847 Register

1 EMIF_CTLCFG_DENALI_PHY_847 Register (Offset = 4D3Ch) [reset = 0h]

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Table 14-24174. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD3Ch**

Figure 14-8023. EMIF_CTLCFG_DENALI_PHY_847 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_SELECT_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_SELECT_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DQ_TSEL_ENABLE_3		
NONE					R/W		
0h					0h		

Table 14-24176. EMIF_CTLCFG_DENALI_PHY_847 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_3	R/W	0h	Operation type tsel enables for DQS signals for slice 3. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_3	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 3. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_3	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 3. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1411 EMIF_CTLCFG_DENALI_PHY_848 Register

1 EMIF_CTLCFG_DENALI_PHY_848 Register (Offset = 4D40h) [reset = 0h]

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Table 14-24177. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD40h**

Figure 14-8024. EMIF_CTLCFG_DENALI_PHY_848 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_3						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_3	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_3							
R/W							
0h							

Table 14-24179. EMIF_CTLCFG_DENALI_PHY_848 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_3	R/W	0h	Data slice initial VREF training start value for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_3	R/W	0h	2 cycle preamble support for slice 3. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_3	R/W	0h	Operation type tsel select values for DQS signals for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1412 EMIF_CTLCFG_DENALI_PHY_849 Register

1 EMIF_CTLCFG_DENALI_PHY_849 Register (Offset = 4D44h) [reset = 0h]

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Table 14-24180. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD44h

Figure 14-8025. EMIF_CTLCFG_DENALI_PHY_849 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_NTP_WDQ_STEP_SIZE_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_NTP_TRAIN_EN_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_VREF_TRAINING_CTRL_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_INITIAL_STOP_POINT_3</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-24182. EMIF_CTLCFG_DENALI_PHY_849 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_3	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_3	R/W	0h	Enable for No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_3	R/W	0h	Data slice vref training enable control for slice 3. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_3	R/W	0h	Data slice initial VREF training stop value for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1413 EMIF_CTLCFG_DENALI_PHY_850 Register

1 EMIF_CTLCFG_DENALI_PHY_850 Register (Offset = 4D48h) [reset = 0h]

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Table 14-24183. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD48h**

Figure 14-8026. EMIF_CTLCFG_DENALI_PHY_850 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_3		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_NTP_WDQ_STOP_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_NTP_WDQ_START_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_START_3							
R/W							
0h							

Table 14-24185. EMIF_CTLCFG_DENALI_PHY_850 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_3	R/W	0h	End of WR DQ target delay in No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_3	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1414 EMIF_CTLCFG_DENALI_PHY_851 Register

1 EMIF_CTLCFG_DENALI_PHY_851 Register (Offset = 4D4Ch) [reset = 0h]

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Table 14-24186. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD4Ch**

Figure 14-8027. EMIF_CTLCFG_DENALI_PHY_851 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WDQLVL_DVW_MIN_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DVW_MIN_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_BIT_EN_3							
R/W							
0h							

Table 14-24188. EMIF_CTLCFG_DENALI_PHY_851 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_3	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 3. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_3	R/W	0h	Minimum data valid window across DQs and ranks for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_3	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1415 EMIF_CTLCFG_DENALI_PHY_852 Register

1 EMIF_CTLCFG_DENALI_PHY_852 Register (Offset = 4D50h) [reset = 0h]

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Table 14-24189. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD50h

Figure 14-8028. EMIF_CTLCFG_DENALI_PHY_852 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_TX_DCD_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_FAST_LVL_EN_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_WDQLVL_PER_START_OFFSET_3					
NONE		R/W					
0h		0h					

Table 14-24191. EMIF_CTLCFG_DENALI_PHY_852 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_3	R/W	0h	Controls TX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_3	R/W	0h	Enable for fast multi-pattern window search for slice 3. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_3	R/W	0h	Peridic training start point offset for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1416 EMIF_CTLCFG_DENALI_PHY_853 Register

1 EMIF_CTLCFG_DENALI_PHY_853 Register (Offset = 4D54h) [reset = 0h]

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Table 14-24192. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD54h

Figure 14-8029. EMIF_CTLCFG_DENALI_PHY_853 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_3_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_2_3				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_1_3				
NONE			R/W				
0h			0h				

Table 14-24194. EMIF_CTLCFG_DENALI_PHY_853 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1417 EMIF_CTLCFG_DENALI_PHY_854 Register

1 EMIF_CTLCFG_DENALI_PHY_854 Register (Offset = 4D58h) [reset = 0h]

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Table 14-24195. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD58h**

Figure 14-8030. EMIF_CTLCFG_DENALI_PHY_854 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_7_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_6_3				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_5_3				
NONE			R/W				
0h			0h				

Table 14-24197. EMIF_CTLCFG_DENALI_PHY_854 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_3	R/W	0h	Controls RX_DCD pin for dm pad for slice 3. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1418 EMIF_CTLCFG_DENALI_PHY_855 Register

1 EMIF_CTLCFG_DENALI_PHY_855 Register (Offset = 4D5Ch) [reset = 0h]

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Table 14-24198. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD5Ch

Figure 14-8031. EMIF_CTLCFG_DENALI_PHY_855 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_PAD_DSLICE_IO_CFG_3						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_FDBK_RX_DCD_3				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_DQS_RX_DCD_3				
NONE			R/W				
0h			0h				

Table 14-24200. EMIF_CTLCFG_DENALI_PHY_855 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_3	R/W	0h	Controls PCLK/PARK pin for pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_3	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 3. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_3	R/W	0h	Controls RX_DCD pin for dqs pad for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1419 EMIF_CTLCFG_DENALI_PHY_856 Register

1 EMIF_CTLCFG_DENALI_PHY_856 Register (Offset = 4D60h) [reset = 0h]

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Table 14-24201. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD60h**

Figure 14-8032. EMIF_CTLCFG_DENALI_PHY_856 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ1_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ0_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ0_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24203. EMIF_CTLCFG_DENALI_PHY_856 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_3	R/W	0h	Read DQ1 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_3	R/W	0h	Read DQ0 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1420 EMIF_CTLCFG_DENALI_PHY_857 Register

1 EMIF_CTLCFG_DENALI_PHY_857 Register (Offset = 4D64h) [reset = 0h]

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Table 14-24204. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD64h**

Figure 14-8033. EMIF_CTLCFG_DENALI_PHY_857 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ3_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ2_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ2_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24206. EMIF_CTLCFG_DENALI_PHY_857 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_3	R/W	0h	Read DQ3 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_3	R/W	0h	Read DQ2 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1421 EMIF_CTLCFG_DENALI_PHY_858 Register

1 EMIF_CTLCFG_DENALI_PHY_858 Register (Offset = 4D68h) [reset = 0h]

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Table 14-24207. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD68h**

Figure 14-8034. EMIF_CTLCFG_DENALI_PHY_858 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ5_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ4_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ4_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24209. EMIF_CTLCFG_DENALI_PHY_858 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_3	R/W	0h	Read DQ5 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_3	R/W	0h	Read DQ4 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1422 EMIF_CTLCFG_DENALI_PHY_859 Register

1 EMIF_CTLCFG_DENALI_PHY_859 Register (Offset = 4D6Ch) [reset = 0h]

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Table 14-24210. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD6Ch**

Figure 14-8035. EMIF_CTLCFG_DENALI_PHY_859 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ7_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ7_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ6_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ6_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24212. EMIF_CTLCFG_DENALI_PHY_859 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_3	R/W	0h	Read DQ7 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_3	R/W	0h	Read DQ6 target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1423 EMIF_CTLCFG_DENALI_PHY_860 Register

1 EMIF_CTLCFG_DENALI_PHY_860 Register (Offset = 4D70h) [reset = 0h]

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Table 14-24213. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD70h**

Figure 14-8036. EMIF_CTLCFG_DENALI_PHY_860 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED					PHY_RX_PCLK_CLK_SEL_3		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24215. EMIF_CTLCFG_DENALI_PHY_860 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_3	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 3. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_3	R/W	0h	RX_PCLK clock frequency selection for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_3	R/W	0h	Read DM/DBI target delay setting for slice 3. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1424 EMIF_CTLCFG_DENALI_PHY_861 Register

1 EMIF_CTLCFG_DENALI_PHY_861 Register (Offset = 4D74h) [reset = 0h]

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Table 14-24216. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD74h**

Figure 14-8037. EMIF_CTLCFG_DENALI_PHY_861 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_3		
NONE					R/W		
0h					0h		

Table 14-24218. EMIF_CTLCFG_DENALI_PHY_861 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DATA_DC_CAL_CLK_SEL_3	R/W	0h	Determines DCC CAL clock for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1425 EMIF_CTLCFG_DENALI_PHY_862 Register

1 EMIF_CTLCFG_DENALI_PHY_862 Register (Offset = 4D78h) [reset = 0h]

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Table 14-24219. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD78h**

Figure 14-8038. EMIF_CTLCFG_DENALI_PHY_862 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_OE_TIMING_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_WR_TIMING_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_RD_TIMING_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_OE_TIMING_3							
R/W							
0h							

Table 14-24221. EMIF_CTLCFG_DENALI_PHY_862 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_3	R/W	0h	Start/end timing values for DQS output enable signals for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_3	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_3	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_3	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1426 EMIF_CTLCFG_DENALI_PHY_863 Register

1 EMIF_CTLCFG_DENALI_PHY_863 Register (Offset = 4D7Ch) [reset = 0h]

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Table 14-24222. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD7Ch

Figure 14-8039. EMIF_CTLCFG_DENALI_PHY_863 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQS_OE_RD_TIMING_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQS_TSEL_RD_TIMING_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_3			
NONE				R/W			
0h				0h			

Table 14-24224. EMIF_CTLCFG_DENALI_PHY_863 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_3	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_3	R/W	0h	Start/end timing values for DQS read based OE extension for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_3	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_3	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1427 EMIF_CTLCFG_DENALI_PHY_864 Register

1 EMIF_CTLCFG_DENALI_PHY_864 Register (Offset = 4D80h) [reset = 0h]

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Table 14-24225. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD80h**

Figure 14-8040. EMIF_CTLCFG_DENALI_PHY_864 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PHY_PAD_VREF_CTRL_DQ_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_VREF_SETTING_TIME_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_3							
R/W							
0h							

Table 14-24227. EMIF_CTLCFG_DENALI_PHY_864 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_3	R/W	0h	Pad VREF control settings for DQ slice 3. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_3	R/W	0h	Number of cycles for vref settle after setting is changed for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1428 EMIF_CTLCFG_DENALI_PHY_865 Register

1 EMIF_CTLCFG_DENALI_PHY_865 Register (Offset = 4D84h) [reset = 0h]

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Table 14-24228. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD84h**

Figure 14-8041. EMIF_CTLCFG_DENALI_PHY_865 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_DQS_IE_TIMING_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_IE_TIMING_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PER_CS_TRAINING_EN_3
NONE							R/W
0h							0h

Table 14-24230. EMIF_CTLCFG_DENALI_PHY_865 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_RDDATA_EN_IE_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_IE_TIMING_3	R/W	0h	Start/end timing values for DQS input enable signals for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_IE_TIMING_3	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PER_CS_TRAINING_EN_3	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 3. Must have same value in all slices. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1429 EMIF_CTLCFG_DENALI_PHY_866 Register

1 EMIF_CTLCFG_DENALI_PHY_866 Register (Offset = 4D88h) [reset = 0h]

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Table 14-24231. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD88h

Figure 14-8042. EMIF_CTLCFG_DENALI_PHY_866 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_WDQLVL_IE_ON_3
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DBI_MODE_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_IE_MODE_3	
NONE						R/W	
0h						0h	

Table 14-24233. EMIF_CTLCFG_DENALI_PHY_866 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_DLY_3	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 3. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_WDQLVL_IE_ON_3	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DBI_MODE_3	R/W	0h	DBI mode for slice 3. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_IE_MODE_3	R/W	0h	Input enable mode bits for slice 3. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1430 EMIF_CTLCFG_DENALI_PHY_867 Register

1 EMIF_CTLCFG_DENALI_PHY_867 Register (Offset = 4D8Ch) [reset = 0h]

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Table 14-24234. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD8Ch

Figure 14-8043. EMIF_CTLCFG_DENALI_PHY_867 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_MASTER_MODE_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED			PHY_RDDATA_EN_OE_DLY_3				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_RDDATA_EN_TSEL_DLY_3				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_3				
NONE			R/W				
0h			0h				

Table 14-24236. EMIF_CTLCFG_DENALI_PHY_867 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_MASTER_MODE_3	R/W	0h	Controller delay line override settings for slice 3. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_OE_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 3. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_TSEL_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 3. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_3	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1431 EMIF_CTLCFG_DENALI_PHY_868 Register

1 EMIF_CTLCFG_DENALI_PHY_868 Register (Offset = 4D90h) [reset = 0h]

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Table 14-24237. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD90h**

Figure 14-8044. EMIF_CTLCFG_DENALI_PHY_868 Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_DELAY_WAIT_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_MASTER_DELAY_STEP_3					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MASTER_DELAY_START_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_START_3							
R/W							
0h							

Table 14-24239. EMIF_CTLCFG_DENALI_PHY_868 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_3	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 3. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_3	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_3	R/W	0h	Start value for controller delay line locking algorithm for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1432 EMIF_CTLCFG_DENALI_PHY_869 Register

1 EMIF_CTLCFG_DENALI_PHY_869 Register (Offset = 4D94h) [reset = 0h]

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Table 14-24240. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD94h**

Figure 14-8045. EMIF_CTLCFG_DENALI_PHY_869 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_3			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DLY_STEP_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RPTR_UPDATE_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_HALF_MEASURE_3							
R/W							
0h							

Table 14-24242. EMIF_CTLCFG_DENALI_PHY_869 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_3	R/W	0h	DQS target delay fine step size during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_3	R/W	0h	DQS target delay step size during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_3	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_3	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1433 EMIF_CTLCFG_DENALI_PHY_870 Register

1 EMIF_CTLCFG_DENALI_PHY_870 Register (Offset = 4D98h) [reset = 0h]

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Table 14-24243. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CD98h

Figure 14-8046. EMIF_CTLCFG_DENALI_PHY_870 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_GTLVL_RESP_WAIT_CNT_3				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_GTLVL_DLY_STEP_3			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_RESP_WAIT_CNT_3					
NONE		R/W					
0h		0h					

Table 14-24245. EMIF_CTLCFG_DENALI_PHY_870 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_3	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 3. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_3	R/W	0h	DQS target delay step size during gate training for slice 3. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_3	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1434 EMIF_CTLCFG_DENALI_PHY_871 Register

1 EMIF_CTLCFG_DENALI_PHY_871 Register (Offset = 4D9Ch) [reset = 0h]

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Table 14-24246. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CD9Ch**

Figure 14-8047. EMIF_CTLCFG_DENALI_PHY_871 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GTLVL_FINAL_STEP_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_FINAL_STEP_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GTLVL_BACK_STEP_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_BACK_STEP_3							
R/W							
0h							

Table 14-24248. EMIF_CTLCFG_DENALI_PHY_871 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_3	R/W	0h	Final backup step delay used in gate training algorithm for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_3	R/W	0h	Interim backup step delay used in gate training algorithm for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1435 EMIF_CTLCFG_DENALI_PHY_872 Register

1 EMIF_CTLCFG_DENALI_PHY_872 Register (Offset = 4DA0h) [reset = 0h]

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Table 14-24249. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDA0h**

Figure 14-8048. EMIF_CTLCFG_DENALI_PHY_872 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_WDQLVL_DM_SEARCH_RANGE_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DM_SEARCH_RANGE_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_3			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DLY_STEP_3							
R/W							
0h							

Table 14-24251. EMIF_CTLCFG_DENALI_PHY_872 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_3	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 3. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_3	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 3. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_3	R/W	0h	DQ target delay step size during write data leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1436 EMIF_CTLCFG_DENALI_PHY_873 Register

1 EMIF_CTLCFG_DENALI_PHY_873 Register (Offset = 4DA4h) [reset = 0h]

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Table 14-24252. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDA4h**

Figure 14-8049. EMIF_CTLCFG_DENALI_PHY_873 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_DLY_STEP_3			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_TOGGLE_PRE_SUPPORT_3
NONE							R/W
0h							0h

Table 14-24254. EMIF_CTLCFG_DENALI_PHY_873 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_3	R/W	0h	DQS target delay step size during read leveling for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_3	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1437 EMIF_CTLCFG_DENALI_PHY_874 Register

1 EMIF_CTLCFG_DENALI_PHY_874 Register (Offset = 4DA8h) [reset = 0h]

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Table 14-24255. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CDA8h

Figure 14-8050. EMIF_CTLCFG_DENALI_PHY_874 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_MAX_EDGE_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_MAX_EDGE_3							
R/W							
0h							

Table 14-24257. EMIF_CTLCFG_DENALI_PHY_874 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_3	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1438 EMIF_CTLCFG_DENALI_PHY_875 Register

1 EMIF_CTLCFG_DENALI_PHY_875 Register (Offset = 4DACh) [reset = 30000h]

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Table 14-24258. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CDACh

Figure 14-8051. EMIF_CTLCFG_DENALI_PHY_875 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_3	
NONE						R/W	
0h						3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_3	
NONE						R/W	
0h						0h	

Table 14-24260. EMIF_CTLCFG_DENALI_PHY_875 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DATA_DC_INIT_DISABLE_3	R/W	3h	Disable duty cycle adjust at initialization for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_3	R/W	0h	Write path clock gating timing for slice 3. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_3	R/W	0h	Write path clock gating disable for slice 3. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.6.6.2.1439 EMIF_CTLCFG_DENALI_PHY_876 Register

1 EMIF_CTLCFG_DENALI_PHY_876 Register (Offset = 4DB0h) [reset = 0h]

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Table 14-24261. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDB0h**

Figure 14-8052. EMIF_CTLCFG_DENALI_PHY_876 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ_INIT_SLV_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQS_INIT_SLV_DELAY_3							
R/W							
0h							

Table 14-24263. EMIF_CTLCFG_DENALI_PHY_876 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_3	R/W	0h	Initial value of write DQ target delay for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_3	R/W	0h	Initial value of write DQS target delay for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1440 EMIF_CTLCFG_DENALI_PHY_877 Register

1 EMIF_CTLCFG_DENALI_PHY_877 Register (Offset = 4DB4h) [reset = 0h]

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Table 14-24264. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDB4h**

Figure 14-8053. EMIF_CTLCFG_DENALI_PHY_877 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DM_CLK_SE_THRSHLD_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_3
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_3
NONE							R/W
0h							0h

Table 14-24266. EMIF_CTLCFG_DENALI_PHY_877 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_3	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_3	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 3. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_DATA_DC_WDQLVL_ENABLE_3	R/W	0h	Enable duty cycle adjust during write DQ training for slice 3. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_DATA_DC_WRLVL_ENABLE_3	R/W	0h	Enable duty cycle adjust during write leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1441 EMIF_CTLCFG_DENALI_PHY_878 Register

1 EMIF_CTLCFG_DENALI_PHY_878 Register (Offset = 4DB8h) [reset = 0h]

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Table 14-24267. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDB8h**

Figure 14-8054. EMIF_CTLCFG_DENALI_PHY_878 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_RDDATA_EN_DLY_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_MEAS_DLY_STEP_ENABLE_3						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_WDQ_OSC_DELTA_3						
NONE	R/W						
0h	0h						

Table 14-24269. EMIF_CTLCFG_DENALI_PHY_878 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_RDDATA_EN_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 3. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_MEAS_DLY_STEP_ENABLE_3	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 3. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_WDQ_OSC_DELTA_3	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1442 EMIF_CTLCFG_DENALI_PHY_879 Register

1 EMIF_CTLCFG_DENALI_PHY_879 Register (Offset = 4DBCh) [reset = 0h]

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Table 14-24270. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDBCh**

Figure 14-8055. EMIF_CTLCFG_DENALI_PHY_879 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_DM_SWIZZLE0_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_DM_SWIZZLE0_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_DM_SWIZZLE0_3							
R/W							
0h							

Table 14-24272. EMIF_CTLCFG_DENALI_PHY_879 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_3	R/W	0h	DQ/DM bit swizzling 0 for slice 3. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1443 EMIF_CTLCFG_DENALI_PHY_880 Register

1 EMIF_CTLCFG_DENALI_PHY_880 Register (Offset = 4DC0h) [reset = 0h]

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Table 14-24273. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDC0h**

Figure 14-8056. EMIF_CTLCFG_DENALI_PHY_880 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_DQ_DM_SWIZZLE1_3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-24275. EMIF_CTLCFG_DENALI_PHY_880 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_3	R/W	0h	DQ/DM bit swizzling 1 for slice 3. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1444 EMIF_CTLCFG_DENALI_PHY_881 Register

1 EMIF_CTLCFG_DENALI_PHY_881 Register (Offset = 4DC4h) [reset = 0h]

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Table 14-24276. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDC4h**

Figure 14-8057. EMIF_CTLCFG_DENALI_PHY_881 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ1_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ0_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24278. EMIF_CTLCFG_DENALI_PHY_881 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ1 for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ0 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1445 EMIF_CTLCFG_DENALI_PHY_882 Register

1 EMIF_CTLCFG_DENALI_PHY_882 Register (Offset = 4DC8h) [reset = 0h]

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Table 14-24279. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CDC8h

Figure 14-8058. EMIF_CTLCFG_DENALI_PHY_882 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ3_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ2_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24281. EMIF_CTLCFG_DENALI_PHY_882 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ3 for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ2 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1446 EMIF_CTLCFG_DENALI_PHY_883 Register

1 EMIF_CTLCFG_DENALI_PHY_883 Register (Offset = 4DCCh) [reset = 0h]

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Table 14-24282. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDCCh**

Figure 14-8059. EMIF_CTLCFG_DENALI_PHY_883 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ5_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ4_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24284. EMIF_CTLCFG_DENALI_PHY_883 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ5 for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ4 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1447 EMIF_CTLCFG_DENALI_PHY_884 Register

1 EMIF_CTLCFG_DENALI_PHY_884 Register (Offset = 4DD0h) [reset = 0h]

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Table 14-24285. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDD0h**

Figure 14-8060. EMIF_CTLCFG_DENALI_PHY_884 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ7_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ6_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24287. EMIF_CTLCFG_DENALI_PHY_884 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ7 for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQ6 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1448 EMIF_CTLCFG_DENALI_PHY_885 Register

1 EMIF_CTLCFG_DENALI_PHY_885 Register (Offset = 4DD4h) [reset = 0h]

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Table 14-24288. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CDD4h

Figure 14-8061. EMIF_CTLCFG_DENALI_PHY_885 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQS_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDM_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24290. EMIF_CTLCFG_DENALI_PHY_885 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DQS for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_3	R/W	0h	Write clock target delay setting for DM for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1449 EMIF_CTLCFG_DENALI_PHY_886 Register

1 EMIF_CTLCFG_DENALI_PHY_886 Register (Offset = 4DD8h) [reset = 0h]

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Table 14-24291. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDD8h**

Figure 14-8062. EMIF_CTLCFG_DENALI_PHY_886 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_3	
NONE						R/W	
0h						0h	

Table 14-24293. EMIF_CTLCFG_DENALI_PHY_886 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 3. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_3	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1450 EMIF_CTLCFG_DENALI_PHY_887 Register

1 EMIF_CTLCFG_DENALI_PHY_887 Register (Offset = 4DDCh) [reset = 0h]

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Table 14-24294. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDDCh**

Figure 14-8063. EMIF_CTLCFG_DENALI_PHY_887 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24296. EMIF_CTLCFG_DENALI_PHY_887 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1451 EMIF_CTLCFG_DENALI_PHY_888 Register

1 EMIF_CTLCFG_DENALI_PHY_888 Register (Offset = 4DE0h) [reset = 0h]

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Table 14-24297. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDE0h**

Figure 14-8064. EMIF_CTLCFG_DENALI_PHY_888 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24299. EMIF_CTLCFG_DENALI_PHY_888 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1452 EMIF_CTLCFG_DENALI_PHY_889 Register

1 EMIF_CTLCFG_DENALI_PHY_889 Register (Offset = 4DE4h) [reset = 0h]

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Table 14-24300. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDE4h**

Figure 14-8065. EMIF_CTLCFG_DENALI_PHY_889 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24302. EMIF_CTLCFG_DENALI_PHY_889 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1453 EMIF_CTLCFG_DENALI_PHY_890 Register

1 EMIF_CTLCFG_DENALI_PHY_890 Register (Offset = 4DE8h) [reset = 0h]

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Table 14-24303. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDE8h**

Figure 14-8066. EMIF_CTLCFG_DENALI_PHY_890 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24305. EMIF_CTLCFG_DENALI_PHY_890 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1454 EMIF_CTLCFG_DENALI_PHY_891 Register

1 EMIF_CTLCFG_DENALI_PHY_891 Register (Offset = 4DECh) [reset = 0h]

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Table 14-24306. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDECh**

Figure 14-8067. EMIF_CTLCFG_DENALI_PHY_891 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24308. EMIF_CTLCFG_DENALI_PHY_891 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1455 EMIF_CTLCFG_DENALI_PHY_892 Register

1 EMIF_CTLCFG_DENALI_PHY_892 Register (Offset = 4DF0h) [reset = 0h]

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Table 14-24309. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDF0h**

Figure 14-8068. EMIF_CTLCFG_DENALI_PHY_892 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24311. EMIF_CTLCFG_DENALI_PHY_892 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1456 EMIF_CTLCFG_DENALI_PHY_893 Register

1 EMIF_CTLCFG_DENALI_PHY_893 Register (Offset = 4DF4h) [reset = 0h]

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Table 14-24312. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDF4h**

Figure 14-8069. EMIF_CTLCFG_DENALI_PHY_893 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24314. EMIF_CTLCFG_DENALI_PHY_893 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1457 EMIF_CTLCFG_DENALI_PHY_894 Register

1 EMIF_CTLCFG_DENALI_PHY_894 Register (Offset = 4DF8h) [reset = 0h]

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Table 14-24315. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CDF8h**

Figure 14-8070. EMIF_CTLCFG_DENALI_PHY_894 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DM_RISE_SLAVE_DELAY_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24317. EMIF_CTLCFG_DENALI_PHY_894 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS target delay setting for DM for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1458 EMIF_CTLCFG_DENALI_PHY_895 Register

1 EMIF_CTLCFG_DENALI_PHY_895 Register (Offset = 4DFCh) [reset = 0h]

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Table 14-24318. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CDFCh

Figure 14-8071. EMIF_CTLCFG_DENALI_PHY_895 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_3							
R/W							
0h							

Table 14-24320. EMIF_CTLCFG_DENALI_PHY_895 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_3	R/W	0h	Read DQS target delay setting for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS target delay setting for DM for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1459 EMIF_CTLCFG_DENALI_PHY_896 Register

1 EMIF_CTLCFG_DENALI_PHY_896 Register (Offset = 4E00h) [reset = 0h]

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Table 14-24321. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE00h**

Figure 14-8072. EMIF_CTLCFG_DENALI_PHY_896 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DELAY_EARLY_THRESHOLD_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRITE_PATH_LAT_ADD_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_LATENCY_ADJUST_3			
NONE				R/W			
0h				0h			

Table 14-24323. EMIF_CTLCFG_DENALI_PHY_896 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_3	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_3	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 3. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_3	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1460 EMIF_CTLCFG_DENALI_PHY_897 Register

1 EMIF_CTLCFG_DENALI_PHY_897 Register (Offset = 4E04h) [reset = 0h]

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Table 14-24324. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 CE04h

Figure 14-8073. EMIF_CTLCFG_DENALI_PHY_897 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_WRLVL_EARLY_FORCE_ZERO_3</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24326. EMIF_CTLCFG_DENALI_PHY_897 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_3	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1461 EMIF_CTLCFG_DENALI_PHY_898 Register

1 EMIF_CTLCFG_DENALI_PHY_898 Register (Offset = 4E08h) [reset = 0h]

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Table 14-24327. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE08h**

Figure 14-8074. EMIF_CTLCFG_DENALI_PHY_898 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_GTLVL_LAT_ADJ_START_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_RDDQS_SLV_DLY_START_3							
R/W							
0h							

Table 14-24329. EMIF_CTLCFG_DENALI_PHY_898 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_3	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_3	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1462 EMIF_CTLCFG_DENALI_PHY_899 Register

1 EMIF_CTLCFG_DENALI_PHY_899 Register (Offset = 4E0Ch) [reset = 0h]

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Table 14-24330. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 CE0Ch**

Figure 14-8075. EMIF_CTLCFG_DENALI_PHY_899 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PASS_3
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_3							
R/W							
0h							

Table 14-24332. EMIF_CTLCFG_DENALI_PHY_899 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_3	R/W	0h	Indicates if No-topology training found a passing result for slice 3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_3	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_3	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1463 EMIF_CTLCFG_DENALI_PHY_900 Register

1 EMIF_CTLCFG_DENALI_PHY_900 Register (Offset = 4E10h) [reset = 0h]

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Table 14-24333. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE10h**

Figure 14-8076. EMIF_CTLCFG_DENALI_PHY_900 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3							
R/W							
0h							

Table 14-24335. EMIF_CTLCFG_DENALI_PHY_900 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1464 EMIF_CTLCFG_DENALI_PHY_901 Register

1 EMIF_CTLCFG_DENALI_PHY_901 Register (Offset = 4E14h) [reset = 20202020h]

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Table 14-24336. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE14h**

Figure 14-8077. EMIF_CTLCFG_DENALI_PHY_901 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_3							
R/W							
20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_3							
R/W							
20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_3							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_3							
R/W							
20h							

Table 14-24338. EMIF_CTLCFG_DENALI_PHY_901 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ2_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ1_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ0_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQS_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1465 EMIF_CTLCFG_DENALI_PHY_902 Register

1 EMIF_CTLCFG_DENALI_PHY_902 Register (Offset = 4E18h) [reset = 20202020h]

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Table 14-24339. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE18h**

Figure 14-8078. EMIF_CTLCFG_DENALI_PHY_902 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_3							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DATA_DC_DQ5_CLK_ADJUST_3							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DATA_DC_DQ4_CLK_ADJUST_3							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DATA_DC_DQ3_CLK_ADJUST_3							
R/W							
20h							

Table 14-24341. EMIF_CTLCFG_DENALI_PHY_902 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DATA_DC_DQ6_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DATA_DC_DQ5_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DQ4_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ3_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1466 EMIF_CTLCFG_DENALI_PHY_903 Register

1 EMIF_CTLCFG_DENALI_PHY_903 Register (Offset = 4E1Ch) [reset = 2020h]

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Table 14-24342. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE1Ch**

Figure 14-8079. EMIF_CTLCFG_DENALI_PHY_903 Name Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_3							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_3							
R/W							
20h							

Table 14-24344. EMIF_CTLCFG_DENALI_PHY_903 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_DSLICE_PAD_BOOSTPN_SETTING_3	R/W	0h	Setting for boost P/N of pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DATA_DC_DM_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_DC_DQ7_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1467 EMIF_CTLCFG_DENALI_PHY_904 Register

1 EMIF_CTLCFG_DENALI_PHY_904 Register (Offset = 4E20h) [reset = 0h]

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Table 14-24345. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 CE20h**

Figure 14-8080. EMIF_CTLCFG_DENALI_PHY_904 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_3	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_3	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTLE_SETTING_3					
NONE		R/W					
0h		0h					

Table 14-24347. EMIF_CTLCFG_DENALI_PHY_904 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DQS_FFE_3	R/W	0h	TX_FFE setting for DQS pad for slice 3. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DQ_FFE_3	R/W	0h	TX_FFE setting for DQ/DM pad for slice 3. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DSLICE_PAD_RX_CTLE_SETTING_3	R/W	0h	Setting for RX ctle P/N of pad for slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1468 EMIF_CTLCFG_DENALI_PHY_1024 Register

1 EMIF_CTLCFG_DENALI_PHY_1024 Register (Offset = 5000h) [reset = 0h]

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Table 14-24348. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D000h**

Figure 14-8081. EMIF_CTLCFG_DENALI_PHY_1024 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">SC_PHY_ADR_MANUAL_CLEAR_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CLK_BYPASS_OVERRIDE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24350. EMIF_CTLCFG_DENALI_PHY_1024 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for address slice 0. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for address slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1469 EMIF_CTLCFG_DENALI_PHY_1025 Register

1 EMIF_CTLCFG_DENALI_PHY_1025 Register (Offset = 5004h) [reset = 1000h]

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Table 14-24351. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D004h**

Figure 14-8082. EMIF_CTLCFG_DENALI_PHY_1025 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
23	22	21	20	19	18	17	16
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
15	14	13	12	11	10	9	8
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
7	6	5	4	3	2	1	0
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							

Table 14-24353. EMIF_CTLCFG_DENALI_PHY_1025 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_0	R	1000h	Observation register containing loopback status/results for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1470 EMIF_CTLCFG_DENALI_PHY_1026 Register

1 EMIF_CTLCFG_DENALI_PHY_1026 Register (Offset = 5008h) [reset = 0h]

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Table 14-24354. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D008h**

Figure 14-8083. EMIF_CTLCFG_DENALI_PHY_1026 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_MEAS_DLY_STEP_VALUE_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_LPBK_ERROR_COUNT_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_LPBK_ERROR_COUNT_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24356. EMIF_CTLCFG_DENALI_PHY_1026 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_0	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1471 EMIF_CTLCFG_DENALI_PHY_1027 Register

1 EMIF_CTLCFG_DENALI_PHY_1027 Register (Offset = 500Ch) [reset = 0h]

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Table 14-24357. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D00Ch**

Figure 14-8084. EMIF_CTLCFG_DENALI_PHY_1027 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_ADR_BASE_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_MASTER_DLY_LOCK_OBS_0		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DLY_LOCK_OBS_0							
R							
0h							

Table 14-24359. EMIF_CTLCFG_DENALI_PHY_1027 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing addr target delay for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing base target delay for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing controller delay results for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1472 EMIF_CTLCFG_DENALI_PHY_1028 Register

1 EMIF_CTLCFG_DENALI_PHY_1028 Register (Offset = 5010h) [reset = 0h]

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Table 14-24360. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D010h

Figure 14-8085. EMIF_CTLCFG_DENALI_PHY_1028 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_TSEL_ENABLE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SC_PHY_ADR_SNAP_OBS_REGS_0</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-24362. EMIF_CTLCFG_DENALI_PHY_1028 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_0	R/W	0h	Enables tsel_en for address slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1473 EMIF_CTLCFG_DENALI_PHY_1029 Register

1 EMIF_CTLCFG_DENALI_PHY_1029 Register (Offset = 5014h) [reset = 100h]

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Table 14-24363. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D014h**

Figure 14-8086. EMIF_CTLCFG_DENALI_PHY_1029 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_ADR_PRBS_PATTERN_START_0						
NONE	R/W						
0h	1h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_ADR_LPBK_CONTROL_0						
NONE	R/W						
0h	0h						

Table 14-24365. EMIF_CTLCFG_DENALI_PHY_1029 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_0	R/W	0h	Power reduction disable for address slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for address slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for address slice 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_0	R/W	0h	Loopback control bits for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1474 EMIF_CTLCFG_DENALI_PHY_1030 Register

1 EMIF_CTLCFG_DENALI_PHY_1030 Register (Offset = 5018h) [reset = 0h]

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Table 14-24366. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D018h

Figure 14-8087. EMIF_CTLCFG_DENALI_PHY_1030 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_0		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_TYPE_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h

Table 14-24368. EMIF_CTLCFG_DENALI_PHY_1030 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_0	R/W	0h	Input enable control for address slice 0. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_0	R/W	0h	DRAM type for address slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1475 EMIF_CTLCFG_DENALI_PHY_1031 Register

1 EMIF_CTLCFG_DENALI_PHY_1031 Register (Offset = 501Ch) [reset = 0h]

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Table 14-24369. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D01Ch

Figure 14-8088. EMIF_CTLCFG_DENALI_PHY_1031 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_ADR_DDL_MODE_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_MODE_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_MODE_0							
R/W							
0h							

Table 14-24371. EMIF_CTLCFG_DENALI_PHY_1031 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_0	R/W	0h	DDL mode for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1476 EMIF_CTLCFG_DENALI_PHY_1032 Register

1 EMIF_CTLCFG_DENALI_PHY_1032 Register (Offset = 5020h) [reset = 0h]

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Table 14-24372. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D020h**

Figure 14-8089. EMIF_CTLCFG_DENALI_PHY_1032 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_DDL_MASK_0					
NONE		R/W					
0h		0h					

Table 14-24374. EMIF_CTLCFG_DENALI_PHY_1032 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_0	R/W	0h	DDL mask for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1477 EMIF_CTLCFG_DENALI_PHY_1033 Register

1 EMIF_CTLCFG_DENALI_PHY_1033 Register (Offset = 5024h) [reset = 0h]

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Table 14-24375. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D024h**

Figure 14-8090. EMIF_CTLCFG_DENALI_PHY_1033 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							

Table 14-24377. EMIF_CTLCFG_DENALI_PHY_1033 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_0	R	0h	Observation register containing DDL test bits for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1478 EMIF_CTLCFG_DENALI_PHY_1034 Register

1 EMIF_CTLCFG_DENALI_PHY_1034 Register (Offset = 5028h) [reset = 0h]

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Table 14-24378. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D028h**

Figure 14-8091. EMIF_CTLCFG_DENALI_PHY_1034 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							

Table 14-24380. EMIF_CTLCFG_DENALI_PHY_1034 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0	R	0h	Observation register containing controller DDL bits for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1479 EMIF_CTLCFG_DENALI_PHY_1035 Register

1 EMIF_CTLCFG_DENALI_PHY_1035 Register (Offset = 502Ch) [reset = 0h]

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Table 14-24381. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D02Ch

Figure 14-8092. EMIF_CTLCFG_DENALI_PHY_1035 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_COARSE_DLY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_COARSE_DLY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_START_0							
R/W							
0h							

Table 14-24383. EMIF_CTLCFG_DENALI_PHY_1035 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_0	R/W	0h	Coarse CA training DDL increment value for address slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_0	R/W	0h	CA training DDL start value for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1480 EMIF_CTLCFG_DENALI_PHY_1036 Register

1 EMIF_CTLCFG_DENALI_PHY_1036 Register (Offset = 5030h) [reset = 0h]

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Table 14-24384. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D030h**

Figure 14-8093. EMIF_CTLCFG_DENALI_PHY_1036 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_CALVL_QTR_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_QTR_0							
R/W							
0h							

Table 14-24386. EMIF_CTLCFG_DENALI_PHY_1036 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_0	R/W	0h	CA training DDL quarter cycle delay value for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1481 EMIF_CTLCFG_DENALI_PHY_1037 Register

1 EMIF_CTLCFG_DENALI_PHY_1037 Register (Offset = 5034h) [reset = 0h]

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Table 14-24387. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D034h**

Figure 14-8094. EMIF_CTLCFG_DENALI_PHY_1037 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							

Table 14-24389. EMIF_CTLCFG_DENALI_PHY_1037 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_0	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1482 EMIF_CTLCFG_DENALI_PHY_1038 Register

1 EMIF_CTLCFG_DENALI_PHY_1038 Register (Offset = 5038h) [reset = 0h]

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Table 14-24390. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D038h**

Figure 14-8095. EMIF_CTLCFG_DENALI_PHY_1038 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							

Table 14-24392. EMIF_CTLCFG_DENALI_PHY_1038 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_0	R/W	0h	CA training rank aggregation control bits for address slice 0. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_0	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1483 EMIF_CTLCFG_DENALI_PHY_1039 Register

1 EMIF_CTLCFG_DENALI_PHY_1039 Register (Offset = 503Ch) [reset = 0h]

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Table 14-24393. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D03Ch**

Figure 14-8096. EMIF_CTLCFG_DENALI_PHY_1039 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CALVL_PERIODIC_START_OFFSET_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_PERIODIC_START_OFFSET_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_RESP_WAIT_CNT_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_CALVL_NUM_PATTERNS_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24395. EMIF_CTLCFG_DENALI_PHY_1039 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_0	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_0	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_0	R/W	0h	Number of patterns to use during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1484 EMIF_CTLCFG_DENALI_PHY_1040 Register

1 EMIF_CTLCFG_DENALI_PHY_1040 Register (Offset = 5040h) [reset = 0h]

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Table 14-24396. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D040h**

Figure 14-8097. EMIF_CTLCFG_DENALI_PHY_1040 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_0
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_0
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_0
NONE							R/W
0h							0h

Table 14-24398. EMIF_CTLCFG_DENALI_PHY_1040 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_0	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_0	W	0h	Clears the CA training state machine error status for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_0	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-24398. EMIF_CTLCFG_DENALI_PHY_1040 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_0	R/W	0h	Enables CA training debug mode for address slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1485 EMIF_CTLCFG_DENALI_PHY_1041 Register

1 EMIF_CTLCFG_DENALI_PHY_1041 Register (Offset = 5044h) [reset = 0h]

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Table 14-24399. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D044h**

Figure 14-8098. EMIF_CTLCFG_DENALI_PHY_1041 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH0_OBS0_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_CH0_OBS0_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_CH0_OBS0_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_CH0_OBS0_0							
R							
0h							

Table 14-24401. EMIF_CTLCFG_DENALI_PHY_1041 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH0_OBS0_0	R	0h	Observation register for CA training for channel 0 slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1486 EMIF_CTLCFG_DENALI_PHY_1042 Register

1 EMIF_CTLCFG_DENALI_PHY_1042 Register (Offset = 5048h) [reset = 0h]

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Table 14-24402. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D048h**

Figure 14-8099. EMIF_CTLCFG_DENALI_PHY_1042 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH1_OBS0_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_CH1_OBS0_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_CH1_OBS0_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH1_OBS0_0							
R							
0h							

Table 14-24404. EMIF_CTLCFG_DENALI_PHY_1042 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH1_OBS0_0	R	0h	Observation register for CA training for channel 1 slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1487 EMIF_CTLCFG_DENALI_PHY_1043 Register

1 EMIF_CTLCFG_DENALI_PHY_1043 Register (Offset = 504Ch) [reset = 0h]

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Table 14-24405. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D04Ch**

Figure 14-8100. EMIF_CTLCFG_DENALI_PHY_1043 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_0							
R							
0h							

Table 14-24407. EMIF_CTLCFG_DENALI_PHY_1043 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_0	R	0h	Observation register contains general CA training bits for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1488 EMIF_CTLCFG_DENALI_PHY_1044 Register

1 EMIF_CTLCFG_DENALI_PHY_1044 Register (Offset = 5050h) [reset = 100h]

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Table 14-24408. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D050h**

Figure 14-8101. EMIF_CTLCFG_DENALI_PHY_1044 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS2_0							
R							
100h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS2_0							
R							
100h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS2_0							
R							
100h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_0							
R							
100h							

Table 14-24410. EMIF_CTLCFG_DENALI_PHY_1044 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_0	R	100h	Observation register contains periodic CA training bits for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1489 EMIF_CTLCFG_DENALI_PHY_1045 Register

1 EMIF_CTLCFG_DENALI_PHY_1045 Register (Offset = 5054h) [reset = 0h]

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Table 14-24411. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D054h**

Figure 14-8102. EMIF_CTLCFG_DENALI_PHY_1045 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_0_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_0_0							
R/W							
0h							

Table 14-24413. EMIF_CTLCFG_DENALI_PHY_1045 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_0	R/W	0h	CA training foreground pattern 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1490 EMIF_CTLCFG_DENALI_PHY_1046 Register

1 EMIF_CTLCFG_DENALI_PHY_1046 Register (Offset = 5058h) [reset = 0h]

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Table 14-24414. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D058h**

Figure 14-8103. EMIF_CTLCFG_DENALI_PHY_1046 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_0_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_0_0							
R/W							
0h							

Table 14-24416. EMIF_CTLCFG_DENALI_PHY_1046 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_0	R/W	0h	CA training background pattern 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1491 EMIF_CTLCFG_DENALI_PHY_1047 Register

1 EMIF_CTLCFG_DENALI_PHY_1047 Register (Offset = 505Ch) [reset = 0h]

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Table 14-24417. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D05Ch**

Figure 14-8104. EMIF_CTLCFG_DENALI_PHY_1047 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_1_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_1_0							
R/W							
0h							

Table 14-24419. EMIF_CTLCFG_DENALI_PHY_1047 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_0	R/W	0h	CA training foreground pattern 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1492 EMIF_CTLCFG_DENALI_PHY_1048 Register

1 EMIF_CTLCFG_DENALI_PHY_1048 Register (Offset = 5060h) [reset = 0h]

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Table 14-24420. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D060h**

Figure 14-8105. EMIF_CTLCFG_DENALI_PHY_1048 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_1_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_1_0							
R/W							
0h							

Table 14-24422. EMIF_CTLCFG_DENALI_PHY_1048 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_0	R/W	0h	CA training background pattern 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1493 EMIF_CTLCFG_DENALI_PHY_1049 Register

1 EMIF_CTLCFG_DENALI_PHY_1049 Register (Offset = 5064h) [reset = 0h]

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Table 14-24423. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D064h

Figure 14-8106. EMIF_CTLCFG_DENALI_PHY_1049 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24425. EMIF_CTLCFG_DENALI_PHY_1049 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_0	R/W	0h	CA training foreground pattern 2 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1494 EMIF_CTLCFG_DENALI_PHY_1050 Register

1 EMIF_CTLCFG_DENALI_PHY_1050 Register (Offset = 5068h) [reset = 0h]

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Table 14-24426. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D068h**

Figure 14-8107. EMIF_CTLCFG_DENALI_PHY_1050 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_BG_2_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24428. EMIF_CTLCFG_DENALI_PHY_1050 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_0	R/W	0h	CA training background pattern 2 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1495 EMIF_CTLCFG_DENALI_PHY_1051 Register

1 EMIF_CTLCFG_DENALI_PHY_1051 Register (Offset = 506Ch) [reset = 0h]

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Table 14-24429. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D06Ch**

Figure 14-8108. EMIF_CTLCFG_DENALI_PHY_1051 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_3_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_3_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_3_0							
R/W							
0h							

Table 14-24431. EMIF_CTLCFG_DENALI_PHY_1051 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_0	R/W	0h	CA training foreground pattern 3 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1496 EMIF_CTLCFG_DENALI_PHY_1052 Register

1 EMIF_CTLCFG_DENALI_PHY_1052 Register (Offset = 5070h) [reset = 0h]

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Table 14-24432. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D070h**

Figure 14-8109. EMIF_CTLCFG_DENALI_PHY_1052 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_3_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_3_0							
R/W							
0h							

Table 14-24434. EMIF_CTLCFG_DENALI_PHY_1052 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_0	R/W	0h	CA training background pattern 3 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1497 EMIF_CTLCFG_DENALI_PHY_1053 Register

1 EMIF_CTLCFG_DENALI_PHY_1053 Register (Offset = 5074h) [reset = 0h]

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Table 14-24435. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D074h

Figure 14-8110. EMIF_CTLCFG_DENALI_PHY_1053 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							

Table 14-24437. EMIF_CTLCFG_DENALI_PHY_1053 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_0	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1498 EMIF_CTLCFG_DENALI_PHY_1054 Register

1 EMIF_CTLCFG_DENALI_PHY_1054 Register (Offset = 5078h) [reset = 0h]

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Table 14-24438. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D078h**

Figure 14-8111. EMIF_CTLCFG_DENALI_PHY_1054 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_ADR_SEG_MASK_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_ADR_BIT_MASK_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_LP4_BOOT_SLV_DELAY_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_LP4_BOOT_SLV_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24440. EMIF_CTLCFG_DENALI_PHY_1054 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_0	R/W	0h	Segment mask bit for address slice 0. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_0	R/W	0h	Mask bit for address slice 0. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_0	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1499 EMIF_CTLCFG_DENALI_PHY_1055 Register

1 EMIF_CTLCFG_DENALI_PHY_1055 Register (Offset = 507Ch) [reset = 0h]

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Table 14-24441. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D07Ch**

Figure 14-8112. EMIF_CTLCFG_DENALI_PHY_1055 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_0					
NONE		R/W					
0h		0h					

Table 14-24443. EMIF_CTLCFG_DENALI_PHY_1055 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_0	R/W	0h	Controls address pad output enable for address slice 0. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_0	R/W	0h	Toggle control during static activity for address slice 0. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_0	R/W	0h	Mask bit for CS training participation for address slice 0. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_0	R/W	0h	Mask bit for CA training participation for address slice 0. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1500 EMIF_CTLCFG_DENALI_PHY_1056 Register

1 EMIF_CTLCFG_DENALI_PHY_1056 Register (Offset = 5080h) [reset = 20202003h]

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Table 14-24444. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D080h**

Figure 14-8113. EMIF_CTLCFG_DENALI_PHY_1056 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR2_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR1_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR0_CLK_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_DC_INIT_DISABLE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-24446. EMIF_CTLCFG_DENALI_PHY_1056 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_DC_ADR2_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 2 for address slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR1_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 1 for address slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR0_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 0 for address slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_DC_INIT_DISABLE_0	R/W	3h	Duty Cycle Corrector disable at initialization for address slice 0. Set to 1 to disable, bit [1] controls data path, bit [0] controls clock path. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1501 EMIF_CTLCFG_DENALI_PHY_1057 Register

1 EMIF_CTLCFG_DENALI_PHY_1057 Register (Offset = 5084h) [reset = 202020h]

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Table 14-24447. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D084h**

Figure 14-8114. EMIF_CTLCFG_DENALI_PHY_1057 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_ADR_DC_ADR5_CLK_ADJUST_0							
R/W							
20h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_ADR4_CLK_ADJUST_0							
R/W							
20h							
7	6	5	4	3	2	1	0
PHY_ADR_DC_ADR3_CLK_ADJUST_0							
R/W							
20h							

Table 14-24449. EMIF_CTLCFG_DENALI_PHY_1057 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_0	R/W	0h	DCC and RX_CAL clk gate disable for address slice 0. 1 = disable clk gate. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR5_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 5 for address slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR4_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 4 for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADR3_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 3 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1502 EMIF_CTLCFG_DENALI_PHY_1058 Register

1 EMIF_CTLCFG_DENALI_PHY_1058 Register (Offset = 5088h) [reset = 0h]

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Table 14-24450. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D088h**

Figure 14-8115. EMIF_CTLCFG_DENALI_PHY_1058 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_DC_ADJUST_START_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_DC_WEIGHT_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_CAL_TIMEOUT_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_CAL_SAMPLE_WAIT_0							
R/W							
0h							

Table 14-24452. EMIF_CTLCFG_DENALI_PHY_1058 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_DC_ADJUST_START_0	R/W	0h	DCC calibration starting value for address slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_ADR_DC_WEIGHT_0	R/W	0h	DCC weighting factor base value for address slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_CAL_TIMEOUT_0	R/W	0h	DCC number of iterations to wait before timeout for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_CAL_SAMPLE_WAIT_0	R/W	0h	DCC cycles to wait after calibration change before sampling results for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1503 EMIF_CTLCFG_DENALI_PHY_1059 Register

1 EMIF_CTLCFG_DENALI_PHY_1059 Register (Offset = 508Ch) [reset = 0h]

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Table 14-24453. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D08Ch**

Figure 14-8116. EMIF_CTLCFG_DENALI_PHY_1059 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DC_CAL_POLARITY_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_DC_ADJUST_DIRECT_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADJUST_THRSHLD_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_ADJUST_SAMPLE_CNT_0							
R/W							
0h							

Table 14-24455. EMIF_CTLCFG_DENALI_PHY_1059 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DC_CAL_POLARITY_0	R/W	0h	DCC calibration polarity for address slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_DC_ADJUST_DIRECT_0	R/W	0h	DCC adjust direction for address slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADJUST_THRSHLD_0	R/W	0h	DCC adjust threshold around the mid-point for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADJUST_SAMPLE_CNT_0	R/W	0h	DCC number of samples to take for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1504 EMIF_CTLCFG_DENALI_PHY_1060 Register

1 EMIF_CTLCFG_DENALI_PHY_1060 Register (Offset = 5090h) [reset = 0h]

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Table 14-24456. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D090h**

Figure 14-8117. EMIF_CTLCFG_DENALI_PHY_1060 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_SW_TXPWR_CTRL_0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CAL_START_0
NONE							R/W
0h							0h

Table 14-24458. EMIF_CTLCFG_DENALI_PHY_1060 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_SW_TXPWR_CTRL_0	R/W	0h	Disable address output enables in deep sleep mode for address slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CAL_START_0	R/W	0h	DCC Manual trigger for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1505 EMIF_CTLCFG_DENALI_PHY_1061 Register

1 EMIF_CTLCFG_DENALI_PHY_1061 Register (Offset = 5094h) [reset = 0h]

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Table 14-24459. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D094h**

Figure 14-8118. EMIF_CTLCFG_DENALI_PHY_1061 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_IO_CFG_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ADR_IO_CFG_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_DC_CAL_CLK_SEL_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_0							
R/W							
0h							

Table 14-24461. EMIF_CTLCFG_DENALI_PHY_1061 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_PAD_ADR_IO_CFG_0	R/W	0h	Controls I/O pads for address pad for address slice 0. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_DC_CAL_CLK_SEL_0	R/W	0h	DCC CAL clock for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_0	R/W	0h	Tsel select values for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1506 EMIF_CTLCFG_DENALI_PHY_1062 Register

1 EMIF_CTLCFG_DENALI_PHY_1062 Register (Offset = 5098h) [reset = 0h]

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Table 14-24462. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D098h

Figure 14-8119. EMIF_CTLCFG_DENALI_PHY_1062 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR0_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_ADR0_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_PAD_ADR_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		

Table 14-24464. EMIF_CTLCFG_DENALI_PHY_1062 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR0_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 0 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_ADR0_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_PAD_ADR_RX_PCLK_CLK_SEL_0	R/W	0h	Reserved for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1507 EMIF_CTLCFG_DENALI_PHY_1063 Register

1 EMIF_CTLCFG_DENALI_PHY_1063 Register (Offset = 509Ch) [reset = 0h]

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Table 14-24465. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D09Ch**

Figure 14-8120. EMIF_CTLCFG_DENALI_PHY_1063 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR2_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR1_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR1_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				

Table 14-24467. EMIF_CTLCFG_DENALI_PHY_1063 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR2_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR1_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 1 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR1_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1508 EMIF_CTLCFG_DENALI_PHY_1064 Register

1 EMIF_CTLCFG_DENALI_PHY_1064 Register (Offset = 50A0h) [reset = 0h]

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Table 14-24468. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D0A0h

Figure 14-8121. EMIF_CTLCFG_DENALI_PHY_1064 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR3_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR2_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR2_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-24470. EMIF_CTLCFG_DENALI_PHY_1064 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 2 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1509 EMIF_CTLCFG_DENALI_PHY_1065 Register

1 EMIF_CTLCFG_DENALI_PHY_1065 Register (Offset = 50A4h) [reset = 0h]

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Table 14-24471. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D0A4h

Figure 14-8122. EMIF_CTLCFG_DENALI_PHY_1065 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR4_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR3_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-24473. EMIF_CTLCFG_DENALI_PHY_1065 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 3 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1510 EMIF_CTLCFG_DENALI_PHY_1066 Register

1 EMIF_CTLCFG_DENALI_PHY_1066 Register (Offset = 50A8h) [reset = 0h]

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Table 14-24474. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D0A8h

Figure 14-8123. EMIF_CTLCFG_DENALI_PHY_1066 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR5_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR4_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR4_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-24476. EMIF_CTLCFG_DENALI_PHY_1066 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 4 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1511 EMIF_CTLCFG_DENALI_PHY_1067 Register

1 EMIF_CTLCFG_DENALI_PHY_1067 Register (Offset = 50ACh) [reset = 0h]

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Table 14-24477. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D0ACh**

Figure 14-8124. EMIF_CTLCFG_DENALI_PHY_1067 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_SW_MASTER_MODE_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR5_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-24479. EMIF_CTLCFG_DENALI_PHY_1067 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_0	R/W	0h	Controller delay line override settings for address slice 0. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 5 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1512 EMIF_CTLCFG_DENALI_PHY_1068 Register

1 EMIF_CTLCFG_DENALI_PHY_1068 Register (Offset = 50B0h) [reset = 0h]

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Table 14-24480. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D0B0h

Figure 14-8125. EMIF_CTLCFG_DENALI_PHY_1068 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_MASTER_DELAY_STEP_0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DELAY_START_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_START_0							
R/W							
0h							

Table 14-24482. EMIF_CTLCFG_DENALI_PHY_1068 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 0. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_0	R/W	0h	Start value for controller delay line locking algorithm for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1513 EMIF_CTLCFG_DENALI_PHY_1069 Register

1 EMIF_CTLCFG_DENALI_PHY_1069 Register (Offset = 50B4h) [reset = 0h]

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Table 14-24483. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D0B4h**

Figure 14-8126. EMIF_CTLCFG_DENALI_PHY_1069 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_SW_CALVL_DVW_MIN_EN_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_SW_CALVL_DVW_MIN_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_SW_CALVL_DVW_MIN_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DELAY_HALF_MEASURE_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24485. EMIF_CTLCFG_DENALI_PHY_1069 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_0	R/W	0h	Enables the software override data valid window size during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_0	R/W	0h	Sets the software override data valid window size during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 0 Reset Source: ctl_amod_g_rst_n

14.6.6.2.1514 EMIF_CTLCFG_DENALI_PHY_1070 Register

1 EMIF_CTLCFG_DENALI_PHY_1070 Register (Offset = 50B8h) [reset = 0h]

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Table 14-24486. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D0B8h**

Figure 14-8127. EMIF_CTLCFG_DENALI_PHY_1070 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_0			
NONE				R/W			
0h				0h			

Table 14-24488. EMIF_CTLCFG_DENALI_PHY_1070 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_0	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1515 EMIF_CTLCFG_DENALI_PHY_1071 Register

1 EMIF_CTLCFG_DENALI_PHY_1071 Register (Offset = 50BCh) [reset = 0h]

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Table 14-24489. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D0BCh**

Figure 14-8128. EMIF_CTLCFG_DENALI_PHY_1071 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_DC_INIT_SLV_DELAY_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_DC_INIT_SLV_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_MEAS_DLY_STEP_ENABLE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_CAPTURE_CNT_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-24491. EMIF_CTLCFG_DENALI_PHY_1071 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_ADR_DC_INIT_SLV_DELAY_0	R/W	0h	DCC initialization value of write ADDR target delay for address slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1516 EMIF_CTLCFG_DENALI_PHY_1072 Register

1 EMIF_CTLCFG_DENALI_PHY_1072 Register (Offset = 50C0h) [reset = 0h]

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Table 14-24492. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D0C0h**

Figure 14-8129. EMIF_CTLCFG_DENALI_PHY_1072 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_DM_CLK_THRSHLD_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CALVL_ENABLE_0
NONE							R/W
0h							0h

Table 14-24494. EMIF_CTLCFG_DENALI_PHY_1072 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PHY_ADR_DC_DM_CLK_THRSHLD_0	R/W	0h	DCC clock measurement cell threshold offset for address slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CALVL_ENABLE_0	R/W	0h	DCC enable duty cycle adjust during CA leveling for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1517 EMIF_CTLCFG_DENALI_PHY_1280 Register

1 EMIF_CTLCFG_DENALI_PHY_1280 Register (Offset = 5400h) [reset = 0h]

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Table 14-24495. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D400h**

Figure 14-8130. EMIF_CTLCFG_DENALI_PHY_1280 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">SC_PHY_ADR_MANUAL_CLEAR_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CLK_BYPASS_OVERRIDE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24497. EMIF_CTLCFG_DENALI_PHY_1280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_1	W	0h	Manual reset/clear of internal logic for address slice 1. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_1	R/W	0h	Bypass mode override setting for address slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1518 EMIF_CTLCFG_DENALI_PHY_1281 Register

1 EMIF_CTLCFG_DENALI_PHY_1281 Register (Offset = 5404h) [reset = 1000h]

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Table 14-24498. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D404h**

Figure 14-8131. EMIF_CTLCFG_DENALI_PHY_1281 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							

Table 14-24500. EMIF_CTLCFG_DENALI_PHY_1281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_1	R	1000h	Observation register containing loopback status/results for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1519 EMIF_CTLCFG_DENALI_PHY_1282 Register

1 EMIF_CTLCFG_DENALI_PHY_1282 Register (Offset = 5408h) [reset = 0h]

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Table 14-24501. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D408h**

Figure 14-8132. EMIF_CTLCFG_DENALI_PHY_1282 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_MEAS_DLY_STEP_VALUE_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_ERROR_COUNT_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_ERROR_COUNT_OBS_1							
R							
0h							

Table 14-24503. EMIF_CTLCFG_DENALI_PHY_1282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_1	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_1	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_1	R	0h	Observation register containing total number of loopback error data for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1520 EMIF_CTLCFG_DENALI_PHY_1283 Register

1 EMIF_CTLCFG_DENALI_PHY_1283 Register (Offset = 540Ch) [reset = 0h]

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Table 14-24504. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D40Ch**

Figure 14-8133. EMIF_CTLCFG_DENALI_PHY_1283 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_ADR_ADDER_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_ADR_BASE_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_MASTER_DLY_LOCK_OBS_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DLY_LOCK_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24506. EMIF_CTLCFG_DENALI_PHY_1283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing addr target delay for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing base target delay for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_1	R	0h	Observation register containing controller delay results for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1521 EMIF_CTLCFG_DENALI_PHY_1284 Register

1 EMIF_CTLCFG_DENALI_PHY_1284 Register (Offset = 5410h) [reset = 0h]

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Table 14-24507. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D410h

Figure 14-8134. EMIF_CTLCFG_DENALI_PHY_1284 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_1
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_1		
NONE					R/W		
0h					0h		

Table 14-24509. EMIF_CTLCFG_DENALI_PHY_1284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_1	R/W	0h	Enables tsel_en for address slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_1	W	0h	Initiates a snapshot of the internal observation registers for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_1	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 1. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_1	R/W	0h	Reserved for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1522 EMIF_CTLCFG_DENALI_PHY_1285 Register

1 EMIF_CTLCFG_DENALI_PHY_1285 Register (Offset = 5414h) [reset = 100h]

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Table 14-24510. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D414h**

Figure 14-8135. EMIF_CTLCFG_DENALI_PHY_1285 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_ADR_PRBS_PATTERN_START_1						
NONE	R/W						
0h	1h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_ADR_LPBK_CONTROL_1						
NONE	R/W						
0h	0h						

Table 14-24512. EMIF_CTLCFG_DENALI_PHY_1285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_1	R/W	0h	Power reduction disable for address slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_1	R/W	0h	PRBS7 mask signal for address slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_1	R/W	1h	PRBS7 start pattern for address slice 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_1	R/W	0h	Loopback control bits for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1523 EMIF_CTLCFG_DENALI_PHY_1286 Register

1 EMIF_CTLCFG_DENALI_PHY_1286 Register (Offset = 5418h) [reset = 0h]

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Table 14-24513. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D418h**

Figure 14-8136. EMIF_CTLCFG_DENALI_PHY_1286 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_1		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_TYPE_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h

Table 14-24515. EMIF_CTLCFG_DENALI_PHY_1286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_1	R/W	0h	Input enable control for address slice 1. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_1	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_1	R/W	0h	DRAM type for address slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_1	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1524 EMIF_CTLCFG_DENALI_PHY_1287 Register

1 EMIF_CTLCFG_DENALI_PHY_1287 Register (Offset = 541Ch) [reset = 0h]

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Table 14-24516. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D41Ch**

Figure 14-8137. EMIF_CTLCFG_DENALI_PHY_1287 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_MODE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_MODE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_MODE_1							
R/W							
0h							

Table 14-24518. EMIF_CTLCFG_DENALI_PHY_1287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_1	R/W	0h	DDL mode for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1525 EMIF_CTLCFG_DENALI_PHY_1288 Register

1 EMIF_CTLCFG_DENALI_PHY_1288 Register (Offset = 5420h) [reset = 0h]

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Table 14-24519. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D420h**

Figure 14-8138. EMIF_CTLCFG_DENALI_PHY_1288 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_DDL_MASK_1					
NONE		R/W					
0h		0h					

Table 14-24521. EMIF_CTLCFG_DENALI_PHY_1288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_1	R/W	0h	DDL mask for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1526 EMIF_CTLCFG_DENALI_PHY_1289 Register

1 EMIF_CTLCFG_DENALI_PHY_1289 Register (Offset = 5424h) [reset = 0h]

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Table 14-24522. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D424h

Figure 14-8139. EMIF_CTLCFG_DENALI_PHY_1289 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							

Table 14-24524. EMIF_CTLCFG_DENALI_PHY_1289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_1	R	0h	Observation register containing DDL test bits for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1527 EMIF_CTLCFG_DENALI_PHY_1290 Register

1 EMIF_CTLCFG_DENALI_PHY_1290 Register (Offset = 5428h) [reset = 0h]

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Table 14-24525. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D428h**

Figure 14-8140. EMIF_CTLCFG_DENALI_PHY_1290 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							

Table 14-24527. EMIF_CTLCFG_DENALI_PHY_1290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1	R	0h	Observation register containing controller DDL bits for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1528 EMIF_CTLCFG_DENALI_PHY_1291 Register

1 EMIF_CTLCFG_DENALI_PHY_1291 Register (Offset = 542Ch) [reset = 0h]

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Table 14-24528. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D42Ch**

Figure 14-8141. EMIF_CTLCFG_DENALI_PHY_1291 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_COARSE_DLY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_COARSE_DLY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_START_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_START_1							
R/W							
0h							

Table 14-24530. EMIF_CTLCFG_DENALI_PHY_1291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_1	R/W	0h	Coarse CA training DDL increment value for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_1	R/W	0h	CA training DDL start value for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1529 EMIF_CTLCFG_DENALI_PHY_1292 Register

1 EMIF_CTLCFG_DENALI_PHY_1292 Register (Offset = 5430h) [reset = 0h]

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Table 14-24531. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D430h**

Figure 14-8142. EMIF_CTLCFG_DENALI_PHY_1292 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_QTR_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_QTR_1							
R/W							
0h							

Table 14-24533. EMIF_CTLCFG_DENALI_PHY_1292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_1	R/W	0h	CA training DDL quarter cycle delay value for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1530 EMIF_CTLCFG_DENALI_PHY_1293 Register

1 EMIF_CTLCFG_DENALI_PHY_1293 Register (Offset = 5434h) [reset = 0h]

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Table 14-24534. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D434h**

Figure 14-8143. EMIF_CTLCFG_DENALI_PHY_1293 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							

Table 14-24536. EMIF_CTLCFG_DENALI_PHY_1293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_1	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1531 EMIF_CTLCFG_DENALI_PHY_1294 Register

1 EMIF_CTLCFG_DENALI_PHY_1294 Register (Offset = 5438h) [reset = 0h]

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Table 14-24537. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D438h**

Figure 14-8144. EMIF_CTLCFG_DENALI_PHY_1294 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							

Table 14-24539. EMIF_CTLCFG_DENALI_PHY_1294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_1	R/W	0h	CA training rank aggregation control bits for address slice 1. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_1	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1532 EMIF_CTLCFG_DENALI_PHY_1295 Register

1 EMIF_CTLCFG_DENALI_PHY_1295 Register (Offset = 543Ch) [reset = 0h]

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Table 14-24540. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D43Ch**

Figure 14-8145. EMIF_CTLCFG_DENALI_PHY_1295 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CALVL_PERIODIC_START_OFFSET_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_PERIODIC_START_OFFSET_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_RESP_WAIT_CNT_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_CALVL_NUM_PATTERNS_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24542. EMIF_CTLCFG_DENALI_PHY_1295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_1	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_1	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_1	R/W	0h	Number of patterns to use during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1533 EMIF_CTLCFG_DENALI_PHY_1296 Register

1 EMIF_CTLCFG_DENALI_PHY_1296 Register (Offset = 5440h) [reset = 0h]

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Table 14-24543. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D440h

Figure 14-8146. EMIF_CTLCFG_DENALI_PHY_1296 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_1
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_1
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_1
NONE							R/W
0h							0h

Table 14-24545. EMIF_CTLCFG_DENALI_PHY_1296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_1	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_1	W	0h	Clears the CA training state machine error status for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_1	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-24545. EMIF_CTLCFG_DENALI_PHY_1296 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_1	R/W	0h	Enables CA training debug mode for address slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1534 EMIF_CTLCFG_DENALI_PHY_1297 Register

1 EMIF_CTLCFG_DENALI_PHY_1297 Register (Offset = 5444h) [reset = 0h]

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Table 14-24546. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D444h**

Figure 14-8147. EMIF_CTLCFG_DENALI_PHY_1297 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH0_OBS0_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_CH0_OBS0_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_CH0_OBS0_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH0_OBS0_1							
R							
0h							

Table 14-24548. EMIF_CTLCFG_DENALI_PHY_1297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH0_OBS0_1	R	0h	Observation register for CA training for channel 0 slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1535 EMIF_CTLCFG_DENALI_PHY_1298 Register

1 EMIF_CTLCFG_DENALI_PHY_1298 Register (Offset = 5448h) [reset = 0h]

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Table 14-24549. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D448h**

Figure 14-8148. EMIF_CTLCFG_DENALI_PHY_1298 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH1_OBS0_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_CH1_OBS0_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_CH1_OBS0_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH1_OBS0_1							
R							
0h							

Table 14-24551. EMIF_CTLCFG_DENALI_PHY_1298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH1_OBS0_1	R	0h	Observation register for CA training for channel 1 slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1536 EMIF_CTLCFG_DENALI_PHY_1299 Register

1 EMIF_CTLCFG_DENALI_PHY_1299 Register (Offset = 544Ch) [reset = 0h]

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Table 14-24552. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D44Ch**

Figure 14-8149. EMIF_CTLCFG_DENALI_PHY_1299 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_1							
R							
0h							

Table 14-24554. EMIF_CTLCFG_DENALI_PHY_1299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_1	R	0h	Observation register contains general CA training bits for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1537 EMIF_CTLCFG_DENALI_PHY_1300 Register

1 EMIF_CTLCFG_DENALI_PHY_1300 Register (Offset = 5450h) [reset = 100h]

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Table 14-24555. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D450h**

Figure 14-8150. EMIF_CTLCFG_DENALI_PHY_1300 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS2_1							
R							
100h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS2_1							
R							
100h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS2_1							
R							
100h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_1							
R							
100h							

Table 14-24557. EMIF_CTLCFG_DENALI_PHY_1300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_1	R	100h	Observation register contains periodic CA training bits for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1538 EMIF_CTLCFG_DENALI_PHY_1301 Register

1 EMIF_CTLCFG_DENALI_PHY_1301 Register (Offset = 5454h) [reset = 0h]

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Table 14-24558. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D454h**

Figure 14-8151. EMIF_CTLCFG_DENALI_PHY_1301 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_0_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_0_1							
R/W							
0h							

Table 14-24560. EMIF_CTLCFG_DENALI_PHY_1301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_1	R/W	0h	CA training foreground pattern 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1539 EMIF_CTLCFG_DENALI_PHY_1302 Register

1 EMIF_CTLCFG_DENALI_PHY_1302 Register (Offset = 5458h) [reset = 0h]

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Table 14-24561. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D458h

Figure 14-8152. EMIF_CTLCFG_DENALI_PHY_1302 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_0_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_0_1							
R/W							
0h							

Table 14-24563. EMIF_CTLCFG_DENALI_PHY_1302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_1	R/W	0h	CA training background pattern 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1540 EMIF_CTLCFG_DENALI_PHY_1303 Register

1 EMIF_CTLCFG_DENALI_PHY_1303 Register (Offset = 545Ch) [reset = 0h]

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Table 14-24564. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D45Ch**

Figure 14-8153. EMIF_CTLCFG_DENALI_PHY_1303 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_1_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_1_1							
R/W							
0h							

Table 14-24566. EMIF_CTLCFG_DENALI_PHY_1303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_1	R/W	0h	CA training foreground pattern 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1541 EMIF_CTLCFG_DENALI_PHY_1304 Register

1 EMIF_CTLCFG_DENALI_PHY_1304 Register (Offset = 5460h) [reset = 0h]

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Table 14-24567. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D460h**

Figure 14-8154. EMIF_CTLCFG_DENALI_PHY_1304 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_1_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_1_1							
R/W							
0h							

Table 14-24569. EMIF_CTLCFG_DENALI_PHY_1304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_1	R/W	0h	CA training background pattern 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1542 EMIF_CTLCFG_DENALI_PHY_1305 Register

1 EMIF_CTLCFG_DENALI_PHY_1305 Register (Offset = 5464h) [reset = 0h]

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Table 14-24570. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D464h**

Figure 14-8155. EMIF_CTLCFG_DENALI_PHY_1305 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_2_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_2_1							
R/W							
0h							

Table 14-24572. EMIF_CTLCFG_DENALI_PHY_1305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_1	R/W	0h	CA training foreground pattern 2 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1543 EMIF_CTLCFG_DENALI_PHY_1306 Register

1 EMIF_CTLCFG_DENALI_PHY_1306 Register (Offset = 5468h) [reset = 0h]

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Table 14-24573. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D468h

Figure 14-8156. EMIF_CTLCFG_DENALI_PHY_1306 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_2_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_2_1							
R/W							
0h							

Table 14-24575. EMIF_CTLCFG_DENALI_PHY_1306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_1	R/W	0h	CA training background pattern 2 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1544 EMIF_CTLCFG_DENALI_PHY_1307 Register

1 EMIF_CTLCFG_DENALI_PHY_1307 Register (Offset = 546Ch) [reset = 0h]

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Table 14-24576. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D46Ch**

Figure 14-8157. EMIF_CTLCFG_DENALI_PHY_1307 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_3_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_3_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_3_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24578. EMIF_CTLCFG_DENALI_PHY_1307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_1	R/W	0h	CA training foreground pattern 3 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1545 EMIF_CTLCFG_DENALI_PHY_1308 Register

1 EMIF_CTLCFG_DENALI_PHY_1308 Register (Offset = 5470h) [reset = 0h]

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Table 14-24579. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D470h**

Figure 14-8158. EMIF_CTLCFG_DENALI_PHY_1308 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_3_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_3_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_3_1							
R/W							
0h							

Table 14-24581. EMIF_CTLCFG_DENALI_PHY_1308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_1	R/W	0h	CA training background pattern 3 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1546 EMIF_CTLCFG_DENALI_PHY_1309 Register

1 EMIF_CTLCFG_DENALI_PHY_1309 Register (Offset = 5474h) [reset = 0h]

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Table 14-24582. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D474h**

Figure 14-8159. EMIF_CTLCFG_DENALI_PHY_1309 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PHY_ADR_ADDR_SEL_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_ADDR_SEL_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_ADDR_SEL_1							
R/W							
0h							

Table 14-24584. EMIF_CTLCFG_DENALI_PHY_1309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_1	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1547 EMIF_CTLCFG_DENALI_PHY_1310 Register

1 EMIF_CTLCFG_DENALI_PHY_1310 Register (Offset = 5478h) [reset = 0h]

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Table 14-24585. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D478h**

Figure 14-8160. EMIF_CTLCFG_DENALI_PHY_1310 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_ADR_BIT_MASK_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LP4_BOOT_SLV_DELAY_1							
R/W							
0h							

Table 14-24587. EMIF_CTLCFG_DENALI_PHY_1310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_1	R/W	0h	Segment mask bit for address slice 1. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_1	R/W	0h	Mask bit for address slice 1. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_1	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1548 EMIF_CTLCFG_DENALI_PHY_1311 Register

1 EMIF_CTLCFG_DENALI_PHY_1311 Register (Offset = 547Ch) [reset = 0h]

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Table 14-24588. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D47Ch**

Figure 14-8161. EMIF_CTLCFG_DENALI_PHY_1311 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_1					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_1					
NONE		R/W					
0h		0h					

Table 14-24590. EMIF_CTLCFG_DENALI_PHY_1311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_1	R/W	0h	Controls address pad output enable for address slice 1. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_1	R/W	0h	Toggle control during static activity for address slice 1. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_1	R/W	0h	Mask bit for CS training participation for address slice 1. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_1	R/W	0h	Mask bit for CA training participation for address slice 1. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1549 EMIF_CTLCFG_DENALI_PHY_1312 Register

1 EMIF_CTLCFG_DENALI_PHY_1312 Register (Offset = 5480h) [reset = 20202003h]

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Table 14-24591. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D480h

Figure 14-8162. EMIF_CTLCFG_DENALI_PHY_1312 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DC_ADR2_CLK_ADJUST_1							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DC_ADR1_CLK_ADJUST_1							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADR0_CLK_ADJUST_1							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_ADR_DC_INIT_DISABLE_1	
NONE						R/W	
0h						3h	

Table 14-24593. EMIF_CTLCFG_DENALI_PHY_1312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_DC_ADR2_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 2 for address slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR1_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 1 for address slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR0_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 0 for address slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_DC_INIT_DISABLE_1	R/W	3h	Duty Cycle Corrector disable at initialization for address slice 1. Set to 1 to disable, bit [1] controls data path, bit [0] controls clock path. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1550 EMIF_CTLCFG_DENALI_PHY_1313 Register

1 EMIF_CTLCFG_DENALI_PHY_1313 Register (Offset = 5484h) [reset = 202020h]

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Table 14-24594. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D484h**

Figure 14-8163. EMIF_CTLCFG_DENALI_PHY_1313 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR5_CLK_ADJUST_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR4_CLK_ADJUST_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_DC_ADR3_CLK_ADJUST_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-24596. EMIF_CTLCFG_DENALI_PHY_1313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_1	R/W	0h	DCC and RX_CAL clk gate disable for address slice 1. 1 = disable clk gate. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR5_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 5 for address slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR4_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 4 for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADR3_CLK_ADJUST_1	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 3 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1551 EMIF_CTLCFG_DENALI_PHY_1314 Register

1 EMIF_CTLCFG_DENALI_PHY_1314 Register (Offset = 5488h) [reset = 0h]

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Table 14-24597. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D488h**

Figure 14-8164. EMIF_CTLCFG_DENALI_PHY_1314 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_DC_ADJUST_START_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_DC_WEIGHT_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_CAL_TIMEOUT_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_CAL_SAMPLE_WAIT_1							
R/W							
0h							

Table 14-24599. EMIF_CTLCFG_DENALI_PHY_1314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_DC_ADJUST_START_1	R/W	0h	DCC calibration starting value for address slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_ADR_DC_WEIGHT_1	R/W	0h	DCC weighting factor base value for address slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_CAL_TIMEOUT_1	R/W	0h	DCC number of iterations to wait before timeout for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_CAL_SAMPLE_WAIT_1	R/W	0h	DCC cycles to wait after calibration change before sampling results for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1552 EMIF_CTLCFG_DENALI_PHY_1315 Register

1 EMIF_CTLCFG_DENALI_PHY_1315 Register (Offset = 548Ch) [reset = 0h]

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Table 14-24600. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D48Ch**

Figure 14-8165. EMIF_CTLCFG_DENALI_PHY_1315 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DC_CAL_POLARITY_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_DC_ADJUST_DIRECT_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADJUST_THRSHLD_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_ADJUST_SAMPLE_CNT_1							
R/W							
0h							

Table 14-24602. EMIF_CTLCFG_DENALI_PHY_1315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DC_CAL_POLARITY_1	R/W	0h	DCC calibration polarity for address slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_DC_ADJUST_DIRECT_1	R/W	0h	DCC adjust direction for address slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADJUST_THRSHLD_1	R/W	0h	DCC adjust threshold around the mid-point for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADJUST_SAMPLE_CNT_1	R/W	0h	DCC number of samples to take for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1553 EMIF_CTLCFG_DENALI_PHY_1316 Register

1 EMIF_CTLCFG_DENALI_PHY_1316 Register (Offset = 5490h) [reset = 0h]

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Table 14-24603. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D490h**

Figure 14-8166. EMIF_CTLCFG_DENALI_PHY_1316 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_SW_TXPWR_CTRL_1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CAL_START_1
NONE							R/W
0h							0h

Table 14-24605. EMIF_CTLCFG_DENALI_PHY_1316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_SW_TXPWR_CTRL_1	R/W	0h	Disable address output enables in deep sleep mode for address slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CAL_START_1	R/W	0h	DCC Manual trigger for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1554 EMIF_CTLCFG_DENALI_PHY_1317 Register

1 EMIF_CTLCFG_DENALI_PHY_1317 Register (Offset = 5494h) [reset = 0h]

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Table 14-24606. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D494h**

Figure 14-8167. EMIF_CTLCFG_DENALI_PHY_1317 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_IO_CFG_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ADR_IO_CFG_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_DC_CAL_CLK_SEL_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_1							
R/W							
0h							

Table 14-24608. EMIF_CTLCFG_DENALI_PHY_1317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_PAD_ADR_IO_CFG_1	R/W	0h	Controls I/O pads for address pad for address slice 1. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_DC_CAL_CLK_SEL_1	R/W	0h	DCC CAL clock for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_1	R/W	0h	Tsel select values for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1555 EMIF_CTLCFG_DENALI_PHY_1318 Register

1 EMIF_CTLCFG_DENALI_PHY_1318 Register (Offset = 5498h) [reset = 0h]

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Table 14-24609. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D498h**

Figure 14-8168. EMIF_CTLCFG_DENALI_PHY_1318 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_ADR0_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED			PHY_ADR0_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED					PHY_PAD_ADR_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		

Table 14-24611. EMIF_CTLCFG_DENALI_PHY_1318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR0_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 0 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_ADR0_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_PAD_ADR_RX_PCLK_CLK_SEL_1	R/W	0h	Reserved for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1556 EMIF_CTLCFG_DENALI_PHY_1319 Register

1 EMIF_CTLCFG_DENALI_PHY_1319 Register (Offset = 549Ch) [reset = 0h]

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Table 14-24612. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D49Ch**

Figure 14-8169. EMIF_CTLCFG_DENALI_PHY_1319 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR2_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR1_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR1_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				

Table 14-24614. EMIF_CTLCFG_DENALI_PHY_1319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR2_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR1_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 1 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR1_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1557 EMIF_CTLCFG_DENALI_PHY_1320 Register

1 EMIF_CTLCFG_DENALI_PHY_1320 Register (Offset = 54A0h) [reset = 0h]

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Table 14-24615. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4A0h**

Figure 14-8170. EMIF_CTLCFG_DENALI_PHY_1320 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR3_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR2_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR2_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-24617. EMIF_CTLCFG_DENALI_PHY_1320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 2 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1558 EMIF_CTLCFG_DENALI_PHY_1321 Register

1 EMIF_CTLCFG_DENALI_PHY_1321 Register (Offset = 54A4h) [reset = 0h]

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Table 14-24618. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4A4h**

Figure 14-8171. EMIF_CTLCFG_DENALI_PHY_1321 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR4_SW_WRADDR_SHIFT_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR3_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR3_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24620. EMIF_CTLCFG_DENALI_PHY_1321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 3 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1559 EMIF_CTLCFG_DENALI_PHY_1322 Register

1 EMIF_CTLCFG_DENALI_PHY_1322 Register (Offset = 54A8h) [reset = 0h]

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Table 14-24621. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4A8h**

Figure 14-8172. EMIF_CTLCFG_DENALI_PHY_1322 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR5_SW_WRADDR_SHIFT_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR4_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR4_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24623. EMIF_CTLCFG_DENALI_PHY_1322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 4 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1560 EMIF_CTLCFG_DENALI_PHY_1323 Register

1 EMIF_CTLCFG_DENALI_PHY_1323 Register (Offset = 54ACh) [reset = 0h]

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Table 14-24624. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D4ACh

Figure 14-8173. EMIF_CTLCFG_DENALI_PHY_1323 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_SW_MASTER_MODE_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR5_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-24626. EMIF_CTLCFG_DENALI_PHY_1323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_1	R/W	0h	Controller delay line override settings for address slice 1. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 5 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1561 EMIF_CTLCFG_DENALI_PHY_1324 Register

1 EMIF_CTLCFG_DENALI_PHY_1324 Register (Offset = 54B0h) [reset = 0h]

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Table 14-24627. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D4B0h

Figure 14-8174. EMIF_CTLCFG_DENALI_PHY_1324 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_MASTER_DELAY_STEP_1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DELAY_START_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_START_1							
R/W							
0h							

Table 14-24629. EMIF_CTLCFG_DENALI_PHY_1324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_1	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 1. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_1	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_1	R/W	0h	Start value for controller delay line locking algorithm for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1562 EMIF_CTLCFG_DENALI_PHY_1325 Register

1 EMIF_CTLCFG_DENALI_PHY_1325 Register (Offset = 54B4h) [reset = 0h]

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Table 14-24630. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4B4h**

Figure 14-8175. EMIF_CTLCFG_DENALI_PHY_1325 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_SW_CALVL_DVW_MIN_EN_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_SW_CALVL_DVW_MIN_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_SW_CALVL_DVW_MIN_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DELAY_HALF_MEASURE_1							
R/W							
0h							

Table 14-24632. EMIF_CTLCFG_DENALI_PHY_1325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_1	R/W	0h	Enables the software override data valid window size during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_1	R/W	0h	Sets the software override data valid window size during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_1	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 1 Reset Source: ctl_amod_g_rst_n

14.6.6.2.1563 EMIF_CTLCFG_DENALI_PHY_1326 Register

1 EMIF_CTLCFG_DENALI_PHY_1326 Register (Offset = 54B8h) [reset = 0h]

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Table 14-24633. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D4B8h

Figure 14-8176. EMIF_CTLCFG_DENALI_PHY_1326 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_1			
NONE				R/W			
0h				0h			

Table 14-24635. EMIF_CTLCFG_DENALI_PHY_1326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_1	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1564 EMIF_CTLCFG_DENALI_PHY_1327 Register

1 EMIF_CTLCFG_DENALI_PHY_1327 Register (Offset = 54BCh) [reset = 0h]

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Table 14-24636. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4BCh**

Figure 14-8177. EMIF_CTLCFG_DENALI_PHY_1327 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_DC_INIT_SLV_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DC_INIT_SLV_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_ADR_MEAS_DLY_STEP_ENABLE_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_1			
NONE				R/W			
0h				0h			

Table 14-24638. EMIF_CTLCFG_DENALI_PHY_1327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_ADR_DC_INIT_SLV_DELAY_1	R/W	0h	DCC initialization value of write ADDR target delay for address slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_1	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1565 EMIF_CTLCFG_DENALI_PHY_1328 Register

1 EMIF_CTLCFG_DENALI_PHY_1328 Register (Offset = 54C0h) [reset = 0h]

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Table 14-24639. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D4C0h**

Figure 14-8178. EMIF_CTLCFG_DENALI_PHY_1328 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_DM_CLK_THRSHLD_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CALVL_ENABLE_1
NONE							R/W
0h							0h

Table 14-24641. EMIF_CTLCFG_DENALI_PHY_1328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PHY_ADR_DC_DM_CLK_THRSHLD_1	R/W	0h	DCC clock measurement cell threshold offset for address slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CALVL_ENABLE_1	R/W	0h	DCC enable duty cycle adjust during CA leveling for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1566 EMIF_CTLCFG_DENALI_PHY_1536 Register

1 EMIF_CTLCFG_DENALI_PHY_1536 Register (Offset = 5800h) [reset = 0h]

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Table 14-24642. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D800h**

Figure 14-8179. EMIF_CTLCFG_DENALI_PHY_1536 Name Register

31	30	29	28	27	26	25	24
RESERVED					SC_PHY_ADR_MANUAL_CLEAR_2		
NONE					W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_CLK_BYPASS_OVERRIDE_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2							
R/W							
0h							

Table 14-24644. EMIF_CTLCFG_DENALI_PHY_1536 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_2	W	0h	Manual reset/clear of internal logic for address slice 2. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_2	R/W	0h	Bypass mode override setting for address slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1567 EMIF_CTLCFG_DENALI_PHY_1537 Register

1 EMIF_CTLCFG_DENALI_PHY_1537 Register (Offset = 5804h) [reset = 1000h]

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Table 14-24645. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D804h**

Figure 14-8180. EMIF_CTLCFG_DENALI_PHY_1537 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							

Table 14-24647. EMIF_CTLCFG_DENALI_PHY_1537 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_2	R	1000h	Observation register containing loopback status/results for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1568 EMIF_CTLCFG_DENALI_PHY_1538 Register

1 EMIF_CTLCFG_DENALI_PHY_1538 Register (Offset = 5808h) [reset = 0h]

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Table 14-24648. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D808h**

Figure 14-8181. EMIF_CTLCFG_DENALI_PHY_1538 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_MEAS_DLY_STEP_VALUE_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_ERROR_COUNT_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_ERROR_COUNT_OBS_2							
R							
0h							

Table 14-24650. EMIF_CTLCFG_DENALI_PHY_1538 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_2	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_2	R	0h	Observation register containing total number of loopback error data for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1569 EMIF_CTLCFG_DENALI_PHY_1539 Register

1 EMIF_CTLCFG_DENALI_PHY_1539 Register (Offset = 580Ch) [reset = 0h]

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Table 14-24651. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D80Ch**

Figure 14-8182. EMIF_CTLCFG_DENALI_PHY_1539 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_ADDER_SLV_DLY_ENC_OBS_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_ADR_BASE_SLV_DLY_ENC_OBS_2						
NONE	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_MASTER_DLY_LOCK_OBS_2		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DLY_LOCK_OBS_2							
R							
0h							

Table 14-24653. EMIF_CTLCFG_DENALI_PHY_1539 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing addr target delay for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing base target delay for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_2	R	0h	Observation register containing controller delay results for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1570 EMIF_CTLCFG_DENALI_PHY_1540 Register

1 EMIF_CTLCFG_DENALI_PHY_1540 Register (Offset = 5810h) [reset = 0h]

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Table 14-24654. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D810h**

Figure 14-8183. EMIF_CTLCFG_DENALI_PHY_1540 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_2
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_2		
NONE					R/W		
0h					0h		

Table 14-24656. EMIF_CTLCFG_DENALI_PHY_1540 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_2	R/W	0h	Enables tsel_en for address slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_2	W	0h	Initiates a snapshot of the internal observation registers for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_2	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 2. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_2	R/W	0h	Reserved for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1571 EMIF_CTLCFG_DENALI_PHY_1541 Register

1 EMIF_CTLCFG_DENALI_PHY_1541 Register (Offset = 5814h) [reset = 100h]

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Table 14-24657. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D814h**

Figure 14-8184. EMIF_CTLCFG_DENALI_PHY_1541 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_ADR_PRBS_PATTERN_START_2						
NONE	R/W						
0h	1h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_ADR_LPBK_CONTROL_2						
NONE	R/W						
0h	0h						

Table 14-24659. EMIF_CTLCFG_DENALI_PHY_1541 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_2	R/W	0h	Power reduction disable for address slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_2	R/W	0h	PRBS7 mask signal for address slice 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_2	R/W	1h	PRBS7 start pattern for address slice 2. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_2	R/W	0h	Loopback control bits for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1572 EMIF_CTLCFG_DENALI_PHY_1542 Register

1 EMIF_CTLCFG_DENALI_PHY_1542 Register (Offset = 5818h) [reset = 0h]

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Table 14-24660. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D818h**

Figure 14-8185. EMIF_CTLCFG_DENALI_PHY_1542 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_2		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_TYPE_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_2
NONE							R/W
0h							0h

Table 14-24662. EMIF_CTLCFG_DENALI_PHY_1542 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_2	R/W	0h	Input enable control for address slice 2. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_2	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_2	R/W	0h	DRAM type for address slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_2	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1573 EMIF_CTLCFG_DENALI_PHY_1543 Register

1 EMIF_CTLCFG_DENALI_PHY_1543 Register (Offset = 581Ch) [reset = 0h]

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Table 14-24663. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D81Ch**

Figure 14-8186. EMIF_CTLCFG_DENALI_PHY_1543 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_MODE_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_MODE_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_MODE_2							
R/W							
0h							

Table 14-24665. EMIF_CTLCFG_DENALI_PHY_1543 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_2	R/W	0h	DDL mode for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1574 EMIF_CTLCFG_DENALI_PHY_1544 Register

1 EMIF_CTLCFG_DENALI_PHY_1544 Register (Offset = 5820h) [reset = 0h]

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Table 14-24666. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D820h**

Figure 14-8187. EMIF_CTLCFG_DENALI_PHY_1544 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_DDL_MASK_2					
NONE		R/W					
0h		0h					

Table 14-24668. EMIF_CTLCFG_DENALI_PHY_1544 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_2	R/W	0h	DDL mask for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1575 EMIF_CTLCFG_DENALI_PHY_1545 Register

1 EMIF_CTLCFG_DENALI_PHY_1545 Register (Offset = 5824h) [reset = 0h]

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Table 14-24669. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D824h**

Figure 14-8188. EMIF_CTLCFG_DENALI_PHY_1545 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							

Table 14-24671. EMIF_CTLCFG_DENALI_PHY_1545 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_2	R	0h	Observation register containing DDL test bits for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1576 EMIF_CTLCFG_DENALI_PHY_1546 Register

1 EMIF_CTLCFG_DENALI_PHY_1546 Register (Offset = 5828h) [reset = 0h]

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Table 14-24672. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 D828h**

Figure 14-8189. EMIF_CTLCFG_DENALI_PHY_1546 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							

Table 14-24674. EMIF_CTLCFG_DENALI_PHY_1546 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2	R	0h	Observation register containing controller DDL bits for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1577 EMIF_CTLCFG_DENALI_PHY_1547 Register

1 EMIF_CTLCFG_DENALI_PHY_1547 Register (Offset = 582Ch) [reset = 0h]

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Table 14-24675. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D82Ch**

Figure 14-8190. EMIF_CTLCFG_DENALI_PHY_1547 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CALVL_COARSE_DLY_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_COARSE_DLY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CALVL_START_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_START_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24677. EMIF_CTLCFG_DENALI_PHY_1547 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_2	R/W	0h	Coarse CA training DDL increment value for address slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_2	R/W	0h	CA training DDL start value for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1578 EMIF_CTLCFG_DENALI_PHY_1548 Register

1 EMIF_CTLCFG_DENALI_PHY_1548 Register (Offset = 5830h) [reset = 0h]

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Table 14-24678. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D830h**

Figure 14-8191. EMIF_CTLCFG_DENALI_PHY_1548 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_QTR_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_QTR_2							
R/W							
0h							

Table 14-24680. EMIF_CTLCFG_DENALI_PHY_1548 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_2	R/W	0h	CA training DDL quarter cycle delay value for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1579 EMIF_CTLCFG_DENALI_PHY_1549 Register

1 EMIF_CTLCFG_DENALI_PHY_1549 Register (Offset = 5834h) [reset = 0h]

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Table 14-24681. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D834h**

Figure 14-8192. EMIF_CTLCFG_DENALI_PHY_1549 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							

Table 14-24683. EMIF_CTLCFG_DENALI_PHY_1549 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_2	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1580 EMIF_CTLCFG_DENALI_PHY_1550 Register

1 EMIF_CTLCFG_DENALI_PHY_1550 Register (Offset = 5838h) [reset = 0h]

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Table 14-24684. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D838h**

Figure 14-8193. EMIF_CTLCFG_DENALI_PHY_1550 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							

Table 14-24686. EMIF_CTLCFG_DENALI_PHY_1550 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_2	R/W	0h	CA training rank aggregation control bits for address slice 2. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_2	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1581 EMIF_CTLCFG_DENALI_PHY_1551 Register

1 EMIF_CTLCFG_DENALI_PHY_1551 Register (Offset = 583Ch) [reset = 0h]

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Table 14-24687. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D83Ch**

Figure 14-8194. EMIF_CTLCFG_DENALI_PHY_1551 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_CALVL_PERIODIC_START_OFFSET_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_PERIODIC_START_OFFSET_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_ADR_CALVL_RESP_WAIT_CNT_2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_CALVL_NUM_PATTERNS_2	
NONE						R/W	
0h						0h	

Table 14-24689. EMIF_CTLCFG_DENALI_PHY_1551 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_2	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_2	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_2	R/W	0h	Number of patterns to use during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1582 EMIF_CTLCFG_DENALI_PHY_1552 Register

1 EMIF_CTLCFG_DENALI_PHY_1552 Register (Offset = 5840h) [reset = 0h]

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Table 14-24690. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D840h

Figure 14-8195. EMIF_CTLCFG_DENALI_PHY_1552 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_2
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_2
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_2
NONE							R/W
0h							0h

Table 14-24692. EMIF_CTLCFG_DENALI_PHY_1552 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_2	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_2	W	0h	Clears the CA training state machine error status for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_2	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-24692. EMIF_CTLCFG_DENALI_PHY_1552 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_2	R/W	0h	Enables CA training debug mode for address slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1583 EMIF_CTLCFG_DENALI_PHY_1553 Register

1 EMIF_CTLCFG_DENALI_PHY_1553 Register (Offset = 5844h) [reset = 0h]

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Table 14-24693. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D844h**

Figure 14-8196. EMIF_CTLCFG_DENALI_PHY_1553 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH0_OBS0_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_CH0_OBS0_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_CH0_OBS0_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH0_OBS0_2							
R							
0h							

Table 14-24695. EMIF_CTLCFG_DENALI_PHY_1553 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH0_OBS0_2	R	0h	Observation register for CA training for channel 0 slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1584 EMIF_CTLCFG_DENALI_PHY_1554 Register

1 EMIF_CTLCFG_DENALI_PHY_1554 Register (Offset = 5848h) [reset = 0h]

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Table 14-24696. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D848h**

Figure 14-8197. EMIF_CTLCFG_DENALI_PHY_1554 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_CH1_OBS0_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_CH1_OBS0_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_CH1_OBS0_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_CH1_OBS0_2							
R							
0h							

Table 14-24698. EMIF_CTLCFG_DENALI_PHY_1554 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_CH1_OBS0_2	R	0h	Observation register for CA training for channel 1 slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1585 EMIF_CTLCFG_DENALI_PHY_1555 Register

1 EMIF_CTLCFG_DENALI_PHY_1555 Register (Offset = 584Ch) [reset = 0h]

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Table 14-24699. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D84Ch**

Figure 14-8198. EMIF_CTLCFG_DENALI_PHY_1555 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_2							
R							
0h							

Table 14-24701. EMIF_CTLCFG_DENALI_PHY_1555 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_2	R	0h	Observation register contains general CA training bits for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1586 EMIF_CTLCFG_DENALI_PHY_1556 Register

1 EMIF_CTLCFG_DENALI_PHY_1556 Register (Offset = 5850h) [reset = 100h]

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Table 14-24702. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 D850h**

Figure 14-8199. EMIF_CTLCFG_DENALI_PHY_1556 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS2_2							
R							
100h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS2_2							
R							
100h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS2_2							
R							
100h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_2							
R							
100h							

Table 14-24704. EMIF_CTLCFG_DENALI_PHY_1556 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_2	R	100h	Observation register contains periodic CA training bits for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1587 EMIF_CTLCFG_DENALI_PHY_1557 Register

1 EMIF_CTLCFG_DENALI_PHY_1557 Register (Offset = 5854h) [reset = 0h]

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Table 14-24705. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 D854h**

Figure 14-8200. EMIF_CTLCFG_DENALI_PHY_1557 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24707. EMIF_CTLCFG_DENALI_PHY_1557 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_2	R/W	0h	CA training foreground pattern 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1588 EMIF_CTLCFG_DENALI_PHY_1558 Register

1 EMIF_CTLCFG_DENALI_PHY_1558 Register (Offset = 5858h) [reset = 0h]

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Table 14-24708. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D858h**

Figure 14-8201. EMIF_CTLCFG_DENALI_PHY_1558 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_BG_0_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24710. EMIF_CTLCFG_DENALI_PHY_1558 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_2	R/W	0h	CA training background pattern 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1589 EMIF_CTLCFG_DENALI_PHY_1559 Register

1 EMIF_CTLCFG_DENALI_PHY_1559 Register (Offset = 585Ch) [reset = 0h]

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Table 14-24711. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D85Ch

Figure 14-8202. EMIF_CTLCFG_DENALI_PHY_1559 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_1_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_1_2							
R/W							
0h							

Table 14-24713. EMIF_CTLCFG_DENALI_PHY_1559 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_2	R/W	0h	CA training foreground pattern 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1590 EMIF_CTLCFG_DENALI_PHY_1560 Register

1 EMIF_CTLCFG_DENALI_PHY_1560 Register (Offset = 5860h) [reset = 0h]

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Table 14-24714. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D860h**

Figure 14-8203. EMIF_CTLCFG_DENALI_PHY_1560 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_1_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_1_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_1_2							
R/W							
0h							

Table 14-24716. EMIF_CTLCFG_DENALI_PHY_1560 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_2	R/W	0h	CA training background pattern 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1591 EMIF_CTLCFG_DENALI_PHY_1561 Register

1 EMIF_CTLCFG_DENALI_PHY_1561 Register (Offset = 5864h) [reset = 0h]

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Table 14-24717. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D864h**

Figure 14-8204. EMIF_CTLCFG_DENALI_PHY_1561 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_2_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_2_2							
R/W							
0h							

Table 14-24719. EMIF_CTLCFG_DENALI_PHY_1561 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_2	R/W	0h	CA training foreground pattern 2 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1592 EMIF_CTLCFG_DENALI_PHY_1562 Register

1 EMIF_CTLCFG_DENALI_PHY_1562 Register (Offset = 5868h) [reset = 0h]

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Table 14-24720. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D868h**

Figure 14-8205. EMIF_CTLCFG_DENALI_PHY_1562 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_2_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_2_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_2_2							
R/W							
0h							

Table 14-24722. EMIF_CTLCFG_DENALI_PHY_1562 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_2	R/W	0h	CA training background pattern 2 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1593 EMIF_CTLCFG_DENALI_PHY_1563 Register

1 EMIF_CTLCFG_DENALI_PHY_1563 Register (Offset = 586Ch) [reset = 0h]

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Table 14-24723. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D86Ch**

Figure 14-8206. EMIF_CTLCFG_DENALI_PHY_1563 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_3_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_3_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_3_2							
R/W							
0h							

Table 14-24725. EMIF_CTLCFG_DENALI_PHY_1563 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_2	R/W	0h	CA training foreground pattern 3 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1594 EMIF_CTLCFG_DENALI_PHY_1564 Register

1 EMIF_CTLCFG_DENALI_PHY_1564 Register (Offset = 5870h) [reset = 0h]

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Table 14-24726. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D870h**

Figure 14-8207. EMIF_CTLCFG_DENALI_PHY_1564 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_3_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_3_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_3_2							
R/W							
0h							

Table 14-24728. EMIF_CTLCFG_DENALI_PHY_1564 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_2	R/W	0h	CA training background pattern 3 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1595 EMIF_CTLCFG_DENALI_PHY_1565 Register

1 EMIF_CTLCFG_DENALI_PHY_1565 Register (Offset = 5874h) [reset = 0h]

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Table 14-24729. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D874h**

Figure 14-8208. EMIF_CTLCFG_DENALI_PHY_1565 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							

Table 14-24731. EMIF_CTLCFG_DENALI_PHY_1565 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_2	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1596 EMIF_CTLCFG_DENALI_PHY_1566 Register

1 EMIF_CTLCFG_DENALI_PHY_1566 Register (Offset = 5878h) [reset = 0h]

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Table 14-24732. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D878h

Figure 14-8209. EMIF_CTLCFG_DENALI_PHY_1566 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_ADR_BIT_MASK_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LP4_BOOT_SLV_DELAY_2							
R/W							
0h							

Table 14-24734. EMIF_CTLCFG_DENALI_PHY_1566 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_2	R/W	0h	Segment mask bit for address slice 2. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_2	R/W	0h	Mask bit for address slice 2. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_2	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1597 EMIF_CTLCFG_DENALI_PHY_1567 Register

1 EMIF_CTLCFG_DENALI_PHY_1567 Register (Offset = 587Ch) [reset = 0h]

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Table 14-24735. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D87Ch**

Figure 14-8210. EMIF_CTLCFG_DENALI_PHY_1567 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_2					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_2					
NONE		R/W					
0h		0h					

Table 14-24737. EMIF_CTLCFG_DENALI_PHY_1567 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_2	R/W	0h	Controls address pad output enable for address slice 2. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_2	R/W	0h	Toggle control during static activity for address slice 2. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_2	R/W	0h	Mask bit for CS training participation for address slice 2. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_2	R/W	0h	Mask bit for CA training participation for address slice 2. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1598 EMIF_CTLCFG_DENALI_PHY_1568 Register

1 EMIF_CTLCFG_DENALI_PHY_1568 Register (Offset = 5880h) [reset = 20202003h]

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Table 14-24738. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D880h**

Figure 14-8211. EMIF_CTLCFG_DENALI_PHY_1568 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DC_ADR2_CLK_ADJUST_2							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DC_ADR1_CLK_ADJUST_2							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADR0_CLK_ADJUST_2							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_ADR_DC_INIT_DISABLE_2	
NONE						R/W	
0h						3h	

Table 14-24740. EMIF_CTLCFG_DENALI_PHY_1568 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_DC_ADR2_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 2 for address slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR1_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 1 for address slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR0_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 0 for address slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_DC_INIT_DISABLE_2	R/W	3h	Duty Cycle Corrector disable at initialization for address slice 2. Set to 1 to disable, bit [1] controls data path, bit [0] controls clock path. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1599 EMIF_CTLCFG_DENALI_PHY_1569 Register

1 EMIF_CTLCFG_DENALI_PHY_1569 Register (Offset = 5884h) [reset = 202020h]

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Table 14-24741. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D884h**

Figure 14-8212. EMIF_CTLCFG_DENALI_PHY_1569 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DC_ADR5_CLK_ADJUST_2							
R/W							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADR4_CLK_ADJUST_2							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_ADR3_CLK_ADJUST_2							
R/W							
20h							

Table 14-24743. EMIF_CTLCFG_DENALI_PHY_1569 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_2	R/W	0h	DCC and RX_CAL clk gate disable for address slice 2. 1 = disable clk gate. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_DC_ADR5_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 5 for address slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADR4_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 4 for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADR3_CLK_ADJUST_2	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 3 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1600 EMIF_CTLCFG_DENALI_PHY_1570 Register

1 EMIF_CTLCFG_DENALI_PHY_1570 Register (Offset = 5888h) [reset = 0h]

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Table 14-24744. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D888h

Figure 14-8213. EMIF_CTLCFG_DENALI_PHY_1570 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_DC_ADJUST_START_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_DC_WEIGHT_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_CAL_TIMEOUT_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_CAL_SAMPLE_WAIT_2							
R/W							
0h							

Table 14-24746. EMIF_CTLCFG_DENALI_PHY_1570 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_DC_ADJUST_START_2	R/W	0h	DCC calibration starting value for address slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_ADR_DC_WEIGHT_2	R/W	0h	DCC weighting factor base value for address slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_CAL_TIMEOUT_2	R/W	0h	DCC number of iterations to wait before timeout for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_CAL_SAMPLE_WAIT_2	R/W	0h	DCC cycles to wait after calibration change before sampling results for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1601 EMIF_CTLCFG_DENALI_PHY_1571 Register

1 EMIF_CTLCFG_DENALI_PHY_1571 Register (Offset = 588Ch) [reset = 0h]

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Table 14-24747. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D88Ch**

Figure 14-8214. EMIF_CTLCFG_DENALI_PHY_1571 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DC_CAL_POLARITY_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_DC_ADJUST_DIRECT_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DC_ADJUST_THRSHLD_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DC_ADJUST_SAMPLE_CNT_2							
R/W							
0h							

Table 14-24749. EMIF_CTLCFG_DENALI_PHY_1571 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_DC_CAL_POLARITY_2	R/W	0h	DCC calibration polarity for address slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_DC_ADJUST_DIRECT_2	R/W	0h	DCC adjust direction for address slice 2. Reset Source: ctl_amod_g_rst_n
15:8	PHY_ADR_DC_ADJUST_THRSHLD_2	R/W	0h	DCC adjust threshold around the mid-point for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_DC_ADJUST_SAMPLE_CNT_2	R/W	0h	DCC number of samples to take for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1602 EMIF_CTLCFG_DENALI_PHY_1572 Register

1 EMIF_CTLCFG_DENALI_PHY_1572 Register (Offset = 5890h) [reset = 0h]

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Table 14-24750. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D890h**

Figure 14-8215. EMIF_CTLCFG_DENALI_PHY_1572 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_SW_TXPWR_CTRL_2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CAL_START_2
NONE							R/W
0h							0h

Table 14-24752. EMIF_CTLCFG_DENALI_PHY_1572 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_SW_TXPWR_CTRL_2	R/W	0h	Disable address output enables in deep sleep mode for address slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CAL_START_2	R/W	0h	DCC Manual trigger for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1603 EMIF_CTLCFG_DENALI_PHY_1573 Register

1 EMIF_CTLCFG_DENALI_PHY_1573 Register (Offset = 5894h) [reset = 0h]

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Table 14-24753. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D894h**

Figure 14-8216. EMIF_CTLCFG_DENALI_PHY_1573 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_IO_CFG_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ADR_IO_CFG_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_DC_CAL_CLK_SEL_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_2							
R/W							
0h							

Table 14-24755. EMIF_CTLCFG_DENALI_PHY_1573 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_PAD_ADR_IO_CFG_2	R/W	0h	Controls I/O pads for address pad for address slice 2. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_DC_CAL_CLK_SEL_2	R/W	0h	DCC CAL clock for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_2	R/W	0h	Tsel select values for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1604 EMIF_CTLCFG_DENALI_PHY_1574 Register

1 EMIF_CTLCFG_DENALI_PHY_1574 Register (Offset = 5898h) [reset = 0h]

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Table 14-24756. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D898h**

Figure 14-8217. EMIF_CTLCFG_DENALI_PHY_1574 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR0_CLK_WR_SLAVE_DELAY_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR0_CLK_WR_SLAVE_DELAY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR0_SW_WRADDR_SHIFT_2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_PAD_ADR_RX_PCLK_CLK_SEL_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-24758. EMIF_CTLCFG_DENALI_PHY_1574 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR0_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 0 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_ADR0_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_PAD_ADR_RX_PCLK_CLK_SEL_2	R/W	0h	Reserved for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1605 EMIF_CTLCFG_DENALI_PHY_1575 Register

1 EMIF_CTLCFG_DENALI_PHY_1575 Register (Offset = 589Ch) [reset = 0h]

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Table 14-24759. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D89Ch

Figure 14-8218. EMIF_CTLCFG_DENALI_PHY_1575 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR2_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR1_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR1_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				

Table 14-24761. EMIF_CTLCFG_DENALI_PHY_1575 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR2_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR1_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 1 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR1_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1606 EMIF_CTLCFG_DENALI_PHY_1576 Register

1 EMIF_CTLCFG_DENALI_PHY_1576 Register (Offset = 58A0h) [reset = 0h]

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Table 14-24762. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D8A0h

Figure 14-8219. EMIF_CTLCFG_DENALI_PHY_1576 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED			PHY_ADR3_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				

15	14	13	12	11	10	9	8
RESERVED					PHY_ADR2_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		

7	6	5	4	3	2	1	0
PHY_ADR2_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-24764. EMIF_CTLCFG_DENALI_PHY_1576 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 2 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1607 EMIF_CTLCFG_DENALI_PHY_1577 Register

1 EMIF_CTLCFG_DENALI_PHY_1577 Register (Offset = 58A4h) [reset = 0h]

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Table 14-24765. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D8A4h**

Figure 14-8220. EMIF_CTLCFG_DENALI_PHY_1577 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR4_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR3_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-24767. EMIF_CTLCFG_DENALI_PHY_1577 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 3 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1608 EMIF_CTLCFG_DENALI_PHY_1578 Register

1 EMIF_CTLCFG_DENALI_PHY_1578 Register (Offset = 58A8h) [reset = 0h]

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Table 14-24768. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D8A8h

Figure 14-8221. EMIF_CTLCFG_DENALI_PHY_1578 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR5_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR4_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR4_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-24770. EMIF_CTLCFG_DENALI_PHY_1578 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 4 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1609 EMIF_CTLCFG_DENALI_PHY_1579 Register

1 EMIF_CTLCFG_DENALI_PHY_1579 Register (Offset = 58ACh) [reset = 0h]

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Table 14-24771. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D8ACh

Figure 14-8222. EMIF_CTLCFG_DENALI_PHY_1579 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_SW_MASTER_MODE_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR5_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-24773. EMIF_CTLCFG_DENALI_PHY_1579 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_2	R/W	0h	Controller delay line override settings for address slice 2. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 5 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1610 EMIF_CTLCFG_DENALI_PHY_1580 Register

1 EMIF_CTLCFG_DENALI_PHY_1580 Register (Offset = 58B0h) [reset = 0h]

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Table 14-24774. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D8B0h**

Figure 14-8223. EMIF_CTLCFG_DENALI_PHY_1580 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DELAY_WAIT_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_ADR_MASTER_DELAY_STEP_2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_MASTER_DELAY_START_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DELAY_START_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24776. EMIF_CTLCFG_DENALI_PHY_1580 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_2	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 2. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_2	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_2	R/W	0h	Start value for controller delay line locking algorithm for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1611 EMIF_CTLCFG_DENALI_PHY_1581 Register

1 EMIF_CTLCFG_DENALI_PHY_1581 Register (Offset = 58B4h) [reset = 0h]

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Table 14-24777. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D8B4h**

Figure 14-8224. EMIF_CTLCFG_DENALI_PHY_1581 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_SW_CALVL_DVW_MIN_EN_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_SW_CALVL_DVW_MIN_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_SW_CALVL_DVW_MIN_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DELAY_HALF_MEASURE_2							
R/W							
0h							

Table 14-24779. EMIF_CTLCFG_DENALI_PHY_1581 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_2	R/W	0h	Enables the software override data valid window size during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_2	R/W	0h	Sets the software override data valid window size during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_2	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 2 Reset Source: ctl_amod_g_rst_n

14.6.6.2.1612 EMIF_CTLCFG_DENALI_PHY_1582 Register

1 EMIF_CTLCFG_DENALI_PHY_1582 Register (Offset = 58B8h) [reset = 0h]

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Table 14-24780. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D8B8h

Figure 14-8225. EMIF_CTLCFG_DENALI_PHY_1582 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_ADR_CALVL_DLY_STEP_2			
NONE				R/W			
0h				0h			

Table 14-24782. EMIF_CTLCFG_DENALI_PHY_1582 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_2	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1613 EMIF_CTLCFG_DENALI_PHY_1583 Register

1 EMIF_CTLCFG_DENALI_PHY_1583 Register (Offset = 58BCh) [reset = 0h]

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Table 14-24783. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 D8BCh**

Figure 14-8226. EMIF_CTLCFG_DENALI_PHY_1583 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_DC_INIT_SLV_DELAY_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_ADR_DC_INIT_SLV_DELAY_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_ADR_MEAS_DLY_STEP_ENABLE_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_2			
NONE				R/W			
0h				0h			

Table 14-24785. EMIF_CTLCFG_DENALI_PHY_1583 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_ADR_DC_INIT_SLV_DELAY_2	R/W	0h	DCC initialization value of write ADDR target delay for address slice 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_2	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1614 EMIF_CTLCFG_DENALI_PHY_1584 Register

1 EMIF_CTLCFG_DENALI_PHY_1584 Register (Offset = 58C0h) [reset = 0h]

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Table 14-24786. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 D8C0h

Figure 14-8227. EMIF_CTLCFG_DENALI_PHY_1584 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_DM_CLK_THRSHLD_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CALVL_ENABLE_2
NONE							R/W
0h							0h

Table 14-24788. EMIF_CTLCFG_DENALI_PHY_1584 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PHY_ADR_DC_DM_CLK_THRSHLD_2	R/W	0h	DCC clock measurement cell threshold offset for address slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_DC_CALVL_ENABLE_2	R/W	0h	DCC enable duty cycle adjust during CA leveling for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1615 EMIF_CTLCFG_DENALI_PHY_1792 Register

1 EMIF_CTLCFG_DENALI_PHY_1792 Register (Offset = 5C00h) [reset = 0h]

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Table 14-24789. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC00h**

Figure 14-8228. EMIF_CTLCFG_DENALI_PHY_1792 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_FREQ_SEL	
NONE						R/W	
0h						0h	

Table 14-24791. EMIF_CTLCFG_DENALI_PHY_1792 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_FREQ_SEL	R/W	0h	Specifies which copy of the frequency-dependent timing parameters will be used by the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1616 EMIF_CTLCFG_DENALI_PHY_1793 Register

1 EMIF_CTLCFG_DENALI_PHY_1793 Register (Offset = 5C04h) [reset = 100h]

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Table 14-24792. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC04h**

Figure 14-8229. EMIF_CTLCFG_DENALI_PHY_1793 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_FREQ_SEL_INDEX	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_FREQ_SEL_MULTICAST_EN
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_FREQ_SEL_FROM_REGIF
NONE							R/W
0h							0h

Table 14-24794. EMIF_CTLCFG_DENALI_PHY_1793 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_FREQ_SEL_INDEX	R/W	0h	Selects which frequency set to update when PHY_FREQ_SEL_MULTICAST_EN is not set. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_FREQ_SEL_MULTICAST_EN	R/W	1h	When set, a register write will update parameters for all frequency sets simultaneously. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_FREQ_SEL_FROM_REGIF	R/W	0h	Indicates which source is used to select the frequency copy. When set to 1, the frequency select source is given by parameter PHY_FREQ_SEL from register I/F. When cleared to 0, the frequency select source is the PHY input signal dfi_frequency Reset Source: ctl_amod_g_rst_n

14.6.6.2.1617 EMIF_CTLCFG_DENALI_PHY_1794 Register

1 EMIF_CTLCFG_DENALI_PHY_1794 Register (Offset = 5C08h) [reset = 0h]

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Table 14-24795. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC08h**

Figure 14-8230. EMIF_CTLCFG_DENALI_PHY_1794 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_SW_GRP3_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_SW_GRP2_SHIFT_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_SW_GRP1_SHIFT_0				
NONE			R/W				
0h			0h				

Table 14-24797. EMIF_CTLCFG_DENALI_PHY_1794 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1618 EMIF_CTLCFG_DENALI_PHY_1795 Register

1 EMIF_CTLCFG_DENALI_PHY_1795 Register (Offset = 5C0Ch) [reset = 0h]

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Table 14-24798. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC0Ch**

Figure 14-8231. EMIF_CTLCFG_DENALI_PHY_1795 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP3_SHIFT_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_SW_GRP2_SHIFT_1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_SW_GRP1_SHIFT_1				
NONE			R/W				
0h			0h				

Table 14-24800. EMIF_CTLCFG_DENALI_PHY_1795 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1619 EMIF_CTLCFG_DENALI_PHY_1796 Register

1 EMIF_CTLCFG_DENALI_PHY_1796 Register (Offset = 5C10h) [reset = 0h]

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Table 14-24801. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC10h

Figure 14-8232. EMIF_CTLCFG_DENALI_PHY_1796 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP3_SHIFT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_SW_GRP2_SHIFT_2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_SW_GRP1_SHIFT_2				
NONE			R/W				
0h			0h				

Table 14-24803. EMIF_CTLCFG_DENALI_PHY_1796 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1620 EMIF_CTLCFG_DENALI_PHY_1797 Register

1 EMIF_CTLCFG_DENALI_PHY_1797 Register (Offset = 5C14h) [reset = 0h]

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Table 14-24804. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC14h

Figure 14-8233. EMIF_CTLCFG_DENALI_PHY_1797 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP3_SHIFT_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_SW_GRP2_SHIFT_3				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_SW_GRP1_SHIFT_3				
NONE			R/W				
0h			0h				

Table 14-24806. EMIF_CTLCFG_DENALI_PHY_1797 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1621 EMIF_CTLCFG_DENALI_PHY_1798 Register

1 EMIF_CTLCFG_DENALI_PHY_1798 Register (Offset = 5C18h) [reset = 0h]

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Table 14-24807. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC18h**

Figure 14-8234. EMIF_CTLCFG_DENALI_PHY_1798 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GRP_BYPASS_OVERRIDE
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
RESERVED			PHY_SW_GRP_BYPASS_SHIFT				
NONE			R/W				
0h			0h				

15	14	13	12	11	10	9	8
RESERVED					PHY_GRP_BYPASS_SLAVE_DELAY		
NONE					R/W		
0h					0h		

7	6	5	4	3	2	1	0
PHY_GRP_BYPASS_SLAVE_DELAY							
R/W							
0h							

Table 14-24809. EMIF_CTLCFG_DENALI_PHY_1798 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_GRP_BYPASS_OVERRIDE	R/W	0h	Address/control group slice bypass mode override setting. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP_BYPASS_SHIFT	R/W	0h	Address/control group slice bypass mode shift settings. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP_BYPASS_SLAVE_DELAY	R/W	0h	Address/control group slice bypass mode target delay setting. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1622 EMIF_CTLCFG_DENALI_PHY_1799 Register

1 EMIF_CTLCFG_DENALI_PHY_1799 Register (Offset = 5C1Ch) [reset = 100h]

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Table 14-24810. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC1Ch**

Figure 14-8235. EMIF_CTLCFG_DENALI_PHY_1799 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CSLVL_START		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CSLVL_START							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_MANUAL_UPDATE_PHYUPD_ENABLE
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SC_PHY_MANUAL_UPDATE
NONE							W
0h							0h

Table 14-24812. EMIF_CTLCFG_DENALI_PHY_1799 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CSLVL_START	R/W	0h	Defines the CS training DDL start value. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_MANUAL_UPDATE_PHYUPD_ENABLE	R/W	1h	Manual update selection of all target delay line settings. Set 1 to assert phyupd_req and wait phyupd_ack to update delay line, set 0 to update delay line directly. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_MANUAL_UPDATE	W	0h	Manual update of all target delay line settings. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1623 EMIF_CTLCFG_DENALI_PHY_1800 Register

1 EMIF_CTLCFG_DENALI_PHY_1800 Register (Offset = 5C20h) [reset = 0h]

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Table 14-24813. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC20h

Figure 14-8236. EMIF_CTLCFG_DENALI_PHY_1800 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>SC_PHY_CSLVL_DEBUG_CONT</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CSLVL_DEBUG_MODE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_CSLVL_COARSE_DLY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CSLVL_COARSE_DLY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24815. EMIF_CTLCFG_DENALI_PHY_1800 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_CSLVL_DEBUG_CONT	W	0h	Allows the CS training state machine to advance [when in debug mode]. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CSLVL_DEBUG_MODE	R/W	0h	Enables CS training debug mode. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CSLVL_COARSE_DLY	R/W	0h	Defines the CS training DDL coarse cycle delay value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1624 EMIF_CTLCFG_DENALI_PHY_1801 Register

1 EMIF_CTLCFG_DENALI_PHY_1801 Register (Offset = 5C24h) [reset = 0h]

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Table 14-24816. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC24h

Figure 14-8237. EMIF_CTLCFG_DENALI_PHY_1801 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_CSLVL_ERROR_CLR
NONE							W
0h							0h

Table 14-24818. EMIF_CTLCFG_DENALI_PHY_1801 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_CSLVL_ERROR_CLR	W	0h	Clears the CS training state machine error status. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1625 EMIF_CTLCFG_DENALI_PHY_1802 Register

1 EMIF_CTLCFG_DENALI_PHY_1802 Register (Offset = 5C28h) [reset = 6800000h]

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Table 14-24819. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC28h**

Figure 14-8238. EMIF_CTLCFG_DENALI_PHY_1802 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS0							
R							
6800000h							
23	22	21	20	19	18	17	16
PHY_CSLVL_OBS0							
R							
6800000h							
15	14	13	12	11	10	9	8
PHY_CSLVL_OBS0							
R							
6800000h							
7	6	5	4	3	2	1	0
PHY_CSLVL_OBS0							
R							
6800000h							

Table 14-24821. EMIF_CTLCFG_DENALI_PHY_1802 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS0	R	6800000h	Observation register for CS training delay values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1626 EMIF_CTLCFG_DENALI_PHY_1803 Register

1 EMIF_CTLCFG_DENALI_PHY_1803 Register (Offset = 5C2Ch) [reset = 0h]

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Table 14-24822. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC2Ch**

Figure 14-8239. EMIF_CTLCFG_DENALI_PHY_1803 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CSLVL_OBS1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CSLVL_OBS1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CSLVL_OBS1							
R							
0h							

Table 14-24824. EMIF_CTLCFG_DENALI_PHY_1803 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS1	R	0h	Observation register for CS training algorithm status. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1627 EMIF_CTLCFG_DENALI_PHY_1804 Register

1 EMIF_CTLCFG_DENALI_PHY_1804 Register (Offset = 5C30h) [reset = 0h]

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Table 14-24825. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC30h**

Figure 14-8240. EMIF_CTLCFG_DENALI_PHY_1804 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_CSLVL_OBS2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CSLVL_OBS2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CSLVL_OBS2							
R							
0h							

Table 14-24827. EMIF_CTLCFG_DENALI_PHY_1804 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS2	R	0h	Observation register for periodic CS training delay values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1628 EMIF_CTLCFG_DENALI_PHY_1805 Register

1 EMIF_CTLCFG_DENALI_PHY_1805 Register (Offset = 5C34h) [reset = 0h]

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Table 14-24828. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC34h**

Figure 14-8241. EMIF_CTLCFG_DENALI_PHY_1805 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LP4_BOOT_DISABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_CSLVL_PERIODIC_START_OFFSET
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CSLVL_PERIODIC_START_OFFSET							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_CSLVL_ENABLE
NONE							R/W
0h							0h

Table 14-24830. EMIF_CTLCFG_DENALI_PHY_1805 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LP4_BOOT_DISABLE	R/W	0h	Controls the handling of the DFI frequency. When set to 1, DFI frequency 0 is considered the first operational frequency. When cleared to 0, DFI frequency 0 is the boot frequency and other DFI frequency values are operational frequencies. Must be cleared to 0 for LPDDR3 devices operating in an LPDDR4 capable configuration. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_CSLVL_PERIODIC_START_OFFSET	R/W	0h	Defines the relative offset from previous LE and TE to start periodic CSLVL with. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CSLVL_ENABLE	R/W	0h	CS training enable. Set to 1 to enable CS training during CA training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1629 EMIF_CTLCFG_DENALI_PHY_1806 Register

1 EMIF_CTLCFG_DENALI_PHY_1806 Register (Offset = 5C38h) [reset = 0h]

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Table 14-24831. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC38h**

Figure 14-8242. EMIF_CTLCFG_DENALI_PHY_1806 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_CSLVL_QTR		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
PHY_CSLVL_QTR							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_CSLVL_CS_MAP			
NONE				R/W			
0h				0h			

Table 14-24833. EMIF_CTLCFG_DENALI_PHY_1806 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:8	PHY_CSLVL_QTR	R/W	0h	Defines the CS training DDL 1/4 cycle delay value. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_CSLVL_CS_MAP	R/W	0h	CS training map. Set each CS bit to 1 to allow that CS to participate in CS training results. NOT CURRENTLY USED. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1630 EMIF_CTLCFG_DENALI_PHY_1807 Register

1 EMIF_CTLCFG_DENALI_PHY_1807 Register (Offset = 5C3Ch) [reset = 0h]

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Table 14-24834. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC3Ch**

Figure 14-8243. EMIF_CTLCFG_DENALI_PHY_1807 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_CALVL_CS_MAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_CSLVL_COARSE_CAPTURE_CNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_CSLVL_COARSE_CHK</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CSLVL_COARSE_CHK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24836. EMIF_CTLCFG_DENALI_PHY_1807 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_CALVL_CS_MAP	R/W	0h	Defines the slice numbers associated with each CS during CA training. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CSLVL_COARSE_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP target delay setting during CS training coarse CA training. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CSLVL_COARSE_CHK	R/W	0h	Defines the CS training coarse CA training DDL 1/16th cycle delay value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1631 EMIF_CTLCFG_DENALI_PHY_1808 Register

1 EMIF_CTLCFG_DENALI_PHY_1808 Register (Offset = 5C40h) [reset = 0h]

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Table 14-24837. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC40h**

Figure 14-8244. EMIF_CTLCFG_DENALI_PHY_1808 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADRCTL_LPDDR
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_DFI_PHYUPD_TYPE	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_ADRCTL_SNAP_OBS_REGS
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE		
NONE					R/W		
0h					0h		

Table 14-24839. EMIF_CTLCFG_DENALI_PHY_1808 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADRCTL_LPDDR	R/W	0h	Adds a cycle of delay for the address/control slices to match the address slice. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_DFI_PHYUPD_TYPE	R/W	0h	Defines the value of the dfi_phyupd_type output signal to MC. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ADRCTL_SNAP_OBS_REGS	W	0h	Initiates a snapshot of the internal observation registers for the address/control block. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE	R/W	0h	Reserved for the address/control controller. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1632 EMIF_CTLCFG_DENALI_PHY_1809 Register

1 EMIF_CTLCFG_DENALI_PHY_1809 Register (Offset = 5C44h) [reset = 100h]

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Table 14-24840. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC44h**

Figure 14-8245. EMIF_CTLCFG_DENALI_PHY_1809 Name Register

31	30	29	28	27	26	25	24
PHY_CLK_DC_CAL_TIMEOUT							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_CLK_DC_CAL_SAMPLE_WAIT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LPDDR3_CS
NONE							R/W
0h							1h
7	6	5	4	3	2	1	0
RESERVED							PHY_LP4_ACTIVE
NONE							R/W
0h							0h

Table 14-24842. EMIF_CTLCFG_DENALI_PHY_1809 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_CLK_DC_CAL_TIMEOUT	R/W	0h	Duty cycle correction maximum iteration count. Reset Source: ctl_amod_g_rst_n
23:16	PHY_CLK_DC_CAL_SAMPLE_WAIT	R/W	0h	Number of cal clock cycles to wait for a sample to be taken. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LPDDR3_CS	R/W	1h	Alters reset state polarity for LPDDR chip selects. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LP4_ACTIVE	R/W	0h	Indicates an LPDDR4 device is connected to the PHY. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1633 EMIF_CTLCFG_DENALI_PHY_1810 Register

1 EMIF_CTLCFG_DENALI_PHY_1810 Register (Offset = 5C48h) [reset = 0h]

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Table 14-24843. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC48h

Figure 14-8246. EMIF_CTLCFG_DENALI_PHY_1810 Name Register

31	30	29	28	27	26	25	24
PHY_CLK_DC_ADJUST_SAMPLE_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_CLK_DC_ADJUST_START					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							PHY_CLK_DC_FREQ_CHG_ADJ
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_DC_WEIGHT	
NONE						R/W	
0h						0h	

Table 14-24845. EMIF_CTLCFG_DENALI_PHY_1810 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_CLK_DC_ADJUST_SAMPLE_CNT	R/W	0h	Duty cycle correction algorithm sample count per adjustment setting. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_CLK_DC_ADJUST_START	R/W	0h	Duty cycle correction algorithm adjustment starting value. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_CLK_DC_FREQ_CHG_ADJ	R/W	0h	Duty cycle correction during frequency change control. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CLK_DC_WEIGHT	R/W	0h	Duty cycle correction weighting factor base value. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1634 EMIF_CTLCFG_DENALI_PHY_1811 Register

1 EMIF_CTLCFG_DENALI_PHY_1811 Register (Offset = 5C4Ch) [reset = 0h]

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Table 14-24846. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC4Ch

Figure 14-8247. EMIF_CTLCFG_DENALI_PHY_1811 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_DC_CAL_START
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CLK_DC_CAL_POLARITY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_CLK_DC_ADJUST_DIRECT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_CLK_DC_ADJUST_THRSHLD							
R/W							
0h							

Table 14-24848. EMIF_CTLCFG_DENALI_PHY_1811 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_DC_CAL_START	R/W	0h	Duty cycle correction calibration manual start. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CLK_DC_CAL_POLARITY	R/W	0h	Duty cycle correction algorithm measurement polarity. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_CLK_DC_ADJUST_DIRECT	R/W	0h	Duty cycle correction algorithm adjustment direction. Reset Source: ctl_amod_g_rst_n
7:0	PHY_CLK_DC_ADJUST_THRSHLD	R/W	0h	Duty cycle correction algorithm threshold delta comparison. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1635 EMIF_CTLCFG_DENALI_PHY_1812 Register

1 EMIF_CTLCFG_DENALI_PHY_1812 Register (Offset = 5C50h) [reset = 0h]

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Table 14-24849. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC50h**

Figure 14-8248. EMIF_CTLCFG_DENALI_PHY_1812 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_TXIO_CTRL_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_SW_TXIO_CTRL_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_CONTINUOUS_CLK_CAL_UPDATE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SC_PHY_UPDATE_CLK_CAL_VALUES
NONE							W
0h							0h

Table 14-24851. EMIF_CTLCFG_DENALI_PHY_1812 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_TXIO_CTRL_1	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SW_TXIO_CTRL_0	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_CONTINUOUS_CLK_CAL_UPDATE	R/W	0h	Continuous update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to keep this enabled. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_UPDATE_CLK_CAL_VALUES	W	0h	Manual update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1636 EMIF_CTLCFG_DENALI_PHY_1813 Register

1 EMIF_CTLCFG_DENALI_PHY_1813 Register (Offset = 5C54h) [reset = 0h]

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Table 14-24852. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC54h**

Figure 14-8249. EMIF_CTLCFG_DENALI_PHY_1813 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_MEMCLK_SW_TXIO_CTRL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_TXIO_CTRL_3			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_TXIO_CTRL_2			
NONE				R/W			
0h				0h			

Table 14-24854. EMIF_CTLCFG_DENALI_PHY_1813 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADRCTL_SW_TXPWR_CTRL_0	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_MEMCLK_SW_TXIO_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_TXIO_CTRL_3	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_SW_TXIO_CTRL_2	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1637 EMIF_CTLCFG_DENALI_PHY_1814 Register

1 EMIF_CTLCFG_DENALI_PHY_1814 Register (Offset = 5C58h) [reset = 0h]

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Table 14-24855. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC58h**

Figure 14-8250. EMIF_CTLCFG_DENALI_PHY_1814 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_MEMCLK_SW_TXPWR_CTRL
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_1			
NONE				R/W			
0h				0h			

Table 14-24857. EMIF_CTLCFG_DENALI_PHY_1814 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_MEMCLK_SW_TXPWR_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADRCTL_SW_TXPWR_CTRL_3	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADRCTL_SW_TXPWR_CTRL_2	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADRCTL_SW_TXPWR_CTRL_1	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1638 EMIF_CTLCFG_DENALI_PHY_1815 Register

1 EMIF_CTLCFG_DENALI_PHY_1815 Register (Offset = 5C5Ch) [reset = 0h]

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Table 14-24858. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC5Ch**

Figure 14-8251. EMIF_CTLCFG_DENALI_PHY_1815 Name Register

31	30	29	28	27	26	25	24
PHY_STATIC_TOG_CONTROL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_STATIC_TOG_CONTROL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_BYTE_DISABLE_STATIC_TOG_DISABLE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_TOP_STATIC_TOG_DISABLE
NONE							R/W
0h							0h

Table 14-24860. EMIF_CTLCFG_DENALI_PHY_1815 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_STATIC_TOG_CONTROL	R/W	0h	Clock divider to create toggle signal. Use long counter as the base. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_BYTE_DISABLE_STATIC_TOG_DISABLE	R/W	0h	Control to disable the toggle signal for data slice during static activity when dfi_data_byte_disable is asserted. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOP_STATIC_TOG_DISABLE	R/W	0h	Disables the generation of the toggle for static clock based paths in the PHY to prevent assymetric aging. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1639 EMIF_CTLCFG_DENALI_PHY_1816 Register

1 EMIF_CTLCFG_DENALI_PHY_1816 Register (Offset = 5C60h) [reset = 0h]

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Table 14-24861. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC60h**

Figure 14-8252. EMIF_CTLCFG_DENALI_PHY_1816 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_LP4_BOOT_PLL_BYPASS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_MEMCLK_STATIC_TOG_DISABLE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADRCTL_STATIC_TOG_DISABLE			
NONE				R/W			
0h				0h			

Table 14-24863. EMIF_CTLCFG_DENALI_PHY_1816 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_LP4_BOOT_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_MEMCLK_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit0: clock disable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADRCTL_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit0: Write path delay line disable; bit1: clock disable; bit2: adrctl controller delay line disable [if exists]; bit3: adrctl misc core clk disable.[if exists] Reset Source: ctl_amod_g_rst_n

14.6.6.2.1640 EMIF_CTLCFG_DENALI_PHY_1817 Register

1 EMIF_CTLCFG_DENALI_PHY_1817 Register (Offset = 5C64h) [reset = 10082650h]

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Table 14-24864. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC64h

Figure 14-8253. EMIF_CTLCFG_DENALI_PHY_1817 Name Register

31	30	29	28	27	26	25	24
PHY_CLK_SWITCH_OBS							
R							
10082650h							
23	22	21	20	19	18	17	16
PHY_CLK_SWITCH_OBS							
R							
10082650h							
15	14	13	12	11	10	9	8
PHY_CLK_SWITCH_OBS							
R							
10082650h							
7	6	5	4	3	2	1	0
PHY_CLK_SWITCH_OBS							
R							
10082650h							

Table 14-24866. EMIF_CTLCFG_DENALI_PHY_1817 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CLK_SWITCH_OBS	R	10082650h	Observation register for Clock switch state machine READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1641 EMIF_CTLCFG_DENALI_PHY_1818 Register

1 EMIF_CTLCFG_DENALI_PHY_1818 Register (Offset = 5C68h) [reset = 0h]

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Table 14-24867. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 DC68h**

Figure 14-8254. EMIF_CTLCFG_DENALI_PHY_1818 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PLL_WAIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PLL_WAIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24869. EMIF_CTLCFG_DENALI_PHY_1818 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_WAIT	R/W	0h	PHY clock PLL wait time after locking. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1642 EMIF_CTLCFG_DENALI_PHY_1819 Register

1 EMIF_CTLCFG_DENALI_PHY_1819 Register (Offset = 5C6Ch) [reset = 0h]

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Table 14-24870. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC6Ch**

Figure 14-8255. EMIF_CTLCFG_DENALI_PHY_1819 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_SW_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-24872. EMIF_CTLCFG_DENALI_PHY_1819 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_SW_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1643 EMIF_CTLCFG_DENALI_PHY_1820 Register

1 EMIF_CTLCFG_DENALI_PHY_1820 Register (Offset = 5C70h) [reset = 0h]

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Table 14-24873. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC70h

Figure 14-8256. EMIF_CTLCFG_DENALI_PHY_1820 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SET_DFI_INPUT_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_SET_DFI_INPUT_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_SET_DFI_INPUT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SET_DFI_INPUT_0			
NONE				R/W			
0h				0h			

Table 14-24875. EMIF_CTLCFG_DENALI_PHY_1820 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SET_DFI_INPUT_3	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SET_DFI_INPUT_2	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SET_DFI_INPUT_1	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_SET_DFI_INPUT_0	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1644 EMIF_CTLCFG_DENALI_PHY_1821 Register

1 EMIF_CTLCFG_DENALI_PHY_1821 Register (Offset = 5C74h) [reset = 0h]

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Table 14-24876. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC74h**

Figure 14-8257. EMIF_CTLCFG_DENALI_PHY_1821 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_0			
NONE				R/W			
0h				0h			

Table 14-24878. EMIF_CTLCFG_DENALI_PHY_1821 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CS_ACS_ALLOCATION_BIT3_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CS_ACS_ALLOCATION_BIT2_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_CS_ACS_ALLOCATION_BIT1_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-24878. EMIF_CTLCFG_DENALI_PHY_1821 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PHY_CS_ACS_ALLOCATION_BIT0_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1645 EMIF_CTLCFG_DENALI_PHY_1822 Register

1 EMIF_CTLCFG_DENALI_PHY_1822 Register (Offset = 5C78h) [reset = 0h]

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Table 14-24879. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC78h**

Figure 14-8258. EMIF_CTLCFG_DENALI_PHY_1822 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_1			
NONE				R/W			
0h				0h			

Table 14-24881. EMIF_CTLCFG_DENALI_PHY_1822 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CS_ACS_ALLOCATION_BIT3_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CS_ACS_ALLOCATION_BIT2_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_CS_ACS_ALLOCATION_BIT1_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-24881. EMIF_CTLCFG_DENALI_PHY_1822 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PHY_CS_ACS_ALLOCATION_BIT0_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1646 EMIF_CTLCFG_DENALI_PHY_1823 Register

1 EMIF_CTLCFG_DENALI_PHY_1823 Register (Offset = 5C7Ch) [reset = 0h]

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Table 14-24882. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DC7Ch

Figure 14-8259. EMIF_CTLCFG_DENALI_PHY_1823 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_2			
NONE				R/W			
0h				0h			

Table 14-24884. EMIF_CTLCFG_DENALI_PHY_1823 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CS_ACS_ALLOCATION_BIT3_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CS_ACS_ALLOCATION_BIT2_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_CS_ACS_ALLOCATION_BIT1_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-24884. EMIF_CTLCFG_DENALI_PHY_1823 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PHY_CS_ACS_ALLOCATION_BIT0_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1647 EMIF_CTLCFG_DENALI_PHY_1824 Register

1 EMIF_CTLCFG_DENALI_PHY_1824 Register (Offset = 5C80h) [reset = 0h]

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Table 14-24885. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC80h**

Figure 14-8260. EMIF_CTLCFG_DENALI_PHY_1824 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_3			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_3			
NONE				R/W			
0h				0h			

Table 14-24887. EMIF_CTLCFG_DENALI_PHY_1824 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CS_ACS_ALLOCATION_BIT3_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CS_ACS_ALLOCATION_BIT2_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_CS_ACS_ALLOCATION_BIT1_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-24887. EMIF_CTLCFG_DENALI_PHY_1824 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PHY_CS_ACS_ALLOCATION_BIT0_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1648 EMIF_CTLCFG_DENALI_PHY_1825 Register

1 EMIF_CTLCFG_DENALI_PHY_1825 Register (Offset = 5C84h) [reset = 120h]

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Table 14-24888. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC84h**

Figure 14-8261. EMIF_CTLCFG_DENALI_PHY_1825 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_CLK_DC_DM_THRSHLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CLK_DC_INIT_DISABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CLK_DC_ADJUST_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-24890. EMIF_CTLCFG_DENALI_PHY_1825 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_CLK_DC_DM_THRSHLD	R/W	0h	Data measurement cell threshold offset. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_CLK_DC_INIT_DISABLE	R/W	1h	Disable duty cycle adjust at initialization. Reset Source: ctl_amod_g_rst_n
7:0	PHY_CLK_DC_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for clock slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1649 EMIF_CTLCFG_DENALI_PHY_1826 Register

1 EMIF_CTLCFG_DENALI_PHY_1826 Register (Offset = 5C88h) [reset = 0h]

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Table 14-24891. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC88h**

Figure 14-8262. EMIF_CTLCFG_DENALI_PHY_1826 Name Register

31	30	29	28	27	26	25	24
PHY_PLL_CTRL_OVERRIDE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PLL_CTRL_OVERRIDE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_LP4_BOOT_PLL_CTRL				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_LP4_BOOT_PLL_CTRL							
R/W							
0h							

Table 14-24893. EMIF_CTLCFG_DENALI_PHY_1826 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_PLL_CTRL_OVERRIDE	R/W	0h	Individual PHY clock PLL control overrides. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_LP4_BOOT_PLL_CTRL	R/W	0h	PHY deskew PLL controls for LPDDR4 boot frequency. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1650 EMIF_CTLCFG_DENALI_PHY_1827 Register

1 EMIF_CTLCFG_DENALI_PHY_1827 Register (Offset = 5C8Ch) [reset = 0h]

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Table 14-24894. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC8Ch**

Figure 14-8263. EMIF_CTLCFG_DENALI_PHY_1827 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">SC_PHY_PLL_SPO_CAL_SNAP_OBS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PLL_SPO_CAL_CTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_USE_PLL_DSKEWCALLOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-24896. EMIF_CTLCFG_DENALI_PHY_1827 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	SC_PHY_PLL_SPO_CAL_SNAP_OBS	W	0h	Register command to take a snapshot of PLL output. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_PLL_SPO_CAL_CTRL	R/W	0h	PLL SPO Cal controls. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_USE_PLL_DSKEWCALLOCK	R/W	0h	Use DSKEWCALLOCK or not. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1651 EMIF_CTLCFG_DENALI_PHY_1828 Register

1 EMIF_CTLCFG_DENALI_PHY_1828 Register (Offset = 5C90h) [reset = 0h]

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Table 14-24897. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC90h**

Figure 14-8264. EMIF_CTLCFG_DENALI_PHY_1828 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PLL_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PLL_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24899. EMIF_CTLCFG_DENALI_PHY_1828 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_OBS_0	R	0h	PHY TOP level clock PLL_0 observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1652 EMIF_CTLCFG_DENALI_PHY_1829 Register

1 EMIF_CTLCFG_DENALI_PHY_1829 Register (Offset = 5C94h) [reset = 0h]

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Table 14-24900. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC94h**

Figure 14-8265. EMIF_CTLCFG_DENALI_PHY_1829 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PLL_SPO_CAL_OBS_0
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PLL_SPO_CAL_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_SPO_CAL_OBS_0							
R							
0h							

Table 14-24902. EMIF_CTLCFG_DENALI_PHY_1829 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PLL_SPO_CAL_OBS_0	R	0h	PHY TOP level PLL_0 SPO Cal observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1653 EMIF_CTLCFG_DENALI_PHY_1830 Register

1 EMIF_CTLCFG_DENALI_PHY_1830 Register (Offset = 5C98h) [reset = 0h]

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Table 14-24903. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC98h**

Figure 14-8266. EMIF_CTLCFG_DENALI_PHY_1830 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_PLL_DESKEWCALIN_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PHY_LP4_BOOT_PLL_DESKEWCALIN_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_PLL_DESKEWCALIN_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_PLL_DESKEWCALIN_0							
R/W							
0h							

Table 14-24905. EMIF_CTLCFG_DENALI_PHY_1830 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_LP4_BOOT_PLL_DESKEWCALIN_0	R/W	0h	PHY TOP level PLL_0 lpddr4 boot deskewcal in values. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PLL_DESKEWCALIN_0	R/W	0h	PHY TOP level PLL_0 deskewcal in values. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1654 EMIF_CTLCFG_DENALI_PHY_1831 Register

1 EMIF_CTLCFG_DENALI_PHY_1831 Register (Offset = 5C9Ch) [reset = 0h]

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Table 14-24906. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DC9Ch**

Figure 14-8267. EMIF_CTLCFG_DENALI_PHY_1831 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_PLL_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_PLL_OBS_1							
R							
0h							

Table 14-24908. EMIF_CTLCFG_DENALI_PHY_1831 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_OBS_1	R	0h	PHY TOP level clock PLL_1 observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1655 EMIF_CTLCFG_DENALI_PHY_1832 Register

1 EMIF_CTLCFG_DENALI_PHY_1832 Register (Offset = 5CA0h) [reset = 0h]

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Table 14-24909. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCA0h

Figure 14-8268. EMIF_CTLCFG_DENALI_PHY_1832 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PLL_SPO_CAL_OBS_1
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PLL_SPO_CAL_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_SPO_CAL_OBS_1							
R							
0h							

Table 14-24911. EMIF_CTLCFG_DENALI_PHY_1832 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PLL_SPO_CAL_OBS_1	R	0h	PHY TOP level PLL_1 SPO Cal observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1656 EMIF_CTLCFG_DENALI_PHY_1833 Register

1 EMIF_CTLCFG_DENALI_PHY_1833 Register (Offset = 5CA4h) [reset = 0h]

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Table 14-24912. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCA4h**

Figure 14-8269. EMIF_CTLCFG_DENALI_PHY_1833 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_PLL_DESKEWCALIN_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_LP4_BOOT_PLL_DESKEWCALIN_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_PLL_DESKEWCALIN_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_DESKEWCALIN_1							
R/W							
0h							

Table 14-24914. EMIF_CTLCFG_DENALI_PHY_1833 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_LP4_BOOT_PLL_DESKEWCALIN_1	R/W	0h	PHY TOP level PLL_1 lpddr4 boot deskewcal in values. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PLL_DESKEWCALIN_1	R/W	0h	PHY TOP level PLL_1 deskewcal in values. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1657 EMIF_CTLCFG_DENALI_PHY_1834 Register

1 EMIF_CTLCFG_DENALI_PHY_1834 Register (Offset = 5CA8h) [reset = 0h]

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Table 14-24915. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCA8h**

Figure 14-8270. EMIF_CTLCFG_DENALI_PHY_1834 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_TCKSRE_WAIT			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_LP4_BOOT_LOW_FREQ_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_PLL_REFOUT_SEL
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_TESTOUT_SEL
NONE							R/W
0h							0h

Table 14-24917. EMIF_CTLCFG_DENALI_PHY_1834 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_TCKSRE_WAIT	R/W	0h	Specifies the number of cycles the PHY should wait before turning off the PLL for a deep sleep or DFS event. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_LP4_BOOT_LOW_FREQ_SEL	R/W	0h	Control the PLL domain enter/exit from the negative clock edge for LPDDR4 boot frequency. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_PLL_REFOUT_SEL	R/W	0h	PHY PLL refout select. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_TESTOUT_SEL	R/W	0h	PHY PLL testout select. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1658 EMIF_CTLCFG_DENALI_PHY_1835 Register

1 EMIF_CTLCFG_DENALI_PHY_1835 Register (Offset = 5CACh) [reset = 0h]

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Table 14-24918. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCACh

Figure 14-8271. EMIF_CTLCFG_DENALI_PHY_1835 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_LP_CTRLUPD_CNTR_CFG	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_LP_CTRLUPD_CNTR_CFG							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LS_IDLE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_LP_WAKEUP							
R/W							
0h							

Table 14-24920. EMIF_CTLCFG_DENALI_PHY_1835 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_LP_CTRLUPD_CNTR_CFG	R/W	0h	Specifies the number of cycles the PHY takes from light sleep req deassert to ack deassert in low power mode. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LS_IDLE_EN	R/W	0h	Indicates the Reduced Idle Power State is enabled in low power mode. Reset Source: ctl_amod_g_rst_n
7:0	PHY_LP_WAKEUP	R/W	0h	Specifies the number of cycles the PHY takes to wakeup in low power mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1659 EMIF_CTLCFG_DENALI_PHY_1836 Register

1 EMIF_CTLCFG_DENALI_PHY_1836 Register (Offset = 5CB0h) [reset = 0h]

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Table 14-24921. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCB0h**

Figure 14-8272. EMIF_CTLCFG_DENALI_PHY_1836 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_TDFI_PHY_WRDELAY
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_DS_EXIT_CTRL
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DS_EXIT_CTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DS_EXIT_CTRL							
R/W							
0h							

Table 14-24923. EMIF_CTLCFG_DENALI_PHY_1836 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_TDFI_PHY_WRDELAY	R/W	0h	DFI timing parameter TDFI_PHY_WRDELAY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PHY_DS_EXIT_CTRL	R/W	0h	Controls to reduce the deep sleep exit latency, when bit 16 is 1 deep sleep exit ack won't wait controller delay line lock. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1660 EMIF_CTLCFG_DENALI_PHY_1837 Register

1 EMIF_CTLCFG_DENALI_PHY_1837 Register (Offset = 5CB4h) [reset = 4410h]

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Table 14-24924. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCB4h

Figure 14-8273. EMIF_CTLCFG_DENALI_PHY_1837 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PAD_FDBK_TERM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_FDBK_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_FDBK_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-24926. EMIF_CTLCFG_DENALI_PHY_1837 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_FDBK_TERM	R/W	4410h	Controls term settings for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1661 EMIF_CTLCFG_DENALI_PHY_1838 Register

1 EMIF_CTLCFG_DENALI_PHY_1838 Register (Offset = 5CB8h) [reset = 4410h]

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Table 14-24927. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCB8h**

Figure 14-8274. EMIF_CTLCFG_DENALI_PHY_1838 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_PAD_DATA_TERM
NONE							R/W
0h							4410h
15	14	13	12	11	10	9	8
PHY_PAD_DATA_TERM							
R/W							
4410h							
7	6	5	4	3	2	1	0
PHY_PAD_DATA_TERM							
R/W							
4410h							

Table 14-24929. EMIF_CTLCFG_DENALI_PHY_1838 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PAD_DATA_TERM	R/W	4410h	Controls term settings for data pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1662 EMIF_CTLCFG_DENALI_PHY_1839 Register

1 EMIF_CTLCFG_DENALI_PHY_1839 Register (Offset = 5CBCh) [reset = 4410h]

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Table 14-24930. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCBCh**

Figure 14-8275. EMIF_CTLCFG_DENALI_PHY_1839 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PAD_DQS_TERM
NONE							R/W
0h							4410h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_DQS_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_DQS_TERM							
R/W							
4410h							

Table 14-24932. EMIF_CTLCFG_DENALI_PHY_1839 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PAD_DQS_TERM	R/W	4410h	Controls term settings for dqs pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1663 EMIF_CTLCFG_DENALI_PHY_1840 Register

1 EMIF_CTLCFG_DENALI_PHY_1840 Register (Offset = 5CC0h) [reset = 4410h]

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Table 14-24933. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCC0h**

Figure 14-8276. EMIF_CTLCFG_DENALI_PHY_1840 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_ADDR_TERM	
NONE						R/W	
0h						4410h	
15	14	13	12	11	10	9	8
PHY_PAD_ADDR_TERM							
R/W							
4410h							
7	6	5	4	3	2	1	0
PHY_PAD_ADDR_TERM							
R/W							
4410h							

Table 14-24935. EMIF_CTLCFG_DENALI_PHY_1840 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ADDR_TERM	R/W	4410h	Controls term settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1664 EMIF_CTLCFG_DENALI_PHY_1841 Register

1 EMIF_CTLCFG_DENALI_PHY_1841 Register (Offset = 5CC4h) [reset = 4410h]

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Table 14-24936. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCC4h

Figure 14-8277. EMIF_CTLCFG_DENALI_PHY_1841 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_CLK_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CLK_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CLK_TERM							
R/W							
4410h							

Table 14-24938. EMIF_CTLCFG_DENALI_PHY_1841 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CLK_TERM	R/W	4410h	Controls term settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1665 EMIF_CTLCFG_DENALI_PHY_1842 Register

1 EMIF_CTLCFG_DENALI_PHY_1842 Register (Offset = 5CC8h) [reset = 4410h]

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Table 14-24939. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCC8h**

Figure 14-8278. EMIF_CTLCFG_DENALI_PHY_1842 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_ERR_TERM	
NONE						R/W	
0h						4410h	
15	14	13	12	11	10	9	8
PHY_PAD_ERR_TERM							
R/W							
4410h							
7	6	5	4	3	2	1	0
PHY_PAD_ERR_TERM							
R/W							
4410h							

Table 14-24941. EMIF_CTLCFG_DENALI_PHY_1842 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ERR_TERM	R/W	4410h	Controls term settings for error pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1666 EMIF_CTLCFG_DENALI_PHY_1843 Register

1 EMIF_CTLCFG_DENALI_PHY_1843 Register (Offset = 5CCCh) [reset = 4410h]

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Table 14-24942. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCCCh**

Figure 14-8279. EMIF_CTLCFG_DENALI_PHY_1843 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PAD_CKE_TERM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_CKE_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_CKE_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-24944. EMIF_CTLCFG_DENALI_PHY_1843 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CKE_TERM	R/W	4410h	Controls term settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1667 EMIF_CTLCFG_DENALI_PHY_1844 Register

1 EMIF_CTLCFG_DENALI_PHY_1844 Register (Offset = 5CD0h) [reset = 4410h]

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Table 14-24945. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCD0h**

Figure 14-8280. EMIF_CTLCFG_DENALI_PHY_1844 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-24947. EMIF_CTLCFG_DENALI_PHY_1844 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_RST_TERM	R/W	4410h	Controls term settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1668 EMIF_CTLCFG_DENALI_PHY_1845 Register

1 EMIF_CTLCFG_DENALI_PHY_1845 Register (Offset = 5CD4h) [reset = 4410h]

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Table 14-24948. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCD4h**

Figure 14-8281. EMIF_CTLCFG_DENALI_PHY_1845 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_CS_TERM	
NONE						R/W	
0h						4410h	
15	14	13	12	11	10	9	8
PHY_PAD_CS_TERM							
R/W							
4410h							
7	6	5	4	3	2	1	0
PHY_PAD_CS_TERM							
R/W							
4410h							

Table 14-24950. EMIF_CTLCFG_DENALI_PHY_1845 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CS_TERM	R/W	4410h	Controls term settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1669 EMIF_CTLCFG_DENALI_PHY_1846 Register

1 EMIF_CTLCFG_DENALI_PHY_1846 Register (Offset = 5CD8h) [reset = 4410h]

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Table 14-24951. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCD8h

Figure 14-8282. EMIF_CTLCFG_DENALI_PHY_1846 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_ODT_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ODT_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ODT_TERM							
R/W							
4410h							

Table 14-24953. EMIF_CTLCFG_DENALI_PHY_1846 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ODT_TERM	R/W	4410h	Controls term settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1670 EMIF_CTLCFG_DENALI_PHY_1847 Register

1 EMIF_CTLCFG_DENALI_PHY_1847 Register (Offset = 5CDCh) [reset = 0h]

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Table 14-24954. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCDCh**

Figure 14-8283. EMIF_CTLCFG_DENALI_PHY_1847 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADRCTL_LP3_RX_CAL				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADRCTL_LP3_RX_CAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADRCTL_RX_CAL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADRCTL_RX_CAL							
R/W							
0h							

Table 14-24956. EMIF_CTLCFG_DENALI_PHY_1847 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:16	PHY_ADRCTL_LP3_RX_CAL	R/W	0h	PHY CKE/RESET_N RX calibration controls. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADRCTL_RX_CAL	R/W	0h	PHY address/control RX calibration controls. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1671 EMIF_CTLCFG_DENALI_PHY_1848 Register

1 EMIF_CTLCFG_DENALI_PHY_1848 Register (Offset = 5CE0h) [reset = 0h]

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Table 14-24957. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCE0h**

Figure 14-8284. EMIF_CTLCFG_DENALI_PHY_1848 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CAL_START_0</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CAL_CLEAR_0</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_CAL_MODE_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CAL_MODE_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24959. EMIF_CTLCFG_DENALI_PHY_1848 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CAL_START_0	W	0h	Manual start for the pad calibration state machine for block 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CAL_CLEAR_0	W	0h	Clear the pad calibration state machine and results for block 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_CAL_MODE_0	R/W	0h	Pad calibration mode bits for block 0. Bit [0] disables pad calibration upon initialization. Bit [1] enables automatic interval based calibration. Bits [3:2] set the base interval for the interval counter. Bits [7:4] are direct connections to pad control signals. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1672 EMIF_CTLCFG_DENALI_PHY_1849 Register

1 EMIF_CTLCFG_DENALI_PHY_1849 Register (Offset = 5CE4h) [reset = 0h]

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Table 14-24960. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCE4h

Figure 14-8285. EMIF_CTLCFG_DENALI_PHY_1849 Name Register

31	30	29	28	27	26	25	24
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							

Table 14-24962. EMIF_CTLCFG_DENALI_PHY_1849 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CAL_INTERVAL_COUNT_0	R/W	0h	Pad calibration interval counter compare value for block 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1673 EMIF_CTLCFG_DENALI_PHY_1850 Register

1 EMIF_CTLCFG_DENALI_PHY_1850 Register (Offset = 5CE8h) [reset = 0h]

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Table 14-24963. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCE8h

Figure 14-8286. EMIF_CTLCFG_DENALI_PHY_1850 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_LP4_BOOT_CAL_CLK_SELECT_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CAL_SAMPLE_WAIT_0							
R/W							
0h							

Table 14-24965. EMIF_CTLCFG_DENALI_PHY_1850 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	PHY_LP4_BOOT_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for LPDDR4 boot frequency for block 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_CAL_SAMPLE_WAIT_0	R/W	0h	Pad calibration state machine wait count in pad clock cycles for block 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1674 EMIF_CTLCFG_DENALI_PHY_1851 Register

1 EMIF_CTLCFG_DENALI_PHY_1851 Register (Offset = 5CECh) [reset = 0h]

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Table 14-24966. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCECh

Figure 14-8287. EMIF_CTLCFG_DENALI_PHY_1851 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT_OBS_0							
R							
0h							

Table 14-24968. EMIF_CTLCFG_DENALI_PHY_1851 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT_OBS_0	R	0h	Pad calibration results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1675 EMIF_CTLCFG_DENALI_PHY_1852 Register

1 EMIF_CTLCFG_DENALI_PHY_1852 Register (Offset = 5CF0h) [reset = 0h]

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Table 14-24969. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DCF0h

Figure 14-8288. EMIF_CTLCFG_DENALI_PHY_1852 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_RESULT2_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_RESULT2_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_RESULT2_OBS_0							
R							
0h							

Table 14-24971. EMIF_CTLCFG_DENALI_PHY_1852 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT2_OBS_0	R	0h	Pad calibration results [CKE/RESET_N] observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1676 EMIF_CTLCFG_DENALI_PHY_1853 Register

1 EMIF_CTLCFG_DENALI_PHY_1853 Register (Offset = 5CF4h) [reset = 0h]

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Table 14-24972. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCF4h**

Figure 14-8289. EMIF_CTLCFG_DENALI_PHY_1853 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT4_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT4_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT4_OBS_0							
R							
0h							

Table 14-24974. EMIF_CTLCFG_DENALI_PHY_1853 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT4_OBS_0	R	0h	Pad calibration pass1 shadow results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1677 EMIF_CTLCFG_DENALI_PHY_1854 Register

1 EMIF_CTLCFG_DENALI_PHY_1854 Register (Offset = 5CF8h) [reset = 0h]

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Table 14-24975. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCF8h**

Figure 14-8290. EMIF_CTLCFG_DENALI_PHY_1854 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT5_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT5_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT5_OBS_0							
R							
0h							

Table 14-24977. EMIF_CTLCFG_DENALI_PHY_1854 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT5_OBS_0	R	0h	Pad calibration pass2 shadow results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1678 EMIF_CTLCFG_DENALI_PHY_1855 Register

1 EMIF_CTLCFG_DENALI_PHY_1855 Register (Offset = 5CFCh) [reset = 0h]

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Table 14-24978. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DCFCh**

Figure 14-8291. EMIF_CTLCFG_DENALI_PHY_1855 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_RESULT6_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_RESULT6_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_RESULT6_OBS_0							
R							
0h							

Table 14-24980. EMIF_CTLCFG_DENALI_PHY_1855 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT6_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1679 EMIF_CTLCFG_DENALI_PHY_1856 Register

1 EMIF_CTLCFG_DENALI_PHY_1856 Register (Offset = 5D00h) [reset = 0h]

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Table 14-24981. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD00h**

Figure 14-8292. EMIF_CTLCFG_DENALI_PHY_1856 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_CAL_CPTR_CNT_0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_CAL_RESULT7_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT7_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT7_OBS_0							
R							
0h							

Table 14-24983. EMIF_CTLCFG_DENALI_PHY_1856 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_CAL_CPTR_CNT_0	R/W	0h	defines sample capture number in pad calibration process Reset Source: ctl_amod_g_rst_n
23:0	PHY_CAL_RESULT7_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1680 EMIF_CTLCFG_DENALI_PHY_1857 Register

1 EMIF_CTLCFG_DENALI_PHY_1857 Register (Offset = 5D04h) [reset = 0h]

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Table 14-24984. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD04h**

Figure 14-8293. EMIF_CTLCFG_DENALI_PHY_1857 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_DBG_CFG_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_CAL_RCV_FINE_ADJ_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_PD_FINE_ADJ_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_PU_FINE_ADJ_0							
R/W							
0h							

Table 14-24986. EMIF_CTLCFG_DENALI_PHY_1857 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CAL_DBG_CFG_0	R/W	0h	defines debug configuration in pad calibration process Reset Source: ctl_amod_g_rst_n
23:16	PHY_CAL_RCV_FINE_ADJ_0	R/W	0h	defines adjustment for RCV code in pad calibration process Reset Source: ctl_amod_g_rst_n
15:8	PHY_CAL_PD_FINE_ADJ_0	R/W	0h	defines adjustment for PD code in pad calibration process Reset Source: ctl_amod_g_rst_n
7:0	PHY_CAL_PU_FINE_ADJ_0	R/W	0h	defines adjustment for PU code in pad calibration process Reset Source: ctl_amod_g_rst_n

14.6.6.2.1681 EMIF_CTLCFG_DENALI_PHY_1858 Register

1 EMIF_CTLCFG_DENALI_PHY_1858 Register (Offset = 5D08h) [reset = 0h]

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Table 14-24987. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DD08h

Figure 14-8294. EMIF_CTLCFG_DENALI_PHY_1858 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_PAD_DBG_CONT_0
NONE							W
0h							0h

Table 14-24989. EMIF_CTLCFG_DENALI_PHY_1858 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_PAD_DBG_CONT_0	W	0h	Allows the pad calibration state machine to advance [when in debug mode] for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1682 EMIF_CTLCFG_DENALI_PHY_1859 Register

1 EMIF_CTLCFG_DENALI_PHY_1859 Register (Offset = 5D0Ch) [reset = 0h]

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Table 14-24990. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD0Ch**

Figure 14-8295. EMIF_CTLCFG_DENALI_PHY_1859 Name Register

31	30	29	28	27	26	25	24
PHY_CAL_RESULT3_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT3_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT3_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT3_OBS_0							
R							
0h							

Table 14-24992. EMIF_CTLCFG_DENALI_PHY_1859 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CAL_RESULT3_OBS_0	R	0h	Pad calibration results first/last0/1 observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1683 EMIF_CTLCFG_DENALI_PHY_1860 Register

1 EMIF_CTLCFG_DENALI_PHY_1860 Register (Offset = 5D10h) [reset = 4102000h]

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Table 14-24993. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD10h**

Figure 14-8296. EMIF_CTLCFG_DENALI_PHY_1860 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CAL_SLOPE_ADJ_0			
NONE				R/W			
0h				41020h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_SLOPE_ADJ_0							
R/W							
41020h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_SLOPE_ADJ_0							
R/W							
41020h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADRCTL_PVT_MAP_0							
R/W							
0h							

Table 14-24995. EMIF_CTLCFG_DENALI_PHY_1860 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:8	PHY_CAL_SLOPE_ADJ_0	R/W	41020h	defines slope configure in pad calibration process Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADRCTL_PVT_MAP_0	R/W	0h	defines slope configure in pad calibration process Reset Source: ctl_amod_g_rst_n

14.6.6.2.1684 EMIF_CTLCFG_DENALI_PHY_1861 Register

1 EMIF_CTLCFG_DENALI_PHY_1861 Register (Offset = 5D14h) [reset = 41020h]

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Table 14-24996. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD14h**

Figure 14-8297. EMIF_CTLCFG_DENALI_PHY_1861 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_CAL_SLOPE_ADJ_PASS2_0			
NONE				R/W			
0h				41020h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_SLOPE_ADJ_PASS2_0							
R/W							
41020h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_SLOPE_ADJ_PASS2_0							
R/W							
41020h							

Table 14-24998. EMIF_CTLCFG_DENALI_PHY_1861 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_CAL_SLOPE_ADJ_PASS2_0	R/W	41020h	defines slope configure for pass2 in pad calibration process Reset Source: ctl_amod_g_rst_n

14.6.6.2.1685 EMIF_CTLCFG_DENALI_PHY_1862 Register

1 EMIF_CTLCFG_DENALI_PHY_1862 Register (Offset = 5D18h) [reset = C98C98h]

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Table 14-24999. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD18h**

Figure 14-8298. EMIF_CTLCFG_DENALI_PHY_1862 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CAL_TWO_PASS_CFG_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>C98C98h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_CAL_TWO_PASS_CFG_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C98C98h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_CAL_TWO_PASS_CFG_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C98C98h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CAL_TWO_PASS_CFG_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C98C98h</td></tr>
</table>

Table 14-25001. EMIF_CTLCFG_DENALI_PHY_1862 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:0	PHY_CAL_TWO_PASS_CFG_0	R/W	C98C98h	defines cal_en configure in pad calibration process Reset Source: ctl_amod_g_rst_n

14.6.6.2.1686 EMIF_CTLCFG_DENALI_PHY_1863 Register

1 EMIF_CTLCFG_DENALI_PHY_1863 Register (Offset = 5D1Ch) [reset = 3F000000h]

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Table 14-25002. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD1Ch**

Figure 14-8299. EMIF_CTLCFG_DENALI_PHY_1863 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">3Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_CAL_SW_CAL_CFG_0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_CAL_SW_CAL_CFG_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_CAL_SW_CAL_CFG_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25004. EMIF_CTLCFG_DENALI_PHY_1863 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pu results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:0	PHY_CAL_SW_CAL_CFG_0	R/W	0h	defines firmware based pad calibration process Reset Source: ctl_amod_g_rst_n

14.6.6.2.1687 EMIF_CTLCFG_DENALI_PHY_1864 Register

1 EMIF_CTLCFG_DENALI_PHY_1864 Register (Offset = 5D20h) [reset = 3F3F1F3Fh]

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Table 14-25005. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DD20h

Figure 14-8300. EMIF_CTLCFG_DENALI_PHY_1864 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					

Table 14-25007. EMIF_CTLCFG_DENALI_PHY_1864 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pd results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pu results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass1 rx results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pd results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n

14.6.6.2.1688 EMIF_CTLCFG_DENALI_PHY_1865 Register

1 EMIF_CTLCFG_DENALI_PHY_1865 Register (Offset = 5D24h) [reset = 1Fh]

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Table 14-25008. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD24h**

Figure 14-8301. EMIF_CTLCFG_DENALI_PHY_1865 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0				
NONE			R/W				
0h			0h				

23	22	21	20	19	18	17	16
RESERVED		PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0					
NONE		R/W					
0h		0h					

15	14	13	12	11	10	9	8
RESERVED		PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0					
NONE		R/W					
0h		0h					

7	6	5	4	3	2	1	0
RESERVED			PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0				
NONE			R/W				
0h			1Fh				

Table 14-25010. EMIF_CTLCFG_DENALI_PHY_1865 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass1 rx results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pd results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pu results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass2 rx results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n

14.6.6.2.1689 EMIF_CTLCFG_DENALI_PHY_1866 Register

1 EMIF_CTLCFG_DENALI_PHY_1866 Register (Offset = 5D28h) [reset = 0h]

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Table 14-25011. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DD28h

Figure 14-8302. EMIF_CTLCFG_DENALI_PHY_1866 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED		PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0					
NONE		R/W					
0h		0h					

Table 14-25013. EMIF_CTLCFG_DENALI_PHY_1866 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass2 rx results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pd results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pu results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n

14.6.6.2.1690 EMIF_CTLCFG_DENALI_PHY_1867 Register

1 EMIF_CTLCFG_DENALI_PHY_1867 Register (Offset = 5D2Ch) [reset = 0h]

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Table 14-25014. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD2Ch**

Figure 14-8303. EMIF_CTLCFG_DENALI_PHY_1867 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_AC_LPBK_ERR_CLEAR
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_ADRCTL_MANUAL_UPDATE
NONE							W
0h							0h
15	14	13	12	11	10	9	8
PHY_PAD_ATB_CTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_ATB_CTRL							
R/W							
0h							

Table 14-25016. EMIF_CTLCFG_DENALI_PHY_1867 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_AC_LPBK_ERR_CLEAR	W	0h	Address/control loopback error clear. Set to 1 to clear error. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADRCTL_MANUAL_UPDATE	W	0h	Address/control manual update of target delay lines. Set to 1 to update. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_PAD_ATB_CTRL	R/W	0h	Pad ATB control settings. Bit [0] is the enable signal. Bits [5:1] are the ATB data signals. Bits [15:8] are the 1 hot select for which pad is selected. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1691 EMIF_CTLCFG_DENALI_PHY_1868 Register

1 EMIF_CTLCFG_DENALI_PHY_1868 Register (Offset = 5D30h) [reset = 0h]

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Table 14-25017. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD30h**

Figure 14-8304. EMIF_CTLCFG_DENALI_PHY_1868 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_AC_LPBK_CONTROL
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AC_LPBK_CONTROL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_AC_LPBK_ENABLE			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_AC_LPBK_OBS_SELECT	
NONE						R/W	
0h						0h	

Table 14-25019. EMIF_CTLCFG_DENALI_PHY_1868 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_AC_LPBK_CONTROL	R/W	0h	Address/control slice loopback control setting. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_AC_LPBK_ENABLE	R/W	0h	Loopback enable for the address/control slices. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_AC_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback address/control slice observation register to the global observation register. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1692 EMIF_CTLCFG_DENALI_PHY_1869 Register

1 EMIF_CTLCFG_DENALI_PHY_1869 Register (Offset = 5D34h) [reset = 1h]

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Table 14-25020. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD34h**

Figure 14-8305. EMIF_CTLCFG_DENALI_PHY_1869 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_AC_PRBS_PATTERN_MASK			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_AC_PRBS_PATTERN_START						
NONE	R/W						
0h	1h						

Table 14-25022. EMIF_CTLCFG_DENALI_PHY_1869 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_AC_PRBS_PATTERN_MASK	R/W	0h	PRBS7 mask signal for address/control slice. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_AC_PRBS_PATTERN_START	R/W	1h	PRBS7 start pattern for address/control slice. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1693 EMIF_CTLCFG_DENALI_PHY_1870 Register

1 EMIF_CTLCFG_DENALI_PHY_1870 Register (Offset = 5D38h) [reset = 0h]

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Table 14-25023. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD38h**

Figure 14-8306. EMIF_CTLCFG_DENALI_PHY_1870 Name Register

31	30	29	28	27	26	25	24
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
23	22	21	20	19	18	17	16
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
15	14	13	12	11	10	9	8
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
7	6	5	4	3	2	1	0
PHY_AC_LPBK_RESULT_OBS							
R							
0h							

Table 14-25025. EMIF_CTLCFG_DENALI_PHY_1870 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AC_LPBK_RESULT_OBS	R	0h	Observation register for the loopback address/control slices. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1694 EMIF_CTLCFG_DENALI_PHY_1871 Register

1 EMIF_CTLCFG_DENALI_PHY_1871 Register (Offset = 5D3Ch) [reset = 0h]

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Table 14-25026. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD3Ch**

Figure 14-8307. EMIF_CTLCFG_DENALI_PHY_1871 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_AC_CLK_LPBK_CONTROL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_AC_CLK_LPBK_ENABLE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_AC_CLK_LPBK_OBS_SELECT
NONE							R/W
0h							0h

Table 14-25028. EMIF_CTLCFG_DENALI_PHY_1871 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PHY_AC_CLK_LPBK_CONTROL	R/W	0h	Mem clk block loopback control setting. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_AC_CLK_LPBK_ENABLE	R/W	0h	Loopback enable for mem clk blocks. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_AC_CLK_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback mem clk block observation register to the global observation register. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1695 EMIF_CTLCFG_DENALI_PHY_1872 Register

1 EMIF_CTLCFG_DENALI_PHY_1872 Register (Offset = 5D40h) [reset = 0h]

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Table 14-25029. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD40h**

Figure 14-8308. EMIF_CTLCFG_DENALI_PHY_1872 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_TOP_PWR_RDC_DISABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_AC_PWR_RDC_DISABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_AC_CLK_LPBK_RESULT_OBS							
R							
0h							
7	6	5	4	3	2	1	0
PHY_AC_CLK_LPBK_RESULT_OBS							
R							
0h							

Table 14-25031. EMIF_CTLCFG_DENALI_PHY_1872 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_TOP_PWR_RDC_DISABLE	R/W	0h	top param power reduction disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_AC_PWR_RDC_DISABLE	R/W	0h	ac slice power reduction disable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_AC_CLK_LPBK_RESULT_OBS	R	0h	Observation register for loopback mem clk blocks. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.6.6.2.1696 EMIF_CTLCFG_DENALI_PHY_1873 Register

1 EMIF_CTLCFG_DENALI_PHY_1873 Register (Offset = 5D44h) [reset = 0h]

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Table 14-25032. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD44h**

Figure 14-8309. EMIF_CTLCFG_DENALI_PHY_1873 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_AC_SLV_DLY_CTRL_GATE_DISABLE
NONE							R/W
0h							0h

Table 14-25034. EMIF_CTLCFG_DENALI_PHY_1873 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_AC_SLV_DLY_CTRL_GATE_DISABLE	R/W	0h	ac slice slv_dly_control block power reduction disable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1697 EMIF_CTLCFG_DENALI_PHY_1874 Register

1 EMIF_CTLCFG_DENALI_PHY_1874 Register (Offset = 5D48h) [reset = 0h]

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Table 14-25035. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD48h**

Figure 14-8310. EMIF_CTLCFG_DENALI_PHY_1874 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							

Table 14-25037. EMIF_CTLCFG_DENALI_PHY_1874 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DATA_BYTE_ORDER_SEL	R/W	0h	Used to define the data slice's byte swap for CA bits 7:0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1698 EMIF_CTLCFG_DENALI_PHY_1875 Register

1 EMIF_CTLCFG_DENALI_PHY_1875 Register (Offset = 5D4Ch) [reset = 0h]

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Table 14-25038. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD4Ch**

Figure 14-8311. EMIF_CTLCFG_DENALI_PHY_1875 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_DISABLE</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_CALVL_DEVICE_MAP</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_LPDDR4_CONNECT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DATA_BYTE_ORDER_SEL_HIGH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25040. EMIF_CTLCFG_DENALI_PHY_1875 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_DISABLE	R/W	0h	Disable the unused adr slice to save power. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_CALVL_DEVICE_MAP	R/W	0h	Define which device's DQ feedback data bits should be used during CA training Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LPDDR4_CONNECT	R/W	0h	PHY is connected to LPDDR4 devices Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_BYTE_ORDER_SEL_HIGH	R/W	0h	Used to define the data slice's byte swap for CA bits 9:8. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1699 EMIF_CTLCFG_DENALI_PHY_1876 Register

1 EMIF_CTLCFG_DENALI_PHY_1876 Register (Offset = 5D50h) [reset = 0h]

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Table 14-25041. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD50h**

Figure 14-8312. EMIF_CTLCFG_DENALI_PHY_1876 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	
NONE						R/W	
0h						0h	

Table 14-25043. EMIF_CTLCFG_DENALI_PHY_1876 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADRCTL_MSTR_DLY_ENC_SEL_3	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 3 . Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_ADRCTL_MSTR_DLY_ENC_SEL_2	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 2 . Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 1 . Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 0 . Reset Source: ctl_amod_g_rst_n

14.6.6.2.1700 EMIF_CTLCFG_DENALI_PHY_1877 Register

1 EMIF_CTLCFG_DENALI_PHY_1877 Register (Offset = 5D54h) [reset = 0h]

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Table 14-25044. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD54h**

Figure 14-8313. EMIF_CTLCFG_DENALI_PHY_1877 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_AC_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_AC_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_AC_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_AC_ENABLE							
R/W							
0h							

Table 14-25046. EMIF_CTLCFG_DENALI_PHY_1877 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_AC_ENABLE	R/W	0h	PHY Address/Control DDL BIST mode enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1701 EMIF_CTLCFG_DENALI_PHY_1878 Register

1 EMIF_CTLCFG_DENALI_PHY_1878 Register (Offset = 5D58h) [reset = 0h]

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Table 14-25047. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD58h**

Figure 14-8314. EMIF_CTLCFG_DENALI_PHY_1878 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DDL_AC_MODE	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_AC_MODE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_AC_MODE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_AC_MODE							
R/W							
0h							

Table 14-25049. EMIF_CTLCFG_DENALI_PHY_1878 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PHY_DDL_AC_MODE	R/W	0h	PHY Address/Control DDL BIST mode. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1702 EMIF_CTLCFG_DENALI_PHY_1879 Register

1 EMIF_CTLCFG_DENALI_PHY_1879 Register (Offset = 5D5Ch) [reset = 0h]

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Table 14-25050. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD5Ch**

Figure 14-8315. EMIF_CTLCFG_DENALI_PHY_1879 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_TRACK_UPD_THRESHOLD_AC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_INIT_UPDATE_CONFIG		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_DDL_AC_MASK					
NONE		R/W					
0h		0h					

Table 14-25052. EMIF_CTLCFG_DENALI_PHY_1879 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_DDL_TRACK_UPD_THRESHOLD_AC	R/W	0h	Specify threshold value for PHY init update tracking for AC slice. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_INIT_UPDATE_CONFIG	R/W	0h	PHY init update function configuration. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_AC_MASK	R/W	0h	PHY Address/Control DDL BIST mask. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1703 EMIF_CTLCFG_DENALI_PHY_1880 Register

1 EMIF_CTLCFG_DENALI_PHY_1880 Register (Offset = 5D60h) [reset = 0h]

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Table 14-25053. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DD60h

Figure 14-8316. EMIF_CTLCFG_DENALI_PHY_1880 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ERR_STATUS		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_ERR_MASK_EN		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
PHY_CA_PARITY_ERR_PULSE_MIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_CA_PARITY_ERR_PULSE_MIN							
R/W							
0h							

Table 14-25055. EMIF_CTLCFG_DENALI_PHY_1880 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ERR_STATUS	R/W	0h	PHY ERROR information. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ERR_MASK_EN	R/W	0h	PHY ERROR information report mask enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_CA_PARITY_ERR_PULSE_MIN	R/W	0h	PHY alert_n pulse width minimux value for CA parity error. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1704 EMIF_CTLCFG_DENALI_PHY_1881 Register

1 EMIF_CTLCFG_DENALI_PHY_1881 Register (Offset = 5D64h) [reset = 0h]

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Table 14-25056. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD64h**

Figure 14-8317. EMIF_CTLCFG_DENALI_PHY_1881 Name Register

31	30	29	28	27	26	25	24
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							

Table 14-25058. EMIF_CTLCFG_DENALI_PHY_1881 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS0_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 0 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1705 EMIF_CTLCFG_DENALI_PHY_1882 Register

1 EMIF_CTLCFG_DENALI_PHY_1882 Register (Offset = 5D68h) [reset = 0h]

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Table 14-25059. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD68h**

Figure 14-8318. EMIF_CTLCFG_DENALI_PHY_1882 Name Register

31	30	29	28	27	26	25	24
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							

Table 14-25061. EMIF_CTLCFG_DENALI_PHY_1882 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS1_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 1 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1706 EMIF_CTLCFG_DENALI_PHY_1883 Register

1 EMIF_CTLCFG_DENALI_PHY_1883 Register (Offset = 5D6Ch) [reset = 0h]

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Table 14-25062. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD6Ch**

Figure 14-8319. EMIF_CTLCFG_DENALI_PHY_1883 Name Register

31	30	29	28	27	26	25	24
PHY_DS2_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS2_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS2_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS2_DQS_ERR_COUNTER							
R							
0h							

Table 14-25064. EMIF_CTLCFG_DENALI_PHY_1883 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS2_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 2 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1707 EMIF_CTLCFG_DENALI_PHY_1884 Register

1 EMIF_CTLCFG_DENALI_PHY_1884 Register (Offset = 5D70h) [reset = 0h]

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Table 14-25065. Instance Table

Instance Name	**Physical Address**
DDR32SS0	**0F30 DD70h**

Figure 14-8320. EMIF_CTLCFG_DENALI_PHY_1884 Name Register

31	30	29	28	27	26	25	24
PHY_DS3_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS3_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS3_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS3_DQS_ERR_COUNTER							
R							
0h							

Table 14-25067. EMIF_CTLCFG_DENALI_PHY_1884 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS3_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 3 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1708 EMIF_CTLCFG_DENALI_PHY_1885 Register

1 EMIF_CTLCFG_DENALI_PHY_1885 Register (Offset = 5D74h) [reset = 2h]

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Table 14-25068. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD74h**

Figure 14-8321. EMIF_CTLCFG_DENALI_PHY_1885 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_DS_INIT_COMPLETE_OBS			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_AC_INIT_COMPLETE_OBS			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AC_INIT_COMPLETE_OBS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DLL_RST_EN	
NONE						R/W	
0h						2h	

Table 14-25070. EMIF_CTLCFG_DENALI_PHY_1885 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_DS_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for data slice. Bit0 is for data_slice0; bit1 is for data_slice 1,... READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:8	PHY_AC_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for adr and ac slice. Bit 0 is for dfi_init_complete for all slices. Bit[7:4] is for adr slice, bit4 is adr_slice0..., if the adr slice number is 3, bit7 is 0. Bit8 is for ac_slice0; bit9 is for ac_slice 1,... READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DLL_RST_EN	R/W	2h	PHY DDL reset software interface enable. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1709 EMIF_CTLCFG_DENALI_PHY_1886 Register

1 EMIF_CTLCFG_DENALI_PHY_1886 Register (Offset = 5D78h) [reset = 0h]

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Table 14-25071. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DD78h

Figure 14-8322. EMIF_CTLCFG_DENALI_PHY_1886 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_GRP_SLV_DLY_ENC_OBS_SELECT				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							PHY_AC_DCC_RXCAL_CTRL_GATE_DISABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_ERR_IE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_UPDATE_MASK
NONE							R/W
0h							0h

Table 14-25073. EMIF_CTLCFG_DENALI_PHY_1886 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_GRP_SLV_DLY_ENC_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice target delay to the encoded value observation register. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_AC_DCC_RXCAL_CTRL_GATE_DISABLE	R/W	0h	Memory clock bit slice DCC block power reduction disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ERR_IE	R/W	0h	Control the IE signal of IO error pad. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_UPDATE_MASK	R/W	0h	Control to disable the generation of dfi_phyupd_req and use of dfi_ctrlupd_req. If this is 0 the PHY is normal mode; if this is 1, the PHY will not respond to dfi_ctrlupd_req or not to send dfi_phyupd_req Reset Source: ctl_amod_g_rst_n

14.6.6.2.1710 EMIF_CTLCFG_DENALI_PHY_1887 Register

1 EMIF_CTLCFG_DENALI_PHY_1887 Register (Offset = 5D7Ch) [reset = 0h]

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Table 14-25074. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD7Ch**

Figure 14-8323. EMIF_CTLCFG_DENALI_PHY_1887 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP_SHIFT_OBS		
NONE					R		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_GRP_SLV_DLY_ENC_OBS		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_GRP_SLV_DLY_ENC_OBS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_GRP_SHIFT_OBS_SELECT			
NONE				R/W			
0h				0h			

Table 14-25076. EMIF_CTLCFG_DENALI_PHY_1887 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_GRP_SHIFT_OBS	R	0h	Observation register for the address/control group automatic half cycle and cycle shift values. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_GRP_SLV_DLY_ENC_OBS	R	0h	Observation register for all address/control group slice target delay encoded values. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GRP_SHIFT_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice automatic cycle/half_cycle shift settings to the observation register. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1711 EMIF_CTLCFG_DENALI_PHY_1888 Register

1 EMIF_CTLCFG_DENALI_PHY_1888 Register (Offset = 5D80h) [reset = 0h]

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Table 14-25077. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD80h**

Figure 14-8324. EMIF_CTLCFG_DENALI_PHY_1888 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_CAL_IO_CFG_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CAL_IO_CFG_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CAL_IO_CFG_0							
R/W							
0h							

Table 14-25079. EMIF_CTLCFG_DENALI_PHY_1888 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CAL_IO_CFG_0	R/W	0h	Pad calibration Controls PCLK/PARK pin and vref switch. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1712 EMIF_CTLCFG_DENALI_PHY_1889 Register

1 EMIF_CTLCFG_DENALI_PHY_1889 Register (Offset = 5D84h) [reset = 0h]

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Table 14-25080. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD84h**

Figure 14-8325. EMIF_CTLCFG_DENALI_PHY_1889 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ACS_RX_PCLK_CLK_SEL		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_ACS_IO_CFG	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_PAD_ACS_IO_CFG							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_ACS_IO_CFG							
R/W							
0h							

Table 14-25082. EMIF_CTLCFG_DENALI_PHY_1889 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_PAD_ACS_RX_PCLK_CLK_SEL	R/W	0h	Controls rx_pclk clk selection for acs pad. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ACS_IO_CFG	R/W	0h	Controls PCLK/PARK pin for acs pad. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1713 EMIF_CTLCFG_DENALI_PHY_1890 Register

1 EMIF_CTLCFG_DENALI_PHY_1890 Register (Offset = 5D88h) [reset = 0h]

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Table 14-25083. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD88h**

Figure 14-8326. EMIF_CTLCFG_DENALI_PHY_1890 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-25085. EMIF_CTLCFG_DENALI_PHY_1890 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1714 EMIF_CTLCFG_DENALI_PHY_1891 Register

1 EMIF_CTLCFG_DENALI_PHY_1891 Register (Offset = 5D8Ch) [reset = 0h]

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Table 14-25086. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD8Ch**

Figure 14-8327. EMIF_CTLCFG_DENALI_PHY_1891 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_LOW_FREQ_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PHY_PLL_CTRL				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PHY_PLL_CTRL							
R/W							
0h							

Table 14-25088. EMIF_CTLCFG_DENALI_PHY_1891 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_LOW_FREQ_SEL	R/W	0h	Enables the PHY to enter/exit the PLL domain from the negative clock edge. Set to 1 at low frequencies to enable. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_PLL_CTRL	R/W	0h	PHY clock PLL controls. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1715 EMIF_CTLCFG_DENALI_PHY_1892 Register

1 EMIF_CTLCFG_DENALI_PHY_1892 Register (Offset = 5D90h) [reset = 0h]

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Table 14-25089. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD90h**

Figure 14-8328. EMIF_CTLCFG_DENALI_PHY_1892 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CSLVL_DLY_STEP			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_CSLVL_CAPTURE_CNT			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_PAD_VREF_CTRL_AC			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_VREF_CTRL_AC							
R/W							
0h							

Table 14-25091. EMIF_CTLCFG_DENALI_PHY_1892 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CSLVL_DLY_STEP	R/W	0h	Sets the delay step size plus 1 during CS training. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CSLVL_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP target delay setting during CS training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PAD_VREF_CTRL_AC	R/W	0h	Pad VREF control settings for the address/control. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1716 EMIF_CTLCFG_DENALI_PHY_1893 Register

1 EMIF_CTLCFG_DENALI_PHY_1893 Register (Offset = 5D94h) [reset = 0h]

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Table 14-25092. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD94h**

Figure 14-8329. EMIF_CTLCFG_DENALI_PHY_1893 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LVL_MEAS_DLY_STEP_ENABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_SW_CSLVL_DVW_MIN_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_SW_CSLVL_DVW_MIN	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_SW_CSLVL_DVW_MIN							
R/W							
0h							

Table 14-25094. EMIF_CTLCFG_DENALI_PHY_1893 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LVL_MEAS_DLY_STEP_ENABLE	R/W	0h	Enables the phy_adr_meas_dly_step_value to be used instead of the phy_cslvl_dly_step parameter. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SW_CSLVL_DVW_MIN_EN	R/W	0h	Enables the software override data valid window size during CS training. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_SW_CSLVL_DVW_MIN	R/W	0h	Sets the software override data valid window size during CS training. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1717 EMIF_CTLCFG_DENALI_PHY_1894 Register

1 EMIF_CTLCFG_DENALI_PHY_1894 Register (Offset = 5D98h) [reset = 0h]

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Table 14-25095. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD98h**

Figure 14-8330. EMIF_CTLCFG_DENALI_PHY_1894 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP1_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-25097. EMIF_CTLCFG_DENALI_PHY_1894 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1718 EMIF_CTLCFG_DENALI_PHY_1895 Register

1 EMIF_CTLCFG_DENALI_PHY_1895 Register (Offset = 5D9Ch) [reset = 0h]

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Table 14-25098. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DD9Ch**

Figure 14-8331. EMIF_CTLCFG_DENALI_PHY_1895 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_GRP3_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP2_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-25100. EMIF_CTLCFG_DENALI_PHY_1895 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1719 EMIF_CTLCFG_DENALI_PHY_1896 Register

1 EMIF_CTLCFG_DENALI_PHY_1896 Register (Offset = 5DA0h) [reset = 0h]

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Table 14-25101. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDA0h**

Figure 14-8332. EMIF_CTLCFG_DENALI_PHY_1896 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP1_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-25103. EMIF_CTLCFG_DENALI_PHY_1896 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1720 EMIF_CTLCFG_DENALI_PHY_1897 Register

1 EMIF_CTLCFG_DENALI_PHY_1897 Register (Offset = 5DA4h) [reset = 0h]

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Table 14-25104. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDA4h**

Figure 14-8333. EMIF_CTLCFG_DENALI_PHY_1897 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP3_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP2_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-25106. EMIF_CTLCFG_DENALI_PHY_1897 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1721 EMIF_CTLCFG_DENALI_PHY_1898 Register

1 EMIF_CTLCFG_DENALI_PHY_1898 Register (Offset = 5DA8h) [reset = 0h]

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Table 14-25107. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DDA8h

Figure 14-8334. EMIF_CTLCFG_DENALI_PHY_1898 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP1_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_2							
R/W							
0h							

Table 14-25109. EMIF_CTLCFG_DENALI_PHY_1898 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1722 EMIF_CTLCFG_DENALI_PHY_1899 Register

1 EMIF_CTLCFG_DENALI_PHY_1899 Register (Offset = 5DACh) [reset = 0h]

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Table 14-25110. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDACh**

Figure 14-8335. EMIF_CTLCFG_DENALI_PHY_1899 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP3_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP2_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP2_SLAVE_DELAY_2							
R/W							
0h							

Table 14-25112. EMIF_CTLCFG_DENALI_PHY_1899 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1723 EMIF_CTLCFG_DENALI_PHY_1900 Register

1 EMIF_CTLCFG_DENALI_PHY_1900 Register (Offset = 5DB0h) [reset = 0h]

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Table 14-25113. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDB0h**

Figure 14-8336. EMIF_CTLCFG_DENALI_PHY_1900 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_3							
R/W							
0h							

Table 14-25115. EMIF_CTLCFG_DENALI_PHY_1900 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1724 EMIF_CTLCFG_DENALI_PHY_1901 Register

1 EMIF_CTLCFG_DENALI_PHY_1901 Register (Offset = 5DB4h) [reset = 0h]

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Table 14-25116. Instance Table

Instance Name	Physical Address
DDR32SS0	0F30 DDB4h

Figure 14-8337. EMIF_CTLCFG_DENALI_PHY_1901 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP1_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP1_SLAVE_DELAY_3							
R/W							
0h							

Table 14-25118. EMIF_CTLCFG_DENALI_PHY_1901 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP1_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1725 EMIF_CTLCFG_DENALI_PHY_1902 Register

1 EMIF_CTLCFG_DENALI_PHY_1902 Register (Offset = 5DB8h) [reset = 0h]

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Table 14-25119. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDB8h**

Figure 14-8338. EMIF_CTLCFG_DENALI_PHY_1902 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_GRP2_SLAVE_DELAY_3</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_GRP2_SLAVE_DELAY_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25121. EMIF_CTLCFG_DENALI_PHY_1902 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1726 EMIF_CTLCFG_DENALI_PHY_1903 Register

1 EMIF_CTLCFG_DENALI_PHY_1903 Register (Offset = 5DBCh) [reset = 0h]

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Table 14-25122. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDBCh**

Figure 14-8339. EMIF_CTLCFG_DENALI_PHY_1903 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP3_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP3_SLAVE_DELAY_3							
R/W							
0h							

Table 14-25124. EMIF_CTLCFG_DENALI_PHY_1903 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP3_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1727 EMIF_CTLCFG_DENALI_PHY_1904 Register

1 EMIF_CTLCFG_DENALI_PHY_1904 Register (Offset = 5DC0h) [reset = 0h]

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Table 14-25125. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDC0h**

Figure 14-8340. EMIF_CTLCFG_DENALI_PHY_1904 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_DC_CAL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-25127. EMIF_CTLCFG_DENALI_PHY_1904 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PHY_CLK_DC_CAL_CLK_SEL	R/W	0h	Determines DCC CAL clock. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1728 EMIF_CTLCFG_DENALI_PHY_1905 Register

1 EMIF_CTLCFG_DENALI_PHY_1905 Register (Offset = 5DC4h) [reset = FFh]

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Table 14-25128. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDC4h**

Figure 14-8341. EMIF_CTLCFG_DENALI_PHY_1905 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_FDBK_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							

Table 14-25130. EMIF_CTLCFG_DENALI_PHY_1905 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_FDBK_DRIVE	R/W	FFh	Controls drive settings for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1729 EMIF_CTLCFG_DENALI_PHY_1906 Register

1 EMIF_CTLCFG_DENALI_PHY_1906 Register (Offset = 5DC8h) [reset = FFh]

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Table 14-25131. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDC8h**

Figure 14-8342. EMIF_CTLCFG_DENALI_PHY_1906 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_FDBK_DRIVE2	
NONE						R/W	
0h						FFh	
15	14	13	12	11	10	9	8
PHY_PAD_FDBK_DRIVE2							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_FDBK_DRIVE2							
R/W							
FFh							

Table 14-25133. EMIF_CTLCFG_DENALI_PHY_1906 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_FDBK_DRIVE2	R/W	FFh	Controls drive settings [enslice/boost] for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1730 EMIF_CTLCFG_DENALI_PHY_1907 Register

1 EMIF_CTLCFG_DENALI_PHY_1907 Register (Offset = 5DCCh) [reset = 0h]

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Table 14-25134. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDCCh**

Figure 14-8343. EMIF_CTLCFG_DENALI_PHY_1907 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PAD_DATA_DRIVE						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_PAD_DATA_DRIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_PAD_DATA_DRIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_DATA_DRIVE							
R/W							
0h							

Table 14-25136. EMIF_CTLCFG_DENALI_PHY_1907 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_PAD_DATA_DRIVE	R/W	0h	Controls drive settings for data pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1731 EMIF_CTLCFG_DENALI_PHY_1908 Register

1 EMIF_CTLCFG_DENALI_PHY_1908 Register (Offset = 5DD0h) [reset = 0h]

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Table 14-25137. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDD0h**

Figure 14-8344. EMIF_CTLCFG_DENALI_PHY_1908 Name Register

31	30	29	28	27	26	25	24
PHY_PAD_DQS_DRIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_PAD_DQS_DRIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_PAD_DQS_DRIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_DQS_DRIVE							
R/W							
0h							

Table 14-25139. EMIF_CTLCFG_DENALI_PHY_1908 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_PAD_DQS_DRIVE	R/W	0h	Controls drive settings for dqs pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1732 EMIF_CTLCFG_DENALI_PHY_1909 Register

1 EMIF_CTLCFG_DENALI_PHY_1909 Register (Offset = 5DD4h) [reset = FFh]

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Table 14-25140. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDD4h**

Figure 14-8345. EMIF_CTLCFG_DENALI_PHY_1909 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ADDR_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							

Table 14-25142. EMIF_CTLCFG_DENALI_PHY_1909 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ADDR_DRIVE	R/W	FFh	Controls drive settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1733 EMIF_CTLCFG_DENALI_PHY_1910 Register

1 EMIF_CTLCFG_DENALI_PHY_1910 Register (Offset = 5DD8h) [reset = FFFF00h]

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Table 14-25143. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDD8h**

Figure 14-8346. EMIF_CTLCFG_DENALI_PHY_1910 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ADDR_DRIVE2			
NONE				R/W			
0h				FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							

Table 14-25145. EMIF_CTLCFG_DENALI_PHY_1910 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ADDR_DRIVE2	R/W	FFFF00h	Controls drive settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1734 EMIF_CTLCFG_DENALI_PHY_1911 Register

1 EMIF_CTLCFG_DENALI_PHY_1911 Register (Offset = 5DDCh) [reset = FFh]

Return to Summary Table

Table 14-25146. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDDCh**

Figure 14-8347. EMIF_CTLCFG_DENALI_PHY_1911 Name Register

31	30	29	28	27	26	25	24
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
23	22	21	20	19	18	17	16
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_CLK_DRIVE							
R/W							
FFh							

Table 14-25148. EMIF_CTLCFG_DENALI_PHY_1911 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_PAD_CLK_DRIVE	R/W	FFh	Controls drive settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1735 EMIF_CTLCFG_DENALI_PHY_1912 Register

1 EMIF_CTLCFG_DENALI_PHY_1912 Register (Offset = 5DE0h) [reset = FFh]

Return to Summary Table

Table 14-25149. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDE0h**

Figure 14-8348. EMIF_CTLCFG_DENALI_PHY_1912 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_PAD_CLK_DRIVE2		
NONE					R/W		
0h					FFh		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CLK_DRIVE2							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CLK_DRIVE2							
R/W							
FFh							

Table 14-25151. EMIF_CTLCFG_DENALI_PHY_1912 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	PHY_PAD_CLK_DRIVE2	R/W	FFh	Controls drive settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1736 EMIF_CTLCFG_DENALI_PHY_1913 Register

1 EMIF_CTLCFG_DENALI_PHY_1913 Register (Offset = 5DE4h) [reset = FFh]

Return to Summary Table

Table 14-25152. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDE4h**

Figure 14-8349. EMIF_CTLCFG_DENALI_PHY_1913 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ERR_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							

Table 14-25154. EMIF_CTLCFG_DENALI_PHY_1913 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ERR_DRIVE	R/W	FFh	Controls drive settings for error pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1737 EMIF_CTLCFG_DENALI_PHY_1914 Register

1 EMIF_CTLCFG_DENALI_PHY_1914 Register (Offset = 5DE8h) [reset = FFFF00h]

Return to Summary Table

Table 14-25155. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDE8h**

Figure 14-8350. EMIF_CTLCFG_DENALI_PHY_1914 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ERR_DRIVE2			
NONE				R/W			
0h				FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							

Table 14-25157. EMIF_CTLCFG_DENALI_PHY_1914 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ERR_DRIVE2	R/W	FFFF00h	Controls drive settings for error pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1738 EMIF_CTLCFG_DENALI_PHY_1915 Register

1 EMIF_CTLCFG_DENALI_PHY_1915 Register (Offset = 5DECh) [reset = FFh]

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Table 14-25158. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDECh**

Figure 14-8351. EMIF_CTLCFG_DENALI_PHY_1915 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_CKE_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_CKE_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CKE_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CKE_DRIVE							
R/W							
FFh							

Table 14-25160. EMIF_CTLCFG_DENALI_PHY_1915 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_CKE_DRIVE	R/W	FFh	Controls drive settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1739 EMIF_CTLCFG_DENALI_PHY_1916 Register

1 EMIF_CTLCFG_DENALI_PHY_1916 Register (Offset = 5DF0h) [reset = 1FFFF00h]

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Table 14-25161. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDF0h**

Figure 14-8352. EMIF_CTLCFG_DENALI_PHY_1916 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_CKE_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							

Table 14-25163. EMIF_CTLCFG_DENALI_PHY_1916 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_CKE_DRIVE2	R/W	1FFFF00h	Controls drive settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1740 EMIF_CTLCFG_DENALI_PHY_1917 Register

1 EMIF_CTLCFG_DENALI_PHY_1917 Register (Offset = 5DF4h) [reset = FFh]

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Table 14-25164. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDF4h**

Figure 14-8353. EMIF_CTLCFG_DENALI_PHY_1917 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_RST_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_RST_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_RST_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_RST_DRIVE							
R/W							
FFh							

Table 14-25166. EMIF_CTLCFG_DENALI_PHY_1917 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_RST_DRIVE	R/W	FFh	Controls drive settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1741 EMIF_CTLCFG_DENALI_PHY_1918 Register

1 EMIF_CTLCFG_DENALI_PHY_1918 Register (Offset = 5DF8h) [reset = 1FFFF00h]

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Table 14-25167. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDF8h**

Figure 14-8354. EMIF_CTLCFG_DENALI_PHY_1918 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_PAD_RST_DRIVE2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1FFFF00h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_PAD_RST_DRIVE2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1FFFF00h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_RST_DRIVE2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1FFFF00h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_RST_DRIVE2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1FFFF00h</td></tr>
</table>

Table 14-25169. EMIF_CTLCFG_DENALI_PHY_1918 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_RST_DRIVE2	R/W	1FFFF00h	Controls drive settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1742 EMIF_CTLCFG_DENALI_PHY_1919 Register

1 EMIF_CTLCFG_DENALI_PHY_1919 Register (Offset = 5DFCh) [reset = FFh]

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Table 14-25170. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DDFCh**

Figure 14-8355. EMIF_CTLCFG_DENALI_PHY_1919 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_CS_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_CS_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CS_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CS_DRIVE							
R/W							
FFh							

Table 14-25172. EMIF_CTLCFG_DENALI_PHY_1919 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_CS_DRIVE	R/W	FFh	Controls drive settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1743 EMIF_CTLCFG_DENALI_PHY_1920 Register

1 EMIF_CTLCFG_DENALI_PHY_1920 Register (Offset = 5E00h) [reset = 1FFFF00h]

Return to Summary Table

Table 14-25173. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DE00h**

Figure 14-8356. EMIF_CTLCFG_DENALI_PHY_1920 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_CS_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							

Table 14-25175. EMIF_CTLCFG_DENALI_PHY_1920 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_CS_DRIVE2	R/W	1FFFF00h	Controls drive settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1744 EMIF_CTLCFG_DENALI_PHY_1921 Register

1 EMIF_CTLCFG_DENALI_PHY_1921 Register (Offset = 5E04h) [reset = FFh]

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Table 14-25176. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DE04h**

Figure 14-8357. EMIF_CTLCFG_DENALI_PHY_1921 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ODT_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_ODT_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_ODT_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_ODT_DRIVE							
R/W							
FFh							

Table 14-25178. EMIF_CTLCFG_DENALI_PHY_1921 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ODT_DRIVE	R/W	FFh	Controls drive settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1745 EMIF_CTLCFG_DENALI_PHY_1922 Register

1 EMIF_CTLCFG_DENALI_PHY_1922 Register (Offset = 5E08h) [reset = 1FFFF00h]

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Table 14-25179. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DE08h**

Figure 14-8358. EMIF_CTLCFG_DENALI_PHY_1922 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ODT_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							

Table 14-25181. EMIF_CTLCFG_DENALI_PHY_1922 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ODT_DRIVE2	R/W	1FFFF00h	Controls drive settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.6.6.2.1746 EMIF_CTLCFG_DENALI_PHY_1923 Register

1 EMIF_CTLCFG_DENALI_PHY_1923 Register (Offset = 5E0Ch) [reset = 0h]

Return to Summary Table

Table 14-25182. Instance Table

Instance Name	Physical Address
DDR32SS0	**0F30 DE0Ch**

Figure 14-8359. EMIF_CTLCFG_DENALI_PHY_1923 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_CAL_SETTLING_PRD_0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_CAL_CLK_SELECT_0		
NONE					R/W		
0h					0h		

Table 14-25184. EMIF_CTLCFG_DENALI_PHY_1923 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_CAL_SETTLING_PRD_0	R/W	0h	Number of clock cycles to extend dfi_phyupd_req after the ack is received for settling of final values Reset Source: ctl_amod_g_rst_n
23:8	PHY_CAL_VREF_SWITCH_TIMER_0	R/W	0h	The settling time for a switch in VREF during IO pad calibration. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for block 0. Reset Source: ctl_amod_g_rst_n

14.7 Time Sync Registers

14.7.1 timesync_event_router

timesync_event_router

14.7.1.1 timesync_event_router Summaries

timesync_event_router Summaries

Table 14-25185. INTR_ROUTER_CFG Registers, Base Address=00A4 0000h, Length=1024

Offset	Length	Register Name	TIMESYNC_EVENT_ROUTER0 Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A4 0000h
4h	32	INTR_ROUTER_CFG_MUXCNTL_J	00A4 0004h + formula

14.7.1.2 timesync_event_router Registers

timesync_event_router Registers

14.7.1.2.1 INTR_ROUTER_CFG_PID Register

1 INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register

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Table 14-25186. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_ROUTER0	**00A4 0000h**

Figure 14-8360. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
694h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-25188. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.7.1.2.2 INTR_ROUTER_CFG_MUXCNTL_j Register

1 INTR_ROUTER_CFG_MUXCNTL_j Register (Offset = 4h + formula) [reset = 0h]

Interrupt mux control register

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Offset = 4h + (j * 4h); where j = 0 to 25d

Table 14-25189. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_ROUTER0	**00A4 0004h + formula**

Figure 14-8361. INTR_ROUTER_CFG_MUXCNTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>INT_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MUX_CNTL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-25191. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.8 DMA Controller Registers

14.8.1 DMASS_BCDMA_0

DMASS_BCDMA_0

14.8.1.1 DMASS_BCDMA_0 Summaries

DMASS_BCDMA_0 Summaries

Table 14-25192. LCDMA_RINGACC_CRED Registers, Base Address=4581 2000h, Length=2048

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	LCDMA_RINGACC_CRED_RING_CRED_J	4581 2000h + formula

Table 14-25193. BCDMA_BCCFG Registers, Base Address=4842 0000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCCFG_CHAN_CFG_J	4842 0000h + formula
64h	32	BCDMA_BCCFG_CHAN_PRI_CTRL_J	4842 0064h + formula
80h	32	BCDMA_BCCFG_CHAN_TST_SCHED_J	4842 0080h + formula

Table 14-25194. BCDMA_TXCCFG Registers, Base Address=484A 4000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCCFG_CHAN_TCFG_J	484A 4000h + formula
64h	32	BCDMA_TXCCFG_CHAN_TPRI_CTRL_J	484A 4064h + formula
68h	32	BCDMA_TXCCFG_CHAN_THREAD_J	484A 4068h + formula
70h	32	BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_J	484A 4070h + formula
80h	32	BCDMA_TXCCFG_CHAN_TST_SCHED_J	484A 4080h + formula

Table 14-25195. BCDMA_RXCCFG Registers, Base Address=484C 2000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCCFG_CHAN_RCFG_J	484C 2000h + formula
64h	32	BCDMA_RXCCFG_CHAN_RPRI_CTRL_J	484C 2064h + formula
68h	32	BCDMA_RXCCFG_CHAN_THREAD_J	484C 2068h + formula
80h	32	BCDMA_RXCCFG_CHAN_RST_SCHED_J	484C 2080h + formula

Table 14-25196. BCDMA_GCFG Registers, Base Address=485C 0100h, Length=256

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_GCFG_REVISION	485C 0100h
4h	32	BCDMA_GCFG_PERF_CTRL	485C 0104h
8h	32	BCDMA_GCFG_EMU_CTRL	485C 0108h
10h	32	BCDMA_GCFG_PSIL_TO	485C 0110h
20h	32	BCDMA_GCFG_CAP0	485C 0120h
24h	32	BCDMA_GCFG_CAP1	485C 0124h
28h	32	BCDMA_GCFG_CAP2	485C 0128h
2Ch	32	BCDMA_GCFG_CAP3	485C 012Ch
30h	32	BCDMA_GCFG_CAP4	485C 0130h
60h	32	BCDMA_GCFG_PM0	485C 0160h
64h	32	BCDMA_GCFG_PM1	485C 0164h

Table 14-25196. BCDMA_GCFG Registers, Base Address=485C 0100h, Length=256 (continued)

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
78h	32	BCDMA_GCFG_DBGADDR	485C 0178h
7Ch	32	BCDMA_GCFG_DBGDATA	485C 017Ch

Table 14-25197. LCDMA_RINGACC_RING_CFG Registers, Base Address=4860 0000h, Length=32768

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
40h	32	LCDMA_RINGACC_RING_CFG_RING_BA_LO_J	4860 0040h + formula
44h	32	LCDMA_RINGACC_RING_CFG_RING_BA_HI_J	4860 0044h + formula
48h	32	LCDMA_RINGACC_RING_CFG_RING_SIZE_J	4860 0048h + formula

Table 14-25198. BCDMA_RXCRT Registers, Base Address=4A82 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCRT_CHAN_CTL_J	4A82 0000h + formula
8h	32	BCDMA_RXCRT_CHAN_SWTRIG_J	4A82 0008h + formula
40h	32	BCDMA_RXCRT_CHAN_STATUS0_J	4A82 0040h + formula
44h	32	BCDMA_RXCRT_CHAN_STATUS1_J	4A82 0044h + formula
80h	32	BCDMA_RXCRT_CHAN_STDATA_J_K	4A82 0080h + formula
200h	32	BCDMA_RXCRT_CHAN_PEER0_J	4A82 0200h + formula
204h	32	BCDMA_RXCRT_CHAN_PEER1_J	4A82 0204h + formula
208h	32	BCDMA_RXCRT_CHAN_PEER2_J	4A82 0208h + formula
20Ch	32	BCDMA_RXCRT_CHAN_PEER3_J	4A82 020Ch + formula
210h	32	BCDMA_RXCRT_CHAN_PEER4_J	4A82 0210h + formula
214h	32	BCDMA_RXCRT_CHAN_PEER5_J	4A82 0214h + formula
218h	32	BCDMA_RXCRT_CHAN_PEER6_J	4A82 0218h + formula
21Ch	32	BCDMA_RXCRT_CHAN_PEER7_J	4A82 021Ch + formula
220h	32	BCDMA_RXCRT_CHAN_PEER8_J	4A82 0220h + formula
224h	32	BCDMA_RXCRT_CHAN_PEER9_J	4A82 0224h + formula
228h	32	BCDMA_RXCRT_CHAN_PEER10_J	4A82 0228h + formula
22Ch	32	BCDMA_RXCRT_CHAN_PEER11_J	4A82 022Ch + formula
230h	32	BCDMA_RXCRT_CHAN_PEER12_J	4A82 0230h + formula
234h	32	BCDMA_RXCRT_CHAN_PEER13_J	4A82 0234h + formula
238h	32	BCDMA_RXCRT_CHAN_PEER14_J	4A82 0238h + formula
23Ch	32	BCDMA_RXCRT_CHAN_PEER15_J	4A82 023Ch + formula
400h	32	BCDMA_RXCRT_CHAN_PCNT_J	4A82 0400h + formula
408h	32	BCDMA_RXCRT_CHAN_BCNT_J	4A82 0408h + formula
410h	32	BCDMA_RXCRT_CHAN_SBCNT_J	4A82 0410h + formula

Table 14-25199. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCRT_CHAN_CTL_J	4AA4 0000h + formula
8h	32	BCDMA_TXCRT_CHAN_SWTRIG_J	4AA4 0008h + formula
40h	32	BCDMA_TXCRT_CHAN_STATUS0_J	4AA4 0040h + formula
44h	32	BCDMA_TXCRT_CHAN_STATUS1_J	4AA4 0044h + formula
80h	32	BCDMA_TXCRT_CHAN_STDATA_J_K	4AA4 0080h + formula

Table 14-25199. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=131072 (continued)

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
200h	32	BCDMA_TXCRT_CHAN_PEER0_J	4AA4 0200h + formula
204h	32	BCDMA_TXCRT_CHAN_PEER1_J	4AA4 0204h + formula
208h	32	BCDMA_TXCRT_CHAN_PEER2_J	4AA4 0208h + formula
20Ch	32	BCDMA_TXCRT_CHAN_PEER3_J	4AA4 020Ch + formula
210h	32	BCDMA_TXCRT_CHAN_PEER4_J	4AA4 0210h + formula
214h	32	BCDMA_TXCRT_CHAN_PEER5_J	4AA4 0214h + formula
218h	32	BCDMA_TXCRT_CHAN_PEER6_J	4AA4 0218h + formula
21Ch	32	BCDMA_TXCRT_CHAN_PEER7_J	4AA4 021Ch + formula
220h	32	BCDMA_TXCRT_CHAN_PEER8_J	4AA4 0220h + formula
224h	32	BCDMA_TXCRT_CHAN_PEER9_J	4AA4 0224h + formula
228h	32	BCDMA_TXCRT_CHAN_PEER10_J	4AA4 0228h + formula
22Ch	32	BCDMA_TXCRT_CHAN_PEER11_J	4AA4 022Ch + formula
230h	32	BCDMA_TXCRT_CHAN_PEER12_J	4AA4 0230h + formula
234h	32	BCDMA_TXCRT_CHAN_PEER13_J	4AA4 0234h + formula
238h	32	BCDMA_TXCRT_CHAN_PEER14_J	4AA4 0238h + formula
23Ch	32	BCDMA_TXCRT_CHAN_PEER15_J	4AA4 023Ch + formula
400h	32	BCDMA_TXCRT_CHAN_PCNT_J	4AA4 0400h + formula
408h	32	BCDMA_TXCRT_CHAN_BCNT_J	4AA4 0408h + formula
410h	32	BCDMA_TXCRT_CHAN_SBCNT_J	4AA4 0410h + formula

Table 14-25200. LCDMA_RINGACC_RINGRT Registers, Base Address=4BC0 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
10h	32	LCDMA_RINGACC_RINGRT_RING_FDB_J	4BC0 0010h + formula
18h	32	LCDMA_RINGACC_RINGRT_RING_FOCC_J	4BC0 0018h + formula
1010h	32	LCDMA_RINGACC_RINGRT_RING_RDB_J	4BC0 1010h + formula
1018h	32	LCDMA_RINGACC_RINGRT_RING_ROCC_J	4BC0 1018h + formula

Table 14-25201. BCDMA_BCRT Registers, Base Address=4C00 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCRT_CHAN_CTL_J	4C00 0000h + formula
8h	32	BCDMA_BCRT_CHAN_SWTRIG_J	4C00 0008h + formula
40h	32	BCDMA_BCRT_CHAN_STATUS0_J	4C00 0040h + formula
44h	32	BCDMA_BCRT_CHAN_STATUS1_J	4C00 0044h + formula
48h	32	BCDMA_BCRT_CHAN_STATUS2_J	4C00 0048h + formula
4Ch	32	BCDMA_BCRT_CHAN_STATUS3_J	4C00 004Ch + formula
80h	32	BCDMA_BCRT_CHAN_STDATA_J_K	4C00 0080h + formula
100h	32	BCDMA_BCRT_CHAN_STDATAW_J_K	4C00 0100h + formula
400h	32	BCDMA_BCRT_CHAN_PCNT_J	4C00 0400h + formula
408h	32	BCDMA_BCRT_CHAN_BCNT_J	4C00 0408h + formula
410h	32	BCDMA_BCRT_CHAN_SBCNT_J	4C00 0410h + formula

14.8.1.2 DMASS_BCDMA_0 Registers

DMASS_BCDMA_0 Registers

14.8.1.2.1 LCDMA_RINGACC_CRED_RING_CRED_j Register

1 LCDMA_RINGACC_CRED_RING_CRED_j Register (Offset = 0h + formula) [reset = 0h]

The Credentials Register provides credentials to be used when performing memory accesses using this flow.

Return to Summary Table

Offset = 0h + (j * 10h); where j = 0 to 81d

Table 14-25202. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4581 2000h + formula**

Figure 14-8362. LCDMA_RINGACC_CRED_RING_CRED_j Name Register

31	30	29	28	27	26	25	24
RESERVED					SECURE	PRIV	
NONE					R/W	R/W	
0h					0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIVID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-25204. LCDMA_RINGACC_CRED_RING_CRED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	SECURE	R/W	0h	Secure attribute Reset Source: rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Privelege attribute Reset Source: rst_mod_g_rst_n
23:16	PRIVID	R/W	0h	Privelege ID attribute Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.8.1.2.2 BCDMA_BCCFG_CHAN_CFG_j Register

1 BCDMA_BCCFG_CHAN_CFG_j Register (Offset = 0h + formula) [reset = C0400h]

The Channel Configuration Register is used to initialize static mode settings for the Block Copy DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Return to Summary Table

Offset = 0h + (j * 100h); where j = 0 to 31d

Table 14-25205. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4842 0000h + formula**

Figure 14-8363. BCDMA_BCCFG_CHAN_CFG_j Name Register

31	30	29	28	27	26	25	24
PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CHAN_TYPE			
NONE				R/NA			
0h				Ch			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				BURST_SIZE		RESERVED	
NONE				R/W		NONE	
0h				1h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-25207. BCDMA_BCCFG_CHAN_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	CHAN_TYPE	R/NA	Ch	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-11 = RESERVED 12 = Channel performs Third Party Block Copy DMA transfers from memory to memory using pass by reference rings. 13-15 = RESERVED Reset Source: rst_mod_g_rst_n `12      Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved

Table 14-25207. BCDMA_BCCFG_CHAN_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.8.1.2.3 BCDMA_BCCFG_CHAN_PRI_CTRL_j Register

1 BCDMA_BCCFG_CHAN_PRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = 64h + (j * 100h); where j = 0 to 31d

Table 14-25208. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4842 0064h + formula**

Figure 14-8364. BCDMA_BCCFG_CHAN_PRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-25210. BCDMA_BCCFG_CHAN_PRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.4 BCDMA_BCCFG_CHAN_TST_SCHED_j Register

1 BCDMA_BCCFG_CHAN_TST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = 80h + (j * 100h); where j = 0 to 31d

Table 14-25211. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4842 0080h + formula**

Figure 14-8365. BCDMA_BCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-25213. BCDMA_BCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx/Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.8.1.2.5 BCDMA_TXCCFG_CHAN_TCFG_j Register

1 BCDMA_TXCCFG_CHAN_TCFG_j Register (Offset = 0h + formula) [reset = A0400h]

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Return to Summary Table

Offset = 0h + (j * 100h); where j = 0 to 21d

Table 14-25214. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4000h + formula**

Figure 14-8366. BCDMA_TXCCFG_CHAN_TCFG_j Name Register

31	30	29	28	27	26	25	24
TX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				TX_CHAN_TYPE			
NONE				R/NA			
0h				Ah			
15	14	13	12	11	10	9	8
RESERVED				TX_BURST_SIZE		TX_TDTYPE	TX_NOTDPKT
NONE				R/W		R/W	R/W
0h				1h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25216. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	TX_CHAN_TYPE	R/NA	Ah	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from memory to PSI-L using pass by reference rings. 11-15 = RESERVED Reset Source: rst_mod_g_rst_n `12      Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved

Table 14-25216. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	TX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9	TX_TDTYPE	R/W	0h	Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral. 0 = return immediately once all traffic is complete in BCDMA. 1 = wait until remote peer sends back a completion message. Reset Source: rst_mod_g_rst_n
8	TX_NOTDPKT	R/W	0h	Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete. 0 = TD packet is sent 1 = Suppress sending TD packet Reset Source: rst_mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.8.1.2.6 BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register

1 BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = 64h + (j * 100h); where j = 0 to 21d

Table 14-25217. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4064h + formula**

Figure 14-8367. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-25219. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.7 BCDMA_TXCCFG_CHAN_THREAD_j Register

1 BCDMA_TXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = 68h + (j * 100h); where j = 0 to 21d

Table 14-25220. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4068h + formula

Figure 14-8368. BCDMA_TXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-25222. BCDMA_TXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.8 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register

1 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register (Offset = 70h + formula) [reset = C0h]

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects.

Return to Summary Table

Offset = 70h + (j * 100h); where j = 0 to 21d

Table 14-25223. Instance Table

Instance Name	**Physical Address**
DMASS0_BCDMA_0	**484A 4070h + formula**

Figure 14-8369. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDEPTH							
R/W							
C0h							

Table 14-25225. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDEPTH	R/W	C0h	FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel. The minimum value is equal to the PSI-L interface data path width (tstrm_wdth), the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth). The fdepth must always be an integer multiple of tstrm_wdth. The reset value of this register varies by channel class (ultra-high capacity/high capacity/normal capacity) but will be equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth). Reset Source: rst_mod_g_rst_n

14.8.1.2.9 BCDMA_TXCCFG_CHAN_TST_SCHED_j Register

1 BCDMA_TXCCFG_CHAN_TST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = 80h + (j * 100h); where j = 0 to 21d

Table 14-25226. Instance Table

Instance Name	**Physical Address**
DMASS0_BCDMA_0	**484A 4080h + formula**

Figure 14-8370. BCDMA_TXCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-25228. BCDMA_TXCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.8.1.2.10 BCDMA_RXCCFG_CHAN_RCFG_j Register

1 BCDMA_RXCCFG_CHAN_RCFG_j Register (Offset = 0h + formula) [reset = A0400h]

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

Return to Summary Table

Offset = 0h + (j * 100h); where j = 0 to 27d

Table 14-25229. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2000h + formula**

Figure 14-8371. BCDMA_RXCCFG_CHAN_RCFG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RX_PAUSE_ON_ERR</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RX_CHAN_TYPE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/NA</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>RX_IGNORE_LONG</td><td colspan="2">RESERVED</td><td colspan="2">RX_BURST_SIZE</td><td colspan="2">RESERVED</td></tr>
<tr><td>NONE</td><td>R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td><td colspan="2">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">1h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25231. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	RX_CHAN_TYPE	R/NA	Ah	Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from PSI-L to memory using pass by reference rings. 11-15 = RESERVED Reset Source: rst_mod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-25231. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RX_IGNORE_LONG	R/W	0h	This field controls whether or not long packets will be treated as exceptions or ignored for the channel. This field is only used when the channel is in split UTC mode. The values are encoded as follows: 0 = Long packets are treated as exceptions and handled appropriately. 1 = Long packets are ignored and the next TR will be fetched even if the current TR is marked or interpreted as EOP. Reset Source: rst_mod_g_rst_n
13:12	RESERVED	NONE	0h	Reserved
11:10	RX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes only if the channel buffer size is greater than 128 bytes 2 = 128 Bytes only if the channel buffer size is greater than 192 bytes 3 = 256 bytes only if the channel buffer size is greater than 320 bytes The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.8.1.2.11 BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register

1 BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = 64h + (j * 100h); where j = 0 to 27d

Table 14-25232. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2064h + formula**

Figure 14-8372. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-25234. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.12 BCDMA_RXCCFG_CHAN_THREAD_j Register

1 BCDMA_RXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = 68h + (j * 100h); where j = 0 to 27d

Table 14-25235. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2068h + formula**

Figure 14-8373. BCDMA_RXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-25237. BCDMA_RXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.13 BCDMA_RXCCFG_CHAN_RST_SCHED_j Register

1 BCDMA_RXCCFG_CHAN_RST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = 80h + (j * 100h); where j = 0 to 27d

Table 14-25238. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2080h + formula**

Figure 14-8374. BCDMA_RXCCFG_CHAN_RST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-25240. BCDMA_RXCCFG_CHAN_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.8.1.2.14 BCDMA_GCFG_REVISION Register

1 BCDMA_GCFG_REVISION Register (Offset = 0h) [reset = 662EB101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-25241. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0100h**

Figure 14-8375. BCDMA_GCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
662Eh							
23	22	21	20	19	18	17	16
MODID							
R							
662Eh							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
16h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-25243. BCDMA_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	662Eh	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	16h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: rst_mod_g_rst_n

14.8.1.2.15 BCDMA_GCFG_PERF_CTRL Register

1 BCDMA_GCFG_PERF_CTRL Register (Offset = 4h) [reset = 40h]

The performance control register contains fields which can be used to adjust the performance of the BCDMA in the system.

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Table 14-25244. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0104h**

Figure 14-8376. BCDMA_GCFG_PERF_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TIMEOUT_CNT							
R/W							
40h							
7	6	5	4	3	2	1	0
TIMEOUT_CNT							
R/W							
40h							

Table 14-25246. BCDMA_GCFG_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TIMEOUT_CNT	R/W	40h	This feature is not currently supported. Reset Source: rst_mod_g_rst_n

14.8.1.2.16 BCDMA_GCFG_EMU_CTRL Register

1 BCDMA_GCFG_EMU_CTRL Register (Offset = 8h) [reset = 0h]

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

Return to Summary Table

Table 14-25247. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0108h**

Figure 14-8377. BCDMA_GCFG_EMU_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-25249. BCDMA_GCFG_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Soft Reset Source: rst_mod_g_rst_n
0	FREE	R/W	0h	Free Reset Source: rst_mod_g_rst_n

14.8.1.2.17 BCDMA_GCFG_PSIL_TO Register

1 BCDMA_GCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

Return to Summary Table

Table 14-25250. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0110h**

Figure 14-8378. BCDMA_GCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-25252. BCDMA_GCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: rst_mod_g_rst_n

14.8.1.2.18 BCDMA_GCFG_CAP0 Register

1 BCDMA_GCFG_CAP0 Register (Offset = 20h) [reset = A800Fh]

The Capabilities Register 0 specifies which standard features this BCDMA instance supports.

Return to Summary Table

Table 14-25253. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0120h**

Figure 14-8379. BCDMA_GCFG_CAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GLOBAL_TRIG	LOCAL_TRIG	EOL	STATIC
NONE				R	R	R	R
0h				1h	0h	1h	0h
15	14	13	12	11	10	9	8
TYPE15	TYPE14	TYPE13	TYPE12	TYPE11	TYPE10	TYPE9	TYPE8
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	1h	1h	1h	1h

Table 14-25255. BCDMA_GCFG_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GLOBAL_TRIG	R	1h	Global triggers 0 and 1 are supported Reset Source: rst_mod_g_rst_n
18	LOCAL_TRIG	R	0h	Dedicated local trigger is supported Reset Source: rst_mod_g_rst_n
17	EOL	R	1h	EOL field is supported Reset Source: rst_mod_g_rst_n
16	STATIC	R	0h	STATIC field is supported Reset Source: rst_mod_g_rst_n
15	TYPE15	R	1h	Type 15 TR is supported Reset Source: rst_mod_g_rst_n
14	TYPE14	R	0h	Type 14 TR is supported Reset Source: rst_mod_g_rst_n
13	TYPE13	R	0h	Type 13 TR is supported Reset Source: rst_mod_g_rst_n
12	TYPE12	R	0h	Type 12 TR is supported Reset Source: rst_mod_g_rst_n

Table 14-25255. BCDMA_GCFG_CAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TYPE11	R	0h	Type 11 TR is supported Reset Source: rst_mod_g_rst_n
10	TYPE10	R	0h	Type 10 TR is supported Reset Source: rst_mod_g_rst_n
9	TYPE9	R	0h	Type 9 TR is supported Reset Source: rst_mod_g_rst_n
8	TYPE8	R	0h	Type 8 TR is supported Reset Source: rst_mod_g_rst_n
7	TYPE7	R	0h	Type 7 TR is supported Reset Source: rst_mod_g_rst_n
6	TYPE6	R	0h	Type 6 TR is supported Reset Source: rst_mod_g_rst_n
5	TYPE5	R	0h	Type 5 TR is supported Reset Source: rst_mod_g_rst_n
4	TYPE4	R	0h	Type 4 TR is supported Reset Source: rst_mod_g_rst_n
3	TYPE3	R	1h	Type 3 TR is supported Reset Source: rst_mod_g_rst_n
2	TYPE2	R	1h	Type 2 TR is supported Reset Source: rst_mod_g_rst_n
1	TYPE1	R	1h	Type 1 TR is supported Reset Source: rst_mod_g_rst_n
0	TYPE0	R	1h	Type 0 TR is supported Reset Source: rst_mod_g_rst_n

14.8.1.2.19 BCDMA_GCFG_CAP1 Register

1 BCDMA_GCFG_CAP1 Register (Offset = 24h) [reset = 0h]

The Capabilities Register 1 specifies which standard features this BCDMA instance supports.

Return to Summary Table

Table 14-25256. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0124h**

Figure 14-8380. BCDMA_GCFG_CAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>SECTR</td><td>DFMT</td><td>ELTYPE</td><td>AMODE</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25258. BCDMA_GCFG_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	SECTR	R	0h	Maximum second TR function that is supported Reset Source: rst_mod_g_rst_n
2	DFMT	R	0h	Maximum data reformatting function that is supported Reset Source: rst_mod_g_rst_n
1	ELTYPE	R	0h	Maximum element type value that is supported. Reset Source: rst_mod_g_rst_n
0	AMODE	R	0h	The maximum AMODE that is supported. If AMODE is supported then DIR field must be supported for that AMODE. Reset Source: rst_mod_g_rst_n

14.8.1.2.20 BCDMA_GCFG_CAP2 Register

1 BCDMA_GCFG_CAP2 Register (Offset = 28h) [reset = 702C20h]

The Capabilities Register 2 specifies how many resources this BCDMA instance supports.

Return to Summary Table

Table 14-25259. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0128h**

Figure 14-8381. BCDMA_GCFG_CAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">RCHAN_CNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1Ch</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RCHAN_CNT</td><td colspan="2">TCHAN_CNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">1Ch</td><td colspan="2">16h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">TCHAN_CNT</td><td>CHAN_CNT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">16h</td><td>20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CHAN_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-25261. BCDMA_GCFG_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:18	RCHAN_CNT	R	1Ch	Rx split channel count Reset Source: rst_mod_g_rst_n
17:9	TCHAN_CNT	R	16h	Tx split channel count Reset Source: rst_mod_g_rst_n
8:0	CHAN_CNT	R	20h	BC channel count Reset Source: rst_mod_g_rst_n

14.8.1.2.21 BCDMA_GCFG_CAP3 Register

1 BCDMA_GCFG_CAP3 Register (Offset = 2Ch) [reset = 0h]

The Capabilities Register 3 specifies how many resources this BCDMA instance supports.

Return to Summary Table

Table 14-25262. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 012Ch**

Figure 14-8382. BCDMA_GCFG_CAP3 Name Register

31	30	29	28	27	26	25	24
UCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
UCHAN_CNT	HCHAN_CNT						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
HCHAN_CNT		RESERVED					
R		NONE					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25264. BCDMA_GCFG_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	UCHAN_CNT	R	0h	BC ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
22:14	HCHAN_CNT	R	0h	BC high capacity internal channel count Reset Source: rst_mod_g_rst_n
13:0	RESERVED	NONE	0h	Reserved

14.8.1.2.22 BCDMA_GCFG_CAP4 Register

1 BCDMA_GCFG_CAP4 Register (Offset = 30h) [reset = 6h]

The Capabilities Register 4 specifies how many resources this BCDMA instance supports.

Return to Summary Table

Table 14-25265. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0130h**

Figure 14-8383. BCDMA_GCFG_CAP4 Name Register

31	30	29	28	27	26	25	24
TUCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
THCHAN_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RUCHAN_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RHCHAN_CNT							
R							
6h							

Table 14-25267. BCDMA_GCFG_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TUCHAN_CNT	R	0h	TX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
23:16	THCHAN_CNT	R	0h	TX high capacity internal channel count Reset Source: rst_mod_g_rst_n
15:8	RUCHAN_CNT	R	0h	RX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
7:0	RHCHAN_CNT	R	6h	RX high capacity internal channel count Reset Source: rst_mod_g_rst_n

14.8.1.2.23 BCDMA_GCFG_PM0 Register

1 BCDMA_GCFG_PM0 Register (Offset = 60h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-25268. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0160h**

Figure 14-8384. BCDMA_GCFG_PM0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NOGATE_RSVD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NOGATE_RSVD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NOGATE_RSVD4</td><td>NOGATE_RDEC2</td><td colspan="2">NOGATE_RSVD3</td><td>NOGATE_SDEC3</td><td colspan="3">NOGATE_RSVD2</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NOGATE_WARB3</td><td colspan="3">NOGATE_RSVD1</td><td>NOGATE_CARB3</td><td>NOGATE_CARB2</td><td colspan="2">NOGATE_RSVD0</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-25270. BCDMA_GCFG_PM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NOGATE_RSVD4	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
14	NOGATE_RDEC2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
13:12	NOGATE_RSVD3	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
11	NOGATE_SDEC3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
10:8	NOGATE_RSVD2	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
7	NOGATE_WARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6:4	NOGATE_RSVD1	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
3	NOGATE_CARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-25270. BCDMA_GCFG_PM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NOGATE_CARB2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
1:0	NOGATE_RSVD0	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n

14.8.1.2.24 BCDMA_GCFG_PM1 Register

1 BCDMA_GCFG_PM1 Register (Offset = 64h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-25271. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0164h**

Figure 14-8385. BCDMA_GCFG_PM1 Name Register

31	30	29	28	27	26	25	24
NOGATE_EDC	NOGATE_STATS	NOGATE_PROXY	NOGATE_PSILIF	NOGATE_P2P	NOGATE_RSVD8	NOGATE_EHANDLER	NOGATE_RINGOCC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOGATE_RPCF	NOGATE_TPCF	NOGATE_PCF	NOGATE_RSVD7		NOGATE_CFG	NOGATE_RSVD6	
R/W	R/W	R/W	R/W		R/W	R/W	
0h	0h	0h	0h		0h	0h	
15	14	13	12	11	10	9	8
NOGATE_RSVD6					NOGATE_TRCU	NOGATE_RSVD5	NOGATE_EVTCU
R/W					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
NOGATE_RWU3	NOGATE_RWU2	NOGATE_RWU1	NOGATE_RWU0	NOGATE_TRU3	NOGATE_TRU2	NOGATE_TRU1	NOGATE_TRU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25273. BCDMA_GCFG_PM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_EDC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
30	NOGATE_STATS	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_PROXY	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_PSILIF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
27	NOGATE_P2P	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_RSVD8	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
25	NOGATE_EHANDLER	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-25273. BCDMA_GCFG_PM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NOGATE_RINGOCC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
23	NOGATE_RPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
22	NOGATE_TPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
21	NOGATE_PCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
20:19	NOGATE_RSVD7	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
18	NOGATE_CFG	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
17:11	NOGATE_RSVD6	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
10	NOGATE_TRCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
9	NOGATE_RSVD5	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
8	NOGATE_EVTCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
7	NOGATE_RWU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6	NOGATE_RWU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
5	NOGATE_RWU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
4	NOGATE_RWU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
3	NOGATE_TRU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
2	NOGATE_TRU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
1	NOGATE_TRU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
0	NOGATE_TRU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

14.8.1.2.25 BCDMA_GCFG_DBGADDR Register

1 BCDMA_GCFG_DBGADDR Register (Offset = 78h) [reset = 0h]

This register provides a writable address which allows debug information to be read from the Debug Data Register

Return to Summary Table

Table 14-25274. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0178h**

Figure 14-8386. BCDMA_GCFG_DBGADDR Name Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W							
0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W							
0h							

Table 14-25276. BCDMA_GCFG_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from Reset Source: rst_mod_g_rst_n
7:0	DBG_ADDR	R/W	0h	Selects offset within unit to access seperate debug registers Reset Source: rst_mod_g_rst_n

14.8.1.2.26 BCDMA_GCFG_DBGDATA Register

1 BCDMA_GCFG_DBGDATA Register (Offset = 7Ch) [reset = 0h]

This register provides read only debug data

Return to Summary Table

Table 14-25277. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 017Ch**

Figure 14-8387. BCDMA_GCFG_DBGDATA Name Register

31	30	29	28	27	26	25	24
DBG_DATA							
R/NA							
0h							
23	22	21	20	19	18	17	16
DBG_DATA							
R/NA							
0h							
15	14	13	12	11	10	9	8
DBG_DATA							
R/NA							
0h							
7	6	5	4	3	2	1	0
DBG_DATA							
R/NA							
0h							

Table 14-25279. BCDMA_GCFG_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBG_DATA	R/NA	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register Reset Source: rst_mod_g_rst_n

14.8.1.2.27 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register (Offset = 40h + formula) [reset = 0h]

The Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 40h + (j * 100h); where j = 0 to 81d

Table 14-25280. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0040h + formula**

Figure 14-8388. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-25282. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Ring base address (LSBs) Reset Source: rst_mod_g_rst_n

14.8.1.2.28 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register (Offset = 44h + formula) [reset = 0h]

The Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 44h + (j * 100h); where j = 0 to 81d

Table 14-25283. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0044h + formula**

Figure 14-8389. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ASEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADDR_HI			
NONE				R/W			
0h				0h			

Table 14-25285. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	ASEL	R/W	0h	Ring base address select Reset Source: rst_mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3:0	ADDR_HI	R/W	0h	Ring base address (MSBs) Reset Source: rst_mod_g_rst_n

14.8.1.2.29 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register

1 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register (Offset = 48h + formula) [reset = 21000000h]

The Ring Size Register contains the element count for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 48h + (j * 100h); where j = 0 to 81d

Table 14-25286. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0048h + formula**

Figure 14-8390. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE			RESERVED		RING_ELSIZE		
R/NA			NONE		R/NA		
1h			0h		1h		
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE							
R/W							
0h							

Table 14-25288. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	QMODE	R/NA	1h	Defines the mode for this ring or queue. Reset Source: rst_mod_g_rst_n `1 exposed ring mode with dual queues (forward/reverse) for SW direct access`
28:27	RESERVED	NONE	0h	Reserved
26:24	RING_ELSIZE	R/NA	1h	Reset Source: rst_mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. Reset Source: rst_mod_g_rst_n

14.8.1.2.30 BCDMA_RXCRT_CHAN_CTL_j Register

1 BCDMA_RXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 27d

Table 14-25289. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0000h + formula**

Figure 14-8391. BCDMA_RXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
RX_ENABLE	RX_TEARDOWN	RX_PAUSE	RX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						RX_STARVATION	RX_ERROR
NONE						R	R
0h						0h	0h

Table 14-25291. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit shoudl be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate tha the channel teardown is complete. If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit. Reset Source: rst_mod_g_rst_n
30	RX_TEARDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n

Table 14-25291. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28	RX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:2	RESERVED	NONE	0h	Reserved
1	RX_STARVATION	R	0h	Rx starvation. This bit is set if the port receives a packet and the ring is empty. The bit clears when the doorbell is written with a positive value. Reset Source: rst_mod_g_rst_n
0	RX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled. Reset Source: rst_mod_g_rst_n

14.8.1.2.31 BCDMA_RXCRT_CHAN_SWTRIG_j Register

1 BCDMA_RXCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = 8h + (j * 1000h); where j = 0 to 27d

Table 14-25292. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0008h + formula**

Figure 14-8392. BCDMA_RXCRT_CHAN_SWTRIG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TRIGGER</td></tr>
<tr><td colspan="7">NONE</td><td>NA/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-25294. BCDMA_RXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.8.1.2.32 BCDMA_RXCRT_CHAN_STATUS0_j Register

1 BCDMA_RXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 40h + (j * 1000h); where j = 0 to 27d

Table 14-25295. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0040h + formula

Figure 14-8393. BCDMA_RXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25297. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-25297. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.8.1.2.33 BCDMA_RXCRT_CHAN_STATUS1_j Register

1 BCDMA_RXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 44h + (j * 1000h); where j = 0 to 27d

Table 14-25298. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0044h + formula**

Figure 14-8394. BCDMA_RXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-25300. BCDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Channel is trying to send data Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has active transactions Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-25300. BCDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.8.1.2.34 BCDMA_RXCRT_CHAN_STDATA_j_k Register

1 BCDMA_RXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = 80h + (j * 1000h) + (k * 4h); where j = 0 to 27d, k = 0 to 31d

Table 14-25301. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0080h + formula**

Figure 14-8395. BCDMA_RXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-25303. BCDMA_RXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.8.1.2.35 BCDMA_RXCRT_CHAN_PEER0_j Register

1 BCDMA_RXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = 200h + (j * 1000h); where j = 0 to 27d

Table 14-25304. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0200h + formula

Figure 14-8396. BCDMA_RXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25306. BCDMA_RXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.36 BCDMA_RXCRT_CHAN_PEER1_j Register

1 BCDMA_RXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = 204h + (j * 1000h); where j = 0 to 27d

Table 14-25307. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0204h + formula

Figure 14-8397. BCDMA_RXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25309. BCDMA_RXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.37 BCDMA_RXCRT_CHAN_PEER2_j Register

1 BCDMA_RXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = 208h + (j * 1000h); where j = 0 to 27d

Table 14-25310. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0208h + formula**

Figure 14-8398. BCDMA_RXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25312. BCDMA_RXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.38 BCDMA_RXCRT_CHAN_PEER3_j Register

1 BCDMA_RXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = 20Ch + (j * 1000h); where j = 0 to 27d

Table 14-25313. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 020Ch + formula**

Figure 14-8399. BCDMA_RXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25315. BCDMA_RXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.39 BCDMA_RXCRT_CHAN_PEER4_j Register

1 BCDMA_RXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = 210h + (j * 1000h); where j = 0 to 27d

Table 14-25316. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0210h + formula**

Figure 14-8400. BCDMA_RXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25318. BCDMA_RXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.40 BCDMA_RXCRT_CHAN_PEER5_j Register

1 BCDMA_RXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = 214h + (j * 1000h); where j = 0 to 27d

Table 14-25319. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0214h + formula**

Figure 14-8401. BCDMA_RXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25321. BCDMA_RXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.41 BCDMA_RXCRT_CHAN_PEER6_j Register

1 BCDMA_RXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = 218h + (j * 1000h); where j = 0 to 27d

Table 14-25322. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0218h + formula

Figure 14-8402. BCDMA_RXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25324. BCDMA_RXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.42 BCDMA_RXCRT_CHAN_PEER7_j Register

1 BCDMA_RXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = 21Ch + (j * 1000h); where j = 0 to 27d

Table 14-25325. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 021Ch + formula**

Figure 14-8403. BCDMA_RXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25327. BCDMA_RXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.43 BCDMA_RXCRT_CHAN_PEER8_j Register

1 BCDMA_RXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = 220h + (j * 1000h); where j = 0 to 27d

Table 14-25328. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0220h + formula**

Figure 14-8404. BCDMA_RXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25330. BCDMA_RXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.44 BCDMA_RXCRT_CHAN_PEER9_j Register

1 BCDMA_RXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = 224h + (j * 1000h); where j = 0 to 27d

Table 14-25331. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0224h + formula**

Figure 14-8405. BCDMA_RXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25333. BCDMA_RXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.45 BCDMA_RXCRT_CHAN_PEER10_j Register

1 BCDMA_RXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = 228h + (j * 1000h); where j = 0 to 27d

Table 14-25334. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0228h + formula**

Figure 14-8406. BCDMA_RXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25336. BCDMA_RXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.46 BCDMA_RXCRT_CHAN_PEER11_j Register

1 BCDMA_RXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = 22Ch + (j * 1000h); where j = 0 to 27d

Table 14-25337. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 022Ch + formula

Figure 14-8407. BCDMA_RXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25339. BCDMA_RXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.47 BCDMA_RXCRT_CHAN_PEER12_j Register

1 BCDMA_RXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = 230h + (j * 1000h); where j = 0 to 27d

Table 14-25340. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0230h + formula**

Figure 14-8408. BCDMA_RXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25342. BCDMA_RXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.48 BCDMA_RXCRT_CHAN_PEER13_j Register

1 BCDMA_RXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = 234h + (j * 1000h); where j = 0 to 27d

Table 14-25343. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0234h + formula**

Figure 14-8409. BCDMA_RXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25345. BCDMA_RXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.49 BCDMA_RXCRT_CHAN_PEER14_j Register

1 BCDMA_RXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = 238h + (j * 1000h); where j = 0 to 27d

Table 14-25346. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0238h + formula**

Figure 14-8410. BCDMA_RXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25348. BCDMA_RXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.50 BCDMA_RXCRT_CHAN_PEER15_j Register

1 BCDMA_RXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = 23Ch + (j * 1000h); where j = 0 to 27d

Table 14-25349. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 023Ch + formula**

Figure 14-8411. BCDMA_RXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							

23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							

15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							

7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25351. BCDMA_RXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.51 BCDMA_RXCRT_CHAN_PCNT_j Register

1 BCDMA_RXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 400h + (j * 1000h); where j = 0 to 27d

Table 14-25352. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0400h + formula**

Figure 14-8412. BCDMA_RXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-25354. BCDMA_RXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.52 BCDMA_RXCRT_CHAN_BCNT_j Register

1 BCDMA_RXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 408h + (j * 1000h); where j = 0 to 27d

Table 14-25355. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0408h + formula**

Figure 14-8413. BCDMA_RXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-25357. BCDMA_RXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.53 BCDMA_RXCRT_CHAN_SBCNT_j Register

1 BCDMA_RXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 410h + (j * 1000h); where j = 0 to 27d

Table 14-25358. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0410h + formula**

Figure 14-8414. BCDMA_RXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-25360. BCDMA_RXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.54 BCDMA_TXCRT_CHAN_CTL_j Register

1 BCDMA_TXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 21d

Table 14-25361. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0000h + formula**

Figure 14-8415. BCDMA_TXCRT_CHAN_CTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>TX_ENABLE</td><td>TX_TEARDOWN</td><td>TX_PAUSE</td><td>TX_FORCED_TEARDOWN</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TX_ERROR</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-25363. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-25363. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.8.1.2.55 BCDMA_TXCRT_CHAN_SWTRIG_j Register

1 BCDMA_TXCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = 8h + (j * 1000h); where j = 0 to 21d

Table 14-25364. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0008h + formula**

Figure 14-8416. BCDMA_TXCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-25366. BCDMA_TXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.8.1.2.56 BCDMA_TXCRT_CHAN_STATUS0_j Register

1 BCDMA_TXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 40h + (j * 1000h); where j = 0 to 21d

Table 14-25367. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0040h + formula**

Figure 14-8417. BCDMA_TXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25369. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-25369. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.8.1.2.57 BCDMA_TXCRT_CHAN_STATUS1_j Register

1 BCDMA_TXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 44h + (j * 1000h); where j = 0 to 21d

Table 14-25370. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0044h + formula

Figure 14-8418. BCDMA_TXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TDNULL
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-25372. BCDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	The channel has met the conditions to do teardown Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has outstanding work to do Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-25372. BCDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.8.1.2.58 BCDMA_TXCRT_CHAN_STDATA_j_k Register

1 BCDMA_TXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = 80h + (j * 1000h) + (k * 4h); where j = 0 to 21d, k = 0 to 31d

Table 14-25373. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0080h + formula**

Figure 14-8419. BCDMA_TXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-25375. BCDMA_TXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.8.1.2.59 BCDMA_TXCRT_CHAN_PEER0_j Register

1 BCDMA_TXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = 200h + (j * 1000h); where j = 0 to 21d

Table 14-25376. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0200h + formula**

Figure 14-8420. BCDMA_TXCRT_CHAN_PEER0_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25378. BCDMA_TXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.60 BCDMA_TXCRT_CHAN_PEER1_j Register

1 BCDMA_TXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = 204h + (j * 1000h); where j = 0 to 21d

Table 14-25379. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0204h + formula**

Figure 14-8421. BCDMA_TXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25381. BCDMA_TXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.61 BCDMA_TXCRT_CHAN_PEER2_j Register

1 BCDMA_TXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = 208h + (j * 1000h); where j = 0 to 21d

Table 14-25382. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0208h + formula**

Figure 14-8422. BCDMA_TXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25384. BCDMA_TXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.62 BCDMA_TXCRT_CHAN_PEER3_j Register

1 BCDMA_TXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = 20Ch + (j * 1000h); where j = 0 to 21d

Table 14-25385. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 020Ch + formula**

Figure 14-8423. BCDMA_TXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25387. BCDMA_TXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.63 BCDMA_TXCRT_CHAN_PEER4_j Register

1 BCDMA_TXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = 210h + (j * 1000h); where j = 0 to 21d

Table 14-25388. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0210h + formula**

Figure 14-8424. BCDMA_TXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25390. BCDMA_TXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.64 BCDMA_TXCRT_CHAN_PEER5_j Register

1 BCDMA_TXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = 214h + (j * 1000h); where j = 0 to 21d

Table 14-25391. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0214h + formula**

Figure 14-8425. BCDMA_TXCRT_CHAN_PEER5_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25393. BCDMA_TXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.65 BCDMA_TXCRT_CHAN_PEER6_j Register

1 BCDMA_TXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = 218h + (j * 1000h); where j = 0 to 21d

Table 14-25394. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0218h + formula**

Figure 14-8426. BCDMA_TXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25396. BCDMA_TXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.66 BCDMA_TXCRT_CHAN_PEER7_j Register

1 BCDMA_TXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = 21Ch + (j * 1000h); where j = 0 to 21d

Table 14-25397. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 021Ch + formula**

Figure 14-8427. BCDMA_TXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25399. BCDMA_TXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.67 BCDMA_TXCRT_CHAN_PEER8_j Register

1 BCDMA_TXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = 220h + (j * 1000h); where j = 0 to 21d

Table 14-25400. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0220h + formula**

Figure 14-8428. BCDMA_TXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25402. BCDMA_TXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.68 BCDMA_TXCRT_CHAN_PEER9_j Register

1 BCDMA_TXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = 224h + (j * 1000h); where j = 0 to 21d

Table 14-25403. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0224h + formula

Figure 14-8429. BCDMA_TXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25405. BCDMA_TXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.69 BCDMA_TXCRT_CHAN_PEER10_j Register

1 BCDMA_TXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = 228h + (j * 1000h); where j = 0 to 21d

Table 14-25406. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0228h + formula**

Figure 14-8430. BCDMA_TXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25408. BCDMA_TXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.70 BCDMA_TXCRT_CHAN_PEER11_j Register

1 BCDMA_TXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = 22Ch + (j * 1000h); where j = 0 to 21d

Table 14-25409. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 022Ch + formula**

Figure 14-8431. BCDMA_TXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25411. BCDMA_TXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.71 BCDMA_TXCRT_CHAN_PEER12_j Register

1 BCDMA_TXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = 230h + (j * 1000h); where j = 0 to 21d

Table 14-25412. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0230h + formula**

Figure 14-8432. BCDMA_TXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25414. BCDMA_TXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.72 BCDMA_TXCRT_CHAN_PEER13_j Register

1 BCDMA_TXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = 234h + (j * 1000h); where j = 0 to 21d

Table 14-25415. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0234h + formula**

Figure 14-8433. BCDMA_TXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25417. BCDMA_TXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.73 BCDMA_TXCRT_CHAN_PEER14_j Register

1 BCDMA_TXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = 238h + (j * 1000h); where j = 0 to 21d

Table 14-25418. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0238h + formula**

Figure 14-8434. BCDMA_TXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25420. BCDMA_TXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.74 BCDMA_TXCRT_CHAN_PEER15_j Register

1 BCDMA_TXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = 23Ch + (j * 1000h); where j = 0 to 21d

Table 14-25421. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 023Ch + formula**

Figure 14-8435. BCDMA_TXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-25423. BCDMA_TXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.8.1.2.75 BCDMA_TXCRT_CHAN_PCNT_j Register

1 BCDMA_TXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 400h + (j * 1000h); where j = 0 to 21d

Table 14-25424. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0400h + formula**

Figure 14-8436. BCDMA_TXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-25426. BCDMA_TXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.76 BCDMA_TXCRT_CHAN_BCNT_j Register

1 BCDMA_TXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 408h + (j * 1000h); where j = 0 to 21d

Table 14-25427. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0408h + formula**

Figure 14-8437. BCDMA_TXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-25429. BCDMA_TXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.77 BCDMA_TXCRT_CHAN_SBCNT_j Register

1 BCDMA_TXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 410h + (j * 1000h); where j = 0 to 21d

Table 14-25430. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0410h + formula**

Figure 14-8438. BCDMA_TXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-25432. BCDMA_TXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.78 LCDMA_RINGACC_RINGRT_RING_FDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_FDB_j Register (Offset = 10h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = 10h + (j * 2000h); where j = 0 to 81d

Table 14-25433. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 0010h + formula**

Figure 14-8439. LCDMA_RINGACC_RINGRT_RING_FDB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-25435. LCDMA_RINGACC_RINGRT_RING_FDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.8.1.2.79 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register (Offset = 18h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = 18h + (j * 2000h); where j = 0 to 81d

Table 14-25436. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 0018h + formula**

Figure 14-8440. LCDMA_RINGACC_RINGRT_RING_FOCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							OCC
NONE							R/NA
0h							0h
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-25438. LCDMA_RINGACC_RINGRT_RING_FOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.8.1.2.80 LCDMA_RINGACC_RINGRT_RING_RDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_RDB_j Register (Offset = 1010h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = 1010h + (j * 2000h); where j = 0 to 81d

Table 14-25439. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 1010h + formula**

Figure 14-8441. LCDMA_RINGACC_RINGRT_RING_RDB_j Name Register

31	30	29	28	27	26	25	24
TDOWN_ACK	RESERVED						
NA/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-25441. LCDMA_RINGACC_RINGRT_RING_RDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_ACK	NA/W	0h	This bit is set to 1 to ackowledge (and clear) the tdown_complete bit in the corresponding Ring N Occupancy Register. this bit is only valid on the reverse rings (rings consumed by the Host SW) Reset Source: rst_mod_g_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.8.1.2.81 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register (Offset = 1018h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = 1018h + (j * 2000h); where j = 0 to 81d

Table 14-25442. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 1018h + formula**

Figure 14-8442. LCDMA_RINGACC_RINGRT_RING_ROCC_j Name Register

31	30	29	28	27	26	25	24
TDOWN_COMPLETE	RESERVED						
R/NA	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							OCC
NONE							R/NA
0h							0h
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-25444. LCDMA_RINGACC_RINGRT_RING_ROCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_COMPLETE	R/NA	0h	This bit when set indicates that a teardown is complete on the channel. This bit is cleared anytime the tdown_ack bit is written as a 1 in the corresponding Ring N Doorbell Register. This bit is only valid on the reverse rings (rings consumed by the Host SW). Reset Source: rst_mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.8.1.2.82 BCDMA_BCRT_CHAN_CTL_j Register

1 BCDMA_BCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 31d

Table 14-25445. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0000h + formula**

Figure 14-8443. BCDMA_BCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	TX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R
0h							0h

Table 14-25447. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-25447. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.8.1.2.83 BCDMA_BCRT_CHAN_SWTRIG_j Register

1 BCDMA_BCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = 8h + (j * 1000h); where j = 0 to 31d

Table 14-25448. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0008h + formula**

Figure 14-8444. BCDMA_BCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-25450. BCDMA_BCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.8.1.2.84 BCDMA_BCRT_CHAN_STATUS0_j Register

1 BCDMA_BCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 40h + (j * 1000h); where j = 0 to 31d

Table 14-25451. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0040h + formula**

Figure 14-8445. BCDMA_BCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-25453. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-25453. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.8.1.2.85 BCDMA_BCRT_CHAN_STATUS1_j Register

1 BCDMA_BCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 44h + (j * 1000h); where j = 0 to 31d

Table 14-25454. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0044h + formula**

Figure 14-8446. BCDMA_BCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TDNULL
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-25456. BCDMA_BCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	Channel is trying to teardown and has met conditions Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule a transaction Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel is active Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-25456. BCDMA_BCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.8.1.2.86 BCDMA_BCRT_CHAN_STATUS2_j Register

1 BCDMA_BCRT_CHAN_STATUS2_j Register (Offset = 48h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 48h + (j * 1000h); where j = 0 to 31d

Table 14-25457. Instance Table

Instance Name	**Physical Address**
DMASS0_BCDMA_0	**4C00 0048h + formula**

Figure 14-8447. BCDMA_BCRT_CHAN_STATUS2_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-25459. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-25459. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.8.1.2.87 BCDMA_BCRT_CHAN_STATUS3_j Register

1 BCDMA_BCRT_CHAN_STATUS3_j Register (Offset = 4Ch + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = 4Ch + (j * 1000h); where j = 0 to 31d

Table 14-25460. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 004Ch + formula**

Figure 14-8448. BCDMA_BCRT_CHAN_STATUS3_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-25462. BCDMA_BCRT_CHAN_STATUS3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Reserved Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Reserved Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	Reserved Reset Source: rst_mod_g_rst_n

Table 14-25462. BCDMA_BCRT_CHAN_STATUS3_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.8.1.2.88 BCDMA_BCRT_CHAN_STDATA_j_k Register

1 BCDMA_BCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = 80h + (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 31d

Table 14-25463. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0080h + formula**

Figure 14-8449. BCDMA_BCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-25465. BCDMA_BCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.8.1.2.89 BCDMA_BCRT_CHAN_STDATAW_j_k Register

1 BCDMA_BCRT_CHAN_STDATAW_j_k Register (Offset = 100h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = 100h + (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 31d

Table 14-25466. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0100h + formula**

Figure 14-8450. BCDMA_BCRT_CHAN_STDATAW_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-25468. BCDMA_BCRT_CHAN_STDATAW_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.8.1.2.90 BCDMA_BCRT_CHAN_PCNT_j Register

1 BCDMA_BCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 400h + (j * 1000h); where j = 0 to 31d

Table 14-25469. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0400h + formula**

Figure 14-8451. BCDMA_BCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-25471. BCDMA_BCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.91 BCDMA_BCRT_CHAN_BCNT_j Register

1 BCDMA_BCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 408h + (j * 1000h); where j = 0 to 31d

Table 14-25472. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0408h + formula**

Figure 14-8452. BCDMA_BCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-25474. BCDMA_BCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.1.2.92 BCDMA_BCRT_CHAN_SBCNT_j Register

1 BCDMA_BCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = 410h + (j * 1000h); where j = 0 to 31d

Table 14-25475. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0410h + formula**

Figure 14-8453. BCDMA_BCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-25477. BCDMA_BCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.8.2 DMASS_ECC_AGGR_0

DMASS_ECC_AGGR_0

14.8.2.1 DMASS_ECC_AGGR_0 Summaries

DMASS_ECC_AGGR_0 Summaries

Table 14-25478. ECC_AGGR Registers, Base Address=3F00 5000h, Length=1024

Offset	Length	Register Name	DMASS0_ECC_AGGR_0 Physical Address
0h	32	ECC_AGGR_REV	3F00 5000h
8h	32	ECC_AGGR_VECTOR	3F00 5008h
Ch	32	ECC_AGGR_STAT	3F00 500Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 5010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 503Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 5040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 5080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 50C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 513Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 5140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 5180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 51C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 5200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 5204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 5208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 520Ch

14.8.2.2 DMASS_ECC_AGGR_0 Registers

DMASS_ECC_AGGR_0 Registers

14.8.2.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

Return to Summary Table

Table 14-25479. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5000h**

Figure 14-8454. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-25481. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.8.2.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-25482. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5008h**

Figure 14-8455. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25484. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.8.2.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Ch]

Misc Status

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Table 14-25485. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 500Ch**

Figure 14-8456. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1Ch</td></tr>
</table>

Table 14-25487. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Ch	Indicates the number of RAMS serviced by the ECC aggregator

14.8.2.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-25488. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5010h + formula**

Figure 14-8457. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-25490. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.8.2.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-25491. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 503Ch**

Figure 14-8458. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25493. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.8.2.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-25494. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5040h**

Figure 14-8459. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25496. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend

Table 14-25496. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.8.2.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-25497. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5080h**

Figure 14-8460. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25499. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-25499. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.8.2.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-25500. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 50C0h**

Figure 14-8461. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25502. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-25502. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.8.2.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-25503. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 513Ch**

Figure 14-8462. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25505. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.8.2.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-25506. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5140h**

Figure 14-8463. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25508. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend

Table 14-25508. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.8.2.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-25509. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5180h**

Figure 14-8464. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25511. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-25511. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.8.2.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-25512. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 51C0h**

Figure 14-8465. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25514. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-25514. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.8.2.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-25515. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5200h**

Figure 14-8466. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-25517. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.8.2.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-25518. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5204h**

Figure 14-8467. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-25520. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.8.2.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-25521. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5208h**

Figure 14-8468. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-25523. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.8.2.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-25524. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 520Ch**

Figure 14-8469. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-25526. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.8.3 DMASS_INTAGGR_0

DMASS_INTAGGR_0

14.8.3.1 DMASS_INTAGGR_0 Summaries

DMASS_INTAGGR_0 Summaries

Table 14-25527. INTAGGR_INTR Registers, Base Address=4800 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_INTR_VINT_ENABLE_SET_J	4800 0000h + formula
8h	64	INTAGGR_INTR_VINT_ENABLE_CLEAR_J	4800 0008h + formula
10h	64	INTAGGR_INTR_VINT_STATUS_SET_J	4800 0010h + formula
18h	64	INTAGGR_INTR_VINT_STATUS_CLEAR_J	4800 0018h + formula
20h	64	INTAGGR_INTR_VINT_STATUSM_J	4800 0020h + formula

Table 14-25528. INTAGGR_IMAP Registers, Base Address=4810 0000h, Length=16384

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_IMAP_GEVI_IMAP_J	4810 0000h + formula

Table 14-25529. INTAGGR_CFG Registers, Base Address=4811 0000h, Length=32

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_CFG_REVISION	4811 0000h
8h	64	INTAGGR_CFG_INTCAP	4811 0008h
10h	64	INTAGGR_CFG_AUXCAP	4811 0010h

Table 14-25530. INTAGGR_L2G Registers, Base Address=4812 0000h, Length=1024

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_L2G_LEVI_MAP_J	4812 0000h + formula

Table 14-25531. INTAGGR_UNMAP Registers, Base Address=4818 0000h, Length=131072

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_UNMAP_UNMAP0_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP1_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP2_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP3_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP4_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP5_MAP	4818 0000h
0h	64	INTAGGR_UNMAP_UNMAP6_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP7_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP8_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP9_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP10_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP11_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP12_MAP_J	4818 0000h + formula
0h	64	INTAGGR_UNMAP_UNMAP13_MAP_J	4818 0000h + formula

Table 14-25531. INTAGGR_UNMAP Registers, Base Address=4818 0000h, Length=131072 (continued)

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_UNMAP_UNMAP14_MAP_J	4818 0000h + formula

Table 14-25532. INTAGGR_MCAST Registers, Base Address=4821 0000h, Length=4096

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_MCAST_GEVI_MCMAP_J	4821 0000h + formula

Table 14-25533. INTAGGR_GCNTCFG Registers, Base Address=4822 0000h, Length=8192

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_GCNTCFG_GEVI_MAP_J	4822 0000h + formula

Table 14-25534. INTAGGR_GCNTRTI Registers, Base Address=4A00 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_GCNTRTI_GEVI_COUNT_J	4A00 0000h + formula

14.8.3.2 DMASS_INTAGGR_0 Registers

DMASS_INTAGGR_0 Registers

14.8.3.2.1 INTAGGR_INTR_VINT_ENABLE_SET_j Register

1 INTAGGR_INTR_VINT_ENABLE_SET_j Register (Offset = 0h + formula) [reset = 0h]

The Interrupt Enable Set register is written by software to enable (i.e. unmask) specified bits to allow their current status to be considered in the generation of the corresponding level sensitive virtual interrupt output.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 183d

Table 14-25535. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4800 0000h + formula**

Figure 14-8470. INTAGGR_INTR_VINT_ENABLE_SET_j Name Register

63	62	61	60	59	58	57	48
INTR_ENABLE							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TS							
0h							

Table 14-25537. INTAGGR_INTR_VINT_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TS	0h	Interrupt enable set value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be set. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.8.3.2.2 INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register

1 INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register (Offset = 8h + formula) [reset = 0h]

The Interrupt Enable Clear register is written by software to disable (i.e. mask) specified bits to disallow their current status from be considered in the generation of the corresponding level sensitive virtual interrupt output.

Return to Summary Table

Offset = 8h + (j * 1000h); where j = 0 to 183d

Table 14-25538. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4800 0008h + formula**

Figure 14-8471. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Name Register

63	62	61	60	59	58	57	48
INTR_ENABLE							
R/W1TC							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TC							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TC							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TC							
0h							

Table 14-25540. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TC	0h	Interrupt enable clear value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be cleared. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.8.3.2.3 INTAGGR_INTR_VINT_STATUS_SET_j Register

1 INTAGGR_INTR_VINT_STATUS_SET_j Register (Offset = 10h + formula) [reset = 0h]

The Interrupt Status register is read by software to determine the cause of an interrupt.

Return to Summary Table

Offset = 10h + (j * 1000h); where j = 0 to 183d

Table 14-25541. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4800 0010h + formula**

Figure 14-8472. INTAGGR_INTR_VINT_STATUS_SET_j Name Register

63	62	61	60	59	58	57	48
INTR_STATUS							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_STATUS							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_STATUS							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_STATUS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_STATUS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_STATUS							
R/W1TS							
0h							

Table 14-25543. INTAGGR_INTR_VINT_STATUS_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TS	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be set Reset Source: srst_n

14.8.3.2.4 INTAGGR_INTR_VINT_STATUS_CLEAR_j Register

1 INTAGGR_INTR_VINT_STATUS_CLEAR_j Register (Offset = 18h + formula) [reset = 0h]

The Interrupt Status register is read by software to determine the cause of an interrupt.

Return to Summary Table

Offset = 18h + (j * 1000h); where j = 0 to 183d

Table 14-25544. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4800 0018h + formula**

Figure 14-8473. INTAGGR_INTR_VINT_STATUS_CLEAR_j Name Register

63	62	61	60	59	58	57	48
INTR_STATUS							
R/W1TC							
0h							
55	54	53	52	51	50	49	48
INTR_STATUS							
R/W1TC							
0h							
47	46	45	44	43	42	41	40
INTR_STATUS							
R/W1TC							
0h							
39	38	37	36	35	34	33	32
INTR_STATUS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
INTR_STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
INTR_STATUS							
R/W1TC							
0h							

Table 14-25546. INTAGGR_INTR_VINT_STATUS_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TC	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be cleared Reset Source: srst_n

14.8.3.2.5 INTAGGR_INTR_VINT_STATUSM_j Register

1 INTAGGR_INTR_VINT_STATUSM_j Register (Offset = 20h + formula) [reset = 0h]

The Interrupt Masked Status register can be read by software to determine the cause of an interrupt.

Return to Summary Table

Offset = 20h + (j * 1000h); where j = 0 to 183d

Table 14-25547. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4800 0020h + formula**

Figure 14-8474. INTAGGR_INTR_VINT_STATUSM_j Name Register

63	62	61	60	59	58	57	48
INTR_STATUSM							
R/NA							
0h							
55	54	53	52	51	50	49	48
INTR_STATUSM							
R/NA							
0h							
47	46	45	44	43	42	41	40
INTR_STATUSM							
R/NA							
0h							
39	38	37	36	35	34	33	32
INTR_STATUSM							
R/NA							
0h							
15	14	13	12	11	10	9	8
INTR_STATUSM							
R/NA							
0h							
7	6	5	4	3	2	1	0
INTR_STATUSM							
R/NA							
0h							

Table 14-25549. INTAGGR_INTR_VINT_STATUSM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUSM	R/NA	0h	Masked state of bits in internal interrupt status register. This value is the result of bitwise ANDing the interrupt enable and status registers Reset Source: srst_n

14.8.3.2.6 INTAGGR_IMAP_GEVI_IMAP_j Register

1 INTAGGR_IMAP_GEVI_IMAP_j Register (Offset = 0h + formula) [reset = 0h]

The Interrupt Mapping Register controls which of N virtual interrupt source outputs this channels physical interrupt sources will map onto.

Return to Summary Table

Offset = 0h + (j * 8h); where j = 0 to 1535d

Table 14-25550. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4810 0000h + formula**

Figure 14-8475. INTAGGR_IMAP_GEVI_IMAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
REGNUM							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		BITNUM					
NONE		R/W					
0h		0h					

Table 14-25552. INTAGGR_IMAP_GEVI_IMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:17	RESERVED	NONE	0h	Reserved
16:8	REGNUM	R/W	0h	Virtual interrupt status register number: this field specifies which of the potential virtual interrupt cause registers the event pending bit will appear in. Reset Source: srst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-25552. INTAGGR_IMAP_GEVI_IMAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BITNUM	R/W	0h	Virtual interrupt cause register bit number: this field specifies which of the 64 bits in the specified virtual interrupt cause register the event pending bit will appear in. Reset Source: srst_n

14.8.3.2.7 INTAGGR_CFG_REVISION Register

1 INTAGGR_CFG_REVISION Register (Offset = 0h) [reset = 66961101h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25553. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4811 0000h**

Figure 14-8476. INTAGGR_CFG_REVISION Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-25555. INTAGGR_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:16	MODID	R	6696h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	2h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n

Table 14-25555. INTAGGR_CFG_REVISION Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.8.3.2.8 INTAGGR_CFG_INTCAP Register

1 INTAGGR_CFG_INTCAP Register (Offset = 8h) [reset = B80600h]

The IntCap Register contains information on virtual interrupts.

Return to Summary Table

Table 14-25556. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4811 0008h**

Figure 14-8477. INTAGGR_CFG_INTCAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SEVT_CNT							
R							
600h							
7	6	5	4	3	2	1	0
SEVT_CNT							
R							
600h							

Table 14-25558. INTAGGR_CFG_INTCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:16	VINTR_CNT	R	B8h	Virtual interrupt register/pin count Reset Source: srst_n
15:0	SEVT_CNT	R	600h	Number of 'event to virt int' mapping registers Reset Source: srst_n

14.8.3.2.9 INTAGGR_CFG_AUXCAP Register

1 INTAGGR_CFG_AUXCAP Register (Offset = 10h) [reset = 301C0080001FFFDCh]

The AuxCap Register contains information on additional capabilities.

Return to Summary Table

Table 14-25559. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4811 0010h**

Figure 14-8478. INTAGGR_CFG_AUXCAP Name Register

63	62	61	60	59	58	57	48
UNMAP_CNT							
R							
301Ch							
55	54	53	52	51	50	49	48
UNMAP_CNT							
R							
301Ch							
47	46	45	44	43	42	41	40
MEVI_CNT							
R							
80h							
39	38	37	36	35	34	33	32
MEVI_CNT							
R							
80h							
15	14	13	12	11	10	9	8
GEVI_CNT							
R							
100h							
7	6	5	4	3	2	1	0
GEVI_CNT							
R							
100h							

Table 14-25561. INTAGGR_CFG_AUXCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	UNMAP_CNT	R	301Ch	Number of multicast event registers. Not all registers in the range are necessarily valid. Reset Source: srst_n
47:32	MEVI_CNT	R	80h	Number of multicast event registers Reset Source: srst_n
31:16	LEVI_CNT	R	20h	Local input events for local to global translation Reset Source: srst_n
15:0	GEVI_CNT	R	100h	Number of event counting registers Reset Source: srst_n

14.8.3.2.10 INTAGGR_L2G_LEVI_MAP_j Register

1 INTAGGR_L2G_LEVI_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

This register determines how the ordinal local event is translated to a global event on the outgoing event transport lane. Both pulse and rising edge local event types are supported. With pulsed events, the event count is determined by the number of cycles for which the event signal remains high. For rising edge events, the count represents the total number of rising edge transitions. The index field of the register determines the outgoing global event index, and the mode bit specifies either pulsed or rising edge local event detection.

Return to Summary Table

Offset = 0h + (j * 20h); where j = 0 to 31d

Table 14-25562. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4812 0000h + formula**

Figure 14-8479. INTAGGR_L2G_LEVI_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GEVIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GEVIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-25564. INTAGGR_L2G_LEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	MODE	R/W	0h	Local event detection mode. This field is set to 0 for pulsed events, and to 1 for rising edge eventss Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved

Table 14-25564. INTAGGR_L2G_LEVI_MAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.11 INTAGGR_UNMAP_UNMAP0_MAP_j Register

1 INTAGGR_UNMAP_UNMAP0_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 8000h + (j * 8h); where j = 0 to 28d

Table 14-25565. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8480. INTAGGR_UNMAP_UNMAP0_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25567. INTAGGR_UNMAP_UNMAP0_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.12 INTAGGR_UNMAP_UNMAP1_MAP_j Register

1 INTAGGR_UNMAP_UNMAP1_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 9000h + (j * 8h); where j = 0 to 98d

Table 14-25568. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8481. INTAGGR_UNMAP_UNMAP1_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25570. INTAGGR_UNMAP_UNMAP1_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.13 INTAGGR_UNMAP_UNMAP2_MAP_j Register

1 INTAGGR_UNMAP_UNMAP2_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = A000h + (j * 8h); where j = 0 to 23d

Table 14-25571. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8482. INTAGGR_UNMAP_UNMAP2_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25573. INTAGGR_UNMAP_UNMAP2_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.14 INTAGGR_UNMAP_UNMAP3_MAP_j Register

1 INTAGGR_UNMAP_UNMAP3_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = B000h + (j * 8h); where j = 0 to 50d

Table 14-25574. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8483. INTAGGR_UNMAP_UNMAP3_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25576. INTAGGR_UNMAP_UNMAP3_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.15 INTAGGR_UNMAP_UNMAP4_MAP_j Register

1 INTAGGR_UNMAP_UNMAP4_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = C000h + (j * 8h); where j = 0 to 50d

Table 14-25577. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8484. INTAGGR_UNMAP_UNMAP4_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25579. INTAGGR_UNMAP_UNMAP4_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.16 INTAGGR_UNMAP_UNMAP5_MAP Register

1 INTAGGR_UNMAP_UNMAP5_MAP Register (Offset = 0h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-25580. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h**

Figure 14-8485. INTAGGR_UNMAP_UNMAP5_MAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25582. INTAGGR_UNMAP_UNMAP5_MAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.17 INTAGGR_UNMAP_UNMAP6_MAP_j Register

1 INTAGGR_UNMAP_UNMAP6_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 10000h + (j * 8h); where j = 0 to 31d

Table 14-25583. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8486. INTAGGR_UNMAP_UNMAP6_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25585. INTAGGR_UNMAP_UNMAP6_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.18 INTAGGR_UNMAP_UNMAP7_MAP_j Register

1 INTAGGR_UNMAP_UNMAP7_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 11000h + (j * 8h); where j = 0 to 31d

Table 14-25586. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8487. INTAGGR_UNMAP_UNMAP7_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25588. INTAGGR_UNMAP_UNMAP7_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.19 INTAGGR_UNMAP_UNMAP8_MAP_j Register

1 INTAGGR_UNMAP_UNMAP8_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 12000h + (j * 8h); where j = 0 to 31d

Table 14-25589. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8488. INTAGGR_UNMAP_UNMAP8_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25591. INTAGGR_UNMAP_UNMAP8_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.20 INTAGGR_UNMAP_UNMAP9_MAP_j Register

1 INTAGGR_UNMAP_UNMAP9_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 13000h + (j * 8h); where j = 0 to 21d

Table 14-25592. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8489. INTAGGR_UNMAP_UNMAP9_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-25594. INTAGGR_UNMAP_UNMAP9_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.21 INTAGGR_UNMAP_UNMAP10_MAP_j Register

1 INTAGGR_UNMAP_UNMAP10_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 14000h + (j * 8h); where j = 0 to 21d

Table 14-25595. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8490. INTAGGR_UNMAP_UNMAP10_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25597. INTAGGR_UNMAP_UNMAP10_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.22 INTAGGR_UNMAP_UNMAP11_MAP_j Register

1 INTAGGR_UNMAP_UNMAP11_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 15000h + (j * 8h); where j = 0 to 21d

Table 14-25598. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8491. INTAGGR_UNMAP_UNMAP11_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25600. INTAGGR_UNMAP_UNMAP11_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.23 INTAGGR_UNMAP_UNMAP12_MAP_j Register

1 INTAGGR_UNMAP_UNMAP12_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 16000h + (j * 8h); where j = 0 to 27d

Table 14-25601. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8492. INTAGGR_UNMAP_UNMAP12_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-25603. INTAGGR_UNMAP_UNMAP12_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.24 INTAGGR_UNMAP_UNMAP13_MAP_j Register

1 INTAGGR_UNMAP_UNMAP13_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 17000h + (j * 8h); where j = 0 to 27d

Table 14-25604. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8493. INTAGGR_UNMAP_UNMAP13_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25606. INTAGGR_UNMAP_UNMAP13_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.25 INTAGGR_UNMAP_UNMAP14_MAP_j Register

1 INTAGGR_UNMAP_UNMAP14_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 18000h + (j * 8h); where j = 0 to 27d

Table 14-25607. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4818 0000h + formula**

Figure 14-8494. INTAGGR_UNMAP_UNMAP14_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-25609. INTAGGR_UNMAP_UNMAP14_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.26 INTAGGR_MCAST_GEVI_MCMAP_j Register

1 INTAGGR_MCAST_GEVI_MCMAP_j Register (Offset = 0h + formula) [reset = FFFF0000FFFFh]

This register determines how ingress global events from the ingress global event ETL are written out to the two egress global event ETL intefaces. The index of each of the two egress events is stored in this register, which is selected based in the ingress event index value.

Return to Summary Table

Offset = 0h + (j * 20h); where j = 0 to 127d

Table 14-25610. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4821 0000h + formula**

Figure 14-8495. INTAGGR_MCAST_GEVI_MCMAP_j Name Register

63	62	61	60	59	58	57	48
IRQMODE1	RESERVED						
R/W	NONE						
0h	0h						
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
GEVIDX1							
R/W							
FFFFh							
39	38	37	36	35	34	33	32
GEVIDX1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
GEVIDX0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX0							
R/W							
FFFFh							

Table 14-25612. INTAGGR_MCAST_GEVI_MCMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63	IRQMODE1	R/W	0h	IRQ Mode Flag 1. When set, this register act like a mapper with bitnum in 37:32 and regnum in 46:38. Reset Source: srst_n
62:48	RESERVED	NONE	0h	Reserved
47:32	GEVIDX1	R/W	FFFFh	Global event index 1. This field specifies the index of the outgoing global event on ETL 1. Set to 0xFFFF to disable. Reset Source: srst_n

Table 14-25612. INTAGGR_MCAST_GEVI_MCMAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31	IRQMODE0	R/W	0h	IRQ Mode Flag 0. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX0	R/W	FFFFh	Global event index 0. This field specifies the index of the outgoing global event on ETL 0. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.27 INTAGGR_GCNTCFG_GEVI_MAP_j Register

1 INTAGGR_GCNTCFG_GEVI_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this event count. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Offset = 0h + (j * 20h); where j = 0 to 255d

Table 14-25613. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4822 0000h + formula**

Figure 14-8496. INTAGGR_GCNTCFG_GEVI_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
GEVIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX							
R/W							
FFFFh							

Table 14-25615. INTAGGR_GCNTCFG_GEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.8.3.2.28 INTAGGR_GCNTRTI_GEVI_COUNT_j Register

1 INTAGGR_GCNTRTI_GEVI_COUNT_j Register (Offset = 0h + formula) [reset = 0h]

The ETL Count register is read by software to determine how many times the event message has been received. This register can be written to decrement the count by a specified amount to acknowledge that a count has been processed by the host.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 255d

Table 14-25616. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	**4A00 0000h + formula**

Figure 14-8497. INTAGGR_GCNTRTI_GEVI_COUNT_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/WTD							
0h							

Table 14-25618. INTAGGR_GCNTRTI_GEVI_COUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:0	CCNT	R/WTD	0h	Current count. This field is incremented by the event count for each message received with this event on the Counted ETL Interface. On write, this field will be decremented by the value written. Writing a value greater than the current count is illegal. Reset Source: srst_n

14.8.4 DMASS_PSILCFG_0

DMASS_PSILCFG_0

14.8.4.1 DMASS_PSILCFG_0 Summaries

DMASS_PSILCFG_0 Summaries

Table 14-25619. PSILCFG Registers, Base Address=4813 0000h, Length=512

Offset	Length	Register Name	DMASS0_PSILCFG_0 Physical Address
0h	32	PSILCFG_REVISION	4813 0000h
10h	32	PSILCFG_PSIL_TO	4813 0010h
100h	32	PSILCFG_CMDA	4813 0100h
104h	32	PSILCFG_CMDB	4813 0104h
108h	32	PSILCFG_WDATA	4813 0108h
140h	32	PSILCFG_RDATA	4813 0140h

14.8.4.2 DMASS_PSILCFG_0 Registers

DMASS_PSILCFG_0 Registers

14.8.4.2.1 PSILCFG_REVISION Register

1 PSILCFG_REVISION Register (Offset = 0h) [reset = 66C00100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25620. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0000h**

Figure 14-8498. PSILCFG_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">66C0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">66C0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-25622. PSILCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	66C0h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: srst_n

14.8.4.2.2 PSILCFG_PSIL_TO Register

1 PSILCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

Return to Summary Table

Table 14-25623. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0010h**

Figure 14-8499. PSILCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-25625. PSILCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access. Once set, this bit is persistent until manually cleared Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: srst_n

14.8.4.2.3 PSILCFG_CMDA Register

1 PSILCFG_CMDA Register (Offset = 100h) [reset = 0h]

The Command Register A contains the busy indicator, direction, and thread number for the configuration transaction.

Return to Summary Table

Table 14-25626. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0100h**

Figure 14-8500. PSILCFG_CMDA Name Register

31	30	29	28	27	26	25	24
PROXY_BUSY	PROXY_DIR	PROXY_TOUT	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PROXY_THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_THREAD_ID							
R/W							
0h							

Table 14-25628. PSILCFG_CMDA Register Field Descriptions

Bit	Field	Type	Reset	Description

31	PROXY_BUSY	R/W	0h	Indication that a configuration read or write is in progress
				Reset Source: srst_n
				`0 No transaction is in progress`
				`1 Transaction is in progress`

30	PROXY_DIR	R/W	0h	Direction of configuration transaction
				Reset Source: srst_n
				`0 Write transaction`
				`1 Read transaction`

29	PROXY_TOUT	R/W	0h	Indication that a timeout occurred. This bit should be written to 0 on each new transaction.
				Reset Source: srst_n
				`0 Transaction completed normally`
				`1 Timeout occurred`

28:16	RESERVED	NONE	0h	Reserved
15:0	PROXY_THREAD_ID	R/W	0h	Thread ID to which configuration read or write is being sent Reset Source: srst_n

14.8.4.2.4 PSILCFG_CMDB Register

1 PSILCFG_CMDB Register (Offset = 104h) [reset = 0h]

The Command Register B contains the byte enables and word address for the configuration transaction.

Return to Summary Table

Table 14-25629. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0104h**

Figure 14-8501. PSILCFG_CMDB Name Register

31	30	29	28	27	26	25	24
PROXY_BYTEN				RESERVED			
R/W				NONE			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PROXY_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_ADDRESS							
R/W							
0h							

Table 14-25631. PSILCFG_CMDB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PROXY_BYTEN	R/W	0h	Byte enables to use for configuration read or write Reset Source: srst_n
27:16	RESERVED	NONE	0h	Reserved
15:0	PROXY_ADDRESS	R/W	0h	Word (32-bit) address within thread configuration space for transaction Reset Source: srst_n 0 `Peer thread ID register. Implemented for src threads only.` 1 `Peer credit register. Implemented for src threads only.` 2 `Enable register` 64 `Capabilities register` 1024 `Static TR register`

14.8.4.2.5 PSILCFG_WDATA Register

1 PSILCFG_WDATA Register (Offset = 108h) [reset = 0h]

The Write Data Register contains the data which is to be written during the configuration transaction.

Return to Summary Table

Table 14-25632. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0108h**

Figure 14-8502. PSILCFG_WDATA Name Register

31	30	29	28	27	26	25	24
PROXY_WDATA							
R/W							
0h							

23	22	21	20	19	18	17	16
PROXY_WDATA							
R/W							
0h							

15	14	13	12	11	10	9	8
PROXY_WDATA							
R/W							
0h							

7	6	5	4	3	2	1	0
PROXY_WDATA							
R/W							
0h							

Table 14-25634. PSILCFG_WDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_WDATA	R/W	0h	Configuration data word to be written Reset Source: srst_n

14.8.4.2.6 PSILCFG_RDATA Register

1 PSILCFG_RDATA Register (Offset = 140h) [reset = 0h]

The Read Data Register contains the data which which was read back during the configuration transaction.

Return to Summary Table

Table 14-25635. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0140h**

Figure 14-8503. PSILCFG_RDATA Name Register

31	30	29	28	27	26	25	24
PROXY_RDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PROXY_RDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PROXY_RDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_RDATA							
R/W							
0h							

Table 14-25637. PSILCFG_RDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_RDATA	R/W	0h	Configuration data word that was read Reset Source: srst_n

14.8.5 DMASS_PSILSS_0

DMASS_PSILSS_0

14.8.5.1 DMASS_PSILSS_0 Summaries

DMASS_PSILSS_0 Summaries

Table 14-25638. PSILSS Registers, Base Address=4814 0000h, Length=4096

Offset	Length	Register Name	DMASS0_PSILSS_0 Physical Address
0h	32	PSILSS_PID	4814 0000h
4h	32	PSILSS_CONFIG	4814 0004h
10h	32	PSILSS_EVENT	4814 0010h
20h	32	PSILSS_LINK	4814 0020h
40h	32	PSILSS_DOWN	4814 0040h

Table 14-25639. PSILSS Registers, Base Address=4823 0000h, Length=4096

Offset	Length	Register Name	DMASS0_PSILSS_0 Physical Address
0h	32	PSILSS_PID	4823 0000h
4h	32	PSILSS_CONFIG	4823 0004h
10h	32	PSILSS_EVENT	4823 0010h
20h	32	PSILSS_LINK	4823 0020h
40h	32	PSILSS_DOWN	4823 0040h

14.8.5.2 DMASS_PSILSS_0 Registers

DMASS_PSILSS_0 Registers

14.8.5.2.1 PSILSS_PID Register

1 PSILSS_PID Register (Offset = 0h) [reset = 66C4C100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25640. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4823 0000h

Figure 14-8504. PSILSS_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		6C4h			
23	22	21	20	19	18	17	16
FUNC							
R							
6C4h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
18h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-25642. PSILSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	6C4h	Module ID Reset Source: rst_mod_g_rst_n
15:11	RTL	R	18h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.8.5.2.2 PSILSS_CONFIG Register

1 PSILSS_CONFIG Register (Offset = 4h) [reset = 3h]

The Config Register shows configured params.

Return to Summary Table

Table 14-25643. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0004h**

Figure 14-8505. PSILSS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ENDPOINTS							
R							
3h							
7	6	5	4	3	2	1	0
ENDPOINTS							
R							
3h							

Table 14-25645. PSILSS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ENDPOINTS	R	3h	Number of endpoints supported. Reset Source: rst_mod_g_rst_n

14.8.5.2.3 PSILSS_EVENT Register

1 PSILSS_EVENT Register (Offset = 10h) [reset = FFFFh]

The Event Register defines the event to produce for a link down event.

Return to Summary Table

Table 14-25646. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0010h**

Figure 14-8506. PSILSS_EVENT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-25648. PSILSS_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	The event to produce. Reset Source: rst_mod_g_rst_n

14.8.5.2.4 PSILSS_LINK Register

1 PSILSS_LINK Register (Offset = 20h) [reset = 0h]

The Link Register shows the current status of the endpoint links.

Return to Summary Table

Table 14-25649. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0020h**

Figure 14-8507. PSILSS_LINK Name Register

31	30	29	28	27	26	25	24
STATUS							
R							
X							
23	22	21	20	19	18	17	16
STATUS							
R							
X							
15	14	13	12	11	10	9	8
STATUS							
R							
X							
7	6	5	4	3	2	1	0
STATUS							
R							
X							

Table 14-25651. PSILSS_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R	X	The status of the endpoint links. Reset Source: rst_mod_g_rst_n

14.8.5.2.5 PSILSS_DOWN Register

1 PSILSS_DOWN Register (Offset = 40h) [reset = 0h]

The Link Down Register shows which links are down for the endpoints.

Return to Summary Table

Table 14-25652. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0040h**

Figure 14-8508. PSILSS_DOWN Name Register

31	30	29	28	27	26	25	24
STATUS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STATUS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STATUS							
R/W1TC							
0h							

Table 14-25654. PSILSS_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R/W1TC	0h	The down status of the endpoint links. Reset Source: rst_mod_g_rst_n

14.8.5.2.6 PSILSS_PID Register

1 PSILSS_PID Register (Offset = 0h) [reset = 66C4C100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25655. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0000h**

Figure 14-8509. PSILSS_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		6C4h			
23	22	21	20	19	18	17	16
FUNC							
R							
6C4h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
18h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-25657. PSILSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	6C4h	Module ID Reset Source: rst_mod_g_rst_n
15:11	RTL	R	18h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.8.5.2.7 PSILSS_CONFIG Register

1 PSILSS_CONFIG Register (Offset = 4h) [reset = 3h]

The Config Register shows configured params.

Return to Summary Table

Table 14-25658. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0004h**

Figure 14-8510. PSILSS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ENDPOINTS							
R							
3h							
7	6	5	4	3	2	1	0
ENDPOINTS							
R							
3h							

Table 14-25660. PSILSS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ENDPOINTS	R	3h	Number of endpoints supported. Reset Source: rst_mod_g_rst_n

14.8.5.2.8 PSILSS_EVENT Register

1 PSILSS_EVENT Register (Offset = 10h) [reset = FFFFh]

The Event Register defines the event to produce for a link down event.

Return to Summary Table

Table 14-25661. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0010h**

Figure 14-8511. PSILSS_EVENT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
EVT							
R/W							
FFFFh							

Table 14-25663. PSILSS_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	The event to produce. Reset Source: rst_mod_g_rst_n

14.8.5.2.9 PSILSS_LINK Register

1 PSILSS_LINK Register (Offset = 20h) [reset = 0h]

The Link Register shows the current status of the endpoint links.

Return to Summary Table

Table 14-25664. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0020h**

Figure 14-8512. PSILSS_LINK Name Register

31	30	29	28	27	26	25	24
STATUS							
R							
X							
23	22	21	20	19	18	17	16
STATUS							
R							
X							
15	14	13	12	11	10	9	8
STATUS							
R							
X							
7	6	5	4	3	2	1	0
STATUS							
R							
X							

Table 14-25666. PSILSS_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R	X	The status of the endpoint links. Reset Source: rst_mod_g_rst_n

14.8.5.2.10 PSILSS_DOWN Register

1 PSILSS_DOWN Register (Offset = 40h) [reset = 0h]

The Link Down Register shows which links are down for the endpoints.

Return to Summary Table

Table 14-25667. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	**4823 0040h**

Figure 14-8513. PSILSS_DOWN Name Register

31	30	29	28	27	26	25	24
STATUS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STATUS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STATUS							
R/W1TC							
0h							

Table 14-25669. PSILSS_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R/W1TC	0h	The down status of the endpoint links. Reset Source: rst_mod_g_rst_n

14.8.6 DMASS_RINGACC_0

DMASS_RINGACC_0

14.8.6.1 DMASS_RINGACC_0 Summaries

DMASS_RINGACC_0 Summaries

Table 14-25670. RINGACC_GCFG Registers, Base Address=4824 0000h, Length=1024

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
0h	32	RINGACC_GCFG_REVISION	4824 0000h
10h	32	RINGACC_GCFG_TRACE_CTL	4824 0010h
20h	32	RINGACC_GCFG_OVRFLOW	4824 0020h
40h	32	RINGACC_GCFG_ERROR_EVT	4824 0040h
44h	32	RINGACC_GCFG_ERROR_LOG	4824 0044h

Table 14-25671. RINGACC_RT Registers, Base Address=4900 0000h, Length=4194304

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
10h	32	RINGACC_RT_RINGRT_DB_J	4900 0010h + formula
18h	32	RINGACC_RT_RINGRT_OCC_J	4900 0018h + formula
1Ch	32	RINGACC_RT_RINGRT_INDX_J	4900 001Ch + formula
20h	32	RINGACC_RT_RINGRT_HWOCC_J	4900 0020h + formula
24h	32	RINGACC_RT_RINGRT_HWINDX_J	4900 0024h + formula

Table 14-25672. RINGACC_CFG Registers, Base Address=4980 0000h, Length=262144

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
40h	32	RINGACC_CFG_RING_BA_LO_J	4980 0040h + formula
44h	32	RINGACC_CFG_RING_BA_HI_J	4980 0044h + formula
48h	32	RINGACC_CFG_RING_SIZE_J	4980 0048h + formula
4Ch	32	RINGACC_CFG_RING_EVENT_J	4980 004Ch + formula
50h	32	RINGACC_CFG_RING_ORDERID_J	4980 0050h + formula

14.8.6.2 DMASS_RINGACC_0 Registers

DMASS_RINGACC_0 Registers

14.8.6.2.1 RINGACC_GCFG_REVISION Register

1 RINGACC_GCFG_REVISION Register (Offset = 0h) [reset = 663C0101h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25673. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0000h**

Figure 14-8514. RINGACC_GCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
663Ch							
23	22	21	20	19	18	17	16
MODID							
R							
663Ch							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-25675. RINGACC_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	663Ch	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.8.6.2.2 RINGACC_GCFG_TRACE_CTL Register

1 RINGACC_GCFG_TRACE_CTL Register (Offset = 10h) [reset = 0h]

Trace Control Register

Return to Summary Table

Table 14-25676. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0010h**

Figure 14-8515. RINGACC_GCFG_TRACE_CTL Name Register

31	30	29	28	27	26	25	24
EN	ALL_QUEUES	MSG	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-25678. RINGACC_GCFG_TRACE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Trace enable 0 = disable 1 = enable. Reset Source: srst_n
30	ALL_QUEUES	R/W	0h	Trace everything 0 = only the selected queue 1 = every queue. Reset Source: srst_n
29	MSG	R/W	0h	Trace message data 0 = include only the operation 1 = include message data. Reset Source: srst_n
28:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue number when tracing a single queue. Reset Source: srst_n

14.8.6.2.3 RINGACC_GCFG_OVRFLOW Register

1 RINGACC_GCFG_OVRFLOW Register (Offset = 20h) [reset = 0h]

Overflow Queue Register

Return to Summary Table

Table 14-25679. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0020h**

Figure 14-8516. RINGACC_GCFG_OVRFLOW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QUEUE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUEUE							
R/W							
0h							

Table 14-25681. RINGACC_GCFG_OVRFLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue to send overflow messages. A value of 0xffff will disable the overflow function. Reset Source: srst_n

14.8.6.2.4 RINGACC_GCFG_ERROR_EVT Register

1 RINGACC_GCFG_ERROR_EVT Register (Offset = 40h) [reset = FFFFh]

The Error Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote detection of a ring memory transaction bus error.

Return to Summary Table

Table 14-25682. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0040h**

Figure 14-8517. RINGACC_GCFG_ERROR_EVT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-25684. RINGACC_GCFG_ERROR_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Event to send when detecting a bus error. Reset Source: srst_n

14.8.6.2.5 RINGACC_GCFG_ERROR_LOG Register

1 RINGACC_GCFG_ERROR_LOG Register (Offset = 44h) [reset = 0h]

Error Log Register. A read of this register will clear the pending error log event and allow a new error to be captured. It does not clear the contents of this register which are only valid while the error event is pending.

Return to Summary Table

Table 14-25685. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0044h**

Figure 14-8518. RINGACC_GCFG_ERROR_LOG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PUSH</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QUEUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QUEUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25687. RINGACC_GCFG_ERROR_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PUSH	R	0h	Bus error was caused by a push. 0 = pop. 1 = push. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R	0h	Queue that received the bus error. Reset Source: srst_n

14.8.6.2.6 RINGACC_RT_RINGRT_DB_j Register

1 RINGACC_RT_RINGRT_DB_j Register (Offset = 10h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = 10h + (j * 1000h); where j = 0 to 19d

Table 14-25688. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0010h + formula**

Figure 14-8519. RINGACC_RT_RINGRT_DB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-25690. RINGACC_RT_RINGRT_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: srst_n

14.8.6.2.7 RINGACC_RT_RINGRT_OCC_j Register

1 RINGACC_RT_RINGRT_OCC_j Register (Offset = 18h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = 18h + (j * 1000h); where j = 0 to 19d

Table 14-25691. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0018h + formula**

Figure 14-8520. RINGACC_RT_RINGRT_OCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			OCC				
NONE			R/NA				
0h			0h				
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-25693. RINGACC_RT_RINGRT_OCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.8.6.2.8 RINGACC_RT_RINGRT_INDX_j Register

1 RINGACC_RT_RINGRT_INDX_j Register (Offset = 1Ch + formula) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current SW read index for the Ring for the channel.

Return to Summary Table

Offset = 1Ch + (j * 1000h); where j = 0 to 19d

Table 14-25694. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 001Ch + formula**

Figure 14-8521. RINGACC_RT_RINGRT_INDX_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INDX			
NONE				R/NA			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDX							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INDX							
R/NA							
0h							

Table 14-25696. RINGACC_RT_RINGRT_INDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current SW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by SW each time SW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.8.6.2.9 RINGACC_RT_RINGRT_HWOCC_j Register

1 RINGACC_RT_RINGRT_HWOCC_j Register (Offset = 20h + formula) [reset = 0h]

The Ring N Hardware Occupancy Register contains the early increment/decrement version of the the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = 20h + (j * 1000h); where j = 0 to 19d

Table 14-25697. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0020h + formula**

Figure 14-8522. RINGACC_RT_RINGRT_HWOCC_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">OCC</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/NA</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25699. RINGACC_RT_RINGRT_HWOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.8.6.2.10 RINGACC_RT_RINGRT_HWINDX_j Register

1 RINGACC_RT_RINGRT_HWINDX_j Register (Offset = 24h + formula) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current HW read index for the Ring for the channel.

Return to Summary Table

Offset = 24h + (j * 1000h); where j = 0 to 19d

Table 14-25700. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0024h + formula**

Figure 14-8523. RINGACC_RT_RINGRT_HWINDX_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INDX			
NONE				R/NA			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDX							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INDX							
R/NA							
0h							

Table 14-25702. RINGACC_RT_RINGRT_HWINDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current HW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by HW each time HW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.8.6.2.11 RINGACC_CFG_RING_BA_LO_j Register

1 RINGACC_CFG_RING_BA_LO_j Register (Offset = 40h + formula) [reset = 0h]

The Tx Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 40h + (j * 100h); where j = 0 to 19d

Table 14-25703. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0040h + formula**

Figure 14-8524. RINGACC_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-25705. RINGACC_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Tx Ring base address (LSBs) Reset Source: srst_n

14.8.6.2.12 RINGACC_CFG_RING_BA_HI_j Register

1 RINGACC_CFG_RING_BA_HI_j Register (Offset = 44h + formula) [reset = 0h]

The Tx Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 44h + (j * 100h); where j = 0 to 19d

Table 14-25706. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0044h + formula**

Figure 14-8525. RINGACC_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_HI							
R/W							
0h							

Table 14-25708. RINGACC_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_HI	R/W	0h	Tx Ring base address (MSBs) Reset Source: srst_n

14.8.6.2.13 RINGACC_CFG_RING_SIZE_j Register

1 RINGACC_CFG_RING_SIZE_j Register (Offset = 48h + formula) [reset = 0h]

The Tx Ring Size Register contains the element size and element counts for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = 48h + (j * 100h); where j = 0 to 19d

Table 14-25709. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0048h + formula**

Figure 14-8526. RINGACC_CFG_RING_SIZE_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">QMODE</td><td colspan="3">RESERVED</td><td colspan="3">ELSIZE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">SIZE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25711. RINGACC_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	QMODE	R/W	0h	Defines the mode for this ring or queue. Reset Source: srst_n 0 exposed ring mode for SW direct access 1 messaging mode when all operations are through bus accesses, allowing multiple producers or consumers. 2 credentials mode is message mode plus stores credentials with each message, requiring the ring size to be doubled to fit the credentials along with the same number of elements when using the first 2 modes. Any exposed memory should be protected by a firewall from unwanted access.
29:27	RESERVED	NONE	0h	Reserved
26:24	ELSIZE	R/W	0h	Ring element size. This field is encoded as follows: 0 = 4 bytes 1 = 8 bytes 2 = 16 bytes 3 = 32 bytes 4 = 64 bytes 5 = 128 bytes 6 = 256 bytes 7 = RESERVED Reset Source: srst_n
23:20	RESERVED	NONE	0h	Reserved

Table 14-25711. RINGACC_CFG_RING_SIZE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. For rings in CREDENTIALS or QM modes the size must be an even number. Reset Source: srst_n

14.8.6.2.14 RINGACC_CFG_RING_EVENT_j Register

1 RINGACC_CFG_RING_EVENT_j Register (Offset = 4Ch + formula) [reset = FFFFh]

The Ring Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote the occurrence of an up event [empty to not-empty] or a down event [non-empty to empty] for this ring.

Return to Summary Table

Offset = 4Ch + (j * 100h); where j = 0 to 19d

Table 14-25712. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 004Ch + formula**

Figure 14-8527. RINGACC_CFG_RING_EVENT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EVT							
R/W							
FFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVT							
R/W							
FFFFh							

Table 14-25714. RINGACC_CFG_RING_EVENT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Defines the event for this ring or queue. Reset Source: srst_n

14.8.6.2.15 RINGACC_CFG_RING_ORDERID_j Register

1 RINGACC_CFG_RING_ORDERID_j Register (Offset = 50h + formula) [reset = 0h]

The Ring OrderID Register contains the bus orderid value for the ring memory access.

Return to Summary Table

Offset = 50h + (j * 100h); where j = 0 to 19d

Table 14-25715. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0050h + formula**

Figure 14-8528. RINGACC_CFG_RING_ORDERID_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
NONE			R/W	R/W			
0h			0h	0h			

Table 14-25717. RINGACC_CFG_RING_ORDERID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for this ring or queue with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction. Reset Source: srst_n
3:0	ORDERID	R/W	0h	Defines the bus orderid value for this ring or queue. Reset Source: srst_n

14.8.7 DMASS_SEC_PROXY_0

DMASS_SEC_PROXY_0

14.8.7.1 DMASS_SEC_PROXY_0 Summaries

DMASS_SEC_PROXY_0 Summaries

Table 14-25718. SEC_PROXY Registers, Base Address=4825 0000h, Length=256

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_PID	4825 0000h
4h	32	SEC_PROXY_CONFIG	4825 0004h
14h	32	SEC_PROXY_GLB_EVT	4825 0014h

Table 14-25719. SEC_PROXY_SCFG Registers, Base Address=4A40 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_SCFG_BUFFER_L	4A40 0000h
4h	32	SEC_PROXY_SCFG_BUFFER_H	4A40 0004h
8h	32	SEC_PROXY_SCFG_TARGET_L	4A40 0008h
Ch	32	SEC_PROXY_SCFG_TARGET_H	4A40 000Ch
10h	32	SEC_PROXY_SCFG_ORDERID	4A40 0010h
0h	32	SEC_PROXY_SCFG_THREAD_CTL_J	4A40 0000h + formula
4h	32	SEC_PROXY_SCFG_THREAD_EVT_MAP_J	4A40 0004h + formula
8h	32	SEC_PROXY_SCFG_THREAD_DST_J	4A40 0008h + formula

Table 14-25720. SEC_PROXY_RT Registers, Base Address=4A60 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_RT_THREAD_STATUS_J	4A60 0000h + formula
4h	32	SEC_PROXY_RT_THREAD_THR_J	4A60 0004h + formula

Table 14-25721. PROXY_TARGET Registers, Base Address=4D00 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	PROXY_TARGET_THREAD_DATA_J	4D00 0000h + formula
4h	32	PROXY_TARGET_THREAD_MESSAGE_J_K	4D00 0004h + formula

14.8.7.2 DMASS_SEC_PROXY_0 Registers

DMASS_SEC_PROXY_0 Registers

14.8.7.2.1 SEC_PROXY_PID Register

1 SEC_PROXY_PID Register (Offset = 0h) [reset = 66367100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-25722. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	4825 0000h

Figure 14-8529. SEC_PROXY_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		636h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
636h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Eh					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-25724. SEC_PROXY_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	636h	Module ID Reset Source: rst_mod_g_rst_n
15:11	RTL	R	Eh	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.8.7.2.2 SEC_PROXY_CONFIG Register

1 SEC_PROXY_CONFIG Register (Offset = 4h) [reset = 40004Ch]

The Config Register shows configured params.

Return to Summary Table

Table 14-25725. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4825 0004h**

Figure 14-8530. SEC_PROXY_CONFIG Name Register

31	30	29	28	27	26	25	24
MSG_SIZE							
R							
40h							
23	22	21	20	19	18	17	16
MSG_SIZE							
R							
40h							
15	14	13	12	11	10	9	8
THREADS							
R							
4Ch							
7	6	5	4	3	2	1	0
THREADS							
R							
4Ch							

Table 14-25727. SEC_PROXY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MSG_SIZE	R	40h	Supported message size in bytes. Reset Source: rst_mod_g_rst_n
15:0	THREADS	R	4Ch	Number of proxy threads supported. Reset Source: rst_mod_g_rst_n

14.8.7.2.3 SEC_PROXY_GLB_EVT Register

1 SEC_PROXY_GLB_EVT Register (Offset = 14h) [reset = FFFFh]

The Global Event Register defines the event to send for a global error.

Return to Summary Table

Table 14-25728. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4825 0014h**

Figure 14-8531. SEC_PROXY_GLB_EVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ERR_EVENT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ERR_EVENT							
R/W							
FFFFh							

Table 14-25730. SEC_PROXY_GLB_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ERR_EVENT	R/W	FFFFh	Global error event destination. 0xFFFF disables the event Reset Source: rst_mod_g_rst_n

14.8.7.2.4 SEC_PROXY_SCFG_BUFFER_L Register

1 SEC_PROXY_SCFG_BUFFER_L Register (Offset = 0h) [reset = 0h]

The Buffer Register defines the pointer for the external buffer.

Return to Summary Table

Table 14-25731. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0000h**

Figure 14-8532. SEC_PROXY_SCFG_BUFFER_L Name Register

31	30	29	28	27	26	25	24
BASE_L							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE_L							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE_L							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_L							
R/W							
0h							

Table 14-25733. SEC_PROXY_SCFG_BUFFER_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE_L	R/W	0h	The base address for the external buffer, lower 32 bits. Reset Source: rst_mod_g_rst_n

14.8.7.2.5 SEC_PROXY_SCFG_BUFFER_H Register

1 SEC_PROXY_SCFG_BUFFER_H Register (Offset = 4h) [reset = 0h]

The Buffer Register defines the pointer for the external buffer.

Return to Summary Table

Table 14-25734. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0004h**

Figure 14-8533. SEC_PROXY_SCFG_BUFFER_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BASE_H							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_H							
R/W							
0h							

Table 14-25736. SEC_PROXY_SCFG_BUFFER_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BASE_H	R/W	0h	The base address for the external buffer, upper 16 bits. Reset Source: rst_mod_g_rst_n

14.8.7.2.6 SEC_PROXY_SCFG_TARGET_L Register

1 SEC_PROXY_SCFG_TARGET_L Register (Offset = 8h) [reset = 400000h]

The Target Register defines the pointer for the external target.

Return to Summary Table

Table 14-25737. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0008h**

Figure 14-8534. SEC_PROXY_SCFG_TARGET_L Name Register

31	30	29	28	27	26	25	24
BASE_L							
R/W							
400000h							
23	22	21	20	19	18	17	16
BASE_L							
R/W							
400000h							
15	14	13	12	11	10	9	8
BASE_L							
R/W							
400000h							
7	6	5	4	3	2	1	0
BASE_L							
R/W							
400000h							

Table 14-25739. SEC_PROXY_SCFG_TARGET_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE_L	R/W	400000h	The base address for the external target, lower 32 bits. Reset Source: rst_mod_g_rst_n

14.8.7.2.7 SEC_PROXY_SCFG_TARGET_H Register

1 SEC_PROXY_SCFG_TARGET_H Register (Offset = Ch) [reset = 0h]

The Target Register defines the pointer for the external target.

Return to Summary Table

Table 14-25740. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 000Ch**

Figure 14-8535. SEC_PROXY_SCFG_TARGET_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASE_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BASE_H							
R/W							
0h							

Table 14-25742. SEC_PROXY_SCFG_TARGET_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BASE_H	R/W	0h	The base address for the external target, upper 16 bits. Reset Source: rst_mod_g_rst_n

14.8.7.2.8 SEC_PROXY_SCFG_ORDERID Register

1 SEC_PROXY_SCFG_ORDERID Register (Offset = 10h) [reset = 0h]

The Buffer OrderID Register contains the bus orderid value for the buffer memory access.

Return to Summary Table

Table 14-25743. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0010h**

Figure 14-8536. SEC_PROXY_SCFG_ORDERID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
NONE			R/W	R/W			
0h			0h	0h			

Table 14-25745. SEC_PROXY_SCFG_ORDERID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for the buffer access with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction. Reset Source: rst_mod_g_rst_n
3:0	ORDERID	R/W	0h	Defines the bus orderid value for the buffer access. Reset Source: rst_mod_g_rst_n

14.8.7.2.9 SEC_PROXY_SCFG_THREAD_CTL_j Register

1 SEC_PROXY_SCFG_THREAD_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Control Register defines controls for proxy thread a.

Return to Summary Table

Offset = 1000h + (j * 1000h); where j = 0 to 75d

Table 14-25746. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0000h + formula**

Figure 14-8537. SEC_PROXY_SCFG_THREAD_CTL_j Name Register

31	30	29	28	27	26	25	24
DIR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAX_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-25748. SEC_PROXY_SCFG_THREAD_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIR	R/W	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only. Reset Source: rst_mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	MAX_CNT	R/W	0h	Max message count allowed for an outbound proxy thread. Is not used otherwise. Reset Source: rst_mod_g_rst_n
15:0	QUEUE	R/W	0h	Queue number in the target to use for the proxy thread. If the target base does not start at queue 0 then this is the relative queue number from that base queue. Reset Source: rst_mod_g_rst_n

14.8.7.2.10 SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register

1 SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register (Offset = 4h + formula) [reset = FFFFFFFFh]

The Event Map Register defines the event numbers for proxy thread a.

Return to Summary Table

Offset = 1004h + (j * 1000h); where j = 0 to 75d

Table 14-25749. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0004h + formula**

Figure 14-8538. SEC_PROXY_SCFG_THREAD_EVT_MAP_j Name Register

31	30	29	28	27	26	25	24
ERR_EVT							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
ERR_EVT							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
THR_EVT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
THR_EVT							
R/W							
FFFFh							

Table 14-25751. SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ERR_EVT	R/W	FFFFh	Event number for an error from the proxy thread. Reset Source: rst_mod_g_rst_n
15:0	THR_EVT	R/W	FFFFh	Event number for a threshold event from the proxy thread. Reset Source: rst_mod_g_rst_n

14.8.7.2.11 SEC_PROXY_SCFG_THREAD_DST_j Register

1 SEC_PROXY_SCFG_THREAD_DST_j Register (Offset = 8h + formula) [reset = 0h]

The Destination Register defines the destination proxy thread for outbound proxy thread a.

Return to Summary Table

Offset = 1008h + (j * 1000h); where j = 0 to 75d

Table 14-25752. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0008h + formula**

Figure 14-8539. SEC_PROXY_SCFG_THREAD_DST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD							
R/W							
0h							

Table 14-25754. SEC_PROXY_SCFG_THREAD_DST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD	R/W	0h	The proxy thread that is the destination of messages from this outbound proxy thread, based on the queue numbers. This is ignored for inbound proxy threads. Reset Source: rst_mod_g_rst_n

14.8.7.2.12 SEC_PROXY_RT_THREAD_STATUS_j Register

1 SEC_PROXY_RT_THREAD_STATUS_j Register (Offset = 0h + formula) [reset = 0h]

The Status Register gives status for proxy thread a.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 75d

Table 14-25755. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A60 0000h + formula**

Figure 14-8540. SEC_PROXY_RT_THREAD_STATUS_j Name Register

31	30	29	28	27	26	25	24
ERROR	DIR	RESERVED					
R/W	R	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
MAX_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CUR_CNT							
R							
0h							

Table 14-25757. SEC_PROXY_RT_THREAD_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERROR	R/W	0h	Error detected on proxy thread. The error will also use the err_evt field to generate an error event which can generate an interrupt. While in error a proxy thread will not process any operations. Write a 0 to clear the error and reset the proxy thread. Reset Source: rst_mod_g_rst_n
30	DIR	R	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only. Reset Source: rst_mod_g_rst_n
29:24	RESERVED	NONE	0h	Reserved
23:16	MAX_CNT	R	0h	Max message count allowed for an outbound proxy thread. Reset Source: rst_mod_g_rst_n
15:8	RESERVED	NONE	0h	Reserved

Table 14-25757. SEC_PROXY_RT_THREAD_STATUS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CUR_CNT	R	0h	Current message count for the proxy thread. For an inbound proxy this is the number of available messages. For an outbound proxy this is the number of free messages that can be written. This value will initialize itself to 0 if the THREAD[a]_CTL register is written with dir set to inbound, or to the max_cnt value if the THREAD[a]_CTL register is written with dir set to outbound, as these are the starting values for a newly configured thread. Reset Source: rst_mod_g_rst_n

14.8.7.2.13 SEC_PROXY_RT_THREAD_THR_j Register

1 SEC_PROXY_RT_THREAD_THR_j Register (Offset = 4h + formula) [reset = 0h]

The Threshold Register controls the threshold for proxy thread a events.

Return to Summary Table

Offset = 4h + (j * 1000h); where j = 0 to 75d

Table 14-25758. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A60 0004h + formula**

Figure 14-8541. SEC_PROXY_RT_THREAD_THR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_CNT							
R/W							
0h							

Table 14-25760. SEC_PROXY_RT_THREAD_THR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	THR_CNT	R/W	0h	Threshold count that causes proxy thread events. For an outbound proxy this will be the number of free messages to cause an event. For an inbound proxy this will be the number of available messages to cause an event. Reset Source: rst_mod_g_rst_n

14.8.7.2.14 PROXY_TARGET_THREAD_DATA_j Register

1 PROXY_TARGET_THREAD_DATA_j Register (Offset = 0h + formula) [reset = 0h]

The Proxy Private register contains private information for the proxy thread a and should not be written, writes are ignored. Reads are allowed to know the source thread of the message.

Return to Summary Table

Offset = 0h + (j * 1000h); where j = 0 to 75d

Table 14-25761. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4D00 0000h + formula**

Figure 14-8542. PROXY_TARGET_THREAD_DATA_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						SRC_THR	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SRC_THR							
R							
0h							

Table 14-25763. PROXY_TARGET_THREAD_DATA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	SRC_THR	R	0h	Proxy source thread of message. Reset Source: rst_mod_g_rst_n

14.8.7.2.15 PROXY_TARGET_THREAD_MESSAGE_j_k Register

1 PROXY_TARGET_THREAD_MESSAGE_j_k Register (Offset = 4h + formula) [reset = 0h]

The Message Data for proxy thread a. The word with index b = 14 contains the completion final byte.

Return to Summary Table

Offset = 4h + (j * 1000h) + (k * 4h); where j = 0 to 75d, k = 0 to 14d

Table 14-25764. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4D00 0004h + formula**

Figure 14-8543. PROXY_TARGET_THREAD_MESSAGE_j_k Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-25766. PROXY_TARGET_THREAD_MESSAGE_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Proxy Message Data Reset Source: rst_mod_g_rst_n

14.8.8 PDMA

PDMA

14.8.8.1 PDMA Summaries

PDMA Summaries

Table 14-25767. ECC_AGGR Registers, Base Address=00C0 0000h, Length=1024

Offset	Length	Register Name	PDMA0 Physical Address	PDMA1 Physical Address
0h	32	ECC_AGGR_REV	00C0 0000h	00C0 1000h
8h	32	ECC_AGGR_VECTOR	00C0 0008h	00C0 1008h
Ch	32	ECC_AGGR_STAT	00C0 000Ch	00C0 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00C0 0010h + formula	00C0 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00C0 003Ch	00C0 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00C0 0040h	00C0 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00C0 0080h	00C0 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00C0 00C0h	00C0 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00C0 013Ch	00C0 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00C0 0140h	00C0 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00C0 0180h	00C0 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00C0 01C0h	00C0 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00C0 0200h	00C0 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00C0 0204h	00C0 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00C0 0208h	00C0 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00C0 020Ch	00C0 120Ch

14.8.8.2 PDMA Registers

PDMA Registers

14.8.8.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

Return to Summary Table

Table 14-25768. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0000h**
PDMA1	**00C0 1000h**

Figure 14-8544. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-25770. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.8.8.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-25771. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0008h**
PDMA1	**00C0 1008h**

Figure 14-8545. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-25773. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.8.8.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

Return to Summary Table

Table 14-25774. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 000Ch**
PDMA1	**00C0 100Ch**

Figure 14-8546. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
4h							

Table 14-25776. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.8.8.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-25777. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0010h + formula**
PDMA1	**00C0 1010h + formula**

Figure 14-8547. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-25779. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.8.8.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-25780. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 003Ch**
PDMA1	**00C0 103Ch**

Figure 14-8548. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25782. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.8.8.2.6 *ECC_AGGR_SEC_STATUS_REG0 Register*

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-25783. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0040h**
PDMA1	**00C0 1040h**

Figure 14-8549. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-25785. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.8.8.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-25786. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0080h**
PDMA1	**00C0 1080h**

Figure 14-8550. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-25788. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.8.8.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-25789. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 00C0h**
PDMA1	**00C0 10C0h**

Figure 14-8551. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-25791. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.8.8.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-25792. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 013Ch**
PDMA1	**00C0 113Ch**

Figure 14-8552. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25794. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.8.8.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-25795. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0140h**
PDMA1	**00C0 1140h**

Figure 14-8553. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-25797. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.8.8.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-25798. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0180h**
PDMA1	**00C0 1180h**

Figure 14-8554. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-25800. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.8.8.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-25801. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 01C0h**
PDMA1	**00C0 11C0h**

Figure 14-8555. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-25803. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.8.8.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-25804. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0200h**
PDMA1	**00C0 1200h**

Figure 14-8556. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-25806. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.8.8.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-25807. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0204h**
PDMA1	**00C0 1204h**

Figure 14-8557. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-25809. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.8.8.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-25810. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0208h**
PDMA1	**00C0 1208h**

Figure 14-8558. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-25812. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.8.8.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-25813. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 020Ch**
PDMA1	**00C0 120Ch**

Figure 14-8559. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-25815. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9 Peripherals Registers

14.9.1 Audio Registers

14.9.1.1 MCASP

MCASP

14.9.1.1.1 MCASP Summaries

MCASP Summaries

Table 14-25816. MCASP Registers, Base Address=02B0 0000h, Length=8192

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
0h	32	MCASP_PID	02B0 0000h	02B1 0000h	02B2 0000h
4h	32	MCASP_PWRIDLESYSCONFIG	02B0 0004h	02B1 0004h	02B2 0004h
10h	32	MCASP_PFUNC	02B0 0010h	02B1 0010h	02B2 0010h
14h	32	MCASP_PDIR	02B0 0014h	02B1 0014h	02B2 0014h
18h	32	MCASP_PDOUT	02B0 0018h	02B1 0018h	02B2 0018h
1Ch	32	MCASP_PDIN	02B0 001Ch	02B1 001Ch	02B2 001Ch
20h	32	MCASP_PDCLR	02B0 0020h	02B1 0020h	02B2 0020h
44h	32	MCASP_GBLCTL	02B0 0044h	02B1 0044h	02B2 0044h
48h	32	MCASP_AMUTE	02B0 0048h	02B1 0048h	02B2 0048h
4Ch	32	MCASP_DLBCTL	02B0 004Ch	02B1 004Ch	02B2 004Ch
50h	32	MCASP_DITCTL	02B0 0050h	02B1 0050h	02B2 0050h
60h	32	MCASP_RGBLCTL	02B0 0060h	02B1 0060h	02B2 0060h
64h	32	MCASP_RMASK	02B0 0064h	02B1 0064h	02B2 0064h
68h	32	MCASP_RFMT	02B0 0068h	02B1 0068h	02B2 0068h
6Ch	32	MCASP_AFSRCTL	02B0 006Ch	02B1 006Ch	02B2 006Ch
70h	32	MCASP_ACLKRCTL	02B0 0070h	02B1 0070h	02B2 0070h
74h	32	MCASP_AHCLKRCTL	02B0 0074h	02B1 0074h	02B2 0074h
78h	32	MCASP_RTDM	02B0 0078h	02B1 0078h	02B2 0078h
7Ch	32	MCASP_RINTCTL	02B0 007Ch	02B1 007Ch	02B2 007Ch
80h	32	MCASP_RSTAT	02B0 0080h	02B1 0080h	02B2 0080h
84h	32	MCASP_RSLOT	02B0 0084h	02B1 0084h	02B2 0084h
88h	32	MCASP_RCLKCHK	02B0 0088h	02B1 0088h	02B2 0088h
8Ch	32	MCASP_PIDTCTL	02B0 008Ch	02B1 008Ch	02B2 008Ch
A0h	32	MCASP_XGBLCTL	02B0 00A0h	02B1 00A0h	02B2 00A0h
A4h	32	MCASP_XMASK	02B0 00A4h	02B1 00A4h	02B2 00A4h
A8h	32	MCASP_XFMT	02B0 00A8h	02B1 00A8h	02B2 00A8h
ACh	32	MCASP_AFSXCTL	02B0 00ACh	02B1 00ACh	02B2 00ACh
B0h	32	MCASP_ACLKXCTL	02B0 00B0h	02B1 00B0h	02B2 00B0h
B4h	32	MCASP_AHCLKXCTL	02B0 00B4h	02B1 00B4h	02B2 00B4h
B8h	32	MCASP_XTDM	02B0 00B8h	02B1 00B8h	02B2 00B8h
BCh	32	MCASP_XINTCTL	02B0 00BCh	02B1 00BCh	02B2 00BCh
C0h	32	MCASP_XSTAT	02B0 00C0h	02B1 00C0h	02B2 00C0h
C4h	32	MCASP_XSLOT	02B0 00C4h	02B1 00C4h	02B2 00C4h
C8h	32	MCASP_XCLKCHK	02B0 00C8h	02B1 00C8h	02B2 00C8h
CCh	32	MCASP_XEVTCTL	02B0 00CCh	02B1 00CCh	02B2 00CCh
100h	32	MCASP_DITCSRA0	02B0 0100h	02B1 0100h	02B2 0100h
104h	32	MCASP_DITCSRA1	02B0 0104h	02B1 0104h	02B2 0104h

Table 14-25816. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
108h	32	MCASP_DITCSRA2	02B0 0108h	02B1 0108h	02B2 0108h
10Ch	32	MCASP_DITCSRA3	02B0 010Ch	02B1 010Ch	02B2 010Ch
110h	32	MCASP_DITCSRA4	02B0 0110h	02B1 0110h	02B2 0110h
114h	32	MCASP_DITCSRA5	02B0 0114h	02B1 0114h	02B2 0114h
118h	32	MCASP_DITCSRB0	02B0 0118h	02B1 0118h	02B2 0118h
11Ch	32	MCASP_DITCSRB1	02B0 011Ch	02B1 011Ch	02B2 011Ch
120h	32	MCASP_DITCSRB2	02B0 0120h	02B1 0120h	02B2 0120h
124h	32	MCASP_DITCSRB3	02B0 0124h	02B1 0124h	02B2 0124h
128h	32	MCASP_DITCSRB4	02B0 0128h	02B1 0128h	02B2 0128h
12Ch	32	MCASP_DITCSRB5	02B0 012Ch	02B1 012Ch	02B2 012Ch
130h	32	MCASP_DITUDRA0	02B0 0130h	02B1 0130h	02B2 0130h
134h	32	MCASP_DITUDRA1	02B0 0134h	02B1 0134h	02B2 0134h
138h	32	MCASP_DITUDRA2	02B0 0138h	02B1 0138h	02B2 0138h
13Ch	32	MCASP_DITUDRA3	02B0 013Ch	02B1 013Ch	02B2 013Ch
140h	32	MCASP_DITUDRA4	02B0 0140h	02B1 0140h	02B2 0140h
144h	32	MCASP_DITUDRA5	02B0 0144h	02B1 0144h	02B2 0144h
148h	32	MCASP_DITUDRB0	02B0 0148h	02B1 0148h	02B2 0148h
14Ch	32	MCASP_DITUDRB1	02B0 014Ch	02B1 014Ch	02B2 014Ch
150h	32	MCASP_DITUDRB2	02B0 0150h	02B1 0150h	02B2 0150h
154h	32	MCASP_DITUDRB3	02B0 0154h	02B1 0154h	02B2 0154h
158h	32	MCASP_DITUDRB4	02B0 0158h	02B1 0158h	02B2 0158h
15Ch	32	MCASP_DITUDRB5	02B0 015Ch	02B1 015Ch	02B2 015Ch
180h	32	MCASP_SRCTL0	02B0 0180h	02B1 0180h	02B2 0180h
184h	32	MCASP_SRCTL1	02B0 0184h	02B1 0184h	02B2 0184h
188h	32	MCASP_SRCTL2	02B0 0188h	02B1 0188h	02B2 0188h
18Ch	32	MCASP_SRCTL3	02B0 018Ch	02B1 018Ch	02B2 018Ch
190h	32	MCASP_SRCTL4	02B0 0190h	02B1 0190h	02B2 0190h
194h	32	MCASP_SRCTL5	02B0 0194h	02B1 0194h	02B2 0194h
198h	32	MCASP_SRCTL6	02B0 0198h	02B1 0198h	02B2 0198h
19Ch	32	MCASP_SRCTL7	02B0 019Ch	02B1 019Ch	02B2 019Ch
1A0h	32	MCASP_SRCTL8	02B0 01A0h	02B1 01A0h	02B2 01A0h
1A4h	32	MCASP_SRCTL9	02B0 01A4h	02B1 01A4h	02B2 01A4h
1A8h	32	MCASP_SRCTL10	02B0 01A8h	02B1 01A8h	02B2 01A8h
1ACh	32	MCASP_SRCTL11	02B0 01ACh	02B1 01ACh	02B2 01ACh
1B0h	32	MCASP_SRCTL12	02B0 01B0h	02B1 01B0h	02B2 01B0h
1B4h	32	MCASP_SRCTL13	02B0 01B4h	02B1 01B4h	02B2 01B4h
1B8h	32	MCASP_SRCTL14	02B0 01B8h	02B1 01B8h	02B2 01B8h
1BCh	32	MCASP_SRCTL15	02B0 01BCh	02B1 01BCh	02B2 01BCh
200h	32	MCASP_XBUF0	02B0 0200h	02B1 0200h	02B2 0200h
204h	32	MCASP_XBUF1	02B0 0204h	02B1 0204h	02B2 0204h
208h	32	MCASP_XBUF2	02B0 0208h	02B1 0208h	02B2 0208h
20Ch	32	MCASP_XBUF3	02B0 020Ch	02B1 020Ch	02B2 020Ch
210h	32	MCASP_XBUF4	02B0 0210h	02B1 0210h	02B2 0210h
214h	32	MCASP_XBUF5	02B0 0214h	02B1 0214h	02B2 0214h

Table 14-25816. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
218h	32	MCASP_XBUF6	02B0 0218h	02B1 0218h	02B2 0218h
21Ch	32	MCASP_XBUF7	02B0 021Ch	02B1 021Ch	02B2 021Ch
220h	32	MCASP_XBUF8	02B0 0220h	02B1 0220h	02B2 0220h
224h	32	MCASP_XBUF9	02B0 0224h	02B1 0224h	02B2 0224h
228h	32	MCASP_XBUF10	02B0 0228h	02B1 0228h	02B2 0228h
22Ch	32	MCASP_XBUF11	02B0 022Ch	02B1 022Ch	02B2 022Ch
230h	32	MCASP_XBUF12	02B0 0230h	02B1 0230h	02B2 0230h
234h	32	MCASP_XBUF13	02B0 0234h	02B1 0234h	02B2 0234h
238h	32	MCASP_XBUF14	02B0 0238h	02B1 0238h	02B2 0238h
23Ch	32	MCASP_XBUF15	02B0 023Ch	02B1 023Ch	02B2 023Ch
280h	32	MCASP_RBUF0	02B0 0280h	02B1 0280h	02B2 0280h
284h	32	MCASP_RBUF1	02B0 0284h	02B1 0284h	02B2 0284h
288h	32	MCASP_RBUF2	02B0 0288h	02B1 0288h	02B2 0288h
28Ch	32	MCASP_RBUF3	02B0 028Ch	02B1 028Ch	02B2 028Ch
290h	32	MCASP_RBUF4	02B0 0290h	02B1 0290h	02B2 0290h
294h	32	MCASP_RBUF5	02B0 0294h	02B1 0294h	02B2 0294h
298h	32	MCASP_RBUF6	02B0 0298h	02B1 0298h	02B2 0298h
29Ch	32	MCASP_RBUF7	02B0 029Ch	02B1 029Ch	02B2 029Ch
2A0h	32	MCASP_RBUF8	02B0 02A0h	02B1 02A0h	02B2 02A0h
2A4h	32	MCASP_RBUF9	02B0 02A4h	02B1 02A4h	02B2 02A4h
2A8h	32	MCASP_RBUF10	02B0 02A8h	02B1 02A8h	02B2 02A8h
2ACh	32	MCASP_RBUF11	02B0 02ACh	02B1 02ACh	02B2 02ACh
2B0h	32	MCASP_RBUF12	02B0 02B0h	02B1 02B0h	02B2 02B0h
2B4h	32	MCASP_RBUF13	02B0 02B4h	02B1 02B4h	02B2 02B4h
2B8h	32	MCASP_RBUF14	02B0 02B8h	02B1 02B8h	02B2 02B8h
2BCh	32	MCASP_RBUF15	02B0 02BCh	02B1 02BCh	02B2 02BCh
1000h	32	MCASP_WFIFOCTL	02B0 1000h	02B1 1000h	02B2 1000h
1004h	32	MCASP_WFIFOSTS	02B0 1004h	02B1 1004h	02B2 1004h
1008h	32	MCASP_RFIFOCTL	02B0 1008h	02B1 1008h	02B2 1008h
100Ch	32	MCASP_RFIFOSTS	02B0 100Ch	02B1 100Ch	02B2 100Ch

14.9.1.1.2 MCASP Registers

MCASP Registers

14.9.1.1.2.1 MCASP_PID Register

1 MCASP_PID Register (Offset = 0h) [reset = 44307B02h]

The revision identification register (PID) contains identification data for the peripheral.

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Table 14-25817. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0000h**
MCASP1	**02B1 0000h**
MCASP2	**02B2 0000h**

Figure 14-8560. MCASP_PID Name Register

31	30	29	28	27	26	25	24
REV							
R							
44307B02h							
23	22	21	20	19	18	17	16
REV							
R							
44307B02h							
15	14	13	12	11	10	9	8
REV							
R							
44307B02h							
7	6	5	4	3	2	1	0
REV							
R							
44307B02h							

Table 14-25819. MCASP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REV	R	44307B02h	Identifies revision of peripheral.

14.9.1.1.2.2 MCASP_PWRIDLESYSCONFIG Register

1 MCASP_PWRIDLESYSCONFIG Register (Offset = 4h) [reset = 2h]

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Table 14-25820. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0004h**
MCASP1	**02B1 0004h**
MCASP2	**02B2 0004h**

Figure 14-8561. MCASP_PWRIDLESYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED66</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED66</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED66</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED66</td><td colspan="4">OTHER</td><td colspan="2">IDLEMODE</td></tr>
<tr><td colspan="2">R</td><td colspan="4">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="4">0h</td><td colspan="2">2h</td></tr>
</table>

Table 14-25822. MCASP_PWRIDLESYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED66	R	0h	
5:2	OTHER	R/W	0h	Reserved for future programming.
1:0	IDLEMODE	R/W	2h	Power management Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0 `Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only.` 1 `No-idle mode: local target never enters idle state. Backup mode, for debug only.` 2 `Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events.` 3 `Reserved.`

14.9.1.1.2.3 MCASP_PFUNC Register

1 MCASP_PFUNC Register (Offset = 10h) [reset = 0h]

The pin function register (PFUNC) specifies the function of AXRn, ACLKX, AHCLKX, AFSX, ACLKR, AHCLKR, and AFSR pins as either a McASP pin or a general-purpose input/output (GPIO) pin. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-25823. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0010h**
MCASP1	**02B1 0010h**
MCASP2	**02B2 0010h**

Figure 14-8562. MCASP_PFUNC Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED67
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED67							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED67							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED67				AXR			
R				R/W			
0h				0h			

Table 14-25825. MCASP_PFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines if AFSR pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
30	AHCLKR	R/W	0h	Determines if AHCLKR pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
29	ACLKR	R/W	0h	Determines if ACLKR pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
28	AFSX	R/W	0h	Determines if AFSX pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
27	AHCLKX	R/W	0h	Determines if AHCLKX pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`

Table 14-25825. MCASP_PFUNC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	ACLKX	R/W	0h	Determines if ACLKX pin functions as McASP or GPIO. 0 Pin functions as McASP pin. 1 Pin functions as GPIO pin.
25	AMUTE	R/W	0h	Determines if AMUTE pin functions as McASP or GPIO. 0 Pin functions as McASP pin. 1 Pin functions as GPIO pin.
24:4	RESERVED67	R	0h	
3:0	AXR	R/W	0h	Determines if AXRn pin functions as McASP or GPIO. 0 Pin functions as McASP pin. 1 Pin functions as GPIO pin.

14.9.1.1.2.4 MCASP_PDIR Register

1 MCASP_PDIR Register (Offset = 14h) [reset = 0h]

The pin direction register (PDIR) specifies the direction of AXRn, ACLKX, AHCLKX, AFSX, ACLKR, AHCLKR, and AFSR pins as either an input or an output pin. Regardless of the pin function register (PFUNC) setting, each PDIR bit must be set to 1 for the specified pin to be enabled as an output and each PDIR bit must be cleared to 0 for the specified pin to be an input. For example, if the McASP is configured to use an internally-generated bit clock and the clock is to be driven out to the system, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be set to 1 (an output). When AXRn is configured to transmit, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be set to 1 (an output). Similarly, when AXRn is configured to receive, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be cleared to 0 (an input). CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation. The number of serializers is device/instance specific. See device datasheet for the number of serializers supported by each instance. Invalid bit settings are reserved.

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Table 14-25826. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0014h**
MCASP1	**02B1 0014h**
MCASP2	**02B2 0014h**

Figure 14-8563. MCASP_PDIR Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED68
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED68							
R							
0h							
15	14	13	12	11	10	9	8
AXR							
R/W							
0h							
7	6	5	4	3	2	1	0
AXR							
R/W							
0h							

Table 14-25828. MCASP_PDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines if AFSR pin functions as an input or output. 0 Pin functions as input. 1 Pin functions as output.
30	AHCLKR	R/W	0h	NOTE: AHCLKR, AHCLKX pins are not available on the SOC pinmux directly, but through a clock routing logic that maps the SOC pins (AUDIO_EXT_REFCLK[1:0]) to the McASP clocks. Therefore, GPIO mode control is not functional for these specific pins. 0 Pin functions as input. 1 Pin functions as output.

Table 14-25828. MCASP_PDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	ACLKR	R/W	0h	Determines if ACLKR pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
28	AFSX	R/W	0h	Determines if AFSX pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
27	AHCLKX	R/W	0h	NOTE: AHCLKR, AHCLKX pins are not available on the SOC pinmux directly, but through a clock routing logic that maps the SOC pins (AUDIO_EXT_REFCLK[1:0]) to the McASP clocks. Therefore, GPIO mode control is not functional for these specific pins. 0 `Pin functions as input.` 1 `Pin functions as output.`
26	ACLKX	R/W	0h	Determines if ACLKX pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
25	AMUTE	R/W	0h	Determines if AMUTE pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
24:16	RESERVED68	R	0h	
15:0	AXR	R/W	0h	Determines if AXRn pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`

14.9.1.1.2.5 MCASP_PDOUT Register

1 MCASP_PDOUT Register (Offset = 18h) [reset = 0h]

The pin data output register (PDOUT) holds a value for data out at all times, and may be read back at all times. The value held by PDOUT is not affected by writing to PDIR and PFUNC. However, the data value in PDOUT is driven out onto the McASP pin only if the corresponding bit in PFUNC is set to 1 (GPIO function) and the corresponding bit in PDIR is set to 1 (output). When reading data, returns the corresponding bit value in PDOUT[n], does not return input from I/O pin; when writing data, writes to the corresponding PDOUT[n] bit. PDOUT has these aliases or alternate addresses: PDSET When written to at this address, writing a 1 to a bit in PDSET sets the corresponding bit in PDOUT to 1; writing a 0 has no effect and keeps the bits in PDOUT unchanged. PDCLR When written to at this address, writing a 1 to a bit in PDCLR clears the corresponding bit in PDOUT to 0; writing a 0 has no effect and keeps the bits in PDOUT unchanged. There is only one set of data out bits, PDOUT[31-0]. The other registers, PDSET and PDCLR, are just different addresses for the same control bits, with different behaviors during writes. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-25829. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0018h**
MCASP1	**02B1 0018h**
MCASP2	**02B2 0018h**

Figure 14-8564. MCASP_PDOUT Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED69
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED69							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED69							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED69				AXR			
R				R/W			
0h				0h			

Table 14-25831. MCASP_PDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines drive on AFSR output pin when the corresponding PFUNC[31] and PDIR[31] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
30	AHCLKR	R/W	0h	Determines drive on AHCLKR output pin when the corresponding PFUNC[30] and PDIR[30] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`

Table 14-25831. MCASP_PDOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	ACLKR	R/W	0h	Determines drive on ACLKR output pin when the corresponding PFUNC[29] and PDIR[29] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
28	AFSX	R/W	0h	Determines drive on AFSX output pin when the corresponding PFUNC[28] and PDIR[28] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
27	AHCLKX	R/W	0h	Determines drive on AHCLKX output pin when the corresponding PFUNC[27] and PDIR[27] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
26	ACLKX	R/W	0h	Determines drive on ACLKX output pin when the corresponding PFUNC[26] and PDIR[26] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
25	AMUTE	R/W	0h	Determines drive on AMUTE output pin when the corresponding PFUNC[25] and PDIR[25] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
24:4	RESERVED69	R	0h	
3:0	AXR	R/W	0h	Determines drive on AXR[n] output pin when the corresponding PFUNC[n] and PDIR[n] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`

14.9.1.1.2.6 MCASP_PDIN Register

1 MCASP_PDIN Register (Offset = 1Ch) [reset = 0h]

The pin data input register (PDIN) holds the I/O pin state of each of the McASP pins. PDIN allows the actual value of the pin to be read, regardless of the state of PFUNC and PDIR. The value after reset for registers 1 through 15 and 24 through 31 depends on how the pins are being driven. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-25832. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 001Ch**
MCASP1	**02B1 001Ch**
MCASP2	**02B2 001Ch**

Figure 14-8565. MCASP_PDIN Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED70							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED70							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED70				AXR			
R				R/W			
0h				0h			

Table 14-25834. MCASP_PDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Logic level on AFSR pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
30	AHCLKR	R/W	0h	Logic level on AHCLKR pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
29	ACLKR	R/W	0h	Logic level on ACLKR pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
28	AFSX	R/W	0h	Logic level on AFSX pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
27	AHCLKX	R/W	0h	Logic level on AHCLKX pin. 0 `Pin is logic low.` 1 `Pin is logic high.`

Table 14-25834. MCASP_PDIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	ACLKX	R/W	0h	Logic level on ACLKX pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
25	AMUTE	R/W	0h	Logic level on AMUTE pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
24:4	RESERVED70	R	0h	
3:0	AXR	R/W	0h	Logic level on AXR[n] pin. 0 `Pin is logic low.` 1 `Pin is logic high.`

14.9.1.1.2.7 MCASP_PDCLR Register

1 MCASP_PDCLR Register (Offset = 20h) [reset = 0h]

The pin data clear register (PDCLR) is an alias of the pin data output register (PDOUT) for writes only. Writing a 1 to the PDCLR bit clears the corresponding bit in PDOUT and, if PFUNC = 1 (GPIO function) and PDIR = 1 (output), drives a logic low on the pin. PDCLR is useful for a multitasking system because it allows you to clear to a logic low only the desired pin(s) within a system without affecting other I/O pins controlled by the same McASP. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-25835. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0020h**
MCASP1	**02B1 0020h**
MCASP2	**02B2 0020h**

Figure 14-8566. MCASP_PDCLR Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED71
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED71							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED71							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED71				AXR			
R				R/W			
0h				0h			

Table 14-25837. MCASP_PDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Allows the corresponding AFSR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[31] bit is cleared to 0.`
30	AHCLKR	R/W	0h	Allows the corresponding AHCLKR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[30] bit is cleared to 0.`
29	ACLKR	R/W	0h	Allows the corresponding ACLKR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[29] bit is cleared to 0.`

Table 14-25837. MCASP_PDCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	AFSX	R/W	0h	Allows the corresponding AFSX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[28] bit is cleared to 0.`
27	AHCLKX	R/W	0h	Allows the corresponding AHCLKX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[27] bit is cleared to 0.`
26	ACLKX	R/W	0h	Allows the corresponding ACLKX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[26] bit is cleared to 0.`
25	AMUTE	R/W	0h	Allows the corresponding AMUTE bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[25] bit is cleared to 0.`
24:4	RESERVED71	R	0h	
3:0	AXR	R/W	0h	Allows the corresponding AXR[n] bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[n] bit is cleared to 0.`

14.9.1.1.2.8 MCASP_GBLCTL Register

1 MCASP_GBLCTL Register (Offset = 44h) [reset = 0h]

The global control register (GBLCTL) provides initialization of the transmit and receive sections. The bit fields in GBLCTL are synchronized and latched by the corresponding clocks (ACLKX for bits 12-8 and ACLKR for bits 4-0). Before GBLCTL is programmed, you must ensure that serial clocks are running. If the corresponding external serial clocks, ACLKX and ACLKR, are not yet running, you should select the internal serial clock source in AHCLKXCTL, AHCLKRCTL, ACLKXCTL, and ACLKRCTL before GBLCTL is programmed. Also, after programming any bits in GBLCTL you should not proceed until you have read back from GBLCTL and verified that the bits are latched in GBLCTL.

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Table 14-25838. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0044h**
MCASP1	**02B1 0044h**
MCASP2	**02B2 0044h**

Figure 14-8567. MCASP_GBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED73							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED73							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED73			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED72			RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-25840. MCASP_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED73	R	0h	
12	XFRST	R/W	0h	Transmit frame sync generator reset enable bit. 0 Transmit frame sync generator is reset. 1 Transmit frame sync generator is active. When released from reset, the transmit frame sync generator begins counting serial clocks and generating frame sync as programmed.

Table 14-25840. MCASP_GBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	XSMRST	R/W	0h	Transmit state machine reset enable bit. 0 Transmit state machine is held in reset. AXRn pin state: If PFUNC[n] = 0 and PDIR[n] = 1; then the serializer drives the AXRn pin to the state specified for inactive time slot (as determined by DISMOD bits in SRCTL). 1 Transmit state machine is released from reset. When released from reset, the transmit state machine immediately transfers data from XRBUF[n] to XRSR[n]. The transmit state machine sets the underrun flag (XUNDRN) in XSTAT, if XRBUF[n] have not been preloaded with data before reset is released. The transmit state machine also immediately begins detecting frame sync and is ready to transmit. Transmit TDM time slot begins at slot 0 after reset is released.
10	XSRCLR	R/W	0h	Transmit serializer clear enable bit. By clearing then setting this bit, the transmit buffer is flushed to an empty state [XDATA = 1]. If XSMRST = 1, XSRCLR = 1, XDATA = 1, and XBUF is not loaded with new data before the start of the next active time slot, an underrun will occur. 0 Transmit serializers are cleared. 1 Transmit serializers are active. When the transmit serializers are first taken out of reset (XSRCLR changes from 0 to 1), the transmit data ready bit (XDATA) in XSTAT is set to indicate XBUF is ready to be written.
9	XHCLKRST	R/W	0h	Transmit high-frequency clock divider reset enable bit. 0 Transmit high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1 Transmit high-frequency clock divider is running.
8	XCLKRST	R/W	0h	Transmit clock divider reset enable bit. 0 Transmit clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1 Transmit clock divider is running.
7:5	RESERVED72	R	0h	
4	RFRST	R/W	0h	Receive frame sync generator reset enable bit. 0 Receive frame sync generator is reset. 1 Receive frame sync generator is active. When released from reset, the receive frame sync generator begins counting serial clocks and generating frame sync as programmed.
3	RSMRST	R/W	0h	Receive state machine reset enable bit. 0 Receive state machine is held in reset. 1 Receive state machine is released from reset. When released from reset, the receive state machine immediately begins detecting frame sync and is ready to receive. Receive TDM time slot begins at slot 0 after reset is released.
2	RSRCLR	R/W	0h	Receive serializer clear enable bit. By clearing then setting this bit, the receive buffer is flushed. 0 Receive serializers are cleared. 1 Receive serializers are active.

Table 14-25840. MCASP_GBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RHCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. 0 Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1 Receive high-frequency clock divider is running.
0	RCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. 0 Receive clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1 Receive clock divider is running.

14.9.1.1.2.9 MCASP_AMUTE Register

1 MCASP_AMUTE Register (Offset = 48h) [reset = 0h]

The audio mute control register (AMUTE) controls the McASP audio mute (AMUTE) output pin. The value after reset for register 4 depends on how the pins are being driven.

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Table 14-25841. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0048h**
MCASP1	**02B1 0048h**
MCASP2	**02B2 0048h**

Figure 14-8568. MCASP_AMUTE Name Register

31	30	29	28	27	26	25	24
RESERVED74							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED74							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED74			XDMAERR	RDMAERR	XCKFAIL	RCKFAIL	XSYNCERR
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RSYNCERR	XUNDRN	ROVRN	INSTAT	INEN	INPOL	MUTEN	
R/W	R/W	R/W	R	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-25843. MCASP_AMUTE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED74	R	0h	
12	XDMAERR	R/W	0h	If transmit DMA error [XDMAERR], drive AMUTE active enable bit. 0 `Drive is disabled. Detection of transmit DMA error is ignored by AMUTE.` 1 `Drive is enabled (active). Upon detection of transmit DMA error, AMUTE is active and is driven according to MUTEN bit.`
11	RDMAERR	R/W	0h	If receive DMA error [RDMAERR], drive AMUTE active enable bit. 0 `Drive is disabled. Detection of receive DMA error is ignored by AMUTE.` 1 `Drive is enabled (active). Upon detection of receive DMA error, AMUTE is active and is driven according to MUTEN bit.`
10	XCKFAIL	R/W	0h	If transmit clock failure [XCKFAIL], drive AMUTE active enable bit. 0 `Drive is disabled. Detection of transmit clock failure is ignored by AMUTE.` 1 `Drive is enabled (active). Upon detection of transmit clock failure, AMUTE is active and is driven according to MUTEN bit`

Table 14-25843. MCASP_AMUTE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RCKFAIL	R/W	0h	If receive clock failure [RCKFAIL], drive AMUTE active enable bit. 0 Drive is disabled. Detection of receive clock failure is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of receive clock failure, AMUTE is active and is driven according to MUTEN bit.
8	XSYNCERR	R/W	0h	If unexpected transmit frame sync error [XSYNCERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of unexpected transmit frame sync error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of unexpected transmit frame sync error, AMUTE is active and is driven according to MUTEN bit.
7	RSYNCERR	R/W	0h	If unexpected receive frame sync error [RSYNCERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of unexpected receive frame sync error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of unexpected receive frame sync error, AMUTE is active and is driven according to MUTEN bit.
6	XUNDRN	R/W	0h	If transmit underrun error [XUNDRN], drive AMUTE active enable bit. 0 Drive is disabled. Detection of transmit underrun error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of transmit underrun error, AMUTE is active and is driven according to MUTEN bit.
5	ROVRN	R/W	0h	If receiver overrun error [ROVRN], drive AMUTE active enable bit. 0 Drive is disabled. Detection of receiver overrun error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of receiver overrun error, AMUTE is active and is driven according to MUTEN bit.
4	INSTAT	R	0h	Determines drive on AXRn pin when PFUNC[n] and PDIR[n] bits are set to 1. 0 AMUTEIN pin is inactive. 1 AMUTEIN pin is active. Audio mute in error is detected.
3	INEN	R/W	0h	Drive AMUTE active when AMUTEIN error is active [INSTAT = 1]. 0 Drive is disabled. AMUTEIN is ignored by AMUTE. 1 Drive is enabled (active). INSTAT = 1 drives AMUTE active.
2	INPOL	R/W	0h	Audio mute in [AMUTEIN] polarity select bit. 0 Polarity is active high. A high on AMUTEIN sets INSTAT to 1. 1 Polarity is active low. A low on AM UTEIN sets INSTAT to 1.
1:0	MUTEN	R/W	0h	AMUTE pin enable bit [unless overridden by GPIO registers]. 0 AMUTE pin is disabled, pin goes to tri-state condition. 1 AMUTE pin is driven high if error is detected. 2 AMUTE pin is driven low if error is detected. 3 Reserved

14.9.1.1.2.10 MCASP_DLBCTL Register

1 MCASP_DLBCTL Register (Offset = 4Ch) [reset = 0h]

The digital loopback control register (DLBCTL) controls the internal loopback settings of the McASP in TDM mode.

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Table 14-25844. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 004Ch**
MCASP1	**02B1 004Ch**
MCASP2	**02B2 004Ch**

Figure 14-8569. MCASP_DLBCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED75</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED75</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED75</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED75</td><td colspan="2">MODE</td><td>ORD</td><td>DLBEN</td></tr>
<tr><td colspan="4">R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25846. MCASP_DLBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED75	R	0h	
3:2	MODE	R/W	0h	Loopback generator mode bits. Applies only when loopback mode is enabled [DLBEN = 1]. 0 Default and reserved on loopback mode (DLBEN = 1). When in non-loopback mode (DLBEN = 0), MODE should be left at default (00). When in loopback mode (DLBEN = 1), MODE = 00 is reserved and is not applicable. 1 Transmit clock and frame sync generators used by both transmit and receive sections. When in loopback mode (DLBEN = 1), MODE must be 01. 2 Reserved. 3 Reserved.

Table 14-25846. MCASP_DLBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ORD	R/W	0h	Loopback order bit when loopback mode is enabled [DLBEN = 1]. 0 Odd serializers N + 1 transmit to even serializers N that receive. The corresponding serializers must be programmed properly. 1 Even serializers N transmit to odd serializers N + 1 that receive. The corresponding serializers must be programmed properly.
0	DLBEN	R/W	0h	Loopback mode enable bit. 0 Loopback mode is disabled. 1 Loopback mode is enabled.

14.9.1.1.2.11 MCASP_DITCTL Register

1 MCASP_DITCTL Register (Offset = 50h) [reset = 0h]

The DIT mode control register (DITCTL) controls DIT operations of the McASP.

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Table 14-25847. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0050h**
MCASP1	**02B1 0050h**
MCASP2	**02B2 0050h**

Figure 14-8570. MCASP_DITCTL Name Register

31	30	29	28	27	26	25	24
RESERVED77							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED77							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED77							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED77				VB	VA	RESERVED76	DITEN
R				R/W	R/W	R	R/W
0h				0h	0h	0h	0h

Table 14-25849. MCASP_DITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED77	R	0h	
3	VB	R/W	0h	Valid bit for odd time slots [DIT right subframe]. 0 V bit is 0 during odd DIT subframes. 1 V bit is 1 during odd DIT subframes.
2	VA	R/W	0h	Valid bit for even time slots [DIT left subframe]. 0 V bit is 0 during even DIT subframes. 1 V bit is 1 during even DIT subframes.
1	RESERVED76	R	0h	
0	DITEN	R/W	0h	DIT mode enable bit. DITEN should only be changed while the XSMRST bit in GBLCTL is in reset [and for startup, XSRCLR also in reset]. However, it is not necessary to reset the XCLKRST or XHCLKRST bits in GBLCTL to change DITEN. 0 DIT mode is disabled. Transmitter operates in TDM or burst mode. 1 DIT mode is enabled. Transmitter operates in DIT encoded mode.

14.9.1.1.2.12 MCASP_RGBLCTL Register

1 MCASP_RGBLCTL Register (Offset = 60h) [reset = 0h]

Alias of the global control register (GBLCTL). Writing to the receiver global control register (RGBLCTL) affects only the receive bits of GBLCTL (bits 4-0). Reads from RGBLCTL return the value of GBLCTL. RGBLCTL allows the receiver to be reset independently from the transmitter.

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Table 14-25850. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0060h**
MCASP1	**02B1 0060h**
MCASP2	**02B2 0060h**

Figure 14-8571. MCASP_RGBLCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED79</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED79</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED79</td><td>XFRST</td><td>XSMRST</td><td>XSRCLR</td><td>XHCLKRST</td><td>XCLKRST</td></tr>
<tr><td colspan="3">R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED78</td><td>RFRST</td><td>RSMRST</td><td>RSRCLR</td><td>RHCLKRST</td><td>RCLKRST</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25852. MCASP_RGBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED79	R	0h	
12	XFRST	R	0h	Transmit frame sync generator reset enable bit. A read of this bit returns the XFRST bit value of GBLCTL. Writes have no effect.
11	XSMRST	R	0h	Transmit state machine reset enable bit. A read of this bit returns the XSMRST bit value of GBLCTL. Writes have no effect.
10	XSRCLR	R	0h	Transmit serializer clear enable bit. A read of this bit returns the XSRCLR bit value of GBLCTL. Writes have no effect.
9	XHCLKRST	R	0h	Transmit high-frequency clock divider reset enable bit. A read of this bit returns the XHCLKRST bit value of GBLCTL. Writes have no effect.
8	XCLKRST	R	0h	Transmit clock divider reset enable bit. A read of this bit returns the XCLKRST bit value of GBLCTL. Writes have no effect.
7:5	RESERVED78	R	0h	
4	RFRST	R/W	0h	Receive frame sync generator reset enable bit. A write to this bit affects the RFRST bit of GBLCTL. 0 Receive frame sync generator is reset. 1 Receive frame sync generator is active.

Table 14-25852. MCASP_RGBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RSMRST	R/W	0h	Receive state machine reset enable bit. A write to this bit affects the RSMRST bit of GBLCTL. 0 `Receive state machine is held in reset.` 1 `Receive state machine is released from reset.`
2	RSRCLR	R/W	0h	Receive serializer clear enable bit. A write to this bit affects the RSRCLR bit of GBLCTL. 0 `Receive serializers are cleared.` 1 `Receive serializers are active.`
1	RHCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. A write to this bit affects the RHCLKRST bit of GBLCTL. 0 `Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1.` 1 `Receive high-frequency clock divider is running.`
0	RCLKRST	R/W	0h	Receive clock divider reset enable bit. A write to this bit affects the RCLKRST bit of GBLCTL. 0 `Receive clock divider is held in reset.` 1 `Receive clock divider is running.`

14.9.1.1.2.13 MCASP_RMASK Register

1 MCASP_RMASK Register (Offset = 64h) [reset = 0h]

The receive format unit bit mask register (RMASK) determines which bits of the received data are masked off and padded with a known value before being read by the CPU or DMA.

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Table 14-25853. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0064h**
MCASP1	**02B1 0064h**
MCASP2	**02B2 0064h**

Figure 14-8572. MCASP_RMASK Name Register

31	30	29	28	27	26	25	24
RMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
RMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
RMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
RMASK							
R/W							
0h							

Table 14-25855. MCASP_RMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RMASK	R/W	0h	Receive data mask n enable bit. 0 `Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in RFMT).` 1 `Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA.`

14.9.1.1.2.14 MCASP_RFMT Register

1 MCASP_RFMT Register (Offset = 68h) [reset = 0h]

The receive bit stream format register (RFMT) configures the receive data format.

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Table 14-25856. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0068h**
MCASP1	**02B1 0068h**
MCASP2	**02B2 0068h**

Figure 14-8573. MCASP_RFMT Name Register

31	30	29	28	27	26	25	24
RESERVED80							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED80						RDATDLY	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RRVRS	RPAD		RPBIT				
R/W	R/W		R/W				
0h	0h		0h				
7	6	5	4	3	2	1	0
RSSZ				RBUSEL	RROT		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-25858. MCASP_RFMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED80	R	0h	
17:16	RDATDLY	R/W	0h	Receive bit delay. 0 `0-bit delay. The first receive data bit, AXRn, occurs in same ACLKR cycle as the receive frame sync (AFSR).` 1 `1-bit delay. The first receive data bit, AXRn, occurs one ACLKR cycle after the receive frame sync (AFSR).` 2 `2-bit delay. The first receive data bit, AXRn, occurs two ACLKR cycles after the receive frame sync (AFSR).` 3 `Reserved.`
15	RRVRS	R/W	0h	Receive serial bitstream order. 0 `Bitstream is LSB first. No bit reversal is performed in receive format bit reverse unit.` 1 `Bitstream is MSB first. Bit reversal is performed in receive format bit reverse unit.`

Table 14-25858. MCASP_RFMT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	RPAD	R/W	0h	Pad value for extra bits in slot not belonging to the word. This field only applies to bits when RMASK[n] = 0. 0 Pad extra bits with 0. 1 Pad extra bits with 1. 2 Pad extra bits with one of the bits from the word as specified by RPBIT bits. 3 Reserved.
12:8	RPBIT	R/W	0h	RPBIT value determines which bit [as read by the CPU or DMA from RBUF[n]] is used to pad the extra bits. This field only applies when RPAD = 2h. 0 Pad with bit 0 value. 1 Pad with bit 1 to bit 31 value from 1h to 1Fh.
7:4	RSSZ	R/W	0h	Receive slot size. 0 Reserved. 1 Reserved. 2 Reserved. 3 Slot size is 8 bits. 4 Reserved 5 Slot size is 12 bits. 6 Reserved 7 Slot size is 16 bits. 8 Reserved 9 Slot size is 20 bits. 10 Reserved 11 Slot size is 24 bits 12 Reserved 13 Slot size is 28 bits. 14 Reserved 15 Slot size is 32 bits.
3	RBUSEL	R/W	0h	Selects whether reads from serializer buffer XRBUF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0 Reads from XRBUF[n] originate on data port. Reads from XRBUF[n] on configuration bus are ignored. 1 Reads from XRBUF[n] originate on configuration bus. Reads from XRBUF[n] on data port are ignored.
2:0	RROT	R/W	0h	Right-rotation value for receive rotate right format unit. 0 Rotate right by 0 (no rotation). 1 Rotate right by 4 bit positions. 2 Rotate right by 8 bit positions. 3 Rotate right by 12 bit positions. 4 Rotate right by 16 bit positions. 5 Rotate right by 20 bit positions. 6 Rotate right by 24 bit positions. 7 Rotate right by 28 bit positions.

14.9.1.1.2.15 MCASP_AFSRCTL Register

1 MCASP_AFSRCTL Register (Offset = 6Ch) [reset = 0h]

The receive frame sync control register (AFSRCTL) configures the receive frame sync (AFSR).

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Table 14-25859. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 006Ch**
MCASP1	**02B1 006Ch**
MCASP2	**02B2 006Ch**

Figure 14-8574. MCASP_AFSRCTL Name Register

31	30	29	28	27	26	25	24
RESERVED83							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED83							
R							
0h							
15	14	13	12	11	10	9	8
RMOD							
R/W							
0h							
7	6	5	4	3	2	1	0
RMOD	RESERVED82		FRWID	RESERVED81		FSRM	FSRP
R/W	R		R/W	R		R/W	R/W
0h	0h		0h	0h		0h	0h

Table 14-25861. MCASP_AFSRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED83	R	0h	
15:7	RMOD	R/W	0h	Receive frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh. 0 Burst mode. 1 Reserved. 2 2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h. 33 Reserved from 21h to 17Fh. 384 384-slot TDM (external DIR IC inputting 384-slot DIR frames to McASP over I2S interface). 385 Reserved from 181h to 1FFh.
6:5	RESERVED82	R	0h	
4	FRWID	R/W	0h	Receive frame sync width select bit indicates the width of the receive frame sync [AFSR] during its active period. 0 Single bit. 1 Single word.
3:2	RESERVED81	R	0h	

Table 14-25861. MCASP_AFSRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSRM	R/W	0h	Receive frame sync generation select bit. 0 `Externally-generated receive frame sync.` 1 `Internally-generated receive frame sync.`
0	FSRP	R/W	0h	Receive frame sync polarity select bit. 0 `A rising edge on receive frame sync (AFSR) indicates the beginning of a frame.` 1 `A falling edge on receive frame sync (AFSR) indicates the beginning of a frame.`

14.9.1.1.2.16 MCASP_ACLKRCTL Register

1 MCASP_ACLKRCTL Register (Offset = 70h) [reset = 20h]

The receive clock control register (ACLKRCTL) configures the receive bit clock (ACLKR) and the receive clock generator.

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Table 14-25862. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0070h**
MCASP1	**02B1 0070h**
MCASP2	**02B2 0070h**

Figure 14-8575. MCASP_ACLKRCTL Name Register

31	30	29	28	27	26	25	24
RESERVED86							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED86			BUSY	DIVBUSY	ADJBUSY	CLKRADJ	
R/W			R/W	R/W	R/W	W	
0h			0h	0h	0h	0h	
15	14	13	12	11	10	9	8
RESERVED85							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKRP	RESERVED84	CLKRM	CLKRDIV				
R/W	R	R/W	R/W				
0h	0h	1h	0h				

Table 14-25864. MCASP_ACLKRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED86	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress
17:16	CLKRADJ	W	0h	CLKRDIV one-shot adjustment
15:8	RESERVED85	R/W	0h	
7	CLKRP	R/W	0h	Receive bitstream clock polarity select bit. 0 `Falling edge. Receiver samples data on the falling edge of the serial clock, so the external transmitter driving this receiver must shift data out on the rising edge of the serial clock.` 1 `Rising edge. Receiver samples data on the rising edge of the serial clock, so the external transmitter driving this receiver must shift data out on the falling edge of the serial clock.`
6	RESERVED84	R	0h	

Table 14-25864. MCASP_ACLKRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLKRM	R/W	1h	Receive bit clock source bit. Note that this bit does not have any effect, if ACLKXCTL.ASYNC = 0. 0 External receive clock source from ACLKR pin. 1 Internal receive clock source from output of programmable bit clock divider.
4:0	CLKRDIV	R/W	0h	Receive bit clock divide ratio bits determine the divide-down ratio from AHCLKR to ACLKR. Note that this bit does not have any effect, if ACLKXCTL.ASYNC = 0. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-32 from 2h to 1Fh.

14.9.1.1.2.17 MCASP_AHCLKRCTL Register

1 MCASP_AHCLKRCTL Register (Offset = 74h) [reset = 8000h]

The receive high-frequency clock control register (AHCLKRCTL) configures the receive high-frequency controller clock (AHCLKR) and the receive clock generator.

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Table 14-25865. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0074h**
MCASP1	**02B1 0074h**
MCASP2	**02B2 0074h**

Figure 14-8576. MCASP_AHCLKRCTL Name Register

31	30	29	28	27	26	25	24
RESERVED88							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED88			BUSY	DIVBUSY	ADJBUSY	HCLKRADJ	
R/W			R/W	R/W	R/W	W	
0h			0h	0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HCLKRM	HCLKRP	RESERVED87		HCLKRDIV			
R/W	R/W	R		R/W			
1h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HCLKRDIV							
R/W							
0h							

Table 14-25867. MCASP_AHCLKRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED88	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress?
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress?
17:16	HCLKRADJ	W	0h	HCLKRDIV one-shot adjustment
15	HCLKRM	R/W	1h	Receive high-frequency clock source bit. 0 External receive high-frequency clock source from AHCLKR pin. 1 Internal receive high-frequency clock source from output of programmable high clock divider.

Table 14-25867. MCASP_AHCLKRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HCLKRP	R/W	0h	Receive bitstream high-frequency clock polarity select bit. 0 AHCLKR is not inverted before programmable bit clock divider. In the special case where the receive bit clock (ACLKR) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKRDIV = 0 in ACLKRCTL), AHCLKR is directly passed through to the ACLKR pin. 1 AHCLKR is inverted before programmable bit clock divider. In the special case where the receive bit clock (ACLKR) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKRDIV = 0 in ACLKRCTL), AHCLKR is directly passed through to the ACLKR pin.
13:12	RESERVED87	R	0h	
11:0	HCLKRDIV	R/W	0h	Receive high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to AHCLKR. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-4096 from 2h to FFFh.

14.9.1.1.2.18 MCASP_RTDM Register

1 MCASP_RTDM Register (Offset = 78h) [reset = 0h]

The receive TDM time slot register (RTDM) specifies which TDM time slot the receiver is active.

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Table 14-25868. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0078h**
MCASP1	**02B1 0078h**
MCASP2	**02B2 0078h**

Figure 14-8577. MCASP_RTDM Name Register

31	30	29	28	27	26	25	24
RTDMS							
R/W							
0h							
23	22	21	20	19	18	17	16
RTDMS							
R/W							
0h							
15	14	13	12	11	10	9	8
RTDMS							
R/W							
0h							
7	6	5	4	3	2	1	0
RTDMS							
R/W							
0h							

Table 14-25870. MCASP_RTDM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RTDMS	R/W	0h	Receiver mode during TDM time slot n. 0 `Receive TDM time slot n is inactive. The receive serializer does not shift in data during this slot.` 1 `Receive TDM time slot n is active. The receive serializer shifts in data during this slot.`

14.9.1.1.2.19 MCASP_RINTCTL Register

1 MCASP_RINTCTL Register (Offset = 7Ch) [reset = 0h]

The receiver interrupt control register (RINTCTL) controls generation of the McASP receive interrupt (RINT). When the register bit(s) is set to 1, the occurrence of the enabled McASP condition(s) generates RINT. See the RSTAT register for a description of the interrupt conditions.

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Table 14-25871. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 007Ch**
MCASP1	**02B1 007Ch**
MCASP2	**02B2 007Ch**

Figure 14-8578. MCASP_RINTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED90							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED90							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED90							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSTAFRM	RESERVED89	RDATA	RLAST	RDMAERR	RCKFAIL	RSYNCERR	ROVRN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25873. MCASP_RINTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED90	R	0h	
7	RSTAFRM	R/W	0h	Receive start of frame interrupt enable bit. 0 `Interrupt is disabled. A receive start of frame interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive start of frame interrupt generates a McASP receive interrupt (RINT).`
6	RESERVED89	R	0h	
5	RDATA	R/W	0h	Receive data ready interrupt enable bit. 0 `Interrupt is disabled. A receive data ready interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive data ready interrupt generates a McASP receive interrupt (RINT).`

Table 14-25873. MCASP_RINTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RLAST	R/W	0h	Receive last slot interrupt enable bit. 0 Interrupt is disabled. A receive last slot interrupt does not generate a McASP receive interrupt (RINT). 1 Interrupt is enabled. A receive last slot interrupt generates a McASP receive interrupt (RINT).
3	RDMAERR	R/W	0h	Receive DMA error interrupt enable bit. 0 Interrupt is disabled. A receive DMA error interrupt does not generate a McASP receive interrupt (RINT). 1 Interrupt is enabled. A receive DMA error interrupt generates a McASP receive interrupt (RINT).
2	RCKFAIL	R/W	0h	Receive clock failure interrupt enable bit. 0 Interrupt is disabled. A receive clock failure interrupt does not generate a McASP receive interrupt (RINT). 1 Interrupt is enabled. A receive clock failure interrupt generates a McASP receive interrupt (RINT).
1	RSYNCERR	R/W	0h	Unexpected receive frame sync interrupt enable bit. 0 Interrupt is disabled. An unexpected receive frame sync interrupt does not generate a McASP receive interrupt (RINT). 1 Interrupt is enabled. An unexpected receive frame sync interrupt generates a McASP receive interrupt (RINT).
0	ROVRN	R/W	0h	Receiver overrun interrupt enable bit. 0 Interrupt is disabled. A receiver overrun interrupt does not generate a McASP receive interrupt (RINT). 1 Interrupt is enabled. A receiver overrun interrupt generates a McASP receive interrupt (RINT).

14.9.1.1.2.20 MCASP_RSTAT Register

1 MCASP_RSTAT Register (Offset = 80h) [reset = 0h]

The receiver status register (RSTAT) provides the receiver status and receive TDM time slot number. If the McASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the McASP logic has priority and the flag remains set. This also causes a new interrupt request to be generated.

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Table 14-25874. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0080h**
MCASP1	**02B1 0080h**
MCASP2	**02B2 0080h**

Figure 14-8579. MCASP_RSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED91							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED91							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED91							RERR
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDMAERR	RSTAFRM	RDATA	RLAST	RTDMSLOT	RCKFAIL	RSYNCERR	ROVRN
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25876. MCASP_RSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED91	R	0h	

8	RERR	R/W	0h	RERR bit always returns a logic-OR of: ROVRN OR RSYNCERR OR RCKFAIL OR RDMAERR. Allows a single bit to be checked to determine if a receiver error interrupt has occurred.
				`0 No errors have occurred.`
				`1 An error has occurred.`

7	RDMAERR	R/W1TC	0h	Receive DMA error flag. RDMAERR is set when the CPU or DMA reads more serializers through the data port in a given time slot than were programmed as receivers. Causes a receive interrupt [RINT], if this bit is set and RDMAERR in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect.
				`0 Receive DMA error did not occur.`
				`1 Receive DMA error did occur.`

Table 14-25876. MCASP_RSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RSTAFRM	R/W1TC	0h	Receive start of frame flag. Causes a receive interrupt [RINT], if this bit is set and RSTAFRM in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 No new receive frame sync (AFSR) is detected. 1 A new receive frame sync (AFSR) is detected.
5	RDATA	R/W1TC	0h	Receive data ready flag. Causes a receive interrupt [RINT], if this bit is set and RDATA in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 No new data in RBUF. 1 Data is transferred from XRSR to RBUF and ready to be serviced by the CPU or DMA. When RDATA is set, it always causes a DMA event (AREVT).
4	RLAST	R/W1TC	0h	Receive last slot flag. RLAST is set along with RDATA, if the current slot is the last slot in a frame. Causes a receive interrupt [RINT], if this bit is set and RLAST in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 Current slot is not the last slot in a frame. 1 Current slot is the last slot in a frame. RDATA is also set.
3	RTDMSLOT	R	0h	Returns the LSB of RSLOT. Allows a single read of RSTAT to determine whether the current TDM time slot is even or odd. 0 Current TDM time slot is odd. 1 Current TDM time slot is even.
2	RCKFAIL	R/W1TC	0h	Receive clock failure flag. RCKFAIL is set when the receive clock failure detection circuit reports an error. Causes a receive interrupt [RINT], if this bit is set and RCKFAIL in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 Receive clock failure did not occur. 1 Receive clock failure did occur.
1	RSYNCERR	R/W1TC	0h	Unexpected receive frame sync flag. RSYNCERR is set when a new receive frame sync [AFSR] occurs before it is expected. Causes a receive interrupt [RINT], if this bit is set and RSYNCERR in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 Unexpected receive frame sync did not occur. 1 Unexpected receive frame sync did occur.
0	ROVRN	R/W1TC	0h	Receiver overrun flag. ROVRN is set when the receive serializer is instructed to transfer data from XRSR to RBUF, but the former data in RBUF has not yet been read by the CPU or DMA. Causes a receive interrupt [RINT], if this bit is set and ROVRN in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 Receiver overrun did not occur. 1 Receiver overrun did occur.

14.9.1.1.2.21 MCASP_RSLOT Register

1 MCASP_RSLOT Register (Offset = 84h) [reset = 0h]

The current receive TDM time slot register (RSLOT) indicates the current time slot for the receive data frame.

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Table 14-25877. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0084h**
MCASP1	**02B1 0084h**
MCASP2	**02B2 0084h**

Figure 14-8580. MCASP_RSLOT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED92</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED92</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED92</td><td>RSLOTCNT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSLOTCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25879. MCASP_RSLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED92	R	0h	
8:0	RSLOTCNT	R	0h	0-17Fh = Current receive time slot count. Legal values: 0 to 383 [17Fh]. TDM function is not supported for > 32 time slots. However, TDM time slot counter may count to 383 when used to receive a DIR block [transferred over TDM format].

14.9.1.1.2.22 MCASP_RCLKCHK Register

1 MCASP_RCLKCHK Register (Offset = 88h) [reset = 0h]

The receive clock check control register (RCLKCHK) configures the receive clock failure detection circuit.

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Table 14-25880. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0088h**
MCASP1	**02B1 0088h**
MCASP2	**02B2 0088h**

Figure 14-8581. MCASP_RCLKCHK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RMIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED93</td><td colspan="4">RPS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-25882. MCASP_RCLKCHK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RCNT	R	0h	Receive clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 receive high-frequency controller clock [AHCLKR] signals, and stores the count in RCNT until the next measurement is taken.
23:16	RMAX	R/W	0h	Receive clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 receive high-frequency controller clock [AHCLKR] signals have been received. If the current counter value is greater than RMAX after counting 32 AHCLKR signals, RCKFAIL in RSTAT is set. The comparison is performed using unsigned arithmetic.
15:8	RMIN	R/W	0h	Receive clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 receive high-frequency controller clock [AHCLKR] signals have been received. If RCNT is less than RMIN after counting 32 AHCLKR signals, RCKFAIL in RSTAT is set. The comparison is performed using unsigned arithmetic.
7:4	RESERVED93	R	0h	

Table 14-25882. MCASP_RCLKCHK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RPS	R/W	0h	Receive clock check prescaler value. 0 `MCASP system clock divided by 1.` 1 `MCASP system clock divided by 2.` 2 `MCASP system clock divided by 4.` 3 `MCASP system clock divided by 8.` 4 `MCASP system clock divided by 16.` 5 `MCASP system clock divided by 32.` 6 `MCASP system clock divided by 64.` 7 `MCASP system clock divided by 128.` 8 `MCASP system clock divided by 256.` 9 `Reserved from 9h to Fh.`

14.9.1.1.2.23 MCASP_PIDTCTL Register

1 MCASP_PIDTCTL Register (Offset = 8Ch) [reset = 0h]

The receiver DMA event control register (PIDTCTL) contains a disable bit for the receiver DMA event. Note for device-specific registers: Accessing PIDTCTL not implemented on a specific device may cause improper operation.

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Table 14-25883. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 008Ch**
MCASP1	**02B1 008Ch**
MCASP2	**02B2 008Ch**

Figure 14-8582. MCASP_PIDTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED94							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED94							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED94							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED94							RDATDMA
R							R/W
0h							0h

Table 14-25885. MCASP_PIDTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED94	R	0h	
0	RDATDMA	R/W	0h	Receive data DMA request enable bit. If Writing to this bit, always write the default value of 0. 0 Receive data DMA request is enabled. 1 Reserved

14.9.1.1.2.24 MCASP_XGBLCTL Register

1 MCASP_XGBLCTL Register (Offset = A0h) [reset = 0h]

Alias of the global control register (GBLCTL). Writing to the transmitter global control register (XGBLCTL) affects only the transmit bits of GBLCTL (bits 12-8). Reads from XGBLCTL return the value of GBLCTL. XGBLCTL allows the transmitter to be reset independently from the receiver. See the GBLCTL register for a detailed description of GBLCTL.

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Table 14-25886. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00A0h**
MCASP1	**02B1 00A0h**
MCASP2	**02B2 00A0h**

Figure 14-8583. MCASP_XGBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED96							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED96							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED96			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED95			RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 14-25888. MCASP_XGBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED96	R	0h	

12	XFRST	R/W	0h	Transmit frame sync generator reset enable bit. A write to this bit affects the XFRST bit of GBLCTL.
				`0 Transmit frame sync generator is reset.`
				`1 Transmit frame sync generator is active.`

11	XSMRST	R/W	0h	Transmit state machine reset enable bit. A write to this bit affects the XSMRST bit of GBLCTL.
				`0 Transmit state machine is held in reset.`
				`1 Transmit state machine is released from reset.`

10	XSRCLR	R/W	0h	Transmit serializer clear enable bit. A write to this bit affects the XSRCLR bit of GBLCTL.
				`0 Transmit serializers are cleared.`
				`1 Transmit serializers are active.`

Table 14-25888. MCASP_XGBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	XHCLKRST	R/W	0h	Transmit high-frequency clock divider reset enable bit. A write to this bit affects the XHCLKRST bit of GBLCTL. 0 `Transmit high-frequency clock divider is held in reset.` 1 `Transmit high-frequency clock divider is running.`
8	XCLKRST	R/W	0h	Transmit clock divider reset enable bit. A write to this bit affects the XCLKRST bit of GBLCTL. 0 `Transmit clock divider is held in reset.` 1 `Transmit clock divider is running.`
7:5	RESERVED95	R	0h	
4	RFRST	R	0h	Receive frame sync generator reset enable bit. A read of this bit returns the RFRST bit value of GBLCTL. Writes have no effect.
3	RSMRST	R	0h	Receive state machine reset enable bit. A read of this bit returns the RSMRST bit value of GBLCTL. Writes have no effect.
2	RSRCLR	R	0h	Receive serializer clear enable bit. A read of this bit returns the RSRSCLR bit value of GBLCTL. Writes have no effect.
1	RHCLKRST	R	0h	Receive high-frequency clock divider reset enable bit. A read of this bit returns the RHCLKRST bit value of GBLCTL. Writes have no effect.
0	RCLKRST	R	0h	Receive clock divider reset enable bit. A read of this bit returns the RCLKRST bit value of GBLCTL. Writes have no effect.

14.9.1.1.2.25 MCASP_XMASK Register

1 MCASP_XMASK Register (Offset = A4h) [reset = 0h]

The transmit format unit bit mask register (XMASK) determines which bits of the transmitted data are masked off and padded with a known value before being shifted out the McASP.

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Table 14-25889. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00A4h**
MCASP1	**02B1 00A4h**
MCASP2	**02B2 00A4h**

Figure 14-8584. MCASP_XMASK Name Register

31	30	29	28	27	26	25	24
XMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
XMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
XMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
XMASK							
R/W							
0h							

Table 14-25891. MCASP_XMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XMASK	R/W	0h	Transmit data mask n enable bit. 0 Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in XFMT), which is transmitted out the McASP in place of the original bit. 1 Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP.

14.9.1.1.2.26 MCASP_XFMT Register

1 MCASP_XFMT Register (Offset = A8h) [reset = 0h]

The transmit bit stream format register (XFMT) configures the transmit data format.

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Table 14-25892. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00A8h**
MCASP1	**02B1 00A8h**
MCASP2	**02B2 00A8h**

Figure 14-8585. MCASP_XFMT Name Register

31	30	29	28	27	26	25	24
RESERVED97							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED97						XDATDLY	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
XRVRS	XPAD		XPBIT				
R/W	R/W		R/W				
0h	0h		0h				
7	6	5	4	3	2	1	0
XSSZ				XBUSEL	XROT		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-25894. MCASP_XFMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED97	R	0h	
17:16	XDATDLY	R/W	0h	Transmit sync bit delay. 0 `0-bit delay. The first transmit data bit, AXRn, occurs in same ACLKX cycle as the transmit frame sync (AFSX).` 1 `1-bit delay. The first transmit data bit, AXRn, occurs one ACLKX cycle after the transmit frame sync (AFSX).` 2 `2-bit delay. The first transmit data bit, AXRn, occurs two ACLKX cycles after the transmit frame sync (AFSX).` 3 `Reserved.`
15	XRVRS	R/W	0h	Transmit serial bitstream order. 0 `Bitstream is LSB first. No bit reversal is performed in transmit format bit reverse unit.` 1 `Bitstream is MSB first. Bit reversal is performed in transmit format bit reverse unit.`

Table 14-25894. MCASP_XFMT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	XPAD	R/W	0h	Pad value for extra bits in slot not belonging to word defined by XMASK. This field only applies to bits when XMASK[n] = 0. 0 Pad extra bits with 0. 1 Pad extra bits with 1. 2 Pad extra bits with one of the bits from the word as specified by XPBIT bits. 3 Reserved.
12:8	XPBIT	R/W	0h	XPBIT value determines which bit [as written by the CPU or DMA to XBUF[n]] is used to pad the extra bits before shifting. This field only applies when XPAD = 2h. 0 Pad with bit 0 value. 1 Pad with bit 1 to bit 31 value from 1h to 1Fh.
7:4	XSSZ	R/W	0h	Transmit slot size. 0 Reserved. 1 Reserved. 2 Reserved. 3 Slot size is 8 bits. 4 Reserved. 5 Slot size is 12 bits. 6 Reserved. 7 Slot size is 16 bits. 8 Reserved. 9 Slot size is 20 bits. 10 Reserved. 11 Slot size is 24 bits. 12 Reserved. 13 Slot size is 28 bits. 14 Reserved. 15 Slot size is 32 bits.
3	XBUSEL	R/W	0h	Selects whether writes to serializer buffer XRBUF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0 Writes to XRBUF[n] originate from the data port. Writes to XRBUF[n] from the configuration bus are ignored with no effect to the McASP. 1 Writes to XRBUF[n] originate from the configuration bus. Writes to XRBUF[n] from the data port are ignored with no effect to the McASP.
2:0	XROT	R/W	0h	Right-rotation value for transmit rotate right format unit. 0 Rotate right by 0 (no rotation). 1 Rotate right by 4 bit positions. 2 Rotate right by 8 bit positions. 3 Rotate right by 12 bit positions. 4 Rotate right by 16 bit positions. 5 Rotate right by 20 bit positions. 6 Rotate right by 24 bit positions. 7 Rotate right by 28 bit positions.

14.9.1.1.2.27 MCASP_AFSXCTL Register

1 MCASP_AFSXCTL Register (Offset = ACh) [reset = 0h]

The transmit frame sync control register (AFSXCTL) configures the transmit frame sync (AFSX).

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Table 14-25895. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00ACh**
MCASP1	**02B1 00ACh**
MCASP2	**02B2 00ACh**

Figure 14-8586. MCASP_AFSXCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED100</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED100</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">XMOD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>XMOD</td><td colspan="2">RESERVED99</td><td>FXWID</td><td colspan="2">RESERVED98</td><td>FSXM</td><td>FSXP</td></tr>
<tr><td>R/W</td><td colspan="2">R</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25897. MCASP_AFSXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED100	R	0h	
15:7	XMOD	R/W	0h	Transmit frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh. 0 Burst mode. 1 Reserved. 2 2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h. 33 Reserved from 21h to 17Fh. 384 384-slot DIT mode. 385 Reserved from 181h to 1FFh.
6:5	RESERVED99	R	0h	
4	FXWID	R/W	0h	Transmit frame sync width select bit indicates the width of the transmit frame sync [AFSX] during its active period. 0 Single bit. 1 Single word.
3:2	RESERVED98	R	0h	
1	FSXM	R/W	0h	Transmit frame sync generation select bit. 0 Externally-generated transmit frame sync. 1 Internally-generated transmit frame sync.

Table 14-25897. MCASP_AFSXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSXP	R/W	0h	Transmit frame sync polarity select bit. 0 `A rising edge on transmit frame sync (AFSX) indicates the beginning of a frame.` 1 `A falling edge on transmit frame sync (AFSX) indicates the beginning of a frame.`

14.9.1.1.2.28 MCASP_ACLKXCTL Register

1 MCASP_ACLKXCTL Register (Offset = B0h) [reset = 60h]

The transmit clock control register (ACLKXCTL) configures the transmit bit clock (ACLKX) and the transmit clock generator.

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Table 14-25898. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00B0h**
MCASP1	**02B1 00B0h**
MCASP2	**02B2 00B0h**

Figure 14-8587. MCASP_ACLKXCTL Name Register

31	30	29	28	27	26	25	24
RESERVED102							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED102			BUSY	DIVBUSY	ADJBUSY	CLKXADJ	
R/W			R/W	R/W	R/W	W	
0h			0h	0h	0h	0h	
15	14	13	12	11	10	9	8
RESERVED101							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKXP	ASYNC	CLKXM	CLKXDIV				
R/W	R/W	R/W	R/W				
0h	1h	1h	0h				

Table 14-25900. MCASP_ACLKXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED102	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress
17:16	CLKXADJ	W	0h	CLKXDIV one-shot adjustment
15:8	RESERVED101	R/W	0h	
7	CLKXP	R/W	0h	Transmit bitstream clock polarity select bit. 0 Rising edge. External receiver samples data on the falling edge of the serial clock, so the transmitter must shift data out on the rising edge of the serial clock. 1 Falling edge. External receiver samples data on the rising edge of the serial clock, so the transmitter must shift data out on the falling edge of the serial clock.

Table 14-25900. MCASP_ACLKXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ASYNC	R/W	1h	Transmit/receive operation asynchronous enable bit. 0 `Synchronous. Transmit clock and frame sync provides the source for both the transmit and receive sections.` 1 `Asynchronous. Separate clock and frame sync used by transmit and receive sections.`
5	CLKXM	R/W	1h	Transmit bit clock source bit. 0 `External transmit clock source from ACLKX pin.` 1 `Internal transmit clock source from output of programmable bit clock divider.`
4:0	CLKXDIV	R/W	0h	Transmit bit clock divide ratio bits determine the divide-down ratio from AHCLKX to ACLKX. 0 `Divide-by-1.` 1 `Divide-by-2.` 2 `Divide-by-3 to divide-by-32 from 2h to 1Fh.`

14.9.1.1.2.29 MCASP_AHCLKXCTL Register

1 MCASP_AHCLKXCTL Register (Offset = B4h) [reset = 8000h]

The transmit high-frequency clock control register (AHCLKXCTL) configures the transmit high-frequency controller clock (AHCLKX) and the transmit clock generator.

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Table 14-25901. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00B4h**
MCASP1	**02B1 00B4h**
MCASP2	**02B2 00B4h**

Figure 14-8588. MCASP_AHCLKXCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED104</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED104</td><td>BUSY</td><td>DIVBUSY</td><td>ADJBUSY</td><td colspan="2">HCLKXADJ</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>HCLKXM</td><td>HCLKXP</td><td colspan="2">RESERVED103</td><td colspan="4">HCLKXDIV</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>0h</td><td colspan="2">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HCLKXDIV</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25903. MCASP_AHCLKXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED104	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress?
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress?
17:16	HCLKXADJ	W	0h	HCLKXDIV one-shot adjustment
15	HCLKXM	R/W	1h	Transmit high-frequency clock source bit. 0 External transmit high-frequency clock source from AHCLKX pin. 1 Internal transmit high-frequency clock source from output of programmable high clock divider.

Table 14-25903. MCASP_AHCLKXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HCLKXP	R/W	0h	Transmit bitstream high-frequency clock polarity select bit. 0 AHCLKX is not inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin. 1 AHCLKX is inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin.
13:12	RESERVED103	R	0h	
11:0	HCLKXDIV	R/W	0h	Transmit high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to AHCLKX. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-4096 from 2h to FFFh.

14.9.1.1.2.30 MCASP_XTDM Register

1 MCASP_XTDM Register (Offset = B8h) [reset = 0h]

The transmit TDM time slot register (XTDM) specifies in which TDM time slot the transmitter is active. TDM time slot counter range is extended to 384 slots (to support SPDIF blocks of 384 subframes). XTDM operates modulo 32, that is, XTDMS specifies the TDM activity for time slots 0, 32, 64, 96, 128, and so on.

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Table 14-25904. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00B8h**
MCASP1	**02B1 00B8h**
MCASP2	**02B2 00B8h**

Figure 14-8589. MCASP_XTDM Name Register

31	30	29	28	27	26	25	24
XTDMS							
R/W							
0h							
23	22	21	20	19	18	17	16
XTDMS							
R/W							
0h							
15	14	13	12	11	10	9	8
XTDMS							
R/W							
0h							
7	6	5	4	3	2	1	0
XTDMS							
R/W							
0h							

Table 14-25906. MCASP_XTDM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XTDMS	R/W	0h	Transmitter mode during TDM time slot n. 0 `Transmit TDM time slot n is inactive. The transmit serializer does not shift out data during this slot.` 1 `Transmit TDM time slot n is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL).`

14.9.1.1.2.31 MCASP_XINTCTL Register

1 MCASP_XINTCTL Register (Offset = BCh) [reset = 0h]

The transmitter interrupt control register (XINTCTL) controls generation of the McASP transmit interrupt (XINT). When the register bit(s) is set to 1, the occurrence of the enabled McASP condition(s) generates XINT. See the XSTAT register for a description of the interrupt conditions.

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Table 14-25907. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00BCh**
MCASP1	**02B1 00BCh**
MCASP2	**02B2 00BCh**

Figure 14-8590. MCASP_XINTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED106							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED106							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED106							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XSTAFRM	RESERVED105	XDATA	XLAST	XDMAERR	XCKFAIL	XSYNCERR	XUNDRN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25909. MCASP_XINTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED106	R	0h	
7	XSTAFRM	R/W	0h	Transmit start of frame interrupt enable bit. 0 `Interrupt is disabled. A transmit start of frame interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit start of frame interrupt generates a McASP transmit interrupt (XINT).`
6	RESERVED105	R	0h	
5	XDATA	R/W	0h	Transmit data ready interrupt enable bit. 0 `Interrupt is disabled. A transmit data ready interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit data ready interrupt generates a McASP transmit interrupt (XINT).`

Table 14-25909. MCASP_XINTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XLAST	R/W	0h	Transmit last slot interrupt enable bit. 0 `Interrupt is disabled. A transmit last slot interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit last slot interrupt generates a McASP transmit interrupt (XINT).`
3	XDMAERR	R/W	0h	Transmit DMA error interrupt enable bit. 0 `Interrupt is disabled. A transmit DMA error interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit DMA error interrupt generates a McASP transmit interrupt (XINT).`
2	XCKFAIL	R/W	0h	Transmit clock failure interrupt enable bit. 0 `Interrupt is disabled. A transmit clock failure interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit clock failure interrupt generates a McASP transmit interrupt (XINT).`
1	XSYNCERR	R/W	0h	Unexpected transmit frame sync interrupt enable bit. 0 `Interrupt is disabled. An unexpected transmit frame sync interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. An unexpected transmit frame sync interrupt generates a McASP transmit interrupt (XINT).`
0	XUNDRN	R/W	0h	Transmitter underrun interrupt enable bit. 0 `Interrupt is disabled. A transmitter underrun interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmitter underrun interrupt generates a McASP transmit interrupt (XINT).`

14.9.1.1.2.32 MCASP_XSTAT Register

1 MCASP_XSTAT Register (Offset = C0h) [reset = 0h]

The transmitter status register (XSTAT) provides the transmitter status and transmit TDM time slot number. If the McASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the McASP logic has priority and the flag remains set. This also causes a new interrupt request to be generated.

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Table 14-25910. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00C0h**
MCASP1	**02B1 00C0h**
MCASP2	**02B2 00C0h**

Figure 14-8591. MCASP_XSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED107							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED107							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED107							XERR
R							R/W
0h							0h

7	6	5	4	3	2	1	0
XDMAERR	XSTAFRM	XDATA	XLAST	XTDMSLOT	XCKFAIL	XSYNCERR	XUNDRN
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25912. MCASP_XSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED107	R	0h	

8	XERR	R/W	0h	XERR bit always returns a logic-OR of: XUNDRN OR XSYNCERR OR XCKFAIL OR XDMAERR. Allows a single bit to be checked to determine if a transmitter error interrupt has occurred.
				`0 No errors have occurred.`
				`1 An error has occurred.`

7	XDMAERR	R/W1TC	0h	Transmit DMA error flag. XDMAERR is set when the CPU or DMA writes more serializers through the data port in a given time slot than were programmed as transmitters. Causes a transmit interrupt [XINT], if this bit is set and XDMAERR in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect.
				`0 Transmit DMA error did not occur.`
				`1 Transmit DMA error did occur.`

Table 14-25912. MCASP_XSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XSTAFRM	R/W1TC	0h	Transmit start of frame flag. Causes a transmit interrupt [XINT], if this bit is set and XSTAFRM in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 No new transmit frame sync (AFSX) is detected. 1 A new transmit frame sync (AFSX) is detected.
5	XDATA	R/W1TC	0h	Transmit data ready flag. Causes a transmit interrupt [XINT], if this bit is set and XDATA in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 XBUF is written and is full. 1 Data is copied from XBUF to XRSR. XBUF is empty and ready to be written. XDATA is also set when the transmit serializers are taken out of reset. When XDATA is set, it always causes a DMA event (AXEVT).
4	XLAST	R/W1TC	0h	Transmit last slot flag. XLAST is set along with XDATA, if the current slot is the last slot in a frame. Causes a transmit interrupt [XINT], if this bit is set and XLAST in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Current slot is not the last slot in a frame. 1 Current slot is the last slot in a frame. XDATA is also set.
3	XTDMSLOT	R	0h	Returns the LSB of XSLOT. Allows a single read of XSTAT to determine whether the current TDM time slot is even or odd. 0 Current TDM time slot is odd. 1 Current TDM time slot is even.
2	XCKFAIL	R/W1TC	0h	Transmit clock failure flag. XCKFAIL is set when the transmit clock failure detection circuit reports an error. Causes a transmit interrupt [XINT], if this bit is set and XCKFAIL in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Transmit clock failure did not occur. 1 Transmit clock failure did occur.
1	XSYNCERR	R/W1TC	0h	Unexpected transmit frame sync flag. XSYNCERR is set when a new transmit frame sync [AFSX] occurs before it is expected. Causes a transmit interrupt [XINT], if this bit is set and XSYNCERR in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Unexpected transmit frame sync did not occur. 1 Unexpected transmit frame sync did occur.
0	XUNDRN	R/W1TC	0h	Transmitter underrun flag. XUNDRN is set when the transmit serializer is instructed to transfer data from XBUF to XRSR, but XBUF has not yet been serviced with new data since the last transfer. Causes a transmit interrupt [XINT], if this bit is set and XUNDRN in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Transmitter underrun did not occur. 1 Transmitter underrun did occur. For details on MCASP action upon underrun conditions, see Buffer Underrun Error - Transmitter.

14.9.1.1.2.33 MCASP_XSLOT Register

1 MCASP_XSLOT Register (Offset = C4h) [reset = 17Fh]

The current transmit TDM time slot register (XSLOT) indicates the current time slot for the transmit data frame.

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Table 14-25913. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00C4h**
MCASP1	**02B1 00C4h**
MCASP2	**02B2 00C4h**

Figure 14-8592. MCASP_XSLOT Name Register

31	30	29	28	27	26	25	24
RESERVED108							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED108							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED108						XSLOTCNT	
R						R	
0h						17Fh	
7	6	5	4	3	2	1	0
XSLOTCNT							
R							
17Fh							

Table 14-25915. MCASP_XSLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED108	R	0h	
9:0	XSLOTCNT	R	17Fh	Current transmit time slot count. Legal values: 0 to 383 [17Fh]. During reset, this counter value is 383 so the next count value, which is used to encode the first DIT group of data, will be 0 and encodes the B preamble. TDM function is not supported for >32 time slots. However, TDM time slot counter may count to 383 when used to transmit a DIT block.

14.9.1.1.2.34 MCASP_XCLKCHK Register

1 MCASP_XCLKCHK Register (Offset = C8h) [reset = 0h]

The transmit clock check control register (XCLKCHK) configures the transmit clock failure detection circuit.

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Table 14-25916. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00C8h**
MCASP1	**02B1 00C8h**
MCASP2	**02B2 00C8h**

Figure 14-8593. MCASP_XCLKCHK Name Register

31	30	29	28	27	26	25	24
XCNT							
R							
0h							
23	22	21	20	19	18	17	16
XMAX							
R/W							
0h							
15	14	13	12	11	10	9	8
XMIN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED109				XPS			
R				R/W			
0h				0h			

Table 14-25918. MCASP_XCLKCHK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	XCNT	R	0h	Transmit clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 transmit high-frequency controller clock [AHCLKX] signals, and stores the count in XCNT until the next measurement is taken.
23:16	XMAX	R/W	0h	Transmit clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 transmit high-frequency controller clock [AHCLKX] signals have been received. If the current counter value is greater than XMAX after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.
15:8	XMIN	R/W	0h	Transmit clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 transmit high-frequency controller clock [AHCLKX] signals have been received. If XCNT is less than XMIN after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.
7:4	RESERVED109	R	0h	

Table 14-25918. MCASP_XCLKCHK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	XPS	R/W	0h	Transmit clock check prescaler value. Fh = Reserved from 9h to Fh. 0 `MCASP system clock divided by 1.` 1 `MCASP system clock divided by 2.` 2 `MCASP system clock divided by 4.` 3 `MCASP system clock divided by 8.` 4 `MCASP system clock divided by 16.` 5 `MCASP system clock divided by 32.` 6 `MCASP system clock divided by 64.` 7 `MCASP system clock divided by 128.` 8 `MCASP system clock divided by 256.` 9 `Reserved from 9h to Fh.`

14.9.1.1.2.35 MCASP_XEVTCTL Register

1 MCASP_XEVTCTL Register (Offset = CCh) [reset = 0h]

The transmitter DMA event control register (XEVTCTL) contains a disable bit for the transmit DMA event. Note for device-specific registers: Accessing XEVTCTL not implemented on a specific device may cause improper device operation.

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Table 14-25919. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 00CCh**
MCASP1	**02B1 00CCh**
MCASP2	**02B2 00CCh**

Figure 14-8594. MCASP_XEVTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED110							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED110							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED110							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED110							XDATDMA
R							R/W
0h							0h

Table 14-25921. MCASP_XEVTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED110	R	0h	

0	XDATDMA	R/W	0h	Transmit data DMA request enable bit. If Writing to this bit, always write the default value of 0.
				`0 Transmit data DMA request is enabled.`
				`1 Reserved`

14.9.1.1.2.36 MCASP_DITCSRA0 Register

1 MCASP_DITCSRA0 Register (Offset = 100h) [reset = 0h]

The DIT left channel status registers (DITCSRA0) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25922. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0100h**
MCASP1	**02B1 0100h**
MCASP2	**02B2 0100h**

Figure 14-8595. MCASP_DITCSRA0 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-25924. MCASP_DITCSRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.37 MCASP_DITCSRA1 Register

1 MCASP_DITCSRA1 Register (Offset = 104h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25925. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0104h**
MCASP1	**02B1 0104h**
MCASP2	**02B2 0104h**

Figure 14-8596. MCASP_DITCSRA1 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-25927. MCASP_DITCSRA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.38 MCASP_DITCSRA2 Register

1 MCASP_DITCSRA2 Register (Offset = 108h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25928. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0108h**
MCASP1	**02B1 0108h**
MCASP2	**02B2 0108h**

Figure 14-8597. MCASP_DITCSRA2 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-25930. MCASP_DITCSRA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.39 MCASP_DITCSRA3 Register

1 MCASP_DITCSRA3 Register (Offset = 10Ch) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25931. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 010Ch**
MCASP1	**02B1 010Ch**
MCASP2	**02B2 010Ch**

Figure 14-8598. MCASP_DITCSRA3 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-25933. MCASP_DITCSRA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.40 MCASP_DITCSRA4 Register

1 MCASP_DITCSRA4 Register (Offset = 110h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25934. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0110h**
MCASP1	**02B1 0110h**
MCASP2	**02B2 0110h**

Figure 14-8599. MCASP_DITCSRA4 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-25936. MCASP_DITCSRA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.41 MCASP_DITCSRA5 Register

1 MCASP_DITCSRA5 Register (Offset = 114h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25937. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0114h**
MCASP1	**02B1 0114h**
MCASP2	**02B2 0114h**

Figure 14-8600. MCASP_DITCSRA5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25939. MCASP_DITCSRA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.9.1.1.2.42 MCASP_DITCSRB0 Register

1 MCASP_DITCSRB0 Register (Offset = 118h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25940. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0118h**
MCASP1	**02B1 0118h**
MCASP2	**02B2 0118h**

Figure 14-8601. MCASP_DITCSRB0 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-25942. MCASP_DITCSRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.43 MCASP_DITCSRB1 Register

1 MCASP_DITCSRB1 Register (Offset = 11Ch) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25943. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 011Ch**
MCASP1	**02B1 011Ch**
MCASP2	**02B2 011Ch**

Figure 14-8602. MCASP_DITCSRB1 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-25945. MCASP_DITCSRB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.44 MCASP_DITCSRB2 Register

1 MCASP_DITCSRB2 Register (Offset = 120h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25946. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0120h**
MCASP1	**02B1 0120h**
MCASP2	**02B2 0120h**

Figure 14-8603. MCASP_DITCSRB2 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-25948. MCASP_DITCSRB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.45 MCASP_DITCSRB3 Register

1 MCASP_DITCSRB3 Register (Offset = 124h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25949. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0124h**
MCASP1	**02B1 0124h**
MCASP2	**02B2 0124h**

Figure 14-8604. MCASP_DITCSRB3 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-25951. MCASP_DITCSRB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.46 MCASP_DITCSRB4 Register

1 MCASP_DITCSRB4 Register (Offset = 128h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25952. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0128h**
MCASP1	**02B1 0128h**
MCASP2	**02B2 0128h**

Figure 14-8605. MCASP_DITCSRB4 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-25954. MCASP_DITCSRB4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.47 MCASP_DITCSRB5 Register

1 MCASP_DITCSRB5 Register (Offset = 12Ch) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-25955. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 012Ch**
MCASP1	**02B1 012Ch**
MCASP2	**02B2 012Ch**

Figure 14-8606. MCASP_DITCSRB5 Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25957. MCASP_DITCSRB5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.9.1.1.2.48 MCASP_DITUDRA0 Register

1 MCASP_DITUDRA0 Register (Offset = 130h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25958. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0130h**
MCASP1	**02B1 0130h**
MCASP2	**02B2 0130h**

Figure 14-8607. MCASP_DITUDRA0 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-25960. MCASP_DITUDRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.49 MCASP_DITUDRA1 Register

1 MCASP_DITUDRA1 Register (Offset = 134h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25961. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0134h**
MCASP1	**02B1 0134h**
MCASP2	**02B2 0134h**

Figure 14-8608. MCASP_DITUDRA1 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-25963. MCASP_DITUDRA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.50 MCASP_DITUDRA2 Register

1 MCASP_DITUDRA2 Register (Offset = 138h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25964. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0138h**
MCASP1	**02B1 0138h**
MCASP2	**02B2 0138h**

Figure 14-8609. MCASP_DITUDRA2 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DITUDRA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DITUDRA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DITUDRA							
R/W							
0h							

Table 14-25966. MCASP_DITUDRA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.51 MCASP_DITUDRA3 Register

1 MCASP_DITUDRA3 Register (Offset = 13Ch) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25967. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 013Ch**
MCASP1	**02B1 013Ch**
MCASP2	**02B2 013Ch**

Figure 14-8610. MCASP_DITUDRA3 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-25969. MCASP_DITUDRA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.52 MCASP_DITUDRA4 Register

1 MCASP_DITUDRA4 Register (Offset = 140h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25970. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0140h**
MCASP1	**02B1 0140h**
MCASP2	**02B2 0140h**

Figure 14-8611. MCASP_DITUDRA4 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-25972. MCASP_DITUDRA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.53 MCASP_DITUDRA5 Register

1 MCASP_DITUDRA5 Register (Offset = 144h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25973. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0144h**
MCASP1	**02B1 0144h**
MCASP2	**02B2 0144h**

Figure 14-8612. MCASP_DITUDRA5 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-25975. MCASP_DITUDRA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.9.1.1.2.54 MCASP_DITUDRB0 Register

1 MCASP_DITUDRB0 Register (Offset = 148h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25976. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0148h**
MCASP1	**02B1 0148h**
MCASP2	**02B2 0148h**

Figure 14-8613. MCASP_DITUDRB0 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25978. MCASP_DITUDRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.55 MCASP_DITUDRB1 Register

1 MCASP_DITUDRB1 Register (Offset = 14Ch) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25979. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 014Ch**
MCASP1	**02B1 014Ch**
MCASP2	**02B2 014Ch**

Figure 14-8614. MCASP_DITUDRB1 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25981. MCASP_DITUDRB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.56 MCASP_DITUDRB2 Register

1 MCASP_DITUDRB2 Register (Offset = 150h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25982. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0150h**
MCASP1	**02B1 0150h**
MCASP2	**02B2 0150h**

Figure 14-8615. MCASP_DITUDRB2 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25984. MCASP_DITUDRB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.57 MCASP_DITUDRB3 Register

1 MCASP_DITUDRB3 Register (Offset = 154h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25985. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0154h**
MCASP1	**02B1 0154h**
MCASP2	**02B2 0154h**

Figure 14-8616. MCASP_DITUDRB3 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25987. MCASP_DITUDRB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.58 MCASP_DITUDRB4 Register

1 MCASP_DITUDRB4 Register (Offset = 158h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25988. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0158h**
MCASP1	**02B1 0158h**
MCASP2	**02B2 0158h**

Figure 14-8617. MCASP_DITUDRB4 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25990. MCASP_DITUDRB4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.59 MCASP_DITUDRB5 Register

1 MCASP_DITUDRB5 Register (Offset = 15Ch) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-25991. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 015Ch**
MCASP1	**02B1 015Ch**
MCASP2	**02B2 015Ch**

Figure 14-8618. MCASP_DITUDRB5 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-25993. MCASP_DITUDRB5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.9.1.1.2.60 MCASP_SRCTL0 Register

1 MCASP_SRCTL0 Register (Offset = 180h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-25994. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0180h**
MCASP1	**02B1 0180h**
MCASP2	**02B2 0180h**

Figure 14-8619. MCASP_SRCTL0 Name Register

31	30	29	28	27	26	25	24
RESERVED111							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED111							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED111							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED111		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-25996. MCASP_SRCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED111	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-25996. MCASP_SRCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.9.1.1.2.61 MCASP_SRCTL1 Register

1 MCASP_SRCTL1 Register (Offset = 184h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-25997. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0184h**
MCASP1	**02B1 0184h**
MCASP2	**02B2 0184h**

Figure 14-8620. MCASP_SRCTL1 Name Register

31	30	29	28	27	26	25	24
RESERVED112							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED112							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED112							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED112		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-25999. MCASP_SRCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED112	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-25999. MCASP_SRCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.9.1.1.2.62 MCASP_SRCTL2 Register

1 MCASP_SRCTL2 Register (Offset = 188h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26000. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0188h**
MCASP1	**02B1 0188h**
MCASP2	**02B2 0188h**

Figure 14-8621. MCASP_SRCTL2 Name Register

31	30	29	28	27	26	25	24
RESERVED113							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED113							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED113							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED113		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26002. MCASP_SRCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED113	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26002. MCASP_SRCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.63 MCASP_SRCTL3 Register

1 MCASP_SRCTL3 Register (Offset = 18Ch) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26003. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 018Ch**
MCASP1	**02B1 018Ch**
MCASP2	**02B2 018Ch**

Figure 14-8622. MCASP_SRCTL3 Name Register

31	30	29	28	27	26	25	24
RESERVED114							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED114							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED114							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED114		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26005. MCASP_SRCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED114	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-26005. MCASP_SRCTL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.64 MCASP_SRCTL4 Register

1 MCASP_SRCTL4 Register (Offset = 190h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26006. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0190h**
MCASP1	**02B1 0190h**
MCASP2	**02B2 0190h**

Figure 14-8623. MCASP_SRCTL4 Name Register

31	30	29	28	27	26	25	24
RESERVED115							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED115							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED115							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED115		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26008. MCASP_SRCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED115	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26008. MCASP_SRCTL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.65 MCASP_SRCTL5 Register

1 MCASP_SRCTL5 Register (Offset = 194h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26009. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0194h**
MCASP1	**02B1 0194h**
MCASP2	**02B2 0194h**

Figure 14-8624. MCASP_SRCTL5 Name Register

31	30	29	28	27	26	25	24
RESERVED116							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED116							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED116							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED116		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26011. MCASP_SRCTL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED116	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26011. MCASP_SRCTL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.9.1.1.2.66 MCASP_SRCTL6 Register

1 MCASP_SRCTL6 Register (Offset = 198h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26012. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0198h**
MCASP1	**02B1 0198h**
MCASP2	**02B2 0198h**

Figure 14-8625. MCASP_SRCTL6 Name Register

31	30	29	28	27	26	25	24
RESERVED117							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED117							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED117							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED117		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26014. MCASP_SRCTL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED117	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26014. MCASP_SRCTL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.67 MCASP_SRCTL7 Register

1 MCASP_SRCTL7 Register (Offset = 19Ch) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26015. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 019Ch**
MCASP1	**02B1 019Ch**
MCASP2	**02B2 019Ch**

Figure 14-8626. MCASP_SRCTL7 Name Register

31	30	29	28	27	26	25	24
RESERVED118							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED118							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED118							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED118		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26017. MCASP_SRCTL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED118	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0` `Receive buffer (RBUF) is empty.`
				`1` `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26017. MCASP_SRCTL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.68 MCASP_SRCTL8 Register

1 MCASP_SRCTL8 Register (Offset = 1A0h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26018. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01A0h**
MCASP1	**02B1 01A0h**
MCASP2	**02B2 01A0h**

Figure 14-8627. MCASP_SRCTL8 Name Register

31	30	29	28	27	26	25	24
RESERVED119							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED119							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED119							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED119		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26020. MCASP_SRCTL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED119	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26020. MCASP_SRCTL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.69 MCASP_SRCTL9 Register

1 MCASP_SRCTL9 Register (Offset = 1A4h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26021. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01A4h**
MCASP1	**02B1 01A4h**
MCASP2	**02B2 01A4h**

Figure 14-8628. MCASP_SRCTL9 Name Register

31	30	29	28	27	26	25	24
RESERVED120							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED120							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED120							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED120		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26023. MCASP_SRCTL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED120	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-26023. MCASP_SRCTL9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.70 MCASP_SRCTL10 Register

1 MCASP_SRCTL10 Register (Offset = 1A8h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26024. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01A8h**
MCASP1	**02B1 01A8h**
MCASP2	**02B2 01A8h**

Figure 14-8629. MCASP_SRCTL10 Name Register

31	30	29	28	27	26	25	24
RESERVED121							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED121							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED121							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED121		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26026. MCASP_SRCTL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED121	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-26026. MCASP_SRCTL10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.71 MCASP_SRCTL11 Register

1 MCASP_SRCTL11 Register (Offset = 1ACh) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26027. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01ACh**
MCASP1	**02B1 01ACh**
MCASP2	**02B2 01ACh**

Figure 14-8630. MCASP_SRCTL11 Name Register

31	30	29	28	27	26	25	24
RESERVED122							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED122							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED122							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED122		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26029. MCASP_SRCTL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED122	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26029. MCASP_SRCTL11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.9.1.1.2.72 MCASP_SRCTL12 Register

1 MCASP_SRCTL12 Register (Offset = 1B0h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26030. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01B0h**
MCASP1	**02B1 01B0h**
MCASP2	**02B2 01B0h**

Figure 14-8631. MCASP_SRCTL12 Name Register

31	30	29	28	27	26	25	24
RESERVED123							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED123							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED123							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED123		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26032. MCASP_SRCTL12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED123	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-26032. MCASP_SRCTL12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.73 MCASP_SRCTL13 Register

1 MCASP_SRCTL13 Register (Offset = 1B4h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26033. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01B4h**
MCASP1	**02B1 01B4h**
MCASP2	**02B2 01B4h**

Figure 14-8632. MCASP_SRCTL13 Name Register

31	30	29	28	27	26	25	24
RESERVED124							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED124							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED124							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED124		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26035. MCASP_SRCTL13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED124	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26035. MCASP_SRCTL13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.74 MCASP_SRCTL14 Register

1 MCASP_SRCTL14 Register (Offset = 1B8h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26036. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01B8h**
MCASP1	**02B1 01B8h**
MCASP2	**02B2 01B8h**

Figure 14-8633. MCASP_SRCTL14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED125</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED125</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED125</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED125</td><td>RRDY</td><td>XRDY</td><td colspan="2">DISMOD</td><td colspan="2">SRMOD</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-26038. MCASP_SRCTL14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED125	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26038. MCASP_SRCTL14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.9.1.1.2.75 MCASP_SRCTL15 Register

1 MCASP_SRCTL15 Register (Offset = 1BCh) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-26039. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 01BCh**
MCASP1	**02B1 01BCh**
MCASP2	**02B2 01BCh**

Figure 14-8634. MCASP_SRCTL15 Name Register

31	30	29	28	27	26	25	24
RESERVED126							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED126							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED126							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED126		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-26041. MCASP_SRCTL15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED126	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-26041. MCASP_SRCTL15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.9.1.1.2.76 MCASP_XBUF0 Register

1 MCASP_XBUF0 Register (Offset = 200h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26042. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0200h**
MCASP1	**02B1 0200h**
MCASP2	**02B2 0200h**

Figure 14-8635. MCASP_XBUF0 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26044. MCASP_XBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.77 MCASP_XBUF1 Register

1 MCASP_XBUF1 Register (Offset = 204h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26045. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0204h**
MCASP1	**02B1 0204h**
MCASP2	**02B2 0204h**

Figure 14-8636. MCASP_XBUF1 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26047. MCASP_XBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.78 MCASP_XBUF2 Register

1 MCASP_XBUF2 Register (Offset = 208h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26048. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0208h**
MCASP1	**02B1 0208h**
MCASP2	**02B2 0208h**

Figure 14-8637. MCASP_XBUF2 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26050. MCASP_XBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.79 MCASP_XBUF3 Register

1 MCASP_XBUF3 Register (Offset = 20Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26051. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 020Ch**
MCASP1	**02B1 020Ch**
MCASP2	**02B2 020Ch**

Figure 14-8638. MCASP_XBUF3 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26053. MCASP_XBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.80 MCASP_XBUF4 Register

1 MCASP_XBUF4 Register (Offset = 210h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26054. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0210h**
MCASP1	**02B1 0210h**
MCASP2	**02B2 0210h**

Figure 14-8639. MCASP_XBUF4 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26056. MCASP_XBUF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.81 MCASP_XBUF5 Register

1 MCASP_XBUF5 Register (Offset = 214h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26057. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0214h**
MCASP1	**02B1 0214h**
MCASP2	**02B2 0214h**

Figure 14-8640. MCASP_XBUF5 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26059. MCASP_XBUF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.82 MCASP_XBUF6 Register

1 MCASP_XBUF6 Register (Offset = 218h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26060. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0218h**
MCASP1	**02B1 0218h**
MCASP2	**02B2 0218h**

Figure 14-8641. MCASP_XBUF6 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26062. MCASP_XBUF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.83 MCASP_XBUF7 Register

1 MCASP_XBUF7 Register (Offset = 21Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26063. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 021Ch**
MCASP1	**02B1 021Ch**
MCASP2	**02B2 021Ch**

Figure 14-8642. MCASP_XBUF7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26065. MCASP_XBUF7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.84 MCASP_XBUF8 Register

1 MCASP_XBUF8 Register (Offset = 220h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26066. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0220h**
MCASP1	**02B1 0220h**
MCASP2	**02B2 0220h**

Figure 14-8643. MCASP_XBUF8 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26068. MCASP_XBUF8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.85 MCASP_XBUF9 Register

1 MCASP_XBUF9 Register (Offset = 224h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26069. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0224h**
MCASP1	**02B1 0224h**
MCASP2	**02B2 0224h**

Figure 14-8644. MCASP_XBUF9 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26071. MCASP_XBUF9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.86 MCASP_XBUF10 Register

1 MCASP_XBUF10 Register (Offset = 228h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26072. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0228h**
MCASP1	**02B1 0228h**
MCASP2	**02B2 0228h**

Figure 14-8645. MCASP_XBUF10 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26074. MCASP_XBUF10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.87 MCASP_XBUF11 Register

1 MCASP_XBUF11 Register (Offset = 22Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26075. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 022Ch**
MCASP1	**02B1 022Ch**
MCASP2	**02B2 022Ch**

Figure 14-8646. MCASP_XBUF11 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26077. MCASP_XBUF11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.88 MCASP_XBUF12 Register

1 MCASP_XBUF12 Register (Offset = 230h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26078. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0230h**
MCASP1	**02B1 0230h**
MCASP2	**02B2 0230h**

Figure 14-8647. MCASP_XBUF12 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26080. MCASP_XBUF12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.89 MCASP_XBUF13 Register

1 MCASP_XBUF13 Register (Offset = 234h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26081. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0234h**
MCASP1	**02B1 0234h**
MCASP2	**02B2 0234h**

Figure 14-8648. MCASP_XBUF13 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26083. MCASP_XBUF13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.90 MCASP_XBUF14 Register

1 MCASP_XBUF14 Register (Offset = 238h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26084. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0238h**
MCASP1	**02B1 0238h**
MCASP2	**02B2 0238h**

Figure 14-8649. MCASP_XBUF14 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26086. MCASP_XBUF14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.91 MCASP_XBUF15 Register

1 MCASP_XBUF15 Register (Offset = 23Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-26087. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 023Ch**
MCASP1	**02B1 023Ch**
MCASP2	**02B2 023Ch**

Figure 14-8650. MCASP_XBUF15 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-26089. MCASP_XBUF15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.9.1.1.2.92 MCASP_RBUF0 Register

1 MCASP_RBUF0 Register (Offset = 280h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26090. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0280h**
MCASP1	**02B1 0280h**
MCASP2	**02B2 0280h**

Figure 14-8651. MCASP_RBUF0 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-26092. MCASP_RBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.93 MCASP_RBUF1 Register

1 MCASP_RBUF1 Register (Offset = 284h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26093. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0284h**
MCASP1	**02B1 0284h**
MCASP2	**02B2 0284h**

Figure 14-8652. MCASP_RBUF1 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-26095. MCASP_RBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.94 MCASP_RBUF2 Register

1 MCASP_RBUF2 Register (Offset = 288h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26096. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0288h**
MCASP1	**02B1 0288h**
MCASP2	**02B2 0288h**

Figure 14-8653. MCASP_RBUF2 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26098. MCASP_RBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.95 MCASP_RBUF3 Register

1 MCASP_RBUF3 Register (Offset = 28Ch) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26099. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 028Ch**
MCASP1	**02B1 028Ch**
MCASP2	**02B2 028Ch**

Figure 14-8654. MCASP_RBUF3 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26101. MCASP_RBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.96 MCASP_RBUF4 Register

1 MCASP_RBUF4 Register (Offset = 290h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26102. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0290h**
MCASP1	**02B1 0290h**
MCASP2	**02B2 0290h**

Figure 14-8655. MCASP_RBUF4 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26104. MCASP_RBUF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.97 MCASP_RBUF5 Register

1 MCASP_RBUF5 Register (Offset = 294h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26105. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0294h**
MCASP1	**02B1 0294h**
MCASP2	**02B2 0294h**

Figure 14-8656. MCASP_RBUF5 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-26107. MCASP_RBUF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.98 MCASP_RBUF6 Register

1 MCASP_RBUF6 Register (Offset = 298h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26108. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 0298h**
MCASP1	**02B1 0298h**
MCASP2	**02B2 0298h**

Figure 14-8657. MCASP_RBUF6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26110. MCASP_RBUF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.99 MCASP_RBUF7 Register

1 MCASP_RBUF7 Register (Offset = 29Ch) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26111. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 029Ch**
MCASP1	**02B1 029Ch**
MCASP2	**02B2 029Ch**

Figure 14-8658. MCASP_RBUF7 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26113. MCASP_RBUF7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.100 MCASP_RBUF8 Register

1 MCASP_RBUF8 Register (Offset = 2A0h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26114. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02A0h**
MCASP1	**02B1 02A0h**
MCASP2	**02B2 02A0h**

Figure 14-8659. MCASP_RBUF8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26116. MCASP_RBUF8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.101 MCASP_RBUF9 Register

1 MCASP_RBUF9 Register (Offset = 2A4h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26117. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02A4h**
MCASP1	**02B1 02A4h**
MCASP2	**02B2 02A4h**

Figure 14-8660. MCASP_RBUF9 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-26119. MCASP_RBUF9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.102 MCASP_RBUF10 Register

1 MCASP_RBUF10 Register (Offset = 2A8h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26120. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02A8h**
MCASP1	**02B1 02A8h**
MCASP2	**02B2 02A8h**

Figure 14-8661. MCASP_RBUF10 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26122. MCASP_RBUF10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.103 MCASP_RBUF11 Register

1 MCASP_RBUF11 Register (Offset = 2ACh) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26123. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02ACh**
MCASP1	**02B1 02ACh**
MCASP2	**02B2 02ACh**

Figure 14-8662. MCASP_RBUF11 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26125. MCASP_RBUF11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.104 MCASP_RBUF12 Register

1 MCASP_RBUF12 Register (Offset = 2B0h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26126. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02B0h**
MCASP1	**02B1 02B0h**
MCASP2	**02B2 02B0h**

Figure 14-8663. MCASP_RBUF12 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-26128. MCASP_RBUF12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.105 MCASP_RBUF13 Register

1 MCASP_RBUF13 Register (Offset = 2B4h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26129. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02B4h**
MCASP1	**02B1 02B4h**
MCASP2	**02B2 02B4h**

Figure 14-8664. MCASP_RBUF13 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26131. MCASP_RBUF13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.106 MCASP_RBUF14 Register

1 MCASP_RBUF14 Register (Offset = 2B8h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26132. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02B8h**
MCASP1	**02B1 02B8h**
MCASP2	**02B2 02B8h**

Figure 14-8665. MCASP_RBUF14 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26134. MCASP_RBUF14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.107 MCASP_RBUF15 Register

1 MCASP_RBUF15 Register (Offset = 2BCh) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-26135. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 02BCh**
MCASP1	**02B1 02BCh**
MCASP2	**02B2 02BCh**

Figure 14-8666. MCASP_RBUF15 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-26137. MCASP_RBUF15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.9.1.1.2.108 MCASP_WFIFOCTL Register

1 MCASP_WFIFOCTL Register (Offset = 1000h) [reset = 1004h]

The WNUMEVT and WNUMDMA values must be set prior to enabling the Write FIFO. If the Write FIFO is to be enabled, it must be enabled prior to taking the McASP out of reset

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Table 14-26138. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 1000h**
MCASP1	**02B1 1000h**
MCASP2	**02B2 1000h**

Figure 14-8667. MCASP_WFIFOCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED127</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED127</td><td>WENA</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">WNUMEVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WNUMDMA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-26140. MCASP_WFIFOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED127	R	0h	
16	WENA	R/W	0h	Write FIFO enable bit. 0 Write FIFO is disabled. The WLVL bit in the Write FIFO status register (WFIFOSTS) is reset to 0 and pointers are initialized, that is, the Write FIFO is flushed. 1 Write FIFO is enabled. If Write FIFO is to be enabled, it must be enabled prior to taking McASP out of reset.
15:8	WNUMEVT	R/W	10h	Write word count per DMA event [32 bit]. When the Write FIFO has space for at least WNUMEVT words of data, then an AXEVT [transmit DMA event] is generated to the host/DMA controller. This value should be set to a non-zero integer multiple of the number of serializers enabled as transmitters. This value must be set prior to enabling the Write FIFO. 416h = 3 to 64 words from 3h to 416h. FFh = Reserved from 41h to FFh. 0 0 words 1 1 word 2 2 words 3 3 to 64 words from 3h to 40h. 65 Reserved from 41h to FFh.

Table 14-26140. MCASP_WFIFOCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	WNUMDMA	R/W	4h	Write word count per transfer [32 bit words]. Upon a transmit DMA event from the McASP, WNUMDMA words are transferred from the Write FIFO to the McASP. This value must equal the number of McASP serializers used as transmitters. This value must be set prior to enabling the Write FIFO. FFh = Reserved from 11h to FFh. 0 0 words 1 1 word 2 2 words 3 3-16 words from 3h to 10h. 17 Reserved from 11h to FFh.

14.9.1.1.2.109 MCASP_WFIFOSTS Register

1 MCASP_WFIFOSTS Register (Offset = 1004h) [reset = 0h]

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Table 14-26141. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 1004h**
MCASP1	**02B1 1004h**
MCASP2	**02B2 1004h**

Figure 14-8668. MCASP_WFIFOSTS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED128</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED128</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED128</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WLVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26143. MCASP_WFIFOSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED128	R	0h	
7:0	WLVL	R	0h	Write level [read-only]. Number of 32 bit words currently in the Write FIFO. 40h = 3 to 64 words currently in Write FIFO from 3h to 40h. FFh = Reserved from 41h to FFh. 0 0 words currently in Write FIFO. 1 1 word currently in Write FIFO. 2 2 words currently in Write FIFO. 3 3 to 64 words currently in Write FIFO from 3h to 40h. 65 Reserved from 41h to FFh.

14.9.1.1.2.110 MCASP_RFIFOCTL Register

1 MCASP_RFIFOCTL Register (Offset = 1008h) [reset = 1004h]

The RNUMEVT and RNUMDMA values must be set prior to enabling the Read FIFO. If the Read FIFO is to be enabled, it must be enabled prior to taking the McASP out of reset

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Table 14-26144. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 1008h**
MCASP1	**02B1 1008h**
MCASP2	**02B2 1008h**

Figure 14-8669. MCASP_RFIFOCTL Name Register

31	30	29	28	27	26	25	24
RESERVED129							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED129							RENA
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RNUMEVT							
R/W							
10h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RNUMDMA							
R/W							
4h							

Table 14-26146. MCASP_RFIFOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED129	R	0h	
16	RENA	R/W	0h	Read FIFO enable bit. 0 `Read FIFO is disabled. The RLVL bit in the Read FIFO status register (RFIFOSTS) is reset to 0 and pointers are initialized, that is, the Read FIFO is flushed.` 1 `Read FIFO is enabled. If Read FIFO is to be enabled, it must be enabled prior to taking McASP out of reset.`
15:8	RNUMEVT	R/W	10h	Read word count per DMA event [32 bit]. When the Read FIFO contains at least RNUMEVT words of data, then an AREVT [receive DMA event] is generated to the host/DMA controller. This value should be set to a non-zero integer multiple of the number of serializers enabled as receivers. This value must be set prior to enabling the Read FIFO. 416h = 3 to 64 words from 3h to 416h. FFh = Reserved from 41h = FFh. 0 `0 words` 1 `1 word` 2 `2 words` 3 `3 to 64 words from 3h to 40h.` 65 `Reserved from 41h to FFh.`

Table 14-26146. MCASP_RFIFOCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	RNUMDMA	R/W	4h	Read word count per transfer [32 bit words]. Upon a receive DMA event from the McASP, the Read FIFO reads RNUMDMA words from the McASP. This value must equal the number of McASP serializers used as receivers. This value must be set prior to enabling the Read FIFO. 10h = 3 to 16 words from 3h to 10h. FFh = Reserved from 11h to FFh. 0 0 words 1 1 word 2 2 words 3 3 to 16 words from 3h to 10h. 17 Reserved from 11h to FFh.

14.9.1.1.2.111 MCASP_RFIFOSTS Register

1 MCASP_RFIFOSTS Register (Offset = 100Ch) [reset = 0h]

Return to Summary Table

Table 14-26147. Instance Table

Instance Name	Physical Address
MCASP0	**02B0 100Ch**
MCASP1	**02B1 100Ch**
MCASP2	**02B2 100Ch**

Figure 14-8670. MCASP_RFIFOSTS Name Register

31	30	29	28	27	26	25	24
RESERVED130							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED130							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED130							
R							
0h							
7	6	5	4	3	2	1	0
RLVL							
R							
0h							

Table 14-26149. MCASP_RFIFOSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED130	R	0h	
7:0	RLVL	R	0h	Read level [read-only]. Number of 32 bit words currently in the Read FIFO. 40h = 3 to 64 words currently in Read FIFO from 3h to 40h. FFh = Reserved from 41h to FFh. 0 0 words currently in Read FIFO. 1 1 word currently in Read FIFO. 2 2 words currently in Read FIFO. 3 3 to 64 words currently in Read FIFO from 3h to 40h. 65 Reserved from 41h to FFh.

14.9.2 General Connectivity Registers

14.9.2.1 GPIO

GPIO

14.9.2.1.1 GPIO Summaries

GPIO Summaries

Table 14-26150. GPIO Registers, Base Address=0060 0000h, Length=256

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
0h	32	GPIO_PID	0060 0000h	0060 1000h	0420 1000h
4h	32	GPIO_PCR	0060 0004h	0060 1004h	0420 1004h
8h	32	GPIO_BINTEN	0060 0008h	0060 1008h	0420 1008h
10h	32	GPIO_DIR01	0060 0010h	0060 1010h	0420 1010h
14h	32	GPIO_OUT_DATA01	0060 0014h	0060 1014h	0420 1014h
18h	32	GPIO_SET_DATA01	0060 0018h	0060 1018h	0420 1018h
1Ch	32	GPIO_CLR_DATA01	0060 001Ch	0060 101Ch	0420 101Ch
20h	32	GPIO_IN_DATA01	0060 0020h	0060 1020h	0420 1020h
24h	32	GPIO_SET_RIS_TRIG01	0060 0024h	0060 1024h	0420 1024h
28h	32	GPIO_CLR_RIS_TRIG01	0060 0028h	0060 1028h	0420 1028h
2Ch	32	GPIO_SET_FAL_TRIG01	0060 002Ch	0060 102Ch	0420 102Ch
30h	32	GPIO_CLR_FAL_TRIG01	0060 0030h	0060 1030h	0420 1030h
34h	32	GPIO_INTSTAT01	0060 0034h	0060 1034h	0420 1034h
38h	32	GPIO_DIR23	0060 0038h	0060 1038h	0420 1038h
3Ch	32	GPIO_OUT_DATA23	0060 003Ch	0060 103Ch	0420 103Ch
40h	32	GPIO_SET_DATA23	0060 0040h	0060 1040h	0420 1040h
44h	32	GPIO_CLR_DATA23	0060 0044h	0060 1044h	0420 1044h
48h	32	GPIO_IN_DATA23	0060 0048h	0060 1048h	0420 1048h
4Ch	32	GPIO_SET_RIS_TRIG23	0060 004Ch	0060 104Ch	0420 104Ch
50h	32	GPIO_CLR_RIS_TRIG23	0060 0050h	0060 1050h	0420 1050h
54h	32	GPIO_SET_FAL_TRIG23	0060 0054h	0060 1054h	0420 1054h
58h	32	GPIO_CLR_FAL_TRIG23	0060 0058h	0060 1058h	0420 1058h
5Ch	32	GPIO_INTSTAT23	0060 005Ch	0060 105Ch	0420 105Ch
60h	32	GPIO_DIR45	0060 0060h	0060 1060h	0420 1060h
64h	32	GPIO_OUT_DATA45	0060 0064h	0060 1064h	0420 1064h
68h	32	GPIO_SET_DATA45	0060 0068h	0060 1068h	0420 1068h
6Ch	32	GPIO_CLR_DATA45	0060 006Ch	0060 106Ch	0420 106Ch
70h	32	GPIO_IN_DATA45	0060 0070h	0060 1070h	0420 1070h
74h	32	GPIO_SET_RIS_TRIG45	0060 0074h	0060 1074h	0420 1074h
78h	32	GPIO_CLR_RIS_TRIG45	0060 0078h	0060 1078h	0420 1078h
7Ch	32	GPIO_SET_FAL_TRIG45	0060 007Ch	0060 107Ch	0420 107Ch
80h	32	GPIO_CLR_FAL_TRIG45	0060 0080h	0060 1080h	0420 1080h
84h	32	GPIO_INTSTAT45	0060 0084h	0060 1084h	0420 1084h
88h	32	GPIO_DIR67	0060 0088h	0060 1088h	0420 1088h
8Ch	32	GPIO_OUT_DATA67	0060 008Ch	0060 108Ch	0420 108Ch
90h	32	GPIO_SET_DATA67	0060 0090h	0060 1090h	0420 1090h
94h	32	GPIO_CLR_DATA67	0060 0094h	0060 1094h	0420 1094h

Table 14-26150. GPIO Registers, Base Address=0060 0000h, Length=256 (continued)

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
98h	32	GPIO_IN_DATA67	0060 0098h	0060 1098h	0420 1098h
9Ch	32	GPIO_SET_RIS_TRIG67	0060 009Ch	0060 109Ch	0420 109Ch
A0h	32	GPIO_CLR_RIS_TRIG67	0060 00A0h	0060 10A0h	0420 10A0h
A4h	32	GPIO_SET_FAL_TRIG67	0060 00A4h	0060 10A4h	0420 10A4h
A8h	32	GPIO_CLR_FAL_TRIG67	0060 00A8h	0060 10A8h	0420 10A8h
ACh	32	GPIO_INTSTAT67	0060 00ACh	0060 10ACh	0420 10ACh
B0h	32	GPIO_DIR8	0060 00B0h	0060 10B0h	0420 10B0h
B4h	32	GPIO_OUT_DATA8	0060 00B4h	0060 10B4h	0420 10B4h
B8h	32	GPIO_SET_DATA8	0060 00B8h	0060 10B8h	0420 10B8h
BCh	32	GPIO_CLR_DATA8	0060 00BCh	0060 10BCh	0420 10BCh
C0h	32	GPIO_IN_DATA8	0060 00C0h	0060 10C0h	0420 10C0h
C4h	32	GPIO_SET_RIS_TRIG8	0060 00C4h	0060 10C4h	0420 10C4h
C8h	32	GPIO_CLR_RIS_TRIG8	0060 00C8h	0060 10C8h	0420 10C8h
CCh	32	GPIO_SET_FAL_TRIG8	0060 00CCh	0060 10CCh	0420 10CCh
D0h	32	GPIO_CLR_FAL_TRIG8	0060 00D0h	0060 10D0h	0420 10D0h
D4h	32	GPIO_INTSTAT8	0060 00D4h	0060 10D4h	0420 10D4h

14.9.2.1.2 GPIO Registers

GPIO Registers

14.9.2.1.2.1 GPIO_PID Register

1 GPIO_PID Register (Offset = 0h) [reset = 44832905h]

GPIO Periperal ID Register

Return to Summary Table

Table 14-26151. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0000h**
GPIO1	**0060 1000h**
MCU_GPIO0	**0420 1000h**

Figure 14-8671. GPIO_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		483h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
483h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
5h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		5h					

Table 14-26153. GPIO_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Current scheme Reset Source: mod_g_srst_n
29:28	RESERVED	R	0h	RESERVED
27:16	FUNC	R	483h	Function code assigned to TCP3 Reset Source: mod_g_srst_n
15:11	RTL	R	5h	RTL Version R code Reset Source: mod_g_srst_n
10:8	MAJOR	R	1h	Major revision X code Reset Source: mod_g_srst_n
7:6	CUSTOM	R	0h	Custom version code Reset Source: mod_g_srst_n
5:0	MINOR	R	5h	Minor revision Y code Reset Source: mod_g_srst_n

14.9.2.1.2.2 GPIO_PCR Register

1 GPIO_PCR Register (Offset = 4h) [reset = 1h]

Peripheral Control Register

Return to Summary Table

Table 14-26154. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0004h**
GPIO1	**0060 1004h**
MCU_GPIO0	**0420 1004h**

Figure 14-8672. GPIO_PCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R	R
0h						0h	1h

Table 14-26156. GPIO_PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode. Reset Source: mod_g_srst_n
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend. Reset Source: mod_g_srst_n

14.9.2.1.2.3 GPIO_BINTEN Register

1 GPIO_BINTEN Register (Offset = 8h) [reset = 0h]

Bit Interrupt Enable Register

Return to Summary Table

Table 14-26157. Instance Table

Instance Name	Physical Address
GPIO0	0060 0008h
GPIO1	0060 1008h
MCU_GPIO0	0420 1008h

Figure 14-8673. GPIO_BINTEN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26159. GPIO_BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	EN	R/W	0h	Per bank interrupt enable. 0 = disable, 1 = enable. Reset Source: mod_g_srst_n

14.9.2.1.2.4 GPIO_DIR01 Register

1 GPIO_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-26160. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0010h**
GPIO1	**0060 1010h**
MCU_GPIO0	**0420 1010h**

Figure 14-8674. GPIO_DIR01 Name Register

31	30	29	28	27	26	25	24
DIR1							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR0							
R/W							
FFFFh							

Table 14-26162. GPIO_DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.2.1.2.5 GPIO_OUT_DATA01 Register

1 GPIO_OUT_DATA01 Register (Offset = 14h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-26163. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0014h**
GPIO1	**0060 1014h**
MCU_GPIO0	**0420 1014h**

Figure 14-8675. GPIO_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24
OUT1							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT1							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT0							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT0							
R/W							
0h							

Table 14-26165. GPIO_OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.6 GPIO_SET_DATA01 Register

1 GPIO_SET_DATA01 Register (Offset = 18h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-26166. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0018h**
GPIO1	**0060 1018h**
MCU_GPIO0	**0420 1018h**

Figure 14-8676. GPIO_SET_DATA01 Name Register

31	30	29	28	27	26	25	24
SET1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET0							
R/W1TS							
0h							

Table 14-26168. GPIO_SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET1	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET0	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.7 GPIO_CLR_DATA01 Register

1 GPIO_CLR_DATA01 Register (Offset = 1Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-26169. Instance Table

Instance Name	Physical Address
GPIO0	**0060 001Ch**
GPIO1	**0060 101Ch**
MCU_GPIO0	**0420 101Ch**

Figure 14-8677. GPIO_CLR_DATA01 Name Register

31	30	29	28	27	26	25	24
CLR1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR0							
R/W1TC							
0h							

Table 14-26171. GPIO_CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR1	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR0	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.8 GPIO_IN_DATA01 Register

1 GPIO_IN_DATA01 Register (Offset = 20h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-26172. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0020h**
GPIO1	**0060 1020h**
MCU_GPIO0	**0420 1020h**

Figure 14-8678. GPIO_IN_DATA01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IN1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IN1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26174. GPIO_IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN1	R	0h	Status of GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	IN0	R	0h	Status of GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.9 GPIO_SET_RIS_TRIG01 Register

1 GPIO_SET_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-26175. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0024h**
GPIO1	**0060 1024h**
MCU_GPIO0	**0420 1024h**

Figure 14-8679. GPIO_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETRIS1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS0							
R/W1TS							
0h							

Table 14-26177. GPIO_SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS1	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETRIS0	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.10 GPIO_CLR_RIS_TRIG01 Register

1 GPIO_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-26178. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0028h**
GPIO1	**0060 1028h**
MCU_GPIO0	**0420 1028h**

Figure 14-8680. GPIO_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
CLRRIS1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS0							
R/W1TC							
0h							

Table 14-26180. GPIO_CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS1	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS0	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.11 GPIO_SET_FAL_TRIG01 Register

1 GPIO_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-26181. Instance Table

Instance Name	Physical Address
GPIO0	**0060 002Ch**
GPIO1	**0060 102Ch**
MCU_GPIO0	**0420 102Ch**

Figure 14-8681. GPIO_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETFAL1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL0							
R/W1TS							
0h							

Table 14-26183. GPIO_SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL1	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETFAL0	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.12 GPIO_CLR_FAL_TRIG01 Register

1 GPIO_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-26184. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0030h**
GPIO1	**0060 1030h**
MCU_GPIO0	**0420 1030h**

Figure 14-8682. GPIO_CLR_FAL_TRIG01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26186. GPIO_CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL1	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL0	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.13 GPIO_INTSTAT01 Register

1 GPIO_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-26187. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0034h**
GPIO1	**0060 1034h**
MCU_GPIO0	**0420 1034h**

Figure 14-8683. GPIO_INTSTAT01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">STAT1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">STAT1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">STAT0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">STAT0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26189. GPIO_INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT1	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT0	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.2.1.2.14 GPIO_DIR23 Register

1 GPIO_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-26190. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0038h**
GPIO1	**0060 1038h**
MCU_GPIO0	**0420 1038h**

Figure 14-8684. GPIO_DIR23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DIR3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DIR3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DIR2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DIR2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-26192. GPIO_DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.2.1.2.15 GPIO_OUT_DATA23 Register

1 GPIO_OUT_DATA23 Register (Offset = 3Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-26193. Instance Table

Instance Name	Physical Address
GPIO0	**0060 003Ch**
GPIO1	**0060 103Ch**
MCU_GPIO0	**0420 103Ch**

Figure 14-8685. GPIO_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24
OUT3							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT3							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT2							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT2							
R/W							
0h							

Table 14-26195. GPIO_OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.16 GPIO_SET_DATA23 Register

1 GPIO_SET_DATA23 Register (Offset = 40h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-26196. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0040h**
GPIO1	**0060 1040h**
MCU_GPIO0	**0420 1040h**

Figure 14-8686. GPIO_SET_DATA23 Name Register

31	30	29	28	27	26	25	24
SET3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET2							
R/W1TS							
0h							

Table 14-26198. GPIO_SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET3	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET2	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.17 GPIO_CLR_DATA23 Register

1 GPIO_CLR_DATA23 Register (Offset = 44h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-26199. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0044h**
GPIO1	**0060 1044h**
MCU_GPIO0	**0420 1044h**

Figure 14-8687. GPIO_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24
CLR3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR2							
R/W1TC							
0h							

Table 14-26201. GPIO_CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR3	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR2	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.18 GPIO_IN_DATA23 Register

1 GPIO_IN_DATA23 Register (Offset = 48h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-26202. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0048h**
GPIO1	**0060 1048h**
MCU_GPIO0	**0420 1048h**

Figure 14-8688. GPIO_IN_DATA23 Name Register

31	30	29	28	27	26	25	24
IN3							
R							
0h							
23	22	21	20	19	18	17	16
IN3							
R							
0h							
15	14	13	12	11	10	9	8
IN2							
R							
0h							
7	6	5	4	3	2	1	0
IN2							
R							
0h							

Table 14-26204. GPIO_IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN3	R	0h	Status of GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	IN2	R	0h	Status of GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.19 GPIO_SET_RIS_TRIG23 Register

1 GPIO_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-26205. Instance Table

Instance Name	Physical Address
GPIO0	**0060 004Ch**
GPIO1	**0060 104Ch**
MCU_GPIO0	**0420 104Ch**

Figure 14-8689. GPIO_SET_RIS_TRIG23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETRIS3</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETRIS3</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETRIS2</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETRIS2</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26207. GPIO_SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS3	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETRIS2	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.20 GPIO_CLR_RIS_TRIG23 Register

1 GPIO_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-26208. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0050h**
GPIO1	**0060 1050h**
MCU_GPIO0	**0420 1050h**

Figure 14-8690. GPIO_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRRIS3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS2							
R/W1TC							
0h							

Table 14-26210. GPIO_CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS3	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS2	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.21 GPIO_SET_FAL_TRIG23 Register

1 GPIO_SET_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-26211. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0054h**
GPIO1	**0060 1054h**
MCU_GPIO0	**0420 1054h**

Figure 14-8691. GPIO_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETFAL3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL2							
R/W1TS							
0h							

Table 14-26213. GPIO_SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL3	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETFAL2	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.22 GPIO_CLR_FAL_TRIG23 Register

1 GPIO_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-26214. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0058h**
GPIO1	**0060 1058h**
MCU_GPIO0	**0420 1058h**

Figure 14-8692. GPIO_CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRFAL3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL2							
R/W1TC							
0h							

Table 14-26216. GPIO_CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL3	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL2	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.23 GPIO_INTSTAT23 Register

1 GPIO_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-26217. Instance Table

Instance Name	Physical Address
GPIO0	**0060 005Ch**
GPIO1	**0060 105Ch**
MCU_GPIO0	**0420 105Ch**

Figure 14-8693. GPIO_INTSTAT23 Name Register

31	30	29	28	27	26	25	24
STAT3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT2							
R/W1TC							
0h							

Table 14-26219. GPIO_INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT3	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT2	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.2.1.2.24 GPIO_DIR45 Register

1 GPIO_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-26220. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0060h**
GPIO1	**0060 1060h**
MCU_GPIO0	**0420 1060h**

Figure 14-8694. GPIO_DIR45 Name Register

31	30	29	28	27	26	25	24
DIR5							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR5							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR4							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR4							
R/W							
FFFFh							

Table 14-26222. GPIO_DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.2.1.2.25 GPIO_OUT_DATA45 Register

1 GPIO_OUT_DATA45 Register (Offset = 64h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-26223. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0064h**
GPIO1	**0060 1064h**
MCU_GPIO0	**0420 1064h**

Figure 14-8695. GPIO_OUT_DATA45 Name Register

31	30	29	28	27	26	25	24
OUT5							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT5							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT4							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT4							
R/W							
0h							

Table 14-26225. GPIO_OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.26 GPIO_SET_DATA45 Register

1 GPIO_SET_DATA45 Register (Offset = 68h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-26226. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0068h**
GPIO1	**0060 1068h**
MCU_GPIO0	**0420 1068h**

Figure 14-8696. GPIO_SET_DATA45 Name Register

31	30	29	28	27	26	25	24
SET5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET4							
R/W1TS							
0h							

Table 14-26228. GPIO_SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET5	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET4	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.27 GPIO_CLR_DATA45 Register

1 GPIO_CLR_DATA45 Register (Offset = 6Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-26229. Instance Table

Instance Name	Physical Address
GPIO0	**0060 006Ch**
GPIO1	**0060 106Ch**
MCU_GPIO0	**0420 106Ch**

Figure 14-8697. GPIO_CLR_DATA45 Name Register

31	30	29	28	27	26	25	24
CLR5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR4							
R/W1TC							
0h							

Table 14-26231. GPIO_CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR5	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR4	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.28 GPIO_IN_DATA45 Register

1 GPIO_IN_DATA45 Register (Offset = 70h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-26232. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0070h**
GPIO1	**0060 1070h**
MCU_GPIO0	**0420 1070h**

Figure 14-8698. GPIO_IN_DATA45 Name Register

31	30	29	28	27	26	25	24
IN5							
R							
0h							
23	22	21	20	19	18	17	16
IN5							
R							
0h							
15	14	13	12	11	10	9	8
IN4							
R							
0h							
7	6	5	4	3	2	1	0
IN4							
R							
0h							

Table 14-26234. GPIO_IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN5	R	0h	Status of GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	IN4	R	0h	Status of GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.29 GPIO_SET_RIS_TRIG45 Register

1 GPIO_SET_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-26235. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0074h**
GPIO1	**0060 1074h**
MCU_GPIO0	**0420 1074h**

Figure 14-8699. GPIO_SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
SETRIS5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS4							
R/W1TS							
0h							

Table 14-26237. GPIO_SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS5	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETRIS4	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.30 GPIO_CLR_RIS_TRIG45 Register

1 GPIO_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-26238. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0078h**
GPIO1	**0060 1078h**
MCU_GPIO0	**0420 1078h**

Figure 14-8700. GPIO_CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRRIS5							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLRRIS5							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLRRIS4							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLRRIS4							
R/W1TC							
0h							

Table 14-26240. GPIO_CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS5	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS4	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.31 GPIO_SET_FAL_TRIG45 Register

1 GPIO_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-26241. Instance Table

Instance Name	Physical Address
GPIO0	**0060 007Ch**
GPIO1	**0060 107Ch**
MCU_GPIO0	**0420 107Ch**

Figure 14-8701. GPIO_SET_FAL_TRIG45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETFAL5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETFAL5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETFAL4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETFAL4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26243. GPIO_SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL5	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETFAL4	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.32 GPIO_CLR_FAL_TRIG45 Register

1 GPIO_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-26244. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0080h**
GPIO1	**0060 1080h**
MCU_GPIO0	**0420 1080h**

Figure 14-8702. GPIO_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRFAL5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL4							
R/W1TC							
0h							

Table 14-26246. GPIO_CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL5	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL4	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.33 GPIO_INTSTAT45 Register

1 GPIO_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-26247. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0084h**
GPIO1	**0060 1084h**
MCU_GPIO0	**0420 1084h**

Figure 14-8703. GPIO_INTSTAT45 Name Register

31	30	29	28	27	26	25	24
STAT5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT4							
R/W1TC							
0h							

Table 14-26249. GPIO_INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT5	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT4	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.2.1.2.34 GPIO_DIR67 Register

1 GPIO_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-26250. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0088h**
GPIO1	**0060 1088h**
MCU_GPIO0	**0420 1088h**

Figure 14-8704. GPIO_DIR67 Name Register

31	30	29	28	27	26	25	24
DIR7							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR7							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR6							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR6							
R/W							
FFFFh							

Table 14-26252. GPIO_DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.2.1.2.35 GPIO_OUT_DATA67 Register

1 GPIO_OUT_DATA67 Register (Offset = 8Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-26253. Instance Table

Instance Name	Physical Address
GPIO0	**0060 008Ch**
GPIO1	**0060 108Ch**
MCU_GPIO0	**0420 108Ch**

Figure 14-8705. GPIO_OUT_DATA67 Name Register

31	30	29	28	27	26	25	24
OUT7							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT7							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT6							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT6							
R/W							
0h							

Table 14-26255. GPIO_OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.36 GPIO_SET_DATA67 Register

1 GPIO_SET_DATA67 Register (Offset = 90h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-26256. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0090h**
GPIO1	**0060 1090h**
MCU_GPIO0	**0420 1090h**

Figure 14-8706. GPIO_SET_DATA67 Name Register

31	30	29	28	27	26	25	24
SET7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET6							
R/W1TS							
0h							

Table 14-26258. GPIO_SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET7	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET6	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.37 GPIO_CLR_DATA67 Register

1 GPIO_CLR_DATA67 Register (Offset = 94h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-26259. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0094h**
GPIO1	**0060 1094h**
MCU_GPIO0	**0420 1094h**

Figure 14-8707. GPIO_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24
CLR7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR6							
R/W1TC							
0h							

Table 14-26261. GPIO_CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR7	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR6	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.38 GPIO_IN_DATA67 Register

1 GPIO_IN_DATA67 Register (Offset = 98h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-26262. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0098h**
GPIO1	**0060 1098h**
MCU_GPIO0	**0420 1098h**

Figure 14-8708. GPIO_IN_DATA67 Name Register

31	30	29	28	27	26	25	24
IN7							
R							
0h							
23	22	21	20	19	18	17	16
IN7							
R							
0h							
15	14	13	12	11	10	9	8
IN6							
R							
0h							
7	6	5	4	3	2	1	0
IN6							
R							
0h							

Table 14-26264. GPIO_IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN7	R	0h	Status of GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	IN6	R	0h	Status of GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.39 GPIO_SET_RIS_TRIG67 Register

1 GPIO_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-26265. Instance Table

Instance Name	Physical Address
GPIO0	**0060 009Ch**
GPIO1	**0060 109Ch**
MCU_GPIO0	**0420 109Ch**

Figure 14-8709. GPIO_SET_RIS_TRIG67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETRIS7</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETRIS7</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETRIS6</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETRIS6</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26267. GPIO_SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS7	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETRIS6	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.40 GPIO_CLR_RIS_TRIG67 Register

1 GPIO_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-26268. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A0h**
GPIO1	**0060 10A0h**
MCU_GPIO0	**0420 10A0h**

Figure 14-8710. GPIO_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRRIS7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS6							
R/W1TC							
0h							

Table 14-26270. GPIO_CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS7	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS6	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.41 GPIO_SET_FAL_TRIG67 Register

1 GPIO_SET_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-26271. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A4h**
GPIO1	**0060 10A4h**
MCU_GPIO0	**0420 10A4h**

Figure 14-8711. GPIO_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETFAL7							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETFAL7							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETFAL6							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETFAL6							
R/W1TS							
0h							

Table 14-26273. GPIO_SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL7	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETFAL6	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.42 GPIO_CLR_FAL_TRIG67 Register

1 GPIO_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-26274. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A8h**
GPIO1	**0060 10A8h**
MCU_GPIO0	**0420 10A8h**

Figure 14-8712. GPIO_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRFAL7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL6							
R/W1TC							
0h							

Table 14-26276. GPIO_CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL7	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL6	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.43 GPIO_INTSTAT67 Register

1 GPIO_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-26277. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00ACh**
GPIO1	**0060 10ACh**
MCU_GPIO0	**0420 10ACh**

Figure 14-8713. GPIO_INTSTAT67 Name Register

31	30	29	28	27	26	25	24
STAT7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT6							
R/W1TC							
0h							

Table 14-26279. GPIO_INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT7	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT6	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.2.1.2.44 GPIO_DIR8 Register

1 GPIO_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-26280. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B0h**
GPIO1	**0060 10B0h**
MCU_GPIO0	**0420 10B0h**

Figure 14-8714. GPIO_DIR8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
FFFFh							
23	22	21	20	19	18	17	16
RESERVED							
R							
FFFFh							
15	14	13	12	11	10	9	8
DIR8							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR8							
R/W							
FFFFh							

Table 14-26282. GPIO_DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	FFFFh	RESERVED
15:0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.2.1.2.45 GPIO_OUT_DATA8 Register

1 GPIO_OUT_DATA8 Register (Offset = B4h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-26283. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B4h**
GPIO1	**0060 10B4h**
MCU_GPIO0	**0420 10B4h**

Figure 14-8715. GPIO_OUT_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
OUT8							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT8							
R/W							
0h							

Table 14-26285. GPIO_OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.46 GPIO_SET_DATA8 Register

1 GPIO_SET_DATA8 Register (Offset = B8h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-26286. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B8h**
GPIO1	**0060 10B8h**
MCU_GPIO0	**0420 10B8h**

Figure 14-8716. GPIO_SET_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
SET8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET8							
R/W1TS							
0h							

Table 14-26288. GPIO_SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	SET8	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.47 GPIO_CLR_DATA8 Register

1 GPIO_CLR_DATA8 Register (Offset = BCh) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-26289. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00BCh**
GPIO1	**0060 10BCh**
MCU_GPIO0	**0420 10BCh**

Figure 14-8717. GPIO_CLR_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CLR8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR8							
R/W1TC							
0h							

Table 14-26291. GPIO_CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	CLR8	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.2.1.2.48 GPIO_IN_DATA8 Register

1 GPIO_IN_DATA8 Register (Offset = C0h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-26292. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C0h**
GPIO1	**0060 10C0h**
MCU_GPIO0	**0420 10C0h**

Figure 14-8718. GPIO_IN_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IN8							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IN8							
R							
0h							

Table 14-26294. GPIO_IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	IN8	R	0h	Status of GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.49 GPIO_SET_RIS_TRIG8 Register

1 GPIO_SET_RIS_TRIG8 Register (Offset = C4h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-26295. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C4h**
GPIO1	**0060 10C4h**
MCU_GPIO0	**0420 10C4h**

Figure 14-8719. GPIO_SET_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETRIS8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS8							
R/W1TS							
0h							

Table 14-26297. GPIO_SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETRIS8	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.50 GPIO_CLR_RIS_TRIG8 Register

1 GPIO_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-26298. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C8h**
GPIO1	**0060 10C8h**
MCU_GPIO0	**0420 10C8h**

Figure 14-8720. GPIO_CLR_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRRIS8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS8							
R/W1TC							
0h							

Table 14-26300. GPIO_CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRRIS8	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.51 GPIO_SET_FAL_TRIG8 Register

1 GPIO_SET_FAL_TRIG8 Register (Offset = CCh) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-26301. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00CCh**
GPIO1	**0060 10CCh**
MCU_GPIO0	**0420 10CCh**

Figure 14-8721. GPIO_SET_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETFAL8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL8							
R/W1TS							
0h							

Table 14-26303. GPIO_SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETFAL8	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.52 GPIO_CLR_FAL_TRIG8 Register

1 GPIO_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-26304. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00D0h**
GPIO1	**0060 10D0h**
MCU_GPIO0	**0420 10D0h**

Figure 14-8722. GPIO_CLR_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRFAL8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL8							
R/W1TC							
0h							

Table 14-26306. GPIO_CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRFAL8	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.2.1.2.53 GPIO_INTSTAT8 Register

1 GPIO_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-26307. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00D4h**
GPIO1	**0060 10D4h**
MCU_GPIO0	**0420 10D4h**

Figure 14-8723. GPIO_INTSTAT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAT8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT8							
R/W1TC							
0h							

Table 14-26309. GPIO_INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	STAT8	R/W1TC	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.2.2 I2C

I2C

14.9.2.2.1 I2C Summaries

I2C Summaries

Table 14-26310. I2C Registers, Base Address=2000 0000h, Length=256

Offset	Length	Register Name	I2C0 Physical Address	I2C1 Physical Address	I2C2 Physical Address
0h	32	I2C_REVNB_LO	2000 0000h	2001 0000h	2002 0000h
4h	32	I2C_REVNB_HI	2000 0004h	2001 0004h	2002 0004h
10h	32	I2C_SYSC	2000 0010h	2001 0010h	2002 0010h
20h	32	I2C_EOI	2000 0020h	2001 0020h	2002 0020h
24h	32	I2C_IRQSTATUS_RAW	2000 0024h	2001 0024h	2002 0024h
28h	32	I2C_IRQSTATUS	2000 0028h	2001 0028h	2002 0028h
2Ch	32	I2C_IRQENABLE_SET	2000 002Ch	2001 002Ch	2002 002Ch
30h	32	I2C_IRQENABLE_CLR	2000 0030h	2001 0030h	2002 0030h
34h	32	I2C_WE	2000 0034h	2001 0034h	2002 0034h
38h	32	I2C_DMARXENABLE_SET	2000 0038h	2001 0038h	2002 0038h
3Ch	32	I2C_DMATXENABLE_SET	2000 003Ch	2001 003Ch	2002 003Ch
40h	32	I2C_DMARXENABLE_CLR	2000 0040h	2001 0040h	2002 0040h
44h	32	I2C_DMATXENABLE_CLR	2000 0044h	2001 0044h	2002 0044h
48h	32	I2C_DMARXWAKE_EN	2000 0048h	2001 0048h	2002 0048h
4Ch	32	I2C_DMATXWAKE_EN	2000 004Ch	2001 004Ch	2002 004Ch
84h	32	I2C_IE	2000 0084h	2001 0084h	2002 0084h
88h	32	I2C_STAT	2000 0088h	2001 0088h	2002 0088h
90h	32	I2C_SYSS	2000 0090h	2001 0090h	2002 0090h
94h	32	I2C_BUF	2000 0094h	2001 0094h	2002 0094h
98h	32	I2C_CNT	2000 0098h	2001 0098h	2002 0098h
9Ch	32	I2C_DATA	2000 009Ch	2001 009Ch	2002 009Ch
A4h	32	I2C_CON	2000 00A4h	2001 00A4h	2002 00A4h
A8h	32	I2C_OA	2000 00A8h	2001 00A8h	2002 00A8h
ACh	32	I2C_SA	2000 00ACh	2001 00ACh	2002 00ACh
B0h	32	I2C_PSC	2000 00B0h	2001 00B0h	2002 00B0h
B4h	32	I2C_SCLL	2000 00B4h	2001 00B4h	2002 00B4h
B8h	32	I2C_SCLH	2000 00B8h	2001 00B8h	2002 00B8h
BCh	32	I2C_SYSTEST	2000 00BCh	2001 00BCh	2002 00BCh
C0h	32	I2C_BUFSTAT	2000 00C0h	2001 00C0h	2002 00C0h
C4h	32	I2C_OA1	2000 00C4h	2001 00C4h	2002 00C4h
C8h	32	I2C_OA2	2000 00C8h	2001 00C8h	2002 00C8h
CCh	32	I2C_OA3	2000 00CCh	2001 00CCh	2002 00CCh
D0h	32	I2C_ACTOA	2000 00D0h	2001 00D0h	2002 00D0h
D4h	32	I2C_SBLOCK	2000 00D4h	2001 00D4h	2002 00D4h

Table 14-26311. I2C Registers, Base Address=2000 0000h, Length=256

Offset	Length	Register Name	I2C3 Physical Address	MCU_I2C0 Physical Address	WKUP_I2C0 Physical Address
0h	32	I2C_REVNB_LO	2003 0000h	0490 0000h	2B20 0000h
4h	32	I2C_REVNB_HI	2003 0004h	0490 0004h	2B20 0004h
10h	32	I2C_SYSC	2003 0010h	0490 0010h	2B20 0010h
20h	32	I2C_EOI	2003 0020h	0490 0020h	2B20 0020h
24h	32	I2C_IRQSTATUS_RAW	2003 0024h	0490 0024h	2B20 0024h
28h	32	I2C_IRQSTATUS	2003 0028h	0490 0028h	2B20 0028h
2Ch	32	I2C_IRQENABLE_SET	2003 002Ch	0490 002Ch	2B20 002Ch
30h	32	I2C_IRQENABLE_CLR	2003 0030h	0490 0030h	2B20 0030h
34h	32	I2C_WE	2003 0034h	0490 0034h	2B20 0034h
38h	32	I2C_DMARXENABLE_SET	2003 0038h	0490 0038h	2B20 0038h
3Ch	32	I2C_DMATXENABLE_SET	2003 003Ch	0490 003Ch	2B20 003Ch
40h	32	I2C_DMARXENABLE_CLR	2003 0040h	0490 0040h	2B20 0040h
44h	32	I2C_DMATXENABLE_CLR	2003 0044h	0490 0044h	2B20 0044h
48h	32	I2C_DMARXWAKE_EN	2003 0048h	0490 0048h	2B20 0048h
4Ch	32	I2C_DMATXWAKE_EN	2003 004Ch	0490 004Ch	2B20 004Ch
84h	32	I2C_IE	2003 0084h	0490 0084h	2B20 0084h
88h	32	I2C_STAT	2003 0088h	0490 0088h	2B20 0088h
90h	32	I2C_SYSS	2003 0090h	0490 0090h	2B20 0090h
94h	32	I2C_BUF	2003 0094h	0490 0094h	2B20 0094h
98h	32	I2C_CNT	2003 0098h	0490 0098h	2B20 0098h
9Ch	32	I2C_DATA	2003 009Ch	0490 009Ch	2B20 009Ch
A4h	32	I2C_CON	2003 00A4h	0490 00A4h	2B20 00A4h
A8h	32	I2C_OA	2003 00A8h	0490 00A8h	2B20 00A8h
ACh	32	I2C_SA	2003 00ACh	0490 00ACh	2B20 00ACh
B0h	32	I2C_PSC	2003 00B0h	0490 00B0h	2B20 00B0h
B4h	32	I2C_SCLL	2003 00B4h	0490 00B4h	2B20 00B4h
B8h	32	I2C_SCLH	2003 00B8h	0490 00B8h	2B20 00B8h
BCh	32	I2C_SYSTEST	2003 00BCh	0490 00BCh	2B20 00BCh
C0h	32	I2C_BUFSTAT	2003 00C0h	0490 00C0h	2B20 00C0h
C4h	32	I2C_OA1	2003 00C4h	0490 00C4h	2B20 00C4h
C8h	32	I2C_OA2	2003 00C8h	0490 00C8h	2B20 00C8h
CCh	32	I2C_OA3	2003 00CCh	0490 00CCh	2B20 00CCh
D0h	32	I2C_ACTOA	2003 00D0h	0490 00D0h	2B20 00D0h
D4h	32	I2C_SBLOCK	2003 00D4h	0490 00D4h	2B20 00D4h

14.9.2.2.2 I2C Registers

I2C Registers

14.9.2.2.2.1 I2C_REVNB_LO Register

1 I2C_REVNB_LO Register (Offset = 0h) [reset = 80Ch]

Revision Number register (Low)

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Table 14-26312. Instance Table

Instance Name	Physical Address
I2C0	**2000 0000h**
I2C1	**2001 0000h**
I2C2	**2002 0000h**
I2C3	**2003 0000h**
MCU_I2C0	**0490 0000h**
WKUP_I2C0	**2B20 0000h**

Figure 14-8724. I2C_REVNB_LO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
1h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		Ch					

Table 14-26314. I2C_REVNB_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:11	RTL	R	1h	RTL version This field changes on bug fix, and resets to
10:8	MAJOR	R	0h	Major Revision This field changes when there is a major feature change This field does not change due to bug fix, or minor feature change
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers 0 if non-custom
5:0	MINOR	R	Ch	Minor Revision This field changes when features are scaled up or down This field does not change due to bug fix, or major feature change

14.9.2.2.2.2 I2C_REVNB_HI Register

1 I2C_REVNB_HI Register (Offset = 4h) [reset = 5040h]

Revision Number register (High)

Return to Summary Table

Table 14-26315. Instance Table

Instance Name	Physical Address
I2C0	**2000 0004h**
I2C1	**2001 0004h**
I2C2	**2002 0004h**
I2C3	**2003 0004h**
MCU_I2C0	**0490 0004h**
WKUP_I2C0	**2B20 0004h**

Figure 14-8725. I2C_REVNB_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SCHEME		RESERVED		FUNC			
R		R		R			
1h		1h		40h			
7	6	5	4	3	2	1	0
FUNC							
R							
40h							

Table 14-26317. I2C_REVNB_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:14	SCHEME	R	1h	Used to distinguish between old Scheme and current Spare bit to encode future schemes
13:12	RESERVED	R	1h	Reads return 0x1
11:0	FUNC	R	40h	Function: Indicates a software compatible module family

14.9.2.2.2.3 I2C_SYSC Register

1 I2C_SYSC Register (Offset = 10h) [reset = 1h]

System Configuration register

Return to Summary Table

Table 14-26318. Instance Table

Instance Name	Physical Address
I2C0	**2000 0010h**
I2C1	**2001 0010h**
I2C2	**2002 0010h**
I2C3	**2003 0010h**
MCU_I2C0	**0490 0010h**
WKUP_I2C0	**2B20 0010h**

Figure 14-8726. I2C_SYSC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">CLKACTIVITY</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">IDLEMODE</td><td>ENAWAKEUP</td><td>SRST</td><td>AUTOIDLE</td></tr>
<tr><td colspan="3">R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-26320. I2C_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED1	R	0h	Reserved
9:8	CLKACTIVITY	R/W	0h	Clock Activity selection bits
7:5	RESERVED	R	0h	Reads return 0
4:3	IDLEMODE	R/W	0h	Idle Mode selection bits
2	ENAWAKEUP	R/W	0h	Enable Wakeup control bit
1	SRST	R/W	0h	SoftReset bit
0	AUTOIDLE	R/W	1h	Autoidle bit

14.9.2.2.2.4 I2C_EOI Register

1 I2C_EOI Register (Offset = 20h) [reset = 0h]

End Of Interrupt number specification

Return to Summary Table

Table 14-26321. Instance Table

Instance Name	Physical Address
I2C0	**2000 0020h**
I2C1	**2001 0020h**
I2C2	**2002 0020h**
I2C3	**2003 0020h**
MCU_I2C0	**0490 0020h**
WKUP_I2C0	**2B20 0020h**

Figure 14-8727. I2C_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINE_NUMBER
R							W
0h							0h

Table 14-26323. I2C_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	LINE_NUMBER	W	0h	Software End Of Interrupt [EOI] control Write number of interrupt output

14.9.2.2.2.5 I2C_IRQSTATUS_RAW Register

1 I2C_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

Per-event raw interrupt status vector

Return to Summary Table

Table 14-26324. Instance Table

Instance Name	Physical Address
I2C0	**2000 0024h**
I2C1	**2001 0024h**
I2C2	**2002 0024h**
I2C3	**2003 0024h**
MCU_I2C0	**0490 0024h**
WKUP_I2C0	**2B20 0024h**

Figure 14-8728. I2C_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26326. I2C_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status
5	GC	R/W1C	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-26326. I2C_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W1C	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W1C	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W1C	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W1C	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.9.2.2.2.6 I2C_IRQSTATUS Register

1 I2C_IRQSTATUS Register (Offset = 28h) [reset = 0h]

Per-event enabled interrupt status vector

Return to Summary Table

Table 14-26327. Instance Table

Instance Name	Physical Address
I2C0	**2000 0028h**
I2C1	**2001 0028h**
I2C2	**2002 0028h**
I2C3	**2003 0028h**
MCU_I2C0	**0490 0028h**
WKUP_I2C0	**2B20 0028h**

Figure 14-8729. I2C_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26329. I2C_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ enabled status
13	RDR	R/W	0h	Receive draining IRQ enabled status
12	BB	R	0h	Bus busy enabled statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun enabled statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow enabled statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ enabled status
8	BF	R/W	0h	Bus Free IRQ enabled status
7	AERR	R/W	0h	Access Error IRQ enabled status
6	STC	R/W	0h	Start Condition IRQ enabled status
5	GC	R/W	0h	General call IRQ enabled status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-26329. I2C_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W	0h	Transmit data ready IRQ enabled status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ enabled status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ enabled status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ enabled status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ enabled status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.9.2.2.2.7 I2C_IRQENABLE_SET Register

1 I2C_IRQENABLE_SET Register (Offset = 2Ch) [reset = 0h]

Per-event interrupt enable bit vector.

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Table 14-26330. Instance Table

Instance Name	Physical Address
I2C0	**2000 002Ch**
I2C1	**2001 002Ch**
I2C2	**2002 002Ch**
I2C3	**2003 002Ch**
MCU_I2C0	**0490 002Ch**
WKUP_I2C0	**2B20 002Ch**

Figure 14-8730. I2C_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26332. I2C_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]

Table 14-26332. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC_IE	R/W	0h	Start Condition interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.9.2.2.2.8 I2C_IRQENABLE_CLR Register

1 I2C_IRQENABLE_CLR Register (Offset = 30h) [reset = 0h]

Per-event interrupt clear bit vector.

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Table 14-26333. Instance Table

Instance Name	Physical Address
I2C0	**2000 0030h**
I2C1	**2001 0030h**
I2C2	**2002 0030h**
I2C3	**2003 0030h**
MCU_I2C0	**0490 0030h**
WKUP_I2C0	**2B20 0030h**

Figure 14-8731. I2C_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26335. I2C_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable clear
10	XUDF	R/W	0h	Transmit underflow enable clear
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]

Table 14-26335. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC_IE	R/W	0h	Start Condition interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.9.2.2.2.9 I2C_WE Register

1 I2C_WE Register (Offset = 34h) [reset = 0h]

I2C wakeup enable vector (legacy).

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Table 14-26336. Instance Table

Instance Name	Physical Address
I2C0	**2000 0034h**
I2C1	**2001 0034h**
I2C2	**2002 0034h**
I2C3	**2003 0034h**
MCU_I2C0	**0490 0034h**
WKUP_I2C0	**2B20 0034h**

Figure 14-8732. I2C_WE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26338. I2C_WE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-26338. I2C_WE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.9.2.2.2.10 I2C_DMARXENABLE_SET Register

1 I2C_DMARXENABLE_SET Register (Offset = 38h) [reset = 0h]

Per-event DMA RX enable set.

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Table 14-26339. Instance Table

Instance Name	Physical Address
I2C0	**2000 0038h**
I2C1	**2001 0038h**
I2C2	**2002 0038h**
I2C3	**2003 0038h**
MCU_I2C0	**0490 0038h**
WKUP_I2C0	**2B20 0038h**

Figure 14-8733. I2C_DMARXENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_SET
R							R/W
0h							0h

Table 14-26341. I2C_DMARXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_SET	R/W	0h	Receive DMA channel enable set

14.9.2.2.2.11 I2C_DMATXENABLE_SET Register

1 I2C_DMATXENABLE_SET Register (Offset = 3Ch) [reset = 0h]

Per-event DMA TX enable set.

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Table 14-26342. Instance Table

Instance Name	Physical Address
I2C0	**2000 003Ch**
I2C1	**2001 003Ch**
I2C2	**2002 003Ch**
I2C3	**2003 003Ch**
MCU_I2C0	**0490 003Ch**
WKUP_I2C0	**2B20 003Ch**

Figure 14-8734. I2C_DMATXENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_SET
R							R/W
0h							0h

Table 14-26344. I2C_DMATXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_SET	R/W	0h	Transmit DMA channel enable set

14.9.2.2.2.12 I2C_DMARXENABLE_CLR Register

1 I2C_DMARXENABLE_CLR Register (Offset = 40h) [reset = 0h]

Per-event DMA RX enable clear.

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Table 14-26345. Instance Table

Instance Name	Physical Address
I2C0	**2000 0040h**
I2C1	**2001 0040h**
I2C2	**2002 0040h**
I2C3	**2003 0040h**
MCU_I2C0	**0490 0040h**
WKUP_I2C0	**2B20 0040h**

Figure 14-8735. I2C_DMARXENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_CLEAR
R							R/W1C
0h							0h

Table 14-26347. I2C_DMARXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_CLEAR	R/W1C	0h	Receive DMA channel enable clear

14.9.2.2.2.13 I2C_DMATXENABLE_CLR Register

1 I2C_DMATXENABLE_CLR Register (Offset = 44h) [reset = 0h]

Per-event DMA TX enable clear.

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Table 14-26348. Instance Table

Instance Name	Physical Address
I2C0	2000 0044h
I2C1	2001 0044h
I2C2	2002 0044h
I2C3	2003 0044h
MCU_I2C0	0490 0044h
WKUP_I2C0	2B20 0044h

Figure 14-8736. I2C_DMATXENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_CLEAR
R							R/W1C
0h							0h

Table 14-26350. I2C_DMATXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_CLEAR	R/W1C	0h	Transmit DMA channel enable clear

14.9.2.2.2.14 I2C_DMARXWAKE_EN Register

1 I2C_DMARXWAKE_EN Register (Offset = 48h) [reset = 0h]

Per-event DMA RX wakeup enable.

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Table 14-26351. Instance Table

Instance Name	Physical Address
I2C0	2000 0048h
I2C1	2001 0048h
I2C2	2002 0048h
I2C3	2003 0048h
MCU_I2C0	0490 0048h
WKUP_I2C0	2B20 0048h

Figure 14-8737. I2C_DMARXWAKE_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26353. I2C_DMARXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-26353. I2C_DMARXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.9.2.2.2.15 I2C_DMATXWAKE_EN Register

1 I2C_DMATXWAKE_EN Register (Offset = 4Ch) [reset = 0h]

Per-event DMA TX wakeup enable.

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Table 14-26354. Instance Table

Instance Name	Physical Address
I2C0	**2000 004Ch**
I2C1	**2001 004Ch**
I2C2	**2002 004Ch**
I2C3	**2003 004Ch**
MCU_I2C0	**0490 004Ch**
WKUP_I2C0	**2B20 004Ch**

Figure 14-8738. I2C_DMATXWAKE_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26356. I2C_DMATXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-26356. I2C_DMATXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.9.2.2.2.16 I2C_IE Register

1 I2C_IE Register (Offset = 84h) [reset = 0h]

I2C interrupt enable vector (legacy).

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Table 14-26357. Instance Table

Instance Name	Physical Address
I2C0	**2000 0084h**
I2C1	**2001 0084h**
I2C2	**2002 0084h**
I2C3	**2003 0084h**
MCU_I2C0	**0490 0084h**
WKUP_I2C0	**2B20 0084h**

Figure 14-8739. I2C_IE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26359. I2C_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]

Table 14-26359. I2C_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC_IE	R/W	0h	Start Condition interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.9.2.2.2.17 I2C_STAT Register

1 I2C_STAT Register (Offset = 88h) [reset = 0h]

I2C interrupt status vector (legacy).

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Table 14-26360. Instance Table

Instance Name	Physical Address
I2C0	2000 0088h
I2C1	2001 0088h
I2C2	2002 0088h
I2C3	2003 0088h
MCU_I2C0	0490 0088h
WKUP_I2C0	2B20 0088h

Figure 14-8740. I2C_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26362. I2C_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status
5	GC	R/W	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-26362. I2C_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.9.2.2.2.18 I2C_SYSS Register

1 I2C_SYSS Register (Offset = 90h) [reset = 0h]

System Status register

Return to Summary Table

Table 14-26363. Instance Table

Instance Name	Physical Address
I2C0	**2000 0090h**
I2C1	**2001 0090h**
I2C2	**2002 0090h**
I2C3	**2003 0090h**
MCU_I2C0	**0490 0090h**
WKUP_I2C0	**2B20 0090h**

Figure 14-8741. I2C_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RDONE
R							R
0h							0h

Table 14-26365. I2C_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	RDONE	R	0h	Reset done bit

14.9.2.2.2.19 I2C_BUF Register

1 I2C_BUF Register (Offset = 94h) [reset = 0h]

Buffer Configuration register

Return to Summary Table

Table 14-26366. Instance Table

Instance Name	Physical Address
I2C0	**2000 0094h**
I2C1	**2001 0094h**
I2C2	**2002 0094h**
I2C3	**2003 0094h**
MCU_I2C0	**0490 0094h**
WKUP_I2C0	**2B20 0094h**

Figure 14-8742. I2C_BUF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RDMA_EN	RXFIFO_CLR	RXTRSH					
R/W	R/W	R/W					
0h	0h	0h					
7	6	5	4	3	2	1	0
XDMA_EN	TXFIFO_CLR	TXTRSH					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-26368. I2C_BUF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RDMA_EN	R/W	0h	Receive DMA channel enable
14	RXFIFO_CLR	R/W	0h	Receive FIFO clear
13:8	RXTRSH	R/W	0h	Threshold value for FIFO buffer in RX mode
7	XDMA_EN	R/W	0h	Transmit DMA channel enable
6	TXFIFO_CLR	R/W	0h	Transmit FIFO clear
5:0	TXTRSH	R/W	0h	Threshold value for FIFO buffer in TX mode

14.9.2.2.2.20 I2C_CNT Register

1 I2C_CNT Register (Offset = 98h) [reset = 0h]

Data counter register

Return to Summary Table

Table 14-26369. Instance Table

Instance Name	Physical Address
I2C0	**2000 0098h**
I2C1	**2001 0098h**
I2C2	**2002 0098h**
I2C3	**2003 0098h**
MCU_I2C0	**0490 0098h**
WKUP_I2C0	**2B20 0098h**

Figure 14-8743. I2C_CNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DCOUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
DCOUNT							
R/W							
0h							

Table 14-26371. I2C_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	DCOUNT	R/W	0h	Data count

14.9.2.2.2.21 I2C_DATA Register

1 I2C_DATA Register (Offset = 9Ch) [reset = 0h]

Data access register

Return to Summary Table

Table 14-26372. Instance Table

Instance Name	Physical Address
I2C0	**2000 009Ch**
I2C1	**2001 009Ch**
I2C2	**2002 009Ch**
I2C3	**2003 009Ch**
MCU_I2C0	**0490 009Ch**
WKUP_I2C0	**2B20 009Ch**

Figure 14-8744. I2C_DATA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-26374. I2C_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RESERVED	R	0h	Reserved
7:0	DATA	R/W	0h	Transmit/Receive data FIFO endpoint

14.9.2.2.2.22 I2C_CON Register

1 I2C_CON Register (Offset = A4h) [reset = 0h]

I2C configuration register.

Return to Summary Table

Table 14-26375. Instance Table

Instance Name	Physical Address
I2C0	**2000 00A4h**
I2C1	**2001 00A4h**
I2C2	**2002 00A4h**
I2C3	**2003 00A4h**
MCU_I2C0	**0490 00A4h**
WKUP_I2C0	**2B20 00A4h**

Figure 14-8745. I2C_CON Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA
R/W	R	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h
7	6	5	4	3	2	1	0
XOA0	XOA1	XOA2	XOA3	RESERVED1		STP	STT
R/W	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-26377. I2C_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	I2C_EN	R/W	0h	I2C module enable
14	RESERVED	R	0h	Reserved
13:12	OPMODE	R/W	0h	Operation mode selection
11	STB	R/W	0h	Start byte mode [controller mode only]
10	MST	R/W	0h	Controller/target mode
9	TRX	R/W	0h	Transmitter/Receiver mode [controller mode only]
8	XSA	R/W	0h	Expand Target address
7	XOA0	R/W	0h	Expand Own address 0
6	XOA1	R/W	0h	Expand Own address 1
5	XOA2	R/W	0h	Expand Own address 2
4	XOA3	R/W	0h	Expand Own address 3
3:2	RESERVED1	R	0h	Reserved

Table 14-26377. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STP	R/W	0h	Stop condition [controller mode only]
0	STT	R/W	0h	Start condition [controller mode only]

14.9.2.2.2.23 I2C_OA Register

1 I2C_OA Register (Offset = A8h) [reset = 0h]

Own address register

Return to Summary Table

Table 14-26378. Instance Table

Instance Name	Physical Address
I2C0	**2000 00A8h**
I2C1	**2001 00A8h**
I2C2	**2002 00A8h**
I2C3	**2003 00A8h**
MCU_I2C0	**0490 00A8h**
WKUP_I2C0	**2B20 00A8h**

Figure 14-8746. I2C_OA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCODE			RESERVED			OA	
R/W			R			R/W	
0h			0h			0h	
7	6	5	4	3	2	1	0
OA							
R/W							
0h							

Table 14-26380. I2C_OA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	MCODE	R/W	0h	Controller Code
12:10	RESERVED	R	0h	Reserved
9:0	OA	R/W	0h	Own address

14.9.2.2.2.24 I2C_SA Register

1 I2C_SA Register (Offset = ACh) [reset = 3FFh]

Target address register

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Table 14-26381. Instance Table

Instance Name	Physical Address
I2C0	**2000 00ACh**
I2C1	**2001 00ACh**
I2C2	**2002 00ACh**
I2C3	**2003 00ACh**
MCU_I2C0	**0490 00ACh**
WKUP_I2C0	**2B20 00ACh**

Figure 14-8747. I2C_SA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SA	
R						R/W	
0h						3FFh	
7	6	5	4	3	2	1	0
SA							
R/W							
3FFh							

Table 14-26383. I2C_SA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	SA	R/W	3FFh	Target address

14.9.2.2.2.25 I2C_PSC Register

1 I2C_PSC Register (Offset = B0h) [reset = 0h]

I2C Clock Prescaler Register

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Table 14-26384. Instance Table

Instance Name	Physical Address
I2C0	2000 00B0h
I2C1	2001 00B0h
I2C2	2002 00B0h
I2C3	2003 00B0h
MCU_I2C0	0490 00B0h
WKUP_I2C0	2B20 00B0h

Figure 14-8748. I2C_PSC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PSC							
R/W							
0h							

Table 14-26386. I2C_PSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RESERVED	R	0h	Reserved
7:0	PSC	R/W	0h	Fast/Standard mode prescale sampling clock divider value 0x0: Divide by 1 0x1: Divide by 2 0xFF: Divide by 256

14.9.2.2.2.26 I2C_SCLL Register

1 I2C_SCLL Register (Offset = B4h) [reset = 0h]

I2C SCL Low Time Register.

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Table 14-26387. Instance Table

Instance Name	Physical Address
I2C0	**2000 00B4h**
I2C1	**2001 00B4h**
I2C2	**2002 00B4h**
I2C3	**2003 00B4h**
MCU_I2C0	**0490 00B4h**
WKUP_I2C0	**2B20 00B4h**

Figure 14-8749. I2C_SCLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSSCLL							
R/W							
0h							
7	6	5	4	3	2	1	0
SCLL							
R/W							
0h							

Table 14-26389. I2C_SCLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSSCLL	R/W	0h	High Speed mode SCL low time
7:0	SCLL	R/W	0h	Fast/Standard mode SCL low time

14.9.2.2.2.27 I2C_SCLH Register

1 I2C_SCLH Register (Offset = B8h) [reset = 0h]

I2C SCL High Time Register.

Return to Summary Table

Table 14-26390. Instance Table

Instance Name	Physical Address
I2C0	**2000 00B8h**
I2C1	**2001 00B8h**
I2C2	**2002 00B8h**
I2C3	**2003 00B8h**
MCU_I2C0	**0490 00B8h**
WKUP_I2C0	**2B20 00B8h**

Figure 14-8750. I2C_SCLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSSCLH							
R/W							
0h							
7	6	5	4	3	2	1	0
SCLH							
R/W							
0h							

Table 14-26392. I2C_SCLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSSCLH	R/W	0h	High Speed mode SCL high time
7:0	SCLH	R/W	0h	Fast/Standard mode SCL high time

14.9.2.2.2.28 I2C_SYSTEST Register

1 I2C_SYSTEST Register (Offset = BCh) [reset = 1E0h]

I2C System Test Register.

Return to Summary Table

Table 14-26393. Instance Table

Instance Name	Physical Address
I2C0	**2000 00BCh**
I2C1	**2001 00BCh**
I2C2	**2002 00BCh**
I2C3	**2003 00BCh**
MCU_I2C0	**0490 00BCh**
WKUP_I2C0	**2B20 00BCh**

Figure 14-8751. I2C_SYSTEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC
R/W	R/W	R/W		R/W	R		R
0h	0h	0h		0h	0h		1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	SCCB_E_O	SCL_I	SCL_O	SDA_I	SDA_O
R	R	R	R/W	R	R/W	R	R/W
1h	1h	1h	0h	0h	0h	0h	0h

Table 14-26395. I2C_SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ST_EN	R/W	0h	System test enable
14	FREE	R/W	0h	Free running mode [on breakpoint]
13:12	TMODE	R/W	0h	Test mode select
11	SSB	R/W	0h	Set status bits
10:9	RESERVED	R	0h	Reserved
8	SCL_I_FUNC	R	1h	SCL line input value [functional mode]
7	SCL_O_FUNC	R	1h	SCL line output value [functional mode]
6	SDA_I_FUNC	R	1h	SDA line input value [functional mode]
5	SDA_O_FUNC	R	1h	SDA line output value [functional mode]
4	SCCB_E_O	R/W	0h	SCCB_E line sense output value
3	SCL_I	R	0h	SCL line sense input value
2	SCL_O	R/W	0h	SCL line drive output value

Table 14-26395. I2C_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SDA_I	R	0h	SDA line sense input value
0	SDA_O	R/W	0h	SDA line drive output value

14.9.2.2.2.29 I2C_BUFSTAT Register

1 I2C_BUFSTAT Register (Offset = C0h) [reset = 8000h]

I2C Buffer Status Register.

Return to Summary Table

Table 14-26396. Instance Table

Instance Name	Physical Address
I2C0	2000 00C0h
I2C1	2001 00C0h
I2C2	2002 00C0h
I2C3	2003 00C0h
MCU_I2C0	0490 00C0h
WKUP_I2C0	2B20 00C0h

Figure 14-8752. I2C_BUFSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">FIFODEPTH</td><td colspan="6">RXSTAT</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">2h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TXSTAT</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-26398. I2C_BUFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:14	FIFODEPTH	R	2h	Internal FIFO buffers depth
13:8	RXSTAT	R	0h	RX Buffer Status
7:6	RESERVED	R	0h	Reserved
5:0	TXSTAT	R	0h	TX Buffer Status

14.9.2.2.2.30 I2C_OA1 Register

1 I2C_OA1 Register (Offset = C4h) [reset = 0h]

I2C Own Address 1 Register

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Table 14-26399. Instance Table

Instance Name	Physical Address
I2C0	**2000 00C4h**
I2C1	**2001 00C4h**
I2C2	**2002 00C4h**
I2C3	**2003 00C4h**
MCU_I2C0	**0490 00C4h**
WKUP_I2C0	**2B20 00C4h**

Figure 14-8753. I2C_OA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">OA1</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OA1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26401. I2C_OA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA1	R/W	0h	Own address 1

14.9.2.2.2.31 I2C_OA2 Register

1 I2C_OA2 Register (Offset = C8h) [reset = 0h]

I2C Own Address 2 Register

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Table 14-26402. Instance Table

Instance Name	Physical Address
I2C0	**2000 00C8h**
I2C1	**2001 00C8h**
I2C2	**2002 00C8h**
I2C3	**2003 00C8h**
MCU_I2C0	**0490 00C8h**
WKUP_I2C0	**2B20 00C8h**

Figure 14-8754. I2C_OA2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						OA2	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OA2							
R/W							
0h							

Table 14-26404. I2C_OA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA2	R/W	0h	Own address 2

14.9.2.2.2.32 I2C_OA3 Register

1 I2C_OA3 Register (Offset = CCh) [reset = 0h]

I2C Own Address 3 Register

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Table 14-26405. Instance Table

Instance Name	Physical Address
I2C0	**2000 00CCh**
I2C1	**2001 00CCh**
I2C2	**2002 00CCh**
I2C3	**2003 00CCh**
MCU_I2C0	**0490 00CCh**
WKUP_I2C0	**2B20 00CCh**

Figure 14-8755. I2C_OA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						OA3	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OA3							
R/W							
0h							

Table 14-26407. I2C_OA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA3	R/W	0h	Own address 3

14.9.2.2.2.33 I2C_ACTOA Register

1 I2C_ACTOA Register (Offset = D0h) [reset = 0h]

I2C Active Own Address Register.

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Table 14-26408. Instance Table

Instance Name	Physical Address
I2C0	2000 00D0h
I2C1	2001 00D0h
I2C2	2002 00D0h
I2C3	2003 00D0h
MCU_I2C0	0490 00D0h
WKUP_I2C0	2B20 00D0h

Figure 14-8756. I2C_ACTOA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				OA3_ACT	OA2_ACT	OA1_ACT	OA0_ACT
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-26410. I2C_ACTOA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:4	RESERVED	R	0h	Reserved
3	OA3_ACT	R	0h	Own Address 3 active
2	OA2_ACT	R	0h	Own Address 2 active
1	OA1_ACT	R	0h	Own Address 1 active
0	OA0_ACT	R	0h	Own Address 0 active

14.9.2.2.2.34 I2C_SBLOCK Register

1 I2C_SBLOCK Register (Offset = D4h) [reset = 0h]

I2C Clock Blocking Enable Register.

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Table 14-26411. Instance Table

Instance Name	Physical Address
I2C0	**2000 00D4h**
I2C1	**2001 00D4h**
I2C2	**2002 00D4h**
I2C3	**2003 00D4h**
MCU_I2C0	**0490 00D4h**
WKUP_I2C0	**2B20 00D4h**

Figure 14-8757. I2C_SBLOCK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>OA3_EN</td><td>OA2_EN</td><td>OA1_EN</td><td>OA0_EN</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26413. I2C_SBLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:4	RESERVED	R	0h	Reserved
3	OA3_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 3
2	OA2_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 2
1	OA1_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 1
0	OA0_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 0

14.9.2.3 MCSPI

MCSPI

14.9.2.3.1 MCSPI Summaries

MCSPI Summaries

Table 14-26414. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	MCSPI_HL_REV	2010 0000h	2011 0000h	2012 0000h
4h	32	MCSPI_HL_HWINFO	2010 0004h	2011 0004h	2012 0004h
10h	32	MCSPI_HL_SYSCONFIG	2010 0010h	2011 0010h	2012 0010h
100h	32	MCSPI_REVISION	2010 0100h	2011 0100h	2012 0100h
110h	32	MCSPI_SYSCONFIG	2010 0110h	2011 0110h	2012 0110h
114h	32	MCSPI_SYSSTATUS	2010 0114h	2011 0114h	2012 0114h
118h	32	MCSPI_IRQSTATUS	2010 0118h	2011 0118h	2012 0118h
11Ch	32	MCSPI_IRQENABLE	2010 011Ch	2011 011Ch	2012 011Ch
120h	32	MCSPI_WAKEUPENABLE	2010 0120h	2011 0120h	2012 0120h
124h	32	MCSPI_SYST	2010 0124h	2011 0124h	2012 0124h
128h	32	MCSPI_MODULCTRL	2010 0128h	2011 0128h	2012 0128h
12Ch	32	MCSPI_CH0CONF	2010 012Ch	2011 012Ch	2012 012Ch
130h	32	MCSPI_CH0STAT	2010 0130h	2011 0130h	2012 0130h
134h	32	MCSPI_CH0CTRL	2010 0134h	2011 0134h	2012 0134h
138h	32	MCSPI_TX0	2010 0138h	2011 0138h	2012 0138h
13Ch	32	MCSPI_RX0	2010 013Ch	2011 013Ch	2012 013Ch
140h	32	MCSPI_CH1CONF	2010 0140h	2011 0140h	2012 0140h
144h	32	MCSPI_CH1STAT	2010 0144h	2011 0144h	2012 0144h
148h	32	MCSPI_CH1CTRL	2010 0148h	2011 0148h	2012 0148h
14Ch	32	MCSPI_TX1	2010 014Ch	2011 014Ch	2012 014Ch
150h	32	MCSPI_RX1	2010 0150h	2011 0150h	2012 0150h
154h	32	MCSPI_CH2CONF	2010 0154h	2011 0154h	2012 0154h
158h	32	MCSPI_CH2STAT	2010 0158h	2011 0158h	2012 0158h
15Ch	32	MCSPI_CH2CTRL	2010 015Ch	2011 015Ch	2012 015Ch
160h	32	MCSPI_TX2	2010 0160h	2011 0160h	2012 0160h
164h	32	MCSPI_RX2	2010 0164h	2011 0164h	2012 0164h
168h	32	MCSPI_CH3CONF	2010 0168h	2011 0168h	2012 0168h
16Ch	32	MCSPI_CH3STAT	2010 016Ch	2011 016Ch	2012 016Ch
170h	32	MCSPI_CH3CTRL	2010 0170h	2011 0170h	2012 0170h
174h	32	MCSPI_TX3	2010 0174h	2011 0174h	2012 0174h
178h	32	MCSPI_RX3	2010 0178h	2011 0178h	2012 0178h
17Ch	32	MCSPI_XFERLEVEL	2010 017Ch	2011 017Ch	2012 017Ch
180h	32	MCSPI_DAFTX	2010 0180h	2011 0180h	2012 0180h
1A0h	32	MCSPI_DAFRX	2010 01A0h	2011 01A0h	2012 01A0h

Table 14-26415. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCU_MCSPI0 Physical Address	MCU_MCSPI1 Physical Address
0h	32	MCSPI_HL_REV	04B0 0000h	04B1 0000h
4h	32	MCSPI_HL_HWINFO	04B0 0004h	04B1 0004h
10h	32	MCSPI_HL_SYSCONFIG	04B0 0010h	04B1 0010h
100h	32	MCSPI_REVISION	04B0 0100h	04B1 0100h
110h	32	MCSPI_SYSCONFIG	04B0 0110h	04B1 0110h
114h	32	MCSPI_SYSSTATUS	04B0 0114h	04B1 0114h
118h	32	MCSPI_IRQSTATUS	04B0 0118h	04B1 0118h
11Ch	32	MCSPI_IRQENABLE	04B0 011Ch	04B1 011Ch
120h	32	MCSPI_WAKEUPENABLE	04B0 0120h	04B1 0120h
124h	32	MCSPI_SYST	04B0 0124h	04B1 0124h
128h	32	MCSPI_MODULCTRL	04B0 0128h	04B1 0128h
12Ch	32	MCSPI_CH0CONF	04B0 012Ch	04B1 012Ch
130h	32	MCSPI_CH0STAT	04B0 0130h	04B1 0130h
134h	32	MCSPI_CH0CTRL	04B0 0134h	04B1 0134h
138h	32	MCSPI_TX0	04B0 0138h	04B1 0138h
13Ch	32	MCSPI_RX0	04B0 013Ch	04B1 013Ch
140h	32	MCSPI_CH1CONF	04B0 0140h	04B1 0140h
144h	32	MCSPI_CH1STAT	04B0 0144h	04B1 0144h
148h	32	MCSPI_CH1CTRL	04B0 0148h	04B1 0148h
14Ch	32	MCSPI_TX1	04B0 014Ch	04B1 014Ch
150h	32	MCSPI_RX1	04B0 0150h	04B1 0150h
154h	32	MCSPI_CH2CONF	04B0 0154h	04B1 0154h
158h	32	MCSPI_CH2STAT	04B0 0158h	04B1 0158h
15Ch	32	MCSPI_CH2CTRL	04B0 015Ch	04B1 015Ch
160h	32	MCSPI_TX2	04B0 0160h	04B1 0160h
164h	32	MCSPI_RX2	04B0 0164h	04B1 0164h
168h	32	MCSPI_CH3CONF	04B0 0168h	04B1 0168h
16Ch	32	MCSPI_CH3STAT	04B0 016Ch	04B1 016Ch
170h	32	MCSPI_CH3CTRL	04B0 0170h	04B1 0170h
174h	32	MCSPI_TX3	04B0 0174h	04B1 0174h
178h	32	MCSPI_RX3	04B0 0178h	04B1 0178h
17Ch	32	MCSPI_XFERLEVEL	04B0 017Ch	04B1 017Ch
180h	32	MCSPI_DAFTX	04B0 0180h	04B1 0180h
1A0h	32	MCSPI_DAFRX	04B0 01A0h	04B1 01A0h

14.9.2.3.2 MCSPI Registers

MCSPI Registers

14.9.2.3.2.1 MCSPI_HL_REV Register

1 MCSPI_HL_REV Register (Offset = 0h) [reset = 40301A0Bh]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-26416. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0000h**
MCSPI1	**2011 0000h**
MCSPI2	**2012 0000h**
MCU_MCSPI0	**04B0 0000h**
MCU_MCSPI1	**04B1 0000h**

Figure 14-8758. MCSPI_HL_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		RSVD		FUNC			
R		R		R			
1h		0h		30h			
23	22	21	20	19	18	17	16
FUNC							
R							
30h							
15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
3h					2h		
7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		Bh					

Table 14-26418. MCSPI_HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old scheme and current
29:28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27:16	FUNC	R	30h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15:11	R_RTL	R	3h	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments
10:8	X_MAJOR	R	2h	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Controller Mode to Utopia Level2 The Func field [or Class/Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters

Table 14-26418. MCSPI_HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers
5:0	Y_MINOR	R	Bh	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

14.9.2.3.2.2 MCSPI_HL_HWINFO Register

1 MCSPI_HL_HWINFO Register (Offset = 4h) [reset = 9h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

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Table 14-26419. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0004h**
MCSPI1	**2011 0004h**
MCSPI2	**2012 0004h**
MCU_MCSPI0	**04B0 0004h**
MCU_MCSPI1	**04B1 0004h**

Figure 14-8759. MCSPI_HL_HWINFO Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	RETMODE	FFNBYTE					USEFIFO
R	R	R					R
0h	0h	4h					1h

Table 14-26421. MCSPI_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET 0 `Retention mode disabled` 1 `Retention mode enabled`
5:1	FFNBYTE	R	4h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account 1 `FIFO 16 bytes depth` 2 `FIFO 32 bytes depth` 4 `FIFO 64 bytes depth` 8 `FIFO 128 bytes depth` 10 `FIFO 256 bytes depth`

Table 14-26421. MCSPI_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management 0 `FIFO not implemented in design` 1 `FIFO and its management implemented in design with depth defined by FFNBYTE generic`

14.9.2.3.2.3 MCSPI_HL_SYSCONFIG Register

1 MCSPI_HL_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Clock management configuration

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Table 14-26422. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0010h**
MCSPI1	**2011 0010h**
MCSPI2	**2012 0010h**
MCU_MCSPI0	**04B0 0010h**
MCU_MCSPI1	**04B1 0010h**

Figure 14-8760. MCSPI_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD				IDLEMODE		FREEEMU	SOFTRESET
R				R/W		R/W	R/W
0h				2h		0h	0h

Table 14-26424. MCSPI_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved

Table 14-26424. MCSPI_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state 0 `Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only.` 1 `No-idle mode: local target never enters IDLE state. Backup mode, for debug only.` 2 `Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.` 3 `Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state.`
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal 0 `IP module is sensitive to emulation suspend.` 1 `IP module is not sensitive to emulation suspend.`
0	SOFTRESET	R/W	0h	Software reset [Optional] 0 `Reset done, no pending action` 1 `Initiate software reset`

14.9.2.3.2.4 MCSPI_REVISION Register

1 MCSPI_REVISION Register (Offset = 100h) [reset = 2Bh]

This register contains the hard coded RTL revision number.

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Table 14-26425. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0100h**
MCSPI1	**2011 0100h**
MCSPI2	**2012 0100h**
MCU_MCSPI0	**04B0 0100h**
MCU_MCSPI1	**04B1 0100h**

Figure 14-8761. MCSPI_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2Bh</td></tr>
</table>

Table 14-26427. MCSPI_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_13	R	0h	Reads returns 0
7:0	REV	R	2Bh	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

14.9.2.3.2.5 MCSPI_SYSCONFIG Register

1 MCSPI_SYSCONFIG Register (Offset = 110h) [reset = 15h]

This register allows controlling various parameters of the OCP interface.

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Table 14-26428. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0110h**
MCSPI1	**2011 0110h**
MCSPI2	**2012 0110h**
MCU_MCSPI0	**04B0 0110h**
MCU_MCSPI1	**04B1 0110h**

Figure 14-8762. MCSPI_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_14							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_14							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_14						CLOCKACTIVITY	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	R/W	R/W
0h			2h		1h	0h	1h

Table 14-26430. MCSPI_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_14	R	0h	Reads returns 0
9:8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period 0 `Interface and functional clocks may be switched off.` 1 `Interface clock is maintained. Functional clock may be switched off.` 2 `Functional clock is maintained. Interface clock may be switched off.` 3 `Interface and functional clocks are maintained.`
7:5	RESERVED_15	R	0h	Reads returns 0

Table 14-26430. MCSPI_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	SIDLEMODE	R/W	2h	Power management 0 If an IDLE request is detected, the MCSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[2] ENAWAKEUP bit is set. 1 If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 2 If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set. 3 Reserved - do not use.
2	ENAWAKEUP	R/W	1h	WakeUp feature control 0 Wake-up capability is disabled. 1 Wake-up capability is enabled.
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0 0 (write) Normal mode 1 (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy 0 Interface clock is free-running. 1 Automatic interface clock gating strategy is applied, based on the configuration interface activity.

14.9.2.3.2.6 MCSPI_SYSSTATUS Register

1 MCSPI_SYSSTATUS Register (Offset = 114h) [reset = 1h]

This register provides status information about the module excluding the interrupt status information

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Table 14-26431. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0114h**
MCSPI1	**2011 0114h**
MCSPI2	**2012 0114h**
MCU_MCSPI0	**04B0 0114h**
MCU_MCSPI1	**04B1 0114h**

Figure 14-8763. MCSPI_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_16							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_16							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_16							RESETDONE
R							R
0h							1h

Table 14-26433. MCSPI_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_16	R	0h	Reserved for module specific status information Read returns 0
0	RESETDONE	R	1h	Internal Reset Monitoring 0 Internal module reset is ongoing 1 Reset completed

14.9.2.3.2.7 MCSPI_IRQSTATUS Register

1 MCSPI_IRQSTATUS Register (Offset = 118h) [reset = 0h]

The interrupt status regroups all the status of the module internal events that can generate an interrupt

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Table 14-26434. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0118h**
MCSPI1	**2011 0118h**
MCSPI2	**2012 0118h**
MCU_MCSPI0	**04B0 0118h**
MCU_MCSPI1	**04B1 0118h**

Figure 14-8764. MCSPI_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_8							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_8						EOW	WKS
R						R/W1TS	R/W1TS
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_7	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED_9	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_10	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26436. MCSPI_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_8	R	0h	Reads returns 0
17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT] 0 Event false 1 Event status bit is reset
16	WKS	R/W1TS	0h	Wake Up event in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 Event status bit unchanged 1 Event is pending
15	RESERVED_7	R	0h	Reads returns 0

Table 14-26436. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled 0 Event status bit unchanged 1 Event is pending
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled 0 Event status bit unchanged 1 Event is pending
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event 0 Event status bit unchanged 1 Event is pending
11	RESERVED_9	R	0h	Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2 0 Event status bit unchanged 1 Event is pending
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2 0 Event status bit unchanged 1 Event is pending
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2 0 Event status bit unchanged 1 Event is pending
7	RESERVED_10	R	0h	Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1 0 Event status bit unchanged 1 Event is pending
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1 0 Event status bit unchanged 1 Event is pending
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1 0 Event status bit unchanged 1 Event is pending
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [responder mode only] Channel 0 0 Event status bit unchanged 1 Event is pending
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0 0 Event status bit unchanged 1 Event is pending
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0 0 Event status bit unchanged 1 Event is pending
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0 0 Event status bit unchanged 1 Event is pending

14.9.2.3.2.8 MCSPI_IRQENABLE Register

1 MCSPI_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

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Table 14-26437. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 011Ch**
MCSPI1	**2011 011Ch**
MCSPI2	**2012 011Ch**
MCU_MCSPI0	**04B0 011Ch**
MCU_MCSPI1	**04B1 011Ch**

Figure 14-8765. MCSPI_IRQENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_5						EOW_ENABLE	WKE
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_4	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED_6	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_3	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26439. MCSPI_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_5	R	0h	Reads return 0

17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable
				`0 Interrupt disabled`
				`1 Interrupt enabled`

16	WKE	R/W	0h	Wake Up event interrupt Enable in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
				`0 Interrupt disabled`
				`1 Interrupt enabled`

15	RESERVED_4	R	0h	Reads returns 0

14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 3
				`0 Interrupt disabled`
				`1 Interrupt enabled`

Table 14-26439. MCSPI_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3 0 `Interrupt disabled` 1 `Interrupt enabled`
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch3 0 `Interrupt disabled` 1 `Interrupt enabled`
11	RESERVED_6	R	0h	Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
7	RESERVED_3	R	0h	Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`

14.9.2.3.2.9 MCSPI_WAKEUPENABLE Register

1 MCSPI_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

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Table 14-26440. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0120h**
MCSPI1	**2011 0120h**
MCSPI2	**2012 0120h**
MCU_MCSPI0	**04B0 0120h**
MCU_MCSPI1	**04B1 0120h**

Figure 14-8766. MCSPI_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_18							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_18							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_18							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_18							WKEN
R							R/W
0h							0h

Table 14-26442. MCSPI_WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 `The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUPis set.` 1 `The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.`

14.9.2.3.2.10 MCSPI_SYST Register

1 MCSPI_SYST Register (Offset = 124h) [reset = 0h]

This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

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Table 14-26443. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0124h**
MCSPI1	**2011 0124h**
MCSPI2	**2012 0124h**
MCU_MCSPI0	**04B0 0124h**
MCU_MCSPI1	**04B1 0124h**

Figure 14-8767. MCSPI_SYST Name Register

31	30	29	28	27	26	25	24
RESERVED_17							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_17							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_17				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26445. MCSPI_SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_17	R	0h	Reads returns 0
11	SSB	R/W	0h	Set status bit 0 `No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPI_IRQSTATUS register.` 1 `Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the MCSPI_IRQSTATUS register.`
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line 0 `Output (as in controller mode)` 1 `Input (as in peripheral mode)`
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1] 0 `Output` 1 `Input`

Table 14-26445. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0] 0 Output 1 Input
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit 0 The pin is driven low. 1 The pin is driven high.
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

14.9.2.3.2.11 MCSPI_MODULCTRL Register

1 MCSPI_MODULCTRL Register (Offset = 128h) [reset = 4h]

This register is dedicated to the configuration of the serial port interface.

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Table 14-26446. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0128h**
MCSPI1	**2011 0128h**
MCSPI2	**2012 0128h**
MCU_MCSPI0	**04B0 0128h**
MCU_MCSPI1	**04B1 0128h**

Figure 14-8768. MCSPI_MODULCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED_11</td><td>FDAA</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MOA</td><td colspan="3">INITDLY</td><td>SYSTEM_TEST</td><td>MS</td><td>PIN34</td><td>SINGLE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26448. MCSPI_MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_11	R	0h	Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers 0 FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers. 1 FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16 0 Multiple word access disabled 1 Multiple word access enabled with FIFO

Table 14-26448. MCSPI_MODULCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE controller mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period 0 No delay for first MCSPI transfer. 1 The controller wait 4 MCSPI bus clock 2 The controller wait 8 MCSPI bus clock 3 The controller wait 16 MCSPI bus clock 4 The controller wait 32 MCSPI bus clock
3	SYSTEM_TEST	R/W	0h	Enables the system test mode 0 Functional mode 1 System test mode (SYSTEST)
2	MS	R/W	1h	Controller/ Responder 0 Controller - The module generates the SPICLK and SPIEN[3:0]. 1 Peripheral - The module receives the SPICLK and SPIEN[3:0].
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in controller or responder mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers 0 SPIEN is used as a chip-select. 1 SPIEN is not used. In this mode all related options to chip-select have no meaning.
0	SINGLE	R/W	0h	Single channel / Multi Channel [controller mode only] 0 More than one channel will be used in controller mode. 1 Only one channel will be used in controller mode. This bit must be set in Force SPIEN[i] mode.

14.9.2.3.2.12 MCSPI_CH0CONF Register

1 MCSPI_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

This register is dedicated to the configuration of the channel 0

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Table 14-26449. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 012Ch**
MCSPI1	**2011 012Ch**
MCSPI2	**2012 012Ch**
MCU_MCSPI0	**04B0 012Ch**
MCU_MCSPI1	**04B1 012Ch**

Figure 14-8769. MCSPI_CH0CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS0		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	22	21	20	19	18	17	16
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-26451. MCSPI_CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-26451. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 `0.5 clock cycle` 1 `1.5 clock cycles` 2 `2.5 clock cycles` 3 `3.5 clock cycles`
24	SBPOL	R/W	0h	Start bit polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 `Default MCSPI transfer length as specified by WL bit field` 1 `Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL`
22:21	SPIENSLV	R/W	0h	Channel 0 only and responder mode only: SPI responder select signal detection Reserved bits for other cases 0 `Detection enabled only on SPIEN[0]` 1 `Detection enabled only on SPIEN[1]` 2 `Detection enabled only on SPIEN[2]` 3 `Detection enabled only on SPIEN[3]`
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 `Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.` 1 `Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.`
19	TURBO	R/W	0h	Turbo mode 0 `Turbo is deactivated (recommended for single MCSPI word transfer).` 1 `Turbo is activated to maximize the throughput for multiple MCSPI words transfer.`
18	IS	R/W	1h	Input Select 0 `Data line 0 (SPIDAT[0]) selected for reception` 1 `Data line 1 (SPIDAT[1]) selected for reception`
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 `Data line 1 (SPIDAT[1]) selected for transmission` 1 `No transmission on Data Line1 (SPIDAT[1])`
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 `Data Line0 (SPIDAT[0]) selected for transmission` 1 `No transmission on data line 0 (SPIDAT[0])`

Table 14-26451. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`
13:12	TRM	R/W	0h	Transmit/Receive modes 0 `Transmit-and-receive mode` 1 `Receive-only mode` 2 `Transmit-only mode` 3 `Reserved`
11:7	WL	R/W	0h	SPI word length 0 `Reserved` 1 `Reserved` 2 `Reserved` 3 `The MCSPI word is 4 bits long` 4 `The MCSPI word is 5 bits long` 5 `The MCSPI word is 6 bits long` 6 `The MCSPI word is 7 bits long` 7 `The MCSPI word is 8 bits long` 8 `The MCSPI word is 9 bits long` 9 `The MCSPI word is 10 bits long` A `The MCSPI word is 11 bits long` B `The MCSPI word is 12 bits long` C `The MCSPI word is 13 bits long` D `The MCSPI word is 14 bits long` E `The MCSPI word is 15 bits long` F `The MCSPI word is 16 bits long` 10 `The MCSPI word is 17 bits long` 11 `The MCSPI word is 18 bits long` 12 `The MCSPI word is 19 bits long` 13 `The MCSPI word is 20 bits long` 14 `The MCSPI word is 21 bits long` 15 `The MCSPI word is 22 bits long` 16 `The MCSPI word is 23 bits long` 17 `The MCSPI word is 24 bits long` 18 `The MCSPI word is 25 bits long` 19 `The MCSPI word is 26 bits long` 1A `The MCSPI word is 27 bits long` 1B `The MCSPI word is 28 bits long` 1C `The MCSPI word is 29 bits long` 1D `The MCSPI word is 30 bits long` 1E `The MCSPI word is 31 bits long` 1F `The MCSPI word is 32 bits long`
6	EPOL	R/W	0h	SPIEN polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`

Table 14-26451. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.2.3.2.13 MCSPI_CH0STAT Register

1 MCSPI_CH0STAT Register (Offset = 130h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 0

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Table 14-26452. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0130h**
MCSPI1	**2011 0130h**
MCSPI2	**2012 0130h**
MCU_MCSPI0	**04B0 0130h**
MCU_MCSPI1	**04B1 0130h**

Figure 14-8770. MCSPI_CH0STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26454. MCSPI_CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 FIFO receive buffer is not full 1 FIFO receive buffer is full
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 FIFO receive buffer is not empty 1 FIFO receive buffer is empty
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 FIFO transmit buffer is not full 1 FIFO transmit buffer is full
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 FIFO transmit buffer is not empty 1 FIFO transmit buffer is empty

Table 14-26454. MCSPI_CH0STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel "i" Receiver Register Status 0 Register is empty. 1 Register is full.

14.9.2.3.2.14 MCSPI_CH0CTRL Register

1 MCSPI_CH0CTRL Register (Offset = 134h) [reset = 0h]

This register is dedicated to enable the channel 0

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Table 14-26455. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0134h**
MCSPI1	**2011 0134h**
MCSPI2	**2012 0134h**
MCU_MCSPI0	**04B0 0134h**
MCU_MCSPI1	**04B1 0134h**

Figure 14-8771. MCSPI_CH0CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 14-26457. MCSPI_CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.9.2.3.2.15 MCSPI_TX0 Register

1 MCSPI_TX0 Register (Offset = 138h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-26458. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0138h**
MCSPI1	**2011 0138h**
MCSPI2	**2012 0138h**
MCU_MCSPI0	**04B0 0138h**
MCU_MCSPI1	**04B1 0138h**

Figure 14-8772. MCSPI_TX0 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-26460. MCSPI_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 0 Data to transmit

14.9.2.3.2.16 MCSPI_RX0 Register

1 MCSPI_RX0 Register (Offset = 13Ch) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-26461. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 013Ch**
MCSPI1	**2011 013Ch**
MCSPI2	**2012 013Ch**
MCU_MCSPI0	**04B0 013Ch**
MCU_MCSPI1	**04B1 013Ch**

Figure 14-8773. MCSPI_RX0 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-26463. MCSPI_RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 0 Received Data

14.9.2.3.2.17 MCSPI_CH1CONF Register

1 MCSPI_CH1CONF Register (Offset = 140h) [reset = 60000h]

This register is dedicated to the configuration of the channel.

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Table 14-26464. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0140h**
MCSPI1	**2011 0140h**
MCSPI2	**2012 0140h**
MCU_MCSPI0	**04B0 0140h**
MCU_MCSPI1	**04B1 0140h**

Figure 14-8774. MCSPI_CH1CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS1		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-26466. MCSPI_CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-26466. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

Table 14-26466. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-26466. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
0	PHA	R/W	0h	SPICLK phase 0 `Data are latched on odd-numbered edges of SPICLK.` 1 `Data are latched on even-numbered edges of SPICLK.`

14.9.2.3.2.18 MCSPI_CH1STAT Register

1 MCSPI_CH1STAT Register (Offset = 144h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 1

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Table 14-26467. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0144h**
MCSPI1	**2011 0144h**
MCSPI2	**2012 0144h**
MCU_MCSPI0	**04B0 0144h**
MCU_MCSPI1	**04B1 0144h**

Figure 14-8775. MCSPI_CH1STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26469. MCSPI_CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-26469. MCSPI_CH1STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.2.3.2.19 MCSPI_CH1CTRL Register

1 MCSPI_CH1CTRL Register (Offset = 148h) [reset = 0h]

This register is dedicated to enable the channel 1

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Table 14-26470. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0148h**
MCSPI1	**2011 0148h**
MCSPI2	**2012 0148h**
MCU_MCSPI0	**04B0 0148h**
MCU_MCSPI1	**04B1 0148h**

Figure 14-8776. MCSPI_CH1CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTCLK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-26472. MCSPI_CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.9.2.3.2.20 MCSPI_TX1 Register

1 MCSPI_TX1 Register (Offset = 14Ch) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-26473. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 014Ch**
MCSPI1	**2011 014Ch**
MCSPI2	**2012 014Ch**
MCU_MCSPI0	**04B0 014Ch**
MCU_MCSPI1	**04B1 014Ch**

Figure 14-8777. MCSPI_TX1 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-26475. MCSPI_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 1 Data to transmit

14.9.2.3.2.21 MCSPI_RX1 Register

1 MCSPI_RX1 Register (Offset = 150h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-26476. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0150h**
MCSPI1	**2011 0150h**
MCSPI2	**2012 0150h**
MCU_MCSPI0	**04B0 0150h**
MCU_MCSPI1	**04B1 0150h**

Figure 14-8778. MCSPI_RX1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26478. MCSPI_RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 1 Received Data

14.9.2.3.2.22 MCSPI_CH2CONF Register

1 MCSPI_CH2CONF Register (Offset = 154h) [reset = 60000h]

This register is dedicated to the configuration of the channel 2

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Table 14-26479. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0154h**
MCSPI1	**2011 0154h**
MCSPI2	**2012 0154h**
MCU_MCSPI0	**04B0 0154h**
MCU_MCSPI1	**04B1 0154h**

Figure 14-8779. MCSPI_CH2CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS2		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	22	21	20	19	18	17	16
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-26481. MCSPI_CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-26481. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

Table 14-26481. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-26481. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.2.3.2.23 MCSPI_CH2STAT Register

1 MCSPI_CH2STAT Register (Offset = 158h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 2

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Table 14-26482. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0158h**
MCSPI1	**2011 0158h**
MCSPI2	**2012 0158h**
MCU_MCSPI0	**04B0 0158h**
MCU_MCSPI1	**04B1 0158h**

Figure 14-8780. MCSPI_CH2STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26484. MCSPI_CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-26484. MCSPI_CH2STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.2.3.2.24 MCSPI_CH2CTRL Register

1 MCSPI_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

This register is dedicated to enable the channel 2

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Table 14-26485. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 015Ch**
MCSPI1	**2011 015Ch**
MCSPI2	**2012 015Ch**
MCU_MCSPI0	**04B0 015Ch**
MCU_MCSPI1	**04B1 015Ch**

Figure 14-8781. MCSPI_CH2CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTCLK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-26487. MCSPI_CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.9.2.3.2.25 MCSPI_TX2 Register

1 MCSPI_TX2 Register (Offset = 160h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-26488. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0160h**
MCSPI1	**2011 0160h**
MCSPI2	**2012 0160h**
MCU_MCSPI0	**04B0 0160h**
MCU_MCSPI1	**04B1 0160h**

Figure 14-8782. MCSPI_TX2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26490. MCSPI_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 2 Data to transmit

14.9.2.3.2.26 MCSPI_RX2 Register

1 MCSPI_RX2 Register (Offset = 164h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-26491. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0164h**
MCSPI1	**2011 0164h**
MCSPI2	**2012 0164h**
MCU_MCSPI0	**04B0 0164h**
MCU_MCSPI1	**04B1 0164h**

Figure 14-8783. MCSPI_RX2 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-26493. MCSPI_RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 2 Received Data

14.9.2.3.2.27 MCSPI_CH3CONF Register

1 MCSPI_CH3CONF Register (Offset = 168h) [reset = 60000h]

This register is dedicated to the configuration of the channel 3

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Table 14-26494. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0168h**
MCSPI1	**2011 0168h**
MCSPI2	**2012 0168h**
MCU_MCSPI0	**04B0 0168h**
MCU_MCSPI1	**04B1 0168h**

Figure 14-8784. MCSPI_CH3CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS3		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-26496. MCSPI_CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-26496. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 `0.5 clock cycle` 1 `1.5 clock cycles` 2 `2.5 clock cycles` 3 `3.5 clock cycles`
24	SBPOL	R/W	0h	Start bit polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 `Default MCSPI transfer length as specified by WL bit field` 1 `Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL`
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 `Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.` 1 `Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.`
19	TURBO	R/W	0h	Turbo mode 0 `Turbo is deactivated (recommended for single MCSPI word transfer).` 1 `Turbo is activated to maximize the throughput for multiple MCSPI words transfer.`
18	IS	R/W	1h	Input Select 0 `Data line 0 (SPIDAT[0]) selected for reception` 1 `Data line 1 (SPIDAT[1]) selected for reception`
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 `Data line 1 (SPIDAT[1]) selected for transmission` 1 `No transmission on Data Line1 (SPIDAT[1])`
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 `Data Line0 (SPIDAT[0]) selected for transmission` 1 `No transmission on data line 0 (SPIDAT[0])`
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`

Table 14-26496. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`
13:12	TRM	R/W	0h	Transmit/Receive modes 0 `Transmit-and-receive mode` 1 `Receive-only mode` 2 `Transmit-only mode` 3 `Reserved`
11:7	WL	R/W	0h	SPI word length 0 `Reserved` 1 `Reserved` 2 `Reserved` 3 `The MCSPI word is 4 bits long` 4 `The MCSPI word is 5 bits long` 5 `The MCSPI word is 6 bits long` 6 `The MCSPI word is 7 bits long` 7 `The MCSPI word is 8 bits long` 8 `The MCSPI word is 9 bits long` 9 `The MCSPI word is 10 bits long` A `The MCSPI word is 11 bits long` B `The MCSPI word is 12 bits long` C `The MCSPI word is 13 bits long` D `The MCSPI word is 14 bits long` E `The MCSPI word is 15 bits long` F `The MCSPI word is 16 bits long` 10 `The MCSPI word is 17 bits long` 11 `The MCSPI word is 18 bits long` 12 `The MCSPI word is 19 bits long` 13 `The MCSPI word is 20 bits long` 14 `The MCSPI word is 21 bits long` 15 `The MCSPI word is 22 bits long` 16 `The MCSPI word is 23 bits long` 17 `The MCSPI word is 24 bits long` 18 `The MCSPI word is 25 bits long` 19 `The MCSPI word is 26 bits long` 1A `The MCSPI word is 27 bits long` 1B `The MCSPI word is 28 bits long` 1C `The MCSPI word is 29 bits long` 1D `The MCSPI word is 30 bits long` 1E `The MCSPI word is 31 bits long` 1F `The MCSPI word is 32 bits long`
6	EPOL	R/W	0h	SPIEN polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`

Table 14-26496. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.2.3.2.28 MCSPI_CH3STAT Register

1 MCSPI_CH3STAT Register (Offset = 16Ch) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 3

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Table 14-26497. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 016Ch**
MCSPI1	**2011 016Ch**
MCSPI2	**2012 016Ch**
MCU_MCSPI0	**04B0 016Ch**
MCU_MCSPI1	**04B1 016Ch**

Figure 14-8785. MCSPI_CH3STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26499. MCSPI_CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-26499. MCSPI_CH3STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.2.3.2.29 MCSPI_CH3CTRL Register

1 MCSPI_CH3CTRL Register (Offset = 170h) [reset = 0h]

This register is dedicated to enable the channel 3

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Table 14-26500. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0170h**
MCSPI1	**2011 0170h**
MCSPI2	**2012 0170h**
MCU_MCSPI0	**04B0 0170h**
MCU_MCSPI1	**04B1 0170h**

Figure 14-8786. MCSPI_CH3CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 14-26502. MCSPI_CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 `Clock ratio is CLKD + 1.` 1 `Clock ratio is CLKD + 1 + 16.` FF `Clock ratio is CLKD + 1 + 4080.`
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 `Channel i is not active.` 1 `Channel i is active.`

14.9.2.3.2.30 MCSPI_TX3 Register

1 MCSPI_TX3 Register (Offset = 174h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-26503. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0174h**
MCSPI1	**2011 0174h**
MCSPI2	**2012 0174h**
MCU_MCSPI0	**04B0 0174h**
MCU_MCSPI1	**04B1 0174h**

Figure 14-8787. MCSPI_TX3 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDATA							
R/W							
0h							

Table 14-26505. MCSPI_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 3 Data to transmit

14.9.2.3.2.31 MCSPI_RX3 Register

1 MCSPI_RX3 Register (Offset = 178h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-26506. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0178h**
MCSPI1	**2011 0178h**
MCSPI2	**2012 0178h**
MCU_MCSPI0	**04B0 0178h**
MCU_MCSPI1	**04B1 0178h**

Figure 14-8788. MCSPI_RX3 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-26508. MCSPI_RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 3 Received Data

14.9.2.3.2.32 MCSPI_XFERLEVEL Register

1 MCSPI_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

This register provides transfer levels needed while using FIFO buffer during transfer.

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Table 14-26509. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 017Ch**
MCSPI1	**2011 017Ch**
MCSPI2	**2012 017Ch**
MCU_MCSPI0	**04B0 017Ch**
MCU_MCSPI1	**04B1 017Ch**

Figure 14-8789. MCSPI_XFERLEVEL Name Register

31	30	29	28	27	26	25	24
WCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
WCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
AFL							
R/W							
0h							
7	6	5	4	3	2	1	0
AEL							
R/W							
0h							

Table 14-26511. MCSPI_XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description

31:16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index
				`0 Counter not used`
				`1 One word`
				`FFFE 65534 MCSPI word`
				`FFFF 65535 MCSPI word`

Table 14-26511. MCSPI_XFERLEVEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE 0 1 byte 1 2 bytes FE 255bytes FF 256bytes
7:0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1 0 1 byte 1 2 bytes FE 255 bytes FF 256bytes

14.9.2.3.2.33 MCSPI_DAFTX Register

1 MCSPI_DAFTX Register (Offset = 180h) [reset = 0h]

This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

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Table 14-26512. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0180h**
MCSPI1	**2011 0180h**
MCSPI2	**2012 0180h**
MCU_MCSPI0	**04B0 0180h**
MCU_MCSPI1	**04B1 0180h**

Figure 14-8790. MCSPI_DAFTX Name Register

31	30	29	28	27	26	25	24
DAFTDATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DAFTDATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DAFTDATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAFTDATA							
R/W							
0h							

Table 14-26514. MCSPI_DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.9.2.3.2.34 MCSPI_DAFRX Register

1 MCSPI_DAFRX Register (Offset = 1A0h) [reset = 0h]

This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

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Table 14-26515. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 01A0h**
MCSPI1	**2011 01A0h**
MCSPI2	**2012 01A0h**
MCU_MCSPI0	**04B0 01A0h**
MCU_MCSPI1	**04B1 01A0h**

Figure 14-8791. MCSPI_DAFRX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26517. MCSPI_DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.9.2.4 UART

UART

14.9.2.4.1 UART Summaries

UART Summaries

Table 14-26518. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	MCU_UART0 Physical Address	UART0 Physical Address	UART1 Physical Address
0h	32	UART_DLL	04A0 0000h	0280 0000h	0281 0000h
0h	32	UART_RHR	04A0 0000h	0280 0000h	0281 0000h
0h	32	UART_THR	04A0 0000h	0280 0000h	0281 0000h
4h	32	UART_DLH	04A0 0004h	0280 0004h	0281 0004h
4h	32	UART_IER_CIR	04A0 0004h	0280 0004h	0281 0004h
4h	32	UART_IER_IRDA	04A0 0004h	0280 0004h	0281 0004h
4h	32	UART_IER_UART	04A0 0004h	0280 0004h	0281 0004h
8h	32	UART_EFR	04A0 0008h	0280 0008h	0281 0008h
8h	32	UART_FCR	04A0 0008h	0280 0008h	0281 0008h
8h	32	UART_IIR_CIR	04A0 0008h	0280 0008h	0281 0008h
8h	32	UART_IIR_IRDA	04A0 0008h	0280 0008h	0281 0008h
8h	32	UART_IIR_UART	04A0 0008h	0280 0008h	0281 0008h
Ch	32	UART_LCR	04A0 000Ch	0280 000Ch	0281 000Ch
10h	32	UART_MCR	04A0 0010h	0280 0010h	0281 0010h
10h	32	UART_XON1_ADDR1	04A0 0010h	0280 0010h	0281 0010h
14h	32	UART_LSR_CIR	04A0 0014h	0280 0014h	0281 0014h
14h	32	UART_LSR_IRDA	04A0 0014h	0280 0014h	0281 0014h
14h	32	UART_LSR_UART	04A0 0014h	0280 0014h	0281 0014h
14h	32	UART_XON2_ADDR2	04A0 0014h	0280 0014h	0281 0014h
18h	32	UART_MSR	04A0 0018h	0280 0018h	0281 0018h
18h	32	UART_TCR	04A0 0018h	0280 0018h	0281 0018h
18h	32	UART_XOFF1	04A0 0018h	0280 0018h	0281 0018h
1Ch	32	UART_SPR	04A0 001Ch	0280 001Ch	0281 001Ch
1Ch	32	UART_TLR	04A0 001Ch	0280 001Ch	0281 001Ch
1Ch	32	UART_XOFF2	04A0 001Ch	0280 001Ch	0281 001Ch
20h	32	UART_MDR1	04A0 0020h	0280 0020h	0281 0020h
24h	32	UART_MDR2	04A0 0024h	0280 0024h	0281 0024h
28h	32	UART_SFLSR	04A0 0028h	0280 0028h	0281 0028h
28h	32	UART_TXFLL	04A0 0028h	0280 0028h	0281 0028h
2Ch	32	UART_RESUME	04A0 002Ch	0280 002Ch	0281 002Ch
2Ch	32	UART_TXFLH	04A0 002Ch	0280 002Ch	0281 002Ch
30h	32	UART_RXFLL	04A0 0030h	0280 0030h	0281 0030h
30h	32	UART_SFREGL	04A0 0030h	0280 0030h	0281 0030h
34h	32	UART_RXFLH	04A0 0034h	0280 0034h	0281 0034h
34h	32	UART_SFREGH	04A0 0034h	0280 0034h	0281 0034h
38h	32	UART_BLR	04A0 0038h	0280 0038h	0281 0038h
38h	32	UART_UASR	04A0 0038h	0280 0038h	0281 0038h

Table 14-26518. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	MCU_UART0 Physical Address	UART0 Physical Address	UART1 Physical Address
3Ch	32	UART_ACREG	04A0 003Ch	0280 003Ch	0281 003Ch
40h	32	UART_SCR	04A0 0040h	0280 0040h	0281 0040h
44h	32	UART_SSR	04A0 0044h	0280 0044h	0281 0044h
48h	32	UART_EBLR	04A0 0048h	0280 0048h	0281 0048h
50h	32	UART_MVR	04A0 0050h	0280 0050h	0281 0050h
54h	32	UART_SYSC	04A0 0054h	0280 0054h	0281 0054h
58h	32	UART_SYSS	04A0 0058h	0280 0058h	0281 0058h
5Ch	32	UART_WER	04A0 005Ch	0280 005Ch	0281 005Ch
60h	32	UART_CFPS	04A0 0060h	0280 0060h	0281 0060h
64h	32	UART_RXFIFO_LVL	04A0 0064h	0280 0064h	0281 0064h
68h	32	UART_TXFIFO_LVL	04A0 0068h	0280 0068h	0281 0068h
6Ch	32	UART_IER2	04A0 006Ch	0280 006Ch	0281 006Ch
70h	32	UART_ISR2	04A0 0070h	0280 0070h	0281 0070h
74h	32	UART_FREQ_SEL	04A0 0074h	0280 0074h	0281 0074h
78h	32	UART_ABAUD_1ST_CHAR	04A0 0078h	0280 0078h	0281 0078h
7Ch	32	UART_BAUD_2ND_CHAR	04A0 007Ch	0280 007Ch	0281 007Ch
80h	32	UART_MDR3	04A0 0080h	0280 0080h	0281 0080h
84h	32	UART_TX_DMA_THRESHOLD	04A0 0084h	0280 0084h	0281 0084h
88h	32	UART_MDR4	04A0 0088h	0280 0088h	0281 0088h
8Ch	32	UART_EFR2	04A0 008Ch	0280 008Ch	0281 008Ch
90h	32	UART_ECR	04A0 0090h	0280 0090h	0281 0090h
94h	32	UART_TIMEGUARD	04A0 0094h	0280 0094h	0281 0094h
98h	32	UART_TIMEOUTL	04A0 0098h	0280 0098h	0281 0098h
9Ch	32	UART_TIMEOUTH	04A0 009Ch	0280 009Ch	0281 009Ch
A0h	32	UART_SCCR	04A0 00A0h	0280 00A0h	0281 00A0h
A4h	32	UART_ERHR	04A0 00A4h	0280 00A4h	0281 00A4h
A4h	32	UART_ETHR	04A0 00A4h	0280 00A4h	0281 00A4h
A8h	32	UART_MAR	04A0 00A8h	0280 00A8h	0281 00A8h
ACh	32	UART_MMR	04A0 00ACh	0280 00ACh	0281 00ACh
B0h	32	UART_MBR	04A0 00B0h	0280 00B0h	0281 00B0h

Table 14-26519. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART2 Physical Address	UART3 Physical Address	UART4 Physical Address
0h	32	UART_DLL	0282 0000h	0283 0000h	0284 0000h
0h	32	UART_RHR	0282 0000h	0283 0000h	0284 0000h
0h	32	UART_THR	0282 0000h	0283 0000h	0284 0000h
4h	32	UART_DLH	0282 0004h	0283 0004h	0284 0004h
4h	32	UART_IER_CIR	0282 0004h	0283 0004h	0284 0004h
4h	32	UART_IER_IRDA	0282 0004h	0283 0004h	0284 0004h
4h	32	UART_IER_UART	0282 0004h	0283 0004h	0284 0004h
8h	32	UART_EFR	0282 0008h	0283 0008h	0284 0008h
8h	32	UART_FCR	0282 0008h	0283 0008h	0284 0008h
8h	32	UART_IIR_CIR	0282 0008h	0283 0008h	0284 0008h

Table 14-26519. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART2 Physical Address	UART3 Physical Address	UART4 Physical Address
8h	32	UART_IIR_IRDA	0282 0008h	0283 0008h	0284 0008h
8h	32	UART_IIR_UART	0282 0008h	0283 0008h	0284 0008h
Ch	32	UART_LCR	0282 000Ch	0283 000Ch	0284 000Ch
10h	32	UART_MCR	0282 0010h	0283 0010h	0284 0010h
10h	32	UART_XON1_ADDR1	0282 0010h	0283 0010h	0284 0010h
14h	32	UART_LSR_CIR	0282 0014h	0283 0014h	0284 0014h
14h	32	UART_LSR_IRDA	0282 0014h	0283 0014h	0284 0014h
14h	32	UART_LSR_UART	0282 0014h	0283 0014h	0284 0014h
14h	32	UART_XON2_ADDR2	0282 0014h	0283 0014h	0284 0014h
18h	32	UART_MSR	0282 0018h	0283 0018h	0284 0018h
18h	32	UART_TCR	0282 0018h	0283 0018h	0284 0018h
18h	32	UART_XOFF1	0282 0018h	0283 0018h	0284 0018h
1Ch	32	UART_SPR	0282 001Ch	0283 001Ch	0284 001Ch
1Ch	32	UART_TLR	0282 001Ch	0283 001Ch	0284 001Ch
1Ch	32	UART_XOFF2	0282 001Ch	0283 001Ch	0284 001Ch
20h	32	UART_MDR1	0282 0020h	0283 0020h	0284 0020h
24h	32	UART_MDR2	0282 0024h	0283 0024h	0284 0024h
28h	32	UART_SFLSR	0282 0028h	0283 0028h	0284 0028h
28h	32	UART_TXFLL	0282 0028h	0283 0028h	0284 0028h
2Ch	32	UART_RESUME	0282 002Ch	0283 002Ch	0284 002Ch
2Ch	32	UART_TXFLH	0282 002Ch	0283 002Ch	0284 002Ch
30h	32	UART_RXFLL	0282 0030h	0283 0030h	0284 0030h
30h	32	UART_SFREGL	0282 0030h	0283 0030h	0284 0030h
34h	32	UART_RXFLH	0282 0034h	0283 0034h	0284 0034h
34h	32	UART_SFREGH	0282 0034h	0283 0034h	0284 0034h
38h	32	UART_BLR	0282 0038h	0283 0038h	0284 0038h
38h	32	UART_UASR	0282 0038h	0283 0038h	0284 0038h
3Ch	32	UART_ACREG	0282 003Ch	0283 003Ch	0284 003Ch
40h	32	UART_SCR	0282 0040h	0283 0040h	0284 0040h
44h	32	UART_SSR	0282 0044h	0283 0044h	0284 0044h
48h	32	UART_EBLR	0282 0048h	0283 0048h	0284 0048h
50h	32	UART_MVR	0282 0050h	0283 0050h	0284 0050h
54h	32	UART_SYSC	0282 0054h	0283 0054h	0284 0054h
58h	32	UART_SYSS	0282 0058h	0283 0058h	0284 0058h
5Ch	32	UART_WER	0282 005Ch	0283 005Ch	0284 005Ch
60h	32	UART_CFPS	0282 0060h	0283 0060h	0284 0060h
64h	32	UART_RXFIFO_LVL	0282 0064h	0283 0064h	0284 0064h
68h	32	UART_TXFIFO_LVL	0282 0068h	0283 0068h	0284 0068h
6Ch	32	UART_IER2	0282 006Ch	0283 006Ch	0284 006Ch
70h	32	UART_ISR2	0282 0070h	0283 0070h	0284 0070h
74h	32	UART_FREQ_SEL	0282 0074h	0283 0074h	0284 0074h
78h	32	UART_ABAUD_1ST_CHAR	0282 0078h	0283 0078h	0284 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0282 007Ch	0283 007Ch	0284 007Ch
80h	32	UART_MDR3	0282 0080h	0283 0080h	0284 0080h

Table 14-26519. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART2 Physical Address	UART3 Physical Address	UART4 Physical Address
84h	32	UART_TX_DMA_THRESHOLD	0282 0084h	0283 0084h	0284 0084h
88h	32	UART_MDR4	0282 0088h	0283 0088h	0284 0088h
8Ch	32	UART_EFR2	0282 008Ch	0283 008Ch	0284 008Ch
90h	32	UART_ECR	0282 0090h	0283 0090h	0284 0090h
94h	32	UART_TIMEGUARD	0282 0094h	0283 0094h	0284 0094h
98h	32	UART_TIMEOUTL	0282 0098h	0283 0098h	0284 0098h
9Ch	32	UART_TIMEOUTH	0282 009Ch	0283 009Ch	0284 009Ch
A0h	32	UART_SCCR	0282 00A0h	0283 00A0h	0284 00A0h
A4h	32	UART_ERHR	0282 00A4h	0283 00A4h	0284 00A4h
A4h	32	UART_ETHR	0282 00A4h	0283 00A4h	0284 00A4h
A8h	32	UART_MAR	0282 00A8h	0283 00A8h	0284 00A8h
ACh	32	UART_MMR	0282 00ACh	0283 00ACh	0284 00ACh
B0h	32	UART_MBR	0282 00B0h	0283 00B0h	0284 00B0h

Table 14-26520. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART5 Physical Address	UART6 Physical Address	WKUP_UART0 Physical Address
0h	32	UART_DLL	0285 0000h	0286 0000h	2B30 0000h
0h	32	UART_RHR	0285 0000h	0286 0000h	2B30 0000h
0h	32	UART_THR	0285 0000h	0286 0000h	2B30 0000h
4h	32	UART_DLH	0285 0004h	0286 0004h	2B30 0004h
4h	32	UART_IER_CIR	0285 0004h	0286 0004h	2B30 0004h
4h	32	UART_IER_IRDA	0285 0004h	0286 0004h	2B30 0004h
4h	32	UART_IER_UART	0285 0004h	0286 0004h	2B30 0004h
8h	32	UART_EFR	0285 0008h	0286 0008h	2B30 0008h
8h	32	UART_FCR	0285 0008h	0286 0008h	2B30 0008h
8h	32	UART_IIR_CIR	0285 0008h	0286 0008h	2B30 0008h
8h	32	UART_IIR_IRDA	0285 0008h	0286 0008h	2B30 0008h
8h	32	UART_IIR_UART	0285 0008h	0286 0008h	2B30 0008h
Ch	32	UART_LCR	0285 000Ch	0286 000Ch	2B30 000Ch
10h	32	UART_MCR	0285 0010h	0286 0010h	2B30 0010h
10h	32	UART_XON1_ADDR1	0285 0010h	0286 0010h	2B30 0010h
14h	32	UART_LSR_CIR	0285 0014h	0286 0014h	2B30 0014h
14h	32	UART_LSR_IRDA	0285 0014h	0286 0014h	2B30 0014h
14h	32	UART_LSR_UART	0285 0014h	0286 0014h	2B30 0014h
14h	32	UART_XON2_ADDR2	0285 0014h	0286 0014h	2B30 0014h
18h	32	UART_MSR	0285 0018h	0286 0018h	2B30 0018h
18h	32	UART_TCR	0285 0018h	0286 0018h	2B30 0018h
18h	32	UART_XOFF1	0285 0018h	0286 0018h	2B30 0018h
1Ch	32	UART_SPR	0285 001Ch	0286 001Ch	2B30 001Ch
1Ch	32	UART_TLR	0285 001Ch	0286 001Ch	2B30 001Ch
1Ch	32	UART_XOFF2	0285 001Ch	0286 001Ch	2B30 001Ch
20h	32	UART_MDR1	0285 0020h	0286 0020h	2B30 0020h
24h	32	UART_MDR2	0285 0024h	0286 0024h	2B30 0024h

Table 14-26520. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART5 Physical Address	UART6 Physical Address	WKUP_UART0 Physical Address
28h	32	UART_SFLSR	0285 0028h	0286 0028h	2B30 0028h
28h	32	UART_TXFLL	0285 0028h	0286 0028h	2B30 0028h
2Ch	32	UART_RESUME	0285 002Ch	0286 002Ch	2B30 002Ch
2Ch	32	UART_TXFLH	0285 002Ch	0286 002Ch	2B30 002Ch
30h	32	UART_RXFLL	0285 0030h	0286 0030h	2B30 0030h
30h	32	UART_SFREGL	0285 0030h	0286 0030h	2B30 0030h
34h	32	UART_RXFLH	0285 0034h	0286 0034h	2B30 0034h
34h	32	UART_SFREGH	0285 0034h	0286 0034h	2B30 0034h
38h	32	UART_BLR	0285 0038h	0286 0038h	2B30 0038h
38h	32	UART_UASR	0285 0038h	0286 0038h	2B30 0038h
3Ch	32	UART_ACREG	0285 003Ch	0286 003Ch	2B30 003Ch
40h	32	UART_SCR	0285 0040h	0286 0040h	2B30 0040h
44h	32	UART_SSR	0285 0044h	0286 0044h	2B30 0044h
48h	32	UART_EBLR	0285 0048h	0286 0048h	2B30 0048h
50h	32	UART_MVR	0285 0050h	0286 0050h	2B30 0050h
54h	32	UART_SYSC	0285 0054h	0286 0054h	2B30 0054h
58h	32	UART_SYSS	0285 0058h	0286 0058h	2B30 0058h
5Ch	32	UART_WER	0285 005Ch	0286 005Ch	2B30 005Ch
60h	32	UART_CFPS	0285 0060h	0286 0060h	2B30 0060h
64h	32	UART_RXFIFO_LVL	0285 0064h	0286 0064h	2B30 0064h
68h	32	UART_TXFIFO_LVL	0285 0068h	0286 0068h	2B30 0068h
6Ch	32	UART_IER2	0285 006Ch	0286 006Ch	2B30 006Ch
70h	32	UART_ISR2	0285 0070h	0286 0070h	2B30 0070h
74h	32	UART_FREQ_SEL	0285 0074h	0286 0074h	2B30 0074h
78h	32	UART_ABAUD_1ST_CHAR	0285 0078h	0286 0078h	2B30 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0285 007Ch	0286 007Ch	2B30 007Ch
80h	32	UART_MDR3	0285 0080h	0286 0080h	2B30 0080h
84h	32	UART_TX_DMA_THRESHOLD	0285 0084h	0286 0084h	2B30 0084h
88h	32	UART_MDR4	0285 0088h	0286 0088h	2B30 0088h
8Ch	32	UART_EFR2	0285 008Ch	0286 008Ch	2B30 008Ch
90h	32	UART_ECR	0285 0090h	0286 0090h	2B30 0090h
94h	32	UART_TIMEGUARD	0285 0094h	0286 0094h	2B30 0094h
98h	32	UART_TIMEOUTL	0285 0098h	0286 0098h	2B30 0098h
9Ch	32	UART_TIMEOUTH	0285 009Ch	0286 009Ch	2B30 009Ch
A0h	32	UART_SCCR	0285 00A0h	0286 00A0h	2B30 00A0h
A4h	32	UART_ERHR	0285 00A4h	0286 00A4h	2B30 00A4h
A4h	32	UART_ETHR	0285 00A4h	0286 00A4h	2B30 00A4h
A8h	32	UART_MAR	0285 00A8h	0286 00A8h	2B30 00A8h
ACh	32	UART_MMR	0285 00ACh	0286 00ACh	2B30 00ACh
B0h	32	UART_MBR	0285 00B0h	0286 00B0h	2B30 00B0h

14.9.2.4.2 UART Registers

UART Registers

14.9.2.4.2.1 UART_DLL Register

1 UART_DLL Register (Offset = 0h) [reset = 0h]

Divisor Latches Low Register

Return to Summary Table

Table 14-26521. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**
WKUP_UART0	**2B30 0000h**

Figure 14-8792. UART_DLL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLOCK_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26523. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value Reset Source: mod_g_arstn

14.9.2.4.2.2 UART_RHR Register

1 UART_RHR Register (Offset = 0h) [reset = 0h]

The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.

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Table 14-26524. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**
WKUP_UART0	**2B30 0000h**

Figure 14-8793. UART_RHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RHR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26526. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RHR	R	0h	Receive holding register Reset Source: mod_g_arstn

14.9.2.4.2.3 UART_THR Register

1 UART_THR Register (Offset = 0h) [reset = 0h]

The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

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Table 14-26527. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**
WKUP_UART0	**2B30 0000h**

Figure 14-8794. UART_THR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THR</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26529. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	THR	W	0h	TRANSMIT HOLDING REGISTER Reset Source: mod_g_arstn

14.9.2.4.2.4 UART_DLH Register

1 UART_DLH Register (Offset = 4h) [reset = 0h]

Divisor Latches High Register

Return to Summary Table

Table 14-26530. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**
WKUP_UART0	**2B30 0004h**

Figure 14-8795. UART_DLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_MSB							
R/W							
0h							

Table 14-26532. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value Reset Source: mod_g_arstn

14.9.2.4.2.5 UART_IER_CIR Register

1 UART_IER_CIR Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

Return to Summary Table

Table 14-26533. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**
WKUP_UART0	**2B30 0004h**

Figure 14-8796. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-26535. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	NOT_USED2	R/W	0h	Reset Source: mod_g_arstn

5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn
				`0 Disables the TX status interrupt.`
				`1 Enables the TX status interrupt.`

4	NOT_USED1	R/W	0h	Reset Source: mod_g_arstn

Table 14-26535. UART_IER_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	RX_STOP_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the receive stop interrupt. 1 Enables the receive stop interrupt.
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the THR interrupt. 1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

14.9.2.4.2.6 UART_IER_IRDA Register

1 UART_IER_IRDA Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 14-26536. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**
WKUP_UART0	**2B30 0004h**

Figure 14-8797. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26538. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the received EOF interrupt.` 1 `Enables the received EOF interrupt.`
6	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the receiver line status interrupt.` 1 `Enables the receiver line status interrupt.`

Table 14-26538. UART_IER_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the TX status interrupt. 1 Enables the TX status interrupt.
4	STS_FIFO_TRIG_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the status FIFO trigger level interrupt. 1 Enables the status FIFO trigger level interrupt.
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	LAST_RX_BYTE_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the last byte of frame in RX FIFO interrupt. 1 Enables the last byte of frame in RX FIFO interrupt.
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the THR interrupt. 1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

14.9.2.4.2.7 UART_IER_UART Register

1 UART_IER_UART Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

Return to Summary Table

Table 14-26539. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**
WKUP_UART0	**2B30 0004h**

Figure 14-8798. UART_IER_UART Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26541. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7	CTS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the CTS* interrupt 1 Enables the CTS* interrupt
6	RTS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RTS* interrupt 1 Enables the RTS* interrupt

Table 14-26541. UART_IER_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	XOFF_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the XOFF interrupt 1 Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	Reset Source: mod_g_arstn 0 Disables sleep mode 1 Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the modem status register interrupt 1 Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the receiver line status interrupt 1 Enables the receiver line status interrupt
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the THR interrupt 1 Enables the THR interrupt
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RHR interrupt and time out interrupt. 1 Enables the RHR interrupt and time out interrupt.

14.9.2.4.2.8 UART_EFR Register

1 UART_EFR Register (Offset = 8h) [reset = 0h]

Enhanced Feature Register

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Table 14-26542. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**
WKUP_UART0	**2B30 0008h**

Figure 14-8799. UART_EFR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-26544. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive). Reset Source: mod_g_arstn
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached. Reset Source: mod_g_arstn

Table 14-26544. UART_EFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected. Reset Source: mod_g_arstn
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0: Disables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. Reset Source: mod_g_arstn
3:0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options Reset Source: mod_g_arstn

14.9.2.4.2.9 UART_FCR Register

1 UART_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register
Notes:
Bits 4 and 5 can only be written to when EFR[4] = 1
Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0)
Always make sure that the FIFO is empty when disabling or enabling the FIFO, or reset it if this can't be guaranteed.
See the Transmit FIFO Trigger section of the device TRM for FCR[5:4] setting restriction when SCR[6]=1
See the Recieve FIFO Trigger section of the device TRM for FCR[7:6] setting restriction when SCR[7]=1

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Table 14-26545. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**
WKUP_UART0	**2B30 0008h**

Figure 14-8800. UART_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
W		W		W	W	W	W
0h		0h		0h	0h	0h	0h

Table 14-26547. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-26547. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1. Reset Source: mod_g_arstn
5:4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1 Reset Source: mod_g_arstn
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. Reset Source: mod_g_arstn 0 DMA_MODE 0 (No DMA) 1 DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 0 No change 1 Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 0 No change 1 Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
0	FIFO_EN	W	0h	Reset Source: mod_g_arstn 0 Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs. 1 : Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

14.9.2.4.2.10 UART_IIR_CIR Register

1 UART_IIR_CIR Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 14-26548. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**
WKUP_UART0	**2B30 0008h**

Figure 14-8801. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE		R	NONE	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-26550. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn
				`0 TX status interrupt inactive`
				`1 TX status interrupt active`

4	RESERVED	NONE	0h	Reserved

3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn
				`0 RX overrun interrupt inactive`
				`1 RX overrun interrupt active`

Table 14-26550. UART_IIR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_STOP_IT	R	0h	Reset Source: mod_g_arstn 0 `Receive stop interrupt inactive` 1 `Receive stop interrupt active`
1	THR_IT	R	0h	Reset Source: mod_g_arstn 0 `THR interrupt inactive` 1 `THR interrupt active`
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 0 `RHR interrupt inactive` 1 `RHR interrupt active`

14.9.2.4.2.11 UART_IIR_IRDA Register

1 UART_IIR_IRDA Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 14-26551. Instance Table

Instance Name	Physical Address
MCU_UART0	04A0 0008h
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-8802. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26553. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R	0h	Reset Source: mod_g_arstn 0 Received EOF interrupt inactive 1 Received EOF interrupt active
6	LINE_STS_IT	R	0h	Reset Source: mod_g_arstn 0 Receiver line status interrupt inactive 1 Receiver line status interrupt active

Table 14-26553. UART_IIR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn 0 `TX status interrupt inactive` 1 `TX status interrupt active`
4	STS_FIFO_IT	R	0h	Reset Source: mod_g_arstn 0 `Status FIFO trigger level interrupt inactive` 1 `Status FIFO trigger level interrupt active`
3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn 0 `RX overrun interrupt inactive` 1 `RX overrun interrupt active`
2	RX_FIFO_LAST_BYTE_IT	R	0h	Reset Source: mod_g_arstn 0 `Last byte of frame in RX FIFO interrupt inactive` 1 `Last byte of frame in RX FIFO interrupt active`
1	THR_IT	R	0h	Reset Source: mod_g_arstn 0 `THR interrupt inactive` 1 `THR interrupt active`
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 0 `RHR interrupt inactive` 1 `RHR interrupt active`

14.9.2.4.2.12 UART_IIR_UART Register

1 UART_IIR_UART Register (Offset = 8h) [reset = 1h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 14-26554. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**
WKUP_UART0	**2B30 0008h**

Figure 14-8803. UART_IIR_UART Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FCR_MIRROR</td><td colspan="5">IT_TYPE</td><td>IT_PENDING</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">0h</td><td>1h</td></tr>
</table>

Table 14-26556. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits. Reset Source: mod_g_arstn

5:1	IT_TYPE	R	0h	Reset Source: mod_g_arstn
				`0      Modem Interrupt. Priority=4`
				`1      THR interrupt.  Priority=3`
				`2      RHR interrupt.  Priority=2`
				`3      Receiver line status error.  Priority=3`
				`6      Rx timeout.  Priority=2`
				`8      Xoff/Special character.  Priority=5`
				`16     CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6`

Table 14-26556. UART_IIR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IT_PENDING	R	1h	Reset Source: mod_g_arstn 0 An interrupt is pending 1 No interrupt is pending

14.9.2.4.2.13 UART_LCR Register

1 UART_LCR Register (Offset = Ch) [reset = 0h]

LCR[6:0] define parameters of the transmission and reception. Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

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Table 14-26557. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 000Ch**
UART0	**0280 000Ch**
UART1	**0281 000Ch**
UART2	**0282 000Ch**
UART3	**0283 000Ch**
UART4	**0284 000Ch**
UART5	**0285 000Ch**
UART6	**0286 000Ch**
WKUP_UART0	**2B30 000Ch**

Figure 14-8804. UART_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIV_EN	BREAK_EN	PARITY_TYPE 2	PARITY_TYPE 1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-26559. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	DIV_EN	R/W	0h	Reset Source: mod_g_arstn 0 Normal operating condition 1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)

Table 14-26559. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BREAK_EN	R/W	0h	Break control bit. Reset Source: mod_g_arstn 0 Normal operating condition. 1 Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data. Reset Source: mod_g_arstn
4	PARITY_TYPE1	R/W	0h	Reset Source: mod_g_arstn 0 Odd parity is generated (if LCR[3] = 1) 1 Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	R/W	0h	Reset Source: mod_g_arstn 0 No parity 1 A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: Reset Source: mod_g_arstn 0 1 stop bits (word length = 5, 6, 7, 8) 1 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1:0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. Reset Source: mod_g_arstn 0 5 bits 1 6 bits 2 7 bits 3 8 bits

14.9.2.4.2.14 UART_MCR Register

1 UART_MCR Register (Offset = 10h) [reset = 0h]

MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

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Table 14-26560. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0010h**
UART0	**0280 0010h**
UART1	**0281 0010h**
UART2	**0282 0010h**
UART3	**0283 0010h**
UART4	**0284 0010h**
UART5	**0285 0010h**
UART6	**0286 0010h**
WKUP_UART0	**2B30 0010h**

Figure 14-8805. UART_MCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>TCR_TLR</td><td>XON_EN</td><td>LOOPBACK_EN</td><td>CD_STS_CH</td><td>RI_STS_CH</td><td>RTS</td><td>DTR</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26562. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RESERVED	R	0h	
6	TCR_TLR	R/W	0h	Reset Source: mod_g_arstn 0 No action 1 Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	Reset Source: mod_g_arstn 0 Disable 'XON any' function 1 Enable 'XON any' function

Table 14-26562. UART_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOOPBACK_EN	R/W	0h	Reset Source: mod_g_arstn 0 Normal operating mode 1 Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally
3	CD_STS_CH	R/W	0h	Reset Source: mod_g_arstn 0 In loopback forces DCD* input high and IRQ outputs to inactive state. 1 In loopback forces DCD* input low and IRQ outputs to inactive state.
2	RI_STS_CH	R/W	0h	Reset Source: mod_g_arstn 0 In loopback forces RI* input high. 1 In loopback forces RI* input low.
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. Reset Source: mod_g_arstn 0 Force RTS* output to inactive (high). 1 Force RTS* output to active (low).
0	DTR	R/W	0h	Reset Source: mod_g_arstn 0 Force DTR* output to inactive (high). 1 Force DTR* output to active (low).

14.9.2.4.2.15 UART_XON1_ADDR1 Register

1 UART_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

XON1/ADDR1 Register

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Table 14-26563. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0010h**
UART0	**0280 0010h**
UART1	**0281 0010h**
UART2	**0282 0010h**
UART3	**0283 0010h**
UART4	**0284 0010h**
UART5	**0285 0010h**
UART6	**0286 0010h**
WKUP_UART0	**2B30 0010h**

Figure 14-8806. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD1							
R/W							
0h							

Table 14-26565. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes. Reset Source: mod_g_arstn

14.9.2.4.2.16 UART_LSR_CIR Register

1 UART_LSR_CIR Register (Offset = 14h) [reset = 81h]

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Table 14-26566. Instance Table

Instance Name	Physical Address
MCU_UART0	04A0 0014h
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
WKUP_UART0	2B30 0014h

Figure 14-8807. UART_LSR_CIR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>THR_EMPTY</td><td>RESERVED</td><td>RX_STOP</td><td colspan="4">RESERVED</td><td>RX_FIFO_E</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td colspan="4">NONE</td><td>R</td></tr>
<tr><td>1h</td><td>0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 14-26568. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 0 `Transmit holding register (TX FIFO) is not empty` 1 `Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed`
6	RESERVED	R	0h	

Table 14-26568. UART_LSR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register Reset Source: mod_g_arstn 0 `Reception is on going or waiting for a new frame` 1 `Reception is completed`
4:1	RESERVED	NONE	0h	Reserved
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 `No data in the receive FIFO` 1 `At least one data character in the RX FIFO`

14.9.2.4.2.17 UART_LSR_IRDA Register

1 UART_LSR_IRDA Register (Offset = 14h) [reset = 83h]

Return to Summary Table

Table 14-26569. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**
WKUP_UART0	**2B30 0014h**

Figure 14-8808. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	1h	1h

Table 14-26571. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 0 Transmit holding register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 0 Status FIFO not full 1 Status FIFO full

Table 14-26571. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_LAST_BYTE	R	0h	Reset Source: mod_g_arstn 0 The RX FIFO (RHR) does not contain the last byte of the frame to be read 1 The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register
4	FRAME_TOO_LONG	R	0h	Reset Source: mod_g_arstn 0 No frame-too-long error in frame 1 Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	R	0h	Reset Source: mod_g_arstn 0 No abort pattern error in frame 1 Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol
2	CRC	R	0h	Reset Source: mod_g_arstn 0 No CRC error in frame 1 CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 Status FIFO not empty 1 Status FIFO empty
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 No data in the receive FIFO 1 At least one data character in the RX FIFO

14.9.2.4.2.18 UART_LSR_UART Register

1 UART_LSR_UART Register (Offset = 14h) [reset = 60h]

Return to Summary Table

Table 14-26572. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**
WKUP_UART0	**2B30 0014h**

Figure 14-8809. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-26574. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_FIFO_STS	R	0h	Reset Source: mod_g_arstn 0 `Normal operation` 1 `At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.`
6	TX_SR_E	R	1h	Reset Source: mod_g_arstn 0 `Transmitter hold (TX FIFO) and shift registers are not empty.` 1 `Transmitter hold (TX FIFO) and shift registers are empty`

Table 14-26574. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 `Transmit hold register (TX FIFO) is not empty` 1 `Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.`
4	RX_BI	R	0h	Reset Source: mod_g_arstn 0 `No break condition` 1 `A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).`
3	RX_FE	R	0h	Reset Source: mod_g_arstn 0 `No framing error in data being read from RX FIFO.` 1 `Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)`
2	RX_PE	R	0h	Reset Source: mod_g_arstn 0 `No parity error in data being read from RX FIFO.` 1 `Parity error in data being read from RX FIFO`
1	RX_OE	R	0h	Reset Source: mod_g_arstn 0 `No overrun error` 1 `Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.`
0	RX_FIFO_E	R	0h	Reset Source: mod_g_arstn 0 `No data in the receive FIFO` 1 `At least one data character in the RX FIFO`

14.9.2.4.2.19 UART_XON2_ADDR2 Register

1 UART_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

XON2/ADDR2 Register

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Table 14-26575. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**
WKUP_UART0	**2B30 0014h**

Figure 14-8810. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD2							
R/W							
0h							

Table 14-26577. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes. Reset Source: mod_g_arstn

14.9.2.4.2.20 UART_MSR Register

1 UART_MSR Register (Offset = 18h) [reset = 0h]

This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

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Table 14-26578. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**
WKUP_UART0	**2B30 0018h**

Figure 14-8811. UART_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26580. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3] Reset Source: mod_g_arstn
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2] Reset Source: mod_g_arstn
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0] Reset Source: mod_g_arstn

Table 14-26580. UART_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1] Reset Source: mod_g_arstn
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read. Reset Source: mod_g_arstn
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read. Reset Source: mod_g_arstn
1	DSR_STS	R	0h	Reset Source: mod_g_arstn 1 `Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read`
0	CTS_STS	R	0h	Reset Source: mod_g_arstn 1 `Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.`

14.9.2.4.2.21 UART_TCR Register

1 UART_TCR Register (Offset = 18h) [reset = Fh]

Transmission Control Register

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Table 14-26581. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**
WKUP_UART0	**2B30 0018h**

Figure 14-8812. UART_TCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RX_FIFO_TRIG_START</td><td colspan="4">RX_FIFO_TRIG_HALT</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-26583. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60) Reset Source: mod_g_arstn
3:0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60) Reset Source: mod_g_arstn

14.9.2.4.2.22 UART_XOFF1 Register

1 UART_XOFF1 Register (Offset = 18h) [reset = 0h]

XOFF1 Register

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Table 14-26584. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**
WKUP_UART0	**2B30 0018h**

Figure 14-8813. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD1							
R/W							
0h							

Table 14-26586. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes. Reset Source: mod_g_arstn

14.9.2.4.2.23 UART_SPR Register

1 UART_SPR Register (Offset = 1Ch) [reset = 0h]

This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

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Table 14-26587. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**
WKUP_UART0	**2B30 001Ch**

Figure 14-8814. UART_SPR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SPR_WORD							
R/W							
0h							

Table 14-26589. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SPR_WORD	R/W	0h	Scratchpad register Reset Source: mod_g_arstn

14.9.2.4.2.24 UART_TLR Register

1 UART_TLR Register (Offset = 1Ch) [reset = 0h]

Trigger Level Register

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Table 14-26590. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**
WKUP_UART0	**2B30 001Ch**

Figure 14-8815. UART_TLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RX_FIFO_TRIG_DMA</td><td colspan="4">TX_FIFO_TRIG_DMA</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26592. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level Reset Source: mod_g_arstn
3:0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level Reset Source: mod_g_arstn

14.9.2.4.2.25 UART_XOFF2 Register

1 UART_XOFF2 Register (Offset = 1Ch) [reset = 0h]

XOFF2 Register

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Table 14-26593. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**
WKUP_UART0	**2B30 001Ch**

Figure 14-8816. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD2							
R/W							
0h							

Table 14-26595. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes. Reset Source: mod_g_arstn

14.9.2.4.2.26 UART_MDR1 Register

1 UART_MDR1 Register (Offset = 20h) [reset = 7h]

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation.
Note: If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (UART_IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (UART_IIR) shows UART mode interrupt flags.

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Table 14-26596. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0020h**
UART0	**0280 0020h**
UART1	**0281 0020h**
UART2	**0282 0020h**
UART3	**0283 0020h**
UART4	**0284 0020h**
UART5	**0285 0020h**
UART6	**0286 0020h**
WKUP_UART0	**2B30 0020h**

Figure 14-8817. UART_MDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	7h		

Table 14-26598. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	FRAME_END_MODE	R/W	0h	IrDA mode only. Reset Source: mod_g_arstn 0 `Frame-length method` 1 `Set EOT bit method`

Table 14-26598. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SIP_MODE	R/W	0h	MIR/FIR modes only. Reset Source: mod_g_arstn 0 Manual SIP mode: SIP is generated with the control of ACREG[3] 1 Automatic SIP mode: SIP is generated after each transmission.
5	SCT	R/W	0h	Store and control the transmission Reset Source: mod_g_arstn 0 Starts the Infrared transmission as soon as a value is written to THR 1 Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. Reset Source: mod_g_arstn 0 No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1 1 TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	R/W	0h	Reset Source: mod_g_arstn 0 IrDA/CIR sleep mode disabled 1 IrDA/CIR sleep mode enabled
2:0	MODE_SELECT	R/W	7h	Reset Source: mod_g_arstn 0 UART 16x mode 1 SIR mode 2 UART 16x auto-baud 3 UART 13x mode 4 MIR mode 5 FIR mode 6 CIR mode 7 Disable (default state)

14.9.2.4.2.27 UART_MDR2 Register

1 UART_MDR2 Register (Offset = 24h) [reset = 0h]

IR-IrDA and IR-CIR modes only. MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0]. Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

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Table 14-26599. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0024h**
UART0	**0280 0024h**
UART1	**0281 0024h**
UART2	**0282 0024h**
UART3	**0283 0024h**
UART4	**0284 0024h**
UART5	**0285 0024h**
UART6	**0286 0024h**
WKUP_UART0	**2B30 0024h**

Figure 14-8818. UART_MDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R/W	R/W	R/W		R/W	R/W		R
0h	0h	0h		0h	0h		0h

Table 14-26601. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] Reset Source: mod_g_arstn 0 Normal mode 1 Alternate mode for SET_TXIR

Table 14-26601. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. Reset Source: mod_g_arstn 0 inversion is performed 1 No inversion is performed
5:4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: Reset Source: mod_g_arstn 0 Pulse width of 3 from 12 cycles 1 Pulse width of 4 from 12 cycles 2 Pulse width of 5 from 12 cycles 3 Pulse width of 6 from 12 cycles
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. Reset Source: mod_g_arstn 0 normal UART mode 1 UART mode with a pulse shaping
2:1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: Reset Source: mod_g_arstn 0 1 entry 1 4 entries 2 7 entries 3 8 entries
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : Reset Source: mod_g_arstn 0 the last bit of the frame has been transmitted successfully without error. 1 an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.

14.9.2.4.2.28 UART_SFLSR Register

1 UART_SFLSR Register (Offset = 28h) [reset = 0h]

IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

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Table 14-26602. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0028h**
UART0	**0280 0028h**
UART1	**0281 0028h**
UART2	**0282 0028h**
UART3	**0283 0028h**
UART4	**0284 0028h**
UART5	**0285 0028h**
UART6	**0286 0028h**
WKUP_UART0	**2B30 0028h**

Figure 14-8819. UART_SFLSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 14-26604. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED5	R	0h	
4	OE_ERROR	R	0h	Reset Source: mod_g_arstn 1 `Overrun error in RX FIFO when frame at top of RX FIFO was received.`
3	FRAME_TOO_LONG_ERROR	R	0h	Reset Source: mod_g_arstn 1 `Frame-length too long error in frame at top of RX FIFO.`

Table 14-26604. UART_SFLSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ABORT_DETECT	R	0h	Reset Source: mod_g_arstn 1 `Abort pattern detected in frame at top of RX FIFO`
1	CRC_ERROR	R	0h	Reset Source: mod_g_arstn 1 `CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO`
0	RESERVED0	R	0h	

14.9.2.4.2.29 UART_TXFLL Register

1 UART_TXFLL Register (Offset = 28h) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-26605. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0028h**
UART0	**0280 0028h**
UART1	**0281 0028h**
UART2	**0282 0028h**
UART3	**0283 0028h**
UART4	**0284 0028h**
UART5	**0285 0028h**
UART6	**0286 0028h**
WKUP_UART0	**2B30 0028h**

Figure 14-8820. UART_TXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
TXFLL							
W							
0h							

Table 14-26607. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	TXFLL	W	0h	LSB register used to specify the frame length Reset Source: mod_g_arstn

14.9.2.4.2.30 UART_RESUME Register

1 UART_RESUME Register (Offset = 2Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

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Table 14-26608. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 002Ch**
UART0	**0280 002Ch**
UART1	**0281 002Ch**
UART2	**0282 002Ch**
UART3	**0283 002Ch**
UART4	**0284 002Ch**
UART5	**0285 002Ch**
UART6	**0286 002Ch**
WKUP_UART0	**2B30 002Ch**

Figure 14-8821. UART_RESUME Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESUME							
R							
0h							

Table 14-26610. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RESUME	R	0h	Dummy read to restart the TX or RX Reset Source: mod_g_arstn

14.9.2.4.2.31 UART_TXFLH Register

1 UART_TXFLH Register (Offset = 2Ch) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-26611. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 002Ch**
UART0	**0280 002Ch**
UART1	**0281 002Ch**
UART2	**0282 002Ch**
UART3	**0283 002Ch**
UART4	**0284 002Ch**
UART5	**0285 002Ch**
UART6	**0286 002Ch**
WKUP_UART0	**2B30 002Ch**

Figure 14-8822. UART_TXFLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TXFLH</td></tr>
<tr><td colspan="3">R</td><td colspan="5">W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-26613. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	
4:0	TXFLH	W	0h	MSB register used to specify the frame length Reset Source: mod_g_arstn

14.9.2.4.2.32 UART_RXFLL Register

1 UART_RXFLL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-26614. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0030h**
UART0	**0280 0030h**
UART1	**0281 0030h**
UART2	**0282 0030h**
UART3	**0283 0030h**
UART4	**0284 0030h**
UART5	**0285 0030h**
UART6	**0286 0030h**
WKUP_UART0	**2B30 0030h**

Figure 14-8823. UART_RXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RXFLL							
W							
0h							

Table 14-26616. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RXFLL	W	0h	LSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.9.2.4.2.33 UART_SFREGL Register

1 UART_SFREGL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-26617. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0030h**
UART0	**0280 0030h**
UART1	**0281 0030h**
UART2	**0282 0030h**
UART3	**0283 0030h**
UART4	**0284 0030h**
UART5	**0285 0030h**
UART6	**0286 0030h**
WKUP_UART0	**2B30 0030h**

Figure 14-8824. UART_SFREGL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SFREGL							
R							
0h							

Table 14-26619. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SFREGL	R	0h	LSB part of the frame length Reset Source: mod_g_arstn

14.9.2.4.2.34 UART_RXFLH Register

1 UART_RXFLH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-26620. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0034h**
UART0	**0280 0034h**
UART1	**0281 0034h**
UART2	**0282 0034h**
UART3	**0283 0034h**
UART4	**0284 0034h**
UART5	**0285 0034h**
UART6	**0286 0034h**
WKUP_UART0	**2B30 0034h**

Figure 14-8825. UART_RXFLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RXFLH</td></tr>
<tr><td colspan="4">R</td><td colspan="4">W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26622. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	RXFLH	W	0h	MSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.9.2.4.2.35 UART_SFREGH Register

1 UART_SFREGH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-26623. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0034h**
UART0	**0280 0034h**
UART1	**0281 0034h**
UART2	**0282 0034h**
UART3	**0283 0034h**
UART4	**0284 0034h**
UART5	**0285 0034h**
UART6	**0286 0034h**
WKUP_UART0	**2B30 0034h**

Figure 14-8826. UART_SFREGH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				SFREGH			
R				R			
0h				0h			

Table 14-26625. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	SFREGH	R	0h	MSB part of the frame length Reset Source: mod_g_arstn

14.9.2.4.2.36 UART_BLR Register

1 UART_BLR Register (Offset = 38h) [reset = 40h]

IrDA modes only. Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

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Table 14-26626. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0038h**
UART0	**0280 0038h**
UART1	**0281 0038h**
UART2	**0282 0038h**
UART3	**0283 0038h**
UART4	**0284 0038h**
UART5	**0285 0038h**
UART6	**0286 0038h**
WKUP_UART0	**2B30 0038h**

Figure 14-8827. UART_BLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R/W1TS	R/W	R					
0h	1h	0h					

Table 14-26628. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing Reset Source: mod_g_arstn
6	XBOF_TYPE	R/W	1h	SIR xBOF select. Reset Source: mod_g_arstn 0 0xFF 1 0xC0

Table 14-26628. UART_BLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	RESERVED	R	0h	

14.9.2.4.2.37 UART_UASR Register

1 UART_UASR Register (Offset = 38h) [reset = 0h]

UART Autobauding Status Register

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Table 14-26629. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0038h**
UART0	**0280 0038h**
UART1	**0281 0038h**
UART2	**0282 0038h**
UART3	**0283 0038h**
UART4	**0284 0038h**
UART5	**0285 0038h**
UART6	**0286 0038h**
WKUP_UART0	**2B30 0038h**

Figure 14-8828. UART_UASR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PARITY_TYPE		BIT_BY_CHAR	SPEED				
R		R	R				
0h		0h	0h				

Table 14-26631. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity Reset Source: mod_g_arstn
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified Reset Source: mod_g_arstn

Table 14-26631. UART_UASR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds Reset Source: mod_g_arstn

14.9.2.4.2.38 UART_ACREG Register

1 UART_ACREG Register (Offset = 3Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

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Table 14-26632. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 003Ch**
UART0	**0280 003Ch**
UART1	**0281 003Ch**
UART2	**0282 003Ch**
UART3	**0283 003Ch**
UART4	**0284 003Ch**
UART5	**0285 003Ch**
UART6	**0286 003Ch**
WKUP_UART0	**2B30 003Ch**

Figure 14-8829. UART_ACREG Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26634. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	PULSE_TYPE	R/W	0h	SIR pulse width select: Reset Source: mod_g_arstn 0 3/16 of baud-rate pulse width 1 1.6us
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. Reset Source: mod_g_arstn 0 SD pin is set to high 1 SD pin is set to low

Table 14-26634. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DIS_IR_RX	R/W	0h	Reset Source: mod_g_arstn 0 Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation). 1 Disables RX input (permanent state - independent of transmit).
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. Reset Source: mod_g_arstn 0 Long stop bits cannot be transmitted, TX underrun is enabled 1 Long stop bits can be transmitted, TX underrun is disabled
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. Reset Source: mod_g_arstn 0 No action 1 Send SIP pulse.
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing. Reset Source: mod_g_arstn
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by Writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame. Reset Source: mod_g_arstn
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO]. Reset Source: mod_g_arstn

14.9.2.4.2.39 UART_SCR Register

1 UART_SCR Register (Offset = 40h) [reset = 0h]

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

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Table 14-26635. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0040h**
UART0	**0280 0040h**
UART1	**0281 0040h**
UART2	**0282 0040h**
UART3	**0283 0040h**
UART4	**0284 0040h**
UART5	**0285 0040h**
UART6	**0286 0040h**
WKUP_UART0	**2B30 0040h**

Figure 14-8830. UART_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

Table 14-26637. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. 1 ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.

Table 14-26637. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL. 1 Enables the granularity of 1 for trigger TX level.
5	DSR_IT	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES DSR* INTERRUPT. 1 ENABLES DSR* INTERRUPT.
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1]. 1 Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	Reset Source: mod_g_arstn 0 Normal mode for THR interrupt (See UART mode interrupts table). 1 THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2:1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 Reset Source: mod_g_arstn 0 DMA mode 0 (no DMA) 1 DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 2 DMA mode 2 (UART_nDMA_REQ[0] in RX) 3 DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	R/W	0h	Reset Source: mod_g_arstn 0 The DMA_MODE is set with FCR[3] 1 The DMA_MODE is set with SCR[2:1]

14.9.2.4.2.40 UART_SSR Register

1 UART_SSR Register (Offset = 44h) [reset = 4h]

Note: Bit 1 is reset only when SCR[4] is reset to 0.

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Table 14-26638. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0044h**
UART0	**0280 0044h**
UART1	**0281 0044h**
UART2	**0282 0044h**
UART3	**0283 0044h**
UART4	**0284 0044h**
UART5	**0285 0044h**
UART6	**0286 0044h**
WKUP_UART0	**2B30 0044h**

Figure 14-8831. UART_SSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R					R/W	R	R
0h					1h	0h	0h

Table 14-26640. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:3	RESERVED	R	0h	
2	DMA_COUNTER_RST	R/W	1h	Reset Source: mod_g_arstn 0 `The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2])` 1 `The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])`

Table 14-26640. UART_SSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	Reset Source: mod_g_arstn 0 `No falling edge event on RX, CTS* and DSR*` 1 `A falling edge occurred on RX, CTS* or DSR*`
0	TX_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 0 `TX FIFO is not full` 1 `TX FIFO is full.`

14.9.2.4.2.41 UART_EBLR Register

1 UART_EBLR Register (Offset = 48h) [reset = 0h]

IR-IrDA and IR-CIR modes only.
In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.
In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).
In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the UART_ACREG[5] to 1.
Note: If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.

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Table 14-26641. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0048h**
UART0	**0280 0048h**
UART1	**0281 0048h**
UART2	**0282 0048h**
UART3	**0283 0048h**
UART4	**0284 0048h**
UART5	**0285 0048h**
UART6	**0286 0048h**
WKUP_UART0	**2B30 0048h**

Figure 14-8832. UART_EBLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
EBLR							
R/W							
0h							

Table 14-26643. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-26643. UART_EBLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits. Reset Source: mod_g_arstn

14.9.2.4.2.42 UART_MVR Register

1 UART_MVR Register (Offset = 50h) [reset = 47424E03h]

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned Notes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification). For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

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Table 14-26644. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0050h**
UART0	**0280 0050h**
UART1	**0281 0050h**
UART2	**0282 0050h**
UART3	**0283 0050h**
UART4	**0284 0050h**
UART5	**0285 0050h**
UART6	**0286 0050h**
WKUP_UART0	**2B30 0050h**

Figure 14-8833. UART_MVR Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		742h			
23	22	21	20	19	18	17	16
FUNC							
R							
742h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					6h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		3h					

Table 14-26646. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme revision number of module Reset Source: mod_g_arstn
29:28	RESERVED	R	0h	
27:16	FUNC	R	742h	Function revision number of module Reset Source: mod_g_arstn

Table 14-26646. UART_MVR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:11	RTL	R	9h	Rtl revision number of module Reset Source: mod_g_arstn
10:8	MAJOR	R	6h	Major revision number of the module. Reset Source: mod_g_arstn
7:6	CUSTOM	R	0h	Custom revision number of the module. Reset Source: mod_g_arstn
5:0	MINOR	R	3h	Minor revision number of the module. Reset Source: mod_g_arstn

14.9.2.4.2.43 UART_SYSC Register

1 UART_SYSC Register (Offset = 54h) [reset = 0h]

The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

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Table 14-26647. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0054h**
UART0	**0280 0054h**
UART1	**0281 0054h**
UART2	**0282 0054h**
UART3	**0283 0054h**
UART4	**0284 0054h**
UART5	**0285 0054h**
UART6	**0286 0054h**
WKUP_UART0	**2B30 0054h**

Figure 14-8834. UART_SYSC Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	W	R/W
0h			0h		0h	0h	0h

Table 14-26649. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	

Table 14-26649. UART_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 Reset Source: mod_g_arstn 0 Force idle. An idle request is acknowledged unconditionally 1 No-idle. An idle request is never acknowledged. 2 Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module. 3 reserved
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL Reset Source: mod_g_arstn 0 Wake up is disabled 1 Wake up capability is enabled
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. Reset Source: mod_g_arstn 0 Normal mode 1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: mod_g_arstn 0 Clock is running 1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

14.9.2.4.2.44 UART_SYSS Register

1 UART_SYSS Register (Offset = 58h) [reset = 0h]

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Table 14-26650. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0058h**
UART0	**0280 0058h**
UART1	**0281 0058h**
UART2	**0282 0058h**
UART3	**0283 0058h**
UART4	**0284 0058h**
UART5	**0285 0058h**
UART6	**0286 0058h**
WKUP_UART0	**2B30 0058h**

Figure 14-8835. UART_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 14-26652. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:1	RESERVED	R	0h	

0	RESETDONE	R	0h	Internal Reset Monitoring
				Reset Source: mod_g_arstn
				`0 Internal Module Reset is ongoing`
				`1 Reset completed`

14.9.2.4.2.45 UART_WER Register

1 UART_WER Register (Offset = 5Ch) [reset = FFh]

The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

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Table 14-26653. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 005Ch**
UART0	**0280 005Ch**
UART1	**0281 005Ch**
UART2	**0282 005Ch**
UART3	**0283 005Ch**
UART4	**0284 005Ch**
UART5	**0285 005Ch**
UART6	**0286 005Ch**
WKUP_UART0	**2B30 005Ch**

Figure 14-8836. UART_WER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>EVENT_7_TX_WAKEUP_EN</td><td>EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT</td><td>EVENT_5_RHR_INTERRUPT</td><td>EVENT_4_RX_ACTIVITY</td><td>EVENT_3_DCD_CD_ACTIVITY</td><td>EVENT_2_RI_ACTIVITY</td><td>EVENT_1_DSR_ACTIVITY</td><td>EVENT_0_CTS_ACTIVITY</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-26655. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	Reset Source: mod_g_arstn 0 `Event is not allowed to wake up the system` 1 `EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT`

Table 14-26655. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
4	EVENT_4_RX_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
1	EVENT_1_DSR_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system

14.9.2.4.2.46 UART_CFPS Register

1 UART_CFPS Register (Offset = 60h) [reset = 69h]

Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

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Table 14-26656. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0060h**
UART0	**0280 0060h**
UART1	**0281 0060h**
UART2	**0282 0060h**
UART3	**0283 0060h**
UART4	**0284 0060h**
UART5	**0285 0060h**
UART6	**0286 0060h**
WKUP_UART0	**2B30 0060h**

Figure 14-8837. UART_CFPS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
CFPS							
R/W							
69h							

Table 14-26658. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-26658. UART_CFPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CFPS	R/W	69h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported. Reset Source: mod_g_arstn

14.9.2.4.2.47 UART_RXFIFO_LVL Register

1 UART_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Level of the RX FIFO

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Table 14-26659. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0064h**
UART0	**0280 0064h**
UART1	**0281 0064h**
UART2	**0282 0064h**
UART3	**0283 0064h**
UART4	**0284 0064h**
UART5	**0285 0064h**
UART6	**0286 0064h**
WKUP_UART0	**2B30 0064h**

Figure 14-8838. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
RXFIFO_LVL							
R							
0h							

Table 14-26661. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	RXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.9.2.4.2.48 UART_TXFIFO_LVL Register

1 UART_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Level of the TX FIFO

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Table 14-26662. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0068h**
UART0	**0280 0068h**
UART1	**0281 0068h**
UART2	**0282 0068h**
UART3	**0283 0068h**
UART4	**0284 0068h**
UART5	**0285 0068h**
UART6	**0286 0068h**
WKUP_UART0	**2B30 0068h**

Figure 14-8839. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
TXFIFO_LVL							
R							
0h							

Table 14-26664. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	TXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.9.2.4.2.49 UART_IER2 Register

1 UART_IER2 Register (Offset = 6Ch) [reset = 0h]

Enables RX/TX FIFOs empty corresponding interrupts.

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Table 14-26665. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 006Ch**
UART0	**0280 006Ch**
UART1	**0281 006Ch**
UART2	**0282 006Ch**
UART3	**0283 006Ch**
UART4	**0284 006Ch**
UART5	**0285 006Ch**
UART6	**0286 006Ch**
WKUP_UART0	**2B30 006Ch**

Figure 14-8840. UART_IER2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-26667. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:3	RESERVED	R	0h	
2	RHR_IT_DIS	R/W	0h	Reset Source: mod_g_arstn 0 Enables the RHR interrupt. 1 Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn

14.9.2.4.2.50 UART_ISR2 Register

1 UART_ISR2 Register (Offset = 70h) [reset = 3h]

Status of RX/TX FIFOs empty corresponding interrupts.

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Table 14-26668. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0070h**
UART0	**0280 0070h**
UART1	**0281 0070h**
UART2	**0282 0070h**
UART3	**0283 0070h**
UART4	**0284 0070h**
UART5	**0285 0070h**
UART6	**0286 0070h**
WKUP_UART0	**2B30 0070h**

Figure 14-8841. UART_ISR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
R						R/W1TC	R/W1TC
0h						1h	1h

Table 14-26670. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:2	RESERVED	R	0h	
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending Reset Source: mod_g_arstn 0 `TXFIFO_EMPTY interrupt not pending.` 1 `TXFIFO_EMPTY interrupt pending.`

Table 14-26670. UART_ISR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending Reset Source: mod_g_arstn 0 `RXFIFO_EMPTY interrupt not pending.` 1 `RXFIFO_EMPTY interrupt pending.`

14.9.2.4.2.51 UART_FREQ_SEL Register

1 UART_FREQ_SEL Register (Offset = 74h) [reset = 1Ah]

Sample per bit value selector

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Table 14-26671. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0074h**
UART0	**0280 0074h**
UART1	**0281 0074h**
UART2	**0282 0074h**
UART3	**0283 0074h**
UART4	**0284 0074h**
UART5	**0285 0074h**
UART6	**0286 0074h**
WKUP_UART0	**2B30 0074h**

Figure 14-8842. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
FREQ_SEL							
R/W							
1Ah							

Table 14-26673. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	RESERVED
7:0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6. Reset Source: mod_g_arstn

14.9.2.4.2.52 UART_ABAUD_1ST_CHAR Register

1 UART_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Unused

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Table 14-26674. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0078h**
UART0	**0280 0078h**
UART1	**0281 0078h**
UART2	**0282 0078h**
UART3	**0283 0078h**
UART4	**0284 0078h**
UART5	**0285 0078h**
UART6	**0286 0078h**
WKUP_UART0	**2B30 0078h**

Figure 14-8843. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26676. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.9.2.4.2.53 UART_BAUD_2ND_CHAR Register

1 UART_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Unused

Return to Summary Table

Table 14-26677. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 007Ch**
UART0	**0280 007Ch**
UART1	**0281 007Ch**
UART2	**0282 007Ch**
UART3	**0283 007Ch**
UART4	**0284 007Ch**
UART5	**0285 007Ch**
UART6	**0286 007Ch**
WKUP_UART0	**2B30 007Ch**

Figure 14-8844. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26679. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.9.2.4.2.54 UART_MDR3 Register

1 UART_MDR3 Register (Offset = 80h) [reset = 0h]

Mode definition register 3.

Return to Summary Table

Table 14-26680. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0080h**
UART0	**0280 0080h**
UART1	**0281 0080h**
UART2	**0282 0080h**
UART3	**0283 0080h**
UART4	**0284 0080h**
UART5	**0285 0080h**
UART6	**0286 0080h**
WKUP_UART0	**2B30 0080h**

Figure 14-8845. UART_MDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-26682. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	
7:5	RESERVED1	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable Reset Source: mod_g_arstn
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0 Reset Source: mod_g_arstn
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD] Reset Source: mod_g_arstn

Table 14-26682. UART_MDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies Reset Source: mod_g_arstn

0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation
				Reset Source: mod_g_arstn
				`0 Enables CIR RX demodulation`
				`1 Disables CIR RX demodulation`

14.9.2.4.2.55 UART_TX_DMA_THRESHOLD Register

1 UART_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Use to manually set the TX DMA threshold level. MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size). If not, 64-tx_trigger_level will be used w/o modifying the value of this register.

Return to Summary Table

Table 14-26683. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0084h**
UART0	**0280 0084h**
UART1	**0281 0084h**
UART2	**0282 0084h**
UART3	**0283 0084h**
UART4	**0284 0084h**
UART5	**0285 0084h**
UART6	**0286 0084h**
WKUP_UART0	**2B30 0084h**

Figure 14-8846. UART_TX_DMA_THRESHOLD Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		TX_DMA_THRESHOLD					
R		R/W					
0h		0h					

Table 14-26685. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	RESERVED
7:6	RESERVED	R	0h	Reserved
5:0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level. Reset Source: mod_g_arstn

14.9.2.4.2.56 UART_MDR4 Register

1 UART_MDR4 Register (Offset = 88h) [reset = 0h]

Mode definition register 4

Return to Summary Table

Table 14-26686. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0088h**
UART0	**0280 0088h**
UART1	**0281 0088h**
UART2	**0282 0088h**
UART3	**0283 0088h**
UART4	**0284 0088h**
UART5	**0285 0088h**
UART6	**0286 0088h**
WKUP_UART0	**2B30 0088h**

Figure 14-8847. UART_MDR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>MODE9</td><td colspan="3">FREQ_SEL_H</td><td colspan="3">MODE</td></tr>
<tr><td>R</td><td>R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-26688. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	RESERVED	R	0h	
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR Reset Source: mod_g_arstn
5:3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode Reset Source: mod_g_arstn

Table 14-26688. UART_MDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] Reset Source: mod_g_arstn 0 disabled (no override) 1 reserved 2 Synchronous mode with external clock 3 Synchronous mode with generated clock 4 ISO 7816 mode T=0 5 ISO 7816 mode T=1 6 reserved 7 reserved

14.9.2.4.2.57 UART_EFR2 Register

1 UART_EFR2 Register (Offset = 8Ch) [reset = 0h]

Enhanced Features Register 2

Return to Summary Table

Table 14-26689. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 008Ch**
UART0	**0280 008Ch**
UART1	**0281 008Ch**
UART2	**0282 008Ch**
UART3	**0283 008Ch**
UART4	**0284 008Ch**
UART5	**0285 008Ch**
UART6	**0286 008Ch**
WKUP_UART0	**2B30 008Ch**

Figure 14-8848. UART_EFR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26691. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode Reset Source: mod_g_arstn
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured Reset Source: mod_g_arstn 0 timeout after at least one character has been received 1 periodic timeout even when no character has been received

Table 14-26691. UART_EFR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control Reset Source: mod_g_arstn
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control Reset Source: mod_g_arstn
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable] Reset Source: mod_g_arstn
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1' Reset Source: mod_g_arstn

1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full
				Reset Source: mod_g_arstn
				`0 data in RHR is not overwritten (standard)`
				`1 data in RHR is overwritten when buffer full (and FIFO disabled)`

0	ENDIAN	R/W	0h	Endianness
				Reset Source: mod_g_arstn
				`0 Little Endian (LSB First)`
				`1 Big Endian (MSB First)`

14.9.2.4.2.58 UART_ECR Register

1 UART_ECR Register (Offset = 90h) [reset = 18h]

Enhanced Control register

Return to Summary Table

Table 14-26692. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0090h**
UART0	**0280 0090h**
UART1	**0281 0090h**
UART2	**0282 0090h**
UART3	**0283 0090h**
UART4	**0284 0090h**
UART5	**0285 0090h**
UART6	**0286 0090h**
WKUP_UART0	**2B30 0090h**

Figure 14-8849. UART_ECR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CLEAR_TX_PE</td><td>TX_EN</td><td>RX_EN</td><td>TX_RST</td><td>RX_RST</td><td>A_MULTIDROP</td></tr>
<tr><td colspan="2">R</td><td>W</td><td>R/W</td><td>R/W</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26694. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:6	RESERVED	R	0h	
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only] Reset Source: mod_g_arstn

4	TX_EN	R/W	1h	Enables/Disables the transmitter
				Reset Source: mod_g_arstn
				`0 Transmitter is shut down`
				`1 Transmitter is working`

Table 14-26694. UART_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RX_EN	R/W	1h	Enables/Disables the receiver Reset Source: mod_g_arstn 0 Receiver is shut down 1 Receiver is operating
2	TX_RST	W	0h	Writing '1' resets the transmitter Reset Source: mod_g_arstn
1	RX_RST	W	0h	Writing '1' resets the receiver Reset Source: mod_g_arstn
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address Reset Source: mod_g_arstn

14.9.2.4.2.59 UART_TIMEGUARD Register

1 UART_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Timeguard

Return to Summary Table

Table 14-26695. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0094h**
UART0	**0280 0094h**
UART1	**0281 0094h**
UART2	**0282 0094h**
UART3	**0283 0094h**
UART4	**0284 0094h**
UART5	**0285 0094h**
UART6	**0286 0094h**
WKUP_UART0	**2B30 0094h**

Figure 14-8850. UART_TIMEGUARD Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEGUARD							
R/W							
0h							

Table 14-26697. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices Reset Source: mod_g_arstn

14.9.2.4.2.60 UART_TIMEOUTL Register

1 UART_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Timeout lower byte

Return to Summary Table

Table 14-26698. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0098h**
UART0	**0280 0098h**
UART1	**0281 0098h**
UART2	**0282 0098h**
UART3	**0283 0098h**
UART4	**0284 0098h**
UART5	**0285 0098h**
UART6	**0286 0098h**
WKUP_UART0	**2B30 0098h**

Figure 14-8851. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_L							
R/W							
0h							

Table 14-26700. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value] Reset Source: mod_g_arstn

14.9.2.4.2.61 UART_TIMEOUTH Register

1 UART_TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Timeout higher byte

Return to Summary Table

Table 14-26701. Instance Table

Instance Name	Physical Address
MCU_UART0	04A0 009Ch
UART0	0280 009Ch
UART1	0281 009Ch
UART2	0282 009Ch
UART3	0283 009Ch
UART4	0284 009Ch
UART5	0285 009Ch
UART6	0286 009Ch
WKUP_UART0	2B30 009Ch

Figure 14-8852. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_H							
R/W							
0h							

Table 14-26703. UART_TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value] Reset Source: mod_g_arstn

14.9.2.4.2.62 UART_SCCR Register

1 UART_SCCR Register (Offset = A0h) [reset = 7h]

Smartcard (ISO7816) mode Control Register

Return to Summary Table

Table 14-26704. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A0h**
UART0	**0280 00A0h**
UART1	**0281 00A0h**
UART2	**0282 00A0h**
UART3	**0283 00A0h**
UART4	**0284 00A0h**
UART5	**0285 00A0h**
UART6	**0286 00A0h**
WKUP_UART0	**2B30 00A0h**

Figure 14-8853. UART_SCCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DSNACK	INACK	RESERVED			MAX_ITERATION		
R/W	R/W	R			R/W		
0h	0h	0h			7h		

Table 14-26706. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
5:3	RESERVED	R	0h	

Table 14-26706. UART_SCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared. Reset Source: mod_g_arstn

14.9.2.4.2.63 UART_ERHR Register

1 UART_ERHR Register (Offset = A4h) [reset = 0h]

Extended Receive Holding Register

Return to Summary Table

Table 14-26707. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A4h**
UART0	**0280 00A4h**
UART1	**0281 00A4h**
UART2	**0282 00A4h**
UART3	**0283 00A4h**
UART4	**0284 00A4h**
UART5	**0285 00A4h**
UART6	**0286 00A4h**
WKUP_UART0	**2B30 00A4h**

Figure 14-8854. UART_ERHR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							ERHR
R							R
0h							0h
7	6	5	4	3	2	1	0
ERHR							
R							
0h							

Table 14-26709. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR Reset Source: mod_g_arstn

14.9.2.4.2.64 UART_ETHR Register

1 UART_ETHR Register (Offset = A4h) [reset = 0h]

Extended Transmit Holding Register

Return to Summary Table

Table 14-26710. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A4h**
UART0	**0280 00A4h**
UART1	**0281 00A4h**
UART2	**0282 00A4h**
UART3	**0283 00A4h**
UART4	**0284 00A4h**
UART5	**0285 00A4h**
UART6	**0286 00A4h**
WKUP_UART0	**2B30 00A4h**

Figure 14-8855. UART_ETHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ETHR</td></tr>
<tr><td colspan="7">R</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ETHR</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26712. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ETHR	W	0h	Extended Transmit Holding Register - allows Writing the full 9bit RHR Reset Source: mod_g_arstn

14.9.2.4.2.65 UART_MAR Register

1 UART_MAR Register (Offset = A8h) [reset = 0h]

Multidrop Address Register

Return to Summary Table

Table 14-26713. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A8h**
UART0	**0280 00A8h**
UART1	**0281 00A8h**
UART2	**0282 00A8h**
UART3	**0283 00A8h**
UART4	**0284 00A8h**
UART5	**0285 00A8h**
UART6	**0286 00A8h**
WKUP_UART0	**2B30 00A8h**

Figure 14-8856. UART_MAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26715. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ADDRESS	R/W	0h	Multidrop match address value Reset Source: mod_g_arstn

14.9.2.4.2.66 UART_MMR Register

1 UART_MMR Register (Offset = ACh) [reset = 0h]

Multidrop Mask Register

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Table 14-26716. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00ACh**
UART0	**0280 00ACh**
UART1	**0281 00ACh**
UART2	**0282 00ACh**
UART3	**0283 00ACh**
UART4	**0284 00ACh**
UART5	**0285 00ACh**
UART6	**0286 00ACh**
WKUP_UART0	**2B30 00ACh**

Figure 14-8857. UART_MMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-26718. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MASK	R/W	0h	Address match masking value ? Writing a 0 to a bit means that the corresponding address bit will be ignored in matching Reset Source: mod_g_arstn

14.9.2.4.2.67 UART_MBR Register

1 UART_MBR Register (Offset = B0h) [reset = 0h]

Multidrop Broadcast Address Register

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Table 14-26719. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00B0h**
UART0	**0280 00B0h**
UART1	**0281 00B0h**
UART2	**0282 00B0h**
UART3	**0283 00B0h**
UART4	**0284 00B0h**
UART5	**0285 00B0h**
UART6	**0286 00B0h**
WKUP_UART0	**2B30 00B0h**

Figure 14-8858. UART_MBR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BROADCAST_ADDRESS							
R/W							
0h							

Table 14-26721. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching Reset Source: mod_g_arstn

14.9.3 High-speed Serial Interfaces Registers

14.9.3.1 cpsw

cpsw

14.9.3.1.1 cpsw Summaries

cpsw Summaries

Table 14-26722. CPSW3_ECC Registers, Base Address=0070 4000h, Length=1024

Offset	Length	Register Name	CPSW0 Physical Address
0h	32	CPSW3_ECC_ECC_REV	0070 4000h
8h	32	CPSW3_ECC_ECC_VECTOR	0070 4008h
Ch	32	CPSW3_ECC_ECC_STAT	0070 400Ch
10h	32	CPSW3_ECC_ECC_RESERVED_SVBUS_J	0070 4010h + formula
3Ch	32	CPSW3_ECC_ECC_SEC_EOI_REG	0070 403Ch
40h	32	CPSW3_ECC_ECC_SEC_STATUS_REG0	0070 4040h
80h	32	CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0	0070 4080h
C0h	32	CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0	0070 40C0h
13Ch	32	CPSW3_ECC_ECC_DED_EOI_REG	0070 413Ch
140h	32	CPSW3_ECC_ECC_DED_STATUS_REG0	0070 4140h
180h	32	CPSW3_ECC_ECC_DED_ENABLE_SET_REG0	0070 4180h
1C0h	32	CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0	0070 41C0h
200h	32	CPSW3_ECC_ECC_AGGR_ENABLE_SET	0070 4200h
204h	32	CPSW3_ECC_ECC_AGGR_ENABLE_CLR	0070 4204h
208h	32	CPSW3_ECC_ECC_AGGR_STATUS_SET	0070 4208h
20Ch	32	CPSW3_ECC_ECC_AGGR_STATUS_CLR	0070 420Ch

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152

Offset	Length	Register Name	CPSW0 Physical Address
0h	32	CPSW3_CPSW_NUSS_IDVER_REG	0800 0000h
4h	32	CPSW3_SYNCE_COUNT_REG	0800 0004h
8h	32	CPSW3_SYNCE_MUX_REG	0800 0008h
Ch	32	CPSW3_CONTROL_REG	0800 000Ch
10h	32	CPSW3_SGMII_NON_FIBER_MODE_REG	0800 0010h
14h	32	CPSW3_SERDES_RESET_ISO_REG	0800 0014h
1Ch	32	CPSW3_SUBSSYSTEM_STATUS_REG	0800 001Ch
20h	32	CPSW3_SUBSYSTEM_CONFIG_REG	0800 0020h
30h	32	CPSW3_RGMII1_STATUS_REG	0800 0030h
34h	32	CPSW3_RGMII2_STATUS_REG	0800 0034h
0h	32	CPSW3_CPSGMII_SGMII_IDVER_REG_J	0800 0000h + formula
4h	32	CPSW3_CPSGMII_SOFT_RESET_REG_J	0800 0004h + formula
10h	32	CPSW3_CPSGMII_CONTROL_REG_J	0800 0010h + formula
14h	32	CPSW3_CPSGMII_STATUS_REG_J	0800 0014h + formula
18h	32	CPSW3_CPSGMII_MR_ADV_ABILITY_REG_J	0800 0018h + formula
1Ch	32	CPSW3_CPSGMII_MR_NP_TX_REG_J	0800 001Ch + formula
20h	32	CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_J	0800 0020h + formula
24h	32	CPSW3_CPSGMII_MR_LP_NP_RX_REG_J	0800 0024h + formula

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
40h	32	CPSW3_CPSGMII_DIAG_CLEAR_REG_J	0800 0040h + formula
44h	32	CPSW3_CPSGMII_DIAG_CONTROL_REG_J	0800 0044h + formula
48h	32	CPSW3_CPSGMII_DIAG_STATUS_REG_J	0800 0048h + formula
0h	32	CPSW3_MDIO_MDIO_VERSION_REG	0800 0000h
4h	32	CPSW3_MDIO_CONTROL_REG	0800 0004h
8h	32	CPSW3_MDIO_ALIVE_REG	0800 0008h
Ch	32	CPSW3_MDIO_LINK_REG	0800 000Ch
10h	32	CPSW3_MDIO_LINK_INT_RAW_REG	0800 0010h
14h	32	CPSW3_MDIO_LINK_INT_MASKED_REG	0800 0014h
18h	32	CPSW3_MDIO_LINK_INT_MASK_SET_REG	0800 0018h
1Ch	32	CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG	0800 001Ch
20h	32	CPSW3_MDIO_USER_INT_RAW_REG	0800 0020h
24h	32	CPSW3_MDIO_USER_INT_MASKED_REG	0800 0024h
28h	32	CPSW3_MDIO_USER_INT_MASK_SET_REG	0800 0028h
2Ch	32	CPSW3_MDIO_USER_INT_MASK_CLEAR_REG	0800 002Ch
30h	32	CPSW3_MDIO_MANUAL_IF_REG	0800 0030h
34h	32	CPSW3_MDIO_POLL_REG	0800 0034h
38h	32	CPSW3_MDIO_POLL_EN_REG	0800 0038h
3Ch	32	CPSW3_MDIO_CLAUS45_REG	0800 003Ch
40h	32	CPSW3_MDIO_USER_ADDR0_REG	0800 0040h
44h	32	CPSW3_MDIO_USER_ADDR1_REG	0800 0044h
0h	32	CPSW3_INTD_REVISION	0800 0000h
10h	32	CPSW3_INTD_EOI_REG	0800 0010h
14h	32	CPSW3_INTD_INTR_VECTOR_REG	0800 0014h
100h	32	CPSW3_INTD_ENABLE_REG_OUT_PULSE_0	0800 0100h
300h	32	CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0	0800 0300h
500h	32	CPSW3_INTD_STATUS_REG_OUT_PULSE_0	0800 0500h
A80h	32	CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE	0800 0A80h
0h	32	CPSW3_CPSW_NU_CPSW_ID_VER_REG	0800 0000h
4h	32	CPSW3_CPSW_NU_CONTROL_REG	0800 0004h
10h	32	CPSW3_CPSW_NU_EM_CONTROL_REG	0800 0010h
14h	32	CPSW3_CPSW_NU_STAT_PORT_EN_REG	0800 0014h
18h	32	CPSW3_CPSW_NU_PTYPE_REG	0800 0018h
1Ch	32	CPSW3_CPSW_NU_SOFT_IDLE_REG	0800 001Ch
20h	32	CPSW3_CPSW_NU_THRU_RATE_REG	0800 0020h
24h	32	CPSW3_CPSW_NU_GAP_THRESH_REG	0800 0024h
2Ch	32	CPSW3_CPSW_NU_EEE_PRESCALE_REG	0800 002Ch
30h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG	0800 0030h
34h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG	0800 0034h
38h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG	0800 0038h
3Ch	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG	0800 003Ch
40h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG	0800 0040h
44h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG	0800 0044h
50h	32	CPSW3_CPSW_NU_VLAN_LTYPE_REG	0800 0050h
54h	32	CPSW3_CPSW_NU_EST_TS_DOMAIN_REG	0800 0054h

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
58h	32	CPSW3_CPSW_NU_CUT_THRESHOLD_REG	0800 0058h
5Ch	32	CPSW3_CPSW_NU_FREQUENCY_REG	0800 005Ch
60h	32	CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG	0800 0060h
100h	32	CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG	0800 0100h
104h	32	CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG	0800 0104h
108h	32	CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG	0800 0108h
10Ch	32	CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG	0800 010Ch
110h	32	CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG	0800 0110h
114h	32	CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG	0800 0114h
118h	32	CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG	0800 0118h
11Ch	32	CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG	0800 011Ch
0h	32	CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_J	0800 0000h + formula
4h	32	CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_J	0800 0004h + formula
4h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG	0800 0004h
8h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG	0800 0008h
10h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG	0800 0010h
14h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG	0800 0014h
18h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG	0800 0018h
1Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG	0800 001Ch
20h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG	0800 0020h
24h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG	0800 0024h
28h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG	0800 0028h
30h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG	0800 0030h
34h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG	0800 0034h
38h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG	0800 0038h
50h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG	0800 0050h
120h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_J	0800 0120h + formula
140h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_J	0800 0140h + formula
160h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_J	0800 0160h + formula
180h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG	0800 0180h
184h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG	0800 0184h
188h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG	0800 0188h

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
18Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG	0800 018Ch
190h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG	0800 0190h
194h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG	0800 0194h
198h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG	0800 0198h
19Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG	0800 019Ch
300h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG	0800 0300h
304h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG	0800 0304h
320h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG	0800 0320h
0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG	0800 0000h
4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG	0800 0004h
8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG	0800 0008h
10h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG	0800 0010h
14h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG	0800 0014h
18h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG	0800 0018h
1Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG	0800 001Ch
20h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG	0800 0020h
24h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG	0800 0024h
28h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG	0800 0028h
30h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG	0800 0030h
34h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG	0800 0034h
38h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG	0800 0038h
40h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG	0800 0040h
44h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG	0800 0044h
48h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG	0800 0048h
50h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG	0800 0050h
60h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG	0800 0060h

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
120h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_J	0800 0120h + formula
140h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_J	0800 0140h + formula
160h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_J	0800 0160h + formula
180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG	0800 0180h
184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG	0800 0184h
188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG	0800 0188h
18Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG	0800 018Ch
190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG	0800 0190h
194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG	0800 0194h
198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG	0800 0198h
19Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG	0800 019Ch
300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG	0800 0300h
304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG	0800 0304h
308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG	0800 0308h
30Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG	0800 030Ch
310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG	0800 0310h
314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG	0800 0314h
318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG	0800 0318h
31Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG	0800 031Ch
320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG	0800 0320h
330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG	0800 0330h
334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG	0800 0334h
338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG	0800 0338h
33Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG	0800 033Ch
340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG	0800 0340h
350h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_J	0800 0350h + formula

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG	0800 0370h
380h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_J	0800 0380h + formula
3A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG	0800 03A0h
3A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG	0800 03A4h
3A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG	0800 03A8h
3ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG	0800 03ACh
3B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG	0800 03B0h
3B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG	0800 03B4h
3B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG	0800 03B8h
3BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG	0800 03BCh
3C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG	0800 03C0h
3C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG	0800 03C4h
0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG	0800 0000h
4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG	0800 0004h
8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG	0800 0008h
10h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG	0800 0010h
14h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG	0800 0014h
18h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG	0800 0018h
1Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG	0800 001Ch
20h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG	0800 0020h
24h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG	0800 0024h
28h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG	0800 0028h
30h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG	0800 0030h
34h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG	0800 0034h
38h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG	0800 0038h
40h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG	0800 0040h

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
44h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG	0800 0044h
48h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG	0800 0048h
50h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG	0800 0050h
60h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG	0800 0060h
120h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_J	0800 0120h + formula
140h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_J	0800 0140h + formula
160h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_J	0800 0160h + formula
180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG	0800 0180h
184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG	0800 0184h
188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG	0800 0188h
18Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG	0800 018Ch
190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG	0800 0190h
194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG	0800 0194h
198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG	0800 0198h
19Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG	0800 019Ch
300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG	0800 0300h
304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG	0800 0304h
308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG	0800 0308h
30Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG	0800 030Ch
310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG	0800 0310h
314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG	0800 0314h
318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG	0800 0318h
31Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG	0800 031Ch
320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG	0800 0320h
330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG	0800 0330h
334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG	0800 0334h

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG	0800 0338h
33Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG	0800 033Ch
340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG	0800 0340h
350h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_J	0800 0350h + formula
370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG	0800 0370h
380h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_J	0800 0380h + formula
3A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG	0800 03A0h
3A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG	0800 03A4h
3A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG	0800 03A8h
3ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG	0800 03ACh
3B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG	0800 03B0h
3B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG	0800 03B4h
3B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG	0800 03B8h
3BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG	0800 03BCh
3C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG	0800 03C0h
3C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG	0800 03C4h
0h	32	CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_J	0800 0000h + formula
0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_J	0800 0000h + formula
4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_J	0800 0004h + formula
8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_J	0800 0008h + formula
Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_J	0800 000Ch + formula
10h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_J	0800 0010h + formula
14h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_J	0800 0014h + formula
18h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_J	0800 0018h + formula
1Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_J	0800 001Ch + formula
20h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_J	0800 0020h + formula
24h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_J	0800 0024h + formula

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
28h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_J	0800 0028h + formula
2Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_J	0800 002Ch + formula
30h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_J	0800 0030h + formula
34h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_J	0800 0034h + formula
38h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_J	0800 0038h + formula
3Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_J	0800 003Ch + formula
40h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_J	0800 0040h + formula
44h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_J	0800 0044h + formula
48h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_J	0800 0048h + formula
4Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_J	0800 004Ch + formula
50h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_J	0800 0050h + formula
54h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_J	0800 0054h + formula
58h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_J	0800 0058h + formula
5Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_J	0800 005Ch + formula
60h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_J	0800 0060h + formula
64h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_J	0800 0064h + formula
68h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_J	0800 0068h + formula
6Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_J	0800 006Ch + formula
70h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_J	0800 0070h + formula
74h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_J	0800 0074h + formula
78h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_J	0800 0078h + formula
7Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_J	0800 007Ch + formula
80h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_J	0800 0080h + formula
84h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_J	0800 0084h + formula
88h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_J	0800 0088h + formula
8Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_J	0800 008Ch + formula
90h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_J	0800 0090h + formula
94h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_J	0800 0094h + formula

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
98h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_J	0800 0098h + formula
9Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_J	0800 009Ch + formula
A0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_J	0800 00A0h + formula
A4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_J	0800 00A4h + formula
A8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_J	0800 00A8h + formula
ACh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_J	0800 00ACh + formula
B0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_J	0800 00B0h + formula
B4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_J	0800 00B4h + formula
B8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_J	0800 00B8h + formula
BCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_J	0800 00BCh + formula
C0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_J	0800 00C0h + formula
C4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_J	0800 00C4h + formula
C8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_J	0800 00C8h + formula
CCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_J	0800 00CCh + formula
D0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_J	0800 00D0h + formula
D4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_J	0800 00D4h + formula
D8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_J	0800 00D8h + formula
DCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_J	0800 00DCh + formula
140h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_J	0800 0140h + formula
144h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_J	0800 0144h + formula
148h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_J	0800 0148h + formula
14Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_J	0800 014Ch + formula
150h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_J	0800 0150h + formula
154h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_J	0800 0154h + formula
17Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_J	0800 017Ch + formula
180h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_J_K	0800 0180h + formula

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
1A0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K	0800 01A0h + formula
1C0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_J_K	0800 01C0h + formula
1E0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K	0800 01E0h + formula
0h	32	CPSW3_CPSW_NU_CPTS_IDVER_REG	0800 0000h
4h	32	CPSW3_CPSW_NU_CPTS_CONTROL_REG	0800 0004h
8h	32	CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG	0800 0008h
Ch	32	CPSW3_CPSW_NU_CPTS_TS_PUSH_REG	0800 000Ch
10h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG	0800 0010h
14h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG	0800 0014h
18h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG	0800 0018h
1Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG	0800 001Ch
20h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG	0800 0020h
24h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG	0800 0024h
28h	32	CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG	0800 0028h
2Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG	0800 002Ch
30h	32	CPSW3_CPSW_NU_CPTS_EVENT_POP_REG	0800 0030h
34h	32	CPSW3_CPSW_NU_CPTS_EVENT_0_REG	0800 0034h
38h	32	CPSW3_CPSW_NU_CPTS_EVENT_1_REG	0800 0038h
3Ch	32	CPSW3_CPSW_NU_CPTS_EVENT_2_REG	0800 003Ch
40h	32	CPSW3_CPSW_NU_CPTS_EVENT_3_REG	0800 0040h
44h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG	0800 0044h
48h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG	0800 0048h
4Ch	32	CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG	0800 004Ch
50h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG	0800 0050h
54h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG	0800 0054h
58h	32	CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG	0800 0058h
D0h	32	CPSW3_CPSW_NU_CPTS_TS_CONFIG	0800 00D0h
0h	32	CPSW3_CPSW_NU_ALE_MOD_VER	0800 0000h
4h	32	CPSW3_CPSW_NU_ALE_ALE_STATUS	0800 0004h
8h	32	CPSW3_CPSW_NU_ALE_ALE_CONTROL	0800 0008h
Ch	32	CPSW3_CPSW_NU_ALE_ALE_CTRL2	0800 000Ch
10h	32	CPSW3_CPSW_NU_ALE_ALE_PRESCALE	0800 0010h
14h	32	CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL	0800 0014h
1Ch	32	CPSW3_CPSW_NU_ALE_ALE_NXT_HDR	0800 001Ch
20h	32	CPSW3_CPSW_NU_ALE_ALE_TBLCTL	0800 0020h
34h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW2	0800 0034h
38h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW1	0800 0038h
3Ch	32	CPSW3_CPSW_NU_ALE_ALE_TBLW0	0800 003Ch
40h	32	CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_J	0800 0040h + formula
90h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER	0800 0090h
94h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST	0800 0094h
98h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST	0800 0098h
9Ch	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG	0800 009Ch

Table 14-26723. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
B4h	32	CPSW3_CPSW_NU_ALE_ALE_FAST_LUT	0800 00B4h
B8h	32	CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG	0800 00B8h
BCh	32	CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL	0800 00BCh
FCh	32	CPSW3_CPSW_NU_ALE_EGRESSOP	0800 00FCh
100h	32	CPSW3_CPSW_NU_ALE_POLICECFG0	0800 0100h
104h	32	CPSW3_CPSW_NU_ALE_POLICECFG1	0800 0104h
108h	32	CPSW3_CPSW_NU_ALE_POLICECFG2	0800 0108h
10Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG3	0800 010Ch
110h	32	CPSW3_CPSW_NU_ALE_POLICECFG4	0800 0110h
118h	32	CPSW3_CPSW_NU_ALE_POLICECFG6	0800 0118h
11Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG7	0800 011Ch
120h	32	CPSW3_CPSW_NU_ALE_POLICETBLCTL	0800 0120h
124h	32	CPSW3_CPSW_NU_ALE_POLICECONTROL	0800 0124h
128h	32	CPSW3_CPSW_NU_ALE_POLICETESTCTL	0800 0128h
12Ch	32	CPSW3_CPSW_NU_ALE_POLICEHSTAT	0800 012Ch
134h	32	CPSW3_CPSW_NU_ALE_THREADMAPDEF	0800 0134h
138h	32	CPSW3_CPSW_NU_ALE_THREADMAPCTL	0800 0138h
13Ch	32	CPSW3_CPSW_NU_ALE_THREADMAPVAL	0800 013Ch
0h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_J	0800 0000h + formula
4h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_J	0800 0004h + formula
8h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_J	0800 0008h + formula
Ch	32	CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_J	0800 000Ch + formula
10h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_J	0800 0010h + formula
14h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_J	0800 0014h + formula
18h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_J	0800 0018h + formula
0h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_J	0800 0000h + formula
4h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_J	0800 0004h + formula
8h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_J	0800 0008h + formula
Ch	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_J	0800 000Ch + formula
10h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_J	0800 0010h + formula
14h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_J	0800 0014h + formula
18h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_J	0800 0018h + formula

14.9.3.1.2 cpsw Registers

cpsw Registers

14.9.3.1.2.1 CPSW3_ECC_ECC_REV Register

1 CPSW3_ECC_ECC_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-26724. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4000h**

Figure 14-8859. CPSW3_ECC_ECC_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-26726. CPSW3_ECC_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.3.1.2.2 CPSW3_ECC_ECC_VECTOR Register

1 CPSW3_ECC_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-26727. Instance Table

Instance Name	**Physical Address**
CPSW0	**0070 4008h**

Figure 14-8860. CPSW3_ECC_ECC_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26729. CPSW3_ECC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.3.1.2.3 CPSW3_ECC_ECC_STAT Register

1 CPSW3_ECC_ECC_STAT Register (Offset = Ch) [reset = 14h]

Misc Status

Return to Summary Table

Table 14-26730. Instance Table

Instance Name	Physical Address
CPSW0	**0070 400Ch**

Figure 14-8861. CPSW3_ECC_ECC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					14h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
14h							

Table 14-26732. CPSW3_ECC_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	14h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.3.1.2.4 CPSW3_ECC_ECC_RESERVED_SVBUS_j Register

1 CPSW3_ECC_ECC_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-26733. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4010h + formula**

Figure 14-8862. CPSW3_ECC_ECC_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-26735. CPSW3_ECC_ECC_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.3.1.2.5 CPSW3_ECC_ECC_SEC_EOI_REG Register

1 CPSW3_ECC_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-26736. Instance Table

Instance Name	Physical Address
CPSW0	**0070 403Ch**

Figure 14-8863. CPSW3_ECC_ECC_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-26738. CPSW3_ECC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.1.2.6 CPSW3_ECC_ECC_SEC_STATUS_REG0 Register

1 CPSW3_ECC_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-26739. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4040h**

Figure 14-8864. CPSW3_ECC_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26741. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend

Table 14-26741. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.9.3.1.2.7 CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register

1 CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-26742. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4080h**

Figure 14-8865. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26744. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend

Table 14-26744. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.9.3.1.2.8 CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register

1 CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-26745. Instance Table

Instance Name	Physical Address
CPSW0	**0070 40C0h**

Figure 14-8866. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26747. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend

Table 14-26747. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.9.3.1.2.9 CPSW3_ECC_ECC_DED_EOI_REG Register

1 CPSW3_ECC_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-26748. Instance Table

Instance Name	Physical Address
CPSW0	**0070 413Ch**

Figure 14-8867. CPSW3_ECC_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-26750. CPSW3_ECC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.1.2.10 CPSW3_ECC_ECC_DED_STATUS_REG0 Register

1 CPSW3_ECC_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-26751. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4140h**

Figure 14-8868. CPSW3_ECC_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26753. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend

Table 14-26753. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.9.3.1.2.11 CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register

1 CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-26754. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4180h**

Figure 14-8869. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26756. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend

Table 14-26756. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.9.3.1.2.12 CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register

1 CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-26757. Instance Table

Instance Name	Physical Address
CPSW0	**0070 41C0h**

Figure 14-8870. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26759. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend

Table 14-26759. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.9.3.1.2.13 CPSW3_ECC_ECC_AGGR_ENABLE_SET Register

1 CPSW3_ECC_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-26760. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4200h**

Figure 14-8871. CPSW3_ECC_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-26762. CPSW3_ECC_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.3.1.2.14 CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register

1 CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-26763. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4204h**

Figure 14-8872. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-26765. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.3.1.2.15 CPSW3_ECC_ECC_AGGR_STATUS_SET Register

1 CPSW3_ECC_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-26766. Instance Table

Instance Name	Physical Address
CPSW0	**0070 4208h**

Figure 14-8873. CPSW3_ECC_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-26768. CPSW3_ECC_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.3.1.2.16 CPSW3_ECC_ECC_AGGR_STATUS_CLR Register

1 CPSW3_ECC_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-26769. Instance Table

Instance Name	Physical Address
CPSW0	**0070 420Ch**

Figure 14-8874. CPSW3_ECC_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-26771. CPSW3_ECC_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.3.1.2.17 CPSW3_CPSW_NUSS_IDVER_REG Register

1 CPSW3_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6BA01103h]

ID Version Register

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Table 14-26772. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-8875. CPSW3_CPSW_NUSS_IDVER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6BA0h							
23	22	21	20	19	18	17	16
IDENT							
R							
6BA0h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
2h					1h		
7	6	5	4	3	2	1	0
MINOR_VER							
R							
3h							

Table 14-26774. CPSW3_CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA0h	Identification value
15:11	RTL_VER	R	2h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	3h	Minor version value

14.9.3.1.2.18 CPSW3_SYNCE_COUNT_REG Register

1 CPSW3_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

SyncE Count Register

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Table 14-26775. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-8876. CPSW3_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24
SYNCE_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNCE_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNCE_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNCE_CNT							
R/W							
0h							

Table 14-26777. CPSW3_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNCE_CNT	R/W	0h	Sync E Count Value

14.9.3.1.2.19 CPSW3_SYNCE_MUX_REG Register

1 CPSW3_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

SyncE Mux Register

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Table 14-26778. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-8877. CPSW3_SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		SYNCE_SEL		SYNCE_PORT_SEL			
NONE		R/W		R/W			
0h		0h		0h			

Table 14-26780. CPSW3_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:4	SYNCE_SEL	R/W	0h	Sync E Interface Select. 0h GMIIn_MRCLK_I input clock from selected port. 1h RMII_MHZ_50_CLK (same for all ports). 2h RGMIIn_RXC_I input clock from selected port. 3h SERDESn_RXCLK from selected port.
3:0	SYNCE_PORT_SEL	R/W	0h	Sync E Port Select This field selects the port that will be used for Synchronous Ethernet receive clock. The port interface is selected with synce_sel. 0h Port 1. 1h Port 2. 2h-Fh Reserved.

14.9.3.1.2.20 CPSW3_CONTROL_REG Register

1 CPSW3_CONTROL_REG Register (Offset = Ch) [reset = 0h]

Control Register

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Table 14-26781. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch**

Figure 14-8878. CPSW3_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EEE_PHY_ONLY	EEE_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-26783. CPSW3_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0h `The low power indicate state includes gating off the CPPI_GCLK to the CPSW.` 1h `The low power indicate state does not gate the clock to the CPSW.`
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0h `EEE is disabled` 1h `EEE is enabled`

14.9.3.1.2.21 CPSW3_SGMII_NON_FIBER_MODE_REG Register

1 CPSW3_SGMII_NON_FIBER_MODE_REG Register (Offset = 10h) [reset = 3h]

SGMII NON FIBER Mode Register

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Table 14-26784. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8879. CPSW3_SGMII_NON_FIBER_MODE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED						SGMII_NON_FIBER_MODE	
NONE						R/W	
0h						3h	

Table 14-26786. CPSW3_SGMII_NON_FIBER_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SGMII_NON_FIBER_MODE	R/W	3h	This register bit goes to the CPSGMII mode input only

14.9.3.1.2.22 CPSW3_SERDES_RESET_ISO_REG Register

1 CPSW3_SERDES_RESET_ISO_REG Register (Offset = 14h) [reset = 0h]

SyncE Mux Register

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Table 14-26787. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-8880. CPSW3_SERDES_RESET_ISO_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SERDES_RESET_ISO	
NONE						R/W	
0h						0h	

Table 14-26789. CPSW3_SERDES_RESET_ISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES_RESET_ISO	R/W	0h	These bits control whether the SERDES ignores the hard reset for isolation or not

14.9.3.1.2.23 CPSW3_SUBSSYSTEM_STATUS_REG Register

1 CPSW3_SUBSSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Subsystem Status Register

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Table 14-26790. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-8881. CPSW3_SUBSSYSTEM_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EEE_CLKSTOP_ACK
NONE							R
0h							0h

Table 14-26792. CPSW3_SUBSSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

14.9.3.1.2.24 CPSW3_SUBSYSTEM_CONFIG_REG Register

1 CPSW3_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 70203h]

Subsystem Configuration Register

Return to Summary Table

Table 14-26793. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h**

Figure 14-8882. CPSW3_SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				XGMII			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
XGMII				QSGMII	SGMII	RGMII	RMII
R				R	R	R	R
0h				0h	1h	1h	1h
15	14	13	12	11	10	9	8
RESERVED			NUM_GENF				
NONE			R				
0h			2h				
7	6	5	4	3	2	1	0
NUM_PORTS							
R							
3h							

Table 14-26795. CPSW3_SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	R	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	R	1h	SGMII is included in the CPSW_NUSS
17	RGMII	R	1h	RGMII is included in the CPSW_NUSS
16	RMII	R	1h	RMII is included in the CPSW_NUSS
15:13	RESERVED	NONE	0h	Reserved
12:8	NUM_GENF	R	2h	The number of CPTS GENF outputs
7:0	NUM_PORTS	R	3h	The total number of ports including the host port 0

14.9.3.1.2.25 CPSW3_RGMII1_STATUS_REG Register

1 CPSW3_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

RGMII1 Status Register

Return to Summary Table

Table 14-26796. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-8883. CPSW3_RGMII1_STATUS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>FULLDUPLEX</td><td colspan="2">SPEED</td><td>LINK</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td colspan="2">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-26798. CPSW3_RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	FULLDUPLEX	R	0h	RGMII Port 1 full duplex:
				`0h Half-duplex`
				`1h Full-duplex`

2:1	SPEED	R	0h	RGMII Port 1 speed:
				`0h 10Mbps`
				`1h 100Mbps`
				`2h 1000Mbps`
				`3h Reserved`

0	LINK	R	0h	RGMII Port 1 link indicator:
				`0h Link is down,`
				`1h Link is up`

14.9.3.1.2.26 CPSW3_RGMII2_STATUS_REG Register

1 CPSW3_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

RGMII2 Status Register

Return to Summary Table

Table 14-26799. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-8884. CPSW3_RGMII2_STATUS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>FULLDUPLEX</td><td colspan="2">SPEED</td><td>LINK</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td colspan="2">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-26801. CPSW3_RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	FULLDUPLEX	R	0h	RGMII Port 2 full dulex: 0h Half-duplex 1h Full-duplex
2:1	SPEED	R	0h	RGMII Port 2 speed: 0h 10Mbps 1h 100Mbps 2h 1000Mbps 3h Reserved
0	LINK	R	0h	RGMII Port 2 link indicator: 0h Link is down 1h Link is up

14.9.3.1.2.27 CPSW3_CPSGMII_SGMII_IDVER_REG_j Register

1 CPSW3_CPSGMII_SGMII_IDVER_REG_j Register (Offset = 0h + formula) [reset = 4EC21102h]

SGMII IDVER register

Return to Summary Table

Offset = 100h + (j * 100h); where j = 0 to 1d

Table 14-26802. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h + formula**

Figure 14-8885. CPSW3_CPSGMII_SGMII_IDVER_REG_j Name Register

31	30	29	28	27	26	25	24
TX_IDENT							
R							
4EC2h							
23	22	21	20	19	18	17	16
TX_IDENT							
R							
4EC2h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
2h					1h		
7	6	5	4	3	2	1	0
MINOR_VER							
R							
2h							

Table 14-26804. CPSW3_CPSGMII_SGMII_IDVER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4EC2h	MODULE value
15:11	RTL_VER	R	2h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	2h	Minor version value

14.9.3.1.2.28 CPSW3_CPSGMII_SOFT_RESET_REG_j Register

1 CPSW3_CPSGMII_SOFT_RESET_REG_j Register (Offset = 4h + formula) [reset = 0h]

SGMII Soft Reset Register

Return to Summary Table

Offset = 104h + (j * 100h); where j = 0 to 1d

Table 14-26805. Instance Table

Instance Name	Physical Address
CPSW0	0800 0004h + formula

Figure 14-8886. CPSW3_CPSGMII_SOFT_RESET_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						RT_SOFT_RESET	SOFT_RESET
NONE						R/W	R/W
0h						0h	0h

Table 14-26807. CPSW3_CPSGMII_SOFT_RESET_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	RT_SOFT_RESET	R/W	0h	Transmit and receive software reset
0	SOFT_RESET	R/W	0h	Software reset

14.9.3.1.2.29 CPSW3_CPSGMII_CONTROL_REG_j Register

1 CPSW3_CPSGMII_CONTROL_REG_j Register (Offset = 10h + formula) [reset = 0h]

SGMII Control Register

Return to Summary Table

Offset = 110h + (j * 100h); where j = 0 to 1d

Table 14-26808. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h + formula**

Figure 14-8887. CPSW3_CPSGMII_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TEST_PATTERN_EN	MASTER	LOOPBACK	MR_NP_LOADED	FAST_LINK_TIMER	MR_AN_RESTART	MR_AN_ENABLE
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26810. CPSW3_CPSGMII_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TEST_PATTERN_EN	R/W	0h	Test pattern enable
5	MASTER	R/W	0h	Controller mode
4	LOOPBACK	R/W	0h	Loopback mode
3	MR_NP_LOADED	R/W	0h	Next page loaded
2	FAST_LINK_TIMER	R/W	0h	Fast link timer
1	MR_AN_RESTART	R/W	0h	Auto-negotiation restart
0	MR_AN_ENABLE	R/W	0h	Auto-negotiation enable

14.9.3.1.2.30 CPSW3_CPSGMII_STATUS_REG_j Register

1 CPSW3_CPSGMII_STATUS_REG_j Register (Offset = 14h + formula) [reset = 0h]

SGMII Status Register

Return to Summary Table

Offset = 114h + (j * 100h); where j = 0 to 1d

Table 14-26811. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h + formula**

Figure 14-8888. CPSW3_CPSGMII_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FIB_SIG_DETECT	LOCK	MR_PAGE_RX	MR_AN_COMPLETE	AN_ERROR	LINK
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-26813. CPSW3_CPSGMII_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	FIB_SIG_DETECT	R	0h	Fiber signal detect
4	LOCK	R	0h	Lock
3	MR_PAGE_RX	R	0h	Next page received
2	MR_AN_COMPLETE	R	0h	Auto-negotiation complete
1	AN_ERROR	R	0h	Auto-negotiation error
0	LINK	R	0h	Link indicator

14.9.3.1.2.31 CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register

1 CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register (Offset = 18h + formula) [reset = 0h]

SGMII MR Advertized Ability Register

Return to Summary Table

Offset = 118h + (j * 100h); where j = 0 to 1d

Table 14-26814. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h + formula**

Figure 14-8889. CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_ADV_ABILITY							
R/W							
0h							
7	6	5	4	3	2	1	0
MR_ADV_ABILITY							
R/W							
0h							

Table 14-26816. CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_ADV_ABILITY	R/W	0h	Advertised ability

14.9.3.1.2.32 CPSW3_CPSGMII_MR_NP_TX_REG_j Register

1 CPSW3_CPSGMII_MR_NP_TX_REG_j Register (Offset = 1Ch + formula) [reset = 0h]

SGMII Next Pate Transmit Register

Return to Summary Table

Offset = 11Ch + (j * 100h); where j = 0 to 1d

Table 14-26817. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch + formula**

Figure 14-8890. CPSW3_CPSGMII_MR_NP_TX_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_NP_TX							
R/W							
0h							
7	6	5	4	3	2	1	0
MR_NP_TX							
R/W							
0h							

Table 14-26819. CPSW3_CPSGMII_MR_NP_TX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_NP_TX	R/W	0h	Next page transmit

14.9.3.1.2.33 CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register

1 CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register (Offset = 20h + formula) [reset = 0h]

SGMII Link Partner Advertized Ability Register

Return to Summary Table

Offset = 120h + (j * 100h); where j = 0 to 1d

Table 14-26820. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h + formula**

Figure 14-8891. CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_LP_ADV_ABILITY							
R							
0h							
7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY							
R							
0h							

Table 14-26822. CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_LP_ADV_ABILITY	R	0h	Link partner advertised ability

14.9.3.1.2.34 CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register

1 CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register (Offset = 24h + formula) [reset = 0h]

SGMII Link Partner Next Page Receive Register

Return to Summary Table

Offset = 124h + (j * 100h); where j = 0 to 1d

Table 14-26823. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h + formula**

Figure 14-8892. CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_LP_NP_RX							
R							
0h							
7	6	5	4	3	2	1	0
MR_LP_NP_RX							
R							
0h							

Table 14-26825. CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received

14.9.3.1.2.35 CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register

1 CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register (Offset = 40h + formula) [reset = 0h]

SGMII Diagnostics Clear Register

Return to Summary Table

Offset = 140h + (j * 100h); where j = 0 to 1d

Table 14-26826. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h + formula**

Figure 14-8893. CPSW3_CPSGMII_DIAG_CLEAR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DIAG_CLEAR
NONE							R/W
0h							0h

Table 14-26828. CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DIAG_CLEAR	R/W	0h	Diagnostics clear

14.9.3.1.2.36 CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register

1 CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register (Offset = 44h + formula) [reset = 0h]

SGMII Diagnostics Control Register

Return to Summary Table

Offset = 144h + (j * 100h); where j = 0 to 1d

Table 14-26829. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h + formula**

Figure 14-8894. CPSW3_CPSGMII_DIAG_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DIAG_SM_SEL			RESERVED		DIAG_EDGE_SEL	
NONE	R/W			NONE		R/W	
0h	0h			0h		0h	

Table 14-26831. CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:4	DIAG_SM_SEL	R/W	0h	Diagnostic select
3:2	RESERVED	NONE	0h	Reserved
1:0	DIAG_EDGE_SEL	R/W	0h	Diagnostics hold signals edge select

14.9.3.1.2.37 CPSW3_CPSGMII_DIAG_STATUS_REG_j Register

1 CPSW3_CPSGMII_DIAG_STATUS_REG_j Register (Offset = 48h + formula) [reset = 0h]

SGMII Diagnostics Status Register

Return to Summary Table

Offset = 148h + (j * 100h); where j = 0 to 1d

Table 14-26832. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0048h + formula**

Figure 14-8895. CPSW3_CPSGMII_DIAG_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DIAG_STATUS							
R							
0h							
7	6	5	4	3	2	1	0
DIAG_STATUS							
R							
0h							

Table 14-26834. CPSW3_CPSGMII_DIAG_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	DIAG_STATUS	R	0h	Diagnostics status

14.9.3.1.2.38 CPSW3_MDIO_MDIO_VERSION_REG Register

1 CPSW3_MDIO_MDIO_VERSION_REG Register (Offset = 0h) [reset = 70907h]

MDIO Version Register

Return to Summary Table

Table 14-26835. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-8896. CPSW3_MDIO_MDIO_VERSION_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="4">7h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">1h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">7h</td></tr>
</table>

Table 14-26837. CPSW3_MDIO_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	Scheme
29:28	BU	R	0h	bu
27:16	MODULE_ID	R	7h	Module ID
15:11	REVRTL	R	1h	RTL version
10:8	REVMAJ	R	1h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	7h	Minor version

14.9.3.1.2.39 CPSW3_MDIO_CONTROL_REG Register

1 CPSW3_MDIO_CONTROL_REG Register (Offset = 4h) [reset = 810000FFh]

MDIO Control Register

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Table 14-26838. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-8897. CPSW3_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R	R/W	NONE	R				
1h	0h	0h	1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
NONE			R/W	R/W	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKDIV							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV							
R/W							
FFh							

Table 14-26840. CPSW3_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1h to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	NONE	0h	Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1h. This implies that MDIOUserAccess1 is the highest available user access channel.
23:21	RESERVED	NONE	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 14-26840. CPSW3_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1h to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	NONE	0h	Reserved
15:0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. When clkdiv is set to 0h, MDCLK is disabled and output is driven to a high logic state. MDCLK frequency = clk frequency/(clkdiv+1).

14.9.3.1.2.40 CPSW3_MDIO_ALIVE_REG Register

1 CPSW3_MDIO_ALIVE_REG Register (Offset = 8h) [reset = 0h]

MDIO Alive Register

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Table 14-26841. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-8898. CPSW3_MDIO_ALIVE_REG Name Register

31	30	29	28	27	26	25	24
ALIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
ALIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
ALIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
ALIVE							
R/W							
0h							

Table 14-26843. CPSW3_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W	0h	MDIO Alive. Each of the 32-bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1h to any bit will clear it, writing a 0h has no effect.

14.9.3.1.2.41 CPSW3_MDIO_LINK_REG Register

1 CPSW3_MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]

MDIO Link Register

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Table 14-26844. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch**

Figure 14-8899. CPSW3_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24
LINK							
R							
0h							
23	22	21	20	19	18	17	16
LINK							
R							
0h							
15	14	13	12	11	10	9	8
LINK							
R							
0h							
7	6	5	4	3	2	1	0
LINK							
R							
0h							

Table 14-26846. CPSW3_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to 0h if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.

14.9.3.1.2.42 CPSW3_MDIO_LINK_INT_RAW_REG Register

1 CPSW3_MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = 0h]

MDIO Link Interrupt Raw Register

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Table 14-26847. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8900. CPSW3_MDIO_LINK_INT_RAW_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">LINKINTRAW</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-26849. CPSW3_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTRAW	R/W	0h	MDIO link change event raw value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. [0]LINKINTRAW and [1]LINKINTRAW correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The [0]LINKINTRAW bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The [1]LINKINTRAW bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the [0]LINKINTRAW bit to a 1h which may be used for test purposes.

14.9.3.1.2.43 CPSW3_MDIO_LINK_INT_MASKED_REG Register

1 CPSW3_MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = 0h]

MDIO Link Interrupt Masked Register

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Table 14-26850. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-8901. CPSW3_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
NONE						R/W	
0h						0h	

Table 14-26852. CPSW3_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding CPSW_MDIO_USER_PHY_SEL_REG_k[6] LINKINT_ENABLE bit was set. CPSW_MDIO_LINK_INT_MASKED_REG[0] LINKINTMASKED and [1] LINKINTMASKED correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the interrupt and writing 0h has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The [0] LINKINTMASKED bit will be asserted '1' when CPSW_MDIO_LINK_INT_RAW_REG[0] LINKINTRAW is asserted '1' and when the CPSW_MDIO_LINK_INT_MASK_SET_REG[0] LINKINTMASKSET bit is set to 1h. Writing a 1h will clear [0] LINKINTMASKED (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The [1] LINKINTMASKED bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

14.9.3.1.2.44 CPSW3_MDIO_LINK_INT_MASK_SET_REG Register

1 CPSW3_MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = 0h]

MDIO Link Interrupt Mask Set Register

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Table 14-26853. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h**

Figure 14-8902. CPSW3_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASKSET
NONE							R/W
0h							0h

Table 14-26855. CPSW3_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when [0] LINKINTRAW is asserted.

14.9.3.1.2.45 CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register

1 CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = 0h]

MDIO Link Interrupt Mask Clear Register

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Table 14-26856. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-8903. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
NONE							R/W
0h							0h

Table 14-26858. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the [0] LINKINTRAW bit value.

14.9.3.1.2.46 CPSW3_MDIO_USER_INT_RAW_REG Register

1 CPSW3_MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = 0h]

MDIO User Interrupt Raw Register

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Table 14-26859. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h**

Figure 14-8904. CPSW3_MDIO_USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
NONE						R/W	
0h						0h	

Table 14-26861. CPSW3_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

14.9.3.1.2.47 CPSW3_MDIO_USER_INT_MASKED_REG Register

1 CPSW3_MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = 0h]

MDIO User Interrupt Masked Register

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Table 14-26862. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-8905. CPSW3_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
NONE						R/W	
0h						0h	

Table 14-26864. CPSW3_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED bits to a 1h. This mode may be used for test purposes.

14.9.3.1.2.48 CPSW3_MDIO_USER_INT_MASK_SET_REG Register

1 CPSW3_MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = 0h]

MDIO User Interrupt Mask Set Register

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Table 14-26865. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h**

Figure 14-8906. CPSW3_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
NONE						R/W	
0h						0h	

Table 14-26867. CPSW3_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

14.9.3.1.2.49 CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register

1 CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = 0h]

MDIO User Interrupt Mask Clear Register

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Table 14-26868. Instance Table

Instance Name	Physical Address
CPSW0	**0800 002Ch**

Figure 14-8907. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
NONE						R/W	
0h						0h	

Table 14-26870. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0h to this register has no effect.

14.9.3.1.2.50 CPSW3_MDIO_MANUAL_IF_REG Register

1 CPSW3_MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = 0h]

MDIO Manual Interface Register

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Table 14-26871. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-8908. CPSW3_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-26873. CPSW3_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO Pin Value. This is the external MDIO data pin value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

14.9.3.1.2.51 CPSW3_MDIO_POLL_REG Register

1 CPSW3_MDIO_POLL_REG Register (Offset = 34h) [reset = 0h]

MDIO Poll Register

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Table 14-26874. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-8909. CPSW3_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPG							
R/W							
0h							

Table 14-26876. CPSW3_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the CPSW_MDIO_MANUAL_IF_REG register `1h Manual Mode.`

30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode.
				When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
				`0h Normal Mode.`
				`1h State Change Mode.`

29:8	RESERVED	NONE	0h	Reserved
7:0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

14.9.3.1.2.52 CPSW3_MDIO_POLL_EN_REG Register

1 CPSW3_MDIO_POLL_EN_REG Register (Offset = 38h) [reset = FFFFFFFFh]

MDIO Poll Enable Register

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Table 14-26877. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-8910. CPSW3_MDIO_POLL_EN_REG Name Register

31	30	29	28	27	26	25	24
POLL_EN							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
POLL_EN							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
POLL_EN							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
POLL_EN							
R/W							
FFFFFFFFh							

Table 14-26879. CPSW3_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	MDIO Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit ([20] PREAMBLE) in the CPSW_MDIO_CONTROL_REG register. However, there does not have to be a PHY at address 31.

14.9.3.1.2.53 CPSW3_MDIO_CLAUS45_REG Register

1 CPSW3_MDIO_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]

MDIO Clause45 Register

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Table 14-26880. Instance Table

Instance Name	Physical Address
CPSW0	**0800 003Ch**

Figure 14-8911. CPSW3_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24
CLAUSE45							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAUSE45							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAUSE45							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAUSE45							
R/W							
0h							

Table 14-26882. CPSW3_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared 0h, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

14.9.3.1.2.54 CPSW3_MDIO_USER_ADDR0_REG Register

1 CPSW3_MDIO_USER_ADDR0_REG Register (Offset = 40h) [reset = 0h]

MDIO Address 0 Register

Return to Summary Table

Table 14-26883. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h**

Figure 14-8912. CPSW3_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USER_ADDR0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USER_ADDR0							
R/W							
0h							

Table 14-26885. CPSW3_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR0	R/W	0h	MDIO User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

14.9.3.1.2.55 CPSW3_MDIO_USER_ADDR1_REG Register

1 CPSW3_MDIO_USER_ADDR1_REG Register (Offset = 44h) [reset = 0h]

MDIO Address 1 Register

Return to Summary Table

Table 14-26886. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h**

Figure 14-8913. CPSW3_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR1							
R/W							
0h							

Table 14-26888. CPSW3_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR1	R/W	0h	MDIO User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

14.9.3.1.2.56 CPSW3_INTD_REVISION Register

1 CPSW3_INTD_REVISION Register (Offset = 0h) [reset = 6690A200h]

Revision Register

Return to Summary Table

Table 14-26889. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-8914. CPSW3_INTD_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		690h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
690h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
14h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-26891. CPSW3_INTD_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	BU
27:16	FUNCTION	R	690h	Module ID
15:11	RTLVER	R	14h	RTL revisions
10:8	MAJREV	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom revision
5:0	MINREV	R	0h	Minor revision

14.9.3.1.2.57 CPSW3_INTD_EOI_REG Register

1 CPSW3_INTD_EOI_REG Register (Offset = 10h) [reset = 0h]

End of Interrupt Register

Return to Summary Table

Table 14-26892. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8915. CPSW3_INTD_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOI_VECTOR							
R/W							
0h							

Table 14-26894. CPSW3_INTD_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

14.9.3.1.2.58 CPSW3_INTD_INTR_VECTOR_REG Register

1 CPSW3_INTD_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]

Interrupt Vector Register

Return to Summary Table

Table 14-26895. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-8916. CPSW3_INTD_INTR_VECTOR_REG Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTR_VECTOR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTR_VECTOR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTR_VECTOR							
R							
0h							

Table 14-26897. CPSW3_INTD_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR	R	0h	Interrupt Vector Register

14.9.3.1.2.59 CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register

1 CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register (Offset = 100h) [reset = 0h]

Enable Register 0

Return to Summary Table

Table 14-26898. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0100h**

Figure 14-8917. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVNT_PENDA
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-26900. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_evnt_penda

14.9.3.1.2.60 CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register

1 CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 300h) [reset = 0h]

Enable Clear Register 0

Return to Summary Table

Table 14-26901. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0300h**

Figure 14-8918. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-26903. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_evnt_penda

14.9.3.1.2.61 CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register

1 CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register (Offset = 500h) [reset = 0h]

Status Register 0

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Table 14-26904. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0500h**

Figure 14-8919. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>STATUS_OUT_PULSE_STAT_PENDA</td><td>STATUS_OUT_PULSE_MDIO_PENDA</td><td>STATUS_OUT_PULSE_EVNT_PENDA</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26906. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda
0	STATUS_OUT_PULSE_EVNT_PENDA	R	0h	Status for out_pulse_en_evnt_penda

14.9.3.1.2.62 CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register

1 CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register (Offset = A80h) [reset = 0h]

Interrupt Vector for out_pulse

Return to Summary Table

Table 14-26907. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0A80h**

Figure 14-8920. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR_OUT_PULSE							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR_OUT_PULSE							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR_OUT_PULSE							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE							
R							
0h							

Table 14-26909. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector

14.9.3.1.2.63 CPSW3_CPSW_NU_CPSW_ID_VER_REG Register

1 CPSW3_CPSW_NU_CPSW_ID_VER_REG Register (Offset = 0h) [reset = 6BA81103h]

CPSW ID Version

Return to Summary Table

Table 14-26910. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-8921. CPSW3_CPSW_NU_CPSW_ID_VER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6BA8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IDENT							
R							
6BA8h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_VER		
R					R		
2h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINOR_VER							
R							
3h							

Table 14-26912. CPSW3_CPSW_NU_CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA8h	Identification Value
15:11	RTL_VER	R	2h	RTL Version Value
10:8	MAJOR_VER	R	1h	Major Version Value
7:0	MINOR_VER	R	3h	Minor Version Value

14.9.3.1.2.64 CPSW3_CPSW_NU_CONTROL_REG Register

1 CPSW3_CPSW_NU_CONTROL_REG Register (Offset = 4h) [reset = 0h]

CPSW Switch Control

Return to Summary Table

Table 14-26913. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-8922. CPSW3_CPSW_NU_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CUT_THRU_ENABLE	EST_ENABLE	IET_ENABLE	EEE_ENABLE
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	P0_TX_CRC_TYPE	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26915. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode. 0h ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data). 1h ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).
30:20	RESERVED	NONE	0h	Reserved
19	CUT_THRU_ENABLE	R/W	0h	Cut Thru Enable. 0h Cut Thru disabled 1h Cut Thru enabled
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) 0h EST is disabled 1h EST is enabled
17	IET_ENABLE	R/W	0h	Intersperced Express Traffic enable (IET) 0h IET is disabled 1h IET is enabled

Table 14-26915. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable 0h Energy Efficient Ethernet is disabled 1h Energy Efficient Ethernet is enabled
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors 0h Packets received with CRC errors on Port 0 are dropped. 1h Packets received with CRC errors on Port 0 are transferred to the destination ports.
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad 0h Short packets are dropped. 1h Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove. 0h Do not remove the CRC on Port 0 transmit (egress) packets. 1h Remove the CRC on all Port 0 transmit (egress) packets.
12	P0_TX_CRC_TYPE	R/W	0h	
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.

Table 14-26915. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged 0h `Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress.` 1h `Priority tagged packets are processed unchanged.`
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged 0h `Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress.` 1h `Priority tagged packets are processed unchanged.`
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged 0h `Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11:0] on ingress.` 1h `Priority tagged packets are processed unchanged.`
2	P0_ENABLE	R/W	0h	Port 0 Enable 0h `CPPI port (port 0) packet operations are disabled` 1h `CPPI port (port 0) packet operations are enabled`
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode: 0h `CPSW_NU is in the VLAN unaware mode.` 1h `CPSW_NU is in the VLAN aware mode.`
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0h `Customer switch. VLAN processing uses the inner_vlan_ltype.` 1h `Service switch. VLAN processing uses the outer_vlan_ltype.`

14.9.3.1.2.65 CPSW3_CPSW_NU_EM_CONTROL_REG Register

1 CPSW3_CPSW_NU_EM_CONTROL_REG Register (Offset = 10h) [reset = 0h]

CPSW Emulation Control

Return to Summary Table

Table 14-26916. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8923. CPSW3_CPSW_NU_EM_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>SOFT</td><td>FREE</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26918. CPSW3_CPSW_NU_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.3.1.2.66 CPSW3_CPSW_NU_STAT_PORT_EN_REG Register

1 CPSW3_CPSW_NU_STAT_PORT_EN_REG Register (Offset = 14h) [reset = 0h]

CPSW Statistics Port Enable

Return to Summary Table

Table 14-26919. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-8924. CPSW3_CPSW_NU_STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26921. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable (if N > 8) 0h Port 8 statistics are not enabled 1h Port 8 statistics are enabled.
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable (if N > 7) 0h Port 7 statistics are not enabled 1h Port 7 statistics are enabled.
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable (if N > 6) 0h Port 6 statistics are not enabled 1h Port 6 statistics are enabled.
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable (if N > 5) 0h Port 5 statistics are not enabled 1h Port 5 statistics are enabled.
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable (if N > 4) 0h Port 4 statistics are not enabled 1h Port 4 statistics are enabled.
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable (if N > 3) 0h Port 3 statistics are not enabled 1h Port 3 statistics are enabled.

Table 14-26921. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable (if N > 2) 0h Port 2 statistics are not enabled 1h Port 2 statistics are enabled.
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable 0h Port 1 statistics are not enabled 1h Port 1 statistics are enabled.
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable 0h Port 0 statistics are not enabled 1h Port 0 statistics are enabled.

14.9.3.1.2.67 CPSW3_CPSW_NU_PTYPE_REG Register

1 CPSW3_CPSW_NU_PTYPE_REG Register (Offset = 18h) [reset = 0h]

CPSW Transmit Priority Type

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Table 14-26922. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h**

Figure 14-8925. CPSW3_CPSW_NU_PTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
RESERVED			ESC_PRI_LD_VAL				
NONE			R/W				
0h			0h				

Table 14-26924. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate (if N > 8) 0h Port 8 priority type fixed 1h Port 8 priority type escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate (if N > 7) 0h Port 7 priority type fixed 1h Port 7 priority type escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate (if N > 6) 0h Port 6 priority type fixed 1h Port 6 priority type escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate (if N > 5) 0h Port 5 priority type fixed 1h Port 5 priority type escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate (if N > 4) 0h Port 4 priority type fixed 1h Port 4 priority type escalate

Table 14-26924. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate (if N > 3) 0h Port 3 priority type fixed 1h Port 3 priority type escalate
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate (if N > 2) 0h Port 2 priority type fixed 1h Port 2 priority type escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate 0h Port 1 priority type fixed 1h Port 1 priority type escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate 0h Port 0 priority type fixed 1h Port 0 priority type escalate
7:5	RESERVED	NONE	0h	Reserved
4:0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value. When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of ESC_PRI_LD_VAL = 2h.

14.9.3.1.2.68 CPSW3_CPSW_NU_SOFT_IDLE_REG Register

1 CPSW3_CPSW_NU_SOFT_IDLE_REG Register (Offset = 1Ch) [reset = 0h]

CPSW Software Idle

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Table 14-26925. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-8926. CPSW3_CPSW_NU_SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
NONE							R/W
0h							0h

Table 14-26927. CPSW3_CPSW_NU_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

0	SOFT_IDLE	R/W	0h	Software Idle.
				`0h Not in Idle.`
				`1h Command a MCU_CPSW0 software Idle. When set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.`

14.9.3.1.2.69 CPSW3_CPSW_NU_THRU_RATE_REG Register

1 CPSW3_CPSW_NU_THRU_RATE_REG Register (Offset = 20h) [reset = 3001h]

CPSW Thru Rate

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Table 14-26928. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h**

Figure 14-8927. CPSW3_CPSW_NU_THRU_RATE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">SL_RX_THRU_RATE</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">3h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">P0_RX_THRU_RATE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
</table>

Table 14-26930. CPSW3_CPSW_NU_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	SL_RX_THRU_RATE	R/W	3h	Ethernet Port Switch FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11:4	RESERVED	NONE	0h	Reserved
3:0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO (port 0) receive through rate. This register value is the maximum throughput of the CPPI FIFO (port 0) into the MCU_CPSW0. The minimum value is 1. This field is not intended to be changed by the user.

14.9.3.1.2.70 CPSW3_CPSW_NU_GAP_THRESH_REG Register

1 CPSW3_CPSW_NU_GAP_THRESH_REG Register (Offset = 24h) [reset = Bh]

CPSW Transmit FIFO Short Gap Threshold

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Table 14-26931. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-8928. CPSW3_CPSW_NU_GAP_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			GAP_THRESH				
NONE			R/W				
0h			Bh				

Table 14-26933. CPSW3_CPSW_NU_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

14.9.3.1.2.71 CPSW3_CPSW_NU_EEE_PRESCALE_REG Register

1 CPSW3_CPSW_NU_EEE_PRESCALE_REG Register (Offset = 2Ch) [reset = 0h]

CPSW Energy Efficient Ethernet Prescale Value

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Table 14-26934. Instance Table

Instance Name	Physical Address
CPSW0	**0800 002Ch**

Figure 14-8929. CPSW3_CPSW_NU_EEE_PRESCALE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">EEE_PRESCALE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EEE_PRESCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26936. CPSW3_CPSW_NU_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

14.9.3.1.2.72 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register

1 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 30h) [reset = FFFFFFFFh]

CPSW PFC Tx Global Out Flow Threshold Set

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Table 14-26937. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-8930. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
Fh				Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
Fh				Fh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
Fh				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
Fh				Fh			

Table 14-26939. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.9.3.1.2.73 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register

1 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 34h) [reset = 0h]

CPSW PFC Tx Global Out Flow Threshold Clear

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Table 14-26940. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-8931. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-26942. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.9.3.1.2.74 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 38h) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set Low

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Table 14-26943. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-8932. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI2							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI1							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI0							
R/W							
FFh							

Table 14-26945. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.9.3.1.2.75 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set High

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Table 14-26946. Instance Table

Instance Name	Physical Address
CPSW0	**0800 003Ch**

Figure 14-8933. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI6							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI5							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI4							
R/W							
FFh							

Table 14-26948. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.9.3.1.2.76 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 40h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear Low

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Table 14-26949. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h**

Figure 14-8934. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI2							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI1							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI0							
R/W							
0h							

Table 14-26951. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.9.3.1.2.77 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 44h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear High

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Table 14-26952. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h**

Figure 14-8935. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI6							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI5							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI4							
R/W							
0h							

Table 14-26954. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.9.3.1.2.78 CPSW3_CPSW_NU_VLAN_LTYPE_REG Register

1 CPSW3_CPSW_NU_VLAN_LTYPE_REG Register (Offset = 50h) [reset = 88A88100h]

VLAN Length/type

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Table 14-26955. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h**

Figure 14-8936. CPSW3_CPSW_NU_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
VLAN_LTYPE_OUTER							
R/W							
88A8h							
23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER							
R/W							
88A8h							
15	14	13	12	11	10	9	8
VLAN_LTYPE_INNER							
R/W							
8100h							
7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER							
R/W							
8100h							

Table 14-26957. CPSW3_CPSW_NU_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15:0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

14.9.3.1.2.79 CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register

1 CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register (Offset = 54h) [reset = 0h]

Enhanced Scheduled Traffic Host Event Domain

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Table 14-26958. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0054h**

Figure 14-8937. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EST_TS_DOMAIN							
R/W							
0h							

Table 14-26960. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

14.9.3.1.2.80 CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register

1 CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register (Offset = 58h) [reset = 0h]

Cut-thru Threshold

Return to Summary Table

Table 14-26961. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0058h**

Figure 14-8938. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CUT_THRESH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26963. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CUT_THRESH	R/W	0h	Cut_thru_threshold. This is not intended to be changed by software.

14.9.3.1.2.81 CPSW3_CPSW_NU_FREQUENCY_REG Register

1 CPSW3_CPSW_NU_FREQUENCY_REG Register (Offset = 5Ch) [reset = 0h]

CPSW CPPI_CLK Frequency in Mhz

Return to Summary Table

Table 14-26964. Instance Table

Instance Name	Physical Address
CPSW0	**0800 005Ch**

Figure 14-8939. CPSW3_CPSW_NU_FREQUENCY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CPSW_FREQUENCY	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPSW_FREQUENCY							
R/W							
0h							

Table 14-26966. CPSW3_CPSW_NU_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	CPSW_FREQUENCY	R/W	0h	CPSW Frequency. This is the frequency in Mhz of the VBUSP_GCLK. The frequency is rounded to the nearest Mhz. This value is used in auto speed detection for cut-thru operations.

14.9.3.1.2.82 CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register

1 CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register (Offset = 60h) [reset = 64h]

IET Hold Count Load Value for cut thru packets

Return to Summary Table

Table 14-26967. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0060h**

Figure 14-8940. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IET_HOLD_CNT_LD_VAL							
R/W							
64h							

Table 14-26969. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	IET_HOLD_CNT_LD_VAL	R/W	64h	Cut-thru IET Hold Count Load Value. This value is loaded into counters to count the time that cut-thru packets are allowed to prempt traffic in advance in order to reduce cut-thru latency with IET operations. This is not intended to be changed by software.

14.9.3.1.2.83 CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register (Offset = 100h) [reset = 7E8h]

Transmit Priority 0 Maximum Length

Return to Summary Table

Table 14-26970. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0100h**

Figure 14-8941. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI0_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI0_MAXLEN							
R/W							
7E8h							

Table 14-26972. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI0_MAXLEN	R/W	7E8h	Transmit Priority 0 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on egress for all ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.84 CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register (Offset = 104h) [reset = 7E8h]

Transmit Priority 1 Maximum Length

Return to Summary Table

Table 14-26973. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0104h**

Figure 14-8942. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI1_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI1_MAXLEN							
R/W							
7E8h							

Table 14-26975. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.85 CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register (Offset = 108h) [reset = 7E8h]

Transmit Priority 2 Maximum Length

Return to Summary Table

Table 14-26976. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0108h**

Figure 14-8943. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI2_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI2_MAXLEN							
R/W							
7E8h							

Table 14-26978. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI2_MAXLEN	R/W	7E8h	Transmit Priority 2 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.86 CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register (Offset = 10Ch) [reset = 7E8h]

Transmit Priority 3 Maximum Length

Return to Summary Table

Table 14-26979. Instance Table

Instance Name	Physical Address
CPSW0	**0800 010Ch**

Figure 14-8944. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI3_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI3_MAXLEN							
R/W							
7E8h							

Table 14-26981. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.87 CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register (Offset = 110h) [reset = 7E8h]

Transmit Priority 4 Maximum Length

Return to Summary Table

Table 14-26982. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0110h**

Figure 14-8945. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI4_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI4_MAXLEN							
R/W							
7E8h							

Table 14-26984. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.88 CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register (Offset = 114h) [reset = 7E8h]

Transmit Priority 5 Maximum Length

Return to Summary Table

Table 14-26985. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0114h**

Figure 14-8946. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI5_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI5_MAXLEN							
R/W							
7E8h							

Table 14-26987. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.89 CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register (Offset = 118h) [reset = 7E8h]

Transmit Priority 6 Maximum Length

Return to Summary Table

Table 14-26988. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0118h**

Figure 14-8947. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI6_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI6_MAXLEN							
R/W							
7E8h							

Table 14-26990. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI6_MAXLEN	R/W	7E8h	Transmit Priority 6 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.90 CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register

1 CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register (Offset = 11Ch) [reset = 7E8h]

Transmit Priority 7 Maximum Length

Return to Summary Table

Table 14-26991. Instance Table

Instance Name	Physical Address
CPSW0	**0800 011Ch**

Figure 14-8948. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI7_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI7_MAXLEN							
R/W							
7E8h							

Table 14-26993. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.3.1.2.91 CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register

1 CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register (Offset = 0h + formula) [reset = 0h]

MDIO User Access Register

Return to Summary Table

Offset = 80h + (j * 8h); where j = 0 to 1d

Table 14-26994. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h + formula**

Figure 14-8949. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Name Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W			R/W				
0h			0h				
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-26996. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1h causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28:26	RESERVED	NONE	0h	Reserved
25:21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20:16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.

Table 14-26996. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

14.9.3.1.2.92 CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register

1 CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register (Offset = 4h + formula) [reset = 0h]

MDIO User PHY Select Register

Return to Summary Table

Offset = 84h + (j * 8h); where j = 0 to 1d

Table 14-26997. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h + formula**

Figure 14-8950. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W	R/W	NONE	R/W				
0h	0h	0h	0h				

Table 14-26999. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in [4-0] PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	NONE	0h	Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored.

14.9.3.1.2.93 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register (Offset = 4h) [reset = 0h]

CPPI Port 0 Control

Return to Summary Table

Table 14-27000. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-8951. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CUT_THRU_MODE_ETH	RX_REMAP_DSCP_V6	RX_REMAP_DSCP_V4	RX_REMAP_VLAN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RX_CHECKSUM_EN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-27002. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

19	CUT_THRU_MODE_ETH	R/W	0h	Port 0 Cut-Thru Mode.
				Packets always egress from the host port (CPPI egress) store-and-forward regardless of this bit setting. This bit determines how a receive port operates when the host port is in a cut-thru packet destination mask.
				`0h` `Force packets with the host port in the destination mask to be store-and-forward to all destination ports.`
				`1h` `The host port operates similar to Ethernet ports. A cut-thru packet with the host in the destination mask will not force the packet to be store-and-forward unless the cut-thru packet is held off due to word counts or because another cut-thru packet on the host port priority.`

18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
16	RX_REMAP_VLAN	R/W	0h	Port 0 receive remap thread to VLAN.
15	RX_ECC_ERR_EN	R/W	0h	Port 0 receive ECC Error Enable. This bit must be set to enable receive ECC error operations

Table 14-27002. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	TX_ECC_ERR_EN	R/W	0h	Port 0 transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations
13:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable 0h IPV6 DSCP priority mapping is disabled 1h IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPV4 DSCP enable 0h IPV4 DSCP priority mapping is disabled 1h IPV4 DSCP priority mapping is enabled
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive (port 0 ingress) Checksum Enable 0h Port 0 receive checksum is disabled 1h Port 0 receive checksum is enabled

14.9.3.1.2.94 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register (Offset = 8h) [reset = 0h]

CPPI Port 0 Flow ID Offset

Return to Summary Table

Table 14-27003. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-8952. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		VALUE					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-27005. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

14.9.3.1.2.95 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register (Offset = 10h) [reset = 1h]

CPPI Port 0 FIFO Block Usage Count

Return to Summary Table

Table 14-27006. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8953. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT					
NONE		R					
0h		1h					

Table 14-27008. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage. This value is the number of blocks allocated in the receive FIFO.

14.9.3.1.2.96 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register (Offset = 14h) [reset = 0h]

CPPI Port 0 VLAN

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Table 14-27009. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0014h**

Figure 14-8954. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">PORT_PRI</td><td>PORT_CFI</td><td colspan="4">PORT_VID</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PORT_VID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27011. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.3.1.2.97 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register (Offset = 18h) [reset = 76543210h]

CPPI Port 0 Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 14-27012. Instance Table

Instance Name	Physical Address
CPSW0	0800 0018h

Figure 14-8955. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27014. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	NONE	0h	Reserved

Table 14-27014. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.3.1.2.98 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register (Offset = 1Ch) [reset = 0h]

CPPI Port 0 Priority Control

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Table 14-27015. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-8956. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>RX_PTYPE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27017. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority).
15:9	RESERVED	NONE	0h	Reserved
8	RX_PTYPE	R/W	0h	Receive Priority Type 0h Fixed priority 1h Round Robin priority
7:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.99 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register (Offset = 20h) [reset = 76543210h]

CPPI Port 0 RX Pkt Pri to Header Pri Map

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Table 14-27018. Instance Table

Instance Name	Physical Address
CPSW0	0800 0020h

Figure 14-8957. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27020. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	NONE	0h	Reserved

Table 14-27020. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.3.1.2.100 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register (Offset = 24h) [reset = 5EEh]

CPPI Port 0 Receive Frame Max Length

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Table 14-27021. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-8958. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">5EEh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5EEh</td></tr>
</table>

Table 14-27023. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_P0_RX_MAXLEN_REG are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when fifo_blk_size = 4. When fifo_blk_size = 1 the maximum value is 2024 (including VLAN).

14.9.3.1.2.101 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register (Offset = 28h) [reset = 1245678h]

CPPI Port 0 Transmit Block Sub Per Priority

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Table 14-27024. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h**

Figure 14-8959. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-27026. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 7 frames (value 0 means use all).
27:24	PRI6	R/W	1h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 6 frames (value 0 means use all).
23:20	PRI5	R/W	2h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 5 frames (value 0 means use all).
19:16	PRI4	R/W	4h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 4 frames (value 0 means use all).
15:12	PRI3	R/W	5h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 3 frames (value 0 means use all).
11:8	PRI2	R/W	6h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 2 frames (value 0 means use all).
7:4	PRI1	R/W	7h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 1 frames (value 0 means use all).

Table 14-27026. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRI0	R/W	8h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 0 frames (value 0 means use all).

14.9.3.1.2.102 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register (Offset = 30h) [reset = 0h]

Port 0 EEE Idle to LPI counter

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Table 14-27027. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-8960. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27029. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

14.9.3.1.2.103 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register (Offset = 34h) [reset = 0h]

Port 0 EEE LPI to wake counter

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Table 14-27030. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-8961. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27032. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

14.9.3.1.2.104 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register (Offset = 38h) [reset = 60h]

Port 0 EEE status

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Table 14-27033. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-8962. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-27035. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.3.1.2.105 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register (Offset = 50h) [reset = 0h]

Port 0 FIFO Status

Return to Summary Table

Table 14-27036. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h**

Figure 14-8963. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-27038. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. Note: For N=2 this field is always zero (there is no transmit FIFO).

14.9.3.1.2.106 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register (Offset = 120h + formula) [reset = 0h]

CPPI Port 0 Receive IPV4/IPV6 DSCP Map N

Return to Summary Table

Offset = 1120h + (j * 4h); where j = 0 to 7d

Table 14-27039. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0120h + formula**

Figure 14-8964. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-27041. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-27041. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.3.1.2.107 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register (Offset = 140h + formula) [reset = 0h]

CPPI Port 0 Rx Priority P Committed Information Rate

Return to Summary Table

Offset = 1140h + (j * 4h); where j = 0 to 7d

Table 14-27042. Instance Table

Instance Name	Physical Address
CPSW0	0800 0140h + formula

Figure 14-8965. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-27044. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N Committed Information Rate Count Value

14.9.3.1.2.108 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register (Offset = 160h + formula) [reset = 0h]

CPPI Port 0 Rx Priority P Excess Information Rate

Return to Summary Table

Offset = 1160h + (j * 4h); where j = 0 to 7d

Table 14-27045. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0160h + formula**

Figure 14-8966. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-27047. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N EIR

14.9.3.1.2.109 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register (Offset = 180h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 14-27048. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0180h**

Figure 14-8967. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI3</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1Fh</td></tr>
</table>

Table 14-27050. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.110 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register (Offset = 184h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set High

Return to Summary Table

Table 14-27051. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0184h**

Figure 14-8968. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27053. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.111 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 188h) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr Low

Return to Summary Table

Table 14-27054. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0188h**

Figure 14-8969. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27056. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.112 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 18Ch) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr High

Return to Summary Table

Table 14-27057. Instance Table

Instance Name	Physical Address
CPSW0	0800 018Ch

Figure 14-8970. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27059. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.113 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 190h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

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Table 14-27060. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0190h**

Figure 14-8971. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-27062. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.114 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 194h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

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Table 14-27063. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0194h**

Figure 14-8972. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27065. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.115 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 198h) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

Return to Summary Table

Table 14-27066. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0198h**

Figure 14-8973. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27068. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.116 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 19Ch) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

Return to Summary Table

Table 14-27069. Instance Table

Instance Name	Physical Address
CPSW0	**0800 019Ch**

Figure 14-8974. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27071. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.117 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register (Offset = 300h) [reset = 4030201h]

CPPI Port 0 CPPI Source ID A

Return to Summary Table

Table 14-27072. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0300h**

Figure 14-8975. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24
PORT4							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PORT3							
R/W							
3h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PORT2							
R/W							
2h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT1							
R/W							
1h							

Table 14-27074. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 4.
23:16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 3.
15:8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 2.
7:0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1.

14.9.3.1.2.118 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register (Offset = 304h) [reset = 8070605h]

CPPI Port 0 CPPI Source ID B

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Table 14-27075. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0304h**

Figure 14-8976. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24
PORT8							
R/W							
8h							
23	22	21	20	19	18	17	16
PORT7							
R/W							
7h							
15	14	13	12	11	10	9	8
PORT6							
R/W							
6h							
7	6	5	4	3	2	1	0
PORT5							
R/W							
5h							

Table 14-27077. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 8.
23:16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 7.
15:8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 6.
7:0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 5.

14.9.3.1.2.119 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register (Offset = 320h) [reset = 0h]

CPPI Port 0 Host Blocks Priority

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Table 14-27078. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0320h**

Figure 14-8977. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-27080. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Host Blocks
27:24	PRI6	R/W	0h	Priority 6 Host Blocks
23:20	PRI5	R/W	0h	Priority 5 Host Blocks
19:16	PRI4	R/W	0h	Priority 4 Host Blocks
15:12	PRI3	R/W	0h	Priority 3 Host Blocks
11:8	PRI2	R/W	0h	Priority 2 Host Blocks
7:4	PRI1	R/W	0h	Priority 1 Host Blocks
3:0	PRI0	R/W	0h	Priority 0 Host Blocks

14.9.3.1.2.120 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register (Offset = 0h) [reset = 0h]

Reserved

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Table 14-27081. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-8978. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-27083. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.9.3.1.2.121 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register (Offset = 4h) [reset = 0h]

Enet Port N Control

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Table 14-27084. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-8979. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-27086. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h EST is disabled on the port 1h EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable. 0h IET is disabled on the port 1h IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations

Table 14-27086. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency 1h Cut-thru packets to the port will be prempted as usual by the express MAC
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h IPV6 DSCP priority mapping is disabled 1h IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h IPV4 DSCP priority mapping is disabled 1h IPV4 DSCP priority mapping is enabled
0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.122 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register (Offset = 8h) [reset = 1004h]

Enet Port N FIFO Max Blocks

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Table 14-27087. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-8980. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-27089. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.9.3.1.2.123 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register (Offset = 10h) [reset = 1h]

Enet Port N FIFO Block Usage Count

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Table 14-27090. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-8981. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 14-27092. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.9.3.1.2.124 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register (Offset = 14h) [reset = 0h]

Enet Port N VLAN

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Table 14-27093. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-8982. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W							
0h							

Table 14-27095. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.3.1.2.125 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register (Offset = 18h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 14-27096. Instance Table

Instance Name	Physical Address
CPSW0	0800 0018h

Figure 14-8983. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27098. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.

Table 14-27098. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.3.1.2.126 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register (Offset = 1Ch) [reset = 9000h]

Enet Port N Priority Control

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Table 14-27099. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 001Ch**

Figure 14-8984. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">TX_HOST_BLKS_REM</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27101. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.127 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register (Offset = 20h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-27102. Instance Table

Instance Name	Physical Address
CPSW0	0800 0020h

Figure 14-8985. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27104. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.

Table 14-27104. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.3.1.2.128 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register (Offset = 24h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

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Table 14-27105. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-8986. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-27107. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.9.3.1.2.129 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register (Offset = 28h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

Return to Summary Table

Table 14-27108. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h**

Figure 14-8987. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-27110. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.9.3.1.2.130 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register (Offset = 30h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

Return to Summary Table

Table 14-27111. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-8988. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27113. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.9.3.1.2.131 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register (Offset = 34h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to Summary Table

Table 14-27114. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-8989. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27116. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.9.3.1.2.132 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register (Offset = 38h) [reset = 62h]

Enet Port N EEE status

Return to Summary Table

Table 14-27117. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-8990. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-27119. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.3.1.2.133 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register (Offset = 40h) [reset = 8h]

Enet Port N IET Control

Return to Summary Table

Table 14-27120. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h**

Figure 14-8991. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLEVERIFY	MAC_HOLD	MAC_PENABLE
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	0h

Table 14-27122. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved

Table 14-27122. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.9.3.1.2.134 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register (Offset = 44h) [reset = 0h]

Enet Port N IET Status

Return to Summary Table

Table 14-27123. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h**

Figure 14-8992. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-27125. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.9.3.1.2.135 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register (Offset = 48h) [reset = 1312D0h]

Enet Port N IET VERIFY

Return to Summary Table

Table 14-27126. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0048h**

Figure 14-8993. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_VERIFY_CNT							
R/W							
1312D0h							
15	14	13	12	11	10	9	8
MAC_VERIFY_CNT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
MAC_VERIFY_CNT							
R/W							
1312D0h							

Table 14-27128. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.9.3.1.2.136 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register (Offset = 50h) [reset = FF00h]

Enet Port N FIFO STATUS

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Table 14-27129. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h**

Figure 14-8994. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R							
FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-27131. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.9.3.1.2.137 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register (Offset = 60h) [reset = 0h]

Enet Port N EST CONTROL

Return to Summary Table

Table 14-27132. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0060h**

Figure 14-8995. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W							
0h							
15	14	13	12	11	10	9	8
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-27134. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-27134. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.9.3.1.2.138 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register (Offset = 120h + formula) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map M

Return to Summary Table

Offset = 2120h + (j * 4h); where j = 0 to 7d

Table 14-27135. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0120h + formula**

Figure 14-8996. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-27137. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-27137. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.3.1.2.139 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register (Offset = 140h + formula) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

Return to Summary Table

Offset = 2140h + (j * 4h); where j = 0 to 7d

Table 14-27138. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0140h + formula**

Figure 14-8997. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-27140. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.9.3.1.2.140 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register (Offset = 160h + formula) [reset = 0h]

Enet Port N Rx Priority P Excess Informatoin Rate Value

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Offset = 2160h + (j * 4h); where j = 0 to 7d

Table 14-27141. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0160h + formula**

Figure 14-8998. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_EIR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_EIR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_EIR							
R/W							
0h							

Table 14-27143. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.9.3.1.2.141 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register (Offset = 180h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set Low

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Table 14-27144. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0180h**

Figure 14-8999. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-27146. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.142 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register (Offset = 184h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set High

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Table 14-27147. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0184h**

Figure 14-9000. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27149. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.143 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

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Table 14-27150. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0188h**

Figure 14-9001. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27152. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.144 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 18Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

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Table 14-27153. Instance Table

Instance Name	Physical Address
CPSW0	**0800 018Ch**

Figure 14-9002. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27155. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.145 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 190h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 14-27156. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0190h**

Figure 14-9003. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-27158. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.146 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 194h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 14-27159. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0194h**

Figure 14-9004. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27161. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.147 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 14-27162. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0198h**

Figure 14-9005. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27164. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.148 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 19Ch) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 14-27165. Instance Table

Instance Name	Physical Address
CPSW0	0800 019Ch

Figure 14-9006. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27167. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.149 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

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Table 14-27168. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0300h**

Figure 14-9007. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27170. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.9.3.1.2.150 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

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Table 14-27171. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0304h**

Figure 14-9008. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27173. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.9.3.1.2.151 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register (Offset = 308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

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Table 14-27174. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0308h**

Figure 14-9009. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-27176. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.9.3.1.2.152 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register (Offset = 30Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

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Table 14-27177. Instance Table

Instance Name	Physical Address
CPSW0	**0800 030Ch**

Figure 14-9010. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-27179. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.9.3.1.2.153 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register (Offset = 310h) [reset = 0h]

Enet Port N Time Sync Control

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Table 14-27180. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0310h**

Figure 14-9011. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27182. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-27182. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.9.3.1.2.154 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register (Offset = 314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-27183. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0314h**

Figure 14-9012. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE1							
R/W							
0h							

Table 14-27185. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.9.3.1.2.155 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register (Offset = 318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-27186. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0318h**

Figure 14-9013. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-27188. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.9.3.1.2.156 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register (Offset = 31Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

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Table 14-27189. Instance Table

Instance Name	Physical Address
CPSW0	**0800 031Ch**

Figure 14-9014. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE2							
R/W							
0h							

Table 14-27191. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h `Unicast disabled` 1h `Unicast enabled`
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h `TTL must be 1h` 1h `TTL may be any value`
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h `Disabled` 1h `Destination port number (decimal) 320 is enabled`
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h `Disabled` 1h `Destination port number (decimal) 319 is enabled`

Table 14-27191. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.9.3.1.2.157 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register (Offset = 320h) [reset = 40000h]

Enet Port N Time Sync Control 2

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Table 14-27192. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0320h**

Figure 14-9015. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TS_DOMAIN_OFFSET</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_MCAST_TYPE_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_MCAST_TYPE_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27194. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.9.3.1.2.158 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register (Offset = 330h) [reset = 0h]

Enet Port N Mac Control

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Table 14-27195. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0330h**

Figure 14-9016. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	RSVD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	6	5	4	3	2	1	0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27197. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h MAC control frames are filtered (but acted upon if enabled). 1h MAC control frames are transferred to memory.

Table 14-27197. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/ code errors and undersized are short frames without errors.
				`0h Short frames are filtered.`
				`1h Short frames are transferred to memory.`

22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set.
				`0h Frames containing errors are filtered.`
				`1h Frames containing errors are transferred to memory.`

21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.

15	IFCTL_A	R/W	0h	Determines the RMII link speed.
				`0h 10Mbps operation`
				`0h 100Mbps operation`

14:13	RESERVED	NONE	0h	Reserved

12	CRC_TYPE	R/W	0h	Port CRC Type.
				`0h Ethernet CRC`
				`1h Castagnoli CRC`

11	CMD_IDLE	R/W	0h	Command Idle.
				`0h Idle not commanded`
				`1h Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)`

10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable.
				`0h Transmit with a short IPG is disabled`
				`1h Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.`

Table 14-27197. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.9.3.1.2.159 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register (Offset = 334h) [reset = F0000000h]

Enet Port N Mac Status

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Table 14-27198. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0334h**

Figure 14-9017. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27200. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command) `0h` The port is not in the Idle state. `1h` The port is in the Idle state.
30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	0h	Reserved
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.

Table 14-27200. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	0h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.9.3.1.2.160 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register (Offset = 338h) [reset = 0h]

Enet Port N Mac Soft Reset

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Table 14-27201. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0338h**

Figure 14-9018. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-27203. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.9.3.1.2.161 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register (Offset = 33Ch) [reset = 0h]

Enet Port N Mac Backoff Test

Return to Summary Table

Table 14-27204. Instance Table

Instance Name	Physical Address
CPSW0	**0800 033Ch**

Figure 14-9019. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RNDNUM							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_BACKOFF							
R							
0h							

Table 14-27206. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-27206. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.9.3.1.2.162 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

Return to Summary Table

Table 14-27207. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0340h**

Figure 14-9020. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-27209. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.3.1.2.163 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register (Offset = 350h + formula) [reset = 0h]

Enet Port N PFC Priority P Rx Pause Timer

Return to Summary Table

Offset = 2350h + (j * 4h); where j = 0 to 7d

Table 14-27210. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0350h + formula**

Figure 14-9021. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-27212. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.3.1.2.164 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

Return to Summary Table

Table 14-27213. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0370h**

Figure 14-9022. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-27215. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.3.1.2.165 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register (Offset = 380h + formula) [reset = 0h]

Enet Port N PFC Priority P Tx Pause Timer

Return to Summary Table

Offset = 2380h + (j * 4h); where j = 0 to 7d

Table 14-27216. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0380h + formula**

Figure 14-9023. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-27218. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.3.1.2.166 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register (Offset = 3A0h) [reset = 0h]

Enet Port N Emulation Control

Return to Summary Table

Table 14-27219. Instance Table

Instance Name	Physical Address
CPSW0	0800 03A0h

Figure 14-9024. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-27221. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.3.1.2.167 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register (Offset = 3A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

Return to Summary Table

Table 14-27222. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03A4h**

Figure 14-9025. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 14-27224. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.9.3.1.2.168 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register (Offset = 3A8h) [reset = 204h]

Enet Port N Port Configuration

Return to Summary Table

Table 14-27225. Instance Table

Instance Name	Physical Address
CPSW0	0800 03A8h

Figure 14-9026. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	6	5	4	3	2	1	0
INTERVLAN_ROUTES							
R							
4h							

Table 14-27227. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Intersperced Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.9.3.1.2.169 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 3ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

Return to Summary Table

Table 14-27228. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03ACh**

Figure 14-9027. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-27230. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.9.3.1.2.170 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register (Offset = 3B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

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Table 14-27231. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B0h**

Figure 14-9028. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 14-27233. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.9.3.1.2.171 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register (Offset = 3B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

Return to Summary Table

Table 14-27234. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B4h**

Figure 14-9029. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SA_39_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SA_47_40</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DA_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DA_15_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27236. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.9.3.1.2.172 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register (Offset = 3B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

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Table 14-27237. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B8h**

Figure 14-9030. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SA_15_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SA_23_16							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SA_31_24							
R/W							
0h							

Table 14-27239. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.9.3.1.2.173 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register (Offset = 3BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

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Table 14-27240. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03BCh**

Figure 14-9031. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
VID							
R/W							
0h							

Table 14-27242. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.9.3.1.2.174 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register (Offset = 3C0h) [reset = 0h]

Enet Port N Cut Thru Priority Enable

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Table 14-27243. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03C0h**

Figure 14-9032. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-27245. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.9.3.1.2.175 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register (Offset = 3C4h) [reset = 0h]

Enet Port Speed

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Table 14-27246. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03C4h**

Figure 14-9033. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PORT_SPEED_CHANGED	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
PORT_AUTO_SPEED				RESERVED			PORT_SPEED_AUTO_EN
R				NONE			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
RESERVED				PORT_SPEED_MANUAL			
NONE				R/W			
0h				0h			

Table 14-27248. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.9.3.1.2.176 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register (Offset = 0h) [reset = 0h]

Reserved

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Table 14-27249. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-9034. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-27251. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.9.3.1.2.177 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register (Offset = 4h) [reset = 0h]

Enet Port N Control

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Table 14-27252. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-9035. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-27254. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved

17	EST_PORT_EN	R/W	0h	EST Port Enable.
				`0h EST is disabled on the port`
				`1h EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`

16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable.
				`0h IET is disabled on the port`
				`1h IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`

15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations

Table 14-27254. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h `Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency` 1h `Cut-thru packets to the port will be prempted as usual by the express MAC`
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h `IPV6 DSCP priority mapping is disabled` 1h `IPV6 DSCP priority mapping is enabled`
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h `IPV4 DSCP priority mapping is disabled` 1h `IPV4 DSCP priority mapping is enabled`
0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.178 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register (Offset = 8h) [reset = 1004h]

Enet Port N FIFO Max Blocks

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Table 14-27255. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-9036. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-27257. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.9.3.1.2.179 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register (Offset = 10h) [reset = 1h]

Enet Port N FIFO Block Usage Count

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Table 14-27258. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-9037. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 14-27260. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.9.3.1.2.180 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register (Offset = 14h) [reset = 0h]

Enet Port N VLAN

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Table 14-27261. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-9038. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W							
0h							

Table 14-27263. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.3.1.2.181 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register (Offset = 18h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 14-27264. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h**

Figure 14-9039. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27266. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.

Table 14-27266. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.3.1.2.182 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register (Offset = 1Ch) [reset = 9000h]

Enet Port N Priority Control

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Table 14-27267. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-9040. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_FLOW_PRI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_HOST_BLKS_REM				RESERVED			
R/W				NONE			
9h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-27269. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.183 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register (Offset = 20h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-27270. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h**

Figure 14-9041. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-27272. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.

Table 14-27272. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.3.1.2.184 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register (Offset = 24h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

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Table 14-27273. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-9042. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">5EEh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5EEh</td></tr>
</table>

Table 14-27275. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.9.3.1.2.185 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register (Offset = 28h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

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Table 14-27276. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h**

Figure 14-9043. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-27278. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.9.3.1.2.186 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register (Offset = 30h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

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Table 14-27279. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-9044. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27281. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.9.3.1.2.187 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register (Offset = 34h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to Summary Table

Table 14-27282. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-9045. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27284. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.9.3.1.2.188 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register (Offset = 38h) [reset = 62h]

Enet Port N EEE status

Return to Summary Table

Table 14-27285. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-9046. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-27287. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.3.1.2.189 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register (Offset = 40h) [reset = 8h]

Enet Port N IET Control

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Table 14-27288. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h**

Figure 14-9047. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLE VERIFY	MAC_HOLD	MAC_PENABLE
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	0h

Table 14-27290. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved

Table 14-27290. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.9.3.1.2.190 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register (Offset = 44h) [reset = 0h]

Enet Port N IET Status

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Table 14-27291. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h**

Figure 14-9048. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-27293. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.9.3.1.2.191 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register (Offset = 48h) [reset = 1312D0h]

Enet Port N IET VERIFY

Return to Summary Table

Table 14-27294. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0048h**

Figure 14-9049. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_VERIFY_CNT							
R/W							
1312D0h							
15	14	13	12	11	10	9	8
MAC_VERIFY_CNT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
MAC_VERIFY_CNT							
R/W							
1312D0h							

Table 14-27296. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.9.3.1.2.192 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register (Offset = 50h) [reset = FF00h]

Enet Port N FIFO STATUS

Return to Summary Table

Table 14-27297. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h**

Figure 14-9050. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R							
FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-27299. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.9.3.1.2.193 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register (Offset = 60h) [reset = 0h]

Enet Port N EST CONTROL

Return to Summary Table

Table 14-27300. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0060h**

Figure 14-9051. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W							
0h							
15	14	13	12	11	10	9	8
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-27302. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-27302. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.9.3.1.2.194 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register (Offset = 120h + formula) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map M

Return to Summary Table

Offset = 3120h + (j * 4h); where j = 0 to 7d

Table 14-27303. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0120h + formula**

Figure 14-9052. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-27305. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-27305. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.3.1.2.195 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register (Offset = 140h + formula) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

Return to Summary Table

Offset = 3140h + (j * 4h); where j = 0 to 7d

Table 14-27306. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0140h + formula**

Figure 14-9053. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-27308. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.9.3.1.2.196 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register (Offset = 160h + formula) [reset = 0h]

Enet Port N Rx Priority P Excess Informatoin Rate Value

Return to Summary Table

Offset = 3160h + (j * 4h); where j = 0 to 7d

Table 14-27309. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0160h + formula**

Figure 14-9054. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-27311. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.9.3.1.2.197 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register (Offset = 180h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 14-27312. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0180h**

Figure 14-9055. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-27314. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.198 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register (Offset = 184h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set High

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Table 14-27315. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0184h**

Figure 14-9056. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27317. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.199 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

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Table 14-27318. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0188h**

Figure 14-9057. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27320. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.200 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 18Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

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Table 14-27321. Instance Table

Instance Name	Physical Address
CPSW0	**0800 018Ch**

Figure 14-9058. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27323. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.201 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 190h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 14-27324. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0190h**

Figure 14-9059. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-27326. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.3.1.2.202 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 194h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 14-27327. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0194h**

Figure 14-9060. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-27329. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.3.1.2.203 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 14-27330. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0198h**

Figure 14-9061. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27332. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.3.1.2.204 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 19Ch) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 14-27333. Instance Table

Instance Name	Physical Address
CPSW0	**0800 019Ch**

Figure 14-9062. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27335. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.3.1.2.205 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

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Table 14-27336. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0300h**

Figure 14-9063. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-27338. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.9.3.1.2.206 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

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Table 14-27339. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0304h**

Figure 14-9064. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-27341. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.9.3.1.2.207 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register (Offset = 308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

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Table 14-27342. Instance Table

Instance Name	Physical Address
CPSW0	0800 0308h

Figure 14-9065. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-27344. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.9.3.1.2.208 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register (Offset = 30Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

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Table 14-27345. Instance Table

Instance Name	Physical Address
CPSW0	**0800 030Ch**

Figure 14-9066. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-27347. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.9.3.1.2.209 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register (Offset = 310h) [reset = 0h]

Enet Port N Time Sync Control

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Table 14-27348. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0310h**

Figure 14-9067. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_MSG_TYPE_EN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27350. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-27350. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.9.3.1.2.210 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register (Offset = 314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-27351. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0314h**

Figure 14-9068. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	14	13	12	11	10	9	8
TS_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE1							
R/W							
0h							

Table 14-27353. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.9.3.1.2.211 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register (Offset = 318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-27354. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0318h**

Figure 14-9069. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-27356. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.9.3.1.2.212 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register (Offset = 31Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

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Table 14-27357. Instance Table

Instance Name	Physical Address
CPSW0	**0800 031Ch**

Figure 14-9070. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE2							
R/W							
0h							

Table 14-27359. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h Unicast disabled 1h Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h TTL must be 1h 1h TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h Disabled 1h Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h Disabled 1h Destination port number (decimal) 319 is enabled

Table 14-27359. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.9.3.1.2.213 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register (Offset = 320h) [reset = 40000h]

Enet Port N Time Sync Control 2

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Table 14-27360. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0320h**

Figure 14-9071. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TS_DOMAIN_OFFSET</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_MCAST_TYPE_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_MCAST_TYPE_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27362. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.9.3.1.2.214 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register (Offset = 330h) [reset = 0h]

Enet Port N Mac Control

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Table 14-27363. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0330h**

Figure 14-9072. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	RSVD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27365. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h `MAC control frames are filtered (but acted upon if enabled).` 1h `MAC control frames are transferred to memory.`

Table 14-27365. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors.
				`0h` `Short frames are filtered.`
				`1h` `Short frames are transferred to memory.`

22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set.
				`0h` `Frames containing errors are filtered.`
				`1h` `Frames containing errors are transferred to memory.`

21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.

15	IFCTL_A	R/W	0h	Determines the RMII link speed.
				`0h` `10Mbps operation`
				`0h` `100Mbps operation`

14:13	RESERVED	NONE	0h	Reserved

12	CRC_TYPE	R/W	0h	Port CRC Type.
				`0h` `Ethernet CRC`
				`1h` `Castagnoli CRC`

11	CMD_IDLE	R/W	0h	Command Idle.
				`0h` `Idle not commanded`
				`1h` `Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)`

10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable.
				`0h` `Transmit with a short IPG is disabled`
				`1h` `Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.`

Table 14-27365. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.9.3.1.2.215 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register (Offset = 334h) [reset = F0000000h]

Enet Port N Mac Status

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Table 14-27366. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0334h**

Figure 14-9073. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27368. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command)
				`0h The port is not in the Idle state.`
				`1h The port is in the Idle state.`

30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	0h	Reserved
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.

Table 14-27368. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	0h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.9.3.1.2.216 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register (Offset = 338h) [reset = 0h]

Enet Port N Mac Soft Reset

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Table 14-27369. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0338h**

Figure 14-9074. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-27371. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.9.3.1.2.217 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register (Offset = 33Ch) [reset = 0h]

Enet Port N Mac Backoff Test

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Table 14-27372. Instance Table

Instance Name	Physical Address
CPSW0	**0800 033Ch**

Figure 14-9075. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RNDNUM							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_BACKOFF							
R							
0h							

Table 14-27374. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-27374. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.9.3.1.2.218 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

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Table 14-27375. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0340h**

Figure 14-9076. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-27377. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.3.1.2.219 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register (Offset = 350h + formula) [reset = 0h]

Enet Port N PFC Priority P Rx Pause Timer

Return to Summary Table

Offset = 3350h + (j * 4h); where j = 0 to 7d

Table 14-27378. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0350h + formula**

Figure 14-9077. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-27380. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.3.1.2.220 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

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Table 14-27381. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0370h**

Figure 14-9078. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27383. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.3.1.2.221 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register (Offset = 380h + formula) [reset = 0h]

Enet Port N PFC Priority P Tx Pause Timer

Return to Summary Table

Offset = 3380h + (j * 4h); where j = 0 to 7d

Table 14-27384. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0380h + formula**

Figure 14-9079. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-27386. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.3.1.2.222 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register (Offset = 3A0h) [reset = 0h]

Enet Port N Emulation Control

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Table 14-27387. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03A0h**

Figure 14-9080. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-27389. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.3.1.2.223 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register (Offset = 3A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

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Table 14-27390. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03A4h**

Figure 14-9081. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_GAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_GAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Ch</td></tr>
</table>

Table 14-27392. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.9.3.1.2.224 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register (Offset = 3A8h) [reset = 204h]

Enet Port N Port Configuration

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Table 14-27393. Instance Table

Instance Name	Physical Address
CPSW0	0800 03A8h

Figure 14-9082. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	6	5	4	3	2	1	0
INTERVLAN_ROUTES							
R							
4h							

Table 14-27395. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Intersperced Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.9.3.1.2.225 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 3ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 14-27396. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03ACh**

Figure 14-9083. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-27398. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.9.3.1.2.226 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register (Offset = 3B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

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Table 14-27399. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B0h**

Figure 14-9084. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 14-27401. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.9.3.1.2.227 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register (Offset = 3B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

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Table 14-27402. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B4h**

Figure 14-9085. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 14-27404. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.9.3.1.2.228 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register (Offset = 3B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

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Table 14-27405. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03B8h**

Figure 14-9086. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 14-27407. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.9.3.1.2.229 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register (Offset = 3BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

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Table 14-27408. Instance Table

Instance Name	Physical Address
CPSW0	0800 03BCh

Figure 14-9087. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
VID							
R/W							
0h							

Table 14-27410. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.9.3.1.2.230 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register (Offset = 3C0h) [reset = 0h]

Enet Port N Cut Thru Priority Enable

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Table 14-27411. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03C0h**

Figure 14-9088. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-27413. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.9.3.1.2.231 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register

1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register (Offset = 3C4h) [reset = 0h]

Enet Port Speed

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Table 14-27414. Instance Table

Instance Name	Physical Address
CPSW0	**0800 03C4h**

Figure 14-9089. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PORT_SPEED_CHANGED	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
PORT_AUTO_SPEED				RESERVED			PORT_SPEED_AUTO_EN
R				NONE			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
RESERVED				PORT_SPEED_MANUAL			
NONE				R/W			
0h				0h			

Table 14-27416. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.9.3.1.2.232 CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register

1 CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register (Offset = 0h + formula) [reset = 0h]

The Revision Register contains the ID and revision information.

Return to Summary Table

Offset = 12000h + (j * 4h); where j = 0 to 255d

Table 14-27417. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h + formula**

Figure 14-9090. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		LOC					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
LOC							
R/W							
0h							
7	6	5	4	3	2	1	0
LOC							
R/W							
0h							

Table 14-27419. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	LOC	R/W	0h	RAM Location

14.9.3.1.2.233 CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register (Offset = 0h + formula) [reset = 0h]

Total number of good frames received

Return to Summary Table

Offset = 1A000h + (j * 200h); where j = 0 to 2d

Table 14-27420. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h + formula**

Figure 14-9091. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27422. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames received

14.9.3.1.2.234 CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register (Offset = 4h + formula) [reset = 0h]

Total number of good broadcast frames received

Return to Summary Table

Offset = 1A004h + (j * 200h); where j = 0 to 2d

Table 14-27423. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h + formula**

Figure 14-9092. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27425. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames received

14.9.3.1.2.235 CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register (Offset = 8h + formula) [reset = 0h]

Total number of good multicast frames received

Return to Summary Table

Offset = 1A008h + (j * 200h); where j = 0 to 2d

Table 14-27426. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h + formula**

Figure 14-9093. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27428. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames received

14.9.3.1.2.236 CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register (Offset = Ch + formula) [reset = 0h]

Total number of pause frames received

Return to Summary Table

Offset = 1A00Ch + (j * 200h); where j = 0 to 2d

Table 14-27429. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch + formula**

Figure 14-9094. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27431. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames received

14.9.3.1.2.237 CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register (Offset = 10h + formula) [reset = 0h]

Total number of CRC errors frames received

Return to Summary Table

Offset = 1A010h + (j * 200h); where j = 0 to 2d

Table 14-27432. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h + formula**

Figure 14-9095. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27434. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of CRC errors frames received

14.9.3.1.2.238 CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register (Offset = 14h + formula) [reset = 0h]

Total number of alignment/code errors received

Return to Summary Table

Offset = 1A014h + (j * 200h); where j = 0 to 2d

Table 14-27435. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h + formula**

Figure 14-9096. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27437. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of alignment/code errors received

14.9.3.1.2.239 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register (Offset = 18h + formula) [reset = 0h]

Total number of oversized frames received

Return to Summary Table

Offset = 1A018h + (j * 200h); where j = 0 to 2d

Table 14-27438. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h + formula**

Figure 14-9097. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-27440. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of oversized frames received

14.9.3.1.2.240 CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register (Offset = 1Ch + formula) [reset = 0h]

Total number of jabber frames received

Return to Summary Table

Offset = 1A01Ch + (j * 200h); where j = 0 to 2d

Table 14-27441. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch + formula**

Figure 14-9098. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27443. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of jabber frames received

14.9.3.1.2.241 CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register (Offset = 20h + formula) [reset = 0h]

Total number of undersized frames received

Return to Summary Table

Offset = 1A020h + (j * 200h); where j = 0 to 2d

Table 14-27444. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h + formula**

Figure 14-9099. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27446. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of undersized frames received

14.9.3.1.2.242 CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register (Offset = 24h + formula) [reset = 0h]

Total number of fragmented frames received

Return to Summary Table

Offset = 1A024h + (j * 200h); where j = 0 to 2d

Table 14-27447. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h + formula**

Figure 14-9100. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27449. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of fragmented frames received

14.9.3.1.2.243 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register (Offset = 28h + formula) [reset = 0h]

Total number of frames dropped by the ALE

Return to Summary Table

Offset = 1A028h + (j * 200h); where j = 0 to 2d

Table 14-27450. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h + formula**

Figure 14-9101. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27452. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames dropped by the ALE

14.9.3.1.2.244 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register (Offset = 2Ch + formula) [reset = 0h]

Total number of overrun frames dropped by the ALE

Return to Summary Table

Offset = 1A02Ch + (j * 200h); where j = 0 to 2d

Table 14-27453. Instance Table

Instance Name	Physical Address
CPSW0	**0800 002Ch + formula**

Figure 14-9102. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27455. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

14.9.3.1.2.245 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register (Offset = 30h + formula) [reset = 0h]

Total number of received bytes in good frames

Return to Summary Table

Offset = 1A030h + (j * 200h); where j = 0 to 2d

Table 14-27456. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h + formula**

Figure 14-9103. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27458. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of received bytes in good frames

14.9.3.1.2.246 CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register (Offset = 34h + formula) [reset = 0h]

Total number of good frames transmitted

Return to Summary Table

Offset = 1A034h + (j * 200h); where j = 0 to 2d

Table 14-27459. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h + formula**

Figure 14-9104. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27461. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames transmitted

14.9.3.1.2.247 CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register (Offset = 38h + formula) [reset = 0h]

Total number of good broadcast frames transmitted

Return to Summary Table

Offset = 1A038h + (j * 200h); where j = 0 to 2d

Table 14-27462. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h + formula**

Figure 14-9105. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27464. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

14.9.3.1.2.248 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register (Offset = 3Ch + formula) [reset = 0h]

Total number of good multicast frames transmitted

Return to Summary Table

Offset = 1A03Ch + (j * 200h); where j = 0 to 2d

Table 14-27465. Instance Table

Instance Name	Physical Address
CPSW0	**0800 003Ch + formula**

Figure 14-9106. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27467. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames transmitted

14.9.3.1.2.249 CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register (Offset = 40h + formula) [reset = 0h]

Total number of pause frames transmitted

Return to Summary Table

Offset = 1A040h + (j * 200h); where j = 0 to 2d

Table 14-27468. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h + formula**

Figure 14-9107. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-27470. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames transmitted

14.9.3.1.2.250 CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register (Offset = 44h + formula) [reset = 0h]

Total number of deferred frames transmitted

Return to Summary Table

Offset = 1A044h + (j * 200h); where j = 0 to 2d

Table 14-27471. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h + formula**

Figure 14-9108. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27473. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of deferred frames transmitted

14.9.3.1.2.251 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register (Offset = 48h + formula) [reset = 0h]

Total number of transmitted frames experiencing a collision

Return to Summary Table

Offset = 1A048h + (j * 200h); where j = 0 to 2d

Table 14-27474. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0048h + formula**

Figure 14-9109. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27476. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

14.9.3.1.2.252 CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register (Offset = 4Ch + formula) [reset = 0h]

Total number of transmitted frames experiencing a single collision

Return to Summary Table

Offset = 1A04Ch + (j * 200h); where j = 0 to 2d

Table 14-27477. Instance Table

Instance Name	Physical Address
CPSW0	**0800 004Ch + formula**

Figure 14-9110. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27479. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

14.9.3.1.2.253 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register (Offset = 50h + formula) [reset = 0h]

Total number of transmitted frames experiencing multiple collisions

Return to Summary Table

Offset = 1A050h + (j * 200h); where j = 0 to 2d

Table 14-27480. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h + formula**

Figure 14-9111. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27482. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

14.9.3.1.2.254 CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register (Offset = 54h + formula) [reset = 0h]

Total number of transmitted frames abandoned due to excessive collisions

Return to Summary Table

Offset = 1A054h + (j * 200h); where j = 0 to 2d

Table 14-27483. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0054h + formula**

Figure 14-9112. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27485. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

14.9.3.1.2.255 CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register (Offset = 58h + formula) [reset = 0h]

Total number of transmitted frames abandoned due to a late collision

Return to Summary Table

Offset = 1A058h + (j * 200h); where j = 0 to 2d

Table 14-27486. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0058h + formula**

Figure 14-9113. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27488. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

14.9.3.1.2.256 CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register (Offset = 5Ch + formula) [reset = 0h]

Total number of receive inter-packet gap errors (10G only)

Return to Summary Table

Offset = 1A05Ch + (j * 200h); where j = 0 to 2d

Table 14-27489. Instance Table

Instance Name	Physical Address
CPSW0	**0800 005Ch + formula**

Figure 14-9114. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-27491. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

14.9.3.1.2.257 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register (Offset = 60h + formula) [reset = 0h]

Total number of transmitted frames that experienced a carrier loss

Return to Summary Table

Offset = 1A060h + (j * 200h); where j = 0 to 2d

Table 14-27492. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0060h + formula**

Figure 14-9115. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27494. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

14.9.3.1.2.258 CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register (Offset = 64h + formula) [reset = 0h]

Total number of bytes in all good frames transmitted

Return to Summary Table

Offset = 1A064h + (j * 200h); where j = 0 to 2d

Table 14-27495. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0064h + formula**

Figure 14-9116. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27497. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

14.9.3.1.2.259 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register (Offset = 68h + formula) [reset = 0h]

Total number of 64-byte frames received and transmitted

Return to Summary Table

Offset = 1A068h + (j * 200h); where j = 0 to 2d

Table 14-27498. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0068h + formula**

Figure 14-9117. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27500. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

14.9.3.1.2.260 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register (Offset = 6Ch + formula) [reset = 0h]

Total number of frames of size 65 to 127 bytes received and transmitted

Return to Summary Table

Offset = 1A06Ch + (j * 200h); where j = 0 to 2d

Table 14-27501. Instance Table

Instance Name	Physical Address
CPSW0	**0800 006Ch + formula**

Figure 14-9118. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27503. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

14.9.3.1.2.261 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register (Offset = 70h + formula) [reset = 0h]

Total number of frames of size 128 to 255 bytes received and transmitted

Return to Summary Table

Offset = 1A070h + (j * 200h); where j = 0 to 2d

Table 14-27504. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0070h + formula**

Figure 14-9119. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27506. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

14.9.3.1.2.262 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register (Offset = 74h + formula) [reset = 0h]

Total number of frames of size 256 to 511 bytes received and transmitted

Return to Summary Table

Offset = 1A074h + (j * 200h); where j = 0 to 2d

Table 14-27507. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0074h + formula**

Figure 14-9120. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27509. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

14.9.3.1.2.263 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register (Offset = 78h + formula) [reset = 0h]

Total number of frames of size 512 to 1023 bytes received and transmitted

Return to Summary Table

Offset = 1A078h + (j * 200h); where j = 0 to 2d

Table 14-27510. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0078h + formula**

Figure 14-9121. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27512. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

14.9.3.1.2.264 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register (Offset = 7Ch + formula) [reset = 0h]

Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

Return to Summary Table

Offset = 1A07Ch + (j * 200h); where j = 0 to 2d

Table 14-27513. Instance Table

Instance Name	Physical Address
CPSW0	**0800 007Ch + formula**

Figure 14-9122. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27515. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

14.9.3.1.2.265 CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register (Offset = 80h + formula) [reset = 0h]

Total number of bytes received and transmitted

Return to Summary Table

Offset = 1A080h + (j * 200h); where j = 0 to 2d

Table 14-27516. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0080h + formula**

Figure 14-9123. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27518. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes received and transmitted

14.9.3.1.2.266 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register (Offset = 84h + formula) [reset = 0h]

Receive Bottom of FIFO Drop

Return to Summary Table

Offset = 1A084h + (j * 200h); where j = 0 to 2d

Table 14-27519. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0084h + formula**

Figure 14-9124. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27521. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

14.9.3.1.2.267 CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register (Offset = 88h + formula) [reset = 0h]

Total number of dropped frames received due to portmask

Return to Summary Table

Offset = 1A088h + (j * 200h); where j = 0 to 2d

Table 14-27522. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0088h + formula**

Figure 14-9125. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27524. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

14.9.3.1.2.268 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register (Offset = 8Ch + formula) [reset = 0h]

Receive Top of FIFO Drop

Return to Summary Table

Offset = 1A08Ch + (j * 200h); where j = 0 to 2d

Table 14-27525. Instance Table

Instance Name	Physical Address
CPSW0	**0800 008Ch + formula**

Figure 14-9126. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27527. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Top of FIFO Drop

14.9.3.1.2.269 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register (Offset = 90h + formula) [reset = 0h]

Total number of dropped frames due to ALE Rate Limiting

Return to Summary Table

Offset = 1A090h + (j * 200h); where j = 0 to 2d

Table 14-27528. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0090h + formula**

Figure 14-9127. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27530. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

14.9.3.1.2.270 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register (Offset = 94h + formula) [reset = 0h]

Total number of dropped frames due to ALE VID Ingress

Return to Summary Table

Offset = 1A094h + (j * 200h); where j = 0 to 2d

Table 14-27531. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0094h + formula**

Figure 14-9128. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27533. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

14.9.3.1.2.271 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register (Offset = 98h + formula) [reset = 0h]

Total number of dropped frames due to DA=SA

Return to Summary Table

Offset = 1A098h + (j * 200h); where j = 0 to 2d

Table 14-27534. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0098h + formula**

Figure 14-9129. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27536. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

14.9.3.1.2.272 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register (Offset = 9Ch + formula) [reset = 0h]

Total number of dropped frames due to ALE Block Mode

Return to Summary Table

Offset = 1A09Ch + (j * 200h); where j = 0 to 2d

Table 14-27537. Instance Table

Instance Name	Physical Address
CPSW0	**0800 009Ch + formula**

Figure 14-9130. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27539. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

14.9.3.1.2.273 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register (Offset = A0h + formula) [reset = 0h]

Total number of dropped frames due to ALE Secure Mode

Return to Summary Table

Offset = 1A0A0h + (j * 200h); where j = 0 to 2d

Table 14-27540. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00A0h + formula**

Figure 14-9131. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27542. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

14.9.3.1.2.274 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register (Offset = A4h + formula) [reset = 0h]

Total number of dropped frames due to ALE Authentication

Return to Summary Table

Offset = 1A0A4h + (j * 200h); where j = 0 to 2d

Table 14-27543. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00A4h + formula**

Figure 14-9132. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27545. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

14.9.3.1.2.275 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register (Offset = A8h + formula) [reset = 0h]

ALE Receive Unknown Unicast

Return to Summary Table

Offset = 1A0A8h + (j * 200h); where j = 0 to 2d

Table 14-27546. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00A8h + formula**

Figure 14-9133. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27548. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast

14.9.3.1.2.276 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register (Offset = ACh + formula) [reset = 0h]

ALE Receive Unknown Unicast Bytecount

Return to Summary Table

Offset = 1A0ACh + (j * 200h); where j = 0 to 2d

Table 14-27549. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00ACh + formula**

Figure 14-9134. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27551. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

14.9.3.1.2.277 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register (Offset = B0h + formula) [reset = 0h]

ALE Receive Unknown Multicast

Return to Summary Table

Offset = 1A0B0h + (j * 200h); where j = 0 to 2d

Table 14-27552. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00B0h + formula**

Figure 14-9135. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27554. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast

14.9.3.1.2.278 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register (Offset = B4h + formula) [reset = 0h]

ALE Receive Unknown Multicast Bytecount

Return to Summary Table

Offset = 1A0B4h + (j * 200h); where j = 0 to 2d

Table 14-27555. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00B4h + formula**

Figure 14-9136. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27557. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

14.9.3.1.2.279 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register (Offset = B8h + formula) [reset = 0h]

ALE Receive Unknown Broadcast

Return to Summary Table

Offset = 1A0B8h + (j * 200h); where j = 0 to 2d

Table 14-27558. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00B8h + formula**

Figure 14-9137. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27560. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

14.9.3.1.2.280 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register (Offset = BCh + formula) [reset = 0h]

ALE Receive Unknown Broadcast Bytecount

Return to Summary Table

Offset = 1A0BCh + (j * 200h); where j = 0 to 2d

Table 14-27561. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00BCh + formula**

Figure 14-9138. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27563. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

14.9.3.1.2.281 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register (Offset = C0h + formula) [reset = 0h]

ALE Policer Matched

Return to Summary Table

Offset = 1A0C0h + (j * 200h); where j = 0 to 2d

Table 14-27564. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00C0h + formula**

Figure 14-9139. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27566. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched

14.9.3.1.2.282 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register (Offset = C4h + formula) [reset = 0h]

ALE Policer Matched and Condition Red

Return to Summary Table

Offset = 1A0C4h + (j * 200h); where j = 0 to 2d

Table 14-27567. Instance Table

Instance Name	Physical Address
CPSW0	0800 00C4h + formula

Figure 14-9140. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27569. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

14.9.3.1.2.283 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register (Offset = C8h + formula) [reset = 0h]

ALE Policer Matched and Condition Yellow

Return to Summary Table

Offset = 1A0C8h + (j * 200h); where j = 0 to 2d

Table 14-27570. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00C8h + formula**

Figure 14-9141. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27572. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

14.9.3.1.2.284 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register (Offset = CCh + formula) [reset = 0h]

ALE Multicast Source Address Drop

Return to Summary Table

Offset = 1A0CCh + (j * 200h); where j = 0 to 2d

Table 14-27573. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00CCh + formula**

Figure 14-9142. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-27575. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Multicast Source Address drop

14.9.3.1.2.285 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register (Offset = D0h + formula) [reset = 0h]

ALE Dual VLAN Drop

Return to Summary Table

Offset = 1A0D0h + (j * 200h); where j = 0 to 2d

Table 14-27576. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00D0h + formula**

Figure 14-9143. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27578. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Dual VLAN drop

14.9.3.1.2.286 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register (Offset = D4h + formula) [reset = 0h]

ALE Length Error Drop

Return to Summary Table

Offset = 1A0D4h + (j * 200h); where j = 0 to 2d

Table 14-27579. Instance Table

Instance Name	Physical Address
CPSW0	0800 00D4h + formula

Figure 14-9144. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27581. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Length Error drop

14.9.3.1.2.287 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register (Offset = D8h + formula) [reset = 0h]

ALE IP Next Header Drop

Return to Summary Table

Offset = 1A0D8h + (j * 200h); where j = 0 to 2d

Table 14-27582. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00D8h + formula**

Figure 14-9145. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27584. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Next Header drop

14.9.3.1.2.288 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register (Offset = DCh + formula) [reset = 0h]

ALE IPV4 Frag Drop

Return to Summary Table

Offset = 1A0DCh + (j * 200h); where j = 0 to 2d

Table 14-27585. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00DCh + formula**

Figure 14-9146. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27587. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE IPV4 Fragment drop

14.9.3.1.2.289 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register (Offset = 140h + formula) [reset = 0h]

IET Receive Assembly Error

Return to Summary Table

Offset = 1A140h + (j * 200h); where j = 0 to 2d

Table 14-27588. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0140h + formula**

Figure 14-9147. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							

Table 14-27590. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_ERROR	R/W	0h	IET Receive Assembly Error

14.9.3.1.2.290 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register (Offset = 144h + formula) [reset = 0h]

IET Receive Assembly Ok

Return to Summary Table

Offset = 1A144h + (j * 200h); where j = 0 to 2d

Table 14-27591. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0144h + formula**

Figure 14-9148. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_ASSEMBLY_OK							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IET_RX_ASSEMBLY_OK							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IET_RX_ASSEMBLY_OK							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IET_RX_ASSEMBLY_OK							
R/W							
0h							

Table 14-27593. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok

14.9.3.1.2.291 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register (Offset = 148h + formula) [reset = 0h]

IET Receive Smd Error

Return to Summary Table

Offset = 1A148h + (j * 200h); where j = 0 to 2d

Table 14-27594. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0148h + formula**

Figure 14-9149. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27596. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error

14.9.3.1.2.292 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register (Offset = 14Ch + formula) [reset = 0h]

IET Receive Frag

Return to Summary Table

Offset = 1A14Ch + (j * 200h); where j = 0 to 2d

Table 14-27597. Instance Table

Instance Name	Physical Address
CPSW0	0800 014Ch + formula

Figure 14-9150. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_FRAG							
R/W							
0h							

Table 14-27599. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_FRAG	R/W	0h	IET Receive Frag

14.9.3.1.2.293 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register (Offset = 150h + formula) [reset = 0h]

IET Transmit Hold

Return to Summary Table

Offset = 1A150h + (j * 200h); where j = 0 to 2d

Table 14-27600. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0150h + formula**

Figure 14-9151. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_HOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_HOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_HOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_HOLD							
R/W							
0h							

Table 14-27602. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_HOLD	R/W	0h	IET Transmit Hold

14.9.3.1.2.294 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register (Offset = 154h + formula) [reset = 0h]

IET Transmit Frag

Return to Summary Table

Offset = 1A154h + (j * 200h); where j = 0 to 2d

Table 14-27603. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0154h + formula**

Figure 14-9152. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_FRAG							
R/W							
0h							

Table 14-27605. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_FRAG	R/W	0h	IET Transmit Frag

14.9.3.1.2.295 CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register (Offset = 17Ch + formula) [reset = 0h]

Transmit Memory Protect CRC Error

Return to Summary Table

Offset = 1A17Ch + (j * 200h); where j = 0 to 2d

Table 14-27606. Instance Table

Instance Name	Physical Address
CPSW0	**0800 017Ch + formula**

Figure 14-9153. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-27608. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

14.9.3.1.2.296 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register (Offset = 180h + formula) [reset = 0h]

ENET Port n PRIORITY N Packet Count

Return to Summary Table

Offset = 1A180h + (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

Table 14-27609. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0180h + formula**

Figure 14-9154. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN							
R/W							
0h							

Table 14-27611. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

14.9.3.1.2.297 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register (Offset = 1A0h + formula) [reset = 0h]

ENET Port n PRIORITY N Packet Byte Count

Return to Summary Table

Offset = 1A1A0h + (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

Table 14-27612. Instance Table

Instance Name	Physical Address
CPSW0	**0800 01A0h + formula**

Figure 14-9155. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT							
R/W							
0h							

Table 14-27614. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

14.9.3.1.2.298 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register (Offset = 1C0h + formula) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Count

Return to Summary Table

Offset = 1A1C0h + (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

Table 14-27615. Instance Table

Instance Name	Physical Address
CPSW0	**0800 01C0h + formula**

Figure 14-9156. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP							
R/W							
0h							

Table 14-27617. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

14.9.3.1.2.299 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register

1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register (Offset = 1E0h + formula) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Byte Count

Return to Summary Table

Offset = 1A1E0h + (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

Table 14-27618. Instance Table

Instance Name	Physical Address
CPSW0	**0800 01E0h + formula**

Figure 14-9157. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							

Table 14-27620. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

14.9.3.1.2.300 CPSW3_CPSW_NU_CPTS_IDVER_REG Register

1 CPSW3_CPSW_NU_CPTS_IDVER_REG Register (Offset = 0h) [reset = 4E8A010Ch]

Identification and Version Register

Return to Summary Table

Table 14-27621. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-9158. CPSW3_CPSW_NU_CPTS_IDVER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Ch</td></tr>
</table>

Table 14-27623. CPSW3_CPSW_NU_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Ch	Minor version value

14.9.3.1.2.301 CPSW3_CPSW_NU_CPTS_CONTROL_REG Register

1 CPSW3_CPSW_NU_CPTS_CONTROL_REG Register (Offset = 4h) [reset = 4h]

Time Sync Control Register

Return to Summary Table

Table 14-27624. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-9159. CPSW3_CPSW_NU_CPTS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W				NONE			
0h				0h			

23	22	21	20	19	18	17	16
RESERVED						TS_GENF_CLR_EN	TS_RX_NO_EVENT
NONE						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h

Table 14-27626. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output time stamp counter bit select. 0h TS_SYNC disabled. 1h-Fh TS_SYNC is time stamp counter bits 31 (Fh) down to 17 (1h).
27:18	RESERVED	NONE	0h	Reserved
17	TS_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable. 0h A CPTS_GENFn output is not cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero. 1h A CPTS_GENFn output is cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events. 0h Ethernet receive timesync events enabled. 1h Ethernet receive timesync events disabled.
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable.
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable.
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable.
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable.

Table 14-27626. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable.
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable.
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable.
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable.
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction. 0h Increase the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) by the PPM value. 1h Decrease the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG and) by the PPM value.
6	TS_COMP_TOG	R/W	0h	Time Stamp Compare Toggle mode. 0h TS_COMP is in non-toggle mode. 1h TS_COMP is in toggle mode.
5	MODE	R/W	0h	64-Bit Mode. 0h The time stamp is 32-bits with the upper 32-bits forced to zero. 1h The time stamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable. 0h The time stamp value increments with the selected RFTCLK 1h The time stamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Time Stamp Enable. 0h Time stamps are disabled on received packets to host. 1h Time stamps enabled on received packets to host (PCIE_CPTS_CONTROL_REG[0] CPTS_EN must be set).
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity. 0h TS_COMP is asserted low. 1h TS_COMP is asserted high.
1	INT_TEST	R/W	0h	Interrupt Test. When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset.

14.9.3.1.2.302 CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register

1 CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = 0h]

RFTCLK Select Register

Return to Summary Table

Table 14-27627. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-9160. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RFTCLK_SEL				
NONE			R/W				
0h			0h				

Table 14-27629. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

4:0	RFTCLK_SEL	R/W	0h	Reference clock select.
				This bit field is used to control an external multiplexer that selects one out of 8 clocks for time sync reference.
				`0h Selects CPSWHSDIV_CLKOUT2 clock`
				`1h Selects MAINHSDIV_CLKOUT3 clock`
				`2h Selects MCU_CPTS0_RFT_CLK I/O pin`
				`3h Selects CPTS0_RFT_CLK I/O pin`
				`4h Selects MCU_EXT_REFCLK0 I/O pin`
				`5h Selects EXT_REFCLK1 I/O pin`
				`6h Selects PCIE0_TXI0_CLK clock`
				`7h Selects PCIE1_TXI0_CLK clock The RFTCLK_SEL value can be written only when the [0] CPTS_EN and [3] TSTAMP_EN bits are cleared to zero in the CPSW_CPTS_CONTROL_REG register.`

14.9.3.1.2.303 CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register (Offset = Ch) [reset = 0h]

Time Stamp Event Push Register

Return to Summary Table

Table 14-27630. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch**

Figure 14-9161. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
NONE							W
0h							0h

Table 14-27632. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PUSH	W	0h	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

14.9.3.1.2.304 CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]

Time Stamp Load Low Value Register

Return to Summary Table

Table 14-27633. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-9162. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-27635. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

14.9.3.1.2.305 CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = 0h]

Time Stamp Load Enable Register

Return to Summary Table

Table 14-27636. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-9163. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
NONE							W
0h							0h

Table 14-27638. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_LOAD_EN	W	0h	Time Stamp Load Enable. Writing a one to this bit enables the time stamp value to be written with the value in CPSW_CPTS_TS_LOAD_VAL_REG/ CPSW_CPTS_TS_LOAD_HIGH_VAL_REG. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the time stamp (CPSW_CPTS_TS_LOAD_HIGH_VAL_REG) are forced to zero in 32-bit mode.

14.9.3.1.2.306 CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register (Offset = 18h) [reset = 0h]

Time Stamp Comparison Low Value Register

Return to Summary Table

Table 14-27639. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h**

Figure 14-9164. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_VAL							
R/W							
0h							

Table 14-27641. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL.

14.9.3.1.2.307 CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

Time Stamp Comparison Length Register

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Table 14-27642. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-9165. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27644. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length. Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the CPSW_GENF_COMP_LOW_REG_L[31-0] COMP_LOW and CPSW_GENF_COMP_HIGH_REG_L[31-0] COMP_HIGH registers are written.

14.9.3.1.2.308 CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register

1 CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = 0h]

Interrupt Status Register Raw

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Table 14-27645. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0020h**

Figure 14-9166. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
NONE							R/W
0h							0h

Table 14-27647. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when CPSW_CPTS_CONTROL_REG[1] INT_TEST = 1h A one in this bit indicates that there are one or more events in the event FIFO.

14.9.3.1.2.309 CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register

1 CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = 0h]

Interrupt Status Register Masked

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Table 14-27648. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0024h**

Figure 14-9167. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
NONE							R
0h							0h

Table 14-27650. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

14.9.3.1.2.310 CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register

1 CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register (Offset = 28h) [reset = 0h]

Interrupt Enable Register

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Table 14-27651. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0028h**

Figure 14-9168. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
NONE							R/W
0h							0h

Table 14-27653. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

14.9.3.1.2.311 CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = 0h]

Time Stamp Comparison Nudge Register

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Table 14-27654. Instance Table

Instance Name	Physical Address
CPSW0	**0800 002Ch**

Figure 14-9169. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-27656. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time stamp Comparison Nudge Value. This two's complement number is added to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value to increase or decrease the TS_COMP length by the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred.

14.9.3.1.2.312 CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register

1 CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register (Offset = 30h) [reset = 0h]

Event Pop Register

Return to Summary Table

Table 14-27657. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0030h**

Figure 14-9170. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
NONE							W
0h							0h

Table 14-27659. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EVENT_POP	W	0h	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the CPSW_CPTS_EVENT_0_REG to CPSW_CPTS_EVENT_3_REG registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

14.9.3.1.2.313 CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register

1 CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

Event 0 Register

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Table 14-27660. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-9171. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-27662. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp is valid for transmit, receive, and time stamp push event types. The time stamp value is not valid for counter roll event types.

14.9.3.1.2.314 CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register

1 CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register (Offset = 38h) [reset = 0h]

Event 1 Register

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Table 14-27663. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-9172. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
NONE		R	R				
0h		0h	0h				

23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R				R			
0h				0h			

15	14	13	12	11	10	9	8
SEQUENCE_ID							
R							
0h							

7	6	5	4	3	2	1	0
SEQUENCE_ID							
R							
0h							

Table 14-27665. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28:24	PORT_NUMBER	R	0h	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware time stamp number.
23:20	EVENT_TYPE	R	0h	Time Sync Event Type 0h Time Stamp Push Event 1h Time Stamp Rollover Event 2h Time Stamp Half Rollover Event 3h Hardware Time Stamp Push Event 4h Ethernet Receive Event 5h Ethernet Transmit Event 6h Time Stamp Compare Event 7h Host Transmit Event 8h-Fh Reserved
19:16	MESSAGE_TYPE	R	0h	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

Table 14-27665. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SEQUENCE_ID	R	0h	Sequence ID. The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.9.3.1.2.315 CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register

1 CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register (Offset = 3Ch) [reset = 0h]

Event 2 Register

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Table 14-27666. Instance Table

Instance Name	Physical Address
CPSW0	**0800 003Ch**

Figure 14-9173. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DOMAIN</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27668. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DOMAIN	R	0h	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.9.3.1.2.316 CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register

1 CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

Event 3 Register

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Table 14-27669. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h**

Figure 14-9174. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TIME_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TIME_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TIME_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIME_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27671. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

14.9.3.1.2.317 CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

Time Stamp Load High Value Register

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Table 14-27672. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0044h**

Figure 14-9175. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							

23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							

15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							

7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-27674. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time Stamp Load high Value. Writing the CPSW_CPTS_TS_LOAD_EN_REG[0] TS_LOAD_EN bit causes the value contained in this register to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode

14.9.3.1.2.318 CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

Time Stamp Comparison High Value Register

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Table 14-27675. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0048h**

Figure 14-9176. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_HIGH_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_HIGH_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL							
R/W							
0h							

Table 14-27677. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time Stamp Comparison High Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the [31-0]TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and CPSW_CPTS_TS_COMP_HIGH_VAL_REG[31-0] TS_COMP_HIGH_VAL. This value is unused in 32-bit mode. The upper 32-bits in CPSW_CPTS_TS_COMP_HIGH_VAL_REG register should be written before the lower 32-bits in the CPSW_CPTS_TS_COMP_VAL_REG register.

14.9.3.1.2.319 CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = 0h]

TS Add Value Register

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Table 14-27678. Instance Table

Instance Name	Physical Address
CPSW0	**0800 004Ch**

Figure 14-9177. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADD_VAL		
NONE					R/W		
0h					0h		

Table 14-27680. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADD_VAL	R/W	0h	The ts_add_value[2:0] is added to 1 to comprise the time stamp increment value. The time stamp increment value is added to the current time stamp (time_stamp[63:0]) on each RCLK. The time stamp increment value can be adjusted by nudge and ppm also. The CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value may be non-zero in 64-bit mode only.

14.9.3.1.2.320 CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

Time Stamp PPM Low Value Register

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Table 14-27681. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0050h**

Figure 14-9178. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_PPM_LOW_VAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_PPM_LOW_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_PPM_LOW_VAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_PPM_LOW_VAL							
R/W							
0h							

Table 14-27683. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

14.9.3.1.2.321 CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = 0h]

Time Stamp PPM High Value Register

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Table 14-27684. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0054h**

Figure 14-9179. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TS_PPM_HIGH_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TS_PPM_HIGH_VAL							
R/W							
0h							

Table 14-27686. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value. This value should be written first (before the low value is written). The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.9.3.1.2.322 CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register

1 CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = 0h]

Time Stamp Nudge Value Register

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Table 14-27687. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0058h**

Figure 14-9180. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TS_NUDGE_VAL							
R/W							
0h							

Table 14-27689. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge Value. This two's complement number is added to the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[[31-0] TIME_STAMP value to increase or decrease the time stamp value by the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL amount. The TS_NUDGE_VAL value is cleared to zero when the nudge has occurred. The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.9.3.1.2.323 CPSW3_CPSW_NU_CPTS_TS_CONFIG Register

1 CPSW3_CPSW_NU_CPTS_TS_CONFIG Register (Offset = D0h) [reset = 2002h]

Time Stamp Configuration Read

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Table 14-27690. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00D0h**

Figure 14-9181. CPSW3_CPSW_NU_CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVNT_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
NUM_GENF							
R							
2h							

Table 14-27692. CPSW3_CPSW_NU_CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	The Event FIFO Depth
7:0	NUM_GENF	R	2h	The number of CPTS GENF outputs

14.9.3.1.2.324 CPSW3_CPSW_NU_ALE_MOD_VER Register

1 CPSW3_CPSW_NU_ALE_MOD_VER Register (Offset = 0h) [reset = 290105h]

The Module and Version Register identifies the module identifier and revision of the ALE_3g512ie module.

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Table 14-27693. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h**

Figure 14-9182. CPSW3_CPSW_NU_ALE_MOD_VER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">29h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">29h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VERSION</td><td colspan="3">MAJOR_REVISION</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM_REVISION</td><td colspan="6">MINOR_REVISION</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">5h</td></tr>
</table>

Table 14-27695. CPSW3_CPSW_NU_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	29h	ALE_3g512ie module ID.
15:11	RTL_VERSION	R	0h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	5h	Minor Revision.

14.9.3.1.2.325 CPSW3_CPSW_NU_ALE_ALE_STATUS Register

1 CPSW3_CPSW_NU_ALE_ALE_STATUS Register (Offset = 4h) [reset = 80000400h]

The ALE status provides information on the ALE configuration and state. The ~iramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry hi is designated by the odd slice index and lo is designated by the even slice index. The slice index is above the ram depth like {SlixeIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

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Table 14-27696. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h**

Figure 14-9183. CPSW3_CPSW_NU_ALE_ALE_STATUS Name Register

31	30	29	28	27	26	25	24
UREGANDREGMSK12	UREGANDREGMSK08	RESERVED					
R	R	NONE					
1h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
POLCNTDIV8							
R							
4h							
7	6	5	4	3	2	1	0
RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R	R	NONE	R				
0h	0h	0h	0h				

Table 14-27698. CPSW3_CPSW_NU_ALE_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29:16	RESERVED	NONE	0h	Reserved
15:8	POLCNTDIV8	R	4h	This is the number of Classifiers the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	NONE	0h	Reserved

Table 14-27698. CPSW3_CPSW_NU_ALE_ALE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

14.9.3.1.2.326 CPSW3_CPSW_NU_ALE_ALE_CONTROL Register

1 CPSW3_CPSW_NU_ALE_ALE_CONTROL Register (Offset = 8h) [reset = 0h]

The ALE Control Register is used to set the ALE modes used for all ports.

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Table 14-27699. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h**

Figure 14-9184. CPSW3_CPSW_NU_ALE_ALE_CONTROL Name Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	22	21	20	19	18	17	16
UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W			NONE			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27701. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28:26	RESERVED	NONE	0h	Reserved

Table 14-27701. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the ~imirror_top port.
23:21	UPD_BW_CTRL	R/W	0h	The ~iupd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the ~iupd_bw_ctrl can be programmed more aggressive. If the ~iupd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
20:18	RESERVED	NONE	0h	Reserved
17:16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when ~ien_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ~ipX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the ~imirror_top port.
9	RESERVED	NONE	0h	Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.

Table 14-27701. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

14.9.3.1.2.327 CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register

1 CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register (Offset = Ch) [reset = 0h]

The ALE Control 2 Register is used to set the extended features used for all ports.

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Table 14-27702. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 000Ch**

Figure 14-9185. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MULTIHOST	RESERVED						MIRROR_MIDX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIRROR_MIDX							
R/W							
0h							

Table 14-27704. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	NONE	0h	Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
26	RESERVED	NONE	0h	Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.

Table 14-27704. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ~iALE_NXT_HDR register values.
19	RESERVED	NONE	0h	Reserved
18:16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the ~itrk_en_dst, ~itrk_en_src, ~itrk_en_pri and ~itrk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the ~iitalic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - ~i00000000 2 - ~i01010101 3 - ~i02102102 4 - ~i03210321
15	MULTIHOST	R/W	0h	The ~multihost allows host traffic to be sent bact to the host if the DA is market for the host port.
14:9	RESERVED	NONE	0h	Reserved
8:0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the ~imirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

14.9.3.1.2.328 CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register

1 CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register (Offset = 10h) [reset = 0h]

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

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Table 14-27705. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h**

Figure 14-9186. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				ALE_PRESCALE			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
ALE_PRESCALE							
R/W							
0h							

7	6	5	4	3	2	1	0
ALE_PRESCALE							
R/W							
0h							

Table 14-27707. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

14.9.3.1.2.329 CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register

1 CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register (Offset = 14h) [reset = 0h]

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

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Table 14-27708. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h**

Figure 14-9187. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALE_AGING_TIMER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ALE_AGING_TIMER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALE_AGING_TIMER							
R/W							
0h							

Table 14-27710. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29:24	RESERVED	NONE	0h	Reserved
23:0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

14.9.3.1.2.330 CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register

1 CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register (Offset = 1Ch) [reset = 0h]

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip_nxt_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

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Table 14-27711. Instance Table

Instance Name	Physical Address
CPSW0	**0800 001Ch**

Figure 14-9188. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24
IP_NXT_HDR3							
R/W							
0h							
23	22	21	20	19	18	17	16
IP_NXT_HDR2							
R/W							
0h							
15	14	13	12	11	10	9	8
IP_NXT_HDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
IP_NXT_HDR0							
R/W							
0h							

Table 14-27713. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IP_NXT_HDR3	R/W	0h	The ~iip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23:16	IP_NXT_HDR2	R/W	0h	The ~iip_nxt_hdr2 is the third protocol or next header compared when enabled.
15:8	IP_NXT_HDR1	R/W	0h	The ~iip_nxt_hdr1 is the second protocol or next header compared when enabled.
7:0	IP_NXT_HDR0	R/W	0h	The ~iip_nxt_hdr0 is the first protocol or next header compared when enabled.

14.9.3.1.2.331 CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register

1 CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register (Offset = 20h) [reset = 0h]

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

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Table 14-27714. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0020h**

Figure 14-9189. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>TABLEWR</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TABLEIDX</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TABLEIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27716. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the ~b TABLEIDX entry will be read into the ~b ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ~b ALE_TBLWx registers and write them to the table at the specified ~b TABLEIDX.
30:9	RESERVED	NONE	0h	Reserved
8:0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

14.9.3.1.2.332 CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register

1 CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register (Offset = 34h) [reset = 0h]

The ALE Table Word 2 is the most significant word of an ALE table entry.

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Table 14-27717. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0034h**

Figure 14-9190. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TABLEWRD2						
NONE	R/W						
0h	0h						

Table 14-27719. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	TABLEWRD2	R/W	0h	Table Entry bits [70:64]

14.9.3.1.2.333 CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register

1 CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register (Offset = 38h) [reset = 0h]

The ALE Table Word 1 is the middle word of an ALE table entry.

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Table 14-27720. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0038h**

Figure 14-9191. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24
TABLEWRD1							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD1							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD1							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD1							
R/W							
0h							

Table 14-27722. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

14.9.3.1.2.334 CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register

1 CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register (Offset = 3Ch) [reset = 0h]

The ALE Table Word 0 is the least significant word of an ALE table entry.

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Table 14-27723. Instance Table

Instance Name	Physical Address
CPSW0	**0800 003Ch**

Figure 14-9192. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Name Register

31	30	29	28	27	26	25	24
TABLEWRD0							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD0							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD0							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD0							
R/W							
0h							

Table 14-27725. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

14.9.3.1.2.335 CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register

1 CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register (Offset = 40h + formula) [reset = 0h]

The ALE Port Control Register sets the port specific modes of operation.

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Offset = 1E040h + (j * 4h); where j = 0 to 2d

Table 14-27726. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0040h + formula**

Figure 14-9193. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">I0_REG_P0_BCAST_LIMIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">I0_REG_P0_MCAST_LIMIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>I0_REG_P0_DROP_DOUBLE_VLAN</td><td>I0_REG_P0_DROP_DUAL_VLAN</td><td>I0_REG_P0_MACONLY_CAF</td><td>I0_REG_P0_DIS_PAUTHMOD</td><td>I0_REG_P0_MACONLY</td><td>I0_REG_P0_TRUNKEN</td><td colspan="2">I0_REG_P0_TRUNKNUM</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>I0_REG_P0_MIRROR_SP</td><td>RESERVED</td><td>I0_REG_P0_NO_SA_UPDATE</td><td>I0_REG_P0_NO_LEARN</td><td>I0_REG_P0_VID_INGRESS_CHECK</td><td>I0_REG_P0_DROP_UN_TAGGED</td><td colspan="2">I0_REG_P0_PORTSTATE</td></tr>
<tr><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-27728. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23:16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The Iy_REG_Py_MCAST_LIMIT bit field is the number of Multicast packets that will be forwarded per CPSW_ALE_PRESCALE time.
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN. When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.

Table 14-27728. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames. When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with Iy_REG_Py_MACONLY set.
12	I0_REG_P0_DIS_PAUTHMOD	R/W	0h	Disable Port authorization. When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only. When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the Iy_REG_Py_MACONLY bit set and the Iy_REG_Py_NO_LEARN also set. If Iy_REG_Py_MACONLY bit is set and the Iy_REG_Py_NO_LEARN is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable. This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the Iy_REG_Py_TRUNKEN its set and having the same Iy_REG_Py_TRUNKNUM will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9:8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number. This field is used as the trunk number when the Iy_REG_Py_TRUNKEN is also set. Ports with the same trunk number that have the Iy_REG_Py_TRUNKEN also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port. This field enables the source port mirror option. When this bit is set any traffic received on the port with the Iy_REG_Py_MIRROR_SP bit set will have its received traffic also sent to the MIRROR_TOP port.
6	RESERVED	NONE	0h	Reserved
5	I0_REG_P0_NO_SA_UPDATE	R/W	0h	No Source Address Update. When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn. When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRESS_CHECK	R/W	0h	VLAN Ingress Check. When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UNTAGGED	R/W	0h	If Drop Untagged. When set will drop packets without a VLAN tag.
1:0	I0_REG_P0_PORTSTATE	R/W	0h	Port State. Defines the current port state used for lookup operations. 0h Disabled 1h Blocked 2h Learning 3h Forwarding

14.9.3.1.2.336 CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register

1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register (Offset = 90h) [reset = 0h]

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

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Table 14-27729. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0090h**

Figure 14-9194. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_MEMBER_LIST		
NONE					R/W		
0h					0h		

Table 14-27731. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

14.9.3.1.2.337 CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register

1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register (Offset = 94h) [reset = 0h]

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

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Table 14-27732. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0094h**

Figure 14-9195. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 14-27734. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

14.9.3.1.2.338 CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register

1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register (Offset = 98h) [reset = 0h]

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

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Table 14-27735. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0098h**

Figure 14-9196. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_REG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 14-27737. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

14.9.3.1.2.339 CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register

1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register (Offset = 9Ch) [reset = 0h]

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

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Table 14-27738. Instance Table

Instance Name	Physical Address
CPSW0	**0800 009Ch**

Figure 14-9197. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_FORCE_UNTAGGED_EGRESS		
NONE					R/W		
0h					0h		

Table 14-27740. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

14.9.3.1.2.340 CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register

1 CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register (Offset = B4h) [reset = 0h]

The Fast LUT registers allows the ports to be placed in Fast LUT mode.

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Table 14-27741. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00B4h**

Figure 14-9198. CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">FAST_LUT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-27743. CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FAST_LUT	R/W	0h	The ~Fast_LUT field alows any port to be Fast_LUT mode, which will cause all lookup operations to start based on DA/SA and VLAN only. That is any data beyong the first 32 are not used in the lookup process.

14.9.3.1.2.341 CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register

1 CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register (Offset = B8h) [reset = 0h]

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostice only.

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Table 14-27744. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00B8h**

Figure 14-9199. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PBCAST_DIAG	RESERVED					PORT_DIAG	
R/W	NONE					R/W	
0h	0h					0h	
7	6	5	4	3	2	1	0
RESERVED				STAT_DIAG			
NONE				R/W			
0h				0h			

Table 14-27746. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PBCAST_DIAG	R/W	0h	When set and the ~iport_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
14:10	RESERVED	NONE	0h	Reserved
9:8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7:4	RESERVED	NONE	0h	Reserved

Table 14-27746. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count.

14.9.3.1.2.342 CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register

1 CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register (Offset = BCh) [reset = 0h]

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

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Table 14-27747. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00BCh**

Figure 14-9200. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OAM_LB_CTRL		
NONE					R/W		
0h					0h		

Table 14-27749. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OAM_LB_CTRL	R/W	0h	The ~ioam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

14.9.3.1.2.343 CPSW3_CPSW_NU_ALE_EGRESSOP Register

1 CPSW3_CPSW_NU_ALE_EGRESSOP Register (Offset = FCh) [reset = 0h]

The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a clasifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

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Table 14-27750. Instance Table

Instance Name	Physical Address
CPSW0	**0800 00FCh**

Figure 14-9201. CPSW3_CPSW_NU_ALE_EGRESSOP Name Register

31	30	29	28	27	26	25	24
EGRESS_OP							
R/W							
0h							
23	22	21	20	19	18	17	16
EGRESS_TRK			TTL_CHECK	RESERVED			
R/W			R/W	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DEST_PORTS		
NONE					R/W		
0h					0h		

Table 14-27752. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23:21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19:3	RESERVED	NONE	0h	Reserved

Table 14-27752. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

14.9.3.1.2.344 CPSW3_CPSW_NU_ALE_POLICECFG0 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG0 Register (Offset = 100h) [reset = 0h]

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

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Table 14-27753. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0100h**

Figure 14-9202. CPSW3_CPSW_NU_ALE_POLICECFG0 Name Register

31	30	29	28	27	26	25	24
PORT_MEN	TRUNKID	RESERVED			PORT_NUM		RESERVED
R/W	R/W	NONE			R/W		NONE
0h	0h	0h			0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PRI_MEN	PRI_VAL		
NONE				R/W	R/W		
0h				0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ONU_MEN	RESERVED						ONU_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ONU_INDEX							
R/W							
0h							

Table 14-27755. CPSW3_CPSW_NU_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/ classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
29:27	RESERVED	NONE	0h	Reserved
26:25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
24:20	RESERVED	NONE	0h	Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18:16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

14.9.3.1.2.345 CPSW3_CPSW_NU_ALE_POLICECFG1 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG1 Register (Offset = 104h) [reset = 0h]

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

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Table 14-27756. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0104h**

Figure 14-9203. CPSW3_CPSW_NU_ALE_POLICECFG1 Name Register

31	30	29	28	27	26	25	24
DST_MEN	RESERVED						DST_INDEX
R/W	NONE						R/W
0h	0h						0h
23	22	21	20	19	18	17	16
DST_INDEX							
R/W							
0h							
15	14	13	12	11	10	9	8
SRC_MEN	RESERVED						SRC_INDEX
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
SRC_INDEX							
R/W							
0h							

Table 14-27758. CPSW3_CPSW_NU_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

14.9.3.1.2.346 CPSW3_CPSW_NU_ALE_POLICECFG2 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG2 Register (Offset = 108h) [reset = 0h]

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

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Table 14-27759. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0108h**

Figure 14-9204. CPSW3_CPSW_NU_ALE_POLICECFG2 Name Register

31	30	29	28	27	26	25	24
OVLAN_MEN	RESERVED						OVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
23	22	21	20	19	18	17	16
OVLAN_INDEX							
R/W							
0h							
15	14	13	12	11	10	9	8
IVLAN_MEN	RESERVED						IVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
IVLAN_INDEX							
R/W							
0h							

Table 14-27761. CPSW3_CPSW_NU_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

14.9.3.1.2.347 CPSW3_CPSW_NU_ALE_POLICECFG3 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG3 Register (Offset = 10Ch) [reset = 0h]

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

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Table 14-27762. Instance Table

Instance Name	Physical Address
CPSW0	**0800 010Ch**

Figure 14-9205. CPSW3_CPSW_NU_ALE_POLICECFG3 Name Register

31	30	29	28	27	26	25	24
ETHERTYPE_MEN	RESERVED						ETHERTYPE_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ETHERTYPE_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPSRC_MEN	RESERVED						IPSRC_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPSRC_INDEX							
R/W							
0h							

Table 14-27764. CPSW3_CPSW_NU_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

14.9.3.1.2.348 CPSW3_CPSW_NU_ALE_POLICECFG4 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG4 Register (Offset = 110h) [reset = 0h]

The Policing Config 4 holds the match enable/match index for the IP Destination address

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Table 14-27765. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0110h**

Figure 14-9206. CPSW3_CPSW_NU_ALE_POLICECFG4 Name Register

31	30	29	28	27	26	25	24
IPDST_MEN	RESERVED						IPDST_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPDST_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-27767. CPSW3_CPSW_NU_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
15:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.349 CPSW3_CPSW_NU_ALE_POLICECFG6 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG6 Register (Offset = 118h) [reset = 0h]

The PIR counter is a 37 bit internal counter where ~ipir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir_idle_inc_val==0) Packet are marked RED or GREEN based on PIR counter only.

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Table 14-27768. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0118h**

Figure 14-9207. CPSW3_CPSW_NU_ALE_POLICECFG6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27770. CPSW3_CPSW_NU_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

14.9.3.1.2.350 CPSW3_CPSW_NU_ALE_POLICECFG7 Register

1 CPSW3_CPSW_NU_ALE_POLICECFG7 Register (Offset = 11Ch) [reset = 0h]

The CIR counter is a 37 bit internal counter where ~icir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir_idle_inc_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

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Table 14-27771. Instance Table

Instance Name	Physical Address
CPSW0	**0800 011Ch**

Figure 14-9208. CPSW3_CPSW_NU_ALE_POLICECFG7 Name Register

31	30	29	28	27	26	25	24
CIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL							
R/W							
0h							

Table 14-27773. CPSW3_CPSW_NU_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

14.9.3.1.2.351 CPSW3_CPSW_NU_ALE_POLICETBLCTL Register

1 CPSW3_CPSW_NU_ALE_POLICETBLCTL Register (Offset = 120h) [reset = 0h]

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

Return to Summary Table

Table 14-27774. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0120h**

Figure 14-9209. CPSW3_CPSW_NU_ALE_POLICETBLCTL Name Register

31	30	29	28	27	26	25	24
WRITE_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			POL_TBL_IDX				
NONE			R/W				
0h			0h				

Table 14-27776. CPSW3_CPSW_NU_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
30:5	RESERVED	NONE	0h	Reserved
4:0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

14.9.3.1.2.352 CPSW3_CPSW_NU_ALE_POLICECONTROL Register

1 CPSW3_CPSW_NU_ALE_POLICECONTROL Register (Offset = 124h) [reset = 0h]

The Control Enables color marking as well as internal ALE packet dropping rules.

Return to Summary Table

Table 14-27777. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0124h**

Figure 14-9210. CPSW3_CPSW_NU_ALE_POLICECONTROL Name Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W	NONE	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
23	22	21	20	19	18	17	16
POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W		R/W	R/W	NONE			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-27779. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	NONE	0h	Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the ~iyellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	NONE	0h	Reserved
26:24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the ~iyellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%

Table 14-27779. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
19:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.353 CPSW3_CPSW_NU_ALE_POLICETESTCTL Register

1 CPSW3_CPSW_NU_ALE_POLICETESTCTL Register (Offset = 128h) [reset = 0h]

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

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Table 14-27780. Instance Table

Instance Name	Physical Address
CPSW0	0800 0128h

Figure 14-9211. CPSW3_CPSW_NU_ALE_POLICETESTCTL Name Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			POL_TEST_IDX				
NONE			R/W				
0h			0h				

Table 14-27782. CPSW3_CPSW_NU_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/ classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27:5	RESERVED	NONE	0h	Reserved
4:0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

14.9.3.1.2.354 CPSW3_CPSW_NU_ALE_POLICEHSTAT Register

1 CPSW3_CPSW_NU_ALE_POLICEHSTAT Register (Offset = 12Ch) [reset = 0h]

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

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Table 14-27783. Instance Table

Instance Name	Physical Address
CPSW0	**0800 012Ch**

Figure 14-9212. CPSW3_CPSW_NU_ALE_POLICEHSTAT Name Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R	R	R	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-27785. CPSW3_CPSW_NU_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match.
28:0	RESERVED	NONE	0h	Reserved

14.9.3.1.2.355 CPSW3_CPSW_NU_ALE_THREADMAPDEF Register

1 CPSW3_CPSW_NU_ALE_THREADMAPDEF Register (Offset = 134h) [reset = 0h]

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

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Table 14-27786. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0134h**

Figure 14-9213. CPSW3_CPSW_NU_ALE_THREADMAPDEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DEFTHREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		DEFTHREADVAL					
NONE		R/W					
0h		0h					

Table 14-27788. CPSW3_CPSW_NU_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the ~idefthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
14:6	RESERVED	NONE	0h	Reserved
5:0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

14.9.3.1.2.356 CPSW3_CPSW_NU_ALE_THREADMAPCTL Register

1 CPSW3_CPSW_NU_ALE_THREADMAPCTL Register (Offset = 138h) [reset = 0h]

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

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Table 14-27789. Instance Table

Instance Name	**Physical Address**
CPSW0	**0800 0138h**

Figure 14-9214. CPSW3_CPSW_NU_ALE_THREADMAPCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CLASSINDEX				
NONE			R/W				
0h			0h				

Table 14-27791. CPSW3_CPSW_NU_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the ~bTHREADMAPVAL register.

14.9.3.1.2.357 CPSW3_CPSW_NU_ALE_THREADMAPVAL Register

1 CPSW3_CPSW_NU_ALE_THREADMAPVAL Register (Offset = 13Ch) [reset = 0h]

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

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Table 14-27792. Instance Table

Instance Name	Physical Address
CPSW0	**0800 013Ch**

Figure 14-9215. CPSW3_CPSW_NU_ALE_THREADMAPVAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>THREAD_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">THREADVAL</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-27794. CPSW3_CPSW_NU_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the ~ithreadval for the selected classifier match. If clear the the thread ID will be determined by the ~bTHREADMAPDEF register settings.
14:6	RESERVED	NONE	0h	Reserved
5:0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

14.9.3.1.2.358 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register (Offset = 0h + formula) [reset = 0h]

Time Stamp Generate Function Comparison Low Value

Return to Summary Table

Offset = E0h + (j * 20h); where j = 0 to 1d

Table 14-27795. Instance Table

Instance Name	Physical Address
CPSW0	0800 0000h + formula

Figure 14-9216. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-27797. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF_COMP_HIGH_REG_I and CPSW_GENF_COMP_LOW_REG_I should only be written when the CPSW_GENF_LENGTH_REG_I[31-0] LENGTH value is zero.

14.9.3.1.2.359 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register (Offset = 4h + formula) [reset = 0h]

Time Stamp Generate Function Comparison high Value

Return to Summary Table

Offset = E4h + (j * 20h); where j = 0 to 1d

Table 14-27798. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h + formula**

Figure 14-9217. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-27800. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits. The CPSW_GENF_COMP_HIGH_REG_I and CPSW_GENF_COMP_LOW_REG_I should only be written when the CPSW_GENF_LENGTH_REG_I[31-0] LENGTH value is zero.

14.9.3.1.2.360 CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register (Offset = 8h + formula) [reset = 0h]

Time Stamp Generate Function Control

Return to Summary Table

Offset = E8h + (j * 20h); where j = 0 to 1d

Table 14-27801. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h + formula**

Figure 14-9218. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-27803. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0h The output TS_GENFn signal asserts low 1h The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

14.9.3.1.2.361 CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register (Offset = Ch + formula) [reset = 0h]

Time Stamp Generate Function Length Value

Return to Summary Table

Offset = ECh + (j * 20h); where j = 0 to 1d

Table 14-27804. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch + formula**

Figure 14-9219. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-27806. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

14.9.3.1.2.362 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register (Offset = 10h + formula) [reset = 0h]

Time Stamp Generate Function PPM Low Value

Return to Summary Table

Offset = F0h + (j * 20h); where j = 0 to 1d

Table 14-27807. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h + formula**

Figure 14-9220. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-27809. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.9.3.1.2.363 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register (Offset = 14h + formula) [reset = 0h]

Time Stamp Generate Function PPM High Value

Return to Summary Table

Offset = F4h + (j * 20h); where j = 0 to 1d

Table 14-27810. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h + formula**

Figure 14-9221. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PPM_HIGH</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PPM_HIGH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27812. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value. This value should be written first (before the low value is written).

14.9.3.1.2.364 CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register (Offset = 18h + formula) [reset = 0h]

Time Stamp Generate Function Nudge Value

Return to Summary Table

Offset = F8h + (j * 20h); where j = 0 to 1d

Table 14-27813. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h + formula**

Figure 14-9222. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-27815. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF_NUDGE_REG_l[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF_NUDGE_REG_l value is cleared to zero when the nudge has occurred.

14.9.3.1.2.365 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register (Offset = 0h + formula) [reset = 0h]

Time Stamp ESTF Generate Function Comparison Low Value

Return to Summary Table

Offset = 200h + (j * 20h); where j = 0 to 1d

Table 14-27816. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0000h + formula**

Figure 14-9223. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-27818. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	ESTFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.9.3.1.2.366 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register (Offset = 4h + formula) [reset = 0h]

Time Stamp ESTF Generate Function Comparison high Value

Return to Summary Table

Offset = 204h + (j * 20h); where j = 0 to 1d

Table 14-27819. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0004h + formula**

Figure 14-9224. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-27821. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	ESTFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.9.3.1.2.367 CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register (Offset = 8h + formula) [reset = 0h]

Time Stamp ESTF Generate Function Control

Return to Summary Table

Offset = 208h + (j * 20h); where j = 0 to 1d

Table 14-27822. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0008h + formula**

Figure 14-9225. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-27824. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) Polarity Invert. 0h The output TS_ESTFn signal asserts low 1h The output TS_ESTFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

14.9.3.1.2.368 CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register (Offset = Ch + formula) [reset = 0h]

Time Stamp ESTF Generate Function Length Value

Return to Summary Table

Offset = 20Ch + (j * 20h); where j = 0 to 1d

Table 14-27825. Instance Table

Instance Name	Physical Address
CPSW0	**0800 000Ch + formula**

Figure 14-9226. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-27827. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Length Value.

14.9.3.1.2.369 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register (Offset = 10h + formula) [reset = 0h]

Time Stamp ESTF Generate Function PPM Low Value

Return to Summary Table

Offset = 210h + (j * 20h); where j = 0 to 1d

Table 14-27828. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0010h + formula**

Figure 14-9227. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-27830. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.9.3.1.2.370 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register (Offset = 14h + formula) [reset = 0h]

Time Stamp ESTF Generate Function PPM High Value

Return to Summary Table

Offset = 214h + (j * 20h); where j = 0 to 1d

Table 14-27831. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0014h + formula**

Figure 14-9228. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPM_HIGH							
R/W							
0h							

Table 14-27833. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM High Value. This value should be written first (before the low value is written).

14.9.3.1.2.371 CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register

1 CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register (Offset = 18h + formula) [reset = 0h]

Time Stamp ESTF Generate Function Nudge Value

Return to Summary Table

Offset = 218h + (j * 20h); where j = 0 to 1d

Table 14-27834. Instance Table

Instance Name	Physical Address
CPSW0	**0800 0018h + formula**

Figure 14-9229. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-27836. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_ESTF_NUDGE_REG_l[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_ESTF_NUDGE_REG_l value is cleared to zero when the nudge has occurred.

14.9.3.2 USB

USB

14.9.3.2.1 USB Summaries

USB Summaries

Table 14-27837. USB2SS_USB2SS_DEBUG_TRACE Registers, Base Address=0070 3000h, Length=512

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
80h	32	USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL	0070 3080h	0070 C080h
0h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_J	0070 3000h + formula	0070 C000h + formula
4h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_J	0070 3004h + formula	0070 C004h + formula
8h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_J	0070 3008h + formula	0070 C008h + formula
Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_J	0070 300Ch + formula	0070 C00Ch + formula
10h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_J	0070 3010h + formula	0070 C010h + formula
14h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_J	0070 3014h + formula	0070 C014h + formula
18h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_J	0070 3018h + formula	0070 C018h + formula
1Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_J	0070 301Ch + formula	0070 C01Ch + formula
20h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_J	0070 3020h + formula	0070 C020h + formula
24h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_J	0070 3024h + formula	0070 C024h + formula
28h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_J	0070 3028h + formula	0070 C028h + formula
2Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_J	0070 302Ch + formula	0070 C02Ch + formula
30h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_J	0070 3030h + formula	0070 C030h + formula
34h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_J	0070 3034h + formula	0070 C034h + formula
38h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_J	0070 3038h + formula	0070 C038h + formula
3Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_J	0070 303Ch + formula	0070 C03Ch + formula

Table 14-27838. USB2SS_USB2SS_CFG Registers, Base Address=0F90 0000h, Length=2048

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_USB2SS_CFG_REVISION	0F90 0000h	0F91 0000h
4h	32	USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL	0F90 0004h	0F91 0004h
8h	32	USB2SS_USB2SS_CFG_PHY_CONFIG	0F90 0008h	0F91 0008h
Ch	32	USB2SS_USB2SS_CFG_PHY_TEST	0F90 000Ch	0F91 000Ch
14h	32	USB2SS_USB2SS_CFG_CORE_STAT	0F90 0014h	0F91 0014h

Table 14-27838. USB2SS_USB2SS_CFG Registers, Base Address=0F90 0000h, Length=2048 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
18h	32	USB2SS_USB2SS_CFG_HOST_VBUS_CTRL	0F90 0018h	0F91 0018h
1Ch	32	USB2SS_USB2SS_CFG_MODE_CONTROL	0F90 001Ch	0F91 001Ch
30h	32	USB2SS_USB2SS_CFG_WAKEUP_CONFIG	0F90 0030h	0F91 0030h
34h	32	USB2SS_USB2SS_CFG_WAKEUP_STAT	0F90 0034h	0F91 0034h
38h	32	USB2SS_USB2SS_CFG_OVERRIDE_CONFIG	0F90 0038h	0F91 0038h
430h	32	USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW	0F90 0430h	0F91 0430h
434h	32	USB2SS_USB2SS_CFG_IRQ_MISC_STATUS	0F90 0434h	0F91 0434h
438h	32	USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET	0F90 0438h	0F91 0438h
43Ch	32	USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR	0F90 043Ch	0F91 043Ch
440h	32	USB2SS_USB2SS_CFG_IRQ_MISC_EOI	0F90 0440h	0F91 0440h
490h	32	USB2SS_USB2SS_CFG_INTR_TEST	0F90 0490h	0F91 0490h
614h	32	USB2SS_USB2SS_CFG_VBUS_FILTER	0F90 0614h	0F91 0614h
618h	32	USB2SS_USB2SS_CFG_VBUS_STAT	0F90 0618h	0F91 0618h
708h	32	USB2SS_USB2SS_CFG_DEBUG_CFG	0F90 0708h	0F91 0708h
70Ch	32	USB2SS_USB2SS_CFG_DEBUG_DATA	0F90 070Ch	0F91 070Ch
714h	32	USB2SS_USB2SS_CFG_HOST_HUB_CTRL	0F90 0714h	0F91 0714h

Table 14-27839. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_PHY2_AFE_TX_REG0	0F90 8000h	0F91 8000h
4h	32	USB2SS_PHY2_AFE_TX_REG1	0F90 8004h	0F91 8004h
8h	32	USB2SS_PHY2_AFE_TX_REG2	0F90 8008h	0F91 8008h
Ch	32	USB2SS_PHY2_AFE_TX_REG3	0F90 800Ch	0F91 800Ch
10h	32	USB2SS_PHY2_AFE_TX_REG4	0F90 8010h	0F91 8010h
14h	32	USB2SS_PHY2_AFE_TX_REG5	0F90 8014h	0F91 8014h
18h	32	USB2SS_PHY2_AFE_TX_REG6	0F90 8018h	0F91 8018h
1Ch	32	USB2SS_PHY2_AFE_TX_REG7	0F90 801Ch	0F91 801Ch
20h	32	USB2SS_PHY2_AFE_TX_REG8	0F90 8020h	0F91 8020h
24h	32	USB2SS_PHY2_AFE_TX_REG9	0F90 8024h	0F91 8024h
28h	32	USB2SS_PHY2_AFE_TX_REG10	0F90 8028h	0F91 8028h
2Ch	32	USB2SS_PHY2_AFE_TX_REG11	0F90 802Ch	0F91 802Ch
30h	32	USB2SS_PHY2_AFE_TX_REG12	0F90 8030h	0F91 8030h
34h	32	USB2SS_PHY2_AFE_RX_REG0	0F90 8034h	0F91 8034h
38h	32	USB2SS_PHY2_AFE_RX_REG1	0F90 8038h	0F91 8038h
3Ch	32	USB2SS_PHY2_AFE_RX_REG2	0F90 803Ch	0F91 803Ch
40h	32	USB2SS_PHY2_AFE_RX_REG3	0F90 8040h	0F91 8040h
44h	32	USB2SS_PHY2_AFE_RX_REG4	0F90 8044h	0F91 8044h
48h	32	USB2SS_PHY2_AFE_RX_REG5	0F90 8048h	0F91 8048h

Table 14-27839. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
4Ch	32	USB2SS_PHY2_AFE_RX_REG6	0F90 804Ch	0F91 804Ch
50h	32	USB2SS_PHY2_AFE_TX_REG13	0F90 8050h	0F91 8050h
54h	32	USB2SS_PHY2_AFE_TX_REG14	0F90 8054h	0F91 8054h
58h	32	USB2SS_PHY2_AFE_RX_REG7	0F90 8058h	0F91 8058h
5Ch	32	USB2SS_PHY2_AFE_RX_REG8	0F90 805Ch	0F91 805Ch
60h	32	USB2SS_PHY2_AFE_UNUSED_REG0	0F90 8060h	0F91 8060h
64h	32	USB2SS_PHY2_AFE_UNUSED_REG1	0F90 8064h	0F91 8064h
80h	32	USB2SS_PHY2_AFE_BG_REG0	0F90 8080h	0F91 8080h
84h	32	USB2SS_PHY2_AFE_BG_REG1	0F90 8084h	0F91 8084h
88h	32	USB2SS_PHY2_AFE_BG_REG2	0F90 8088h	0F91 8088h
8Ch	32	USB2SS_PHY2_AFE_BG_REG3	0F90 808Ch	0F91 808Ch
90h	32	USB2SS_PHY2_AFE_CALIB_REG0	0F90 8090h	0F91 8090h
94h	32	USB2SS_PHY2_AFE_BC_REG0	0F90 8094h	0F91 8094h
98h	32	USB2SS_PHY2_AFE_BC_REG1	0F90 8098h	0F91 8098h
9Ch	32	USB2SS_PHY2_AFE_BC_REG2	0F90 809Ch	0F91 809Ch
A0h	32	USB2SS_PHY2_AFE_BC_REG3	0F90 80A0h	0F91 80A0h
A4h	32	USB2SS_PHY2_AFE_BC_REG4	0F90 80A4h	0F91 80A4h
A8h	32	USB2SS_PHY2_AFE_BC_REG5	0F90 80A8h	0F91 80A8h
ACh	32	USB2SS_PHY2_AFE_BC_REG6	0F90 80ACh	0F91 80ACh
B0h	32	USB2SS_PHY2_AFE_PLL_REG0	0F90 80B0h	0F91 80B0h
B4h	32	USB2SS_PHY2_AFE_PLL_REG1	0F90 80B4h	0F91 80B4h
B8h	32	USB2SS_PHY2_AFE_PLL_REG2	0F90 80B8h	0F91 80B8h
BCh	32	USB2SS_PHY2_AFE_PLL_REG3	0F90 80BCh	0F91 80BCh
C0h	32	USB2SS_PHY2_AFE_PLL_REG4	0F90 80C0h	0F91 80C0h
C4h	32	USB2SS_PHY2_AFE_PLL_REG5	0F90 80C4h	0F91 80C4h
C8h	32	USB2SS_PHY2_AFE_BG_REG4	0F90 80C8h	0F91 80C8h
CCh	32	USB2SS_PHY2_AFE_CALIB_REG1	0F90 80CCh	0F91 80CCh
D0h	32	USB2SS_PHY2_AFE_BC_REG7	0F90 80D0h	0F91 80D0h
D4h	32	USB2SS_PHY2_AFE_PLL_REG6	0F90 80D4h	0F91 80D4h
D8h	32	USB2SS_PHY2_AFE_UNUSED_REG2	0F90 80D8h	0F91 80D8h
DCh	32	USB2SS_PHY2_AFE_UNUSED_REG3	0F90 80DCh	0F91 80DCh
100h	32	USB2SS_PHY2_PLL_REG0	0F90 8100h	0F91 8100h
104h	32	USB2SS_PHY2_PLL_REG1	0F90 8104h	0F91 8104h
108h	32	USB2SS_PHY2_PLL_REG2	0F90 8108h	0F91 8108h
10Ch	32	USB2SS_PHY2_PLL_REG3	0F90 810Ch	0F91 810Ch
110h	32	USB2SS_PHY2_PLL_REG4	0F90 8110h	0F91 8110h
114h	32	USB2SS_PHY2_PLL_REG5	0F90 8114h	0F91 8114h
118h	32	USB2SS_PHY2_PLL_REG6	0F90 8118h	0F91 8118h
11Ch	32	USB2SS_PHY2_PLL_REG7	0F90 811Ch	0F91 811Ch
120h	32	USB2SS_PHY2_PLL_REG8	0F90 8120h	0F91 8120h
124h	32	USB2SS_PHY2_PLL_REG9	0F90 8124h	0F91 8124h
128h	32	USB2SS_PHY2_PLL_REG10	0F90 8128h	0F91 8128h
12Ch	32	USB2SS_PHY2_PLL_REG11	0F90 812Ch	0F91 812Ch
130h	32	USB2SS_PHY2_PLL_REG12	0F90 8130h	0F91 8130h
134h	32	USB2SS_PHY2_PLL_REG13	0F90 8134h	0F91 8134h

Table 14-27839. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
138h	32	USB2SS_PHY2_PLL_REG14	0F90 8138h	0F91 8138h
13Ch	32	USB2SS_PHY2_PLL_UNUSED_REG0	0F90 813Ch	0F91 813Ch
140h	32	USB2SS_PHY2_PLL_UNUSED_REG1	0F90 8140h	0F91 8140h
144h	32	USB2SS_PHY2_PLL_REG15	0F90 8144h	0F91 8144h
148h	32	USB2SS_PHY2_PLL_REG16	0F90 8148h	0F91 8148h
14Ch	32	USB2SS_PHY2_PLL_UNUSED_REG2	0F90 814Ch	0F91 814Ch
180h	32	USB2SS_PHY2_CALIB_REG0	0F90 8180h	0F91 8180h
184h	32	USB2SS_PHY2_CALIB_REG1	0F90 8184h	0F91 8184h
188h	32	USB2SS_PHY2_BC_REG0	0F90 8188h	0F91 8188h
18Ch	32	USB2SS_PHY2_BC_REG1	0F90 818Ch	0F91 818Ch
190h	32	USB2SS_PHY2_BC_REG2	0F90 8190h	0F91 8190h
194h	32	USB2SS_PHY2_BC_REG3	0F90 8194h	0F91 8194h
198h	32	USB2SS_PHY2_BC_REG4	0F90 8198h	0F91 8198h
19Ch	32	USB2SS_PHY2_BC_REG5	0F90 819Ch	0F91 819Ch
1A0h	32	USB2SS_PHY2_BC_REG6	0F90 81A0h	0F91 81A0h
1A4h	32	USB2SS_PHY2_BC_REG7	0F90 81A4h	0F91 81A4h
1A8h	32	USB2SS_PHY2_TED_REG0	0F90 81A8h	0F91 81A8h
1ACh	32	USB2SS_PHY2_TED_REG1	0F90 81ACh	0F91 81ACh
1B0h	32	USB2SS_PHY2_TED_REG2	0F90 81B0h	0F91 81B0h
1B4h	32	USB2SS_PHY2_CALIB_REG2	0F90 81B4h	0F91 81B4h
1B8h	32	USB2SS_PHY2_CALIB_REG3	0F90 81B8h	0F91 81B8h
1BCh	32	USB2SS_PHY2_BC_REG8	0F90 81BCh	0F91 81BCh
1C0h	32	USB2SS_PHY2_BC_REG9	0F90 81C0h	0F91 81C0h
1C4h	32	USB2SS_PHY2_BC_REG10	0F90 81C4h	0F91 81C4h
1C8h	32	USB2SS_PHY2_BC_REG11	0F90 81C8h	0F91 81C8h
1CCh	32	USB2SS_PHY2_BC_REG12	0F90 81CCh	0F91 81CCh
1D0h	32	USB2SS_PHY2_TED_REG3	0F90 81D0h	0F91 81D0h
1D4h	32	USB2SS_PHY2_TED_REG4	0F90 81D4h	0F91 81D4h
1D8h	32	USB2SS_PHY2_DIG_UNUSED_REG0	0F90 81D8h	0F91 81D8h
1DCh	32	USB2SS_PHY2_DIG_UNUSED_REG1	0F90 81DCh	0F91 81DCh
1E0h	32	USB2SS_PHY2_DIG_UNUSED_REG2	0F90 81E0h	0F91 81E0h
1E4h	32	USB2SS_PHY2_DIG_UNUSED_REG3	0F90 81E4h	0F91 81E4h
1E8h	32	USB2SS_PHY2_INTERRUPT_REG1	0F90 81E8h	0F91 81E8h
1ECh	32	USB2SS_PHY2_INTERRUPT_REG2	0F90 81ECh	0F91 81ECh
200h	32	USB2SS_PHY2_RX_REG0	0F90 8200h	0F91 8200h
204h	32	USB2SS_PHY2_RX_REG1	0F90 8204h	0F91 8204h
208h	32	USB2SS_PHY2_TX_REG0	0F90 8208h	0F91 8208h
20Ch	32	USB2SS_PHY2_TX_REG1	0F90 820Ch	0F91 820Ch
210h	32	USB2SS_PHY2_CDR_REG0	0F90 8210h	0F91 8210h
214h	32	USB2SS_PHY2_CDR_REG1	0F90 8214h	0F91 8214h
218h	32	USB2SS_PHY2_CDR_REG2	0F90 8218h	0F91 8218h
21Ch	32	USB2SS_PHY2_CDR_REG3	0F90 821Ch	0F91 821Ch
220h	32	USB2SS_PHY2_CDR_REG4	0F90 8220h	0F91 8220h
224h	32	USB2SS_PHY2_CDR_REG5	0F90 8224h	0F91 8224h
228h	32	USB2SS_PHY2_CDR_REG6	0F90 8228h	0F91 8228h

Table 14-27839. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
22Ch	32	USB2SS_PHY2_CDR_REG7	0F90 822Ch	0F91 822Ch
230h	32	USB2SS_PHY2_CDR_REG8	0F90 8230h	0F91 8230h
234h	32	USB2SS_PHY2_RX_REG2	0F90 8234h	0F91 8234h
238h	32	USB2SS_PHY2_RX_REG3	0F90 8238h	0F91 8238h
23Ch	32	USB2SS_PHY2_RX_REG4	0F90 823Ch	0F91 823Ch
240h	32	USB2SS_PHY2_RX_REG5	0F90 8240h	0F91 8240h
244h	32	USB2SS_PHY2_RX_REG6	0F90 8244h	0F91 8244h
248h	32	USB2SS_PHY2_RX_REG7	0F90 8248h	0F91 8248h
24Ch	32	USB2SS_PHY2_TX_REG2	0F90 824Ch	0F91 824Ch
250h	32	USB2SS_PHY2_TX_REG3	0F90 8250h	0F91 8250h
254h	32	USB2SS_PHY2_TX_REG4	0F90 8254h	0F91 8254h
258h	32	USB2SS_PHY2_CDR_REG9	0F90 8258h	0F91 8258h
25Ch	32	USB2SS_PHY2_CDR_REG10	0F90 825Ch	0F91 825Ch
260h	32	USB2SS_PHY2_CDR_REG11	0F90 8260h	0F91 8260h
264h	32	USB2SS_PHY2_CDR_RE12	0F90 8264h	0F91 8264h
268h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG0	0F90 8268h	0F91 8268h
26Ch	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG1	0F90 826Ch	0F91 826Ch
270h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG2	0F90 8270h	0F91 8270h
274h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG3	0F90 8274h	0F91 8274h
280h	32	USB2SS_PHY2_UTMI_REG0	0F90 8280h	0F91 8280h
284h	32	USB2SS_PHY2_UTMI_REG1	0F90 8284h	0F91 8284h
288h	32	USB2SS_PHY2_UTMI_REG2	0F90 8288h	0F91 8288h
28Ch	32	USB2SS_PHY2_UTMI_REG3	0F90 828Ch	0F91 828Ch
290h	32	USB2SS_PHY2_UTMI_REG4	0F90 8290h	0F91 8290h
294h	32	USB2SS_PHY2_UTMI_REG5	0F90 8294h	0F91 8294h
298h	32	USB2SS_PHY2_UTMI_REG6	0F90 8298h	0F91 8298h
29Ch	32	USB2SS_PHY2_UTMI_REG7	0F90 829Ch	0F91 829Ch
2A0h	32	USB2SS_PHY2_UTMI_REG8	0F90 82A0h	0F91 82A0h
2A4h	32	USB2SS_PHY2_UTMI_REG9	0F90 82A4h	0F91 82A4h
2A8h	32	USB2SS_PHY2_UTMI_REG10	0F90 82A8h	0F91 82A8h
2ACh	32	USB2SS_PHY2_UTMI_REG11	0F90 82ACh	0F91 82ACh
2B0h	32	USB2SS_PHY2_UTMI_REG12	0F90 82B0h	0F91 82B0h
2B4h	32	USB2SS_PHY2_UTMI_REG13	0F90 82B4h	0F91 82B4h
2B8h	32	USB2SS_PHY2_UTMI_REG14	0F90 82B8h	0F91 82B8h
2BCh	32	USB2SS_PHY2_UTMI_REG15	0F90 82BCh	0F91 82BCh
2C0h	32	USB2SS_PHY2_UTMI_REG16	0F90 82C0h	0F91 82C0h
2C4h	32	USB2SS_PHY2_UTMI_REG17	0F90 82C4h	0F91 82C4h
2C8h	32	USB2SS_PHY2_UTMI_REG18	0F90 82C8h	0F91 82C8h
2CCh	32	USB2SS_PHY2_UTMI_REG19	0F90 82CCh	0F91 82CCh
2D0h	32	USB2SS_PHY2_UTMI_REG20	0F90 82D0h	0F91 82D0h
2D4h	32	USB2SS_PHY2_UTMI_REG21	0F90 82D4h	0F91 82D4h
2D8h	32	USB2SS_PHY2_UTMI_REG22	0F90 82D8h	0F91 82D8h

Table 14-27839. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
2DCh	32	USB2SS_PHY2_UTMI_REG23	0F90 82DCh	0F91 82DCh
2E0h	32	USB2SS_PHY2_UTMI_REG24	0F90 82E0h	0F91 82E0h
2E4h	32	USB2SS_PHY2_UTMI_REG25	0F90 82E4h	0F91 82E4h
2E8h	32	USB2SS_PHY2_UTMI_REG26	0F90 82E8h	0F91 82E8h
2ECh	32	USB2SS_PHY2_UTMI_REG27	0F90 82ECh	0F91 82ECh
2F0h	32	USB2SS_PHY2_UTMI_REG28	0F90 82F0h	0F91 82F0h
2F4h	32	USB2SS_PHY2_UTMI_REG29	0F90 82F4h	0F91 82F4h
2F8h	32	USB2SS_PHY2_UTMI_REG30	0F90 82F8h	0F91 82F8h
2FCh	32	USB2SS_PHY2_UTMI_UNUSED_REG0	0F90 82FCh	0F91 82FCh
300h	32	USB2SS_PHY2_UTMI_UNUSED_REG1	0F90 8300h	0F91 8300h
304h	32	USB2SS_PHY2_UTMI_UNUSED_REG2	0F90 8304h	0F91 8304h
308h	32	USB2SS_PHY2_UTMI_UNUSED_REG3	0F90 8308h	0F91 8308h
30Ch	32	USB2SS_PHY2_UTMI_REG31	0F90 830Ch	0F91 830Ch
310h	32	USB2SS_PHY2_UTMI_REG32	0F90 8310h	0F91 8310h
314h	32	USB2SS_PHY2_UTMI_REG33	0F90 8314h	0F91 8314h
318h	32	USB2SS_PHY2_UTMI_REG34	0F90 8318h	0F91 8318h
31Ch	32	USB2SS_PHY2_UTMI_REG35	0F90 831Ch	0F91 831Ch
320h	32	USB2SS_PHY2_UTMI_REG36	0F90 8320h	0F91 8320h
324h	32	USB2SS_PHY2_UTMI_REG37	0F90 8324h	0F91 8324h
328h	32	USB2SS_PHY2_UTMI_REG38	0F90 8328h	0F91 8328h
32Ch	32	USB2SS_PHY2_UTMI_REG39	0F90 832Ch	0F91 832Ch
330h	32	USB2SS_PHY2_UTMI_REG40	0F90 8330h	0F91 8330h
334h	32	USB2SS_PHY2_UTMI_REG41	0F90 8334h	0F91 8334h
338h	32	USB2SS_PHY2_UTMI_REG42	0F90 8338h	0F91 8338h
33Ch	32	USB2SS_PHY2_UTMI_REG43	0F90 833Ch	0F91 833Ch
340h	32	USB2SS_PHY2_UTMI_REG44	0F90 8340h	0F91 8340h
344h	32	USB2SS_PHY2_UTMI_REG45	0F90 8344h	0F91 8344h
348h	32	USB2SS_PHY2_UTMI_REG46	0F90 8348h	0F91 8348h
34Ch	32	USB2SS_PHY2_UTMI_REG47	0F90 834Ch	0F91 834Ch
350h	32	USB2SS_PHY2_UTMI_REG48	0F90 8350h	0F91 8350h
354h	32	USB2SS_PHY2_UTMI_REG49	0F90 8354h	0F91 8354h
358h	32	USB2SS_PHY2_UTMI_REG50	0F90 8358h	0F91 8358h
35Ch	32	USB2SS_PHY2_UTMI_REG51	0F90 835Ch	0F91 835Ch
360h	32	USB2SS_PHY2_UTMI_REG52	0F90 8360h	0F91 8360h
364h	32	USB2SS_PHY2_UTMI_REG53	0F90 8364h	0F91 8364h
368h	32	USB2SS_PHY2_UTMI_REG54	0F90 8368h	0F91 8368h
36Ch	32	USB2SS_PHY2_UTMI_REG55	0F90 836Ch	0F91 836Ch
370h	32	USB2SS_PHY2_UTMI_REG56	0F90 8370h	0F91 8370h
374h	32	USB2SS_PHY2_UTMI_REG57	0F90 8374h	0F91 8374h
378h	32	USB2SS_PHY2_UTMI_REG58	0F90 8378h	0F91 8378h
37Ch	32	USB2SS_PHY2_UTMI_REG59	0F90 837Ch	0F91 837Ch
380h	32	USB2SS_PHY2_UTMI_UNUSED_REG6	0F90 8380h	0F91 8380h
384h	32	USB2SS_PHY2_UTMI_UNUSED_REG7	0F90 8384h	0F91 8384h

Table 14-27840. ECC_AGGR Registers, Base Address=0F98 0000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	ECC_AGGR_REV	0F98 0000h	0F99 0000h
8h	32	ECC_AGGR_VECTOR	0F98 0008h	0F99 0008h
Ch	32	ECC_AGGR_STAT	0F98 000Ch	0F99 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0F98 0010h + formula	0F99 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0F98 003Ch	0F99 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0F98 0040h	0F99 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0F98 0080h	0F99 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0F98 00C0h	0F99 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0F98 013Ch	0F99 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0F98 0140h	0F99 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0F98 0180h	0F99 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0F98 01C0h	0F99 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0F98 0200h	0F99 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0F98 0204h	0F99 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0F98 0208h	0F99 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0F98 020Ch	0F99 020Ch

Table 14-27841. USB2SS_CAP Registers, Base Address=3100 0000h, Length=32

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_CAP_CAPLENGTH	3100 0000h	3110 0000h
4h	32	USB2SS_CAP_HCSPARAMS1	3100 0004h	3110 0004h
8h	32	USB2SS_CAP_HCSPARAMS2	3100 0008h	3110 0008h
Ch	32	USB2SS_CAP_HCSPARAMS3	3100 000Ch	3110 000Ch
10h	32	USB2SS_CAP_HCCPARAMS1	3100 0010h	3110 0010h
14h	32	USB2SS_CAP_DBOFF	3100 0014h	3110 0014h
18h	32	USB2SS_CAP_RTSOFF	3100 0018h	3110 0018h
1Ch	32	USB2SS_CAP_HCCPARAMS2	3100 001Ch	3110 001Ch

Table 14-27842. USB2SS_OPER Registers, Base Address=3100 0020h, Length=64

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_OPER_USBCMD	3100 0020h	3110 0020h
4h	32	USB2SS_OPER_USBSTS	3100 0024h	3110 0024h
8h	32	USB2SS_OPER_PAGESIZE	3100 0028h	3110 0028h
14h	32	USB2SS_OPER_DNCTRL	3100 0034h	3110 0034h
18h	32	USB2SS_OPER_CRCR_LO	3100 0038h	3110 0038h
1Ch	32	USB2SS_OPER_CRCR_HI	3100 003Ch	3110 003Ch
30h	32	USB2SS_OPER_DCBAAP_LO	3100 0050h	3110 0050h
34h	32	USB2SS_OPER_DCBAAP_HI	3100 0054h	3110 0054h
38h	32	USB2SS_OPER_CONFIG	3100 0058h	3110 0058h

Table 14-27843. USB2SS_PORT Registers, Base Address=3100 0420h, Length=32

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_PORT_XHCI_PORT_20_PORTSC_20	3100 0420h	3110 0420h
4h	32	USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20	3100 0424h	3110 0424h
8h	32	USB2SS_PORT_XHCI_PORT_20_PORTLI_20	3100 0428h	3110 0428h
Ch	32	USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20	3100 042Ch	3110 042Ch
4h	32	USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30	3100 0424h	3110 0424h
8h	32	USB2SS_PORT_XHCI_PORT_30_PORTLI_30	3100 0428h	3110 0428h
Ch	32	USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30	3100 042Ch	3110 042Ch

Table 14-27844. USB2SS_RUNTIME Registers, Base Address=3100 0440h, Length=32

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_RUNTIME_MFINDEX	3100 0440h	3110 0440h
4h	32	USB2SS_RUNTIME_RSVDZ	3100 0444h	3110 0444h

Table 14-27845. USB2SS_INTR Registers, Base Address=3100 0460h, Length=64

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_INTR_XHCI_INTR_IMAN_J	3100 0460h + formula	3110 0460h + formula
4h	32	USB2SS_INTR_XHCI_INTR_IMOD_J	3100 0464h + formula	3110 0464h + formula
8h	32	USB2SS_INTR_XHCI_INTR_ERSTSZ_J	3100 0468h + formula	3110 0468h + formula
Ch	32	USB2SS_INTR_XHCI_INTR_RSVDP_J	3100 046Ch + formula	3110 046Ch + formula
10h	32	USB2SS_INTR_XHCI_INTR_ERSTBA_LO_J	3100 0470h + formula	3110 0470h + formula
14h	32	USB2SS_INTR_XHCI_INTR_ERSTBA_HI_J	3100 0474h + formula	3110 0474h + formula
18h	32	USB2SS_INTR_XHCI_INTR_ERDP_LO_J	3100 0478h + formula	3110 0478h + formula
1Ch	32	USB2SS_INTR_XHCI_INTR_ERDP_HI_J	3100 047Ch + formula	3110 047Ch + formula

Table 14-27846. USB2SS_DBARR Registers, Base Address=3100 0560h, Length=512

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_DBARR_XHCI_DB_DB_J	3100 0560h + formula	3110 0560h + formula

Table 14-27847. USB2SS_EXTCAP Registers, Base Address=3100 0960h, Length=16

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_EXTCAP_USBLEGSUP	3100 0960h	3110 0960h
4h	32	USB2SS_EXTCAP_USBLEGCTLSTS	3100 0964h	3110 0964h

Table 14-27848. USB2SS_SUPPRTCAP2 Registers, Base Address=3100 0970h, Length=16

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW0	3100 0970h	3110 0970h

Table 14-27848. USB2SS_SUPPRTCAP2 Registers, Base Address=3100 0970h, Length=16 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
4h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW1	3100 0974h	3110 0974h
8h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW2	3100 0978h	3110 0978h
Ch	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW3	3100 097Ch	3110 097Ch

Table 14-27849. USB2SS_SUPPRTCAP3 Registers, Base Address=3100 0980h, Length=32

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW0	3100 0980h	3110 0980h
4h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW1	3100 0984h	3110 0984h
8h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW2	3100 0988h	3110 0988h
Ch	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW3	3100 098Ch	3110 098Ch

Table 14-27850. USB2SS_GBL Registers, Base Address=3100 C100h, Length=2048

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_GBL_GSBUSCFG0	3100 C100h	3110 C100h
4h	32	USB2SS_GBL_GSBUSCFG1	3100 C104h	3110 C104h
8h	32	USB2SS_GBL_GTXTHRCFG	3100 C108h	3110 C108h
Ch	32	USB2SS_GBL_GRXTHRCFG	3100 C10Ch	3110 C10Ch
10h	32	USB2SS_GBL_GCTL	3100 C110h	3110 C110h
14h	32	USB2SS_GBL_GPMSTS	3100 C114h	3110 C114h
18h	32	USB2SS_GBL_GSTS	3100 C118h	3110 C118h
1Ch	32	USB2SS_GBL_GUCTL1	3100 C11Ch	3110 C11Ch
20h	32	USB2SS_GBL_GSNPSID	3100 C120h	3110 C120h
24h	32	USB2SS_GBL_GGPIO	3100 C124h	3110 C124h
28h	32	USB2SS_GBL_GUID	3100 C128h	3110 C128h
2Ch	32	USB2SS_GBL_GUCTL	3100 C12Ch	3110 C12Ch
30h	32	USB2SS_GBL_GBUSERRADDRLO	3100 C130h	3110 C130h
34h	32	USB2SS_GBL_GBUSERRADDRHI	3100 C134h	3110 C134h
38h	32	USB2SS_GBL_GPRTBIMAPLO	3100 C138h	3110 C138h
3Ch	32	USB2SS_GBL_GPRTBIMAPHI	3100 C13Ch	3110 C13Ch
40h	32	USB2SS_GBL_GHWPARAMS0	3100 C140h	3110 C140h
44h	32	USB2SS_GBL_GHWPARAMS1	3100 C144h	3110 C144h
48h	32	USB2SS_GBL_GHWPARAMS2	3100 C148h	3110 C148h
4Ch	32	USB2SS_GBL_GHWPARAMS3	3100 C14Ch	3110 C14Ch
50h	32	USB2SS_GBL_GHWPARAMS4	3100 C150h	3110 C150h
54h	32	USB2SS_GBL_GHWPARAMS5	3100 C154h	3110 C154h
58h	32	USB2SS_GBL_GHWPARAMS6	3100 C158h	3110 C158h
5Ch	32	USB2SS_GBL_GHWPARAMS7	3100 C15Ch	3110 C15Ch
60h	32	USB2SS_GBL_GDBGFIFOSPACE	3100 C160h	3110 C160h
64h	32	USB2SS_GBL_GDBGLTSSM	3100 C164h	3110 C164h
68h	32	USB2SS_GBL_GDBGLNMCC	3100 C168h	3110 C168h
6Ch	32	USB2SS_GBL_GDBGBMU	3100 C16Ch	3110 C16Ch
70h	32	USB2SS_GBL_GDBGLSPMUX_HST	3100 C170h	3110 C170h
74h	32	USB2SS_GBL_GDBGLSP	3100 C174h	3110 C174h
78h	32	USB2SS_GBL_GDBGEPINFO0	3100 C178h	3110 C178h

Table 14-27850. USB2SS_GBL Registers, Base Address=3100 C100h, Length=2048 (continued)

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
7Ch	32	USB2SS_GBL_GDBGEPINFO1	3100 C17Ch	3110 C17Ch
80h	32	USB2SS_GBL_GPRTBIMAP_HSLO	3100 C180h	3110 C180h
84h	32	USB2SS_GBL_GPRTBIMAP_HSHI	3100 C184h	3110 C184h
88h	32	USB2SS_GBL_GPRTBIMAP_FSLO	3100 C188h	3110 C188h
8Ch	32	USB2SS_GBL_GPRTBIMAP_FSHI	3100 C18Ch	3110 C18Ch
94h	32	USB2SS_GBL_RESERVED_94	3100 C194h	3110 C194h
98h	32	USB2SS_GBL_RESERVED_98	3100 C198h	3110 C198h
9Ch	32	USB2SS_GBL_GUCTL2	3100 C19Ch	3110 C19Ch
500h	32	USB2SS_GBL_GHWPARAMS8	3100 C600h	3110 C600h
50Ch	32	USB2SS_GBL_GUCTL3	3100 C60Ch	3110 C60Ch
510h	32	USB2SS_GBL_GTXFIFOPRIDEV	3100 C610h	3110 C610h
518h	32	USB2SS_GBL_GTXFIFOPRIHST	3100 C618h	3110 C618h
51Ch	32	USB2SS_GBL_GRXFIFOPRIHST	3100 C61Ch	3110 C61Ch
524h	32	USB2SS_GBL_GDMAHLRATIO	3100 C624h	3110 C624h
530h	32	USB2SS_GBL_GFLADJ	3100 C630h	3110 C630h
0h	32	USB2SS_GBL_GPHY_GUSB2PHYCFG	3100 C100h	3110 C100h
0h	32	USB2SS_GBL_GI2C_GUSB2I2CCTL	3100 C100h	3110 C100h
0h	32	USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI	3100 C100h	3110 C100h
0h	32	USB2SS_GBL_GPIPE_GUSB3PIPECTL	3100 C100h	3110 C100h
0h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0	3100 C100h	3110 C100h
4h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1	3100 C104h	3110 C104h
8h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2	3100 C108h	3110 C108h
Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3	3100 C10Ch	3110 C10Ch
10h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4	3100 C110h	3110 C110h
14h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5	3100 C114h	3110 C114h
18h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6	3100 C118h	3110 C118h
1Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7	3100 C11Ch	3110 C11Ch
20h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8	3100 C120h	3110 C120h
24h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9	3100 C124h	3110 C124h
28h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10	3100 C128h	3110 C128h
2Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11	3100 C12Ch	3110 C12Ch
30h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12	3100 C130h	3110 C130h
34h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13	3100 C134h	3110 C134h
38h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14	3100 C138h	3110 C138h
3Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15	3100 C13Ch	3110 C13Ch
0h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0	3100 C100h	3110 C100h
4h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1	3100 C104h	3110 C104h
8h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2	3100 C108h	3110 C108h
0h	32	USB2SS_GBL_GEVNT_GEVNTADRLO_J	3100 C100h + formula	3110 C100h + formula
4h	32	USB2SS_GBL_GEVNT_GEVNTADRHI_J	3100 C104h + formula	3110 C104h + formula
8h	32	USB2SS_GBL_GEVNT_GEVNTSIZ_J	3100 C108h + formula	3110 C108h + formula
Ch	32	USB2SS_GBL_GEVNT_GEVNTCOUNT_J	3100 C10Ch + formula	3110 C10Ch + formula
0h	32	USB2SS_GBL_GRHB_GUSB2RHBCTL	3100 C100h	3110 C100h

Table 14-27851. USB2SS_DEV Registers, Base Address=3100 C700h, Length=2048

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_DEV_DCFG	3100 C700h	3110 C700h
4h	32	USB2SS_DEV_DCTL	3100 C704h	3110 C704h
8h	32	USB2SS_DEV_DEVTEN	3100 C708h	3110 C708h
Ch	32	USB2SS_DEV_DSTS	3100 C70Ch	3110 C70Ch
10h	32	USB2SS_DEV_DGCMDPAR	3100 C710h	3110 C710h
14h	32	USB2SS_DEV_DGCMD	3100 C714h	3110 C714h
20h	32	USB2SS_DEV_DALEPENA	3100 C720h	3110 C720h
0h	32	USB2SS_DEV_DEV_RESERVED_RSVD_J	3100 C700h + formula	3110 C700h + formula
0h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_J	3100 C700h + formula	3110 C700h + formula
4h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_J	3100 C704h + formula	3110 C704h + formula
8h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_J	3100 C708h + formula	3110 C708h + formula
Ch	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_J	3100 C70Ch + formula	3110 C70Ch + formula
0h	32	USB2SS_DEV_DEV_INTR_DEV_IMOD_J	3100 C700h + formula	3110 C700h + formula

Table 14-27852. USB2SS_LINK Registers, Base Address=3100 D000h, Length=128

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_LINK_LINK_LU1LFPSRXTIM	3100 D000h	3110 D000h
20h	32	USB2SS_LINK_LINK_LINK_SETTINGS	3100 D020h	3110 D020h
24h	32	USB2SS_LINK_LINK_LLUCTL	3100 D024h	3110 D024h
28h	32	USB2SS_LINK_LINK_LPTMDPDELAY	3100 D028h	3110 D028h

Table 14-27853. USB2SS_DEBUG Registers, Base Address=3100 D800h, Length=512

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_DEBUG_DEBUG_U3RHBDBG	3100 D800h	3110 D800h

Table 14-27854. USB2SS_DEBUG_RAM0 Registers, Base Address=3104 0000h, Length=65536

Offset	Length	Register Name	USB0 Physical Address	USB1 Physical Address
0h	32	USB2SS_DEBUG_RAM0_RAM0_J	3104 0000h + formula	3114 0000h + formula

14.9.3.2.2 USB Registers

USB Registers

14.9.3.2.2.1 USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register

1 USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register (Offset = 80h) [reset = 0h]

Debug trace control register

Return to Summary Table

Table 14-27855. Instance Table

Instance Name	Physical Address
USB0	**0070 3080h**
USB1	**0070 C080h**

Figure 14-9230. USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD				EN_OUT_EP14	EN_OUT_EP15	EN_IN_EP14	EN_IN_EP15
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27857. USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved bits Reset Source: cfg_srst_n
3	EN_OUT_EP14	R/W	0h	Debug trace enable for OUT Endpoint 14 Reset Source: cfg_srst_n
2	EN_OUT_EP15	R/W	0h	Debug trace enable for OUT Endpoint 15 Reset Source: cfg_srst_n
1	EN_IN_EP14	R/W	0h	Debug trace enable for IN Endpoint 14 Reset Source: cfg_srst_n
0	EN_IN_EP15	R/W	0h	Debug trace enable for IN Endpoint 15 Reset Source: cfg_srst_n

14.9.3.2.2.2 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register (Offset = 0h + formula) [reset = 0h]

TRB0 Word 0. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 0h + (j * 40h); where j = 0 to 1d

Table 14-27858. Instance Table

Instance Name	Physical Address
USB0	0070 3000h + formula
USB1	0070 C000h + formula

Figure 14-9231. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27860. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n

Table 14-27860. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.9.3.2.2.3 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Register (Offset = 4h + formula) [reset = 0h]

TRB0 Word 1. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 4h + (j * 40h); where j = 0 to 1d

Table 14-27861. Instance Table

Instance Name	Physical Address
USB0	**0070 3004h + formula**
USB1	**0070 C004h + formula**

Figure 14-9232. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BUFSIZ							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUFSIZ							
R/W							
0h							

Table 14-27863. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.9.3.2.2.4 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Register (Offset = 8h + formula) [reset = 0h]

TRB0 Word 2. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 8h + (j * 40h); where j = 0 to 1d

Table 14-27864. Instance Table

Instance Name	Physical Address
USB0	**0070 3008h + formula**
USB1	**0070 C008h + formula**

Figure 14-9233. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-27866. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.9.3.2.2.5 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Register (Offset = Ch + formula) [reset = 0h]

TRB0 Word 3. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = Ch + (j * 40h); where j = 0 to 1d

Table 14-27867. Instance Table

Instance Name	Physical Address
USB0	**0070 300Ch + formula**
USB1	**0070 C00Ch + formula**

Figure 14-9234. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRL							
R/W							
0h							

Table 14-27869. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.9.3.2.2.6 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register (Offset = 10h + formula) [reset = 0h]

TRB1 Word 0. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 10h + (j * 40h); where j = 0 to 1d

Table 14-27870. Instance Table

Instance Name	Physical Address
USB0	0070 3010h + formula
USB1	0070 C010h + formula

Figure 14-9235. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27872. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n

Table 14-27872. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.9.3.2.2.7 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Register (Offset = 14h + formula) [reset = 0h]

TRB1 Word 1. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 14h + (j * 40h); where j = 0 to 1d

Table 14-27873. Instance Table

Instance Name	Physical Address
USB0	**0070 3014h + formula**
USB1	**0070 C014h + formula**

Figure 14-9236. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-27875. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.9.3.2.2.8 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Register (Offset = 18h + formula) [reset = 0h]

TRB1 Word 2. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 18h + (j * 40h); where j = 0 to 1d

Table 14-27876. Instance Table

Instance Name	Physical Address
USB0	**0070 3018h + formula**
USB1	**0070 C018h + formula**

Figure 14-9237. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-27878. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.9.3.2.2.9 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Register (Offset = 1Ch + formula) [reset = 0h]

TRB1 Word 3. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 1Ch + (j * 40h); where j = 0 to 1d

Table 14-27879. Instance Table

Instance Name	Physical Address
USB0	**0070 301Ch + formula**
USB1	**0070 C01Ch + formula**

Figure 14-9238. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRL							
R/W							
0h							

Table 14-27881. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.9.3.2.2.10 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register (Offset = 20h + formula) [reset = 0h]

TRB2 Word 0. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 20h + (j * 40h); where j = 0 to 1d

Table 14-27882. Instance Table

Instance Name	Physical Address
USB0	**0070 3020h + formula**
USB1	**0070 C020h + formula**

Figure 14-9239. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27884. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n

Table 14-27884. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.9.3.2.2.11 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Register (Offset = 24h + formula) [reset = 0h]

TRB2 Word 1. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 24h + (j * 40h); where j = 0 to 1d

Table 14-27885. Instance Table

Instance Name	Physical Address
USB0	**0070 3024h + formula**
USB1	**0070 C024h + formula**

Figure 14-9240. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-27887. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.9.3.2.2.12 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Register (Offset = 28h + formula) [reset = 0h]

TRB2 Word 2. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 28h + (j * 40h); where j = 0 to 1d

Table 14-27888. Instance Table

Instance Name	Physical Address
USB0	**0070 3028h + formula**
USB1	**0070 C028h + formula**

Figure 14-9241. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-27890. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.9.3.2.2.13 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Register (Offset = 2Ch + formula) [reset = 0h]

TRB2 Word 3. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 2Ch + (j * 40h); where j = 0 to 1d

Table 14-27891. Instance Table

Instance Name	Physical Address
USB0	0070 302Ch + formula
USB1	0070 C02Ch + formula

Figure 14-9242. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BPTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BPTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BPTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BPTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27893. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.9.3.2.2.14 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register (Offset = 30h + formula) [reset = 0h]

TRB3 Word 0. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 30h + (j * 40h); where j = 0 to 1d

Table 14-27894. Instance Table

Instance Name	Physical Address
USB0	**0070 3030h + formula**
USB1	**0070 C030h + formula**

Figure 14-9243. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27896. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n

Table 14-27896. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.9.3.2.2.15 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Register (Offset = 34h + formula) [reset = 0h]

TRB3 Word 1. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 34h + (j * 40h); where j = 0 to 1d

Table 14-27897. Instance Table

Instance Name	Physical Address
USB0	**0070 3034h + formula**
USB1	**0070 C034h + formula**

Figure 14-9244. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BUFSIZ							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUFSIZ							
R/W							
0h							

Table 14-27899. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.9.3.2.2.16 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Register (Offset = 38h + formula) [reset = 0h]

TRB3 Word 2. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 38h + (j * 40h); where j = 0 to 1d

Table 14-27900. Instance Table

Instance Name	Physical Address
USB0	**0070 3038h + formula**
USB1	**0070 C038h + formula**

Figure 14-9245. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-27902. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.9.3.2.2.17 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Register

1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Register (Offset = 3Ch + formula) [reset = 0h]

TRB3 Word 3. Please refer to Controller programming guide for more details on these fields.

Return to Summary Table

Offset = 3Ch + (j * 40h); where j = 0 to 1d

Table 14-27903. Instance Table

Instance Name	Physical Address
USB0	0070 303Ch + formula
USB1	0070 C03Ch + formula

Figure 14-9246. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRL							
R/W							
0h							

Table 14-27905. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.9.3.2.2.18 USB2SS_USB2SS_CFG_REVISION Register

1 USB2SS_USB2SS_CFG_REVISION Register (Offset = 0h) [reset = 68214900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-27906. Instance Table

Instance Name	Physical Address
USB0	**0F90 0000h**
USB1	**0F91 0000h**

Figure 14-9247. USB2SS_USB2SS_CFG_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		821h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
821h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-27908. USB2SS_USB2SS_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: cfg_srst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: cfg_srst_n
27:16	MODULE_ID	R	821h	Module ID Reset Source: cfg_srst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: cfg_srst_n
10:8	MAJOR	R	1h	Major revision Reset Source: cfg_srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: cfg_srst_n
5:0	MINOR	R	0h	Minor revision Reset Source: cfg_srst_n

14.9.3.2.2.19 USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register

1 USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register (Offset = 4h) [reset = 10000h]

This register contains bits for indicating overcurrent condition on VBUS to Controller

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Table 14-27909. Instance Table

Instance Name	Physical Address
USB0	**0F90 0004h**
USB1	**0F91 0004h**

Figure 14-9248. USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD3							
R							
0h							
23	22	21	20	19	18	17	16
RSVD3							OVERCURRENT_N
R							R/W
0h							1h
15	14	13	12	11	10	9	8
RSVD2							OVERCURRENT_SEL
R							R/W
0h							0h
7	6	5	4	3	2	1	0
RSVD1							
R							
0h							

Table 14-27911. USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RSVD3	R	0h	Reserved bits Reset Source: cfg_srst_n
16	OVERCURRENT_N	R/W	1h	Overcurrent indicator to the Controller Reset Source: cfg_srst_n
15:9	RSVD2	R	0h	Reserved bits Reset Source: cfg_srst_n
8	OVERCURRENT_SEL	R/W	0h	Overcurrent MMR select. Has to be written before setting pwrup_rst_n bit. 1 - overcurrent MMR bit is used, 0 - port_overcurrent_n input is used Reset Source: cfg_srst_n
7:0	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n

14.9.3.2.2.20 USB2SS_USB2SS_CFG_PHY_CONFIG Register

1 USB2SS_USB2SS_CFG_PHY_CONFIG Register (Offset = 8h) [reset = 2h]

Wrapper register containing static settings. All bits in this register directly drive the USB2 PHY inputs. Please refer to USB2 PHY user guide for more information.

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Table 14-27912. Instance Table

Instance Name	Physical Address
USB0	**0F90 0008h**
USB1	**0F91 0008h**

Figure 14-9249. USB2SS_USB2SS_CFG_PHY_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED31_9							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_9							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_9							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED31_9			RESERVED4_3		VBUS_SEL		LANE_REVERSE
R			R/W		R/W		R/W
0h			0h		1h		0h

Table 14-27914. USB2SS_USB2SS_CFG_PHY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED31_9	R	0h	Reserved bits
4:3	RESERVED4_3	R/W	0h	Reserved bits
2:1	VBUS_SEL	R/W	1h	This register directly drives the vbus_sel[1:0] input to the PHY. VBUS select - 00: VBUS = 5.25V/3.3V, 01: VBUS/3 external divider is active, so VBUS could be upto 11V. Reset Source: cfg_srst_n
0	LANE_REVERSE	R/W	0h	This register directly drives the lane_reverse input to USB2 PHY. Lane reverse selection. When set, this bit indicates that D+ and D- lines have to be swapped. Reset Source: cfg_srst_n

14.9.3.2.2.21 USB2SS_USB2SS_CFG_PHY_TEST Register

1 USB2SS_USB2SS_CFG_PHY_TEST Register (Offset = Ch) [reset = 0h]

Register containing PLL bypass select, BIST control and status

Return to Summary Table

Table 14-27915. Instance Table

Instance Name	Physical Address
USB0	**0F90 000Ch**
USB1	**0F91 000Ch**

Figure 14-9250. USB2SS_USB2SS_CFG_PHY_TEST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED31_18</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED31_18</td><td>BIST_MODE</td><td>BIST_ERROR_COUNT</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">BIST_ERROR_COUNT</td><td>BIST_ERROR</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BIST_COMPLETE</td><td>BIST_ON</td><td>BIST_MODE_EN</td><td colspan="4">BIST_MODE_SEL</td><td>RESERVED0</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-27917. USB2SS_USB2SS_CFG_PHY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED31_18	R	0h	Reserved bits
17	BIST_MODE	R/W	0h	Set for bist mode. This is used for overriding PHY ports for BIST. Reset Source: cfg_srst_n
16:9	BIST_ERROR_COUNT	R	0h	Number of bytes that have errors while running BIST. The count resets when bist_on is set. Reset Source: cfg_srst_n
8	BIST_ERROR	R	0h	If set, this bit indicates that BIST completed with error. Reset Source: cfg_srst_n
7	BIST_COMPLETE	R	0h	If set, this bit indicates that the BIST operation is completed. Reset Source: cfg_srst_n
6	BIST_ON	R/W	0h	Setting this bit starts the BIST operation. Reset Source: cfg_srst_n
5	BIST_MODE_EN	R/W	0h	BIST Mode Enable. 0 = BIST not enabled, 1 = BIST enabled Reset Source: cfg_srst_n

Table 14-27917. USB2SS_USB2SS_CFG_PHY_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:1	BIST_MODE_SEL	R/W	0h	BIST Mode Selection. bist_mode_sel[3]: 0 = 8-bit interface, 1 = 16-bit interface; bist_mode_sel[2]: 0 = error injection disabled, 1 = error injection enabled; bist_mode_sel[1]: 0 = device mode, 1 = host mode; bist_mode_sel[0]: 0 = High Speed mode, 1 = Full Speed mode. Reset Source: cfg_srst_n
0	RESERVED0	R/W	0h	Reserved bits

14.9.3.2.2.22 USB2SS_USB2SS_CFG_CORE_STAT Register

1 USB2SS_USB2SS_CFG_CORE_STAT Register (Offset = 14h) [reset = 27E8h]

Register containing miscellaneous status bits from the core

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Table 14-27918. Instance Table

Instance Name	Physical Address
USB0	**0F90 0014h**
USB1	**0F91 0014h**

Figure 14-9251. USB2SS_USB2SS_CFG_CORE_STAT Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD1	HUB_VBUS_CTRL	OPERATIONAL_MODE		HOST_CURRENT_BELT			
R	R	R		R			
0h	0h	2h		7E8h			
7	6	5	4	3	2	1	0
HOST_CURRENT_BELT							
R							
7E8h							

Table 14-27920. USB2SS_USB2SS_CFG_CORE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
14	HUB_VBUS_CTRL	R	0h	Indicates whether core is asking for VBUS to be turned on in host mode. Reset Source: cfg_srst_n
13:12	OPERATIONAL_MODE	R	2h	Indicates current operational mode of Controller. This directly reflects the value programmed into GCTL.PRTCAPDIR Controller register. 2'b01 - Host, 2'b10 - Device. Reset Source: cfg_srst_n
11:0	HOST_CURRENT_BELT	R	7E8h	Indicates minimum of all received device BELT values and the BELT value set by the Set Latency Tolerance Value command. Reset Source: cfg_srst_n

14.9.3.2.2.23 USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register

1 USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register (Offset = 18h) [reset = 0h]

Register containing software bit for overriding drive VBUS

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Table 14-27921. Instance Table

Instance Name	Physical Address
USB0	**0F90 0018h**
USB1	**0F91 0018h**

Figure 14-9252. USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DRV_VBUS_OVERRIDE	DRV_VBUS_OVERRIDE_VAL
NONE						R/W	R/W
0h						0h	0h

Table 14-27923. USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DRV_VBUS_OVERRIDE	R/W	0h	Setting this bit enables drive VBUS override. Drive VBUS output reflects drv_vbus_override_val field value. Reset Source: cfg_srst_n
0	DRV_VBUS_OVERRIDE_VAL	R/W	0h	Drive VBUS output override value. Reset Source: cfg_srst_n

14.9.3.2.2.24 USB2SS_USB2SS_CFG_MODE_CONTROL Register

1 USB2SS_USB2SS_CFG_MODE_CONTROL Register (Offset = 1Ch) [reset = 0h]

Register containing software bit for indicating DRD mode is determined

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Table 14-27924. Instance Table

Instance Name	Physical Address
USB0	**0F90 001Ch**
USB1	**0F91 001Ch**

Figure 14-9253. USB2SS_USB2SS_CFG_MODE_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>MODE_VALID</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-27926. USB2SS_USB2SS_CFG_MODE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MODE_VALID	R/W	0h	For DRD applications, software sets this bit when the role is determined based on connect event and ID value from GPIO. Software clears this bit when a disconnect event happens and role is no longer valid. Software can also set this once during initialization for fixed role applications. Reset Source: cfg_srst_n

14.9.3.2.2.25 USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register

1 USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register (Offset = 30h) [reset = 0h]

Register containing low power mode wakeup enables

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Table 14-27927. Instance Table

Instance Name	Physical Address
USB0	**0F90 0030h**
USB1	**0F91 0030h**

Figure 14-9254. USB2SS_USB2SS_CFG_WAKEUP_CONFIG Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD1				OVERCURRENT_WAKEUP_EN	LINESTATE_WAKEUP_EN	SESSVALID_WAKEUP_EN	VBUSVALID_WAKEUP_EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-27929. USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
3	OVERCURRENT_WAKEUP_EN	R/W	0h	overcurrent event wakeup enable Reset Source: cfg_srst_n
2	LINESTATE_WAKEUP_EN	R/W	0h	linestate event wakeup enable Reset Source: cfg_srst_n
1	SESSVALID_WAKEUP_EN	R/W	0h	SESSVALID event wakeup enable Reset Source: cfg_srst_n
0	VBUSVALID_WAKEUP_EN	R/W	0h	VBUSVALID event wakeup enable Reset Source: cfg_srst_n

14.9.3.2.2.26 USB2SS_USB2SS_CFG_WAKEUP_STAT Register

1 USB2SS_USB2SS_CFG_WAKEUP_STAT Register (Offset = 34h) [reset = 0h]

Register containing low power mode status bits. The status bits are set when the corresponding wakeup event happens and the corresponding enable in WAKEUP_CONFIG MMR is set. In addition, these bits are only set if clockstop request from PSC is active in order to ensure that these are captured only during low power mode and not during regular operation. These bits can only be set by hardware and once set, they can only be cleared by software by setting wakeup_stat_clear field.

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Table 14-27930. Instance Table

Instance Name	Physical Address
USB0	**0F90 0034h**
USB1	**0F91 0034h**

Figure 14-9255. USB2SS_USB2SS_CFG_WAKEUP_STAT Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD1	OVERCURRENT_N_WAKEUP_CURRENT	OVERCURRENT_N_WAKEUP_PREV	LINESTATE_WAKEUP_CURRENT		LINESTATE_WAKEUP_PREV		SESSVALID_WAKEUP_CURRENT
R	R	R	R		R		R
0h	0h	0h	0h		0h		0h
7	6	5	4	3	2	1	0
SESSVALID_WAKEUP_PREV	VBUSVALID_WAKEUP_CURRENT	VBUSVALID_WAKEUP_PREV	OVERCURRENT_N_WAKEUP_STAT	LINESTATE_WAKEUP_STAT	SESSVALID_WAKEUP_STAT	VBUSVALID_WAKEUP_STAT	WAKEUP_STAT_CLEAR
R	R	R	R	R	R	R	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27932. USB2SS_USB2SS_CFG_WAKEUP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
14	OVERCURRENT_N_WAKEUP_CURRENT	R	0h	overcurrent_n current value during wakeup event Reset Source: cfg_srst_n
13	OVERCURRENT_N_WAKEUP_PREV	R	0h	overcurrent_n previous value during wakeup event Reset Source: cfg_srst_n
12:11	LINESTATE_WAKEUP_CURRENT	R	0h	Linestate current value during wakeup event Reset Source: cfg_srst_n
10:9	LINESTATE_WAKEUP_PREV	R	0h	Linestate previous value during wakeup event Reset Source: cfg_srst_n

Table 14-27932. USB2SS_USB2SS_CFG_WAKEUP_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SESSVALID_WAKEUP_CURRENT	R	0h	SESSVALID current value during wakeup event Reset Source: cfg_srst_n
7	SESSVALID_WAKEUP_PREV	R	0h	SESSVALID previous value during wakeup event Reset Source: cfg_srst_n
6	VBUSVALID_WAKEUP_CURRENT	R	0h	VBUSVALID current value during wakeup event Reset Source: cfg_srst_n
5	VBUSVALID_WAKEUP_PREV	R	0h	VBUSVALID previous value during wakeup event Reset Source: cfg_srst_n
4	OVERCURRENT_N_WAKEUP_STAT	R	0h	overcurrent_n event wakeup status. This is only looking for change on port_overcurrent_n input and does not include overcurrent MMR. This is because wakeup is required only for a port event and for any software write to happen, SOC should already have been awake. Also SOC may be tying off port_overcurrent_n, so this event may never trigger. Reset Source: cfg_srst_n
3	LINESTATE_WAKEUP_STAT	R	0h	linestate event wakeup status Reset Source: cfg_srst_n
2	SESSVALID_WAKEUP_STAT	R	0h	SESSVALID event wakeup status Reset Source: cfg_srst_n
1	VBUSVALID_WAKEUP_STAT	R	0h	VBUSVALID event wakeup status Reset Source: cfg_srst_n
0	WAKEUP_STAT_CLEAR	R/W1TC	0h	Clears all the *_wakeup_stat bits in this register Reset Source: cfg_srst_n

14.9.3.2.2.27 USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register

1 USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register (Offset = 38h) [reset = 0h]

Register containing various overrides

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Table 14-27933. Instance Table

Instance Name	Physical Address
USB0	**0F90 0038h**
USB1	**0F91 0038h**

Figure 14-9256. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Name Register

31	30	29	28	27	26	25	24
PHY_HVM_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							XCVRSEL_HVM_OVERRIDE_VAL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
XCVRSEL_HVM_OVERRIDE_VAL	TERMSEL_HVM_OVERRIDE_VAL	OPMODE_HVM_OVERRIDE_VAL		DMPULLDOWN_HVM_OVERRIDE_VAL	DPPULLDOWN_HVM_OVERRIDE_VAL	RESERVED	
R/W	R/W	R/W		R/W	R/W	NONE	
0h	0h	0h		0h	0h	0h	
7	6	5	4	3	2	1	0
SUSPEND_OVERRIDE_VAL	SUSPEND_OVERRIDE_SEL	TXBITSTUFFEN_OVERRIDE_VAL	TXBITSTUFFEN_OVERRIDE_SEL	SESSVALID_OVERRIDE_VAL	SESSVALID_OVERRIDE_SEL	VBUSVALID_OVERRIDE_VAL	VBUSVALID_OVERRIDE_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-27935. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_HVM_EN	R/W	0h	Enable PHY HVM overrides. Reset Source: cfg_srst_n
30:17	RESERVED	NONE	0h	Reserved
16:15	XCVRSEL_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY xcvr input. The value in this field is applied to PHY xcvrsel input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
14	TERMSEL_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY termsel input. The value in this field is applied to PHY termsel input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
13:12	OPMODE_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY opmode input. The value in this field is applied to PHY opmode input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n

Table 14-27935. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DMPULLDOWN_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY dmpulldown input. The value in this field is applied to PHY dmpulldown input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
10	DPPULLDOWN_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY dppulldown input. The value in this field is applied to PHY dppulldown input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
9:8	RESERVED	NONE	0h	Reserved
7	SUSPEND_OVERRIDE_VAL	R/W	0h	Suspend override value. 0 - suspendm is asserted and clockstop idle term indicates idle, 1 - suspendm is deasserted and clockstop idle term indicates non-idle. Reset Source: cfg_srst_n
6	SUSPEND_OVERRIDE_SEL	R/W	0h	Suspend override selector. This has to be set to override utmi_suspend_n from Controller that goes to clockstop idle. This does not affect suspend going to PHY. Only purpose of this is to ease clockstop interface DV. Reset Source: cfg_srst_n
5	TXBITSTUFFEN_OVERRIDE_VAL	R/W	0h	TXBITSTUFFENABLE override value Reset Source: cfg_srst_n
4	TXBITSTUFFEN_OVERRIDE_SEL	R/W	0h	TXBITSTUFFENABLE override selector. This has to be set to override TXBITSTUFFENABLE to PHY. Reset Source: cfg_srst_n
3	SESSVALID_OVERRIDE_VAL	R/W	0h	SESSVALID override value. 1 - Session is valid, 0 - Session is not valid Reset Source: cfg_srst_n
2	SESSVALID_OVERRIDE_SEL	R/W	0h	SESSVALID override selector. This has to be set to override sessvalid from PHY to Controller. Reset Source: cfg_srst_n
1	VBUSVALID_OVERRIDE_VAL	R/W	0h	VBUSVALID override value. 1 - VBUS is valid, 0 - VBUS is not valid Reset Source: cfg_srst_n
0	VBUSVALID_OVERRIDE_SEL	R/W	0h	VBUSVALID override selector. This has to be set to override vbusvalid from PHY to Controller. Reset Source: cfg_srst_n

14.9.3.2.2.28 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register

1 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register (Offset = 430h) [reset = 0h]

The IRQ_STATUS_RAW_MISC register allows the usbss interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-27936. Instance Table

Instance Name	Physical Address
USB0	**0F90 0430h**
USB1	**0F91 0430h**

Figure 14-9257. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TS	R	R/W1TS	R			
0h	0h	0h	0h	0h			

15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-27938. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TS	0h	Set when VBUSVALID changes state Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TS	0h	Set when SESSVALID changes state Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.9.3.2.2.29 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register

1 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register (Offset = 434h) [reset = 0h]

The IRQ_STATUS_MISC register allows the usbss interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-27939. Instance Table

Instance Name	Physical Address
USB0	**0F90 0434h**
USB1	**0F91 0434h**

Figure 14-9258. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TC	R	R/W1TC	R			
0h	0h	0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED19_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED19_0							
R							
0h							

Table 14-27941. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TC	0h	Set when VBUSVALID changes state Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TC	0h	Set when SESSVALID changes state Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.9.3.2.2.30 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register

1 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register (Offset = 438h) [reset = 0h]

The IRQ_ENABLE_SET_MISC register allows the usbss interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-27942. Instance Table

Instance Name	Physical Address
USB0	**0F90 0438h**
USB1	**0F91 0438h**

Figure 14-9259. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TS	R	R/W1TS	R			
0h	0h	0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-27944. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TS	0h	Event enable Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TS	0h	Event enable Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.9.3.2.2.31 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register

1 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register (Offset = 43Ch) [reset = 0h]

The IRQ_ENABLE_CLR_MISC register allows the usbss interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-27945. Instance Table

Instance Name	Physical Address
USB0	**0F90 043Ch**
USB1	**0F91 043Ch**

Figure 14-9260. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TC	R	R/W1TC	R			
0h	0h	0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-27947. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TC	0h	Event enable Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TC	0h	Event enable Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.9.3.2.2.32 USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register

1 USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register (Offset = 440h) [reset = 0h]

EOI vector for re-triggering interrupts

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Table 14-27948. Instance Table

Instance Name	Physical Address
USB0	**0F90 0440h**
USB1	**0F91 0440h**

Figure 14-9261. USB2SS_USB2SS_CFG_IRQ_MISC_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-27950. USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	EOI vector for misc interrupt. Has to be written to 0 after ISR services misc interrupt. Reset Source: cfg_srst_n

14.9.3.2.2.33 USB2SS_USB2SS_CFG_INTR_TEST Register

1 USB2SS_USB2SS_CFG_INTR_TEST Register (Offset = 490h) [reset = 0h]

Register for overriding various Controller interrupts for easy activation during DV. NOTE: This is only for internal purposes and should NOT be used during functional operation.

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Table 14-27951. Instance Table

Instance Name	Physical Address
USB0	**0F90 0490h**
USB1	**0F91 0490h**

Figure 14-9262. USB2SS_USB2SS_CFG_INTR_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							HOST_SYSTEM_ERR_TEST
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
IRQ_TEST							
R/W							
0h							

Table 14-27953. USB2SS_USB2SS_CFG_INTR_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	HOST_SYSTEM_ERR_TEST	R/W	0h	Test for host system error interrupt. Set 1 to cause host_system_error_intr to trigger and clear this bit to clear the interrupt condition. Reset Source: cfg_srst_n
7:0	IRQ_TEST	R/W	0h	Test for irq interrupts from core. Each bit sets corresponding irq_intr bit. Set 1 to each bit based on whether that interrupt needs to trigger and clear the bit in ISR to clear interrupt condition. Reset Source: cfg_srst_n

14.9.3.2.2.34 USB2SS_USB2SS_CFG_VBUS_FILTER Register

1 USB2SS_USB2SS_CFG_VBUS_FILTER Register (Offset = 614h) [reset = 104h]

The vbus comparator signals may be filtered by controlling these register values.

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Table 14-27954. Instance Table

Instance Name	Physical Address
USB0	**0F90 0614h**
USB1	**0F91 0614h**

Figure 14-9263. USB2SS_USB2SS_CFG_VBUS_FILTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED31_9</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED31_9</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED31_9</td><td>SESSVALID_BYPASS</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SESSVALID_THRESH</td><td colspan="3">RESERVED5_3</td><td>VBUSVALID_BYPASS</td><td colspan="2">VBUSVALID_THRESH</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">R</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td>1h</td><td colspan="2">0h</td></tr>
</table>

Table 14-27956. USB2SS_USB2SS_CFG_VBUS_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED31_9	R	0h	Reserved bits
8	SESSVALID_BYPASS	R/W	1h	0= use filter, 1= bypass filter Reset Source: cfg_srst_n
7:6	SESSVALID_THRESH	R/W	0h	00= 1us,01= 100us,10= 5ms,11= 50ms. 4 utmi_clk latency for sessvalid Reset Source: cfg_srst_n
5:3	RESERVED5_3	R	0h	Reserved bits
2	VBUSVALID_BYPASS	R/W	1h	0= use filter, 1= bypass filter for vbusvalid Reset Source: cfg_srst_n
1:0	VBUSVALID_THRESH	R/W	0h	00= 1us,01= 100us,10= 5ms,11= 50ms. 4 utmi_clk latency for vbusvalid Reset Source: cfg_srst_n

14.9.3.2.2.35 USB2SS_USB2SS_CFG_VBUS_STAT Register

1 USB2SS_USB2SS_CFG_VBUS_STAT Register (Offset = 618h) [reset = 0h]

Status bits of VBUS detected signals after filter.

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Table 14-27957. Instance Table

Instance Name	Physical Address
USB0	**0F90 0618h**
USB1	**0F91 0618h**

Figure 14-9264. USB2SS_USB2SS_CFG_VBUS_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED31_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED31_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED31_3							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED31_3					SESSVALID	RESERVED1_1	VBUSVALID
R					R	R	R
0h					0h	0h	0h

Table 14-27959. USB2SS_USB2SS_CFG_VBUS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED31_3	R	0h	Reserved bits
2	SESSVALID	R	0h	Filtered SESSVALID Reset Source: cfg_srst_n
1	RESERVED1_1	R	0h	Reserved bits
0	VBUSVALID	R	0h	Filtered VBUSVALID Reset Source: cfg_srst_n

14.9.3.2.2.36 USB2SS_USB2SS_CFG_DEBUG_CFG Register

1 USB2SS_USB2SS_CFG_DEBUG_CFG Register (Offset = 708h) [reset = 0h]

Configuration of debug data for observation. 0x0 or 0x7 = debug outputs are tied low, 0x1 = debug outputs are UTMI interface signals, 0x2 = debug outputs are Controller debug[31:0] output 0x3 = debug outputs are Controller debug[63:32] output, 0x4 = debug outputs are clk_gate_ctrl and debug[66:64] Controller outputs, 0x5 = debug outputs are controller logic_analyzer_trace[31:0], 0x6 = debug outputs are controller logic_analyzer_trace[63:32]

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Table 14-27960. Instance Table

Instance Name	Physical Address
USB0	**0F90 0708h**
USB1	**0F91 0708h**

Figure 14-9265. USB2SS_USB2SS_CFG_DEBUG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED31_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_3							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED31_3					SEL		
R					R/W		
0h					0h		

Table 14-27962. USB2SS_USB2SS_CFG_DEBUG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED31_3	R	0h	Reserved
2:0	SEL	R/W	0h	selection of observed local signals Reset Source: cfg_srst_n

14.9.3.2.2.37 USB2SS_USB2SS_CFG_DEBUG_DATA Register

1 USB2SS_USB2SS_CFG_DEBUG_DATA Register (Offset = 70Ch) [reset = 0h]

Debug data

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Table 14-27963. Instance Table

Instance Name	Physical Address
USB0	**0F90 070Ch**
USB1	**0F91 070Ch**

Figure 14-9266. USB2SS_USB2SS_CFG_DEBUG_DATA Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-27965. USB2SS_USB2SS_CFG_DEBUG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	tmp Reset Source: cfg_srst_n

14.9.3.2.2.38 USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register

1 USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register (Offset = 714h) [reset = 2h]

The HOST_HUB_CTRL Register is a collection of various input signals that control the xHC controllers Host or Hub interfaces. These signals are used regardless if a Host or Hub is implemented or not.

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Table 14-27966. Instance Table

Instance Name	Physical Address
USB0	**0F90 0714h**
USB1	**0F91 0714h**

Figure 14-9267. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RSVD3</td><td colspan="2">BUS_FILTER_BYPASS</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">BUS_FILTER_BYPASS</td><td>HUB_PORT_PERM_ATTACH</td><td colspan="3">RSVD2</td><td>HOST_PORT_POWER_CONTROL_PRESENT</td><td>RSVD1</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="3">R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="3">0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-27968. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RSVD3	R	0h	Reserved bits Reset Source: cfg_srst_n
9:6	BUS_FILTER_BYPASS	R/W	0h	Bus Filter Bypass bit [0]: bypass the filter for vbusvalid bit bit [2]: bypass the filter for sessvalid Reset Source: cfg_srst_n
5	HUB_PORT_PERM_ATTACH	R/W	0h	Indicates if the device attached to a downstream port is permanently attached or not. Bit 6 is the USB2 port and bit 7 is the SS port. 0 - Not permanently attached 1 - Permanently attached Reset Source: cfg_srst_n
4:2	RSVD2	R	0h	Reserved bits Reset Source: cfg_srst_n

Table 14-27968. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HOST_PORT_POWER_CONTROL_PRESENT	R/W	1h	This port defines the bit [3] of Capability Parameters (HCCPARAMS). Change the PPC value through the pin Port Power Control (PPC). This indicates whether the host controller implementation includes port power control. 0 - Indicates that the port does not have port power switches. 1 - Indicates that the port has port power switches. Reset Source: cfg_srst_n
0	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n

14.9.3.2.2.39 USB2SS_PHY2_AFE_TX_REG0 Register

1 USB2SS_PHY2_AFE_TX_REG0 Register (Offset = 0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-27969. Instance Table

Instance Name	Physical Address
USB0	**0F90 8000h**
USB1	**0F91 8000h**

Figure 14-9268. USB2SS_PHY2_AFE_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG0	BF_6_2					BF_1	BF_0
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-27971. USB2SS_PHY2_AFE_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:2	BF_6_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	BF_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.40 USB2SS_PHY2_AFE_TX_REG1 Register

1 USB2SS_PHY2_AFE_TX_REG1 Register (Offset = 4h) [reset = 0h]

HS TX trimming

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Table 14-27972. Instance Table

Instance Name	Physical Address
USB0	**0F90 8004h**
USB1	**0F91 8004h**

Figure 14-9269. USB2SS_PHY2_AFE_TX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_ANA_REG1	BF_6_1						BF_0
R/W	R/W						R/W
0h	0h						0h

Table 14-27974. USB2SS_PHY2_AFE_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG1	R/W	0h	0 SCALE1 VALUE IS 0, 1 SCALE1 VALUE IS 0.5 Reset Source: usb2_sync_preset_n

Table 14-27974. USB2SS_PHY2_AFE_TX_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:1	BF_6_1	R/W	0h	000000 BOOST CODE VALUE IS 0, 000001 BOOST CODE VALUE IS 1, 000010 BOOST CODE VALUE IS 2, 00011 BOOST CODE VALUE IS 3, 000100 BOOST CODE VALUE IS 4, 000101 BOOST CODE VALUE IS 5, 000110 BOOST CODE VALUE IS 6, 000111 BOOST CODE VALUE IS 7, 001000 BOOST CODE VALUE IS 8, 001001 BOOST CODE VALUE IS 9, 001010 BOOST CODE VALUE IS 10, 001011 BOOST CODE VALUE IS 11, 001100 BOOST CODE VALUE IS 12, 001101 BOOST CODE VALUE IS 13, 001110 BOOST CODE VALUE IS 14, 001111 BOOST CODE VALUE IS 15, 010000 BOOST CODE VALUE IS 16, 010001 BOOST CODE VALUE IS 17, 010010 BOOST CODE VALUE IS 18, 010011 BOOST CODE VALUE IS 19, 010100 BOOST CODE VALUE IS 20, 010101 BOOST CODE VALUE IS 21, 010110 BOOST CODE VALUE IS 22, 010111 BOOST CODE VALUE IS 23, 011000 BOOST CODE VALUE IS 24, 011001 BOOST CODE VALUE IS 24, 011010 BOOST CODE VALUE IS 26, 011011 BOOST CODE VALUE IS 27, 011100 BOOST CODE VALUE IS 28, 011101 BOOST CODE VALUE IS 29, 011110 BOOST CODE VALUE IS 30, 011111 BOOST CODE VALUE IS 31, 100000 BOOST CODE VALUE IS 16, 100001 BOOST CODE VALUE IS 17, 100010 BOOST CODE VALUE IS 18, 100011 BOOST CODE VALUE IS 19, 100100 BOOST CODE VALUE IS 20, 100101 BOOST CODE VALUE IS 21, 100110 BOOST CODE VALUE IS 22, 100111 BOOST CODE VALUE IS 23, 101000 BOOST CODE VALUE IS 24 , 101001 BOOST CODE VALUE IS 24, 101010 BOOST CODE VALUE IS 26, 101011 BOOST CODE VALUE IS 27, 101100 BOOST CODE VALUE IS 28, 101101 BOOST CODE VALUE IS 29, 101110 BOOST CODE VALUE IS 30, 101111 BOOST CODE VALUE IS 31, 110000 BOOST CODE VALUE IS 32, 110001 BOOST CODE VALUE IS 33, 110010 BOOST CODE VALUE IS 34, 110011 BOOST CODE VALUE IS 35, 110100 BOOST CODE VALUE IS 36, 110101 BOOST CODE VALUE IS 37, 110110 BOOST CODE VALUE IS 38, 110111 BOOST CODE VALUE IS 39, 111000 BOOST CODE VALUE IS 40, 111001 BOOST CODE VALUE IS 41, 111010 BOOST CODE VALUE IS 42, 111011 BOOST CODE VALUE IS 43, 111100 BOOST CODE VALUE IS 44, 111101 BOOST CODE VALUE IS 45, 111110 BOOST CODE VALUE IS 46, 111111 BOOST CODE VALUE IS 47. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default BOOST CODE = 8, 1 BOOST CODE can be controlled by BITS [6:1]. Reset Source: usb2_sync_preset_n

14.9.3.2.2.41 USB2SS_PHY2_AFE_TX_REG2 Register

1 USB2SS_PHY2_AFE_TX_REG2 Register (Offset = 8h) [reset = 0h]

HS TX trimming

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Table 14-27975. Instance Table

Instance Name	Physical Address
USB0	**0F90 8008h**
USB1	**0F91 8008h**

Figure 14-9270. USB2SS_PHY2_AFE_TX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG2	BF_6	BF_5_1					BF_0
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-27977. USB2SS_PHY2_AFE_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-27977. USB2SS_PHY2_AFE_TX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:1	BF_5_1	R/W	0h	00000 DEEMP CODE VALUE IS 0, 00001 DEEMP CODE VALUE IS 1, 00010 DEEMP CODE VALUE IS 2, 00011 DEEMP CODE VALUE IS 3, 00100 DEEMP CODE VALUE IS 4, 00101 DEEMP CODE VALUE IS 5, 00110 DEEMP CODE VALUE IS 6, 00111 DEEMP CODE VALUE IS 7, 01000 DEEMP CODE VALUE IS 8, 01001 DEEMP CODE VALUE IS 9, 01010 DEEMP CODE VALUE IS 10, 01011 DEEMP CODE VALUE IS 11, 01100 DEEMP CODE VALUE IS 12, 01101 DEEMP CODE VALUE IS 13, 01110 DEEMP CODE VALUE IS 14, 01111 DEEMP CODE VALUE IS 15, 10000 DEEMP CODE VALUE IS 8, 10001 DEEMP CODE VALUE IS 9, 10010 DEEMP CODE VALUE IS 10, 10011 DEEMP CODE VALUE IS 11, 10100 DEEMP CODE VALUE IS 12, 10101 DEEMP CODE VALUE IS 13, 10110 DEEMP CODE VALUE IS 14, 10111 DEEMP CODE VALUE IS 15, 11000 DEEMP CODE VALUE IS 16, 11001 DEEMP CODE VALUE IS 17, 11010 DEEMP CODE VALUE IS 18, 11011 DEEMP CODE VALUE IS 19, 11100 DEEMP CODE VALUE IS 20, 11101 DEEMP CODE VALUE IS 21, 11110 DEEMP CODE VALUE IS 22, 11111 DEEMP CODE VALUE IS 23. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default DEEMP CODE = 8, 1 DEEMP CODE can be controlled by BITS 5:1. Reset Source: usb2_sync_preset_n

14.9.3.2.2.42 USB2SS_PHY2_AFE_TX_REG3 Register

1 USB2SS_PHY2_AFE_TX_REG3 Register (Offset = Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-27978. Instance Table

Instance Name	Physical Address
USB0	**0F90 800Ch**
USB1	**0F91 800Ch**

Figure 14-9271. USB2SS_PHY2_AFE_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_ANA_REG3			BF_4_1				BF_0
R/W			R/W				R/W
0h			0h				0h

Table 14-27980. USB2SS_PHY2_AFE_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	TX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.43 USB2SS_PHY2_AFE_TX_REG4 Register

1 USB2SS_PHY2_AFE_TX_REG4 Register (Offset = 10h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-27981. Instance Table

Instance Name	Physical Address
USB0	**0F90 8010h**
USB1	**0F91 8010h**

Figure 14-9272. USB2SS_PHY2_AFE_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG4	BF_6	BF_5	BF_4_1				BF_0
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-27983. USB2SS_PHY2_AFE_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.44 USB2SS_PHY2_AFE_TX_REG5 Register

1 USB2SS_PHY2_AFE_TX_REG5 Register (Offset = 14h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-27984. Instance Table

Instance Name	Physical Address
USB0	**0F90 8014h**
USB1	**0F91 8014h**

Figure 14-9273. USB2SS_PHY2_AFE_TX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_TX_REG5	BF_6_1						BF_0
R/W	R/W						R/W
0h	0h						0h

Table 14-27986. USB2SS_PHY2_AFE_TX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AFE_TX_REG5	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6:1	BF_6_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.45 USB2SS_PHY2_AFE_TX_REG6 Register

1 USB2SS_PHY2_AFE_TX_REG6 Register (Offset = 18h) [reset = 0h]

LSTX rise time trimming

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Table 14-27987. Instance Table

Instance Name	Physical Address
USB0	**0F90 8018h**
USB1	**0F91 8018h**

Figure 14-9274. USB2SS_PHY2_AFE_TX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG6							
R/W							
0h							

Table 14-27989. USB2SS_PHY2_AFE_TX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG6	R/W	0h	Bit 7 = unused. Bbits 6:3= 0000 Typical LSTx rise time = 375ns, 0001 Typical LSTx rise time =215ns, 0010 Typical LSTx rise time =215ns, 0011 Typical LSTx rise time =150ns, 0100 Typical LSTx rise time =215ns, 0101 Typical LSTx rise time =150ns, 0110 Typical LSTx rise time =150ns, 0111 Typical LSTx rise time =115ns, 1000 Typical LSTx rise time =150ns, 1001 Typical LSTx rise time =115ns, 1010 Typical LSTx rise time =115ns, 1011 Typical LSTx rise time =94ns, 1100 Typical LSTx rise time =115ns, 1101 Typical LSTx rise time =94ns, 1110 Typical LSTx rise time =94ns, 1111 Typical LSTx rise time =79ns. Bit 6= 0 Typical LSTx rise time is set to default value of 150ns, 1 LSTX RISE TIME IS DETERMINED BY BITS 6:2. Bits 1:0 = reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.46 USB2SS_PHY2_AFE_TX_REG7 Register

1 USB2SS_PHY2_AFE_TX_REG7 Register (Offset = 1Ch) [reset = 0h]

FSTX rise time trimming

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Table 14-27990. Instance Table

Instance Name	Physical Address
USB0	**0F90 801Ch**
USB1	**0F91 801Ch**

Figure 14-9275. USB2SS_PHY2_AFE_TX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG7							
R/W							
0h							

Table 14-27992. USB2SS_PHY2_AFE_TX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG7	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx rise time = 16.6ns, 0001 Typical FSTx rise time =16.1ns, 0010 Typical FSTx rise time =15.6ns, 0011 Typical FSTx rise time =15.2ns, 0100 Typical FSTx rise time =14.7ns, 0101 Typical FSTx rise time =14.3ns, 0110 Typical FSTx rise time =13.9ns, 0111 Typical FSTx rise time =13.6ns, 1000 Typical FSTx rise time =13.2ns, 1001 Typical FSTx rise time =12.9ns, 1010 Typical FSTx rise time =12.6ns, 1011 Typical FSTx rise time =12.3ns, 1100 Typical FSTx rise time =12.0ns, 1101 Typical FSTx rise time =11.7ns, 1110 Typical FSTx rise time =11.5ns, 1111 Typical FSTx rise time =11.2ns. Bit 0= 0 FSTx rise time at typical corner is set to default value of 12ns, 1 FSTX RISE TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.9.3.2.2.47 USB2SS_PHY2_AFE_TX_REG8 Register

1 USB2SS_PHY2_AFE_TX_REG8 Register (Offset = 20h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-27993. Instance Table

Instance Name	Physical Address
USB0	**0F90 8020h**
USB1	**0F91 8020h**

Figure 14-9276. USB2SS_PHY2_AFE_TX_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG8							
R/W							
0h							

Table 14-27995. USB2SS_PHY2_AFE_TX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG8	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.48 USB2SS_PHY2_AFE_TX_REG9 Register

1 USB2SS_PHY2_AFE_TX_REG9 Register (Offset = 24h) [reset = 0h]

Register AFE_TX_REG9

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Table 14-27996. Instance Table

Instance Name	Physical Address
USB0	**0F90 8024h**
USB1	**0F91 8024h**

Figure 14-9277. USB2SS_PHY2_AFE_TX_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG9							
R/W							
0h							

Table 14-27998. USB2SS_PHY2_AFE_TX_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG9	R/W	0h	Bits 7:4= 0000 Typical LSTx fall time = 450ns, 0001 Typical LSTx fall time = 225ns, 0010 Typical LSTx fall time =150ns, 0011 Typical LSTx fall time =225ns, 0100 Typical LSTx fall time =150ns, 0101 Typical LSTx fall time =150ns, 0110 Typical LSTx fall time =112ns, 0111 Typical LSTx fall time =150ns, 1000 Typical LSTx fall time =112ns, 1001 Typical LSTx fall time =112ns, 1010 Typical LSTx fall time =90ns, 1011 Typical LSTx fall time =112ns, 1100 Typical LSTx fall time =90ns, 1101 Typical LSTx fall time =90ns, 1110 Typical LSTx fall time =75ns, 1111 Typical LSTx fall time = 150ns. bit 3 = 0 LSTX FALL TIME IS DETERMINED BY DESIGN, 1 LSTX FALL TIME IS DETERMINED BY BITS 7:4. Bits 2:1= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.49 USB2SS_PHY2_AFE_TX_REG10 Register

1 USB2SS_PHY2_AFE_TX_REG10 Register (Offset = 28h) [reset = 0h]

FSTX fall time trimming

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Table 14-27999. Instance Table

Instance Name	Physical Address
USB0	**0F90 8028h**
USB1	**0F91 8028h**

Figure 14-9278. USB2SS_PHY2_AFE_TX_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG10							
R/W							
0h							

Table 14-28001. USB2SS_PHY2_AFE_TX_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG10	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx fall time = 16.6ns, 0001 Typical FSTx fall time =16.1ns, 0010 Typical FSTx fall time =15.6ns, 0011 Typical FSTx fall time =15.2ns, 0100 Typical FSTx fall time =14.7ns, 0101 Typical FSTx fall time =14.3ns, 0110 Typical FSTx fall time =13.9ns, 0111 Typical FSTx fall time =13.6ns, 1000 Typical FSTx fall time =13.2ns, 1001 Typical FSTx fall time =12.9ns, 1010 Typical FSTx fall time =12.6ns, 1011 Typical FSTx fall time =12.3ns, 1100 Typical FSTx fall time =12ns, 1101 Typical FSTx fall time =11.7, 1110 Typical FSTx fall time =11.5ns, 1111 Typical FSTx fall time =11.2ns. bit 0 = 0 Typical FSTx fall time set to default value of 12ns, 1 FSTX fall TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.9.3.2.2.50 USB2SS_PHY2_AFE_TX_REG11 Register

1 USB2SS_PHY2_AFE_TX_REG11 Register (Offset = 2Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28002. Instance Table

Instance Name	Physical Address
USB0	**0F90 802Ch**
USB1	**0F91 802Ch**

Figure 14-9279. USB2SS_PHY2_AFE_TX_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG11							
R/W							
0h							

Table 14-28004. USB2SS_PHY2_AFE_TX_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG11	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.51 USB2SS_PHY2_AFE_TX_REG12 Register

1 USB2SS_PHY2_AFE_TX_REG12 Register (Offset = 30h) [reset = 0h]

Register AFE_TX_REG12

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Table 14-28005. Instance Table

Instance Name	Physical Address
USB0	**0F90 8030h**
USB1	**0F91 8030h**

Figure 14-9280. USB2SS_PHY2_AFE_TX_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG12	BF_6	BF_5	BF_4	BF_3	BF_2	BF_1_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-28007. USB2SS_PHY2_AFE_TX_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG12	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BF_4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BF_3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BF_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28007. USB2SS_PHY2_AFE_TX_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	BF_1_0	R/W	0h	00- SCALE2 set to 0, 01- SCALE2 set to 1, 10- SCALE2 set to 1, 11- SCALE2 set to 2 Reset Source: usb2_sync_preset_n

14.9.3.2.2.52 USB2SS_PHY2_AFE_RX_REG0 Register

1 USB2SS_PHY2_AFE_RX_REG0 Register (Offset = 34h) [reset = 0h]

Trim the squelch threshold

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Table 14-28008. Instance Table

Instance Name	Physical Address
USB0	**0F90 8034h**
USB1	**0F91 8034h**

Figure 14-9281. USB2SS_PHY2_AFE_RX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG0							
R/W							
0h							

Table 14-28010. USB2SS_PHY2_AFE_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG0	R/W	0h	Bits 7:6= reserved. Bits 5:0= 000000 keep squelch threshold at default value, 100000 increade squelch threshold by 5mv, 110000 increade squelch threshold by 10mv, 111000 increade squelch threshold by 15mv, 000001 reduce squelch threshold by 5mv, 000011 reduce squelch threshold by 10mv, 000111 reduce squelch threshold by 15mv. Reset Source: usb2_sync_preset_n

14.9.3.2.2.53 USB2SS_PHY2_AFE_RX_REG1 Register

1 USB2SS_PHY2_AFE_RX_REG1 Register (Offset = 38h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28011. Instance Table

Instance Name	Physical Address
USB0	**0F90 8038h**
USB1	**0F91 8038h**

Figure 14-9282. USB2SS_PHY2_AFE_RX_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_ANA_REG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28013. USB2SS_PHY2_AFE_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.54 USB2SS_PHY2_AFE_RX_REG2 Register

1 USB2SS_PHY2_AFE_RX_REG2 Register (Offset = 3Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28014. Instance Table

Instance Name	Physical Address
USB0	**0F90 803Ch**
USB1	**0F91 803Ch**

Figure 14-9283. USB2SS_PHY2_AFE_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG2							
R/W							
0h							

Table 14-28016. USB2SS_PHY2_AFE_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG2	R/W	0h	reerved Reset Source: usb2_sync_preset_n

14.9.3.2.2.55 USB2SS_PHY2_AFE_RX_REG3 Register

1 USB2SS_PHY2_AFE_RX_REG3 Register (Offset = 40h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28017. Instance Table

Instance Name	Physical Address
USB0	**0F90 8040h**
USB1	**0F91 8040h**

Figure 14-9284. USB2SS_PHY2_AFE_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG3							
R/W							
0h							

Table 14-28019. USB2SS_PHY2_AFE_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.56 USB2SS_PHY2_AFE_RX_REG4 Register

1 USB2SS_PHY2_AFE_RX_REG4 Register (Offset = 44h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28020. Instance Table

Instance Name	Physical Address
USB0	**0F90 8044h**
USB1	**0F91 8044h**

Figure 14-9285. USB2SS_PHY2_AFE_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG4							
R/W							
0h							

Table 14-28022. USB2SS_PHY2_AFE_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.57 USB2SS_PHY2_AFE_RX_REG5 Register

1 USB2SS_PHY2_AFE_RX_REG5 Register (Offset = 48h) [reset = 0h]

Single ended receivers threshold trimming

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Table 14-28023. Instance Table

Instance Name	Physical Address
USB0	**0F90 8048h**
USB1	**0F91 8048h**

Figure 14-9286. USB2SS_PHY2_AFE_RX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG5							
R/W							
0h							

Table 14-28025. USB2SS_PHY2_AFE_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG5	R/W	0h	Bits 7:3= reserved. Bits 2:1= 01 Switching thresholds for single ended receivers increased by 100mV, 10 Switching thresholds for single ended receivers reduced by 100mV. Bit 0= 0 Default Switching Thresholds for Single ended receivers, 1 SERx Switching Thresholds are controlled by bits [2:1]. Reset Source: usb2_sync_preset_n

14.9.3.2.2.58 USB2SS_PHY2_AFE_RX_REG6 Register

1 USB2SS_PHY2_AFE_RX_REG6 Register (Offset = 4Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28026. Instance Table

Instance Name	Physical Address
USB0	**0F90 804Ch**
USB1	**0F91 804Ch**

Figure 14-9287. USB2SS_PHY2_AFE_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG6							
R/W							
0h							

Table 14-28028. USB2SS_PHY2_AFE_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.59 USB2SS_PHY2_AFE_TX_REG13 Register

1 USB2SS_PHY2_AFE_TX_REG13 Register (Offset = 50h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28029. Instance Table

Instance Name	Physical Address
USB0	**0F90 8050h**
USB1	**0F91 8050h**

Figure 14-9288. USB2SS_PHY2_AFE_TX_REG13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_ANA_REG13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28031. USB2SS_PHY2_AFE_TX_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG13	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.60 USB2SS_PHY2_AFE_TX_REG14 Register

1 USB2SS_PHY2_AFE_TX_REG14 Register (Offset = 54h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28032. Instance Table

Instance Name	Physical Address
USB0	**0F90 8054h**
USB1	**0F91 8054h**

Figure 14-9289. USB2SS_PHY2_AFE_TX_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG14							
R							
0h							

Table 14-28034. USB2SS_PHY2_AFE_TX_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG14	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.61 USB2SS_PHY2_AFE_RX_REG7 Register

1 USB2SS_PHY2_AFE_RX_REG7 Register (Offset = 58h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28035. Instance Table

Instance Name	Physical Address
USB0	**0F90 8058h**
USB1	**0F91 8058h**

Figure 14-9290. USB2SS_PHY2_AFE_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG7							
R							
0h							

Table 14-28037. USB2SS_PHY2_AFE_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.62 USB2SS_PHY2_AFE_RX_REG8 Register

1 USB2SS_PHY2_AFE_RX_REG8 Register (Offset = 5Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28038. Instance Table

Instance Name	Physical Address
USB0	**0F90 805Ch**
USB1	**0F91 805Ch**

Figure 14-9291. USB2SS_PHY2_AFE_RX_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG8							
R							
0h							

Table 14-28040. USB2SS_PHY2_AFE_RX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.63 USB2SS_PHY2_AFE_UNUSED_REG0 Register

1 USB2SS_PHY2_AFE_UNUSED_REG0 Register (Offset = 60h) [reset = 0h]

AFE_UNUSED_REG0

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Table 14-28041. Instance Table

Instance Name	Physical Address
USB0	**0F90 8060h**
USB1	**0F91 8060h**

Figure 14-9292. USB2SS_PHY2_AFE_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG0							
R/W							
0h							

Table 14-28043. USB2SS_PHY2_AFE_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG0	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.64 USB2SS_PHY2_AFE_UNUSED_REG1 Register

1 USB2SS_PHY2_AFE_UNUSED_REG1 Register (Offset = 64h) [reset = 0h]

AFE_UNUSED_REG1

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Table 14-28044. Instance Table

Instance Name	Physical Address
USB0	**0F90 8064h**
USB1	**0F91 8064h**

Figure 14-9293. USB2SS_PHY2_AFE_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG1							
R/W							
0h							

Table 14-28046. USB2SS_PHY2_AFE_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG1	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.65 USB2SS_PHY2_AFE_BG_REG0 Register

1 USB2SS_PHY2_AFE_BG_REG0 Register (Offset = 80h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28047. Instance Table

Instance Name	Physical Address
USB0	**0F90 8080h**
USB1	**0F91 8080h**

Figure 14-9294. USB2SS_PHY2_AFE_BG_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG0							
R/W							
0h							

Table 14-28049. USB2SS_PHY2_AFE_BG_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.66 USB2SS_PHY2_AFE_BG_REG1 Register

1 USB2SS_PHY2_AFE_BG_REG1 Register (Offset = 84h) [reset = 0h]

BG bias current trimming

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Table 14-28050. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 8084h**
USB1	**0F91 8084h**

Figure 14-9295. USB2SS_PHY2_AFE_BG_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG1							
R/W							
0h							

Table 14-28052. USB2SS_PHY2_AFE_BG_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG1	R/W	0h	Bits 7:6= 00- PLL charge pump bias current 5uA, 01- PLL charge pump bias current 4uA, 10- PLL charge pump bias current 6uA, 11- PLL charge pump bias current 5uA. Bits 5:4= 00- PLL DAC bias bias current bias current 5uA, 01- PLL DAC bias bias current bias current 4uA, 10- PLL DAC bias current current 6uA, 11- PLL DAC bias current current 5uA. Bits 3:2= 00- PLL DAC cascode bias current current 5uA, 01- PLL DAC cascode bias current current 4uA, 10- PLL DAC cascode bias current current 6uA, 11- PLL DAC cascode bias current current 5uA. Bits 1:0= 00- OTG block bias current 5uA, 01- OTG block bias current 6uA, 10- OTG block bias current 6uA, 11- OTG block bias current 5uA. Reset Source: usb2_sync_preset_n

14.9.3.2.2.67 USB2SS_PHY2_AFE_BG_REG2 Register

1 USB2SS_PHY2_AFE_BG_REG2 Register (Offset = 88h) [reset = 0h]

BG bias current trimming

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Table 14-28053. Instance Table

Instance Name	Physical Address
USB0	**0F90 8088h**
USB1	**0F91 8088h**

Figure 14-9296. USB2SS_PHY2_AFE_BG_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG2							
R/W							
0h							

Table 14-28055. USB2SS_PHY2_AFE_BG_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG2	R/W	0h	Bits 7:5= 000 High speed receiver bias 5uA, 100 High speed receiver bias 1uA, 001 High speed receiver bias 4uA, 010 High speed receiver bias 6uA, 101 High speed receiver bias 2uA. Bits 4:2= 000 Trasmission Envelope Detector bias current 5uA, 100 Trasmission Envelope Detector bias current 1uA, 001 Trasmission Envelope Detector bias current 4uA, 101 Trasmission Envelope Detector bias current 6uA, 101 Trasmission Envelope Detector bias current 2uA. Bits 1:0=00 PLL LDO bias current 5uA, 01 PLL LDO bias current 6uA, 10 PLL LDO bias current 4uA, 11 PLL LDO bias current 5uA Reset Source: usb2_sync_preset_n

14.9.3.2.2.68 USB2SS_PHY2_AFE_BG_REG3 Register

1 USB2SS_PHY2_AFE_BG_REG3 Register (Offset = 8Ch) [reset = 2h]

Register AFE_BG_REG3

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Table 14-28056. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 808Ch**
USB1	**0F91 808Ch**

Figure 14-9297. USB2SS_PHY2_AFE_BG_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG3							
R/W							
2h							

Table 14-28058. USB2SS_PHY2_AFE_BG_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG3	R/W	2h	Bits 7:6= reserved, Bits 5:4= 00 [Default] BG_OK_CORE Generated Internally, 01 BG_OK_CORE Generated Internally, 10 Force BG_OK_CORE =0, 11 Force BG_OK_CORE =1. Bits 3:0=0000 Invalid state, 0001 Higher start sense voltage, weaker start-up pull down, 0010 Default start sense voltage, 0100 Low start sense voltage, strong start-up pull down, 1000 Lowest start sense voltage, strongest start-up pull down. Reset Source: usb2_sync_preset_n

14.9.3.2.2.69 USB2SS_PHY2_AFE_CALIB_REG0 Register

1 USB2SS_PHY2_AFE_CALIB_REG0 Register (Offset = 90h) [reset = 0h]

Calibration resistance trimming

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Table 14-28059. Instance Table

Instance Name	Physical Address
USB0	**0F90 8090h**
USB1	**0F91 8090h**

Figure 14-9298. USB2SS_PHY2_AFE_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ANA_REG0							
R/W							
0h							

Table 14-28061. USB2SS_PHY2_AFE_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG0	R/W	0h	Bits 5:0= 000000 Calibrate termination resistor to default value, 000001 Calibrate termination resistor by -%5 to default value, 000011 Calibrate termination resistor by -%10 to default value, 000111 Calibrate termination resistor by - %15 to default value, 001000 Calibrate termination resistor by +5% to default value, 011000 Calibrate termination resistor by +10% to default value, 111000 Calibrate termination resistor by +15% to default value. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.70 USB2SS_PHY2_AFE_BC_REG0 Register

1 USB2SS_PHY2_AFE_BC_REG0 Register (Offset = 94h) [reset = 0h]

register AFE_BC_REG0

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Table 14-28062. Instance Table

Instance Name	Physical Address
USB0	**0F90 8094h**
USB1	**0F91 8094h**

Figure 14-9299. USB2SS_PHY2_AFE_BC_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG0							
R/W							
0h							

Table 14-28064. USB2SS_PHY2_AFE_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

Table 14-28064. USB2SS_PHY2_AFE_BC_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	BC_ANA_REG0	R/W	0h	Bit 0= 0 Battery_charging_DAC_RES_CALIB CODE CANNOT BE CONTROLLED BY ANALOG TEST BITS, 1 Battery_charging_DAC_RES_CALIB CODE CAN BE CONTROLLED BY ANALOG TEST BITS. Bits 5:1= 00000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 0, 00001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 1, 00010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 2, 00011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 3, 00100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 4, 00101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 5, 00110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 6, 00111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 7, 01000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 8, 01001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 9, 01010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 10, 01011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 11, 01100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 12, 01101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 13, 01110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 14, 01111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 15, 10000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 16, 10001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 17, 10010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 18, 10011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 19, 10100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 20, 10101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 21, 10110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 22, 10111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 23, 11000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 26, 11011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 27, 11100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 28, 11101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 29, 11110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 30, 11111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 31. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.71 USB2SS_PHY2_AFE_BC_REG1 Register

1 USB2SS_PHY2_AFE_BC_REG1 Register (Offset = 98h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28065. Instance Table

Instance Name	Physical Address
USB0	**0F90 8098h**
USB1	**0F91 8098h**

Figure 14-9300. USB2SS_PHY2_AFE_BC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG1							
R/W							
0h							

Table 14-28067. USB2SS_PHY2_AFE_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.72 USB2SS_PHY2_AFE_BC_REG2 Register

1 USB2SS_PHY2_AFE_BC_REG2 Register (Offset = 9Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28068. Instance Table

Instance Name	Physical Address
USB0	**0F90 809Ch**
USB1	**0F91 809Ch**

Figure 14-9301. USB2SS_PHY2_AFE_BC_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BC_ANA_REG2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28070. USB2SS_PHY2_AFE_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.73 USB2SS_PHY2_AFE_BC_REG3 Register

1 USB2SS_PHY2_AFE_BC_REG3 Register (Offset = A0h) [reset = 0h]

Register AFE_BC_REG3

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Table 14-28071. Instance Table

Instance Name	Physical Address
USB0	**0F90 80A0h**
USB1	**0F91 80A0h**

Figure 14-9302. USB2SS_PHY2_AFE_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG3							
R/W							
0h							

Table 14-28073. USB2SS_PHY2_AFE_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG3	R/W	0h	Bit 0= 0 Do not overdrive SESS_VLD comparator enable signal, 1 Overdrive SESS_VLD comparator enable signal. Bit 1= 0 SESS_VLD comparator disabled, 1 SESS_VLD comparator enabled. Bit 2= 0 Do not overdrive VBUS_VLD comparator enable signal, 1 Overdrive VBUS_VLD comparator enable signal. Bit 3= 0 VBUS_VLD comparator disabled, 1 VBUS_VLD comparator enabled. Bit 4= 0 Do not overdrive ID comparator enable signal, 1 Overdrive ID comparator enable signal. Bit 5= 0 ID comparator disabled, 1 ID comparator enabled. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.74 USB2SS_PHY2_AFE_BC_REG4 Register

1 USB2SS_PHY2_AFE_BC_REG4 Register (Offset = A4h) [reset = 0h]

Register AFE_BC_REG4

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Table 14-28074. Instance Table

Instance Name	Physical Address
USB0	**0F90 80A4h**
USB1	**0F91 80A4h**

Figure 14-9303. USB2SS_PHY2_AFE_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG4							
R/W							
0h							

Table 14-28076. USB2SS_PHY2_AFE_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG4	R/W	0h	Bits 2:0= reserved. Bit 3= 0- VBUS_VLD comparator output low, 1- VBUS_VLD comparator output high. Bit 4= 0- Do not overdrive VBUS_VLD comparator output, 1- Overdrive VBUS_VLD comparator output. Bit 5= 0- SESS_VLD comparator output low, 1- SESS_VLD comparator output high. Bit 6= 0- Do not overdrive SESS_VLD comparator output, 1- Overdrive SESS_VLD comparator output. Bit 7= 0- ID comparator output low, 1- ID comparator output high. Reset Source: usb2_sync_preset_n

14.9.3.2.2.75 USB2SS_PHY2_AFE_BC_REG5 Register

1 USB2SS_PHY2_AFE_BC_REG5 Register (Offset = A8h) [reset = 0h]

Register AFE_BC_REG5

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Table 14-28077. Instance Table

Instance Name	Physical Address
USB0	**0F90 80A8h**
USB1	**0F91 80A8h**

Figure 14-9304. USB2SS_PHY2_AFE_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG5							
R/W							
0h							

Table 14-28079. USB2SS_PHY2_AFE_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG5	R/W	0h	Bit 0= 0- Do not overdrive ID comparator output, 1- Overdrive ID comparator output. Bit 1= 0 Do not overdrive VBUS_DIV signal, 1- Overdrive VBUS_DIV signal. Bit 2= 0- VBUS_DIV signal low, 1- VBUS_DIV signal high. Bits 7:3= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.76 USB2SS_PHY2_AFE_BC_REG6 Register

1 USB2SS_PHY2_AFE_BC_REG6 Register (Offset = ACh) [reset = 0h]

Register AFE_BC_REG6

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Table 14-28080. Instance Table

Instance Name	Physical Address
USB0	**0F90 80ACh**
USB1	**0F91 80ACh**

Figure 14-9305. USB2SS_PHY2_AFE_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG6							
R/W							
0h							

Table 14-28082. USB2SS_PHY2_AFE_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG6	R/W	0h	register AFE_BC_REG6 Reset Source: usb2_sync_preset_n

14.9.3.2.2.77 USB2SS_PHY2_AFE_PLL_REG0 Register

1 USB2SS_PHY2_AFE_PLL_REG0 Register (Offset = B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28083. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B0h**
USB1	**0F91 80B0h**

Figure 14-9306. USB2SS_PHY2_AFE_PLL_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG0							
R/W							
0h							

Table 14-28085. USB2SS_PHY2_AFE_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.78 USB2SS_PHY2_AFE_PLL_REG1 Register

1 USB2SS_PHY2_AFE_PLL_REG1 Register (Offset = B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28086. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B4h**
USB1	**0F91 80B4h**

Figure 14-9307. USB2SS_PHY2_AFE_PLL_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG1							
R/W							
0h							

Table 14-28088. USB2SS_PHY2_AFE_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.79 USB2SS_PHY2_AFE_PLL_REG2 Register

1 USB2SS_PHY2_AFE_PLL_REG2 Register (Offset = B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28089. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B8h**
USB1	**0F91 80B8h**

Figure 14-9308. USB2SS_PHY2_AFE_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG2							
R/W							
0h							

Table 14-28091. USB2SS_PHY2_AFE_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.80 USB2SS_PHY2_AFE_PLL_REG3 Register

1 USB2SS_PHY2_AFE_PLL_REG3 Register (Offset = BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28092. Instance Table

Instance Name	Physical Address
USB0	**0F90 80BCh**
USB1	**0F91 80BCh**

Figure 14-9309. USB2SS_PHY2_AFE_PLL_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">AFE_PLL_REG3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28094. USB2SS_PHY2_AFE_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.81 USB2SS_PHY2_AFE_PLL_REG4 Register

1 USB2SS_PHY2_AFE_PLL_REG4 Register (Offset = C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28095. Instance Table

Instance Name	Physical Address
USB0	**0F90 80C0h**
USB1	**0F91 80C0h**

Figure 14-9310. USB2SS_PHY2_AFE_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG4							
R/W							
0h							

Table 14-28097. USB2SS_PHY2_AFE_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.82 USB2SS_PHY2_AFE_PLL_REG5 Register

1 USB2SS_PHY2_AFE_PLL_REG5 Register (Offset = C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28098. Instance Table

Instance Name	Physical Address
USB0	**0F90 80C4h**
USB1	**0F91 80C4h**

Figure 14-9311. USB2SS_PHY2_AFE_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG5							
R/W							
0h							

Table 14-28100. USB2SS_PHY2_AFE_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.83 USB2SS_PHY2_AFE_BG_REG4 Register

1 USB2SS_PHY2_AFE_BG_REG4 Register (Offset = C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28101. Instance Table

Instance Name	Physical Address
USB0	**0F90 80C8h**
USB1	**0F91 80C8h**

Figure 14-9312. USB2SS_PHY2_AFE_BG_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BG_ANA_REG4							
R							
0h							

Table 14-28103. USB2SS_PHY2_AFE_BG_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG4	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.84 USB2SS_PHY2_AFE_CALIB_REG1 Register

1 USB2SS_PHY2_AFE_CALIB_REG1 Register (Offset = CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28104. Instance Table

Instance Name	Physical Address
USB0	**0F90 80CCh**
USB1	**0F91 80CCh**

Figure 14-9313. USB2SS_PHY2_AFE_CALIB_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ANA_REG1							
R							
0h							

Table 14-28106. USB2SS_PHY2_AFE_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG1	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.85 USB2SS_PHY2_AFE_BC_REG7 Register

1 USB2SS_PHY2_AFE_BC_REG7 Register (Offset = D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28107. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D0h**
USB1	**0F91 80D0h**

Figure 14-9314. USB2SS_PHY2_AFE_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG7							
R							
0h							

Table 14-28109. USB2SS_PHY2_AFE_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.86 USB2SS_PHY2_AFE_PLL_REG6 Register

1 USB2SS_PHY2_AFE_PLL_REG6 Register (Offset = D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28110. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D4h**
USB1	**0F91 80D4h**

Figure 14-9315. USB2SS_PHY2_AFE_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_ANA_REG6							
R							
0h							

Table 14-28112. USB2SS_PHY2_AFE_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PLL_ANA_REG6	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.87 USB2SS_PHY2_AFE_UNUSED_REG2 Register

1 USB2SS_PHY2_AFE_UNUSED_REG2 Register (Offset = D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28113. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D8h**
USB1	**0F91 80D8h**

Figure 14-9316. USB2SS_PHY2_AFE_UNUSED_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28115. USB2SS_PHY2_AFE_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.88 USB2SS_PHY2_AFE_UNUSED_REG3 Register

1 USB2SS_PHY2_AFE_UNUSED_REG3 Register (Offset = DCh) [reset = 0h]

AFE_UNUSED_REG3

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Table 14-28116. Instance Table

Instance Name	Physical Address
USB0	**0F90 80DCh**
USB1	**0F91 80DCh**

Figure 14-9317. USB2SS_PHY2_AFE_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28118. USB2SS_PHY2_AFE_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.89 USB2SS_PHY2_PLL_REG0 Register

1 USB2SS_PHY2_PLL_REG0 Register (Offset = 100h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28119. Instance Table

Instance Name	Physical Address
USB0	**0F90 8100h**
USB1	**0F91 8100h**

Figure 14-9318. USB2SS_PHY2_PLL_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INITIAL_WAIT_TIME</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28121. USB2SS_PHY2_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INITIAL_WAIT_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.90 USB2SS_PHY2_PLL_REG1 Register

1 USB2SS_PHY2_PLL_REG1 Register (Offset = 104h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28122. Instance Table

Instance Name	Physical Address
USB0	**0F90 8104h**
USB1	**0F91 8104h**

Figure 14-9319. USB2SS_PHY2_PLL_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RST_FDBK_DIV_DELAY_VALUE</td><td>RST_FDBK_DIV_DELAY_EN</td><td>FBDIV_EN</td><td>INITIAL_WAIT_TIME_EN</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28124. USB2SS_PHY2_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	RST_FDBK_DIV_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RST_FDBK_DIV_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FBDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INITIAL_WAIT_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.91 USB2SS_PHY2_PLL_REG2 Register

1 USB2SS_PHY2_PLL_REG2 Register (Offset = 108h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28125. Instance Table

Instance Name	Physical Address
USB0	**0F90 8108h**
USB1	**0F91 8108h**

Figure 14-9320. USB2SS_PHY2_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	VCO_SETTLING_TIME_EN	VCO_SETTLING_TIME					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-28127. USB2SS_PHY2_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	VCO_SETTLING_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	VCO_SETTLING_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.92 USB2SS_PHY2_PLL_REG3 Register

1 USB2SS_PHY2_PLL_REG3 Register (Offset = 10Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28128. Instance Table

Instance Name	Physical Address
USB0	**0F90 810Ch**
USB1	**0F91 810Ch**

Figure 14-9321. USB2SS_PHY2_PLL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FBDIV_VALUE							
R/W							
0h							

Table 14-28130. USB2SS_PHY2_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FBDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.93 USB2SS_PHY2_PLL_REG4 Register

1 USB2SS_PHY2_PLL_REG4 Register (Offset = 110h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28131. Instance Table

Instance Name	Physical Address
USB0	**0F90 8110h**
USB1	**0F91 8110h**

Figure 14-9322. USB2SS_PHY2_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	PLL_LOCK_TIME_15	PD_PFD_VALUE	PD_PFD_EN	PLL_LOCK_EN	PLL_LOCK_VALUE	COARSEDONE_EN	COARSEDONE_VALUE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28133. USB2SS_PHY2_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	PLL_LOCK_TIME_15	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PD_PFD_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PD_PFD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LOCK_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28133. USB2SS_PHY2_PLL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	COARSEDONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSEDONE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.94 USB2SS_PHY2_PLL_REG5 Register

1 USB2SS_PHY2_PLL_REG5 Register (Offset = 114h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28134. Instance Table

Instance Name	Physical Address
USB0	**0F90 8114h**
USB1	**0F91 8114h**

Figure 14-9323. USB2SS_PHY2_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
STARTLOOP_EN_4_0	STARTLOOP_EN_5	STARTLOOP_5	STARTLOOP_4_0				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 14-28136. USB2SS_PHY2_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	STARTLOOP_EN_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	STARTLOOP_EN_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	STARTLOOP_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	STARTLOOP_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.95 USB2SS_PHY2_PLL_REG6 Register

1 USB2SS_PHY2_PLL_REG6 Register (Offset = 118h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28137. Instance Table

Instance Name	Physical Address
USB0	**0F90 8118h**
USB1	**0F91 8118h**

Figure 14-9324. USB2SS_PHY2_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	COARSE_CODE_SEL	LSB_ERROR_0P5	BIG_JUMP_EN	VCO_CNT_WINDOW_VALUE	VCO_CNT_WINDOW_EN	RST_FDBK_DIV_VALUE	RST_FDBK_DIV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28139. USB2SS_PHY2_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	COARSE_CODE_SEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSB_ERROR_0P5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIG_JUMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VCO_CNT_WINDOW_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VCO_CNT_WINDOW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28139. USB2SS_PHY2_PLL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RST_FDBK_DIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RST_FDBK_DIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.96 USB2SS_PHY2_PLL_REG7 Register

1 USB2SS_PHY2_PLL_REG7 Register (Offset = 11Ch) [reset = 0h]

refclock selection

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Table 14-28140. Instance Table

Instance Name	Physical Address
USB0	**0F90 811Ch**
USB1	**0F91 811Ch**

Figure 14-9325. USB2SS_PHY2_PLL_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			REFCLK_SEL				REFCLK_SEL_EN
R/W			R/W				R/W
0h			0h				0h

Table 14-28142. USB2SS_PHY2_PLL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4:1	REFCLK_SEL	R/W	0h	0000 Refclock selection for 9.6 MHz, 0001 Refclock selection for 10 MHz, 0010 Refclock selection for 12 MHz, 0011 Refclock selection for 19.2 MHz, 0100 Refclock selection for 20 MHz, 0101 Refclock selection for 24 MHz, 0110 Refclock selection for 25 MHz, 0111 Refclock selection for 26 MHz, 1000 Refclock selection for 38.4 MHz, 1001 Refclock selection for 40 MHz, 1010 Refclock selection for 48 MHz, 1011 Refclock selection for 50 MHz, 1100 Refclock selection for 52 MHz, 1101 Refclock selection for 9.6 MHz, 1110 Refclock selection for 9.6 MHz, 1111 Refclock selection for 9.6 MHz. Reset Source: usb2_sync_preset_n
0	REFCLK_SEL_EN	R/W	0h	0 PLLREFSEL Value not taken from PLL_REG7[4:1], 1 PLLREFSEL Value taken from PLL_REG7[4:1]. Reset Source: usb2_sync_preset_n

14.9.3.2.2.97 USB2SS_PHY2_PLL_REG8 Register

1 USB2SS_PHY2_PLL_REG8 Register (Offset = 120h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28143. Instance Table

Instance Name	Physical Address
USB0	**0F90 8120h**
USB1	**0F91 8120h**

Figure 14-9326. USB2SS_PHY2_PLL_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE							
R/W							
0h							

Table 14-28145. USB2SS_PHY2_PLL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.98 USB2SS_PHY2_PLL_REG9 Register

1 USB2SS_PHY2_PLL_REG9 Register (Offset = 124h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28146. Instance Table

Instance Name	Physical Address
USB0	**0F90 8124h**
USB1	**0F91 8124h**

Figure 14-9327. USB2SS_PHY2_PLL_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE	V2I_CODE_EN	V2I_CODE					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-28148. USB2SS_PHY2_PLL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	V2I_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	V2I_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.99 USB2SS_PHY2_PLL_REG10 Register

1 USB2SS_PHY2_PLL_REG10 Register (Offset = 128h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28149. Instance Table

Instance Name	Physical Address
USB0	**0F90 8128h**
USB1	**0F91 8128h**

Figure 14-9328. USB2SS_PHY2_PLL_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	IPDIV_VALUE					IPDIV_EN	COARSE_CODE_EN
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-28151. USB2SS_PHY2_PLL_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:2	IPDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	IPDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSE_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.100 USB2SS_PHY2_PLL_REG11 Register

1 USB2SS_PHY2_PLL_REG11 Register (Offset = 12Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28152. Instance Table

Instance Name	Physical Address
USB0	**0F90 812Ch**
USB1	**0F91 812Ch**

Figure 14-9329. USB2SS_PHY2_PLL_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_STANDBY	PLL_STANDBY_EN	PLL_PD	PLL_PD_EN	PLL_PSO_DEL	PLL_PSO_DEL_EN	PLL_PSO	PLL_PSO_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28154. USB2SS_PHY2_PLL_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_STANDBY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_STANDBY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_PD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_PD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_PSO_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28154. USB2SS_PHY2_PLL_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PLL_PSO_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	PLL_PSO	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_PSO_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.101 USB2SS_PHY2_PLL_REG12 Register

1 USB2SS_PHY2_PLL_REG12 Register (Offset = 130h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28155. Instance Table

Instance Name	Physical Address
USB0	**0F90 8130h**
USB1	**0F91 8130h**

Figure 14-9330. USB2SS_PHY2_PLL_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED		PLL_LDO_REF_EN	PLL_LDO_REF_EN_EN	PLL_LDO_CORE_EN	PLL_LDO_CORE_EN_EN	PLL_PD_ANA	PLL_PD_ANA_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-28157. USB2SS_PHY2_PLL_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5	PLL_LDO_REF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_REF_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LDO_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LDO_CORE_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	PLL_PD_ANA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28157. USB2SS_PHY2_PLL_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL_PD_ANA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.102 USB2SS_PHY2_PLL_REG13 Register

1 USB2SS_PHY2_PLL_REG13 Register (Offset = 134h) [reset = 0h]

PLL clockon test mode

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Table 14-28158. Instance Table

Instance Name	Physical Address
USB0	**0F90 8134h**
USB1	**0F91 8134h**

Figure 14-9331. USB2SS_PHY2_PLL_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_CLKON	PLL_LDO_REF_CORE						PLL_LDO_REF_CORE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-28160. USB2SS_PHY2_PLL_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	0 pll clock is not always running, 1 pll clock is always running. Reset Source: usb2_sync_preset_n
6:1	PLL_LDO_REF_CORE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_REF_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.103 USB2SS_PHY2_PLL_REG14 Register

1 USB2SS_PHY2_PLL_REG14 Register (Offset = 138h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28161. Instance Table

Instance Name	Physical Address
USB0	**0F90 8138h**
USB1	**0F91 8138h**

Figure 14-9332. USB2SS_PHY2_PLL_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_LDO_CNT_THRESHOLD			PLL_LDO_CNT_THRESHOLD_EN	PLL_LDO_ISO_CNT_THRESHOLD			PLL_LDO_ISO_CNT_THRESHOLD_EN
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-28163. USB2SS_PHY2_PLL_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	PLL_LDO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PLL_LDO_ISO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_ISO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.104 USB2SS_PHY2_PLL_UNUSED_REG0 Register

1 USB2SS_PHY2_PLL_UNUSED_REG0 Register (Offset = 13Ch) [reset = 0h]

unused

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Table 14-28164. Instance Table

Instance Name	Physical Address
USB0	**0F90 813Ch**
USB1	**0F91 813Ch**

Figure 14-9333. USB2SS_PHY2_PLL_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28166. USB2SS_PHY2_PLL_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.105 USB2SS_PHY2_PLL_UNUSED_REG1 Register

1 USB2SS_PHY2_PLL_UNUSED_REG1 Register (Offset = 140h) [reset = 0h]

unused

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Table 14-28167. Instance Table

Instance Name	Physical Address
USB0	**0F90 8140h**
USB1	**0F91 8140h**

Figure 14-9334. USB2SS_PHY2_PLL_UNUSED_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28169. USB2SS_PHY2_PLL_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.106 USB2SS_PHY2_PLL_REG15 Register

1 USB2SS_PHY2_PLL_REG15 Register (Offset = 144h) [reset = 0h]

Coarse_code values

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Table 14-28170. Instance Table

Instance Name	Physical Address
USB0	**0F90 8144h**
USB1	**0F91 8144h**

Figure 14-9335. USB2SS_PHY2_PLL_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_LOCK	COARSEDONE	VCO_CNT_WIN	RST_FDBK_DIV	UNUSED	PD_PFD	STARTLOOP	COARSE_CODE_8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28172. USB2SS_PHY2_PLL_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_LOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	COARSEDONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	VCO_CNT_WIN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RST_FDBK_DIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	PD_PFD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28172. USB2SS_PHY2_PLL_REG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STARTLOOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSE_CODE_8	R	0h	0 MSB of coarse_code for PLL VCO. Reset Source: usb2_sync_preset_n

14.9.3.2.2.107 USB2SS_PHY2_PLL_REG16 Register

1 USB2SS_PHY2_PLL_REG16 Register (Offset = 148h) [reset = 0h]

Coarse_code values

Return to Summary Table

Table 14-28173. Instance Table

Instance Name	Physical Address
USB0	**0F90 8148h**
USB1	**0F91 8148h**

Figure 14-9336. USB2SS_PHY2_PLL_REG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE							
R							
0h							

Table 14-28175. USB2SS_PHY2_PLL_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R	0h	01011010 8 LSBs of coarse code for PLL VCO Reset Source: usb2_sync_preset_n

14.9.3.2.2.108 USB2SS_PHY2_PLL_UNUSED_REG2 Register

1 USB2SS_PHY2_PLL_UNUSED_REG2 Register (Offset = 14Ch) [reset = 0h]

unused

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Table 14-28176. Instance Table

Instance Name	Physical Address
USB0	**0F90 814Ch**
USB1	**0F91 814Ch**

Figure 14-9337. USB2SS_PHY2_PLL_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-28178. USB2SS_PHY2_PLL_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.109 USB2SS_PHY2_CALIB_REG0 Register

1 USB2SS_PHY2_CALIB_REG0 Register (Offset = 180h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28179. Instance Table

Instance Name	Physical Address
USB0	**0F90 8180h**
USB1	**0F91 8180h**

Figure 14-9338. USB2SS_PHY2_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CLK	CALIB_CLK_EN	COMP_OUT	INIT_WAIT_OVR				INIT_WAIT_OVR_EN
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-28181. USB2SS_PHY2_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CLK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_CLK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	INIT_WAIT_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INIT_WAIT_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.110 USB2SS_PHY2_CALIB_REG1 Register

1 USB2SS_PHY2_CALIB_REG1 Register (Offset = 184h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28182. Instance Table

Instance Name	Physical Address
USB0	**0F90 8184h**
USB1	**0F91 8184h**

Figure 14-9339. USB2SS_PHY2_CALIB_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	CALIB_CODE						CALIB_CODE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-28184. USB2SS_PHY2_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:1	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.111 USB2SS_PHY2_BC_REG0 Register

1 USB2SS_PHY2_BC_REG0 Register (Offset = 188h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28185. Instance Table

Instance Name	Physical Address
USB0	**0F90 8188h**
USB1	**0F91 8188h**

Figure 14-9340. USB2SS_PHY2_BC_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				ADP_EN	ADP_EN_EN	ID_PULLUP	ID_PULLUP_EN
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-28187. USB2SS_PHY2_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
3	ADP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	ADP_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ID_PULLUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ID_PULLUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.112 USB2SS_PHY2_BC_REG1 Register

1 USB2SS_PHY2_BC_REG1 Register (Offset = 18Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28188. Instance Table

Instance Name	Physical Address
USB0	**0F90 818Ch**
USB1	**0F91 818Ch**

Figure 14-9341. USB2SS_PHY2_BC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADP_SOURCE_I_EN	ADP_SOURCE_I_EN_CTRL	ADP_SINK_I_EN	ADP_SINK_I_EN_CTRL	ADP_SENSE_EN	ADP_SENSE_EN_CTRL	ADP_PROBE_EN	ADP_PROBE_EN_CTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28190. USB2SS_PHY2_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ADP_SOURCE_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SOURCE_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_SINK_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ADP_SINK_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	ADP_SENSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28190. USB2SS_PHY2_BC_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ADP_SENSE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ADP_PROBE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ADP_PROBE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.113 USB2SS_PHY2_BC_REG2 Register

1 USB2SS_PHY2_BC_REG2 Register (Offset = 190h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28191. Instance Table

Instance Name	Physical Address
USB0	**0F90 8190h**
USB1	**0F91 8190h**

Figure 14-9342. USB2SS_PHY2_BC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IDM_SINK_EN_VALUE	IDM_SINK_EN_CNTRL	IDP_SINK_EN_VALUE	IDP_SINK_EN_CNTRL	IDP_SRC_EN_VALUE	IDP_SRC_EN_CNTRL	BC_EN_VALUE	BC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28193. USB2SS_PHY2_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IDM_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	IDM_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	IDP_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	IDP_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	IDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28193. USB2SS_PHY2_BC_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	BC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.114 USB2SS_PHY2_BC_REG3 Register

1 USB2SS_PHY2_BC_REG3 Register (Offset = 194h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28194. Instance Table

Instance Name	Physical Address
USB0	**0F90 8194h**
USB1	**0F91 8194h**

Figure 14-9343. USB2SS_PHY2_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DM_VDAT_REF_COMP_EN_VALUE	DM_VDAT_REF_COMP_EN_CNTRL	DP_VDAT_REF_COMP_EN_VALUE	DP_VDAT_REF_COMP_EN_CNTRL	VDP_SRC_EN_VALUE	VDP_SRC_EN_CNTRL	VDM_SRC_EN_VALUE	VDM_SRC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28196. USB2SS_PHY2_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28196. USB2SS_PHY2_BC_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	VDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	VDM_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	VDM_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.115 USB2SS_PHY2_BC_REG4 Register

1 USB2SS_PHY2_BC_REG4 Register (Offset = 198h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28197. Instance Table

Instance Name	Physical Address
USB0	**0F90 8198h**
USB1	**0F91 8198h**

Figure 14-9344. USB2SS_PHY2_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_A_REF_EN_VALUE	RID_A_REF_EN_CNTRL	RID_FLOAT_REF_EN_VALUE	RID_FLOAT_REF_EN_CNTRL	RID_NONFLOAT_COMP_EN_VALUE	RID_NONFLOAT_COMP_EN_CNTRL	RID_FLOAT_COMP_EN_VALUE	RID_FLOAT_COMP_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28199. USB2SS_PHY2_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_A_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_A_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_NONFLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28199. USB2SS_PHY2_BC_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RID_NONFLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RID_FLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_FLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.116 USB2SS_PHY2_BC_REG5 Register

1 USB2SS_PHY2_BC_REG5 Register (Offset = 19Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28200. Instance Table

Instance Name	Physical Address
USB0	**0F90 819Ch**
USB1	**0F91 819Ch**

Figure 14-9345. USB2SS_PHY2_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_B_C_COMP_EN_VALUE	RID_B_C_COMP_EN_CNTRL	RID_A_COMP_EN_VALUE	RID_A_COMP_EN_CNTRL	RID_C_REF_EN_VALUE	RID_C_REF_EN_CNTRL	RID_B_REF_EN_VALUE	RID_B_REF_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28202. USB2SS_PHY2_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_B_C_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_B_C_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_A_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_A_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_C_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28202. USB2SS_PHY2_BC_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RID_C_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RID_B_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_B_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.117 USB2SS_PHY2_BC_REG6 Register

1 USB2SS_PHY2_BC_REG6 Register (Offset = 1A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28203. Instance Table

Instance Name	Physical Address
USB0	**0F90 81A0h**
USB1	**0F91 81A0h**

Figure 14-9346. USB2SS_PHY2_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_DELAY_VALUE					BC_DELAY_EN	DM_VLGC_COMP_EN_VALUE	DM_VLGC_COMP_EN_CNTRL
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-28205. USB2SS_PHY2_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	BC_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BC_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_VLGC_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DM_VLGC_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.118 USB2SS_PHY2_BC_REG7 Register

1 USB2SS_PHY2_BC_REG7 Register (Offset = 1A4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28206. Instance Table

Instance Name	Physical Address
USB0	**0F90 81A4h**
USB1	**0F91 81A4h**

Figure 14-9347. USB2SS_PHY2_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_NONFLOAT_SRC_EN_VALUE	RID_NONFLOAT_SRC_EN_CNTRL	RID_FLOAT_SRC_EN_VALUE	RID_FLOAT_SRC_EN_CNTRL	RESET_CNTRL	DM_CURRENT_SRC_EN_VALUE	DM_CURRENT_SRC_EN_CNTRL	UNUSED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28208. USB2SS_PHY2_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_NONFLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_NONFLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RESET_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28208. USB2SS_PHY2_BC_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DM_CURRENT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_CURRENT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.119 USB2SS_PHY2_TED_REG0 Register

1 USB2SS_PHY2_TED_REG0 Register (Offset = 1A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28209. Instance Table

Instance Name	Physical Address
USB0	**0F90 81A8h**
USB1	**0F91 81A8h**

Figure 14-9348. USB2SS_PHY2_TED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_UP_EN	DELAY_VALUE		DELAY_EN	CALIB_DONE	CALIIB_DONE_EN	COMP_OUT_DOWN_INV	COMP_OUT_UP_INV
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h

Table 14-28211. USB2SS_PHY2_TED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	DELAY_VALUE	R/W	0h	Delay is 8us Reset Source: usb2_sync_preset_n
4	DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIIB_DONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	COMP_OUT_DOWN_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28211. USB2SS_PHY2_TED_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMP_OUT_UP_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.120 USB2SS_PHY2_TED_REG1 Register

1 USB2SS_PHY2_TED_REG1 Register (Offset = 1ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28212. Instance Table

Instance Name	Physical Address
USB0	**0F90 81ACh**
USB1	**0F91 81ACh**

Figure 14-9349. USB2SS_PHY2_TED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_DOWN				CALIB_CODE_UP			
R/W				R/W			
0h				0h			

Table 14-28214. USB2SS_PHY2_TED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	CALIB_CODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.121 USB2SS_PHY2_TED_REG2 Register

1 USB2SS_PHY2_TED_REG2 Register (Offset = 1B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28215. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B0h**
USB1	**0F91 81B0h**

Figure 14-9350. USB2SS_PHY2_TED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			CALIB_MODE_DN	CALIB_MODE_DN_EN	CALIB_MODE_UP	CALIB_MODE_UP_EN	CALIB_CODE_DN_EN
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-28217. USB2SS_PHY2_TED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4	CALIB_MODE_DN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_MODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_MODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_MODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28217. USB2SS_PHY2_TED_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CALIB_CODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.122 USB2SS_PHY2_CALIB_REG2 Register

1 USB2SS_PHY2_CALIB_REG2 Register (Offset = 1B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28218. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B4h**
USB1	**0F91 81B4h**

Figure 14-9351. USB2SS_PHY2_CALIB_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				CALIB_CMP	CALIB_PD	CALIB_CLOCK	CALIB_DONE
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-28220. USB2SS_PHY2_CALIB_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
3	CALIB_CMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.123 USB2SS_PHY2_CALIB_REG3 Register

1 USB2SS_PHY2_CALIB_REG3 Register (Offset = 1B8h) [reset = 0h]

Resistor calibration code

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Table 14-28221. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B8h**
USB1	**0F91 81B8h**

Figure 14-9352. USB2SS_PHY2_CALIB_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			BG_UNIT_RES_CALIB				
R			R				
0h			0h				

Table 14-28223. USB2SS_PHY2_CALIB_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
4:0	BG_UNIT_RES_CALIB	R	0h	Resistor calibration code from the calibration block Reset Source: usb2_sync_preset_n

14.9.3.2.2.124 USB2SS_PHY2_BC_REG8 Register

1 USB2SS_PHY2_BC_REG8 Register (Offset = 1BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28224. Instance Table

Instance Name	Physical Address
USB0	**0F90 81BCh**
USB1	**0F91 81BCh**

Figure 14-9353. USB2SS_PHY2_BC_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DCD_COMP	ADP_SENSE	ADP_PROBE	BVALID	VBUSVALID	IDDIG	UNUSED	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	

Table 14-28226. USB2SS_PHY2_BC_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DCD_COMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SENSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_PROBE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	IDDIG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28226. USB2SS_PHY2_BC_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.125 USB2SS_PHY2_BC_REG9 Register

1 USB2SS_PHY2_BC_REG9 Register (Offset = 1C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28227. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C0h**
USB1	**0F91 81C0h**

Figure 14-9354. USB2SS_PHY2_BC_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DM_VDAT_REF_COMP_EN	O_DP_VDAT_REF_COMP_EN	O_VDM_SRC_EN	O_VDP_SRC_EN	O_IDM_SINK_EN	O_IDP_SINK_EN	O_IDP_SRC_EN	O_BC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28229. USB2SS_PHY2_BC_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DM_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DP_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_VDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_VDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_IDM_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28229. USB2SS_PHY2_BC_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_IDP_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_IDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.126 USB2SS_PHY2_BC_REG10 Register

1 USB2SS_PHY2_BC_REG10 Register (Offset = 1C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28230. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C4h**
USB1	**0F91 81C4h**

Figure 14-9355. USB2SS_PHY2_BC_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_RID_B_C_COMP_EN	O_RID_A_COMP_EN	O_RID_C_REF_EN	O_RID_B_REF_EN	O_RID_A_REF_EN	O_RID_FLOAT_REF_EN	O_RID_NONFLOAT_SRC_EN	O_RID_FLOAT_SRC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28232. USB2SS_PHY2_BC_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_RID_B_C_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_RID_A_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RID_C_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_RID_B_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_RID_A_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28232. USB2SS_PHY2_BC_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_RID_FLOAT_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_RID_NONFLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_RID_FLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.127 USB2SS_PHY2_BC_REG11 Register

1 USB2SS_PHY2_BC_REG11 Register (Offset = 1C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28233. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C8h**
USB1	**0F91 81C8h**

Figure 14-9356. USB2SS_PHY2_BC_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_IDM_SRC_EN	I_AFE_RXDP_ANA	I_AFE_RXDM_ANA	I_RID_B_C_COMP_STS	I_RID_A_COMP_STS	I_DM_VDAT_REF_COMP_STS	I_DP_VDAT_REF_COMP_STS	O_DM_VLGC_COMP_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28235. USB2SS_PHY2_BC_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_IDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_AFE_RXDP_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	I_AFE_RXDM_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	I_RID_B_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	I_RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28235. USB2SS_PHY2_BC_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	I_DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	I_DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_DM_VLGC_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.128 USB2SS_PHY2_BC_REG12 Register

1 USB2SS_PHY2_BC_REG12 Register (Offset = 1CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28236. Instance Table

Instance Name	Physical Address
USB0	**0F90 81CCh**
USB1	**0F91 81CCh**

Figure 14-9357. USB2SS_PHY2_BC_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_GND_COMP_STS	RID_FLOAT_COMP_STS	RID_C_COMP_STS	RID_B_COMP_STS	RID_A_COMP_STS	DM_VLGC_COMP_STS	DM_VDAT_REF_COMP_STS	DP_VDAT_REF_COMP_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28238. USB2SS_PHY2_BC_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_GND_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_FLOAT_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_B_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28238. USB2SS_PHY2_BC_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DM_VLGC_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.129 USB2SS_PHY2_TED_REG3 Register

1 USB2SS_PHY2_TED_REG3 Register (Offset = 1D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28239. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D0h**
USB1	**0F91 81D0h**

Figure 14-9358. USB2SS_PHY2_TED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_DOWN				COMPARATOR_DOWN	CALIB_DONE_DOWN	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-28241. USB2SS_PHY2_TED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.130 USB2SS_PHY2_TED_REG4 Register

1 USB2SS_PHY2_TED_REG4 Register (Offset = 1D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28242. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D4h**
USB1	**0F91 81D4h**

Figure 14-9359. USB2SS_PHY2_TED_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_UP				COMPARATOR_UP	CALIB_DONE_UP	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-28244. USB2SS_PHY2_TED_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.131 USB2SS_PHY2_DIG_UNUSED_REG0 Register

1 USB2SS_PHY2_DIG_UNUSED_REG0 Register (Offset = 1D8h) [reset = 0h]

UNUSED

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Table 14-28245. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D8h**
USB1	**0F91 81D8h**

Figure 14-9360. USB2SS_PHY2_DIG_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
GLITCH_FILTER_EN	UNUSED						
R/W	R/W						
0h	0h						

Table 14-28247. USB2SS_PHY2_DIG_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	GLITCH_FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.132 USB2SS_PHY2_DIG_UNUSED_REG1 Register

1 USB2SS_PHY2_DIG_UNUSED_REG1 Register (Offset = 1DCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28248. Instance Table

Instance Name	Physical Address
USB0	**0F90 81DCh**
USB1	**0F91 81DCh**

Figure 14-9361. USB2SS_PHY2_DIG_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					THRESHOLD_OVR_VALUE_MSB		THRESHOLD_OVR_EN
R/W					R/W		R/W
0h					0h		0h

Table 14-28250. USB2SS_PHY2_DIG_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
2:1	THRESHOLD_OVR_VALUE_MSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	THRESHOLD_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.133 USB2SS_PHY2_DIG_UNUSED_REG2 Register

1 USB2SS_PHY2_DIG_UNUSED_REG2 Register (Offset = 1E0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28251. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E0h**
USB1	**0F91 81E0h**

Figure 14-9362. USB2SS_PHY2_DIG_UNUSED_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THRESHOLD_OVR_VALUE_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28253. USB2SS_PHY2_DIG_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	THRESHOLD_OVR_VALUE_LSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.134 USB2SS_PHY2_DIG_UNUSED_REG3 Register

1 USB2SS_PHY2_DIG_UNUSED_REG3 Register (Offset = 1E4h) [reset = 0h]

UNUSED

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Table 14-28254. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E4h**
USB1	**0F91 81E4h**

Figure 14-9363. USB2SS_PHY2_DIG_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28256. USB2SS_PHY2_DIG_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.135 USB2SS_PHY2_INTERRUPT_REG1 Register

1 USB2SS_PHY2_INTERRUPT_REG1 Register (Offset = 1E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28257. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E8h**
USB1	**0F91 81E8h**

Figure 14-9364. USB2SS_PHY2_INTERRUPT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IRSR	ISR	UNUSED					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-28259. USB2SS_PHY2_INTERRUPT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IRSR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ISR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.136 USB2SS_PHY2_INTERRUPT_REG2 Register

1 USB2SS_PHY2_INTERRUPT_REG2 Register (Offset = 1ECh) [reset = 1h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28260. Instance Table

Instance Name	Physical Address
USB0	**0F90 81ECh**
USB1	**0F91 81ECh**

Figure 14-9365. USB2SS_PHY2_INTERRUPT_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">UNUSED</td><td>IMR</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-28262. USB2SS_PHY2_INTERRUPT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
0	IMR	R/W	1h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.137 USB2SS_PHY2_RX_REG0 Register

1 USB2SS_PHY2_RX_REG0 Register (Offset = 200h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28263. Instance Table

Instance Name	Physical Address
USB0	**0F90 8200h**
USB1	**0F91 8200h**

Figure 14-9366. USB2SS_PHY2_RX_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">FSLS_NO_EOP_TIMEOUT</td><td>FSLS_TIMEOUT_EN</td><td>HS_SYNC_DET_BITS</td><td colspan="2">FS_EOP_SE0_THRESHOLD</td><td>FS_EOP_SE0_EN</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-28265. USB2SS_PHY2_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	FSLS_NO_EOP_TIMEOUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SYNC_DET_BITS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	FS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.138 USB2SS_PHY2_RX_REG1 Register

1 USB2SS_PHY2_RX_REG1 Register (Offset = 204h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28266. Instance Table

Instance Name	Physical Address
USB0	**0F90 8204h**
USB1	**0F91 8204h**

Figure 14-9367. USB2SS_PHY2_RX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LS_EOP_SE0_THRESHOLD						LS_EOP_SE0_EN	FS_NO_EOP_TIMEOUT_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-28268. USB2SS_PHY2_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	LS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_NO_EOP_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.139 USB2SS_PHY2_TX_REG0 Register

1 USB2SS_PHY2_TX_REG0 Register (Offset = 208h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28269. Instance Table

Instance Name	Physical Address
USB0	**0F90 8208h**
USB1	**0F91 8208h**

Figure 14-9368. USB2SS_PHY2_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				FS_PREAMBLE_EN	SOF_EXTENSION		SOF_EXTENSION_EN
R/W				R/W	R/W		R/W
0h				0h	0h		0h

Table 14-28271. USB2SS_PHY2_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
3	FS_PREAMBLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SOF_EXTENSION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SOF_EXTENSION_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.140 USB2SS_PHY2_TX_REG1 Register

1 USB2SS_PHY2_TX_REG1 Register (Offset = 20Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28272. Instance Table

Instance Name	Physical Address
USB0	**0F90 820Ch**
USB1	**0F91 820Ch**

Figure 14-9369. USB2SS_PHY2_TX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE_VALUE							
R/W							
0h							

Table 14-28274. USB2SS_PHY2_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.141 USB2SS_PHY2_CDR_REG0 Register

1 USB2SS_PHY2_CDR_REG0 Register (Offset = 210h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28275. Instance Table

Instance Name	Physical Address
USB0	**0F90 8210h**
USB1	**0F91 8210h**

Figure 14-9370. USB2SS_PHY2_CDR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		PLL_CLKDIV		PLL_CLKDIV_EN	SQUELCH_DELAY		SQUELCH_DELAY_EN
R/W		R/W		R/W	R/W		R/W
0h		0h		0h	0h		0h

Table 14-28277. USB2SS_PHY2_CDR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5:4	PLL_CLKDIV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_CLKDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SQUELCH_DELAY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SQUELCH_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.142 USB2SS_PHY2_CDR_REG1 Register

1 USB2SS_PHY2_CDR_REG1 Register (Offset = 214h) [reset = 0h]

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Table 14-28278. Instance Table

Instance Name	Physical Address
USB0	**0F90 8214h**
USB1	**0F91 8214h**

Figure 14-9371. USB2SS_PHY2_CDR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	CALIB_COMP_OUT	CALIB_SPC_THRESHOLD			CALIB_SPC_THRESHOLD_EN	CALIB_ITERATION	DYNAMIC_CALIB_EN
R/W	R/W	R/W			R/W	R/W	R/W
0h	0h	0h			0h	0h	0h

Table 14-28280. USB2SS_PHY2_CDR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	CALIB_COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:3	CALIB_SPC_THRESHOLD	R/W	0h	000 The time interval between succesive calibrations is 0us, 001 The time interval between succesive calibrations is 1us, 010 The time interval between succesive calibrations is 2us, 011 The time interval between succesive calibrations is 3us, 100 The time interval between succesive calibrations is 4us, 101 The time interval between succesive calibrations is 5us, 110 The time interval between succesive calibrations is 6us, 111 The time interval between succesive calibrations is 7us. Reset Source: usb2_sync_preset_n
2	CALIB_SPC_THRESHOLD_EN	R/W	0h	0 The time interval between succesive calibrations is taken as 5us by default, 1 The time interval between succesive calibrations is taken from CDR_REG1[5:3] Reset Source: usb2_sync_preset_n

Table 14-28280. USB2SS_PHY2_CDR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_ITERATION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DYNAMIC_CALIB_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.143 USB2SS_PHY2_CDR_REG2 Register

1 USB2SS_PHY2_CDR_REG2 Register (Offset = 218h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28281. Instance Table

Instance Name	Physical Address
USB0	**0F90 8218h**
USB1	**0F91 8218h**

Figure 14-9372. USB2SS_PHY2_CDR_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	HSRX_EN_DEL	HSRX_EN_DEL_EN	HSRX_EN	HSRX_EN_EN	CALIB_CLOCK	CALIB_CLOCK_EN	CALIB_OUT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28283. USB2SS_PHY2_CDR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	HSRX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSRX_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_CLOCK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28283. USB2SS_PHY2_CDR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_CLOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_OUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.144 USB2SS_PHY2_CDR_REG3 Register

1 USB2SS_PHY2_CDR_REG3 Register (Offset = 21Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28284. Instance Table

Instance Name	Physical Address
USB0	**0F90 821Ch**
USB1	**0F91 821Ch**

Figure 14-9373. USB2SS_PHY2_CDR_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ACTIVE	CALIB_DONE	CALIB_CODE					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-28286. USB2SS_PHY2_CDR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_ACTIVE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.145 USB2SS_PHY2_CDR_REG4 Register

1 USB2SS_PHY2_CDR_REG4 Register (Offset = 220h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28287. Instance Table

Instance Name	Physical Address
USB0	**0F90 8220h**
USB1	**0F91 8220h**

Figure 14-9374. USB2SS_PHY2_CDR_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLK_GATE_VALUE	CLK_GATE_EN	CLK_GATE_SQ_MASK	LATENCY_THRESHOLD		LATENCY_THRESHOLD_EN	DECISION_ERROR_EN	FILTER_EN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-28289. USB2SS_PHY2_CDR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLK_GATE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CLK_GATE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	CLK_GATE_SQ_MASK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	LATENCY_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LATENCY_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28289. USB2SS_PHY2_CDR_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DECISION_ERROR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.146 USB2SS_PHY2_CDR_REG5 Register

1 USB2SS_PHY2_CDR_REG5 Register (Offset = 224h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28290. Instance Table

Instance Name	Physical Address
USB0	**0F90 8224h**
USB1	**0F91 8224h**

Figure 14-9375. USB2SS_PHY2_CDR_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					SAMPLE_5X_EN	SMALL_PULSE	SMALL_PULSE_EN
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-28292. USB2SS_PHY2_CDR_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
2	SAMPLE_5X_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SMALL_PULSE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SMALL_PULSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.147 USB2SS_PHY2_CDR_REG6 Register

1 USB2SS_PHY2_CDR_REG6 Register (Offset = 228h) [reset = 0h]

unused

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Table 14-28293. Instance Table

Instance Name	Physical Address
USB0	**0F90 8228h**
USB1	**0F91 8228h**

Figure 14-9376. USB2SS_PHY2_CDR_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28295. USB2SS_PHY2_CDR_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.148 USB2SS_PHY2_CDR_REG7 Register

1 USB2SS_PHY2_CDR_REG7 Register (Offset = 22Ch) [reset = 0h]

unused

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Table 14-28296. Instance Table

Instance Name	Physical Address
USB0	**0F90 822Ch**
USB1	**0F91 822Ch**

Figure 14-9377. USB2SS_PHY2_CDR_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28298. USB2SS_PHY2_CDR_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.149 USB2SS_PHY2_CDR_REG8 Register

1 USB2SS_PHY2_CDR_REG8 Register (Offset = 230h) [reset = 0h]

unused

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Table 14-28299. Instance Table

Instance Name	Physical Address
USB0	**0F90 8230h**
USB1	**0F91 8230h**

Figure 14-9378. USB2SS_PHY2_CDR_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28301. USB2SS_PHY2_CDR_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.150 USB2SS_PHY2_RX_REG2 Register

1 USB2SS_PHY2_RX_REG2 Register (Offset = 234h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28302. Instance Table

Instance Name	Physical Address
USB0	**0F90 8234h**
USB1	**0F91 8234h**

Figure 14-9379. USB2SS_PHY2_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EB_ERROR	CDR_ERROR	SYNC_DETECTED	EOP_DETECTED	HS_EOP_CONDITION	NORMAL_EOP	ALIGNMENT_ERROR	NO_EOP
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28304. USB2SS_PHY2_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EB_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CDR_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SYNC_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_EOP_CONDITION	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28304. USB2SS_PHY2_RX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NORMAL_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ALIGNMENT_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	NO_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.151 USB2SS_PHY2_RX_REG3 Register

1 USB2SS_PHY2_RX_REG3 Register (Offset = 238h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28305. Instance Table

Instance Name	Physical Address
USB0	**0F90 8238h**
USB1	**0F91 8238h**

Figure 14-9380. USB2SS_PHY2_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_EOP_DETECTED	SE0_VALIDATED	LSFS_EOP_DETECTED	BIT_UNSTUFF_ERROR	RX_STATE_BITUNSTUFF			START_FLAG
R	R	R	R	R			R
0h	0h	0h	0h	0h			0h

Table 14-28307. USB2SS_PHY2_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SE0_VALIDATED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSFS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIT_UNSTUFF_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	RX_STATE_BITUNSTUFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28307. USB2SS_PHY2_RX_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	START_FLAG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.152 USB2SS_PHY2_RX_REG4 Register

1 USB2SS_PHY2_RX_REG4 Register (Offset = 23Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28308. Instance Table

Instance Name	Physical Address
USB0	**0F90 823Ch**
USB1	**0F91 823Ch**

Figure 14-9381. USB2SS_PHY2_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXACTIVE_REG	DEASSERT_RXACTIVE_REG	UNUSED					
R	R	R					
0h	0h	0h					

Table 14-28310. USB2SS_PHY2_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DEASSERT_RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.153 USB2SS_PHY2_RX_REG5 Register

1 USB2SS_PHY2_RX_REG5 Register (Offset = 240h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28311. Instance Table

Instance Name	Physical Address
USB0	**0F90 8240h**
USB1	**0F91 8240h**

Figure 14-9382. USB2SS_PHY2_RX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIE_CNT_UPPER							
R							
0h							

Table 14-28313. USB2SS_PHY2_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SIE_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.154 USB2SS_PHY2_RX_REG6 Register

1 USB2SS_PHY2_RX_REG6 Register (Offset = 244h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28314. Instance Table

Instance Name	Physical Address
USB0	**0F90 8244h**
USB1	**0F91 8244h**

Figure 14-9383. USB2SS_PHY2_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CNT_UPPER							
R							
0h							

Table 14-28316. USB2SS_PHY2_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PHY_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.155 USB2SS_PHY2_RX_REG7 Register

1 USB2SS_PHY2_RX_REG7 Register (Offset = 248h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28317. Instance Table

Instance Name	Physical Address
USB0	**0F90 8248h**
USB1	**0F91 8248h**

Figure 14-9384. USB2SS_PHY2_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHY_CNT_LOWER				SIE_CNT_LOWER			
R				R			
0h				0h			

Table 14-28319. USB2SS_PHY2_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PHY_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SIE_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.156 USB2SS_PHY2_TX_REG2 Register

1 USB2SS_PHY2_TX_REG2 Register (Offset = 24Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28320. Instance Table

Instance Name	Physical Address
USB0	**0F90 824Ch**
USB1	**0F91 824Ch**

Figure 14-9385. USB2SS_PHY2_TX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_HS_STATE				EOP_TRANSMITTED	HS_BITSTUFF_EN	RESUME_EOP	REMOTE_WAKEUP
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-28322. USB2SS_PHY2_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_HS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_TRANSMITTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RESUME_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	REMOTE_WAKEUP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.157 USB2SS_PHY2_TX_REG3 Register

1 USB2SS_PHY2_TX_REG3 Register (Offset = 250h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28323. Instance Table

Instance Name	Physical Address
USB0	**0F90 8250h**
USB1	**0F91 8250h**

Figure 14-9386. USB2SS_PHY2_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_LSFS_STATE				PD_STATE			PREAMBLE_SENT
R				R			R
0h				0h			0h

Table 14-28325. USB2SS_PHY2_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_LSFS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PD_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PREAMBLE_SENT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.158 USB2SS_PHY2_TX_REG4 Register

1 USB2SS_PHY2_TX_REG4 Register (Offset = 254h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28326. Instance Table

Instance Name	Physical Address
USB0	**0F90 8254h**
USB1	**0F91 8254h**

Figure 14-9387. USB2SS_PHY2_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED						LSFS_BITSTUFF_EN	LS_KEEP_ALIVE
R						R	R
0h						0h	0h

Table 14-28328. USB2SS_PHY2_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
1	LSFS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LS_KEEP_ALIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.159 USB2SS_PHY2_CDR_REG9 Register

1 USB2SS_PHY2_CDR_REG9 Register (Offset = 258h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28329. Instance Table

Instance Name	Physical Address
USB0	**0F90 8258h**
USB1	**0F91 8258h**

Figure 14-9388. USB2SS_PHY2_CDR_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					I_ANA_COMP_OUT	SAMPLER_CALIB_DONE	ANA_CALIB_ACTIVE
R					R	R	R
0h					0h	0h	0h

Table 14-28331. USB2SS_PHY2_CDR_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	I_ANA_COMP_OUT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SAMPLER_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ANA_CALIB_ACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.160 USB2SS_PHY2_CDR_REG10 Register

1 USB2SS_PHY2_CDR_REG10 Register (Offset = 25Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28332. Instance Table

Instance Name	Physical Address
USB0	**0F90 825Ch**
USB1	**0F91 825Ch**

Figure 14-9389. USB2SS_PHY2_CDR_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		CALIB_CODE					
R		R					
0h		0h					

Table 14-28334. USB2SS_PHY2_CDR_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.161 USB2SS_PHY2_CDR_REG11 Register

1 USB2SS_PHY2_CDR_REG11 Register (Offset = 260h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28335. Instance Table

Instance Name	Physical Address
USB0	**0F90 8260h**
USB1	**0F91 8260h**

Figure 14-9390. USB2SS_PHY2_CDR_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SMALL_PULSE				O_HSRX_REC_DICISION_ERROR	O_ANA_CLK_GATE	RECEIVE_START	I_ANA_TED_SQUELCH
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-28337. USB2SS_PHY2_CDR_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SMALL_PULSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_HSRX_REC_DICISION_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_ANA_CLK_GATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RECEIVE_START	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	I_ANA_TED_SQUELCH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.162 USB2SS_PHY2_CDR_RE12 Register

1 USB2SS_PHY2_CDR_RE12 Register (Offset = 264h) [reset = 0h]

unused

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Table 14-28338. Instance Table

Instance Name	Physical Address
USB0	**0F90 8264h**
USB1	**0F91 8264h**

Figure 14-9391. USB2SS_PHY2_CDR_RE12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-28340. USB2SS_PHY2_CDR_RE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.163 USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register

1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register (Offset = 268h) [reset = 0h]

UNUSED

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Table 14-28341. Instance Table

Instance Name	Physical Address
USB0	**0F90 8268h**
USB1	**0F91 8268h**

Figure 14-9392. USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28343. USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.164 USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register

1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register (Offset = 26Ch) [reset = 0h]

UNUSED

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Table 14-28344. Instance Table

Instance Name	Physical Address
USB0	**0F90 826Ch**
USB1	**0F91 826Ch**

Figure 14-9393. USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28346. USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.165 USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register

1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register (Offset = 270h) [reset = 0h]

UNUSED

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Table 14-28347. Instance Table

Instance Name	Physical Address
USB0	**0F90 8270h**
USB1	**0F91 8270h**

Figure 14-9394. USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28349. USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.166 USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register

1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register (Offset = 274h) [reset = 0h]

UNUSED

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Table 14-28350. Instance Table

Instance Name	Physical Address
USB0	**0F90 8274h**
USB1	**0F91 8274h**

Figure 14-9395. USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28352. USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.3.2.2.167 USB2SS_PHY2_UTMI_REG0 Register

1 USB2SS_PHY2_UTMI_REG0 Register (Offset = 280h) [reset = 0h]

register UTMI_REG0

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Table 14-28353. Instance Table

Instance Name	Physical Address
USB0	**0F90 8280h**
USB1	**0F91 8280h**

Figure 14-9396. USB2SS_PHY2_UTMI_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LOOPBACK_SEL		LOOPBACK_EN	BIST_MODE_SEL				BIST_EN
R/W		R/W	R/W				R/W
0h		0h	0h				0h

Table 14-28355. USB2SS_PHY2_UTMI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	LOOPBACK_SEL	R/W	0h	00 Loopback mode selection = 00 : Reserved, 01 Loopback mode selection = 01 : LS, 10 Loopback mode selection = 10 : FS, 11 Loopback mode selection = 11 : HS Reset Source: usb2_sync_preset_n
5	LOOPBACK_EN	R/W	0h	0 Loopback mode selection is taken from primary input port-loopback[1:0], 1 Loopback mode selection is taken from UTMI_REG0[7:6]. Reset Source: usb2_sync_preset_n
4:1	BIST_MODE_SEL	R/W	0h	0 BIST for 8 bit, 1 BIST for 16 bit, 0 Error injection disabled, 1 Error injection enabled, 0 BIST for device mode, 1 BIST for host mode, 0 BIST for HS mode, 1 BIST for FS mode. Reset Source: usb2_sync_preset_n
0	BIST_EN	R/W	0h	0 BIST control signals taken from primary input BIST related ports, 1 BIST signals taken from UTMI REG0[4:1], UTMI_REG1[7:6], UTMI_REG5[7:6] Reset Source: usb2_sync_preset_n

14.9.3.2.2.168 USB2SS_PHY2_UTMI_REG1 Register

1 USB2SS_PHY2_UTMI_REG1 Register (Offset = 284h) [reset = 0h]

bist error injection, soft resets

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Table 14-28356. Instance Table

Instance Name	Physical Address
USB0	**0F90 8284h**
USB1	**0F91 8284h**

Figure 14-9397. USB2SS_PHY2_UTMI_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_ERR		BIST_SOFT_RST	TX_LSFS_SOFT_RST	TX_HS_SOFT_RST	CLKDIV_SOFT_RST	CALIB_SOFT_RST	PHY_SOFT_RST
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-28358. USB2SS_PHY2_UTMI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_ERR	R/W	0h	00 Introduce error on first packet, bist error injection = 00, 01 Introduce error on second packet,bist error injection = 01, 10 Introduce error on third packet, bist error injection = 10, 11 Introduce error on last packet, bist error injection = 11. Reset Source: usb2_sync_preset_n
5	BIST_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_LSFS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CLKDIV_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28358. USB2SS_PHY2_UTMI_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PHY_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.169 USB2SS_PHY2_UTMI_REG2 Register

1 USB2SS_PHY2_UTMI_REG2 Register (Offset = 288h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28359. Instance Table

Instance Name	Physical Address
USB0	**0F90 8288h**
USB1	**0F91 8288h**

Figure 14-9398. USB2SS_PHY2_UTMI_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_CNTRL_SOFT_RST	SHIFT_REG_SOFT_RST	BITUNSTUFF_SOFT_RST	NRZI_DEC_SOFT_RST	EOP_DET_SOFT_RST	SYNC_DET_SOFT_RST	LSFS_DLL_SOFT_RST	RX_HS_SOFT_RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28361. USB2SS_PHY2_UTMI_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_CNTRL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SHIFT_REG_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BITUNSTUFF_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	NRZI_DEC_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28361. USB2SS_PHY2_UTMI_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SYNC_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LSFS_DLL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.170 USB2SS_PHY2_UTMI_REG3 Register

1 USB2SS_PHY2_UTMI_REG3 Register (Offset = 28Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28362. Instance Table

Instance Name	Physical Address
USB0	**0F90 828Ch**
USB1	**0F91 828Ch**

Figure 14-9399. USB2SS_PHY2_UTMI_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_RX_ERR	LS_LINESTATE_FIL_EN	FS_LINESTATE_FIL_CNT					FS_LINESTATE_FIL_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-28364. USB2SS_PHY2_UTMI_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_RX_ERR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	LS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	FS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.171 USB2SS_PHY2_UTMI_REG4 Register

1 USB2SS_PHY2_UTMI_REG4 Register (Offset = 290h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28365. Instance Table

Instance Name	Physical Address
USB0	**0F90 8290h**
USB1	**0F91 8290h**

Figure 14-9400. USB2SS_PHY2_UTMI_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LS_LINESTATE_FIL_CNT							
R/W							
0h							

Table 14-28367. USB2SS_PHY2_UTMI_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	LS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.172 USB2SS_PHY2_UTMI_REG5 Register

1 USB2SS_PHY2_UTMI_REG5 Register (Offset = 294h) [reset = 0h]

BIST, hsrx data

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Table 14-28368. Instance Table

Instance Name	Physical Address
USB0	**0F90 8294h**
USB1	**0F91 8294h**

Figure 14-9401. USB2SS_PHY2_UTMI_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_MODE_EN	BIST_ON	HSTX_BOOST_DEAMP_OFF	HSTX_BOOST	HS_SAMP	HS_SAMP_EN	HSRX	HSRX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28370. USB2SS_PHY2_UTMI_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BIST_MODE_EN	R/W	0h	0 BIST mode en is taken from primary input port- bist_mode_en, 1 bist_mode_en is turned on. Reset Source: usb2_sync_preset_n
6	BIST_ON	R/W	0h	0 BIST on is taken from primary input port- bist_on, 1 bist_on is enabled. Reset Source: usb2_sync_preset_n
5	HSTX_BOOST_DEAMP_OFF	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_BOOST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SAMP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28370. USB2SS_PHY2_UTMI_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HS_SAMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HSRX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.173 USB2SS_PHY2_UTMI_REG6 Register

1 USB2SS_PHY2_UTMI_REG6 Register (Offset = 298h) [reset = 0h]

vbusvalid control, hs drive en threshold

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Table 14-28371. Instance Table

Instance Name	Physical Address
USB0	**0F90 8298h**
USB1	**0F91 8298h**

Figure 14-9402. USB2SS_PHY2_UTMI_REG6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>VBUSVALID_CNTRL</td><td>VBUSVALID_L3_DEV_EN</td><td colspan="5">HS_DRVEN_THRESHOLD</td><td>HS_DRVEN_TH_EN</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="5">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
</table>

Table 14-28373. USB2SS_PHY2_UTMI_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	VBUSVALID_CNTRL	R/W	0h	0 vbusvalid comparator is not enabled in L3 device Powered Off state, 1 vbusvalid comparator is enabled in L3 device Powered Off state Reset Source: usb2_sync_preset_n
6	VBUSVALID_L3_DEV_EN	R/W	0h	0 Vbusvalid comparator output comes on vbusvalid primary output port, 1 Sessvalid comparator output comes on vbusvalid primary output port. Reset Source: usb2_sync_preset_n
5:1	HS_DRVEN_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_DRVEN_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.174 USB2SS_PHY2_UTMI_REG7 Register

1 USB2SS_PHY2_UTMI_REG7 Register (Offset = 29Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28374. Instance Table

Instance Name	Physical Address
USB0	**0F90 829Ch**
USB1	**0F91 829Ch**

Figure 14-9403. USB2SS_PHY2_UTMI_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HSTX_BC_MODE	HSTX_BC_EN	HSTX_CHIRP_MODE	HSTX_CHIRP_EN	HSTX_EN_DEL	HSTX_EN_DEL_EN	HSTX	HSTX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28376. USB2SS_PHY2_UTMI_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HSTX_BC_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HSTX_BC_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_CHIRP_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_CHIRP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28376. USB2SS_PHY2_UTMI_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HSTX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HSTX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.175 USB2SS_PHY2_UTMI_REG8 Register

1 USB2SS_PHY2_UTMI_REG8 Register (Offset = 2A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28377. Instance Table

Instance Name	Physical Address
USB0	**0F90 82A0h**
USB1	**0F91 82A0h**

Figure 14-9404. USB2SS_PHY2_UTMI_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_TERM	HS_TERM_EN	HSTX_DATA	HSTX_DATA_EN	HSTX_DRV	HSTX_DRV_EN	HSTX_PREDRV	HSTX_PREDRV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28379. USB2SS_PHY2_UTMI_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_TERM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HS_TERM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28379. USB2SS_PHY2_UTMI_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HSTX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HSTX_PREDRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_PREDRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.176 USB2SS_PHY2_UTMI_REG9 Register

1 USB2SS_PHY2_UTMI_REG9 Register (Offset = 2A4h) [reset = 0h]

hs delay values

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Table 14-28380. Instance Table

Instance Name	Physical Address
USB0	**0F90 82A4h**
USB1	**0F91 82A4h**

Figure 14-9405. USB2SS_PHY2_UTMI_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLKOFF_EN	SDC_SPACE			SDC_SPACE_EN	HSTX_EN_DEL_TH		HSTX_EN_DEL_TH_EN
R/W	R/W			R/W	R/W		R/W
0h	0h			0h	0h		0h

Table 14-28382. USB2SS_PHY2_UTMI_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLKOFF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:4	SDC_SPACE	R/W	0h	000- The time between successive resistor calibration is 0ms, 001- The time between successive resistor calibration is 500ms, 010- The time between successive resistor calibration is 1000ms, 011- The time between successive resistor calibration is1500ms, 100- The time between successive resistor calibration is 2000ms, 101- The time between successive resistor calibration is 2500ms, 110- The time between successive resistor calibration is 3000ms, 111- The time between successive resistor calibration is 3500ms. Reset Source: usb2_sync_preset_n
3	SDC_SPACE_EN	R/W	0h	0- The time between successive resistor calibration taken as 1s by default, 1- The time between successive resistor calibration taken from UTMI_REG9[6:4]. Reset Source: usb2_sync_preset_n
2:1	HSTX_EN_DEL_TH	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28382. USB2SS_PHY2_UTMI_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSTX_EN_DEL_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.177 USB2SS_PHY2_UTMI_REG10 Register

1 USB2SS_PHY2_UTMI_REG10 Register (Offset = 2A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28383. Instance Table

Instance Name	Physical Address
USB0	**0F90 82A8h**
USB1	**0F91 82A8h**

Figure 14-9406. USB2SS_PHY2_UTMI_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_CLKON	PLL_CLKON_EN	BG_PD_BG_OK	BG_PD_BG_OK_EN	LSFS_SERX	LSFS_SERX_EN	LSFS_RX	LSFS_RX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28385. USB2SS_PHY2_UTMI_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_CLKON_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BG_PD_BG_OK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BG_PD_BG_OK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_SERX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28385. USB2SS_PHY2_UTMI_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LSFS_SERX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LSFS_RX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LSFS_RX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.178 USB2SS_PHY2_UTMI_REG11 Register

1 USB2SS_PHY2_UTMI_REG11 Register (Offset = 2ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28386. Instance Table

Instance Name	Physical Address
USB0	**0F90 82ACh**
USB1	**0F91 82ACh**

Figure 14-9407. USB2SS_PHY2_UTMI_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLEAN_LINESTATE_SERX_MASK_EN	SERX_MASK_EN	SERX_MASK_THRESHOLD		LSFS_TX	LSFS_TX_EN	FSLS_EDGESEL	FSLS_EDGESEL_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-28388. USB2SS_PHY2_UTMI_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLEAN_LINESTATE_SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	SERX_MASK_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_TX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LSFS_TX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28388. USB2SS_PHY2_UTMI_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSLS_EDGESEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FSLS_EDGESEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.179 USB2SS_PHY2_UTMI_REG12 Register

1 USB2SS_PHY2_UTMI_REG12 Register (Offset = 2B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28389. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B0h**
USB1	**0F91 82B0h**

Figure 14-9408. USB2SS_PHY2_UTMI_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SERX_BIAS_EN		FSLS_TX_DATA	FSLS_TX_DATA_EN	FSLS_TX_SE0	FSLS_TX_SE0_EN	FSLS_TX_DRV	FSLS_TX_DRV_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-28391. USB2SS_PHY2_UTMI_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SERX_BIAS_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	FSLS_TX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	FSLS_TX_SE0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	FSLS_TX_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28391. USB2SS_PHY2_UTMI_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSLS_TX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FSLS_TX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.180 USB2SS_PHY2_UTMI_REG13 Register

1 USB2SS_PHY2_UTMI_REG13 Register (Offset = 2B4h) [reset = 0h]

serial mode

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Table 14-28392. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B4h**
USB1	**0F91 82B4h**

Figure 14-9409. USB2SS_PHY2_UTMI_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FSLS_SERIALMODE_PULLUP2	FSLS_SERIALMODE_PULLUP2_EN	DM_PULLDOWN	DM_PULLDOWN_EN	DP_PULLDOWN	DP_PULLDOWN_EN	LANE_REVERSE	LANE_REVERSE_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28394. USB2SS_PHY2_UTMI_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLS_SERIALMODE_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FSLS_SERIALMODE_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DM_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DM_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DP_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28394. USB2SS_PHY2_UTMI_REG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DP_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LANE_REVERSE	R/W	0h	0- Polarity inversion of DP/DM is not done, 1- Polarity inversion of DP/DM is done Reset Source: usb2_sync_preset_n
0	LANE_REVERSE_EN	R/W	0h	0- Lane Reverse Value is taken from primary input portlane_reverse, 1- Lane Reverse Value taken from UTMI_REG13[1] Reset Source: usb2_sync_preset_n

14.9.3.2.2.181 USB2SS_PHY2_UTMI_REG14 Register

1 USB2SS_PHY2_UTMI_REG14 Register (Offset = 2B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28395. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B8h**
USB1	**0F91 82B8h**

Figure 14-9410. USB2SS_PHY2_UTMI_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DM_PULLUP2	DM_PULLUP2_EN	DP_PULLUP2	DP_PULLUP2_EN	DM_PULLUP1	DM_PULLUP1_EN	DP_PULLUP1	DP_PULLUP1_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28397. USB2SS_PHY2_UTMI_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DM_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28397. USB2SS_PHY2_UTMI_REG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DM_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DP_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.182 USB2SS_PHY2_UTMI_REG15 Register

1 USB2SS_PHY2_UTMI_REG15 Register (Offset = 2BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28398. Instance Table

Instance Name	Physical Address
USB0	**0F90 82BCh**
USB1	**0F91 82BCh**

Figure 14-9411. USB2SS_PHY2_UTMI_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TXVALID_GATE_THRESHOLD_FS		TXVALID_GATE_THRESHOLD_HS		TED_EN_VALUE	TED_EN_CNT	ED_EN_VALUE	ED_EN_CNT
R/W		R/W		R/W	R/W	R/W	R/W
0h		0h		0h	0h	0h	0h

Table 14-28400. USB2SS_PHY2_UTMI_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	TXVALID_GATE_THRESHOLD_FS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	TXVALID_GATE_THRESHOLD_HS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	TED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28400. USB2SS_PHY2_UTMI_REG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.183 USB2SS_PHY2_UTMI_REG16 Register

1 USB2SS_PHY2_UTMI_REG16 Register (Offset = 2C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28401. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C0h**
USB1	**0F91 82C0h**

Figure 14-9412. USB2SS_PHY2_UTMI_REG16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28403. USB2SS_PHY2_UTMI_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.184 USB2SS_PHY2_UTMI_REG17 Register

1 USB2SS_PHY2_UTMI_REG17 Register (Offset = 2C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-28404. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C4h**
USB1	**0F91 82C4h**

Figure 14-9413. USB2SS_PHY2_UTMI_REG17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SQUELCH_COUNT_IDLE		SQUELCH_COUNT_IDLE_EN	TX_SQ_CNT				TX_SQ_CNT_EN
R/W		R/W	R/W				R/W
0h		0h	0h				0h

Table 14-28406. USB2SS_PHY2_UTMI_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SQUELCH_COUNT_IDLE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SQUELCH_COUNT_IDLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	TX_SQ_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	TX_SQ_CNT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.185 USB2SS_PHY2_UTMI_REG18 Register

1 USB2SS_PHY2_UTMI_REG18 Register (Offset = 2C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28407. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C8h**
USB1	**0F91 82C8h**

Figure 14-9414. USB2SS_PHY2_UTMI_REG18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SLEEP_VALUE	SLEEP_EN	BIST_POWERUP	BIST_POWERUP_EN	POWERUP_EN	UNUSED	CLIPPER_EN	CLIPPER_EN_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28409. USB2SS_PHY2_UTMI_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	SLEEP_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SLEEP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BIST_POWERUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIST_POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28409. USB2SS_PHY2_UTMI_REG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CLIPPER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CLIPPER_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.186 USB2SS_PHY2_UTMI_REG19 Register

1 USB2SS_PHY2_UTMI_REG19 Register (Offset = 2CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28410. Instance Table

Instance Name	Physical Address
USB0	**0F90 82CCh**
USB1	**0F91 82CCh**

Figure 14-9415. USB2SS_PHY2_UTMI_REG19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							TED_SW_EN
R/W							R/W
0h							0h

Table 14-28412. USB2SS_PHY2_UTMI_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
0	TED_SW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.187 USB2SS_PHY2_UTMI_REG20 Register

1 USB2SS_PHY2_UTMI_REG20 Register (Offset = 2D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28413. Instance Table

Instance Name	Physical Address
USB0	**0F90 82D0h**
USB1	**0F91 82D0h**

Figure 14-9416. USB2SS_PHY2_UTMI_REG20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HOSTDISCON_RST_REG	HOSTDISCON_RST_REG_EN	CALIB_RST_DT					CALIB_RST_DT_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-28415. USB2SS_PHY2_UTMI_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HOSTDISCON_RST_REG	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HOSTDISCON_RST_REG_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	CALIB_RST_DT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_RST_DT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.188 USB2SS_PHY2_UTMI_REG21 Register

1 USB2SS_PHY2_UTMI_REG21 Register (Offset = 2D4h) [reset = 0h]

Register UTMI_REG21

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Table 14-28416. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 82D4h**
USB1	**0F91 82D4h**

Figure 14-9417. USB2SS_PHY2_UTMI_REG21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_TRIGER_POSEDGE	AUTO_CAL_ENABLE	ABSVALID	ABSVALID_EN	VBUSVALID	VBUSVALID_EN	SUSPENDM	SUSPENDM_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28418. USB2SS_PHY2_UTMI_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_TRIGER_POSEDGE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AUTO_CAL_ENABLE	R/W	0h	0- Dynamic resistor calibration is disabled, 1- Dynamic resistor calibration is enabled Reset Source: usb2_sync_preset_n
5	ABSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ABSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28418. USB2SS_PHY2_UTMI_REG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	VBUSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SUSPENDM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SUSPENDM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.189 USB2SS_PHY2_UTMI_REG22 Register

1 USB2SS_PHY2_UTMI_REG22 Register (Offset = 2D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28419. Instance Table

Instance Name	Physical Address
USB0	**0F90 82D8h**
USB1	**0F91 82D8h**

Figure 14-9418. USB2SS_PHY2_UTMI_REG22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BCCALIB_OFFSET							
R/W							
0h							

Table 14-28421. USB2SS_PHY2_UTMI_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BCCALIB_OFFSET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.190 USB2SS_PHY2_UTMI_REG23 Register

1 USB2SS_PHY2_UTMI_REG23 Register (Offset = 2DCh) [reset = 0h]

hscalib code offset

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Table 14-28422. Instance Table

Instance Name	Physical Address
USB0	**0F90 82DCh**
USB1	**0F91 82DCh**

Figure 14-9419. USB2SS_PHY2_UTMI_REG23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HSCALIB_OFFSET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28424. USB2SS_PHY2_UTMI_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to HSTX is not offsetted, 1- Offset given by bits [6:2] is considered for computation of final resistor code going to HSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the resistor calibration code before giving the code to HSTX, 1- Subtract the offset given in bits [6:2] from the reistor calibration code before giving code to HSTX. Bits 6:2= 00000 Programmable offset value for hs resistor calib code -HS OFFSET. Bit 7= reserved Reset Source: usb2_sync_preset_n

14.9.3.2.2.191 USB2SS_PHY2_UTMI_REG24 Register

1 USB2SS_PHY2_UTMI_REG24 Register (Offset = 2E0h) [reset = 0h]

fscalib code offset

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Table 14-28425. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E0h**
USB1	**0F91 82E0h**

Figure 14-9420. USB2SS_PHY2_UTMI_REG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSCALIB_OFFSET							
R/W							
0h							

Table 14-28427. USB2SS_PHY2_UTMI_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to FSTX is not offsetted, 1- Offset given by bits [6:2] is used for computation of final resistor code going to FSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the Resistor calibration code before giving the code to FSTX, 1- Subtract the offset given in bits [6:2] from the Resistor calibration code before giving code to FSTX. Bits 6:2= 00000 Programmable offset value for fs resistor calib code - FS OFFSET. Bit 7= reserved. Reset Source: usb2_sync_preset_n

14.9.3.2.2.192 USB2SS_PHY2_UTMI_REG25 Register

1 USB2SS_PHY2_UTMI_REG25 Register (Offset = 2E4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-28428. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E4h**
USB1	**0F91 82E4h**

Figure 14-9421. USB2SS_PHY2_UTMI_REG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	HSCALIB						
R/W	R/W						
0h	0h						

Table 14-28430. USB2SS_PHY2_UTMI_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	HSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.193 USB2SS_PHY2_UTMI_REG26 Register

1 USB2SS_PHY2_UTMI_REG26 Register (Offset = 2E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28431. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E8h**
USB1	**0F91 82E8h**

Figure 14-9422. USB2SS_PHY2_UTMI_REG26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	FSCALIB						
R/W	R/W						
0h	0h						

Table 14-28433. USB2SS_PHY2_UTMI_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	FSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.194 USB2SS_PHY2_UTMI_REG27 Register

1 USB2SS_PHY2_UTMI_REG27 Register (Offset = 2ECh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28434. Instance Table

Instance Name	Physical Address
USB0	**0F90 82ECh**
USB1	**0F91 82ECh**

Figure 14-9423. USB2SS_PHY2_UTMI_REG27 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>UNUSED</td><td colspan="7">BCCALIB</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-28436. USB2SS_PHY2_UTMI_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	BCCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.195 USB2SS_PHY2_UTMI_REG28 Register

1 USB2SS_PHY2_UTMI_REG28 Register (Offset = 2F0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28437. Instance Table

Instance Name	Physical Address
USB0	**0F90 82F0h**
USB1	**0F91 82F0h**

Figure 14-9424. USB2SS_PHY2_UTMI_REG28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CDR_EB_WR_RESET	UNUSED						SERX_EN_CNTRL_OPMODE01
R/W	R/W						R/W
0h	0h						0h

Table 14-28439. USB2SS_PHY2_UTMI_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CDR_EB_WR_RESET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:1	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SERX_EN_CNTRL_OPMODE01	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.196 USB2SS_PHY2_UTMI_REG29 Register

1 USB2SS_PHY2_UTMI_REG29 Register (Offset = 2F4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28440. Instance Table

Instance Name	Physical Address
USB0	**0F90 82F4h**
USB1	**0F91 82F4h**

Figure 14-9425. USB2SS_PHY2_UTMI_REG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		PLL_STANDALONE	PLL_STANDALONE_EN	SPARE_OUT			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

Table 14-28442. USB2SS_PHY2_UTMI_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_STANDALONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_STANDALONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SPARE_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.197 USB2SS_PHY2_UTMI_REG30 Register

1 USB2SS_PHY2_UTMI_REG30 Register (Offset = 2F8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28443. Instance Table

Instance Name	Physical Address
USB0	**0F90 82F8h**
USB1	**0F91 82F8h**

Figure 14-9426. USB2SS_PHY2_UTMI_REG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	PLL_480_CLOCK_GATE_OVR	SCAN_ATS_HS_CLOCK_GATE_OVR	VCO_PLL_CLOCK_GATE_OVR	DIG_DIV_REFCLOCK_GATE_OVR	FB_CLOCK_GATE_OVR	ANA_DIV_REFCLOCK_GATE_OVR	HS_CLOCK_GATE_OVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28445. USB2SS_PHY2_UTMI_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	PLL_480_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SCAN_ATS_HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	VCO_PLL_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DIG_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28445. USB2SS_PHY2_UTMI_REG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	FB_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ANA_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.198 USB2SS_PHY2_UTMI_UNUSED_REG0 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG0 Register (Offset = 2FCh) [reset = 0h]

unused

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Table 14-28446. Instance Table

Instance Name	Physical Address
USB0	**0F90 82FCh**
USB1	**0F91 82FCh**

Figure 14-9427. USB2SS_PHY2_UTMI_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28448. USB2SS_PHY2_UTMI_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.199 USB2SS_PHY2_UTMI_UNUSED_REG1 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG1 Register (Offset = 300h) [reset = 0h]

unused

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Table 14-28449. Instance Table

Instance Name	Physical Address
USB0	**0F90 8300h**
USB1	**0F91 8300h**

Figure 14-9428. USB2SS_PHY2_UTMI_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28451. USB2SS_PHY2_UTMI_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.200 USB2SS_PHY2_UTMI_UNUSED_REG2 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG2 Register (Offset = 304h) [reset = 0h]

unused

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Table 14-28452. Instance Table

Instance Name	Physical Address
USB0	**0F90 8304h**
USB1	**0F91 8304h**

Figure 14-9429. USB2SS_PHY2_UTMI_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28454. USB2SS_PHY2_UTMI_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.201 USB2SS_PHY2_UTMI_UNUSED_REG3 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG3 Register (Offset = 308h) [reset = 0h]

unused

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Table 14-28455. Instance Table

Instance Name	Physical Address
USB0	**0F90 8308h**
USB1	**0F91 8308h**

Figure 14-9430. USB2SS_PHY2_UTMI_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-28457. USB2SS_PHY2_UTMI_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.202 USB2SS_PHY2_UTMI_REG31 Register

1 USB2SS_PHY2_UTMI_REG31 Register (Offset = 30Ch) [reset = 0h]

bist

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Table 14-28458. Instance Table

Instance Name	Physical Address
USB0	**0F90 830Ch**
USB1	**0F91 830Ch**

Figure 14-9431. USB2SS_PHY2_UTMI_REG31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">UNUSED</td><td>BIST_ERROR</td><td>BIST_COMPLETE</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28460. USB2SS_PHY2_UTMI_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
1	BIST_ERROR	R	0h	0- BIST resulted in no Error, 1- BIST resulted in Error Reset Source: usb2_sync_preset_n
0	BIST_COMPLETE	R	0h	0- BIST is Not complete, 1- BIST is Complete Reset Source: usb2_sync_preset_n

14.9.3.2.2.203 USB2SS_PHY2_UTMI_REG32 Register

1 USB2SS_PHY2_UTMI_REG32 Register (Offset = 310h) [reset = 0h]

bist error count

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Table 14-28461. Instance Table

Instance Name	Physical Address
USB0	**0F90 8310h**
USB1	**0F91 8310h**

Figure 14-9432. USB2SS_PHY2_UTMI_REG32 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_ERR_COUNT							
R							
0h							

Table 14-28463. USB2SS_PHY2_UTMI_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BIST_ERR_COUNT	R	0h	00000000 Number of bytes that resulted in error while running BIST Reset Source: usb2_sync_preset_n

14.9.3.2.2.204 USB2SS_PHY2_UTMI_REG33 Register

1 USB2SS_PHY2_UTMI_REG33 Register (Offset = 314h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28464. Instance Table

Instance Name	Physical Address
USB0	**0F90 8314h**
USB1	**0F91 8314h**

Figure 14-9433. USB2SS_PHY2_UTMI_REG33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_POWERGOOD	AFE_HSRX_DIFF_DATA	HSRX_EN	HSRX_SAMPLER_ENABLE	CHIRP_MODE_EN	HSTX_EN	HSTX_EN_DELAYED	HSTX_BOOST_DEAMP_OFF
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28466. USB2SS_PHY2_UTMI_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BG_POWERGOOD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AFE_HSRX_DIFF_DATA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_SAMPLER_ENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CHIRP_MODE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28466. USB2SS_PHY2_UTMI_REG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HSTX_EN_DELAYED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_BOOST_DEAMP_OFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.205 USB2SS_PHY2_UTMI_REG34 Register

1 USB2SS_PHY2_UTMI_REG34 Register (Offset = 318h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28467. Instance Table

Instance Name	Physical Address
USB0	**0F90 8318h**
USB1	**0F91 8318h**

Figure 14-9434. USB2SS_PHY2_UTMI_REG34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DPRPU1_EN	O_DMRPU1_EN	O_DPRPU2_EN	O_DMRPU2_EN	O_DPRPD_EN	O_DMRPD_EN	O_OTGC_ID_PULLUP_EN	O_FS_EDGE_SEL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28469. USB2SS_PHY2_UTMI_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DPRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DMRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_DPRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_DMRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_DPRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28469. USB2SS_PHY2_UTMI_REG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_DMRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_OTGC_ID_PULLUP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_FS_EDGE_SEL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.206 USB2SS_PHY2_UTMI_REG35 Register

1 USB2SS_PHY2_UTMI_REG35 Register (Offset = 31Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28470. Instance Table

Instance Name	Physical Address
USB0	**0F90 831Ch**
USB1	**0F91 831Ch**

Figure 14-9435. USB2SS_PHY2_UTMI_REG35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
I_AFE_LSFSRX_ANA	O_LSFSTX_EN	O_LSFSDRV_EN	O_LSFS_DDI	O_ASSERT_SEZERO	O_LSFSRX_EN	O_SERX_EN	O_SERX_BIAS_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28472. USB2SS_PHY2_UTMI_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_AFE_LSFSRX_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_LSFSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_LSFSDRV_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_LSFS_DDI	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_ASSERT_SEZERO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28472. USB2SS_PHY2_UTMI_REG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_LSFSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_SERX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_SERX_BIAS_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.207 USB2SS_PHY2_UTMI_REG36 Register

1 USB2SS_PHY2_UTMI_REG36 Register (Offset = 320h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28473. Instance Table

Instance Name	Physical Address
USB0	**0F90 8320h**
USB1	**0F91 8320h**

Figure 14-9436. USB2SS_PHY2_UTMI_REG36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_PSO	O_PLL_PSO_DELAY	O_PLL_PD	O_PLL_IPDIV				
R	R	R	R				
0h	0h	0h	0h				

Table 14-28475. USB2SS_PHY2_UTMI_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_PSO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_PSO_DELAY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	O_PLL_IPDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.208 USB2SS_PHY2_UTMI_REG37 Register

1 USB2SS_PHY2_UTMI_REG37 Register (Offset = 324h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28476. Instance Table

Instance Name	Physical Address
USB0	**0F90 8324h**
USB1	**0F91 8324h**

Figure 14-9437. USB2SS_PHY2_UTMI_REG37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_FBDIV_VALUE							
R							
0h							

Table 14-28478. USB2SS_PHY2_UTMI_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	O_PLL_FBDIV_VALUE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.209 USB2SS_PHY2_UTMI_REG38 Register

1 USB2SS_PHY2_UTMI_REG38 Register (Offset = 328h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28479. Instance Table

Instance Name	Physical Address
USB0	**0F90 8328h**
USB1	**0F91 8328h**

Figure 14-9438. USB2SS_PHY2_UTMI_REG38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_STANDBY	O_PLL_LDO_CORE_EN	O_PLL_LDO_REF_EN	O_AFE_SUSPENDM	O_OTGC_VBUSVALID_EN	O_OTGC_ABSVALID_EN	O_AFE_CLIPPER_EN	O_PLL_LDO_ISOLATION_CNTRL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28481. USB2SS_PHY2_UTMI_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_STANDBY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_LDO_CORE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_LDO_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_AFE_SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_OTGC_VBUSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28481. USB2SS_PHY2_UTMI_REG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_OTGC_ABSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_AFE_CLIPPER_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_PLL_LDO_ISOLATION_CNTRL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.210 USB2SS_PHY2_UTMI_REG39 Register

1 USB2SS_PHY2_UTMI_REG39 Register (Offset = 32Ch) [reset = 0h]

unused

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Table 14-28482. Instance Table

Instance Name	Physical Address
USB0	**0F90 832Ch**
USB1	**0F91 832Ch**

Figure 14-9439. USB2SS_PHY2_UTMI_REG39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-28484. USB2SS_PHY2_UTMI_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.211 USB2SS_PHY2_UTMI_REG40 Register

1 USB2SS_PHY2_UTMI_REG40 Register (Offset = 330h) [reset = 0h]

unused

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Table 14-28485. Instance Table

Instance Name	Physical Address
USB0	**0F90 8330h**
USB1	**0F91 8330h**

Figure 14-9440. USB2SS_PHY2_UTMI_REG40 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28487. USB2SS_PHY2_UTMI_REG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.212 USB2SS_PHY2_UTMI_REG41 Register

1 USB2SS_PHY2_UTMI_REG41 Register (Offset = 334h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28488. Instance Table

Instance Name	Physical Address
USB0	**0F90 8334h**
USB1	**0F91 8334h**

Figure 14-9441. USB2SS_PHY2_UTMI_REG41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
I_TED_SQUELCH_ANA	I_USB2_RESCAL_CALIB_DONE	HS_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-28490. USB2SS_PHY2_UTMI_REG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_TED_SQUELCH_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_USB2_RESCAL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	HS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.213 USB2SS_PHY2_UTMI_REG42 Register

1 USB2SS_PHY2_UTMI_REG42 Register (Offset = 338h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28491. Instance Table

Instance Name	Physical Address
USB0	**0F90 8338h**
USB1	**0F91 8338h**

Figure 14-9442. USB2SS_PHY2_UTMI_REG42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS_SOF	ALL_CALIB_DONE	FS_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-28493. USB2SS_PHY2_UTMI_REG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_SOF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ALL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	FS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.214 USB2SS_PHY2_UTMI_REG43 Register

1 USB2SS_PHY2_UTMI_REG43 Register (Offset = 33Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28494. Instance Table

Instance Name	Physical Address
USB0	**0F90 833Ch**
USB1	**0F91 833Ch**

Figure 14-9443. USB2SS_PHY2_UTMI_REG43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LS_MODE	FS_MODE_PRE	BC_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-28496. USB2SS_PHY2_UTMI_REG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LS_MODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FS_MODE_PRE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	BC_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.215 USB2SS_PHY2_UTMI_REG44 Register

1 USB2SS_PHY2_UTMI_REG44 Register (Offset = 340h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28497. Instance Table

Instance Name	Physical Address
USB0	**0F90 8340h**
USB1	**0F91 8340h**

Figure 14-9444. USB2SS_PHY2_UTMI_REG44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RSTN_REFCLOCK	RSTN_HS_CLOCK	RSTN_HS_TX_CLOCK	RSTN_BYTE_CLOCK	RSTN_SIECLOCK	RSTN_CLKDIV	RSTN_CALIB_CLKDIV	UDC_RSTN_CDR_ASYNC
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28499. USB2SS_PHY2_UTMI_REG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RSTN_REFCLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RSTN_HS_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RSTN_HS_TX_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RSTN_BYTE_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RSTN_SIECLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28499. USB2SS_PHY2_UTMI_REG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RSTN_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RSTN_CALIB_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UDC_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.216 USB2SS_PHY2_UTMI_REG45 Register

1 USB2SS_PHY2_UTMI_REG45 Register (Offset = 344h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28500. Instance Table

Instance Name	Physical Address
USB0	**0F90 8344h**
USB1	**0F91 8344h**

Figure 14-9445. USB2SS_PHY2_UTMI_REG45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UDC_CALIB_RSTN	UDC_APB_RSTN	O_RSTN_CDR_ASYNC	O_PLL_CALIB_RSTN	BIST_MODE_RSTN	O_USB2_CALIB_RSTN	UDC_BC_CALIB_RSTN	GLOBAL_RESETN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28502. USB2SS_PHY2_UTMI_REG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UDC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	UDC_APB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_PLL_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BIST_MODE_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28502. USB2SS_PHY2_UTMI_REG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_USB2_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	UDC_BC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	GLOBAL_RESETN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.217 USB2SS_PHY2_UTMI_REG46 Register

1 USB2SS_PHY2_UTMI_REG46 Register (Offset = 348h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28503. Instance Table

Instance Name	Physical Address
USB0	**0F90 8348h**
USB1	**0F91 8348h**

Figure 14-9446. USB2SS_PHY2_UTMI_REG46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	RECOVERY_CNT_EN	CLEAN_LINESTATE		BC_STATE_MACHINE_STATUS			
R	R	R		R			
0h	0h	0h		0h			

Table 14-28505. USB2SS_PHY2_UTMI_REG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
6	RECOVERY_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	CLEAN_LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	BC_STATE_MACHINE_STATUS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.218 USB2SS_PHY2_UTMI_REG47 Register

1 USB2SS_PHY2_UTMI_REG47 Register (Offset = 34Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28506. Instance Table

Instance Name	Physical Address
USB0	**0F90 834Ch**
USB1	**0F91 834Ch**

Figure 14-9447. USB2SS_PHY2_UTMI_REG47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FILTER_CNT_EN	HOST_OPMODE		DEV_OPMODE		I_DED_ANA	HS_HOSTDISCONNECT	LSFS_HOSTDISCONNECT
R	R		R		R	R	R
0h	0h		0h		0h	0h	0h

Table 14-28508. USB2SS_PHY2_UTMI_REG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FILTER_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	HOST_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	DEV_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	I_DED_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28508. USB2SS_PHY2_UTMI_REG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LSFS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.219 USB2SS_PHY2_UTMI_REG48 Register

1 USB2SS_PHY2_UTMI_REG48 Register (Offset = 350h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28509. Instance Table

Instance Name	Physical Address
USB0	**0F90 8350h**
USB1	**0F91 8350h**

Figure 14-9448. USB2SS_PHY2_UTMI_REG48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_TX_STATE		DATA_CNT_TX					
R		R					
0h		0h					

Table 14-28511. USB2SS_PHY2_UTMI_REG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_TX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.220 USB2SS_PHY2_UTMI_REG49 Register

1 USB2SS_PHY2_UTMI_REG49 Register (Offset = 354h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28512. Instance Table

Instance Name	Physical Address
USB0	**0F90 8354h**
USB1	**0F91 8354h**

Figure 14-9449. USB2SS_PHY2_UTMI_REG49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_RX_STATE		DATA_CNT_RX					
R		R					
0h		0h					

Table 14-28514. USB2SS_PHY2_UTMI_REG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_RX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.221 USB2SS_PHY2_UTMI_REG50 Register

1 USB2SS_PHY2_UTMI_REG50 Register (Offset = 358h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28515. Instance Table

Instance Name	Physical Address
USB0	0F90 8358h
USB1	0F91 8358h

Figure 14-9450. USB2SS_PHY2_UTMI_REG50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_TOP_STATE				INC_DATA_CNT_TX	INC_DATA_CNT_RX	O_BG_PD	O_BG_PD_BG_OK
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-28517. USB2SS_PHY2_UTMI_REG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	BIST_TOP_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	INC_DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	INC_DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_BG_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BG_PD_BG_OK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.222 USB2SS_PHY2_UTMI_REG51 Register

1 USB2SS_PHY2_UTMI_REG51 Register (Offset = 35Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28518. Instance Table

Instance Name	Physical Address
USB0	**0F90 835Ch**
USB1	**0F91 835Ch**

Figure 14-9451. USB2SS_PHY2_UTMI_REG51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POWERDOWN		RESET	SUSPENDM	TERMSELECT	DATABUS16_8	DPPULLDOWN	DMPULLDOWN
R		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-28520. USB2SS_PHY2_UTMI_REG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	POWERDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RESET	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TERMSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DATABUS16_8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DPPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28520. USB2SS_PHY2_UTMI_REG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.223 USB2SS_PHY2_UTMI_REG52 Register

1 USB2SS_PHY2_UTMI_REG52 Register (Offset = 360h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28521. Instance Table

Instance Name	Physical Address
USB0	**0F90 8360h**
USB1	**0F91 8360h**

Figure 14-9452. USB2SS_PHY2_UTMI_REG52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LANE_REVERSE	TXBITSTUFFENABLE	TXBITSTUFFENABLEH	XCVRSELECT		LINESTATE		HOSTDISCONNECT
R	R	R	R		R		R
0h	0h	0h	0h		0h		0h

Table 14-28523. USB2SS_PHY2_UTMI_REG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LANE_REVERSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXBITSTUFFENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXBITSTUFFENABLEH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	XCVRSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28523. USB2SS_PHY2_UTMI_REG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.224 USB2SS_PHY2_UTMI_REG53 Register

1 USB2SS_PHY2_UTMI_REG53 Register (Offset = 364h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28524. Instance Table

Instance Name	Physical Address
USB0	**0F90 8364h**
USB1	**0F91 8364h**

Figure 14-9453. USB2SS_PHY2_UTMI_REG53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLSSERIALMODE	TX_ENABLE_N	TX_DAT	TX_SE0	SLEEPM	UNUSED	OPMODE	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	

Table 14-28526. USB2SS_PHY2_UTMI_REG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLSSERIALMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TX_ENABLE_N	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TX_DAT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_SE0	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	SLEEPM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28526. USB2SS_PHY2_UTMI_REG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.225 USB2SS_PHY2_UTMI_REG54 Register

1 USB2SS_PHY2_UTMI_REG54 Register (Offset = 368h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28527. Instance Table

Instance Name	Physical Address
USB0	**0F90 8368h**
USB1	**0F91 8368h**

Figure 14-9454. USB2SS_PHY2_UTMI_REG54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_DP	RX_DM	RX_RCV	UNUSED				
R	R	R	R				
0h	0h	0h	0h				

Table 14-28529. USB2SS_PHY2_UTMI_REG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_DP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RX_DM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RX_RCV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.226 USB2SS_PHY2_UTMI_REG55 Register

1 USB2SS_PHY2_UTMI_REG55 Register (Offset = 36Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28530. Instance Table

Instance Name	Physical Address
USB0	**0F90 836Ch**
USB1	**0F91 836Ch**

Figure 14-9455. USB2SS_PHY2_UTMI_REG55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TXVALIDH	TXVALID	TXREADY	RXVALIDH	RXVALID	RXACTIVE	RXERROR	UNUSED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28532. USB2SS_PHY2_UTMI_REG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXREADY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RXACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-28532. USB2SS_PHY2_UTMI_REG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RXERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.227 USB2SS_PHY2_UTMI_REG56 Register

1 USB2SS_PHY2_UTMI_REG56 Register (Offset = 370h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28533. Instance Table

Instance Name	Physical Address
USB0	**0F90 8370h**
USB1	**0F91 8370h**

Figure 14-9456. USB2SS_PHY2_UTMI_REG56 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATAIN_UPPER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28535. USB2SS_PHY2_UTMI_REG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.228 USB2SS_PHY2_UTMI_REG57 Register

1 USB2SS_PHY2_UTMI_REG57 Register (Offset = 374h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28536. Instance Table

Instance Name	Physical Address
USB0	**0F90 8374h**
USB1	**0F91 8374h**

Figure 14-9457. USB2SS_PHY2_UTMI_REG57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAIN_LOWER							
R							
0h							

Table 14-28538. USB2SS_PHY2_UTMI_REG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.229 USB2SS_PHY2_UTMI_REG58 Register

1 USB2SS_PHY2_UTMI_REG58 Register (Offset = 378h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28539. Instance Table

Instance Name	Physical Address
USB0	**0F90 8378h**
USB1	**0F91 8378h**

Figure 14-9458. USB2SS_PHY2_UTMI_REG58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATAOUT_UPPER							
R							
0h							

Table 14-28541. USB2SS_PHY2_UTMI_REG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.230 USB2SS_PHY2_UTMI_REG59 Register

1 USB2SS_PHY2_UTMI_REG59 Register (Offset = 37Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-28542. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 837Ch**
USB1	**0F91 837Ch**

Figure 14-9459. USB2SS_PHY2_UTMI_REG59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAOUT_LOWER							
R							
0h							

Table 14-28544. USB2SS_PHY2_UTMI_REG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.3.2.2.231 USB2SS_PHY2_UTMI_UNUSED_REG6 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG6 Register (Offset = 380h) [reset = 0h]

UNUSED

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Table 14-28545. Instance Table

Instance Name	Physical Address
USB0	**0F90 8380h**
USB1	**0F91 8380h**

Figure 14-9460. USB2SS_PHY2_UTMI_UNUSED_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-28547. USB2SS_PHY2_UTMI_UNUSED_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.232 USB2SS_PHY2_UTMI_UNUSED_REG7 Register

1 USB2SS_PHY2_UTMI_UNUSED_REG7 Register (Offset = 384h) [reset = 0h]

UNUSED

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Table 14-28548. Instance Table

Instance Name	Physical Address
USB0	**0F90 8384h**
USB1	**0F91 8384h**

Figure 14-9461. USB2SS_PHY2_UTMI_UNUSED_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-28550. USB2SS_PHY2_UTMI_UNUSED_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3.2.2.233 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-28551. Instance Table

Instance Name	Physical Address
USB0	**0F98 0000h**
USB1	**0F99 0000h**

Figure 14-9462. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-28553. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.3.2.2.234 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-28554. Instance Table

Instance Name	**Physical Address**
USB0	**0F98 0008h**
USB1	**0F99 0008h**

Figure 14-9463. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-28556. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.3.2.2.235 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2h]

Misc Status

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Table 14-28557. Instance Table

Instance Name	Physical Address
USB0	**0F98 000Ch**
USB1	**0F99 000Ch**

Figure 14-9464. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					2h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
2h							

Table 14-28559. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.3.2.2.236 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-28560. Instance Table

Instance Name	Physical Address
USB0	**0F98 0010h + formula**
USB1	**0F99 0010h + formula**

Figure 14-9465. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-28562. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.3.2.2.237 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-28563. Instance Table

Instance Name	Physical Address
USB0	**0F98 003Ch**
USB1	**0F99 003Ch**

Figure 14-9466. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-28565. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.2.2.238 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-28566. Instance Table

Instance Name	Physical Address
USB0	**0F98 0040h**
USB1	**0F99 0040h**

Figure 14-9467. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_PEND	RAMECC_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-28568. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ctrl_ram0_pend
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.9.3.2.2.239 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-28569. Instance Table

Instance Name	Physical Address
USB0	**0F98 0080h**
USB1	**0F99 0080h**

Figure 14-9468. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_SET	RAMECC_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-28571. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.9.3.2.2.240 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-28572. Instance Table

Instance Name	Physical Address
USB0	**0F98 00C0h**
USB1	**0F99 00C0h**

Figure 14-9469. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_CLR	RAMECC_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-28574. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.9.3.2.2.241 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-28575. Instance Table

Instance Name	Physical Address
USB0	**0F98 013Ch**
USB1	**0F99 013Ch**

Figure 14-9470. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-28577. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.2.2.242 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-28578. Instance Table

Instance Name	Physical Address
USB0	**0F98 0140h**
USB1	**0F99 0140h**

Figure 14-9471. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_PEND	RAMECC_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-28580. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ctrl_ram0_pend
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.9.3.2.2.243 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-28581. Instance Table

Instance Name	Physical Address
USB0	**0F98 0180h**
USB1	**0F99 0180h**

Figure 14-9472. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_SET	RAMECC_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-28583. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.9.3.2.2.244 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-28584. Instance Table

Instance Name	Physical Address
USB0	**0F98 01C0h**
USB1	**0F99 01C0h**

Figure 14-9473. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MEM_CTRL_RAM0_ENABLE_CLR	RAMECC_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-28586. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.9.3.2.2.245 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-28587. Instance Table

Instance Name	Physical Address
USB0	**0F98 0200h**
USB1	**0F99 0200h**

Figure 14-9474. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-28589. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.3.2.2.246 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-28590. Instance Table

Instance Name	Physical Address
USB0	**0F98 0204h**
USB1	**0F99 0204h**

Figure 14-9475. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-28592. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.3.2.2.247 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-28593. Instance Table

Instance Name	Physical Address
USB0	**0F98 0208h**
USB1	**0F99 0208h**

Figure 14-9476. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-28595. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.3.2.2.248 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-28596. Instance Table

Instance Name	Physical Address
USB0	**0F98 020Ch**
USB1	**0F99 020Ch**

Figure 14-9477. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-28598. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.3.2.2.249 USB2SS_CAP_CAPLENGTH Register

1 USB2SS_CAP_CAPLENGTH Register (Offset = 0h) [reset = 1100020h]

Capability Registers Length Host Controller Operational Registers = Base address + CAPLENGTH where CAPLENGTH is DWC_USB3_HOST_CAP_REG_LEN whose default value is 20h.

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Table 14-28599. Instance Table

Instance Name	Physical Address
USB0	**3100 0000h**
USB1	**3110 0000h**

Figure 14-9478. USB2SS_CAP_CAPLENGTH Name Register

31	30	29	28	27	26	25	24
HCIVERSION							
R							
110h							
23	22	21	20	19	18	17	16
HCIVERSION							
R							
110h							
15	14	13	12	11	10	9	8
RESERVED_15_8							
R							
0h							
7	6	5	4	3	2	1	0
CAPLENGTH							
R							
20h							

Table 14-28601. USB2SS_CAP_CAPLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HCIVERSION	R	110h	HC Interface Version Number [HCIVERSION] Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	CAPLENGTH	R	20h	Capability Registers Length [CAPLENGTH] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.250 USB2SS_CAP_HCSPARAMS1 Register

1 USB2SS_CAP_HCSPARAMS1 Register (Offset = 4h) [reset = 1000840h]

Structural Parameters 1 Register For register definitions, refer to the xHCI specification.

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Table 14-28602. Instance Table

Instance Name	Physical Address
USB0	**3100 0004h**
USB1	**3110 0004h**

Figure 14-9479. USB2SS_CAP_HCSPARAMS1 Name Register

31	30	29	28	27	26	25	24
MAXPORTS							
R							
1h							
23	22	21	20	19	18	17	16
RESERVED_23_19					MAXINTRS		
R					R		
0h					8h		
15	14	13	12	11	10	9	8
MAXINTRS							
R							
8h							
7	6	5	4	3	2	1	0
MAXSLOTS							
R							
40h							

Table 14-28604. USB2SS_CAP_HCSPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAXPORTS	R	1h	Number of Ports [MaxPorts] - Number of ports implemented is defined by the parameter [DWC_USB3_HOST_NUM_U2_ROOT_PORTS + DWC_USB3_HOST_NUM_U3_ROOT_PORTS] - Number of ports enabled is controlled by the controller input signals host_num_u2_port[3:0]+host_num_u3_port[3:0] Note: In USB 2.0-only mode, the host_num_u3_port signal is zero. Reset Source: rst_mod_g_rst_n
23:19	RESERVED_23_19	R	0h	Reserved
18:8	MAXINTRS	R	8h	Number of Interrupters [MaxIntrs] Defined by the configurable parameter DWC_USB3_HOST_NUM_INTERRUPTER_SUPT Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTS	R	40h	Number of device slots [MaxSlots] Defined by configurable parameter DWC_USB3_NUM_DEVICE_SUPT Reset Source: rst_mod_g_rst_n

14.9.3.2.2.251 USB2SS_CAP_HCSPARAMS2 Register

1 USB2SS_CAP_HCSPARAMS2 Register (Offset = 8h) [reset = 140000F1h]

Structural Parameters 2 Register For register definitions, refer to the xHCI specification.

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Table 14-28605. Instance Table

Instance Name	Physical Address
USB0	**3100 0008h**
USB1	**3110 0008h**

Figure 14-9480. USB2SS_CAP_HCSPARAMS2 Name Register

31	30	29	28	27	26	25	24
MAXSCRATCHPADBUFS					SPR	MAXSCRATCHPADBUFS_HI	
R					R	R	
2h					1h	0h	
23	22	21	20	19	18	17	16
MAXSCRATCHPADBUFS_HI			RESERVED_20_8				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_20_8							
R							
0h							
7	6	5	4	3	2	1	0
ERSTMAX				IST			
R				R			
Fh				1h			

Table 14-28607. USB2SS_CAP_HCSPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	MAXSCRATCHPADBUFS	R	2h	Max Scratchpad Bufs Lo The value is calculated based on chosen configuration parameter values. Possible values are 1-4. Reset Source: rst_mod_g_rst_n
26	SPR	R	1h	Scratchpad Restore [SPR] Reset Source: rst_mod_g_rst_n
25:21	MAXSCRATCHPADBUFS_HI	R	0h	Max Scratchpad Bufs HI The controller automatically updates this field. Reset Source: rst_mod_g_rst_n
20:8	RESERVED_20_8	R	0h	Reserved
7:4	ERSTMAX	R	Fh	Event Ring Segment Table Max [ERST Max] Reset Source: rst_mod_g_rst_n
3:0	IST	R	1h	Isochronous Scheduling Threshold [IST] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.252 USB2SS_CAP_HCSPARAMS3 Register

1 USB2SS_CAP_HCSPARAMS3 Register (Offset = Ch) [reset = 7FF000Ah]

Structural Parameters 3 Register For register definitions, refer to the xHCI specification.

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Table 14-28608. Instance Table

Instance Name	Physical Address
USB0	**3100 000Ch**
USB1	**3110 000Ch**

Figure 14-9481. USB2SS_CAP_HCSPARAMS3 Name Register

31	30	29	28	27	26	25	24
U2_DEVICE_EXIT_LAT							
R							
7FFh							
23	22	21	20	19	18	17	16
U2_DEVICE_EXIT_LAT							
R							
7FFh							
15	14	13	12	11	10	9	8
RESERVED_15_8							
R							
0h							
7	6	5	4	3	2	1	0
U1_DEVICE_EXIT_LAT							
R							
Ah							

Table 14-28610. USB2SS_CAP_HCSPARAMS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	U2_DEVICE_EXIT_LAT	R	7FFh	U2 Device Exit Latency Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	U1_DEVICE_EXIT_LAT	R	Ah	U1 Device Exit Latency Reset Source: rst_mod_g_rst_n

14.9.3.2.2.253 USB2SS_CAP_HCCPARAMS1 Register

1 USB2SS_CAP_HCCPARAMS1 Register (Offset = 10h) [reset = 258FE6Dh]

Capability Parameters 1 Register For register definitions, refer to the xHCI specification.

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Table 14-28611. Instance Table

Instance Name	Physical Address
USB0	**3100 0010h**
USB1	**3110 0010h**

Figure 14-9482. USB2SS_CAP_HCCPARAMS1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">XECP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">258h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">XECP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">258h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAXPSASIZE</td><td>CFC</td><td>SEC</td><td>SPC</td><td>PAE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">Fh</td><td>1h</td><td>1h</td><td>1h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NSS</td><td>LTC</td><td>LHRC</td><td>PIND</td><td>PPC</td><td>CSZ</td><td>BNC</td><td>AC64</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-28613. USB2SS_CAP_HCCPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XECP	R	258h	xHCI Extended Capabilities Pointer [xECP] Based on configuration, controller automatically updates it. Refer to <workspace>/src/DWC_usb3_params.v for details on DWC_USB3_HC_XECP. Reset Source: rst_mod_g_rst_n
15:12	MAXPSASIZE	R	Fh	Maximum Primary Stream Array Size [MaxPSASize] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
11	CFC	R	1h	Contiguous Frame ID Capability [CFC] Reset Source: rst_mod_g_rst_n
10	SEC	R	1h	Stopped EDLTA Capability [SEC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28613. USB2SS_CAP_HCCPARAMS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SPC	R	1h	Short Packet Capability [SPC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
8	PAE	R	0h	Parse All Event Data [PAE] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7	NSS	R	0h	No Secondary SID Support [NSS] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
6	LTC	R	1h	Latency Tolerance Messaging Capability [LTC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5	LHRC	R	1h	Light HC Reset Capability For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	PIND	R	0h	Port Indicators [PIND] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3	PPC	R	1h	Port Power Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	CSZ	R	1h	Context Size [CSZ] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	BNC	R	0h	BW Negotiation Capability [BNC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	AC64	R	1h	64-bit Addressing Capability [AC64] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.254 USB2SS_CAP_DBOFF Register

1 USB2SS_CAP_DBOFF Register (Offset = 14h) [reset = 560h]

Doorbell Offset Register For register definitions, refer to the xHCI specification.

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Table 14-28614. Instance Table

Instance Name	Physical Address
USB0	**3100 0014h**
USB1	**3110 0014h**

Figure 14-9483. USB2SS_CAP_DBOFF Name Register

31	30	29	28	27	26	25	24
DOORBELL_ARRAY_OFFSET							
R							
158h							
23	22	21	20	19	18	17	16
DOORBELL_ARRAY_OFFSET							
R							
158h							
15	14	13	12	11	10	9	8
DOORBELL_ARRAY_OFFSET							
R							
158h							
7	6	5	4	3	2	1	0
DOORBELL_ARRAY_OFFSET						RESERVED_1_0	
R						R	
158h						0h	

Table 14-28616. USB2SS_CAP_DBOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	DOORBELL_ARRAY_OFFSET	R	158h	Doorbell Array Offset - RO Based on configuration, the controller automatically updates it. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1:0	RESERVED_1_0	R	0h	Reserved

14.9.3.2.2.255 USB2SS_CAP_RTSOFF Register

1 USB2SS_CAP_RTSOFF Register (Offset = 18h) [reset = 440h]

Runtime Register Space Offset Register

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Table 14-28617. Instance Table

Instance Name	Physical Address
USB0	**3100 0018h**
USB1	**3110 0018h**

Figure 14-9484. USB2SS_CAP_RTSOFF Name Register

31	30	29	28	27	26	25	24
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
23	22	21	20	19	18	17	16
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
15	14	13	12	11	10	9	8
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
7	6	5	4	3	2	1	0
RUNTIME_REG_SPACE_OFFSET			RESERVED_4_0				
R			R				
22h			0h				

Table 14-28619. USB2SS_CAP_RTSOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RUNTIME_REG_SPACE_OFFSET	R	22h	Runtime Register Space Offset Based on configuration, the controller automatically updates it. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4:0	RESERVED_4_0	R	0h	Reserved

14.9.3.2.2.256 USB2SS_CAP_HCCPARAMS2 Register

1 USB2SS_CAP_HCCPARAMS2 Register (Offset = 1Ch) [reset = 2Fh]

Host Controller Capability Parameters 2 For register definitions, refer to the xHCI specification.

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Table 14-28620. Instance Table

Instance Name	Physical Address
USB0	**3100 001Ch**
USB1	**3110 001Ch**

Figure 14-9485. USB2SS_CAP_HCCPARAMS2 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_6							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_6							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_6							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_6		CIC	LEC	CTC	FSC	CMC	U3C
R		R	R	R	R	R	R
0h		1h	0h	1h	1h	1h	1h

Table 14-28622. USB2SS_CAP_HCCPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_31_6	R	0h	Reserved
5	CIC	R	1h	Configuration Information Capability [CIC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	LEC	R	0h	Large ESIT Payload Capability [LEC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3	CTC	R	1h	Compliance Transition Capability [CTC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	FSC	R	1h	Force Save Context Capability [FSC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28622. USB2SS_CAP_HCCPARAMS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CMC	R	1h	Configure Endpoint Command Max Exit Latency Too Large Capability [CMC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	U3C	R	1h	U3 Entry Capability [U3C] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.257 USB2SS_OPER_USBCMD Register

1 USB2SS_OPER_USBCMD Register (Offset = 0h) [reset = 0h]

USB Command Register For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28623. Instance Table

Instance Name	Physical Address
USB0	**3100 0020h**
USB1	**3110 0020h**

Figure 14-9486. USB2SS_OPER_USBCMD Name Register

31	30	29	28	27	26	25	24
RESERVED_31_14							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_14							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_31_14		CME	RESERVED_12	EU3S	EWE	CRS	CSS
R		R/W	R	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LHCRST	RESERVED_6_4			HSEE	INTE	HCRST	R_S
R/W	R			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Table 14-28625. USB2SS_OPER_USBCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved
13	CME	R/W	0h	CEM Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
12	RESERVED_12	R	0h	Reserved
11	EU3S	R/W	0h	EU3S For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
10	EWE	R/W	0h	EWE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28625. USB2SS_OPER_USBCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CRS	R/W	0h	Controller Restore State This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
8	CSS	R/W	0h	Controller Save State This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
7	LHCRST	R/W	0h	Light Host Controller Reset For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. The following bits reset the internal logic of the host controller. Under soft reset, some CSR accesses may fail [Timeout]. - HCRST - LHCRST Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
6:4	RESERVED_6_4	R	0h	Reserved
3	HSEE	R/W	0h	HSEE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	INTE	R/W	0h	INTE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	HCRST	R/W	0h	HCRST The following bits reset the internal logic of the host controller. Under soft reset, some CSR accesses may fail [Timeout]. - HCRST - LHCRST Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
0	R_S	R/W	0h	R_S For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Due to side-effects this reguster field is not recommended for Bit-Bash testing. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.258 USB2SS_OPER_USBSTS Register

1 USB2SS_OPER_USBSTS Register (Offset = 4h) [reset = 801h]

USB Status Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28626. Instance Table

Instance Name	Physical Address
USB0	**3100 0024h**
USB1	**3110 0024h**

Figure 14-9487. USB2SS_OPER_USBSTS Name Register

31	30	29	28	27	26	25	24
RESERVED_31_13							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_13							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_13			HCE	CNR	SRE	RSS	SSS
R			R	R	R/W1TC	R	R
0h			0h	1h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_7_5			PCD	EINT	HSE	RESERVED_1	HCH
R			R/W1TC	R/W1TC	R/W1TC	R	R
0h			0h	0h	0h	0h	1h

Table 14-28628. USB2SS_OPER_USBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12	HCE	R	0h	Host Controller Error [HCE] - RO Default = 0. '0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. This flag must be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of the Databook for more information. Reset Source: rst_mod_g_rst_n
11	CNR	R	1h	Controller Not Ready [CNR] - RO Default = '1'. '0' = Ready and '1' = Not Ready. Software must not write to thes Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag remains cleared ['0'] until the next Chip Hardware Reset. Reset Source: rst_mod_g_rst_n

Table 14-28628. USB2SS_OPER_USBSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SRE	R/W1TC	0h	Save/Restore Error This bit is currently not supported. Reset Source: rst_mod_g_rst_n
9	RSS	R	0h	Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the restore process, it completes the command by setting DSTS.RSS to '0'. Reset Source: rst_mod_g_rst_n
8	SSS	R	0h	Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to '0'. Reset Source: rst_mod_g_rst_n
7:5	RESERVED_7_5	R	0h	Reserved
4	PCD	R/W1TC	0h	Reset Value for PCD Reset Source: rst_mod_g_rst_n
3	EINT	R/W1TC	0h	Reset Value for EINT Reset Source: rst_mod_g_rst_n
2	HSE	R/W1TC	0h	HSE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.. Reset Source: rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved
0	HCH	R	1h	HCH For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.259 USB2SS_OPER_PAGESIZE Register

1 USB2SS_OPER_PAGESIZE Register (Offset = 8h) [reset = 1h]

Page Size Register Bit Definitions Use this register to enable or disable the reporting of specific USB Device Notification Transaction Packets being received. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event is generated when the respective notification packet is received. After reset, all notifications are disabled. Refer to section 6.4.2.7 of the Databook for more information. This register is written as a Dword. Byte writes produce undefined results.

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Table 14-28629. Instance Table

Instance Name	Physical Address
USB0	**3100 0028h**
USB1	**3110 0028h**

Figure 14-9488. USB2SS_OPER_PAGESIZE Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
PAGE_SIZE							
R							
1h							
7	6	5	4	3	2	1	0
PAGE_SIZE							
R							
1h							

Table 14-28631. USB2SS_OPER_PAGESIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	PAGE_SIZE	R	1h	PAGE_SIZE Reset Source: rst_mod_g_rst_n

14.9.3.2.2.260 USB2SS_OPER_DNCTRL Register

1 USB2SS_OPER_DNCTRL Register (Offset = 14h) [reset = 0h]

Device Notification Register Bit Definitions For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28632. Instance Table

Instance Name	Physical Address
USB0	**3100 0034h**
USB1	**3110 0034h**

Figure 14-9489. USB2SS_OPER_DNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
N0_N15							
R/W							
0h							
7	6	5	4	3	2	1	0
N0_N15							
R/W							
0h							

Table 14-28634. USB2SS_OPER_DNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	N0_N15	R/W	0h	N0_N15 For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.261 USB2SS_OPER_CRCR_LO Register

1 USB2SS_OPER_CRCR_LO Register (Offset = 18h) [reset = 0h]

CRCR_LO For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28635. Instance Table

Instance Name	Physical Address
USB0	**3100 0038h**
USB1	**3110 0038h**

Figure 14-9490. USB2SS_OPER_CRCR_LO Name Register

31	30	29	28	27	26	25	24
CMD_RING_PNTR							
W							
0h							
23	22	21	20	19	18	17	16
CMD_RING_PNTR							
W							
0h							
15	14	13	12	11	10	9	8
CMD_RING_PNTR							
W							
0h							
7	6	5	4	3	2	1	0
CMD_RING_PNTR		RESERVED_5_4		CRR	CA	CS	RCS
W		R		R	W	W	W
0h		0h		0h	0h	0h	0h

Table 14-28637. USB2SS_OPER_CRCR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	CMD_RING_PNTR	W	0h	CMD_RING_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5:4	RESERVED_5_4	R	0h	Reserved
3	CRR	R	0h	CRR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	CA	W	0h	CA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28637. USB2SS_OPER_CRCR_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CS	W	0h	CS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	RCS	W	0h	RCS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.262 USB2SS_OPER_CRCR_HI Register

1 USB2SS_OPER_CRCR_HI Register (Offset = 1Ch) [reset = 0h]

CRCR_HI

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Table 14-28638. Instance Table

Instance Name	Physical Address
USB0	**3100 003Ch**
USB1	**3110 003Ch**

Figure 14-9491. USB2SS_OPER_CRCR_HI Name Register

31	30	29	28	27	26	25	24
CMD_RING_PNTR							
W							
0h							
23	22	21	20	19	18	17	16
CMD_RING_PNTR							
W							
0h							
15	14	13	12	11	10	9	8
CMD_RING_PNTR							
W							
0h							
7	6	5	4	3	2	1	0
CMD_RING_PNTR							
W							
0h							

Table 14-28640. USB2SS_OPER_CRCR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMD_RING_PNTR	W	0h	COMMAND_RING_POINTER Reading this field always returns '0'. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.263 USB2SS_OPER_DCBAAP_LO Register

1 USB2SS_OPER_DCBAAP_LO Register (Offset = 30h) [reset = 0h]

DCBAAP_LO

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Table 14-28641. Instance Table

Instance Name	Physical Address
USB0	**3100 0050h**
USB1	**3110 0050h**

Figure 14-9492. USB2SS_OPER_DCBAAP_LO Name Register

31	30	29	28	27	26	25	24
DEVICE_CONTEXT_BAAP							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVICE_CONTEXT_BAAP							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVICE_CONTEXT_BAAP							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVICE_CONTEXT_BAAP		RESERVED_5_0					
R/W		R					
0h		0h					

Table 14-28643. USB2SS_OPER_DCBAAP_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	DEVICE_CONTEXT_BAAP	R/W	0h	DEVICE_CONTEXT_BAAP For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5:0	RESERVED_5_0	R	0h	Reserved

14.9.3.2.2.264 USB2SS_OPER_DCBAAP_HI Register

1 USB2SS_OPER_DCBAAP_HI Register (Offset = 34h) [reset = 0h]

DCBAAP_HI For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28644. Instance Table

Instance Name	Physical Address
USB0	**3100 0054h**
USB1	**3110 0054h**

Figure 14-9493. USB2SS_OPER_DCBAAP_HI Name Register

31	30	29	28	27	26	25	24
DEVICE_CONTEXT_BAAP							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVICE_CONTEXT_BAAP							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVICE_CONTEXT_BAAP							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVICE_CONTEXT_BAAP							
R/W							
0h							

Table 14-28646. USB2SS_OPER_DCBAAP_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVICE_CONTEXT_BAAP	R/W	0h	DEVICE_CONTEXT_BAAP Reset Source: rst_mod_g_rst_n

14.9.3.2.2.265 USB2SS_OPER_CONFIG Register

1 USB2SS_OPER_CONFIG Register (Offset = 38h) [reset = 0h]

Configure Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). The initial conditions of a port are described in section 4.19 of the Databook.

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Table 14-28647. Instance Table

Instance Name	Physical Address
USB0	**3100 0058h**
USB1	**3110 0058h**

Figure 14-9494. USB2SS_OPER_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_31_10							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_10							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_10						CIE	U3E
R						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
MAXSLOTSEN							
R/W							
0h							

Table 14-28649. USB2SS_OPER_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_31_10	R	0h	Reserved
9	CIE	R/W	0h	Configuration Information Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
8	U3E	R/W	0h	U3 Entry Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTSEN	R/W	0h	MAXSLOTSEN For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.266 USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register

1 USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register (Offset = 0h) [reset = 2A0h]

Port Status and Control Register Bit Definitions The PORTSC Register Access fails (Timeout) if the UTMI/ULPI clock is not running or one of the following bits is asserted. - PR - ORC

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Table 14-28650. Instance Table

Instance Name	Physical Address
USB0	**3100 0420h**
USB1	**3110 0420h**

Figure 14-9495. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Name Register

31	30	29	28	27	26	25	24
RESERVED_31	DR	RESERVED_29_28		WOE	WDE	WCE	CAS
R	R	R		R/W	R/W	R/W	R
0h	0h	0h		0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED_23	PLC	PRC	OCC	RESERVED_19	PEC	CSC	LWS
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PIC		PORTSPEED				PP	PLS
R/W		R				R/W	R/W
0h		0h				1h	5h
7	6	5	4	3	2	1	0
PLS			PR	OCA	RESERVED_2	PED	CCS
R/W			R/W1TS	R	R	R/W1TC	R
5h			0h	0h	0h	0h	0h

Table 14-28652. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Programming this field with random data will cause side effect i.e. Register Access will fail [Timeout] if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.
30	DR	R	0h	Reset Value For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
29:28	RESERVED_29_28	R	0h	Reserved
27	WOE	R/W	0h	WOE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28652. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	WDE	R/W	0h	WDE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
25	WCE	R/W	0h	WCE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24	CAS	R	0h	Cold Attach Status For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23	RESERVED_23	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
22	PLC	R/W1TC	0h	PLC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
21	PRC	R/W1TC	0h	PRC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
20	OCC	R/W1TC	0h	OCC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
19	RESERVED_19	R/W1TC	0h	WRC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
18	PEC	R/W1TC	0h	PEC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
17	CSC	R/W1TC	0h	CSC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
16	LWS	R/W	0h	LWS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28652. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	PIC	R/W	0h	PIC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
13:10	PORTSPEED	R	0h	PORTSPEED For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
9	PP	R/W	1h	PP For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
8:5	PLS	R/W	5h	PLS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	PR	R/W1TS	0h	PR set_register_field_attribute DWC_usb3_map/ DWC_usb3_block_Host_Cntrl_Port_Reg_Set/PORTSC_20_REGS/ PORTSC_20/PR VolatileMemory 1 Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
3	OCA	R	0h	OCA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved
1	PED	R/W1TC	0h	PED For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	CCS	R	0h	CCS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.267 USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register

1 USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register (Offset = 4h) [reset = 0h]

USB3 Port Power Management Status and Control Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-28653. Instance Table

Instance Name	Physical Address
USB0	**3100 0424h**
USB1	**3110 0424h**

Figure 14-9496. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">PRTTSTCTRL</td><td colspan="4">RESERVED_27_17</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED_27_17</td><td>HLE</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L1DSLOT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">HIRD</td><td>RWE</td><td colspan="3">L1S</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-28655. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRTTSTCTRL	R/W	0h	Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
27:17	RESERVED_27_17	R	0h	Reserved
16	HLE	R/W	0h	Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	L1DSLOT	R/W	0h	L1DSLOT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28655. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	HIRD	R/W	0h	Host Initiated Resume Duration [HIRD] - RW. Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it [the xHC] initiates an exit from L1. The HIRD value is encoded as follows: Value Description 0h 50us. [default] 1h 125us. 2h 200us. Fh 1.175 ms. The value of 0000b is interpreted as 50us. Each incrementing value up adds 75us. to the previous value. For example, 0001b is 125us, 0010b is 200us and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2ms. Note that the HIRD field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 for more information on HIRD use. Refer to Section 4.1 of the USB2 LPM spec for more information on the use of the HIRD field. Reset Source: rst_mod_g_rst_n
3	RWE	R/W	0h	RWE Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2:0	L1S	R	0h	L1 Status [L1S] - RO. Default = 0. This field is used by software to determine whether an L1-based suspend request [LMP transaction] was successful, specifically: Value Meaning 0 Invalid - This field is ignored by software. - 1 Success - Port successfully transitioned to L1 [ACK] - 2 Not Yet - Device is unable to enter L1 at this time [NYET] - 3 Not Supported -Device does not support L1 transitions [STALL] - 4 Timeout/Error -Device failed to respond to the LPM Transaction or an error occurred - 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state [PLS = '0' or '2']. Refer to section 4.23.5.1.1 for more information. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.268 USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register

1 USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register (Offset = 8h) [reset = 0h]

Port Link Info Register Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-28656. Instance Table

Instance Name	Physical Address
USB0	**3100 0428h**
USB1	**3110 0428h**

Figure 14-9497. USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28658. USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.9.3.2.2.269 USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register

1 USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register (Offset = Ch) [reset = 0h]

USB2 Port Hardware LPM Control Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28659. Instance Table

Instance Name	Physical Address
USB0	**3100 042Ch**
USB1	**3110 042Ch**

Figure 14-9498. USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_31_14</td><td colspan="4">HIRDD</td><td colspan="2">L1_TIMEOUT</td></tr>
<tr><td colspan="2">R</td><td colspan="4">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="4">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">L1_TIMEOUT</td><td colspan="2">HIRDM</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-28661. USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
13:10	HIRDD	R/W	0h	PORTHLPMC_20 HIRDD Reset Source: rst_mod_g_rst_n
9:2	L1_TIMEOUT	R/W	0h	PORTHLPMC_20 L1_TIMEOUT. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28661. USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	HIRDM	R/W	0h	Host Initiated Resume Duration Mode [HIRDM] - RWS. Default = 0h. Indicates which HIRD value must be used. The following are permissible values: Value Description 0 Initiate L1 using HIRD only on timeout. [default] 1 Initiate L1 using HIRDD on timeout. If rejected by device, initiate L1 using HIRD. 3-2 Reserved. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.270 USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register

1 USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register (Offset = 4h) [reset = 0h]

USB3 Port Power Management Status and Control Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

Return to Summary Table

Table 14-28662. Instance Table

Instance Name	Physical Address
USB0	**3100 0424h**
USB1	**3110 0424h**

Figure 14-9499. USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_17</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED_31_17</td><td>FLA</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">U2_TIMEOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">U1_TIMEOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28664. USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R	0h	Reserved
16	FLA	R/W	0h	FLA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	U2_TIMEOUT	R/W	0h	U2_TIMEOUT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	U1_TIMEOUT	R/W	0h	U1_TIMEOUT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.271 USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register

1 USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register (Offset = 8h) [reset = 0h]

Port Link Info Register Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

Return to Summary Table

Table 14-28665. Instance Table

Instance Name	Physical Address
USB0	**3100 0428h**
USB1	**3110 0428h**

Figure 14-9500. USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
LINK_ERROR_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
LINK_ERROR_COUNT							
R							
0h							

Table 14-28667. USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	LINK_ERROR_COUNT	R	0h	LINK_ERROR_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.272 USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register

1 USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register (Offset = Ch) [reset = 0h]

USB2 Port Hardware LPM Control Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Table 14-28668. Instance Table

Instance Name	Physical Address
USB0	**3100 042Ch**
USB1	**3110 042Ch**

Figure 14-9501. USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28670. USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.

14.9.3.2.2.273 USB2SS_RUNTIME_MFINDEX Register

1 USB2SS_RUNTIME_MFINDEX Register (Offset = 0h) [reset = 0h]

Microframe Index Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Table 14-28671. Instance Table

Instance Name	Physical Address
USB0	**3100 0440h**
USB1	**3110 0440h**

Figure 14-9502. USB2SS_RUNTIME_MFINDEX Name Register

31	30	29	28	27	26	25	24
RESERVED_31_14							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_14							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_14		MICROFRAME_INDEX					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
MICROFRAME_INDEX							
R							
0h							

Table 14-28673. USB2SS_RUNTIME_MFINDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved
13:0	MICROFRAME_INDEX	R	0h	MICROFRAME_INDEX For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.274 USB2SS_RUNTIME_RSVDZ Register

1 USB2SS_RUNTIME_RSVDZ Register (Offset = 4h) [reset = 0h]

RsvdZ For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Table 14-28674. Instance Table

Instance Name	Physical Address
USB0	**3100 0444h**
USB1	**3110 0444h**

Figure 14-9503. USB2SS_RUNTIME_RSVDZ Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28676. USB2SS_RUNTIME_RSVDZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.9.3.2.2.275 USB2SS_INTR_XHCI_INTR_IMAN_j Register

1 USB2SS_INTR_XHCI_INTR_IMAN_j Register (Offset = 0h + formula) [reset = 0h]

Interrupter Management Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Offset = 0h + (j * 20h); where j = 0 to 7d

Table 14-28677. Instance Table

Instance Name	Physical Address
USB0	**3100 0460h + formula**
USB1	**3110 0460h + formula**

Figure 14-9504. USB2SS_INTR_XHCI_INTR_IMAN_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_2						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-28679. USB2SS_INTR_XHCI_INTR_IMAN_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_31_2	R	0h	Reserved
1	IE	R/W	0h	IE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	IP Interrupt Pending For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.276 USB2SS_INTR_XHCI_INTR_IMOD_j Register

1 USB2SS_INTR_XHCI_INTR_IMOD_j Register (Offset = 4h + formula) [reset = FA0h]

Interrupter Moderation Register The software may use this register to pace (or even out) the delivery of interrupts to the host CPU. This register provides a guaranteed inter-interrupt delay between interrupts asserted by the xHC, regardless of USB traffic conditions. To independently validate configuration settings, software may use the following algorithm to convert the inter-interrupt Interval value to the common 'interrupts/sec' performance metric.

Return to Summary Table

Offset = 4h + (j * 20h); where j = 0 to 7d

Table 14-28680. Instance Table

Instance Name	Physical Address
USB0	**3100 0464h + formula**
USB1	**3110 0464h + formula**

Figure 14-9505. USB2SS_INTR_XHCI_INTR_IMOD_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
</table>

Table 14-28682. USB2SS_INTR_XHCI_INTR_IMOD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC] - RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt is signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n

Table 14-28682. USB2SS_INTR_XHCI_INTR_IMOD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI] - RW. Default = '4000' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts is generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.277 USB2SS_INTR_XHCI_INTR_ERSTSZ_j Register

1 USB2SS_INTR_XHCI_INTR_ERSTSZ_j Register (Offset = 8h + formula) [reset = 0h]

Event Ring Segment Table Size Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Offset = 8h + (j * 20h); where j = 0 to 7d

Table 14-28683. Instance Table

Instance Name	Physical Address
USB0	**3100 0468h + formula**
USB1	**3110 0468h + formula**

Figure 14-9506. USB2SS_INTR_XHCI_INTR_ERSTSZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
ERS_TABLE_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
ERS_TABLE_SIZE							
R/W							
0h							

Table 14-28685. USB2SS_INTR_XHCI_INTR_ERSTSZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	ERS_TABLE_SIZE	R/W	0h	ERS_TABLE_SIZE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.278 USB2SS_INTR_XHCI_INTR_RSVDP_j Register

1 USB2SS_INTR_XHCI_INTR_RSVDP_j Register (Offset = Ch + formula) [reset = 0h]

RsvdP

Return to Summary Table

Offset = Ch + (j * 20h); where j = 0 to 7d

Table 14-28686. Instance Table

Instance Name	Physical Address
USB0	3100 046Ch + formula
USB1	3110 046Ch + formula

Figure 14-9507. USB2SS_INTR_XHCI_INTR_RSVDP_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28688. USB2SS_INTR_XHCI_INTR_RSVDP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.9.3.2.2.279 USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Register

1 USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Register (Offset = 10h + formula) [reset = 0h]

ERSTBA_LO

Return to Summary Table

Offset = 10h + (j * 20h); where j = 0 to 7d

Table 14-28689. Instance Table

Instance Name	Physical Address
USB0	**3100 0470h + formula**
USB1	**3110 0470h + formula**

Figure 14-9508. USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERS_TABLE_BAR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERS_TABLE_BAR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERS_TABLE_BAR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">ERS_TABLE_BAR</td><td colspan="6">RESERVED_5_0</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-28691. USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERS_TABLE_BAR	R/W	0h	ERS_TABLE_BAR Reset Source: rst_mod_g_rst_n
5:0	RESERVED_5_0	R	0h	Reserved

14.9.3.2.2.280 USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Register

1 USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Register (Offset = 14h + formula) [reset = 0h]

ERSTBA_HI

Return to Summary Table

Offset = 14h + (j * 20h); where j = 0 to 7d

Table 14-28692. Instance Table

Instance Name	Physical Address
USB0	**3100 0474h + formula**
USB1	**3110 0474h + formula**

Figure 14-9509. USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Name Register

31	30	29	28	27	26	25	24
ERS_TABLE_BAR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERS_TABLE_BAR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERS_TABLE_BAR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERS_TABLE_BAR							
R/W							
0h							

Table 14-28694. USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERS_TABLE_BAR	R/W	0h	ERS_TABLE_BAR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.281 USB2SS_INTR_XHCI_INTR_ERDP_LO_j Register

1 USB2SS_INTR_XHCI_INTR_ERDP_LO_j Register (Offset = 18h + formula) [reset = 0h]

ERDP_LO For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

Return to Summary Table

Offset = 18h + (j * 20h); where j = 0 to 7d

Table 14-28695. Instance Table

Instance Name	Physical Address
USB0	**3100 0478h + formula**
USB1	**3110 0478h + formula**

Figure 14-9510. USB2SS_INTR_XHCI_INTR_ERDP_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ERD_PNTR</td><td>EHB</td><td colspan="3">DESI</td></tr>
<tr><td colspan="4">R/W</td><td>R/W1TC</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-28697. USB2SS_INTR_XHCI_INTR_ERDP_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERD_PNTR	R/W	0h	ERD_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28697. USB2SS_INTR_XHCI_INTR_ERDP_LO_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EHB	R/W1TC	0h	HC OS Owned SemaphoreERS_TABLE_SIZEHC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable - SMI on OS Ownership Enable - SMI on PCI Command Enable - SMI on BAR Enable - SMI on Event Interrupt - SMI on Host System Error - SMI on OS Ownership Change - SMI on PCI Command - SMI on BAR - Compatible Port Count - HC OS Owned Semaphore - HC BIOS Owned Semaphore - USB SMI Enable - SMI on Host System Error Enable - SMI on OS Ownership Enable - SMI on PCI Command Enable - SMI on BAR Enable - SMI on Event Interrupt - SMI on Host System Error - SMI on OS Ownership Change - SMI on PCI Command - SMI on BAR - Compatible Port Count Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	DESI - For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.282 USB2SS_INTR_XHCI_INTR_ERDP_HI_j Register

1 USB2SS_INTR_XHCI_INTR_ERDP_HI_j Register (Offset = 1Ch + formula) [reset = 0h]

ERDP_HI

Return to Summary Table

Offset = 1Ch + (j * 20h); where j = 0 to 7d

Table 14-28698. Instance Table

Instance Name	Physical Address
USB0	**3100 047Ch + formula**
USB1	**3110 047Ch + formula**

Figure 14-9511. USB2SS_INTR_XHCI_INTR_ERDP_HI_j Name Register

31	30	29	28	27	26	25	24
ERD_PNTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERD_PNTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERD_PNTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERD_PNTR							
R/W							
0h							

Table 14-28700. USB2SS_INTR_XHCI_INTR_ERDP_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERD_PNTR	R/W	0h	ERD_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.283 USB2SS_DBARR_XHCI_DB_DB_j Register

1 USB2SS_DBARR_XHCI_DB_DB_j Register (Offset = 0h + formula) [reset = 0h]

Doorbell Register Bit Field Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0. Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 64d

Table 14-28701. Instance Table

Instance Name	Physical Address
USB0	**3100 0560h + formula**
USB1	**3110 0560h + formula**

Figure 14-9512. USB2SS_DBARR_XHCI_DB_DB_j Name Register

31	30	29	28	27	26	25	24
DB_STREAM_ID							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DB_STREAM_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15_8							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DB_TARGET							
R/W							
0h							

Table 14-28703. USB2SS_DBARR_XHCI_DB_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DB_STREAM_ID	R/W	0h	DB_STREAM_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	DB_TARGET	R/W	0h	DB_TARGET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.284 USB2SS_EXTCAP_USBLEGSUP Register

1 USB2SS_EXTCAP_USBLEGSUP Register (Offset = 0h) [reset = 401h]

USBLEGSUP

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Table 14-28704. Instance Table

Instance Name	Physical Address
USB0	**3100 0960h**
USB1	**3110 0960h**

Figure 14-9513. USB2SS_EXTCAP_USBLEGSUP Name Register

31	30	29	28	27	26	25	24
RESERVED_31_25							HC_OS_OWNED
R							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED_23_17							HC_BIOS_OWNED
R							R/W
0h							0h
15	14	13	12	11	10	9	8
NEXT_CAPABILITY_POINTER							
R							
4h							
7	6	5	4	3	2	1	0
CAPABILITY_ID							
R							
1h							

Table 14-28706. USB2SS_EXTCAP_USBLEGSUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_31_25	R	0h	Reserved
24	HC_OS_OWNED	R/W	0h	HC_OS_OWNED SEMAPHORE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23:17	RESERVED_23_17	R	0h	Reserved
16	HC_BIOS_OWNED	R/W	0h	HC_BIOS_OWNED SEMAPHORE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	4h	NEXT_CAPABILITY_POINTER For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-28706. USB2SS_EXTCAP_USBLEGSUP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CAPABILITY_ID	R	1h	CAPABILITY_ID set_register_field_attribute DWC_usb3_map/ DWC_usb3_block_HC_Extended_Capability_Register/ USBLEGSUP/CAPABILITY_ID RegisterResetValue 0x1 For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.285 USB2SS_EXTCAP_USBLEGCTLSTS Register

1 USB2SS_EXTCAP_USBLEGCTLSTS Register (Offset = 4h) [reset = 0h]

USBLEGCTLSTS

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Table 14-28707. Instance Table

Instance Name	Physical Address
USB0	**3100 0964h**
USB1	**3110 0964h**

Figure 14-9514. USB2SS_EXTCAP_USBLEGCTLSTS Name Register

31	30	29	28	27	26	25	24
SMI_ON_BAR	SMI_ON_PCI	SMI_ON_OS	RESERVED_28_21				
R/W1TC	R/W1TC	R/W1TC	R				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_28_21			SMI_ON_HOST	RESERVED_19_17			SMI_ON_EVENT
R			R	R			R
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMI_ON_BAR_E	SMI_ON_PCI_E	SMI_ON_OS_E	RESERVED_12_5				
R/W	R/W	R/W	R				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_12_5			SMI_ON_HOST_E	RESERVED_3_1			USB_SMI_ENABLE
R			R/W	R			R/W
0h			0h	0h			0h

Table 14-28709. USB2SS_EXTCAP_USBLEGCTLSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SMI_ON_BAR	R/W1TC	0h	SMI_ON_BAR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
30	SMI_ON_PCI	R/W1TC	0h	SMI_ON_PCI COMMAND For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
29	SMI_ON_OS	R/W1TC	0h	SMI_ON_OS OWNERSHIP CHANGE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
28:21	RESERVED_28_21	R	0h	Reserved

Table 14-28709. USB2SS_EXTCAP_USBLEGCTLSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	SMI_ON_HOST	R	0h	SMI_ON_HOST SYSTEM ERROR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
19:17	RESERVED_19_17	R	0h	Reserved
16	SMI_ON_EVENT	R	0h	SMI_ON_EVENT INTERRUPT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15	SMI_ON_BAR_E	R/W	0h	SMI_ON_BAR ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
14	SMI_ON_PCI_E	R/W	0h	SMI_ON_PCI COMMAND ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
13	SMI_ON_OS_E	R/W	0h	SMI_ON_OS OWNERSHIP ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
12:5	RESERVED_12_5	R	0h	Reserved
4	SMI_ON_HOST_E	R/W	0h	SMI_ON_HOST SYSTEM ERROR ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3:1	RESERVED_3_1	R	0h	Reserved
0	USB_SMI_ENABLE	R/W	0h	USB_SMI_ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.286 USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register

1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register (Offset = 0h) [reset = 2000002h]

SUPTPRT2_DW0

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Table 14-28710. Instance Table

Instance Name	Physical Address
USB0	**3100 0970h**
USB1	**3110 0970h**

Figure 14-9515. USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REVISION							
R							
2h							
23	22	21	20	19	18	17	16
MINOR_REVISION							
R							
0h							
15	14	13	12	11	10	9	8
NEXT_CAPABILITY_POINTER							
R							
0h							
7	6	5	4	3	2	1	0
CAPABILITY_ID							
R							
2h							

Table 14-28712. USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REVISION	R	2h	MAJOR_REVISION Reset Source: rst_mod_g_rst_n
23:16	MINOR_REVISION	R	0h	MINOR_REVISION Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	0h	NEXT_CAPABILITY_POINTER Reset Source: rst_mod_g_rst_n
7:0	CAPABILITY_ID	R	2h	CAPABILITY_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.287 USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register

1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register (Offset = 4h) [reset = 20425355h]

Register SUPTPRT2_DW1

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Table 14-28713. Instance Table

Instance Name	Physical Address
USB0	**3100 0974h**
USB1	**3110 0974h**

Figure 14-9516. USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Name Register

31	30	29	28	27	26	25	24
NAME_STRING							
R							
20425355h							
23	22	21	20	19	18	17	16
NAME_STRING							
R							
20425355h							
15	14	13	12	11	10	9	8
NAME_STRING							
R							
20425355h							
7	6	5	4	3	2	1	0
NAME_STRING							
R							
20425355h							

Table 14-28715. USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NAME_STRING	R	20425355h	NAME_STRING For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.288 USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register

1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register (Offset = 8h) [reset = 180101h]

xHCI Supported Protocol Capability_ Data Word 2 For a description of other register fields, see section 7.2 of the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28716. Instance Table

Instance Name	Physical Address
USB0	**3100 0978h**
USB1	**3110 0978h**

Figure 14-9517. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Name Register

31	30	29	28	27	26	25	24
PSIC				MHD			RESERVED_24_21
R				R			R
0h				0h			0h
23	22	21	20	19	18	17	16
RESERVED_24_21			BLC	HLC	IHI	HSO	RESERVED
R			R	R	R	R	NONE
0h			1h	1h	0h	0h	0h
15	14	13	12	11	10	9	8
COMPATIBLE_PORT_COUNT							
R							
1h							
7	6	5	4	3	2	1	0
COMPATIBLE_PORT_OFFSET							
R							
1h							

Table 14-28718. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	0h	PSIC Reset Source: rst_mod_g_rst_n
27:25	MHD	R	0h	Hub Depth For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24:21	RESERVED_24_21	R	0h	Reserved
20	BLC	R	1h	BESL LPM Capability. When this bit is set to: - 1: The ports described by this xHCI Supported Protocol Capability applies BESL timing to the BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. - 0: The ports described by this xHCI Supported Protocol Capability applies HIRD timing to the BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. Reset Source: rst_mod_g_rst_n

Table 14-28718. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	HLC	R	1h	Compatible Port Offset. Compatible Port Count Refer to Table 7-3 in the Databook. Reset Source: rst_mod_g_rst_n
18	IHI	R	0h	IHI Reset Source: rst_mod_g_rst_n
17	HSO	R	0h	HSO Reset Source: rst_mod_g_rst_n
16	RESERVED	NONE	0h	Reserved
15:8	COMPATIBLE_PORT_COUNT	R	1h	COMPATIBLE_PORT_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	1h	COMPATIBLE_PORT_OFFSET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.289 USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register

1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register (Offset = Ch) [reset = 0h]

Register SUPTPRT2_DW3

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Table 14-28719. Instance Table

Instance Name	Physical Address
USB0	**3100 097Ch**
USB1	**3110 097Ch**

Figure 14-9518. USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_5							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_5							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_5			PROTCL_SLT_TY				
R			R				
0h			0h				

Table 14-28721. USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_31_5	R	0h	Reserved
4:0	PROTCL_SLT_TY	R	0h	Protocol Slot Type Reset Source: rst_mod_g_rst_n

14.9.3.2.2.290 USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register

1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register (Offset = 0h) [reset = 0h]

Register SUPTPRT3_DW0

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Table 14-28722. Instance Table

Instance Name	Physical Address
USB0	**3100 0980h**
USB1	**3110 0980h**

Figure 14-9519. USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REVISION							
R							
0h							
23	22	21	20	19	18	17	16
MINOR_REVISION							
R							
0h							
15	14	13	12	11	10	9	8
NEXT_CAPABILITY_POINTER							
R							
0h							
7	6	5	4	3	2	1	0
CAPABILITY_ID							
R							
0h							

Table 14-28724. USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REVISION	R	0h	MAJOR_REVISION For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23:16	MINOR_REVISION	R	0h	MINOR_REVISION For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	0h	NEXT_CAPABILITY_POINTER For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	CAPABILITY_ID	R	0h	CAPABILITY_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.291 USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register

1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register (Offset = 4h) [reset = 0h]

Register SUPTPRT3_DW1

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Table 14-28725. Instance Table

Instance Name	Physical Address
USB0	**3100 0984h**
USB1	**3110 0984h**

Figure 14-9520. USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Name Register

31	30	29	28	27	26	25	24
NAME_STRING							
R							
0h							
23	22	21	20	19	18	17	16
NAME_STRING							
R							
0h							
15	14	13	12	11	10	9	8
NAME_STRING							
R							
0h							
7	6	5	4	3	2	1	0
NAME_STRING							
R							
0h							

Table 14-28727. USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NAME_STRING	R	0h	NAME_STRING For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.292 USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register

1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register (Offset = 8h) [reset = 102h]

SUPTPRT3_DW2 For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-28728. Instance Table

Instance Name	Physical Address
USB0	**3100 0988h**
USB1	**3110 0988h**

Figure 14-9521. USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Name Register

31	30	29	28	27	26	25	24
PSIC				MHD			RESERVED
R				R			NONE
0h				0h			0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
COMPATIBLE_PORT_COUNT							
R							
1h							
7	6	5	4	3	2	1	0
COMPATIBLE_PORT_OFFSET							
R							
2h							

Table 14-28730. USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	0h	PSIC Reset Source: rst_mod_g_rst_n
27:25	MHD	R	0h	Hub Depth For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24:16	RESERVED	NONE	0h	Reserved
15:8	COMPATIBLE_PORT_COUNT	R	1h	COMPATIBLE_PORT_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	2h	COMPATIBLE_PORT_OFFSET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.293 USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register

1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register (Offset = Ch) [reset = 0h]

SUPTPRT3_DW3

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Table 14-28731. Instance Table

Instance Name	Physical Address
USB0	**3100 098Ch**
USB1	**3110 098Ch**

Figure 14-9522. USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_5							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_5							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_5			PROTCL_SLT_TY				
R			R				
0h			0h				

Table 14-28733. USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_31_5	R	0h	Reserved
4:0	PROTCL_SLT_TY	R	0h	Protocol Slot Type Reset Source: rst_mod_g_rst_n

14.9.3.2.2.294 USB2SS_GBL_GSBUSCFG0 Register

1 USB2SS_GBL_GSBUSCFG0 Register (Offset = 0h) [reset = 6h]

Global SoC Bus Configuration Register 0 This register configures system bus DMA options for the initiator bus, which may be configured as AHB, AXI, or Native. Options include burst length and cache type (bufferable/ posted, cacheable/snoop, and so on). The application can program this register upon power-on, or a change in mode of operation after the DMA engine is halted. xHCI Register Power-On Value: If you are using a standard xHCI host driver, make sure to set the register's power-on value during coreConsultant configuration (DWC_USB3_GSBUSCFG0_INIT parameter) because the standard xHCI driver does not access this register. For more details on this register, refer to the following sections: - "Usage of Global SoC Bus Configuration Register 0 (GSBUSCFG0)" section in the Programming Guide - "System Bus Interface" section in the Databook

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Table 14-28734. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9523. USB2SS_GBL_GSBUSCFG0 Name Register

31	30	29	28	27	26	25	24
DATRDREQINFO				DESRDREQINFO			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATWRREQINFO				DESWRREQINFO			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15_12				DATBIGEND	DESBIGEND	RESERVED_9_8	
R				R/W	R/W	R	
0h				0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INCR256BRSTENA	INCR128BRSTENA	INCR64BRSTENA	INCR32BRSTENA	INCR16BRSTENA	INCR8BRSTENA	INCR4BRSTENA	INCRBRSTENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	1h	0h

Table 14-28736. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	DATRDREQINFO	R/W	0h	DATRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Read [DatRdReqInfo] Input to BUS-GM. Reset Source: rst_mod_g_rst_n
27:24	DESRDREQINFO	R/W	0h	DESRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Read [DesRdReqInfo]. Input to BUS-GM. Reset Source: rst_mod_g_rst_n

Table 14-28736. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	DATWRREQINFO	R/W	0h	DATWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Write [DatWrReqInfo]. Input to BUS-GM. Reset Source: rst_mod_g_rst_n
19:16	DESWRREQINFO	R/W	0h	DESWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Write [DesWrReqInfo] Input to BUS-GM. Reset Source: rst_mod_g_rst_n
15:12	RESERVED_15_12	R	0h	Reserved for future use
11	DATBIGEND	R/W	0h	Data Access is Big Endian This bit controls the endian mode for data accesses. - Little-endian [default]. - Big-endian. In big-endian mode, DMA access [both read and write] for packet data a Byte Invariant Big-Endian mode [see "Little-Endian and Big-Endian" section in the User Guide]. Note: Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI initiator [DWC_USB3_MBUS_TYPE=1], this bit must be set to zero. Reset Source: rst_mod_g_rst_n
10	DESBIGEND	R/W	0h	Descriptor Access is Big Endian This bit controls the endian mode for descriptor accesses. - Little-endian [default] - Big-endian In big-endian mode, DMA access [both read and write] for descriptors uses a Byte Invariant Big-Endian mode [see "Little-Endian and Big-Endian" section in the User Guide. Data is considered as 'embedded data' in the descriptors in the following cases: - Device mode: The buffer pointer of a Setup TRB points to the Setup TRB itself. - Host mode: The Immediate Data [IDT] bit in a Transfer TRB is set to 1. In device mode, if the system uses different endian modes for descriptor and data, software must not use 'embedded' data. In host mode, if the system uses different endian modes for data and descriptors, the controller treats 'embedded data' as descriptor [not as data] in terms of endian mode handling. If this is not the expectation of the system, the software must manipulate the 'embedded data' accordingly. Note: Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI initiator [DWC_USB3_MBUS_TYPE=1], this bit must be set to zero. Reset Source: rst_mod_g_rst_n
9:8	RESERVED_9_8	R	0h	Reserved
7	INCR256BRSTENA	R/W	0h	INCR256 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 256-beat burst. Reset Source: rst_mod_g_rst_n

Table 14-28736. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INCR128BRSTENA	R/W	0h	INCR128 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 128-beat burst. Reset Source: rst_mod_g_rst_n
5	INCR64BRSTENA	R/W	0h	INCR64 Burst Type Enable - Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 64-beat burst. Reset Source: rst_mod_g_rst_n
4	INCR32BRSTENA	R/W	0h	INCR32 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 32-beat burst. Reset Source: rst_mod_g_rst_n
3	INCR16BRSTENA	R/W	0h	INCR16 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to '1', the AHB/AXI initiator uses INCR to do the 16-beat burst. Reset Source: rst_mod_g_rst_n
2	INCR8BRSTENA	R/W	1h	INCR8 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI initiator uses INCR to do the 8-beat burst. Reset Source: rst_mod_g_rst_n
1	INCR4BRSTENA	R/W	1h	INCR4 Burst Type Enable Input to BUS-GM. For the AXI configuration, when this bit is enabled the controller is allowed to do bursts of beat length 1, 2, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers. Reset Source: rst_mod_g_rst_n

Table 14-28736. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INCRBRSTENA	R/W	0h	Undefined Length INCR Burst Type Enable [INCRBrstEna] Input to BUS-GM. This bit determines the set of burst lengths the initiator interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables [INCR256/128/64/32/16/8/4]. 0: INCRX burst mode HBURST [for AHB configurations] and ARLEN/AWLEN [for AXI configurations] do not use INCR except in case of non-aligned burst transfers. In the case of address-aligned transfers, they use only the following burst lengths: - 1 - 2, 4 [if GSBUSCFG0.INCR4BrstEna = 1] - 8 [if GSBUSCFG0.INCR8BrstEna = 1] - 16 [if GSBUSCFG0.INCR16BrstEna = 1] - 32 [if GSBUSCFG0.INCR32BrstEna = 1] - 64 [if GSBUSCFG0.INCR64BrstEna = 1] - 128 [if GSBUSCFG0.INCR128BrstEna = 1] - 256 [if GSBUSCFG0.INCR256BrstEna = 1] Note: - In case of non-address-aligned transfers, INCR may get generated at the beginning and end of the transfers to align the address boundaries, even though INCR is disabled. - In AHB mode, if INCRX burst mode is enabled, but none of the supported INCRx bursts bits are enabled, then the controller will perform [undefined length] INCR bursts. 1: INCR [undefined length] burst mode - AHB configurations: HBURST uses SINGLE or INCR of any length with handling 1KB boundary breakup. - AXI configurations: ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the initiator interface uses only power-of-2 burst lengths [as enabled via GSBUSCFG0[7:0]]. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.295 USB2SS_GBL_GSBUSCFG1 Register

1 USB2SS_GBL_GSBUSCFG1 Register (Offset = 4h) [reset = 300h]

Global SoC Bus Configuration Register 1 xHCI Register Power-On Value: If you are using a standard xHCI host driver, make sure to set the register's power-on value during coreConsultant configuration (DWC_USB3_GSBUSCFG1_INIT parameter) because the standard xHCI driver does not access this register. For more details on this register, refer to "System Bus Interface" section in the Databook.

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Table 14-28737. Instance Table

Instance Name	Physical Address
USB0	**3100 C104h**
USB1	**3110 C104h**

Figure 14-9524. USB2SS_GBL_GSBUSCFG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_31_13</td><td>EN1KPAGE</td><td colspan="4">PIPETRANSLIMIT</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_7_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28739. USB2SS_GBL_GSBUSCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12	EN1KPAGE	R/W	0h	1k Page Boundary Enable By default [this bit is disabled] the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI initiator [DMA data] breaks transfers at the 1k page boundary. Reset Source: rst_mod_g_rst_n

Table 14-28739. USB2SS_GBL_GSBUSCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	PIPETRANSLIMIT	R/W	3h	AXI Pipelined Transfers Burst Request Limit The field controls the number of outstanding pipelined transfer requests the AXI initiator pushes to the AXI target. When the AXI initiator reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: - 'h0: 1 request - 'h1: 2 requests - 'h2: 3 requests - 'h3: 4 requests - ... - 'hF: 16 requests Reset Source: rst_mod_g_rst_n
7:0	RESERVED_7_0	R	0h	Reserved

14.9.3.2.2.296 USB2SS_GBL_GTXTHRCFG Register

1 USB2SS_GBL_GTXTHRCFG Register (Offset = 8h) [reset = 0h]

Global Tx Threshold Control Register For more information on - Using this register, refer to "Packet Threshold and Burst Features for High Latency Systems" section in the Databook. - Selecting values for the fields of this register, see the "TX/RX Data FIFO Sizes and TX/RX Threshold Control Register Settings" section in the User Guide. Note: - GTXTHRCFG register is not applicable for Debug Target. - GTXTHRCFG register is not applicable in USB 2.0-only mode.

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Table 14-28740. Instance Table

Instance Name	Physical Address
USB0	**3100 C108h**
USB1	**3110 C108h**

Figure 14-9525. USB2SS_GBL_GTXTHRCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_31	RESERVED_30	USBTXPKTCNTSEL	RESERVED_28	USBTXPKTCNT			
R	R	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
USBMAXTXBURSTSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_15	RESERVED_14	RESERVED_13_11			RESERVED_10_0		
R	R	R			R		
0h	0h	0h			0h		
7	6	5	4	3	2	1	0
RESERVED_10_0							
R							
0h							

Table 14-28742. USB2SS_GBL_GTXTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R	0h	Reserved
30	RESERVED_30	R	0h	Reserved
29	USBTXPKTCNTSEL	R/W	0h	USB Transmit Packet Count Enable This field enables/disables the USB transmission multi-packet thresholding: - 0: USB transmission multi-packet thresholding is disabled. the controller can start transmission on the USB after the entire [one full] packet has been fetched into the corresponding TXFIFO. - 1: USB transmission multi-packet thresholding is enabled. The controller can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction [burst] are already in the corresponding TXFIFO. This mode is valid in both host and device modes. It is only used for SuperSpeed operation. Reset Source: rst_mod_g_rst_n
28	RESERVED_28	R	0h	Reserved

Table 14-28742. USB2SS_GBL_GTXTHRCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:24	USBTXPKTCNT	R/W	0h	USB Transmit Packet Count This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction [burst]. This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: - In device mode, if device controller does not have the TRBs for the number of packets or if it cannot fetch the TRBs because of high latency or switching between other endpoints, then it does not wait for the threshold number of packets. The threshold number of packets will be honored only when the TRBs are available in the controller for the number of packets before it starts the data fetch. - This field must be less than or equal to the USB Maximum TX Burst Size field. Reset Source: rst_mod_g_rst_n
23:16	USBMAXTXBURSTSIZE	R/W	0h	USB Maximum TX Burst Size When UsbTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the controller can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the controller can do. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in UsbTxPktCnt is less than this value. Valid values are from 1 to 16. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved_15
14	RESERVED_14	R	0h	Reserved1[Rsvd/Rs] Register field must write only 0 by the application. The read value must be treated as X [unknown].
13:11	RESERVED_13_11	R	0h	Reserved [Rsvd/Rs] The register field must write only 0 by the application. The read value must be treated as X [unknown].
10:0	RESERVED_10_0	R	0h	Reserved for future use

14.9.3.2.2.297 USB2SS_GBL_GRXTHRCFG Register

1 USB2SS_GBL_GRXTHRCFG Register (Offset = Ch) [reset = 0h]

Global Rx Threshold Control Register In a normal case, a Tx burst starts as soon as one packet is prefetched. an Rx burst starts as soon as 1-packet space is available. This works well as long as the system bus is faster than the USB 3.0 bus (a 1024-bytes packet takes ~2.2 microseconds on the USB bus in SS mode). If the system bus latency is larger than 2.2 microseconds to access a 1024-byte packet, then starting a burst on 1-packet condition leads to an early abort of the burst causing unnecessary performance reduction. To avoid underrun and overrun during the burst, in a high-latency bus system (like USB), threshold and burst size control is provided through GTXTHRCFG and GRXTHRCFG registers. Bit [29] of the GTXTHRCFG and GRXTHRCFG registers enables this feature. For more information on - Using this register, refer to "Packet Threshold and Burst Features for High Latency Systems" section in the Databook. - Selecting values for the fields of this register, see the "TX/RX Data FIFO Sizes and TX/RX Threshold Control Register Settings" section in the User Guide. Note: - GRXTHRCFG register is not applicable for Debug Target. - There is an issue when ACK TP with NumP=0 followed by ACK TP with NumP=1 without ERDY TP sent by the device controller during a burst bulk OUT transfer. This may cause third-party USB 3.0 host controllers to keep waiting for the ERDY TP. The USB 3.0 specification states that "When an endpoint is not in a flow control condition, it shall not send an ERDY TP unless the endpoint is a Bulk endpoint that supports streams." In this case, after the device sent the ACK TP (nump=1), the endpoint was not in the flow control, so it did not send an ERDY. The device would have sent ERDY if the next OUT packet was not received. When the next OUT packet was received, at that time there was enough buffer space to accept it, so the device accepted the packet by informing host that it is not no longer in the flow control. The Host should wait for the responses for all the OUT packets to return and then decide if the endpoint is still in flow control or not. The USB 3.1 specification supersedes all the USB 3.0 specification. The errata states that "If the host continues, or resumes, transactions to an endpoint, the endpoint shall re-evaluate its flow control state and respond appropriately." However, there are no ECNs on the USB 3.0 for this issue. To work around this issue, the Global Rx Threshold mode must be disable by setting GRXTHRCFG.UsbRxPktCntSel=0. Instead, software can program the DCFG.NUMP mode (where fixed NUMP is transmitted always) instead of the RX threshold based nump mode to prevent the device from sending ACK TP with NumP=0. The NUMP in the ACK TP is the minimum value of (DCFG.NUMP, bMaxBurstSize) for each endpoint.

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Table 14-28743. Instance Table

Instance Name	Physical Address
USB0	**3100 C10Ch**
USB1	**3110 C10Ch**

Figure 14-9526. USB2SS_GBL_GRXTHRCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_31_30		USBRXPKTCNTSEL	RESERVED_28	USBRXPKTCNT			
R		R/W	R	R/W			
0h		0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
USBMAXRXBURSTSIZE					RESERVED_18_16		
R/W					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15	RESERVED_14_13		RESVISOCOUTSPC				
R	R		R/W				
0h	0h		0h				

Figure 14-9526. USB2SS_GBL_GRXTHRCFG Name Register (continued)

7	6	5	4	3	2	1	0
RESVISOCOUTSPC							
R/W							
0h							

Table 14-28745. USB2SS_GBL_GRXTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_31_30	R	0h	Reserved
29	USBRXPKTCNTSEL	R/W	0h	USB Receive Packet Count Enable This field enables/disables the USB reception multi-packet thresholding: - 0: The controller can only start reception on the USB when the RX FIFO has space for at least one packet. - 1: The controller can only start reception on the USB when the RX FIFO has space for at least UsbRxPktCnt amount of packets. This mode is valid in both host and device mode. It is only used for SuperSpeed. In device mode, - Setting this bit to 1 also enables the functionality of reporting NUMP in the ACK TP based on the RX FIFO space instead of reporting a fixed NUMP derived from DCFG.NUMP for non-control endpoints. - If you are using external buffer control [EBC] feature, disable this mode by setting UsbRxPktCntSel to 0. Reset Source: rst_mod_g_rst_n
28	RESERVED_28	R	0h	Reserved
27:24	USBRXPKTCNT	R/W	0h	USB Receive Packet Count In host mode, this field specifies the space [in terms of the number of packets] that must be available in the RX FIFO before the controller can start the corresponding USB RX transaction [burst]. In device mode, this field specifies the space [in terms of the number of packets] that must be available in the RX FIFO before the controller can send ERDY for a flow-controlled endpoint. This field is valid only when the USB Receive Packet Count Enable field is set to 1. The valid values for this field are from 1 to 15. Note: This field must be less than or equal to the USB Maximum Receive Burst Size field. Reset Source: rst_mod_g_rst_n
23:19	USBMAXRXBURSTSIZE	R/W	0h	USB Maximum Receive Burst Size In host mode, this field specifies the Maximum Bulk IN burst the DWC_usb3 controller can perform. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. You can program a smaller value to this field to limit the RX burst size that the controller can perform. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. In device mode, this field specifies the NUMP value that is sent in ERDY for an OUT endpoint. The programmed value should not exceed the RXFIFO size. This field is valid only when UsbRxPktCntSel is one. The valid values for this field are from 1 to 16. Reset Source: rst_mod_g_rst_n
18:16	RESERVED_18_16	R	0h	Reserved
15	RESERVED_15	R	0h	Reserved
14:13	RESERVED_14_13	R	0h	Reserved

Table 14-28745. USB2SS_GBL_GRXTHRCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:0	RESVISOCOUTSPC	R/W	0h	Space reserved in Rx FIFO for ISOC OUT In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped. If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of RX FIFO is 8192. Therefore, this field is 13 bits wide. The value of space reserved is in terms of DWC_USB3_MDWIDTH. For SS, the space reservation is always rounded off to the nearest packet boundary. Therefore, it is always recommended to program a value corresponding to MPS or its multiples. For HS/FS, the space reservation is the actual value. Note: For SS, reserve space for ISOC when the Rx FIFO space can accommodate two MPS or more. Otherwise, this may result in degraded performance for non-ISOC packets. If the space is entirely allocated for ISOC, the non-ISOC packets will be completely dropped. To help you decide during the time of configuring the controller, refer to the "Device-Mode Receive Path" section in the Databook. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.298 USB2SS_GBL_GCTL Register

1 USB2SS_GBL_GCTL Register (Offset = 10h) [reset = 2001h]

Global Core Control Register Refer to <workspace>/src/DWC_usb3_params.v for details on DWC_USB3_GCTL_INIT. Note: When Hibernation is not enabled, you can write any value to GblHibernationEn. It always returns 0 when read.

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Table 14-28746. Instance Table

Instance Name	Physical Address
USB0	**3100 C110h**
USB1	**3110 C110h**

Figure 14-9527. USB2SS_GBL_GCTL Name Register

31	30	29	28	27	26	25	24
PWRDNSCALE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWRDNSCALE					MASTERFILTBYPASS	BYPSSETADDR	U2RSTECN
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FRMSCLDWN		PRTCAPDIR		CORESOFTRESET	SOFITPSYNC	U1U2TIMERSCALE	DEBUGATTACH
R/W		R/W		R/W	R/W	R/W	R/W
0h		2h		0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMCLKSEL		SCALEDOWN		DISSCRAMBLE	U2EXIT_LFPS	GBLHIBERNATIONEN	DSBLCLKGTNG
R/W		R/W		R/W	R/W	R	R/W
0h		0h		0h	0h	0h	1h

Table 14-28748. USB2SS_GBL_GCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	PWRDNSCALE	R/W	0h	Power Down Scale [PwrDnScale] The USB3 suspend_clk input replaces pipe3_rx_pclk as a clock source to a small part of the USB3 controller that operates when the SS PHY is in its lowest power [P3] state, and therefore does not provide a clock. The Power Down Scale field specifies how many suspend_clk periods fit into a 16 kHz clock period. When performing the division, round up the remainder. For example, when using an 8-bit/16-bit/32-bit PHY and 25-MHz Suspend clock, Power Down Scale = 25000 kHz/16 kHz = 13'd1563 [rounder up] Note: - Minimum Suspend clock frequency is 32 kHz - Maximum Suspend clock frequency is 125 MHz The LTSSM uses Suspend clock for 12-ms and 100-ms timers during suspend mode. According to the USB 3.0 specification, the accuracy on these timers is 0% to +50%. - 12 ms + 0~+50% accuracy = 18 ms [Range is 12 ms - 18 ms] - 100 ms + 0~+50% accuracy = 150 ms [Range is 100 ms - 150 ms]. The suspend clock accuracy requirement is: - [12,000/62.5] * [GCTL[31:19]] * actual suspend_clk_period must be between 12,000 and 18,000 - [100,0000/62.5] * [GCTL[31:19]] * actual suspend_clk_period must be between 100,000 and 150,000 For example, if your suspend_clk frequency varies from 7.5 MHz to 10.5MHz, then the value needs to programmed is: Power Down Scale = 10500/16 = 657 [rounded up. and fastest frequency used]. Reset Source: rst_mod_g_rst_n
18	MASTERFILTBYPASS	R/W	0h	Initiator Filter Bypass When this bit is set to 1'b1, irrespective of the parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in the DWC_usb3_filter module are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0. Reset Source: rst_mod_g_rst_n
17	BYPSSETADDR	R/W	0h	Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device controller uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device controller respond to a new address. When the xHCI Debug capability is enabled and this bit is set, the Debug Target immediately enters the configured state without requiring the Debug Host to send a SetAddress or SetConfig request. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0. Reset Source: rst_mod_g_rst_n
16	U2RSTECN	R/W	0h	U2RSTECN If the SuperSpeed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode. For each attempt, the device checks receiver termination eight times. From 2.60a release, this bit controls whether to check for Rx.Detect eight times or one time for every attempt. Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode. Reset Source: rst_mod_g_rst_n

Table 14-28748. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	FRMSCLDWN	R/W	0h	FRMSCLDWN This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: - Value of 2'h3 implements interval to be 15.625 us - Value of 2'h2 implements interval to be 31.25 us - Value of 2'h1 implements interval to be 62.5 us - Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. When xHCI Debug Capability is enabled, this field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. - 2'h0: 1024 bytes - 2'h1: 512 bytes - 2'h2: 256 bytes - 2'h3: 128 bytes Reset Source: rst_mod_g_rst_n
13:12	PRTCAPDIR	R/W	2h	PRTCAPDIR: Port Capability Direction [PrtCapDir] - 2'b01: for Host configurations - 2'b10: for Device configurations Note: For static Host-only/Device-only applications, use DRD Host or DRD Device mode. The combination of GCTL.PrtCapDir=2'b11 with SRP and HNP/RSP disabled is not recommended for these applications. The sequence for switching modes in DRD configuration is as follows: Switching from Device to Host: 1. Reset the controller using GCTL[11] [CoreSoftReset]. 2. Set GCTL[13:12] [PrtCapDir] to 2'b01 [Host mode]. 3. Reset the host using USBCMD.HCRESET. Switching from Host to Device: 1. Reset the controller using GCTL[11] [CoreSoftReset]. 2. Set GCTL[13:12] [PrtCapDir] to 2'b10 [Device mode]. 3. Reset the device by setting DCTL[30] [CSftRst]. Reset Source: rst_mod_g_rst_n
11	CORESOFTRESET	R/W	0h	Core Soft Reset [CoreSoftReset] - 1'b0 - No soft reset - 1'b1 - Soft reset to controller Clears the interrupts and all the CSRs except the following registers: - GCTL - GUCTL - GSTS - GSNPSID - GGPIO - GUID - GUSB2PHYCFGn registers - GUSB3PIPECTLn registers - DCFG - DCTL - DEVTEN - DSTS When you reset PHYs [using GUBS3PHYCFG or GUSB3PIPECTL registers], you must keep the controller in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets. Refer to the "Reset Generation" section in the Databook. Note: This bit is for debug purposes only. Use USBCMD.HCRESET in xHCI Mode and DCTL.SoftReset in device mode for soft reset. Programming this field with random data will reset the internal logic of the host controller. Due to this side effect Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n

Table 14-28748. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SOFITPSYNC	R/W	0h	SOFITPSYNC If this bit is set to '0' operating in host mode, the controller keeps the UTMI/ULPI PHY on the first port in a non-suspended state whenever there is a SuperSpeed port that is not in Rx.Detect, SS.Disable and U3. If this bit is set to '1' operating in host mode, the controller keeps the UTMI/ULPI PHY on the first port in a non-suspended state whenever the other non-SuperSpeed ports are not in a suspended state. This feature is useful because it saves power by suspending UTMI/ULPI when SuperSpeed only is active, and it helps resolve when the PHY does not transmit a host resume unless it is placed in suspend state. This bit must be programmed as a part of initialization at power-on reset, and must not be dynamically changed afterwards. Note: - USB2PHYCFGn[6].PhySusp eventually decides to put the UTMI/ULPI PHY in to suspend state. In addition, when this bit is set to '1', the controller generates ITP from the ref_clk based counter. Otherwise, ITP and SOF are generated from utmi/ulpi_clk[0] based counter. To program the reference clock period inside the controller, refer to GUCTL[31:22].REFCLKPER. - This feature is valid in Host and DRD configurations and used only in Host mode operation. - If you never use this feature or the GFLADJ.GFLADJ_REFCLK_LPM_SEL, the minimum frequency for the ref_clk can be as low as 32KHz. You can connect the suspend_clk [as low as 32 KHz] to the ref_clk. - If you plan to enable hardware-based LPM or software-based LPM [PORTPMSC. HLE=1], then you cannot use this feature. Turn off this feature by setting this bit to '0' and use the GFLADJ.GFLADJ_REFCLK_LPM_SEL feature. - If you set this bit to '1', the GUSB2PHYCFG.U2_FREECLK_EXISTS bit and the DWC_USB3_FREECLK_USB2_EXIST parameter must be set to '0'. Program this bit to 0 if the controller is intended to be operated in USB 3.0 mode. Reset Source: rst_mod_g_rst_n
9	U1U2TIMERSCALE	R/W	0h	Disable U1/U2 timer Scaledown [U1U2TimerScale]. If set to '1' along with GCTL[5:4] [ScaleDown] = 2'bX1, disables the scale down of U1/U2 inactive timer values. This is for simulation mode only. Reset Source: rst_mod_g_rst_n
8	DEBUGATTACH	R/W	0h	Debug Attach When this bit is set, - SS Link proceeds directly to the Polling link state [after RUN/STOP in the DCTL register is asserted] without checking remote termination. - Link LFPS polling timeout is infinite. - Polling timeout during TS1 is infinite [in case link is waiting for TXEQ to finish]. Reset Source: rst_mod_g_rst_n

Table 14-28748. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	RAMCLKSEL	R/W	0h	RAM Clock Select [RAMClkSel] - 2'b00: bus clock - 2'b01: pipe clock [Only used in device mode] - 2'b10: In device mode , pipe/2 clock.In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2/U3 ports - 2'b11: In device mode, selects mac2_clk as ram_clk [when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode] In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2/U3 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00. For more information on how to select the RAM clock, see the "Clock Generation and Clock Tree Synthesis [CTS] Requirements" section in the Databook. Note: - In device mode, if you set RAMClkSel to 2'b11 [mac2_clk], the controller internally switches the ram_clk to bus_clk when the link state changes to Suspend [L2 or L3], and switches the ram_clk back to mac2_clk when the link state changes to resume or U2. - In host mode, if a value of 2/3 is chosen, then controller switches ram_clk between bus_clk, mac2_clk and pipe_clk, pipe_clk/2, based on the state of the U2/U3 ports. For example, if only the U2 port is active and the U3 ports are suspended, then the ram_clk is switched to mac2_clk. When only the U3 ports are active and the U2 ports are suspended, the controller internally switches the ram_clk to pipe3 clock and when all U2 and U3 ports are suspended, it switches the ram_clk to bus_clk. This allows decoupling the ram_clk from the bus_clk, and depending on the bandwidth requirement allows the bus_clk to be run at a lower frequency than the ram_clk requirements. The bus_clk frequency still cannot be less than 60MHz in host mode, and this is not verified. A value of 2 can be chosen only if the pipe data width is 8 or 16 bits. In this case the when the ram_clk is switched to pipe_clk, it uses pipe_clk/2 instead of pipe_clk. If a value of 3 is chosen for RAMClkSel, then when ram_clk is switched to pipe_clk, then pipe_clk is used without any divider. - In device mode, when RAMClkSel != 2'b00, the bus_clk_early frequency can be a minimum of 1 MHz. This is tested in simulation and also in hardware with Linux, Microsoft Windows 8, and MCCI Windows7 host drivers. Only control and non periodic transfers are supported when bus_clk is 1 MHz. For periodic applications, the bus_clk_early minimum frequency is higher depending on your application and SoC bus. Even though 1 MHz has been tested with standard host drivers, Synopsys recommends 5 MHz minimum for ASIC designs to provide a margin or at least have a backup option to increase the bus_clk frequency to 5 MHz if needed. Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n

Table 14-28748. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	SCALEDOWN	R/W	0h	Scale-Down Mode [ScaleDown] When Scale-Down mode is enabled for simulation, the controller uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume - 2'b10: Enables scale-down of Device mode suspend and resume timing values only. - 2'b11: Enables bit 0 and bit 1 scale-down timing values. SS Mode - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scaled down SS timing and repeat values including: [1] Number of TxEq training sequences reduce to 8. [2] LFPS polling burst time reduce to 256 nS. [3] LFPS warm reset receive reduce to 30 uS. Refer to the rtl_vip_scaledown_mapping.xls file under <workspace>/sim/SoC_sim directory for the complete list. - 2'b10: No TxEq training sequences are sent. Overrides Bit 4. - 2'b11: Enables bit 0 and bit 1 scale-down timing values. Reset Source: rst_mod_g_rst_n
3	DISSCRAMBLE	R/W	0h	Disable Scrambling [DisScramble] Transmit request to Link Partner on next transition to Recovery or Polling. Reset Source: rst_mod_g_rst_n
2	U2EXIT_LFPS	R/W	0h	U2EXIT_LFPS If this bit is, - 0: the link treats 248ns LFPS as a valid U2 exit. - 1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third-party host/device controller. This host/device controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the host/device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the host/device can stay in U2 while ignoring this glitch from the host/ device controller. This bit is applicable for both host and device controller. This bit is added to improve interoperability with a third party host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller. Reset Source: rst_mod_g_rst_n
1	GBLHIBERNATIONEN	R	0h	GblHibernationEn This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any controller state. In addition, the PMUs never drive the PHY interfaces and let the controller continue to drive the PHY interfaces. Reset Source: rst_mod_g_rst_n
0	DSBLCLKGTNG	R/W	1h	Disable Clock Gating [DsblClkGtng] This bit is set to 1 and the controller is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.299 USB2SS_GBL_GPMSTS Register

1 USB2SS_GBL_GPMSTS Register (Offset = 14h) [reset = 0h]

Global Power Management Status Register This debug register gives information on which event caused the hibernation exit. It provides internal status and state machine information, and is for Synopsys use only for debugging purposes. This register is not applicable in USB 2.0-only mode.

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Table 14-28749. Instance Table

Instance Name	Physical Address
USB0	**3100 C114h**
USB1	**3110 C114h**

Figure 14-9528. USB2SS_GBL_GPMSTS Name Register

31	30	29	28	27	26	25	24
PORTSEL				RESERVED_27_17			
W				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_27_17							U3WAKEUP
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
U3WAKEUP				RESERVED_10_11		U2WAKEUP	
R				R		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
U2WAKEUP							
R							
0h							

Table 14-28751. USB2SS_GBL_GPMSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PORTSEL	W	0h	Global Power Management Status Register, PortSel This field selects the port number. Reset Source: rst_mod_g_rst_n
27:17	RESERVED_27_17	R	0h	Reserved
16:12	U3WAKEUP	R	0h	U3Wakeup This field gives the following USB 3.0 port wakeup conditions: - Bit [12]: Overcurrent Detected - Bit [13]: Resume Detected - Bit [14]: Connect Detected - Bit [15]: Disconnect Detected - Bit [16]: Last Connection State Reset Source: rst_mod_g_rst_n
11:10	RESERVED_10_11	R	0h	Reserved

Table 14-28751. USB2SS_GBL_GPMSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	U2WAKEUP	R	0h	U2Wakeup This field indicates the following USB 2.0 port wakeup conditions: - Bit [0]: Overcurrent Detected - Bit [1]: Resume Detected - Bit [2]: Connect Detected - Bit [3]: Disconnect Detected - Bit [4]: Last Connection State - Bit [5]: ID Change Detected - Bit [6]: SRP Request Detected - Bit [7]: ULPI Interrupt Detected - Bit [8]: USB Reset Detected - Bit [9]: Resume Detected Changed Reset Source: rst_mod_g_rst_n

14.9.3.2.2.300 USB2SS_GBL_GSTS Register

1 USB2SS_GBL_GSTS Register (Offset = 18h) [reset = 7E800000h]

Global Status Register

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Table 14-28752. Instance Table

Instance Name	Physical Address
USB0	**3100 C118h**
USB1	**3110 C118h**

Figure 14-9529. USB2SS_GBL_GSTS Name Register

31	30	29	28	27	26	25	24
CBELT							
R							
7E8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CBELT				RESERVED_19_12			
R				R			
7E8h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_19_12				SSIC_IP	OTG_IP	BC_IP	ADP_IP
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOST_IP	DEVICE_IP	CSRTIMEOUT	BUSERRADDR VLD	RESERVED_3_2		CURMOD	
R	R	R/W1TC	R/W1TC	R		R	
0h	0h	0h	0h	0h		0h	

Table 14-28754. USB2SS_GBL_GSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	CBELT	R	7E8h	Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command. Reset Source: rst_mod_g_rst_n
19:12	RESERVED_19_12	R	0h	Reserved
11	SSIC_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n
10	OTG_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n
9	BC_IP	R	0h	Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register. Reset Source: rst_mod_g_rst_n
8	ADP_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n

Table 14-28754. USB2SS_GBL_GSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	HOST_IP	R	0h	Host Interrupt Pending: This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue. Reset Source: rst_mod_g_rst_n
6	DEVICE_IP	R	0h	Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral [device] operation in the Device event queue. Reset Source: rst_mod_g_rst_n
5	CSRTIMEOUT	R/W1TC	0h	CSR Timeout When this bit is 1'b1, it indicates that the software performed a write or read to a controller register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles [default: h1FFFF]. Reset Source: rst_mod_g_rst_n
4	BUSERRADDRVLD	R/W1TC	0h	Bus Error Address Valid [BusErrAddrVld] Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n
3:2	RESERVED_3_2	R	0h	Reserved
1:0	CURMOD	R	0h	Current Mode of Operation [CurMod] Indicates the current mode of operation: - 2'b00: Device mode - 2'b01: Host mode Reset Source: rst_mod_g_rst_n

14.9.3.2.2.301 USB2SS_GBL_GUCTL1 Register

1 USB2SS_GBL_GUCTL1 Register (Offset = 1Ch) [reset = 198Bh]

Global User Control Register 1

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Table 14-28755. Instance Table

Instance Name	Physical Address
USB0	**3100 C11Ch**
USB1	**3110 C11Ch**

Figure 14-9530. USB2SS_GBL_GUCTL1 Name Register

31	30	29	28	27	26	25	24
DEV_DECOUPLE_L1L2_EVT	DS_RXDET_MAX_TOUT_CTRL	FILTER_SE0_FSLS_EOP	TX_IPGAP_LINECHECK_DIS	DEV_TRB_OUT_SPR_IND	DEV_FORCE_20_CLK_FOR_30_CLK	P3_IN_U2	DEV_L1_EXIT_BY_HW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
IP_GAP_ADD_ON			DEV_LSP_TAIL_LOCK_DIS	NAK_PER_ENH_FS	NAK_PER_ENH_HS	PARKMODE_DISABLE_SS	PARKMODE_DISABLE_HS
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PARKMODE_DISABLE_FSLS	RESERVED_14_13		DISUSB2REFCLKGTNG	DISREFCLKGTNG	RESUME_OPMODE_HS_HOST	DEV_HS_NYET_BULK_SPR	L1_SUSP_THRLD_EN_FOR_HOST
R/W	R		R	R	R/W	R/W	R/W
0h	0h		1h	1h	0h	0h	1h
7	6	5	4	3	2	1	0
L1_SUSP_THRLD_FOR_HOST				HC_ERRATA_ENABLE	HC_PARCHK_DISABLE	OVRLD_L1_SUSP_COM	LOA_FILTER_EN
R/W				R/W	R/W	R/W	R/W
8h				1h	0h	1h	1h

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DEV_DECOUPLE_L1L2_EVT	R/W	0h	DEV_DECOUPLE_L1L2_EVT - 0: Default behavior, no change in device events L1/L2U3 events are not decoupled [old behavior of v2.90a and before] - 1: Feature enabled, L1 and L2 events are separated when operating in 2.0 mode. Separate event enable bits for L1 suspend and wake events. This bit is applicable for device mode only. If this feature is enabled, L1 suspend and wake events have individual controls to enable/mask them. Enable this feature if you want to get L1 [LPM] events separtely and not combined with L2 events when operating in 2.0 speeds. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	DS_RXDET_MAX_TOUT_CTRL	R/W	0h	DS_RXDET_MAX_TOUT_CTRL This bit is used to control the tRxDetectTimeoutDFP timer for the SuperSpeed link. - 0: Default behavior. 12ms is used as tRxDetectTimeoutDFP. - 1: 120ms is used as the tRxDetectTimeoutDFP. This bit is used only in host mode. For more details, refer to ECN020 for USB 3.0 Specification. Reset Source: rst_mod_g_rst_n
29	FILTER_SE0_FSLS_EOP	R/W	0h	FILTER_SE0_FSLS_EOP - 0: Default behavior, no change in Linestate check for SE0 detection in FS/LS - 1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the controller will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the controller will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the LineState has SE0 glitches during transmission. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
28	TX_IPGAP_LINECHECK_DIS	R/W	0h	TX_IPGAP_LINECHECK_DIS - 0: Default behavior, no change in Linestate check - 1: Feature enabled, 2.0 MAC disables Linestate check during HS transmit This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token [during token-to-token and token-to-data IPGAP]. When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the controller will ignore the linestate after TX and wait for fixed clocks [40 bit times equivalent] after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between [tkn to tkn/data] is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state [J] during transmission. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	DEV_TRB_OUT_SPR_IND	R/W	0h	DEV_TRB_OUT_SPR_IND - 0: Default behavior, no change in TRB status dword - 1: Feature enabled, OUT TRB status indicates Short Packet This bit is applicable for device mode only [and ignored in host mode]. If the device application [software/hardware] wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the {trbstatus, RSVD, SPR, PCM1, bufsize} dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
26	DEV_FORCE_20_CLK_FOR_30_CLK	R/W	0h	DEV_FORCE_20_CLK_FOR_30_CLK - 0: Default behavior, Uses 3.0 clock when operating in 2.0 mode - 1: Feature enabled This bit is applicable [and to be set] for device mode [DCFG.Speed != SS] only. In the 3.0 device controller, if the controller is programmed to operate in 2.0 only [that is, Device Speed is programmed to 2.0 speeds in DCFG[Speed]], then setting this bit makes the internal 2.0 [utmi/ulpi] clock to be routed as the 3.0 [pipe] clock. Enabling this feature allows the pipe3 clock to be not-running when forcibly operating in 2.0 device mode. Note: - When using this feature, all pipe3 inputs must be in inactive mode. In particular, the pipe3 clocks must not be running and the pipe3_phystatus_async must be tied to 0. This bit should not be set if the controller is programmed to operate in SuperSpeed mode [even when it falls back to 2.0]. - This bit is quasi-static, that is, it must not be changed during operation. - If the parameter "DWC_USB3_REMOVE_PIPE_CLK_MUX_FOR_20_MODE" is enabled, then muxing 2.0 clock/signals to pipe_clk/signals have to be done outside the controller for this feature to work. Reset Source: rst_mod_g_rst_n
25	P3_IN_U2	R/W	0h	P3_IN_U2 - 0: Default behavior, When SuperSpeed link is in U2, PowerState P2 is attempted on the PIPE Interface. - 1: When SuperSpeed link is in U2, PowerState P3 is attempted if GUSB3PIPECTL[17] is set. Setting this bit enables P3 Power State when the SuperSpeed link is in U2. Another Power Saving option. Check with your PHY vendor before enabling this option.When setting this bit to 1 to enable P3 in P2, GUSB3PIPECTL[27] should be set to 0 to make sure that the U2 exit is attempted in P0. This bit should be set only when GCTL.SOFITPSYNC=1 or GFLADJ.GFLADJ_REFCLK_LPM_SEL=1. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	DEV_L1_EXIT_BY_HW	R/W	0h	DEV_L1_EXIT_BY_HW - 0: Default behavior, disables device L1 hardware exit logic - 1: feature enabled This bit is applicable for device mode [2.0] only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wakeup signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This hardware remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control - When control transfers are in progress, the LPM will be rejected [NYET response]. Only after control transfers are completed [either with ACK/STALL], LPM will be accepted - For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. - When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
23:21	IP_GAP_ADD_ON	R/W	0h	This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC. This should be programmed to a non zero value only in case where you need to increase the default inter packet delay calculations in the USB 2.0 MAC module DWC_usb3_u2mac.v Reset Source: rst_mod_g_rst_n
20	DEV_LSP_TAIL_LOCK_DIS	R/W	0h	DEV_LSP_TAIL_LOCK_DIS - 0: Default behavior, enables device lsp lock logic for tail TRB update - 1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAK_PER_ENH_FS	R/W	0h	NAK_PER_ENH_FS - 1: Enables performance enhancement for FS async endpoints in the presence of NAKs - 0: Enhancement not applied If a periodic endpoint is present , and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints [bulk/ control] and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers. Reset Source: rst_mod_g_rst_n
18	NAK_PER_ENH_HS	R/W	0h	NAK_PER_ENH_HS - 1: Enables performance enhancement for HS async endpoints in the presence of NAKs - 0: Enhancement not applied If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in decrease in performance of other High Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints [bulk/ control] and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers. Reset Source: rst_mod_g_rst_n
17	PARKMODE_DISABLE_SS	R/W	0h	PARKMODE_DISABLE_SS This bit is used only in host mode, and is for debug purpose only. When this bit is set to '1' all SS bus instances in park mode are disabled. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PARKMODE_DISABLE_HS	R/W	0h	PARKMODE_DISABLE_HS This bit is used only in host mode. When this bit is set to '1' all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few high speed devices [such as Sandisk Cruzer Blade 4GB VID:1921, PID:21863 and Flex Drive VID:3744, PID:8552] when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices. Reset Source: rst_mod_g_rst_n
15	PARKMODE_DISABLE_FSLS	R/W	0h	PARKMODE_DISABLE_FSLS This bit is used only in host mode, and is for debug purpose only. When this bit is set to '1' all FS/LS bus instances in park mode disabled. Reset Source: rst_mod_g_rst_n
14:13	RESERVED_14_13	R	0h	Reserved
12	DISUSB2REFCLKGTNG	R	1h	Disable ref_clk gating for 2.0 PHY [DisUSB2RefClkGtng] If ref_clk gating is disabled, then the ref_clk input cannot be turned off to the USB 2.0 PHY and controller. This is independent of the GCTL[DisClkGtng] setting. - 1'b0: ref_clk gating enabled for USB 2.0 PHY - 1'b1: ref_clk gating disabled for USB 2.0 PHY Reset Source: rst_mod_g_rst_n
11	DISREFCLKGTNG	R	1h	Disable ref_clk gating [DisRefClkGtng] If the ref_clk gating is disabled then input ref_clk cannot be turned off to SSPHY and controller. This is independent of GCTL[DisClkGtng] setting. - 1'b0: ref_clk gating Enabled for SSPHY - 1'b1: ref_clk gating Disabled for SSPHY Reset Source: rst_mod_g_rst_n
10	RESUME_OPMODE_HS_HOST	R/W	0h	RESUME_OPMODE_HS_HOST This bit is used only in host mode, and is for USB 2.0 opmode behavior in HS Resume. - When this bit is set to '1', the UTMI/ULPI opmode will be changed to "normal" along with HS terminations after EOR. This option is to support certain legacy UTMI/ULPI PHYs. - When this bit is set to '0', the UTMI/ULPI opmode will be changed to "normal" 2us after HS terminations change after EOR. This is the default behavior. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DEV_HS_NYET_BULK_SPR	R/W	0h	DEV_HS_NYET_BULK_SPR - 0: Default behavior, no change in device response - 1: Feature enabled, HS bulk OUT short packet gets NYET response This bit is applicable for device mode only [and ignored in host mode] to be used in 2.0 operation. If this bit is set, the device controller sends NYET response instead of ACK response for a successfully received bulk OUT short packet. If NYET is sent after receiving short packet, then the host would PING before sending the next OUT. this improves the performance as well as clears up the buffer/cache on the host side. Internal to the device controller, short packet [SPR=1] processing takes some time, and during this time, the USB is flow controlled. With NYET response instead of ACK on short packet, the host does not send another OUT-DATA without pinging in HS mode. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
8	L1_SUSP_THRLD_EN_FOR_HOST	R/W	1h	L1_SUSP_THRLD_EN_FOR_HOST This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals [see "LPM Interface Signals" table in the Databook] as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: - The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0. Reset Source: rst_mod_g_rst_n
7:4	L1_SUSP_THRLD_FOR_HOST	R/W	8h	L1_SUSP_THRLD_FOR_HOST This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit. Reset Source: rst_mod_g_rst_n
3	HC_ERRATA_ENABLE	R/W	1h	Host ELD Enable [HELDEn] When this bit is set to 1, it enables the Exit Latency Delta [ELD] support defined in the xHCI 1.0 Errata. This bit is used only in the host mode. This bit has to be set to 1 in Host mode. Reset Source: rst_mod_g_rst_n
2	HC_PARCHK_DISABLE	R/W	0h	Host Parameter Check Disable [HParChkDisable] When this bit is set to '0' [by default], the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating 'PARAMETER ERROR'. When the bit is set to '1', the xHC does not perform parameter checks and does not generate 'PARAMETER ERROR' completion code. Reset Source: rst_mod_g_rst_n

Table 14-28757. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVRLD_L1_SUSP_COM	R/W	1h	OVRLD_L1_SUSP_COM If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition. Note: The recommended connection for the SUSPENDM/SLEEPM signals to the PHY with respect to this bit is as follows. For non-zero ports: Connect: - utmi_sleep_n[n] to SLEEPM[n] - [utmi_suspend_n[n] & utmi_l1_suspend_n[n]] to SUSPENDM[n] - USB2 PHYCLK[n] to utmi_clk[n] GUCTL1.OVRLD_L1_SUSP_COM impacts only Port0. For Port0: For Synopsys PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=1. With this connection, the PHY keeps PLL active so that FREECLK is always available irrespective of suspend/sleep. - Connect USB2 PHY COMMONONN to 0. - Connect utmi_sleep_n[0] to SLEEPM[0]. - Connect [utmi_suspend_n[0] & utmi_l1_suspend_n[0]] to SUSPENDM[0]. - Connect USB2 PHY FREECLK to utmi_clk[0]. - Leave utmi_suspend_com_n, utmi_l1_suspend_com_n unconnected. - GUCTL1.OVRLD_L1_SUSP_COM can be set to any value. For Third Party PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=0. With this connection the PHY can shut off all the clocks when the required conditions are met [like, GUSB2PHYCFGn[8,6], GUCTL1[1], GFLADJ[23], GCTL[10], Suspend condition, HW LPM enable etc]. - Connect -utmi_suspend_com_n to SUSPENDM[0] [or equivalent]. - Connect -utmi_l1_suspend_com_n to SLEEPM[0] [or equivalent]. - Connect PHYCLK0 [first port clock] to utmi_clk[0]. - Leave utmi_suspend_n[0], utmi_l1_suspend_ n[0], utmi_sleep_n[0] unconnected. - Set GUCTL1.OVRLD_L1_SUSP_COM to 1'b1. Reset Source: rst_mod_g_rst_n
0	LOA_FILTER_EN	R/W	1h	LOA_FILTER_EN If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.302 USB2SS_GBL_GSNPSID Register

1 USB2SS_GBL_GSNPSID Register (Offset = 20h) [reset = 5533330Bh]

Global Synopsys ID Register This is a read-only register that contains the release number of the controller.

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Table 14-28758. Instance Table

Instance Name	Physical Address
USB0	**3100 C120h**
USB1	**3110 C120h**

Figure 14-9531. USB2SS_GBL_GSNPSID Name Register

31	30	29	28	27	26	25	24
SYNOPSYSID							
R							
5533330Bh							
23	22	21	20	19	18	17	16
SYNOPSYSID							
R							
5533330Bh							
15	14	13	12	11	10	9	8
SYNOPSYSID							
R							
5533330Bh							
7	6	5	4	3	2	1	0
SYNOPSYSID							
R							
5533330Bh							

Table 14-28760. USB2SS_GBL_GSNPSID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNOPSYSID	R	5533330Bh	Synopsys ID - SynopsysID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 [DWC_usb3]. - SynopsysID[15:0] indicates the release number. Current Release is 3.30a. Software uses this register to configure release-specific features in the driver. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.303 USB2SS_GBL_GGPIO Register

1 USB2SS_GBL_GGPIO Register (Offset = 24h) [reset = 0h]

Global General Purpose Input/Output Register The application can use this register for general purpose input and output ports or for debugging.

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Table 14-28761. Instance Table

Instance Name	Physical Address
USB0	**3100 C124h**
USB1	**3110 C124h**

Figure 14-9532. USB2SS_GBL_GGPIO Name Register

31	30	29	28	27	26	25	24
GPO							
R/W							
0h							
23	22	21	20	19	18	17	16
GPO							
R/W							
0h							
15	14	13	12	11	10	9	8
GPI							
R							
0h							
7	6	5	4	3	2	1	0
GPI							
R							
0h							

Table 14-28763. USB2SS_GBL_GGPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GPO	R/W	0h	General Purpose Output The value of this field is driven out on the gp_out[15:0] output port. Reset Source: rst_mod_g_rst_n
15:0	GPI	R	0h	General Purpose Input The read value of this field reflects the gp_in[15:0] input signal value. Note: Register bit-bash test should not check for reset value of this field since its not predictable. depends on the gp_in port. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.304 USB2SS_GBL_GUID Register

1 USB2SS_GBL_GUID Register (Offset = 28h) [reset = 0h]

Global User ID Register This is a read/write register containing the User ID. The power-on value for this register is specified as the User Identification Register. Power-on value during coreConsultant configuration (parameter DWC_USB3_USERID). This register can be used in the following ways: - To store the version or revision of your system. - To store hardware configurations that are outside the controller. - As a scratch register.

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Table 14-28764. Instance Table

Instance Name	Physical Address
USB0	**3100 C128h**
USB1	**3110 C128h**

Figure 14-9533. USB2SS_GBL_GUID Name Register

31	30	29	28	27	26	25	24
USERID							
R/W							
0h							
23	22	21	20	19	18	17	16
USERID							
R/W							
0h							
15	14	13	12	11	10	9	8
USERID							
R/W							
0h							
7	6	5	4	3	2	1	0
USERID							
R/W							
0h							

Table 14-28766. USB2SS_GBL_GUID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USERID	R/W	0h	USERID Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.305 USB2SS_GBL_GUCTL Register

1 USB2SS_GBL_GUCTL Register (Offset = 2Ch) [reset = C800010h]

Global User Control Register: This register provides a few options for the software to control the controller behavior in the Host mode. Most of the options are used to improve host inter-operability with different devices.

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Table 14-28767. Instance Table

Instance Name	Physical Address
USB0	**3100 C12Ch**
USB1	**3110 C12Ch**

Figure 14-9534. USB2SS_GBL_GUCTL Name Register

31	30	29	28	27	26	25	24
REFCLKPER							
R/W							
32h							
23	22	21	20	19	18	17	16
REFCLKPER		NOEXTRDL	RESERVED_20_18			SPRSCTRLTRANSEN	RESBWHSEPS
R/W		R/W	R			R/W	R/W
32h		0h	0h			0h	0h
15	14	13	12	11	10	9	8
RESERVED_15	USBHSTINAUTORETRYEN	ENOVERLAPCHK	EXTCAPSUPPTEN	INSRTEXTRFSBODI	DTCT		DTFT
R	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		10h
7	6	5	4	3	2	1	0
DTFT							
R/W							
10h							

Table 14-28769. USB2SS_GBL_GUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	REFCLKPER	R/W	32h	REFCLKPER This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 [8ns/125 MHz]. This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to '1'. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to '0' at any time. If you never plan to use this feature, then set this field to 'h8, the default value. Reset Source: rst_mod_g_rst_n

Table 14-28769. USB2SS_GBL_GUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NOEXTRDL	R/W	0h	No Extra Delay Between SOF and the First Packet[NoExtrDl] Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. - 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. - 1'b1: Host doesn't wait after a SOF before it sends the first USB packet. Reset Source: rst_mod_g_rst_n
20:18	RESERVED_20_18	R	0h	Reserved
17	SPRSCTRLTRANSEN	R/W	0h	Sparse Control Transaction Enable Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames. Reset Source: rst_mod_g_rst_n
16	RESBWHSEPS	R/W	0h	Reserving 85% Bandwidth for HS Periodic EPs [ResBwHSEPS] By default, HC reserves 800f the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 800andwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices [HD Webcams] are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 paylod per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved
14	USBHSTINAUTORETRYEN	R/W	0h	Host IN Auto Retry [USBHstInAutoRetryEn] When set, this field enables the Auto Retry feature. For IN transfers [non-isochronous] that encounter data packets with CRC errors or internal overrun scenarios, the auto retry feature causes the Host controller to reply to the device with a non-terminating retry ACK [that is, an ACK transaction packet with Retry = 1 and NumP != 0]. If the Auto Retry feature is disabled [default], the controller will respond with a terminating retry ACK [that is, an ACK transaction packet with Retry = 1 and NumP = 0]. - 1'b0: Auto Retry Disabled - 1'b1: Auto Retry Enabled Note: When enabling Auto Retry feature, if the system latency is large enough to cause the internal PSQ full [PSQ can be full as the result of messages not being processed because of pending fetches before flushing the TxQ due to NRDY/ERDY conditions], then the host controller can generate a transaction error. Reset Source: rst_mod_g_rst_n

Table 14-28769. USB2SS_GBL_GUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENOVERLAPCHK	R/W	0h	Enable Check for LFPS Overlap During Remote Ux Exit: If this bit is set to, - 1'b1: The SuperSpeed link when exiting U1/U2/U3 waits for either the remote link LFPS or TS1/TS2 training symbols before it confirms that the LFPS handshake is complete. This is done to handle the case where the LFPS glitch causes the link to start exiting from the low power state. Looking for the LFPS overlap makes sure that the link partner also sees the LFPS. - 1'b0: When the link exists U1/U2/U3 because of a remote exit, it does not look for an LFPS overlap. Reset Source: rst_mod_g_rst_n
12	EXTCAPSUPPTEN	R/W	0h	External Extended Capability Support Enable [ExtCapSuptEN] When set, this field enables extended capabilities to be implemented outside the controller. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in "Debug Capability" returns 16. A read to the first DWORD of the last internal extended capability [the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled] returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability [for example, at address N+16 where N is the address of this DWORD]. If enabled, an external address decoder that snoops the xHC target interface must be implemented. If it sees an access to N+16 or greater, the target access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer field. This indicates there are no more capabilities. Reset Source: rst_mod_g_rst_n
11	INSRTEXTRFSBODI	R/W	0h	Insert Extra Delay Between FS Bulk OUT Transactions [InsrtExtrFSBODI]. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. - 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. - 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices. Reset Source: rst_mod_g_rst_n

Table 14-28769. USB2SS_GBL_GUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:9	DTCT	R/W	0h	Device Timeout Coarse Tuning [DTCT] This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The controller first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: - 2'b00: 0 usec -> use DTFT value instead - 2'b01: 500 usec - 2'b10: 1.5 msec - 2'b11: 6.5 msec Note: When the system latency is larger than the programmed DTCT/DTFT value, if the host controller is not able to accept certain transactions on the bus [because of system bus delays], the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay. Reset Source: rst_mod_g_rst_n
8:0	DTFT	R/W	10h	Device Timeout Fine Tuning [DTFT] This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk [8 ns period], this is calculated as follows: [DTFT value] * 256 * [8 ns] Quick Reference: - if DTFT = 0x2, 2*256*8 = 4usec timeout - if DTFT = 0x5, 5*256*8 = 10usec timeout - if DTFT = 0xA, 10*256*8 = 20usec timeout - if DTFT = 0x10, 16*256*8 = 32usec timeout - if DTFT = 0x19, 25*256*8 = 51usec timeout - if DTFT = 0x31, 49*256*8 = 100usec timeout - if DTFT = 0x62, 98*256*8 = 200usec timeout Note: When the system latency is larger than the programmed DTCT/DTFT value, if the host controller is not able to accept certain transactions on the bus [because of system bus delays], the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.306 USB2SS_GBL_GBUSERRADDRLO Register

1 USB2SS_GBL_GBUSERRADDRLO Register (Offset = 30h) [reset = 0h]

Gobal SoC Bus Error Address Register - Low This is an alternate register for the GBUSERRADDR register.

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Table 14-28770. Instance Table

Instance Name	Physical Address
USB0	**3100 C130h**
USB1	**3110 C130h**

Figure 14-9535. USB2SS_GBL_GBUSERRADDRLO Name Register

31	30	29	28	27	26	25	24
BUSERRADDR							
R							
0h							
23	22	21	20	19	18	17	16
BUSERRADDR							
R							
0h							
15	14	13	12	11	10	9	8
BUSERRADDR							
R							
0h							
7	6	5	4	3	2	1	0
BUSERRADDR							
R							
0h							

Table 14-28772. USB2SS_GBL_GBUSERRADDRLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUSERRADDR	R	0h	Bus Address - Low [BusAddrLo] This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.307 USB2SS_GBL_GBUSERRADDRHI Register

1 USB2SS_GBL_GBUSERRADDRHI Register (Offset = 34h) [reset = 0h]

Gobal SoC Bus Error Address Register - High This is an alternate register for the GBUSERRADDR register.

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Table 14-28773. Instance Table

Instance Name	Physical Address
USB0	**3100 C134h**
USB1	**3110 C134h**

Figure 14-9536. USB2SS_GBL_GBUSERRADDRHI Name Register

31	30	29	28	27	26	25	24
BUSERRADDR							
R							
0h							
23	22	21	20	19	18	17	16
BUSERRADDR							
R							
0h							
15	14	13	12	11	10	9	8
BUSERRADDR							
R							
0h							
7	6	5	4	3	2	1	0
BUSERRADDR							
R							
0h							

Table 14-28775. USB2SS_GBL_GBUSERRADDRHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUSERRADDR	R	0h	Bus Address - High [BusAddrHi] This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.308 USB2SS_GBL_GPRTBIMAPLO Register

1 USB2SS_GBL_GPRTBIMAPLO Register (Offset = 38h) [reset = 0h]

Global SS Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP register. Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. For a configuration with number of USB 3.0 ports same as number of SS Bus Instances, do not remap during debug session. If you remap for some reason, then the debug host must be connected to a port which has a dedicated SS Bus Instance. For example, if DWC_USB3_NUM_U3_ROOT_PORTS =3 and DWC_USB3_NUM_SS_USB_INSTANCES=3, and software maps the first SS port to the first SS BI and the second/third port to the second BI, then the debug host can be connected to the first port only. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-28776. Instance Table

Instance Name	Physical Address
USB0	**3100 C138h**
USB1	**3110 C138h**

Figure 14-9537. USB2SS_GBL_GPRTBIMAPLO Name Register

31	30	29	28	27	26	25	24
BINUM8				BINUM7			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BINUM6				BINUM5			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BINUM4				BINUM3			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BINUM2				BINUM1			
R				R/W			
0h				0h			

Table 14-28778. USB2SS_GBL_GPRTBIMAPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: SS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: SS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6: SS USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-28778. USB2SS_GBL_GPRTBIMAPLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BINUM5	R	0h	BINUM5: SS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM4	R	0h	BINUM4: SS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM3	R	0h	BINUM3: SS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM2	R	0h	BINUM2: SS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: SS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.309 USB2SS_GBL_GPRTBIMAPHI Register

1 USB2SS_GBL_GPRTBIMAPHI Register (Offset = 3Ch) [reset = 0h]

Global SS Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP register. For a configuration with number of USB 3.0 ports same as number of SS Bus Instances, do not remap during debug session. If you remap for some reason, then the debug host must be connected to a port which has a dedicated SS Bus Instance. For example, if DWC_USB3_NUM_U3_ROOT_PORTS =3 and DWC_USB3_NUM_SS_USB_INSTANCES=3, and software maps the first SS port to the first SS BI and the second/third port to the second BI, then the debug host can be connected to the first port only. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-28779. Instance Table

Instance Name	Physical Address
USB0	**3100 C13Ch**
USB1	**3110 C13Ch**

Figure 14-9538. USB2SS_GBL_GPRTBIMAPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_28				BINUM15			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BINUM14				BINUM13			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BINUM12				BINUM11			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BINUM10				BINUM9			
R				R			
0h				0h			

Table 14-28781. USB2SS_GBL_GPRTBIMAPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: SS USB Instance Number for Port 15. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: SS USB Instance Number for Port 14. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: SS USB Instance Number for Port 13. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: SS USB Instance Number for Port 12. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-28781. USB2SS_GBL_GPRTBIMAPHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	BINUM11	R	0h	BINUM11: SS USB Instance Number for Port 11. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM10	R	0h	BINUM10: SS USB Instance Number for Port 10. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM9	R	0h	BINUM9: SS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.310 USB2SS_GBL_GHWPARAMS0 Register

1 USB2SS_GBL_GHWPARAMS0 Register (Offset = 40h) [reset = 4020400Ah]

Global Hardware Parameters Register 0 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28782. Instance Table

Instance Name	Physical Address
USB0	**3100 C140h**
USB1	**3110 C140h**

Figure 14-9539. USB2SS_GBL_GHWPARAMS0 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS0_31_24							
R							
40h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS0_23_16							
R							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS0_15_8							
R							
40h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS0_7_6		GHWPARAMS0_5_3			GHWPARAMS0_2_0		
R		R			R		
0h		1h			2h		

Table 14-28784. USB2SS_GBL_GHWPARAMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GHWPARAMS0_31_24	R	40h	DWC_USB3_AWIDTH Reset Source: rst_mod_g_rst_n
23:16	GHWPARAMS0_23_16	R	20h	DWC_USB3_SDWIDTH Reset Source: rst_mod_g_rst_n
15:8	GHWPARAMS0_15_8	R	40h	DWC_USB3_MDWIDTH Reset Source: rst_mod_g_rst_n
7:6	GHWPARAMS0_7_6	R	0h	DWC_USB3_SBUS_TYPE Reset Source: rst_mod_g_rst_n
5:3	GHWPARAMS0_5_3	R	1h	DWC_USB3_MBUS_TYPE Reset Source: rst_mod_g_rst_n
2:0	GHWPARAMS0_2_0	R	2h	DWC_USB3_MODE Reset Source: rst_mod_g_rst_n

14.9.3.2.2.311 USB2SS_GBL_GHWPARAMS1 Register

1 USB2SS_GBL_GHWPARAMS1 Register (Offset = 44h) [reset = 1A4493Bh]

Global Hardware Parameters Register 1 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28785. Instance Table

Instance Name	Physical Address
USB0	**3100 C144h**
USB1	**3110 C144h**

Figure 14-9540. USB2SS_GBL_GHWPARAMS1 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS1_31	GHWPARAMS1_30	GHWPARAMS1_29	GHWPARAMS1_28	GHWPARAMS1_27	GHWPARAMS1_26	GHWPARAMS1_25_24	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	1h	
23	22	21	20	19	18	17	16
GHWPARAMS1_23	GHWPARAMS1_22_21		GHWPARAMS1_20_15				
R	R		R				
1h	1h		8h				
15	14	13	12	11	10	9	8
GHWPARAMS1_20_15	GHWPARAMS1_14_12			GHWPARAMS1_11_9			GHWPARAMS1_8_6
R	R			R			R
8h	4h			4h			4h
7	6	5	4	3	2	1	0
GHWPARAMS1_8_6		GHWPARAMS1_5_3			GHWPARAMS1_2_0		
R		R			R		
4h		7h			3h		

Table 14-28787. USB2SS_GBL_GHWPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GHWPARAMS1_31	R	0h	DWC_USB3_EN_DBC Reset Source: rst_mod_g_rst_n
30	GHWPARAMS1_30	R	0h	DWC_USB3_RM_OPT_FEATURES Reset Source: rst_mod_g_rst_n
29	GHWPARAMS1_29	R	0h	Reserved1 Reset Source: rst_mod_g_rst_n
28	GHWPARAMS1_28	R	0h	DWC_USB3_RAM_BUS_CLKS_SYNC Reset Source: rst_mod_g_rst_n
27	GHWPARAMS1_27	R	0h	DWC_USB3_MAC_RAM_CLKS_SYNC Reset Source: rst_mod_g_rst_n

Table 14-28787. USB2SS_GBL_GHWPARAMS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	GHWPARAMS1_26	R	0h	DWC_USB3_MAC_PHY_CLKS_SYNC Reset Source: rst_mod_g_rst_n
25:24	GHWPARAMS1_25_24	R	1h	DWC_USB3_EN_PWROPT Reset Source: rst_mod_g_rst_n
23	GHWPARAMS1_23	R	1h	DWC_USB3_SPRAM_TYP Reset Source: rst_mod_g_rst_n
22:21	GHWPARAMS1_22_21	R	1h	DWC_USB3_NUM_RAMS Reset Source: rst_mod_g_rst_n
20:15	GHWPARAMS1_20_15	R	8h	DWC_USB3_DEVICE_NUM_INT For details on DWC_USB3_DEVICE_NUM_INT, refer to <workspace>/src/DWC_usb3_params.v file. Reset Source: rst_mod_g_rst_n
14:12	GHWPARAMS1_14_12	R	4h	DWC_USB3_ASPACEWIDTH Reset Source: rst_mod_g_rst_n
11:9	GHWPARAMS1_11_9	R	4h	DWC_USB3_REQINFOWIDTH Reset Source: rst_mod_g_rst_n
8:6	GHWPARAMS1_8_6	R	4h	DWC_USB3_DATAINFOWIDTH Reset Source: rst_mod_g_rst_n
5:3	GHWPARAMS1_5_3	R	7h	DWC_USB3_BURSTWIDTH-1 Reset Source: rst_mod_g_rst_n
2:0	GHWPARAMS1_2_0	R	3h	DWC_USB3_IDWIDTH-1 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.312 USB2SS_GBL_GHWPARAMS2 Register

1 USB2SS_GBL_GHWPARAMS2 Register (Offset = 48h) [reset = 0h]

Global Hardware Parameters Register 2 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28788. Instance Table

Instance Name	Physical Address
USB0	**3100 C148h**
USB1	**3110 C148h**

Figure 14-9541. USB2SS_GBL_GHWPARAMS2 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS2_31_0							
R							
0h							
23	22	21	20	19	18	17	16
GHWPARAMS2_31_0							
R							
0h							
15	14	13	12	11	10	9	8
GHWPARAMS2_31_0							
R							
0h							
7	6	5	4	3	2	1	0
GHWPARAMS2_31_0							
R							
0h							

Table 14-28790. USB2SS_GBL_GHWPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GHWPARAMS2_31_0	R	0h	DWC_USB3_USERID Reset Source: rst_mod_g_rst_n

14.9.3.2.2.313 USB2SS_GBL_GHWPARAMS3 Register

1 USB2SS_GBL_GHWPARAMS3 Register (Offset = 4Ch) [reset = 10420084h]

Global Hardware Parameters Register 3 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28791. Instance Table

Instance Name	Physical Address
USB0	**3100 C14Ch**
USB1	**3110 C14Ch**

Figure 14-9542. USB2SS_GBL_GHWPARAMS3 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS3_31	GHWPARAMS3_30_23						
R	R						
0h	20h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS3_30_23	GHWPARAMS3_22_18					GHWPARAMS3_17_12	
R	R					R	
20h	10h					20h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS3_17_12				GHWPARAMS3_11	GHWPARAMS3_10	GHWPARAMS3_9_8	
R				R	R	R	
20h				0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS3_7_6		GHWPARAMS3_5_4		GHWPARAMS3_3_2		GHWPARAMS3_1_0	
R		R		R		R	
2h		0h		1h		0h	

Table 14-28793. USB2SS_GBL_GHWPARAMS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GHWPARAMS3_31	R	0h	Reserved Reset Source: rst_mod_g_rst_n
30:23	GHWPARAMS3_30_23	R	20h	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES Reset Source: rst_mod_g_rst_n
22:18	GHWPARAMS3_22_18	R	10h	DWC_USB3_NUM_IN_EPS Reset Source: rst_mod_g_rst_n
17:12	GHWPARAMS3_17_12	R	20h	DWC_USB3_NUM_EPS Reset Source: rst_mod_g_rst_n
11	GHWPARAMS3_11	R	0h	DWC_USB3_ULPI_CARKIT Reset Source: rst_mod_g_rst_n

Table 14-28793. USB2SS_GBL_GHWPARAMS3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	GHWPARAMS3_10	R	0h	DWC_USB3_VENDOR_CTL_INTERFACE Reset Source: rst_mod_g_rst_n
9:8	GHWPARAMS3_9_8	R	0h	Reserved Reset Source: rst_mod_g_rst_n
7:6	GHWPARAMS3_7_6	R	2h	DWC_USB3_HSPHY_DWIDTH Reset Source: rst_mod_g_rst_n
5:4	GHWPARAMS3_5_4	R	0h	DWC_USB3_FSPHY_INTERFACE Reset Source: rst_mod_g_rst_n
3:2	GHWPARAMS3_3_2	R	1h	DWC_USB3_HSPHY_INTERFACE Reset Source: rst_mod_g_rst_n
1:0	GHWPARAMS3_1_0	R	0h	DWC_USB3_SSPHY_INTERFACE Reset Source: rst_mod_g_rst_n

14.9.3.2.2.314 USB2SS_GBL_GHWPARAMS4 Register

1 USB2SS_GBL_GHWPARAMS4 Register (Offset = 50h) [reset = 47A22004h]

Global Hardware Parameters Register 4 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28794. Instance Table

Instance Name	Physical Address
USB0	**3100 C150h**
USB1	**3110 C150h**

Figure 14-9543. USB2SS_GBL_GHWPARAMS4 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS4_31_28				GHWPARAMS4_27_24			
R				R			
4h				7h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS4_23	GHWPARAMS4_22	GHWPARAMS4_21	GHWPARAMS4_20_17				GHWPARAMS4_16_13
R	R	R	R				R
1h	0h	1h	1h				1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS4_16_13			GHWPARAMS4_12	GHWPARAMS4_11	GHWPARAMS4_10_9		GHWPARAMS4_8_7
R			R	R	R		R
1h			0h	0h	0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS4_8_7	GHWPARAMS4_6	GHWPARAMS4_5_0					
R	R	R					
0h	0h	4h					

Table 14-28796. USB2SS_GBL_GHWPARAMS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	GHWPARAMS4_31_28	R	4h	DWC_USB3_BMU_LSP_DEPTH Reset Source: rst_mod_g_rst_n
27:24	GHWPARAMS4_27_24	R	7h	DWC_USB3_BMU_PTL_DEPTH-1 Reset Source: rst_mod_g_rst_n
23	GHWPARAMS4_23	R	1h	DWC_USB3_EN_ISOC_SUPT Reset Source: rst_mod_g_rst_n
22	GHWPARAMS4_22	R	0h	Reserved Reset Source: rst_mod_g_rst_n
21	GHWPARAMS4_21	R	1h	DWC_USB3_EXT_BUFF_CONTROL Reset Source: rst_mod_g_rst_n

Table 14-28796. USB2SS_GBL_GHWPARAMS4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:17	GHWPARAMS4_20_17	R	1h	DWC_USB3_NUM_SS_USB_INSTANCES Reset Source: rst_mod_g_rst_n
16:13	GHWPARAMS4_16_13	R	1h	DWC_USB3_HIBER_SCRATCHBUFS Number of external scratchpad buffers the controller requires to save its internal state in the device mode. Each buffer is assumed to be 4KB. The scratchpad buffer array must have this many buffer pointers. Reset Source: rst_mod_g_rst_n
12	GHWPARAMS4_12	R	0h	Reserved Reset Source: rst_mod_g_rst_n
11	GHWPARAMS4_11	R	0h	Reserved Reset Source: rst_mod_g_rst_n
10:9	GHWPARAMS4_10_9	R	0h	Reserved Reset Source: rst_mod_g_rst_n
8:7	GHWPARAMS4_8_7	R	0h	Reserved Reset Source: rst_mod_g_rst_n
6	GHWPARAMS4_6	R	0h	Reserved Reset Source: rst_mod_g_rst_n
5:0	GHWPARAMS4_5_0	R	4h	DWC_USB3_CACHE_TRBS_PER_TRANSFER Reset Source: rst_mod_g_rst_n

14.9.3.2.2.315 USB2SS_GBL_GHWPARAMS5 Register

1 USB2SS_GBL_GHWPARAMS5 Register (Offset = 54h) [reset = 4202088h]

Global Hardware Parameters Register 5 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28797. Instance Table

Instance Name	Physical Address
USB0	**3100 C154h**
USB1	**3110 C154h**

Figure 14-9544. USB2SS_GBL_GHWPARAMS5 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS5_31_28				GHWPARAMS5_27_22			
R				R			
0h				10h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS5_27_22		GHWPARAMS5_21_16					
R		R					
10h		20h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS5_15_10						GHWPARAMS5_9_4	
R						R	
8h						8h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS5_9_4				GHWPARAMS5_3_0			
R				R			
8h				8h			

Table 14-28799. USB2SS_GBL_GHWPARAMS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	GHWPARAMS5_31_28	R	0h	Reserved Reset Source: rst_mod_g_rst_n
27:22	GHWPARAMS5_27_22	R	10h	DWC_USB3_DFQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
21:16	GHWPARAMS5_21_16	R	20h	DWC_USB3_DWQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
15:10	GHWPARAMS5_15_10	R	8h	DWC_USB3_TXQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
9:4	GHWPARAMS5_9_4	R	8h	DWC_USB3_RXQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
3:0	GHWPARAMS5_3_0	R	8h	DWC_USB3_BMU_BUSGM_DEPTH Reset Source: rst_mod_g_rst_n

14.9.3.2.2.316 USB2SS_GBL_GHWPARAMS6 Register

1 USB2SS_GBL_GHWPARAMS6 Register (Offset = 58h) [reset = 1C268020h]

Global Hardware Parameters Register 6 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28800. Instance Table

Instance Name	Physical Address
USB0	**3100 C158h**
USB1	**3110 C158h**

Figure 14-9545. USB2SS_GBL_GHWPARAMS6 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS6_31_16							
R							
1C26h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS6_31_16							
R							
1C26h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BUSFLTRSSUPPORT	BCSUPPORT	OTG_SS_SUPPORT	ADPSUPPORT	HNPSUPPORT	SRPSUPPORT	GHWPARAMS6_9_8	
R	R	R	R	R	R	R	
1h	0h	0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS6_7	GHWPARAMS6_6	GHWPARAMS6_5_0					
R	R	R					
0h	0h	20h					

Table 14-28802. USB2SS_GBL_GHWPARAMS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GHWPARAMS6_31_16	R	1C26h	DWC_USB3_RAM0_DEPTH Reset Source: rst_mod_g_rst_n
15	BUSFLTRSSUPPORT	R	1h	DWC_USB3_EN_BUS_FILTERS Reset Source: rst_mod_g_rst_n
14	BCSUPPORT	R	0h	DWC_USB3_EN_BC Reset Source: rst_mod_g_rst_n
13	OTG_SS_SUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
12	ADPSUPPORT	R	0h	DWC_USB3_EN_ADP Reset Source: rst_mod_g_rst_n

Table 14-28802. USB2SS_GBL_GHWPARAMS6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	HNPSUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
10	SRPSUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
9:8	GHWPARAMS6_9_8	R	0h	Reserved Reset Source: rst_mod_g_rst_n
7	GHWPARAMS6_7	R	0h	DWC_USB3_EN_FPGA Reset Source: rst_mod_g_rst_n
6	GHWPARAMS6_6	R	0h	DWC_USB3_EN_DBG_PORTS Reset Source: rst_mod_g_rst_n
5:0	GHWPARAMS6_5_0	R	20h	DWC_USB3_PSQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n

14.9.3.2.2.317 USB2SS_GBL_GHWPARAMS7 Register

1 USB2SS_GBL_GHWPARAMS7 Register (Offset = 5Ch) [reset = 0h]

Global Hardware Parameters Register 7 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28803. Instance Table

Instance Name	Physical Address
USB0	**3100 C15Ch**
USB1	**3110 C15Ch**

Figure 14-9546. USB2SS_GBL_GHWPARAMS7 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS7_31_16							
R							
0h							
23	22	21	20	19	18	17	16
GHWPARAMS7_31_16							
R							
0h							
15	14	13	12	11	10	9	8
GHWPARAMS7_15_0							
R							
0h							
7	6	5	4	3	2	1	0
GHWPARAMS7_15_0							
R							
0h							

Table 14-28805. USB2SS_GBL_GHWPARAMS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GHWPARAMS7_31_16	R	0h	DWC_USB3_RAM2_DEPTH Reset Source: rst_mod_g_rst_n
15:0	GHWPARAMS7_15_0	R	0h	DWC_USB3_RAM1_DEPTH Reset Source: rst_mod_g_rst_n

14.9.3.2.2.318 USB2SS_GBL_GDBGFIFOSPACE Register

1 USB2SS_GBL_GDBGFIFOSPACE Register (Offset = 60h) [reset = C0000h]

Global Debug Queue/FIFO Space Available Register Bit Bash test should not be done on this debug register.

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Table 14-28806. Instance Table

Instance Name	Physical Address
USB0	**3100 C160h**
USB1	**3110 C160h**

Figure 14-9547. USB2SS_GBL_GDBGFIFOSPACE Name Register

31	30	29	28	27	26	25	24
SPACE_AVAILABLE							
R							
Ch							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPACE_AVAILABLE							
R							
Ch							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15_9							FIFO_QUEUE_SELECT
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO_QUEUE_SELECT							
R/W							
0h							

Table 14-28808. USB2SS_GBL_GDBGFIFOSPACE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPACE_AVAILABLE	R	Ch	SPACE_AVAILABLE Reset Source: rst_mod_g_rst_n
15:9	RESERVED_15_9	R	0h	Reserved

Table 14-28808. USB2SS_GBL_GDBGFIFOSPACE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:0	FIFO_QUEUE_SELECT	R/W	0h	FIFO/Queue Select [or] Port-Select - FIFO/Queue Select[8:5] indicates the FIFO/Queue Type - FIFO/Queue Select[4:0] indicates the FIFO/Queue Number For example, 9'b0_0010_0001 refers to RxFIFO_1 and 9'b0_0101_1110 refers to TxReqQ_30. - 9'b0_0001_1111 to 9'b0_0000_0000: TxFIFO_31 to TxFIFO_0 - 9'b0_0011_1111 to 9'b0_0010_0000: RxFIFO_31 to RxFIFO_0 - 9'b0_0101_1111 to 9'b0_0100_0000: TxReqQ_31 to TxReqQ_0 - 9'b0_0111_1111 to 9'b0_0110_0000: RxReqQ_31 to RxReqQ_0 - 9'b0_1001_1111 to 9'b0_1000_0000: RxInfoQ_31 to RxInfoQ_0 - 9'b0_1010_0000: DescFetchQ_0 [for backwards compatibility] - 9'b0_1010_0001: EventQ_0 [for backwards compatibility] - 9'b0_1010_0010: ProtocolStatusQ_0 - 9'b0_1101_1111 to 9'b0_1110_0000: DescFetchQ_31 to DescFetchQ_0 - 9'b0_1111_1111 to 9'b0_1110_0000: WriteBack/EventQ_31 to WriteBack/EventQ_0 - 9'b1_0000_0111 to 9'b1_0000_0000: AuxEventQ_7 to AuxEventQ_0 [if EN_SEPARATE_DESC_QUEUES=1] Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.319 USB2SS_GBL_GDBGLTSSM Register

1 USB2SS_GBL_GDBGLTSSM Register (Offset = 64h) [reset = 41010440h]

Global Debug LTSSM Register In multi-port host configuration, the port-number is defined by Port-Select[3:0] field in the GDBGFIFOSPACE register. Note: - GDBGLTSSM register is not applicable for USB 2.0-only mode. - Bit Bash test should not be done on this debug register.

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Table 14-28809. Instance Table

Instance Name	Physical Address
USB0	**3100 C164h**
USB1	**3110 C164h**

Figure 14-9548. USB2SS_GBL_GDBGLTSSM Name Register

31	30	29	28	27	26	25	24
RESERVED_31_31	RXELECIDLE	X3_XS_SWAPPING	X3_DS_HOST_SHUTDOWN	PRTDIRECTION	LTDBTIMEOUT	LTDBLINKSTATE	
R	R	R	R	R	R	R	
0h	1h	0h	0h	0h	0h	4h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LTDBLINKSTATE		LTDBSUBSTATE				ELASTICBUFFERMODE	TXELECLDLE
R		R				R	R
4h		0h				0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RXPOLARITY	TXDETRXLOOPBACK	LTDBPHYCMDSTATE			POWERDOWN		RXEQTRAIN
R	R	R			R		R
0h	0h	0h			2h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXDEEMPHASIS		LTDBCLKSTATE			TXSWING	RXTERMINATION	TXONESZEROS
R		R			R	R	R
1h		0h			0h	0h	0h

Table 14-28811. USB2SS_GBL_GDBGLTSSM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31_31	R	0h	Reserved
30	RXELECIDLE	R	1h	RxElecidle For description of RxElecIdle, see table 5-4, "Status Interface Signals" of the PIPE3 Specification. Reset Source: rst_mod_g_rst_n
29	X3_XS_SWAPPING	R	0h	Reserved Reset Source: rst_mod_g_rst_n
28	X3_DS_HOST_SHUTDOWN	R	0h	Reserved Reset Source: rst_mod_g_rst_n
27	PRTDIRECTION	R	0h	Reserved Reset Source: rst_mod_g_rst_n
26	LTDBTIMEOUT	R	0h	LTDB Timeout [LTDBTimeout] Reset Source: rst_mod_g_rst_n

Table 14-28811. USB2SS_GBL_GDBGLTSSM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:22	LTDBLINKSTATE	R	4h	LTDB Link State [LTDBLinkState] Reset Source: rst_mod_g_rst_n
21:18	LTDBSUBSTATE	R	0h	LTDB Sub-State [LTDBSubState] Reset Source: rst_mod_g_rst_n
17	ELASTICBUFFERMODE	R	0h	Elastic Buffer Mode [ElasticBufferMode] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
16	TXELECLDLE	R	1h	Tx Elec Idle [TxElecIdle] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
15	RXPOLARITY	R	0h	Rx Polarity [RxPolarity] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
14	TXDETRXLOOPBACK	R	0h	Tx Detect Rx/Loopback [TxDetRxLoopback] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
13:11	LTDBPHYCMDSTATE	R	0h	LTSSM PHY command State [LTDBPhyCmdState] - 000: PHY_IDLE [PHY command state is in IDLE. No PHY request pending] - 001: PHY_DET [Request to start Receiver detection] - 010: PHY_DET_3 [Wait for Phy_Status [Receiver detection]] - 011: PHY_PWR_DLY [Delay Pipe3_PowerDown P0 -> P1/P2/P3 request] - 100: PHY_PWR_A [Delay for internal logic] - 101: PHY_PWR_B [Wait for Phy_Status[Power state change request]] Reset Source: rst_mod_g_rst_n
10:9	POWERDOWN	R	2h	POWERDOWN [PowerDown] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
8	RXEQTRAIN	R	0h	RxEq Train For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
7:6	TXDEEMPHASIS	R	1h	TXDEEMPHASIS [TxDeemphasis] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
5:3	LTDBCLKSTATE	R	0h	LTSSM Clock State [LTDBClkState] In multi-port host configuration, the port number is defined by Port-Select[3:0] field in the GDBGFIFOSPACE register. Note: GDBGLTSSM register is not applicable for USB 2.0-only mode. - 000: CLK_NORM [PHY is in non-P3 state and PCLK is running] - 001: CLK_TO_P3 [P3 entry request to PHY]. - 010: CLK_WAIT1 [Wait for Phy_Status [P3 request]]. - 011: CLK_P3 [PHY is in P3 and PCLK is not running]. - 100: CLK_TO_P0 [P3 exit request to PHY]. - 101: CLK_WAIT2 [Wait for Phy_Status [P3 exit request]] Reset Source: rst_mod_g_rst_n
2	TXSWING	R	0h	Tx Swing [TxSwing] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n

Table 14-28811. USB2SS_GBL_GDBGLTSSM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RXTERMINATION	R	0h	Rx Termination [RxTermination] For details on DWC_USB3_PIPE_RXTERM_RESET_VAL, refer to <workspace>/src/DWC_usb3_params.v Reset Source: rst_mod_g_rst_n
0	TXONESZEROS	R	0h	Tx Ones/Zeros [TxOnesZeros] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.320 USB2SS_GBL_GDBGLNMCC Register

1 USB2SS_GBL_GDBGLNMCC Register (Offset = 68h) [reset = 0h]

Global Debug LNMCC Register Bit Bash test should not be done on this debug register.

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Table 14-28812. Instance Table

Instance Name	Physical Address
USB0	**3100 C168h**
USB1	**3110 C168h**

Figure 14-9549. USB2SS_GBL_GDBGLNMCC Name Register

31	30	29	28	27	26	25	24
RESERVED_31_9							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_9							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_31_9							LNMCC_BERC
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LNMCC_BERC							
R							
0h							

Table 14-28814. USB2SS_GBL_GDBGLNMCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_31_9	R	0h	Reserved
8:0	LNMCC_BERC	R	0h	This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.321 USB2SS_GBL_GDBGBMU Register

1 USB2SS_GBL_GDBGBMU Register (Offset = 6Ch) [reset = 0h]

Global Debug BMU Register Bit Bash test should not be done on this debug register.

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Table 14-28815. Instance Table

Instance Name	Physical Address
USB0	**3100 C16Ch**
USB1	**3110 C16Ch**

Figure 14-9550. USB2SS_GBL_GDBGBMU Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BMU_BCU</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BMU_BCU</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BMU_BCU</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">BMU_DCU</td><td colspan="4">BMU_CCU</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28817. USB2SS_GBL_GDBGBMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	BMU_BCU	R	0h	BMU_BCU Debug information Reset Source: rst_mod_g_rst_n
7:4	BMU_DCU	R	0h	BMU_DCU Debug information Reset Source: rst_mod_g_rst_n
3:0	BMU_CCU	R	0h	BMU_CCU Debug information Reset Source: rst_mod_g_rst_n

14.9.3.2.2.322 USB2SS_GBL_GDBGLSPMUX_HST Register

1 USB2SS_GBL_GDBGLSPMUX_HST Register (Offset = 70h) [reset = 3F0000h]

Global Debug LSP MUX Register - Host This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-28818. Instance Table

Instance Name	Physical Address
USB0	**3100 C170h**
USB1	**3110 C170h**

Figure 14-9551. USB2SS_GBL_GDBGLSPMUX_HST Name Register

31	30	29	28	27	26	25	24
RESERVED_31_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOGIC_ANALYZER_TRACE							
R/W							
3Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15_14		HOSTSELECT					
R		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOSTSELECT							
R/W							
0h							

Table 14-28820. USB2SS_GBL_GDBGLSPMUX_HST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_31_24	R	0h	Reserved
23:16	LOGIC_ANALYZER_TRACE	R/W	3Fh	logic_analyzer_trace Port MUX Select Currently only bits[21:16] are used. For details on how the mux controls the debug traces, refer to the "assign logic_analyzer_trace =" code section in the DWC_usb3.v file. A value of 6'h3F drives 0s on the logic_analyzer_trace signal. If you plan to OR [instead using a mux] this signal with other trace signals in your system to generate a common trace signal, you can use this feature. Reset Source: rst_mod_g_rst_n
15:14	RESERVED_15_14	R	0h	Reserved
13:0	HOSTSELECT	R/W	0h	Device LSP Select Selects the LSP debug information presented in the GDBGLSP register in host mode. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.323 USB2SS_GBL_GDBGLSP Register

1 USB2SS_GBL_GDBGLSP Register (Offset = 74h) [reset = 0h]

Global Debug LSP Register This register is for internal debug purposes only. This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-28821. Instance Table

Instance Name	Physical Address
USB0	**3100 C174h**
USB1	**3110 C174h**

Figure 14-9552. USB2SS_GBL_GDBGLSP Name Register

31	30	29	28	27	26	25	24
LSPDEBUG							
R							
0h							
23	22	21	20	19	18	17	16
LSPDEBUG							
R							
0h							
15	14	13	12	11	10	9	8
LSPDEBUG							
R							
0h							
7	6	5	4	3	2	1	0
LSPDEBUG							
R							
0h							

Table 14-28823. USB2SS_GBL_GDBGLSP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LSPDEBUG	R	0h	LSP Debug Information Reset Source: rst_mod_g_rst_n

14.9.3.2.2.324 USB2SS_GBL_GDBGEPINFO0 Register

1 USB2SS_GBL_GDBGEPINFO0 Register (Offset = 78h) [reset = 0h]

Global Debug Endpoint Information Register 0 This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-28824. Instance Table

Instance Name	Physical Address
USB0	**3100 C178h**
USB1	**3110 C178h**

Figure 14-9553. USB2SS_GBL_GDBGEPINFO0 Name Register

31	30	29	28	27	26	25	24
EPDEBUG							
R							
0h							
23	22	21	20	19	18	17	16
EPDEBUG							
R							
0h							
15	14	13	12	11	10	9	8
EPDEBUG							
R							
0h							
7	6	5	4	3	2	1	0
EPDEBUG							
R							
0h							

Table 14-28826. USB2SS_GBL_GDBGEPINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPDEBUG	R	0h	Endpoint Debug Information, bits[31:0] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.325 USB2SS_GBL_GDBGEPINFO1 Register

1 USB2SS_GBL_GDBGEPINFO1 Register (Offset = 7Ch) [reset = 800000h]

Global Debug Endpoint Information Register 1 This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-28827. Instance Table

Instance Name	Physical Address
USB0	**3100 C17Ch**
USB1	**3110 C17Ch**

Figure 14-9554. USB2SS_GBL_GDBGEPINFO1 Name Register

31	30	29	28	27	26	25	24
EPDEBUG							
R							
800000h							
23	22	21	20	19	18	17	16
EPDEBUG							
R							
800000h							
15	14	13	12	11	10	9	8
EPDEBUG							
R							
800000h							
7	6	5	4	3	2	1	0
EPDEBUG							
R							
800000h							

Table 14-28829. USB2SS_GBL_GDBGEPINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPDEBUG	R	800000h	Endpoint Debug Information, bits[63:32] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.326 USB2SS_GBL_GPRTBIMAP_HSLO Register

1 USB2SS_GBL_GPRTBIMAP_HSLO Register (Offset = 80h) [reset = 0h]

Global High-Speed Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP_HS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_HS register.

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Table 14-28830. Instance Table

Instance Name	Physical Address
USB0	**3100 C180h**
USB1	**3110 C180h**

Figure 14-9555. USB2SS_GBL_GPRTBIMAP_HSLO Name Register

31	30	29	28	27	26	25	24
BINUM8				BINUM7			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM6				BINUM5			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM4				BINUM3			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM2				BINUM1			
R				R/W			
0h				0h			

Table 14-28832. USB2SS_GBL_GPRTBIMAP_HSLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: HS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: HS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6 USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM5	R	0h	BINUM5: HS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM4	R	0h	BINUM4: HS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-28832. USB2SS_GBL_GPRTBIMAP_HSLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	BINUM3	R	0h	BINUM3: HS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM2	R	0h	BINUM2: HS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: HS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.327 USB2SS_GBL_GPRTBIMAP_HSHI Register

1 USB2SS_GBL_GPRTBIMAP_HSHI Register (Offset = 84h) [reset = 0h]

Global High-Speed Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP_HS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-28833. Instance Table

Instance Name	Physical Address
USB0	**3100 C184h**
USB1	**3110 C184h**

Figure 14-9556. USB2SS_GBL_GPRTBIMAP_HSHI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED_31_28</td><td colspan="4">BINUM15</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BINUM14</td><td colspan="4">BINUM13</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BINUM12</td><td colspan="4">BINUM11</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">BINUM10</td><td colspan="4">BINUM9</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28835. USB2SS_GBL_GPRTBIMAP_HSHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: HS USB Instance Number for Port 15. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: HS USB Instance Number for Port 14. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: HS USB Instance Number for Port 13. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: HS USB Instance Number for Port 12. SApplication-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM11	R	0h	BINUM11: HS USB Instance Number for 11. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-28835. USB2SS_GBL_GPRTBIMAP_HSHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	BINUM10	R	0h	BINUM10: HS USB Instance Number for Port 10. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM9	R	0h	BINUM9: HS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.328 USB2SS_GBL_GPRTBIMAP_FSLO Register

1 USB2SS_GBL_GPRTBIMAP_FSLO Register (Offset = 88h) [reset = 0h]

Global Full-Speed Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP_FS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_FS register.

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Table 14-28836. Instance Table

Instance Name	Physical Address
USB0	**3100 C188h**
USB1	**3110 C188h**

Figure 14-9557. USB2SS_GBL_GPRTBIMAP_FSLO Name Register

31	30	29	28	27	26	25	24
BINUM8				BINUM7			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BINUM6				BINUM5			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BINUM4				BINUM3			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BINUM2				BINUM1			
R				R/W			
0h				0h			

Table 14-28838. USB2SS_GBL_GPRTBIMAP_FSLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: FS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: FS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6: FS USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM5	R	0h	BINUM5: FS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM4	R	0h	BINUM4: FS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-28838. USB2SS_GBL_GPRTBIMAP_FSLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	BINUM3	R	0h	BINUM3: FS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM2	R	0h	BINUM2: FS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: FS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.329 USB2SS_GBL_GPRTBIMAP_FSHI Register

1 USB2SS_GBL_GPRTBIMAP_FSHI Register (Offset = 8Ch) [reset = 0h]

Global Full-Speed Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP_FS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_FS register.

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Table 14-28839. Instance Table

Instance Name	Physical Address
USB0	**3100 C18Ch**
USB1	**3110 C18Ch**

Figure 14-9558. USB2SS_GBL_GPRTBIMAP_FSHI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_28				BINUM15			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM14				BINUM13			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM12				BINUM11			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM10				BINUM9			
R				R			
0h				0h			

Table 14-28841. USB2SS_GBL_GPRTBIMAP_FSHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: FS USB Instance Number for Port 15. Application-programmable ID field Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: FS USB Instance Number for Port 14. Application-programmable ID field Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: FS USB Instance Number for Port 13. Application-programmable ID field Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: FS USB Instance Number for Port 12. Application-programmable ID field Reset Source: rst_mod_g_rst_n
11:8	BINUM11	R	0h	BINUM11: FS USB Instance Number for Port 11. Application-programmable ID field Reset Source: rst_mod_g_rst_n

Table 14-28841. USB2SS_GBL_GPRTBIMAP_FSHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	BINUM10	R	0h	BINUM10: FS USB Instance Number for Port 10. Application-programmable ID field Reset Source: rst_mod_g_rst_n
3:0	BINUM9	R	0h	BINUM9: FS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.330 USB2SS_GBL_RESERVED_94 Register

1 USB2SS_GBL_RESERVED_94 Register (Offset = 94h) [reset = 0h]

Future Reserved Register at offset 0x94

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Table 14-28842. Instance Table

Instance Name	Physical Address
USB0	**3100 C194h**
USB1	**3110 C194h**

Figure 14-9559. USB2SS_GBL_RESERVED_94 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28844. USB2SS_GBL_RESERVED_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Future use Register field

14.9.3.2.2.331 USB2SS_GBL_RESERVED_98 Register

1 USB2SS_GBL_RESERVED_98 Register (Offset = 98h) [reset = 0h]

Future Reserved Register at offset 0x98

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Table 14-28845. Instance Table

Instance Name	Physical Address
USB0	**3100 C198h**
USB1	**3110 C198h**

Figure 14-9560. USB2SS_GBL_RESERVED_98 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28847. USB2SS_GBL_RESERVED_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Field for future use

14.9.3.2.2.332 USB2SS_GBL_GUCTL2 Register

1 USB2SS_GBL_GUCTL2 Register (Offset = 9Ch) [reset = 0h]

Global User Control Register 2: This register provides a few options for the software to control the controller behavior in the Host and device mode. Most of the options are used to improve inter-operability with different hosts and devices.

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Table 14-28848. Instance Table

Instance Name	Physical Address
USB0	**3100 C19Ch**
USB1	**3110 C19Ch**

Figure 14-9561. USB2SS_GBL_GUCTL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_26						EN_HP_PM_TIMER	
R/W						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EN_HP_PM_TIMER					NOLOWPWRDUR		
R/W					R/W		
0h					0h		
15	14	13	12	11	10	9	8
NOLOWPWRDUR	RST_ACTBITLATER	RESERVED_13	ENABLEEPCACHEEVICT	DISABLECFC	RXPINGDURATION		
R/W	R/W	R	R/W	R/W	R/W		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
RXPINGDURATION			TXPINGDURATION				
R/W			R/W				
0h			0h				

Table 14-28850. USB2SS_GBL_GUCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED_31_26	R/W	0h	Reserved
25:19	EN_HP_PM_TIMER	R/W	0h	This register field is used to set new HP and PM timers. - To enable PM timer, set GUCTL2[19] bit as 1. - To enable HP timer, set GUCTL2[20] bit as 1. Default value of HP timer is 4us when HP PM timer is not enabled. when new HP timer is enabled default value is 12us. Use GUCTL2[25:21] to specify HP timer value in microseconds. Reset Source: rst_mod_g_rst_n

Table 14-28850. USB2SS_GBL_GUCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:15	NOLOWPWRDUR	R/W	0h	No Low Power Duration [NOLOWPWRDUR] This bit is applicable for device mode only and is ignored in host mode. After starting a transfer on a SS ISOC endpoint, the application must program these bits to prevent the device to lose frame synchronization over a period of time. Based on this count-down counter, the device will wake itself from U1/U2 low power states. After entering to U0 state and receiving two ITPs [which will sync-up the host and the device], U1/U2 low power entry is allowed. Each count represents the duration in terms of milliseconds. For example, a value of 3 represents 3ms. Note: - To disable this feature, set this field to 4'b0. - These bits are applicable only in device mode and ignored in host mode. - Some xHCI hosts do not send ITPs when performing ISOC transfers when the link enters U1/U2 low power states. This causes the device to lose frame synchronization over a period of time resulting in ISOC packets being dropped. Reset Source: rst_mod_g_rst_n
14	RST_ACTBITLATER	R/W	0h	Enable clearing of the command active bit for the ENDXFER command after the command execution is completed. This bit is valid in device mode only. Reset Source: rst_mod_g_rst_n
13	RESERVED_13	R	0h	Reserved for future use
12	ENABLEEPCACHEEVICT	R/W	0h	Enable Evicting Endpoint cache after Flow Control for bulk endpoints. In 3.00a release, a performance enhancement was done to keep the non-stream capable bulk IN endpoint in cache after flow control. Setting this bit will disable this enhancement. This should be set only for debug purpose. Reset Source: rst_mod_g_rst_n
11	DISABLECFC	R/W	0h	Disable xHCI Errata Feature Contiguous Frame ID Capability This field controls the xHCI Errata feature Contiguous FrameID capability. When set, the xHCI HCCPARAMS1 bit 11 will be set to 0 indicating that CFC is not supported. Disable this feature only if your application cannot tolerate Misssed Service Error events for Isoc transfers, and your system latencies are large to cause Missed Service errors even if the software is following the Isochronous Thresholding rules. Reset Source: rst_mod_g_rst_n
10:5	RXPINGDURATION	R/W	0h	Recieve Ping Maximum Duration This field is relevant to Host mode and controls the maximum duration of received LFPS to be treated as a Ping LFPS. The Max duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 32 indicates 256 ns. Reset Source: rst_mod_g_rst_n
4:0	TXPINGDURATION	R/W	0h	Transmit Ping Maximum Duration This field is relevant to Device mode and controls the maximum duration for which the controller should instruct the PHY to transmit a Ping LFPS. The duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 13 indicates 104 ns. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.333 USB2SS_GBL_GHWPARAMS8 Register

1 USB2SS_GBL_GHWPARAMS8 Register (Offset = 500h) [reset = 660h]

Global Hardware Parameters Register 8 This register contains the hardware configuration options that you can select in the coreConsultant GUI. For a description of each parameter, refer to the "Parameter Descriptions" chapter in the Databook. This information is also available in coreConsultant by right-clicking the parameter label and selecting "What's This" or by clicking the Help tab. Note: Some of the global hardware parameters are not currently modifiable in coreConsultant. These settings are in the <workspace>/src/DWC_usb3_params.v file. you must not change them.

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Table 14-28851. Instance Table

Instance Name	Physical Address
USB0	**3100 C600h**
USB1	**3110 C600h**

Figure 14-9562. USB2SS_GBL_GHWPARAMS8 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS8_32_0							
R							
660h							
23	22	21	20	19	18	17	16
GHWPARAMS8_32_0							
R							
660h							
15	14	13	12	11	10	9	8
GHWPARAMS8_32_0							
R							
660h							
7	6	5	4	3	2	1	0
GHWPARAMS8_32_0							
R							
660h							

Table 14-28853. USB2SS_GBL_GHWPARAMS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GHWPARAMS8_32_0	R	660h	DWC_USB3_DCACHE_DEPTH_INFO Reset Source: rst_mod_g_rst_n

14.9.3.2.2.334 USB2SS_GBL_GUCTL3 Register

1 USB2SS_GBL_GUCTL3 Register (Offset = 50Ch) [reset = 0h]

Global User Control Register 3 This register provides a few options for the software to control the controller behavior in the Host mode. Most of the options are used to improve host inter-operability with different devices.

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Table 14-28854. Instance Table

Instance Name	Physical Address
USB0	**3100 C60Ch**
USB1	**3110 C60Ch**

Figure 14-9563. USB2SS_GBL_GUCTL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_17							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_17							SCH_PING_EARLY
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED_15_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_15_0							
R/W							
0h							

Table 14-28856. USB2SS_GBL_GUCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R/W	0h	Reserved
16	SCH_PING_EARLY	R/W	0h	Enable SuperSpeed Ping Transaction Packet scheduling early in the microframe. This bit is valid in Host mode only. Reset Source: rst_mod_g_rst_n
15:0	RESERVED_15_0	R/W	0h	Reserved

14.9.3.2.2.335 USB2SS_GBL_GTXFIFOPRIDEV Register

1 USB2SS_GBL_GTXFIFOPRIDEV Register (Offset = 510h) [reset = 0h]

Global Device TX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: - 1. High-priority TXFIFOs are granted access using round-robin arbitration - 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the controller is configured to operate in the device mode (includes DRD mode). The register size corresponds to the number of Device IN endpoints. Note - Since the device mode uses only one RXFIFO, there is no Device RXFIFO DMA Priority Register.

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Table 14-28857. Instance Table

Instance Name	Physical Address
USB0	**3100 C610h**
USB1	**3110 C610h**

Figure 14-9564. USB2SS_GBL_GTXFIFOPRIDEV Name Register

31	30	29	28	27	26	25	24
RESERVED_31_N							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_N							
R							
0h							
15	14	13	12	11	10	9	8
GTXFIFOPRIDEV							
R/W							
0h							
7	6	5	4	3	2	1	0
GTXFIFOPRIDEV							
R/W							
0h							

Table 14-28859. USB2SS_GBL_GTXFIFOPRIDEV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_N	R	0h	Reserved
15:0	GTXFIFOPRIDEV	R/W	0h	Device TxFIFO priority Reset Source: rst_mod_g_rst_n

14.9.3.2.2.336 USB2SS_GBL_GTXFIFOPRIHST Register

1 USB2SS_GBL_GTXFIFOPRIHST Register (Offset = 518h) [reset = 0h]

Global Host TX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: - 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). - 2. The TX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD mode). The register size corresponds to the number of configured USB bus instances. for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

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Table 14-28860. Instance Table

Instance Name	Physical Address
USB0	**3100 C618h**
USB1	**3110 C618h**

Figure 14-9565. USB2SS_GBL_GTXFIFOPRIHST Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_31_16							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_31_16					GTXFIFOPRIHST		
R					R/W		
0h					0h		

Table 14-28862. USB2SS_GBL_GTXFIFOPRIHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_31_16	R	0h	Reserved
2:0	GTXFIFOPRIHST	R/W	0h	Host TxFIFO priority Reset Source: rst_mod_g_rst_n

14.9.3.2.2.337 USB2SS_GBL_GRXFIFOPRIHST Register

1 USB2SS_GBL_GRXFIFOPRIHST Register (Offset = 51Ch) [reset = 0h]

Global Host RX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: - 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). - 2. The RX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD mode). The register size corresponds to the number of configured USB bus instances. for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

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Table 14-28863. Instance Table

Instance Name	Physical Address
USB0	**3100 C61Ch**
USB1	**3110 C61Ch**

Figure 14-9566. USB2SS_GBL_GRXFIFOPRIHST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED_31_16</td><td colspan="3">GRXFIFOPRIHST</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-28865. USB2SS_GBL_GRXFIFOPRIHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_31_16	R	0h	Reserved
2:0	GRXFIFOPRIHST	R/W	0h	Host RxFIFO priority Reset Source: rst_mod_g_rst_n

14.9.3.2.2.338 USB2SS_GBL_GDMAHLRATIO Register

1 USB2SS_GBL_GDMAHLRATIO Register (Offset = 524h) [reset = 0h]

Global Host FIFO DMA High-Low Priority Ratio Register This register specifies the relative priority of the SS FIFOs with respect to the HS/FSLS FIFOs. The DMA arbiter prioritizes the HS/FSLS round-robin arbiter group every DMA High-Low Priority Ratio grants as indicated in the register separately for TX and RX. To illustrate, consider that all FIFOs are requesting access simultaneously, and the ratio is 4. SS gets priority for 4 packets, HS/FSLS gets priority for 1 packet, SS gets priority for 4 packets, HS/FSLS gets priority for 1 packet, and so on. If FIFOs from both speed groups are not requesting access simultaneously then, - if SS got grants 4 out of the last 4 times, then HS/FSLS get the priority on any future request. - if HS/FSLS got the grant last time, SS gets the priority on the next request. - if there is a valid request on either SS or HS/FSLS, a grant is always awarded. there is no idle. This register is present if the controller is configured to operate in host mode (includes DRD).

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Table 14-28866. Instance Table

Instance Name	Physical Address
USB0	3100 C624h
USB1	3110 C624h

Figure 14-9567. USB2SS_GBL_GDMAHLRATIO Name Register

31	30	29	28	27	26	25	24
RESERVED_31_13							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_13							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_31_13			HSTRXFIFO				
R			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_7_5			HSTTXFIFO				
R			R/W				
0h			0h				

Table 14-28868. USB2SS_GBL_GDMAHLRATIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12:8	HSTRXFIFO	R/W	0h	Host RXFIFO DMA High-Low Priority Reset Source: rst_mod_g_rst_n
7:5	RESERVED_7_5	R	0h	Reserved
4:0	HSTTXFIFO	R/W	0h	Host TXFIFO DMA High-Low Priority Reset Source: rst_mod_g_rst_n

14.9.3.2.2.339 USB2SS_GBL_GFLADJ Register

1 USB2SS_GBL_GFLADJ Register (Offset = 530h) [reset = 0h]

Global Frame Length Adjustment Register This register provides options for the software to control the controller behavior with respect to SOF (Start of Frame) and ITP (Isochronous Timestamp Packet) timers and frame timer functionality. It provides an option to override the fladj_30mhz_reg sideband signal. In addition, it enables running SOF or ITP frame timer counters completely from the ref_clk. This facilitates hardware LPM in host mode with the SOF or ITP counters being run from the ref_clk signal.

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Table 14-28869. Instance Table

Instance Name	Physical Address
USB0	**3100 C630h**
USB1	**3110 C630h**

Figure 14-9568. USB2SS_GBL_GFLADJ Name Register

31	30	29	28	27	26	25	24
GFLADJ_REFCLK_240MHZDECR_PLS1	GFLADJ_REFCLK_240MHZ_DECR						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
GFLADJ_REFCLK_LPM_SEL	RESERVED_22	GFLADJ_REFCLK_FLADJ					
R/W	R	R/W					
0h	0h	0h					
15	14	13	12	11	10	9	8
GFLADJ_REFCLK_FLADJ							
R/W							
0h							
7	6	5	4	3	2	1	0
GFLADJ_30MHZ_SDBND_SEL	RESERVED_6	GFLADJ_30MHZ					
R/W	R	R/W					
0h	0h	0h					

Table 14-28871. USB2SS_GBL_GFLADJ Register Field Descriptions

Bit	Field	Type	Reset	Description

31	GFLADJ_REFCLK_240MHZDECR_PLS1	R/W	0h	GFLADJ_REFCLK_240MHZDECR_PLS1
				This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk.
				Set this bit to a '1' only if GFLADJ_REFCLK_LPM_SEL is set to '1' and the fractional component of 240/ref_frequency is greater than or equal to 0.5.
				Examples:
				If the ref_clk is 19.2 MHz then
				- GUCTL.REF_CLK_PERIOD = 52
				- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = [240/19.2] = 12.5
				- GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 1
				If the ref_clk is 24 MHz then
				- GUCTL.REF_CLK_PERIOD = 41
				- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = [240/24] = 10
				- GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0
				Reset Source: rst_mod_g_rst_n

30:24	GFLADJ_REFCLK_240MHZ_DECR	R/W	0h	This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock.
				This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to '1'.
				The value is derived as follows:
				GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency
				Examples:
				If the ref_clk is 24 MHz then
				- GUCTL.REF_CLK_PERIOD = 41
				- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10
				If the ref_clk is 48 MHz then
				- GUCTL.REF_CLK_PERIOD = 20
				- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/48 = 5
				If the ref_clk is 17 MHz then
				- GUCTL.REF_CLK_PERIOD = 58
				- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/17 = 14
				Reset Source: rst_mod_g_rst_n

23	GFLADJ_REFCLK_LPM_SEL	R/W	0h	This bit enables the functionality of running SOF/ITP counters on the ref_clk. This bit must not be set to '1' if GCTL.SOFITPSYNC bit is set to '1'. Similarly, if GFLADJ_REFCLK_LPM_SEL set to '1', GCTL.SOFITPSYNC must not be set to '1'. In device mode, setting this bit to '1' enables SOF tracking using ref_clk. When GFLADJ_REFCLK_LPM_SEL is set to '1' the overloading of the suspend control of the USB 2.0 first port PHY [UTMI/ULPI] with USB 3.0 port states is removed. For example, for Synopsys PHY, the COMMONONN signal can be tied to '1'. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the controller must be connected to the FREECLK of the PHY. Note: If you set this bit to '1', the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to '0'. Reset Source: rst_mod_g_rst_n
22	RESERVED_22	R	0h	Reserved for future use

Table 14-28871. USB2SS_GBL_GFLADJ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

21:8	GFLADJ_REFCLK_FLADJ	R/W	0h	This field indicates the frame length adjustment to be applied when SOF/ITP counter is running on the ref_clk.
				This register value is used to adjust the ITP interval when GCTL[SOFITPSYNC] is set to '1'. SOF and ITP interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to '1'.
				This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to '1' or GCTL.SOFITPSYNC is set to '1'.
				The value is derived as follows:
				FLADJ_REF_CLK_FLADJ=[[125000/ ref_clk_period_integer]-[125000/ref_clk_period]] * ref_clk_period
				where
				- the ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal [fractional] value that is programmed in the GUCTL.REF_CLK_PERIOD field.
				- the ref_clk_period is the ref_clk period including the fractional value.
				Examples:
				If the ref_clk is 24 MHz then
				- GUCTL.REF_CLK_PERIOD = 41
				- GFLADJ.GLADJ_REFCLK_FLADJ = [[125000/41]-[125000/41.6666]]*41.6666 = 2032 [ignoring the fractional value]
				If the ref_clk is 48 MHz then
				- GUCTL.REF_CLK_PERIOD = 20
				- GFLADJ.GLADJ_REFCLK_FLADJ = [[125000/20]-[125000/20.8333]]*20.8333 = 5208 [ignoring the fractional value]
				Reset Source: rst_mod_g_rst_n

7	GFLADJ_30MHZ_SDBND_SEL	R/W	0h	GFLADJ_30MHZ_SDBND_SEL This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF/ITP. When this bit is set to, - 1, the controller uses the register field GFLADJ.GFLADJ_30MHZ value - 0, the controller uses the input signal fladj_30mhz_reg value Reset Source: rst_mod_g_rst_n
6	RESERVED_6	R	0h	Reserved for future use
5:0	GFLADJ_30MHZ	R/W	0h	GFLADJ_30MHZ This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register [FLADJ]," of the xHCI Specification. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.340 USB2SS_GBL_GPHY_GUSB2PHYCFG Register

1 USB2SS_GBL_GPHY_GUSB2PHYCFG Register (Offset = 0h) [reset = 102400h]

Global USB2 PHY Configuration Register The application must program this register before starting any transactions on either the SoC bus or the USB. In Device-only configurations, only one register is needed. In Host mode, per-port registers are implemented.

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Table 14-28872. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9569. USB2SS_GBL_GPHY_GUSB2PHYCFG Name Register

31	30	29	28	27	26	25	24
PHYSOFTRST	U2_FREECLK_EXISTS	ULPI_LPM_WITH_OPMODE_CHK	HSIC_CON_WIDTH_ADJ		INV_SEL_HSIC	OVRD_FSLS_DISC_TIME	LSTRD
R/W	R/W	R/W	R		R	R/W	R/W
0h	0h	0h	0h		0h	0h	0h
23	22	21	20	19	18	17	16
LSTRD		LSIPD			ULPIEXTVBUSINDIACTOR	ULPIEXTVBUSDRV	RESERVED_16
R/W		R/W			R/W	R/W	R
0h		2h			0h	0h	0h
15	14	13	12	11	10	9	8
ULPIAUTORES	RESERVED_14	USBTRDTIM				XCVRDLY	ENBLSLPM
R/W	R	R/W				R/W	R/W
0h	0h	9h				0h	0h
7	6	5	4	3	2	1	0
PHYSEL	SUSPENDUSB20	FSINTF	ULPI_UTMI_SEL	PHYIF	TOUTCAL		
W	R/W	R	R	R/W	R/W		
0h	0h	0h	0h	0h	0h		

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHYSOFTRST	R/W	0h	UTMI PHY Soft Reset [PHYSoftRst] Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl.Reset register, and the controller automatically writes to this register when the controller is reset [vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset] Reset Source: rst_mod_g_rst_n

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	U2_FREECLK_EXISTS	R/W	0h	U2_FREECLK_EXISTS Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The controller uses the Port-0 clock for generating the internal mac2 clock. - 1'b0: USB 2.0 free clock does not exist - 1'b1: USB 2.0 free clock exists Note: When the controller is configured as device-only [DWC_USB3_MODE = 0], do not set this bit to 1. Reset Source: rst_mod_g_rst_n
29	ULPI_LPM_WITH_OPMODE_CHK	R/W	0h	ULPI_LPM_WITH_OPMODE_CHK Support the LPM over ULPI without NOPID token to the ULPI PHY. If this bit is set, the ULPI PHY is expected to qualify the EXT PID with OPMODE=2'b00 for LPM and not treat it as a NOPID. Check with your PHY vendor about your PHY behavior. This bit is valid only when the DWC_USB3_HSPHY_INTERFACE parameter is 2 or 3. - 1'b0: A NOPID is sent before sending an EXTPID for LPM. - 1'b1: An EXTPID is sent without previously sending a NOPID. Note: This bit is valid only in host mode. This bit should be '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
28:27	HSIC_CON_WIDTH_ADJ	R	0h	HSIC_CON_WIDTH_ADJ This bit is used in the HSIC device mode of operation. By default, the connect duration for the HSIC device controller is thrice the strobe period. You can change this duration to 4, 5, or 6 times the strobe period by setting the value of this field to 1, 2, or 3. This value is added to the default connect duration. Reset Source: rst_mod_g_rst_n
26	INV_SEL_HSIC	R	0h	INV_SEL_HSIC The application driver uses this bit to control the HSIC enable/disable function. When set to '1', this bit overrides and functionally inverts the "if_select_hsic" input signal. If {INV_SEL_HSIC, if_select_hsic} is: - 00: HSIC Capability is disabled. - 01: HSIC Capability is enabled. - 10: HSIC Capability is enabled. - 11: HSIC Capability is disabled. If the controller operates as non-HSIC-capable, it can only connect to non-HSIC-capable PHYs. If it operates as HSIC-capable, it can connect to HSIC-capable PHYs. This bit is reserved if the DWC_USB3_ENABLE_HSIC parameter is set to '0'. When selecting the HSIC feature, set the host side to HSIC mode first, then set the device mode side. If the device side is set to HSIC mode first and if the host does not see a connection in HSIC mode, then you must de-select the device HSIC mode and select it again using the if_select_hsic setting or register bit GUSB2PHYCFGn[26] to ensure that the device can connect to the host. Reset Source: rst_mod_g_rst_n
25	OVRD_FSLS_DISC_TIME	R/W	0h	Overriding the FS/LS disconnect time to 32us. - If this value is 0, the FS/LS disconnect time is set to 2.5us as per the USB specification. - If this value is non-0, the disconnect detection time is set to 32us. Normally, this value is set to 0. However, if the USB 2.0 PHYs introduce noise on the UTMI linestate and cause SE0 glitches longer than 2.5us, then a false disconnect condition may get triggered. To avoid interoperability issues with these PHYs, this bit can be set to 1. Reset Source: rst_mod_g_rst_n

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24:22	LSTRD	R/W	0h	LS Turnaround Time [LSTRDTIM] This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: - 0: 2 bit times - 1: 2.5 bit times - 2: 3 bit times - 3: 3.5 bit times - 4: 4 bit times - 5: 4.5 bit times - 6: 5 bit times - 7: 5.5 bit times Note: - This field is applicable only in Host mode. - For normal operation [to work with most LS devices], set the default value of this field to 3'h0 [2 bit times]. - The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly. - Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay [~1 LS bit time] from the device's delay requirement. Reset Source: rst_mod_g_rst_n
21:19	LSIPD	R/W	2h	LS Inter-Packet Time [LSIPD] This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: - 0: 2 bit times - 1: 2.5 bit times - 2: 3 bit times - 3: 3.5 bit times - 4: 4 bit times - 5: 4.5 bit times - 6: 5 bit times - 7: 5.5 bit times Note: - This field is applicable only in Host mode. - For normal operation [to work with most LS devices], set the default value of this field to 3'h2 [3 bit times]. - The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. - Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay [~1 LS bit time] from the device's delay requirement. Reset Source: rst_mod_g_rst_n
18	ULPIEXTVBUSINDIACTOR	R/W	0h	ULPI External VBUS Indicator [ULPIExtVbusIndicator] Indicates the ULPI PHY VBUS over-current indicator. - 1'b0: PHY uses an internal VBUS valid comparator. - 1'b1: PHY uses an external VBUS valid comparator. Valid only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3 Reset Source: rst_mod_g_rst_n

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	ULPIEXTVBUSDRV	R/W	0h	ULPI External VBUS Drive [ULPIExtVbusDrv] Selects supply source to drive 5V on VBUS, in the ULPI PHY. - 1'b0: PHY drives VBUS with internal charge pump [default]. - 1'b1: PHY drives VBUS with an external supply. [Only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3] Reset Source: rst_mod_g_rst_n
16	RESERVED_16	R	0h	Reserved
15	ULPIAUTORES	R/W	0h	ULPI Auto Resume [ULPIAutoRes] Sets the AutoResume bit in Interface Control register on the ULPI PHY. - 1'b0: PHY does not use the AutoResume feature. - 1'b1: PHY uses the AutoResume feature. Valid only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3 Reset Source: rst_mod_g_rst_n
14	RESERVED_14	R	0h	Reserved
13:10	USBTRDTIM	R/W	9h	USB 2.0 Turnaround Time [USBTrdTim] Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller [PFC] to fetch data from the DFIFO [SPRAM]. The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: - 4'h5: When the MAC interface is 16-bit UTMI+. - 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode. Reset Source: rst_mod_g_rst_n
9	XCVRDLY	R/W	0h	Transceiver Delay: Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal [for HS] and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay [of approximately 2.5 us] is introduced from the time when the Transceiver Select is set to 2'b00 [HS] to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: - If you enable the hibernation feature when the device controller comes out of power-off, you must re-initialize this bit with the appropriate value because the controller does not save and restore this bit value during hibernation. - This bit is valid only in device mode. Reset Source: rst_mod_g_rst_n
8	ENBLSLPM	R/W	0h	Enable utmi_sleep_n and utmi_l1_suspend_n [EnblSlpM] The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. - 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is not transferred to the external PHY. - 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is transferred to the external PHY. Note: This bit must be set high for Port0 if Synopsys PHY is used. Note: In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk [utmi_clk/ulpi_clk] is gated off, the command will not get completed. Reset Source: rst_mod_g_rst_n

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PHYSEL	W	0h	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select a high-speed PHY or a full-speed transceiver. - 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. This bit is always 0, with Write Only access. - 1'b1: USB 1.1 full-speed serial transceiver. This bit is always 1, with Write Only access. If both interface types are selected in coreConsultant [that is, parameters' values are not zero], the application uses this bit to select the active interface is active, with Read-Write bit access. Note: USB 1.1 full-serial transceiver is not supported. This bit always reads as 1'b0. Reset Source: rst_mod_g_rst_n
6	SUSPENDUSB20	R/W	0h	Suspend USB2.0 HS/FS/LS PHY [SusPHY] When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD configurations, it is recommended that this bit is set to 0 during coreConsultant configuration. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the controller initialization completes. For all other configurations, this bit can be set to 1 during controller configuration. Note: - In host mode, on reset, this bit is set to 1. Software can override this bit after reset. - In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk [utmi_clk/ulpi_clk] is gated off, the command will not get completed. Reset Source: rst_mod_g_rst_n
5	FSINTF	R	0h	Full-Speed Serial Interface Select [FSIntf] The application uses this bit to select a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. - 1'b0: 6-pin unidirectional full-speed serial interface. This bit is set to 0 with Read Only access. - 1'b1: 3-pin bidirectional full-speed serial interface. This bit is set to 0 with Read Only access. Note: USB 1.1 full-speed serial interface is not supported. This bit always reads as 1'b0. Reset Source: rst_mod_g_rst_n
4	ULPI_UTMI_SEL	R	0h	ULPI or UTMI+ Select [ULPI_UTMI_Sel] The application uses this bit to select a UTMI+ or ULPI Interface. - 1'b0: UTMI+ Interface - 1'b1: ULPI Interface This bit is writable only if UTMI+ and ULPI is specified for High-Speed PHY Interface[s] in coreConsultant configuration [DWC_USB3_HSPHY_INTERFACE = 3]. Otherwise, this bit is read-only and the value depends on the interface selected through DWC_USB3_HSPHY_INTERFACE. Reset Source: rst_mod_g_rst_n

Table 14-28874. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PHYIF	R/W	0h	PHY Interface [PHYIf] If UTMI+ is selected, the application uses this bit to configure the controller to support a UTMI+ PHY with an 8- or 16-bit interface. - 1'b0: 8 bits - 1'b1: 16 bits ULPI Mode: 1'b0 Note: - All the enabled 2.0 ports must have the same clock frequency as Port0 clock frequency [utmi_clk[0]]. - The UTMI 8-bit and 16-bit modes cannot be used together for different ports at the same time [that is, all the ports must be in 8-bit mode, or all of them must be in 16-bit mode, at a time]. - If any of the USB 2.0 ports is selected as ULPI port for operation, then all the USB 2.0 ports must be operating at 60 MHz. Reset Source: rst_mod_g_rst_n
2:0	TOUTCAL	R/W	0h	HS/FS Timeout Calibration [TOutCal] The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor. this factor is added to the high-speed/full-speed interpacket timeout duration in the controller to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 [inclusive] bit times. The USB standard timeout value for full-speed operation is 16 to 18 [inclusive] bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: - One 30-MHz PHY clock = 16 bit times - One 60-MHz PHY clock = 8 bit times Full-speed operation: - One 30-MHz PHY clock = 0.4 bit times - One 60-MHz PHY clock = 0.2 bit times - One 48-MHz PHY clock = 0.25 bit times Reset Source: rst_mod_g_rst_n

14.9.3.2.2.341 USB2SS_GBL_GI2C_GUSB2I2CCTL Register

1 USB2SS_GBL_GI2C_GUSB2I2CCTL Register (Offset = 0h) [reset = 0h]

Reserved Register

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Table 14-28875. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9570. USB2SS_GBL_GI2C_GUSB2I2CCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28877. USB2SS_GBL_GI2C_GUSB2I2CCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved for future use

14.9.3.2.2.342 USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register

1 USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register (Offset = 0h) [reset = 0h]

Global USB 2.0 ULPI PHY Vendor Control Register The application uses this register to access the PHY registers. This register is always implemented when the ULPI PHY Interface is enabled during coreConsultant configuration (parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3). For an ULPI PHY, the controller uses the ULPI interface for PHY register access. The application sets the Vendor Control register for PHY register access and times the PHY register access. The application polls the VStatus Done bit in this register for the completion of the PHY register access. In Device-only configurations, only one register is needed. In Host mode, per-port registers are implemented.

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Table 14-28878. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9571. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_27					DISUIPIDRVR	NEWREGREQ	VSTSDONE
R					R	R	R
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VSTSBSY	REGWR	REGADDR					
R	R	R					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXTREGADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REGDATA							
R							
0h							

Table 14-28880. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED_31_27	R	0h	Reserved
26	DISUIPIDRVR	R	0h	DISUIPIDRVR Reset Source: rst_mod_g_rst_n
25	NEWREGREQ	R	0h	New Register Request The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n [1'b0] on the UTMI interface. Reset Source: rst_mod_g_rst_n
24	VSTSDONE	R	0h	VSTSDONE Reset Source: rst_mod_g_rst_n
23	VSTSBSY	R	0h	VSTSBSY Reset Source: rst_mod_g_rst_n

Table 14-28880. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	REGWR	R	0h	Register Write The application sets this bit for register writes and clears it for register reads. Note: This bit is applicable for ULPI register read/write access only. Reset Source: rst_mod_g_rst_n
21:16	REGADDR	R	0h	Register Address The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. Note: These bits are applicable for ULPI only. Reset Source: rst_mod_g_rst_n
15:8	EXTREGADDR	R	0h	EXTREGADDR Reset Source: rst_mod_g_rst_n
7:0	REGDATA	R	0h	REGDATA Reset Source: rst_mod_g_rst_n

14.9.3.2.2.343 USB2SS_GBL_GPIPE_GUSB3PIPECTL Register

1 USB2SS_GBL_GPIPE_GUSB3PIPECTL Register (Offset = 0h) [reset = 10C8002h]

Global USB 3.0 PIPE Control Register The application uses this register to configure the USB3 PHY and PIPE interface. Device-only configuration requires only one register. In Host mode, registers are implemented for each port. For more details on GUSB3PIPECTL(#n) bits, refer to section "GUSB3PIPECTLn Register" in the User Guide. Note: - GUSB3PIPECTLn registers are not applicable for USB 2.0-only mode.

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Table 14-28881. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9572. USB2SS_GBL_GPIPE_GUSB3PIPECTL Name Register

31	30	29	28	27	26	25	24
PHYSOFTRST	HSTPRTCMPL	U2P3OK	DISRXDETP3	UX_EXIT_IN_PX	PING_ENHANCEMENT_EN	U1U2EXITFAIL_TO_RECOV	REQUEST_P1P2P3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h
23	22	21	20	19	18	17	16
STARTRXDETU3RXDET	DISRXDETU3RXDET	DELAYP1P2P3			DELAYP1TRANS	SUSPENDENABLE	DATWIDTH
W	R/W	R/W			R/W	R/W	R
0h	0h	1h			1h	0h	1h
15	14	13	12	11	10	9	8
DATWIDTH	ABORTRXDETINU2	SKIPRXDET	LFPSP0ALGN	P3P2TRANOK	P3EXSIGP2	LFPSFILTER	RX_DETECT_TO_POLLING_LFPS_CONTROL
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SSICEN	TX_SWING	TX_MARGIN			SS_TX_DE_EMPHASIS		ELASTIC_BUFFER_MODE
R/W	R/W	R/W			R/W		R/W
0h	0h	0h			1h		0h

Table 14-28883. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHYSOFTRST	R/W	0h	USB3 PHY Soft Reset After setting this bit to '1', the software needs to clear this bit. For more information, refer to Figure "Software Resets and PHY Clock Sequencing and Requirements" in the Databook. Reset Source: rst_mod_g_rst_n

Table 14-28883. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	HSTPRTCMPL	R/W	0h	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: - 1. Disconnect any plugged in devices. - 2. Perform USBCMD.HCRST or power-on-chip reset. - 3. Set PORTSC.PLS=0xA. - 4. Set PORTSC.PP=0. - 5. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence [toggle the set GUSB3PIPECTL. HstPrtCmpl]: - 1. Set GUSB3PIPECTL.HstPrtCmpl=0. - 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset. Reset Source: rst_mod_g_rst_n
29	U2P3OK	R/W	0h	P3 OK for SSInactive [SSIP3ok] - 0: During link state SS.Inactive, put PHY in P2 [Default] - 1: During link state SS.Inactive, put PHY in P3. Reset Source: rst_mod_g_rst_n
28	DISRXDETP3	R/W	0h	Disabled receiver detection in P3 [DisRxDetP3] - 0: If PHY is in P3 and controller needs to perform receiver detection, The controller performs receiver detection in P3. [Default] - 1: If PHY is in P3 and controller needs to perform receiver detection, The controller changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3. Reset Source: rst_mod_g_rst_n
27	UX_EXIT_IN_PX	R/W	0h	Ux Exit in Px [Ux_exit_in_Px] - 0: The controller does U1/U2/U3 exit in PHY power state P0 [default behavior]. - 1: The controller does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
26	PING_ENHANCEMENT_EN	R/W	0h	Ping Enhancement Enable [ping_enhancement_en] When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns [one mac3_clk]. This field is valid for the downstream port only. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
25	U1U2EXITFAIL_TO_RECOV	R/W	0h	U1U2exitfail to Recovery [u1u2exitfail_to_recov] When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake. Reset Source: rst_mod_g_rst_n

Table 14-28883. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	REQUEST_P1P2P3	R/W	1h	Always Request P1/P2/P3 for U1/U2/U3 [request_p1p2p3] When set, the controller always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit [remotely initiated, or locally initiated] happens, the controller does not request P1/P2/P3 power state change. Note: This bit must be set to '1' for Synopsys PHY. For third-party SS PHY, check with your PHY vendor. Reset Source: rst_mod_g_rst_n
23	STARTRXDETU3RXDET	W	0h	Start Receiver Detection in U3/Rx.Detect [StartRxdetU3RxDet] If DWC_USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the controller starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to '0' for Upstream ports. This feature must not be enabled for normal operation. If have to use this feature, contact Synopsys. Reset Source: rst_mod_g_rst_n
22	DISRXDETU3RXDET	R/W	0h	Disable Receiver Detection in U3/Rx.Det When set, the controller does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to "0" for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact Synopsys. Reset Source: rst_mod_g_rst_n
21:19	DELAYP1P2P3	R/W	1h	Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until [DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8] 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality. Reset Source: rst_mod_g_rst_n
18	DELAYP1TRANS	R/W	1h	Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. - 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIdle is 1 and pipe3_RxValid is 0 - 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIdle and pipe3_RxValid. Note: - If you are using Synopsys PHY, contact Synopsys Customer Support for recommendation on setting this bit because it is node dependent. - If you are using a third-party SS PHY, check with your PHY vendor for recommendation on setting this bit. Reset Source: rst_mod_g_rst_n
17	SUSPENDENABLE	R/W	0h	Suspend USB3.0 SS PHY [Suspend_en] When set, and if Suspend conditions are valid, the USB 3.0 PHY enters Suspend mode. For DRD configurations, it is recommended that this bit is set to '0' during coreConsultant configuration. If it is set to '1', then the application must clear this bit after power-on reset. Application needs to set it to '1' after the controller initialization is completed. For all other configurations, this bit can be set to '1' during controller configuration. Reset Source: rst_mod_g_rst_n

Table 14-28883. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	DATWIDTH	R	1h	PIPE Data Width [DatWidth] - 2'b00: 32 bits - 2'b01: 16 bits One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth. The simulation testbench uses the coreConsultant parameter to configure the VIP. These bits in the coreConsultant parameter must match your PHY data width and the pipe3_DataBusWidth port. Note: 8-bit data width is not supported. Reset Source: rst_mod_g_rst_n
14	ABORTRXDETINU2	R/W	0h	Abort Rx Detect in U2 [AbortRxDetInU2] When set and the link state is U2, the controller will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
13	SKIPRXDET	R/W	0h	Skip Rx Detect: When set, the controller skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation. Reset Source: rst_mod_g_rst_n
12	LFPSP0ALGN	R/W	0h	LFPS P0 Align: When set, - The controller deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. - The controller requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with Synopsys PHY. For other USB 3.0 Host, Device, and DRD cores, this bit is not required. Reset Source: rst_mod_g_rst_n
11	P3P2TRANOK	R/W	0h	P3 P2 Transitions OK [P3P2TranOK] When set, the controller transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
10	P3EXSIGP2	R/W	0h	P3 Exit Signal in P2 [P3ExSigP2] When this bit is set, the controller always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-Synopsys PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
9	LFPSFILTER	R/W	0h	LFPS Filter [LFPSFilt] When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted. Reset Source: rst_mod_g_rst_n

Table 14-28883. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RX_DETECT_TO_POLLING_LFPS_CONTROL	R/W	0h	RX_DETECT to Polling.LFPS Control - 1'b0 [Default]: Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. - 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active [VTX-CM-ACPP_ACTIVE <100mv] if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us. Reset Source: rst_mod_g_rst_n
7	SSICEN	R/W	0h	This field is not used. Reset Source: rst_mod_g_rst_n
6	TX_SWING	R/W	0h	Tx Swing [TxSwing] Refer to the PIPE3 specification. Reset Source: rst_mod_g_rst_n
5:3	TX_MARGIN	R/W	0h	Tx Margin[2:0] [TxMargin] Refer to Table 5-3 of the PIPE3 Specification. Reset Source: rst_mod_g_rst_n
2:1	SS_TX_DE_EMPHASIS	R/W	1h	Tx Deemphasis [TxDeemphasis] The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode. [Refer to Table 5-3 of the PIPE3 specification.] Reset Source: rst_mod_g_rst_n
0	ELASTIC_BUFFER_MODE	R/W	0h	Elastic Buffer Mode [ElasticBufferMode] [Refer to Table 5-3 of the PIPE3 specification.] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.344 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register (Offset = 0h) [reset = 593000Ch]

Global Transmit FIFO Size Register This register specifies the RAM start address and depth (both in MDWIDTH-bit words) for each implemented TxFIFO. The number of TxFIFOs depends on the configuration parameters including the number of Device IN Endpoints, number of Host Bus Instances, and presence of Debug Capability. The register default values for each mode are assigned in coreConsultant based on the maximum packet size, number of packets to be buffered, speed of host bus instance, bus latency, and mode of operation (host, device, or, DBC). Upon reset and mode transitions, hardware automatically programs these registers to the default values. Consequently, there is typically no need for the software to modify the pre-defined default values. For the debug capability mode, the currently mapped EP0 IN and EP1 IN TxFIFO numbers can be read from the GFIFOPRIDBC register. For more details on the usage of the GTXFIFOSIZn and GRXFIFOSIZn registers for different modes of operation, refer to "Memory Requirements" chapter in the Databook.

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Table 14-28884. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9573. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
593h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
593h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
Ch							

Table 14-28886. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	593h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	Ch	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.345 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register (Offset = 4h) [reset = 59F0209h]

Register GTXFIFOSIZ 1

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Table 14-28887. Instance Table

Instance Name	Physical Address
USB0	**3100 C104h**
USB1	**3110 C104h**

Figure 14-9574. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
59Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
59Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
209h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
209h							

Table 14-28889. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	59Fh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.9.3.2.2.346 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register (Offset = 8h) [reset = 7A80209h]

Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words.

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Table 14-28890. Instance Table

Instance Name	Physical Address
USB0	**3100 C108h**
USB1	**3110 C108h**

Figure 14-9575. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
7A8h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
7A8h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-28892. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	7A8h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.347 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register (Offset = Ch) [reset = 9B10209h]

Register GTXFIFOSIZ 3

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Table 14-28893. Instance Table

Instance Name	Physical Address
USB0	**3100 C10Ch**
USB1	**3110 C10Ch**

Figure 14-9576. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
9B1h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
9B1h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-28895. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	9B1h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.348 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register (Offset = 10h) [reset = BBA0209h]

Register GTXFIFOSIZ 4

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Table 14-28896. Instance Table

Instance Name	Physical Address
USB0	**3100 C110h**
USB1	**3110 C110h**

Figure 14-9577. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
BBAh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
BBAh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-28898. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	BBAh	TXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.349 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register (Offset = 14h) [reset = DC30209h]

Register GTXFIFOSIZ 5

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Table 14-28899. Instance Table

Instance Name	Physical Address
USB0	**3100 C114h**
USB1	**3110 C114h**

Figure 14-9578. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
DC3h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
DC3h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-28901. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	DC3h	Transmit FIFOn RAM Start Address Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.350 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register (Offset = 18h) [reset = FCC0209h]

Register GTXFIFOSIZ 6

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Table 14-28902. Instance Table

Instance Name	Physical Address
USB0	**3100 C118h**
USB1	**3110 C118h**

Figure 14-9579. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
FCCh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
FCCh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-28904. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	FCCh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.351 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register (Offset = 1Ch) [reset = 11D50209h]

Register GTXFIFOSIZ 7

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Table 14-28905. Instance Table

Instance Name	Physical Address
USB0	**3100 C11Ch**
USB1	**3110 C11Ch**

Figure 14-9580. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
11D5h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
11D5h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
209h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
209h							

Table 14-28907. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	11D5h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.352 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register (Offset = 20h) [reset = 13DE0105h]

Register GTXFIFOSIZ 8

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Table 14-28908. Instance Table

Instance Name	Physical Address
USB0	**3100 C120h**
USB1	**3110 C120h**

Figure 14-9581. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
13DEh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
13DEh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28910. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	13DEh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.353 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register (Offset = 24h) [reset = 14E30105h]

Register GTXFIFOSIZ 9

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Table 14-28911. Instance Table

Instance Name	Physical Address
USB0	**3100 C124h**
USB1	**3110 C124h**

Figure 14-9582. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
14E3h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
14E3h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28913. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	14E3h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.354 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register (Offset = 28h) [reset = 15E80105h]

GTXFIFOSIZ 10

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Table 14-28914. Instance Table

Instance Name	Physical Address
USB0	**3100 C128h**
USB1	**3110 C128h**

Figure 14-9583. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
15E8h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
15E8h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28916. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	15E8h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.355 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register (Offset = 2Ch) [reset = 16ED0105h]

Register GTXFIFOSIZ 11

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Table 14-28917. Instance Table

Instance Name	Physical Address
USB0	**3100 C12Ch**
USB1	**3110 C12Ch**

Figure 14-9584. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
16EDh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
16EDh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28919. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	16EDh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.356 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register (Offset = 30h) [reset = 17F20105h]

GTXFIFOSIZ 12

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Table 14-28920. Instance Table

Instance Name	Physical Address
USB0	**3100 C130h**
USB1	**3110 C130h**

Figure 14-9585. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
17F2h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
17F2h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28922. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	17F2h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.357 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register (Offset = 34h) [reset = 18F70105h]

Register GTXFIFOSIZ 13

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Table 14-28923. Instance Table

Instance Name	Physical Address
USB0	**3100 C134h**
USB1	**3110 C134h**

Figure 14-9586. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
18F7h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
18F7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
105h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
105h							

Table 14-28925. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	18F7h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.9.3.2.2.358 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register (Offset = 38h) [reset = 19FC0105h]

Register GTXFIFOSIZ 14

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Table 14-28926. Instance Table

Instance Name	Physical Address
USB0	**3100 C138h**
USB1	**3110 C138h**

Figure 14-9587. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
19FCh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
19FCh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28928. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	19FCh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.9.3.2.2.359 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register

1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register (Offset = 3Ch) [reset = 1B010105h]

Register GTXFIFOSIZ 15

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Table 14-28929. Instance Table

Instance Name	Physical Address
USB0	**3100 C13Ch**
USB1	**3110 C13Ch**

Figure 14-9588. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
1B01h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
1B01h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-28931. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	1B01h	TXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.9.3.2.2.360 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register

1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register (Offset = 0h) [reset = 38A0209h]

Global Receive FIFO Size Register This register specifies the RAM start address and depth (both in MDWIDTH-bit words) for each implemented RxFIFO. The number of RxFIFOs depends on the configuration parameters including the number of Host Bus Instances and presence of Debug Capability. device mode requires only one RxFIFO. The register default values for each mode are assigned in coreConsultant based on the maximum packet size, number of packets to be buffered, speed of the host bus instance, bus latency, and mode of operation (host, device, or DBC). Upon reset and mode transitions, hardware automatically programs these registers to the default values. Consequently, there is typically no need for the software to modify the pre-defined default values. For the debug capability mode, the currently mapped RxFIFO number can be read from the GFIFOPRIDBC register. For more details on the usage of the GTXFIFOSIZn and GRXFIFOSIZn registers for different modes of operation, refer to "Memory Requirements" chapter in the Databook.

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Table 14-28932. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9589. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Name Register

31	30	29	28	27	26	25	24
RXFSTADDR_N							
R/W							
38Ah							
23	22	21	20	19	18	17	16
RXFSTADDR_N							
R/W							
38Ah							
15	14	13	12	11	10	9	8
RXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
RXFDEP_N							
R/W							
209h							

Table 14-28934. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	38Ah	RxFIFOn RAM Start Address [RxFStAddr_n] This field contains the memory start address for RxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	209h	RxFIFO Depth [RxFDep_n] This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.361 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register

1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register (Offset = 4h) [reset = 5930000h]

Register

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Table 14-28935. Instance Table

Instance Name	Physical Address
USB0	**3100 C104h**
USB1	**3110 C104h**

Figure 14-9590. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Name Register

31	30	29	28	27	26	25	24
RXFSTADDR_N							
R/W							
593h							
23	22	21	20	19	18	17	16
RXFSTADDR_N							
R/W							
593h							
15	14	13	12	11	10	9	8
RXFDEP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
RXFDEP_N							
R/W							
0h							

Table 14-28937. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	593h	RXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	0h	RxFIFO Depth This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.362 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register

1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register (Offset = 8h) [reset = 5930000h]

Register

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Table 14-28938. Instance Table

Instance Name	Physical Address
USB0	**3100 C108h**
USB1	**3110 C108h**

Figure 14-9591. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Name Register

31	30	29	28	27	26	25	24
RXFSTADDR_N							
R/W							
593h							
23	22	21	20	19	18	17	16
RXFSTADDR_N							
R/W							
593h							
15	14	13	12	11	10	9	8
RXFDEP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
RXFDEP_N							
R/W							
0h							

Table 14-28940. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	593h	RAM Start Address This field contains the memory start address for RxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	0h	RxFIFO Depth This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.363 USB2SS_GBL_GEVNT_GEVNTADRLO_j Register

1 USB2SS_GBL_GEVNT_GEVNTADRLO_j Register (Offset = 0h + formula) [reset = 0h]

Global Event Buffer Address (Low) Register This is an alternate register for the GEVNTADRn register.

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Offset = 300h + (j * 10h); where j = 0 to 7d

Table 14-28941. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h + formula**
USB1	**3110 C100h + formula**

Figure 14-9592. USB2SS_GBL_GEVNT_GEVNTADRLO_j Name Register

31	30	29	28	27	26	25	24
EVNTADRLO							
R/W							
0h							
23	22	21	20	19	18	17	16
EVNTADRLO							
R/W							
0h							
15	14	13	12	11	10	9	8
EVNTADRLO							
R/W							
0h							
7	6	5	4	3	2	1	0
EVNTADRLO							
R/W							
0h							

Table 14-28943. USB2SS_GBL_GEVNT_GEVNTADRLO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTADRLO	R/W	0h	Event Buffer Address [EvntAdrLo] Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.364 USB2SS_GBL_GEVNT_GEVNTADRHI_j Register

1 USB2SS_GBL_GEVNT_GEVNTADRHI_j Register (Offset = 4h + formula) [reset = 0h]

Global Event Buffer Address (High) Register This is an alternate register for the GEVNTADRn register.

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Offset = 304h + (j * 10h); where j = 0 to 7d

Table 14-28944. Instance Table

Instance Name	Physical Address
USB0	**3100 C104h + formula**
USB1	**3110 C104h + formula**

Figure 14-9593. USB2SS_GBL_GEVNT_GEVNTADRHI_j Name Register

31	30	29	28	27	26	25	24
EVNTADRHI							
R/W							
0h							
23	22	21	20	19	18	17	16
EVNTADRHI							
R/W							
0h							
15	14	13	12	11	10	9	8
EVNTADRHI							
R/W							
0h							
7	6	5	4	3	2	1	0
EVNTADRHI							
R/W							
0h							

Table 14-28946. USB2SS_GBL_GEVNT_GEVNTADRHI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTADRHI	R/W	0h	Event Buffer Address [EvntAdrHi] Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.365 USB2SS_GBL_GEVNT_GEVNTSIZ_j Register

1 USB2SS_GBL_GEVNT_GEVNTSIZ_j Register (Offset = 8h + formula) [reset = 0h]

Global Event Buffer Size Register This register holds the Event Buffer Size and the Event Interrupt Mask bit. During power-on initialization, software must initialize the size with the number of bytes allocated for the Event Buffer. The Event Interrupt Mask will mask the interrupt, but events are still queued. After configuration, software must preserve the Event Buffer Size value when changing the Event Interrupt Mask.

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Offset = 308h + (j * 10h); where j = 0 to 7d

Table 14-28947. Instance Table

Instance Name	Physical Address
USB0	**3100 C108h + formula**
USB1	**3110 C108h + formula**

Figure 14-9594. USB2SS_GBL_GEVNT_GEVNTSIZ_j Name Register

31	30	29	28	27	26	25	24
EVNTINTRPTMASK	RESERVED_30_16						
R/W	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED_30_16							
R							
0h							
15	14	13	12	11	10	9	8
EVENTSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENTSIZ							
R/W							
0h							

Table 14-28949. USB2SS_GBL_GEVNT_GEVNTSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVNTINTRPTMASK	R/W	0h	Event Interrupt Mask [EvntIntMask]. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued. Reset Source: rst_mod_g_rst_n
30:16	RESERVED_30_16	R	0h	Reserved
15:0	EVENTSIZ	R/W	0h	Event Buffer Size in bytes [EVNTSiz] Holds the size of the Event Buffer in bytes. must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.366 USB2SS_GBL_GEVNT_GEVNTCOUNT_j Register

1 USB2SS_GBL_GEVNT_GEVNTCOUNT_j Register (Offset = Ch + formula) [reset = 0h]

Global Event Buffer Count Register This register holds the number of valid bytes in the Event Buffer. During initialization, software must initialize the count by writing 0 to the Event Count field. Each time the hardware writes a new event to the Event Buffer, it increments this count. Most events are four bytes, but some events may span over multiple four byte entries. Whenever the count is greater than zero and if enabled, conditions for interrupt moderation are satisfied, the hardware raises the corresponding interrupt line (depending on the EvntIntMask bit in the GEVNTSIZn register). On an interrupt, software processes one or more events out of the Event Buffer. Afterwards, software must write the Event Count field with the number of bytes it processed. If Interrupt Moderation is enabled, then software needs to clear EVNT_HANDLER_BUSY bit. Clock crossing delays may result in the continuous assertion of the interrupt after software acknowledges the last event. Therefore, when the interrupt line is asserted, software must read the GEVNTCOUNT register and only process events if the GEVNTCOUNT is greater than 0.

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Offset = 30Ch + (j * 10h); where j = 0 to 7d

Table 14-28950. Instance Table

Instance Name	Physical Address
USB0	**3100 C10Ch + formula**
USB1	**3110 C10Ch + formula**

Figure 14-9595. USB2SS_GBL_GEVNT_GEVNTCOUNT_j Name Register

31	30	29	28	27	26	25	24
EVNT_HANDLER_BUSY	RESERVED_30_16						
R/W	R						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED_30_16							
R							
0h							

15	14	13	12	11	10	9	8
EVNTCOUNT							
R/W							
0h							

7	6	5	4	3	2	1	0
EVNTCOUNT							
R/W							
0h							

Table 14-28952. USB2SS_GBL_GEVNT_GEVNTCOUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVNT_HANDLER_BUSY	R/W	0h	Event Handler Busy Device software event handler busy indication. The controller sets this bit when the interrupt line is asserted due to pending events. Software clears this bit [with 1'b1] when it has finished processing the events [along with updating the EVNTCOUNT in this register]. The controller does not raise the interrupt line for a new event unless this bit is cleared. Note: When Interrupt moderation is disabled [that is, DEVICE_IMODI = 0], this bit is ignored. Reset Source: rst_mod_g_rst_n
30:16	RESERVED_30_16	R	0h	Reserved
15:0	EVNTCOUNT	R/W	0h	Event Count [EVNTCount] When read, returns the number of valid events in the Event Buffer [in bytes]. When written, hardware decrements the count by the value written. When Interrupt moderation is enabled [that is, DEVICE_IMODI!= 0], the interrupt line gets de-asserted when the first write happens on this register to decrement the count. When Interrupt moderation is disabled [that is, DEVICE_IMODI = 0], the Interrupt line continues to get asserted until the event count becomes zero [no-moderation behavior]. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.367 USB2SS_GBL_GRHB_GUSB2RHBCTL Register

1 USB2SS_GBL_GRHB_GUSB2RHBCTL Register (Offset = 0h) [reset = 0h]

Global USB 2.0 Root Hub Control Register The application must program this register before starting any transactions on the USB if a non-default value is desired. In Host mode, per-port registers are implemented.

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Table 14-28953. Instance Table

Instance Name	Physical Address
USB0	**3100 C100h**
USB1	**3110 C100h**

Figure 14-9596. USB2SS_GBL_GRHB_GUSB2RHBCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_4							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_4							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_4				OVRD_L1TIMEOUT			
R				R/W			
0h				0h			

Table 14-28955. USB2SS_GBL_GRHB_GUSB2RHBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_31_4	R	0h	Reserved
3:0	OVRD_L1TIMEOUT	R/W	0h	Overriding the driver programmed L1TIMEOUT value. If this value is 0, the L1 Timeout value is taken from the xHCI PORTHLPMC register. If this value is non-0, then this will override the L1 Timeout value programmed in the xHCI PORTHLPMC register. In that case the actual L1 Timeout would be 2 ^ <OVRD_L1TIMEOUT-1> * 8us. [1=8us, 2=16us, 3=32us etc] Reset Source: rst_mod_g_rst_n

14.9.3.2.2.368 USB2SS_DEV_DCFG Register

1 USB2SS_DEV_DCFG Register (Offset = 0h) [reset = 80800h]

Device Configuration Register. This register configures the controller in Device mode after power-on or after certain control commands or enumeration. Do not make changes to this register after initial programming.

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Table 14-28956. Instance Table

Instance Name	Physical Address
USB0	**3100 C700h**
USB1	**3110 C700h**

Figure 14-9597. USB2SS_DEV_DCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_31_25							RESERVED_24
R							R
0h							0h
23	22	21	20	19	18	17	16
IGNSTRMPP	LPMCAP	NUMP					INTRNUM
R/W	R/W	R/W					R/W
0h	0h	4h					0h
15	14	13	12	11	10	9	8
INTRNUM				RESERVED_10_11		DEVADDR	
R/W				R		R/W	
0h				2h		0h	
7	6	5	4	3	2	1	0
DEVADDR					DEVSPD		
R/W					R/W		
0h					0h		

Table 14-28958. USB2SS_DEV_DCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_31_25	R	0h	Reserved
24	RESERVED_24	R	0h	reserved
23	IGNSTRMPP	R/W	0h	IgnoreStreamPP This bit only affects stream-capable bulk endpoints. When this bit is set to '0' and the controller receives a Data Packet with the Packet Pending [PP] bit set to 0 for OUT endpoints, or it receives an ACK with the NumP field set to 0 and PP set to 0 for IN endpoints, the controller attempts to search for another stream [CStream] to initiate to the host. However, there are two situations where this behavior is not optimal: - When the host is setting PP=0 even though it has not finished the stream, or - When the endpoint on the device is configured with one transfer resource and therefore does not have any other streams to initiate to the host. When this bit is set to '1', the controller ignores the Packet Pending bit for the purposes of stream selection and does not search for another stream when it receives DP[PP=0] or ACK[NumP=0, PP=0]. This can enhance the performance when the device system bus bandwidth is low or the host responds to the controller's ERDY transmission very quickly. Reset Source: rst_mod_g_rst_n

Table 14-28958. USB2SS_DEV_DCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	LPMCAP	R/W	0h	LPM Capable The application uses this bit to control the LPM capabilities of the DWC_usb3 controller. If the controller operates as a non-LPM-capable device, it cannot respond to LPM transactions. - 1'b0: LPM capability is not enabled. - 1'b1: LPM capability is enabled. Reset Source: rst_mod_g_rst_n
21:17	NUMP	R/W	4h	Number of Receive Buffers. This bit indicates the number of receive buffers to be reported in the ACK TP. The DWC_usb3 controller uses this field for non-control endpoints if GRXTHRCFG.UsbRxPktCntSel is set to '0'. The application can program this value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency. For an OUT endpoint, this field controls the number of receive buffers reported in the NumP field of the ACK TP transmitted by the controller. Note: This bit is used in host mode when Debug Capability is enabled. Reset Source: rst_mod_g_rst_n
16:12	INTRNUM	R/W	0h	Interrupt number Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts [see DEVT] are generated. Reset Source: rst_mod_g_rst_n
11:10	RESERVED_10_11	R	2h	Reserved
9:3	DEVADDR	R/W	0h	Device Address. The application must perform the following: - Program this field after every SetAddress request. - Reset this field to zero after USB reset. Reset Source: rst_mod_g_rst_n
2:0	DEVSPD	R/W	0h	Device Speed. Indicates the speed at which the application requires the controller to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the controller is connected. - 3'b100: SuperSpeed [USB 3.0 PHY clock is 125 MHz or 250 MHz] - 3'b000: High-speed [USB 2.0 PHY clock is 30 MHz or 60 MHz] - 3'b001: Full-speed [USB 2.0 PHY clock is 30 MHz or 60 MHz] Reset Source: rst_mod_g_rst_n 0 `HighSpe` 1 `FullSpeed` 4 `SuperSpeed`

14.9.3.2.2.369 USB2SS_DEV_DCTL Register

1 USB2SS_DEV_DCTL Register (Offset = 4h) [reset = F00000h]

Device Control Register Note: When Hibernation is not enabled using GCTL.GblHibernationEn field, - you can write any value to CSS, CRS, L1HibernationEn, and KeepConnect fields - L1HibernationEn, and KeepConnect fields always return 0 when read in this hibernation-disabled state

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Table 14-28959. Instance Table

Instance Name	Physical Address
USB0	**3100 C704h**
USB1	**3110 C704h**

Figure 14-9598. USB2SS_DEV_DCTL Name Register

31	30	29	28	27	26	25	24
RUN_STOP	CSFTRST	RESERVED_29	HIRDTHRES				
R/W	R/W1TS	R	R/W				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
LPM_NYET_THRES				KEEPCONNECT	L1HIBERNATIONEN	CRS	CSS
R/W				W	W	R/W	R/W
Fh				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED_15_13			INITU2ENA	ACCEPTU2ENA	INITU1ENA	ACCEPTU1ENA	ULSTCHNGREQ
R			R/W	R/W	R/W	R/W	W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ULSTCHNGREQ			TSTCTL				RESERVED_0
W			R/W				R
0h			0h				0h

Table 14-28961. USB2SS_DEV_DCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RUN_STOP	R/W	0h	Run/Stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the controller is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: - After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. - The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. - When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. For more details, see "Low Power Operation" section of the Databook. Note: The following is the minimum duration under various conditions for which the soft disconnect [SftDiscon] bit must be set for the USB host to detect a device disconnect: 30ms: - For SuperSpeed, when the device state is Suspended, Idle, Transmit, or Receive. 10ms: - For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended [performing transactions] - For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Supended [performing transactions] To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration. Reset Source: rst_mod_g_rst_n

Table 14-28961. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	CSFTRST	R/W1TS	0h	Core Soft Reset Resets the all clock domains as follows: - This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. - All module state machines [except the SoC Bus Target Unit] are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. - Any transactions on the SoC bus Initiator are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the controller. This is a self-clearing bit. the controller clears this bit after all necessary logic is reset in the controller, which may take several clocks depending on the current state of the controller. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain [synchronization delay]. Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation. Note: Programming this field with random data causes side effect . Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
29	RESERVED_29	R	0h	Reserved1
28:24	HIRDTHRES	R/W	0h	HIRD Threshold [HIRD_Thres] The controller asserts output signals utmi_l1_suspend_n and utmi_sleep_n [see "LPM Interface Signals" table in the Databook] on the basis of this signal: The controller asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: - HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] - HIRD_Thres[4] is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - If the HIRD value is less than HIRD_Thres[3:0] or - HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation. Reset Source: rst_mod_g_rst_n
23:20	LPM_NYET_THRES	R/W	Fh	LPM NYET Threshold When LPM Errata is enabled: Bits [23:20]: LPM NYET Response Threshold [LPM_NYET_thres] Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. - DCFG.LPMCap is 1'b0 - The controller always responds with Timeout [that is, no response]. - DCFG.LPMCap is 1'b1 - The controller responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: - There are no PID or CRC5 errors in both the EXT token and the LPM token [if not true, inactivity results in a timeout ERROR]. - No data is pending in the TxFIFO and RxFIFO is empty [else NYET]. - The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0] Reset Source: rst_mod_g_rst_n

Table 14-28961. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	KEEPCONNECT	W	0h	Keep Connect When '1', this bit enables the save and restore programming model by preventing the controller from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device controller disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ['0'], or if the controller must not disconnect when RunStop is set to 0 ['1']. This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2. Note: If Hibernation is disabled, that is, GCTL[1].GblHibernationEn = 0, this bit is tied to zero. Reset Source: rst_mod_g_rst_n
18	L1HIBERNATIONEN	W	0h	L1HibernationEn When this bit is set along with KeepConnect, the device controller generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The controller does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1. Note: If Hibernation is disabled, that is, GCTL[1].GblHibernationEn = 0, this bit is tied to zero. Reset Source: rst_mod_g_rst_n
17	CRS	R/W	0h	Controller Restore State [CRS] This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
16	CSS	R/W	0h	Controller Save State [CSS] This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
15:13	RESERVED_15_13	R	0h	Reserved
12	INITU2ENA	R/W	0h	Initiate U2 Enable - 1'b0: May not initiate U2 [default] - 1'b1: May initiate U2 On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature[U2_ENABLE], and clears this bit when ClearFeature[U2_ENABLE] is received. If DCTL[11] [AcceptU2Ena] is 0, the link immediately exits U2 state. Reset Source: rst_mod_g_rst_n
11	ACCEPTU2ENA	R/W	0h	Accept U2 Enable - 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set [default] - 1'b1: Controller accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command. Reset Source: rst_mod_g_rst_n

Table 14-28961. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INITU1ENA	R/W	0h	Initiate U1 Enable - 1'b0: May not initiate U1 [default]. - 1'b1: May initiate U1. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature[U1_ENABLE], and clears this bit when ClearFeature[U1_ENABLE] is received. If DCTL[9] [AcceptU1Ena] is 0, the link immediately exits U1 state. Reset Source: rst_mod_g_rst_n
9	ACCEPTU1ENA	R/W	0h	Accept U1 Enable - 1'b0: Controller rejects U1 except when Force_LinkPM_Accept bit is set [default] - 1'b1: Controller accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command. Reset Source: rst_mod_g_rst_n
8:5	ULSTCHNGREQ	W	0h	ULSTCHNGREQ Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the controller. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Refer to the USB 3.0 specification. Alternatively, you can force the local link directly into compliance mode, by resetting the SS link with the RUN/STOP bit set to zero. If you then write '10' to the USB/Link State Change field and '1' to RUN/STOP, the link goes to compliance mode. Once you are in compliance, you may alternately write zero and '10' to this field to advance the compliance pattern. In SS mode: - Value Requested Link State Transition/Action - 0 No Action - 4 SS.Disabled - 5 Rx.Detect - 6 SS.Inactive - 8 U3 exit request - 10 Compliance - Others: Reserved In HS/FS/LS mode: - ValueRequested USB state transition - 8 Remote wakeup request - Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state [DSTS[21:18] is 3 - refer to Table "Fields for Register: DSTS"]. Note: After coming out of hibernation, software must write 8 [Recovery] into this field to confirm exit from the suspended state. Reset Source: rst_mod_g_rst_n

Table 14-28961. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:1	TSTCTL	R/W	0h	Test Control - 4'b000: Test mode disabled - 4'b001: Test_J mode - 4'b010: Test_K mode - 4'b011: Test_SE0_NAK mode - 4'b100: Test_Packet mode - 4'b101: Test_Force_Enable - Others: Reserved Reset Source: rst_mod_g_rst_n
0	RESERVED_0	R	0h	Reserved

14.9.3.2.2.370 USB2SS_DEV_DEVTEN Register

1 USB2SS_DEV_DEVTEN Register (Offset = 8h) [reset = 0h]

Device Event Enable Register This register controls the generation of device-specific events (see "Event Buffer Content for Device-Specific Events (DEVT)" section). If an enable bit is set to 0, the event will not be generated.

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Table 14-28962. Instance Table

Instance Name	Physical Address
USB0	**3100 C708h**
USB1	**3110 C708h**

Figure 14-9599. USB2SS_DEV_DEVTEN Name Register

31	30	29	28	27	26	25	24
RESERVED_31_17							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_17							ECCERREN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15	L1WKUPEVTEN	RESERVED	VENDEVTSTRCVDEN	RESERVED_11	RESERVED_10	ERRTICERREVTEN	L1SUSPEN
R	R/W	NONE	R/W	R	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SOFTEVTEN	U3L2L1SUSPEN	HIBERNATIONREQEVTEN	WKUPEVTEN	ULSTCNGEN	CONNECTDONEEVTEN	USBRSTEVTEN	DISSCONNEVTEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28964. USB2SS_DEV_DEVTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R	0h	Reserved
16	ECCERREN	R	0h	ECC Error Enable. If this bit is set to 1, the controller reports an ECC error to the software when an uncorrectable ECC occurs internally. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved
14	L1WKUPEVTEN	R/W	0h	L1 Resume Detected Event Enable. Note: If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for L1 Resume Detected Event Enable. Reset Source: rst_mod_g_rst_n
13	RESERVED	NONE	0h	Reserved
12	VENDEVTSTRCVDEN	R/W	0h	Vendor Device Test LMP Received Event [VndrDevTstRcvedEn] Reset Source: rst_mod_g_rst_n
11	RESERVED_11	R	0h	Reserved
10	RESERVED_10	R	0h	Reserved

Table 14-28964. USB2SS_DEV_DEVTEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ERRTICERREVTEN	R/W	0h	Erratic Error Event Enable Reset Source: rst_mod_g_rst_n
8	L1SUSPEN	R/W	0h	L1 Suspend Event Enable Note: Only if GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, this bit is for L1 Suspend Event Enable. Reset Source: rst_mod_g_rst_n
7	SOFTEVTEN	R/W	0h	Start of [u]frame Reset Source: rst_mod_g_rst_n
6	U3L2L1SUSPEN	R/W	0h	U3/L2 or U3/L2L1 Suspend Event Enable. Note: - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Suspend Event Enable. - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Suspend Event Enable. Reset Source: rst_mod_g_rst_n
5	HIBERNATIONREQEVTEN	R/W	0h	This bit enables/disables the generation of the Hibernation Request Event. Reset Source: rst_mod_g_rst_n
4	WKUPEVTEN	R/W	0h	U3/L2 or U3/L2L1 Resume Detected Event Enable. Note: - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Resume Detected Event Enable. - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Resume Detected Event Enable. Reset Source: rst_mod_g_rst_n
3	ULSTCNGEN	R/W	0h	USB/Link State Change Event Enable Reset Source: rst_mod_g_rst_n
2	CONNECTDONEEVTEN	R/W	0h	Connection Done Enable Reset Source: rst_mod_g_rst_n
1	USBRSTEVTEN	R/W	0h	USB Reset Enable Reset Source: rst_mod_g_rst_n
0	DISSCONNEVTEN	R/W	0h	Disconnect Detected Event Enable Reset Source: rst_mod_g_rst_n

14.9.3.2.2.371 USB2SS_DEV_DSTS Register

1 USB2SS_DEV_DSTS Register (Offset = Ch) [reset = 520004h]

Device Status Register This register indicates the status of the device controller with respect to USB-related events. Note: When Hibernation is not enabled, RSS and SSS fields always return 0 when read.

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Table 14-28965. Instance Table

Instance Name	Physical Address
USB0	**3100 C70Ch**
USB1	**3110 C70Ch**

Figure 14-9600. USB2SS_DEV_DSTS Name Register

31	30	29	28	27	26	25	24
RESERVED_31_30		DCNRD	SRE	RESERVED_27_26		RSS	SSS
R		R	R/W1TC	R		R	R
0h		0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
COREIDLE	DEVCTRLHLT	USBLNKST				RXFIFOEMPTY	SOFFN
R	R	R				R	R
0h	1h	4h				1h	0h
15	14	13	12	11	10	9	8
SOFFN							
R							
0h							
7	6	5	4	3	2	1	0
SOFFN					CONNECTSPD		
R					R		
0h					4h		

Table 14-28967. USB2SS_DEV_DSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_31_30	R	0h	Reserved
29	DCNRD	R	0h	Device Controller Not Ready The bit indicates that the controller is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to 2 and GCTL[1].GblHibernationEn =1. Reset Source: rst_mod_g_rst_n
28	SRE	R/W1TC	0h	Save Restore Error. Currently not supported. Reset Source: rst_mod_g_rst_n
27:26	RESERVED_27_26	R	0h	Reserved

Table 14-28967. USB2SS_DEV_DSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	RSS	R	0h	RSS Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to '0'. Reset Source: rst_mod_g_rst_n
24	SSS	R	0h	SSS Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to '0'. Reset Source: rst_mod_g_rst_n
23	COREIDLE	R	0h	Core Idle The bit indicates that the controller finished transferring all RxFIFO data to system memory, Writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the controller and does not hold a static value. Reset Source: rst_mod_g_rst_n
22	DEVCTRLHLT	R	1h	Device Controller Halted This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The controller sets this bit to 1 when, after SW sets Run/Stop to 0, the controller is idle and the lower layer finishes the disconnect process. When Halted=1, the controller does not generate Device events. Note: - The controller does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated [by Writing to GEVNTCOUNTn] while it is waiting for this bit to be set to 1. - When Interrupt Moderation is enabled, there could be delay in raising the interrupt line when the event count is non-zero. Software should read the GEVNTCOUNT register directly and acknowledge them. Reset Source: rst_mod_g_rst_n

Table 14-28967. USB2SS_DEV_DSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:18	USBLNKST	R	4h	USBLNKST. USB/Link State In SS mode: LTSSM State - 4'h0: U0 - 4'h1: U1 - 4'h2: U2 - 4'h3: U3 - 4'h4: SS_DIS - 4'h5: RX_DET - 4'h6: SS_INACT - 4'h7: POLL - 4'h8: RECOV - 4'h9: HRESET - 4'ha: CMPLY - 4'hb: LPBK - 4'hf: Resume/Reset In HS/FS/LS mode: - 4'h0: On state - 4'h2: Sleep [L1] state - 4'h3: Suspend [L2] state - 4'h4: Disconnected state [Default state] - 4'h5: Early Suspend state [valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0] - 4'he: Reset [valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1] - 4'hf: Resume [valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1] The link state Resume/Reset indicates that the controller received a resume or USB reset request from the host while the link was in hibernation. Software must write '8' [Recovery] to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to '1' and DSTS[29].DCNRD = 0. The Early Suspend link state is an early indication of device suspend in HS/FS. The link state changes to Early Suspend after detecting bus idle for 3ms. - In HS operation, this is an indication that the USB bus [that is, LineState] has been in idle [SE0] for 3ms. However, it does not confirm whether the next process is Suspend or Reset. The device checks the bus again after pull up enable delay and if the line state indicates Suspend [full speed J], then the device waits for an additional time [~3ms] to indicate the actual Suspend state. - In FS operation, this is an indication that the USB bus [that is, LineState] has been in idle [J] for 3ms. The device waits for an additional time [~3ms of Idle] to indicate the actual Suspend state. Reset Source: rst_mod_g_rst_n
17	RXFIFOEMPTY	R	1h	RxFIFO Empty. Reset Source: rst_mod_g_rst_n
16:3	SOFFN	R	0h	Frame/Microframe Number of the Received SOF. When the controller is operating at SuperSpeed, - [16:3] indicates the uframe/ITP number When the controller is operating at high-speed, - [16:6] indicates the frame number - [5:3] indicates the microframe number When the controller is operating at full-speed, - [16:14] is not used. Software can ignore these 3 bits - [13:3] indicates the frame number Note: After power-on reset, the controller generates the microframe number internally for every 125us if the USB host has not issued SOF/ITP yet. During P3 state, the duration of SOFFN is based on the suspend_clk frequency. Reset Source: rst_mod_g_rst_n

Table 14-28967. USB2SS_DEV_DSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	CONNECTSPD	R	4h	Connected Speed [ConnectSpd] Indicates the speed at which the DWC_usb3 controller has come up after speed detection through a chirp sequence. - 3'b100: SuperSpeed [PHY clock is running at 125 or 250 MHz] - 3'b000: High-speed [PHY clock is running at 30 or 60 MHz] - 3'b001: Full-speed [PHY clock is running at 30 or 60 MHz] Low-speed is not supported for devices using a UTMI+ PHY. Reset Source: rst_mod_g_rst_n 0 `HighSpeed` 1 `FullSpeed` 4 `SuperSpeed`

14.9.3.2.2.372 USB2SS_DEV_DGCMDPAR Register

1 USB2SS_DEV_DGCMDPAR Register (Offset = 10h) [reset = 0h]

Device Generic Command Parameter Register This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

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Table 14-28968. Instance Table

Instance Name	Physical Address
USB0	**3100 C710h**
USB1	**3110 C710h**

Figure 14-9601. USB2SS_DEV_DGCMDPAR Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PARAMETER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PARAMETER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PARAMETER							
R/W							
0h							

Table 14-28970. USB2SS_DEV_DGCMDPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.9.3.2.2.373 USB2SS_DEV_DGCMD Register

1 USB2SS_DEV_DGCMD Register (Offset = 14h) [reset = 0h]

Device Generic Command Register This register enables software to program the controller using a single generic command interface to send link management packets and notifications. This register contains command, control, and status fields relevant to the current generic command, while the DGCMDPAR register provides the command parameter.

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Table 14-28971. Instance Table

Instance Name	Physical Address
USB0	**3100 C714h**
USB1	**3110 C714h**

Figure 14-9602. USB2SS_DEV_DGCMD Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CMDSTATUS				RESERVED_11	CMDACT	RESERVED_9	CMDIOC
R				R	R/W1TS	R	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMDTYP							
R/W							
0h							

Table 14-28973. USB2SS_DEV_DGCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:12	CMDSTATUS	R	0h	Command Status - 1: CmdErr: Indicates that the device controller encountered an error while processing the command. - 0: Indicates command success Reset Source: rst_mod_g_rst_n
11	RESERVED_11	R	0h	Reserved
10	CMDACT	R/W1TS	0h	Command Active The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command. Reset Source: rst_mod_g_rst_n
9	RESERVED_9	R	0h	Reserved

Table 14-28973. USB2SS_DEV_DGCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CMDIOC	R/W	0h	Command Interrupt on Complete When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'. Reset Source: rst_mod_g_rst_n
7:0	CMDTYP	R/W	0h	CMDTYP Generic Command Type Specifies the type of generic command the software driver is requesting the controller to perform. - 02h: Set Periodic Parameters - 04h: Set Scratchpad Buffer Array Address Lo - 05h: Set Scratchpad Buffer Array Address Hi - 07h: Transmit Device Notification - 09h: Selected FIFO Flush - 0Ah: All FIFO Flush - 0Ch: Set Endpoint NRDY - 10h: Run SoC Bus LoopBack Test - 11h: Restart After Disconnect All other values are reserved. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.374 USB2SS_DEV_DALEPENA Register

1 USB2SS_DEV_DALEPENA Register (Offset = 20h) [reset = 0h]

Device Active USB Endpoint Enable Register. This register indicates whether a USB endpoint is active in a given configuration or interface.

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Table 14-28974. Instance Table

Instance Name	Physical Address
USB0	**3100 C720h**
USB1	**3110 C720h**

Figure 14-9603. USB2SS_DEV_DALEPENA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">USBACTEP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">USBACTEP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">USBACTEP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">USBACTEP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28976. USB2SS_DEV_DALEPENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USBACTEP	R/W	0h	USBACTEP USB Active Endpoints [USBActEP] This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0.15 and OUT endpoints 0.15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: - Bit[0]: USB EP0-OUT - Bit[1]: USB EP0-IN - Bit[2]: USB EP1-OUT - Bit[3]: USB EP1-IN The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints [resources] after USBReset. Hardware clears these bits for all endpoints [other than EP0-OUT and EP0-IN] after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits. For more information, see "Flexible Endpoint Mapping" section in the Databook. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.375 USB2SS_DEV_DEV_RESERVED_RSVD_j Register

1 USB2SS_DEV_DEV_RESERVED_RSVD_j Register (Offset = 0h + formula) [reset = 0h]

Reserved

Return to Summary Table

Offset = 24h + (j * 4h); where j = 0 to 31d

Table 14-28977. Instance Table

Instance Name	Physical Address
USB0	**3100 C700h + formula**
USB1	**3110 C700h + formula**

Figure 14-9604. USB2SS_DEV_DEV_RESERVED_RSVD_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-28979. USB2SS_DEV_DEV_RESERVED_RSVD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.9.3.2.2.376 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Register

1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Register (Offset = 0h + formula) [reset = 0h]

Device Physical Endpoint-n Command Parameter 2 Register (DEPCMDPAR2n) This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

Return to Summary Table

Offset = 100h + (j * 10h); where j = 0 to 31d

Table 14-28980. Instance Table

Instance Name	Physical Address
USB0	**3100 C700h + formula**
USB1	**3110 C700h + formula**

Figure 14-9605. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-28982. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.9.3.2.2.377 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Register

1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Register (Offset = 4h + formula) [reset = 0h]

Device Physical Endpoint-n Command Parameter 1 Register (DEPCMDPAR1n)

Return to Summary Table

Offset = 104h + (j * 10h); where j = 0 to 31d

Table 14-28983. Instance Table

Instance Name	Physical Address
USB0	**3100 C704h + formula**
USB1	**3110 C704h + formula**

Figure 14-9606. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-28985. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.9.3.2.2.378 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Register

1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Register (Offset = 8h + formula) [reset = 0h]

Device Physical Endpoint-n Command Parameter 0 Register (DEPCMDPAR0n)

Return to Summary Table

Offset = 108h + (j * 10h); where j = 0 to 31d

Table 14-28986. Instance Table

Instance Name	Physical Address
USB0	**3100 C708h + formula**
USB1	**3110 C708h + formula**

Figure 14-9607. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-28988. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.9.3.2.2.379 USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register

1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register (Offset = Ch + formula) [reset = 0h]

Device Physical Endpoint-n Command Register This register enables software to issue physical endpoint-specific commands. This register contains command, control, and status fields relevant to the current generic command, while the DEPCMDPAR[2:0]n registers provide command parameters and return status information. Several fields (including Command Type) are write-only, so their read values are undefined. After power-on, prior to issuing the first endpoint command, the read value of this register is undefined. In particular, the CmdAct bit may be set after power-on. In this case, it is safe to issue an endpoint command.

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Offset = 10Ch + (j * 10h); where j = 0 to 31d

Table 14-28989. Instance Table

Instance Name	Physical Address
USB0	**3100 C70Ch + formula**
USB1	**3110 C70Ch + formula**

Figure 14-9608. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Name Register

31	30	29	28	27	26	25	24
COMMANDPARAM							
R/W							
0h							
23	22	21	20	19	18	17	16
COMMANDPARAM							
R/W							
0h							
15	14	13	12	11	10	9	8
CMDSTATUS				HIPRI_FORCERM	CMDACT	RESERVED_9	CMDIOC
R/W				R/W	R/W	R	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_7_4				CMDTYP			
R				R/W			
0h				0h			

Table 14-28991. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COMMANDPARAM	R/W	0h	Command Parameters or Event Parameters Command Parameters [CommandParam], when this register is written: For Start Transfer command: - [31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint - [31:16]: StartMicroFramNum: Indicates the [micro]frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands - [22:16]: Transfer Resource Index [XferRscIdx]. The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters [EventParam], when this register is read. Refer to bits [31:16] in Table "Device Endpoint-n Events: DEPEVT". Reset Source: rst_mod_g_rst_n
15:12	CMDSTATUS	R/W	0h	Command Completion Status [CmdStatus] Additional information about the completion of this command is available in this field. The information is in the same format as bits 15:12 of the Endpoint Command Complete event, see "Device Endpoint-n Events: DEPEVT" table in the Programming Guide. Reset Source: rst_mod_g_rst_n
11	HIPRI_FORCERM	R/W	0h	HighPriority/ForceRM [HiPri_ForceRM] - HighPriority: Only valid for Start Transfer command - ForceRM: Only valid for End Transfer command - ClearPendIN: Only valid for Clear Stall command . Software sets this bit to clear any pending IN transaction [on that endpoint] stuck at the lower layers when a Clear Stall command is issued. Reset Source: rst_mod_g_rst_n
10	CMDACT	R/W	0h	Command Active [CmdAct] Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place. Reset Source: rst_mod_g_rst_n
9	RESERVED_9	R	0h	Reserved
8	CMDIOC	R/W	0h	CMDIOC Command Interrupt on Complete [CmdIOC] When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_7_4	R	0h	Reserved

Table 14-28991. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CMDTYP	R/W	0h	Command Type Specifies the type of command the software driver is requesting the controller to perform. - 00h: Reserved - 01h: Set Endpoint Configuration - -64 or 96-bit Parameter - 02h: Set Endpoint Transfer Resource Configuration - 32-bit Parameter - 03h: Get Endpoint State - No Parameter Needed - 04h: Set Stall - No Parameter Needed - 05h: Clear Stall [see Set Stall] - No Parameter Needed - 06h: Start Transfer - 64-bit Parameter - 07h: Update Transfer - No Parameter Needed - 08h: End Transfer - No Parameter Needed - 09h: Start New Configuration - No Parameter Needed Reset Source: rst_mod_g_rst_n

14.9.3.2.2.380 USB2SS_DEV_DEV_INTR_DEV_IMOD_j Register

1 USB2SS_DEV_DEV_INTR_DEV_IMOD_j Register (Offset = 0h + formula) [reset = 0h]

Device Interrupt Moderation Register (DEV_IMOD) This register controls the Interrupt Moderation feature that allows the device software to throttle the interrupt rate. Key Functions: - Interrupt Moderation is enabled only when the IMOD Interval is programmed to a non-zero value. - Interrupt is asserted whenever the IMOD (down) counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events (that is, event count is non-zero) - GEVNTCOUNT[EVNT_HANDLER_BUSY] is set by hardware when interrupt is asserted, and cleared by software when interrupt processing is completed. - The Interrupt line is de-asserted after the first write to the event count. - IMOD counter is loaded with IMOD interval whenever the Interrupt line is de-asserted.

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Offset = 300h + (j * 4h); where j = 0 to 7d

Table 14-28992. Instance Table

Instance Name	Physical Address
USB0	**3100 C700h + formula**
USB1	**3110 C700h + formula**

Figure 14-9609. USB2SS_DEV_DEV_INTR_DEV_IMOD_j Name Register

31	30	29	28	27	26	25	24
DEVICE_IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVICE_IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVICE_IMODI							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVICE_IMODI							
R/W							
0h							

Table 14-28994. USB2SS_DEV_DEV_INTR_DEV_IMOD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DEVICE_IMODC	R/W	0h	Interrupt Moderation Down Counter Loaded with the DEVICE_IMODI value, whenever the hardware interrupt[n] line is de-asserted from the asserted state, counts down to 0, and stops. The interrupt[n] is signaled whenever this counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events [that is, event count is non-zero]. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n

Table 14-28994. USB2SS_DEV_DEV_INTR_DEV_IMOD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	DEVICE_IMODI	R/W	0h	Moderation Interval [DEVICE_IMODI] This field holds the minimum inter-interrupt interval between events. The interval is specified in terms of 250ns increments. A value of 0 disables the interrupt throttling logic and interrupts are generated immediately if event count becomes non-zero. In scaledown simulation mode, 4 ram clocks are used to time 250ns. Reset Source: rst_mod_g_rst_n

14.9.3.2.2.381 USB2SS_LINK_LINK_LU1LFPSRXTIM Register

1 USB2SS_LINK_LINK_LU1LFPSRXTIM Register (Offset = 0h) [reset = 1F1Fh]

U1/U2 LFPS Rx Timer Register - Link Layer Register for U1/U2 LFPS RX Timers. - This register is common for all SS ports.

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Table 14-28995. Instance Table

Instance Name	Physical Address
USB0	**3100 D000h**
USB1	**3110 D000h**

Figure 14-9610. USB2SS_LINK_LINK_LU1LFPSRXTIM Name Register

31	30	29	28	27	26	25	24
RESERVED_16_31							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_16_31							
R/W							
0h							
15	14	13	12	11	10	9	8
U1U2_LFPS_EXIT_RX_CLK							
R/W							
1Fh							
7	6	5	4	3	2	1	0
U1U2_EXIT_RSP_RX_CLK							
R/W							
1Fh							

Table 14-28997. USB2SS_LINK_LINK_LU1LFPSRXTIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_16_31	R/W	0h	Reserved
15:8	U1U2_LFPS_EXIT_RX_CLK	R/W	1Fh	Programmable U1U2 LFPS EXIT RX CLKS - Applicable to Remote Partner initiated Ux exit: Time to recognize valid Ux exit request from the remote partner. - This field is encoded as the pipe clk [8ns] count for the LFPS. -- 1: 8ns -- 2: 16ns -- 3: 24ns, and so on Reset Source: rst_mod_g_rst_n
7:0	U1U2_EXIT_RSP_RX_CLK	R/W	1Fh	Programmable U1U2 EXIT RESP RX CLKS - Applicable to locally initiated Ux exit: Minimum LFPS reception from remote to consider Ux exit handshake is successful. - This field is encoded as the pipe clk [8ns] count for the LFPS. -- 1: 8ns -- 2: 16ns -- 3: 24ns, and so on Reset Source: rst_mod_g_rst_n

14.9.3.2.2.382 USB2SS_LINK_LINK_LINK_SETTINGS Register

1 USB2SS_LINK_LINK_LINK_SETTINGS Register (Offset = 20h) [reset = 45900000h]

Link Setting Register - Link Layer User Control Register for enabling Link/PHY-specific options. - This register is common for all SS ports.

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Table 14-28998. Instance Table

Instance Name	Physical Address
USB0	**3100 D020h**
USB1	**3110 D020h**

Figure 14-9611. USB2SS_LINK_LINK_LINK_SETTINGS Name Register

31	30	29	28	27	26	25	24
RESERVED_31	U1_RESID_TIMER_US			RESERVED_27	PM_LC_TIMER_US		
R/W	R/W			R/W	R/W		
0h	4h			0h	5h		
23	22	21	20	19	18	17	16
PM_ENTRY_TIMER_US				RESERVED_0_19			
R/W				R/W			
9h				0h			
15	14	13	12	11	10	9	8
RESERVED_0_19							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_0_19							
R/W							
0h							

Table 14-29000. USB2SS_LINK_LINK_LINK_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R/W	0h	Reserved
30:28	U1_RESID_TIMER_US	R/W	4h	Programmable U1 MIN RESIDENCY TIMER This field specifies U1 MIN RESIDENCY TIMER value in us. Set to 0 to disable the timer. Reset Source: rst_mod_g_rst_n
27	RESERVED_27	R/W	0h	Reserved
26:24	PM_LC_TIMER_US	R/W	5h	Programmable PM_LC_TIMER This field specifies PM_LC_TIMER value in us. Reset Source: rst_mod_g_rst_n
23:20	PM_ENTRY_TIMER_US	R/W	9h	Programmable PM_ENTRY_TIMER This field specifies PM_ENTRY_TIMER value in us. Reset Source: rst_mod_g_rst_n
19:0	RESERVED_0_19	R/W	0h	Reserved

14.9.3.2.2.383 USB2SS_LINK_LINK_LLUCTL Register

1 USB2SS_LINK_LINK_LLUCTL Register (Offset = 24h) [reset = 800080h]

Link User Control Register - Link Layer User Control Register for enabling Link/PHY-specific options. - This register is common for all SS ports.

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Table 14-29001. Instance Table

Instance Name	Physical Address
USB0	**3100 D024h**
USB1	**3110 D024h**

Figure 14-9612. USB2SS_LINK_LINK_LLUCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_30_31		SUPPORT_P4_PG	SUPPORT_P4	RESERVED_24_27			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DISRXDET_LTSSM_TIMER_OVRRD	RESERVED_13_22						
R/W	R/W						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_13_22			U2P3CPMOK	EN_RESET_PIPE_AFTER_PHY_MUX	RESERVED_8_10		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MASK_PIPE_RESET	RESERVED_6	NO_UX_EXIT_P0_TRANS	RESERVED_0_4				
R/W	R/W	R/W	R/W				
1h	0h	0h	0h				

Table 14-29003. USB2SS_LINK_LINK_LLUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_30_31	R/W	0h	Reserved
29	SUPPORT_P4_PG	R/W	0h	PHY P4 Power gate mode [PG] is enabled. Set this bit if the PHY supports PG mode in P4. This bit is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
28	SUPPORT_P4	R/W	0h	Support PHY P3.CPM and P4 Power States. When this bit is set, the controller puts the PHY in P3.CPM or P4 in certain states. This bit is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
27:24	RESERVED_24_27	R/W	0h	Reserved
23	DISRXDET_LTSSM_TIMER_OVRRD	R/W	1h	DisRxDet_LTSSM_Timer_Ovrrd. When DisRxDetU3RxDet is asserted in Polling or U1, the timeout expires immediately. Reset Source: rst_mod_g_rst_n

Table 14-29003. USB2SS_LINK_LINK_LLUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:13	RESERVED_13_22	R/W	0h	Reserved
12	U2P3CPMOK	R/W	0h	P3CPM OK for U2/SSInactive [U2P3CPMok] - 0: During link state U2/SS.Inactive, put PHY in P2 [Default] - 1: During link state U2/SS.Inactive, put PHY in P3CPM. Note: For a port, if both GUCTL1[25]=1 and LUCTL[12]=1, LUCTL[12]=1 takes priority. Reset Source: rst_mod_g_rst_n
11	EN_RESET_PIPE_AFTER_PHY_MUX	R/W	0h	en_reset_pipe_after_phy_mux. The controller issues USB 3.0 PHY reset after DisRxDetU3RxDet is de-asserted. Reset Source: rst_mod_g_rst_n
10:8	RESERVED_8_10	R/W	0h	Reserved
7	MASK_PIPE_RESET	R/W	1h	Mask pipe reset. If this bit is set, controller blocks pipe_reset_n from going to the PHY when DisRxDetU3RxDet=1. Reset Source: rst_mod_g_rst_n
6	RESERVED_6	R/W	0h	Reserved
5	NO_UX_EXIT_P0_TRANS	R/W	0h	no_ux_exit_p0_trans. Link LTSSM detects Ux_exit LFPS when P0 transition is on-going by default. If this bit is set, Link LTSSM may miss Ux_exit LFPS when P0 transition is happening. Reset Source: rst_mod_g_rst_n
4:0	RESERVED_0_4	R/W	0h	Reserved

14.9.3.2.2.384 USB2SS_LINK_LINK_LPTMDPDELAY Register

1 USB2SS_LINK_LINK_LPTMDPDELAY Register (Offset = 28h) [reset = C00h]

Link Datapath Delay Register - Link Layer Timer Register for P3CPM/P4 Residency. - This register is common for all SS ports.

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Table 14-29004. Instance Table

Instance Name	Physical Address
USB0	**3100 D028h**
USB1	**3110 D028h**

Figure 14-9613. USB2SS_LINK_LINK_LPTMDPDELAY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_22_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED_22_31</td><td colspan="6">P3CPMP4_RESIDENCY</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">P3CPMP4_RESIDENCY</td><td colspan="2">RESERVED_0_9</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">3h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_0_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29006. USB2SS_LINK_LINK_LPTMDPDELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED_22_31	R/W	0h	Reserved
21:10	P3CPMP4_RESIDENCY	R/W	3h	p3cpmp4 residency timer value. Minimum number of suspend_clk periods that the controller needs to stay in P3.CPM or P4 before exiting P3.CPM or P4. This field is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
9:0	RESERVED_0_9	R/W	0h	Reserved

14.9.3.2.2.385 USB2SS_DEBUG_DEBUG_U3RHBDBG Register

1 USB2SS_DEBUG_DEBUG_U3RHBDBG Register (Offset = 0h) [reset = 0h]

U3 Root Hub Debug Register

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Table 14-29007. Instance Table

Instance Name	Physical Address
USB0	**3100 D800h**
USB1	**3110 D800h**

Figure 14-9614. USB2SS_DEBUG_DEBUG_U3RHBDBG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_1</td><td>TPCFG_TOUT_CTRL</td><td colspan="3">RESERVED_0_2</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-29009. USB2SS_DEBUG_DEBUG_U3RHBDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_1	R	0h	Reserved_1
3	TPCFG_TOUT_CTRL	R/W	0h	tpcfg_tout_ctrl This bit controls the USB 3.0 port configuration timeout duration. - 1: The port configuration timeout counter resets when the link is not in U0. - 0: The port configuration timeout counter does not reset if the link enters recovery or exits U0. Reset Source: rst_mod_g_rst_n
2:0	RESERVED_0_2	R	0h	Reserved_0_2

14.9.3.2.2.386 USB2SS_DEBUG_RAM0_RAM0_j Register

1 USB2SS_DEBUG_RAM0_RAM0_j Register (Offset = 0h + formula) [reset = 0h]

RAM0 memory region accessible through config interface for debug purpose only.

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Offset = 0h + (j * 4h); where j = 0 to 14411d

Table 14-29010. Instance Table

Instance Name	Physical Address
USB0	**3104 0000h + formula**
USB1	**3114 0000h + formula**

Figure 14-9615. USB2SS_DEBUG_RAM0_RAM0_j Name Register

31	30	29	28	27	26	25	24
MEM							
R/W							
0h							
23	22	21	20	19	18	17	16
MEM							
R/W							
0h							
15	14	13	12	11	10	9	8
MEM							
R/W							
0h							
7	6	5	4	3	2	1	0
MEM							
R/W							
0h							

Table 14-29012. USB2SS_DEBUG_RAM0_RAM0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEM	R/W	0h	Memory location Reset Source: rst_mod_g_rst_n

14.9.4 Memory Interfaces Registers

14.9.4.1 FSS

FSS

14.9.4.1.1 FSS Summaries

FSS Summaries

Table 14-29013. FSS_GENREGS Registers, Base Address=0FC0 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS_GENREGS_REVISION	0FC0 0000h

14.9.4.1.2 FSS Registers

FSS Registers

14.9.4.1.2.1 FSS_GENREGS_REVISION Register

1 FSS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502101h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-29014. Instance Table

Instance Name	Physical Address
FSS0	**0FC0 0000h**

Figure 14-9616. FSS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							
23	22	21	20	19	18	17	16
MODID							
R							
6850h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
4h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-29016. FSS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: vbus_mod_g_rst_n

14.9.4.2 FSS_FSAS_0

FSS_FSAS_0

14.9.4.2.1 FSS_FSAS_0 Summaries

FSS_FSAS_0 Summaries

Table 14-29017. FSS_FSAS_GENREGS Registers, Base Address=0FC1 0000h, Length=256

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_FSAS_GENREGS_REVISION	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_SYSCONFIG	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_FRAG_ADR	0FC1 0008h
Ch	32	FSS_FSAS_GENREGS_FRAG_CTL	0FC1 000Ch
0h	32	FSS_FSAS_GENREGS_IRQ_EOI	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_IRQ_STATUS_RAW	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_IRQ_STATUS	0FC1 0008h
Ch	32	FSS_FSAS_GENREGS_IRQ_ENABLE_SET	0FC1 000Ch
10h	32	FSS_FSAS_GENREGS_IRQ_ENABLE_CLR	0FC1 0010h
0h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	0FC1 0000h + formula
4h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	0FC1 0004h + formula
0h	32	FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_ERR_ECC_TYPE	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_ERR_WRT_TYPE	0FC1 0008h

Table 14-29018. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_FSAS_OTFA_REGS_REVID	0FC2 0000h
4h	32	FSS_FSAS_OTFA_REGS_SCFG	0FC2 0004h
8h	32	FSS_FSAS_OTFA_REGS_ISR	0FC2 0008h
Ch	32	FSS_FSAS_OTFA_REGS_IS	0FC2 000Ch
10h	32	FSS_FSAS_OTFA_REGS_IES	0FC2 0010h
14h	32	FSS_FSAS_OTFA_REGS_IEC	0FC2 0014h
18h	32	FSS_FSAS_OTFA_REGS_CCFG	0FC2 0018h
1Ch	32	FSS_FSAS_OTFA_REGS_CSTATUS	0FC2 001Ch
20h	32	FSS_FSAS_OTFA_REGS_RGCFG0	0FC2 0020h
24h	32	FSS_FSAS_OTFA_REGS_RGMACST0	0FC2 0024h
28h	32	FSS_FSAS_OTFA_REGS_RGST0	0FC2 0028h
2Ch	32	FSS_FSAS_OTFA_REGS_RGSI0	0FC2 002Ch
30h	32	FSS_FSAS_OTFA_REGS_RKEYE00	0FC2 0030h
34h	32	FSS_FSAS_OTFA_REGS_RKEYE01	0FC2 0034h
38h	32	FSS_FSAS_OTFA_REGS_RKEYE02	0FC2 0038h
3Ch	32	FSS_FSAS_OTFA_REGS_RKEYE03	0FC2 003Ch
40h	32	FSS_FSAS_OTFA_REGS_RKEYE04	0FC2 0040h
44h	32	FSS_FSAS_OTFA_REGS_RKEYE05	0FC2 0044h
48h	32	FSS_FSAS_OTFA_REGS_RKEYE06	0FC2 0048h
4Ch	32	FSS_FSAS_OTFA_REGS_RKEYE07	0FC2 004Ch

Table 14-29018. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
50h	32	FSS_FSAS_OTFA_REGS_RKEYEP00	0FC2 0050h
54h	32	FSS_FSAS_OTFA_REGS_RKEYEP01	0FC2 0054h
58h	32	FSS_FSAS_OTFA_REGS_RKEYEP02	0FC2 0058h
5Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP03	0FC2 005Ch
60h	32	FSS_FSAS_OTFA_REGS_RKEYEP04	0FC2 0060h
64h	32	FSS_FSAS_OTFA_REGS_RKEYEP05	0FC2 0064h
68h	32	FSS_FSAS_OTFA_REGS_RKEYEP06	0FC2 0068h
6Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP07	0FC2 006Ch
70h	32	FSS_FSAS_OTFA_REGS_RKEYA00	0FC2 0070h
74h	32	FSS_FSAS_OTFA_REGS_RKEYA01	0FC2 0074h
78h	32	FSS_FSAS_OTFA_REGS_RKEYA02	0FC2 0078h
7Ch	32	FSS_FSAS_OTFA_REGS_RKEYA03	0FC2 007Ch
80h	32	FSS_FSAS_OTFA_REGS_RKEYAP00	0FC2 0080h
84h	32	FSS_FSAS_OTFA_REGS_RKEYAP01	0FC2 0084h
88h	32	FSS_FSAS_OTFA_REGS_RKEYAP02	0FC2 0088h
8Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP03	0FC2 008Ch
90h	32	FSS_FSAS_OTFA_REGS_RIV00	0FC2 0090h
94h	32	FSS_FSAS_OTFA_REGS_RIV01	0FC2 0094h
98h	32	FSS_FSAS_OTFA_REGS_RIV02	0FC2 0098h
9Ch	32	FSS_FSAS_OTFA_REGS_RIV03	0FC2 009Ch
A0h	32	FSS_FSAS_OTFA_REGS_RGCFG1	0FC2 00A0h
A4h	32	FSS_FSAS_OTFA_REGS_RGMACST1	0FC2 00A4h
A8h	32	FSS_FSAS_OTFA_REGS_RGST1	0FC2 00A8h
ACh	32	FSS_FSAS_OTFA_REGS_RGSI1	0FC2 00ACh
B0h	32	FSS_FSAS_OTFA_REGS_RKEYE10	0FC2 00B0h
B4h	32	FSS_FSAS_OTFA_REGS_RKEYE11	0FC2 00B4h
B8h	32	FSS_FSAS_OTFA_REGS_RKEYE12	0FC2 00B8h
BCh	32	FSS_FSAS_OTFA_REGS_RKEYE13	0FC2 00BCh
C0h	32	FSS_FSAS_OTFA_REGS_RKEYE14	0FC2 00C0h
C4h	32	FSS_FSAS_OTFA_REGS_RKEYE15	0FC2 00C4h
C8h	32	FSS_FSAS_OTFA_REGS_RKEYE16	0FC2 00C8h
CCh	32	FSS_FSAS_OTFA_REGS_RKEYE17	0FC2 00CCh
D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP10	0FC2 00D0h
D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP11	0FC2 00D4h
D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP12	0FC2 00D8h
DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP13	0FC2 00DCh
E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP14	0FC2 00E0h
E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP15	0FC2 00E4h
E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP16	0FC2 00E8h
ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP17	0FC2 00ECh
F0h	32	FSS_FSAS_OTFA_REGS_RKEYA10	0FC2 00F0h
F4h	32	FSS_FSAS_OTFA_REGS_RKEYA11	0FC2 00F4h
F8h	32	FSS_FSAS_OTFA_REGS_RKEYA12	0FC2 00F8h
FCh	32	FSS_FSAS_OTFA_REGS_RKEYA13	0FC2 00FCh

Table 14-29018. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
100h	32	FSS_FSAS_OTFA_REGS_RKEYAP10	0FC2 0100h
104h	32	FSS_FSAS_OTFA_REGS_RKEYAP11	0FC2 0104h
108h	32	FSS_FSAS_OTFA_REGS_RKEYAP12	0FC2 0108h
10Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP13	0FC2 010Ch
110h	32	FSS_FSAS_OTFA_REGS_RIV10	0FC2 0110h
114h	32	FSS_FSAS_OTFA_REGS_RIV11	0FC2 0114h
118h	32	FSS_FSAS_OTFA_REGS_RIV12	0FC2 0118h
11Ch	32	FSS_FSAS_OTFA_REGS_RIV13	0FC2 011Ch
120h	32	FSS_FSAS_OTFA_REGS_RGCFG2	0FC2 0120h
124h	32	FSS_FSAS_OTFA_REGS_RGMACST2	0FC2 0124h
128h	32	FSS_FSAS_OTFA_REGS_RGST2	0FC2 0128h
12Ch	32	FSS_FSAS_OTFA_REGS_RGSI2	0FC2 012Ch
130h	32	FSS_FSAS_OTFA_REGS_RKEYE20	0FC2 0130h
134h	32	FSS_FSAS_OTFA_REGS_RKEYE21	0FC2 0134h
138h	32	FSS_FSAS_OTFA_REGS_RKEYE22	0FC2 0138h
13Ch	32	FSS_FSAS_OTFA_REGS_RKEYE23	0FC2 013Ch
140h	32	FSS_FSAS_OTFA_REGS_RKEYE24	0FC2 0140h
144h	32	FSS_FSAS_OTFA_REGS_RKEYE25	0FC2 0144h
148h	32	FSS_FSAS_OTFA_REGS_RKEYE26	0FC2 0148h
14Ch	32	FSS_FSAS_OTFA_REGS_RKEYE27	0FC2 014Ch
150h	32	FSS_FSAS_OTFA_REGS_RKEYEP20	0FC2 0150h
154h	32	FSS_FSAS_OTFA_REGS_RKEYEP21	0FC2 0154h
158h	32	FSS_FSAS_OTFA_REGS_RKEYEP22	0FC2 0158h
15Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP23	0FC2 015Ch
160h	32	FSS_FSAS_OTFA_REGS_RKEYEP24	0FC2 0160h
164h	32	FSS_FSAS_OTFA_REGS_RKEYEP25	0FC2 0164h
168h	32	FSS_FSAS_OTFA_REGS_RKEYEP26	0FC2 0168h
16Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP27	0FC2 016Ch
170h	32	FSS_FSAS_OTFA_REGS_RKEYA20	0FC2 0170h
174h	32	FSS_FSAS_OTFA_REGS_RKEYA21	0FC2 0174h
178h	32	FSS_FSAS_OTFA_REGS_RKEYA22	0FC2 0178h
17Ch	32	FSS_FSAS_OTFA_REGS_RKEYA23	0FC2 017Ch
180h	32	FSS_FSAS_OTFA_REGS_RKEYAP20	0FC2 0180h
184h	32	FSS_FSAS_OTFA_REGS_RKEYAP21	0FC2 0184h
188h	32	FSS_FSAS_OTFA_REGS_RKEYAP22	0FC2 0188h
18Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP23	0FC2 018Ch
190h	32	FSS_FSAS_OTFA_REGS_RIV20	0FC2 0190h
194h	32	FSS_FSAS_OTFA_REGS_RIV21	0FC2 0194h
198h	32	FSS_FSAS_OTFA_REGS_RIV22	0FC2 0198h
19Ch	32	FSS_FSAS_OTFA_REGS_RIV23	0FC2 019Ch
1A0h	32	FSS_FSAS_OTFA_REGS_RGCFG3	0FC2 01A0h
1A4h	32	FSS_FSAS_OTFA_REGS_RGMACST3	0FC2 01A4h
1A8h	32	FSS_FSAS_OTFA_REGS_RGST3	0FC2 01A8h
1ACh	32	FSS_FSAS_OTFA_REGS_RGSI3	0FC2 01ACh

Table 14-29018. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
1B0h	32	FSS_FSAS_OTFA_REGS_RKEYE30	0FC2 01B0h
1B4h	32	FSS_FSAS_OTFA_REGS_RKEYE31	0FC2 01B4h
1B8h	32	FSS_FSAS_OTFA_REGS_RKEYE32	0FC2 01B8h
1BCh	32	FSS_FSAS_OTFA_REGS_RKEYE33	0FC2 01BCh
1C0h	32	FSS_FSAS_OTFA_REGS_RKEYE34	0FC2 01C0h
1C4h	32	FSS_FSAS_OTFA_REGS_RKEYE35	0FC2 01C4h
1C8h	32	FSS_FSAS_OTFA_REGS_RKEYE36	0FC2 01C8h
1CCh	32	FSS_FSAS_OTFA_REGS_RKEYE37	0FC2 01CCh
1D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP30	0FC2 01D0h
1D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP31	0FC2 01D4h
1D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP32	0FC2 01D8h
1DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP33	0FC2 01DCh
1E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP34	0FC2 01E0h
1E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP35	0FC2 01E4h
1E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP36	0FC2 01E8h
1ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP37	0FC2 01ECh
1F0h	32	FSS_FSAS_OTFA_REGS_RKEYA30	0FC2 01F0h
1F4h	32	FSS_FSAS_OTFA_REGS_RKEYA31	0FC2 01F4h
1F8h	32	FSS_FSAS_OTFA_REGS_RKEYA32	0FC2 01F8h
1FCh	32	FSS_FSAS_OTFA_REGS_RKEYA33	0FC2 01FCh
200h	32	FSS_FSAS_OTFA_REGS_RKEYAP30	0FC2 0200h
204h	32	FSS_FSAS_OTFA_REGS_RKEYAP31	0FC2 0204h
208h	32	FSS_FSAS_OTFA_REGS_RKEYAP32	0FC2 0208h
20Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP33	0FC2 020Ch
210h	32	FSS_FSAS_OTFA_REGS_RIV30	0FC2 0210h
214h	32	FSS_FSAS_OTFA_REGS_RIV31	0FC2 0214h
218h	32	FSS_FSAS_OTFA_REGS_RIV32	0FC2 0218h
21Ch	32	FSS_FSAS_OTFA_REGS_RIV33	0FC2 021Ch
220h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO0	0FC2 0220h
224h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO1	0FC2 0224h
228h	32	FSS_FSAS_OTFA_REGS_MACCACHEINFO	0FC2 0228h
22Ch	32	FSS_FSAS_OTFA_REGS_RMWRMCNT	0FC2 022Ch

Table 14-29019. FSS_DAT_REG1 Registers, Base Address=6000 0000h, Length=134217728

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG1_HPB_DATA_MEM_J	6000 0000h + formula

Table 14-29020. FSS_DAT_REG0 Registers, Base Address=0004 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG0_HPB_DATA_MEM_J	0004 0000 0000h + formula

Table 14-29021. FSS_DAT_REG3 Registers, Base Address=0005 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG3_HPB_DATA_MEM_J	0005 0000 0000h + formula

14.9.4.2.2 FSS_FSAS_0 Registers

FSS_FSAS_0 Registers

14.9.4.2.2.1 FSS_FSAS_GENREGS_REVISION Register

1 FSS_FSAS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502101h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-29022. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h**

Figure 14-9617. FSS_FSAS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
6850h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
4h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-29024. FSS_FSAS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.2 FSS_FSAS_GENREGS_SYSCONFIG Register

1 FSS_FSAS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 0h]

Controls various parameters of the cotroller state.

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Table 14-29025. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC1 0004h

Figure 14-9618. FSS_FSAS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							OSPI_32B_DISABLE_MODE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	RESERVED	ECC_EN
R/W	R/W	NONE		R/W	R	NONE	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-29027. FSS_FSAS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled Reset Source: vbus_mod_g_rst_n
7	DISXIP	R/W	0h	0 XIP Prefetch Enabled. 1 XIP prefetch disabled Reset Source: vbus_mod_g_rst_n
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled Reset Source: vbus_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation Reset Source: vbus_mod_g_rst_n
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security Reset Source: vbus_mod_g_rst_n
1	RESERVED	NONE	0h	Reserved
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.3 FSS_FSAS_GENREGS_FRAG_ADR Register

1 FSS_FSAS_GENREGS_FRAG_ADR Register (Offset = 8h) [reset = 0h]

This FRAG_ADR is the address of a request that frag_hi or frag_lo boundary occurs

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Table 14-29028. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-9619. FSS_FSAS_GENREGS_FRAG_ADR Name Register

31	30	29	28	27	26	25	24
FRAG_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
FRAG_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
FRAG_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
FRAG_ADDR							
R/W							
0h							

Table 14-29030. FSS_FSAS_GENREGS_FRAG_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAG_ADDR	R/W	0h	This address is used to determine the boundary of frag_hi and flag_lo Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.4 FSS_FSAS_GENREGS_FRAG_CTL Register

1 FSS_FSAS_GENREGS_FRAG_CTL Register (Offset = Ch) [reset = 3h]

The FRAG_CTL determins which frag region is fragmented

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Table 14-29031. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 000Ch**

Figure 14-9620. FSS_FSAS_GENREGS_FRAG_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						FRAG_HI	FRAG_LO
NONE						R/W	R/W
0h						1h	1h

Table 14-29033. FSS_FSAS_GENREGS_FRAG_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	FRAG_HI	R/W	1h	When set any address greater than or equal to frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n
0	FRAG_LO	R/W	1h	When set any address less than frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.5 FSS_FSAS_GENREGS_IRQ_EOI Register

1 FSS_FSAS_GENREGS_IRQ_EOI Register (Offset = 0h) [reset = 0h]

The End of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the EOI for MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

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Table 14-29034. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC1 0000h

Figure 14-9621. FSS_FSAS_GENREGS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-29036. FSS_FSAS_GENREGS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	Write with bit position of targeted interrupt. (E.g. Ext FSS ECC is bit 0). Upon write, level interrupt will clear and if un-serviced will issue another pulse interrupt Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.6 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register

1 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register (Offset = 4h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-29037. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0004h**

Figure 14-9622. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-29039. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.7 FSS_FSAS_GENREGS_IRQ_STATUS Register

1 FSS_FSAS_GENREGS_IRQ_STATUS Register (Offset = 8h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-29040. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-9623. FSS_FSAS_GENREGS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-29042. FSS_FSAS_GENREGS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.8 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register

1 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register (Offset = Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-29043. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 000Ch**

Figure 14-9624. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-29045. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.9 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register

1 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register (Offset = 10h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-29046. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0010h**

Figure 14-9625. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-29048. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.10 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register

1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register (Offset = 0h + formula) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Offset = 30h + (j * 8h); where j = 0 to 3d

Table 14-29049. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h + formula**

Figure 14-9626. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 14-29051. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.11 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register

1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register (Offset = 4h + formula) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

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Offset = 34h + (j * 8h); where j = 0 to 3d

Table 14-29052. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC1 0004h + formula

Figure 14-9627. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE							
R/W							
0h							

Table 14-29054. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.12 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register

1 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 0h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

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Table 14-29055. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h**

Figure 14-9628. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

31	30	29	28	27	26	25	24
ECC_ERROR_BLOCK_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ERROR_BLOCK_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ERROR_BLOCK_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR			RESERVED				
R			NONE				
0h			0h				

Table 14-29057. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address Reset Source: vbus_mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.9.4.2.2.13 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register

1 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register (Offset = 4h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

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Table 14-29058. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC1 0004h

Figure 14-9629. FSS_FSAS_GENREGS_ERR_ECC_TYPE Name Register

31	30	29	28	27	26	25	24
ECC_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECC_ERR_ADR	ECC_ERR_MAC	ECC_ERR_DA1	ECC_ERR_DA0	ECC_ERR_DED	ECC_ERR_SEC
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-29060. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field Reset Source: vbus_mod_g_rst_n
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field Reset Source: vbus_mod_g_rst_n
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word Reset Source: vbus_mod_g_rst_n
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word Reset Source: vbus_mod_g_rst_n

Table 14-29060. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block Reset Source: vbus_mod_g_rst_n
0	ECC_ERR_SEC	R	0h	hen set indicates that there was a single error detected for the block Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.14 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register

1 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register (Offset = 8h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

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Table 14-29061. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-9630. FSS_FSAS_GENREGS_ERR_WRT_TYPE Name Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
NONE		R	R	R			
0h		0h	0h	0h			
7	6	5	4	3	2	1	0
WRT_ERR_ROUTEID							
R							
0h							

Table 14-29063. FSS_FSAS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables Reset Source: vbus_mod_g_rst_n
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address Reset Source: vbus_mod_g_rst_n
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Initiator that caused the write error Reset Source: vbus_mod_g_rst_n

14.9.4.2.2.15 FSS_FSAS_OTFA_REGS_REVID Register

1 FSS_FSAS_OTFA_REGS_REVID Register (Offset = 0h) [reset = 47500100h]

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Table 14-29064. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0000h**

Figure 14-9631. FSS_FSAS_OTFA_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REVID							
R							
47500100h							
23	22	21	20	19	18	17	16
REVID							
R							
47500100h							
15	14	13	12	11	10	9	8
REVID							
R							
47500100h							
7	6	5	4	3	2	1	0
REVID							
R							
47500100h							

Table 14-29066. FSS_FSAS_OTFA_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	47500100h	REVID Reset Source: rst_modg_rst_n

14.9.4.2.2.16 FSS_FSAS_OTFA_REGS_SCFG Register

1 FSS_FSAS_OTFA_REGS_SCFG Register (Offset = 4h) [reset = 2h]

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Table 14-29067. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0004h**

Figure 14-9632. FSS_FSAS_OTFA_REGS_SCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE_MODE	
NONE						R/W	
0h						2h	

Table 14-29069. FSS_FSAS_OTFA_REGS_SCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	IDLE_MODE	R/W	2h	IDLE MODE Reset Source: rst_modg_rst_n

14.9.4.2.2.17 FSS_FSAS_OTFA_REGS_ISR Register

1 FSS_FSAS_OTFA_REGS_ISR Register (Offset = 8h) [reset = 0h]

IRQSTATUS_RAW

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Table 14-29070. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0008h**

Figure 14-9633. FSS_FSAS_OTFA_REGS_ISR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-29072. FSS_FSAS_OTFA_REGS_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.4.2.2.18 FSS_FSAS_OTFA_REGS_IS Register

1 FSS_FSAS_OTFA_REGS_IS Register (Offset = Ch) [reset = 0h]

IRQSTATUS

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Table 14-29073. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 000Ch**

Figure 14-9634. FSS_FSAS_OTFA_REGS_IS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-29075. FSS_FSAS_OTFA_REGS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.4.2.2.19 FSS_FSAS_OTFA_REGS_IES Register

1 FSS_FSAS_OTFA_REGS_IES Register (Offset = 10h) [reset = 0h]

IRQENABLE_SET

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Table 14-29076. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0010h**

Figure 14-9635. FSS_FSAS_OTFA_REGS_IES Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29078. FSS_FSAS_OTFA_REGS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.4.2.2.20 FSS_FSAS_OTFA_REGS_IEC Register

1 FSS_FSAS_OTFA_REGS_IEC Register (Offset = 14h) [reset = 0h]

IRQENABLE_CLR

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Table 14-29079. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0014h**

Figure 14-9636. FSS_FSAS_OTFA_REGS_IEC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-29081. FSS_FSAS_OTFA_REGS_IEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.4.2.2.21 FSS_FSAS_OTFA_REGS_CCFG Register

1 FSS_FSAS_OTFA_REGS_CCFG Register (Offset = 18h) [reset = 0h]

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Table 14-29082. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0018h**

Figure 14-9637. FSS_FSAS_OTFA_REGS_CCFG Name Register

31	30	29	28	27	26	25	24
MASTER_EN_RD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ERROR_RESP_EN	OTFA_WAIT
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED	CACHE_ENABLE	CACHE_EVICT_MODE	KEY_SIZE	RD_WRT_OPT			
NONE	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-29084. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MASTER_EN_RD	R/W	0h	This register controls the enabling the functionality of this IP Disabled and Bypass mode active Reset Source: rst_modg_rst_n
30:10	RESERVED	NONE	0h	Reserved
9	ERROR_RESP_EN	R/W	0h	This register controls the enabling the the ocp error response for mac errors Reset Source: rst_modg_rst_n
8	OTFA_WAIT	R/W	0h	This register allows the ability to stop accepting any new transactions from getting accepted and allow the current transactions to complete Reset Source: rst_modg_rst_n
7	RESERVED	NONE	0h	Reserved
6	CACHE_ENABLE	R/W	0h	MAC cache enable Reset Source: rst_modg_rst_n
5	CACHE_EVICT_MODE	R/W	0h	cache evict mode Reset Source: rst_modg_rst_n
4	KEY_SIZE	R/W	0h	Key Size, 0 128 Bit 1 256 Bit Reset Source: rst_modg_rst_n

Table 14-29084. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RD_WRT_OPT	R/W	0h	This register defines the static allocation of the AES cores to read transactions. The remainder will be allocated to write transactions Reset Source: rst_modg_rst_n

14.9.4.2.2.22 FSS_FSAS_OTFA_REGS_CSTATUS Register

1 FSS_FSAS_OTFA_REGS_CSTATUS Register (Offset = 1Ch) [reset = 0h]

CryptoStatus

Return to Summary Table

Table 14-29085. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 001Ch

Figure 14-9638. FSS_FSAS_OTFA_REGS_CSTATUS Name Register

31	30	29	28	27	26	25	24
BUSY	CRYPTO_BUSY	RD_STALL_EVENT_CNT					
R	R	R/W1TC					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_STALL_EVENT_CNT							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_STALL_EVENT_CNT					
NONE		R/W1TC					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_STALL_EVENT_CNT							
R/W1TC							
0h							

Table 14-29087. FSS_FSAS_OTFA_REGS_CSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
30	CRYPTO_BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
29:16	RD_STALL_EVENT_CNT	R/W1TC	0h	rd stall event do to lack of eng Reset Source: rst_modg_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	WRT_STALL_EVENT_CNT	R/W1TC	0h	wrt stall event do to lack of eng Reset Source: rst_modg_rst_n

14.9.4.2.2.23 FSS_FSAS_OTFA_REGS_RGCFG0 Register

1 FSS_FSAS_OTFA_REGS_RGCFG0 Register (Offset = 20h) [reset = 0h]

RegionCfg0

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Table 14-29088. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0020h**

Figure 14-9639. FSS_FSAS_OTFA_REGS_RGCFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT0	MAC_MODE0		AES_MODE0	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-29090. FSS_FSAS_OTFA_REGS_RGCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT0	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE0	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE0	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.4.2.2.24 FSS_FSAS_OTFA_REGS_RGMACST0 Register

1 FSS_FSAS_OTFA_REGS_RGMACST0 Register (Offset = 24h) [reset = 0h]

RegionMacStart0

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Table 14-29091. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0024h**

Figure 14-9640. FSS_FSAS_OTFA_REGS_RGMACST0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">M_START0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M_START0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M_START0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29093. FSS_FSAS_OTFA_REGS_RGMACST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START0	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.25 FSS_FSAS_OTFA_REGS_RGST0 Register

1 FSS_FSAS_OTFA_REGS_RGST0 Register (Offset = 28h) [reset = 0h]

RegionStart0

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Table 14-29094. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0028h**

Figure 14-9641. FSS_FSAS_OTFA_REGS_RGST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START0							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START0							
R/W							
0h							

Table 14-29096. FSS_FSAS_OTFA_REGS_RGST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START0	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.26 FSS_FSAS_OTFA_REGS_RGSI0 Register

1 FSS_FSAS_OTFA_REGS_RGSI0 Register (Offset = 2Ch) [reset = 0h]

RegionSize0

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Table 14-29097. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 002Ch**

Figure 14-9642. FSS_FSAS_OTFA_REGS_RGSI0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_SIZE0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_SIZE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_SIZE0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29099. FSS_FSAS_OTFA_REGS_RGSI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE0	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.27 FSS_FSAS_OTFA_REGS_RKEYE00 Register

1 FSS_FSAS_OTFA_REGS_RKEYE00 Register (Offset = 30h) [reset = 0h]

RegionKeyE00

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Table 14-29100. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0030h**

Figure 14-9643. FSS_FSAS_OTFA_REGS_RKEYE00 Name Register

31	30	29	28	27	26	25	24
R_KEY_E00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E00							
R/W							
0h							

Table 14-29102. FSS_FSAS_OTFA_REGS_RKEYE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E00	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.28 FSS_FSAS_OTFA_REGS_RKEYE01 Register

1 FSS_FSAS_OTFA_REGS_RKEYE01 Register (Offset = 34h) [reset = 0h]

RegionKeyE01

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Table 14-29103. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0034h**

Figure 14-9644. FSS_FSAS_OTFA_REGS_RKEYE01 Name Register

31	30	29	28	27	26	25	24
R_KEY_E01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E01							
R/W							
0h							

Table 14-29105. FSS_FSAS_OTFA_REGS_RKEYE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E01	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.29 FSS_FSAS_OTFA_REGS_RKEYE02 Register

1 FSS_FSAS_OTFA_REGS_RKEYE02 Register (Offset = 38h) [reset = 0h]

RegionKeyE02

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Table 14-29106. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0038h**

Figure 14-9645. FSS_FSAS_OTFA_REGS_RKEYE02 Name Register

31	30	29	28	27	26	25	24
R_KEY_E02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E02							
R/W							
0h							

Table 14-29108. FSS_FSAS_OTFA_REGS_RKEYE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E02	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.30 FSS_FSAS_OTFA_REGS_RKEYE03 Register

1 FSS_FSAS_OTFA_REGS_RKEYE03 Register (Offset = 3Ch) [reset = 0h]

RegionKeyE03

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Table 14-29109. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 003Ch**

Figure 14-9646. FSS_FSAS_OTFA_REGS_RKEYE03 Name Register

31	30	29	28	27	26	25	24
R_KEY_E03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E03							
R/W							
0h							

Table 14-29111. FSS_FSAS_OTFA_REGS_RKEYE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E03	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.31 FSS_FSAS_OTFA_REGS_RKEYE04 Register

1 FSS_FSAS_OTFA_REGS_RKEYE04 Register (Offset = 40h) [reset = 0h]

RegionKeyE04

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Table 14-29112. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0040h**

Figure 14-9647. FSS_FSAS_OTFA_REGS_RKEYE04 Name Register

31	30	29	28	27	26	25	24
R_KEY_E04							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E04							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E04							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E04							
R/W							
0h							

Table 14-29114. FSS_FSAS_OTFA_REGS_RKEYE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E04	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.32 FSS_FSAS_OTFA_REGS_RKEYE05 Register

1 FSS_FSAS_OTFA_REGS_RKEYE05 Register (Offset = 44h) [reset = 0h]

RegionKeyE05

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Table 14-29115. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0044h**

Figure 14-9648. FSS_FSAS_OTFA_REGS_RKEYE05 Name Register

31	30	29	28	27	26	25	24
R_KEY_E05							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E05							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E05							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E05							
R/W							
0h							

Table 14-29117. FSS_FSAS_OTFA_REGS_RKEYE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E05	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.33 FSS_FSAS_OTFA_REGS_RKEYE06 Register

1 FSS_FSAS_OTFA_REGS_RKEYE06 Register (Offset = 48h) [reset = 0h]

RegionKeyE06

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Table 14-29118. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0048h**

Figure 14-9649. FSS_FSAS_OTFA_REGS_RKEYE06 Name Register

31	30	29	28	27	26	25	24
R_KEY_E06							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E06							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E06							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E06							
R/W							
0h							

Table 14-29120. FSS_FSAS_OTFA_REGS_RKEYE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E06	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.34 FSS_FSAS_OTFA_REGS_RKEYE07 Register

1 FSS_FSAS_OTFA_REGS_RKEYE07 Register (Offset = 4Ch) [reset = 0h]

RegionKeyE07

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Table 14-29121. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 004Ch**

Figure 14-9650. FSS_FSAS_OTFA_REGS_RKEYE07 Name Register

31	30	29	28	27	26	25	24
R_KEY_E07							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E07							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E07							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E07							
R/W							
0h							

Table 14-29123. FSS_FSAS_OTFA_REGS_RKEYE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E07	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.35 FSS_FSAS_OTFA_REGS_RKEYEP00 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP00 Register (Offset = 50h) [reset = 0h]

RegionKeyEP00

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Table 14-29124. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0050h**

Figure 14-9651. FSS_FSAS_OTFA_REGS_RKEYEP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP00							
R/W							
0h							

Table 14-29126. FSS_FSAS_OTFA_REGS_RKEYEP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP00	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.36 FSS_FSAS_OTFA_REGS_RKEYEP01 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP01 Register (Offset = 54h) [reset = 0h]

RegionKeyEP01

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Table 14-29127. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0054h**

Figure 14-9652. FSS_FSAS_OTFA_REGS_RKEYEP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP01							
R/W							
0h							

Table 14-29129. FSS_FSAS_OTFA_REGS_RKEYEP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP01	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.37 FSS_FSAS_OTFA_REGS_RKEYEP02 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP02 Register (Offset = 58h) [reset = 0h]

RegionKeyEP02

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Table 14-29130. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0058h**

Figure 14-9653. FSS_FSAS_OTFA_REGS_RKEYEP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP02							
R/W							
0h							

Table 14-29132. FSS_FSAS_OTFA_REGS_RKEYEP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP02	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.38 FSS_FSAS_OTFA_REGS_RKEYEP03 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP03 Register (Offset = 5Ch) [reset = 0h]

RegionKeyEP03

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Table 14-29133. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 005Ch**

Figure 14-9654. FSS_FSAS_OTFA_REGS_RKEYEP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP03							
R/W							
0h							

Table 14-29135. FSS_FSAS_OTFA_REGS_RKEYEP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP03	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.39 FSS_FSAS_OTFA_REGS_RKEYEP04 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP04 Register (Offset = 60h) [reset = 0h]

RegionKeyEP04

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Table 14-29136. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0060h**

Figure 14-9655. FSS_FSAS_OTFA_REGS_RKEYEP04 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP04							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP04							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP04							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP04							
R/W							
0h							

Table 14-29138. FSS_FSAS_OTFA_REGS_RKEYEP04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP04	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.40 FSS_FSAS_OTFA_REGS_RKEYEP05 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP05 Register (Offset = 64h) [reset = 0h]

RegionKeyEP05

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Table 14-29139. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 0064h**

Figure 14-9656. FSS_FSAS_OTFA_REGS_RKEYEP05 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP05							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP05							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP05							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP05							
R/W							
0h							

Table 14-29141. FSS_FSAS_OTFA_REGS_RKEYEP05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP05	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.41 FSS_FSAS_OTFA_REGS_RKEYEP06 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP06 Register (Offset = 68h) [reset = 0h]

RegionKeyEP06

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Table 14-29142. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0068h**

Figure 14-9657. FSS_FSAS_OTFA_REGS_RKEYEP06 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP06							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP06							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP06							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP06							
R/W							
0h							

Table 14-29144. FSS_FSAS_OTFA_REGS_RKEYEP06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP06	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.42 FSS_FSAS_OTFA_REGS_RKEYEP07 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP07 Register (Offset = 6Ch) [reset = 0h]

RegionKeyEP07

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Table 14-29145. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 006Ch**

Figure 14-9658. FSS_FSAS_OTFA_REGS_RKEYEP07 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP07							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP07							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP07							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP07							
R/W							
0h							

Table 14-29147. FSS_FSAS_OTFA_REGS_RKEYEP07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP07	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.43 FSS_FSAS_OTFA_REGS_RKEYA00 Register

1 FSS_FSAS_OTFA_REGS_RKEYA00 Register (Offset = 70h) [reset = 0h]

RegionKeyA00

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Table 14-29148. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0070h**

Figure 14-9659. FSS_FSAS_OTFA_REGS_RKEYA00 Name Register

31	30	29	28	27	26	25	24
R_KEY_A00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A00							
R/W							
0h							

Table 14-29150. FSS_FSAS_OTFA_REGS_RKEYA00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A00	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.44 FSS_FSAS_OTFA_REGS_RKEYA01 Register

1 FSS_FSAS_OTFA_REGS_RKEYA01 Register (Offset = 74h) [reset = 0h]

RegionKeyA01

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Table 14-29151. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0074h**

Figure 14-9660. FSS_FSAS_OTFA_REGS_RKEYA01 Name Register

31	30	29	28	27	26	25	24
R_KEY_A01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A01							
R/W							
0h							

Table 14-29153. FSS_FSAS_OTFA_REGS_RKEYA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A01	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.45 FSS_FSAS_OTFA_REGS_RKEYA02 Register

1 FSS_FSAS_OTFA_REGS_RKEYA02 Register (Offset = 78h) [reset = 0h]

RegionKeyA02

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Table 14-29154. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0078h**

Figure 14-9661. FSS_FSAS_OTFA_REGS_RKEYA02 Name Register

31	30	29	28	27	26	25	24
R_KEY_A02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A02							
R/W							
0h							

Table 14-29156. FSS_FSAS_OTFA_REGS_RKEYA02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A02	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.46 FSS_FSAS_OTFA_REGS_RKEYA03 Register

1 FSS_FSAS_OTFA_REGS_RKEYA03 Register (Offset = 7Ch) [reset = 0h]

RegionKeyA03

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Table 14-29157. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 007Ch**

Figure 14-9662. FSS_FSAS_OTFA_REGS_RKEYA03 Name Register

31	30	29	28	27	26	25	24
R_KEY_A03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A03							
R/W							
0h							

Table 14-29159. FSS_FSAS_OTFA_REGS_RKEYA03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A03	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.47 FSS_FSAS_OTFA_REGS_RKEYAP00 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP00 Register (Offset = 80h) [reset = 0h]

RegionKeyAP00

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Table 14-29160. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0080h**

Figure 14-9663. FSS_FSAS_OTFA_REGS_RKEYAP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP00							
R/W							
0h							

Table 14-29162. FSS_FSAS_OTFA_REGS_RKEYAP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP00	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.48 FSS_FSAS_OTFA_REGS_RKEYAP01 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP01 Register (Offset = 84h) [reset = 0h]

RegionKeyAP01

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Table 14-29163. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0084h**

Figure 14-9664. FSS_FSAS_OTFA_REGS_RKEYAP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP01							
R/W							
0h							

Table 14-29165. FSS_FSAS_OTFA_REGS_RKEYAP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP01	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.49 FSS_FSAS_OTFA_REGS_RKEYAP02 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP02 Register (Offset = 88h) [reset = 0h]

RegionKeyAP02

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Table 14-29166. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0088h**

Figure 14-9665. FSS_FSAS_OTFA_REGS_RKEYAP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP02							
R/W							
0h							

Table 14-29168. FSS_FSAS_OTFA_REGS_RKEYAP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP02	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.50 FSS_FSAS_OTFA_REGS_RKEYAP03 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP03 Register (Offset = 8Ch) [reset = 0h]

RegionKeyAP03

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Table 14-29169. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 008Ch**

Figure 14-9666. FSS_FSAS_OTFA_REGS_RKEYAP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP03							
R/W							
0h							

Table 14-29171. FSS_FSAS_OTFA_REGS_RKEYAP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP03	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.51 FSS_FSAS_OTFA_REGS_RIV00 Register

1 FSS_FSAS_OTFA_REGS_RIV00 Register (Offset = 90h) [reset = 0h]

RegionIV00

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Table 14-29172. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0090h**

Figure 14-9667. FSS_FSAS_OTFA_REGS_RIV00 Name Register

31	30	29	28	27	26	25	24
R_IV00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV00							
R/W							
0h							

Table 14-29174. FSS_FSAS_OTFA_REGS_RIV00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV00	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.52 FSS_FSAS_OTFA_REGS_RIV01 Register

1 FSS_FSAS_OTFA_REGS_RIV01 Register (Offset = 94h) [reset = 0h]

RegionIV01

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Table 14-29175. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0094h**

Figure 14-9668. FSS_FSAS_OTFA_REGS_RIV01 Name Register

31	30	29	28	27	26	25	24
R_IV01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV01							
R/W							
0h							

Table 14-29177. FSS_FSAS_OTFA_REGS_RIV01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV01	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.53 FSS_FSAS_OTFA_REGS_RIV02 Register

1 FSS_FSAS_OTFA_REGS_RIV02 Register (Offset = 98h) [reset = 0h]

RegionIV02

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Table 14-29178. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0098h**

Figure 14-9669. FSS_FSAS_OTFA_REGS_RIV02 Name Register

31	30	29	28	27	26	25	24
R_IV02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV02							
R/W							
0h							

Table 14-29180. FSS_FSAS_OTFA_REGS_RIV02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV02	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.54 FSS_FSAS_OTFA_REGS_RIV03 Register

1 FSS_FSAS_OTFA_REGS_RIV03 Register (Offset = 9Ch) [reset = 0h]

RegionIV03

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Table 14-29181. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 009Ch**

Figure 14-9670. FSS_FSAS_OTFA_REGS_RIV03 Name Register

31	30	29	28	27	26	25	24
R_IV03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV03							
R/W							
0h							

Table 14-29183. FSS_FSAS_OTFA_REGS_RIV03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV03	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.55 FSS_FSAS_OTFA_REGS_RGCFG1 Register

1 FSS_FSAS_OTFA_REGS_RGCFG1 Register (Offset = A0h) [reset = 0h]

RegionCfg1

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Table 14-29184. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00A0h**

Figure 14-9671. FSS_FSAS_OTFA_REGS_RGCFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT1	MAC_MODE1		AES_MODE1	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-29186. FSS_FSAS_OTFA_REGS_RGCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT1	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE1	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE1	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.4.2.2.56 FSS_FSAS_OTFA_REGS_RGMACST1 Register

1 FSS_FSAS_OTFA_REGS_RGMACST1 Register (Offset = A4h) [reset = 0h]

RegionMacStart1

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Table 14-29187. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00A4h**

Figure 14-9672. FSS_FSAS_OTFA_REGS_RGMACST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START1							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START1							
R/W							
0h							

Table 14-29189. FSS_FSAS_OTFA_REGS_RGMACST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START1	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.57 FSS_FSAS_OTFA_REGS_RGST1 Register

1 FSS_FSAS_OTFA_REGS_RGST1 Register (Offset = A8h) [reset = 0h]

RegionStart1

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Table 14-29190. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00A8h**

Figure 14-9673. FSS_FSAS_OTFA_REGS_RGST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START1							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START1							
R/W							
0h							

Table 14-29192. FSS_FSAS_OTFA_REGS_RGST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START1	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.58 FSS_FSAS_OTFA_REGS_RGSI1 Register

1 FSS_FSAS_OTFA_REGS_RGSI1 Register (Offset = ACh) [reset = 0h]

RegionSize1

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Table 14-29193. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00ACh**

Figure 14-9674. FSS_FSAS_OTFA_REGS_RGSI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE1							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE1							
R/W							
0h							

Table 14-29195. FSS_FSAS_OTFA_REGS_RGSI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE1	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.59 FSS_FSAS_OTFA_REGS_RKEYE10 Register

1 FSS_FSAS_OTFA_REGS_RKEYE10 Register (Offset = B0h) [reset = 0h]

RegionKeyE10

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Table 14-29196. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B0h**

Figure 14-9675. FSS_FSAS_OTFA_REGS_RKEYE10 Name Register

31	30	29	28	27	26	25	24
R_KEY_E10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E10							
R/W							
0h							

Table 14-29198. FSS_FSAS_OTFA_REGS_RKEYE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E10	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.60 FSS_FSAS_OTFA_REGS_RKEYE11 Register

1 FSS_FSAS_OTFA_REGS_RKEYE11 Register (Offset = B4h) [reset = 0h]

RegionKeyE11

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Table 14-29199. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B4h**

Figure 14-9676. FSS_FSAS_OTFA_REGS_RKEYE11 Name Register

31	30	29	28	27	26	25	24
R_KEY_E11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E11							
R/W							
0h							

Table 14-29201. FSS_FSAS_OTFA_REGS_RKEYE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E11	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.61 FSS_FSAS_OTFA_REGS_RKEYE12 Register

1 FSS_FSAS_OTFA_REGS_RKEYE12 Register (Offset = B8h) [reset = 0h]

RegionKeyE12

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Table 14-29202. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B8h**

Figure 14-9677. FSS_FSAS_OTFA_REGS_RKEYE12 Name Register

31	30	29	28	27	26	25	24
R_KEY_E12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E12							
R/W							
0h							

Table 14-29204. FSS_FSAS_OTFA_REGS_RKEYE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E12	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.62 FSS_FSAS_OTFA_REGS_RKEYE13 Register

1 FSS_FSAS_OTFA_REGS_RKEYE13 Register (Offset = BCh) [reset = 0h]

RegionKeyE13

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Table 14-29205. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 00BCh**

Figure 14-9678. FSS_FSAS_OTFA_REGS_RKEYE13 Name Register

31	30	29	28	27	26	25	24
R_KEY_E13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E13							
R/W							
0h							

Table 14-29207. FSS_FSAS_OTFA_REGS_RKEYE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E13	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.63 FSS_FSAS_OTFA_REGS_RKEYE14 Register

1 FSS_FSAS_OTFA_REGS_RKEYE14 Register (Offset = C0h) [reset = 0h]

RegionKeyE14

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Table 14-29208. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C0h**

Figure 14-9679. FSS_FSAS_OTFA_REGS_RKEYE14 Name Register

31	30	29	28	27	26	25	24
R_KEY_E14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E14							
R/W							
0h							

Table 14-29210. FSS_FSAS_OTFA_REGS_RKEYE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E14	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.64 FSS_FSAS_OTFA_REGS_RKEYE15 Register

1 FSS_FSAS_OTFA_REGS_RKEYE15 Register (Offset = C4h) [reset = 0h]

RegionKeyE15

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Table 14-29211. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C4h**

Figure 14-9680. FSS_FSAS_OTFA_REGS_RKEYE15 Name Register

31	30	29	28	27	26	25	24
R_KEY_E15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E15							
R/W							
0h							

Table 14-29213. FSS_FSAS_OTFA_REGS_RKEYE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E15	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.65 FSS_FSAS_OTFA_REGS_RKEYE16 Register

1 FSS_FSAS_OTFA_REGS_RKEYE16 Register (Offset = C8h) [reset = 0h]

RegionKeyE16

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Table 14-29214. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C8h**

Figure 14-9681. FSS_FSAS_OTFA_REGS_RKEYE16 Name Register

31	30	29	28	27	26	25	24
R_KEY_E16							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E16							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E16							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E16							
R/W							
0h							

Table 14-29216. FSS_FSAS_OTFA_REGS_RKEYE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E16	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.66 FSS_FSAS_OTFA_REGS_RKEYE17 Register

1 FSS_FSAS_OTFA_REGS_RKEYE17 Register (Offset = CCh) [reset = 0h]

RegionKeyE17

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Table 14-29217. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00CCh**

Figure 14-9682. FSS_FSAS_OTFA_REGS_RKEYE17 Name Register

31	30	29	28	27	26	25	24
R_KEY_E17							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E17							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E17							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E17							
R/W							
0h							

Table 14-29219. FSS_FSAS_OTFA_REGS_RKEYE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E17	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.67 FSS_FSAS_OTFA_REGS_RKEYEP10 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP10 Register (Offset = D0h) [reset = 0h]

RegionKeyEP10

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Table 14-29220. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D0h**

Figure 14-9683. FSS_FSAS_OTFA_REGS_RKEYEP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP10							
R/W							
0h							

Table 14-29222. FSS_FSAS_OTFA_REGS_RKEYEP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP10	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.68 FSS_FSAS_OTFA_REGS_RKEYEP11 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP11 Register (Offset = D4h) [reset = 0h]

RegionKeyEP11

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Table 14-29223. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D4h**

Figure 14-9684. FSS_FSAS_OTFA_REGS_RKEYEP11 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP11							
R/W							
0h							

Table 14-29225. FSS_FSAS_OTFA_REGS_RKEYEP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP11	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.69 FSS_FSAS_OTFA_REGS_RKEYEP12 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP12 Register (Offset = D8h) [reset = 0h]

RegionKeyEP12

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Table 14-29226. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D8h**

Figure 14-9685. FSS_FSAS_OTFA_REGS_RKEYEP12 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_EP12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_EP12							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_EP12							
R/W							
0h							

Table 14-29228. FSS_FSAS_OTFA_REGS_RKEYEP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP12	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.70 FSS_FSAS_OTFA_REGS_RKEYEP13 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP13 Register (Offset = DCh) [reset = 0h]

RegionKeyEP13

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Table 14-29229. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 00DCh

Figure 14-9686. FSS_FSAS_OTFA_REGS_RKEYEP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP13							
R/W							
0h							

Table 14-29231. FSS_FSAS_OTFA_REGS_RKEYEP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP13	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.71 FSS_FSAS_OTFA_REGS_RKEYEP14 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP14 Register (Offset = E0h) [reset = 0h]

RegionKeyEP14

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Table 14-29232. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00E0h**

Figure 14-9687. FSS_FSAS_OTFA_REGS_RKEYEP14 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP14							
R/W							
0h							

Table 14-29234. FSS_FSAS_OTFA_REGS_RKEYEP14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP14	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.72 FSS_FSAS_OTFA_REGS_RKEYEP15 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP15 Register (Offset = E4h) [reset = 0h]

RegionKeyEP15

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Table 14-29235. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00E4h**

Figure 14-9688. FSS_FSAS_OTFA_REGS_RKEYEP15 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP15							
R/W							
0h							

Table 14-29237. FSS_FSAS_OTFA_REGS_RKEYEP15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP15	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.73 FSS_FSAS_OTFA_REGS_RKEYEP16 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP16 Register (Offset = E8h) [reset = 0h]

RegionKeyEP16

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Table 14-29238. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 00E8h

Figure 14-9689. FSS_FSAS_OTFA_REGS_RKEYEP16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29240. FSS_FSAS_OTFA_REGS_RKEYEP16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP16	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.74 FSS_FSAS_OTFA_REGS_RKEYEP17 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP17 Register (Offset = ECh) [reset = 0h]

RegionKeyEP17

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Table 14-29241. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 00ECh**

Figure 14-9690. FSS_FSAS_OTFA_REGS_RKEYEP17 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP17							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP17							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP17							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP17							
R/W							
0h							

Table 14-29243. FSS_FSAS_OTFA_REGS_RKEYEP17 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	R_KEY_EP17	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.75 FSS_FSAS_OTFA_REGS_RKEYA10 Register

1 FSS_FSAS_OTFA_REGS_RKEYA10 Register (Offset = F0h) [reset = 0h]

RegionKeyA10

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Table 14-29244. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00F0h**

Figure 14-9691. FSS_FSAS_OTFA_REGS_RKEYA10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29246. FSS_FSAS_OTFA_REGS_RKEYA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A10	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.76 FSS_FSAS_OTFA_REGS_RKEYA11 Register

1 FSS_FSAS_OTFA_REGS_RKEYA11 Register (Offset = F4h) [reset = 0h]

RegionKeyA11

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Table 14-29247. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00F4h**

Figure 14-9692. FSS_FSAS_OTFA_REGS_RKEYA11 Name Register

31	30	29	28	27	26	25	24
R_KEY_A11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A11							
R/W							
0h							

Table 14-29249. FSS_FSAS_OTFA_REGS_RKEYA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A11	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.77 FSS_FSAS_OTFA_REGS_RKEYA12 Register

1 FSS_FSAS_OTFA_REGS_RKEYA12 Register (Offset = F8h) [reset = 0h]

RegionKeyA12

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Table 14-29250. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00F8h**

Figure 14-9693. FSS_FSAS_OTFA_REGS_RKEYA12 Name Register

31	30	29	28	27	26	25	24
R_KEY_A12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_A12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_A12							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_A12							
R/W							
0h							

Table 14-29252. FSS_FSAS_OTFA_REGS_RKEYA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A12	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.78 FSS_FSAS_OTFA_REGS_RKEYA13 Register

1 FSS_FSAS_OTFA_REGS_RKEYA13 Register (Offset = FCh) [reset = 0h]

RegionKeyA13

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Table 14-29253. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00FCh**

Figure 14-9694. FSS_FSAS_OTFA_REGS_RKEYA13 Name Register

31	30	29	28	27	26	25	24
R_KEY_A13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A13							
R/W							
0h							

Table 14-29255. FSS_FSAS_OTFA_REGS_RKEYA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A13	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.79 FSS_FSAS_OTFA_REGS_RKEYAP10 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP10 Register (Offset = 100h) [reset = 0h]

RegionKeyAP10

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Table 14-29256. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 0100h**

Figure 14-9695. FSS_FSAS_OTFA_REGS_RKEYAP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP10							
R/W							
0h							

Table 14-29258. FSS_FSAS_OTFA_REGS_RKEYAP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP10	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.80 FSS_FSAS_OTFA_REGS_RKEYAP11 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP11 Register (Offset = 104h) [reset = 0h]

RegionKeyAP11

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Table 14-29259. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0104h**

Figure 14-9696. FSS_FSAS_OTFA_REGS_RKEYAP11 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP11							
R/W							
0h							

Table 14-29261. FSS_FSAS_OTFA_REGS_RKEYAP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP11	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.81 FSS_FSAS_OTFA_REGS_RKEYAP12 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP12 Register (Offset = 108h) [reset = 0h]

RegionKeyAP12

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Table 14-29262. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0108h**

Figure 14-9697. FSS_FSAS_OTFA_REGS_RKEYAP12 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP12							
R/W							
0h							

Table 14-29264. FSS_FSAS_OTFA_REGS_RKEYAP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP12	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.82 FSS_FSAS_OTFA_REGS_RKEYAP13 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP13 Register (Offset = 10Ch) [reset = 0h]

RegionKeyAP13

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Table 14-29265. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 010Ch**

Figure 14-9698. FSS_FSAS_OTFA_REGS_RKEYAP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP13							
R/W							
0h							

Table 14-29267. FSS_FSAS_OTFA_REGS_RKEYAP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP13	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.83 FSS_FSAS_OTFA_REGS_RIV10 Register

1 FSS_FSAS_OTFA_REGS_RIV10 Register (Offset = 110h) [reset = 0h]

RegionIV10

Return to Summary Table

Table 14-29268. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0110h**

Figure 14-9699. FSS_FSAS_OTFA_REGS_RIV10 Name Register

31	30	29	28	27	26	25	24
R_IV10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV10							
R/W							
0h							

Table 14-29270. FSS_FSAS_OTFA_REGS_RIV10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV10	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.84 FSS_FSAS_OTFA_REGS_RIV11 Register

1 FSS_FSAS_OTFA_REGS_RIV11 Register (Offset = 114h) [reset = 0h]

RegionIV11

Return to Summary Table

Table 14-29271. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0114h**

Figure 14-9700. FSS_FSAS_OTFA_REGS_RIV11 Name Register

31	30	29	28	27	26	25	24
R_IV11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV11							
R/W							
0h							

Table 14-29273. FSS_FSAS_OTFA_REGS_RIV11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV11	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.85 FSS_FSAS_OTFA_REGS_RIV12 Register

1 FSS_FSAS_OTFA_REGS_RIV12 Register (Offset = 118h) [reset = 0h]

RegionIV12

Return to Summary Table

Table 14-29274. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0118h**

Figure 14-9701. FSS_FSAS_OTFA_REGS_RIV12 Name Register

31	30	29	28	27	26	25	24
R_IV12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV12							
R/W							
0h							

Table 14-29276. FSS_FSAS_OTFA_REGS_RIV12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV12	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.86 FSS_FSAS_OTFA_REGS_RIV13 Register

1 FSS_FSAS_OTFA_REGS_RIV13 Register (Offset = 11Ch) [reset = 0h]

RegionIV13

Return to Summary Table

Table 14-29277. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 011Ch**

Figure 14-9702. FSS_FSAS_OTFA_REGS_RIV13 Name Register

31	30	29	28	27	26	25	24
R_IV13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV13							
R/W							
0h							

Table 14-29279. FSS_FSAS_OTFA_REGS_RIV13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV13	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.87 FSS_FSAS_OTFA_REGS_RGCFG2 Register

1 FSS_FSAS_OTFA_REGS_RGCFG2 Register (Offset = 120h) [reset = 0h]

RegionCfg2

Return to Summary Table

Table 14-29280. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0120h**

Figure 14-9703. FSS_FSAS_OTFA_REGS_RGCFG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>WRT_PROTECT2</td><td colspan="2">MAC_MODE2</td><td colspan="2">AES_MODE2</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-29282. FSS_FSAS_OTFA_REGS_RGCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT2	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE2	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE2	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.4.2.2.88 FSS_FSAS_OTFA_REGS_RGMACST2 Register

1 FSS_FSAS_OTFA_REGS_RGMACST2 Register (Offset = 124h) [reset = 0h]

RegionMacStart2

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Table 14-29283. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0124h**

Figure 14-9704. FSS_FSAS_OTFA_REGS_RGMACST2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">M_START2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29285. FSS_FSAS_OTFA_REGS_RGMACST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START2	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.89 FSS_FSAS_OTFA_REGS_RGST2 Register

1 FSS_FSAS_OTFA_REGS_RGST2 Register (Offset = 128h) [reset = 0h]

RegionStart2

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Table 14-29286. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0128h**

Figure 14-9705. FSS_FSAS_OTFA_REGS_RGST2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START2							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START2							
R/W							
0h							

Table 14-29288. FSS_FSAS_OTFA_REGS_RGST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START2	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.90 FSS_FSAS_OTFA_REGS_RGSI2 Register

1 FSS_FSAS_OTFA_REGS_RGSI2 Register (Offset = 12Ch) [reset = 0h]

RegionSize2

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Table 14-29289. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 012Ch**

Figure 14-9706. FSS_FSAS_OTFA_REGS_RGSI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE2							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE2							
R/W							
0h							

Table 14-29291. FSS_FSAS_OTFA_REGS_RGSI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE2	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.91 FSS_FSAS_OTFA_REGS_RKEYE20 Register

1 FSS_FSAS_OTFA_REGS_RKEYE20 Register (Offset = 130h) [reset = 0h]

RegionKeyE20

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Table 14-29292. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0130h**

Figure 14-9707. FSS_FSAS_OTFA_REGS_RKEYE20 Name Register

31	30	29	28	27	26	25	24
R_KEY_E20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E20							
R/W							
0h							

Table 14-29294. FSS_FSAS_OTFA_REGS_RKEYE20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E20	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.92 FSS_FSAS_OTFA_REGS_RKEYE21 Register

1 FSS_FSAS_OTFA_REGS_RKEYE21 Register (Offset = 134h) [reset = 0h]

RegionKeyE21

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Table 14-29295. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0134h**

Figure 14-9708. FSS_FSAS_OTFA_REGS_RKEYE21 Name Register

31	30	29	28	27	26	25	24
R_KEY_E21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E21							
R/W							
0h							

Table 14-29297. FSS_FSAS_OTFA_REGS_RKEYE21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E21	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.93 FSS_FSAS_OTFA_REGS_RKEYE22 Register

1 FSS_FSAS_OTFA_REGS_RKEYE22 Register (Offset = 138h) [reset = 0h]

RegionKeyE22

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Table 14-29298. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0138h**

Figure 14-9709. FSS_FSAS_OTFA_REGS_RKEYE22 Name Register

31	30	29	28	27	26	25	24
R_KEY_E22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E22							
R/W							
0h							

Table 14-29300. FSS_FSAS_OTFA_REGS_RKEYE22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E22	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.94 FSS_FSAS_OTFA_REGS_RKEYE23 Register

1 FSS_FSAS_OTFA_REGS_RKEYE23 Register (Offset = 13Ch) [reset = 0h]

RegionKeyE23

Return to Summary Table

Table 14-29301. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 013Ch**

Figure 14-9710. FSS_FSAS_OTFA_REGS_RKEYE23 Name Register

31	30	29	28	27	26	25	24
R_KEY_E23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E23							
R/W							
0h							

Table 14-29303. FSS_FSAS_OTFA_REGS_RKEYE23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E23	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.95 FSS_FSAS_OTFA_REGS_RKEYE24 Register

1 FSS_FSAS_OTFA_REGS_RKEYE24 Register (Offset = 140h) [reset = 0h]

RegionKeyE24

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Table 14-29304. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0140h**

Figure 14-9711. FSS_FSAS_OTFA_REGS_RKEYE24 Name Register

31	30	29	28	27	26	25	24
R_KEY_E24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E24							
R/W							
0h							

Table 14-29306. FSS_FSAS_OTFA_REGS_RKEYE24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E24	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.96 FSS_FSAS_OTFA_REGS_RKEYE25 Register

1 FSS_FSAS_OTFA_REGS_RKEYE25 Register (Offset = 144h) [reset = 0h]

RegionKeyE25

Return to Summary Table

Table 14-29307. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0144h**

Figure 14-9712. FSS_FSAS_OTFA_REGS_RKEYE25 Name Register

31	30	29	28	27	26	25	24
R_KEY_E25							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E25							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E25							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E25							
R/W							
0h							

Table 14-29309. FSS_FSAS_OTFA_REGS_RKEYE25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E25	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.97 FSS_FSAS_OTFA_REGS_RKEYE26 Register

1 FSS_FSAS_OTFA_REGS_RKEYE26 Register (Offset = 148h) [reset = 0h]

RegionKeyE26

Return to Summary Table

Table 14-29310. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0148h

Figure 14-9713. FSS_FSAS_OTFA_REGS_RKEYE26 Name Register

31	30	29	28	27	26	25	24
R_KEY_E26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E26							
R/W							
0h							

Table 14-29312. FSS_FSAS_OTFA_REGS_RKEYE26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E26	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.98 FSS_FSAS_OTFA_REGS_RKEYE27 Register

1 FSS_FSAS_OTFA_REGS_RKEYE27 Register (Offset = 14Ch) [reset = 0h]

RegionKeyE27

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Table 14-29313. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 014Ch**

Figure 14-9714. FSS_FSAS_OTFA_REGS_RKEYE27 Name Register

31	30	29	28	27	26	25	24
R_KEY_E27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E27							
R/W							
0h							

Table 14-29315. FSS_FSAS_OTFA_REGS_RKEYE27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E27	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.99 FSS_FSAS_OTFA_REGS_RKEYEP20 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP20 Register (Offset = 150h) [reset = 0h]

RegionKeyEP20

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Table 14-29316. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0150h**

Figure 14-9715. FSS_FSAS_OTFA_REGS_RKEYEP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_EP20							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_EP20							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_EP20							
R/W							
0h							

Table 14-29318. FSS_FSAS_OTFA_REGS_RKEYEP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP20	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.100 FSS_FSAS_OTFA_REGS_RKEYEP21 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP21 Register (Offset = 154h) [reset = 0h]

RegionKeyEP21

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Table 14-29319. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0154h

Figure 14-9716. FSS_FSAS_OTFA_REGS_RKEYEP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP21							
R/W							
0h							

Table 14-29321. FSS_FSAS_OTFA_REGS_RKEYEP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP21	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.101 FSS_FSAS_OTFA_REGS_RKEYEP22 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP22 Register (Offset = 158h) [reset = 0h]

RegionKeyEP22

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Table 14-29322. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0158h**

Figure 14-9717. FSS_FSAS_OTFA_REGS_RKEYEP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP22							
R/W							
0h							

Table 14-29324. FSS_FSAS_OTFA_REGS_RKEYEP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP22	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.102 FSS_FSAS_OTFA_REGS_RKEYEP23 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP23 Register (Offset = 15Ch) [reset = 0h]

RegionKeyEP23

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Table 14-29325. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 015Ch**

Figure 14-9718. FSS_FSAS_OTFA_REGS_RKEYEP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP23							
R/W							
0h							

Table 14-29327. FSS_FSAS_OTFA_REGS_RKEYEP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP23	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.103 FSS_FSAS_OTFA_REGS_RKEYEP24 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP24 Register (Offset = 160h) [reset = 0h]

RegionKeyEP24

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Table 14-29328. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0160h**

Figure 14-9719. FSS_FSAS_OTFA_REGS_RKEYEP24 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP24							
R/W							
0h							

Table 14-29330. FSS_FSAS_OTFA_REGS_RKEYEP24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP24	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.104 FSS_FSAS_OTFA_REGS_RKEYEP25 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP25 Register (Offset = 164h) [reset = 0h]

RegionKeyEP25

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Table 14-29331. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0164h**

Figure 14-9720. FSS_FSAS_OTFA_REGS_RKEYEP25 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP25							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP25							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP25							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP25							
R/W							
0h							

Table 14-29333. FSS_FSAS_OTFA_REGS_RKEYEP25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP25	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.105 FSS_FSAS_OTFA_REGS_RKEYEP26 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP26 Register (Offset = 168h) [reset = 0h]

RegionKeyEP26

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Table 14-29334. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0168h**

Figure 14-9721. FSS_FSAS_OTFA_REGS_RKEYEP26 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP26							
R/W							
0h							

Table 14-29336. FSS_FSAS_OTFA_REGS_RKEYEP26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP26	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.106 FSS_FSAS_OTFA_REGS_RKEYEP27 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP27 Register (Offset = 16Ch) [reset = 0h]

RegionKeyEP27

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Table 14-29337. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 016Ch**

Figure 14-9722. FSS_FSAS_OTFA_REGS_RKEYEP27 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP27							
R/W							
0h							

Table 14-29339. FSS_FSAS_OTFA_REGS_RKEYEP27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP27	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.107 FSS_FSAS_OTFA_REGS_RKEYA20 Register

1 FSS_FSAS_OTFA_REGS_RKEYA20 Register (Offset = 170h) [reset = 0h]

RegionKeyA20

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Table 14-29340. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0170h**

Figure 14-9723. FSS_FSAS_OTFA_REGS_RKEYA20 Name Register

31	30	29	28	27	26	25	24
R_KEY_A20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A20							
R/W							
0h							

Table 14-29342. FSS_FSAS_OTFA_REGS_RKEYA20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A20	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.108 FSS_FSAS_OTFA_REGS_RKEYA21 Register

1 FSS_FSAS_OTFA_REGS_RKEYA21 Register (Offset = 174h) [reset = 0h]

RegionKeyA21

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Table 14-29343. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0174h**

Figure 14-9724. FSS_FSAS_OTFA_REGS_RKEYA21 Name Register

31	30	29	28	27	26	25	24
R_KEY_A21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A21							
R/W							
0h							

Table 14-29345. FSS_FSAS_OTFA_REGS_RKEYA21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A21	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.109 FSS_FSAS_OTFA_REGS_RKEYA22 Register

1 FSS_FSAS_OTFA_REGS_RKEYA22 Register (Offset = 178h) [reset = 0h]

RegionKeyA22

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Table 14-29346. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 0178h**

Figure 14-9725. FSS_FSAS_OTFA_REGS_RKEYA22 Name Register

31	30	29	28	27	26	25	24
R_KEY_A22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A22							
R/W							
0h							

Table 14-29348. FSS_FSAS_OTFA_REGS_RKEYA22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A22	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.110 FSS_FSAS_OTFA_REGS_RKEYA23 Register

1 FSS_FSAS_OTFA_REGS_RKEYA23 Register (Offset = 17Ch) [reset = 0h]

RegionKeyA23

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Table 14-29349. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 017Ch**

Figure 14-9726. FSS_FSAS_OTFA_REGS_RKEYA23 Name Register

31	30	29	28	27	26	25	24
R_KEY_A23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A23							
R/W							
0h							

Table 14-29351. FSS_FSAS_OTFA_REGS_RKEYA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A23	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.111 FSS_FSAS_OTFA_REGS_RKEYAP20 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP20 Register (Offset = 180h) [reset = 0h]

RegionKeyAP20

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Table 14-29352. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0180h**

Figure 14-9727. FSS_FSAS_OTFA_REGS_RKEYAP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP20							
R/W							
0h							

Table 14-29354. FSS_FSAS_OTFA_REGS_RKEYAP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP20	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.112 FSS_FSAS_OTFA_REGS_RKEYAP21 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP21 Register (Offset = 184h) [reset = 0h]

RegionKeyAP21

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Table 14-29355. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0184h**

Figure 14-9728. FSS_FSAS_OTFA_REGS_RKEYAP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP21							
R/W							
0h							

Table 14-29357. FSS_FSAS_OTFA_REGS_RKEYAP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP21	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.113 FSS_FSAS_OTFA_REGS_RKEYAP22 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP22 Register (Offset = 188h) [reset = 0h]

RegionKeyAP22

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Table 14-29358. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0188h**

Figure 14-9729. FSS_FSAS_OTFA_REGS_RKEYAP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP22							
R/W							
0h							

Table 14-29360. FSS_FSAS_OTFA_REGS_RKEYAP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP22	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.114 FSS_FSAS_OTFA_REGS_RKEYAP23 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP23 Register (Offset = 18Ch) [reset = 0h]

RegionKeyAP23

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Table 14-29361. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 018Ch**

Figure 14-9730. FSS_FSAS_OTFA_REGS_RKEYAP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP23							
R/W							
0h							

Table 14-29363. FSS_FSAS_OTFA_REGS_RKEYAP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP23	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.115 FSS_FSAS_OTFA_REGS_RIV20 Register

1 FSS_FSAS_OTFA_REGS_RIV20 Register (Offset = 190h) [reset = 0h]

RegionIV20

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Table 14-29364. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0190h**

Figure 14-9731. FSS_FSAS_OTFA_REGS_RIV20 Name Register

31	30	29	28	27	26	25	24
R_IV20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV20							
R/W							
0h							

Table 14-29366. FSS_FSAS_OTFA_REGS_RIV20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV20	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.116 FSS_FSAS_OTFA_REGS_RIV21 Register

1 FSS_FSAS_OTFA_REGS_RIV21 Register (Offset = 194h) [reset = 0h]

RegionIV21

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Table 14-29367. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0194h**

Figure 14-9732. FSS_FSAS_OTFA_REGS_RIV21 Name Register

31	30	29	28	27	26	25	24
R_IV21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV21							
R/W							
0h							

Table 14-29369. FSS_FSAS_OTFA_REGS_RIV21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV21	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.117 FSS_FSAS_OTFA_REGS_RIV22 Register

1 FSS_FSAS_OTFA_REGS_RIV22 Register (Offset = 198h) [reset = 0h]

RegionIV22

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Table 14-29370. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0198h**

Figure 14-9733. FSS_FSAS_OTFA_REGS_RIV22 Name Register

31	30	29	28	27	26	25	24
R_IV22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV22							
R/W							
0h							

Table 14-29372. FSS_FSAS_OTFA_REGS_RIV22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV22	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.118 FSS_FSAS_OTFA_REGS_RIV23 Register

1 FSS_FSAS_OTFA_REGS_RIV23 Register (Offset = 19Ch) [reset = 0h]

RegionIV23

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Table 14-29373. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 019Ch**

Figure 14-9734. FSS_FSAS_OTFA_REGS_RIV23 Name Register

31	30	29	28	27	26	25	24
R_IV23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV23							
R/W							
0h							

Table 14-29375. FSS_FSAS_OTFA_REGS_RIV23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV23	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.119 FSS_FSAS_OTFA_REGS_RGCFG3 Register

1 FSS_FSAS_OTFA_REGS_RGCFG3 Register (Offset = 1A0h) [reset = 0h]

RegionCfg3

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Table 14-29376. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01A0h**

Figure 14-9735. FSS_FSAS_OTFA_REGS_RGCFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT3	MAC_MODE3		AES_MODE3	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-29378. FSS_FSAS_OTFA_REGS_RGCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT3	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE3	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE3	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.4.2.2.120 FSS_FSAS_OTFA_REGS_RGMACST3 Register

1 FSS_FSAS_OTFA_REGS_RGMACST3 Register (Offset = 1A4h) [reset = 0h]

RegionMacStart3

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Table 14-29379. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01A4h**

Figure 14-9736. FSS_FSAS_OTFA_REGS_RGMACST3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START3							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START3							
R/W							
0h							

Table 14-29381. FSS_FSAS_OTFA_REGS_RGMACST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START3	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.121 FSS_FSAS_OTFA_REGS_RGST3 Register

1 FSS_FSAS_OTFA_REGS_RGST3 Register (Offset = 1A8h) [reset = 0h]

RegionStart3

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Table 14-29382. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01A8h

Figure 14-9737. FSS_FSAS_OTFA_REGS_RGST3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				R_START3			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
R_START3							
R/W							
0h							

7	6	5	4	3	2	1	0
R_START3							
R/W							
0h							

Table 14-29384. FSS_FSAS_OTFA_REGS_RGST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START3	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.122 FSS_FSAS_OTFA_REGS_RGSI3 Register

1 FSS_FSAS_OTFA_REGS_RGSI3 Register (Offset = 1ACh) [reset = 0h]

RegionSize3

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Table 14-29385. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01ACh**

Figure 14-9738. FSS_FSAS_OTFA_REGS_RGSI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE3							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE3							
R/W							
0h							

Table 14-29387. FSS_FSAS_OTFA_REGS_RGSI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE3	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.4.2.2.123 FSS_FSAS_OTFA_REGS_RKEYE30 Register

1 FSS_FSAS_OTFA_REGS_RKEYE30 Register (Offset = 1B0h) [reset = 0h]

RegionKeyE30

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Table 14-29388. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01B0h**

Figure 14-9739. FSS_FSAS_OTFA_REGS_RKEYE30 Name Register

31	30	29	28	27	26	25	24
R_KEY_E30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E30							
R/W							
0h							

Table 14-29390. FSS_FSAS_OTFA_REGS_RKEYE30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E30	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.124 FSS_FSAS_OTFA_REGS_RKEYE31 Register

1 FSS_FSAS_OTFA_REGS_RKEYE31 Register (Offset = 1B4h) [reset = 0h]

RegionKeyE31

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Table 14-29391. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01B4h**

Figure 14-9740. FSS_FSAS_OTFA_REGS_RKEYE31 Name Register

31	30	29	28	27	26	25	24
R_KEY_E31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E31							
R/W							
0h							

Table 14-29393. FSS_FSAS_OTFA_REGS_RKEYE31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E31	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.125 FSS_FSAS_OTFA_REGS_RKEYE32 Register

1 FSS_FSAS_OTFA_REGS_RKEYE32 Register (Offset = 1B8h) [reset = 0h]

RegionKeyE32

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Table 14-29394. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01B8h**

Figure 14-9741. FSS_FSAS_OTFA_REGS_RKEYE32 Name Register

31	30	29	28	27	26	25	24
R_KEY_E32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E32							
R/W							
0h							

Table 14-29396. FSS_FSAS_OTFA_REGS_RKEYE32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E32	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.126 FSS_FSAS_OTFA_REGS_RKEYE33 Register

1 FSS_FSAS_OTFA_REGS_RKEYE33 Register (Offset = 1BCh) [reset = 0h]

RegionKeyE33

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Table 14-29397. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01BCh**

Figure 14-9742. FSS_FSAS_OTFA_REGS_RKEYE33 Name Register

31	30	29	28	27	26	25	24
R_KEY_E33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E33							
R/W							
0h							

Table 14-29399. FSS_FSAS_OTFA_REGS_RKEYE33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E33	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.127 FSS_FSAS_OTFA_REGS_RKEYE34 Register

1 FSS_FSAS_OTFA_REGS_RKEYE34 Register (Offset = 1C0h) [reset = 0h]

RegionKeyE34

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Table 14-29400. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C0h**

Figure 14-9743. FSS_FSAS_OTFA_REGS_RKEYE34 Name Register

31	30	29	28	27	26	25	24
R_KEY_E34							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_E34							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_E34							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_E34							
R/W							
0h							

Table 14-29402. FSS_FSAS_OTFA_REGS_RKEYE34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E34	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.128 FSS_FSAS_OTFA_REGS_RKEYE35 Register

1 FSS_FSAS_OTFA_REGS_RKEYE35 Register (Offset = 1C4h) [reset = 0h]

RegionKeyE35

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Table 14-29403. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C4h**

Figure 14-9744. FSS_FSAS_OTFA_REGS_RKEYE35 Name Register

31	30	29	28	27	26	25	24
R_KEY_E35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E35							
R/W							
0h							

Table 14-29405. FSS_FSAS_OTFA_REGS_RKEYE35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E35	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.129 FSS_FSAS_OTFA_REGS_RKEYE36 Register

1 FSS_FSAS_OTFA_REGS_RKEYE36 Register (Offset = 1C8h) [reset = 0h]

RegionKeyE36

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Table 14-29406. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C8h**

Figure 14-9745. FSS_FSAS_OTFA_REGS_RKEYE36 Name Register

31	30	29	28	27	26	25	24
R_KEY_E36							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E36							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E36							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E36							
R/W							
0h							

Table 14-29408. FSS_FSAS_OTFA_REGS_RKEYE36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E36	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.130 FSS_FSAS_OTFA_REGS_RKEYE37 Register

1 FSS_FSAS_OTFA_REGS_RKEYE37 Register (Offset = 1CCh) [reset = 0h]

RegionKeyE37

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Table 14-29409. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01CCh**

Figure 14-9746. FSS_FSAS_OTFA_REGS_RKEYE37 Name Register

31	30	29	28	27	26	25	24
R_KEY_E37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E37							
R/W							
0h							

Table 14-29411. FSS_FSAS_OTFA_REGS_RKEYE37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E37	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.4.2.2.131 FSS_FSAS_OTFA_REGS_RKEYEP30 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP30 Register (Offset = 1D0h) [reset = 0h]

RegionKeyEP30

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Table 14-29412. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D0h**

Figure 14-9747. FSS_FSAS_OTFA_REGS_RKEYEP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP30							
R/W							
0h							

Table 14-29414. FSS_FSAS_OTFA_REGS_RKEYEP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP30	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.132 FSS_FSAS_OTFA_REGS_RKEYEP31 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP31 Register (Offset = 1D4h) [reset = 0h]

RegionKeyEP31

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Table 14-29415. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D4h**

Figure 14-9748. FSS_FSAS_OTFA_REGS_RKEYEP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP31							
R/W							
0h							

Table 14-29417. FSS_FSAS_OTFA_REGS_RKEYEP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP31	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.133 FSS_FSAS_OTFA_REGS_RKEYEP32 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP32 Register (Offset = 1D8h) [reset = 0h]

RegionKeyEP32

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Table 14-29418. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D8h**

Figure 14-9749. FSS_FSAS_OTFA_REGS_RKEYEP32 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP32							
R/W							
0h							

Table 14-29420. FSS_FSAS_OTFA_REGS_RKEYEP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP32	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.134 FSS_FSAS_OTFA_REGS_RKEYEP33 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP33 Register (Offset = 1DCh) [reset = 0h]

RegionKeyEP33

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Table 14-29421. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01DCh**

Figure 14-9750. FSS_FSAS_OTFA_REGS_RKEYEP33 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP33							
R/W							
0h							

Table 14-29423. FSS_FSAS_OTFA_REGS_RKEYEP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP33	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.135 FSS_FSAS_OTFA_REGS_RKEYEP34 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP34 Register (Offset = 1E0h) [reset = 0h]

RegionKeyEP34

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Table 14-29424. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01E0h**

Figure 14-9751. FSS_FSAS_OTFA_REGS_RKEYEP34 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP34							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP34							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP34							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP34							
R/W							
0h							

Table 14-29426. FSS_FSAS_OTFA_REGS_RKEYEP34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP34	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.136 FSS_FSAS_OTFA_REGS_RKEYEP35 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP35 Register (Offset = 1E4h) [reset = 0h]

RegionKeyEP35

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Table 14-29427. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01E4h**

Figure 14-9752. FSS_FSAS_OTFA_REGS_RKEYEP35 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP35							
R/W							
0h							

Table 14-29429. FSS_FSAS_OTFA_REGS_RKEYEP35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP35	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.137 FSS_FSAS_OTFA_REGS_RKEYEP36 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP36 Register (Offset = 1E8h) [reset = 0h]

RegionKeyEP36

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Table 14-29430. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01E8h

Figure 14-9753. FSS_FSAS_OTFA_REGS_RKEYEP36 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP36							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP36							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP36							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP36							
R/W							
0h							

Table 14-29432. FSS_FSAS_OTFA_REGS_RKEYEP36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP36	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.138 FSS_FSAS_OTFA_REGS_RKEYEP37 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP37 Register (Offset = 1ECh) [reset = 0h]

RegionKeyEP37

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Table 14-29433. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01ECh**

Figure 14-9754. FSS_FSAS_OTFA_REGS_RKEYEP37 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP37							
R/W							
0h							

Table 14-29435. FSS_FSAS_OTFA_REGS_RKEYEP37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP37	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.4.2.2.139 FSS_FSAS_OTFA_REGS_RKEYA30 Register

1 FSS_FSAS_OTFA_REGS_RKEYA30 Register (Offset = 1F0h) [reset = 0h]

RegionKeyA30

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Table 14-29436. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01F0h**

Figure 14-9755. FSS_FSAS_OTFA_REGS_RKEYA30 Name Register

31	30	29	28	27	26	25	24
R_KEY_A30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A30							
R/W							
0h							

Table 14-29438. FSS_FSAS_OTFA_REGS_RKEYA30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A30	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.140 FSS_FSAS_OTFA_REGS_RKEYA31 Register

1 FSS_FSAS_OTFA_REGS_RKEYA31 Register (Offset = 1F4h) [reset = 0h]

RegionKeyA31

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Table 14-29439. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01F4h**

Figure 14-9756. FSS_FSAS_OTFA_REGS_RKEYA31 Name Register

31	30	29	28	27	26	25	24
R_KEY_A31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A31							
R/W							
0h							

Table 14-29441. FSS_FSAS_OTFA_REGS_RKEYA31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A31	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.141 FSS_FSAS_OTFA_REGS_RKEYA32 Register

1 FSS_FSAS_OTFA_REGS_RKEYA32 Register (Offset = 1F8h) [reset = 0h]

RegionKeyA32

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Table 14-29442. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01F8h**

Figure 14-9757. FSS_FSAS_OTFA_REGS_RKEYA32 Name Register

31	30	29	28	27	26	25	24
R_KEY_A32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A32							
R/W							
0h							

Table 14-29444. FSS_FSAS_OTFA_REGS_RKEYA32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A32	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.142 FSS_FSAS_OTFA_REGS_RKEYA33 Register

1 FSS_FSAS_OTFA_REGS_RKEYA33 Register (Offset = 1FCh) [reset = 0h]

RegionKeyA33

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Table 14-29445. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01FCh**

Figure 14-9758. FSS_FSAS_OTFA_REGS_RKEYA33 Name Register

31	30	29	28	27	26	25	24
R_KEY_A33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A33							
R/W							
0h							

Table 14-29447. FSS_FSAS_OTFA_REGS_RKEYA33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A33	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.4.2.2.143 FSS_FSAS_OTFA_REGS_RKEYAP30 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP30 Register (Offset = 200h) [reset = 0h]

RegionKeyAP30

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Table 14-29448. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0200h**

Figure 14-9759. FSS_FSAS_OTFA_REGS_RKEYAP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP30							
R/W							
0h							

Table 14-29450. FSS_FSAS_OTFA_REGS_RKEYAP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP30	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.144 FSS_FSAS_OTFA_REGS_RKEYAP31 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP31 Register (Offset = 204h) [reset = 0h]

RegionKeyAP31

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Table 14-29451. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0204h**

Figure 14-9760. FSS_FSAS_OTFA_REGS_RKEYAP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP31							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_AP31							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_AP31							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_AP31							
R/W							
0h							

Table 14-29453. FSS_FSAS_OTFA_REGS_RKEYAP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP31	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.145 FSS_FSAS_OTFA_REGS_RKEYAP32 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP32 Register (Offset = 208h) [reset = 0h]

RegionKeyAP32

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Table 14-29454. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0208h**

Figure 14-9761. FSS_FSAS_OTFA_REGS_RKEYAP32 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP32							
R/W							
0h							

Table 14-29456. FSS_FSAS_OTFA_REGS_RKEYAP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP32	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.146 FSS_FSAS_OTFA_REGS_RKEYAP33 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP33 Register (Offset = 20Ch) [reset = 0h]

RegionKeyAP33

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Table 14-29457. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 020Ch**

Figure 14-9762. FSS_FSAS_OTFA_REGS_RKEYAP33 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP33							
R/W							
0h							

Table 14-29459. FSS_FSAS_OTFA_REGS_RKEYAP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP33	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.4.2.2.147 FSS_FSAS_OTFA_REGS_RIV30 Register

1 FSS_FSAS_OTFA_REGS_RIV30 Register (Offset = 210h) [reset = 0h]

RegionIV30

Return to Summary Table

Table 14-29460. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0210h**

Figure 14-9763. FSS_FSAS_OTFA_REGS_RIV30 Name Register

31	30	29	28	27	26	25	24
R_IV30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV30							
R/W							
0h							

Table 14-29462. FSS_FSAS_OTFA_REGS_RIV30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV30	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.148 FSS_FSAS_OTFA_REGS_RIV31 Register

1 FSS_FSAS_OTFA_REGS_RIV31 Register (Offset = 214h) [reset = 0h]

RegionIV31

Return to Summary Table

Table 14-29463. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0214h**

Figure 14-9764. FSS_FSAS_OTFA_REGS_RIV31 Name Register

31	30	29	28	27	26	25	24
R_IV31							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_IV31							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_IV31							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_IV31							
R/W							
0h							

Table 14-29465. FSS_FSAS_OTFA_REGS_RIV31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV31	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.149 FSS_FSAS_OTFA_REGS_RIV32 Register

1 FSS_FSAS_OTFA_REGS_RIV32 Register (Offset = 218h) [reset = 0h]

RegionIV32

Return to Summary Table

Table 14-29466. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0218h**

Figure 14-9765. FSS_FSAS_OTFA_REGS_RIV32 Name Register

31	30	29	28	27	26	25	24
R_IV32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV32							
R/W							
0h							

Table 14-29468. FSS_FSAS_OTFA_REGS_RIV32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV32	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.150 FSS_FSAS_OTFA_REGS_RIV33 Register

1 FSS_FSAS_OTFA_REGS_RIV33 Register (Offset = 21Ch) [reset = 0h]

RegionIV33

Return to Summary Table

Table 14-29469. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 021Ch**

Figure 14-9766. FSS_FSAS_OTFA_REGS_RIV33 Name Register

31	30	29	28	27	26	25	24
R_IV33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV33							
R/W							
0h							

Table 14-29471. FSS_FSAS_OTFA_REGS_RIV33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV33	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.4.2.2.151 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register

1 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register (Offset = 220h) [reset = 0h]

IRQAdditionalInfo0

Return to Summary Table

Table 14-29472. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0220h**

Figure 14-9767. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Name Register

31	30	29	28	27	26	25	24
IRQ_MADDR							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MADDR							
R							
0h							
15	14	13	12	11	10	9	8
IRQ_MADDR							
R							
0h							
7	6	5	4	3	2	1	0
IRQ_MADDR							
R							
0h							

Table 14-29474. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IRQ_MADDR	R	0h	Initiator Address which caused the event Reset Source: rst_modg_rst_n

14.9.4.2.2.152 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register

1 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register (Offset = 224h) [reset = 0h]

IRQAdditionalInfo1

Return to Summary Table

Table 14-29475. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0224h**

Figure 14-9768. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">IRQ_MLEN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">IRQ_MLEN</td><td colspan="3">IRQ_MSEQ</td><td colspan="3">IRQ_MCMD</td></tr>
<tr><td colspan="2">R</td><td colspan="3">R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IRQ_MID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29477. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:14	IRQ_MLEN	R	0h	Initiator LENGTH which caused the event Reset Source: rst_modg_rst_n
13:11	IRQ_MSEQ	R	0h	Initiator SEQ which caused the event Reset Source: rst_modg_rst_n
10:8	IRQ_MCMD	R	0h	Initiator CMD which caused the event Reset Source: rst_modg_rst_n
7:0	IRQ_MID	R	0h	Initiator TAG ID which caused the event Reset Source: rst_modg_rst_n

14.9.4.2.2.153 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register

1 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register (Offset = 228h) [reset = 0h]

MACCacheInfo

Return to Summary Table

Table 14-29478. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0228h**

Figure 14-9769. FSS_FSAS_OTFA_REGS_MACCACHEINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CACHE_MISS_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
CACHE_MISS_EVENT_CNT							
R							
0h							

Table 14-29480. FSS_FSAS_OTFA_REGS_MACCACHEINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CACHE_MISS_EVENT_CNT	R	0h	MAC Cache Miss event cnt Reset Source: rst_modg_rst_n

14.9.4.2.2.154 FSS_FSAS_OTFA_REGS_RMWRMCNT Register

1 FSS_FSAS_OTFA_REGS_RMWRMCNT Register (Offset = 22Ch) [reset = 0h]

RMWRMCnt

Return to Summary Table

Table 14-29481. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 022Ch**

Figure 14-9770. FSS_FSAS_OTFA_REGS_RMWRMCNT Name Register

31	30	29	28	27	26	25	24
RM_EVENT_CNT							
R							
0h							
23	22	21	20	19	18	17	16
RM_EVENT_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RMW_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RMW_EVENT_CNT							
R							
0h							

Table 14-29483. FSS_FSAS_OTFA_REGS_RMWRMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RM_EVENT_CNT	R	0h	RM event cnt Reset Source: rst_modg_rst_n
15:0	RMW_EVENT_CNT	R	0h	RMW event cnt Reset Source: rst_modg_rst_n

14.9.4.2.2.155 FSS_DAT_REG1_HPB_DATA_MEM_j Register

1 FSS_DAT_REG1_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS boot data region1

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 134217727d

Table 14-29484. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**6000 0000h + formula**

Figure 14-9771. FSS_DAT_REG1_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-29486. FSS_DAT_REG1_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.9.4.2.2.156 FSS_DAT_REG0_HPB_DATA_MEM_j Register

1 FSS_DAT_REG0_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS data region0

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 4294967295d

Table 14-29487. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0004 0000 0000h + formula**

Figure 14-9772. FSS_DAT_REG0_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-29489. FSS_DAT_REG0_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region0 Reset Source: rst_mod_g_rst_n

14.9.4.2.2.157 FSS_DAT_REG3_HPB_DATA_MEM_j Register

1 FSS_DAT_REG3_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS bypass data region3

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 4294967295d

Table 14-29490. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0005 0000 0000h + formula**

Figure 14-9773. FSS_DAT_REG3_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-29492. FSS_DAT_REG3_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.9.4.3 FSS_OSPI_0

FSS_OSPI_0

14.9.4.3.1 FSS_OSPI_0 Summaries

FSS_OSPI_0 Summaries

Table 14-29493. ECC_AGGR Registers, Base Address=0071 6000h, Length=1024

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	ECC_AGGR_REV	0071 6000h
8h	32	ECC_AGGR_VECTOR	0071 6008h
Ch	32	ECC_AGGR_STAT	0071 600Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 6010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 603Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 6040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 6080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 60C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 613Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 6140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 6180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 61C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 6200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 6204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 6208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 620Ch

Table 14-29494. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	OSPI_FLASH_CFG_CONFIG_REG	0FC4 0000h
4h	32	OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG	0FC4 0004h
8h	32	OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG	0FC4 0008h
Ch	32	OSPI_FLASH_CFG_DEV_DELAY_REG	0FC4 000Ch
10h	32	OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG	0FC4 0010h
14h	32	OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG	0FC4 0014h
18h	32	OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG	0FC4 0018h
1Ch	32	OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG	0FC4 001Ch
20h	32	OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG	0FC4 0020h
24h	32	OSPI_FLASH_CFG_REMAP_ADDR_REG	0FC4 0024h
28h	32	OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG	0FC4 0028h
2Ch	32	OSPI_FLASH_CFG_SRAM_FILL_REG	0FC4 002Ch
30h	32	OSPI_FLASH_CFG_TX_THRESH_REG	0FC4 0030h
34h	32	OSPI_FLASH_CFG_RX_THRESH_REG	0FC4 0034h
38h	32	OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG	0FC4 0038h
3Ch	32	OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG	0FC4 003Ch
40h	32	OSPI_FLASH_CFG_IRQ_STATUS_REG	0FC4 0040h
44h	32	OSPI_FLASH_CFG_IRQ_MASK_REG	0FC4 0044h

Table 14-29494. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256 (continued)

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
50h	32	OSPI_FLASH_CFG_LOWER_WR_PROT_REG	0FC4 0050h
54h	32	OSPI_FLASH_CFG_UPPER_WR_PROT_REG	0FC4 0054h
58h	32	OSPI_FLASH_CFG_WR_PROT_CTRL_REG	0FC4 0058h
60h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG	0FC4 0060h
64h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG	0FC4 0064h
68h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG	0FC4 0068h
6Ch	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG	0FC4 006Ch
70h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG	0FC4 0070h
74h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG	0FC4 0074h
78h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG	0FC4 0078h
7Ch	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG	0FC4 007Ch
80h	32	OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG	0FC4 0080h
8Ch	32	OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG	0FC4 008Ch
90h	32	OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG	0FC4 0090h
94h	32	OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG	0FC4 0094h
A0h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG	0FC4 00A0h
A4h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG	0FC4 00A4h
A8h	32	OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG	0FC4 00A8h
ACh	32	OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG	0FC4 00ACh
B0h	32	OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG	0FC4 00B0h
B4h	32	OSPI_FLASH_CFG_PHY_CONFIGURATION_REG	0FC4 00B4h
B8h	32	OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG	0FC4 00B8h
BCh	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG	0FC4 00BCh
C0h	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG	0FC4 00C0h
E0h	32	OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG	0FC4 00E0h
E4h	32	OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG	0FC4 00E4h
FCh	32	OSPI_FLASH_CFG_MODULE_ID_REG	0FC4 00FCh

Table 14-29495. OSPI_CFG Registers, Base Address=0FC4 4000h, Length=512

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	OSPI_CFG_PID	0FC4 4000h
4h	32	OSPI_CFG_CTRL	0FC4 4004h
8h	32	OSPI_CFG_STAT	0FC4 4008h
20h	32	OSPI_CFG_EOI	0FC4 4020h

14.9.4.3.2 FSS_OSPI_0 Registers

FSS_OSPI_0 Registers

14.9.4.3.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-29496. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6000h**

Figure 14-9774. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-29498. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.4.3.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-29499. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6008h**

Figure 14-9775. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-29501. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.4.3.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-29502. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 600Ch**

Figure 14-9776. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-29504. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.4.3.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-29505. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6010h + formula**

Figure 14-9777. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-29507. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.3.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-29508. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 603Ch**

Figure 14-9778. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-29510. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29511. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6040h**

Figure 14-9779. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-29513. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.9.4.3.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29514. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6080h**

Figure 14-9780. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SRAM_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-29516. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.9.4.3.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29517. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 60C0h**

Figure 14-9781. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29519. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.9.4.3.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-29520. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 613Ch**

Figure 14-9782. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-29522. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.3.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29523. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6140h**

Figure 14-9783. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-29525. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.9.4.3.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29526. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0071 6180h

Figure 14-9784. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-29528. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.9.4.3.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29529. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 61C0h**

Figure 14-9785. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29531. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.9.4.3.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-29532. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6200h**

Figure 14-9786. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-29534. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.4.3.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-29535. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6204h**

Figure 14-9787. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-29537. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.4.3.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-29538. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6208h**

Figure 14-9788. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-29540. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.4.3.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-29541. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 620Ch**

Figure 14-9789. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-29543. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.4.3.2.17 OSPI_FLASH_CFG_CONFIG_REG Register

1 OSPI_FLASH_CFG_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

Octal-SPI Configuration Register

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Table 14-29544. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0000h**

Figure 14-9790. OSPI_FLASH_CFG_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_EN_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R	R/W	R/W	R			R/W	R/W
1h	0h	0h	0h			0h	0h
23	22	21	20	19	18	17	16
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD				ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD
R/W	R/W				R/W	R/W	R/W
0h	Fh				0h	0h	0h
15	14	13	12	11	10	9	8
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD				PERIPH_SEL_DEC_FLD	ENB_LEGACY_IP_MODE_FLD
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	6	5	4	3	2	1	0
ENB_DIR_ACC_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	1h

Table 14-29546. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_EN_FLD	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode [i.e. Macronix MX25]. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register [Lower] and from Opcode Extension Register [Upper].
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC [Macronix MX25]. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode.
28:26	CONFIG_RESV2_FLD	R	0h	Reserved
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.

Table 14-29546. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol.
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder: Value=0 : Active target is selected based on Peripheral Chip Select Lines [bits [13:10]]. Value=1 Active target is selected based on actual AHB address [the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register]
22:19	MSTR_BAUD_DIV_FLD	R/W	Fh	Initiator Mode Baud Rate Divisor: SPI baud rate = [initiator reference clock] baud_rate_divisor
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode [as per the contents of its non- volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited.
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable AHB Address Re-mapping: [Direct Access Mode Only] When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register.
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.
13:10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110 xx01 1101 x011 1011 0111 0111 1111 1111 [no peripheral selected] else ss[3:0] directly drives n_ss_out[3:0]
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode: 0 : only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode [n_ss_out = ss]
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable: 0 : Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.

Table 14-29546. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller: 0 : disable the Direct Access Controller once current transfer of the data word [FF_W] is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output]
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0 : the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word: 0 : the SPI clock is quiescent low 1 : the SPI clock is quiescent high
0	ENB_SPI_FLD	R/W	1h	Octal-SPI Enable: 0 : disable the Octal-SPI, once current transfer of the data word [FF_W] is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

14.9.4.3.2.18 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

Device Read Instruction Configuration Register

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Table 14-29547. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0004h

Figure 14-9791. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RD_INSTR_RESV5_FLD			DUMMY_RD_CLK_CYCLES_FLD				
R			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RD_INSTR_RESV4_FLD			MODE_BIT_ENABLE_FLD	RD_INSTR_RESV3_FLD		DATA_XFER_TYPE_EXT_MODE_FLD	
R			R/W	R		R/W	
0h			0h	0h		0h	
15	14	13	12	11	10	9	8
RD_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		RD_INSTR_RESV1_FLD	DDR_EN_FLD	INSTR_TYPE_FLD	
R		R/W		R	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
RD_OPCODE_NON_XIP_FLD							
R/W							
3h							

Table 14-29549. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28:24	DUMMY_RD_CLK_CYCLES_FLD	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction.
23:21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FLD	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19:18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	RD_INSTR_RESV2_FLD	R	0h	Reserved

Table 14-29549. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved
10	DDR_EN_FLD	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands
9:8	INSTR_TYPE_FLD	R/W	0h	Instruction Type: 0 : Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1 : Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2 : Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2 and DQ3] 3 : Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7:0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

14.9.4.3.2.19 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

Device Write Instruction Configuration Register

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Table 14-29550. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0008h**

Figure 14-9792. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
WR_INSTR_RESV4_FLD			DUMMY_WR_CLK_CYCLES_FLD				
R			R/W				
0h			0h				
23	22	21	20	19	18	17	16
WR_INSTR_RESV3_FLD						DATA_XFER_TYPE_EXT_MODE_FLD	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
WR_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		WR_INSTR_RESV1_FLD			WEL_DIS_FLD
R		R/W		R			R/W
0h		0h		0h			0h
7	6	5	4	3	2	1	0
WR_OPCODE_FLD							
R/W							
2h							

Table 14-29552. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28:24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction.
23:18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11:9	WR_INSTR_RESV1_FLD	R	0h	Reserved
8	WEL_DIS_FLD	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC

Table 14-29552. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	WR_OPCODE_FLD	R/W	2h	Write Opcode

14.9.4.3.2.20 OSPI_FLASH_CFG_DEV_DELAY_REG Register

1 OSPI_FLASH_CFG_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the initiator output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI initiator ref clock.

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Table 14-29553. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 000Ch**

Figure 14-9793. OSPI_FLASH_CFG_DEV_DELAY_REG Name Register

31	30	29	28	27	26	25	24
D_NSS_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
D_BTWN_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
D_AFTER_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
D_INIT_FLD							
R/W							
0h							

Table 14-29555. OSPI_FLASH_CFG_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert: Delay in initiator reference clocks for the length that the initiator mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23:16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in initiator reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different targets and requires the transmit FIFO to be empty.
15:8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit: Delay in initiator reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out]. By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7:0	D_INIT_FLD	R/W	0h	Clock Delay with n_ss_out: Delay in initiator reference clocks between setting n_ss_out low and first bit transfer.

14.9.4.3.2.21 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register

1 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

Read Data Capture Register

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Table 14-29556. Instance Table

Instance Name	**Physical Address**
FSS0_OSPI_0	**0FC4 0010h**

Figure 14-9794. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RD_DATA_RESV3_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RD_DATA_RESV3_FLD</td><td colspan="4">DDR_READ_DELAY_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RD_DATA_RESV2_FLD</td><td>DQS_ENABLE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RD_DATA_RESV1_FLD</td><td>SAMPLE_EDGE_SEL_FLD</td><td colspan="4">DELAY_FLD</td><td>BYPASS_FLD</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 14-29558. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RD_DATA_RESV3_FLD	R	0h	Reserved
19:16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15:9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk..
7:6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled
4:1	DELAY_FLD	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles
0	BYPASS_FLD	R/W	1h	Bypass the adapted loopback clock circuit

14.9.4.3.2.22 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 101002h]

Device Size Configuration Register

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Table 14-29559. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0014h**

Figure 14-9795. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R			R/W		R/W		R/W
0h			0h		0h		0h
23	22	21	20	19	18	17	16
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W	R/W		R/W				
0h	0h		10h				
15	14	13	12	11	10	9	8
BYTES_PER_DEVICE_PAGE_FLD							
R/W							
100h							
7	6	5	4	3	2	1	0
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W				R/W			
100h				2h			

Table 14-29561. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28:27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
26:25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
24:23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
22:21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
20:16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number.
15:4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3:0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

14.9.4.3.2.23 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register

1 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

SRAM Partition Configuration Register

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Table 14-29562. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0018h**

Figure 14-9796. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Name Register

31	30	29	28	27	26	25	24
SRAM_PARTITION_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_PARTITION_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_PARTITION_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
80h							

Table 14-29564. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7:0	ADDR_FLD	R/W	80h	Indirect Read Partition Size: Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

14.9.4.3.2.24 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register

1 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

Indirect AHB Address Trigger Register

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Table 14-29565. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 001Ch**

Figure 14-9797. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-29567. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM.

14.9.4.3.2.25 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register

1 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register (Offset = 20h) [reset = 0h]

DMA Peripheral Configuration Register

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Table 14-29568. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0020h**

Figure 14-9798. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DMA_PERIPH_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DMA_PERIPH_RESV2_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMA_PERIPH_RESV2_FLD				NUM_BURST_REQ_BYTES_FLD			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMA_PERIPH_RESV1_FLD				NUM_SINGLE_REQ_BYTES_FLD			
R				R/W			
0h				0h			

Table 14-29570. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	DMA_PERIPH_RESV2_FLD	R	0h	Reserved
11:8	NUM_BURST_REQ_BYTES_FLD	R/W	0h	Number of Burst Bytes: Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.
7:4	DMA_PERIPH_RESV1_FLD	R	0h	Reserved
3:0	NUM_SINGLE_REQ_BYTES_FLD	R/W	0h	Number of Single Bytes: Number of bytes in a single type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.

14.9.4.3.2.26 OSPI_FLASH_CFG_REMAP_ADDR_REG Register

1 OSPI_FLASH_CFG_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

Remap Address Register

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Table 14-29571. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0024h**

Figure 14-9799. OSPI_FLASH_CFG_REMAP_ADDR_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-29573. OSPI_FLASH_CFG_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device.

14.9.4.3.2.27 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register

1 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

Mode Bit Configuration Register

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Table 14-29574. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0028h**

Figure 14-9800. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RX_CRC_DATA_LOW_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CRC_DATA_UP_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_OUT_ENABLE_FLD	MODE_BIT_RESV1_FLD				CHUNK_SIZE_FLD		
R/W	R				R/W		
0h	0h				2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MODE_FLD							
R/W							
0h							

Table 14-29576. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower] The first CRC byte returned after RX data chunk.
23:16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper] The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14:11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10:8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers.
7:0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

14.9.4.3.2.28 OSPI_FLASH_CFG_SRAM_FILL_REG Register

1 OSPI_FLASH_CFG_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

SRAM Fill Register

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Table 14-29577. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 002Ch**

Figure 14-9801. OSPI_FLASH_CFG_SRAM_FILL_REG Name Register

31	30	29	28	27	26	25	24
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_FILL_INDAC_READ_FLD							
R							
0h							
7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD							
R							
0h							

Table 14-29579. OSPI_FLASH_CFG_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]: Identifies the current fill level of the SRAM Indirect Write partition
15:0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]: Identifies the current fill level of the SRAM Indirect Read partition

14.9.4.3.2.29 OSPI_FLASH_CFG_TX_THRESH_REG Register

1 OSPI_FLASH_CFG_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

TX Threshold Register

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Table 14-29580. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0030h**

Figure 14-9802. OSPI_FLASH_CFG_TX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
TX_THRESH_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_THRESH_RESV_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_THRESH_RESV_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-29582. OSPI_FLASH_CFG_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	TX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

14.9.4.3.2.30 OSPI_FLASH_CFG_RX_THRESH_REG Register

1 OSPI_FLASH_CFG_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

RX Threshold Register

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Table 14-29583. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0034h**

Figure 14-9803. OSPI_FLASH_CFG_RX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
RX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
RX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
RX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-29585. OSPI_FLASH_CFG_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated

14.9.4.3.2.31 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register

1 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 10005h]

Write Completion Control Register: This register defines how the controller will poll the device following a write transfer

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Table 14-29586. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0038h**

Figure 14-9804. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Name Register

31	30	29	28	27	26	25	24
POLL_REP_DELAY_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
POLL_COUNT_FLD							
R/W							
1h							
15	14	13	12	11	10	9	8
ENABLE_POLLING_EXP_FLD	DISABLE_POLLING_FLD	POLLING_POLARITY_FLD	WR_COMP_CTRL_RESV1_FLD		POLLING_BIT_INDEX_FLD		
R/W	R/W	R/W	R		R/W		
0h	0h	0h	0h		0h		
7	6	5	4	3	2	1	0
OPCODE_FLD							
R/W							
5h							

Table 14-29588. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	POLL_REP_DELAY_FLD	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase
23:16	POLL_COUNT_FLD	R/W	1h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register.
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Set to '1' for enabling auto-polling expiration.
14	DISABLE_POLLING_FLD	R/W	0h	This switches off the automatic polling function
13	POLLING_POLARITY_FLD	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'.
12:11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved
10:8	POLLING_BIT_INDEX_FLD	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for.
7:0	OPCODE_FLD	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05

14.9.4.3.2.32 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register

1 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

Polling Expiration Register

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Table 14-29589. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 003Ch**

Figure 14-9805. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Name Register

31	30	29	28	27	26	25	24
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							

Table 14-29591. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFFh	Number of polls cycles before expiration

14.9.4.3.2.33 OSPI_FLASH_CFG_IRQ_STATUS_REG Register

1 OSPI_FLASH_CFG_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

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Table 14-29592. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0040h**

Figure 14-9806. OSPI_FLASH_CFG_IRQ_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREACH_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29594. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1TC	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1TC	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1TC	0h	RX CRC data valid New RX CRC data was captured from Flash Device
16	RX_CRC_DATA_ERR_FLD	R/W1TC	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller.
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1TC	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1TC	0h	The maximum number of programmed polls cycles is expired
12	INDRD_SRAM_FULL_FLD	R/W1TC	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation

Table 14-29594. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_FLD	R/W1TC	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full 1 : FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1TC	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL_FLD	R/W1TC	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full, 1 : FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1TC	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries
7	RECV_OVERFLOW_FLD	R/W1TC	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0 : no overflow has been detected. 1 : an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1TC	0h	Indirect Transfer Watermark Level Breached
5	ILLEGAL_ACCESS_DET_FLD	R/W1TC	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1TC	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1TC	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1TC	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation
1	UNDERFLOW_DET_FLD	R/W1TC	0h	Underflow Detected: 0 : no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1TC	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in initiator mode [multi-initiator contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0 : no mode fault has been detected 1 : a mode fault has occurred

14.9.4.3.2.34 OSPI_FLASH_CFG_IRQ_MASK_REG Register

1 OSPI_FLASH_CFG_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled. 1 : the interrupt for the corresponding interrupt status register bit is enabled.

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Table 14-29595. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0044h

Figure 14-9807. OSPI_FLASH_CFG_IRQ_MASK_REG Name Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MASK_RESV_FLD				ECC_FAIL_MASK_FLD	TX_CRC_CHUNK_BRK_MASK_FLD	RX_CRC_DATA_VAL_MASK_FLD	RX_CRC_DATA_ERR_MASK_FLD
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_MASK_RESV1_FLD	STIG_REQ_MASK_FLD	POLL_EXP_INT_MASK_FLD	INDRD_SRAM_FULL_MASK_FLD	RX_FIFO_FULL_MASK_FLD	RX_FIFO_NOT_EMPTY_MASK_FLD	TX_FIFO_FULL_MASK_FLD	TX_FIFO_NOT_FULL_MASK_FLD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_MASK_FLD	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	ILLEGAL_ACCESS_DET_MASK_FLD	PROT_WR_ATTEMPT_MASK_FLD	INDIRECT_READ_REJECT_MASK_FLD	INDIRECT_OP_DONE_MASK_FLD	UNDERFLOW_DET_MASK_FLD	MODE_M_FAIL_MASK_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29597. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask

Table 14-29597. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DET_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DET_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

14.9.4.3.2.35 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register

1 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

Lower Write Protection Register

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Table 14-29598. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0050h**

Figure 14-9808. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-29600. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.9.4.3.2.36 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register

1 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

Upper Write Protection Register

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Table 14-29601. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0054h**

Figure 14-9809. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-29603. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.9.4.3.2.37 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register

1 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

Write Protection Control Register

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Table 14-29604. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0058h**

Figure 14-9810. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Name Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
WR_PROT_CTRL_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
WR_PROT_CTRL_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R						R/W	R/W
0h						0h	0h

Table 14-29606. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to.

14.9.4.3.2.38 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

Indirect Read Transfer Control Register

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Table 14-29607. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0060h**

Figure 14-9811. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_RD_XFER_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_RD_XFER_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R/W1TC	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-29609. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Two indirect read operations have been queued
3	SRAM_FULL_FLD	R/W1TC	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.; indirect operation [status]
2	RD_STATUS_FLD	R	0h	Indirect Read Status: Indirect read operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

14.9.4.3.2.39 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

Indirect Read Transfer Watermark Register

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Table 14-29610. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0064h**

Figure 14-9812. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
0h							

Table 14-29612. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all zeroes.

14.9.4.3.2.40 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

Indirect Read Transfer Start Address Register

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Table 14-29613. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0068h**

Figure 14-9813. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-29615. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the start address from which the indirect access will commence its READ operation.

14.9.4.3.2.41 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

Indirect Read Transfer Number Bytes Register

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Table 14-29616. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 006Ch**

Figure 14-9814. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-29618. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.9.4.3.2.42 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

Indirect Write Transfer Control Register

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Table 14-29619. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0070h**

Figure 14-9815. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-29621. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status: Indirect write operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

14.9.4.3.2.43 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

Indirect Write Transfer Watermark Register

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Table 14-29622. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0074h**

Figure 14-9816. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
FFFFFFFFh							

Table 14-29624. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all ones.

14.9.4.3.2.44 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

Indirect Write Transfer Start Address Register

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Table 14-29625. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0078h**

Figure 14-9817. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-29627. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation.

14.9.4.3.2.45 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

Indirect Write Transfer Number Bytes Register

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Table 14-29628. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 007Ch**

Figure 14-9818. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-29630. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.9.4.3.2.46 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

1 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

Indirect Trigger Address Range Register

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Table 14-29631. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0080h**

Figure 14-9819. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Name Register

31	30	29	28	27	26	25	24
IND_RANGE_RESV1_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IND_RANGE_RESV1_FLD							
R							
0h							
15	14	13	12	11	10	9	8
IND_RANGE_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
IND_RANGE_RESV1_FLD				IND_RANGE_WIDTH_FLD			
R				R/W			
0h				4h			

Table 14-29633. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3:0	IND_RANGE_WIDTH_FLD	R/W	4h	This is the address offset of Indirect Trigger Address Register.

14.9.4.3.2.47 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register

1 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

Flash Command Control Memory Register

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Table 14-29634. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 008Ch**

Figure 14-9820. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Name Register

31	30	29	28	27	26	25	24
FLASH_COMMAND_CTRL_MEM_RESV1_FLD			MEM_BANK_ADDR_FLD				
R			R/W				
0h			0h				
23	22	21	20	19	18	17	16
MEM_BANK_ADDR_FLD				FLASH_COMMAND_CTRL_MEM_RESV2_FLD	NB_OF_STIG_READ_BYTES_FLD		
R/W				R	R/W		
0h				0h	0h		
15	14	13	12	11	10	9	8
MEM_BANK_READ_DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
FLASH_COMMAND_CTRL_MEM_RESV3_FLD						MEM_BANK_REQ_IN_PROGRESS_FLD	TRIGGER_MEM_BANK_REQ_FLD
R						R	W
0h						0h	0h

Table 14-29636. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28:20	MEM_BANK_ADDR_FLD	R/W	0h	The address of the Memory Bank which data will be read from.
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved
18:16	NB_OF_STIG_READ_BYTES_FLD	R/W	0h	It defines the number of read bytes for the extended STIG.
15:8	MEM_BANK_READ_DATA_FLD	R	0h	Last requested data from the STIG Memory Bank.
7:2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

14.9.4.3.2.48 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register

1 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

Flash Command Control Register

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Table 14-29637. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0090h**

Figure 14-9821. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENB_READ_DATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_ADDR_FLD	ENB_MODE_BIT_FLD	NUM_ADDR_BYTES_FLD	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENB_WRITE_DATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_DUMMY_CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BANK_EN_FLD	CMD_EXEC_STATUS_FLD	CMD_EXEC_FLD
R/W	R				R/W	R	W
0h	0h				0h	0h	0h

Table 14-29639. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CMD_OPCODE_FLD	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field [bit 0] of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field [bits 31:24] requires read data bytes to be received from the device.
22:20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes.
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via Writing a 1 to the execute field.

Table 14-29639. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
17:16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes: Set to the number of address bytes required [the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS]. This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14:12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes.
11:7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register.
6:3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

14.9.4.3.2.49 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register

1 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

Flash Command Address Register

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Table 14-29640. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0094h**

Figure 14-9822. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-29642. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Command Address: This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the address used by the command specified in the opcode field [bits 31:24] of the Flash Command Control register.

14.9.4.3.2.50 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register

1 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

Flash Command Read Data Register (Lower)

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Table 14-29643. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A0h**

Figure 14-9823. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-29645. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.9.4.3.2.51 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register

1 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

Flash Command Read Data Register (Upper)

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Table 14-29646. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A4h**

Figure 14-9824. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-29648. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.9.4.3.2.52 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register

1 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

Flash Command Write Data Register (Lower)

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Table 14-29649. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A8h**

Figure 14-9825. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-29651. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.9.4.3.2.53 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register

1 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

Flash Command Write Data Register (Upper)

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Table 14-29652. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00ACh**

Figure 14-9826. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-29654. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.9.4.3.2.54 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register

1 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

Polling Flash Status Register

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Table 14-29655. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00B0h**

Figure 14-9827. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R							
0h							
23	22	21	20	19	18	17	16
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DEVICE_STATUS_RSVD_FLD1							DEVICE_STATUS_VALID_FLD
R							R
0h							0h
7	6	5	4	3	2	1	0
DEVICE_STATUS_FLD							
R							
0h							

Table 14-29657. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19:16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling
15:9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid.
7:0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device

14.9.4.3.2.55 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register

1 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

PHY Configuration Register

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Table 14-29658. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00B4h**

Figure 14-9828. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Name Register

31	30	29	28	27	26	25	24
PHY_CONFIG_RESYNC_FLD	PHY_CONFIG_RESET_FLD	PHY_CONFIG_RX_DLL_BYPASS_FLD	PHY_CONFIG_RESV2_FLD				
W	W	R/W	R				
0h	1h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CONFIG_RESV2_FLD	PHY_CONFIG_TX_DLL_DELAY_FLD						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CONFIG_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CONFIG_RESV1_FLD	PHY_CONFIG_RX_DLL_DELAY_FLD						
R	R/W						
0h	0h						

Table 14-29660. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed.
28:23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22:16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk.
15:7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved
6:0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk.

14.9.4.3.2.56 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register

1 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 800000h]

PHY DLL Initiator Control Register

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Table 14-29661. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 00B8h

Figure 14-9829. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_CONTROL_RESV3_FLD							PHY_MASTER_LOCK_MODE_FLD
R							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_MASTER_BYPASS_MODE_FLD	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD			PHY_MASTER_CONTROL_RESV2_FLD	PHY_MASTER_NB_INDICATIONS_FLD		
R/W	R/W			R	R/W		
1h	0h			0h	0h		
15	14	13	12	11	10	9	8
PHY_MASTER_CONTROL_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
PHY_MASTER_CONTROL_RESV1_FLD	PHY_MASTER_INITIAL_DELAY_FLD						
R	R/W						
0h	0h						

Table 14-29663. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the initiator delay line locks on a full cycle or half cycle of delay.
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the initiator and target DLLs.
22:20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops.
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18:16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15:7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved

Table 14-29663. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the DLL.

14.9.4.3.2.57 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register

1 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

DLL Observable Register Lower

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Table 14-29664. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00BCh**

Figure 14-9830. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD		DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD
R					R		R
0h					0h		0h

Table 14-29666. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative dll_lock_inc register.
23:16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative dll_lock_dec register.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14:8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	Reports the DLL encoder value from the initiator DLL to the target DLLs.
7:3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	Reports the number of increments or decrements required for the initiator DLL to complete the locking process.
2:1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	Defines the mode in which the DLL has achieved the lock.

Table 14-29666. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	Indicates status of DLL.

14.9.4.3.2.58 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register

1 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

DLL Observable Register Upper

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Table 14-29667. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00C0h**

Figure 14-9831. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_UPPER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_UPPER_RESV2_FLD	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_UPPER_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_UPPER_RESV1_FLD	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						

Table 14-29669. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22:16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the TX delay line for this slice.
15:7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6:0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the RX delay line for this slice.

14.9.4.3.2.59 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register

1 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

Opcode Extension Register (Lower)

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Table 14-29670. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00E0h**

Figure 14-9832. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Name Register

31	30	29	28	27	26	25	24
EXT_READ_OPCODE_FLD							
R/W							
13h							
23	22	21	20	19	18	17	16
EXT_WRITE_OPCODE_FLD							
R/W							
EDh							
15	14	13	12	11	10	9	8
EXT_POLL_OPCODE_FLD							
R/W							
FAh							
7	6	5	4	3	2	1	0
EXT_STIG_OPCODE_FLD							
R/W							
0h							

Table 14-29672. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcode
23:16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode
15:8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode
7:0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode

14.9.4.3.2.60 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register

1 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 6F90000h]

Opcode Extension Register (Upper)

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Table 14-29673. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00E4h**

Figure 14-9833. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Name Register

31	30	29	28	27	26	25	24
WEL_OPCODE_FLD							
R/W							
6h							
23	22	21	20	19	18	17	16
EXT_WEL_OPCODE_FLD							
R/W							
F9h							
15	14	13	12	11	10	9	8
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							

Table 14-29675. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WEL_OPCODE_FLD	R/W	6h	First byte of any WEL Opcode
23:16	EXT_WEL_OPCODE_FLD	R/W	F9h	Supplement byte of any WEL Opcode
15:0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

14.9.4.3.2.61 OSPI_FLASH_CFG_MODULE_ID_REG Register

1 OSPI_FLASH_CFG_MODULE_ID_REG Register (Offset = FCh) [reset = 3000300h]

Module ID Register

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Table 14-29676. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00FCh**

Figure 14-9834. OSPI_FLASH_CFG_MODULE_ID_REG Name Register

31	30	29	28	27	26	25	24
FIX_PATCH_FLD							
R							
3h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID_FLD							
R							
3h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODULE_ID_FLD							
R							
3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MODULE_ID_RESV_FLD						CONF_FLD	
R						R	
0h						0h	

Table 14-29678. OSPI_FLASH_CFG_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23:8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7:2	MODULE_ID_RESV_FLD	R	0h	Reserved
1:0	CONF_FLD	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration

14.9.4.3.2.62 OSPI_CFG_PID Register

1 OSPI_CFG_PID Register (Offset = 0h) [reset = 68748100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-29679. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4000h**

Figure 14-9835. OSPI_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		874h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
874h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-29681. OSPI_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: psrst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: psrst_n
27:16	MODULE_ID	R	874h	Module ID Reset Source: psrst_n
15:11	RTL	R	10h	RTL revision. Will vary depending on release. Reset Source: psrst_n
10:8	MAJOR	R	1h	Major revision Reset Source: psrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: psrst_n
5:0	MINOR	R	0h	Minor revision Reset Source: psrst_n

14.9.4.3.2.63 OSPI_CFG_CTRL Register

1 OSPI_CFG_CTRL Register (Offset = 4h) [reset = 0h]

The Control Register contains general control bits for the ospi

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Table 14-29682. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4004h**

Figure 14-9836. OSPI_CFG_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PIPELINE_MODE_FLUSH	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		

Table 14-29684. OSPI_CFG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PIPELINE_MODE_FLUSH	R/W	0h	1 - Flush Cadence Flash Controller FIFO by forcin gAHB SEL low. 0 - AHB Sel to Cadence Controller is 1 Reset Source: psrst_n
2:0	RESERVED	NONE	0h	Reserved

14.9.4.3.2.64 OSPI_CFG_STAT Register

1 OSPI_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the ospi

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Table 14-29685. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4008h**

Figure 14-9837. OSPI_CFG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
NONE						R	NONE
0h						0h	0h

Table 14-29687. OSPI_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: psrst_n
0	RESERVED	NONE	0h	Reserved

14.9.4.3.2.65 OSPI_CFG_EOI Register

1 OSPI_CFG_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-29688. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 4020h

Figure 14-9838. OSPI_CFG_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-29690. OSPI_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targetted interrupt. (E.g. Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt Reset Source: psrst_n

14.9.4.4 GPMC

GPMC

14.9.4.4.1 GPMC Summaries

GPMC Summaries

Table 14-29691. GPMC Registers, Base Address=3B00 0000h, Length=1024

Offset	Length	Register Name	GPMC0 Physical Address
0h	32	GPMC_REVISION	3B00 0000h
10h	32	GPMC_SYSCONFIG	3B00 0010h
14h	32	GPMC_SYSSTATUS	3B00 0014h
18h	32	GPMC_IRQSTATUS	3B00 0018h
1Ch	32	GPMC_IRQENABLE	3B00 001Ch
40h	32	GPMC_TIMEOUT_CONTROL	3B00 0040h
44h	32	GPMC_ERR_ADDRESS	3B00 0044h
48h	32	GPMC_ERR_TYPE	3B00 0048h
50h	32	GPMC_CONFIG	3B00 0050h
54h	32	GPMC_STATUS	3B00 0054h
1E0h	32	GPMC_PREFETCH_CONFIG1	3B00 01E0h
1E4h	32	GPMC_PREFETCH_CONFIG2	3B00 01E4h
1ECh	32	GPMC_PREFETCH_CONTROL	3B00 01ECh
1F0h	32	GPMC_PREFETCH_STATUS	3B00 01F0h
1F4h	32	GPMC_ECC_CONFIG	3B00 01F4h
1F8h	32	GPMC_ECC_CONTROL	3B00 01F8h
1FCh	32	GPMC_ECC_SIZE_CONFIG	3B00 01FCh
200h	32	GPMC_ECC_RESULT_J	3B00 0200h + formula
2D0h	32	GPMC_BCH_SWDATA	3B00 02D0h
0h	32	GPMC_CONFIG1_J	3B00 0000h + formula
4h	32	GPMC_CONFIG2_J	3B00 0004h + formula
8h	32	GPMC_CONFIG3_J	3B00 0008h + formula
Ch	32	GPMC_CONFIG4_J	3B00 000Ch + formula
10h	32	GPMC_CONFIG5_J	3B00 0010h + formula
14h	32	GPMC_CONFIG6_J	3B00 0014h + formula
18h	32	GPMC_CONFIG7_J	3B00 0018h + formula
1Ch	32	GPMC_NAND_COMMAND_J	3B00 001Ch + formula
20h	32	GPMC_NAND_ADDRESS_J	3B00 0020h + formula
24h	32	GPMC_NAND_DATA_J	3B00 0024h + formula
0h	32	GPMC_BCH_RESULT_0_J	3B00 0000h + formula
4h	32	GPMC_BCH_RESULT_1_J	3B00 0004h + formula
8h	32	GPMC_BCH_RESULT_2_J	3B00 0008h + formula
Ch	32	GPMC_BCH_RESULT_3_J	3B00 000Ch + formula
0h	32	GPMC_BCH_RESULT_4_J	3B00 0000h + formula
4h	32	GPMC_BCH_RESULT_5_J	3B00 0004h + formula
8h	32	GPMC_BCH_RESULT_6_J	3B00 0008h + formula

14.9.4.4.2 GPMC Registers

GPMC Registers

14.9.4.4.2.1 GPMC_REVISION Register

1 GPMC_REVISION Register (Offset = 0h) [reset = 60h]

This register contains the IP revision code

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Table 14-29692. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h**

Figure 14-9839. GPMC_REVISION Name Register

31	30	29	28	27	26	25	24
RESERVED_230							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_230							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_230							
R							
0h							
7	6	5	4	3	2	1	0
REV							
R							
60h							

Table 14-29694. GPMC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_230	R	0h	Reads returns 0
7:0	REV	R	60h	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0, 0x21 for 2.1 Reset Source: func_mod_g_arst_n

14.9.4.4.2.2 GPMC_SYSCONFIG Register

1 GPMC_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register controls the various parameters of the OCP interface

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Table 14-29695. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0010h**

Figure 14-9840. GPMC_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_234							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_234							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_234							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_234			IDLEMODE		RESERVED_233	RESERVED	AUTOIDLE
R			R/W		R	R/W	R/W
0h			0h		0h	0h	0h

Table 14-29697. GPMC_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_234	R	0h	Write 0's for future compatibility Reads return 0
4:3	IDLEMODE	R/W	0h	Reset Source: func_mod_g_arst_n 0 Force-idle. An idle request is acknowledged unconditionally 1 No-idle. An idle request is never acknowledged 2 Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 3 reserved do not use
2	RESERVED_233	R	0h	Write 0 for future compatibility Reads returns 0
1	RESERVED	R/W	0h	This bit must be kept 0 for normal functioning of the IP. Do not set this bit to 1 0 Normal mode 1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: func_mod_g_arst_n 0 OCP clock is free-running 1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

14.9.4.4.2.3 GPMC_SYSSTATUS Register

1 GPMC_SYSSTATUS Register (Offset = 14h) [reset = 0h]

This register provides status information about the module, excluding the interrupt status information

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Table 14-29698. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0014h

Figure 14-9841. GPMC_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_235							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_235							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_235							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 14-29700. GPMC_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_235	R	0h	Reads returns 0
7:1	RESERVED	R	0h	Reads returns 0 [reserved for OCP-socket status information]
0	RESETDONE	R	0h	Internal reset monitoring Reset Source: func_mod_g_arst_n 0 Internal module reset in on-going 1 Reset completed

14.9.4.4.2.4 GPMC_IRQSTATUS Register

1 GPMC_IRQSTATUS Register (Offset = 18h) [reset = 0h]

This interrupt status register regroups all the status of the module internal events that can generate an interrupt.

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Table 14-29701. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0018h**

Figure 14-9842. GPMC_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_218							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_218							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_218				WAIT3EDGEDETECTIONSTATUS	WAIT2EDGEDETECTIONSTATUS	WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_219						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS
R						R/W1TC	R/W1TC
0h						0h	0h

Table 14-29703. GPMC_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_218	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT3 input pin has not been detected` 0 `Write 0: Wait3EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT3 input pin has been detected` 1 `Write 1: Wait3EdgeDetection status bit is reset`
10	WAIT2EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT2 input pin has not been detected` 0 `Write 0: Wait2EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT2 input pin has been detected` 1 `Write 1: Wait2EdgeDetection status bit is reset`

Table 14-29703. GPMC_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	WAIT1EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT1 input pin has not been detected` 0 `Write 0: Wait1EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT1 input pin has been detected` 1 `Write 1: Wait1EdgeDetection status bit is reset`
8	WAIT0EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT0 input pin has not been detected` 0 `Write 0: Wait0EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT0 input pin has been detected` 1 `Write 1: Wait0EdgeDetection status bit is reset`
7:2	RESERVED_219	R	0h	Write 0's for future compatibility. Read returns 0
1	TERMINALCOUNTSTATUS	R/W1TC	0h	Status of the TerminalCountEvent interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: Indicates that CountValue is greater than 0` 0 `Write 0: TerminalCountEvent status bit unchanged` 1 `Read 1: Indicates that CountValue is equal to 0` 1 `Write 1: TerminalCountEvent status bit is reset`
0	FIFOEVENTSTATUS	R/W1TC	0h	Status of the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: Indicates than less than FIFOThreshold bytes are available in prefetch mode and less than FIFOThreshold bytes free places are available in write posting mode.` 0 `Write 0: FIFOEvent status bit unchanged` 1 `Read 1: Indicates than at least FIFOThreshold bytes are available in prefetch mode and at least FIFOThreshold bytes free places are available in write posting mode.` 1 `Write 1: FIFOEvent status bit is reset`

14.9.4.4.2.5 GPMC_IRQENABLE Register

1 GPMC_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.

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Table 14-29704. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 001Ch**

Figure 14-9843. GPMC_IRQENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_216							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_216							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_216				WAIT3EDGEDETECTIONENABLE	WAIT2EDGEDETECTIONENABLE	WAIT1EDGEDETECTIONENABLE	WAIT0EDGEDETECTIONENABLE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_217						TERMINALCOUNTEVENTENABLE	FIFOEVENTENABLE
R						R/W	R/W
0h						0h	0h

Table 14-29706. GPMC_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_216	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3EDGEDETECTIONENABLE	R/W	0h	Enables the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait3EdgeDetection interrupt is masked 1 Wait3EdgeDetection event generates an interrupt if occurs
10	WAIT2EDGEDETECTIONENABLE	R/W	0h	Enables the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait2EdgeDetection interrupt is masked 1 Wait2EdgeDetection event generates an interrupt if occurs
9	WAIT1EDGEDETECTIONENABLE	R/W	0h	Enables the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait1EdgeDetection interrupt is masked 1 Wait1EdgeDetection event generates an interrupt if occurs

Table 14-29706. GPMC_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WAIT0EDGEDETECTIONENABLE	R/W	0h	Enables the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Wait0EdgeDetection interrupt is masked` 1 `Wait0EdgeDetection event generates an interrupt if occurs`
7:2	RESERVED_217	R	0h	Write 0's for future compatibility. Read returns 0
1	TERMINALCOUNTEVENTENABLE	R/W	0h	Enables TerminalCountEvent interrupt issuing in pre-fetch or write posting mode Reset Source: func_mod_g_arst_n 0 `TerminalCountEvent interrupt is masked` 1 `TerminalCountEvent interrupt is not masked`
0	FIFOEVENTENABLE	R/W	0h	Enables the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 0 `FIFOEvent interrupt is masked` 1 `FIFOEvent interrupt is not masked`

14.9.4.4.2.6 GPMC_TIMEOUT_CONTROL Register

1 GPMC_TIMEOUT_CONTROL Register (Offset = 40h) [reset = 1FF0h]

The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter

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Table 14-29707. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0040h**

Figure 14-9844. GPMC_TIMEOUT_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_237</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_237</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_237</td><td colspan="5">TIMEOUTSTARTVALUE</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TIMEOUTSTARTVALUE</td><td colspan="3">RESERVED_238</td><td>TIMEOUTENABLE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">1FFh</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-29709. GPMC_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_237	R	0h	Write 0's for future compatibility. Read returns 0
12:4	TIMEOUTSTARTVALUE	R/W	1FFh	Start value of the time-out counter [0x000 corresponds to 0 GPMC.FCLK cycle, 0x001 corresponds to 1 GmpcClk cycle, &, 0x1FF corresponds to 511 GPMC.FCLK cyles.] Reset Source: func_mod_g_arst_n
3:1	RESERVED_238	R	0h	Write 0's for future compatibility. Read returns 0
0	TIMEOUTENABLE	R/W	0h	Enable bit of the TimeOut feature Reset Source: func_mod_g_arst_n 0 TimeOut feature is disabled 1 TimeOut feature is enabled

14.9.4.4.2.7 GPMC_ERR_ADDRESS Register

1 GPMC_ERR_ADDRESS Register (Offset = 44h) [reset = 0h]

The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs

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Table 14-29710. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0044h**

Figure 14-9845. GPMC_ERR_ADDRESS Name Register

31	30	29	28	27	26	25	24
RESERVED_212	ILLEGALADD						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
ILLEGALADD							
R							
0h							
15	14	13	12	11	10	9	8
ILLEGALADD							
R							
0h							
7	6	5	4	3	2	1	0
ILLEGALADD							
R							
0h							

Table 14-29712. GPMC_ERR_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_212	R	0h	Write 0's for future compatibility. Read returns 0
30:0	ILLEGALADD	R	0h	Address of illegal access : A30[0 for memory region, 1 for GPMC register region] and A29-A0[1 GBytes maximum] Reset Source: func_mod_g_arst_n

14.9.4.4.2.8 GPMC_ERR_TYPE Register

1 GPMC_ERR_TYPE Register (Offset = 48h) [reset = 0h]

The GPMC_ERR_TYPE register stores the type of error when an error occurs

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Table 14-29713. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0048h

Figure 14-9846. GPMC_ERR_TYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_215</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_215</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED_215</td><td colspan="3">ILLEGALMCMD</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_213</td><td>ERRORNOTSUPPADD</td><td>ERRORNOTSUPPMCMD</td><td>ERRORTIMEOUT</td><td>RESERVED_214</td><td>ERRORVALID</td></tr>
<tr><td colspan="3">R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R/W1TC</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29715. GPMC_ERR_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED_215	R	0h	Write 0's for future compatibility. Read returns 0
10:8	ILLEGALMCMD	R	0h	System Command of the transaction that caused the error Reset Source: func_mod_g_arst_n
7:5	RESERVED_213	R	0h	Write 0's for future compatibility. Read returns 0

4	ERRORNOTSUPPADD	R	0h	Not supported Address error
				Reset Source: func_mod_g_arst_n
				`0 No error occurs`
				`1 The error is due to a non supported Address`

3	ERRORNOTSUPPMCMD	R	0h	Not supported Command error
				Reset Source: func_mod_g_arst_n
				`0 No error occurs`
				`1 The error is due to a non supported Command`

2	ERRORTIMEOUT	R	0h	Time-out error
				Reset Source: func_mod_g_arst_n
				`0 No error occurs`
				`1 The error is due to a time out`

1	RESERVED_214	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29715. GPMC_ERR_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ERRORVALID	R/W1TC	0h	Error validity status - Must be explicitely cleared with a write 1 transaction Reset Source: func_mod_g_arst_n 0 All error fields no longer valid 1 Error detected and logged in the other error fields

14.9.4.4.2.9 GPMC_CONFIG Register

1 GPMC_CONFIG Register (Offset = 50h) [reset = A00h]

The configuration register allows global configuration of the GPMC

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Table 14-29716. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0050h**

Figure 14-9847. GPMC_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_1</td><td>WAIT3PINPOLARITY</td><td>WAIT2PINPOLARITY</td><td>WAIT1PINPOLARITY</td><td>WAIT0PINPOLARITY</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>1h</td><td>0h</td><td>1h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_0</td><td>WRITEPROTECT</td><td colspan="2">RESERVED_2</td><td>LIMITEDADDRESS</td><td>NANDFORCEPOSTEDWRITE</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29718. GPMC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT3 Reset Source: func_mod_g_arst_n 0 `WAIT3 active low` 1 `WAIT3 active high`
10	WAIT2PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT2 Reset Source: func_mod_g_arst_n 0 `WAIT2 active low` 1 `WAIT2 active high`
9	WAIT1PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT1 Reset Source: func_mod_g_arst_n 0 `WAIT1 active low` 1 `WAIT1 active high`
8	WAIT0PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT0 Reset Source: func_mod_g_arst_n 0 `WAIT0 active low` 1 `WAIT0 active high`

Table 14-29718. GPMC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
4	WRITEPROTECT	R/W	0h	Controls the WP output pin level Reset Source: func_mod_g_arst_n 0 `WP output pin is low` 1 `WP output pin is high`
3:2	RESERVED_2	R	0h	Write 0's for future compatibility. Read returns 0
1	LIMITEDADDRESS	R/W	0h	Limited Address device support Reset Source: func_mod_g_arst_n 0 `No effect` 1 `A26-A11 are not modified during an external memory access.`
0	NANDFORCEPOSTEDWRITE	R/W	0h	Enables the Force Posted Write feature to NAND Cmd/Add/Data location Reset Source: func_mod_g_arst_n 0 `Disables  Force Posted Write` 1 `Enables Force Posted Write`

14.9.4.4.2.10 GPMC_STATUS Register

1 GPMC_STATUS Register (Offset = 54h) [reset = 1h]

The status register provides global status bits of the GPMC

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Table 14-29719. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0054h**

Figure 14-9848. GPMC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_231							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_231							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_231				WAIT3STATUS	WAIT2STATUS	WAIT1STATUS	WAIT0STATUS
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_232							EMPTYWRITEBUFFERSTATUS
R							R
0h							1h

Table 14-29721. GPMC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_231	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3STATUS	R	0h	Is a copy of input pin WAIT3. [Reset value is WAIT3 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT3 de-asserted` 1 `WAIT3 asserted`
10	WAIT2STATUS	R	0h	Is a copy of input pin WAIT2. [Reset value is WAIT2 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT2 de-asserted` 1 `WAIT2 asserted`
9	WAIT1STATUS	R	0h	Is a copy of input pin WAIT1. [Reset value is WAIT1 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT1 de-asserted` 1 `WAIT1 asserted`

Table 14-29721. GPMC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WAIT0STATUS	R	0h	Is a copy of input pin WAIT0. [Reset value is WAIT0 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT0 de-asserted` 1 `WAIT0 asserted`
7:1	RESERVED_232	R	0h	Write 0's for future compatibility Reads returns 0
0	EMPTYWRITEBUFFERSTATUS	R	1h	Stores the empty status of the write buffer Reset Source: func_mod_g_arst_n 0 `Write Buffer is not empty` 1 `Write Buffer is empty`

14.9.4.4.2.11 GPMC_PREFETCH_CONFIG1 Register

1 GPMC_PREFETCH_CONFIG1 Register (Offset = 1E0h) [reset = 4000h]

Prefetch engine configuration 1

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Table 14-29722. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01E0h**

Figure 14-9849. GPMC_PREFETCH_CONFIG1 Name Register

31	30	29	28	27	26	25	24
RESERVED_221	CYCLEOPTIMIZATION			ENABLEOPTIMIZEDACCESS	ENGINECSSELECTOR		
R	R/W			R/W	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
PFPWENROUNDROBIN	RESERVED_224			PFPWWEIGHTEDPRIO			
R/W	R			R/W			
0h	0h			0h			
15	14	13	12	11	10	9	8
RESERVED_220	FIFOTHRESHOLD						
R	R/W						
0h	40h						
7	6	5	4	3	2	1	0
ENABLEENGINE	RESERVED_223	WAITPINSELECTOR		SYNCHROMODE	DMAMODE	ENDIANISMTYPE	ACCESSMODE
R/W	R	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-29724. GPMC_PREFETCH_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_221	R	0h	Write 0's for future compatibility. Read returns 0
30:28	CYCLEOPTIMIZATION	R/W	0h	Define the number of GPMC.FCLK cycles to be substracted from RdCycleTime, WrCycleTime, AccessTime, CSRdOffTime, CSWrOffTime, ADVRdOffTime, ADVWrOffTime, OEOffTime, WEOffTime [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0x7 corresponds to 7 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
27	ENABLEOPTIMIZEDACCESS	R/W	0h	Enables access cycle optimization Reset Source: func_mod_g_arst_n 0 Access cycle optimization is disabled 1 Access cycle optimization is enabled
26:24	ENGINECSSELECTOR	R/W	0h	Selects the CS where Prefetch Postwrite engine is active [0x0 corresponds toCS0, 0x1 corresponds to CS1, &, 0x7 corresponds to CS7] Reset Source: func_mod_g_arst_n

Table 14-29724. GPMC_PREFETCH_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	PFPWENROUNDROBIN	R/W	0h	Enables the PFPW RoundRobin arbitration Reset Source: func_mod_g_arst_n 0 `Prefetch Postwrite engine round robin arbitration is disabled` 1 `Prefetch Postwrite engine round robin arbitration is enabled`
22:20	RESERVED_224	R	0h	Write 0's for future compatibility. Read returns 0
19:16	PFPWWEIGHTEDPRIO	R/W	0h	When an arbitration occurs between a direct memory access and a PFPW engine access, the direct memory access is always serviced. If the PFPWEnRoundRobin is enabled, 0x0 means : the next access is granted to the PFPW engine, 0x1 means : the two next accesses are granted to the PFPW engine, ..., 0xF means : the 16 next accesses are granted to the PFPW engine. Reset Source: func_mod_g_arst_n
15	RESERVED_220	R	0h	Write 0's for future compatibility. Read returns 0
14:8	FIFOTHRESHOLD	R/W	40h	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request [0x00 corresponds to 0 byte, 0x01 corresponds to 1 byte, &, 0x40 corresponds to 64 bytes] Reset Source: func_mod_g_arst_n
7	ENABLEENGINE	R/W	0h	Enables the Prefetch Postwite engine Reset Source: func_mod_g_arst_n 0 `Prefetch Postwrite engine is disabled` 1 `Prefetch Postwrite engine is enabled`
6	RESERVED_223	R	0h	Write 0's for future compatibility. Read returns 0
5:4	WAITPINSELECTOR	R/W	0h	Select which wait pin edge detector should start the engine in synchronized mode Reset Source: func_mod_g_arst_n 0 `Selects Wait0EdgeDetection` 1 `Selects Wait1EdgeDetection` 2 `Selects Wait2EdgeDetection` 3 `Selects Wait3EdgeDetection`
3	SYNCHROMODE	R/W	0h	Selects when the engine starts the access to CS Reset Source: func_mod_g_arst_n 0 `Engine starts the access to CS as soon as StartEngine is set` 1 `Engine starts the access to CS as soon as StartEngine is set AND wait to non wait edge detection on the selected wait pin`
2	DMAMODE	R/W	0h	Selects interrupt synchronization or DMA request synchronization Reset Source: func_mod_g_arst_n 0 `Interrupt synchronization is enabled. Only interrupt line will be activated on FIFO threshold crossing.` 1 `DMA request synchronization is enabled.A DMA request protocol is used.`
1	ENDIANISMTYPE	R/W	0h	Selects endianism for prefetch data [0x0 for Little Endian and 0x1 for Big Endian] Reset Source: func_mod_g_arst_n
0	ACCESSMODE	R/W	0h	Selects pre-fetch read or write posting accesses Reset Source: func_mod_g_arst_n 0 `Pre-fetch read mode` 1 `Write posting mode`

14.9.4.4.2.12 GPMC_PREFETCH_CONFIG2 Register

1 GPMC_PREFETCH_CONFIG2 Register (Offset = 1E4h) [reset = 0h]

Prefetch engine configuration 2

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Table 14-29725. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01E4h**

Figure 14-9850. GPMC_PREFETCH_CONFIG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_224</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_224</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_224</td><td colspan="6">TRANSFERCOUNT</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRANSFERCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29727. GPMC_PREFETCH_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_224	R	0h	Write 0's for future compatibility. Read returns 0
13:0	TRANSFERCOUNT	R/W	0h	Selects the number of bytes to be read or written by the engine to the selected CS [0x0000 corresponds to 0 byte, 0x0001 corresponds to 1 byte, &, 0x2000 corresponds to 8 Kbytes] Reset Source: func_mod_g_arst_n

14.9.4.4.2.13 GPMC_PREFETCH_CONTROL Register

1 GPMC_PREFETCH_CONTROL Register (Offset = 1ECh) [reset = 0h]

Prefetch engine control

Return to Summary Table

Table 14-29728. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01ECh**

Figure 14-9851. GPMC_PREFETCH_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED_225							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_225							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_225							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_225							STARTENGINE
R							R/W
0h							0h

Table 14-29730. GPMC_PREFETCH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_225	R	0h	Write 0's for future compatibility. Read returns 0
0	STARTENGINE	R/W	0h	Resets the FIFO pointer and starts the engine Reset Source: func_mod_g_arst_n 0 `write 0 stops the engine Read 0: engine is stopped` 1 `write 1 resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine. Read 1: engine is running`

14.9.4.4.2.14 GPMC_PREFETCH_STATUS Register

1 GPMC_PREFETCH_STATUS Register (Offset = 1F0h) [reset = 0h]

Prefetch engine status

Return to Summary Table

Table 14-29731. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F0h**

Figure 14-9852. GPMC_PREFETCH_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_227	FIFOPOINTER						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED_228							FIFOTHRESHOLDSTATUS
R							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED_226		COUNTVALUE					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
COUNTVALUE							
R							
0h							

Table 14-29733. GPMC_PREFETCH_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_227	R	0h	Write 0's for future compatibility. Read returns 0
30:24	FIFOPOINTER	R	0h	Number of available bytes to be read or number of free empty byte places to be written [0x00 corresponds to 0 byte available to be read or 0 free empty place to be written, &, 0x40 corresponds to 64 bytes available to be read or 64 empty places to be written] Reset Source: func_mod_g_arst_n
23:17	RESERVED_228	R	0h	Write 0's for future compatibility. Read returns 0
16	FIFOTHRESHOLDSTATUS	R	0h	Set when FIFOPointer exceeds FIFOThreshold value Reset Source: func_mod_g_arst_n 0 `FIFOPointer smaller or equal to FIFOThreshold. Writing to this bit has no effect` 1 `FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect`
15:14	RESERVED_226	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29733. GPMC_PREFETCH_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:0	COUNTVALUE	R	0h	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value [0x0000 corresponds to 0 byte remaining to be read or to be written, 0x0001 corresponds to 1 byte remaining to be read or to be written, &, 0x2000 corresponds to 8 Kbytes remaining to be read or to be written] Reset Source: func_mod_g_arst_n

14.9.4.4.2.15 GPMC_ECC_CONFIG Register

1 GPMC_ECC_CONFIG Register (Offset = 1F4h) [reset = 1030h]

ECC configuration

Return to Summary Table

Table 14-29734. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F4h**

Figure 14-9853. GPMC_ECC_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_206							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_206							ECCALGORITHM
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_205		ECCBCHTSEL		ECCWRAPMODE			
R		R/W		R/W			
0h		1h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC16B	ECCTOPSECTOR			ECCCS			ECCENABLE
R/W	R/W			R/W			R/W
0h	3h			0h			0h

Table 14-29736. GPMC_ECC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_206	R	0h	Write 0's for future compatibility. Read returns 0
16	ECCALGORITHM	R/W	0h	ECC algorithm used 0x0: Hamming code 0x1: BCH code Reset Source: func_mod_g_arst_n
15:14	RESERVED_205	R	0h	Write 0's for future compatibility. Read returns 0
13:12	ECCBCHTSEL	R/W	1h	Error correction capability used for BCH 0x0: up to 4 bits error correction [t = 4] 0x1: up to 8 bits error correction [t=8] 0x2: up to 16 bits error correction [t=16] 0x3: reserved Reset Source: func_mod_g_arst_n
11:8	ECCWRAPMODE	R/W	0h	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details Reset Source: func_mod_g_arst_n
7	ECC16B	R/W	0h	Selects an ECC calculated on 16 columns Reset Source: func_mod_g_arst_n 0 ECC calculated on 8 columns 1 ECC calculated on 16 columns

Table 14-29736. GPMC_ECC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	ECCTOPSECTOR	R/W	3h	Number of sectors to process with the BCH algorithm 0x0: 1 sector [512kB page] 0x1: 2 sectors ... 0x3: 4 sectors [2kB page] ... 0x7: 8 sectors [4kB page] Reset Source: func_mod_g_arst_n
3:1	ECCCS	R/W	0h	Selects the CS where ECC is computed Reset Source: func_mod_g_arst_n 0 Chip select 0 1 Chip select 1 2 Chip select 2 3 Chip select 3 4 Chip select 4 5 Chip select 5 6 Chip select 6 7 Chip select 7
0	ECCENABLE	R/W	0h	Enables the ECC feature Reset Source: func_mod_g_arst_n 0 ECC disabled 1 ECC enabled

14.9.4.4.2.16 GPMC_ECC_CONTROL Register

1 GPMC_ECC_CONTROL Register (Offset = 1F8h) [reset = 0h]

ECC control

Return to Summary Table

Table 14-29737. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F8h**

Figure 14-9854. GPMC_ECC_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED_207							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_207							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_207							ECCCLEAR
R							R/W1TC
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_208				ECCPOINTER			
R				R/W			
0h				0h			

Table 14-29739. GPMC_ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_207	R	0h	Write 0's for future compatibility. Read returns 0
8	ECCCLEAR	R/W1TC	0h	Clear all ECC result registers [Reads returns 0 - Writes 1 to this field clear all ECC result registers - Writes 0 are ignored] Reset Source: func_mod_g_arst_n
7:4	RESERVED_208	R	0h	Write 0's for future compatibility. Read returns 0
3:0	ECCPOINTER	R/W	0h	Selects ECC result register [Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored]; Other enums: Writing other values disables the ECC engine [ECCEnable bit of GPMC_ECC_CONFIG set to 0] Reset Source: func_mod_g_arst_n 0 writing 0000 disables the ECC engine (ECCEnable bit of GPMC_ECC_CONFIG set to 0) 1 ECC result register 1 is selected 2 ECC result register 2 is selected 3 ECC result register 3 is selected 4 ECC result register 4 is selected 5 ECC result register 5 is selected 6 ECC result register 6 is selected 7 ECC result register 7 is selected 8 ECC result register 8 is selected 9 ECC result register 9 is selected

14.9.4.4.2.17 GPMC_ECC_SIZE_CONFIG Register

1 GPMC_ECC_SIZE_CONFIG Register (Offset = 1FCh) [reset = FFFFF000h]

ECC size

Return to Summary Table

Table 14-29740. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01FCh**

Figure 14-9855. GPMC_ECC_SIZE_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ECCSIZE1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">ECCSIZE1</td><td colspan="6">ECCSIZE0</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">3FFh</td><td colspan="6">3FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">ECCSIZE0</td><td colspan="3">RESERVED_209</td><td>ECC9RESULTSIZE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">3FFh</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ECC8RESULTSIZE</td><td>ECC7RESULTSIZE</td><td>ECC6RESULTSIZE</td><td>ECC5RESULTSIZE</td><td>ECC4RESULTSIZE</td><td>ECC3RESULTSIZE</td><td>ECC2RESULTSIZE</td><td>ECC1RESULTSIZE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29742. GPMC_ECC_SIZE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	ECCSIZE1	R/W	3FFh	Defines ECC size 1 [For Hamming Code: 0x000 corresponds to 2 Bytes, 0x001 corresponds to 4 Bytes, 0x002 corresponds to 6 Bytes, 0x003 corresponds to 8 Bytes, &, 0x0FF corresponds to 512 Bytes. Max supported value is 0x0FF.] [For BCH: 0x000 corresponds to 0 nibbles, 0x001 corresponds to 1 nibble, 0x002 corresponds to 2 nibbles, 0x003 corresponds to 3 nibbles, &, 0x3FF corresponds to 1023 nibbles.] Reset Source: func_mod_g_arst_n
21:12	ECCSIZE0	R/W	3FFh	Defines ECC size 0 [For Hamming Code: 0x000 corresponds to 2 Bytes, 0x001 corresponds to 4 Bytes, 0x002 corresponds to 6 Bytes, 0x003 corresponds to 8 Bytes, &, 0x0FF corresponds to 512 Bytes. Max supported value is 0x0FF.] [For BCH: 0x000 corresponds to 0 nibbles, 0x001 corresponds to 1 nibble, 0x002 corresponds to 2 nibbles, 0x003 corresponds to 3 nibbles, &, 0x3FF corresponds to 1023 nibbles.] Reset Source: func_mod_g_arst_n
11:9	RESERVED_209	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29742. GPMC_ECC_SIZE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ECC9RESULTSIZE	R/W	0h	Selects ECC size for ECC 9 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
7	ECC8RESULTSIZE	R/W	0h	Selects ECC size for ECC 8 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
6	ECC7RESULTSIZE	R/W	0h	Selects ECC size for ECC 7 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
5	ECC6RESULTSIZE	R/W	0h	Selects ECC size for ECC 6 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
4	ECC5RESULTSIZE	R/W	0h	Selects ECC size for ECC 5 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
3	ECC4RESULTSIZE	R/W	0h	Selects ECC size for ECC 4 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
2	ECC3RESULTSIZE	R/W	0h	Selects ECC size for ECC 3 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
1	ECC2RESULTSIZE	R/W	0h	Selects ECC size for ECC 2 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
0	ECC1RESULTSIZE	R/W	0h	Selects ECC size for ECC 1 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`

14.9.4.4.2.18 GPMC_ECC_RESULT_j Register

1 GPMC_ECC_RESULT_j Register (Offset = 200h + formula) [reset = 0h]

ECC result register

Return to Summary Table

Offset = 260h + (j * 4h); where j = 0 to 8d

Table 14-29743. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0200h + formula**

Figure 14-9856. GPMC_ECC_RESULT_j Name Register

31	30	29	28	27	26	25	24
RESERVED_188				P2048O	P1024O	P512O	P256O
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P128O	P64O	P32O	P16O	P8O	P4O	P2O	P1O
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_187				P2048E	P1024E	P512E	P256E
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P128E	P64E	P32E	P16E	P8E	P4E	P2E	P1E
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29745. GPMC_ECC_RESULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_188	R	0h	Write 0's for future compatibility. Read returns 0
27	P2048O	R	0h	Odd Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
26	P1024O	R	0h	Odd Row Parity bit 1024 Reset Source: func_mod_g_arst_n
25	P512O	R	0h	Odd Row Parity bit 512 Reset Source: func_mod_g_arst_n
24	P256O	R	0h	Odd Row Parity bit 256 Reset Source: func_mod_g_arst_n
23	P128O	R	0h	Odd Row Parity bit 128 Reset Source: func_mod_g_arst_n
22	P64O	R	0h	Odd Row Parity bit 64 Reset Source: func_mod_g_arst_n
21	P32O	R	0h	Odd Row Parity bit 32 Reset Source: func_mod_g_arst_n

Table 14-29745. GPMC_ECC_RESULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	P16O	R	0h	Odd Row Parity bit 16 Reset Source: func_mod_g_arst_n
19	P8O	R	0h	Odd Row Parity bit 8 Reset Source: func_mod_g_arst_n
18	P4O	R	0h	Odd Column Parity bit 4 Reset Source: func_mod_g_arst_n
17	P2O	R	0h	Odd Column Parity bit 2 Reset Source: func_mod_g_arst_n
16	P1O	R	0h	Odd Column Parity bit 1 Reset Source: func_mod_g_arst_n
15:12	RESERVED_187	R	0h	Write 0's for future compatibility. Read returns 0
11	P2048E	R	0h	Even Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
10	P1024E	R	0h	Even Row Parity bit 1024 Reset Source: func_mod_g_arst_n
9	P512E	R	0h	Even Row Parity bit 512 Reset Source: func_mod_g_arst_n
8	P256E	R	0h	Even Row Parity bit 256 Reset Source: func_mod_g_arst_n
7	P128E	R	0h	Even Row Parity bit 128 Reset Source: func_mod_g_arst_n
6	P64E	R	0h	Even Row Parity bit 64 Reset Source: func_mod_g_arst_n
5	P32E	R	0h	Even Row Parity bit 32 Reset Source: func_mod_g_arst_n
4	P16E	R	0h	Even Row Parity bit 16 Reset Source: func_mod_g_arst_n
3	P8E	R	0h	Even Row Parity bit 8 Reset Source: func_mod_g_arst_n
2	P4E	R	0h	Even Column Parity bit 4 Reset Source: func_mod_g_arst_n
1	P2E	R	0h	Even Column Parity bit 2 Reset Source: func_mod_g_arst_n
0	P1E	R	0h	Even Column Parity bit 1 Reset Source: func_mod_g_arst_n

14.9.4.4.2.19 GPMC_BCH_SWDATA Register

1 GPMC_BCH_SWDATA Register (Offset = 2D0h) [reset = 0h]

This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.

Return to Summary Table

Table 14-29746. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 02D0h**

Figure 14-9857. GPMC_BCH_SWDATA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BCH_DATA</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BCH_DATA</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29748. GPMC_BCH_SWDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved
15:0	BCH_DATA	W	0h	Data to be included in the BCH calculation. Only bits 0 to 7 are taken into account if the calculator is configured to use 8 bits data [ECC16B = 0] Reset Source: func_mod_g_arst_n

14.9.4.4.2.20 GPMC_CONFIG1_j Register

1 GPMC_CONFIG1_j Register (Offset = 0h + formula) [reset = 0h]

The configuration 1 register sets signal control parameters per chip select

Return to Summary Table

Offset = 60h + (j * 30h); where j = 0 to 7d

Table 14-29749. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h + formula**

Figure 14-9858. GPMC_CONFIG1_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WRAPBURST</td><td>READMULTIPLE</td><td>READTYPE</td><td>WRITEMULTIPLE</td><td>WRITETYPE</td><td colspan="2">CLKACTIVATIONTIME</td><td>ATTACHEDDEVICEPAGELENGTH</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>ATTACHEDDEVICEPAGELENGTH</td><td>WAITREADMONITORING</td><td>WAITWRITEMONITORING</td><td>RESERVED_9</td><td colspan="2">WAITMONITORINGTIME</td><td colspan="2">WAITPINSELECT</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_11</td><td colspan="2">DEVICESIZE</td><td colspan="2">DEVICETYPE</td><td colspan="2">MUXADDDATA</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_12</td><td>TIMEPARAGRANULARITY</td><td colspan="2">RESERVED_10</td><td colspan="2">GPMCFCLKDIVIDER</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-29751. GPMC_CONFIG1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRAPBURST	R/W	0h	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst Reset Source: func_mod_g_arst_n 0 `Synchronous wrapping burst not supported` 1 `Synchronous wrapping burst supported`
30	READMULTIPLE	R/W	0h	Selects the read single or multiple access Reset Source: func_mod_g_arst_n 0 `single access` 1 `multiple access (burst if synchonous, page if asynchronous)`
29	READTYPE	R/W	0h	Selects the read mode operation Reset Source: func_mod_g_arst_n 0 `Read Asynchronous` 1 `Read Synchronous`

Table 14-29751. GPMC_CONFIG1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	WRITEMULTIPLE	R/W	0h	Selects the write single or multiple access Reset Source: func_mod_g_arst_n 0 single access 1 multiple access (burst if synchonous, considered as single if asynchronous)
27	WRITETYPE	R/W	0h	Selects the write mode operation Reset Source: func_mod_g_arst_n 0 Write Asynchronous 1 Write Synchronous
26:25	CLKACTIVATIONTIME	R/W	0h	Output GPMC.CLK activation time Reset Source: func_mod_g_arst_n 0 First rising edge of GPMC.CLK at Start Access Time 1 First rising edge of GPMC.CLK one GPMC.FCLK cycle after Start Access Time 2 First rising edge of GPMC.CLK two GPMC.FCLK cycles after Start Access Time 3 not defined
24:23	ATTACHEDDEVICEPAGELENGTH	R/W	0h	Specifies the attached device page [burst] length Reset Source: func_mod_g_arst_n 0 4 Words 1 8 Words 2 16 Words 3 32 Words
22	WAITREADMONITORING	R/W	0h	Selects the Wait monitoring configuration for Read accesses [Reset value is BOOTWAITEN input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 Wait pin is not monitored for read accesses 1 Wait pin is monitored for read accesses
21	WAITWRITEMONITORING	R/W	0h	Selects the Wait monitoring configuration for Write accesses Reset Source: func_mod_g_arst_n 0 Wait pin is not monitored for write accesses 1 Wait pin is monitored for write accesses
20	RESERVED_9	R	0h	Write 0's for future compatibility. Read returns 0
19:18	WAITMONITORINGTIME	R/W	0h	Selects input pin Wait monitoring time Reset Source: func_mod_g_arst_n 0 Wait pin is monitored with valid data 1 Wait pin is monitored one GPMC.CLK cycle before valid data 2 Wait pin is monitored two GPMC.CLK cycle before valid data 3 not defined
17:16	WAITPINSELECT	R/W	0h	Selects the input WAIT pin for this chip select [Reset value is BOOTWAITSELECT input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Wait input pin is WAIT0 1 Wait input pin is WAIT1 2 Wait input pin is WAIT2 3 Wait input pin is WAIT3
15:14	RESERVED_11	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29751. GPMC_CONFIG1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	DEVICESIZE	R/W	0h	Selects the device size attached [Reset value is BOOTDEVICESIZE input pin sampled at IC reset for CS0 and 01 for CS1-7] Reset Source: func_mod_g_arst_n 0 8 bit 1 16 bit 2 32 bit 3 reserved
11:10	DEVICETYPE	R/W	0h	Selects the attached device type Reset Source: func_mod_g_arst_n 0 NOR Flash, pSRAM, asynchronous devices 1 reserved 2 NAND Flash stream mode 3 reserved
9:8	MUXADDDATA	R/W	0h	Enables the Address and data multiplexed protocol [Reset value is CS0MUXDEVICE input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Non Multiplexed attached device 1 AAD-Mux protocol device 2 Address and data multiplexed attached device 3 Reserved
7:5	RESERVED_12	R	0h	Write 0's for future compatibility. Read returns 0
4	TIMEPARAGRANULARITY	R/W	0h	Signals timing latencies scalar factor [Rd/WRCycleTime, AccessTime, PageBurstAccessTime, CSOnTime, CSRd/WrOffTime, ADVOnTime, ADVRd/WrOffTime, OEOnTime, OEOffTime, WEOnTime, WEOffTime, Cycle2CycleDelay, BusTurnAround, TimeOutStartValue] Reset Source: func_mod_g_arst_n 0 x1 latencies 1 x2 latencies
3:2	RESERVED_10	R	0h	Write 0's for future compatibility. Read returns 0
1:0	GPMCFCLKDIVIDER	R/W	0h	Divides the GPMC.FCLK clock Reset Source: func_mod_g_arst_n 0 GPMC.CLK frequency = GPMC.FCLK frequency 1 GPMC.CLK frequency = GPMC.FCLK frequency / 2 2 GPMC.CLK frequency = GPMC.FCLK frequency / 3 3 GPMC.CLK frequency = GPMC.FCLK frequency /4

14.9.4.4.2.21 GPMC_CONFIG2_j Register

1 GPMC_CONFIG2_j Register (Offset = 4h + formula) [reset = 101001h]

Chip-select signal timing parameter configuration

Return to Summary Table

Offset = 64h + (j * 30h); where j = 0 to 7d

Table 14-29752. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0004h + formula**

Figure 14-9859. GPMC_CONFIG2_j Name Register

31	30	29	28	27	26	25	24
RESERVED_43							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_43			CSWROFFTIME				
R			R/W				
0h			10h				
15	14	13	12	11	10	9	8
RESERVED_45			CSRDOFFTIME				
R			R/W				
0h			10h				
7	6	5	4	3	2	1	0
CSEXTRADELAY	RESERVED_44			CSONTIME			
R/W	R			R/W			
0h	0h			1h			

Table 14-29754. GPMC_CONFIG2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED_43	R	0h	Write 0's for future compatibility Reads returns 0
20:16	CSWROFFTIME	R/W	10h	CS# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_45	R	0h	Write 0's for future compatibility. Read returns 0
12:8	CSRDOFFTIME	R/W	10h	CS# de-assertion time from start cycle time for read accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	CSEXTRADELAY	R/W	0h	CS# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 `CS# Timing control signal is not delayed` 1 `CS# Timing control signal is delayed of half GPMC.FCLK clock cycle`
6:4	RESERVED_44	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29754. GPMC_CONFIG2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CSONTIME	R/W	1h	CS# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.4.4.2.22 GPMC_CONFIG3_j Register

1 GPMC_CONFIG3_j Register (Offset = 8h + formula) [reset = 22060514h]

ADV# signal timing parameter configuration

Return to Summary Table

Offset = 68h + (j * 30h); where j = 0 to 7d

Table 14-29755. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0008h + formula

Figure 14-9860. GPMC_CONFIG3_j Name Register

31	30	29	28	27	26	25	24
RESERVED_1	ADVAADMUXWROFFTIME			RESERVED_0	ADVAADMUXRDOFFTIME		
R	R/W			R	R/W		
0h	2h			0h	2h		
23	22	21	20	19	18	17	16
RESERVED_68			ADVWROFFTIME				
R			R/W				
0h			6h				
15	14	13	12	11	10	9	8
RESERVED_69			ADVRDOFFTIME				
R			R/W				
0h			5h				
7	6	5	4	3	2	1	0
ADVEXTRADELAY	ADVAADMUXONTIME			ADVONTIME			
R/W	R/W			R/W			
0h	1h			4h			

Table 14-29757. GPMC_CONFIG3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
30:28	ADVAADMUXWROFFTIME	R/W	2h	ADV# de-assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
27	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
26:24	ADVAADMUXRDOFFTIME	R/W	2h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
23:21	RESERVED_68	R	0h	Write 0's for future compatibility. Read returns 0
20:16	ADVWROFFTIME	R/W	6h	ADV# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_69	R	0h	Write 0's for future compatibility. Read returns 0
12:8	ADVRDOFFTIME	R/W	5h	ADV# de-assertion time from start cycle time for read accesses[0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-29757. GPMC_CONFIG3_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ADVEXTRADELAY	R/W	0h	ADV# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 `ADV# Timing control signal is not delayed` 1 `ADV# Timing control signal is delayed of half GPMC.FCLK clock cycle`
6:4	ADVAADMUXONTIME	R/W	1h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
3:0	ADVONTIME	R/W	4h	ADV# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.4.4.2.23 GPMC_CONFIG4_j Register

1 GPMC_CONFIG4_j Register (Offset = Ch + formula) [reset = 10057016h]

WE# and OE# signals timing parameter configuration

Return to Summary Table

Offset = 6Ch + (j * 30h); where j = 0 to 7d

Table 14-29758. Instance Table

Instance Name	Physical Address
GPMC0	3B00 000Ch + formula

Figure 14-9861. GPMC_CONFIG4_j Name Register

31	30	29	28	27	26	25	24
RESERVED			WEOFFTIME				
R			R/W				
0h			10h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WEEXTRADELAY	RESERVED_92			WEONTIME			
R/W	R			R/W			
0h	0h			5h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OEAADMUXOFFTIME			OEOFFTIME				
R/W			R/W				
3h			10h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OEEXTRADELAY	OEAADMUXONTIME			OEONTIME			
R/W	R/W			R/W			
0h	1h			6h			

Table 14-29760. GPMC_CONFIG4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	R	0h	Write 0's for future compatibility. Read returns 0
28:24	WEOFFTIME	R/W	10h	WE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23	WEEXTRADELAY	R/W	0h	WE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 `WE# Timing control signal is not delayed` 1 `WE# Timing control signal is delayed of half GPMC.FCLK clock cycle`
22:20	RESERVED_92	R	0h	Write 0's for future compatibility. Read returns 0
19:16	WEONTIME	R/W	5h	WE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-29760. GPMC_CONFIG4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	OEAADMUXOFFTIME	R/W	3h	OE# de-assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n
12:8	OEOFFTIME	R/W	10h	OE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	OEEXTRADELAY	R/W	0h	OE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 `OE# Timing control signal is not delayed` 1 `OE# Timing control signal is delayed of half GPMC.FCLK clock cycle`
6:4	OEAADMUXONTIME	R/W	1h	OE# assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n
3:0	OEONTIME	R/W	6h	OE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.4.4.2.24 GPMC_CONFIG5_j Register

1 GPMC_CONFIG5_j Register (Offset = 10h + formula) [reset = 10F1111h]

RdAccessTime and CycleTime timing parameters configuration

Return to Summary Table

Offset = 70h + (j * 30h); where j = 0 to 7d

Table 14-29761. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0010h + formula**

Figure 14-9862. GPMC_CONFIG5_j Name Register

31	30	29	28	27	26	25	24
RESERVED_124				PAGEBURSTACCESSTIME			
R				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_125			RDACCESSTIME				
R			R/W				
0h			Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_126			WRCYCLETIME				
R			R/W				
0h			11h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_123			RDCYCLETIME				
R			R/W				
0h			11h				

Table 14-29763. GPMC_CONFIG5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_124	R	0h	Write 0's for future compatibility. Read returns 0
27:24	PAGEBURSTACCESSTIME	R/W	1h	Delay between successive words in a multiple access [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:21	RESERVED_125	R	0h	Write 0's for future compatibility. Read returns 0
20:16	RDACCESSTIME	R/W	Fh	Delay between start cycle time and first data valid [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_126	R	0h	Write 0's for future compatibility Reads returns 0
12:8	WRCYCLETIME	R/W	11h	Total write cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7:5	RESERVED_123	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-29763. GPMC_CONFIG5_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	RDCYCLETIME	R/W	11h	Total read cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.4.4.2.25 GPMC_CONFIG6_j Register

1 GPMC_CONFIG6_j Register (Offset = 14h + formula) [reset = 8F070000h]

WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration

Return to Summary Table

Offset = 74h + (j * 30h); where j = 0 to 7d

Table 14-29764. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0014h + formula**

Figure 14-9863. GPMC_CONFIG6_j Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED_0		WRACCESSTIME				
R/W	R		R/W				
1h	0h		Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_155				WRDATAONADMUXBUS			
R				R/W			
0h				7h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				CYCLE2CYCLEDELAY			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYCLE2CYCLE SAMECSEN	CYCLE2CYCLE DIFFCSEN	RESERVED_156		BUSTURNAROUND			
R/W	R/W	R		R/W			
0h	0h	0h		0h			

Table 14-29766. GPMC_CONFIG6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	1h	TI Internal use - Do not modify
30:29	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
28:24	WRACCESSTIME	R/W	Fh	Delay from StartAccessTime to the GPMC.FCLK rising edge corresponding the the GPMC.CLK rising edge used by the attached memory for the first data capture [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:20	RESERVED_155	R	0h	Write 0's for future compatibility. Read returns 0
19:16	WRDATAONADMUXBUS	R/W	7h	Specifies on which GPMC.FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus Reset Source: func_mod_g_arst_n
15:12	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
11:8	CYCLE2CYCLEDELAY	R/W	0h	Chip select high pulse delay between two successive accesses [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-29766. GPMC_CONFIG6_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CYCLE2CYCLESAMECSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to the same chip-select [any access type] Reset Source: func_mod_g_arst_n 0 `No delay between the two accesses` 1 `Add Cycle2CycleDelay`
6	CYCLE2CYCLEDIFFCSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to a different chip-select [any access type] Reset Source: func_mod_g_arst_n 0 `No delay between the two accesses` 1 `Add Cycle2CycleDelay`
5:4	RESERVED_156	R	0h	Write 0's for future compatibility Reads returns 0
3:0	BUSTURNAROUND	R/W	0h	Bus turn around latency between two successive accesses to the same chip-select [rd to wr] or to a different chip-select [read to read and read to write] [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.4.4.2.26 GPMC_CONFIG7_j Register

1 GPMC_CONFIG7_j Register (Offset = 18h + formula) [reset = F40h]

Chip-select address mapping configuration Note: For CS0, the register reset is 0xf40 while for all the other instances CS1-CS7, the reset is 0xf00.

Return to Summary Table

Offset = 78h + (j * 30h); where j = 0 to 7d

Table 14-29767. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0018h + formula**

Figure 14-9864. GPMC_CONFIG7_j Name Register

31	30	29	28	27	26	25	24
RESERVED_171							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_171							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_171				MASKADDRESS			
R				R/W			
0h				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_172	CSVALID	BASEADDRESS					
R	R/W	R/W					
0h	1h	0h					

Table 14-29769. GPMC_CONFIG7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_171	R	0h	Write 0's for future compatibility. Read returns 0
11:8	MASKADDRESS	R/W	Fh	Chip-select mask address Reset Source: func_mod_g_arst_n
7	RESERVED_172	R	0h	Write 0's for future compatibility. Read returns 0
6	CSVALID	R/W	1h	Chip-select enable [reset value is 1 for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Chip-select disabled 1 Chip-select enabled
5:0	BASEADDRESS	R/W	0h	Chip-select base address Reset Source: func_mod_g_arst_n

14.9.4.4.2.27 GPMC_NAND_COMMAND_j Register

1 GPMC_NAND_COMMAND_j Register (Offset = 1Ch + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = 7Ch + (j * 30h); where j = 0 to 7d

Table 14-29770. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 001Ch + formula**

Figure 14-9865. GPMC_NAND_COMMAND_j Name Register

31	30	29	28	27	26	25	24
GPMC_NAND_COMMAND_0							
W							
0h							
23	22	21	20	19	18	17	16
GPMC_NAND_COMMAND_0							
W							
0h							
15	14	13	12	11	10	9	8
GPMC_NAND_COMMAND_0							
W							
0h							
7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND_0							
W							
0h							

Table 14-29772. GPMC_NAND_COMMAND_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_COMMAND_0	W	0h	Reset Source: func_mod_g_arst_n

14.9.4.4.2.28 GPMC_NAND_ADDRESS_j Register

1 GPMC_NAND_ADDRESS_j Register (Offset = 20h + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = 80h + (j * 30h); where j = 0 to 7d

Table 14-29773. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0020h + formula**

Figure 14-9866. GPMC_NAND_ADDRESS_j Name Register

31	30	29	28	27	26	25	24
GPMC_NAND_ADDRESS_0							
W							
0h							
23	22	21	20	19	18	17	16
GPMC_NAND_ADDRESS_0							
W							
0h							
15	14	13	12	11	10	9	8
GPMC_NAND_ADDRESS_0							
W							
0h							
7	6	5	4	3	2	1	0
GPMC_NAND_ADDRESS_0							
W							
0h							

Table 14-29775. GPMC_NAND_ADDRESS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_ADDRESS_0	W	0h	Reset Source: func_mod_g_arst_n

14.9.4.4.2.29 GPMC_NAND_DATA_j Register

1 GPMC_NAND_DATA_j Register (Offset = 24h + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = 84h + (j * 30h); where j = 0 to 7d

Table 14-29776. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0024h + formula**

Figure 14-9867. GPMC_NAND_DATA_j Name Register

31	30	29	28	27	26	25	24
GPMC_NAND_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
GPMC_NAND_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
GPMC_NAND_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
GPMC_NAND_DATA_0							
R/W							
0h							

Table 14-29778. GPMC_NAND_DATA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_DATA_0	R/W	0h	Reset Source: func_mod_g_arst_n

14.9.4.4.2.30 GPMC_BCH_RESULT_0_j Register

1 GPMC_BCH_RESULT_0_j Register (Offset = 0h + formula) [reset = 0h]

BCH ECC result, bits 0 to 31

Return to Summary Table

Offset = 240h + (j * 10h); where j = 0 to 7d

Table 14-29779. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h + formula**

Figure 14-9868. GPMC_BCH_RESULT_0_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_0							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_0							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_0							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_0							
R							
0h							

Table 14-29781. GPMC_BCH_RESULT_0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_0	R	0h	BCH ECC result, bits 0 to 31 Reset Source: func_mod_g_arst_n

14.9.4.4.2.31 GPMC_BCH_RESULT_1_j Register

1 GPMC_BCH_RESULT_1_j Register (Offset = 4h + formula) [reset = 0h]

BCH ECC result, bits 32 to 63

Return to Summary Table

Offset = 244h + (j * 10h); where j = 0 to 7d

Table 14-29782. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0004h + formula**

Figure 14-9869. GPMC_BCH_RESULT_1_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_1							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_1							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_1							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_1							
R							
0h							

Table 14-29784. GPMC_BCH_RESULT_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_1	R	0h	BCH ECC result, bits 32 to 63 Reset Source: func_mod_g_arst_n

14.9.4.4.2.32 GPMC_BCH_RESULT_2_j Register

1 GPMC_BCH_RESULT_2_j Register (Offset = 8h + formula) [reset = 0h]

BCH ECC result, bits 64 to 95

Return to Summary Table

Offset = 248h + (j * 10h); where j = 0 to 7d

Table 14-29785. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0008h + formula**

Figure 14-9870. GPMC_BCH_RESULT_2_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_2							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_2							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_2							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_2							
R							
0h							

Table 14-29787. GPMC_BCH_RESULT_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_2	R	0h	BCH ECC result, bits 64 to 95 Reset Source: func_mod_g_arst_n

14.9.4.4.2.33 GPMC_BCH_RESULT_3_j Register

1 GPMC_BCH_RESULT_3_j Register (Offset = Ch + formula) [reset = 0h]

BCH ECC result, bits 96 to 127

Return to Summary Table

Offset = 24Ch + (j * 10h); where j = 0 to 7d

Table 14-29788. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 000Ch + formula**

Figure 14-9871. GPMC_BCH_RESULT_3_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_3							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_3							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_3							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_3							
R							
0h							

Table 14-29790. GPMC_BCH_RESULT_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_3	R	0h	BCH ECC result, bits 96 to 127 Reset Source: func_mod_g_arst_n

14.9.4.4.2.34 GPMC_BCH_RESULT_4_j Register

1 GPMC_BCH_RESULT_4_j Register (Offset = 0h + formula) [reset = 0h]

BCH ECC result, bits 128 to 159

Return to Summary Table

Offset = 300h + (j * 10h); where j = 0 to 7d

Table 14-29791. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h + formula**

Figure 14-9872. GPMC_BCH_RESULT_4_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_4							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_4							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_4							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_4							
R							
0h							

Table 14-29793. GPMC_BCH_RESULT_4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_4	R	0h	BCH ECC result, bits 128 to 159 Reset Source: func_mod_g_arst_n

14.9.4.4.2.35 GPMC_BCH_RESULT_5_j Register

1 GPMC_BCH_RESULT_5_j Register (Offset = 4h + formula) [reset = 0h]

BCH ECC result, bits 160 to 191

Return to Summary Table

Offset = 304h + (j * 10h); where j = 0 to 7d

Table 14-29794. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0004h + formula**

Figure 14-9873. GPMC_BCH_RESULT_5_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_5							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_5							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_5							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_5							
R							
0h							

Table 14-29796. GPMC_BCH_RESULT_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_5	R	0h	BCH ECC result, bits 160 to 191 Reset Source: func_mod_g_arst_n

14.9.4.4.2.36 GPMC_BCH_RESULT_6_j Register

1 GPMC_BCH_RESULT_6_j Register (Offset = 8h + formula) [reset = 0h]

BCH ECC result, bits 192 to 207

Return to Summary Table

Offset = 308h + (j * 10h); where j = 0 to 7d

Table 14-29797. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0008h + formula**

Figure 14-9874. GPMC_BCH_RESULT_6_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
BCH_RESULT_6							
R							
0h							

7	6	5	4	3	2	1	0
BCH_RESULT_6							
R							
0h							

Table 14-29799. GPMC_BCH_RESULT_6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved
15:0	BCH_RESULT_6	R	0h	BCH ECC result, bits 192 to 207 Reset Source: func_mod_g_arst_n

14.9.4.5 ELM

ELM

14.9.4.5.1 ELM Summaries

ELM Summaries

Table 14-29800. ELM Registers, Base Address=2501 0000h, Length=4096

Offset	Length	Register Name	ELM0 Physical Address
0h	32	ELM_REVISION	2501 0000h
10h	32	ELM_SYSCONFIG	2501 0010h
14h	32	ELM_SYSSTS	2501 0014h
18h	32	ELM_IRQSTS	2501 0018h
1Ch	32	ELM_IRQEN	2501 001Ch
20h	32	ELM_LOCATION_CONFIG	2501 0020h
80h	32	ELM_PAGE_CTRL	2501 0080h
0h	32	ELM_SYNDROME_FRAGMENT_0_J	2501 0000h + formula
4h	32	ELM_SYNDROME_FRAGMENT_1_J	2501 0004h + formula
8h	32	ELM_SYNDROME_FRAGMENT_2_J	2501 0008h + formula
Ch	32	ELM_SYNDROME_FRAGMENT_3_J	2501 000Ch + formula
10h	32	ELM_SYNDROME_FRAGMENT_4_J	2501 0010h + formula
14h	32	ELM_SYNDROME_FRAGMENT_5_J	2501 0014h + formula
18h	32	ELM_SYNDROME_FRAGMENT_6_J	2501 0018h + formula
0h	32	ELM_LOCATION_STS_J	2501 0000h + formula
80h	32	ELM_ERROR_LOCATION_0_J	2501 0080h + formula
84h	32	ELM_ERROR_LOCATION_1_J	2501 0084h + formula
88h	32	ELM_ERROR_LOCATION_2_J	2501 0088h + formula
8Ch	32	ELM_ERROR_LOCATION_3_J	2501 008Ch + formula
90h	32	ELM_ERROR_LOCATION_4_J	2501 0090h + formula
94h	32	ELM_ERROR_LOCATION_5_J	2501 0094h + formula
98h	32	ELM_ERROR_LOCATION_6_J	2501 0098h + formula
9Ch	32	ELM_ERROR_LOCATION_7_J	2501 009Ch + formula
A0h	32	ELM_ERROR_LOCATION_8_J	2501 00A0h + formula
A4h	32	ELM_ERROR_LOCATION_9_J	2501 00A4h + formula
A8h	32	ELM_ERROR_LOCATION_10_J	2501 00A8h + formula
ACh	32	ELM_ERROR_LOCATION_11_J	2501 00ACh + formula
B0h	32	ELM_ERROR_LOCATION_12_J	2501 00B0h + formula
B4h	32	ELM_ERROR_LOCATION_13_J	2501 00B4h + formula
B8h	32	ELM_ERROR_LOCATION_14_J	2501 00B8h + formula
BCh	32	ELM_ERROR_LOCATION_15_J	2501 00BCh + formula

14.9.4.5.2 ELM Registers

ELM Registers

14.9.4.5.2.1 ELM_REVISION Register

1 ELM_REVISION Register (Offset = 0h) [reset = 20h]

This register contains the IP revision code. (A write to this register has no effect, the same as the reset)

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Table 14-29801. Instance Table

Instance Name	Physical Address
ELM0	**2501 0000h**

Figure 14-9875. ELM_REVISION Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0							
R							
0h							
7	6	5	4	3	2	1	0
REV_NUMBER							
R							
20h							

Table 14-29803. ELM_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_0	R	0h	Read returns 0
7:0	REV_NUMBER	R	20h	IP revision number [RTL] [7:4] Major revision [3:0] Minor revision Reset Source: mod_g_arst_n

14.9.4.5.2.2 ELM_SYSCONFIG Register

1 ELM_SYSCONFIG Register (Offset = 10h) [reset = 11h]

This register allows controlling various parameters of the OCP interface

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Table 14-29804. Instance Table

Instance Name	Physical Address
ELM0	**2501 0010h**

Figure 14-9876. ELM_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED_2</td><td>CLOCKACTIVITYOCP</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_1</td><td colspan="2">SIDLEMODE</td><td>RESERVED_0</td><td>SOFTRESET</td><td>AUTOGATING</td></tr>
<tr><td colspan="3">R</td><td colspan="2">R/W</td><td>R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">2h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-29806. ELM_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_2	R	0h	Reserved
8	CLOCKACTIVITYOCP	R/W	0h	OCP Clock activity when module is in IDLE mode [during wake up mode period] Reset Source: mod_g_arst_n
7:5	RESERVED_1	R	0h	Reserved
4:3	SIDLEMODE	R/W	2h	Slave interface power management [IDLE req/ack control] Reset Source: mod_g_arst_n
2	RESERVED_0	R	0h	Reserved
1	SOFTRESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware [During reads, it always returns 0] It has same effect as the OCP Hardware reset Reset Source: mod_g_arst_n
0	AUTOGATING	R/W	1h	Internal OCP clock gating strategy [no module visible impact other than saving power] Reset Source: mod_g_arst_n

14.9.4.5.2.3 ELM_SYSSTS Register

1 ELM_SYSSTS Register (Offset = 14h) [reset = 0h]

Internal Reset monitoring (OCP domain) Undefined since: on HW perspective reset state is 0 on SW user perspective when module is accessible is 1

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Table 14-29807. Instance Table

Instance Name	Physical Address
ELM0	**2501 0014h**

Figure 14-9877. ELM_SYSSTS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_0</td><td>RESETDONE</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-29809. ELM_SYSSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_0	R	0h	Reserved
0	RESETDONE	R	0h	Internal Reset monitoring [OCP domain] Undefined since: on HW perspective reset state is 0 on SW user perspective when module is accessible is 1 Reset Source: mod_g_arst_n

14.9.4.5.2.4 ELM_IRQSTS Register

1 ELM_IRQSTS Register (Offset = 18h) [reset = 0h]

Interrupt status. This register doubles as a status register for the error location processes.

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Table 14-29810. Instance Table

Instance Name	Physical Address
ELM0	**2501 0018h**

Figure 14-9878. ELM_IRQSTS Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0							PAGE_VALID
R							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29812. ELM_IRQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved
8	PAGE_VALID	R/W1TC	0h	Error location status for a full page, based on the mask definition Read 0x0: error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 0x1: all error locations valid Write 0x0: no effect Write 0x1: clear interrupt Reset Source: mod_g_arst_n
7	LOC_VALID_7	R/W1TC	0h	Error location status for syndrome polynomial 7 Read 0x0: no syndrome processed or process in progress Read 0x1: error location process completed Write 0x0: no effect Write 0x1: clear interrupt Reset Source: mod_g_arst_n
6	LOC_VALID_6	R/W1TC	0h	Error location status for syndrome polynomial 6 Reset Source: mod_g_arst_n
5	LOC_VALID_5	R/W1TC	0h	Error location status for syndrome polynomial 5 Reset Source: mod_g_arst_n
4	LOC_VALID_4	R/W1TC	0h	Error location status for syndrome polynomial 4 Reset Source: mod_g_arst_n
3	LOC_VALID_3	R/W1TC	0h	Error location status for syndrome polynomial 3 Reset Source: mod_g_arst_n

Table 14-29812. ELM_IRQSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOC_VALID_2	R/W1TC	0h	Error location status for syndrome polynomial 2 Reset Source: mod_g_arst_n
1	LOC_VALID_1	R/W1TC	0h	Error location status for syndrome polynomial 1 Reset Source: mod_g_arst_n
0	LOC_VALID_0	R/W1TC	0h	Error location status for syndrome polynomial 0 Reset Source: mod_g_arst_n

14.9.4.5.2.5 ELM_IRQEN Register

1 ELM_IRQEN Register (Offset = 1Ch) [reset = 0h]

Interrupt enable

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Table 14-29813. Instance Table

Instance Name	Physical Address
ELM0	**2501 001Ch**

Figure 14-9879. ELM_IRQEN Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0							PAGE_MASK
R							R/W
0h							0h
7	6	5	4	3	2	1	0
LOCATION_MASK_7	LOCATION_MASK_6	LOCATION_MASK_5	LOCATION_MASK_4	LOCATION_MASK_3	LOCATION_MASK_2	LOCATION_MASK_1	LOCATION_MASK_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29815. ELM_IRQEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved
8	PAGE_MASK	R/W	0h	Page interrupt mask bit 0: disable interrupt 1: enable interrupt Reset Source: mod_g_arst_n
7	LOCATION_MASK_7	R/W	0h	Error location interrupt mask bit for syndrome polynomial 7 Reset Source: mod_g_arst_n
6	LOCATION_MASK_6	R/W	0h	Error location interrupt mask bit for syndrome polynomial 6 Reset Source: mod_g_arst_n
5	LOCATION_MASK_5	R/W	0h	Error location interrupt mask bit for syndrome polynomial 5 Reset Source: mod_g_arst_n
4	LOCATION_MASK_4	R/W	0h	Error location interrupt mask bit for syndrome polynomial 4 Reset Source: mod_g_arst_n
3	LOCATION_MASK_3	R/W	0h	Error location interrupt mask bit for syndrome polynomial 3 Reset Source: mod_g_arst_n
2	LOCATION_MASK_2	R/W	0h	Error location interrupt mask bit for syndrome polynomial 2 Reset Source: mod_g_arst_n
1	LOCATION_MASK_1	R/W	0h	Error location interrupt mask bit for syndrome polynomial 1 Reset Source: mod_g_arst_n

Table 14-29815. ELM_IRQEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOCATION_MASK_0	R/W	0h	Error location interrupt mask bit for syndrome polynomial 0 0: disable interrupt 1: enable interrupt Reset Source: mod_g_arst_n

14.9.4.5.2.6 ELM_LOCATION_CONFIG Register

1 ELM_LOCATION_CONFIG Register (Offset = 20h) [reset = 0h]

ECC algorithm parameters

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Table 14-29816. Instance Table

Instance Name	Physical Address
ELM0	**2501 0020h**

Figure 14-9880. ELM_LOCATION_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_1					ECC_SIZE		
R					R/W		
0h					0h		
23	22	21	20	19	18	17	16
ECC_SIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_0						ECC_BCH_LEVEL	
R						R/W	
0h						0h	

Table 14-29818. ELM_LOCATION_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED_1	R	0h	Reserved
26:16	ECC_SIZE	R/W	0h	Maximum size of the buffers for which the error location engine is used, in number of nibbles [4-bits entities] Reset Source: mod_g_arst_n
15:2	RESERVED_0	R	0h	Reserved
1:0	ECC_BCH_LEVEL	R/W	0h	Error correction level 0x0: 4 bits 0x1: 8 bits 0x2: 16 bits 0x3: reserved Reset Source: mod_g_arst_n

14.9.4.5.2.7 ELM_PAGE_CTRL Register

1 ELM_PAGE_CTRL Register (Offset = 80h) [reset = 0h]

Page definition

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Table 14-29819. Instance Table

Instance Name	Physical Address
ELM0	**2501 0080h**

Figure 14-9881. ELM_PAGE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0							
R							
0h							
7	6	5	4	3	2	1	0
SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29821. ELM_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_0	R	0h	Reserved
7	SECTOR_7	R/W	0h	Set to 1 if syndrome polynomial 7 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
6	SECTOR_6	R/W	0h	Set to 1 if syndrome polynomial 6 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
5	SECTOR_5	R/W	0h	Set to 1 if syndrome polynomial 5 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
4	SECTOR_4	R/W	0h	Set to 1 if syndrome polynomial 4 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
3	SECTOR_3	R/W	0h	Set to 1 if syndrome polynomial 3 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
2	SECTOR_2	R/W	0h	Set to 1 if syndrome polynomial 2 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n

Table 14-29821. ELM_PAGE_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SECTOR_1	R/W	0h	Set to 1 if syndrome polynomial 1 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
0	SECTOR_0	R/W	0h	Set to 1 if syndrome polynomial 0 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n

14.9.4.5.2.8 ELM_SYNDROME_FRAGMENT_0_j Register

1 ELM_SYNDROME_FRAGMENT_0_j Register (Offset = 0h + formula) [reset = 0h]

Input syndrome polynomial bits 0 to 31.

Return to Summary Table

Offset = 400h + (j * 40h); where j = 0 to 7d

Table 14-29822. Instance Table

Instance Name	Physical Address
ELM0	**2501 0000h + formula**

Figure 14-9882. ELM_SYNDROME_FRAGMENT_0_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SYNDROME_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SYNDROME_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SYNDROME_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYNDROME_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29824. ELM_SYNDROME_FRAGMENT_0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_0	R/W	0h	Syndrome bits 0 to 31 Reset Source: mod_g_arst_n

14.9.4.5.2.9 ELM_SYNDROME_FRAGMENT_1_j Register

1 ELM_SYNDROME_FRAGMENT_1_j Register (Offset = 4h + formula) [reset = 0h]

Input syndrome polynomial bits 32 to 63.

Return to Summary Table

Offset = 404h + (j * 40h); where j = 0 to 7d

Table 14-29825. Instance Table

Instance Name	Physical Address
ELM0	**2501 0004h + formula**

Figure 14-9883. ELM_SYNDROME_FRAGMENT_1_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SYNDROME_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SYNDROME_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SYNDROME_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYNDROME_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29827. ELM_SYNDROME_FRAGMENT_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_1	R/W	0h	Syndrome bits 32 to 63 Reset Source: mod_g_arst_n

14.9.4.5.2.10 ELM_SYNDROME_FRAGMENT_2_j Register

1 ELM_SYNDROME_FRAGMENT_2_j Register (Offset = 8h + formula) [reset = 0h]

Input syndrome polynomial bits 64 to 95.

Return to Summary Table

Offset = 408h + (j * 40h); where j = 0 to 7d

Table 14-29828. Instance Table

Instance Name	Physical Address
ELM0	**2501 0008h + formula**

Figure 14-9884. ELM_SYNDROME_FRAGMENT_2_j Name Register

31	30	29	28	27	26	25	24
SYNDROME_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNDROME_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNDROME_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNDROME_2							
R/W							
0h							

Table 14-29830. ELM_SYNDROME_FRAGMENT_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_2	R/W	0h	Syndrome bits 64 to 95 Reset Source: mod_g_arst_n

14.9.4.5.2.11 ELM_SYNDROME_FRAGMENT_3_j Register

1 ELM_SYNDROME_FRAGMENT_3_j Register (Offset = Ch + formula) [reset = 0h]

Input syndrome polynomial bits 96 to 127

Return to Summary Table

Offset = 40Ch + (j * 40h); where j = 0 to 7d

Table 14-29831. Instance Table

Instance Name	Physical Address
ELM0	**2501 000Ch + formula**

Figure 14-9885. ELM_SYNDROME_FRAGMENT_3_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SYNDROME_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SYNDROME_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SYNDROME_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYNDROME_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29833. ELM_SYNDROME_FRAGMENT_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_3	R/W	0h	Syndrome bits 96 to 127 Reset Source: mod_g_arst_n

14.9.4.5.2.12 ELM_SYNDROME_FRAGMENT_4_j Register

1 ELM_SYNDROME_FRAGMENT_4_j Register (Offset = 10h + formula) [reset = 0h]

Input syndrome polynomial bits 128 to 159.

Return to Summary Table

Offset = 410h + (j * 40h); where j = 0 to 7d

Table 14-29834. Instance Table

Instance Name	Physical Address
ELM0	**2501 0010h + formula**

Figure 14-9886. ELM_SYNDROME_FRAGMENT_4_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SYNDROME_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SYNDROME_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SYNDROME_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYNDROME_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29836. ELM_SYNDROME_FRAGMENT_4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_4	R/W	0h	Syndrome bits 128 to 159 Reset Source: mod_g_arst_n

14.9.4.5.2.13 ELM_SYNDROME_FRAGMENT_5_j Register

1 ELM_SYNDROME_FRAGMENT_5_j Register (Offset = 14h + formula) [reset = 0h]

Input syndrome polynomial bits 160 to 191.

Return to Summary Table

Offset = 414h + (j * 40h); where j = 0 to 7d

Table 14-29837. Instance Table

Instance Name	Physical Address
ELM0	**2501 0014h + formula**

Figure 14-9887. ELM_SYNDROME_FRAGMENT_5_j Name Register

31	30	29	28	27	26	25	24
SYNDROME_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNDROME_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNDROME_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNDROME_5							
R/W							
0h							

Table 14-29839. ELM_SYNDROME_FRAGMENT_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_5	R/W	0h	Syndrome bits 160 to 191 Reset Source: mod_g_arst_n

14.9.4.5.2.14 ELM_SYNDROME_FRAGMENT_6_j Register

1 ELM_SYNDROME_FRAGMENT_6_j Register (Offset = 18h + formula) [reset = 0h]

Input syndrome polynomial bits 192 to 207.

Return to Summary Table

Offset = 418h + (j * 40h); where j = 0 to 7d

Table 14-29840. Instance Table

Instance Name	Physical Address
ELM0	**2501 0018h + formula**

Figure 14-9888. ELM_SYNDROME_FRAGMENT_6_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							SYNDROME_VALID
R							R/W
0h							0h
15	14	13	12	11	10	9	8
SYNDROME_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNDROME_6							
R/W							
0h							

Table 14-29842. ELM_SYNDROME_FRAGMENT_6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Reserved
16	SYNDROME_VALID	R/W	0h	Syndrome valid bit 0x0: this syndrome polynomial should not be processed 0x1: this syndrome polynomial must be processed Reset Source: mod_g_arst_n
15:0	SYNDROME_6	R/W	0h	Syndrome bits 192 to 207 Reset Source: mod_g_arst_n

14.9.4.5.2.15 ELM_LOCATION_STS_j Register

1 ELM_LOCATION_STS_j Register (Offset = 0h + formula) [reset = 0h]

Exit status for the syndrome polynomial processing

Return to Summary Table

Offset = 800h + (j * 100h); where j = 0 to 7d

Table 14-29843. Instance Table

Instance Name	Physical Address
ELM0	**2501 0000h + formula**

Figure 14-9889. ELM_LOCATION_STS_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_0							ECC_CORRECTABLE
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			ECC_NB_ERRORS				
R			R				
0h			0h				

Table 14-29845. ELM_LOCATION_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved
8	ECC_CORRECTABLE	R	0h	Error location process exit status 0x0: ECC error location process failed Number of errors and error locations are invalid 0x1: all errors were successfully located Number of errors and error locations are valid Reset Source: mod_g_arst_n
7:5	RESERVED_1	R	0h	Reserved
4:0	ECC_NB_ERRORS	R	0h	Number of errors detected and located Reset Source: mod_g_arst_n

14.9.4.5.2.16 ELM_ERROR_LOCATION_0_j Register

1 ELM_ERROR_LOCATION_0_j Register (Offset = 80h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 880h + (j * 100h); where j = 0 to 7d

Table 14-29846. Instance Table

Instance Name	Physical Address
ELM0	**2501 0080h + formula**

Figure 14-9890. ELM_ERROR_LOCATION_0_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29848. ELM_ERROR_LOCATION_0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.17 ELM_ERROR_LOCATION_1_j Register

1 ELM_ERROR_LOCATION_1_j Register (Offset = 84h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 884h + (j * 100h); where j = 0 to 7d

Table 14-29849. Instance Table

Instance Name	Physical Address
ELM0	**2501 0084h + formula**

Figure 14-9891. ELM_ERROR_LOCATION_1_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29851. ELM_ERROR_LOCATION_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.18 ELM_ERROR_LOCATION_2_j Register

1 ELM_ERROR_LOCATION_2_j Register (Offset = 88h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 888h + (j * 100h); where j = 0 to 7d

Table 14-29852. Instance Table

Instance Name	Physical Address
ELM0	**2501 0088h + formula**

Figure 14-9892. ELM_ERROR_LOCATION_2_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29854. ELM_ERROR_LOCATION_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.19 ELM_ERROR_LOCATION_3_j Register

1 ELM_ERROR_LOCATION_3_j Register (Offset = 8Ch + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 88Ch + (j * 100h); where j = 0 to 7d

Table 14-29855. Instance Table

Instance Name	Physical Address
ELM0	**2501 008Ch + formula**

Figure 14-9893. ELM_ERROR_LOCATION_3_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29857. ELM_ERROR_LOCATION_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.20 ELM_ERROR_LOCATION_4_j Register

1 ELM_ERROR_LOCATION_4_j Register (Offset = 90h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 890h + (j * 100h); where j = 0 to 7d

Table 14-29858. Instance Table

Instance Name	Physical Address
ELM0	**2501 0090h + formula**

Figure 14-9894. ELM_ERROR_LOCATION_4_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29860. ELM_ERROR_LOCATION_4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.21 ELM_ERROR_LOCATION_5_j Register

1 ELM_ERROR_LOCATION_5_j Register (Offset = 94h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 894h + (j * 100h); where j = 0 to 7d

Table 14-29861. Instance Table

Instance Name	Physical Address
ELM0	**2501 0094h + formula**

Figure 14-9895. ELM_ERROR_LOCATION_5_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_0</td><td colspan="5">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29863. ELM_ERROR_LOCATION_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.22 ELM_ERROR_LOCATION_6_j Register

1 ELM_ERROR_LOCATION_6_j Register (Offset = 98h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 898h + (j * 100h); where j = 0 to 7d

Table 14-29864. Instance Table

Instance Name	Physical Address
ELM0	**2501 0098h + formula**

Figure 14-9896. ELM_ERROR_LOCATION_6_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29866. ELM_ERROR_LOCATION_6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.23 ELM_ERROR_LOCATION_7_j Register

1 ELM_ERROR_LOCATION_7_j Register (Offset = 9Ch + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 89Ch + (j * 100h); where j = 0 to 7d

Table 14-29867. Instance Table

Instance Name	Physical Address
ELM0	**2501 009Ch + formula**

Figure 14-9897. ELM_ERROR_LOCATION_7_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29869. ELM_ERROR_LOCATION_7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.24 ELM_ERROR_LOCATION_8_j Register

1 ELM_ERROR_LOCATION_8_j Register (Offset = A0h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8A0h + (j * 100h); where j = 0 to 7d

Table 14-29870. Instance Table

Instance Name	Physical Address
ELM0	**2501 00A0h + formula**

Figure 14-9898. ELM_ERROR_LOCATION_8_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_0</td><td colspan="5">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29872. ELM_ERROR_LOCATION_8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.25 ELM_ERROR_LOCATION_9_j Register

1 ELM_ERROR_LOCATION_9_j Register (Offset = A4h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8A4h + (j * 100h); where j = 0 to 7d

Table 14-29873. Instance Table

Instance Name	Physical Address
ELM0	**2501 00A4h + formula**

Figure 14-9899. ELM_ERROR_LOCATION_9_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_0</td><td colspan="5">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29875. ELM_ERROR_LOCATION_9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.26 ELM_ERROR_LOCATION_10_j Register

1 ELM_ERROR_LOCATION_10_j Register (Offset = A8h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8A8h + (j * 100h); where j = 0 to 7d

Table 14-29876. Instance Table

Instance Name	Physical Address
ELM0	**2501 00A8h + formula**

Figure 14-9900. ELM_ERROR_LOCATION_10_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29878. ELM_ERROR_LOCATION_10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.27 ELM_ERROR_LOCATION_11_j Register

1 ELM_ERROR_LOCATION_11_j Register (Offset = ACh + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8ACh + (j * 100h); where j = 0 to 7d

Table 14-29879. Instance Table

Instance Name	Physical Address
ELM0	**2501 00ACh + formula**

Figure 14-9901. ELM_ERROR_LOCATION_11_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29881. ELM_ERROR_LOCATION_11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.28 ELM_ERROR_LOCATION_12_j Register

1 ELM_ERROR_LOCATION_12_j Register (Offset = B0h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8B0h + (j * 100h); where j = 0 to 7d

Table 14-29882. Instance Table

Instance Name	Physical Address
ELM0	**2501 00B0h + formula**

Figure 14-9902. ELM_ERROR_LOCATION_12_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29884. ELM_ERROR_LOCATION_12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.29 ELM_ERROR_LOCATION_13_j Register

1 ELM_ERROR_LOCATION_13_j Register (Offset = B4h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8B4h + (j * 100h); where j = 0 to 7d

Table 14-29885. Instance Table

Instance Name	Physical Address
ELM0	**2501 00B4h + formula**

Figure 14-9903. ELM_ERROR_LOCATION_13_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29887. ELM_ERROR_LOCATION_13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.30 ELM_ERROR_LOCATION_14_j Register

1 ELM_ERROR_LOCATION_14_j Register (Offset = B8h + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8B8h + (j * 100h); where j = 0 to 7d

Table 14-29888. Instance Table

Instance Name	Physical Address
ELM0	**2501 00B8h + formula**

Figure 14-9904. ELM_ERROR_LOCATION_14_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29890. ELM_ERROR_LOCATION_14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.5.2.31 ELM_ERROR_LOCATION_15_j Register

1 ELM_ERROR_LOCATION_15_j Register (Offset = BCh + formula) [reset = 0h]

Error location register

Return to Summary Table

Offset = 8BCh + (j * 100h); where j = 0 to 7d

Table 14-29891. Instance Table

Instance Name	Physical Address
ELM0	**2501 00BCh + formula**

Figure 14-9905. ELM_ERROR_LOCATION_15_j Name Register

31	30	29	28	27	26	25	24
RESERVED_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_0			ECC_ERROR_LOCATION				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
ECC_ERROR_LOCATION							
R							
0h							

Table 14-29893. ELM_ERROR_LOCATION_15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

14.9.4.6 MMCSD0

MMCSD0

14.9.4.6.1 MMCSD0 Summaries

MMCSD0 Summaries

Table 14-29894. ECC_AGGR Registers, Base Address=0070 6000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	ECC_AGGR_REV	0070 6000h
8h	32	ECC_AGGR_VECTOR	0070 6008h
Ch	32	ECC_AGGR_STAT	0070 600Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 6010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 603Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 6040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 6080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 60C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 613Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 6140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 6180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 61C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 6200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 6204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 6208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 620Ch

Table 14-29895. ECC_AGGR Registers, Base Address=0070 7000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	ECC_AGGR_REV	0070 7000h
8h	32	ECC_AGGR_VECTOR	0070 7008h
Ch	32	ECC_AGGR_STAT	0070 700Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 7010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 703Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 7040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 7080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 70C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 713Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 7140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 7180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 71C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 7200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 7204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 7208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 720Ch

Table 14-29896. MMC_CTLCFG Registers, Base Address=0FA1 0000h, Length=4096

Offset	Length	Register Name	MMCSD0 Physical Address
0h	16	MMC_CTLCFG_SDMA_SYS_ADDR_LO	0FA1 0000h
2h	16	MMC_CTLCFG_SDMA_SYS_ADDR_HI	0FA1 0002h
4h	16	MMC_CTLCFG_BLOCK_SIZE	0FA1 0004h
6h	16	MMC_CTLCFG_BLOCK_COUNT	0FA1 0006h
8h	16	MMC_CTLCFG_ARGUMENT1_LO	0FA1 0008h
Ah	16	MMC_CTLCFG_ARGUMENT1_HI	0FA1 000Ah
Ch	16	MMC_CTLCFG_TRANSFER_MODE	0FA1 000Ch
Eh	16	MMC_CTLCFG_COMMAND	0FA1 000Eh
10h	16	MMC_CTLCFG_RESPONSE_J	0FA1 0010h + formula
20h	32	MMC_CTLCFG_DATA_PORT	0FA1 0020h
24h	32	MMC_CTLCFG_PRESENTSTATE	0FA1 0024h
28h	8	MMC_CTLCFG_HOST_CONTROL1	0FA1 0028h
29h	8	MMC_CTLCFG_POWER_CONTROL	0FA1 0029h
2Ah	8	MMC_CTLCFG_BLOCK_GAP_CONTROL	0FA1 002Ah
2Bh	8	MMC_CTLCFG_WAKEUP_CONTROL	0FA1 002Bh
2Ch	16	MMC_CTLCFG_CLOCK_CONTROL	0FA1 002Ch
2Eh	8	MMC_CTLCFG_TIMEOUT_CONTROL	0FA1 002Eh
2Fh	8	MMC_CTLCFG_SOFTWARE_RESET	0FA1 002Fh
30h	16	MMC_CTLCFG_NORMAL_INTR_STS	0FA1 0030h
32h	16	MMC_CTLCFG_ERROR_INTR_STS	0FA1 0032h
34h	16	MMC_CTLCFG_NORMAL_INTR_STS_ENA	0FA1 0034h
36h	16	MMC_CTLCFG_ERROR_INTR_STS_ENA	0FA1 0036h
38h	16	MMC_CTLCFG_NORMAL_INTR_SIG_ENA	0FA1 0038h
3Ah	16	MMC_CTLCFG_ERROR_INTR_SIG_ENA	0FA1 003Ah
3Ch	16	MMC_CTLCFG_AUTOCMD_ERR_STS	0FA1 003Ch
3Eh	16	MMC_CTLCFG_HOST_CONTROL2	0FA1 003Eh
40h	64	MMC_CTLCFG_CAPABILITIES	0FA1 0040h
48h	64	MMC_CTLCFG_MAX_CURRENT_CAP	0FA1 0048h
50h	16	MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS	0FA1 0050h
52h	16	MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS	0FA1 0052h
54h	8	MMC_CTLCFG_ADMA_ERR_STATUS	0FA1 0054h
58h	64	MMC_CTLCFG_ADMA_SYS_ADDRESS	0FA1 0058h
60h	16	MMC_CTLCFG_PRESET_VALUE0	0FA1 0060h
62h	16	MMC_CTLCFG_PRESET_VALUE1	0FA1 0062h
64h	16	MMC_CTLCFG_PRESET_VALUE2	0FA1 0064h
66h	16	MMC_CTLCFG_PRESET_VALUE3	0FA1 0066h
68h	16	MMC_CTLCFG_PRESET_VALUE4	0FA1 0068h
6Ah	16	MMC_CTLCFG_PRESET_VALUE5	0FA1 006Ah
6Ch	16	MMC_CTLCFG_PRESET_VALUE6	0FA1 006Ch
6Eh	16	MMC_CTLCFG_PRESET_VALUE7	0FA1 006Eh
72h	16	MMC_CTLCFG_PRESET_VALUE8	0FA1 0072h
74h	16	MMC_CTLCFG_PRESET_VALUE10	0FA1 0074h
78h	64	MMC_CTLCFG_ADMA3_DESC_ADDRESS	0FA1 0078h
80h	16	MMC_CTLCFG_UHS2_BLOCK_SIZE	0FA1 0080h
84h	32	MMC_CTLCFG_UHS2_BLOCK_COUNT	0FA1 0084h

Table 14-29896. MMC_CTLCFG Registers, Base Address=0FA1 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD0 Physical Address
88h	8	MMC_CTLCFG_UHS2_COMMAND_PKT_J	0FA1 0088h + formula
9Ch	16	MMC_CTLCFG_UHS2_XFER_MODE	0FA1 009Ch
9Eh	16	MMC_CTLCFG_UHS2_COMMAND	0FA1 009Eh
A0h	8	MMC_CTLCFG_UHS2_RESPONSE_J	0FA1 00A0h + formula
B4h	8	MMC_CTLCFG_UHS2_MESSAGE_SELECT	0FA1 00B4h
B8h	32	MMC_CTLCFG_UHS2_MESSAGE	0FA1 00B8h
BCh	16	MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS	0FA1 00BCh
BEh	8	MMC_CTLCFG_UHS2_DEVICE_SELECT	0FA1 00BEh
BFh	8	MMC_CTLCFG_UHS2_DEVICE_INT_CODE	0FA1 00BFh
C0h	16	MMC_CTLCFG_UHS2_SOFTWARE_RESET	0FA1 00C0h
C2h	16	MMC_CTLCFG_UHS2_TIMER_CONTROL	0FA1 00C2h
C4h	32	MMC_CTLCFG_UHS2_ERR_INTR_STS	0FA1 00C4h
C8h	32	MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA	0FA1 00C8h
CCh	32	MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA	0FA1 00CCh
E0h	16	MMC_CTLCFG_UHS2_SETTINGS_PTR	0FA1 00E0h
E2h	16	MMC_CTLCFG_UHS2_CAPABILITIES_PTR	0FA1 00E2h
E4h	16	MMC_CTLCFG_UHS2_TEST_PTR	0FA1 00E4h
E6h	16	MMC_CTLCFG_SHARED_BUS_CTRL_PTR	0FA1 00E6h
E8h	16	MMC_CTLCFG_VENDOR_SPECFIC_PTR	0FA1 00E8h
F4h	32	MMC_CTLCFG_BOOT_TIMEOUT_CONTROL	0FA1 00F4h
F8h	32	MMC_CTLCFG_VENDOR_REGISTER	0FA1 00F8h
FCh	16	MMC_CTLCFG_SLOT_INT_STS	0FA1 00FCh
FEh	16	MMC_CTLCFG_HOST_CONTROLLER_VER	0FA1 00FEh
100h	32	MMC_CTLCFG_UHS2_GEN_SETTINGS	0FA1 0100h
104h	32	MMC_CTLCFG_UHS2_PHY_SETTINGS	0FA1 0104h
108h	64	MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS	0FA1 0108h
110h	32	MMC_CTLCFG_UHS2_GEN_CAP	0FA1 0110h
114h	32	MMC_CTLCFG_UHS2_PHY_CAP	0FA1 0114h
118h	64	MMC_CTLCFG_UHS2_LNK_TRN_CAP	0FA1 0118h
120h	32	MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS	0FA1 0120h
200h	32	MMC_CTLCFG_CQ_VERSION	0FA1 0200h
204h	32	MMC_CTLCFG_CQ_CAPABILITIES	0FA1 0204h
208h	32	MMC_CTLCFG_CQ_CONFIG	0FA1 0208h
20Ch	32	MMC_CTLCFG_CQ_CONTROL	0FA1 020Ch
210h	32	MMC_CTLCFG_CQ_INTR_STS	0FA1 0210h
214h	32	MMC_CTLCFG_CQ_INTR_STS_ENA	0FA1 0214h
218h	32	MMC_CTLCFG_CQ_INTR_SIG_ENA	0FA1 0218h
21Ch	32	MMC_CTLCFG_CQ_INTR_COALESCING	0FA1 021Ch
220h	32	MMC_CTLCFG_CQ_TDL_BASE_ADDR	0FA1 0220h
224h	32	MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS	0FA1 0224h
228h	32	MMC_CTLCFG_CQ_TASK_DOOR_BELL	0FA1 0228h
22Ch	32	MMC_CTLCFG_CQ_TASK_COMP_NOTIF	0FA1 022Ch
230h	32	MMC_CTLCFG_CQ_DEV_QUEUE_STATUS	0FA1 0230h
234h	32	MMC_CTLCFG_CQ_DEV_PENDING_TASKS	0FA1 0234h
238h	32	MMC_CTLCFG_CQ_TASK_CLEAR	0FA1 0238h

Table 14-29896. MMC_CTLCFG Registers, Base Address=0FA1 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD0 Physical Address
240h	32	MMC_CTLCFG_CQ_SEND_STS_CONFIG1	0FA1 0240h
244h	32	MMC_CTLCFG_CQ_SEND_STS_CONFIG2	0FA1 0244h
248h	32	MMC_CTLCFG_CQ_DCMD_RESPONSE	0FA1 0248h
250h	32	MMC_CTLCFG_CQ_RESP_ERR_MASK	0FA1 0250h
254h	32	MMC_CTLCFG_CQ_TASK_ERR_INFO	0FA1 0254h
258h	32	MMC_CTLCFG_CQ_CMD_RESP_INDEX	0FA1 0258h
25Ch	32	MMC_CTLCFG_CQ_CMD_RESP_ARG	0FA1 025Ch
260h	32	MMC_CTLCFG_CQ_ERROR_TASK_ID	0FA1 0260h

Table 14-29897. MMC_SSCFG Registers, Base Address=0FA1 8000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	MMC_SSCFG_SS_ID_REV_REG	0FA1 8000h
10h	32	MMC_SSCFG_CTL_CFG_1_REG	0FA1 8010h
14h	32	MMC_SSCFG_CTL_CFG_2_REG	0FA1 8014h
18h	32	MMC_SSCFG_CTL_CFG_3_REG	0FA1 8018h
1Ch	32	MMC_SSCFG_CTL_CFG_4_REG	0FA1 801Ch
20h	32	MMC_SSCFG_CTL_CFG_5_REG	0FA1 8020h
24h	32	MMC_SSCFG_CTL_CFG_6_REG	0FA1 8024h
28h	32	MMC_SSCFG_CTL_CFG_7_REG	0FA1 8028h
2Ch	32	MMC_SSCFG_CTL_CFG_8_REG	0FA1 802Ch
30h	32	MMC_SSCFG_CTL_CFG_9_REG	0FA1 8030h
34h	32	MMC_SSCFG_CTL_CFG_10_REG	0FA1 8034h
38h	32	MMC_SSCFG_CTL_CFG_11_REG	0FA1 8038h
3Ch	32	MMC_SSCFG_CTL_CFG_12_REG	0FA1 803Ch
40h	32	MMC_SSCFG_CTL_CFG_13_REG	0FA1 8040h
44h	32	MMC_SSCFG_CTL_CFG_14_REG	0FA1 8044h
60h	32	MMC_SSCFG_CTL_STAT_1_REG	0FA1 8060h
64h	32	MMC_SSCFG_CTL_STAT_2_REG	0FA1 8064h
68h	32	MMC_SSCFG_CTL_STAT_3_REG	0FA1 8068h
6Ch	32	MMC_SSCFG_CTL_STAT_4_REG	0FA1 806Ch
70h	32	MMC_SSCFG_CTL_STAT_5_REG	0FA1 8070h
74h	32	MMC_SSCFG_CTL_STAT_6_REG	0FA1 8074h
100h	32	MMC_SSCFG_PHY_CTRL_1_REG	0FA1 8100h
104h	32	MMC_SSCFG_PHY_CTRL_2_REG	0FA1 8104h
108h	32	MMC_SSCFG_PHY_CTRL_3_REG	0FA1 8108h
10Ch	32	MMC_SSCFG_PHY_CTRL_4_REG	0FA1 810Ch
110h	32	MMC_SSCFG_PHY_CTRL_5_REG	0FA1 8110h
114h	32	MMC_SSCFG_PHY_CTRL_6_REG	0FA1 8114h
130h	32	MMC_SSCFG_PHY_STAT_1_REG	0FA1 8130h
134h	32	MMC_SSCFG_PHY_STAT_2_REG	0FA1 8134h

14.9.4.6.2 MMCSD0 Registers

MMCSD0 Registers

14.9.4.6.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-29898. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7000h**

Figure 14-9906. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-29900. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.4.6.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-29901. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7008h**

Figure 14-9907. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-29903. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.4.6.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-29904. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 700Ch**

Figure 14-9908. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 14-29906. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.4.6.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-29907. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7010h + formula**

Figure 14-9909. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-29909. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.6.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-29910. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 703Ch**

Figure 14-9910. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-29912. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.6.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29913. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7040h**

Figure 14-9911. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-29915. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.6.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29916. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7080h**

Figure 14-9912. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-29918. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.6.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29919. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 70C0h**

Figure 14-9913. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29921. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.6.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-29922. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 713Ch**

Figure 14-9914. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-29924. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.6.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29925. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7140h**

Figure 14-9915. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-29927. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.6.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29928. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7180h**

Figure 14-9916. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-29930. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.6.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29931. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 71C0h**

Figure 14-9917. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29933. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.6.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-29934. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7200h**

Figure 14-9918. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-29936. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.4.6.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-29937. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7204h**

Figure 14-9919. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29939. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.4.6.2.15 *ECC_AGGR_AGGR_STATUS_SET Register*

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-29940. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7208h**

Figure 14-9920. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-29942. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.4.6.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-29943. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 720Ch**

Figure 14-9921. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-29945. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.4.6.2.17 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

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Table 14-29946. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7000h**

Figure 14-9922. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-29948. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.4.6.2.18 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-29949. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7008h**

Figure 14-9923. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-29951. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.4.6.2.19 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-29952. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 700Ch**

Figure 14-9924. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-29954. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.4.6.2.20 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-29955. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7010h + formula**

Figure 14-9925. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-29957. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.6.2.21 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-29958. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 703Ch**

Figure 14-9926. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-29960. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.6.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29961. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7040h**

Figure 14-9927. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-29963. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.6.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29964. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7080h**

Figure 14-9928. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-29966. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.6.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29967. Instance Table

Instance Name	**Physical Address**
MMCSD0	**0070 70C0h**

Figure 14-9929. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29969. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.6.2.25 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-29970. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 713Ch**

Figure 14-9930. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-29972. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.6.2.26 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-29973. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7140h**

Figure 14-9931. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-29975. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.6.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-29976. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7180h**

Figure 14-9932. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-29978. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.6.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-29979. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 71C0h**

Figure 14-9933. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-29981. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.6.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-29982. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7200h**

Figure 14-9934. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-29984. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.4.6.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-29985. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7204h**

Figure 14-9935. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-29987. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.4.6.2.31 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-29988. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 7208h**

Figure 14-9936. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-29990. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.4.6.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-29991. Instance Table

Instance Name	Physical Address
MMCSD0	**0070 720Ch**

Figure 14-9937. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-29993. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.4.6.2.33 MMC_CTLCFG_SDMA_SYS_ADDR_LO Register

1 MMC_CTLCFG_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-29994. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0000h**

Figure 14-9938. MMC_CTLCFG_SDMA_SYS_ADDR_LO Name Register

15	14	13	12	11	10	9	8
SDMA_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
SDMA_ADDRESS							
R/W							
0h							

Table 14-29996. MMC_CTLCFG_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	When Host Version 4 Enable is set to 0 in the Host Control 2 register,DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When Host Version 4 Enable is set to 1, SDMA uses ADMA System Address register [05Fh-058h] instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23.[1] SDMA System Address [Host Version 4 Enable = 0] This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Reading this register during SDMA transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data posi- tion can be read from this register. The SDMA transfer waits at the every boundary specified by the SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register [003h] is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. [2] 32-bit Block Count [Host Version 4 Enable = 1] Host Controller Version 4.10 re-defines this register as 32-bit Block Count [Refer to Section 1.15 for more details about block count extension]. In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23. The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero. This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.34 MMC_CTLCFG_SDMA_SYS_ADDR_HI Register

1 MMC_CTLCFG_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-29997. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0002h**

Figure 14-9939. MMC_CTLCFG_SDMA_SYS_ADDR_HI Name Register

15	14	13	12	11	10	9	8
SDMA_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
SDMA_ADDRESS							
R/W							
0h							

Table 14-29999. MMC_CTLCFG_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.35 MMC_CTLCFG_BLOCK_SIZE Register

1 MMC_CTLCFG_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-30000. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0004h**

Figure 14-9940. MMC_CTLCFG_BLOCK_SIZE Name Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_SIZE							
R/W							
0h							

Table 14-30002. MMC_CTLCFG_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_SIZE	R/W	0h	To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. Reset Source: vbus_amod_g_rst_n 0 4KB 1 8KB 2 16KB 3 32KB 4 64KB 5 128KB 6 256KB 7 512KB
11:0	XFER_BLK_SIZE	R/W	0h	This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing [i.e after a transaction has stopped]. Read operations during transfer return an invalid value and write operations shall be ignored. Reset Source: vbus_amod_g_rst_n 0 No data transfer 1 1 Byte 2 2 Bytes 512 512 Bytes 2048 2048 Bytes

14.9.4.6.2.36 MMC_CTLCFG_BLOCK_COUNT Register

1 MMC_CTLCFG_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-30003. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0006h**

Figure 14-9941. MMC_CTLCFG_BLOCK_COUNT Name Register

15	14	13	12	11	10	9	8
XFER_BLK_CNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_CNT							
R/W							
0h							

Table 14-30005. MMC_CTLCFG_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	XFER_BLK_CNT	R/W	0h	Host Controller Version 4.10 extends block count to 32-bit [Refer to Section 1.15].Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows: [1] If Host Version 4 Enable in the Host Control 2 register is set to 0 or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected [2] If Host Version 4 Enable is set to 1 and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected.Use of 16-bit/32-bit Block Count register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count.The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred.This register should be accessed only when no transaction is executing [i.e., after transactions are stopped]. During data transfer,read operations on this register may return an invalid value and write operations are ignored. Reset Source: vbus_amod_g_rst_n 0 Stop count 1 1 block 2 2 blocks 3 3 blocks 65535 65535 blocks

14.9.4.6.2.37 MMC_CTLCFG_ARGUMENT1_LO Register

1 MMC_CTLCFG_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

This register contains Lower bits of SD Command Argument

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Table 14-30006. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0008h**

Figure 14-9942. MMC_CTLCFG_ARGUMENT1_LO Name Register

15	14	13	12	11	10	9	8
CMD_ARG1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_ARG1							
R/W							
0h							

Table 14-30008. MMC_CTLCFG_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit23-8 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.38 MMC_CTLCFG_ARGUMENT1_HI Register

1 MMC_CTLCFG_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

This register contains higher bits of SD Command Argument

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Table 14-30009. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 000Ah**

Figure 14-9943. MMC_CTLCFG_ARGUMENT1_HI Name Register

15	14	13	12	11	10	9	8
CMD_ARG1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMD_ARG1							
R/W							
0h							

Table 14-30011. MMC_CTLCFG_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit39-24 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.39 MMC_CTLCFG_TRANSFER_MODE Register

1 MMC_CTLCFG_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-30012. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 000Ch**

Figure 14-9944. MMC_CTLCFG_TRANSFER_MODE Name Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	R/W		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-30014. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	NONE	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error,sets this bit to 0 and waits Command Complete Interrupt and then checks the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Command Complete Signal Enable. Reset Source: vbus_amod_g_rst_n 0 `Enable Response Interrupt` 1 `Disable Response Interrupt`
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.If Host Driver checks response error, this bit is set to 0 and Response Interrupt Disable is set to 0.If Host Controller checks response error, sets this bit to 1 and sets Response Interrupt Disable to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the Response Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Disable Response Error Check` 1 `Enable Response Error Check`

Table 14-30014. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 .Bit31 OUT_OF_RANGE .Bit30 ADDRESS_ERROR .Bit29 BLOCK_LEN_ERROR .Bit26 WP_VIOLATION .Bit25 CARD_IS_LOCKED .Bit23 COM_CRC_ERROR .Bit21 CARD_ECC_FAILED .Bit20 CC_ERROR .Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE Reset Source: vbus_amod_g_rst_n 0 `Memory` 1 `SDIO`
5	MULTI_BLK_SEL	R/W	0h	This bit enables multiple block data transfers. Reset Source: vbus_amod_g_rst_n 0 `Single Block transfer` 1 `Multiple Block transfer`
4	DATA_XFER_DIR	R/W	0h	This bit defines the direction of data transfers. Reset Source: vbus_amod_g_rst_n 0 `Write from Host to Card` 1 `Read from Card to Host`

Table 14-30014. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	AUTO_CMD_ENA	R/W	0h	There are three methods to stop Multiple-block read and write operation. [1] Auto CMD12 Enable: Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 01b, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. When Host Version 4 Enable =0, CMD12 is issued when 16-bit Block Count is expired. When Host Version 4 Enable =1, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired. [2] Auto CMD23 Enable: When this bit field is set to 10b, the Host Controller issues a CMD23 automatically before issuing a command specified in the Command register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. The following conditions are required to use the Auto CMD23. Auto CMD23 Supported [Host Controller Version is 3.00 or later]. A memory card that supports CMD23 [SCR[33]=1]. If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By Writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register.32-bit block count value for CMD23 is set to 32-bit Block Count [SDMA System Address] register. [3] Auto CMD Auto Select [Version 4.10] As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this Auto CMD Auto Select mode. Selection of Auto CMD depends on setting of CMD23 Enable in the Host Control 2 register which indicates whether card supports CMD23. If CMD23 Enable =1, Auto CMD23 is used and if CMD23 Enable =0, Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable. Reset Source: vbus_amod_g_rst_n 0 `Auto CMD Disable` 1 `Auto CMD12 Enable` 2 `Auto CMD23 Enable` 3 `Auto CMD Auto Select`
1	BLK_CNT_ENA	R/W	0h	This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. Reset Source: vbus_amod_g_rst_n 0 `Disable Block count` 1 `Enable Block count`
0	DMA_ENA	R/W	0h	DMA can be enabled only if DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register [00Fh]. Reset Source: vbus_amod_g_rst_n 0 `DMA mode is Disabled` 1 `DMA mode is Enabled`

14.9.4.6.2.40 MMC_CTLCFG_COMMAND Register

1 MMC_CTLCFG_COMMAND Register (Offset = Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-30015. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 000Eh**

Figure 14-9945. MMC_CTLCFG_COMMAND Name Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W		R/W	R/W	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	

Table 14-30017. MMC_CTLCFG_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	NONE	0h	Reserved
13:8	CMD_INDEX	R/W	0h	This bit shall be set to the command number [CMD0-63, ACMD0-63]. Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	There are three types of special commands. Suspend, Resume andAbort. These bits shall bet set to 00b for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting Continue Request in the Block Gap Control Register. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. Abort Command: If this command is set when exe- cuting a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a writetransfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. Reset Source: vbus_amod_g_rst_n 0 `Normal` 1 `Suspend` 2 `Resume` 3 `Abort`

Table 14-30017. MMC_CTLCFG_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line [ex. CMD52]. 2. Commands with no data transferbut using busy signal on DAT[0]line [R1b or R5b ex. CMD38]. 3. Resume Command. Reset Source: vbus_amod_g_rst_n 0 Data not Present 1 Data present
4	CMD_INDEX_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. Reset Source: vbus_amod_g_rst_n 0 Disable Command Index Check 1 Enable Command Index Check
3	CMD_CRC_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. Reset Source: vbus_amod_g_rst_n 0 Disable Command CRC Check 1 Enable Command CRC Check
2	SUB_CMD	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17]. When issuing a main command, this bit is set to 0 and when issuing a sub command, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register.Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command. Reset Source: vbus_amod_g_rst_n 0 Main Command 1 Sub Command
1:0	RESP_TYPE_SEL	R/W	0h	Response Type Select. Reset Source: vbus_amod_g_rst_n 0 No Response 1 Response length 136 2 Response length 48 3 Response length 48 check Busy after response

14.9.4.6.2.41 MMC_CTLCFG_RESPONSE_j Register

1 MMC_CTLCFG_RESPONSE_j Register (Offset = 10h + formula) [reset = 0h]

This register is used to store responses from SD Cards

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Offset = 10h + (j * 2h); where j = 0 to 7d

Table 14-30018. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0010h + formula**

Figure 14-9946. MMC_CTLCFG_RESPONSE_j Name Register

15	14	13	12	11	10	9	8
CMD_RESP							
R							
0h							
7	6	5	4	3	2	1	0
CMD_RESP							
R							
0h							

Table 14-30020. MMC_CTLCFG_RESPONSE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_RESP	R	0h	R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.42 MMC_CTLCFG_DATA_PORT Register

1 MMC_CTLCFG_DATA_PORT Register (Offset = 20h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30021. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0020h**

Figure 14-9947. MMC_CTLCFG_DATA_PORT Name Register

31	30	29	28	27	26	25	24
BUF_RD_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
BUF_RD_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
BUF_RD_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
BUF_RD_DATA							
R/W							
0h							

Table 14-30023. MMC_CTLCFG_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUF_RD_DATA	R/W	0h	The Host Controller Buffer can be accessed through this 32-bit Data Port Register. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.43 MMC_CTLCFG_PRESENTSTATE Register

1 MMC_CTLCFG_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

The Host Driver can get status of the Host Controller from this 32-bit read-only register

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Table 14-30024. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0024h**

Figure 14-9948. MMC_CTLCFG_PRESENTSTATE Name Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISS_BY_ERR	RESERVED		SDIF_CMDIN
R	R	R	R	R	NONE		R
0h	0h	0h	0h	0h	0h		1h
23	22	21	20	19	18	17	16
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R	R	R	R	R	R	R	R
1h	1h	1h	1h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 regis-ter. UHS-II interface initialization is activated by setting SD Clock Enable in the Clock Control reg-ister. Host Controller drives STB.L on D0 lanefrom EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1 if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when Reading this status [Refer to Figure 3-35 about details of this method]. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200us period from set- ting SD Clock Enable until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Inter-face Enable is set to 0 or Host full reset is exe-cuted. '0' UHS-II IF is not detected '1' UHS-II IF is detected Reset Source: vbus_amod_g_rst_n

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	UHS2_IF_LANE_SYNC	R	0h	This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On detecting UHS-II Interface [D31=1], Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller pro-vides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane. In case of Version 4.00, this bit indicates comple-tion of Device PHY Initialization by detecting LIDL LSS on D1 lane.From Version 4.10, Host Controller may imple-ment a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0 even LIDL LSS is detected on D1 lane.Host Driver detects PHY Initialization Failure by timeout.This bit is cleared by when D0 lane is set to EIDL,UHS-II Interface Enable is set to 0 or executes Host full reset. Reset Source: vbus_amod_g_rst_n 0 UHS-II PHY is not initialized 1 UHS-II PHY is initialized
29	UHS2_DORMANT	R	0h	This status indicates whether UHS-II lanes enterDormant state. This function is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On issuing GO_DORMAT_STATE com-mand, Go Dormant Command [111b]; is set to Command type in the UHS-II Command register.This command type acts as a trigger to enterlanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiv-ing STB.H and EIDL on D1 lane. This bit is set to 1 after the time of T_DMT_ENTRY [750 RCLK cycle] or more from detecting EIDL on D1 lane. RCLK may be stopped in dormant state, by setting SD Clock Enable to 0 in the Clock Control register while In Dormant State bit is set to 1. On WritingClock Control register with setting SD Clock Enable to 1, Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0. In case of the card enters Hibernate Mode [RCLK is stopped], Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the Power Control register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0 or executesHost full reset. Reset Source: vbus_amod_g_rst_n 0 Not in DORMANT state 1 In DORMANT state
28	SUB_COMMAND_STS	R	0h	The Command register and Response register are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the Error Interrupt Status register or in the UHS-II Error Interrupt Status register. Refer to Section 1.17 about details of response error statuses. Just before Reading of this register, the Sub Command Flag of the Command register or the UHS-II Command register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error [D27 of this register] or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the Auto CMD Error Status register. 1 - Sub Command Status 0 - Main Command Status Reset Source: vbus_amod_g_rst_n

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMD_NOT_ISS_BY_ERR	R	0h	Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error. [Equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the Auto CMD Error Status register.] This status is set to 1 when Host Controller cannot issue a command after setting Command register or UHS-II Command register.Refer to Section 3.10 about 2L-HD error case inUHS-II mode.Sub Command Status [D28] indicates which command is not issued [main or sub]. 1 - Command cannot be issued 0 - No error for issuing a command Reset Source: vbus_amod_g_rst_n
26:25	RESERVED	NONE	0h	Reserved
24	SDIF_CMDIN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
23	SDIF_DAT3IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3]. Reset Source: vbus_amod_g_rst_n
22	SDIF_DAT2IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2]. Reset Source: vbus_amod_g_rst_n
21	SDIF_DAT1IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1]. Reset Source: vbus_amod_g_rst_n
20	SDIF_DAT0IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. Reset Source: vbus_amod_g_rst_n

19	WRITE_PROTECT	R	0h	The Write Protect Switch is supported for memory and combo cards.This bit reflects the SDWP# pin.
				Reset Source: vbus_amod_g_rst_n
				`0 Write protected (SDWP# = 1)`
				`1 Write enabled (SDWP# = 0)`

18	CARD_DETECT	R	0h	This bit reflects the inverse value of the SDCD# pin. '0' No Card present [SDCD# = 1] '1' Card present [SDCD# = 0] Reset Source: vbus_amod_g_rst_n
17	CARD_STATE_STABLE	R	0h	This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1,it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. '0' Reset of Debouncing '1' No Card or Inserted Reset Source: vbus_amod_g_rst_n

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CARD_INSERTED	R	0h	This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SD Bus Power in the Power Control register and SD Clock Enable in the Clock control register. In addition the HD should clear the HC by the Software Reset For All in Software register. The card detect is active regardless of the SD Bus Power. '0' Reset or Debouncing or No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	BUF_RD_ENA	R	0h	This status is used for non-DMA read transfers.This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. Reset Source: vbus_amod_g_rst_n 0 Read Disable 1 Read Enable
10	BUF_WR_ENA	R	0h	This status is used for non-DMA write transfers.This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. Reset Source: vbus_amod_g_rst_n 0 Write Disable 1 Write Enable
9	RD_XFER_ACTIVE	R	0h	This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: After the end bit of the read command. When Writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: When the last data block as specified by block length is transferred to the system. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. '0' No valid data '1' Transferring data Reset Source: vbus_amod_g_rst_n 0 No valid data 1 Transferring data

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WR_XFER_ACTIVE	R	0h	This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: After the end bit of the write command. When Writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count [Single or Multiple] After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. Reset Source: vbus_amod_g_rst_n 0 No valid data 1 Transferring data
7	SDIF_DAT7IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
6	SDIF_DAT6IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
5	SDIF_DAT5IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
4	SDIF_DAT4IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
3	RETUNING_REQ	R	0h	Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 [using fixed sampling clock]. Reset Source: vbus_amod_g_rst_n 0 Fixed or well tuned sampling clock 1 Sampling clock needs re-tuning
2	DATA_LINE_ACTIVE	R	0h	This bit indicates whether one of the DAT line on SD bus is in use. Reset Source: vbus_amod_g_rst_n 0 DAT line inactive 1 DAT line active

Table 14-30026. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INHIBIT_DAT	R	0h	This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit [DAT] [ex. R1b, R5b type]. Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. '0' Can issue command which uses the DAT line '1' Cannot issue command which uses the DATline Reset Source: vbus_amod_g_rst_n
0	INHIBIT_CMD	R	0h	SD Mode If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register [00Fh] is written. This bit is cleared when the command response is received. Even if the Command Inhibit [DAT] is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 gener- ates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issuethe command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Com- mand Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 opera- tion, Host Controller shall manage to issue two commands: CMD12 and a command set by Com-mand register. UHS-II Mode This bit is 0 means that a command packet can be issued by the Host Controller. While this bit is set to 1, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from UHS-II BlockSize [Offset 080h] to the UHS-II Command [Offset 09Eh]. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status-register. 1- Host Controller is not ready to issue a com-mand 0 - Host Controller is ready to issue a command Version 4.10 adds a new control to prevent error statuses from overWriting by receipt of a next com-mand. This status keeps indicating 1 while any of response error statuses is set to 1 [as described in Section 1.17], Command Not Issued by Error in this register is set to 1 or Command Not Issued by Auto CMD12 Error in the Auto CMD Error Status register is set to 1. Software Reset For CMD Lineis used to clear the error statuses above and this status. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.44 MMC_CTLCFG_HOST_CONTROL1 Register

1 MMC_CTLCFG_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

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Table 14-30027. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0028h**

Figure 14-9949. MMC_CTLCFG_HOST_CONTROL1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT		HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-30029. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	This bit selects source for card detection. '0' SDCD# is selected [for normal use] '1' The card detect test level is selected Reset Source: vbus_amod_g_rst_n
6	CD_TEST_LEVEL	R/W	0h	This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates [card ins or card removal] interrupt when the normal int sts enable bit is set. '0' No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
5	EXT_DATA_WIDTH	R/W	0h	This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.This bit is not effective when multiple devices are installed on a bus slot [Slot Type is set to 10b in the Capabilities register]. In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register. Reset Source: vbus_amod_g_rst_n 0 `Bus width is selected by data transfer width` 1 `8-bit bus width`

Table 14-30029. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	DMA_SELECT	R/W	0h	This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the Capabilities register. Selected DMA is enabled by DMA Enable of the Transfer Mode register in SD mode and DMA Enable of UHS-II Transfer Mode register in UHS-II mode. [1] Up to Version 3.00 When Host Version 4 Enable is set to 0, setting of this field is compatible to Host Controller Version 3.00.SDMA is initiated by Writing to the Command register when this field is set to 00b and the SDMA System Address regis-ter [32-bit] is used. SDMA does not support 64-bit address-ing.ADMA2 is initiated by Writing to the Command register when this field is set to 10b or 11b. Lower 32-bit of the ADMA Sys-tem Address register is used when this field is set to 10b and 64-bit of the ADMA System Address register is used when this field is set to 11b. Support of 64-bit System Addressing is indicated by 64-bit System Address Support for V3 in the Capabilities register. 64-bit AMDA2 uses 96-bit Descriptor. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 -32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected [Optional] [2] Version 4.00 or later When Host Version 4 Enable is set to 1, setting of this field is changed as follows. SDMA is initiated by Host Driver writes to the Command reg-ister when this field is set to 00b.ADMA2 is initiated by Host Driver writes to the Command register when this field is set to 10b or 11b and by ADMA3 sets to the ADMA System Address register when this field is set to 11b. ADMA3 is initiated by Host Driver writes to the ADMA3 IDAddress register when this field is set to 11b. 00 - SDMA is selected 01 - Not Used [New assignment is not allowed] 10 - ADMA2 is selected [AMDA3 is not supported or dis-abled] 11 - ADMA2 or ADMA3 is selected Support of 64-bit DMA and 128-bit Descriptor is indicated by 64-bit System Address Support for V4 in the Capabilities register. If the support bit is set to 1, all supported DMAs [depends on Support, ADMA2 Support and ADMA3 Sup-port] shall support 64-bit addressing. 64-bit Addressing in the Host Controller 2 register selects either 32-bit or 64-bit system addressing of DMAs. Reset Source: vbus_amod_g_rst_n
2	HIGH_SPEED_ENA	R/W	0h	This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 [default], the HC outputs CMD line and DAT lines at the falling edge of the SD clock [up to 25 MHz/20MHz for MMC]. If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock [up to 50 MHz for SD/52MHz for MMC]/ 208Mhz [for SD3.0] If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode. Reset Source: vbus_amod_g_rst_n 0 Normal Speed Mode 1 High Speed Mode
1	DATA_WIDTH	R/W	0h	This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode. Reset Source: vbus_amod_g_rst_n 0 1 bit mode 1 4 bit mode

Table 14-30029. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LED_CONTROL	R/W	0h	This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. Reset Source: vbus_amod_g_rst_n 0 `LED off` 1 `LED on`

14.9.4.6.2.45 MMC_CTLCFG_POWER_CONTROL Register

1 MMC_CTLCFG_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

This register is used to program the SD Bus power and voltage level

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Table 14-30030. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0029h**

Figure 14-9950. MMC_CTLCFG_POWER_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-30032. MMC_CTLCFG_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	UHS2_VOLTAGE	R/W	0h	This field determines supply voltage range to VDD2. This field can be set to 101b if 1.8V VDD2 Support in the Capabilities register is set to 1. '000' VDD2 Not supported '001'- '011' Reserved '100' Reserved for 1.2V '101' 1.8V '110' Not Used '111' Not Used Reset Source: vbus_amod_g_rst_n
4	UHS2_POWER	R/W	0h	Setting this bit enables providing VDD2. '0' Power Off '1' Power On Reset Source: vbus_amod_g_rst_n 0 Power Off 1 Power On
3:1	SD_BUS_VOLTAGE	R/W	0h	By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. '000'- '100' Reserved '101' 1.8V '110' 3.0V '111' 3.3V Reset Source: vbus_amod_g_rst_n 0 Reserved 5 1.8V 6 3.0V 7 3.3V

Table 14-30032. MMC_CTLCFG_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Control-ler should immediately stop driving CMD and DAT[3:0] [tri-state], and drive SDCLK to low level [Refer to Section 2.2.14]. If card is connectedto Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1.In UHS-II mode, before clearing this bit, Host Driver shall clear SD Clock Enable and before stopping to sup-ply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt. Reset Source: vbus_amod_g_rst_n 0 Power Off 1 Power On

14.9.4.6.2.46 MMC_CTLCFG_BLOCK_GAP_CONTROL Register

1 MMC_CTLCFG_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

This register is used to program the block gap request, read wait control and interrupt at block gap

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Table 14-30033. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 002Ah**

Figure 14-9951. MMC_CTLCFG_BLOCK_GAP_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	SPI_MODE	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h

Table 14-30035. MMC_CTLCFG_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	To check for the boot acknowledge in boot operation. Reset Source: vbus_amod_g_rst_n 0 Will not wait for boot ack from eMMC card 1 Wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	To start boot code access in alternative mode. Reset Source: vbus_amod_g_rst_n 0 To stop alternative boot code access 1 To start alternative boot code access
5	BOOT_ENABLE	R/W	0h	To start boot code access. Reset Source: vbus_amod_g_rst_n 0 To stop boot code access 1 To start boot code access
4	SPI_MODE	R/W	0h	SPI mode enable bit. Reset Source: vbus_amod_g_rst_n 0 SD Mode 1 SPI Mode
3	INTRPT_AT_BLK_GAP	R/W	0h	This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. Reset Source: vbus_amod_g_rst_n

Table 14-30035. MMC_CTLCFG_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported. In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card. Reset Source: vbus_amod_g_rst_n 0 `Disable Read-Wait Control` 1 `Enable Read-Wait Control`
1	CONTINUE	R/W	0h	This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The Host Controller automatically clears this bit when the transaction re-starts. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. In SD mode, this bit is cleared in either of the following cases: [1] In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. [2] In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. '0' Ignore '1' Restart Reset Source: vbus_amod_g_rst_n 0 `Ignore` 1 `Restart`
0	STOP_AT_BLK_GAP	R/W	0h	This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit [DAT] in the Present State register. In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst [Flow Control basis]. Host Control-ler waits for sending Flow Control MSG until Continue Request is set to 1. '0' Transfer '1' Stop Reset Source: vbus_amod_g_rst_n 0 `Transfer` 1 `Stop`

14.9.4.6.2.47 MMC_CTLCFG_WAKEUP_CONTROL Register

1 MMC_CTLCFG_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

This register is used to program the wakeup functionality

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Table 14-30036. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 002Bh**

Figure 14-9952. MMC_CTLCFG_WAKEUP_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-30038. MMC_CTLCFG_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	CARD_REMOVAL	R/W	0h	This bit enables wakeup event via Card removal assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card removal
1	CARD_INSERTION	R/W	0h	This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card Insertion
0	CARD_INTERRUPT	R/W	0h	This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.This bit can be set to 1 if FN_WUS [Wake Up Support] in CIS is set to 1. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card Interrupt

14.9.4.6.2.48 MMC_CTLCFG_CLOCK_CONTROL Register

1 MMC_CTLCFG_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

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Table 14-30039. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 002Ch**

Figure 14-9953. MMC_CTLCFG_CLOCK_CONTROL Name Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W							
0h							

7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS		CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA
R/W		R/W	NONE	R/W	R/W	R	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-30041. MMC_CTLCFG_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SDCLK_FRQSEL	R/W	0h	This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. [1] 8-bit Divided Clock Mode 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock[10MHz-63MHz] Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. [1] 25 MHz divider value. [2] 400 KHz divider value. The frequency of the SDCLK is set by the following formula: Clock Frequency = [Baseclock] / divisor. Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. Maximum Frequency for SD = 50Mhz [base clock] Maximum Frequency for MMC = 52Mhz [base clock] Minimum Frequency = 195.3125Khz [50Mhz / 256], same calculation for MMC also. [2] 10-bit Divided Clock Mode Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to10 bits and all divider values shall be supported. 3FFh --1/2046 Divided Clock N -------1/2N Divided Clock [Duty 50%] 002h -- 1/4 Divided Clock 001h ---1/2 Divided Clock 000h --- Base Clock [10MHz-254MHz] Reset Source: vbus_amod_g_rst_n
7:6	SDCLK_FRQSEL_UPBITS	R/W	0h	Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select. Reset Source: vbus_amod_g_rst_n
5	CLKGEN_SEL	R/W	0h	This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported [non-zero value is set to Clock Multiplier in the Capabilities register], this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. '0' Divided Clock Mode '1' Programmable Clock Mode Reset Source: vbus_amod_g_rst_n 0 Divided Clock Mode 1 Programmable Clock Mode
4	RESERVED	NONE	0h	Reserved

Table 14-30041. MMC_CTLCFG_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL_ENA	R/W	0h	This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable and PLL Enable and to minimize output latency [ex. SDCLK/RCLK, D0lane] from SD Clock Enable. There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable. [1] When Host Version 4 Enable =0 [Host Driver Version 3, which does not support this bit] or this bit is not implemented,Internal Clock Enable [or SD Clock Enable] may activate PLL [exit low power mode and start locking clock]. [2] When Host Version 4 Enable =1 [Host Driver Version 4],Internal Clock Enable is set before setting this bit and then setting this bit may activate PLL [exit low power mode and start locking clock]. Reset Source: vbus_amod_g_rst_n 0 `PLL is in low power mode` 1 `PLL is enabled`
2	SD_CLK_ENA	R/W	0h	The HC shall stop SDCLK when Writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until SDCLK is stopped [Stop at SDCLK = 0]. If the HC detects the No Card state, this bit shall be cleared. Reset Source: vbus_amod_g_rst_n 0 `Disable providing SDCLK` 1 `Enable providing SDCLK`
1	INT_CLK_STABLE	R	0h	This bit is set to 1 when SD clock is stable after Writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. Note: This is useful when using PLL for a clock oscillator that requires setup time. Reset Source: vbus_amod_g_rst_n 0 `Not Ready` 1 `Ready`
0	INT_CLK_ENA	R/W	0h	This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. Reset Source: vbus_amod_g_rst_n 0 `Stop` 1 `Oscillate`

14.9.4.6.2.49 MMC_CTLCFG_TIMEOUT_CONTROL Register

1 MMC_CTLCFG_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

The register sets the Data Timeout counter value

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Table 14-30042. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 002Eh**

Figure 14-9954. MMC_CTLCFG_TIMEOUT_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
NONE				R/W			
0h				0h			

Table 14-30044. MMC_CTLCFG_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE	0h	Reserved
3:0	COUNTER_VALUE	R/W	0h	This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sdclockTMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable [in the Error Interrupt Status Enable register]. 1111 - Reserved 1110 - TMCLK * 2^27 -------------------- -------------------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13 Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.50 MMC_CTLCFG_SOFTWARE_RESET Register

1 MMC_CTLCFG_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

This register is used to program the software reset for data, command and for all

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Table 14-30045. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 002Fh**

Figure 14-9955. MMC_CTLCFG_SOFTWARE_RESET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_ DAT	SWRST_FOR_ CMD	SWRST_FOR_ ALL
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-30047. MMC_CTLCFG_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	SWRST_FOR_DAT	R/W	0h	Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register: Buffer is cleared and Initialized. Present State register: Buffer read Enable, Buffer write Enable, Read Transfer Active, Write Transfer Active, DAT Line Active, Command Inhibit [DAT]. Block Gap Control register: Continue Request, Stop At Block Gap Request. Normal Interrupt Status register: Buffer Read Ready, Buffer Write Ready, Block Gap Event, Transfer Complete. Reset Source: vbus_amod_g_rst_n 0 Work 1 Reset
1	SWRST_FOR_CMD	R/W	0h	Software Reset For CMD Line Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit [including response error statuses related to Com-mand Inhibit [CMD] control] and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub com- mand response errors. The following registers and bits are cleared by this bit: Present State register Command Inhibit [CMD] Normal Interrupt Status register Command Complete Error Interrupt Status [from Version 4.10] Response error statuses related to Com-mand Inhibit [CMD] Reset Source: vbus_amod_g_rst_n 0 Work 1 Reset

Table 14-30047. MMC_CTLCFG_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SWRST_FOR_ALL	R/W	0h	This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. Reset Source: vbus_amod_g_rst_n 0 `Work` 1 `Reset`

14.9.4.6.2.51 MMC_CTLCFG_NORMAL_INTR_STS Register

1 MMC_CTLCFG_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

This register gives the status of all the interrupts

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Table 14-30048. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0030h**

Figure 14-9956. MMC_CTLCFG_NORMAL_INTR_STS Name Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R	R/W1TC	R/W1TC	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30050. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the UHS-II Error Interrupt Status register are set, this bit is also set. '0' No error '1' Error Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Error interrupt is generated
14	BOOT_COMPLETE	R/W1TC	0h	This status is set if the boot operation gets terminated. '0' Boot operation is not terminated '1' Boot operation is terminated Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Boot Terminate interrupt is generated
13	RCV_BOOT_ACK	R/W1TC	0h	This status is set if the boot acknowledge is received from device. '0' Boot ack not recieved '1' Boot ack is recieved Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Boot acknowledge is received
12	RETUNING_EVENT	R	0h	This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer [not large block count] can be completed without re-tuning.In UHS-II mode, this bit is not effective '0' Re-tuning not required '1' Re-tuning should be performed Reset Source: vbus_amod_g_rst_n

Table 14-30050. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	INTC	R	0h	This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Reset Source: vbus_amod_g_rst_n
10	INTB	R	0h	This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Reset Source: vbus_amod_g_rst_n
9	INTA	R	0h	This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. NOTE : INT_A, INT_B, and INT_C are to be implemented based on the Application Requirements. By default these are not implemented as there is no specific requirement from Customers. Reset Source: vbus_amod_g_rst_n
8	CARD_INTR	R	0h	When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt status latched in the Host Controller and to stop driv-ing the interrupt signal to the Host System.After completion of the card interrupt service [It should reset interrupt factors in the SD card and the interrupt signal may not be asserted],set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt fac-tor. [1] DAT[1] Interrupt Input in SD Mode In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt sig-nal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the inter-rupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is sta-ble. [2] DAT[2] Interrupt Input in UHS-II Mode When Card Inserted in the Present State reg-ister and SD Bus Power for VDD1 in the Power Control register are set to 1, Host Con-troller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3V signal level. DAT[2] interrupt is masked by setting Card Interrupt Status Enable to 0 in the Normal Interrupt register.When either Card Inserted or SD Bus Power for VDD1 is set to 0, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card. [3] INT MSG in UHS-II Mode INT MSG is enabled by setting INT MSG Enable in the UHS-II Device Select register. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the UHS-II Device Interrupt Status regis- ter is set to 1, INT MSG interrupt is generated. INT MSG interrupt is cleared by Writing a cor-respondent bit to 1 in the UHS-II Device Inter-rupt Status register. Masking DAT[2] interrupt also disables INT MSG interrupt due to Card Interrupt Status Enable is set to 0. SDIO Ver-sion 4.00 does not support INT MSG. '0' No Card Interrupt '1' Generate Card Interrupt Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Card interrupt is generated

Table 14-30050. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REM	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Removed Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Card removal interrupt is generated`
6	CARD_INS	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 0 to 1.When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Inserted Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Card insertion interrupt is generated`
5	BUF_RD_READY	R/W1TC	0h	This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to read buffer, '1' Ready to read buffer Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Buffer Read Ready interrupt is generated`
4	BUF_WR_READY	R/W1TC	0h	This status is set if the Buffer Write Enable changes from 0 to 1.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to write to buffer, '1' Ready to write to buffer Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Buffer Write Ready interrupt is generated`
3	DMA_INTERRUPT	R/W1TC	0h	This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser. '0' No DMA Interrupt '1' DMA Interrupt is generated Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `DMA interrupt is generated`

Table 14-30050. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W1TC	0h	If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status [When the transaction is stopped at SD Bus timing. The Read Wait must be supported inorder to use this function]. Write Transaction: This bit is set at the falling edge of Write Transfer Active Status [After getting CRC status at SD Bus timing]. In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' No Block Gap Event '1' Transaction stopped at Block Gap Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Block Gap Event is generated
1	XFER_COMPLETE	R/W1TC	0h	This bit is set when a read / write transaction is completed. SD Mode Read Transaction: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length [After the last data has been read to the Host Sys- tem]. The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control Register [After valid data has been read to the Host System]. Write Transaction: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control Register and data transfers completed. [After valid data is written to the SD card and the busy signal is released]. Note: Transfer Complete has higher priority than Data Time-out Error. If both bits are set to 1, the data transfer can be considered complete. Note: While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1 Command with Busy: This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit[DAT] in the Present State register.UHS-I mode While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1. '0' No Data Transfer Complete, '1' Data Transfer Complete UHS-II Mode This interrupt is generated in following twocases: [a] EBSY Completion [for EBSY supported commands] When EBSY Wait in the UHS-II Transfer Mode register is set to 1, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation. [b] Stop and Continue during DCMD Data Transfer When Stop At Block Gap Request in the Block Gap Control register is set to 1 and data transfer is stopped at the Flow Control. Following is for both SD mode and UHS-II mode. The table below shows that Transfer Com-plete has higher priority than Data Timeout Error. If both bits are set to 1, execution of a command can be considered to be completed. 1 - Command execution is completed 0 - Not complete Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Transfer complete interrupt is generated

Table 14-30050. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_COMPLETE	R/W1TC	0h	SD Mode This bit is set when we get the end bit of the command response [Except Auto CMD12 and Auto CMD23] Note: Command Time-out Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. Version 4.00 defines response check function for R1 and R5. If Response Interrupt Disable in the Transfer Mode register is set to 1, gen-eration of this interrupt is prohibited regardless of Command Complete Signal Enable. UHS-II Mode If Response Interrupt Disable is set to 0 in the UHS-II Transfer Mode register, this interrupt is generated when response packet is received.If Response Interrupt Disable is set to 1 in the UHS-II Transfer Mode register, generation of this interrupt is prohibited regardless of Com-mand Complete Signal Enable. '0' No Command Complete, '1' Command Complete Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Command complete interrupt is generated`

14.9.4.6.2.52 MMC_CTLCFG_ERROR_INTR_STS Register

1 MMC_CTLCFG_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

This register gives the status of the error interrupts

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Table 14-30051. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0032h**

Figure 14-9957. MMC_CTLCFG_ERROR_INTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30053. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	R/W1TC	0h	Occurs when detecting ERROR in m_hresp[dma transaction] Reset Source: vbus_amod_g_rst_n 0 No Error 1 Host Error
11	RESP	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1.If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Response Error
10	TUNING	R/W1TC	0h	This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure [Occurrence of an error during tuning procedure is indicated by Sampling Select]. By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning.To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Turning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Tuning Error

Table 14-30053. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADMA	R/W1TC	0h	This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `ADMA Error`
8	AUTO_CMD	R/W1TC	0h	Auto CMD12 and Auto CMD23 use this error status.This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared with clearing of this bit [another implementation is also allowed]. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Auto CMD Error`
7	CURR_LIMIT	R/W1TC	0h	By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Power Fail`
6	DATA_ENDBIT	R/W1TC	0h	Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data Endbit Error`
5	DATA_CRC	R/W1TC	0h	Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data CRC Error`
4	DATA_TIMEOUT	R/W1TC	0h	Occurs when detecting one of following timeout conditions: 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data Timeout Error`
3	CMD_INDEX	R/W1TC	0h	Occurs if a Command Index error occurs in the Command Response. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command Index Error`

Table 14-30053. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CMD_ENDBIT	R/W1TC	0h	Occurs when detecting that the end bit of a command response is 0. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command End bit Error`
1	CMD_CRC	R/W1TC	0h	Command CRC Error is generated in two cases. 1. If a response is returned and the Command Time-out Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command [Stop driving CMD line] and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command CRC Error`
0	CMD_TIMEOUT	R/W1TC	0h	Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command Timeout Error`

14.9.4.6.2.53 MMC_CTLCFG_NORMAL_INTR_STS_ENA Register

1 MMC_CTLCFG_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

This register is used to enable the normal interrupt status register fields

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Table 14-30054. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0034h**

Figure 14-9958. MMC_CTLCFG_NORMAL_INTR_STS_ENA Name Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30056. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HC shall control error Interrupts using the Error Interrupt Status Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
12	RETUNING_EVENT	R/W	0h	0 - Masked 1 - Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	INTC	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30056. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
9	INTA	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
8	CARD_INTERRUPT	R/W	0h	If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. By setting this bit to 0, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state [ex. floating]. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
3	DMA_INTERRUPT	R/W	0h	'0' Masked, '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

Table 14-30056. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

14.9.4.6.2.54 MMC_CTLCFG_ERROR_INTR_STS_ENA Register

1 MMC_CTLCFG_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

This register is used to enable the Error Interrupt Status register fields

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Table 14-30057. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0036h**

Figure 14-9959. MMC_CTLCFG_ERROR_INTR_STS_ENA Name Register

15	14	13	12	11	10	9	8
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30059. MMC_CTLCFG_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	RESP	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
10	TUNING	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
9	ADMA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30059. MMC_CTLCFG_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

14.9.4.6.2.55 MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register

1 MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

This register is used to enable the Normal Interrupt Signal register

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Table 14-30060. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0038h**

Figure 14-9960. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Name Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30062. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HD shall control error Interrupts using the Error Interrupt Signal Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
12	RETUNING_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
11	INTC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

Table 14-30062. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
9	INTA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
8	CARD_INTERRUPT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
3	DMA_INTERRUPT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30062. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

14.9.4.6.2.56 MMC_CTLCFG_ERROR_INTR_SIG_ENA Register

1 MMC_CTLCFG_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

This register is used to enable Error Interrupt Signal register

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Table 14-30063. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 003Ah**

Figure 14-9961. MMC_CTLCFG_ERROR_INTR_SIG_ENA Name Register

15	14	13	12	11	10	9	8
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30065. MMC_CTLCFG_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	RESP	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
10	TUNING	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
9	ADMA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30065. MMC_CTLCFG_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

14.9.4.6.2.57 MMC_CTLCFG_AUTOCMD_ERR_STS Register

1 MMC_CTLCFG_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

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Table 14-30066. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 003Ch**

Figure 14-9962. MMC_CTLCFG_AUTOCMD_ERR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISSUED	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R	NONE	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30068. MMC_CTLCFG_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error [D04- D01] in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Not Issued`
6	RESERVED	NONE	0h	Reserved
5	RESP	R	0h	This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or Auto CMD23. This status should be ignored if any bit of D00 to D04 is set to 1. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Auto Command Response Error`
4	INDEX	R	0h	Occurs if the Command Index error occurs in response to a command. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Auto Command Index Error`
3	ENDBIT	R	0h	Occurs when detecting that the end bit of command response is 0. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Auto Command End Bit Error`

Table 14-30068. MMC_CTLCFG_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	CRC	R	0h	Occurs when detecting a CRC error in the command response.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Auto Command CRC Error`

1	TIMEOUT	R	0h	Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.If this bit is set to 1, the other error status bits [D04 - D02] are meaningless.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Auto Command Timeout Error`

0	ACMD12_NOT_EXEC	R	0h	If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits [D04 - D01] are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Not Executed`

14.9.4.6.2.58 MMC_CTLCFG_HOST_CONTROL2 Register

1 MMC_CTLCFG_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

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Table 14-30069. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 003Eh**

Figure 14-9963. MMC_CTLCFG_HOST_CONTROL2 Name Register

15	14	13	12	11	10	9	8
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SAMPLING_CLK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1		V1P8_SIGNAL_ENA	UHS_MODE_SELECT		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		

Table 14-30071. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers. Reset Source: vbus_amod_g_rst_n 0 `SDCLK and Driver Strength are controlled by Host Driver` 1 `Automatic Selection by Preset Value are Enabled`
14	ASYNCH_INTR_ENA	R/W	0h	This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode [and zero is set to Interrupt Pin Select in the Shared Bus Control register]. If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. Reset Source: vbus_amod_g_rst_n 0 `Asynchronous Interrupt disabled` 1 `Asynchronous Interrupt enabled`

Table 14-30071. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	BIT64_ADDRESSING	R/W	0h	This field is effective when Host Version 4.00 Enable is set to 1. Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the Capabilities register. . Reset Source: vbus_amod_g_rst_n 0 `32 bit addressing` 1 `64 bit addressing`
12	HOST_VER40_ENA	R/W	0h	This bit selects either Version 3.00 compatible mode or Ver4.mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit. In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified. SDMA Address SDMA uses ADMA System Address register [05Fh-058h] instead of SDMA System Address register [Offset 003-000h] ADMA2 / ADMA3 Selection ADMA3 is selected by DMA Select in the Host Control 1 regis-ter. 64bit ADMA Descriptor Size 128bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1. Selection of 32-bit / 64-bit System Addressing Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of DMA Select in the Host Control 1 register. 32-bit Block Count SDMA System Address register [003h-000h] is modified to 32-bit Block Count register. Reset Source: vbus_amod_g_rst_n 0 `Version 3.00 Compatible Mode` 1 `Version 4 Mode`
11	CMD23_ENA	R/W	0h	In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 [SCR[33]=1], this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Refer to Auto CMD Enable in the Transfer Mode regis-ter. Reset Source: vbus_amod_g_rst_n 0 `CMD23 Disable` 1 `CMD23 Enable`
10	ADMA2_LEN_MODE	R/W	0h	This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit. Reset Source: vbus_amod_g_rst_n 0 `16-bit Data Length Mode` 1 `26-bit Data Length Mode`
9	DRIVER_STRENGTH2	R/W	0h	This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value. Reset Source: vbus_amod_g_rst_n

Table 14-30071. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	UHS2_INTF_ENABLE	R/W	0h	This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1. Before trying to start SD mode initialization, this bit shall be set to 0. This bit is used to enable UHS-II IF Detection, Lane Synchroni-zation and In Dormant State in the Present State register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines [CLK, CMD and DAT[3:2]] floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict. '0' 4-bit SD Interface enabled '1' UHS-II Interface enabled Reset Source: vbus_amod_g_rst_n 0 4-bit SD Interface enabled 1 UHS-II Interface enabled
7	SAMPLING_CLK_SELECT	R/W	0h	This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by Writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. Reset Source: vbus_amod_g_rst_n 0 Fixed clock is used to sample data 1 Tuned clock is used to sample data
6	EXECUTE_TUNING	R/W	0h	This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by Writing 0 for more detail about tuning procedure. '0' Not Tuned or Tuning Completed '1' Execute Tuning Reset Source: vbus_amod_g_rst_n
5:4	DRIVER_STRENGTH1	R/W	0h	Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected (Default) 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected

Table 14-30071. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	V1P8_SIGNAL_ENA	R/W	0h	This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling [One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register] and the card or device supports UHS-I. '0' 3.3V Signalling, '1' 1.8V Signalling Reset Source: vbus_amod_g_rst_n 0 `3.3V Signalling` 1 `1.8V Signalling`
2:0	UHS_MODE_SELECT	R/W	0h	This field is used to select one of UHS-I modes or UHS-II mode.In case of UHS-I mode, this field is effective when 1.8V Signal-ing Enable is set to 1. In case of UHS-II mode, 1.8V Signaling Enable shall be set to 0. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode. If Preset Value Enable in the Host Control 2 register is set to 1,Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail. Reset Source: vbus_amod_g_rst_n 0 `SDR12` 1 `SDR25` 2 `SDR50` 3 `SDR104` 4 `DDR50` 5 `HS400` 6 `Reserved` 7 `UHS-II`

14.9.4.6.2.59 MMC_CTLCFG_CAPABILITIES Register

1 MMC_CTLCFG_CAPABILITIES Register (Offset = 40h) [reset = 180004073DECC7F4h]

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initializa-tion.

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Table 14-30072. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0040h**

Figure 14-9964. MMC_CTLCFG_CAPABILITIES Name Register

63	62	61	60	59	58	57	48
HS400_SUPPORT	RESERVED		VDD2_1P8_SUPPORT	ADMA3_SUPPORT	RESERVED	SPI_BLK_MODE	SPI_SUPPORT
R	NONE		R	R	NONE	R	R
0h	0h		1h	1h	0h	0h	0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R							
0h							
47	46	45	44	43	42	41	40
RETUNING_MODES		TUNING_FOR_SDR50	RESERVED	RETUNING_TIMER_CNT			
R		R	NONE	R			
0h		0h	0h	4h			
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUPPORT	DRIVERC_SUPPORT	DRIVERA_SUPPORT	UHS2_SUPPORT	DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
NONE	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	1h	1h	1h
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R							
C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R	NONE	R					
0h	1h	1h					

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description

63	HS400_SUPPORT	R	0h	1 HS400 is Supported
				0 HS400 is Not Supported
				Reset Source: vbus_amod_g_rst_n
				`0       HS400 Mode is not Supported`
				`1       HS400 Mode is Supported`

62:61	RESERVED	NONE	0h	Reserved

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
60	VDD2_1P8_SUPPORT	R	1h	This field indicates that support of VDD2 on Host system. Reset Source: vbus_amod_g_rst_n 0 `1.8V VDD2 is not Supported` 1 `1.8V VDD2 is Supported`
59	ADMA3_SUPPORT	R	1h	This field indicates that support of ADMA3 on Host Controller. Reset Source: vbus_amod_g_rst_n 0 `ADMA3 is not Supported` 1 `ADMA3 is Supported`
58	RESERVED	NONE	0h	Reserved
57	SPI_BLK_MODE	R	0h	This field indicates whether SPI Block Mode is supported or not. Reset Source: vbus_amod_g_rst_n 0 `SPI Block Mode is not Supported` 1 `SPI Block Mode is Supported`
56	SPI_SUPPORT	R	0h	This field indicates whether SPI Mode is supported or not. Reset Source: vbus_amod_g_rst_n 0 `SPI Mode is not Supported` 1 `SPI Mode is Supported`
55:48	CLOCK_MULTIPLIER	R	0h	This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. 'FF' Clock Multiplier M = 256 --------- '02' Clock Multiplier M = 3 '01' Clock Multiplier M = 2 '00' Clock Multiplier is Not Supported. Reset Source: vbus_amod_g_rst_n
47:46	RETUNING_MODES	R	0h	This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. '00' Mode 1 '01' Mode 2 '10' Mode 3 '11' Reserved. There are two re-tuning timings:Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue. Reset Source: vbus_amod_g_rst_n 0 `Mode 1` 1 `Mode 2` 2 `Mode 3` 3 `Reserved`
45	TUNING_FOR_SDR50	R	0h	If this bit is set to 1, this Host Controller requires tuning to operate SDR50. [Tuning is always required to operate SDR104]. '0' '1' Reset Source: vbus_amod_g_rst_n 0 `SDR50 does not require tuning` 1 `SDR50 requires tuning`
44	RESERVED	NONE	0h	Reserved

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
43:40	RETUNING_TIMER_CNT	R	4h	This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ------ n = 2[n-1] seconds ------ Bh = 1024 seconds Fh - Ch = Reserved Reset Source: vbus_amod_g_rst_n
39	RESERVED	NONE	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	This bit indicates support of Driver Type D for 1.8 Signaling. '0' Driver Type D is Not supported, '1' Driver Type D is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type D is not Supported` 1 `Driver Type D is Supported`
37	DRIVERC_SUPPORT	R	0h	This bit indicates support of Driver Type C for 1.8 Signaling. '0' Driver Type C is Not supported, '1' Driver Type C is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type C is not Supported` 1 `Driver Type C is Supported`
36	DRIVERA_SUPPORT	R	0h	This bit indicates support of Driver Type A for 1.8 Signaling. '0' Driver Type A is Not supported, '1' Driver Type A is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type A is not Supported` 1 `Driver Type A is Supported`
35	UHS2_SUPPORT	R	0h	This bit indicates whether Host controller supports UHS-II. If this bit is set to 1, 1.8V VDD2 Support shall be set to 1 [Host Sys- tem shall support VDD2 power supply]. 1 UHS-II is Supported 0 UHS-II is Not Supported Reset Source: vbus_amod_g_rst_n 0 `UHS-II is not Supported` 1 `UHS-II is Supported`
34	DDR50_SUPPORT	R	1h	This bit indicates whether DDR50 is supported or not. Reset Source: vbus_amod_g_rst_n 0 `DDR50 is not Supported` 1 `DDR50 is Supported`
33	SDR104_SUPPORT	R	1h	This bit indicates whether SDR104 is supported or not.SDR104 requires tuning. Reset Source: vbus_amod_g_rst_n 0 `SDR104 is not Supported` 1 `SDR104 is Supported`
32	SDR50_SUPPORT	R	1h	If SDR104 is supported, this bit shall be set to 1. Bit 40 indicates whether SDR50 requires tuning or not. Reset Source: vbus_amod_g_rst_n 0 `SDR50 is not Supported` 1 `SDR50 is Supported`

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31:30	SLOT_TYPE	R	0h	This field indicates usage of a slot by a specific Host System. [A host controller register set is defined perslot.] Embedded slot for one device [01b] means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot [10b] can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus [10b], the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. Reset Source: vbus_amod_g_rst_n 0 Removeable Card Slot 1 Embedded Slot for One Device 2 Shared Bus Slot (SD Mode) 3 Reserved
29	ASYNCH_INTR_SUPPORT	R	1h	Refer to SDIO Specification Version 3.00 about asynchronous interrupt. Reset Source: vbus_amod_g_rst_n 0 Asynchronous Interrupt not Supported 1 Asynchronous Interrupt Supported
28	ADDR_64BIT_SUPPORT_V3	R	1h	IMeaning of this bit is different depends on Versions [Refer to Table 2-35 for more details]. Host Controller Version 3.00 and Ver4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes. SDMA cannot be used in 64-bit Address-ing in Version 3 mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows: In case of Host Controller Version 3, 64-bit ADMA2 is enabled by DMA Select =11b in the Host Control 1 register. In case of Host Controller Version 4, 64-bitADMA2 for Version 3 is enabled by setting Host Version 4 Enable =0 and DMA Select = 11b. 1 - 64-bit System Address for V3 is Supported 0 - 64-bit System Address for V3 is not Supported Reset Source: vbus_amod_g_rst_n 0 64-bit System Address for V3 is not Supported 1 64-bit System Address for V3 is Supported
27	ADDR_64BIT_SUPPORT_V4	R	1h	This bit is added from Version 4.10. Set-ting 1 to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode [Refer to Table 2-35 for the summary of 64-bit system address support].. When this bit is set to 1, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to 64bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Address-ing for Version 4 is enabled by setting Host Version 4 Enable =1, 64-bit Address-ing =1 in the Host Control 2 register.SDMA can be used and ADMA2 uses 128-bit Descriptor. Reset Source: vbus_amod_g_rst_n 0 64-bit System Address for V4 is not Supported 1 64-bit System Address for V4 is Supported

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	VOLT_1P8_SUPPORT	R	1h	This bit indicates whether the HC supports 1.8V. Reset Source: vbus_amod_g_rst_n 0 1.8V Not Supported 1 1.8V Supported
25	VOLT_3P0_SUPPORT	R	0h	This bit indicates whether the HC supports 3.0V. Reset Source: vbus_amod_g_rst_n 0 3.0V Not Supported 1 3.3V Supported
24	VOLT_3P3_SUPPORT	R	1h	This bit indicates whether the HC supports 3.3V. Reset Source: vbus_amod_g_rst_n 0 3.3V Not Supported 1 3.3V Supported
23	SUSP_RES_SUPPORT	R	1h	This bit indicates whether the HC supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend / Resume commands. Reset Source: vbus_amod_g_rst_n 0 Suspend and Resume mechanism Not Supported 1 Suspend and Resume mechanism Supported
22	SDMA_SUPPORT	R	1h	This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. Reset Source: vbus_amod_g_rst_n 0 SDMA Not Supported 1 SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25Mhz to 50 Mhz [for SD]/ 20MHz to 52MHz [for MMC]. Reset Source: vbus_amod_g_rst_n 0 High Speed Not Supported 1 High Speed Supported
20	RESERVED	NONE	0h	Reserved
19	ADMA2_SUPPORT	R	1h	'0' ADMA2 Not Supported '1' ADMA2 Supported Reset Source: vbus_amod_g_rst_n 0 ADMA2 Not Supported 1 ADMA2 Supported
18	BUS_8BIT_SUPPORT	R	1h	This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when Slot Type is set to 10b. In this case, refer to Bus Width Preset in the Shared Bus resister. Reset Source: vbus_amod_g_rst_n 0 Extended Media Bus Not Supported 1 Extended Media Bus Supported

Table 14-30074. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	MAX_BLK_LENGTH	R	0h	This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. Reset Source: vbus_amod_g_rst_n 0 512 byte 1 1024 byte 2 2048 byte 3 4096 byte
15:8	BASE_CLK_FREQ	R	C8h	[1]6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1MHz. The supported clock range is 10MHz to 63MHz. '11xx xxxxb' Not Supported '0011 1111b' 63MHz '0000 0010b' 2MHz '0000 0001b' 1MHz '0000 0000b'Get Information via another method [2]8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00.Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. 'FFh' 255MHz '02h' 2MHz '01h' 1MHz '00h' Get Information via another method. If the real frequency is 16.5MHz, the lager value shall be set 0001 0001b [17MHz] because the Host Driver use this value to calculate the clock divider value [Refer to the SDCLK Frequency Select in the Clock Control register.] and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method. Reset Source: vbus_amod_g_rst_n
7	TIMEOUT_CLK_UNIT	R	0h	This bit shows the unit of base clock frequency used to detect Data Timeout Error. Reset Source: vbus_amod_g_rst_n 0 KHz 1 MHz
6	RESERVED	NONE	1h	Reserved
5:0	TIMEOUT_CLK_FREQ	R	1h	This bit shows the base clock frequency used to detect Data Timeout Error. '000000' Get Information via another method, 'not 0' 1KHz to 63KHz/ 1MHz to 63MHz Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.60 MMC_CTLCFG_MAX_CURRENT_CAP Register

1 MMC_CTLCFG_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

This register indicates maximum current capability for each voltage

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Table 14-30075. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0048h**

Figure 14-9965. MMC_CTLCFG_MAX_CURRENT_CAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
VDD2_1P8V							
R							
0h							
15	14	13	12	11	10	9	8
VDD1_3P0V							
R							
0h							
7	6	5	4	3	2	1	0
VDD1_3P3V							
R							
0h							

Table 14-30077. MMC_CTLCFG_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved
39:32	VDD2_1P8V	R	0h	Maximum Current for 1.8V VDD2 Reset Source: vbus_amod_g_rst_n
31:24	RESERVED	NONE	0h	Reserved
23:16	VDD1_1P8V	R	0h	Maximum Current for 1.8V VDD1 Reset Source: vbus_amod_g_rst_n
15:8	VDD1_3P0V	R	0h	Maximum Current for 3.0V VDD1 Reset Source: vbus_amod_g_rst_n

Table 14-30077. MMC_CTLCFG_MAX_CURRENT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	VDD1_3P3V	R	0h	Maximum Current for 3.3V VDD1 Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.61 MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register

1 MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written. Writing 1 : set each bit of the Auto CMD12 Error Status Register Writing 0 : no effect.

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Table 14-30078. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0050h**

Figure 14-9966. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30080. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
6	RESERVED	NONE	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error.. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
4	INDEX	W	0h	Force Event for AUTO CMD Index Error.. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated

Table 14-30080. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`

14.9.4.6.2.62 MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register

1 MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

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Table 14-30081. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0052h**

Figure 14-9967. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			W	W	W	W	W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30083. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	W	0h	Force Event for Host Error Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
11	RESP	W	0h	Force Event for Response Error Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
10	TUNING	W	0h	Force Event for Tuning Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
9	ADMA	W	0h	Force Event for ADMA Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
7	CURR_LIM	W	0h	Force Event for Current Limit Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`

Table 14-30083. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
5	DAT_CRC	W	0h	Force Event for Data CRC Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
3	CMD_INDEX	W	0h	Force Event for Command Index Error Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
1	CMD_CRC	W	0h	Force Event for Command CRC Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated

14.9.4.6.2.63 MMC_CTLCFG_ADMA_ERR_STATUS Register

1 MMC_CTLCFG_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

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Table 14-30084. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0054h**

Figure 14-9968. MMC_CTLCFG_ADMA_ERR_STATUS Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ADMA_LENGTH_ERR</td><td colspan="2">ADMA_ERR_STATE</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td colspan="2">R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-30086. MMC_CTLCFG_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Error set`
1:0	ADMA_ERR_STATE	R	0h	This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 D00 : ADMA Error State when error occurred Contents of SYS_SDR register. Reset Source: vbus_amod_g_rst_n 0 `ST_STOP(Stop DMA) Points to next of the error descriptor` 1 `ST_FDS(Fetch Descriptor)Points to the error descriptor` 2 `Never set this state(Not Used)` 3 `ST_TFR(Transfer Data) Points to the next of the error descriptor`

14.9.4.6.2.64 MMC_CTLCFG_ADMA_SYS_ADDRESS Register

1 MMC_CTLCFG_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = 0h]

This register contains the physical address used for ADMA data transfer

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Table 14-30087. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0058h**

Figure 14-9969. MMC_CTLCFG_ADMA_SYS_ADDRESS Name Register

63	62	61	60	59	58	57	48
ADMA_ADDR							
R/W							
0h							
55	54	53	52	51	50	49	48
ADMA_ADDR							
R/W							
0h							
47	46	45	44	43	42	41	40
ADMA_ADDR							
R/W							
0h							
39	38	37	36	35	34	33	32
ADMA_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
ADMA_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADMA_ADDR							
R/W							
0h							

Table 14-30089. MMC_CTLCFG_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	ADMA_ADDR	R/W	0h	The 32-bit addressing Host Driver uses lower 32-bit of this register [upper 32-bit should be set to 0] and shall program Descriptor Table on 32-bit boundary andset 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 00b. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register andassumes it to be 000b. SDMA If Host Version 4.00 Enable is set to 1, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register [Offset 003-000h]. SDMA can be used in 32-bit and 64-bit addressing in Version 4.00. ADMA2 This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. ADMA3 This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register,which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. Register Value - 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.65 MMC_CTLCFG_PRESET_VALUE0 Register

1 MMC_CTLCFG_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30090. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0060h**

Figure 14-9970. MMC_CTLCFG_PRESET_VALUE0 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	100h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
100h							

Table 14-30092. MMC_CTLCFG_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	100h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.66 MMC_CTLCFG_PRESET_VALUE1 Register

1 MMC_CTLCFG_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30093. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0062h**

Figure 14-9971. MMC_CTLCFG_PRESET_VALUE1 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	4h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
4h							

Table 14-30095. MMC_CTLCFG_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description

15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.
				Reset Source: vbus_amod_g_rst_n
				`0 Driver Type B is Selected`
				`1 Driver Type A is Selected`
				`2 Driver Type C is Selected`
				`3 Driver Type D is Selected`

13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.67 MMC_CTLCFG_PRESET_VALUE2 Register

1 MMC_CTLCFG_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30096. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0064h**

Figure 14-9972. MMC_CTLCFG_PRESET_VALUE2 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30098. MMC_CTLCFG_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.68 MMC_CTLCFG_PRESET_VALUE3 Register

1 MMC_CTLCFG_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30099. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0066h**

Figure 14-9973. MMC_CTLCFG_PRESET_VALUE3 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	4h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
4h							

Table 14-30101. MMC_CTLCFG_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.69 MMC_CTLCFG_PRESET_VALUE4 Register

1 MMC_CTLCFG_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30102. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0068h**

Figure 14-9974. MMC_CTLCFG_PRESET_VALUE4 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30104. MMC_CTLCFG_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.70 MMC_CTLCFG_PRESET_VALUE5 Register

1 MMC_CTLCFG_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30105. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 006Ah**

Figure 14-9975. MMC_CTLCFG_PRESET_VALUE5 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
1h							

Table 14-30107. MMC_CTLCFG_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	1h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.71 MMC_CTLCFG_PRESET_VALUE6 Register

1 MMC_CTLCFG_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30108. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 006Ch**

Figure 14-9976. MMC_CTLCFG_PRESET_VALUE6 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R							
0h							

Table 14-30110. MMC_CTLCFG_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.72 MMC_CTLCFG_PRESET_VALUE7 Register

1 MMC_CTLCFG_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30111. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 006Eh**

Figure 14-9977. MMC_CTLCFG_PRESET_VALUE7 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30113. MMC_CTLCFG_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description

15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.
				Reset Source: vbus_amod_g_rst_n
				`0 Driver Type B is Selected`
				`1 Driver Type A is Selected`
				`2 Driver Type C is Selected`
				`3 Driver Type D is Selected`

13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.73 MMC_CTLCFG_PRESET_VALUE8 Register

1 MMC_CTLCFG_PRESET_VALUE8 Register (Offset = 72h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30114. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0072h**

Figure 14-9978. MMC_CTLCFG_PRESET_VALUE8 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
0h							

Table 14-30116. MMC_CTLCFG_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.74 MMC_CTLCFG_PRESET_VALUE10 Register

1 MMC_CTLCFG_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30117. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0074h**

Figure 14-9979. MMC_CTLCFG_PRESET_VALUE10 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
0h							

Table 14-30119. MMC_CTLCFG_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.75 MMC_CTLCFG_ADMA3_DESC_ADDRESS Register

1 MMC_CTLCFG_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = 0h]

The start address of Integrated DMA Descriptor is set to this register.

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Table 14-30120. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0078h**

Figure 14-9980. MMC_CTLCFG_ADMA3_DESC_ADDRESS Name Register

63	62	61	60	59	58	57	48
INTG_DESC_ADDR							
R/W							
0h							
55	54	53	52	51	50	49	48
INTG_DESC_ADDR							
R/W							
0h							
47	46	45	44	43	42	41	40
INTG_DESC_ADDR							
R/W							
0h							
39	38	37	36	35	34	33	32
INTG_DESC_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
INTG_DESC_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
INTG_DESC_ADDR							
R/W							
0h							

Table 14-30122. MMC_CTLCFG_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTG_DESC_ADDR	R/W	0h	The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. The 32-bit addressing Host Driver uses lower 32- bit of this register and shall program Descriptor Table on 32-bit boundary.ADMA3 ignores lower 2-bit of this register and assumes it to be 00b. Writing to 07Bh starts ADMA3 data transfer. The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 000b. Writing to 07Fh starts ADMA3 data transfer. Register Value- 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.76 MMC_CTLCFG_UHS2_BLOCK_SIZE Register

1 MMC_CTLCFG_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-30123. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0080h**

Figure 14-9981. MMC_CTLCFG_UHS2_BLOCK_SIZE Name Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_BOUNDARY			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_SIZE							
R/W							
0h							

Table 14-30125. MMC_CTLCFG_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_BOUNDARY	R/W	0h	When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of sys-tem memory management is set to this field. Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the ADMA System Address register. SDMA waits until the ADMA System Address register is written. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the UHS-II Transfer Mode register is set to 1. ADMA does not use this field. Reset Source: vbus_amod_g_rst_n 0 4K Bytes 1 8K Bytes 2 16K Bytes 3 32K Bytes 4 64K Bytes 5 128K Bytes 6 256K Bytes 7 512K Bytes
11:0	XFER_BLK_SIZE	R/W	0h	This register specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes. Vari-able block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This register is effective when Data Present is set to 1 in UHS-II Command register. Reset Source: vbus_amod_g_rst_n 0 No data transfer 1 1 Byte 2 2 Bytes 512 512 Bytes 2048 2048 Bytes

14.9.4.6.2.77 MMC_CTLCFG_UHS2_BLOCK_COUNT Register

1 MMC_CTLCFG_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-30126. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0084h**

Figure 14-9982. MMC_CTLCFG_UHS2_BLOCK_COUNT Name Register

31	30	29	28	27	26	25	24
XFER_BLK_COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
XFER_BLK_COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
XFER_BLK_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
XFER_BLK_COUNT							
R/W							
0h							

Table 14-30128. MMC_CTLCFG_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XFER_BLK_COUNT	R/W	0h	This register is effective when Data Present is set to 1 in UHS-II Command register and is enabled when Block Count Enable is set to 1 and Block / Byte Mode is set to 0 in the UHS-II Transfer Mode register. Data transfer stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred. This register should be accessed only when no transaction is executing [i.e.,after transactions are stopped]. During data transfer, read operations on this register may return an invalid value and write operations are ignored. 00000000h - Stop Count 00000001h - 1 block 00000002h - 2 blocks .... FFFFFFFFh - 4G blocks -1. Reset Source: vbus_amod_g_rst_n 0 Stop Count 1 1 block 2 2 blocks 3 3 blocks 4294967295 4G blocks -1

14.9.4.6.2.78 MMC_CTLCFG_UHS2_COMMAND_PKT_j Register

1 MMC_CTLCFG_UHS2_COMMAND_PKT_j Register (Offset = 88h + formula) [reset = 0h]

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes. The command length varies depends on a Command Packet type. The length is specified by the UHS-II Command register.

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Offset = 88h + (j * 1h); where j = 0 to 19d

Table 14-30129. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0088h + formula**

Figure 14-9983. MMC_CTLCFG_UHS2_COMMAND_PKT_j Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W							
0h							

Table 14-30131. MMC_CTLCFG_UHS2_COMMAND_PKT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CMD_PKT_BYTE	R/W	0h	UHS-II Command Packet image is set to this register.The command length varies depends on a Command Packet type. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.79 MMC_CTLCFG_UHS2_XFER_MODE Register

1 MMC_CTLCFG_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-30132. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 009Ch**

Figure 14-9984. MMC_CTLCFG_UHS2_XFER_MODE Name Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W	R/W	NONE					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-30134. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Use of 2 lane half duplex mode is determined by Host Driver. Reset Source: vbus_amod_g_rst_n 0 Full Duplex Mode 1 Half Duplex Mode
14	EBSY_WAIT	R/W	0h	This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer.If this bit is set to 1, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, Transfer Com-plete in the Normal Interrupt Status reg-ister is set to 1 to indicate end ofbusy. If an error is indicated in EBSY packet [ex. Memory Error], EBSY Error in the UHS-II Error Interrupt Status register is set to 1. Setting of EBSY Error also sets Error Interrupt to 1 in the Normal Inter-rupt Status register. Error Interrupt and Transfer Complete shall be set together. '1' Wait EBSY, '0' Issue a command without busy. Reset Source: vbus_amod_g_rst_n
13:9	RESERVED	NONE	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0 and waits Command Complete Interrupt and then check the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Com-mand Complete Signal Enable. Reset Source: vbus_amod_g_rst_n 0 Enable Response Interrupt 1 Disable Response Interrupt

Table 14-30134. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver.Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0 and Response Inter-rupt Disable is set to 0. If Host Control-ler checks response error, sets this bit to 1 and sets Response Interrupt Dis-able to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Disable Response Error Check` 1 `Enable Response Error Check`
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE Reset Source: vbus_amod_g_rst_n 0 `Memory` 1 `SDIO`
5	BYTE_MODE	R/W	0h	This bit specifies whether data transfer is in byte mode or block mode when Data Present is set to 1. This bit is effective to a command with data trans-fer. Reset Source: vbus_amod_g_rst_n 0 `Block Mode` 1 `Byte Mode`
4	DATA_XFER_DIR	R/W	0h	This bit specifies direction of data trans-fer when Data Present is set to 1. This bit is effective to a command with data transfer. 0 - Read [Card to Host] 1 - Write [Host to Card] Reset Source: vbus_amod_g_rst_n 0 `Read from Card to Host` 1 `Write from Host to Card`
3:2	RESERVED	NONE	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	This bit specifies whether data transfer usesUHS-II Block Count register. If this bit is set to 1, data transfer is terminated by Block Count. Setting to UHS-II Block Count register shall be equivalent to TLEN in UHS-II Command Packet reg-ister. Reset Source: vbus_amod_g_rst_n 0 `Disable Block count` 1 `Enable Block count`

Table 14-30134. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMA_ENA	R/W	0h	This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by DMA Select in the Host Control 1 register. Reset Source: vbus_amod_g_rst_n 0 `DMA mode is Disabled` 1 `DMA mode is Enabled`

14.9.4.6.2.80 MMC_CTLCFG_UHS2_COMMAND Register

1 MMC_CTLCFG_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-30135. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 009Eh**

Figure 14-9985. MMC_CTLCFG_UHS2_COMMAND Name Register

15	14	13	12	11	10	9	8
RESERVED			PKT_LENGTH				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED	
R/W		R/W	NONE		R/W	NONE	
0h		0h	0h		0h	0h	

Table 14-30137. MMC_CTLCFG_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12:8	PKT_LENGTH	R/W	0h	A command packet length, which is set in the UHS-II Command Packet register, is set to this register. 00011b - 00000b - 3-0 Bytes [Not used] 00100b - 4 Bytes .... 10100b - 20 Bytes 11111b 10101b Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	This field is used to distinguish a spe-cific command like abort command. If this field is set to 00b, the UHS-II RES Packet is stored in UHS-II Response register [0B3h-0A0h]. To avoid overwrit-ing the UHS-II Response register, when this filed is set to 01b, the RES Packet [4 bytes length] of TRANS_ABORT CCMD is stored in the Response regis-ter [013h-010h] and when this filed is set to 10b, the RES Packet [8 bytes length] of memory or SDIO abort com-mand [CMD12 or SDIO Abort com-mand] is stored in the Response register [01Fh-018h]. When this filed is set to 11b, Host Controller controls lane to go into dormant state. '00' Normal Command '01' TRANS_ABORT CCMD '10' CMD12 or SDIO Abort Command '11' Go Dormant Command Reset Source: vbus_amod_g_rst_n 0 Normal command 1 TRANS_ABORT CCMD 2 Abort command 3 Go dormant command

Table 14-30137. MMC_CTLCFG_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	This bit specifies whether the command is accompanied by data packet. Reset Source: vbus_amod_g_rst_n 0 `Data not Present` 1 `Data present`
4:3	RESERVED	NONE	0h	Reserved
2	SUB_COMMAND	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17].When issuing a main command, this bit is set to 0 and when issuing a sub com-mand, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register. Reset Source: vbus_amod_g_rst_n 0 `Main Command` 1 `Sub Command`
1:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.81 MMC_CTLCFG_UHS2_RESPONSE_j Register

1 MMC_CTLCFG_UHS2_RESPONSE_j Register (Offset = A0h + formula) [reset = 0h]

This register is used to store received UHS-II RES Packet image

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Offset = A0h + (j * 1h); where j = 0 to 19d

Table 14-30138. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00A0h + formula**

Figure 14-9986. MMC_CTLCFG_UHS2_RESPONSE_j Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R							
0h							

Table 14-30140. MMC_CTLCFG_UHS2_RESPONSE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESP_PKT_BYTE	R	0h	Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.82 MMC_CTLCFG_UHS2_MESSAGE_SELECT Register

1 MMC_CTLCFG_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30141. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00B4h**

Figure 14-9987. MMC_CTLCFG_UHS2_MESSAGE_SELECT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						MSG_SEL	
NONE						R/W	
0h						0h	

Table 14-30143. MMC_CTLCFG_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	NONE	0h	Reserved
1:0	MSG_SEL	R/W	0h	Host Controller holds 4 MSG packets in FIFO buffer.One of 4 MSGs can be read from the UHS-II MSG register [0BB-0B8h] by setting this register.[Assumed for debug usage.] '00' The latest MSG '01' One MSG before '10' Two MSGs before '11' Three MSGs before Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.83 MMC_CTLCFG_UHS2_MESSAGE Register

1 MMC_CTLCFG_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30144. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00B8h**

Figure 14-9988. MMC_CTLCFG_UHS2_MESSAGE Name Register

31	30	29	28	27	26	25	24
MSG_BYTE3							
R							
0h							
23	22	21	20	19	18	17	16
MSG_BYTE2							
R							
0h							
15	14	13	12	11	10	9	8
MSG_BYTE1							
R							
0h							
7	6	5	4	3	2	1	0
MSG_BYTE0							
R							
0h							

Table 14-30146. MMC_CTLCFG_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSG_BYTE3	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
23:16	MSG_BYTE2	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
15:8	MSG_BYTE1	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n

Table 14-30146. MMC_CTLCFG_UHS2_MESSAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	MSG_BYTE0	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.84 MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register

1 MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

This register shows receipt of INT MSG from which device

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Table 14-30147. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00BCh**

Figure 14-9989. MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Name Register

15	14	13	12	11	10	9	8
DEV_INT_STS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
DEV_INT_STS							
R/W1TC							
0h							

Table 14-30149. MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DEV_INT_STS	R/W1TC	0h	This register shows receipt of INT MSG from which device and is effective when INT MSG Enable is set to 1 in the UHS- II Device Select register. On receiving INT MSG from a device, Host Controller saves the INT MSG to UHS-II Device Interrupt Code register. A bit of this register, which is corre- spondent to Device ID, is set to 1 and generate Card Interrupt in Normal Interrupt Status register. Writing a bit to 1 clears the status bit [interrupt is treated] and Writing a bit to 0 keeps the status value [interrupt is untreated]. If INT MSG Enable is set to 0, this register is cleared to 0 and Host Controller ignores receipt of INT MSG. Effective bit range of this register is determined by Number of Devices Supported in the UHS-II General Capabilities regis-ter. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0. D00 - Not used [Reserved] D01 - Setting 1 means INT MSG is received from Device ID 1 D02 - Setting 1 means INT MSG is received from Device ID 2 .... D15 - Setting 1 means INT MSG is received from Device ID 15 Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.85 MMC_CTLCFG_UHS2_DEVICE_SELECT Register

1 MMC_CTLCFG_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

UHS-II Device Select Register

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Table 14-30150. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00BEh**

Figure 14-9990. MMC_CTLCFG_UHS2_DEVICE_SELECT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-30152. MMC_CTLCFG_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	This bit enables receipt of INT MSG. If this bit is set to 1,receipt of INT MSG is informed by Card Interrupt in the Nor-mal Interrupt Status register. If this bit is set to 0, Host Con-troller ignores receipt of INT MSG and may not set the UHS-II Device Interrupt Code register. Support of INT MSG Interrupt is optional. If trying to set this bit to 1 but still this bit is read 0, INT MSG Interrupt is not sup-ported by the Host Controller. In this case, UHS-II Device Interrupt Status register always shall be read 0 and UHS-II Device Interrupt Code register may not be implemented. '0' Disabled '1' Enabled Reset Source: vbus_amod_g_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	DEV_SEL	R/W	0h	Host Controller holds an INT MSG packet per device. One of INT MSGs [up to 15] can be selected by this field and read from the UHS-II Device Interrupt Code Register [0BFh]. This field is effective when INT MSG Enable is set to 1. The number of devices implemented in the Host Controller is indicated by Number of Devices supported in the UHS-II General Capabilities register. 0h Unselected [Default] 1h INT MSG of Device ID 1 is selected 2h INT MSG of Device ID 2 is selected .... Fh INT MSG of Device ID 15 is selected Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.86 MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register

1 MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register.

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Table 14-30153. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00BFh**

Figure 14-9991. MMC_CTLCFG_UHS2_DEVICE_INT_CODE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
DEV_INTR							
R							
0h							

Table 14-30155. MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_INTR	R	0h	This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register. Host Controller holds an INT MSG packet per device. One of INT MSGs [Code length is 1 byte] up to 15 can be read from this register by select-ing UHS-II Device Select. The number of the registers to hold INT MSGs is determined by Number of Devices Sup-ported in the UHS-II General Capabili-ties register. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.87 MMC_CTLCFG_UHS2_SOFTWARE_RESET Register

1 MMC_CTLCFG_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

UHS-II Software Reset Register

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Table 14-30156. Instance Table

Instance Name	**Physical Address**
MMCSD0	**0FA1 00C0h**

Figure 14-9992. MMC_CTLCFG_UHS2_SOFTWARE_RESET Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
NONE						R/W	R/W
0h						0h	0h

Table 14-30158. MMC_CTLCFG_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	NONE	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	Host Driver set this bit to 1 to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completionof SD-TRAN reset. If CMD0 is issued, SD-TRAN Initial- ization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required. '0' Not Affected '1' Reset SD TRAN Host Controller requires to do followings: [1] SD Clock Enable is maintained.[Continue to provide RCLK]. [2] All setting register is maintained. [3] Internal sequencers are reset to just after power on.be able to issue a command. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. [5] Data transfer is terminated and data in buffer is dis-carded. Reset Source: vbus_amod_g_rst_n 0 Not Affected 1 Reset SDTRAN
0	HOST_FULL_RESET	R/W	0h	On issuing FULL_RESET CCMD, Host Driver set this bit to 1 to reset Host Controller. This bit is cleared auto-matically at completion of Host Controller reset. Initial- ization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained. Host Controller requires to do followings: [1] SD Clock Enable is cleared. [Internal Clock is still synchronized]. [2] All setting register is cleared. [3] Internal sequencers are reset to just after power on. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. Reset Source: vbus_amod_g_rst_n 0 Not Affected 1 Reset Host Conroller

14.9.4.6.2.88 MMC_CTLCFG_UHS2_TIMER_CONTROL Register

1 MMC_CTLCFG_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

UHS-II Timeout Control Register

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Table 14-30159. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00C2h**

Figure 14-9993. MMC_CTLCFG_UHS2_TIMER_CONTROL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W				R/W			
0h				0h			

Table 14-30161. MMC_CTLCFG_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:4	DEADLOCK_TIMEOUT_CTR	R/W	0h	This value determines the deadlock period while host expecting to receive a packet [1 second]. Tim-eout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n
3:0	CMDRESP_TIMEOUT_CTR	R/W	0h	This value determines the interval between com-mand packet and response packet [5ms]. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.89 MMC_CTLCFG_UHS2_ERR_INTR_STS Register

1 MMC_CTLCFG_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

This register gives the status of all UHS-II interrupts

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Table 14-30162. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00C4h**

Figure 14-9994. MMC_CTLCFG_UHS2_ERR_INTR_STS Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC_ERR					RESERVED		
R/W1TC					NONE		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W1TC	R/W1TC
0h						0h	0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W1TC	NONE						R/W1TC
0h	0h						0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1TC	NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30164. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC_ERR	R/W1TC	0h	Vendor may use this field for vendor specific error status. '0' Interrupt is not generated '1' Vendor Specific Error Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1TC	0h	Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout [1 second]. Timeout value is determined by the setting of Timeout Counter Value for Deadlock in UHS-II Timer Control register. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Deadlock Error
16	CMD_RESP_TIMEOUT	R/W1TC	0h	Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout [5ms]. Timeout value is determined by the setting of Timeout Counter Value for CMD_RES in UHS-II Timer Control register. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Resp packet timeout Error

Table 14-30164. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W1TC	0h	Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the ADMA Error Status [054h], which is defined in the Host spec 3.00. Reset Source: vbus_amod_g_rst_n 0 No Error 1 ADMA2/3 Error
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W1TC	0h	On receiving EBSY packet, if the packet indicates an error, this bit is set to 1. Setting of this bit also sets Error Interrupt and Transfer Completer together in the Normal Interrupt Status register. This error check is effective for a command with setting EBSY Wait in the UHS-II Transfer Mode register. Reset Source: vbus_amod_g_rst_n 0 No Error 1 EBSY Error
7	UNRECOVERABLE	R/W1TC	0h	Setting of this bit means that Unrecoverable Error is set in a packet from a device. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Device Unrecoverable Error
6	RESERVED	NONE	0h	Reserved
5	TID	R/W1TC	0h	Setting of this bit means that TID Error occurs. Reset Source: vbus_amod_g_rst_n 0 No Error 1 TID Error
4	FRAMING	R/W1TC	0h	Setting of this bit means that Framing Error occurs during a packet receiving. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Framing Error
3	CRC	R/W1TC	0h	Setting of this bit means that CRC Error occurs during a packet receiving. Reset Source: vbus_amod_g_rst_n 0 No Error 1 CRC Error
2	RETRY_EXPIRED	R/W1TC	0h	Setting of this bit means that Retry Counter Expired Error occurs during data transfer.If this bit is set,either Framing Error or CRC Error in this register shall be set. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Retry Expired Error
1	RESP_PKT	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to1 in the UHS- II Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response,this bit is set to 1. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Resp packet Error

Table 14-30164. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HEADER	R/W1TC	0h	Setting of this bit means that Header Error occurs in a received packet. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Header Error

14.9.4.6.2.90 MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register

1 MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

This register is used to enable the UHS-II Error Interrupt Status register fields

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Table 14-30165. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00C8h**

Figure 14-9995. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W					NONE		
0h					0h		

23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30167. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting this bit to 1 enables setting of Vendor Specific Error bit in the UHS-II Error Interrupt Status register. 0h - Status is Disabled 1h - Status is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for Dead lock bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for CMD_RES bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled

Table 14-30167. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables setting of ADMA2/3 Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W	0h	Setting this bit to 1 enables setting of EBSY Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables setting of Unrecoverable Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables setting of TID Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
4	FRAMING	R/W	0h	Setting this bit to 1 enables setting of Framing Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
3	CRC	R/W	0h	Setting this bit to 1 enables setting of CRC Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
2	RETRY_EXPIRED	R/W	0h	Setting this bit to 1 enables setting of Retry Expired bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables setting of RES Packet Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`
0	HEADER	R/W	0h	Setting this bit to 1 enables setting of Header Error bit in the UHS-II Error Interrupt Status Register. Reset Source: vbus_amod_g_rst_n 0 `Status is Disabled` 1 `Status is Enabled`

14.9.4.6.2.91 MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register

1 MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

This register is used to generate UHS-II Interrupt signals

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Table 14-30168. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00CCh**

Figure 14-9996. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">VENDOR_SPECFIC</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>DEADLOCK_TIMEOUT</td><td>CMD_RESP_TIMEOUT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>ADMA2_ADMA3</td><td colspan="6">RESERVED</td><td>EBSY</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>UNRECOVERABLE</td><td>RESERVED</td><td>TID</td><td>FRAMING</td><td>CRC</td><td>RETRY_EXPIRED_SIG_ENA</td><td>RESP_PKT</td><td>HEADER</td></tr>
<tr><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-30170. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting of a bit to 1 in this field enables generating interrupt signal when corre-spondent bit of Vendor Specific Error is set in the UHS-II Error Interrupt Status Register. 0h - Interrupt Signal is Disabled 1h - Interrupt Signal is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for Dead lock bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for CMD_RES bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled

Table 14-30170. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables generating interrupt signal when ADMA2/3 Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W	0h	Setting this bit to 1 enables generating interrupt signal when EBSY Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Unrecoverable Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables generating interrupt signal when TID Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
4	FRAMING	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Framing Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
3	CRC	R/W	0h	Setting this bit to 1 enables generating interrupt signal when CRC Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Retry Expired bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when RES Packet Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`
0	HEADER	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Header Error bit is set in the UHS-II Error Interrupt Status Register. Reset Source: vbus_amod_g_rst_n 0 `Interrupt Signal is Disabled` 1 `Interrupt Signal is Enabled`

14.9.4.6.2.92 MMC_CTLCFG_UHS2_SETTINGS_PTR Register

1 MMC_CTLCFG_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

This register is pointer for UHS-II settings.

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Table 14-30171. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00E0h**

Figure 14-9997. MMC_CTLCFG_UHS2_SETTINGS_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_SETTINGS_PTR							
R							
100h							
7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR							
R							
100h							

Table 14-30173. MMC_CTLCFG_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.93 MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register

1 MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

This register is pointer for UHS-II Capabilities Register.

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Table 14-30174. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00E2h**

Figure 14-9998. MMC_CTLCFG_UHS2_CAPABILITIES_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_CAPABILITIES_PTR							
R							
110h							
7	6	5	4	3	2	1	0
UHS2_CAPABILITIES_PTR							
R							
110h							

Table 14-30176. MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.94 MMC_CTLCFG_UHS2_TEST_PTR Register

1 MMC_CTLCFG_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

This register is pointer for UHS-II Test Register.

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Table 14-30177. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00E4h**

Figure 14-9999. MMC_CTLCFG_UHS2_TEST_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_TEST_PTR							
R							
120h							
7	6	5	4	3	2	1	0
UHS2_TEST_PTR							
R							
120h							

Table 14-30179. MMC_CTLCFG_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.95 MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register

1 MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

This register is pointer for UHS-II Shared Bus Control Register.

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Table 14-30180. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00E6h**

Figure 14-10000. MMC_CTLCFG_SHARED_BUS_CTRL_PTR Name Register

15	14	13	12	11	10	9	8
SHARED_BUS_CTRL_PTR							
R							
130h							
7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR							
R							
130h							

Table 14-30182. MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.96 MMC_CTLCFG_VENDOR_SPECFIC_PTR Register

1 MMC_CTLCFG_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

This register is pointer for UHS-II Vendor Specific Pointer Register.

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Table 14-30183. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00E8h**

Figure 14-10001. MMC_CTLCFG_VENDOR_SPECFIC_PTR Name Register

15	14	13	12	11	10	9	8
VENDOR_SPECFIC_PTR							
R							
140h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VENDOR_SPECFIC_PTR							
R							
140h							

Table 14-30185. MMC_CTLCFG_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.97 MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register

1 MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

This is used to program the boot timeout value counter

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Table 14-30186. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00F4h**

Figure 14-10002. MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Name Register

31	30	29	28	27	26	25	24
DATA_TIMEOUT_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_TIMEOUT_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_TIMEOUT_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT							
R/W							
0h							

Table 14-30188. MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_TIMEOUT_CNT	R/W	0h	This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.The value is in number of sd clock. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.98 MMC_CTLCFG_VENDOR_REGISTER Register

1 MMC_CTLCFG_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

Vendor register added for autogate sdclk, cmd11 power down timer, enhancedstrobe and eMMC hardware reset

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Table 14-30189. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00F8h**

Figure 14-10003. MMC_CTLCFG_VENDOR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							AUTOGATE_SDCLK
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
CMD11_PD_TIMER							
R/W							
1388h							
7	6	5	4	3	2	1	0
CMD11_PD_TIMER						EMMC_HW_RESET	ENHANCED_STROBE
R/W						R/W	R/W
1388h						0h	0h

Table 14-30191. MMC_CTLCFG_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device Reset Source: vbus_amod_g_rst_n 0 `Autogating of sdclk is Disabled` 1 `Autogating of sdclk is Enabled`
15:2	CMD11_PD_TIMER	R/W	1388h	cmd11 power-down timer value Reset Source: vbus_amod_g_rst_n
1	EMMC_HW_RESET	R/W	0h	Hardware reset signal is generared for eMMC card when this bit is set Reset Source: vbus_amod_g_rst_n 0 `Deassert the hardware reset pin` 1 `Drives the hardware reset pin as ZERO (Active LOW to eMMC card)`
0	ENHANCED_STROBE	R/W	0h	This bit enables the enhanced strobe logic of the Host Controller Reset Source: vbus_amod_g_rst_n 0 `Enhanced strobe is Disabled` 1 `Enhanced strobe is Enabled`

14.9.4.6.2.99 MMC_CTLCFG_SLOT_INT_STS Register

1 MMC_CTLCFG_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

This register is used to read the interrupt signal for each slot.

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Table 14-30192. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00FCh**

Figure 14-10004. MMC_CTLCFG_SLOT_INT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTR_SIG							
R							
0h							

Table 14-30194. MMC_CTLCFG_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:0	INTR_SIG	R	0h	These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.100 MMC_CTLCFG_HOST_CONTROLLER_VER Register

1 MMC_CTLCFG_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

This register is used to read the vendor version number and specification version number

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Table 14-30195. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 00FEh**

Figure 14-10005. MMC_CTLCFG_HOST_CONTROLLER_VER Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VEN_VER_NUM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SPEC_VER_NUM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-30197. MMC_CTLCFG_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	VEN_VER_NUM	R	10h	The Vendor Version Number is set to 0x10 [1.0] Reset Source: vbus_amod_g_rst_n
7:0	SPEC_VER_NUM	R	4h	This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. 00h - SD Host Controller Specification Version 1.00 01h - SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 02h - SD Host Controller Specification Version 3.00 03h - SD Host Controller Specification Version 4.00 04h - SD Host Controller Specification Version 4.10 'others' Reserved Reset Source: vbus_amod_g_rst_n 0 `SD Host Controller Specification Version 1.00` 1 `SD Host Controller Specification Version 2.00` 2 `SD Host Controller Specification Version 3.00` 3 `SD Host Controller Specification Version 4.00` 4 `SD Host Controller Specification Version 4.10`

14.9.4.6.2.101 MMC_CTLCFG_UHS2_GEN_SETTINGS Register

1 MMC_CTLCFG_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

Start Address of General settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30198. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0100h**

Figure 14-10006. MMC_CTLCFG_UHS2_GEN_SETTINGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		NUMLANES					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							POWER_MODE
NONE							R/W
0h							0h

Table 14-30200. MMC_CTLCFG_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	NUMLANES	R/W	0h	The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0000b - 2 Lanes FD or 2L-HD 0001b - Not Used 0010b - 3 Lanes 2D1U-FD [Embedded] 0011b - 3 Lanes 1D2U-FD [Embedded] 0100b - 4 Lanes 2D2U-FD [Embedded] others - Reserved Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

0	POWER_MODE	R/W	0h	This field determines either Fast mode or Low Power mode.Host and all devices connected to the host shall be set to the same mode.
				Reset Source: vbus_amod_g_rst_n
				`0 Fast mode`
				`1 Low power mode`

14.9.4.6.2.102 MMC_CTLCFG_UHS2_PHY_SETTINGS Register

1 MMC_CTLCFG_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

Start Address of PHY settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30201. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0104h**

Figure 14-10007. MMC_CTLCFG_UHS2_PHY_SETTINGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
N_LSS_DIR				N_LSS_SYN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HIBERNATE_ENA	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_RANGE		RESERVED					
R/W		NONE					
0h		0h					

Table 14-30203. MMC_CTLCFG_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R/W	0h	The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h - 8 x16 LSS 1h - 8 x 1 LSS 2h - 8 x 2 LSS 3h - 8 x 3 LSS .... Fh - 8 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R/W	0h	The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n

Table 14-30203. MMC_CTLCFG_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	HIBERNATE_ENA	R/W	0h	After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off. Reset Source: vbus_amod_g_rst_n 0 Hibernate Disabled 1 Hibernate Enabled
14:8	RESERVED	NONE	0h	Reserved
7:6	SPEED_RANGE	R/W	0h	PLL multiplier is selected by this field.Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State. '00' Range A [Default] '01' Range B '10' Reserved '11' Reserved Reset Source: vbus_amod_g_rst_n 0 Range A (Default) 1 Range B 2 Reserved 3 Reserved
5:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.103 MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register

1 MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30204. Instance Table

Instance Name	**Physical Address**
MMCSD0	**0FA1 0108h**

Figure 14-10008. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W							
0h							
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30206. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved

Table 14-30206. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	N_DATA_GAP	R/W	0h	The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS Reset Source: vbus_amod_g_rst_n 0 No Gap 1 1 LSS 2 2 LSS 3 3 LSS 255 255 LSS
31:18	RESERVED	NONE	0h	Reserved
17:16	RETRY_COUNT	R/W	0h	Data Burst retry count is set to this field. '00' Retry Disabled '01' 1 time '10' 2 times '11' 3 times Reset Source: vbus_amod_g_rst_n 0 Retry Disabled 1 Retry 1time 2 Retry 2times 3 Retry 3times
15:8	HOST_NFCU	R/W	0h	Host Driver sets the number of blocks in Data Burst [Flow Control] to this field.The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Blocks 03h - 3 Blocks .... FFh - 255 Blocks Reset Source: vbus_amod_g_rst_n 0 256 Blocks 1 1 Block 2 2 Blocks 3 3 Blocks 255 255 Blocks
7:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.104 MMC_CTLCFG_UHS2_GEN_CAP Register

1 MMC_CTLCFG_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

Start Address of General Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-30207. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0110h**

Figure 14-10009. MMC_CTLCFG_UHS2_GEN_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CORECFG_UHS2_BUS_TOPLOGY		CORECFG_UHS2_MAX_DEVICES				DEVICE_TYPE	
R		R				R	
0h		1h				0h	
15	14	13	12	11	10	9	8
RESERVED	CFG_64BIT_ADDRESSING	NUM_LANES					
NONE	R	R					
0h	1h	Fh					
7	6	5	4	3	2	1	0
GAP				DAP			
R				R			
1h				1h			

Table 14-30209. MMC_CTLCFG_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:22	CORECFG_UHS2_BUS_TOPLOGY	R	0h	This field indicates one of bus topologies configured by a Host system. '00' P2P Connection '01' Ring Connection '10' HUB Connection '11' HUB is connected in Ring Reset Source: vbus_amod_g_rst_n 0 P2P Connection 1 Ring Connection 2 HUB Connection 3 HUB is connected in Ring

Table 14-30209. MMC_CTLCFG_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

21:18	CORECFG_UHS2_MAX_DEVICES	R	1h	This field indicates the maximum number of devices supported by the Host Controller.
				0h - Not used
				1h - 1 Devices
				2h - 2 Devices
				.....
				....
				Fh - 15 Devices
				Reset Source: vbus_amod_g_rst_n
				`0 Not used`
				`1 1 Device`
				`2 2 Devices`
				`15 15 Devices`

17:16	DEVICE_TYPE	R	0h	This field indicates device type configured by a Host system. '00' Removable Card[P2P] '01' Embedded Devices '10' Embedded Devices+Removable Card '11' Reserved Reset Source: vbus_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	This field indicates support of 64-bit addressing by the Host Controller. '0' 32-bit Addressing is supported '1' 32-bit and 64-bit Addressing is supported Reset Source: vbus_amod_g_rst_n
13:8	NUM_LANES	R	Fh	This field indicates support of lanes by the Host Controller.0 mean not supported and 1 means supported. D08 - 2L-HD D09 - 2D1U-FD D10 - 1D2U-FD D11 - 2D2U-FD D12 - Reserved D13 - Reserved Reset Source: vbus_amod_g_rst_n
7:4	GAP	R	1h	This field indicates the maximum capability of host power supply for a group configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -Not used 1h - 360 mW 2h - 720 mW .... Fh - 360x15 mW Reset Source: vbus_amod_g_rst_n
3:0	DAP	R	1h	This field indicates the maximum capability of host power supply for a device configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -360 mW [Default] 1h - 360 mW 2h - 720 mW .... Fh - 360 x15 mW Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.105 MMC_CTLCFG_UHS2_PHY_CAP Register

1 MMC_CTLCFG_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

Start Address of PHY Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-30210. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0114h**

Figure 14-10010. MMC_CTLCFG_UHS2_PHY_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R				R			
1h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R		NONE					
0h		0h					

Table 14-30212. MMC_CTLCFG_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R	1h	This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R	1h	This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
15:8	RESERVED	NONE	0h	Reserved

Table 14-30212. MMC_CTLCFG_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SPEED_RANGE	R	0h	This field indicates supported Speed Range by the Host Controller '00' Range A [Default] '01' Range A and Range B '10' Reserved '11' Reserved Reset Source: vbus_amod_g_rst_n 0 `Range A (Default)` 1 `Range A and Range B` 2 `Reserved` 3 `Reserved`
5:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.106 MMC_CTLCFG_UHS2_LNK_TRN_CAP Register

1 MMC_CTLCFG_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Capabilities Register.

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Table 14-30213. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0118h**

Figure 14-10011. MMC_CTLCFG_UHS2_LNK_TRN_CAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R							
81h							
15	14	13	12	11	10	9	8
N_FCU							
R							
1h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30215. MMC_CTLCFG_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved

Table 14-30215. MMC_CTLCFG_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	N_DATA_GAP	R	81h	This field indicates the minimum number of data gap[DIDL] supported by the Host Controller. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS Reset Source: vbus_amod_g_rst_n 0 No Gap 1 1 LSS 2 2 LSS 3 3 LSS 255 255 LSS
31:20	MAX_BLK_LENGTH	R	200h	This field indicates maximum block length by the Host Controller. 000h - Not Used 001h - 1 byte 002h - 2 bytes .... 200h - 512 bytes .... 800h - 2048 bytes 801h-FFFh -Not Used Reset Source: vbus_amod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved
15:8	N_FCU	R	1h	This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller.This value is determined by supported buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Block 03h - 3 Block .... FFh - 255 Blocks Reset Source: vbus_amod_g_rst_n 0 256 Blocks 1 1 Block 2 2 Blocks 3 3 Blocks 255 255 Blocks
7:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.107 MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register

1 MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

This register is not physically implemented, rather it is an address where UHS-II Error Interrupt Status register can be written.

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Table 14-30216. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0120h**

Figure 14-10012. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
W					NONE		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
NONE						W	W
0h						0h	0h
15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W	NONE						W
0h	0h						0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30218. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h - Not Affected 1h - Vendor Specific Error Status is set Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved

17	TIMEOUT_DEADLOCK	W	0h	Setting this bit forces the Host Controller to set Timeout for Deadlock in the UHS-II Error Interrupt Status register.
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Timeout for Deadlock Error status is set`

16	TIMEOUT_CMD_RES	W	0h	Setting this bit forces the Host Controller to set Timeout for CMD_RES in the UHS-II Error Interrupt Status register.
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Timout for CMD_RES Status is set`

Table 14-30218. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA	W	0h	Setting this bit forces the Host Controller to set ADMA Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 ADMA error status is set
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	W	0h	Setting this bit forces the Host Controller to set EBSY Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 EBSY error status is set
7	UNRECOVERABLE	W	0h	Setting this bit forces the Host Controller to set Unrecover-able Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Unrecoverable error status is set
6	RESERVED	NONE	0h	Reserved
5	TID	W	0h	Setting this bit forces the Host Controller to set TID Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 TID error status is set
4	FRAMING	W	0h	Setting this bit forces the Host Controller to set Framing Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Framing error status is set
3	CRC	W	0h	Setting this bit forces the Host Controller to set CRC Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 CRC error status is set
2	RETRY_EXPIRED	W	0h	Setting this bit forces the Host Controller to set Retry Expired in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Retry expired error status is set
1	RES_PKT	W	0h	Setting this bit forces the Host Controller to set RES Packet Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 RES packet error status is set
0	HEADER	W	0h	Setting this bit forces the Host Controller to set Header Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Header error status is set

14.9.4.6.2.108 MMC_CTLCFG_CQ_VERSION Register

1 MMC_CTLCFG_CQ_VERSION Register (Offset = 200h) [reset = 510h]

This register provides information about the version of the eMMC CQ standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1 The following table describes the CQBASE+00h: CQVReservedER Command Queueing Version.

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Table 14-30219. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0200h**

Figure 14-10013. MMC_CTLCFG_CQ_VERSION Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EMMC_MAJOR_VER_NUM			
NONE				R			
0h				5h			
7	6	5	4	3	2	1	0
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R				R			
1h				0h			

Table 14-30221. MMC_CTLCFG_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number [digit left of decimal point],in BCD format Reset Source: vbus_amod_g_rst_n
7:4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number [digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n
3:0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix [2nd digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.109 MMC_CTLCFG_CQ_CAPABILITIES Register

1 MMC_CTLCFG_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

This register is reserved for capability indication.

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Table 14-30222. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0204h**

Figure 14-10014. MMC_CTLCFG_CQ_CAPABILITIES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CF_MUL				RESERVED		CF_VAL	
R				NONE		R	
3h				0h		C8h	
7	6	5	4	3	2	1	0
CF_VAL							
R							
C8h							

Table 14-30224. MMC_CTLCFG_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CF_MUL	R	3h	Internal Timer Clock Frequency Multiplier [ITCFMUL] ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the SQS polling period. See ITCFVAL definition for details. Field Value Description: 0h = 0.001 MHz 1h = 0.01 MHz 2h = 0.1 MHz 3h = 1 MHz 4h = 10 MHz Other values are reserved Reset Source: vbus_amod_g_rst_n 3 1 MHz 4 10 MHz
11:10	RESERVED	NONE	0h	Reserved

Table 14-30224. MMC_CTLCFG_CQ_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	CF_VAL	R	C8h	Internal Timer Clock Frequency Value [ITCFVAL] TCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the polling period when using periodic SEND_QUEUE_ STATUS [CMD13] polling. The clock frequency is calculated as ITCFVAL*ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h [= 192 decimal] and ITCFMUL shall be 2h [0.1 MHz 192 * 0.1 MHz 19.2 MHz] Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.110 MMC_CTLCFG_CQ_CONFIG Register

1 MMC_CTLCFG_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

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Table 14-30225. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0208h**

Figure 14-10015. MMC_CTLCFG_CQ_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED							CQ_ENABLE
NONE							R/W
0h							0h

Table 14-30227. MMC_CTLCFG_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	DCMD_ENA	R/W	0h	Direct Command [DCMD] Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descrip-tor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor Reset Source: vbus_amod_g_rst_n 0 Task descriptor in slot #31 is a Data Transfer Task Descriptor 1 Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RESERVED	NONE	0h	Reserved

Table 14-30227. MMC_CTLCFG_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TASK_DESC_SIZE	R/W	0h	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queueing Enable bit is 0 [command queueing is disabled] Bit Value Description 1 = Task descriptor size is 128 bits 0 = Task descriptor size is 64 bits Reset Source: vbus_amod_g_rst_n 0 Task descriptor size is 64 bits 1 Task descriptor size is 128 bits
7:1	RESERVED	NONE	0h	Reserved
0	CQ_ENABLE	R/W	0h	Command Queueing Enable Software shall write 1 this bit when in order to enable command queueing mode [i.e. enable CQE]. When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queueing mode,it shall clear all previous tasks if such exist before setting this bit to 0. Reset Source: vbus_amod_g_rst_n 0 Command Queueing mode is Disabled 1 Command Queueing mode is Enabled

14.9.4.6.2.111 MMC_CTLCFG_CQ_CONTROL Register

1 MMC_CTLCFG_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

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Table 14-30228. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 020Ch**

Figure 14-10016. MMC_CTLCFG_CQ_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>CLEAR_ALL_TASKS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>HALT_BIT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30230. MMC_CTLCFG_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	Clear All Tasks Software shall write 1 this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state [i.e.Halt bit is 1]. When software writes 1, the value of the register is updated to 1, and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit.Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect. Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-30230. MMC_CTLCFG_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	Halt Host software shall write 1 to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command [CMDQ_TASK_MGMT] When software writes 1, CQE shall complete the ongo-ing task if such a task is in progress. Once the task is completed and CQE is in idle state,CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state [i.e. resume CQE activity], soft-ware shall clear this bit [write 0]. Writing 0 when thevalue is already 0 shall have no effect. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.112 MMC_CTLCFG_CQ_INTR_STS Register

1 MMC_CTLCFG_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in CQ ISTE register.

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Table 14-30231. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0210h**

Figure 14-10017. MMC_CTLCFG_CQ_INTR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-30233. MMC_CTLCFG_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

4	TASK_ERROR	R/W1TC	0h	Task Error Interrupt [TERR] This bit is asserted when task error is detected due to invalid task descriptor
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Task Error interrupt is generated`

3	TASK_CLEARED	R/W1TC	0h	Task Cleared [TCL] This status bit is asserted [if CQISTE.TCL=1] when a task clear operation is completed by CQE. The com-pleted task clear operation is either an individual task clear [CQTCLR] or clearing of all tasks [CQCTL].
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Task clear interrupt is generated`

Table 14-30233. MMC_CTLCFG_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W1TC	0h	Response Error Detected Interrupt [RED] This status bit is asserted [if CQISTE.RED=1] when a response is received with an error bit set in the device status field. The contents of the device status field are listed in Section 6.13.Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Reset Source: vbus_amod_g_rst_n
1	TASK_COMPLETE	R/W1TC	0h	Task Complete Interrupt [TCC] This status bit is asserted [if CQISTE.TCC=1] when atleast one of the following two conditions are met: [1] A task is completed and the INT bit is set in its Task Descriptor [2] Interrupt caused by Interrupt Coalescing logic [see Section C.4.9] Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Task complete interrupt is generated
0	HALT_COMPLETE	R/W1TC	0h	Halt Complete Interrupt [HAC] This status bit is asserted [if CQISTE.HAC=1] when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Halt complete interrupt is generated

14.9.4.6.2.113 MMC_CTLCFG_CQ_INTR_STS_ENA Register

1 MMC_CTLCFG_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

This register enables and disables the reporting of the corresponding interrupt to host soft-ware in 299 CQIS register. When a bit is set (1) and the corresponding interrupt c -ondition is active, then the 300 bit is CQIS is asserted. Interrupt sources that are disabled (0) are not indicated in the CQIS 301 register. This register is bit-index matched to CQIS register.

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Table 14-30234. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0214h**

Figure 14-10018. MMC_CTLCFG_CQ_INTR_STS_ENA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-30236. MMC_CTLCFG_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Status Enable 1 = CQIS.TERR will be set when its interrupt condition is active 0 = CQIS.TERR is disabled Reset Source: vbus_amod_g_rst_n 0 1
3	TASK_CLEARED	R/W	0h	Task Cleared Status Enable [TCL] 1 = CQIS.TCL will be set when its interrupt condition is active 0 = CQIS.TCL is disabled Reset Source: vbus_amod_g_rst_n 0 1

Table 14-30236. MMC_CTLCFG_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	Response Error Detected Status Enable [RED] 1 = CQIS.RED will be set when its interrupt condition is active 0 = CQIS.RED is disabled Reset Source: vbus_amod_g_rst_n 0 1
1	TASK_COMPLETE	R/W	0h	Task Complete Status Enable [TCC] 1 = CQIS.TCC will be set when its interrupt condition is active 0 = CQIS.TCC is disabled Reset Source: vbus_amod_g_rst_n 0 1
0	HALT_COMPLETE	R/W	0h	Halt Complete Status Enable [HAC] 1 = CQIS.HAC will be set when its interrupt condition is active 0 = CQIS.HAC is disabled Reset Source: vbus_amod_g_rst_n 0 1

14.9.4.6.2.114 MMC_CTLCFG_CQ_INTR_SIG_ENA Register

1 MMC_CTLCFG_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1) and the corresponding bit in CQIS is set, then an interrupt is gene -rated. Interrupt sources 305 that are disabled (0) are still indicated in the CQIS register. This register is bit-index matched 306 to CQIS register.

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Table 14-30237. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0218h**

Figure 14-10019. MMC_CTLCFG_CQ_INTR_SIG_ENA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>TASK_ERROR</td><td>TASK_CLEARED</td><td>RESP_ERR_DET</td><td>TASK_COMPLETE</td><td>HALT_COMPLETE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-30239. MMC_CTLCFG_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Signal Enable [TERR] When set and CQIS.TERR is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
3	TASK_CLEARED	R/W	0h	Task Cleared Signal Enable [TCL] When set and CQIS.TCL is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1

Table 14-30239. MMC_CTLCFG_CQ_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	Response Error Detected Signal Enable [TCC] When set and CQIS.RED is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
1	TASK_COMPLETE	R/W	0h	Task Complete Signal Enable [TCC] When set and CQIS.TCC is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
0	HALT_COMPLETE	R/W	0h	Halt Complete Signal Enable [HAC] When set and CQIS.HAC is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1

14.9.4.6.2.115 MMC_CTLCFG_CQ_INTR_COALESCING Register

1 MMC_CTLCFG_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

This register controls the interrupt coalescing feature.

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Table 14-30240. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 021Ch**

Figure 14-10020. MMC_CTLCFG_CQ_INTR_COALESCING Name Register

31	30	29	28	27	26	25	24
CQINTCOALESC_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			IC_STATUS	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
RESERVED			CTR_THRESHOLD				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED	TIMEOUT_VAL						
NONE	R/W						
0h	0h						

Table 14-30242. MMC_CTLCFG_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated. Reset Source: vbus_amod_g_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	IC_STATUS	R	0h	This bit indicates to software whether any tasks [with INT=0] have completed and counted towards interrupt coalescing [i.e., ICSB is set if and only if IC counter > 0]. Bit Value Description 1 = At least one task completion has been counted [IC counter >0] 0 = No task completions have occurred since last counter reset [IC counter =0] Reset Source: vbus_amod_g_rst_n
19:13	RESERVED	NONE	0h	Reserved

Table 14-30242. MMC_CTLCFG_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	CTR_THRESHOLD	R/W	0h	Interrupt Coalescing Counter Threshold [ICCTH]: Software uses this field to configure the number of task completions [only tasks with INT=0 in the Task Descriptor] which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 NOTE : When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated.In order to write to this field, the ICCTHWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TIMEOUT_VAL	R/W	0h	Interrupt Coalescing Timeout Value [ICTOVAL]: Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register.The minimum value is 01h [1024 clock periods] and the maximum value is 7Fh [127*1024 clock periods]. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us NOTE: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.116 MMC_CTLCFG_CQ_TDL_BASE_ADDR Register

1 MMC_CTLCFG_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

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Table 14-30243. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0220h**

Figure 14-10021. MMC_CTLCFG_CQ_TDL_BASE_ADDR Name Register

31	30	29	28	27	26	25	24
CQTDLBA_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CQTDLBA_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CQTDLBA_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CQTDLBA_LO							
R/W							
0h							

Table 14-30245. MMC_CTLCFG_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_LO	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the LSB bits [bits 31:0] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This address shall be set on Byte1 KByte boundary.: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.117 MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register

1 MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

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Table 14-30246. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0224h**

Figure 14-10022. MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Name Register

31	30	29	28	27	26	25	24
CQTDLBA_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
CQTDLBA_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
CQTDLBA_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
CQTDLBA_HI							
R/W							
0h							

Table 14-30248. MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_HI	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the MSB bits [bits 63:32] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This register is reserved when using 32-bit addressing mode. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.118 MMC_CTLCFG_CQ_TASK_DOOR_BELL Register

1 MMC_CTLCFG_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

Using this register, software triggers CQE to process a new task.

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Table 14-30249. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0228h**

Figure 14-10023. MMC_CTLCFG_CQ_TASK_DOOR_BELL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CQTDB_VAL</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CQTDB_VAL</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CQTDB_VAL</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CQTDB_VAL</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30251. MMC_CTLCFG_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDB_VAL	R/W1TS	0h	Command Queueing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start pro-cessing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transac-tions. CQE processes Data Transfer tasks by Reading the Task Descriptor and sending QUEUED_TASK_PARAMS[CMD44] and QUEUED_TASK_ADDRESS [CMD45]commands to the device. CQE processes DCMD tasks [in slot #31, when enabled]by Reading the Task Descriptor, and generating the com-mand encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: [a] When a task execution is completed [with success or error] [b] The task is cleared using CQTCLR register [c] All tasks are cleared using CQCTL register [d] CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time [batch submission] by Writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index,starting with the lowest index. If one or more tasks in the batch are marked with QBR,the ordering of execution will be based on said process-ing order. Writing 0 by software shall have no impact on the hard-ware, and will not change the value of the register bit. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.119 MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register

1 MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

This register is used by CQE to notify software about completed tasks.

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Table 14-30252. Instance Table

Instance Name	**Physical Address**
MMCSD0	**0FA1 022Ch**

Figure 14-10024. MMC_CTLCFG_CQ_TASK_COMP_NOTIF Name Register

31	30	29	28	27	26	25	24
CQTCN_VAL							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CQTCN_VAL							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CQTCN_VAL							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CQTCN_VAL							
R/W1TC							
0h							

Table 14-30254. MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCN_VAL	R/W1TC	0h	CQE shall set bit n of this register [at the same time it clears bit n of CQTDBR] when a task execution is com-pleted [with success or error]. When receiving interrupt for task completion, software may read this register to know which tasks have finished. After Reading this register, software may clear the rele-vant bit fields by Writing 1 to the corresponding bits. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.120 MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register

1 MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

This register stores the most recent value of the device s queue status.

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Table 14-30255. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0230h**

Figure 14-10025. MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Name Register

31	30	29	28	27	26	25	24
CQDQ_STS							
R							
0h							
23	22	21	20	19	18	17	16
CQDQ_STS							
R							
0h							
15	14	13	12	11	10	9	8
CQDQ_STS							
R							
0h							
7	6	5	4	3	2	1	0
CQDQ_STS							
R							
0h							

Table 14-30257. MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDQ_STS	R	0h	Every time the Host controller receives a queue status register [QSR] from the device, it updates this register with the response of status command, i.e. the devices queue status. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.121 MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register

1 MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

This register indicates to software which tasks are queued in the device, awaiting execution.

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Table 14-30258. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0234h**

Figure 14-10026. MMC_CTLCFG_CQ_DEV_PENDING_TASKS Name Register

31	30	29	28	27	26	25	24
CQDP_TSKS							
R							
0h							
23	22	21	20	19	18	17	16
CQDP_TSKS							
R							
0h							
15	14	13	12	11	10	9	8
CQDP_TSKS							
R							
0h							
7	6	5	4	3	2	1	0
CQDP_TSKS							
R							
0h							

Table 14-30260. MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDP_TSKS	R	0h	Bit n of this register is set if and only if QUEUED_TASK_PARAMS [CMD44] and QUEUED_TASK_ADDRESS [CMD45] were sent for this specific task and if this task hasnt been executed yet.CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution.Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued,the driver sends a CMDQ_TASK_MGMT [CMD48] to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.122 MMC_CTLCFG_CQ_TASK_CLEAR Register

1 MMC_CTLCFG_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

This register is used for removing an outstanding task in the CQE. 327. The register should be used only when CQE is in Halt state.

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Table 14-30261. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0238h**

Figure 14-10027. MMC_CTLCFG_CQ_TASK_CLEAR Name Register

31	30	29	28	27	26	25	24
CQTCLR							
R/W							
0h							
23	22	21	20	19	18	17	16
CQTCLR							
R/W							
0h							
15	14	13	12	11	10	9	8
CQTCLR							
R/W							
0h							
7	6	5	4	3	2	1	0
CQTCLR							
R/W							
0h							

Table 14-30263. MMC_CTLCFG_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCLR	R/W	0h	Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued.This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit.When software writes 1 to a bit in this register,CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields [sets a value of 0] in CQTCLR and in CQTDBR once clear operation is complete.Software should poll on the CQTCLR until it is cleared to verify clear operation was complete.Writing to this register only clears the task in the CQE and does not have impact on the device. In order to dis-card the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state.Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register.Writing 0 to a register bit shall have no impact. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.123 MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register

1 MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

The register controls the when SEND_QUEUE_STATUS commands are sent.

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Table 14-30264. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0240h**

Figure 14-10028. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CMD_BLK_CNTR			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CMD_IDLE_TIMER							
R/W							
1000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_IDLE_TIMER							
R/W							
1000h							

Table 14-30266. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	CMD_BLK_CNTR	R/W	1h	This field indicates to CQE when to send SEND_QUEUE_STATUS [CMD13] command to inquire the status of the devices task queue.A value of n means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction.A value of 0 means that SEND_QUEUE_STATUS [CMD13] command shall not be sent during the transac-tion. Instead it will be sent only when the data lines are idle.A value of 1 means that STATUS command is to be sent during the last block of the transaction. Reset Source: vbus_amod_g_rst_n

Table 14-30266. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	CMD_IDLE_TIMER	R/W	1000h	This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS [CMD13] polling.Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS.Timer units are clock periods of theclock whose fre-quency is specified in the Internal Timer Clock Fre-quency field CQCAP register.The minimum value is 0001h [1 clock period] and the maximum value is FFFFh [65535 clock periods]. Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in CQSST is 1000h, the calcu.lated polling period is 4096*52.08 ns= 213.33 us. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.124 MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register

1 MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argu-ment.

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Table 14-30267. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0244h**

Figure 14-10029. MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_RCA							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_RCA							
R/W							
0h							

Table 14-30269. MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_RCA	R/W	0h	This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS [CMD13] com-mand. argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS [CMD13] command. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.125 MMC_CTLCFG_CQ_DCMD_RESPONSE Register

1 MMC_CTLCFG_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

This register is used for passing the response of a DCMD task to software.

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Table 14-30270. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0248h**

Figure 14-10030. MMC_CTLCFG_CQ_DCMD_RESPONSE Name Register

31	30	29	28	27	26	25	24
LAST_RESP							
R							
0h							
23	22	21	20	19	18	17	16
LAST_RESP							
R							
0h							
15	14	13	12	11	10	9	8
LAST_RESP							
R							
0h							
7	6	5	4	3	2	1	0
LAST_RESP							
R							
0h							

Table 14-30272. MMC_CTLCFG_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_RESP	R	0h	This register contains the response of the command generated by the last direct-command [DCMD] task which was sent.CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQT-DBR register is cleared by CQE. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.126 MMC_CTLCFG_CQ_RESP_ERR_MASK Register

1 MMC_CTLCFG_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

This register controls the generation of Response Error Detection (RED) interrupt.

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Table 14-30273. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0250h**

Figure 14-10031. MMC_CTLCFG_CQ_RESP_ERR_MASK Name Register

31	30	29	28	27	26	25	24
CQRMEM							
R/W							
FDF9A080h							
23	22	21	20	19	18	17	16
CQRMEM							
R/W							
FDF9A080h							
15	14	13	12	11	10	9	8
CQRMEM							
R/W							
FDF9A080h							
7	6	5	4	3	2	1	0
CQRMEM							
R/W							
FDF9A080h							

Table 14-30275. MMC_CTLCFG_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQRMEM	R/W	FDF9A080h	This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses.Bit Value Description [for any bit i]:1 = When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0 = When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an inter-rupt on all Error type bits in the device status, as defined in Section 6.13.NOTE: Responses to CMD13 [SQS] encode the QSR,so they are ignored by this logic Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.127 MMC_CTLCFG_CQ_TASK_ERR_INFO Register

1 MMC_CTLCFG_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.Software is expected to use this information in the error recovery procedure.

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Table 14-30276. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0254h**

Figure 14-10032. MMC_CTLCFG_CQ_TASK_ERR_INFO Name Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED		DATERR_TASK_ID				
R	NONE		R				
0h	0h		0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		DATERR_CMD_INDEX					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESP_MODE_VALID	RESERVED		RESP_MODE_TASK_ID				
R	NONE		R				
0h	0h		0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RESP_MODE_CMD_INDEX					
NONE		R					
0h		0h					

Table 14-30278. MMC_CTLCFG_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/ indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
30:29	RESERVED	NONE	0h	Reserved
28:24	DATERR_TASK_ID	R	0h	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller Reset Source: vbus_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-30278. MMC_CTLCFG_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	DATERR_CMD_INDEX	R	0h	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK[CMD46] or EXECUTE_WRITE_TASK [CMD47] accord-ing to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
15	RESP_MODE_VALID	R	0h	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/ indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
14:13	RESERVED	NONE	0h	Reserved
12:8	RESP_MODE_TASK_ID	R	0h	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	RESP_MODE_CMD_INDEX	R	0h	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.128 MMC_CTLCFG_CQ_CMD_RESP_INDEX Register

1 MMC_CTLCFG_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-30279. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0258h**

Figure 14-10033. MMC_CTLCFG_CQ_CMD_RESP_INDEX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		LAST_CRI					
NONE		R					
0h		0h					

Table 14-30281. MMC_CTLCFG_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	LAST_CRI	R	0h	This field stores the index of the last received command response. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.129 MMC_CTLCFG_CQ_CMD_RESP_ARG Register

1 MMC_CTLCFG_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-30282. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 025Ch**

Figure 14-10034. MMC_CTLCFG_CQ_CMD_RESP_ARG Name Register

31	30	29	28	27	26	25	24
LAST_CRA							
R							
0h							
23	22	21	20	19	18	17	16
LAST_CRA							
R							
0h							
15	14	13	12	11	10	9	8
LAST_CRA							
R							
0h							
7	6	5	4	3	2	1	0
LAST_CRA							
R							
0h							

Table 14-30284. MMC_CTLCFG_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_CRA	R	0h	This field stores the argument of the last received com-mand. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.130 MMC_CTLCFG_CQ_ERROR_TASK_ID Register

1 MMC_CTLCFG_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

CQ Error Task ID Register

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Table 14-30285. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 0260h**

Figure 14-10035. MMC_CTLCFG_CQ_ERROR_TASK_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TERR_ID				
NONE			R				
0h			0h				

Table 14-30287. MMC_CTLCFG_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	TERR_ID	R	0h	Task Error ID Reset Source: vbus_amod_g_rst_n

14.9.4.6.2.131 MMC_SSCFG_SS_ID_REV_REG Register

1 MMC_SSCFG_SS_ID_REV_REG Register (Offset = 0h) [reset = 68421200h]

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem

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Table 14-30288. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8000h**

Figure 14-10036. MMC_SSCFG_SS_ID_REV_REG Name Register

31	30	29	28	27	26	25	24
MOD_ID							
R							
6842h							
23	22	21	20	19	18	17	16
MOD_ID							
R							
6842h							
15	14	13	12	11	10	9	8
RTL_VER					MAJ_REV		
R					R		
2h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MIN_REV					
R		R					
0h		0h					

Table 14-30290. MMC_SSCFG_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MOD_ID	R	6842h	Module ID Reset Source: vbus_smod_g_rst_n
15:11	RTL_VER	R	2h	RTL version Reset Source: vbus_smod_g_rst_n
10:8	MAJ_REV	R	2h	Major revision Reset Source: vbus_smod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_smod_g_rst_n
5:0	MIN_REV	R	0h	Minor revision Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.132 MMC_SSCFG_CTL_CFG_1_REG Register

1 MMC_SSCFG_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

The Controller Config 1 Register contains various fields to control the configuration ports on the eMMC/SD Controller.

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Table 14-30291. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8010h**

Figure 14-10037. MMC_SSCFG_CTL_CFG_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		TUNINGCOUNT					
NONE		R/W					
0h		20h					
23	22	21	20	19	18	17	16
RESERVED			ASYNCWKUPENA	RESERVED			
NONE			R/W	NONE			
0h			1h	0h			
15	14	13	12	11	10	9	8
CQFMUL				RESERVED		CQFVAL	
R/W				NONE		R/W	
3h				0h		C8h	
7	6	5	4	3	2	1	0
CQFVAL							
R/W							
C8h							

Table 14-30293. MMC_SSCFG_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TUNINGCOUNT	R/W	20h	Configures the Number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure. Reset Source: vbus_smod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0: Synchronous Wakeup Mode: The xin_clk has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the xin_clk and the Wakeup Event is generated. The Assertion and deassertion of the wakeup Event signal synchronous to xin_clk. 1: Asyncrhonous Wakeup Mode: The xin_clk and the host_clk can be stopped in this mode and the Wake up Event is asynchronously generated based on the Card Insertion/Removal/Interrupt Events. The Assertion and deassertion of the wakeup Event signal is asynchronous. Reset Source: vbus_smod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved

Table 14-30293. MMC_SSCFG_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.133 MMC_SSCFG_CTL_CFG_2_REG Register

1 MMC_SSCFG_CTL_CFG_2_REG Register (Offset = 14h) [reset = 25ECC801h]

The Controller Config 2 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the lsb fields in the Capabilities Register inside the eMMC/SD Controller.

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Table 14-30294. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8014h**

Figure 14-10038. MMC_SSCFG_CTL_CFG_2_REG Name Register

31	30	29	28	27	26	25	24
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W		R/W	NONE		R/W	R/W	R/W
0h		1h	0h		1h	0h	1h

23	22	21	20	19	18	17	16
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W	R/W	R/W	NONE	R/W	R/W	R/W	
1h	1h	1h	0h	1h	1h	0h	

15	14	13	12	11	10	9	8
BASECLKFREQ							
R/W							
C8h							

7	6	5	4	3	2	1	0
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W	NONE	R/W					
0h	0h	1h					

Table 14-30296. MMC_SSCFG_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SLOTTYPE	R/W	0h	Slot Type. Should be set based on the final product usage. 00 - Removable SCard Slot, 01 - Embedded Slot for One Device, 10 - Shared Bus Slot, 11 - Reserved. Reset Source: vbus_smod_g_rst_n
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support. Suggested Value is 1'b1 (The Core supports monitoring of Asynchronous Interrupt). Reset Source: vbus_smod_g_rst_n
28:27	RESERVED	NONE	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8V Support. Suggested Value is 1'b1 (The 1.8 Volt Switching is supported by Core). Optionally can be set to 1'b0 if the application doesn't want 1.8V switching (SD3.0). Reset Source: vbus_smod_g_rst_n
25	SUPPORT3P0VOLT	R/W	0h	3.0V Support. Should be set based on whether 3.0V is supported on the SD Interface. Reset Source: vbus_smod_g_rst_n

Table 14-30296. MMC_SSCFG_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SUPPORT3P3VOLT	R/W	1h	3.3V Support. Suggested Value is 1'b1 as the 3.3 V is the default voltage on the SD Interface. Reset Source: vbus_smod_g_rst_n
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support. Suggested Value is 1'b1 (The Suspend/ Resume is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support Suspend/Resume Mode. Reset Source: vbus_smod_g_rst_n
22	SDMASUPPORT	R/W	1h	SDMA Support. Suggested Value is 1'b1 (The SDMA is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support SDMA Mode. Reset Source: vbus_smod_g_rst_n
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support. Suggested Value is 1'b1 (The High Speed mode is supported by Core). Reset Source: vbus_smod_g_rst_n
20	RESERVED	NONE	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support. Suggested Value is 1'b1 (The ADMA2 is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support ADMA2 Mode. Reset Source: vbus_smod_g_rst_n
18	SUPPORT8BIT	R/W	1h	8-bit Support for Embedded Device. Suggested Value is 1'b1 (The Core supports 8-bit Interface). Optionally an be set to 1'b0 if the Application supports only 4-bit SD Interface. Reset Source: vbus_smod_g_rst_n
17:16	MAXBLKLENGTH	R/W	0h	Max Block Length. Maximum Block Length supported by the Core/ Device. 00: 512 (Bytes), 01: 1024, 10: 2048, 11: Reserved. Reset Source: vbus_smod_g_rst_n
15:8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock. This is the frequency of the xin_clk. Reset Source: vbus_smod_g_rst_n
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit. Suggested Value is 1'b0 (KHz). Reset Source: vbus_smod_g_rst_n
6	RESERVED	NONE	0h	Reserved
5:0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency. Suggested Value is 1 KHz. Internally the 1msec Timer is used for Timeout Detection. The 1msec Timer is generated from the xin_clk. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.134 MMC_SSCFG_CTL_CFG_3_REG Register

1 MMC_SSCFG_CTL_CFG_3_REG Register (Offset = 18h) [reset = 18000407h]

The Controller Config 3 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the msb fields in the Capabilities Register inside the eMMC/SD Controller.

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Table 14-30297. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8018h**

Figure 14-10039. MMC_SSCFG_CTL_CFG_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			SUPPORT1P8VDD2	ADMA3SUPPORT	RESERVED		
NONE			R/W	R/W	NONE		
0h			1h	1h	0h		

23	22	21	20	19	18	17	16
CLOCKMULTIPLIER							
R/W							
0h							

15	14	13	12	11	10	9	8
RETUNINGMODES		TUNINGFORSDR50	RESERVED	RETUNINGTIMERCNT			
R/W		R/W	NONE	R/W			
0h		0h	0h	4h			

7	6	5	4	3	2	1	0
TYPE4SUPPORT	DDRIVERSUPPORT	CDRIVERSUPPORT	ADRIVERSUPPORT	RESERVED	DDR50SUPPORT	SDR104SUPPORT	SDR50SUPPORT
R/W	R/W	R/W	R/W	NONE	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	1h	1h

Table 14-30299. MMC_SSCFG_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8V VDD2 Support. Reset Source: vbus_smod_g_rst_n
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support. Reset Source: vbus_smod_g_rst_n
26:24	RESERVED	NONE	0h	Reserved
23:16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier. This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. FFh Clock Multiplier M = 256, ..., 02h Clock Multiplier M = 3, 01h Clock Multiplier M = 2, 00h Clock Multiplier is Not Supported. Reset Source: vbus_smod_g_rst_n
15:14	RETUNINGMODES	R/W	0h	Re-Tuning Modes. Should be set to 2'b00 as the Core supports only the Software Timer based Re-Tuning. Reset Source: vbus_smod_g_rst_n

Table 14-30299. MMC_SSCFG_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50. This bit should be set if the Application wants Tuning be used for SDR50 Modes. The Core operates with or with out tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay. Reset Source: vbus_smod_g_rst_n
12	RESERVED	NONE	0h	Reserved
11:8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning. This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer. Reset Source: vbus_smod_g_rst_n
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support. This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support. This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support. This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support. This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	DDR50SUPPORT	R/W	1h	DDR50 Support. Suggested Value is 1'b1 (The Core supports DDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support DDR50. Reset Source: vbus_smod_g_rst_n
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1'b1 (The Core supports SDR104 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR104. Reset Source: vbus_smod_g_rst_n
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1'b1 (The Core supports SDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.135 MMC_SSCFG_CTL_CFG_4_REG Register

1 MMC_SSCFG_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

The Controller Config 4 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the lsb fields in the Maximum Current Capabilities Register inside the eMMC/SD Controller.

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Table 14-30300. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 801Ch**

Figure 14-10040. MMC_SSCFG_CTL_CFG_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAXCURRENT1P8V							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXCURRENT3P0V							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXCURRENT3P3V							
R/W							
0h							

Table 14-30302. MMC_SSCFG_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAXCURRENT1P8V	R/W	0h	Maximum Current for 1.8V. Reset Source: vbus_smod_g_rst_n
15:8	MAXCURRENT3P0V	R/W	0h	Maximum Current for 3.0V. Reset Source: vbus_smod_g_rst_n
7:0	MAXCURRENT3P3V	R/W	0h	Maximum Current for 3.3V. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.136 MMC_SSCFG_CTL_CFG_5_REG Register

1 MMC_SSCFG_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

The Controller Config 5 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the msb fields in the Maximum Current Capabilities Register inside the eMMC/SD Controller.

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Table 14-30303. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8020h**

Figure 14-10041. MMC_SSCFG_CTL_CFG_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MAXCURRENTVDD2							
R/W							
0h							

Table 14-30305. MMC_SSCFG_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MAXCURRENTVDD2	R/W	0h	Maximum Current for 1.8 V (VDD2). Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.137 MMC_SSCFG_CTL_CFG_6_REG Register

1 MMC_SSCFG_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

The Controller Config 6 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for Initialization inside the eMMC/SD Controller.

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Table 14-30306. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8024h**

Figure 14-10042. MMC_SSCFG_CTL_CFG_6_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			INITPRESETVAL				
NONE			R/W				
0h			100h				
7	6	5	4	3	2	1	0
INITPRESETVAL							
R/W							
100h							

Table 14-30308. MMC_SSCFG_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	INITPRESETVAL	R/W	100h	Preset Value for Initialization. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.138 MMC_SSCFG_CTL_CFG_7_REG Register

1 MMC_SSCFG_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

The Controller Config 7 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for Default Speed inside the eMMC/SD Controller.

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Table 14-30309. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8028h**

Figure 14-10043. MMC_SSCFG_CTL_CFG_7_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DSPDPRESETVAL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DSPDPRESETVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-30311. MMC_SSCFG_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	DSPDPRESETVAL	R/W	4h	Preset Value for Default Speed. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.139 MMC_SSCFG_CTL_CFG_8_REG Register

1 MMC_SSCFG_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

The Controller Config 8 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for High Speed inside the eMMC/SD Controller.

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Table 14-30312. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 802Ch**

Figure 14-10044. MMC_SSCFG_CTL_CFG_8_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			HSPDPRESETVAL				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
HSPDPRESETVAL							
R/W							
2h							

Table 14-30314. MMC_SSCFG_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	HSPDPRESETVAL	R/W	2h	Preset Value for High Speed. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.140 MMC_SSCFG_CTL_CFG_9_REG Register

1 MMC_SSCFG_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

The Controller Config 9 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR12 inside the eMMC/SD Controller.

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Table 14-30315. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8030h**

Figure 14-10045. MMC_SSCFG_CTL_CFG_9_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR12PRESETVAL				
NONE			R/W				
0h			4h				
7	6	5	4	3	2	1	0
SDR12PRESETVAL							
R/W							
4h							

Table 14-30317. MMC_SSCFG_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR12PRESETVAL	R/W	4h	Preset Value for SDR12. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.141 MMC_SSCFG_CTL_CFG_10_REG Register

1 MMC_SSCFG_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

The Controller Config 10 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR25 inside the eMMC/SD Controller.

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Table 14-30318. Instance Table

Instance Name	**Physical Address**
MMCSD0	**0FA1 8034h**

Figure 14-10046. MMC_SSCFG_CTL_CFG_10_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR25PRESETVAL				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
SDR25PRESETVAL							
R/W							
2h							

Table 14-30320. MMC_SSCFG_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR25PRESETVAL	R/W	2h	Preset Value for SDR25. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.142 MMC_SSCFG_CTL_CFG_11_REG Register

1 MMC_SSCFG_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

The Controller Config 11 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR50 inside the eMMC/SD Controller.

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Table 14-30321. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8038h**

Figure 14-10047. MMC_SSCFG_CTL_CFG_11_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR50PRESETVAL				
NONE			R/W				
0h			1h				
7	6	5	4	3	2	1	0
SDR50PRESETVAL							
R/W							
1h							

Table 14-30323. MMC_SSCFG_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR50PRESETVAL	R/W	1h	Preset Value for SDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.143 MMC_SSCFG_CTL_CFG_12_REG Register

1 MMC_SSCFG_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

The Controller Config 12 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR104 inside the eMMC/SD Controller.

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Table 14-30324. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 803Ch**

Figure 14-10048. MMC_SSCFG_CTL_CFG_12_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR104PRESETVAL				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
SDR104PRESETVAL							
R/W							
0h							

Table 14-30326. MMC_SSCFG_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR104PRESETVAL	R/W	0h	Preset Value for SDR104. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.144 MMC_SSCFG_CTL_CFG_13_REG Register

1 MMC_SSCFG_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

The Controller Config 13 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for DDR50 inside the eMMC/SD Controller.

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Table 14-30327. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8040h**

Figure 14-10049. MMC_SSCFG_CTL_CFG_13_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DDR50PRESETVAL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DDR50PRESETVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-30329. MMC_SSCFG_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	DDR50PRESETVAL	R/W	2h	Preset Value for DDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.145 MMC_SSCFG_CTL_CFG_14_REG Register

1 MMC_SSCFG_CTL_CFG_14_REG Register (Offset = 44h) [reset = 0h]

The Controller Config 14 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for HS400 inside the eMMC/SD Controller.

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Table 14-30330. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8044h**

Figure 14-10050. MMC_SSCFG_CTL_CFG_14_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30332. MMC_SSCFG_CTL_CFG_14_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.146 MMC_SSCFG_CTL_STAT_1_REG Register

1 MMC_SSCFG_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30333. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8060h**

Figure 14-10051. MMC_SSCFG_CTL_STAT_1_REG Name Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED		RXCLKTAPSEL				
R	NONE		R				
1h	0h		0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMADEBUGBUS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMADEBUGBUS							
R							
0h							

Table 14-30335. MMC_SSCFG_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable S/W to gate off the clocks. Reset Source: vbus_smod_g_rst_n
30:29	RESERVED	NONE	0h	Reserved
28:24	RXCLKTAPSEL	R	0h	Controller HW tunning RX clock tap selection value. Reset Source: vbus_smod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.147 MMC_SSCFG_CTL_STAT_2_REG Register

1 MMC_SSCFG_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30336. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8064h**

Figure 14-10052. MMC_SSCFG_CTL_STAT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CMDDEBUGBUS							
R							
10h							
7	6	5	4	3	2	1	0
CMDDEBUGBUS							
R							
10h							

Table 14-30338. MMC_SSCFG_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.148 MMC_SSCFG_CTL_STAT_3_REG Register

1 MMC_SSCFG_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30339. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8068h**

Figure 14-10053. MMC_SSCFG_CTL_STAT_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TXDDEBUGBUS							
R							
0h							
7	6	5	4	3	2	1	0
TXDDEBUGBUS							
R							
0h							

Table 14-30341. MMC_SSCFG_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.149 MMC_SSCFG_CTL_STAT_4_REG Register

1 MMC_SSCFG_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30342. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 806Ch**

Figure 14-10054. MMC_SSCFG_CTL_STAT_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RXDDEBUGBUS0							
R							
0h							
7	6	5	4	3	2	1	0
RXDDEBUGBUS0							
R							
0h							

Table 14-30344. MMC_SSCFG_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK). Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.150 MMC_SSCFG_CTL_STAT_5_REG Register

1 MMC_SSCFG_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30345. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8070h**

Figure 14-10055. MMC_SSCFG_CTL_STAT_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RXDDEBUGBUS1							
R							
8h							
7	6	5	4	3	2	1	0
RXDDEBUGBUS1							
R							
8h							

Table 14-30347. MMC_SSCFG_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK). Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.151 MMC_SSCFG_CTL_STAT_6_REG Register

1 MMC_SSCFG_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30348. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8074h**

Figure 14-10056. MMC_SSCFG_CTL_STAT_6_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TUNDEBUGBUS							
R							
0h							
7	6	5	4	3	2	1	0
TUNDEBUGBUS							
R							
0h							

Table 14-30350. MMC_SSCFG_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.152 MMC_SSCFG_PHY_CTRL_1_REG Register

1 MMC_SSCFG_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80000000h]

The PHY Control 1 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30351. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8100h**

Figure 14-10057. MMC_SSCFG_PHY_CTRL_1_REG Name Register

31	30	29	28	27	26	25	24
IOMUX_ENABLE	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30353. MMC_SSCFG_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOMUX_ENABLE	R/W	1h	IO mux enable. Set 1 for GPIO. Set 0 for eMMC/SD Reset Source: vbus_smod_g_rst_n
30:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.153 MMC_SSCFG_PHY_CTRL_2_REG Register

1 MMC_SSCFG_PHY_CTRL_2_REG Register (Offset = 104h) [reset = 0h]

The PHY Control 2 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30354. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8104h**

Figure 14-10058. MMC_SSCFG_PHY_CTRL_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30356. MMC_SSCFG_PHY_CTRL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.154 MMC_SSCFG_PHY_CTRL_3_REG Register

1 MMC_SSCFG_PHY_CTRL_3_REG Register (Offset = 108h) [reset = 0h]

The PHY Control 3 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30357. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8108h**

Figure 14-10059. MMC_SSCFG_PHY_CTRL_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30359. MMC_SSCFG_PHY_CTRL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.155 MMC_SSCFG_PHY_CTRL_4_REG Register

1 MMC_SSCFG_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

The PHY Control 4 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30360. Instance Table

Instance Name	Physical Address
MMCSD0	0FA1 810Ch

Figure 14-10060. MMC_SSCFG_PHY_CTRL_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED			OTAPDLYENA	RESERVED			OTAPDLYSEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

15	14	13	12	11	10	9	8
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W				NONE		R/W	R/W
0h				0h		0h	0h

7	6	5	4	3	2	1	0
RESERVED			ITAPDLYSEL				
NONE			R/W				
0h			0h				

Table 14-30362. MMC_SSCFG_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable. Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
19:17	RESERVED	NONE	0h	Reserved
16:12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select. Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window. It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches. Reset Source: vbus_smod_g_rst_n
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable. This is used for the manual control of the RX clock Tap Delay in non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n

Table 14-30362. MMC_SSCFG_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	RESERVED	NONE	0h	Reserved
4:0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select. Manual control of the RX clock Tap Delay in the non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n

14.9.4.6.2.156 MMC_SSCFG_PHY_CTRL_5_REG Register

1 MMC_SSCFG_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

The PHY Control 5 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30363. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8110h**

Figure 14-10061. MMC_SSCFG_PHY_CTRL_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RESERVED		
NONE					R/W		
0h					0h		

Table 14-30365. MMC_SSCFG_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	R/W	0h	Reserved

14.9.4.6.2.157 MMC_SSCFG_PHY_CTRL_6_REG Register

1 MMC_SSCFG_PHY_CTRL_6_REG Register (Offset = 114h) [reset = 0h]

The PHY Control 6 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30366. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8114h**

Figure 14-10062. MMC_SSCFG_PHY_CTRL_6_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30368. MMC_SSCFG_PHY_CTRL_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.158 MMC_SSCFG_PHY_STAT_1_REG Register

1 MMC_SSCFG_PHY_STAT_1_REG Register (Offset = 130h) [reset = 0h]

The PHY Status 1 Register contains various fields to reflect the status of the eMMC/SD PHY ports. For detailed functionality of the eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-30369. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8130h**

Figure 14-10063. MMC_SSCFG_PHY_STAT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30371. MMC_SSCFG_PHY_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.159 MMC_SSCFG_PHY_STAT_2_REG Register

1 MMC_SSCFG_PHY_STAT_2_REG Register (Offset = 134h) [reset = 0h]

The PHY Status 2 Register contains various fields to reflect the status of the eMMC/SD PHY ports. For detailed functionality of the eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-30372. Instance Table

Instance Name	Physical Address
MMCSD0	**0FA1 8134h**

Figure 14-10064. MMC_SSCFG_PHY_STAT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30374. MMC_SSCFG_PHY_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7 MMCSD1/MMCSD2

MMCSD1/MMCSD2

14.9.4.7.1 MMCSD1/MMCSD2 Summaries

MMCSD1/MMCSD2 Summaries

Table 14-30375. ECC_AGGR Registers, Base Address=0070 8000h, Length=1024

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
0h	32	ECC_AGGR_REV	0070 8000h	0070 B000h
8h	32	ECC_AGGR_VECTOR	0070 8008h	0070 B008h
Ch	32	ECC_AGGR_STAT	0070 800Ch	0070 B00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 8010h + formula	0070 B010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 803Ch	0070 B03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 8040h	0070 B040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 8080h	0070 B080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 80C0h	0070 B0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 813Ch	0070 B13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 8140h	0070 B140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 8180h	0070 B180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 81C0h	0070 B1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 8200h	0070 B200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 8204h	0070 B204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 8208h	0070 B208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 820Ch	0070 B20Ch

Table 14-30376. ECC_AGGR Registers, Base Address=0070 9000h, Length=1024

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
0h	32	ECC_AGGR_REV	0070 9000h	0070 A000h
8h	32	ECC_AGGR_VECTOR	0070 9008h	0070 A008h
Ch	32	ECC_AGGR_STAT	0070 900Ch	0070 A00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 9010h + formula	0070 A010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 903Ch	0070 A03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 9040h	0070 A040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 9080h	0070 A080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 90C0h	0070 A0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 913Ch	0070 A13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 9140h	0070 A140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 9180h	0070 A180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 91C0h	0070 A1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 9200h	0070 A200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 9204h	0070 A204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 9208h	0070 A208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 920Ch	0070 A20Ch

Table 14-30377. MMC_CTLCFG Registers, Base Address=0FA0 0000h, Length=4096

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
0h	16	MMC_CTLCFG_SDMA_SYS_ADDR_LO	0FA0 0000h	0FA2 0000h
2h	16	MMC_CTLCFG_SDMA_SYS_ADDR_HI	0FA0 0002h	0FA2 0002h
4h	16	MMC_CTLCFG_BLOCK_SIZE	0FA0 0004h	0FA2 0004h
6h	16	MMC_CTLCFG_BLOCK_COUNT	0FA0 0006h	0FA2 0006h
8h	16	MMC_CTLCFG_ARGUMENT1_LO	0FA0 0008h	0FA2 0008h
Ah	16	MMC_CTLCFG_ARGUMENT1_HI	0FA0 000Ah	0FA2 000Ah
Ch	16	MMC_CTLCFG_TRANSFER_MODE	0FA0 000Ch	0FA2 000Ch
Eh	16	MMC_CTLCFG_COMMAND	0FA0 000Eh	0FA2 000Eh
10h	16	MMC_CTLCFG_RESPONSE_J	0FA0 0010h + formula	0FA2 0010h + formula
20h	32	MMC_CTLCFG_DATA_PORT	0FA0 0020h	0FA2 0020h
24h	32	MMC_CTLCFG_PRESENTSTATE	0FA0 0024h	0FA2 0024h
28h	8	MMC_CTLCFG_HOST_CONTROL1	0FA0 0028h	0FA2 0028h
29h	8	MMC_CTLCFG_POWER_CONTROL	0FA0 0029h	0FA2 0029h
2Ah	8	MMC_CTLCFG_BLOCK_GAP_CONTROL	0FA0 002Ah	0FA2 002Ah
2Bh	8	MMC_CTLCFG_WAKEUP_CONTROL	0FA0 002Bh	0FA2 002Bh
2Ch	16	MMC_CTLCFG_CLOCK_CONTROL	0FA0 002Ch	0FA2 002Ch
2Eh	8	MMC_CTLCFG_TIMEOUT_CONTROL	0FA0 002Eh	0FA2 002Eh
2Fh	8	MMC_CTLCFG_SOFTWARE_RESET	0FA0 002Fh	0FA2 002Fh
30h	16	MMC_CTLCFG_NORMAL_INTR_STS	0FA0 0030h	0FA2 0030h
32h	16	MMC_CTLCFG_ERROR_INTR_STS	0FA0 0032h	0FA2 0032h
34h	16	MMC_CTLCFG_NORMAL_INTR_STS_ENA	0FA0 0034h	0FA2 0034h
36h	16	MMC_CTLCFG_ERROR_INTR_STS_ENA	0FA0 0036h	0FA2 0036h
38h	16	MMC_CTLCFG_NORMAL_INTR_SIG_ENA	0FA0 0038h	0FA2 0038h
3Ah	16	MMC_CTLCFG_ERROR_INTR_SIG_ENA	0FA0 003Ah	0FA2 003Ah
3Ch	16	MMC_CTLCFG_AUTOCMD_ERR_STS	0FA0 003Ch	0FA2 003Ch
3Eh	16	MMC_CTLCFG_HOST_CONTROL2	0FA0 003Eh	0FA2 003Eh
40h	64	MMC_CTLCFG_CAPABILITIES	0FA0 0040h	0FA2 0040h
48h	64	MMC_CTLCFG_MAX_CURRENT_CAP	0FA0 0048h	0FA2 0048h
50h	16	MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS	0FA0 0050h	0FA2 0050h
52h	16	MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS	0FA0 0052h	0FA2 0052h
54h	8	MMC_CTLCFG_ADMA_ERR_STATUS	0FA0 0054h	0FA2 0054h
58h	64	MMC_CTLCFG_ADMA_SYS_ADDRESS	0FA0 0058h	0FA2 0058h
60h	16	MMC_CTLCFG_PRESET_VALUE0	0FA0 0060h	0FA2 0060h
62h	16	MMC_CTLCFG_PRESET_VALUE1	0FA0 0062h	0FA2 0062h
64h	16	MMC_CTLCFG_PRESET_VALUE2	0FA0 0064h	0FA2 0064h
66h	16	MMC_CTLCFG_PRESET_VALUE3	0FA0 0066h	0FA2 0066h
68h	16	MMC_CTLCFG_PRESET_VALUE4	0FA0 0068h	0FA2 0068h
6Ah	16	MMC_CTLCFG_PRESET_VALUE5	0FA0 006Ah	0FA2 006Ah
6Ch	16	MMC_CTLCFG_PRESET_VALUE6	0FA0 006Ch	0FA2 006Ch
6Eh	16	MMC_CTLCFG_PRESET_VALUE7	0FA0 006Eh	0FA2 006Eh
72h	16	MMC_CTLCFG_PRESET_VALUE8	0FA0 0072h	0FA2 0072h
74h	16	MMC_CTLCFG_PRESET_VALUE10	0FA0 0074h	0FA2 0074h
78h	64	MMC_CTLCFG_ADMA3_DESC_ADDRESS	0FA0 0078h	0FA2 0078h
80h	16	MMC_CTLCFG_UHS2_BLOCK_SIZE	0FA0 0080h	0FA2 0080h

Table 14-30377. MMC_CTLCFG Registers, Base Address=0FA0 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
84h	32	MMC_CTLCFG_UHS2_BLOCK_COUNT	0FA0 0084h	0FA2 0084h
88h	8	MMC_CTLCFG_UHS2_COMMAND_PKT_J	0FA0 0088h + formula	0FA2 0088h + formula
9Ch	16	MMC_CTLCFG_UHS2_XFER_MODE	0FA0 009Ch	0FA2 009Ch
9Eh	16	MMC_CTLCFG_UHS2_COMMAND	0FA0 009Eh	0FA2 009Eh
A0h	8	MMC_CTLCFG_UHS2_RESPONSE_J	0FA0 00A0h + formula	0FA2 00A0h + formula
B4h	8	MMC_CTLCFG_UHS2_MESSAGE_SELECT	0FA0 00B4h	0FA2 00B4h
B8h	32	MMC_CTLCFG_UHS2_MESSAGE	0FA0 00B8h	0FA2 00B8h
BCh	16	MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS	0FA0 00BCh	0FA2 00BCh
BEh	8	MMC_CTLCFG_UHS2_DEVICE_SELECT	0FA0 00BEh	0FA2 00BEh
BFh	8	MMC_CTLCFG_UHS2_DEVICE_INT_CODE	0FA0 00BFh	0FA2 00BFh
C0h	16	MMC_CTLCFG_UHS2_SOFTWARE_RESET	0FA0 00C0h	0FA2 00C0h
C2h	16	MMC_CTLCFG_UHS2_TIMER_CONTROL	0FA0 00C2h	0FA2 00C2h
C4h	32	MMC_CTLCFG_UHS2_ERR_INTR_STS	0FA0 00C4h	0FA2 00C4h
C8h	32	MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA	0FA0 00C8h	0FA2 00C8h
CCh	32	MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA	0FA0 00CCh	0FA2 00CCh
E0h	16	MMC_CTLCFG_UHS2_SETTINGS_PTR	0FA0 00E0h	0FA2 00E0h
E2h	16	MMC_CTLCFG_UHS2_CAPABILITIES_PTR	0FA0 00E2h	0FA2 00E2h
E4h	16	MMC_CTLCFG_UHS2_TEST_PTR	0FA0 00E4h	0FA2 00E4h
E6h	16	MMC_CTLCFG_SHARED_BUS_CTRL_PTR	0FA0 00E6h	0FA2 00E6h
E8h	16	MMC_CTLCFG_VENDOR_SPECFIC_PTR	0FA0 00E8h	0FA2 00E8h
F4h	32	MMC_CTLCFG_BOOT_TIMEOUT_CONTROL	0FA0 00F4h	0FA2 00F4h
F8h	32	MMC_CTLCFG_VENDOR_REGISTER	0FA0 00F8h	0FA2 00F8h
FCh	16	MMC_CTLCFG_SLOT_INT_STS	0FA0 00FCh	0FA2 00FCh
FEh	16	MMC_CTLCFG_HOST_CONTROLLER_VER	0FA0 00FEh	0FA2 00FEh
100h	32	MMC_CTLCFG_UHS2_GEN_SETTINGS	0FA0 0100h	0FA2 0100h
104h	32	MMC_CTLCFG_UHS2_PHY_SETTINGS	0FA0 0104h	0FA2 0104h
108h	64	MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS	0FA0 0108h	0FA2 0108h
110h	32	MMC_CTLCFG_UHS2_GEN_CAP	0FA0 0110h	0FA2 0110h
114h	32	MMC_CTLCFG_UHS2_PHY_CAP	0FA0 0114h	0FA2 0114h
118h	64	MMC_CTLCFG_UHS2_LNK_TRN_CAP	0FA0 0118h	0FA2 0118h
120h	32	MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS	0FA0 0120h	0FA2 0120h
200h	32	MMC_CTLCFG_CQ_VERSION	0FA0 0200h	0FA2 0200h
204h	32	MMC_CTLCFG_CQ_CAPABILITIES	0FA0 0204h	0FA2 0204h
208h	32	MMC_CTLCFG_CQ_CONFIG	0FA0 0208h	0FA2 0208h
20Ch	32	MMC_CTLCFG_CQ_CONTROL	0FA0 020Ch	0FA2 020Ch
210h	32	MMC_CTLCFG_CQ_INTR_STS	0FA0 0210h	0FA2 0210h
214h	32	MMC_CTLCFG_CQ_INTR_STS_ENA	0FA0 0214h	0FA2 0214h

Table 14-30377. MMC_CTLCFG Registers, Base Address=0FA0 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
218h	32	MMC_CTLCFG_CQ_INTR_SIG_ENA	0FA0 0218h	0FA2 0218h
21Ch	32	MMC_CTLCFG_CQ_INTR_COALESCING	0FA0 021Ch	0FA2 021Ch
220h	32	MMC_CTLCFG_CQ_TDL_BASE_ADDR	0FA0 0220h	0FA2 0220h
224h	32	MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS	0FA0 0224h	0FA2 0224h
228h	32	MMC_CTLCFG_CQ_TASK_DOOR_BELL	0FA0 0228h	0FA2 0228h
22Ch	32	MMC_CTLCFG_CQ_TASK_COMP_NOTIF	0FA0 022Ch	0FA2 022Ch
230h	32	MMC_CTLCFG_CQ_DEV_QUEUE_STATUS	0FA0 0230h	0FA2 0230h
234h	32	MMC_CTLCFG_CQ_DEV_PENDING_TASKS	0FA0 0234h	0FA2 0234h
238h	32	MMC_CTLCFG_CQ_TASK_CLEAR	0FA0 0238h	0FA2 0238h
240h	32	MMC_CTLCFG_CQ_SEND_STS_CONFIG1	0FA0 0240h	0FA2 0240h
244h	32	MMC_CTLCFG_CQ_SEND_STS_CONFIG2	0FA0 0244h	0FA2 0244h
248h	32	MMC_CTLCFG_CQ_DCMD_RESPONSE	0FA0 0248h	0FA2 0248h
250h	32	MMC_CTLCFG_CQ_RESP_ERR_MASK	0FA0 0250h	0FA2 0250h
254h	32	MMC_CTLCFG_CQ_TASK_ERR_INFO	0FA0 0254h	0FA2 0254h
258h	32	MMC_CTLCFG_CQ_CMD_RESP_INDEX	0FA0 0258h	0FA2 0258h
25Ch	32	MMC_CTLCFG_CQ_CMD_RESP_ARG	0FA0 025Ch	0FA2 025Ch
260h	32	MMC_CTLCFG_CQ_ERROR_TASK_ID	0FA0 0260h	0FA2 0260h

Table 14-30378. MMC_SSCFG Registers, Base Address=0FA0 8000h, Length=1024

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
0h	32	MMC_SSCFG_SS_ID_REV_REG	0FA0 8000h	0FA2 8000h
10h	32	MMC_SSCFG_CTL_CFG_1_REG	0FA0 8010h	0FA2 8010h
14h	32	MMC_SSCFG_CTL_CFG_2_REG	0FA0 8014h	0FA2 8014h
18h	32	MMC_SSCFG_CTL_CFG_3_REG	0FA0 8018h	0FA2 8018h
1Ch	32	MMC_SSCFG_CTL_CFG_4_REG	0FA0 801Ch	0FA2 801Ch
20h	32	MMC_SSCFG_CTL_CFG_5_REG	0FA0 8020h	0FA2 8020h
24h	32	MMC_SSCFG_CTL_CFG_6_REG	0FA0 8024h	0FA2 8024h
28h	32	MMC_SSCFG_CTL_CFG_7_REG	0FA0 8028h	0FA2 8028h
2Ch	32	MMC_SSCFG_CTL_CFG_8_REG	0FA0 802Ch	0FA2 802Ch
30h	32	MMC_SSCFG_CTL_CFG_9_REG	0FA0 8030h	0FA2 8030h
34h	32	MMC_SSCFG_CTL_CFG_10_REG	0FA0 8034h	0FA2 8034h
38h	32	MMC_SSCFG_CTL_CFG_11_REG	0FA0 8038h	0FA2 8038h
3Ch	32	MMC_SSCFG_CTL_CFG_12_REG	0FA0 803Ch	0FA2 803Ch
40h	32	MMC_SSCFG_CTL_CFG_13_REG	0FA0 8040h	0FA2 8040h
44h	32	MMC_SSCFG_CTL_CFG_14_REG	0FA0 8044h	0FA2 8044h
60h	32	MMC_SSCFG_CTL_STAT_1_REG	0FA0 8060h	0FA2 8060h
64h	32	MMC_SSCFG_CTL_STAT_2_REG	0FA0 8064h	0FA2 8064h
68h	32	MMC_SSCFG_CTL_STAT_3_REG	0FA0 8068h	0FA2 8068h
6Ch	32	MMC_SSCFG_CTL_STAT_4_REG	0FA0 806Ch	0FA2 806Ch
70h	32	MMC_SSCFG_CTL_STAT_5_REG	0FA0 8070h	0FA2 8070h
74h	32	MMC_SSCFG_CTL_STAT_6_REG	0FA0 8074h	0FA2 8074h
100h	32	MMC_SSCFG_PHY_CTRL_1_REG	0FA0 8100h	0FA2 8100h

Table 14-30378. MMC_SSCFG Registers, Base Address=0FA0 8000h, Length=1024 (continued)

Offset	Length	Register Name	MMCSD1 Physical Address	MMCSD2 Physical Address
104h	32	MMC_SSCFG_PHY_CTRL_2_REG	0FA0 8104h	0FA2 8104h
108h	32	MMC_SSCFG_PHY_CTRL_3_REG	0FA0 8108h	0FA2 8108h
10Ch	32	MMC_SSCFG_PHY_CTRL_4_REG	0FA0 810Ch	0FA2 810Ch
110h	32	MMC_SSCFG_PHY_CTRL_5_REG	0FA0 8110h	0FA2 8110h
114h	32	MMC_SSCFG_PHY_CTRL_6_REG	0FA0 8114h	0FA2 8114h
130h	32	MMC_SSCFG_PHY_STAT_1_REG	0FA0 8130h	0FA2 8130h
134h	32	MMC_SSCFG_PHY_STAT_2_REG	0FA0 8134h	0FA2 8134h

14.9.4.7.2 MMCSD1/MMCSD2 Registers

MMCSD1/MMCSD2 Registers

14.9.4.7.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

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Table 14-30379. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9000h**
MMCSD2	**0070 A000h**

Figure 14-10065. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-30381. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.9.4.7.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-30382. Instance Table

Instance Name	**Physical Address**
MMCSD1	**0070 9008h**
MMCSD2	**0070 A008h**

Figure 14-10066. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30384. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.4.7.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-30385. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 900Ch**
MMCSD2	**0070 A00Ch**

Figure 14-10067. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-30387. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.4.7.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-30388. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9010h + formula**
MMCSD2	**0070 A010h + formula**

Figure 14-10068. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-30390. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.7.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-30391. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 903Ch**
MMCSD2	**0070 A03Ch**

Figure 14-10069. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-30393. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.7.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-30394. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9040h**
MMCSD2	**0070 A040h**

Figure 14-10070. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-30396. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.7.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-30397. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9080h**
MMCSD2	**0070 A080h**

Figure 14-10071. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-30399. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.7.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-30400. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 90C0h**
MMCSD2	**0070 A0C0h**

Figure 14-10072. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-30402. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.7.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-30403. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 913Ch**
MMCSD2	**0070 A13Ch**

Figure 14-10073. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-30405. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.7.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-30406. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9140h**
MMCSD2	**0070 A140h**

Figure 14-10074. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-30408. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.7.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-30409. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9180h**
MMCSD2	**0070 A180h**

Figure 14-10075. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-30411. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.7.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-30412. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 91C0h**
MMCSD2	**0070 A1C0h**

Figure 14-10076. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-30414. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.7.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-30415. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9200h**
MMCSD2	**0070 A200h**

Figure 14-10077. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-30417. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.4.7.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-30418. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9204h**
MMCSD2	**0070 A204h**

Figure 14-10078. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-30420. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.4.7.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-30421. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9208h**
MMCSD2	**0070 A208h**

Figure 14-10079. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-30423. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.4.7.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-30424. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 920Ch**
MMCSD2	**0070 A20Ch**

Figure 14-10080. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-30426. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.4.7.2.17 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

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Table 14-30427. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9000h**
MMCSD2	**0070 A000h**

Figure 14-10081. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-30429. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.9.4.7.2.18 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-30430. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9008h**
MMCSD2	**0070 A008h**

Figure 14-10082. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-30432. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.4.7.2.19 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-30433. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 900Ch**
MMCSD2	**0070 A00Ch**

Figure 14-10083. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-30435. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.4.7.2.20 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-30436. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9010h + formula**
MMCSD2	**0070 A010h + formula**

Figure 14-10084. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-30438. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.7.2.21 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-30439. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 903Ch**
MMCSD2	**0070 A03Ch**

Figure 14-10085. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30441. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.7.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-30442. Instance Table

Instance Name	**Physical Address**
MMCSD1	**0070 9040h**
MMCSD2	**0070 A040h**

Figure 14-10086. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-30444. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.7.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-30445. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9080h**
MMCSD2	**0070 A080h**

Figure 14-10087. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TXMEM_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30447. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.7.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-30448. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 90C0h**
MMCSD2	**0070 A0C0h**

Figure 14-10088. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TXMEM_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30450. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.7.2.25 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-30451. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 913Ch**
MMCSD2	**0070 A13Ch**

Figure 14-10089. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-30453. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.4.7.2.26 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-30454. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9140h**
MMCSD2	**0070 A140h**

Figure 14-10090. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-30456. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.9.4.7.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-30457. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9180h**
MMCSD2	**0070 A180h**

Figure 14-10091. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-30459. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.9.4.7.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-30460. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 91C0h**
MMCSD2	**0070 A1C0h**

Figure 14-10092. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-30462. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.9.4.7.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-30463. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9200h**
MMCSD2	**0070 A200h**

Figure 14-10093. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-30465. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.4.7.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-30466. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9204h**
MMCSD2	**0070 A204h**

Figure 14-10094. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-30468. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.4.7.2.31 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-30469. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 9208h**
MMCSD2	**0070 A208h**

Figure 14-10095. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-30471. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.4.7.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-30472. Instance Table

Instance Name	Physical Address
MMCSD1	**0070 920Ch**
MMCSD2	**0070 A20Ch**

Figure 14-10096. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-30474. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.4.7.2.33 MMC_CTLCFG_SDMA_SYS_ADDR_LO Register

1 MMC_CTLCFG_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-30475. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0000h**
MMCSD2	**0FA2 0000h**

Figure 14-10097. MMC_CTLCFG_SDMA_SYS_ADDR_LO Name Register

15	14	13	12	11	10	9	8
SDMA_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
SDMA_ADDRESS							
R/W							
0h							

Table 14-30477. MMC_CTLCFG_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	When Host Version 4 Enable is set to 0 in the Host Control 2 register,DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When Host Version 4 Enable is set to 1, SDMA uses ADMA System Address register [05Fh-058h] instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23.[1] SDMA System Address [Host Version 4 Enable = 0] This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Reading this register during SDMA transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data posi- tion can be read from this register. The SDMA transfer waits at the every boundary specified by the SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register [003h] is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. [2] 32-bit Block Count [Host Version 4 Enable = 1] Host Controller Version 4.10 re-defines this register as 32-bit Block Count [Refer to Section 1.15 for more details about block count extension]. In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23. The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero. This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.34 MMC_CTLCFG_SDMA_SYS_ADDR_HI Register

1 MMC_CTLCFG_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-30478. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0002h**
MMCSD2	**0FA2 0002h**

Figure 14-10098. MMC_CTLCFG_SDMA_SYS_ADDR_HI Name Register

15	14	13	12	11	10	9	8
SDMA_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
SDMA_ADDRESS							
R/W							
0h							

Table 14-30480. MMC_CTLCFG_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.35 MMC_CTLCFG_BLOCK_SIZE Register

1 MMC_CTLCFG_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-30481. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0004h**
MMCSD2	**0FA2 0004h**

Figure 14-10099. MMC_CTLCFG_BLOCK_SIZE Name Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W							
0h							

Table 14-30483. MMC_CTLCFG_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_SIZE	R/W	0h	To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. Reset Source: vbus_amod_g_rst_n 0 `4KB` 1 `8KB` 2 `16KB` 3 `32KB` 4 `64KB` 5 `128KB` 6 `256KB` 7 `512KB`
11:0	XFER_BLK_SIZE	R/W	0h	This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing [i.e after a transaction has stopped]. Read operations during transfer return an invalid value and write operations shall be ignored. Reset Source: vbus_amod_g_rst_n 0 `No data transfer` 1 `1 Byte` 2 `2 Bytes` 512 `512 Bytes` 2048 `2048 Bytes`

14.9.4.7.2.36 MMC_CTLCFG_BLOCK_COUNT Register

1 MMC_CTLCFG_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-30484. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0006h**
MMCSD2	**0FA2 0006h**

Figure 14-10100. MMC_CTLCFG_BLOCK_COUNT Name Register

15	14	13	12	11	10	9	8
XFER_BLK_CNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_CNT							
R/W							
0h							

Table 14-30486. MMC_CTLCFG_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	XFER_BLK_CNT	R/W	0h	Host Controller Version 4.10 extends block count to 32-bit [Refer to Section 1.15].Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows: [1] If Host Version 4 Enable in the Host Control 2 register is set to 0 or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected [2] If Host Version 4 Enable is set to 1 and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected.Use of 16-bit/32-bit Block Count register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count.The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred.This register should be accessed only when no transaction is executing [i.e., after transactions are stopped]. During data transfer,read operations on this register may return an invalid value and write operations are ignored. Reset Source: vbus_amod_g_rst_n 0 Stop count 1 1 block 2 2 blocks 3 3 blocks 65535 65535 blocks

14.9.4.7.2.37 MMC_CTLCFG_ARGUMENT1_LO Register

1 MMC_CTLCFG_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

This register contains Lower bits of SD Command Argument

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Table 14-30487. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0008h**
MMCSD2	**0FA2 0008h**

Figure 14-10101. MMC_CTLCFG_ARGUMENT1_LO Name Register

15	14	13	12	11	10	9	8
CMD_ARG1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_ARG1							
R/W							
0h							

Table 14-30489. MMC_CTLCFG_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit23-8 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.38 MMC_CTLCFG_ARGUMENT1_HI Register

1 MMC_CTLCFG_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

This register contains higher bits of SD Command Argument

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Table 14-30490. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 000Ah**
MMCSD2	**0FA2 000Ah**

Figure 14-10102. MMC_CTLCFG_ARGUMENT1_HI Name Register

15	14	13	12	11	10	9	8
CMD_ARG1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMD_ARG1							
R/W							
0h							

Table 14-30492. MMC_CTLCFG_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit39-24 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.39 MMC_CTLCFG_TRANSFER_MODE Register

1 MMC_CTLCFG_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-30493. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 000Ch**
MMCSD2	**0FA2 000Ch**

Figure 14-10103. MMC_CTLCFG_TRANSFER_MODE Name Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	R/W		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-30495. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	NONE	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error,sets this bit to 0 and waits Command Complete Interrupt and then checks the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Command Complete Signal Enable. Reset Source: vbus_amod_g_rst_n 0 Enable Response Interrupt 1 Disable Response Interrupt
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.If Host Driver checks response error, this bit is set to 0 and Response Interrupt Disable is set to 0.If Host Controller checks response error, sets this bit to 1 and sets Response Interrupt Disable to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the Response Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Disable Response Error Check 1 Enable Response Error Check

Table 14-30495. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 .Bit31 OUT_OF_RANGE .Bit30 ADDRESS_ERROR .Bit29 BLOCK_LEN_ERROR .Bit26 WP_VIOLATION .Bit25 CARD_IS_LOCKED .Bit23 COM_CRC_ERROR .Bit21 CARD_ECC_FAILED .Bit20 CC_ERROR .Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE Reset Source: vbus_amod_g_rst_n 0 `Memory` 1 `SDIO`
5	MULTI_BLK_SEL	R/W	0h	This bit enables multiple block data transfers. Reset Source: vbus_amod_g_rst_n 0 `Single Block transfer` 1 `Multiple Block transfer`
4	DATA_XFER_DIR	R/W	0h	This bit defines the direction of data transfers. Reset Source: vbus_amod_g_rst_n 0 `Write from Host to Card` 1 `Read from Card to Host`

Table 14-30495. MMC_CTLCFG_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	AUTO_CMD_ENA	R/W	0h	There are three methods to stop Multiple-block read and write operation. [1] Auto CMD12 Enable: Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 01b, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. When Host Version 4 Enable =0, CMD12 is issued when 16-bit Block Count is expired. When Host Version 4 Enable =1, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired. [2] Auto CMD23 Enable: When this bit field is set to 10b, the Host Controller issues a CMD23 automatically before issuing a command specified in the Command register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. The following conditions are required to use the Auto CMD23. Auto CMD23 Supported [Host Controller Version is 3.00 or later]. A memory card that supports CMD23 [SCR[33]=1]. If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By Writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register.32-bit block count value for CMD23 is set to 32-bit Block Count [SDMA System Address] register. [3] Auto CMD Auto Select [Version 4.10] As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this Auto CMD Auto Select mode. Selection of Auto CMD depends on setting of CMD23 Enable in the Host Control 2 register which indicates whether card supports CMD23. If CMD23 Enable =1, Auto CMD23 is used and if CMD23 Enable =0, Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable. Reset Source: vbus_amod_g_rst_n 0 Auto CMD Disable 1 Auto CMD12 Enable 2 Auto CMD23 Enable 3 Auto CMD Auto Select
1	BLK_CNT_ENA	R/W	0h	This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. Reset Source: vbus_amod_g_rst_n 0 Disable Block count 1 Enable Block count
0	DMA_ENA	R/W	0h	DMA can be enabled only if DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register [00Fh]. Reset Source: vbus_amod_g_rst_n 0 DMA mode is Disabled 1 DMA mode is Enabled

14.9.4.7.2.40 MMC_CTLCFG_COMMAND Register

1 MMC_CTLCFG_COMMAND Register (Offset = Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-30496. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 000Eh**
MMCSD2	**0FA2 000Eh**

Figure 14-10104. MMC_CTLCFG_COMMAND Name Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W		R/W	R/W	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	

Table 14-30498. MMC_CTLCFG_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	NONE	0h	Reserved
13:8	CMD_INDEX	R/W	0h	This bit shall be set to the command number [CMD0-63, ACMD0-63]. Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	There are three types of special commands. Suspend, Resume andAbort. These bits shall bet set to 00b for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting Continue Request in the Block Gap Control Register. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. Abort Command: If this command is set when exe- cuting a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a writetransfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. Reset Source: vbus_amod_g_rst_n 0 Normal 1 Suspend 2 Resume 3 Abort

Table 14-30498. MMC_CTLCFG_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line [ex. CMD52]. 2. Commands with no data transferbut using busy signal on DAT[0]line [R1b or R5b ex. CMD38]. 3. Resume Command. Reset Source: vbus_amod_g_rst_n 0 `Data not Present` 1 `Data present`
4	CMD_INDEX_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. Reset Source: vbus_amod_g_rst_n 0 `Disable Command Index Check` 1 `Enable Command Index Check`
3	CMD_CRC_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. Reset Source: vbus_amod_g_rst_n 0 `Disable Command CRC Check` 1 `Enable Command CRC Check`
2	SUB_CMD	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17]. When issuing a main command, this bit is set to 0 and when issuing a sub command, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register.Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command. Reset Source: vbus_amod_g_rst_n 0 `Main Command` 1 `Sub Command`
1:0	RESP_TYPE_SEL	R/W	0h	Response Type Select. Reset Source: vbus_amod_g_rst_n 0 `No Response` 1 `Response length 136` 2 `Response length 48` 3 `Response length 48 check Busy after response`

14.9.4.7.2.41 MMC_CTLCFG_RESPONSE_j Register

1 MMC_CTLCFG_RESPONSE_j Register (Offset = 10h + formula) [reset = 0h]

This register is used to store responses from SD Cards

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Offset = 10h + (j * 2h); where j = 0 to 7d

Table 14-30499. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0010h + formula**
MMCSD2	**0FA2 0010h + formula**

Figure 14-10105. MMC_CTLCFG_RESPONSE_j Name Register

15	14	13	12	11	10	9	8
CMD_RESP							
R							
0h							
7	6	5	4	3	2	1	0
CMD_RESP							
R							
0h							

Table 14-30501. MMC_CTLCFG_RESPONSE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_RESP	R	0h	R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.42 MMC_CTLCFG_DATA_PORT Register

1 MMC_CTLCFG_DATA_PORT Register (Offset = 20h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30502. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0020h**
MMCSD2	**0FA2 0020h**

Figure 14-10106. MMC_CTLCFG_DATA_PORT Name Register

31	30	29	28	27	26	25	24
BUF_RD_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
BUF_RD_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
BUF_RD_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
BUF_RD_DATA							
R/W							
0h							

Table 14-30504. MMC_CTLCFG_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUF_RD_DATA	R/W	0h	The Host Controller Buffer can be accessed through this 32-bit Data Port Register. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.43 MMC_CTLCFG_PRESENTSTATE Register

1 MMC_CTLCFG_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

The Host Driver can get status of the Host Controller from this 32-bit read-only register

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Table 14-30505. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0024h**
MMCSD2	**0FA2 0024h**

Figure 14-10107. MMC_CTLCFG_PRESENTSTATE Name Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISS_BY_ERR	RESERVED		SDIF_CMDIN
R	R	R	R	R	NONE		R
0h	0h	0h	0h	0h	0h		1h
23	22	21	20	19	18	17	16
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R	R	R	R	R	R	R	R
1h	1h	1h	1h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 regis-ter. UHS-II interface initialization is activated by setting SD Clock Enable in the Clock Control reg-ister. Host Controller drives STB.L on D0 lanefrom EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1 if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when Reading this status [Refer to Figure 3-35 about details of this method]. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200us period from set- ting SD Clock Enable until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Inter-face Enable is set to 0 or Host full reset is exe-cuted. '0' UHS-II IF is not detected '1' UHS-II IF is detected Reset Source: vbus_amod_g_rst_n

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

30	UHS2_IF_LANE_SYNC	R	0h	This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On detecting UHS-II Interface [D31=1], Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller pro-vides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane.
				In case of Version 4.00, this bit indicates comple-tion of Device PHY Initialization by detecting LIDL LSS on D1 lane.From Version 4.10, Host Controller may imple-ment a specific PHY verification method and PHY
				Initialization Failure can be indicated by keeping this bit to 0
				even LIDL LSS is detected on D1 lane.Host Driver detects PHY Initialization Failure by timeout.This bit is cleared by when D0 lane is set to EIDL,UHS-II Interface Enable is set to 0 or executes Host full reset.
				Reset Source: vbus_amod_g_rst_n
				`0 UHS-II PHY is not initialized`
				`1 UHS-II PHY is initialized`

29	UHS2_DORMANT	R	0h	This status indicates whether UHS-II lanes enterDormant state. This function is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On issuing GO_DORMAT_STATE com-mand, Go Dormant Command [111b]; is set to Command type in the UHS-II Command register.This command type acts as a trigger to enterlanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiv-ing STB.H and EIDL on D1 lane. This bit is set to 1 after the time of T_DMT_ENTRY [750 RCLK cycle] or more from detecting EIDL on D1 lane.
				RCLK may be stopped in dormant state, by setting SD Clock Enable to 0 in the Clock Control register while In Dormant State bit is set to 1. On WritingClock Control register with setting SD Clock Enable to 1, Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0. In case of the card enters Hibernate Mode [RCLK is stopped], Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the Power Control register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0 or executesHost full reset.
				Reset Source: vbus_amod_g_rst_n
				`0 Not in DORMANT state`
				`1 In DORMANT state`

28	SUB_COMMAND_STS	R	0h	The Command register and Response register are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the Error Interrupt Status register or in the UHS-II Error Interrupt Status register. Refer to Section 1.17 about details of response error statuses. Just before Reading of this register, the Sub Command Flag of the Command register or the UHS-II Command register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error [D27 of this register] or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the Auto CMD Error Status register. 1 - Sub Command Status 0 - Main Command Status Reset Source: vbus_amod_g_rst_n

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMD_NOT_ISS_BY_ERR	R	0h	Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error. [Equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the Auto CMD Error Status register.] This status is set to 1 when Host Controller cannot issue a command after setting Command register or UHS-II Command register.Refer to Section 3.10 about 2L-HD error case inUHS-II mode.Sub Command Status [D28] indicates which command is not issued [main or sub]. 1 - Command cannot be issued 0 - No error for issuing a command Reset Source: vbus_amod_g_rst_n
26:25	RESERVED	NONE	0h	Reserved
24	SDIF_CMDIN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
23	SDIF_DAT3IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3]. Reset Source: vbus_amod_g_rst_n
22	SDIF_DAT2IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2]. Reset Source: vbus_amod_g_rst_n
21	SDIF_DAT1IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1]. Reset Source: vbus_amod_g_rst_n
20	SDIF_DAT0IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. Reset Source: vbus_amod_g_rst_n

19	WRITE_PROTECT	R	0h	The Write Protect Switch is supported for memory and combo cards.This bit reflects the SDWP# pin.
				Reset Source: vbus_amod_g_rst_n
				`0 Write protected (SDWP# = 1)`
				`1 Write enabled (SDWP# = 0)`

18	CARD_DETECT	R	0h	This bit reflects the inverse value of the SDCD# pin. '0' No Card present [SDCD# = 1] '1' Card present [SDCD# = 0] Reset Source: vbus_amod_g_rst_n
17	CARD_STATE_STABLE	R	0h	This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1,it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. '0' Reset of Debouncing '1' No Card or Inserted Reset Source: vbus_amod_g_rst_n

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CARD_INSERTED	R	0h	This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SD Bus Power in the Power Control register and SD Clock Enable in the Clock control register. In addition the HD should clear the HC by the Software Reset For All in Software register. The card detect is active regardless of the SD Bus Power. '0' Reset or Debouncing or No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	BUF_RD_ENA	R	0h	This status is used for non-DMA read transfers.This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. Reset Source: vbus_amod_g_rst_n 0 `Read Disable` 1 `Read Enable`
10	BUF_WR_ENA	R	0h	This status is used for non-DMA write transfers.This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. Reset Source: vbus_amod_g_rst_n 0 `Write Disable` 1 `Write Enable`
9	RD_XFER_ACTIVE	R	0h	This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: After the end bit of the read command. When Writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: When the last data block as specified by block length is transferred to the system. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. '0' No valid data '1' Transferring data Reset Source: vbus_amod_g_rst_n 0 `No valid data` 1 `Transferring data`

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WR_XFER_ACTIVE	R	0h	This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: After the end bit of the write command. When Writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count [Single or Multiple] After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. Reset Source: vbus_amod_g_rst_n 0 No valid data 1 Transferring data
7	SDIF_DAT7IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
6	SDIF_DAT6IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
5	SDIF_DAT5IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
4	SDIF_DAT4IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
3	RETUNING_REQ	R	0h	Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 [using fixed sampling clock]. Reset Source: vbus_amod_g_rst_n 0 Fixed or well tuned sampling clock 1 Sampling clock needs re-tuning
2	DATA_LINE_ACTIVE	R	0h	This bit indicates whether one of the DAT line on SD bus is in use. Reset Source: vbus_amod_g_rst_n 0 DAT line inactive 1 DAT line active

Table 14-30507. MMC_CTLCFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INHIBIT_DAT	R	0h	This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit [DAT] [ex. R1b, R5b type]. Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. '0' Can issue command which uses the DAT line '1' Cannot issue command which uses the DATline Reset Source: vbus_amod_g_rst_n
0	INHIBIT_CMD	R	0h	SD Mode If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register [00Fh] is written. This bit is cleared when the command response is received. Even if the Command Inhibit [DAT] is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 gener- ates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issuethe command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Com- mand Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 opera- tion, Host Controller shall manage to issue two commands: CMD12 and a command set by Com-mand register. UHS-II Mode This bit is 0 means that a command packet can be issued by the Host Controller. While this bit is set to 1, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from UHS-II BlockSize [Offset 080h] to the UHS-II Command [Offset 09Eh]. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status-register. 1- Host Controller is not ready to issue a com-mand 0 - Host Controller is ready to issue a command Version 4.10 adds a new control to prevent error statuses from overWriting by receipt of a next com-mand. This status keeps indicating 1 while any of response error statuses is set to 1 [as described in Section 1.17], Command Not Issued by Error in this register is set to 1 or Command Not Issued by Auto CMD12 Error in the Auto CMD Error Status register is set to 1. Software Reset For CMD Lineis used to clear the error statuses above and this status. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.44 MMC_CTLCFG_HOST_CONTROL1 Register

1 MMC_CTLCFG_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

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Table 14-30508. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0028h**
MMCSD2	**0FA2 0028h**

Figure 14-10108. MMC_CTLCFG_HOST_CONTROL1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT		HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-30510. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	This bit selects source for card detection. '0' SDCD# is selected [for normal use] '1' The card detect test level is selected Reset Source: vbus_amod_g_rst_n
6	CD_TEST_LEVEL	R/W	0h	This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates [card ins or card removal] interrupt when the normal int sts enable bit is set. '0' No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
5	EXT_DATA_WIDTH	R/W	0h	This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.This bit is not effective when multiple devices are installed on a bus slot [Slot Type is set to 10b in the Capabilities register]. In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register. Reset Source: vbus_amod_g_rst_n 0 `Bus width is selected by data transfer width` 1 `8-bit bus width`

Table 14-30510. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	DMA_SELECT	R/W	0h	This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the Capabilities register. Selected DMA is enabled by DMA Enable of the Transfer Mode register in SD mode and DMA Enable of UHS-II Transfer Mode register in UHS-II mode. [1] Up to Version 3.00 When Host Version 4 Enable is set to 0, setting of this field is compatible to Host Controller Version 3.00.SDMA is initiated by Writing to the Command register when this field is set to 00b and the SDMA System Address regis-ter [32-bit] is used. SDMA does not support 64-bit address-ing.ADMA2 is initiated by Writing to the Command register when this field is set to 10b or 11b. Lower 32-bit of the ADMA Sys-tem Address register is used when this field is set to 10b and 64-bit of the ADMA System Address register is used when this field is set to 11b. Support of 64-bit System Addressing is indicated by 64-bit System Address Support for V3 in the Capabilities register. 64-bit AMDA2 uses 96-bit Descriptor. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 -32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected [Optional] [2] Version 4.00 or later When Host Version 4 Enable is set to 1, setting of this field is changed as follows. SDMA is initiated by Host Driver writes to the Command reg-ister when this field is set to 00b.ADMA2 is initiated by Host Driver writes to the Command register when this field is set to 10b or 11b and by ADMA3 sets to the ADMA System Address register when this field is set to 11b. ADMA3 is initiated by Host Driver writes to the ADMA3 IDAddress register when this field is set to 11b. 00 - SDMA is selected 01 - Not Used [New assignment is not allowed] 10 - ADMA2 is selected [AMDA3 is not supported or dis-abled] 11 - ADMA2 or ADMA3 is selected Support of 64-bit DMA and 128-bit Descriptor is indicated by 64-bit System Address Support for V4 in the Capabilities register. If the support bit is set to 1, all supported DMAs [depends on Support, ADMA2 Support and ADMA3 Sup-port] shall support 64-bit addressing. 64-bit Addressing in the Host Controller 2 register selects either 32-bit or 64-bit system addressing of DMAs. Reset Source: vbus_amod_g_rst_n
2	HIGH_SPEED_ENA	R/W	0h	This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 [default], the HC outputs CMD line and DAT lines at the falling edge of the SD clock [up to 25 MHz/20MHz for MMC]. If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock [up to 50 MHz for SD/52MHz for MMC]/ 208Mhz [for SD3.0] If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode. Reset Source: vbus_amod_g_rst_n 0 Normal Speed Mode 1 High Speed Mode
1	DATA_WIDTH	R/W	0h	This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode. Reset Source: vbus_amod_g_rst_n 0 1 bit mode 1 4 bit mode

Table 14-30510. MMC_CTLCFG_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LED_CONTROL	R/W	0h	This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. Reset Source: vbus_amod_g_rst_n 0 `LED off` 1 `LED on`

14.9.4.7.2.45 MMC_CTLCFG_POWER_CONTROL Register

1 MMC_CTLCFG_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

This register is used to program the SD Bus power and voltage level

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Table 14-30511. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0029h**
MMCSD2	**0FA2 0029h**

Figure 14-10109. MMC_CTLCFG_POWER_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-30513. MMC_CTLCFG_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	UHS2_VOLTAGE	R/W	0h	This field determines supply voltage range to VDD2. This field can be set to 101b if 1.8V VDD2 Support in the Capabilities register is set to 1. '000' VDD2 Not supported '001'- '011' Reserved '100' Reserved for 1.2V '101' 1.8V '110' Not Used '111' Not Used Reset Source: vbus_amod_g_rst_n
4	UHS2_POWER	R/W	0h	Setting this bit enables providing VDD2. '0' Power Off '1' Power On Reset Source: vbus_amod_g_rst_n 0 Power Off 1 Power On
3:1	SD_BUS_VOLTAGE	R/W	0h	By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. '000'- '100' Reserved '101' 1.8V '110' 3.0V '111' 3.3V Reset Source: vbus_amod_g_rst_n 0 Reserved 5 1.8V 6 3.0V 7 3.3V

Table 14-30513. MMC_CTLCFG_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Control-ler should immediately stop driving CMD and DAT[3:0] [tri-state], and drive SDCLK to low level [Refer to Section 2.2.14]. If card is connectedto Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1.In UHS-II mode, before clearing this bit, Host Driver shall clear SD Clock Enable and before stopping to sup-ply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt. Reset Source: vbus_amod_g_rst_n 0 Power Off 1 Power On

14.9.4.7.2.46 MMC_CTLCFG_BLOCK_GAP_CONTROL Register

1 MMC_CTLCFG_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

This register is used to program the block gap request, read wait control and interrupt at block gap

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Table 14-30514. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 002Ah**
MMCSD2	**0FA2 002Ah**

Figure 14-10110. MMC_CTLCFG_BLOCK_GAP_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	SPI_MODE	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h

Table 14-30516. MMC_CTLCFG_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	To check for the boot acknowledge in boot operation. Reset Source: vbus_amod_g_rst_n 0 Will not wait for boot ack from eMMC card 1 Wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	To start boot code access in alternative mode. Reset Source: vbus_amod_g_rst_n 0 To stop alternative boot code access 1 To start alternative boot code access
5	BOOT_ENABLE	R/W	0h	To start boot code access. Reset Source: vbus_amod_g_rst_n 0 To stop boot code access 1 To start boot code access
4	SPI_MODE	R/W	0h	SPI mode enable bit. Reset Source: vbus_amod_g_rst_n 0 SD Mode 1 SPI Mode
3	INTRPT_AT_BLK_GAP	R/W	0h	This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. Reset Source: vbus_amod_g_rst_n

Table 14-30516. MMC_CTLCFG_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported. In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card. Reset Source: vbus_amod_g_rst_n 0 `Disable Read-Wait Control` 1 `Enable Read-Wait Control`
1	CONTINUE	R/W	0h	This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The Host Controller automatically clears this bit when the transaction re-starts. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. In SD mode, this bit is cleared in either of the following cases: [1] In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. [2] In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. '0' Ignore '1' Restart Reset Source: vbus_amod_g_rst_n 0 `Ignore` 1 `Restart`
0	STOP_AT_BLK_GAP	R/W	0h	This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit [DAT] in the Present State register. In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst [Flow Control basis]. Host Control-ler waits for sending Flow Control MSG until Continue Request is set to 1. '0' Transfer '1' Stop Reset Source: vbus_amod_g_rst_n 0 `Transfer` 1 `Stop`

14.9.4.7.2.47 MMC_CTLCFG_WAKEUP_CONTROL Register

1 MMC_CTLCFG_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

This register is used to program the wakeup functionality

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Table 14-30517. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 002Bh**
MMCSD2	**0FA2 002Bh**

Figure 14-10111. MMC_CTLCFG_WAKEUP_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-30519. MMC_CTLCFG_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	CARD_REMOVAL	R/W	0h	This bit enables wakeup event via Card removal assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card removal
1	CARD_INSERTION	R/W	0h	This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card Insertion
0	CARD_INTERRUPT	R/W	0h	This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.This bit can be set to 1 if FN_WUS [Wake Up Support] in CIS is set to 1. Reset Source: vbus_amod_g_rst_n 0 Disable wakeup event 1 Enable wakeup event via Card Interrupt

14.9.4.7.2.48 MMC_CTLCFG_CLOCK_CONTROL Register

1 MMC_CTLCFG_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

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Table 14-30520. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 002Ch**
MMCSD2	**0FA2 002Ch**

Figure 14-10112. MMC_CTLCFG_CLOCK_CONTROL Name Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W							
0h							

7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS		CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA
R/W		R/W	NONE	R/W	R/W	R	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-30522. MMC_CTLCFG_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SDCLK_FRQSEL	R/W	0h	This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. [1] 8-bit Divided Clock Mode 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock[10MHz-63MHz] Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. [1] 25 MHz divider value. [2] 400 KHz divider value. The frequency of the SDCLK is set by the following formula: Clock Frequency = [Baseclock] / divisor. Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. Maximum Frequency for SD = 50Mhz [base clock] Maximum Frequency for MMC = 52Mhz [base clock] Minimum Frequency = 195.3125Khz [50Mhz / 256], same calculation for MMC also. [2] 10-bit Divided Clock Mode Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to10 bits and all divider values shall be supported. 3FFh --1/2046 Divided Clock N -------1/2N Divided Clock [Duty 50%] 002h -- 1/4 Divided Clock 001h ---1/2 Divided Clock 000h --- Base Clock [10MHz-254MHz] Reset Source: vbus_amod_g_rst_n
7:6	SDCLK_FRQSEL_UPBITS	R/W	0h	Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select. Reset Source: vbus_amod_g_rst_n
5	CLKGEN_SEL	R/W	0h	This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported [non-zero value is set to Clock Multiplier in the Capabilities register], this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. '0' Divided Clock Mode '1' Programmable Clock Mode Reset Source: vbus_amod_g_rst_n 0 Divided Clock Mode 1 Programmable Clock Mode
4	RESERVED	NONE	0h	Reserved

Table 14-30522. MMC_CTLCFG_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL_ENA	R/W	0h	This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable and PLL Enable and to minimize output latency [ex. SDCLK/RCLK, D0lane] from SD Clock Enable. There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable. [1] When Host Version 4 Enable =0 [Host Driver Version 3, which does not support this bit] or this bit is not implemented,Internal Clock Enable [or SD Clock Enable] may activate PLL [exit low power mode and start locking clock]. [2] When Host Version 4 Enable =1 [Host Driver Version 4],Internal Clock Enable is set before setting this bit and then setting this bit may activate PLL [exit low power mode and start locking clock]. Reset Source: vbus_amod_g_rst_n 0 `PLL is in low power mode` 1 `PLL is enabled`
2	SD_CLK_ENA	R/W	0h	The HC shall stop SDCLK when Writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until SDCLK is stopped [Stop at SDCLK = 0]. If the HC detects the No Card state, this bit shall be cleared. Reset Source: vbus_amod_g_rst_n 0 `Disable providing SDCLK` 1 `Enable providing SDCLK`
1	INT_CLK_STABLE	R	0h	This bit is set to 1 when SD clock is stable after Writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. Note: This is useful when using PLL for a clock oscillator that requires setup time. Reset Source: vbus_amod_g_rst_n 0 `Not Ready` 1 `Ready`
0	INT_CLK_ENA	R/W	0h	This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. Reset Source: vbus_amod_g_rst_n 0 `Stop` 1 `Oscillate`

14.9.4.7.2.49 MMC_CTLCFG_TIMEOUT_CONTROL Register

1 MMC_CTLCFG_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

The register sets the Data Timeout counter value

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Table 14-30523. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 002Eh**
MMCSD2	**0FA2 002Eh**

Figure 14-10113. MMC_CTLCFG_TIMEOUT_CONTROL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
NONE				R/W			
0h				0h			

Table 14-30525. MMC_CTLCFG_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE	0h	Reserved
3:0	COUNTER_VALUE	R/W	0h	This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sdclockTMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable [in the Error Interrupt Status Enable register]. 1111 - Reserved 1110 - TMCLK * 2^27 -------------------- -------------------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13 Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.50 MMC_CTLCFG_SOFTWARE_RESET Register

1 MMC_CTLCFG_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

This register is used to program the software reset for data, command and for all

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Table 14-30526. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 002Fh**
MMCSD2	**0FA2 002Fh**

Figure 14-10114. MMC_CTLCFG_SOFTWARE_RESET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_DAT	SWRST_FOR_CMD	SWRST_FOR_ALL
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-30528. MMC_CTLCFG_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	SWRST_FOR_DAT	R/W	0h	Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register: Buffer is cleared and Initialized. Present State register: Buffer read Enable, Buffer write Enable, Read Transfer Active, Write Transfer Active, DAT Line Active, Command Inhibit [DAT]. Block Gap Control register: Continue Request, Stop At Block Gap Request. Normal Interrupt Status register: Buffer Read Ready, Buffer Write Ready, Block Gap Event, Transfer Complete. Reset Source: vbus_amod_g_rst_n 0 Work 1 Reset
1	SWRST_FOR_CMD	R/W	0h	Software Reset For CMD Line Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit [including response error statuses related to Com-mand Inhibit [CMD] control] and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub com- mand response errors. The following registers and bits are cleared by this bit: Present State register Command Inhibit [CMD] Normal Interrupt Status register Command Complete Error Interrupt Status [from Version 4.10] Response error statuses related to Com-mand Inhibit [CMD] Reset Source: vbus_amod_g_rst_n 0 Work 1 Reset

Table 14-30528. MMC_CTLCFG_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SWRST_FOR_ALL	R/W	0h	This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. Reset Source: vbus_amod_g_rst_n 0 `Work` 1 `Reset`

14.9.4.7.2.51 MMC_CTLCFG_NORMAL_INTR_STS Register

1 MMC_CTLCFG_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

This register gives the status of all the interrupts

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Table 14-30529. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0030h**
MMCSD2	**0FA2 0030h**

Figure 14-10115. MMC_CTLCFG_NORMAL_INTR_STS Name Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R	R/W1TC	R/W1TC	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description

15	ERROR_INTR	R	0h	If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first.
				In UHS-II mode is enabled, if any of the bits in the UHS-II Error Interrupt Status register are set, this bit is also set.
				'0' No error
				'1' Error
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Error interrupt is generated`

14	BOOT_COMPLETE	R/W1TC	0h	This status is set if the boot operation gets terminated.
				'0' Boot operation is not terminated
				'1' Boot operation is terminated
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Boot Terminate interrupt is generated`

13	RCV_BOOT_ACK	R/W1TC	0h	This status is set if the boot acknowledge is received from device.
				'0' Boot ack not recieved
				'1' Boot ack is recieved
				Reset Source: vbus_amod_g_rst_n
				`0 No Interrupt`
				`1 Boot acknowledge is received`

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RETUNING_EVENT	R	0h	This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer [not large block count] can be completed without re-tuning.In UHS-II mode, this bit is not effective '0' Re-tuning not required '1' Re-tuning should be performed Reset Source: vbus_amod_g_rst_n
11	INTC	R	0h	This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Reset Source: vbus_amod_g_rst_n
10	INTB	R	0h	This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Reset Source: vbus_amod_g_rst_n
9	INTA	R	0h	This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. NOTE : INT_A, INT_B, and INT_C are to be implemented based on the Application Requirements. By default these are not implemented as there is no specific requirement from Customers. Reset Source: vbus_amod_g_rst_n

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTR	R	0h	When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt status latched in the Host Controller and to stop driv-ing the interrupt signal to the Host System.After completion of the card interrupt service [It should reset interrupt factors in the SD card and the interrupt signal may not be asserted],set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt fac-tor. [1] DAT[1] Interrupt Input in SD Mode In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt sig-nal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the inter-rupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is sta-ble. [2] DAT[2] Interrupt Input in UHS-II Mode When Card Inserted in the Present State reg-ister and SD Bus Power for VDD1 in the Power Control register are set to 1, Host Con-troller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3V signal level. DAT[2] interrupt is masked by setting Card Interrupt Status Enable to 0 in the Normal Interrupt register.When either Card Inserted or SD Bus Power for VDD1 is set to 0, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card. [3] INT MSG in UHS-II Mode INT MSG is enabled by setting INT MSG Enable in the UHS-II Device Select register. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the UHS-II Device Interrupt Status regis- ter is set to 1, INT MSG interrupt is generated. INT MSG interrupt is cleared by Writing a cor-respondent bit to 1 in the UHS-II Device Inter-rupt Status register. Masking DAT[2] interrupt also disables INT MSG interupt due to Card Interrupt Status Enable is set to 0. SDIO Ver-sion 4.00 does not support INT MSG. '0' No Card Interrupt '1' Generate Card Interrupt Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Card interrupt is generated
7	CARD_REM	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Removed Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Card removal interrupt is generated

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CARD_INS	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 0 to 1.When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Inserted Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Card insertion interrupt is generated
5	BUF_RD_READY	R/W1TC	0h	This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to read buffer, '1' Ready to read buffer Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Buffer Read Ready interrupt is generated
4	BUF_WR_READY	R/W1TC	0h	This status is set if the Buffer Write Enable changes from 0 to 1.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to write to buffer, '1' Ready to write to buffer Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Buffer Write Ready interrupt is generated
3	DMA_INTERRUPT	R/W1TC	0h	This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser. '0' No DMA Interrupt '1' DMA Interrupt is generated Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 DMA interrupt is generated
2	BLK_GAP_EVENT	R/W1TC	0h	If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status [When the transaction is stopped at SD Bus timing. The Read Wait must be supported inorder to use this function]. Write Transaction: This bit is set at the falling edge of Write Transfer Active Status [After getting CRC status at SD Bus timing]. In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' No Block Gap Event '1' Transaction stopped at Block Gap Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Block Gap Event is generated

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1TC	0h	This bit is set when a read / write transaction is completed. SD Mode Read Transaction: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length [After the last data has been read to the Host Sys- tem]. The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control Register [After valid data has been read to the Host System]. Write Transaction: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control Register and data transfers completed. [After valid data is written to the SD card and the busy signal is released]. Note: Transfer Complete has higher priority than Data Time-out Error. If both bits are set to 1, the data transfer can be considered complete. Note: While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1 Command with Busy: This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit[DAT] in the Present State register.UHS-I mode While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1. '0' No Data Transfer Complete, '1' Data Transfer Complete UHS-II Mode This interrupt is generated in following twocases: [a] EBSY Completion [for EBSY supported commands] When EBSY Wait in the UHS-II Transfer Mode register is set to 1, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation. [b] Stop and Continue during DCMD Data Transfer When Stop At Block Gap Request in the Block Gap Control register is set to 1 and data transfer is stopped at the Flow Control. Following is for both SD mode and UHS-II mode. The table below shows that Transfer Com-plete has higher priority than Data Timeout Error. If both bits are set to 1, execution of a command can be considered to be completed. 1 - Command execution is completed 0 - Not complete Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Transfer complete interrupt is generated

Table 14-30531. MMC_CTLCFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_COMPLETE	R/W1TC	0h	SD Mode This bit is set when we get the end bit of the command response [Except Auto CMD12 and Auto CMD23] Note: Command Time-out Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. Version 4.00 defines response check function for R1 and R5. If Response Interrupt Disable in the Transfer Mode register is set to 1, gen-eration of this interrupt is prohibited regardless of Command Complete Signal Enable. UHS-II Mode If Response Interrupt Disable is set to 0 in the UHS-II Transfer Mode register, this interrupt is generated when response packet is received.If Response Interrupt Disable is set to 1 in the UHS-II Transfer Mode register, generation of this interrupt is prohibited regardless of Com-mand Complete Signal Enable. '0' No Command Complete, '1' Command Complete Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Command complete interrupt is generated`

14.9.4.7.2.52 MMC_CTLCFG_ERROR_INTR_STS Register

1 MMC_CTLCFG_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

This register gives the status of the error interrupts

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Table 14-30532. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0032h**
MMCSD2	**0FA2 0032h**

Figure 14-10116. MMC_CTLCFG_ERROR_INTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30534. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	R/W1TC	0h	Occurs when detecting ERROR in m_hresp[dma transaction] Reset Source: vbus_amod_g_rst_n 0 No Error 1 Host Error
11	RESP	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1.If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Response Error
10	TUNING	R/W1TC	0h	This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure [Occurrence of an error during tuning procedure is indicated by Sampling Select]. By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning.To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Turning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Tuning Error

Table 14-30534. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADMA	R/W1TC	0h	This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `ADMA Error`
8	AUTO_CMD	R/W1TC	0h	Auto CMD12 and Auto CMD23 use this error status.This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared with clearing of this bit [another implementation is also allowed]. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Auto CMD Error`
7	CURR_LIMIT	R/W1TC	0h	By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Power Fail`
6	DATA_ENDBIT	R/W1TC	0h	Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data Endbit Error`
5	DATA_CRC	R/W1TC	0h	Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data CRC Error`
4	DATA_TIMEOUT	R/W1TC	0h	Occurs when detecting one of following timeout conditions: 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Data Timeout Error`
3	CMD_INDEX	R/W1TC	0h	Occurs if a Command Index error occurs in the Command Response. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command Index Error`

Table 14-30534. MMC_CTLCFG_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CMD_ENDBIT	R/W1TC	0h	Occurs when detecting that the end bit of a command response is 0. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command End bit Error`
1	CMD_CRC	R/W1TC	0h	Command CRC Error is generated in two cases. 1. If a response is returned and the Command Time-out Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command [Stop driving CMD line] and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command CRC Error`
0	CMD_TIMEOUT	R/W1TC	0h	Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Command Timeout Error`

14.9.4.7.2.53 MMC_CTLCFG_NORMAL_INTR_STS_ENA Register

1 MMC_CTLCFG_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

This register is used to enable the normal interrupt status register fields

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Table 14-30535. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0034h**
MMCSD2	**0FA2 0034h**

Figure 14-10117. MMC_CTLCFG_NORMAL_INTR_STS_ENA Name Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30537. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HC shall control error Interrupts using the Error Interrupt Status Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
12	RETUNING_EVENT	R/W	0h	0 - Masked 1 - Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	INTC	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30537. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
9	INTA	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
8	CARD_INTERRUPT	R/W	0h	If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. By setting this bit to 0, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state [ex. floating]. Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
3	DMA_INTERRUPT	R/W	0h	'0' Masked, '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

Table 14-30537. MMC_CTLCFG_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

14.9.4.7.2.54 MMC_CTLCFG_ERROR_INTR_STS_ENA Register

1 MMC_CTLCFG_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

This register is used to enable the Error Interrupt Status register fields

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Table 14-30538. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0036h**
MMCSD2	**0FA2 0036h**

Figure 14-10118. MMC_CTLCFG_ERROR_INTR_STS_ENA Name Register

15	14	13	12	11	10	9	8
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30540. MMC_CTLCFG_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
11	RESP	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
10	TUNING	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
9	ADMA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

Table 14-30540. MMC_CTLCFG_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

14.9.4.7.2.55 MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register

1 MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

This register is used to enable the Normal Interrupt Signal register

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Table 14-30541. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0038h**
MMCSD2	**0FA2 0038h**

Figure 14-10119. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Name Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30543. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HD shall control error Interrupts using the Error Interrupt Signal Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
12	RETUNING_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	INTC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30543. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
9	INTA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
8	CARD_INTERRUPT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
3	DMA_INTERRUPT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30543. MMC_CTLCFG_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 `Masked` 1 `Enabled`

14.9.4.7.2.56 MMC_CTLCFG_ERROR_INTR_SIG_ENA Register

1 MMC_CTLCFG_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

This register is used to enable Error Interrupt Signal register

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Table 14-30544. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 003Ah**
MMCSD2	**0FA2 003Ah**

Figure 14-10120. MMC_CTLCFG_ERROR_INTR_SIG_ENA Name Register

15	14	13	12	11	10	9	8
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30546. MMC_CTLCFG_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
11	RESP	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
10	TUNING	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
9	ADMA	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

Table 14-30546. MMC_CTLCFG_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled Reset Source: vbus_amod_g_rst_n 0 Masked 1 Enabled

14.9.4.7.2.57 MMC_CTLCFG_AUTOCMD_ERR_STS Register

1 MMC_CTLCFG_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

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Table 14-30547. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 003Ch**
MMCSD2	**0FA2 003Ch**

Figure 14-10121. MMC_CTLCFG_AUTOCMD_ERR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
CMD_NOT_ISSUED	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R	NONE	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30549. MMC_CTLCFG_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved

7	CMD_NOT_ISSUED	R	0h	Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error [D04- D01] in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Not Issued`

6	RESERVED	NONE	0h	Reserved

5	RESP	R	0h	This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or Auto CMD23. This status should be ignored if any bit of D00 to D04 is set to 1.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Auto Command Response Error`

4	INDEX	R	0h	Occurs if the Command Index error occurs in response to a command.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Auto Command Index Error`

3	ENDBIT	R	0h	Occurs when detecting that the end bit of command response is 0.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Auto Command End Bit Error`

Table 14-30549. MMC_CTLCFG_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CRC	R	0h	Occurs when detecting a CRC error in the command response. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Auto Command CRC Error
1	TIMEOUT	R	0h	Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.If this bit is set to 1, the other error status bits [D04 - D02] are meaningless. Reset Source: vbus_amod_g_rst_n 0 No Error 1 Auto Command Timeout Error
0	ACMD12_NOT_EXEC	R	0h	If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits [D04 - D01] are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 Reset Source: vbus_amod_g_rst_n 0 No Error 1 Not Executed

14.9.4.7.2.58 MMC_CTLCFG_HOST_CONTROL2 Register

1 MMC_CTLCFG_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

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Table 14-30550. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 003Eh**
MMCSD2	**0FA2 003Eh**

Figure 14-10122. MMC_CTLCFG_HOST_CONTROL2 Name Register

15	14	13	12	11	10	9	8
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPLING_CLK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1		V1P8_SIGNAL_ENA	UHS_MODE_SELECT		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		

Table 14-30552. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers. Reset Source: vbus_amod_g_rst_n 0 SDCLK and Driver Strength are controlled by Host Driver 1 Automatic Selection by Preset Value are Enabled
14	ASYNCH_INTR_ENA	R/W	0h	This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode [and zero is set to Interrupt Pin Select in the Shared Bus Control register]. If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. Reset Source: vbus_amod_g_rst_n 0 Asynchronous Interrupt disabled 1 Asynchronous Interrupt enabled

Table 14-30552. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	BIT64_ADDRESSING	R/W	0h	This field is effective when Host Version 4.00 Enable is set to 1. Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the Capabilities register. . Reset Source: vbus_amod_g_rst_n 0 32 bit addressing 1 64 bit addressing
12	HOST_VER40_ENA	R/W	0h	This bit selects either Version 3.00 compatible mode or Ver4.mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit. In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified. SDMA Address SDMA uses ADMA System Address register [05Fh-058h] instead of SDMA System Address register [Offset 003-000h] ADMA2 / ADMA3 Selection ADMA3 is selected by DMA Select in the Host Control 1 regis-ter. 64bit ADMA Descriptor Size 128bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1. Selection of 32-bit / 64-bit System Addressing Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of DMA Select in the Host Control 1 register. 32-bit Block Count SDMA System Address register [003h-000h] is modified to 32-bit Block Count register. Reset Source: vbus_amod_g_rst_n 0 Version 3.00 Compatible Mode 1 Version 4 Mode
11	CMD23_ENA	R/W	0h	In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 [SCR[33]=1], this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Refer to Auto CMD Enable in the Transfer Mode regis-ter. Reset Source: vbus_amod_g_rst_n 0 CMD23 Disable 1 CMD23 Enable
10	ADMA2_LEN_MODE	R/W	0h	This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit. Reset Source: vbus_amod_g_rst_n 0 16-bit Data Length Mode 1 26-bit Data Length Mode
9	DRIVER_STRENGTH2	R/W	0h	This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value. Reset Source: vbus_amod_g_rst_n

Table 14-30552. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	UHS2_INTF_ENABLE	R/W	0h	This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1. Before trying to start SD mode initialization, this bit shall be set to 0. This bit is used to enable UHS-II IF Detection, Lane Synchroni-zation and In Dormant State in the Present State register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines [CLK, CMD and DAT[3:2]] floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict. '0' 4-bit SD Interface enabled '1' UHS-II Interface enabled Reset Source: vbus_amod_g_rst_n 0 `4-bit SD Interface enabled` 1 `UHS-II Interface enabled`
7	SAMPLING_CLK_SELECT	R/W	0h	This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by Writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. Reset Source: vbus_amod_g_rst_n 0 `Fixed clock is used to sample data` 1 `Tuned clock is used to sample data`
6	EXECUTE_TUNING	R/W	0h	This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by Writing 0 for more detail about tuning procedure. '0' Not Tuned or Tuning Completed '1' Execute Tuning Reset Source: vbus_amod_g_rst_n
5:4	DRIVER_STRENGTH1	R/W	0h	Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected (Default)` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`

Table 14-30552. MMC_CTLCFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	V1P8_SIGNAL_ENA	R/W	0h	This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling [One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register] and the card or device supports UHS-I. '0' 3.3V Signalling, '1' 1.8V Signalling Reset Source: vbus_amod_g_rst_n 0 `3.3V Signalling` 1 `1.8V Signalling`
2:0	UHS_MODE_SELECT	R/W	0h	This field is used to select one of UHS-I modes or UHS-II mode.In case of UHS-I mode, this field is effective when 1.8V Signal-ing Enable is set to 1. In case of UHS-II mode, 1.8V Signaling Enable shall be set to 0. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode. If Preset Value Enable in the Host Control 2 register is set to 1,Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail. Reset Source: vbus_amod_g_rst_n 0 `SDR12` 1 `SDR25` 2 `SDR50` 3 `SDR104` 4 `DDR50` 5 `HS400` 6 `Reserved` 7 `UHS-II`

14.9.4.7.2.59 MMC_CTLCFG_CAPABILITIES Register

1 MMC_CTLCFG_CAPABILITIES Register (Offset = 40h) [reset = 180004073DE8C820h]

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initializa-tion.

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Table 14-30553. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0040h**
MMCSD2	**0FA2 0040h**

Figure 14-10123. MMC_CTLCFG_CAPABILITIES Name Register

63	62	61	60	59	58	57	48
HS400_SUPPORT	RESERVED		VDD2_1P8_SUPPORT	ADMA3_SUPPORT	RESERVED	SPI_BLK_MODE	SPI_SUPPORT
R	NONE		R	R	NONE	R	R
0h	0h		1h	1h	0h	0h	0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R							
0h							
47	46	45	44	43	42	41	40
RETUNING_MODES		TUNING_FOR_SDR50	RESERVED	RETUNING_TIMER_CNT			
R		R	NONE	R			
0h		0h	0h	4h			
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUPPORT	DRIVERC_SUPPORT	DRIVERA_SUPPORT	UHS2_SUPPORT	DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
NONE	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	1h	1h	1h
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R							
C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R	NONE	R					
0h	0h	1h					

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	0h	1 HS400 is Supported 0 HS400 is Not Supported Reset Source: vbus_amod_g_rst_n 0 HS400 Mode is not Supported 1 HS400 Mode is Supported
62:61	RESERVED	NONE	0h	Reserved

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
60	VDD2_1P8_SUPPORT	R	1h	This field indicates that support of VDD2 on Host system. Reset Source: vbus_amod_g_rst_n 0 1.8V VDD2 is not Supported 1 1.8V VDD2 is Supported
59	ADMA3_SUPPORT	R	1h	This field indicates that support of ADMA3 on Host Controller. Reset Source: vbus_amod_g_rst_n 0 ADMA3 is not Supported 1 ADMA3 is Supported
58	RESERVED	NONE	0h	Reserved
57	SPI_BLK_MODE	R	0h	This field indicates whether SPI Block Mode is supported or not. Reset Source: vbus_amod_g_rst_n 0 SPI Block Mode is not Supported 1 SPI Block Mode is Supported
56	SPI_SUPPORT	R	0h	This field indicates whether SPI Mode is supported or not. Reset Source: vbus_amod_g_rst_n 0 SPI Mode is not Supported 1 SPI Mode is Supported
55:48	CLOCK_MULTIPLIER	R	0h	This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. 'FF' Clock Multiplier M = 256 --------- '02' Clock Multiplier M = 3 '01' Clock Multiplier M = 2 '00' Clock Multiplier is Not Supported. Reset Source: vbus_amod_g_rst_n
47:46	RETUNING_MODES	R	0h	This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. '00' Mode 1 '01' Mode 2 '10' Mode 3 '11' Reserved. There are two re-tuning timings:Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue. Reset Source: vbus_amod_g_rst_n 0 Mode 1 1 Mode 2 2 Mode 3 3 Reserved
45	TUNING_FOR_SDR50	R	0h	If this bit is set to 1, this Host Controller requires tuning to operate SDR50. [Tuning is always required to operate SDR104]. '0' '1' Reset Source: vbus_amod_g_rst_n 0 SDR50 does not require tuning 1 SDR50 requires tuning
44	RESERVED	NONE	0h	Reserved

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
43:40	RETUNING_TIMER_CNT	R	4h	This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ------ n = 2[n-1] seconds ------ Bh = 1024 seconds Fh - Ch = Reserved Reset Source: vbus_amod_g_rst_n
39	RESERVED	NONE	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	This bit indicates support of Driver Type D for 1.8 Signaling. '0' Driver Type D is Not supported, '1' Driver Type D is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type D is not Supported` 1 `Driver Type D is Supported`
37	DRIVERC_SUPPORT	R	0h	This bit indicates support of Driver Type C for 1.8 Signaling. '0' Driver Type C is Not supported, '1' Driver Type C is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type C is not Supported` 1 `Driver Type C is Supported`
36	DRIVERA_SUPPORT	R	0h	This bit indicates support of Driver Type A for 1.8 Signaling. '0' Driver Type A is Not supported, '1' Driver Type A is supported Reset Source: vbus_amod_g_rst_n 0 `Driver Type A is not Supported` 1 `Driver Type A is Supported`
35	UHS2_SUPPORT	R	0h	This bit indicates whether Host controller supports UHS-II. If this bit is set to 1, 1.8V VDD2 Support shall be set to 1 [Host Sys- tem shall support VDD2 power supply]. 1 UHS-II is Supported 0 UHS-II is Not Supported Reset Source: vbus_amod_g_rst_n 0 `UHS-II is not Supported` 1 `UHS-II is Supported`
34	DDR50_SUPPORT	R	1h	This bit indicates whether DDR50 is supported or not. Reset Source: vbus_amod_g_rst_n 0 `DDR50 is not Supported` 1 `DDR50 is Supported`
33	SDR104_SUPPORT	R	1h	This bit indicates whether SDR104 is supported or not.SDR104 requires tuning. Reset Source: vbus_amod_g_rst_n 0 `SDR104 is not Supported` 1 `SDR104 is Supported`
32	SDR50_SUPPORT	R	1h	If SDR104 is supported, this bit shall be set to 1. Bit 40 indicates whether SDR50 requires tuning or not. Reset Source: vbus_amod_g_rst_n 0 `SDR50 is not Supported` 1 `SDR50 is Supported`

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31:30	SLOT_TYPE	R	0h	This field indicates usage of a slot by a specific Host System. [A host controller register set is defined perslot.] Embedded slot for one device [01b] means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot [10b] can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus [10b], the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. Reset Source: vbus_amod_g_rst_n 0 `Removeable Card Slot` 1 `Embedded Slot for One Device` 2 `Shared Bus Slot (SD Mode)` 3 `Reserved`
29	ASYNCH_INTR_SUPPORT	R	1h	Refer to SDIO Specification Version 3.00 about asynchronous interrupt. Reset Source: vbus_amod_g_rst_n 0 `Asynchronous Interrupt not Supported` 1 `Asynchronous Interrupt Supported`
28	ADDR_64BIT_SUPPORT_V3	R	1h	IMeaning of this bit is different depends on Versions [Refer to Table 2-35 for more details]. Host Controller Version 3.00 and Ver4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes. SDMA cannot be used in 64-bit Address-ing in Version 3 mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows: In case of Host Controller Version 3, 64-bit ADMA2 is enabled by DMA Select =11b in the Host Control 1 register. In case of Host Controller Version 4, 64-bitADMA2 for Version 3 is enabled by setting Host Version 4 Enable =0 and DMA Select = 11b. 1 - 64-bit System Address for V3 is Supported 0 - 64-bit System Address for V3 is not Supported Reset Source: vbus_amod_g_rst_n 0 `64-bit System Address for V3 is not Supported` 1 `64-bit System Address for V3 is Supported`
27	ADDR_64BIT_SUPPORT_V4	R	1h	This bit is added from Version 4.10. Set-ting 1 to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode [Refer to Table 2-35 for the summary of 64-bit system address support].. When this bit is set to 1, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to 64bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Address-ing for Version 4 is enabled by setting Host Version 4 Enable =1, 64-bit Address-ing =1 in the Host Control 2 register.SDMA can be used and ADMA2 uses 128-bit Descriptor. Reset Source: vbus_amod_g_rst_n 0 `64-bit System Address for V4 is not Supported` 1 `64-bit System Address for V4 is Supported`

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	VOLT_1P8_SUPPORT	R	1h	This bit indicates whether the HC supports 1.8V. Reset Source: vbus_amod_g_rst_n 0 1.8V Not Supported 1 1.8V Supported
25	VOLT_3P0_SUPPORT	R	0h	This bit indicates whether the HC supports 3.0V. Reset Source: vbus_amod_g_rst_n 0 3.0V Not Supported 1 3.3V Supported
24	VOLT_3P3_SUPPORT	R	1h	This bit indicates whether the HC supports 3.3V. Reset Source: vbus_amod_g_rst_n 0 3.3V Not Supported 1 3.3V Supported
23	SUSP_RES_SUPPORT	R	1h	This bit indicates whether the HC supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend / Resume commands. Reset Source: vbus_amod_g_rst_n 0 Suspend and Resume mechanism Not Supported 1 Suspend and Resume mechanism Supported
22	SDMA_SUPPORT	R	1h	This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. Reset Source: vbus_amod_g_rst_n 0 SDMA Not Supported 1 SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25Mhz to 50 Mhz [for SD]/ 20MHz to 52MHz [for MMC]. Reset Source: vbus_amod_g_rst_n 0 High Speed Not Supported 1 High Speed Supported
20	RESERVED	NONE	0h	Reserved
19	ADMA2_SUPPORT	R	1h	'0' ADMA2 Not Supported '1' ADMA2 Supported Reset Source: vbus_amod_g_rst_n 0 ADMA2 Not Supported 1 ADMA2 Supported
18	BUS_8BIT_SUPPORT	R	0h	This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when Slot Type is set to 10b. In this case, refer to Bus Width Preset in the Shared Bus resister. Reset Source: vbus_amod_g_rst_n 0 Extended Media Bus Not Supported 1 Extended Media Bus Supported

Table 14-30555. MMC_CTLCFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	MAX_BLK_LENGTH	R	0h	This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. Reset Source: vbus_amod_g_rst_n 0 512 byte 1 1024 byte 2 2048 byte 3 4096 byte
15:8	BASE_CLK_FREQ	R	C8h	[1]6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1MHz. The supported clock range is 10MHz to 63MHz. '11xx xxxxb' Not Supported '0011 1111b' 63MHz '0000 0010b' 2MHz '0000 0001b' 1MHz '0000 0000b'Get Information via another method [2]8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00.Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. 'FFh' 255MHz '02h' 2MHz '01h' 1MHz '00h' Get Information via another method. If the real frequency is 16.5MHz, the lager value shall be set 0001 0001b [17MHz] because the Host Driver use this value to calculate the clock divider value [Refer to the SDCLK Frequency Select in the Clock Control register.] and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method. Reset Source: vbus_amod_g_rst_n
7	TIMEOUT_CLK_UNIT	R	0h	This bit shows the unit of base clock frequency used to detect Data Timeout Error. Reset Source: vbus_amod_g_rst_n 0 KHz 1 MHz
6	RESERVED	NONE	0h	Reserved
5:0	TIMEOUT_CLK_FREQ	R	1h	This bit shows the base clock frequency used to detect Data Timeout Error. '000000' Get Information via another method, 'not 0' 1KHz to 63KHz/ 1MHz to 63MHz Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.60 MMC_CTLCFG_MAX_CURRENT_CAP Register

1 MMC_CTLCFG_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

This register indicates maximum current capability for each voltage

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Table 14-30556. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0048h**
MMCSD2	**0FA2 0048h**

Figure 14-10124. MMC_CTLCFG_MAX_CURRENT_CAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
VDD2_1P8V							
R							
0h							
15	14	13	12	11	10	9	8
VDD1_3P0V							
R							
0h							
7	6	5	4	3	2	1	0
VDD1_3P3V							
R							
0h							

Table 14-30558. MMC_CTLCFG_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved
39:32	VDD2_1P8V	R	0h	Maximum Current for 1.8V VDD2 Reset Source: vbus_amod_g_rst_n
31:24	RESERVED	NONE	0h	Reserved
23:16	VDD1_1P8V	R	0h	Maximum Current for 1.8V VDD1 Reset Source: vbus_amod_g_rst_n
15:8	VDD1_3P0V	R	0h	Maximum Current for 3.0V VDD1 Reset Source: vbus_amod_g_rst_n

Table 14-30558. MMC_CTLCFG_MAX_CURRENT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	VDD1_3P3V	R	0h	Maximum Current for 3.3V VDD1 Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.61 MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register

1 MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written. Writing 1 : set each bit of the Auto CMD12 Error Status Register Writing 0 : no effect.

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Table 14-30559. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0050h**
MMCSD2	**0FA2 0050h**

Figure 14-10125. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30561. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
6	RESERVED	NONE	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error.. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
4	INDEX	W	0h	Force Event for AUTO CMD Index Error.. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated

Table 14-30561. MMC_CTLCFG_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated

14.9.4.7.2.62 MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register

1 MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

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Table 14-30562. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0052h**
MMCSD2	**0FA2 0052h**

Figure 14-10126. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			W	W	W	W	W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30564. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	W	0h	Force Event for Host Error Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
11	RESP	W	0h	Force Event for Response Error Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
10	TUNING	W	0h	Force Event for Tuning Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
9	ADMA	W	0h	Force Event for ADMA Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated
7	CURR_LIM	W	0h	Force Event for Current Limit Error. Reset Source: vbus_amod_g_rst_n 0 No Interrupt 1 Interrupt is generated

Table 14-30564. MMC_CTLCFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
5	DAT_CRC	W	0h	Force Event for Data CRC Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
3	CMD_INDEX	W	0h	Force Event for Command Index Error Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
1	CMD_CRC	W	0h	Force Event for Command CRC Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Interrupt is generated`

14.9.4.7.2.63 MMC_CTLCFG_ADMA_ERR_STATUS Register

1 MMC_CTLCFG_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

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Table 14-30565. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0054h**
MMCSD2	**0FA2 0054h**

Figure 14-10127. MMC_CTLCFG_ADMA_ERR_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
NONE					R	R	
0h					0h	0h	

Table 14-30567. MMC_CTLCFG_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Error set`
1:0	ADMA_ERR_STATE	R	0h	This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 D00 : ADMA Error State when error occurred Contents of SYS_SDR register. Reset Source: vbus_amod_g_rst_n 0 `ST_STOP(Stop DMA) Points to next of the error descriptor` 1 `ST_FDS(Fetch Descriptor)Points to the error descriptor` 2 `Never set this state(Not Used)` 3 `ST_TFR(Transfer Data) Points to the next of the error descriptor`

14.9.4.7.2.64 MMC_CTLCFG_ADMA_SYS_ADDRESS Register

1 MMC_CTLCFG_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = 0h]

This register contains the physical address used for ADMA data transfer

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Table 14-30568. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0058h**
MMCSD2	**0FA2 0058h**

Figure 14-10128. MMC_CTLCFG_ADMA_SYS_ADDRESS Name Register

63	62	61	60	59	58	57	48
ADMA_ADDR							
R/W							
0h							
55	54	53	52	51	50	49	48
ADMA_ADDR							
R/W							
0h							
47	46	45	44	43	42	41	40
ADMA_ADDR							
R/W							
0h							
39	38	37	36	35	34	33	32
ADMA_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
ADMA_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADMA_ADDR							
R/W							
0h							

Table 14-30570. MMC_CTLCFG_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	ADMA_ADDR	R/W	0h	The 32-bit addressing Host Driver uses lower 32-bit of this register [upper 32-bit should be set to 0] and shall program Descriptor Table on 32-bit boundary andset 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 00b. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register andassumes it to be 000b. SDMA If Host Version 4.00 Enable is set to 1, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register [Offset 003-000h]. SDMA can be used in 32-bit and 64-bit addressing in Version 4.00. ADMA2 This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. ADMA3 This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register,which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. Register Value - 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.65 MMC_CTLCFG_PRESET_VALUE0 Register

1 MMC_CTLCFG_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30571. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0060h**
MMCSD2	**0FA2 0060h**

Figure 14-10129. MMC_CTLCFG_PRESET_VALUE0 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	100h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
100h							

Table 14-30573. MMC_CTLCFG_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	100h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.66 MMC_CTLCFG_PRESET_VALUE1 Register

1 MMC_CTLCFG_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30574. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0062h**
MMCSD2	**0FA2 0062h**

Figure 14-10130. MMC_CTLCFG_PRESET_VALUE1 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R</td><td colspan="3">NONE</td><td>R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td><td colspan="2">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-30576. MMC_CTLCFG_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.67 MMC_CTLCFG_PRESET_VALUE2 Register

1 MMC_CTLCFG_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30577. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0064h**
MMCSD2	**0FA2 0064h**

Figure 14-10131. MMC_CTLCFG_PRESET_VALUE2 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30579. MMC_CTLCFG_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.68 MMC_CTLCFG_PRESET_VALUE3 Register

1 MMC_CTLCFG_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30580. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0066h**
MMCSD2	**0FA2 0066h**

Figure 14-10132. MMC_CTLCFG_PRESET_VALUE3 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	4h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
4h							

Table 14-30582. MMC_CTLCFG_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.69 MMC_CTLCFG_PRESET_VALUE4 Register

1 MMC_CTLCFG_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30583. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0068h**
MMCSD2	**0FA2 0068h**

Figure 14-10133. MMC_CTLCFG_PRESET_VALUE4 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30585. MMC_CTLCFG_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.70 MMC_CTLCFG_PRESET_VALUE5 Register

1 MMC_CTLCFG_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30586. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 006Ah**
MMCSD2	**0FA2 006Ah**

Figure 14-10134. MMC_CTLCFG_PRESET_VALUE5 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
1h							

Table 14-30588. MMC_CTLCFG_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	1h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.71 MMC_CTLCFG_PRESET_VALUE6 Register

1 MMC_CTLCFG_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30589. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 006Ch**
MMCSD2	**0FA2 006Ch**

Figure 14-10135. MMC_CTLCFG_PRESET_VALUE6 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
0h							

Table 14-30591. MMC_CTLCFG_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.72 MMC_CTLCFG_PRESET_VALUE7 Register

1 MMC_CTLCFG_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30592. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 006Eh**
MMCSD2	**0FA2 006Eh**

Figure 14-10136. MMC_CTLCFG_PRESET_VALUE7 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
2h							

Table 14-30594. MMC_CTLCFG_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 `Driver Type B is Selected` 1 `Driver Type A is Selected` 2 `Driver Type C is Selected` 3 `Driver Type D is Selected`
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.73 MMC_CTLCFG_PRESET_VALUE8 Register

1 MMC_CTLCFG_PRESET_VALUE8 Register (Offset = 72h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30595. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0072h**
MMCSD2	**0FA2 0072h**

Figure 14-10137. MMC_CTLCFG_PRESET_VALUE8 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
0h							

Table 14-30597. MMC_CTLCFG_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.74 MMC_CTLCFG_PRESET_VALUE10 Register

1 MMC_CTLCFG_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-30598. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0074h**
MMCSD2	**0FA2 0074h**

Figure 14-10138. MMC_CTLCFG_PRESET_VALUE10 Name Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R							
0h							

Table 14-30600. MMC_CTLCFG_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Reset Source: vbus_amod_g_rst_n 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.75 MMC_CTLCFG_ADMA3_DESC_ADDRESS Register

1 MMC_CTLCFG_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = 0h]

The start address of Integrated DMA Descriptor is set to this register.

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Table 14-30601. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0078h**
MMCSD2	**0FA2 0078h**

Figure 14-10139. MMC_CTLCFG_ADMA3_DESC_ADDRESS Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTG_DESC_ADDR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30603. MMC_CTLCFG_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTG_DESC_ADDR	R/W	0h	The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. The 32-bit addressing Host Driver uses lower 32- bit of this register and shall program Descriptor Table on 32-bit boundary.ADMA3 ignores lower 2-bit of this register and assumes it to be 00b. Writing to 07Bh starts ADMA3 data transfer. The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 000b. Writing to 07Fh starts ADMA3 data transfer. Register Value- 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.76 MMC_CTLCFG_UHS2_BLOCK_SIZE Register

1 MMC_CTLCFG_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-30604. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0080h**
MMCSD2	**0FA2 0080h**

Figure 14-10140. MMC_CTLCFG_UHS2_BLOCK_SIZE Name Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_BOUNDARY			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_SIZE							
R/W							
0h							

Table 14-30606. MMC_CTLCFG_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_BOUNDARY	R/W	0h	When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of sys-tem memory management is set to this field. Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the ADMA System Address register. SDMA waits until the ADMA System Address register is written. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the UHS-II Transfer Mode register is set to 1. ADMA does not use this field. Reset Source: vbus_amod_g_rst_n 0 4K Bytes 1 8K Bytes 2 16K Bytes 3 32K Bytes 4 64K Bytes 5 128K Bytes 6 256K Bytes 7 512K Bytes

Table 14-30606. MMC_CTLCFG_UHS2_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	XFER_BLK_SIZE	R/W	0h	This register specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes. Vari-able block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This register is effective when Data Present is set to 1 in UHS-II Command register. Reset Source: vbus_amod_g_rst_n 0 No data transfer 1 1 Byte 2 2 Bytes 512 512 Bytes 2048 2048 Bytes

14.9.4.7.2.77 MMC_CTLCFG_UHS2_BLOCK_COUNT Register

1 MMC_CTLCFG_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-30607. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0084h**
MMCSD2	**0FA2 0084h**

Figure 14-10141. MMC_CTLCFG_UHS2_BLOCK_COUNT Name Register

31	30	29	28	27	26	25	24
XFER_BLK_COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
XFER_BLK_COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
XFER_BLK_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
XFER_BLK_COUNT							
R/W							
0h							

Table 14-30609. MMC_CTLCFG_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XFER_BLK_COUNT	R/W	0h	This register is effective when Data Present is set to 1 in UHS-II Command register and is enabled when Block Count Enable is set to 1 and Block / Byte Mode is set to 0 in the UHS-II Transfer Mode register. Data transfer stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred. This register should be accessed only when no transaction is executing [i.e.,after transactions are stopped]. During data transfer, read operations on this register may return an invalid value and write operations are ignored. 00000000h - Stop Count 00000001h - 1 block 00000002h - 2 blocks .... FFFFFFFFh - 4G blocks -1. Reset Source: vbus_amod_g_rst_n 0 Stop Count 1 1 block 2 2 blocks 3 3 blocks 4294967295 4G blocks -1

14.9.4.7.2.78 MMC_CTLCFG_UHS2_COMMAND_PKT_j Register

1 MMC_CTLCFG_UHS2_COMMAND_PKT_j Register (Offset = 88h + formula) [reset = 0h]

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes. The command length varies depends on a Command Packet type. The length is specified by the UHS-II Command register.

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Offset = 88h + (j * 1h); where j = 0 to 19d

Table 14-30610. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0088h + formula**
MMCSD2	**0FA2 0088h + formula**

Figure 14-10142. MMC_CTLCFG_UHS2_COMMAND_PKT_j Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W							
0h							

Table 14-30612. MMC_CTLCFG_UHS2_COMMAND_PKT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CMD_PKT_BYTE	R/W	0h	UHS-II Command Packet image is set to this register.The command length varies depends on a Command Packet type. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.79 MMC_CTLCFG_UHS2_XFER_MODE Register

1 MMC_CTLCFG_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-30613. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 009Ch**
MMCSD2	**0FA2 009Ch**

Figure 14-10143. MMC_CTLCFG_UHS2_XFER_MODE Name Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W	R/W	NONE					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-30615. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Use of 2 lane half duplex mode is determined by Host Driver. Reset Source: vbus_amod_g_rst_n 0 Full Duplex Mode 1 Half Duplex Mode
14	EBSY_WAIT	R/W	0h	This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer.If this bit is set to 1, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, Transfer Com-plete in the Normal Interrupt Status reg-ister is set to 1 to indicate end ofbusy. If an error is indicated in EBSY packet [ex. Memory Error], EBSY Error in the UHS-II Error Interrupt Status register is set to 1. Setting of EBSY Error also sets Error Interrupt to 1 in the Normal Inter-rupt Status register. Error Interrupt and Transfer Complete shall be set together. '1' Wait EBSY, '0' Issue a command without busy. Reset Source: vbus_amod_g_rst_n
13:9	RESERVED	NONE	0h	Reserved

Table 14-30615. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0 and waits Command Complete Interrupt and then check the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Com-mand Complete Signal Enable. Reset Source: vbus_amod_g_rst_n 0 `Enable Response Interrupt` 1 `Disable Response Interrupt`
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver.Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0 and Response Inter-rupt Disable is set to 0. If Host Control-ler checks response error, sets this bit to 1 and sets Response Interrupt Dis-able to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `Disable Response Error Check` 1 `Enable Response Error Check`
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE Reset Source: vbus_amod_g_rst_n 0 `Memory` 1 `SDIO`
5	BYTE_MODE	R/W	0h	This bit specifies whether data transfer is in byte mode or block mode when Data Present is set to 1. This bit is effective to a command with data trans-fer. Reset Source: vbus_amod_g_rst_n 0 `Block Mode` 1 `Byte Mode`

Table 14-30615. MMC_CTLCFG_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_XFER_DIR	R/W	0h	This bit specifies direction of data trans-fer when Data Present is set to 1. This bit is effective to a command with data transfer. 0 - Read [Card to Host] 1 - Write [Host to Card] Reset Source: vbus_amod_g_rst_n 0 `Read from Card to Host` 1 `Write from Host to Card`
3:2	RESERVED	NONE	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	This bit specifies whether data transfer usesUHS-II Block Count register. If this bit is set to 1, data transfer is terminated by Block Count. Setting to UHS-II Block Count register shall be equivalent to TLEN in UHS-II Command Packet reg-ister. Reset Source: vbus_amod_g_rst_n 0 `Disable Block count` 1 `Enable Block count`
0	DMA_ENA	R/W	0h	This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by DMA Select in the Host Control 1 register. Reset Source: vbus_amod_g_rst_n 0 `DMA mode is Disabled` 1 `DMA mode is Enabled`

14.9.4.7.2.80 MMC_CTLCFG_UHS2_COMMAND Register

1 MMC_CTLCFG_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-30616. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 009Eh**
MMCSD2	**0FA2 009Eh**

Figure 14-10144. MMC_CTLCFG_UHS2_COMMAND Name Register

15	14	13	12	11	10	9	8
RESERVED			PKT_LENGTH				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_TYPE		DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED	
R/W		R/W	NONE		R/W	NONE	
0h		0h	0h		0h	0h	

Table 14-30618. MMC_CTLCFG_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12:8	PKT_LENGTH	R/W	0h	A command packet length, which is set in the UHS-II Command Packet register, is set to this register. 00011b - 00000b - 3-0 Bytes [Not used] 00100b - 4 Bytes .... 10100b - 20 Bytes 11111b 10101b Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	This field is used to distinguish a spe-cific command like abort command. If this field is set to 00b, the UHS-II RES Packet is stored in UHS-II Response register [0B3h-0A0h]. To avoid overwrit-ing the UHS-II Response register, when this filed is set to 01b, the RES Packet [4 bytes length] of TRANS_ABORT CCMD is stored in the Response regis-ter [013h-010h] and when this filed is set to 10b, the RES Packet [8 bytes length] of memory or SDIO abort com-mand [CMD12 or SDIO Abort com-mand] is stored in the Response register [01Fh-018h]. When this filed is set to 11b, Host Controller controls lane to go into dormant state. '00' Normal Command '01' TRANS_ABORT CCMD '10' CMD12 or SDIO Abort Command '11' Go Dormant Command Reset Source: vbus_amod_g_rst_n 0 `Normal command` 1 `TRANS_ABORT CCMD` 2 `Abort command` 3 `Go dormant command`

Table 14-30618. MMC_CTLCFG_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	This bit specifies whether the command is accompanied by data packet. Reset Source: vbus_amod_g_rst_n 0 `Data not Present` 1 `Data present`
4:3	RESERVED	NONE	0h	Reserved
2	SUB_COMMAND	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17].When issuing a main command, this bit is set to 0 and when issuing a sub com-mand, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register. Reset Source: vbus_amod_g_rst_n 0 `Main Command` 1 `Sub Command`
1:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.81 MMC_CTLCFG_UHS2_RESPONSE_j Register

1 MMC_CTLCFG_UHS2_RESPONSE_j Register (Offset = A0h + formula) [reset = 0h]

This register is used to store received UHS-II RES Packet image

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Offset = A0h + (j * 1h); where j = 0 to 19d

Table 14-30619. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00A0h + formula**
MMCSD2	**0FA2 00A0h + formula**

Figure 14-10145. MMC_CTLCFG_UHS2_RESPONSE_j Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R							
0h							

Table 14-30621. MMC_CTLCFG_UHS2_RESPONSE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESP_PKT_BYTE	R	0h	Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.82 MMC_CTLCFG_UHS2_MESSAGE_SELECT Register

1 MMC_CTLCFG_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30622. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00B4h**
MMCSD2	**0FA2 00B4h**

Figure 14-10146. MMC_CTLCFG_UHS2_MESSAGE_SELECT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						MSG_SEL	
NONE						R/W	
0h						0h	

Table 14-30624. MMC_CTLCFG_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	NONE	0h	Reserved
1:0	MSG_SEL	R/W	0h	Host Controller holds 4 MSG packets in FIFO buffer.One of 4 MSGs can be read from the UHS-II MSG register [0BB-0B8h] by setting this register.[Assumed for debug usage.] '00' The latest MSG '01' One MSG before '10' Two MSGs before '11' Three MSGs before Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.83 MMC_CTLCFG_UHS2_MESSAGE Register

1 MMC_CTLCFG_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

This register is used to access internal buffer

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Table 14-30625. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00B8h**
MMCSD2	**0FA2 00B8h**

Figure 14-10147. MMC_CTLCFG_UHS2_MESSAGE Name Register

31	30	29	28	27	26	25	24
MSG_BYTE3							
R							
0h							
23	22	21	20	19	18	17	16
MSG_BYTE2							
R							
0h							
15	14	13	12	11	10	9	8
MSG_BYTE1							
R							
0h							
7	6	5	4	3	2	1	0
MSG_BYTE0							
R							
0h							

Table 14-30627. MMC_CTLCFG_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSG_BYTE3	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
23:16	MSG_BYTE2	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
15:8	MSG_BYTE1	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/ toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n

Table 14-30627. MMC_CTLCFG_UHS2_MESSAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	MSG_BYTE0	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.84 MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register

1 MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

This register shows receipt of INT MSG from which device

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Table 14-30628. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00BCh**
MMCSD2	**0FA2 00BCh**

Figure 14-10148. MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Name Register

15	14	13	12	11	10	9	8
DEV_INT_STS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
DEV_INT_STS							
R/W1TC							
0h							

Table 14-30630. MMC_CTLCFG_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DEV_INT_STS	R/W1TC	0h	This register shows receipt of INT MSG from which device and is effective when INT MSG Enable is set to 1 in the UHS- II Device Select register. On receiving INT MSG from a device, Host Controller saves the INT MSG to UHS-II Device Interrupt Code register. A bit of this register, which is corre- spondent to Device ID, is set to 1 and generate Card Interrupt in Normal Interrupt Status register. Writing a bit to 1 clears the status bit [interrupt is treated] and Writing a bit to 0 keeps the status value [interrupt is untreated]. If INT MSG Enable is set to 0, this register is cleared to 0 and Host Controller ignores receipt of INT MSG. Effective bit range of this register is determined by Number of Devices Supported in the UHS-II General Capabilities regis-ter. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0. D00 - Not used [Reserved] D01 - Setting 1 means INT MSG is received from Device ID 1 D02 - Setting 1 means INT MSG is received from Device ID 2 .... D15 - Setting 1 means INT MSG is received from Device ID 15 Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.85 MMC_CTLCFG_UHS2_DEVICE_SELECT Register

1 MMC_CTLCFG_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

UHS-II Device Select Register

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Table 14-30631. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00BEh**
MMCSD2	**0FA2 00BEh**

Figure 14-10149. MMC_CTLCFG_UHS2_DEVICE_SELECT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-30633. MMC_CTLCFG_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	This bit enables receipt of INT MSG. If this bit is set to 1,receipt of INT MSG is informed by Card Interrupt in the Nor-mal Interrupt Status register. If this bit is set to 0, Host Con-troller ignores receipt of INT MSG and may not set the UHS-II Device Interrupt Code register. Support of INT MSG Interrupt is optional. If trying to set this bit to 1 but still this bit is read 0, INT MSG Interrupt is not sup-ported by the Host Controller. In this case, UHS-II Device Interrupt Status register always shall be read 0 and UHS-II Device Interrupt Code register may not be implemented. '0' Disabled '1' Enabled Reset Source: vbus_amod_g_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	DEV_SEL	R/W	0h	Host Controller holds an INT MSG packet per device. One of INT MSGs [up to 15] can be selected by this field and read from the UHS-II Device Interrupt Code Register [0BFh]. This field is effective when INT MSG Enable is set to 1. The number of devices implemented in the Host Controller is indicated by Number of Devices supported in the UHS-II General Capabilities register. 0h Unselected [Default] 1h INT MSG of Device ID 1 is selected 2h INT MSG of Device ID 2 is selected .... Fh INT MSG of Device ID 15 is selected Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.86 MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register

1 MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register.

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Table 14-30634. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00BFh**
MMCSD2	**0FA2 00BFh**

Figure 14-10150. MMC_CTLCFG_UHS2_DEVICE_INT_CODE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
DEV_INTR							
R							
0h							

Table 14-30636. MMC_CTLCFG_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_INTR	R	0h	This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register. Host Controller holds an INT MSG packet per device. One of INT MSGs [Code length is 1 byte] up to 15 can be read from this register by select-ing UHS-II Device Select. The number of the registers to hold INT MSGs is determined by Number of Devices Sup-ported in the UHS-II General Capabili-ties register. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.87 MMC_CTLCFG_UHS2_SOFTWARE_RESET Register

1 MMC_CTLCFG_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

UHS-II Software Reset Register

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Table 14-30637. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00C0h**
MMCSD2	**0FA2 00C0h**

Figure 14-10151. MMC_CTLCFG_UHS2_SOFTWARE_RESET Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
NONE						R/W	R/W
0h						0h	0h

Table 14-30639. MMC_CTLCFG_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	NONE	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	Host Driver set this bit to 1 to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completionof SD-TRAN reset. If CMD0 is issued, SD-TRAN Initial- ization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required. '0' Not Affected '1' Reset SD TRAN Host Controller requires to do followings: [1] SD Clock Enable is maintained.[Continue to provide RCLK]. [2] All setting register is maintained. [3] Internal sequencers are reset to just after power on.be able to issue a command. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. [5] Data transfer is terminated and data in buffer is dis-carded. Reset Source: vbus_amod_g_rst_n 0 Not Affected 1 Reset SDTRAN

Table 14-30639. MMC_CTLCFG_UHS2_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_FULL_RESET	R/W	0h	On issuing FULL_RESET CCMD, Host Driver set this bit to 1 to reset Host Controller. This bit is cleared auto-matically at completion of Host Controller reset. Initial- ization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained. Host Controller requires to do followings: [1] SD Clock Enable is cleared. [Internal Clock is still synchronized]. [2] All setting register is cleared. [3] Internal sequencers are reset to just after power on. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. Reset Source: vbus_amod_g_rst_n 0 Not Affected 1 Reset Host Conroller

14.9.4.7.2.88 MMC_CTLCFG_UHS2_TIMER_CONTROL Register

1 MMC_CTLCFG_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

UHS-II Timeout Control Register

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Table 14-30640. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00C2h**
MMCSD2	**0FA2 00C2h**

Figure 14-10152. MMC_CTLCFG_UHS2_TIMER_CONTROL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W				R/W			
0h				0h			

Table 14-30642. MMC_CTLCFG_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:4	DEADLOCK_TIMEOUT_CTR	R/W	0h	This value determines the deadlock period while host expecting to receive a packet [1 second]. Tim-eout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n
3:0	CMDRESP_TIMEOUT_CTR	R/W	0h	This value determines the interval between com-mand packet and response packet [5ms]. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.89 MMC_CTLCFG_UHS2_ERR_INTR_STS Register

1 MMC_CTLCFG_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

This register gives the status of all UHS-II interrupts

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Table 14-30643. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00C4h**
MMCSD2	**0FA2 00C4h**

Figure 14-10153. MMC_CTLCFG_UHS2_ERR_INTR_STS Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC_ERR					RESERVED		
R/W1TC					NONE		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W1TC	R/W1TC
0h						0h	0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W1TC	NONE						R/W1TC
0h	0h						0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1TC	NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30645. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC_ERR	R/W1TC	0h	Vendor may use this field for vendor specific error status. '0' Interrupt is not generated '1' Vendor Specific Error Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved

17	DEADLOCK_TIMEOUT	R/W1TC	0h	Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout [1 second]. Timeout value is determined by the setting of Timeout Counter Value for Deadlock in UHS-II Timer Control register.
				Reset Source: vbus_amod_g_rst_n
				`0 No Error`
				`1 Deadlock Error`

Table 14-30645. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W1TC	0h	Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout [5ms]. Timeout value is determined by the setting of Timeout Counter Value for CMD_RES in UHS-II Timer Control register. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Resp packet timeout Error`
15	ADMA2_ADMA3	R/W1TC	0h	Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the ADMA Error Status [054h], which is defined in the Host spec 3.00. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `ADMA2/3 Error`
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W1TC	0h	On receiving EBSY packet, if the packet indicates an error, this bit is set to 1. Setting of this bit also sets Error Interrupt and Transfer Completer together in the Normal Interrupt Status register. This error check is effective for a command with setting EBSY Wait in the UHS-II Transfer Mode register. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `EBSY Error`
7	UNRECOVERABLE	R/W1TC	0h	Setting of this bit means that Unrecoverable Error is set in a packet from a device. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Device Unrecoverable Error`
6	RESERVED	NONE	0h	Reserved
5	TID	R/W1TC	0h	Setting of this bit means that TID Error occurs. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `TID Error`
4	FRAMING	R/W1TC	0h	Setting of this bit means that Framing Error occurs during a packet receiving. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Framing Error`
3	CRC	R/W1TC	0h	Setting of this bit means that CRC Error occurs during a packet receiving. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `CRC Error`
2	RETRY_EXPIRED	R/W1TC	0h	Setting of this bit means that Retry Counter Expired Error occurs during data transfer.If this bit is set,either Framing Error or CRC Error in this register shall be set. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Retry Expired Error`

Table 14-30645. MMC_CTLCFG_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESP_PKT	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to1 in the UHS- II Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response,this bit is set to 1. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Resp packet Error`
0	HEADER	R/W1TC	0h	Setting of this bit means that Header Error occurs in a received packet. Reset Source: vbus_amod_g_rst_n 0 `No Error` 1 `Header Error`

14.9.4.7.2.90 MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register

1 MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

This register is used to enable the UHS-II Error Interrupt Status register fields

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Table 14-30646. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00C8h**
MMCSD2	**0FA2 00C8h**

Figure 14-10154. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W					NONE		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30648. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting this bit to 1 enables setting of Vendor Specific Error bit in the UHS-II Error Interrupt Status register. 0h - Status is Disabled 1h - Status is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for Dead lock bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for CMD_RES bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled

Table 14-30648. MMC_CTLCFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables setting of ADMA2/3 Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W	0h	Setting this bit to 1 enables setting of EBSY Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables setting of Unrecoverable Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables setting of TID Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
4	FRAMING	R/W	0h	Setting this bit to 1 enables setting of Framing Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
3	CRC	R/W	0h	Setting this bit to 1 enables setting of CRC Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
2	RETRY_EXPIRED	R/W	0h	Setting this bit to 1 enables setting of Retry Expired bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables setting of RES Packet Error bit in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled
0	HEADER	R/W	0h	Setting this bit to 1 enables setting of Header Error bit in the UHS-II Error Interrupt Status Register. Reset Source: vbus_amod_g_rst_n 0 Status is Disabled 1 Status is Enabled

14.9.4.7.2.91 MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register

1 MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

This register is used to generate UHS-II Interrupt signals

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Table 14-30649. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00CCh**
MMCSD2	**0FA2 00CCh**

Figure 14-10155. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W					NONE		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADMA2_ADMA3	RESERVED						EBSY
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED_SIG_ENA	RESP_PKT	HEADER
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30651. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting of a bit to 1 in this field enables generating interrupt signal when corre-spondent bit of Vendor Specific Error is set in the UHS-II Error Interrupt Status Register. 0h - Interrupt Signal is Disabled 1h - Interrupt Signal is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for Dead lock bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for CMD_RES bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled

Table 14-30651. MMC_CTLCFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables generating interrupt signal when ADMA2/3 Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W	0h	Setting this bit to 1 enables generating interrupt signal when EBSY Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Unrecoverable Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables generating interrupt signal when TID Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
4	FRAMING	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Framing Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
3	CRC	R/W	0h	Setting this bit to 1 enables generating interrupt signal when CRC Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Retry Expired bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when RES Packet Error bit is set in the UHS-II Error InterruptStatus Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled
0	HEADER	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Header Error bit is set in the UHS-II Error Interrupt Status Register. Reset Source: vbus_amod_g_rst_n 0 Interrupt Signal is Disabled 1 Interrupt Signal is Enabled

14.9.4.7.2.92 MMC_CTLCFG_UHS2_SETTINGS_PTR Register

1 MMC_CTLCFG_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

This register is pointer for UHS-II settings.

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Table 14-30652. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00E0h**
MMCSD2	**0FA2 00E0h**

Figure 14-10156. MMC_CTLCFG_UHS2_SETTINGS_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_SETTINGS_PTR							
R							
100h							
7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR							
R							
100h							

Table 14-30654. MMC_CTLCFG_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.93 MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register

1 MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

This register is pointer for UHS-II Capabilities Register.

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Table 14-30655. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00E2h**
MMCSD2	**0FA2 00E2h**

Figure 14-10157. MMC_CTLCFG_UHS2_CAPABILITIES_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_CAPABILITIES_PTR							
R							
110h							
7	6	5	4	3	2	1	0
UHS2_CAPABILITIES_PTR							
R							
110h							

Table 14-30657. MMC_CTLCFG_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.94 MMC_CTLCFG_UHS2_TEST_PTR Register

1 MMC_CTLCFG_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

This register is pointer for UHS-II Test Register.

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Table 14-30658. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00E4h**
MMCSD2	**0FA2 00E4h**

Figure 14-10158. MMC_CTLCFG_UHS2_TEST_PTR Name Register

15	14	13	12	11	10	9	8
UHS2_TEST_PTR							
R							
120h							
7	6	5	4	3	2	1	0
UHS2_TEST_PTR							
R							
120h							

Table 14-30660. MMC_CTLCFG_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.95 MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register

1 MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

This register is pointer for UHS-II Shared Bus Control Register.

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Table 14-30661. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00E6h**
MMCSD2	**0FA2 00E6h**

Figure 14-10159. MMC_CTLCFG_SHARED_BUS_CTRL_PTR Name Register

15	14	13	12	11	10	9	8
SHARED_BUS_CTRL_PTR							
R							
130h							
7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR							
R							
130h							

Table 14-30663. MMC_CTLCFG_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.96 MMC_CTLCFG_VENDOR_SPECFIC_PTR Register

1 MMC_CTLCFG_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

This register is pointer for UHS-II Vendor Specific Pointer Register.

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Table 14-30664. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00E8h**
MMCSD2	**0FA2 00E8h**

Figure 14-10160. MMC_CTLCFG_VENDOR_SPECFIC_PTR Name Register

15	14	13	12	11	10	9	8
VENDOR_SPECFIC_PTR							
R							
140h							
7	6	5	4	3	2	1	0
VENDOR_SPECFIC_PTR							
R							
140h							

Table 14-30666. MMC_CTLCFG_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.97 MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register

1 MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

This is used to program the boot timeout value counter

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Table 14-30667. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00F4h**
MMCSD2	**0FA2 00F4h**

Figure 14-10161. MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Name Register

31	30	29	28	27	26	25	24
DATA_TIMEOUT_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_TIMEOUT_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_TIMEOUT_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT							
R/W							
0h							

Table 14-30669. MMC_CTLCFG_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_TIMEOUT_CNT	R/W	0h	This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.The value is in number of sd clock. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.98 MMC_CTLCFG_VENDOR_REGISTER Register

1 MMC_CTLCFG_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

Vendor register added for autogate sdclk, cmd11 power down timer, enhancedstrobe and eMMC hardware reset

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Table 14-30670. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00F8h**
MMCSD2	**0FA2 00F8h**

Figure 14-10162. MMC_CTLCFG_VENDOR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							AUTOGATE_SDCLK
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CMD11_PD_TIMER							
R/W							
1388h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD11_PD_TIMER						EMMC_HW_RESET	ENHANCED_STROBE
R/W						R/W	R/W
1388h						0h	0h

Table 14-30672. MMC_CTLCFG_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device Reset Source: vbus_amod_g_rst_n 0 `Autogating of sdclk is Disabled` 1 `Autogating of sdclk is Enabled`
15:2	CMD11_PD_TIMER	R/W	1388h	cmd11 power-down timer value Reset Source: vbus_amod_g_rst_n
1	EMMC_HW_RESET	R/W	0h	Hardware reset signal is generared for eMMC card when this bit is set Reset Source: vbus_amod_g_rst_n 0 `Deassert the hardware reset pin` 1 `Drives the hardware reset pin as ZERO (Active LOW to eMMC card)`

Table 14-30672. MMC_CTLCFG_VENDOR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ENHANCED_STROBE	R/W	0h	This bit enables the enhanced strobe logic of the Host Controller Reset Source: vbus_amod_g_rst_n 0 Enhanced strobe is Disabled 1 Enhanced strobe is Enabled

14.9.4.7.2.99 MMC_CTLCFG_SLOT_INT_STS Register

1 MMC_CTLCFG_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

This register is used to read the interrupt signal for each slot.

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Table 14-30673. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00FCh**
MMCSD2	**0FA2 00FCh**

Figure 14-10163. MMC_CTLCFG_SLOT_INT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTR_SIG							
R							
0h							

Table 14-30675. MMC_CTLCFG_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:0	INTR_SIG	R	0h	These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.100 MMC_CTLCFG_HOST_CONTROLLER_VER Register

1 MMC_CTLCFG_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

This register is used to read the vendor version number and specification version number

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Table 14-30676. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 00FEh**
MMCSD2	**0FA2 00FEh**

Figure 14-10164. MMC_CTLCFG_HOST_CONTROLLER_VER Name Register

15	14	13	12	11	10	9	8
VEN_VER_NUM							
R							
10h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEC_VER_NUM							
R							
4h							

Table 14-30678. MMC_CTLCFG_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	VEN_VER_NUM	R	10h	The Vendor Version Number is set to 0x10 [1.0] Reset Source: vbus_amod_g_rst_n
7:0	SPEC_VER_NUM	R	4h	This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. 00h - SD Host Controller Specification Version 1.00 01h - SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 02h - SD Host Controller Specification Version 3.00 03h - SD Host Controller Specification Version 4.00 04h - SD Host Controller Specification Version 4.10 'others' Reserved Reset Source: vbus_amod_g_rst_n 0 `SD Host Controller Specification Version 1.00` 1 `SD Host Controller Specification Version 2.00` 2 `SD Host Controller Specification Version 3.00` 3 `SD Host Controller Specification Version 4.00` 4 `SD Host Controller Specification Version 4.10`

14.9.4.7.2.101 MMC_CTLCFG_UHS2_GEN_SETTINGS Register

1 MMC_CTLCFG_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

Start Address of General settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30679. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0100h**
MMCSD2	**0FA2 0100h**

Figure 14-10165. MMC_CTLCFG_UHS2_GEN_SETTINGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		NUMLANES					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							POWER_MODE
NONE							R/W
0h							0h

Table 14-30681. MMC_CTLCFG_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	NUMLANES	R/W	0h	The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0000b - 2 Lanes FD or 2L-HD 0001b - Not Used 0010b - 3 Lanes 2D1U-FD [Embedded] 0011b - 3 Lanes 1D2U-FD [Embedded] 0100b - 4 Lanes 2D2U-FD [Embedded] others - Reserved Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	POWER_MODE	R/W	0h	This field determines either Fast mode or Low Power mode.Host and all devices connected to the host shall be set to the same mode. Reset Source: vbus_amod_g_rst_n 0 Fast mode 1 Low power mode

14.9.4.7.2.102 MMC_CTLCFG_UHS2_PHY_SETTINGS Register

1 MMC_CTLCFG_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

Start Address of PHY settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30682. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0104h**
MMCSD2	**0FA2 0104h**

Figure 14-10166. MMC_CTLCFG_UHS2_PHY_SETTINGS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">N_LSS_DIR</td><td colspan="4">N_LSS_SYN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>HIBERNATE_ENA</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SPEED_RANGE</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-30684. MMC_CTLCFG_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R/W	0h	The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h - 8 x16 LSS 1h - 8 x 1 LSS 2h - 8 x 2 LSS 3h - 8 x 3 LSS .... Fh - 8 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R/W	0h	The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n

Table 14-30684. MMC_CTLCFG_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	HIBERNATE_ENA	R/W	0h	After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off. Reset Source: vbus_amod_g_rst_n 0 `Hibernate Disabled` 1 `Hibernate Enabled`
14:8	RESERVED	NONE	0h	Reserved
7:6	SPEED_RANGE	R/W	0h	PLL multiplier is selected by this field.Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State. '00' Range A [Default] '01' Range B '10' Reserved '11' Reserved Reset Source: vbus_amod_g_rst_n 0 `Range A (Default)` 1 `Range B` 2 `Reserved` 3 `Reserved`
5:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.103 MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register

1 MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-30685. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0108h**
MMCSD2	**0FA2 0108h**

Figure 14-10167. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W							
0h							
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30687. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved

Table 14-30687. MMC_CTLCFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	N_DATA_GAP	R/W	0h	The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS Reset Source: vbus_amod_g_rst_n 0 No Gap 1 1 LSS 2 2 LSS 3 3 LSS 255 255 LSS
31:18	RESERVED	NONE	0h	Reserved
17:16	RETRY_COUNT	R/W	0h	Data Burst retry count is set to this field. '00' Retry Disabled '01' 1 time '10' 2 times '11' 3 times Reset Source: vbus_amod_g_rst_n 0 Retry Disabled 1 Retry 1time 2 Retry 2times 3 Retry 3times
15:8	HOST_NFCU	R/W	0h	Host Driver sets the number of blocks in Data Burst [Flow Control] to this field.The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Blocks 03h - 3 Blocks .... FFh - 255 Blocks Reset Source: vbus_amod_g_rst_n 0 256 Blocks 1 1 Block 2 2 Blocks 3 3 Blocks 255 255 Blocks
7:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.104 MMC_CTLCFG_UHS2_GEN_CAP Register

1 MMC_CTLCFG_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

Start Address of General Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-30688. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0110h**
MMCSD2	**0FA2 0110h**

Figure 14-10168. MMC_CTLCFG_UHS2_GEN_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
CORECFG_UHS2_BUS_TOPLOGY		CORECFG_UHS2_MAX_DEVICES				DEVICE_TYPE	
R		R				R	
0h		1h				0h	

15	14	13	12	11	10	9	8
RESERVED	CFG_64BIT_ADDRESSING	NUM_LANES					
NONE	R	R					
0h	1h	Fh					

7	6	5	4	3	2	1	0
GAP				DAP			
R				R			
1h				1h			

Table 14-30690. MMC_CTLCFG_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:22	CORECFG_UHS2_BUS_TOPLOGY	R	0h	This field indicates one of bus topologies configured by a Host system. '00' P2P Connection '01' Ring Connection '10' HUB Connection '11' HUB is connected in Ring Reset Source: vbus_amod_g_rst_n 0 P2P Connection 1 Ring Connection 2 HUB Connection 3 HUB is connected in Ring

Table 14-30690. MMC_CTLCFG_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

21:18	CORECFG_UHS2_MAX_DEVICES	R	1h	This field indicates the maximum number of devices supported by the Host Controller.
				0h - Not used
				1h - 1 Devices
				2h - 2 Devices
				.....
				....
				Fh - 15 Devices
				Reset Source: vbus_amod_g_rst_n
				`0 Not used`
				`1 1 Device`
				`2 2 Devices`
				`15 15 Devices`

17:16	DEVICE_TYPE	R	0h	This field indicates device type configured by a Host system. '00' Removable Card[P2P] '01' Embedded Devices '10' Embedded Devices+Removable Card '11' Reserved Reset Source: vbus_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	This field indicates support of 64-bit addressing by the Host Controller. '0' 32-bit Addressing is supported '1' 32-bit and 64-bit Addressing is supported Reset Source: vbus_amod_g_rst_n
13:8	NUM_LANES	R	Fh	This field indicates support of lanes by the Host Controller.0 mean not supported and 1 means supported. D08 - 2L-HD D09 - 2D1U-FD D10 - 1D2U-FD D11 - 2D2U-FD D12 - Reserved D13 - Reserved Reset Source: vbus_amod_g_rst_n
7:4	GAP	R	1h	This field indicates the maximum capability of host power supply for a group configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -Not used 1h - 360 mW 2h - 720 mW .... Fh - 360x15 mW Reset Source: vbus_amod_g_rst_n
3:0	DAP	R	1h	This field indicates the maximum capability of host power supply for a device configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -360 mW [Default] 1h - 360 mW 2h - 720 mW .... Fh - 360 x15 mW Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.105 MMC_CTLCFG_UHS2_PHY_CAP Register

1 MMC_CTLCFG_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

Start Address of PHY Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-30691. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0114h**
MMCSD2	**0FA2 0114h**

Figure 14-10169. MMC_CTLCFG_UHS2_PHY_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
N_LSS_DIR				N_LSS_SYN			
R				R			
1h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_RANGE		RESERVED					
R		NONE					
0h		0h					

Table 14-30693. MMC_CTLCFG_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R	1h	This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R	1h	This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
15:8	RESERVED	NONE	0h	Reserved

Table 14-30693. MMC_CTLCFG_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SPEED_RANGE	R	0h	This field indicates supported Speed Range by the Host Controller '00' Range A [Default] '01' Range A and Range B '10' Reserved '11' Reserved Reset Source: vbus_amod_g_rst_n 0 Range A (Default) 1 Range A and Range B 2 Reserved 3 Reserved
5:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.106 MMC_CTLCFG_UHS2_LNK_TRN_CAP Register

1 MMC_CTLCFG_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Capabilities Register.

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Table 14-30694. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0118h**
MMCSD2	**0FA2 0118h**

Figure 14-10170. MMC_CTLCFG_UHS2_LNK_TRN_CAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R							
81h							
15	14	13	12	11	10	9	8
N_FCU							
R							
1h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30696. MMC_CTLCFG_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved

Table 14-30696. MMC_CTLCFG_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	N_DATA_GAP	R	81h	This field indicates the minimum number of data gap[DIDL] supported by the Host Controller. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS Reset Source: vbus_amod_g_rst_n 0 No Gap 1 1 LSS 2 2 LSS 3 3 LSS 255 255 LSS
31:20	MAX_BLK_LENGTH	R	200h	This field indicates maximum block length by the Host Controller. 000h - Not Used 001h - 1 byte 002h - 2 bytes .... 200h - 512 bytes .... 800h - 2048 bytes 801h-FFFh -Not Used Reset Source: vbus_amod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved
15:8	N_FCU	R	1h	This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller.This value is determined by supported buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Block 03h - 3 Block .... FFh - 255 Blocks Reset Source: vbus_amod_g_rst_n 0 256 Blocks 1 1 Block 2 2 Blocks 3 3 Blocks 255 255 Blocks
7:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.107 MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register

1 MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

This register is not physically implemented, rather it is an address where UHS-II Error Interrupt Status register can be written.

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Table 14-30697. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0120h**
MMCSD2	**0FA2 0120h**

Figure 14-10171. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Name Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
W					NONE		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
NONE						W	W
0h						0h	0h
15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W	NONE						W
0h	0h						0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30699. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h - Not Affected 1h - Vendor Specific Error Status is set Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved

17	TIMEOUT_DEADLOCK	W	0h	Setting this bit forces the Host Controller to set Timeout for Deadlock in the UHS-II Error Interrupt Status register.
				Reset Source: vbus_amod_g_rst_n
				`0       No Interrupt`
				`1       Timeout for Deadlock Error status is set`

16	TIMEOUT_CMD_RES	W	0h	Setting this bit forces the Host Controller to set Timeout for CMD_RES in the UHS-II Error Interrupt Status register.
				Reset Source: vbus_amod_g_rst_n
				`0       No Interrupt`
				`1       Timout for CMD_RES Status is set`

Table 14-30699. MMC_CTLCFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA	W	0h	Setting this bit forces the Host Controller to set ADMA Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `ADMA error status is set`
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	W	0h	Setting this bit forces the Host Controller to set EBSY Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `EBSY error status is set`
7	UNRECOVERABLE	W	0h	Setting this bit forces the Host Controller to set Unrecover-able Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Unrecoverable error status is set`
6	RESERVED	NONE	0h	Reserved
5	TID	W	0h	Setting this bit forces the Host Controller to set TID Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `TID error status is set`
4	FRAMING	W	0h	Setting this bit forces the Host Controller to set Framing Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Framing error status is set`
3	CRC	W	0h	Setting this bit forces the Host Controller to set CRC Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `CRC error status is set`
2	RETRY_EXPIRED	W	0h	Setting this bit forces the Host Controller to set Retry Expired in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Retry expired error status is set`
1	RES_PKT	W	0h	Setting this bit forces the Host Controller to set RES Packet Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `RES packet error status is set`
0	HEADER	W	0h	Setting this bit forces the Host Controller to set Header Error in the UHS-II Error Interrupt Status register. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Header error status is set`

14.9.4.7.2.108 MMC_CTLCFG_CQ_VERSION Register

1 MMC_CTLCFG_CQ_VERSION Register (Offset = 200h) [reset = 510h]

This register provides information about the version of the eMMC CQ standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1 The following table describes the CQBASE+00h: CQVReservedER Command Queueing Version.

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Table 14-30700. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0200h**
MMCSD2	**0FA2 0200h**

Figure 14-10172. MMC_CTLCFG_CQ_VERSION Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EMMC_MAJOR_VER_NUM			
NONE				R			
0h				5h			
7	6	5	4	3	2	1	0
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R				R			
1h				0h			

Table 14-30702. MMC_CTLCFG_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number [digit left of decimal point],in BCD format Reset Source: vbus_amod_g_rst_n
7:4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number [digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n
3:0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix [2nd digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.109 MMC_CTLCFG_CQ_CAPABILITIES Register

1 MMC_CTLCFG_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

This register is reserved for capability indication.

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Table 14-30703. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0204h**
MMCSD2	**0FA2 0204h**

Figure 14-10173. MMC_CTLCFG_CQ_CAPABILITIES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CF_MUL				RESERVED		CF_VAL	
R				NONE		R	
3h				0h		C8h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CF_VAL							
R							
C8h							

Table 14-30705. MMC_CTLCFG_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CF_MUL	R	3h	Internal Timer Clock Frequency Multiplier [ITCFMUL] ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the SQS polling period. See ITCFVAL definition for details. Field Value Description: 0h = 0.001 MHz 1h = 0.01 MHz 2h = 0.1 MHz 3h = 1 MHz 4h = 10 MHz Other values are reserved Reset Source: vbus_amod_g_rst_n 3 1 MHz 4 10 MHz
11:10	RESERVED	NONE	0h	Reserved

Table 14-30705. MMC_CTLCFG_CQ_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	CF_VAL	R	C8h	Internal Timer Clock Frequency Value [ITCFVAL] TCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the polling period when using periodic SEND_QUEUE_ STATUS [CMD13] polling. The clock frequency is calculated as ITCFVAL*ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h [= 192 decimal] and ITCFMUL shall be 2h [0.1 MHz 192 * 0.1 MHz 19.2 MHz] Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.110 MMC_CTLCFG_CQ_CONFIG Register

1 MMC_CTLCFG_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

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Table 14-30706. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0208h**
MMCSD2	**0FA2 0208h**

Figure 14-10174. MMC_CTLCFG_CQ_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>DCMD_ENA</td><td colspan="3">RESERVED</td><td>TASK_DESC_SIZE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CQ_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30708. MMC_CTLCFG_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	DCMD_ENA	R/W	0h	Direct Command [DCMD] Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descrip-tor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor Reset Source: vbus_amod_g_rst_n 0 Task descriptor in slot #31 is a Data Transfer Task Descriptor 1 Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RESERVED	NONE	0h	Reserved

Table 14-30708. MMC_CTLCFG_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TASK_DESC_SIZE	R/W	0h	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queueing Enable bit is 0 [command queueing is disabled] Bit Value Description 1 = Task descriptor size is 128 bits 0 = Task descriptor size is 64 bits Reset Source: vbus_amod_g_rst_n 0 `Task descriptor size is 64 bits` 1 `Task descriptor size is 128 bits`
7:1	RESERVED	NONE	0h	Reserved
0	CQ_ENABLE	R/W	0h	Command Queueing Enable Software shall write 1 this bit when in order to enable command queueing mode [i.e. enable CQE]. When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queueing mode,it shall clear all previous tasks if such exist before setting this bit to 0. Reset Source: vbus_amod_g_rst_n 0 `Command Queueing mode is Disabled` 1 `Command Queueing mode is Enabled`

14.9.4.7.2.111 MMC_CTLCFG_CQ_CONTROL Register

1 MMC_CTLCFG_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

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Table 14-30709. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 020Ch**
MMCSD2	**0FA2 020Ch**

Figure 14-10175. MMC_CTLCFG_CQ_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CLEAR_ALL_TASKS
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							HALT_BIT
NONE							R/W
0h							0h

Table 14-30711. MMC_CTLCFG_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	Clear All Tasks Software shall write 1 this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state [i.e.Halt bit is 1]. When software writes 1, the value of the register is updated to 1, and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit.Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect. Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-30711. MMC_CTLCFG_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	Halt Host software shall write 1 to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command [CMDQ_TASK_MGMT] When software writes 1, CQE shall complete the ongo-ing task if such a task is in progress. Once the task is completed and CQE is in idle state,CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state [i.e. resume CQE activity], soft-ware shall clear this bit [write 0]. Writing 0 when thevalue is already 0 shall have no effect. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.112 MMC_CTLCFG_CQ_INTR_STS Register

1 MMC_CTLCFG_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in CQ ISTE register.

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Table 14-30712. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0210h**
MMCSD2	**0FA2 0210h**

Figure 14-10176. MMC_CTLCFG_CQ_INTR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-30714. MMC_CTLCFG_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W1TC	0h	Task Error Interrupt [TERR] This bit is asserted when task error is detected due to invalid task descriptor Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Task Error interrupt is generated`
3	TASK_CLEARED	R/W1TC	0h	Task Cleared [TCL] This status bit is asserted [if CQISTE.TCL=1] when a task clear operation is completed by CQE. The com-pleted task clear operation is either an individual task clear [CQTCLR] or clearing of all tasks [CQCTL]. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Task clear interrupt is generated`

Table 14-30714. MMC_CTLCFG_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W1TC	0h	Response Error Detected Interrupt [RED] This status bit is asserted [if CQISTE.RED=1] when a response is received with an error bit set in the device status field. The contents of the device status field are listed in Section 6.13.Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Reset Source: vbus_amod_g_rst_n
1	TASK_COMPLETE	R/W1TC	0h	Task Complete Interrupt [TCC] This status bit is asserted [if CQISTE.TCC=1] when atleast one of the following two conditions are met: [1] A task is completed and the INT bit is set in its Task Descriptor [2] Interrupt caused by Interrupt Coalescing logic [see Section C.4.9] Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Task complete interrupt is generated`
0	HALT_COMPLETE	R/W1TC	0h	Halt Complete Interrupt [HAC] This status bit is asserted [if CQISTE.HAC=1] when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state. Reset Source: vbus_amod_g_rst_n 0 `No Interrupt` 1 `Halt complete interrupt is generated`

14.9.4.7.2.113 MMC_CTLCFG_CQ_INTR_STS_ENA Register

1 MMC_CTLCFG_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

This register enables and disables the reporting of the corresponding interrupt to host soft-ware in 299 CQIS register. When a bit is set (1) and the corresponding interrupt c -ondition is active, then the 300 bit is CQIS is asserted. Interrupt sources that are disabled (0) are not indicated in the CQIS 301 register. This register is bit-index matched to CQIS register.

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Table 14-30715. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0214h**
MMCSD2	**0FA2 0214h**

Figure 14-10177. MMC_CTLCFG_CQ_INTR_STS_ENA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-30717. MMC_CTLCFG_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Status Enable 1 = CQIS.TERR will be set when its interrupt condition is active 0 = CQIS.TERR is disabled Reset Source: vbus_amod_g_rst_n 0 1
3	TASK_CLEARED	R/W	0h	Task Cleared Status Enable [TCL] 1 = CQIS.TCL will be set when its interrupt condition is active 0 = CQIS.TCL is disabled Reset Source: vbus_amod_g_rst_n 0 1

Table 14-30717. MMC_CTLCFG_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	Response Error Detected Status Enable [RED] 1 = CQIS.RED will be set when its interrupt condition is active 0 = CQIS.RED is disabled Reset Source: vbus_amod_g_rst_n 0 1
1	TASK_COMPLETE	R/W	0h	Task Complete Status Enable [TCC] 1 = CQIS.TCC will be set when its interrupt condition is active 0 = CQIS.TCC is disabled Reset Source: vbus_amod_g_rst_n 0 1
0	HALT_COMPLETE	R/W	0h	Halt Complete Status Enable [HAC] 1 = CQIS.HAC will be set when its interrupt condition is active 0 = CQIS.HAC is disabled Reset Source: vbus_amod_g_rst_n 0 1

14.9.4.7.2.114 MMC_CTLCFG_CQ_INTR_SIG_ENA Register

1 MMC_CTLCFG_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1) and the corresponding bit in CQIS is set, then an interrupt is gene -rated. Interrupt sources 305 that are disabled (0) are still indicated in the CQIS register. This register is bit-index matched 306 to CQIS register.

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Table 14-30718. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0218h**
MMCSD2	**0FA2 0218h**

Figure 14-10178. MMC_CTLCFG_CQ_INTR_SIG_ENA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-30720. MMC_CTLCFG_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Signal Enable [TERR] When set and CQIS.TERR is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
3	TASK_CLEARED	R/W	0h	Task Cleared Signal Enable [TCL] When set and CQIS.TCL is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1

Table 14-30720. MMC_CTLCFG_CQ_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	Response Error Detected Signal Enable [TCC] When set and CQIS.RED is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
1	TASK_COMPLETE	R/W	0h	Task Complete Signal Enable [TCC] When set and CQIS.TCC is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1
0	HALT_COMPLETE	R/W	0h	Halt Complete Signal Enable [HAC] When set and CQIS.HAC is asserted, the CQE shall generate an interrupt Reset Source: vbus_amod_g_rst_n 0 1

14.9.4.7.2.115 MMC_CTLCFG_CQ_INTR_COALESCING Register

1 MMC_CTLCFG_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

This register controls the interrupt coalescing feature.

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Table 14-30721. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 021Ch**
MMCSD2	**0FA2 021Ch**

Figure 14-10179. MMC_CTLCFG_CQ_INTR_COALESCING Name Register

31	30	29	28	27	26	25	24
CQINTCOALESC_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			IC_STATUS	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			CTR_THRESHOLD				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TIMEOUT_VAL						
NONE	R/W						
0h	0h						

Table 14-30723. MMC_CTLCFG_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated. Reset Source: vbus_amod_g_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	IC_STATUS	R	0h	This bit indicates to software whether any tasks [with INT=0] have completed and counted towards interrupt coalescing [i.e., ICSB is set if and only if IC counter > 0]. Bit Value Description 1 = At least one task completion has been counted [IC counter >0] 0 = No task completions have occurred since last counter reset [IC counter =0] Reset Source: vbus_amod_g_rst_n
19:13	RESERVED	NONE	0h	Reserved

Table 14-30723. MMC_CTLCFG_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	CTR_THRESHOLD	R/W	0h	Interrupt Coalescing Counter Threshold [ICCTH]: Software uses this field to configure the number of task completions [only tasks with INT=0 in the Task Descriptor] which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 NOTE : When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated.In order to write to this field, the ICCTHWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TIMEOUT_VAL	R/W	0h	Interrupt Coalescing Timeout Value [ICTOVAL]: Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register.The minimum value is 01h [1024 clock periods] and the maximum value is 7Fh [127*1024 clock periods]. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us NOTE: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.116 MMC_CTLCFG_CQ_TDL_BASE_ADDR Register

1 MMC_CTLCFG_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

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Table 14-30724. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0220h**
MMCSD2	**0FA2 0220h**

Figure 14-10180. MMC_CTLCFG_CQ_TDL_BASE_ADDR Name Register

31	30	29	28	27	26	25	24
CQTDLBA_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CQTDLBA_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CQTDLBA_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CQTDLBA_LO							
R/W							
0h							

Table 14-30726. MMC_CTLCFG_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_LO	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the LSB bits [bits 31:0] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This address shall be set on Byte1 KByte boundary.: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.117 MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register

1 MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

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Table 14-30727. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0224h**
MMCSD2	**0FA2 0224h**

Figure 14-10181. MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Name Register

31	30	29	28	27	26	25	24
CQTDLBA_HI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CQTDLBA_HI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CQTDLBA_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CQTDLBA_HI							
R/W							
0h							

Table 14-30729. MMC_CTLCFG_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_HI	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the MSB bits [bits 63:32] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This register is reserved when using 32-bit addressing mode. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.118 MMC_CTLCFG_CQ_TASK_DOOR_BELL Register

1 MMC_CTLCFG_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

Using this register, software triggers CQE to process a new task.

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Table 14-30730. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0228h**
MMCSD2	**0FA2 0228h**

Figure 14-10182. MMC_CTLCFG_CQ_TASK_DOOR_BELL Name Register

31	30	29	28	27	26	25	24
CQTDB_VAL							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
CQTDB_VAL							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
CQTDB_VAL							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
CQTDB_VAL							
R/W1TS							
0h							

Table 14-30732. MMC_CTLCFG_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDB_VAL	R/W1TS	0h	Command Queueing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start pro-cessing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transac-tions. CQE processes Data Transfer tasks by Reading the Task Descriptor and sending QUEUED_TASK_PARAMS[CMD44] and QUEUED_TASK_ADDRESS [CMD45]commands to the device. CQE processes DCMD tasks [in slot #31, when enabled]by Reading the Task Descriptor, and generating the com-mand encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: [a] When a task execution is completed [with success or error] [b] The task is cleared using CQTCLR register [c] All tasks are cleared using CQCTL register [d] CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time [batch submission] by Writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index,starting with the lowest index. If one or more tasks in the batch are marked with QBR,the ordering of execution will be based on said process-ing order. Writing 0 by software shall have no impact on the hard-ware, and will not change the value of the register bit. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.119 MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register

1 MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

This register is used by CQE to notify software about completed tasks.

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Table 14-30733. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 022Ch**
MMCSD2	**0FA2 022Ch**

Figure 14-10183. MMC_CTLCFG_CQ_TASK_COMP_NOTIF Name Register

31	30	29	28	27	26	25	24
CQTCN_VAL							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CQTCN_VAL							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CQTCN_VAL							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CQTCN_VAL							
R/W1TC							
0h							

Table 14-30735. MMC_CTLCFG_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCN_VAL	R/W1TC	0h	CQE shall set bit n of this register [at the same time it clears bit n of CQTDBR] when a task execution is com-pleted [with success or error]. When receiving interrupt for task completion, software may read this register to know which tasks have finished. After Reading this register, software may clear the rele-vant bit fields by Writing 1 to the corresponding bits. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.120 MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register

1 MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

This register stores the most recent value of the device s queue status.

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Table 14-30736. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0230h**
MMCSD2	**0FA2 0230h**

Figure 14-10184. MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CQDQ_STS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CQDQ_STS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CQDQ_STS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CQDQ_STS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30738. MMC_CTLCFG_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDQ_STS	R	0h	Every time the Host controller receives a queue status register [QSR] from the device, it updates this register with the response of status command, i.e. the devices queue status. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.121 MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register

1 MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

This register indicates to software which tasks are queued in the device, awaiting execution.

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Table 14-30739. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0234h**
MMCSD2	**0FA2 0234h**

Figure 14-10185. MMC_CTLCFG_CQ_DEV_PENDING_TASKS Name Register

31	30	29	28	27	26	25	24
CQDP_TSKS							
R							
0h							
23	22	21	20	19	18	17	16
CQDP_TSKS							
R							
0h							
15	14	13	12	11	10	9	8
CQDP_TSKS							
R							
0h							
7	6	5	4	3	2	1	0
CQDP_TSKS							
R							
0h							

Table 14-30741. MMC_CTLCFG_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDP_TSKS	R	0h	Bit n of this register is set if and only if QUEUED_TASK_PARAMS [CMD44] and QUEUED_TASK_ADDRESS [CMD45] were sent for this specific task and if this task hasnt been executed yet.CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution.Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued,the driver sends a CMDQ_TASK_MGMT [CMD48] to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.122 MMC_CTLCFG_CQ_TASK_CLEAR Register

1 MMC_CTLCFG_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

This register is used for removing an outstanding task in the CQE. 327. The register should be used only when CQE is in Halt state.

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Table 14-30742. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0238h**
MMCSD2	**0FA2 0238h**

Figure 14-10186. MMC_CTLCFG_CQ_TASK_CLEAR Name Register

31	30	29	28	27	26	25	24
CQTCLR							
R/W							
0h							
23	22	21	20	19	18	17	16
CQTCLR							
R/W							
0h							
15	14	13	12	11	10	9	8
CQTCLR							
R/W							
0h							
7	6	5	4	3	2	1	0
CQTCLR							
R/W							
0h							

Table 14-30744. MMC_CTLCFG_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCLR	R/W	0h	Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued.This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit.When software writes 1 to a bit in this register,CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields [sets a value of 0] in CQTCLR and in CQTDBR once clear operation is complete.Software should poll on the CQTCLR until it is cleared to verify clear operation was complete.Writing to this register only clears the task in the CQE and does not have impact on the device. In order to dis-card the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state.Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQTCL register.Writing 0 to a register bit shall have no impact. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.123 MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register

1 MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

The register controls the when SEND_QUEUE_STATUS commands are sent.

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Table 14-30745. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0240h**
MMCSD2	**0FA2 0240h**

Figure 14-10187. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CMD_BLK_CNTR			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
CMD_IDLE_TIMER							
R/W							
1000h							
7	6	5	4	3	2	1	0
CMD_IDLE_TIMER							
R/W							
1000h							

Table 14-30747. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	CMD_BLK_CNTR	R/W	1h	This field indicates to CQE when to send SEND_QUEUE_STATUS [CMD13] command to inquire the status of the devices task queue.A value of n means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction.A value of 0 means that SEND_QUEUE_STATUS [CMD13] command shall not be sent during the transac-tion. Instead it will be sent only when the data lines are idle.A value of 1 means that STATUS command is to be sent during the last block of the transaction. Reset Source: vbus_amod_g_rst_n

Table 14-30747. MMC_CTLCFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	CMD_IDLE_TIMER	R/W	1000h	This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS [CMD13] polling.Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS.Timer units are clock periods of theclock whose fre-quency is specified in the Internal Timer Clock Fre-quency field CQCAP register.The minimum value is 0001h [1 clock period] and the maximum value is FFFFh [65535 clock periods]. Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in CQSST is 1000h, the calcu.lated polling period is 4096*52.08 ns= 213.33 us. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.124 MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register

1 MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argu-ment.

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Table 14-30748. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0244h**
MMCSD2	**0FA2 0244h**

Figure 14-10188. MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_RCA							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_RCA							
R/W							
0h							

Table 14-30750. MMC_CTLCFG_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_RCA	R/W	0h	This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS [CMD13] com-mand. argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS [CMD13] command. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.125 MMC_CTLCFG_CQ_DCMD_RESPONSE Register

1 MMC_CTLCFG_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

This register is used for passing the response of a DCMD task to software.

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Table 14-30751. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0248h**
MMCSD2	**0FA2 0248h**

Figure 14-10189. MMC_CTLCFG_CQ_DCMD_RESPONSE Name Register

31	30	29	28	27	26	25	24
LAST_RESP							
R							
0h							
23	22	21	20	19	18	17	16
LAST_RESP							
R							
0h							
15	14	13	12	11	10	9	8
LAST_RESP							
R							
0h							
7	6	5	4	3	2	1	0
LAST_RESP							
R							
0h							

Table 14-30753. MMC_CTLCFG_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_RESP	R	0h	This register contains the response of the command generated by the last direct-command [DCMD] task which was sent.CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQT-DBR register is cleared by CQE. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.126 MMC_CTLCFG_CQ_RESP_ERR_MASK Register

1 MMC_CTLCFG_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

This register controls the generation of Response Error Detection (RED) interrupt.

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Table 14-30754. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0250h**
MMCSD2	**0FA2 0250h**

Figure 14-10190. MMC_CTLCFG_CQ_RESP_ERR_MASK Name Register

31	30	29	28	27	26	25	24
CQRMEM							
R/W							
FDF9A080h							
23	22	21	20	19	18	17	16
CQRMEM							
R/W							
FDF9A080h							
15	14	13	12	11	10	9	8
CQRMEM							
R/W							
FDF9A080h							
7	6	5	4	3	2	1	0
CQRMEM							
R/W							
FDF9A080h							

Table 14-30756. MMC_CTLCFG_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQRMEM	R/W	FDF9A080h	This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses.Bit Value Description [for any bit i]:1 = When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0 = When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an inter-rupt on all Error type bits in the device status, as defined in Section 6.13.NOTE: Responses to CMD13 [SQS] encode the QSR,so they are ignored by this logic Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.127 MMC_CTLCFG_CQ_TASK_ERR_INFO Register

1 MMC_CTLCFG_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.Software is expected to use this information in the error recovery procedure.

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Table 14-30757. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0254h**
MMCSD2	**0FA2 0254h**

Figure 14-10191. MMC_CTLCFG_CQ_TASK_ERR_INFO Name Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED		DATERR_TASK_ID				
R	NONE		R				
0h	0h		0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		DATERR_CMD_INDEX					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESP_MODE_VALID	RESERVED		RESP_MODE_TASK_ID				
R	NONE		R				
0h	0h		0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RESP_MODE_CMD_INDEX					
NONE		R					
0h		0h					

Table 14-30759. MMC_CTLCFG_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/ indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
30:29	RESERVED	NONE	0h	Reserved
28:24	DATERR_TASK_ID	R	0h	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller Reset Source: vbus_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-30759. MMC_CTLCFG_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	DATERR_CMD_INDEX	R	0h	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK[CMD46] or EXECUTE_WRITE_TASK [CMD47] accord-ing to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
15	RESP_MODE_VALID	R	0h	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/ indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
14:13	RESERVED	NONE	0h	Reserved
12:8	RESP_MODE_TASK_ID	R	0h	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	RESP_MODE_CMD_INDEX	R	0h	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.128 MMC_CTLCFG_CQ_CMD_RESP_INDEX Register

1 MMC_CTLCFG_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-30760. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0258h**
MMCSD2	**0FA2 0258h**

Figure 14-10192. MMC_CTLCFG_CQ_CMD_RESP_INDEX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">LAST_CRI</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-30762. MMC_CTLCFG_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	LAST_CRI	R	0h	This field stores the index of the last received command response. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.129 MMC_CTLCFG_CQ_CMD_RESP_ARG Register

1 MMC_CTLCFG_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-30763. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 025Ch**
MMCSD2	**0FA2 025Ch**

Figure 14-10193. MMC_CTLCFG_CQ_CMD_RESP_ARG Name Register

31	30	29	28	27	26	25	24
LAST_CRA							
R							
0h							
23	22	21	20	19	18	17	16
LAST_CRA							
R							
0h							
15	14	13	12	11	10	9	8
LAST_CRA							
R							
0h							
7	6	5	4	3	2	1	0
LAST_CRA							
R							
0h							

Table 14-30765. MMC_CTLCFG_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_CRA	R	0h	This field stores the argument of the last received com-mand. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.130 MMC_CTLCFG_CQ_ERROR_TASK_ID Register

1 MMC_CTLCFG_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

CQ Error Task ID Register

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Table 14-30766. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 0260h**
MMCSD2	**0FA2 0260h**

Figure 14-10194. MMC_CTLCFG_CQ_ERROR_TASK_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TERR_ID				
NONE			R				
0h			0h				

Table 14-30768. MMC_CTLCFG_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	TERR_ID	R	0h	Task Error ID Reset Source: vbus_amod_g_rst_n

14.9.4.7.2.131 MMC_SSCFG_SS_ID_REV_REG Register

1 MMC_SSCFG_SS_ID_REV_REG Register (Offset = 0h) [reset = 68403A00h]

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem

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Table 14-30769. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8000h**
MMCSD2	**0FA2 8000h**

Figure 14-10195. MMC_SSCFG_SS_ID_REV_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6840h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6840h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJ_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MIN_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-30771. MMC_SSCFG_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MOD_ID	R	6840h	Module ID Reset Source: vbus_smod_g_rst_n
15:11	RTL_VER	R	7h	RTL version Reset Source: vbus_smod_g_rst_n
10:8	MAJ_REV	R	2h	Major revision Reset Source: vbus_smod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_smod_g_rst_n
5:0	MIN_REV	R	0h	Minor revision Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.132 MMC_SSCFG_CTL_CFG_1_REG Register

1 MMC_SSCFG_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

The Controller Config 1 Register contains various fields to control the configuration ports on the eMMC/SD Controller.

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Table 14-30772. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8010h**
MMCSD2	**0FA2 8010h**

Figure 14-10196. MMC_SSCFG_CTL_CFG_1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TUNINGCOUNT</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>ASYNCWKUPENA</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CQFMUL</td><td colspan="2">RESERVED</td><td colspan="2">CQFVAL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">3h</td><td colspan="2">0h</td><td colspan="2">C8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CQFVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C8h</td></tr>
</table>

Table 14-30774. MMC_SSCFG_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TUNINGCOUNT	R/W	20h	Configures the Number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure. Reset Source: vbus_smod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0: Synchronous Wakeup Mode: The xin_clk has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the xin_clk and the Wakeup Event is generated. The Assertion and deassertion of the wakeup Event signal synchronous to xin_clk. 1: Asyncrhonous Wakeup Mode: The xin_clk and the host_clk can be stopped in this mode and the Wake up Event is asynchronously generated based on the Card Insertion/Removal/Interrupt Events. The Assertion and deassertion of the wakeup Event signal is asynchronous. Reset Source: vbus_smod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved

Table 14-30774. MMC_SSCFG_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.133 MMC_SSCFG_CTL_CFG_2_REG Register

1 MMC_SSCFG_CTL_CFG_2_REG Register (Offset = 14h) [reset = 25E8C801h]

The Controller Config 2 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the lsb fields in the Capabilities Register inside the eMMC/SD Controller.

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Table 14-30775. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8014h**
MMCSD2	**0FA2 8014h**

Figure 14-10197. MMC_SSCFG_CTL_CFG_2_REG Name Register

31	30	29	28	27	26	25	24
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W		R/W	NONE		R/W	R/W	R/W
0h		1h	0h		1h	0h	1h
23	22	21	20	19	18	17	16
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W	R/W	R/W	NONE	R/W	R/W	R/W	
1h	1h	1h	0h	1h	0h	0h	
15	14	13	12	11	10	9	8
BASECLKFREQ							
R/W							
C8h							
7	6	5	4	3	2	1	0
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W	NONE	R/W					
0h	0h	1h					

Table 14-30777. MMC_SSCFG_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SLOTTYPE	R/W	0h	Slot Type. Should be set based on the final product usage. 00 - Removable SCard Slot, 01 - Embedded Slot for One Device, 10 - Shared Bus Slot, 11 - Reserved. Reset Source: vbus_smod_g_rst_n
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support. Suggested Value is 1'b1 (The Core supports monitoring of Asynchronous Interrupt). Reset Source: vbus_smod_g_rst_n
28:27	RESERVED	NONE	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8V Support. Suggested Value is 1'b1 (The 1.8 Volt Switching is supported by Core). Optionally can be set to 1'b0 if the application doesn't want 1.8V switching (SD3.0). Reset Source: vbus_smod_g_rst_n
25	SUPPORT3P0VOLT	R/W	0h	3.0V Support. Should be set based on whether 3.0V is supported on the SD Interface. Reset Source: vbus_smod_g_rst_n

Table 14-30777. MMC_SSCFG_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SUPPORT3P3VOLT	R/W	1h	3.3V Support. Suggested Value is 1'b1 as the 3.3 V is the default voltage on the SD Interface. Reset Source: vbus_smod_g_rst_n
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support. Suggested Value is 1'b1 (The Suspend/ Resume is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support Suspend/Resume Mode. Reset Source: vbus_smod_g_rst_n
22	SDMASUPPORT	R/W	1h	SDMA Support. Suggested Value is 1'b1 (The SDMA is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support SDMA Mode. Reset Source: vbus_smod_g_rst_n
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support. Suggested Value is 1'b1 (The High Speed mode is supported by Core). Reset Source: vbus_smod_g_rst_n
20	RESERVED	NONE	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support. Suggested Value is 1'b1 (The ADMA2 is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support ADMA2 Mode. Reset Source: vbus_smod_g_rst_n
18	SUPPORT8BIT	R/W	0h	8-bit Support for Embedded Device. Suggested Value is 1'b1 (The Core supports 8-bit Interface). Optionally an be set to 1'b0 if the Application supports only 4-bit SD Interface. Reset Source: vbus_smod_g_rst_n
17:16	MAXBLKLENGTH	R/W	0h	Max Block Length. Maximum Block Length supported by the Core/ Device. 00: 512 (Bytes), 01: 1024, 10: 2048, 11: Reserved. Reset Source: vbus_smod_g_rst_n
15:8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock. This is the frequency of the xin_clk. Reset Source: vbus_smod_g_rst_n
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit. Suggested Value is 1'b0 (KHz). Reset Source: vbus_smod_g_rst_n
6	RESERVED	NONE	0h	Reserved
5:0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency. Suggested Value is 1 KHz. Internally the 1msec Timer is used for Timeout Detection. The 1msec Timer is generated from the xin_clk. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.134 MMC_SSCFG_CTL_CFG_3_REG Register

1 MMC_SSCFG_CTL_CFG_3_REG Register (Offset = 18h) [reset = 18000407h]

The Controller Config 3 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the msb fields in the Capabilities Register inside the eMMC/SD Controller.

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Table 14-30778. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8018h**
MMCSD2	**0FA2 8018h**

Figure 14-10198. MMC_SSCFG_CTL_CFG_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			SUPPORT1P8VDD2	ADMA3SUPPORT	RESERVED		
NONE			R/W	R/W	NONE		
0h			1h	1h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLOCKMULTIPLIER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RETUNINGMODES		TUNINGFORSDR50	RESERVED	RETUNINGTIMERCNT			
R/W		R/W	NONE	R/W			
0h		0h	0h	4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TYPE4SUPPORT	DDRIVERSUPPORT	CDRIVERSUPPORT	ADRIVERSUPPORT	RESERVED	DDR50SUPPORT	SDR104SUPPORT	SDR50SUPPORT
R/W	R/W	R/W	R/W	NONE	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	1h	1h

Table 14-30780. MMC_SSCFG_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8V VDD2 Support. Reset Source: vbus_smod_g_rst_n
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support. Reset Source: vbus_smod_g_rst_n
26:24	RESERVED	NONE	0h	Reserved
23:16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier. This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. FFh Clock Multiplier M = 256, ..., 02h Clock Multiplier M = 3, 01h Clock Multiplier M = 2, 00h Clock Multiplier is Not Supported. Reset Source: vbus_smod_g_rst_n
15:14	RETUNINGMODES	R/W	0h	Re-Tuning Modes. Should be set to 2'b00 as the Core supports only the Software Timer based Re-Tuning. Reset Source: vbus_smod_g_rst_n

Table 14-30780. MMC_SSCFG_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50. This bit should be set if the Application wants Tuning be used for SDR50 Modes. The Core operates with or with out tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay. Reset Source: vbus_smod_g_rst_n
12	RESERVED	NONE	0h	Reserved
11:8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning. This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer. Reset Source: vbus_smod_g_rst_n
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support. This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support. This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support. This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support. This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	DDR50SUPPORT	R/W	1h	DDR50 Support. Suggested Value is 1'b1 (The Core supports DDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support DDR50. Reset Source: vbus_smod_g_rst_n
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1'b1 (The Core supports SDR104 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR104. Reset Source: vbus_smod_g_rst_n
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1'b1 (The Core supports SDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.135 MMC_SSCFG_CTL_CFG_4_REG Register

1 MMC_SSCFG_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

The Controller Config 4 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the lsb fields in the Maximum Current Capabilities Register inside the eMMC/SD Controller.

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Table 14-30781. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 801Ch**
MMCSD2	**0FA2 801Ch**

Figure 14-10199. MMC_SSCFG_CTL_CFG_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAXCURRENT1P8V							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXCURRENT3P0V							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXCURRENT3P3V							
R/W							
0h							

Table 14-30783. MMC_SSCFG_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAXCURRENT1P8V	R/W	0h	Maximum Current for 1.8V. Reset Source: vbus_smod_g_rst_n
15:8	MAXCURRENT3P0V	R/W	0h	Maximum Current for 3.0V. Reset Source: vbus_smod_g_rst_n
7:0	MAXCURRENT3P3V	R/W	0h	Maximum Current for 3.3V. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.136 MMC_SSCFG_CTL_CFG_5_REG Register

1 MMC_SSCFG_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

The Controller Config 5 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the msb fields in the Maximum Current Capabilities Register inside the eMMC/SD Controller.

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Table 14-30784. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8020h**
MMCSD2	**0FA2 8020h**

Figure 14-10200. MMC_SSCFG_CTL_CFG_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MAXCURRENTVDD2							
R/W							
0h							

Table 14-30786. MMC_SSCFG_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MAXCURRENTVDD2	R/W	0h	Maximum Current for 1.8 V (VDD2). Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.137 MMC_SSCFG_CTL_CFG_6_REG Register

1 MMC_SSCFG_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

The Controller Config 6 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for Initialization inside the eMMC/SD Controller.

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Table 14-30787. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8024h**
MMCSD2	**0FA2 8024h**

Figure 14-10201. MMC_SSCFG_CTL_CFG_6_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			INITPRESETVAL				
NONE			R/W				
0h			100h				
7	6	5	4	3	2	1	0
INITPRESETVAL							
R/W							
100h							

Table 14-30789. MMC_SSCFG_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	INITPRESETVAL	R/W	100h	Preset Value for Initialization. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.138 MMC_SSCFG_CTL_CFG_7_REG Register

1 MMC_SSCFG_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

The Controller Config 7 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for Default Speed inside the eMMC/SD Controller.

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Table 14-30790. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8028h**
MMCSD2	**0FA2 8028h**

Figure 14-10202. MMC_SSCFG_CTL_CFG_7_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			DSPDPRESETVAL				
NONE			R/W				
0h			4h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DSPDPRESETVAL							
R/W							
4h							

Table 14-30792. MMC_SSCFG_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	DSPDPRESETVAL	R/W	4h	Preset Value for Default Speed. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.139 MMC_SSCFG_CTL_CFG_8_REG Register

1 MMC_SSCFG_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

The Controller Config 8 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for High Speed inside the eMMC/SD Controller.

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Table 14-30793. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 802Ch**
MMCSD2	**0FA2 802Ch**

Figure 14-10203. MMC_SSCFG_CTL_CFG_8_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			HSPDPRESETVAL				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
HSPDPRESETVAL							
R/W							
2h							

Table 14-30795. MMC_SSCFG_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	HSPDPRESETVAL	R/W	2h	Preset Value for High Speed. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.140 MMC_SSCFG_CTL_CFG_9_REG Register

1 MMC_SSCFG_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

The Controller Config 9 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR12 inside the eMMC/SD Controller.

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Table 14-30796. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8030h**
MMCSD2	**0FA2 8030h**

Figure 14-10204. MMC_SSCFG_CTL_CFG_9_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR12PRESETVAL				
NONE			R/W				
0h			4h				
7	6	5	4	3	2	1	0
SDR12PRESETVAL							
R/W							
4h							

Table 14-30798. MMC_SSCFG_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR12PRESETVAL	R/W	4h	Preset Value for SDR12. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.141 MMC_SSCFG_CTL_CFG_10_REG Register

1 MMC_SSCFG_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

The Controller Config 10 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR25 inside the eMMC/SD Controller.

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Table 14-30799. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8034h**
MMCSD2	**0FA2 8034h**

Figure 14-10205. MMC_SSCFG_CTL_CFG_10_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR25PRESETVAL				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
SDR25PRESETVAL							
R/W							
2h							

Table 14-30801. MMC_SSCFG_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR25PRESETVAL	R/W	2h	Preset Value for SDR25. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.142 MMC_SSCFG_CTL_CFG_11_REG Register

1 MMC_SSCFG_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

The Controller Config 11 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR50 inside the eMMC/SD Controller.

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Table 14-30802. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8038h**
MMCSD2	**0FA2 8038h**

Figure 14-10206. MMC_SSCFG_CTL_CFG_11_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR50PRESETVAL				
NONE			R/W				
0h			1h				
7	6	5	4	3	2	1	0
SDR50PRESETVAL							
R/W							
1h							

Table 14-30804. MMC_SSCFG_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR50PRESETVAL	R/W	1h	Preset Value for SDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.143 MMC_SSCFG_CTL_CFG_12_REG Register

1 MMC_SSCFG_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

The Controller Config 12 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for SDR104 inside the eMMC/SD Controller.

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Table 14-30805. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 803Ch**
MMCSD2	**0FA2 803Ch**

Figure 14-10207. MMC_SSCFG_CTL_CFG_12_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SDR104PRESETVAL				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
SDR104PRESETVAL							
R/W							
0h							

Table 14-30807. MMC_SSCFG_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR104PRESETVAL	R/W	0h	Preset Value for SDR104. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.144 MMC_SSCFG_CTL_CFG_13_REG Register

1 MMC_SSCFG_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

The Controller Config 13 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for DDR50 inside the eMMC/SD Controller.

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Table 14-30808. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8040h**
MMCSD2	**0FA2 8040h**

Figure 14-10208. MMC_SSCFG_CTL_CFG_13_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DDR50PRESETVAL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DDR50PRESETVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-30810. MMC_SSCFG_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	DDR50PRESETVAL	R/W	2h	Preset Value for DDR50. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.145 MMC_SSCFG_CTL_CFG_14_REG Register

1 MMC_SSCFG_CTL_CFG_14_REG Register (Offset = 44h) [reset = 0h]

The Controller Config 14 Register contains various fields to control the configuration ports on the eMMC/SD Controller. This register sets the fields in the Preset Values Register for HS400 inside the eMMC/SD Controller.

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Table 14-30811. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8044h**
MMCSD2	**0FA2 8044h**

Figure 14-10209. MMC_SSCFG_CTL_CFG_14_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30813. MMC_SSCFG_CTL_CFG_14_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.146 MMC_SSCFG_CTL_STAT_1_REG Register

1 MMC_SSCFG_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30814. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8060h**
MMCSD2	**0FA2 8060h**

Figure 14-10210. MMC_SSCFG_CTL_STAT_1_REG Name Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMADEBUGBUS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMADEBUGBUS							
R							
0h							

Table 14-30816. MMC_SSCFG_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable S/W to gate off the clocks. Reset Source: vbus_smod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.147 MMC_SSCFG_CTL_STAT_2_REG Register

1 MMC_SSCFG_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30817. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8064h**
MMCSD2	**0FA2 8064h**

Figure 14-10211. MMC_SSCFG_CTL_STAT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CMDDEBUGBUS							
R							
10h							
7	6	5	4	3	2	1	0
CMDDEBUGBUS							
R							
10h							

Table 14-30819. MMC_SSCFG_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.148 MMC_SSCFG_CTL_STAT_3_REG Register

1 MMC_SSCFG_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30820. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8068h**
MMCSD2	**0FA2 8068h**

Figure 14-10212. MMC_SSCFG_CTL_STAT_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TXDDEBUGBUS							
R							
0h							
7	6	5	4	3	2	1	0
TXDDEBUGBUS							
R							
0h							

Table 14-30822. MMC_SSCFG_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.149 MMC_SSCFG_CTL_STAT_4_REG Register

1 MMC_SSCFG_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30823. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 806Ch**
MMCSD2	**0FA2 806Ch**

Figure 14-10213. MMC_SSCFG_CTL_STAT_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RXDDEBUGBUS0							
R							
0h							
7	6	5	4	3	2	1	0
RXDDEBUGBUS0							
R							
0h							

Table 14-30825. MMC_SSCFG_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK). Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.150 MMC_SSCFG_CTL_STAT_5_REG Register

1 MMC_SSCFG_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30826. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8070h**
MMCSD2	**0FA2 8070h**

Figure 14-10214. MMC_SSCFG_CTL_STAT_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RXDDEBUGBUS1							
R							
8h							
7	6	5	4	3	2	1	0
RXDDEBUGBUS1							
R							
8h							

Table 14-30828. MMC_SSCFG_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK). Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.151 MMC_SSCFG_CTL_STAT_6_REG Register

1 MMC_SSCFG_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the eMMC/SD Controller. For detailed functionality of the eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-30829. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8074h**
MMCSD2	**0FA2 8074h**

Figure 14-10215. MMC_SSCFG_CTL_STAT_6_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TUNDEBUGBUS							
R							
0h							
7	6	5	4	3	2	1	0
TUNDEBUGBUS							
R							
0h							

Table 14-30831. MMC_SSCFG_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.152 MMC_SSCFG_PHY_CTRL_1_REG Register

1 MMC_SSCFG_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80000000h]

The PHY Control 1 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30832. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8100h**
MMCSD2	**0FA2 8100h**

Figure 14-10216. MMC_SSCFG_PHY_CTRL_1_REG Name Register

31	30	29	28	27	26	25	24
IOMUX_ENABLE	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30834. MMC_SSCFG_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOMUX_ENABLE	R/W	1h	IO mux enable. Set 1 for GPIO. Set 0 for eMMC/SD Reset Source: vbus_smod_g_rst_n
30:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.153 MMC_SSCFG_PHY_CTRL_2_REG Register

1 MMC_SSCFG_PHY_CTRL_2_REG Register (Offset = 104h) [reset = 0h]

The PHY Control 2 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30835. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8104h**
MMCSD2	**0FA2 8104h**

Figure 14-10217. MMC_SSCFG_PHY_CTRL_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30837. MMC_SSCFG_PHY_CTRL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.154 MMC_SSCFG_PHY_CTRL_3_REG Register

1 MMC_SSCFG_PHY_CTRL_3_REG Register (Offset = 108h) [reset = 0h]

The PHY Control 3 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30838. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8108h**
MMCSD2	**0FA2 8108h**

Figure 14-10218. MMC_SSCFG_PHY_CTRL_3_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30840. MMC_SSCFG_PHY_CTRL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.155 MMC_SSCFG_PHY_CTRL_4_REG Register

1 MMC_SSCFG_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

The PHY Control 4 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30841. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 810Ch**
MMCSD2	**0FA2 810Ch**

Figure 14-10219. MMC_SSCFG_PHY_CTRL_4_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			OTAPDLYENA	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W				NONE		R/W	R/W
0h				0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ITAPDLYSEL				
NONE			R/W				
0h			0h				

Table 14-30843. MMC_SSCFG_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable. Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved
15:12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select. Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window. It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches. Reset Source: vbus_smod_g_rst_n

Table 14-30843. MMC_SSCFG_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable. This is used for the manual control of the RX clock Tap Delay in non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select. Manual control of the RX clock Tap Delay in the non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n

14.9.4.7.2.156 MMC_SSCFG_PHY_CTRL_5_REG Register

1 MMC_SSCFG_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

The PHY Control 5 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30844. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8110h**
MMCSD2	**0FA2 8110h**

Figure 14-10220. MMC_SSCFG_PHY_CTRL_5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RESERVED		
NONE					R/W		
0h					0h		

Table 14-30846. MMC_SSCFG_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	R/W	0h	Reserved

14.9.4.7.2.157 MMC_SSCFG_PHY_CTRL_6_REG Register

1 MMC_SSCFG_PHY_CTRL_6_REG Register (Offset = 114h) [reset = 0h]

The PHY Control 6 Register contains various fields to control the ports on the eMMC/SD PHY. For detailed functionality of the eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-30847. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8114h**
MMCSD2	**0FA2 8114h**

Figure 14-10221. MMC_SSCFG_PHY_CTRL_6_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30849. MMC_SSCFG_PHY_CTRL_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.158 MMC_SSCFG_PHY_STAT_1_REG Register

1 MMC_SSCFG_PHY_STAT_1_REG Register (Offset = 130h) [reset = 0h]

The PHY Status 1 Register contains various fields to reflect the status of the eMMC/SD PHY ports. For detailed functionality of the eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-30850. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8130h**
MMCSD2	**0FA2 8130h**

Figure 14-10222. MMC_SSCFG_PHY_STAT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30852. MMC_SSCFG_PHY_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.7.2.159 MMC_SSCFG_PHY_STAT_2_REG Register

1 MMC_SSCFG_PHY_STAT_2_REG Register (Offset = 134h) [reset = 0h]

The PHY Status 2 Register contains various fields to reflect the status of the eMMC/SD PHY ports. For detailed functionality of the eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-30853. Instance Table

Instance Name	Physical Address
MMCSD1	**0FA0 8134h**
MMCSD2	**0FA2 8134h**

Figure 14-10223. MMC_SSCFG_PHY_STAT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30855. MMC_SSCFG_PHY_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5 Industrial and Control Interfaces Registers

14.9.5.1 MCAN

MCAN

14.9.5.1.1 MCAN Summaries

MCAN Summaries

Table 14-30856. MCAN Registers, Base Address=2070 0000h, Length=256

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
0h	32	MCAN_PID	2070 0000h	04E0 9000h	04E1 9000h
4h	32	MCAN_CTRL	2070 0004h	04E0 9004h	04E1 9004h
8h	32	MCAN_STAT	2070 0008h	04E0 9008h	04E1 9008h
Ch	32	MCAN_ICS	2070 000Ch	04E0 900Ch	04E1 900Ch
10h	32	MCAN_IRS	2070 0010h	04E0 9010h	04E1 9010h
14h	32	MCAN_IECS	2070 0014h	04E0 9014h	04E1 9014h
18h	32	MCAN_IE	2070 0018h	04E0 9018h	04E1 9018h
1Ch	32	MCAN_IES	2070 001Ch	04E0 901Ch	04E1 901Ch
20h	32	MCAN_EOI	2070 0020h	04E0 9020h	04E1 9020h
24h	32	MCAN_EXT_TS_PRESCALER	2070 0024h	04E0 9024h	04E1 9024h
28h	32	MCAN_EXT_TS_UNSERVICED_INTR_CNTR	2070 0028h	04E0 9028h	04E1 9028h

Table 14-30857. MCAN_CORE Registers, Base Address=2070 1000h, Length=512

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
0h	32	MCAN_CORE_CREL	2070 1000h	04E0 8000h	04E1 8000h
4h	32	MCAN_CORE_ENDN	2070 1004h	04E0 8004h	04E1 8004h
8h	32	MCAN_CORE_CUST	2070 1008h	04E0 8008h	04E1 8008h
Ch	32	MCAN_CORE_DBTP	2070 100Ch	04E0 800Ch	04E1 800Ch
10h	32	MCAN_CORE_TEST	2070 1010h	04E0 8010h	04E1 8010h
14h	32	MCAN_CORE_RWD	2070 1014h	04E0 8014h	04E1 8014h
18h	32	MCAN_CORE_CCCR	2070 1018h	04E0 8018h	04E1 8018h
1Ch	32	MCAN_CORE_NBTP	2070 101Ch	04E0 801Ch	04E1 801Ch
20h	32	MCAN_CORE_TSCC	2070 1020h	04E0 8020h	04E1 8020h
24h	32	MCAN_CORE_TSCV	2070 1024h	04E0 8024h	04E1 8024h
28h	32	MCAN_CORE_TOCC	2070 1028h	04E0 8028h	04E1 8028h
2Ch	32	MCAN_CORE_TOCV	2070 102Ch	04E0 802Ch	04E1 802Ch
30h	32	MCAN_CORE_RESERVED00	2070 1030h	04E0 8030h	04E1 8030h
34h	32	MCAN_CORE_RESERVED11	2070 1034h	04E0 8034h	04E1 8034h
38h	32	MCAN_CORE_RESERVED22	2070 1038h	04E0 8038h	04E1 8038h
3Ch	32	MCAN_CORE_RESERVED33	2070 103Ch	04E0 803Ch	04E1 803Ch
40h	32	MCAN_CORE_ECR	2070 1040h	04E0 8040h	04E1 8040h
44h	32	MCAN_CORE_PSR	2070 1044h	04E0 8044h	04E1 8044h
48h	32	MCAN_CORE_TDCR	2070 1048h	04E0 8048h	04E1 8048h
4Ch	32	MCAN_CORE_RESERVED44	2070 104Ch	04E0 804Ch	04E1 804Ch
50h	32	MCAN_CORE_IR	2070 1050h	04E0 8050h	04E1 8050h

Table 14-30857. MCAN_CORE Registers, Base Address=2070 1000h, Length=512 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
54h	32	MCAN_CORE_IE	2070 1054h	04E0 8054h	04E1 8054h
58h	32	MCAN_CORE_ILS	2070 1058h	04E0 8058h	04E1 8058h
5Ch	32	MCAN_CORE_ILE	2070 105Ch	04E0 805Ch	04E1 805Ch
60h	32	MCAN_CORE_RESERVED55	2070 1060h	04E0 8060h	04E1 8060h
64h	32	MCAN_CORE_RESERVED66	2070 1064h	04E0 8064h	04E1 8064h
68h	32	MCAN_CORE_RESERVED77	2070 1068h	04E0 8068h	04E1 8068h
6Ch	32	MCAN_CORE_RESERVED88	2070 106Ch	04E0 806Ch	04E1 806Ch
70h	32	MCAN_CORE_RESERVED99	2070 1070h	04E0 8070h	04E1 8070h
74h	32	MCAN_CORE_RESERVED1010	2070 1074h	04E0 8074h	04E1 8074h
78h	32	MCAN_CORE_RESERVED1111	2070 1078h	04E0 8078h	04E1 8078h
7Ch	32	MCAN_CORE_RESERVED1212	2070 107Ch	04E0 807Ch	04E1 807Ch
80h	32	MCAN_CORE_GFC	2070 1080h	04E0 8080h	04E1 8080h
84h	32	MCAN_CORE_SIDFC	2070 1084h	04E0 8084h	04E1 8084h
88h	32	MCAN_CORE_XIDFC	2070 1088h	04E0 8088h	04E1 8088h
8Ch	32	MCAN_CORE_RESERVED1313	2070 108Ch	04E0 808Ch	04E1 808Ch
90h	32	MCAN_CORE_XIDAM	2070 1090h	04E0 8090h	04E1 8090h
94h	32	MCAN_CORE_HPMS	2070 1094h	04E0 8094h	04E1 8094h
98h	32	MCAN_CORE_NDAT1	2070 1098h	04E0 8098h	04E1 8098h
9Ch	32	MCAN_CORE_NDAT2	2070 109Ch	04E0 809Ch	04E1 809Ch
A0h	32	MCAN_CORE_RXF0C	2070 10A0h	04E0 80A0h	04E1 80A0h
A4h	32	MCAN_CORE_RXF0S	2070 10A4h	04E0 80A4h	04E1 80A4h
A8h	32	MCAN_CORE_RXF0A	2070 10A8h	04E0 80A8h	04E1 80A8h
ACh	32	MCAN_CORE_RXBC	2070 10ACh	04E0 80ACh	04E1 80ACh
B0h	32	MCAN_CORE_RXF1C	2070 10B0h	04E0 80B0h	04E1 80B0h
B4h	32	MCAN_CORE_RXF1S	2070 10B4h	04E0 80B4h	04E1 80B4h
B8h	32	MCAN_CORE_RXF1A	2070 10B8h	04E0 80B8h	04E1 80B8h
BCh	32	MCAN_CORE_RXESC	2070 10BCh	04E0 80BCh	04E1 80BCh
C0h	32	MCAN_CORE_TXBC	2070 10C0h	04E0 80C0h	04E1 80C0h
C4h	32	MCAN_CORE_TXFQS	2070 10C4h	04E0 80C4h	04E1 80C4h
C8h	32	MCAN_CORE_TXESC	2070 10C8h	04E0 80C8h	04E1 80C8h
CCh	32	MCAN_CORE_TXBRP	2070 10CCh	04E0 80CCh	04E1 80CCh
D0h	32	MCAN_CORE_TXBAR	2070 10D0h	04E0 80D0h	04E1 80D0h
D4h	32	MCAN_CORE_TXBCR	2070 10D4h	04E0 80D4h	04E1 80D4h
D8h	32	MCAN_CORE_TXBTO	2070 10D8h	04E0 80D8h	04E1 80D8h
DCh	32	MCAN_CORE_TXBCF	2070 10DCh	04E0 80DCh	04E1 80DCh
E0h	32	MCAN_CORE_TXBTIE	2070 10E0h	04E0 80E0h	04E1 80E0h
E4h	32	MCAN_CORE_TXBCIE	2070 10E4h	04E0 80E4h	04E1 80E4h
E8h	32	MCAN_CORE_RESERVED1414	2070 10E8h	04E0 80E8h	04E1 80E8h
ECh	32	MCAN_CORE_RESERVED1515	2070 10ECh	04E0 80ECh	04E1 80ECh
F0h	32	MCAN_CORE_TXEFC	2070 10F0h	04E0 80F0h	04E1 80F0h
F4h	32	MCAN_CORE_TXEFS	2070 10F4h	04E0 80F4h	04E1 80F4h
F8h	32	MCAN_CORE_TXEFA	2070 10F8h	04E0 80F8h	04E1 80F8h
FCh	32	MCAN_CORE_RESERVED1616	2070 10FCh	04E0 80FCh	04E1 80FCh

Table 14-30857. MCAN_CORE Registers, Base Address=2070 1000h, Length=512 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
100h	32	MCAN_CORE_RESERVUPPER256_J	2070 1100h + formula	04E0 8100h + formula	04E1 8100h + formula

Table 14-30858. MCAN_MSGMEM_RAM Registers, Base Address=2070 8000h, Length=32768

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
0h	32	MCAN_MSGMEM_RAM_RAM_REG_J	2070 8000h + formula	04E0 0000h + formula	04E1 0000h + formula

Table 14-30859. ECC_AGGR Registers, Base Address=2401 8000h, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCU_MCAN0 Physical Address	MCU_MCAN1 Physical Address
0h	32	ECC_AGGR_REV	2401 8000h	0470 1000h	0470 2000h
8h	32	ECC_AGGR_VECTOR	2401 8008h	0470 1008h	0470 2008h
Ch	32	ECC_AGGR_STAT	2401 800Ch	0470 100Ch	0470 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	2401 8010h + formula	0470 1010h + formula	0470 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	2401 803Ch	0470 103Ch	0470 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2401 8040h	0470 1040h	0470 2040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2401 8080h	0470 1080h	0470 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2401 80C0h	0470 10C0h	0470 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2401 813Ch	0470 113Ch	0470 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2401 8140h	0470 1140h	0470 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2401 8180h	0470 1180h	0470 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2401 81C0h	0470 11C0h	0470 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2401 8200h	0470 1200h	0470 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2401 8204h	0470 1204h	0470 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2401 8208h	0470 1208h	0470 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2401 820Ch	0470 120Ch	0470 220Ch

14.9.5.1.2 MCAN Registers

MCAN Registers

14.9.5.1.2.1 MCAN_PID Register

1 MCAN_PID Register (Offset = 0h) [reset = 68E05901h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-30860. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0000h**
MCU_MCAN0	**04E0 9000h**
MCU_MCAN1	**04E1 9000h**

Figure 14-10224. MCAN_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		8E0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
8E0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Bh					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-30862. MCAN_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: hsrst_n
29:28	BU	R	2h	Business Unit Reset Source: hsrst_n `2h Processors`
27:16	MODULE_ID	R	8E0h	Module ID Reset Source: hsrst_n
15:11	RTL	R	Bh	RTL Revision Reset Source: hsrst_n
10:8	MAJOR	R	1h	Major Revision Reset Source: hsrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: hsrst_n
5:0	MINOR	R	1h	Minor Revision Reset Source: hsrst_n

14.9.5.1.2.2 MCAN_CTRL Register

1 MCAN_CTRL Register (Offset = 4h) [reset = 8h]

The Control Register contains general control bits for the MCANSS

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Table 14-30863. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0004h**
MCU_MCAN0	**04E0 9004h**
MCU_MCAN1	**04E1 9004h**

Figure 14-10225. MCAN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREQEN	DBGSUSP_FREE	RESERVED		
NONE	R/W	R/W	R/W	R/W	NONE		
0h	0h	0h	0h	1h	0h		

Table 14-30865. MCAN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	EXT_TS_CNTR_EN	R/W	0h	External Timestamp Counter Enable Reset Source: hsrst_n
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable Reset Source: hsrst_n
4	WAKEUPREQEN	R/W	0h	Wakeup Request Enable Reset Source: hsrst_n

3	DBGSUSP_FREE	R/W	1h	Debug Suspend
				Reset Source: hsrst_n
				`0h Honor debug suspend`
				`1h Disregard debug suspend`

2:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.3 MCAN_STAT Register

1 MCAN_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the MCANSS

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Table 14-30866. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0008h**
MCU_MCAN0	**04E0 9008h**
MCU_MCAN1	**04E1 9008h**

Figure 14-10226. MCAN_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_FDOE	MEM_INIT_DONE	RESERVED
NONE					R	R	NONE
0h					X	0h	0h

Table 14-30868. MCAN_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_FDOE	R	X	Enable FD (Flexible Data-Rate) Configuration Reflects the value of mcanss_enable_fdoe configuration port, Reset Source: hsrst_n xh mcanss_enable_fdoe.
1	MEM_INIT_DONE	R	0h	Memory Initialization Reset Source: hsrst_n 0h Memory initialization is in progress 1h Memory intialization done
0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.4 MCAN_ICS Register

1 MCAN_ICS Register (Offset = Ch) [reset = 0h]

Write to clear interrupt bits

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Table 14-30869. Instance Table

Instance Name	Physical Address
MCAN0	**2070 000Ch**
MCU_MCAN0	**04E0 900Ch**
MCU_MCAN1	**04E1 900Ch**

Figure 14-10227. MCAN_ICS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							W
0h							0h

Table 14-30871. MCAN_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to clear bits. Reset Source: hsrst_n

14.9.5.1.2.5 MCAN_IRS Register

1 MCAN_IRS Register (Offset = 10h) [reset = 0h]

Read raw interrupt status. Write '1' to set interrupt bits.

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Table 14-30872. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0010h**
MCU_MCAN0	**04E0 9010h**
MCU_MCAN1	**04E1 9010h**

Figure 14-10228. MCAN_IRS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-30874. MCAN_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to set bits. Reset Source: hsrst_n

14.9.5.1.2.6 MCAN_IECS Register

1 MCAN_IECS Register (Offset = 14h) [reset = 0h]

Write to clear interrupt enable bits

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Table 14-30875. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0014h**
MCU_MCAN0	**04E0 9014h**
MCU_MCAN1	**04E1 9014h**

Figure 14-10229. MCAN_IECS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EXT_TS_CNTR_OVFL</td></tr>
<tr><td colspan="7">NONE</td><td>W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30877. MCAN_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W1TC	0h	External Timestamp Counter Overflow Interrupt Write 1h to clear bits. Reset Source: hsrst_n

14.9.5.1.2.7 MCAN_IE Register

1 MCAN_IE Register (Offset = 18h) [reset = 0h]

Read interrupt Enable

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Table 14-30878. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0018h**
MCU_MCAN0	**04E0 9018h**
MCU_MCAN1	**04E1 9018h**

Figure 14-10230. MCAN_IE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-30880. MCAN_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Write 1h to set bits. Reset Source: hsrst_n

14.9.5.1.2.8 MCAN_IES Register

1 MCAN_IES Register (Offset = 1Ch) [reset = 0h]

Read Enabled Interrupts

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Table 14-30881. Instance Table

Instance Name	Physical Address
MCAN0	**2070 001Ch**
MCU_MCAN0	**04E0 901Ch**
MCU_MCAN1	**04E1 901Ch**

Figure 14-10231. MCAN_IES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EXT_TS_CNTR_OVFL
NONE							R
0h							0h

Table 14-30883. MCAN_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow Interrupt Reset Source: hsrst_n

14.9.5.1.2.9 MCAN_EOI Register

1 MCAN_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-30884. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0020h**
MCU_MCAN0	**04E0 9020h**
MCU_MCAN1	**04E1 9020h**

Figure 14-10232. MCAN_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-30886. MCAN_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	End Of Interrupt Write with bit position of the targeted interrupt (example: external timestamp is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1h will issue another pulse interrupt. Reset Source: hsrst_n 0h `EOI value for external timestamp interrupt` 1h `EOI value for mcan[0] interrupt` 2h `EOI value for mcan[1] interrupt`

14.9.5.1.2.10 MCAN_EXT_TS_PRESCALER Register

1 MCAN_EXT_TS_PRESCALER Register (Offset = 24h) [reset = 0h]

External TImeStamp PreScaler

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Table 14-30887. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0024h**
MCU_MCAN0	**04E0 9024h**
MCU_MCAN1	**04E1 9024h**

Figure 14-10233. MCAN_EXT_TS_PRESCALER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRESCALER							
R/W							
0h							
15	14	13	12	11	10	9	8
PRESCALER							
R/W							
0h							
7	6	5	4	3	2	1	0
PRESCALER							
R/W							
0h							

Table 14-30889. MCAN_EXT_TS_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PRESCALER	R/W	0h	External Timestamp Prescaler Reload Value External timestamp count rate is host clock rate divided by this value with one exception - a value of 0h has the same effect as 1h. Reset Source: hsrst_n

14.9.5.1.2.11 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register

1 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 28h) [reset = 0h]

External TImeStamp Unserviced Interrupts Counter

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Table 14-30890. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0028h**
MCU_MCAN0	**04E0 9028h**
MCU_MCAN1	**04E1 9028h**

Figure 14-10234. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EXT_TS_INTR_CNTR				
NONE			R				
0h			0h				

Table 14-30892. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EXT_TS_INTR_CNTR	R	0h	Number of Unserviced Rollover Interrupts If > 1h an EOI write will issue another pulse interrupt. Reset Source: hsrst_n

14.9.5.1.2.12 MCAN_CORE_CREL Register

1 MCAN_CORE_CREL Register (Offset = 0h) [reset = 32380608h]

Release dependent constant (version + date)

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Table 14-30893. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1000h**
MCU_MCAN0	**04E0 8000h**
MCU_MCAN1	**04E1 8000h**

Figure 14-10235. MCAN_CORE_CREL Name Register

31	30	29	28	27	26	25	24
REL				STEP			
R				R			
3h				2h			
23	22	21	20	19	18	17	16
SUBSTEP				YEAR			
R				R			
3h				8h			
15	14	13	12	11	10	9	8
MON							
R							
6h							
7	6	5	4	3	2	1	0
DAY							
R							
8h							

Table 14-30895. MCAN_CORE_CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REL	R	3h	Core Release One digit, BCD-coded. Reset Source: hsrst_n
27:24	STEP	R	2h	Step of Core Release One digit, BCD-coded. Reset Source: hsrst_n
23:20	SUBSTEP	R	3h	Sub-step of Core Release One digit, BCD-coded. Reset Source: hsrst_n
19:16	YEAR	R	8h	Time Stamp Year One digit, BCD-coded. Reset Source: hsrst_n
15:8	MON	R	6h	Time Stamp Month Two digits, BCD-coded. Reset Source: hsrst_n

Table 14-30895. MCAN_CORE_CREL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	DAY	R	8h	Time Stamp Day Two digits, BCD-coded. Reset Source: hsrst_n

14.9.5.1.2.13 MCAN_CORE_ENDN Register

1 MCAN_CORE_ENDN Register (Offset = 4h) [reset = 87654321h]

Constant "0x8765 4321"

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Table 14-30896. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1004h**
MCU_MCAN0	**04E0 8004h**
MCU_MCAN1	**04E1 8004h**

Figure 14-10236. MCAN_CORE_ENDN Name Register

31	30	29	28	27	26	25	24
ETV							
R							
87654321h							
23	22	21	20	19	18	17	16
ETV							
R							
87654321h							
15	14	13	12	11	10	9	8
ETV							
R							
87654321h							
7	6	5	4	3	2	1	0
ETV							
R							
87654321h							

Table 14-30898. MCAN_CORE_ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ETV	R	87654321h	Endianness Test Value The endianness test value is 8765 4321h. Reset Source: hsrst_n

14.9.5.1.2.14 MCAN_CORE_CUST Register

1 MCAN_CORE_CUST Register (Offset = 8h) [reset = 0h]

Optional customer-specific register

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Table 14-30899. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1008h**
MCU_MCAN0	**04E0 8008h**
MCU_MCAN1	**04E1 8008h**

Figure 14-10237. MCAN_CORE_CUST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30901. MCAN_CORE_CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.15 MCAN_CORE_DBTP Register

1 MCAN_CORE_DBTP Register (Offset = Ch) [reset = A33h]

Configuration of data phase bit timing, transmitter delay compensation enable

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Table 14-30902. Instance Table

Instance Name	Physical Address
MCAN0	**2070 100Ch**
MCU_MCAN0	**04E0 800Ch**
MCU_MCAN1	**04E1 800Ch**

Figure 14-10238. MCAN_CORE_DBTP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDC	RESERVED		DBRP				
R/W	NONE		R/W				
0h	0h		0h				
15	14	13	12	11	10	9	8
RESERVED			DTSEG1				
NONE			R/W				
0h			Ah				
7	6	5	4	3	2	1	0
DTSEG2				DSJW			
R/W				R/W			
3h				3h			

Table 14-30904. MCAN_CORE_DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23	TDC	R/W	0h	Transmitter Delay Compensation
				Reset Source: hsrst_n
				`0h      Transmitter Delay Compensation disabled`
				`1h      Transmitter Delay Compensation enabled`

22:21	RESERVED	NONE	0h	Reserved
20:16	DBRP	R/W	0h	Data Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved

Table 14-30904. MCAN_CORE_DBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	DTSEG1	R/W	Ah	Data time segment before sample point Valid values are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n
7:4	DTSEG2	R/W	3h	Data time segment after sample point Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n
3:0	DSJW	R/W	3h	Data (Re)Synchronization Jump Width Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n

14.9.5.1.2.16 MCAN_CORE_TEST Register

1 MCAN_CORE_TEST Register (Offset = 10h) [reset = 0h]

Test mode selection

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Table 14-30905. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1010h**
MCU_MCAN0	**04E0 8010h**
MCU_MCAN1	**04E1 8010h**

Figure 14-10239. MCAN_CORE_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX	TX		LBCK	RESERVED			
R	R/W		R/W	NONE			
0h	0h		0h	0h			

Table 14-30907. MCAN_CORE_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX	R	0h	Receive Pin Monitors the actual value of the MCAN RX pin Reset Source: hsrst_n 0h The CAN bus is dominant (MCAN RX = 0h) 1h The CAN bus is recessive (MCAN RX = 1h)
6:5	TX	R/W	0h	Control of Transmit Pin Reset Source: hsrst_n 0h Reset value, the MCAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 1h Sample Point can be monitored at the MCAN TX pin 2h Dominant (0) level at the MCAN TX pin 3h Recessive (1) at the MCAN TX pin
4	LBCK	R/W	0h	Loopback Mode Reset Source: hsrst_n 0h Reset value, Loopback Mode is disabled 1h Loopback Mode is enabled (see Test Modes)

Table 14-30907. MCAN_CORE_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.17 MCAN_CORE_RWD Register

1 MCAN_CORE_RWD Register (Offset = 14h) [reset = 0h]

Monitors the READY output of the Message RAM

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Table 14-30908. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1014h**
MCU_MCAN0	**04E0 8014h**
MCU_MCAN1	**04E1 8014h**

Figure 14-10240. MCAN_CORE_RWD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDV							
R							
0h							
7	6	5	4	3	2	1	0
WDC							
R/W							
0h							

Table 14-30910. MCAN_CORE_RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDV	R	0h	Watchdog Value Actual Message RAM Watchdog Counter Value. Reset Source: hsrst_n
7:0	WDC	R/W	0h	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of 0h the counter is disabled. Reset Source: hsrst_n

14.9.5.1.2.18 MCAN_CORE_CCCR Register

1 MCAN_CORE_CCCR Register (Offset = 18h) [reset = 1h]

Operation mode configuration

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Table 14-30911. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1018h**
MCU_MCAN0	**04E0 8018h**
MCU_MCAN1	**04E1 8018h**

Figure 14-10241. MCAN_CORE_CCCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NISO	TXP	EFBI	PXHD	RESERVED		BRSE	FDOE
R/W	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	0h	0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Table 14-30913. MCAN_CORE_CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved

15	NISO	R/W	0h	Non ISO Operation
				Reset Source: hsrst_n
				`0h` `CAN FD frame format according to ISO 11898-1:2015.`
				`1h` `CAN FD frame format according to Bosch CAN FD Specification 1.0.`

14	TXP	R/W	0h	Transmit Pause
				If this bit is set, the MCAN module pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Tx Handling) .
				Reset Source: hsrst_n
				`0h` `Transmit pause disabled`
				`1h` `Transmit pause enabled`

13	EFBI	R/W	0h	Edge Filtering during Bus Integration
				Reset Source: hsrst_n
				`0h` `Edge filtering disabled`
				`1h` `Two consecutive dominant tq required to detect an edge for hard synchronization`

Table 14-30913. MCAN_CORE_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PXHD	R/W	0h	Protocol Exception Handling Disable Note: When protocol exception handling is disabled, the MCAN module will transmit an error frame when it detects a protocol exception condition. Reset Source: hsrst_n 0h Protocol exception handling enabled 1h Protocol exception handling disabled
11:10	RESERVED	NONE	0h	Reserved
9	BRSE	R/W	0h	Bit Rate Switch Enable Note: When CAN FD operation is disabled the MCAN_CCCR[8] FDOE = 0h Reset Source: hsrst_n 0h Bit rate switching for transmissions disabled 1h Bit rate switching for transmissions enabled
8	FDOE	R/W	0h	FD Operation Enable Reset Source: hsrst_n 0h FD operation disabled 1h FD operation enabled
7	TEST	R/W	0h	Test Mode Enable Reset Source: hsrst_n 0h Normal operation. The MCAN_TEST register holds reset values. 1h Test Mode. Write access to the MCAN_TEST register enabled.
6	DAR	R/W	0h	Disable Automatic Retransmission Reset Source: hsrst_n 0h Automatic retransmission of messages not transmitted successfully enabled 1h Automatic retransmission disabled
5	MON	R/W	0h	Bus Monitoring Mode The MCAN_CCCR[5] MON bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. Reset Source: hsrst_n 0h Bus Monitoring Mode is disabled 1h Bus Monitoring Mode is enabled
4	CSR	R/W	0h	Clock Stop Request Reset Source: hsrst_n 0h No clock stop is requested 1h Clock stop requested. When clock stop is requested, first the MCAN_CCCR[0] INIT bit and then the MCAN_CCCR[3] CSA bit will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge Reset Source: hsrst_n 0h No clock stop acknowledged 1h The MCAN module may be set in power down by stopping MCAN interface clock and MCAN functional clock

Table 14-30913. MCAN_CORE_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	ASM	R/W	0h	Restricted Operation Mode
				The MCAN_CCCR[2] ASM bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time.
				For a description of the Restricted Operation Mode, see Restricted Operation Mode.
				Reset Source: hsrst_n
				`0h` `Normal CAN operation`
				`1h` `Restricted Operation Mode active`

1	CCE	R/W	0h	Configuration Change Enable
				Reset Source: hsrst_n
				`0h` `The Host CPU has no write access to the protected configuration registers`
				`1h` `The Host CPU has write access to the protected configuration registers (while the MCAN_CCCR[0] INIT = 1h)`

0	INIT	R/W	1h	Initialization
				Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the MCAN_CCCR[0] INIT bit can be read back. Therefore the software has to assure that the previous value written to the MCAN_CCCR[0] INIT bit has been accepted by Reading the MCAN_CCCR[0] INIT bit before setting the MCAN_CCCR[0] INIT bit to a new value.
				Reset Source: hsrst_n
				`0h` `Normal Operation`
				`1h` `Initialization is started`

14.9.5.1.2.19 MCAN_CORE_NBTP Register

1 MCAN_CORE_NBTP Register (Offset = 1Ch) [reset = 6000A03h]

Configuration of arbitration phase bit timing

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Table 14-30914. Instance Table

Instance Name	Physical Address
MCAN0	**2070 101Ch**
MCU_MCAN0	**04E0 801Ch**
MCU_MCAN1	**04E1 801Ch**

Figure 14-10242. MCAN_CORE_NBTP Name Register

31	30	29	28	27	26	25	24
NSJW							NBRP
R/W							R/W
3h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NBRP							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NTSEG1							
R/W							
Ah							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	NTSEG2						
NONE	R/W						
0h	3h						

Table 14-30916. MCAN_CORE_NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NSJW	R/W	3h	Nominal (Re)Synchronization Jump Width Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
24:16	NBRP	R/W	0h	Nominal Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 511 (0h-1FFh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
15:8	NTSEG1	R/W	Ah	Nominal Time segment before sample point Valid values are 1 to 255 (1h-FFh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved

Table 14-30916. MCAN_CORE_NBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NTSEG2	R/W	3h	Nominal Time segment after sample point Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0600 0A03h configures the MCAN module for a bit rate of 500 kbit/s. Reset Source: hsrst_n

14.9.5.1.2.20 MCAN_CORE_TSCC Register

1 MCAN_CORE_TSCC Register (Offset = 20h) [reset = 0h]

Timestamp counter prescaler setting, selection of internal/external timestamp vector

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Table 14-30917. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1020h**
MCU_MCAN0	**04E0 8020h**
MCU_MCAN1	**04E1 8020h**

Figure 14-10243. MCAN_CORE_TSCC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TCP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TSS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-30919. MCAN_CORE_TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	TCP	R/W	0h	Timestamp Counter Prescaler Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1-16 (0h-Fh)]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation (MCAN_TSCC[1-0] TSS = 2h) Reset Source: hsrst_n
15:2	RESERVED	NONE	0h	Reserved

1:0	TSS	R/W	0h	Timestamp Select
				Reset Source: hsrst_n
				`0h Timestamp counter value always 0h`
				`1h Timestamp counter value incremented according to the MCAN_TSCC[19-16] TCP field`
				`2h External timestamp counter value used`
				`3h Same as 0h`

14.9.5.1.2.21 MCAN_CORE_TSCV Register

1 MCAN_CORE_TSCV Register (Offset = 24h) [reset = 0h]

Read/reset timestamp counter

Return to Summary Table

Table 14-30920. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1024h**
MCU_MCAN0	**04E0 8024h**
MCU_MCAN1	**04E1 8024h**

Figure 14-10244. MCAN_CORE_TSCV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TSC							
R/WTC							
0h							
7	6	5	4	3	2	1	0
TSC							
R/WTC							
0h							

Table 14-30922. MCAN_CORE_TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TSC	R/WTC	0h	Timestamp Counter The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When the MCAN_TSCC[1-0] TSS = 1h, the Timestamp Counter is incremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. A wrap around sets interrupt flag MCAN_IR[16] TSW. Write access resets the counter to zero. When the MCAN_TSCC[1-0] TSS = 2h, the MCAN_TSCV[15-0] TSC field reflects the external Timestamp Counter value. A write access has no impact. Note: A 'wrap around' is a change of the Timestamp Counter value from non-zero to zero not caused by write access to the MCAN_TSCV register. Reset Source: hsrst_n

14.9.5.1.2.22 MCAN_CORE_TOCC Register

1 MCAN_CORE_TOCC Register (Offset = 28h) [reset = FFFF0000h]

Configuration of timeout period, selection of timeout counter operation mode

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Table 14-30923. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1028h**
MCU_MCAN0	**04E0 8028h**
MCU_MCAN1	**04E1 8028h**

Figure 14-10245. MCAN_CORE_TOCC Name Register

31	30	29	28	27	26	25	24
TOP							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
TOP							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TOS		ETOC
NONE					R/W		R/W
0h					0h		0h

Table 14-30925. MCAN_CORE_TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TOP	R/W	FFFFh	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Reset Source: hsrst_n
15:3	RESERVED	NONE	0h	Reserved
2:1	TOS	R/W	0h	Timeout Select When operating in Continuous mode, a write to the MCAN_TOCV[15-0] TOC field presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored. Reset Source: hsrst_n 0h Continuous operation 1h Timeout controlled by Tx Event FIFO 2h Timeout controlled by Rx FIFO 0 3h Timeout controlled by Rx FIFO 1

Table 14-30925. MCAN_CORE_TOCC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

0	ETOC	R/W	0h	Enable Timeout Counter
				Reset Source: hsrst_n
				`0h     Timeout Counter disabled`
				`1h     Timeout Counter enabled`

14.9.5.1.2.23 MCAN_CORE_TOCV Register

1 MCAN_CORE_TOCV Register (Offset = 2Ch) [reset = FFFFh]

Read/reset timeout counter

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Table 14-30926. Instance Table

Instance Name	Physical Address
MCAN0	**2070 102Ch**
MCU_MCAN0	**04E0 802Ch**
MCU_MCAN1	**04E1 802Ch**

Figure 14-10246. MCAN_CORE_TOCV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TOC</td></tr>
<tr><td colspan="8">R/WTC</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TOC</td></tr>
<tr><td colspan="8">R/WTC</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-30928. MCAN_CORE_TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TOC	R/WTC	FFFFh	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. When decremented to zero, interrupt flag MCAN_IR[18] TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via the MCAN_TOCC[2-1] TOS field. Reset Source: hsrst_n

14.9.5.1.2.24 MCAN_CORE_RESERVED00 Register

1 MCAN_CORE_RESERVED00 Register (Offset = 30h) [reset = 0h]

Reserved field

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Table 14-30929. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1030h**
MCU_MCAN0	**04E0 8030h**
MCU_MCAN1	**04E1 8030h**

Figure 14-10247. MCAN_CORE_RESERVED00 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30931. MCAN_CORE_RESERVED00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.25 MCAN_CORE_RESERVED11 Register

1 MCAN_CORE_RESERVED11 Register (Offset = 34h) [reset = 0h]

Reserved field

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Table 14-30932. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1034h**
MCU_MCAN0	**04E0 8034h**
MCU_MCAN1	**04E1 8034h**

Figure 14-10248. MCAN_CORE_RESERVED11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30934. MCAN_CORE_RESERVED11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.26 MCAN_CORE_RESERVED22 Register

1 MCAN_CORE_RESERVED22 Register (Offset = 38h) [reset = 0h]

Reserved field

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Table 14-30935. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1038h**
MCU_MCAN0	**04E0 8038h**
MCU_MCAN1	**04E1 8038h**

Figure 14-10249. MCAN_CORE_RESERVED22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30937. MCAN_CORE_RESERVED22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.27 MCAN_CORE_RESERVED33 Register

1 MCAN_CORE_RESERVED33 Register (Offset = 3Ch) [reset = 0h]

Reserved field

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Table 14-30938. Instance Table

Instance Name	Physical Address
MCAN0	**2070 103Ch**
MCU_MCAN0	**04E0 803Ch**
MCU_MCAN1	**04E1 803Ch**

Figure 14-10250. MCAN_CORE_RESERVED33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30940. MCAN_CORE_RESERVED33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.28 MCAN_CORE_ECR Register

1 MCAN_CORE_ECR Register (Offset = 40h) [reset = 0h]

State of Rx/Tx Error Counter, CAN Error Logging

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Table 14-30941. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1040h**
MCU_MCAN0	**04E0 8040h**
MCU_MCAN1	**04E1 8040h**

Figure 14-10251. MCAN_CORE_ECR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CEL							
R							
0h							
15	14	13	12	11	10	9	8
RP	REC						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
TEC							
R							
0h							

Table 14-30943. MCAN_CORE_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	CEL	R	0h	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to the MCAN_ECR[23-16] CEL field. The counter stops at FFh; the next increment of the MCAN_ECR[7-0] TEC or MCAN_ECR[14-8] REC fields sets interrupt flag MCAN_IR[22] ELO. Reset Source: hsrst_n

15	RP	R	0h	Receive Error Passive
				Reset Source: hsrst_n
				`0h The Receive Error Counter is below the error passive level of 128`
				`1h The Receive Error Counter has reached the error passive level of 128`

14:8	REC	R	0h	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127. Reset Source: hsrst_n

Table 14-30943. MCAN_CORE_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	TEC	R	0h	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255. Note: When the MCAN_CCCR[2] ASM bit is set, the CAN protocol controller does not increment the MCAN_ECR[7-0] TEC and MCAN_ECR[14-8] REC fields when a CAN protocol error is detected, but the MCAN_ECR[23-16] CEL field is still incremented. Reset Source: hsrst_n

14.9.5.1.2.29 MCAN_CORE_PSR Register

1 MCAN_CORE_PSR Register (Offset = 44h) [reset = 707h]

CAN protocol controller status, transmitter delay compensation value

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Table 14-30944. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1044h**
MCU_MCAN0	**04E0 8044h**
MCU_MCAN1	**04E1 8044h**

Figure 14-10252. MCAN_CORE_PSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDCV						
NONE	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PXE	RFDF	RBRS	RESI	DLEC		
NONE	R	R	R	R	R		
0h	0h	0h	0h	0h	7h		
7	6	5	4	3	2	1	0
BO	EW	EP	ACT		LEC		
R	R	R	R		R		
0h	0h	0h	0h		7h		

Table 14-30946. MCAN_CORE_PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TDCV	R	0h	Transmitter Delay Compensation Value Position of the secondary sample point, defined by the sum of the measured delay from the MCAN TX to MCAN RX pins and the MCAN_TDCR[14-8] TDCO field. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n
15	RESERVED	NONE	0h	Reserved

14	PXE	R	0h	Protocol Exception Event
				Reset Source: hsrst_n
				`0h No protocol exception event occurred since last read access`
				`1h Protocol exception event occurred`

Table 14-30946. MCAN_CORE_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RFDF	R	0h	Received a CAN FD Message This bit is set independent of acceptance filtering. Reset Source: hsrst_n 0h Since this bit was reset by the Host CPU, no CAN FD message has been received 1h Message in CAN FD format with FDF flag set has been received
12	RBRS	R	0h	BRS flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. Reset Source: hsrst_n 0h Last received CAN FD message did not have its BRS flag set 1h Last received CAN FD message had its BRS flag set
11	RESI	R	0h	ESI flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. Reset Source: hsrst_n 0h Last received CAN FD message did not have its ESI flag set 1h Last received CAN FD message had its ESI flag set
10:8	DLEC	R	7h	Data Phase Last Error Code Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for the MCAN_PSR[2-0] LEC field. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Reset Source: hsrst_n
7	BO	R	0h	Bus_Off Status Reset Source: hsrst_n 0h The MCAN module is not Bus_Off 1h The MCAN module is in Bus_Off state
6	EW	R	0h	Warning Status Reset Source: hsrst_n 0h Both error counters are below the Error_Warning limit of 96 1h At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive Reset Source: hsrst_n 0h The MCAN module is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1h The MCAN module is in the Error_Passive state

Table 14-30946. MCAN_CORE_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	ACT	R	0h	Activity Monitors the module's CAN communication state. Note: ACT is set to 0h by a Protocol Exception Event. Reset Source: hsrst_n 0h Synchronizing - node is synchronizing on CAN communication 1h Idle - node is neither receiver nor transmitter 2h Receiver - node is operating as receiver 3h Transmitter - node is operating as transmitter
2:0	LEC	R	7h	Last Error Code The MCAN_PSR[2-0] LEC field indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0h when a message has been transferred (reception or transmission) without error. Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in the MCAN_PSR[10-8] DLEC field instead of the MCAN_PSR[2-0] LEC field. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. Reset Source: hsrst_n 0h No Error: No error occurred since the MCAN_PSR[2-0] LEC field has been reset by successful reception or transmission. 1h Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2h Form Error: A fixed format part of a received frame has the wrong format. 3h AckError: The message transmitted by the MCAN module was not acknowledged by another node. 4h Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value 1), but the monitored bus value was dominant. 5h Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the Host CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6h CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7h NoChange: Any read access to the Protocol Status Register re-initializes the MCAN_PSR[2-0] LEC field to 7h. When the MCAN_PSR[2-0] LEC field shows the value 7h, no CAN bus event was detected since the last Host CPU read access to the Protocol Status Register.

14.9.5.1.2.30 MCAN_CORE_TDCR Register

1 MCAN_CORE_TDCR Register (Offset = 48h) [reset = 0h]

configuration of transmitter delay compensation offset and filter window length

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Table 14-30947. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1048h**
MCU_MCAN0	**04E0 8048h**
MCU_MCAN1	**04E1 8048h**

Figure 14-10253. MCAN_CORE_TDCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	TDCO						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	TDCF						
NONE	R/W						
0h	0h						

Table 14-30949. MCAN_CORE_TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:8	TDCO	R/W	0h	Transmitter Delay Compensation Offset Offset value defining the distance between the measured delay from the MCAN RX and MCAN TX pins and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	TDCF	R/W	0h	Transmitter Delay Compensation Filter Window Length Defines the minimum value for the SSP position, dominant edges on the MCAN RX pin that would result in an earlier SSP position are ignored for transmitter delay measure-ment. The feature is enabled when the MCAN_TDCR[6-0] TDCF field is configured to a value greater than the MCAN_TDCR[14-8] TDCO field. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n

14.9.5.1.2.31 MCAN_CORE_RESERVED44 Register

1 MCAN_CORE_RESERVED44 Register (Offset = 4Ch) [reset = 0h]

Reserved field

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Table 14-30950. Instance Table

Instance Name	Physical Address
MCAN0	**2070 104Ch**
MCU_MCAN0	**04E0 804Ch**
MCU_MCAN1	**04E1 804Ch**

Figure 14-10254. MCAN_CORE_RESERVED44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30952. MCAN_CORE_RESERVED44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.32 MCAN_CORE_IR Register

1 MCAN_CORE_IR Register (Offset = 50h) [reset = 0h]

Interrupt flags

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Table 14-30953. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1050h**
MCU_MCAN0	**04E0 8050h**
MCU_MCAN1	**04E1 8050h**

Figure 14-10255. MCAN_CORE_IR Name Register

31	30	29	28	27	26	25	24
RESERVED		ARA	PED	PEA	WDI	BO	EW
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EP	ELO	BEU	RESERVED	DRX	TOO	MRAF	TSW
R/W1TC	R/W1TC	R/W1TC	NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30955. MCAN_CORE_IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARA	R/W1TC	0h	Access to Reserved Address
				Reset Source: hsrst_n
				`0h No access to reserved address occurred`
				`1h Access to reserved address occurred`

28	PED	R/W1TC	0h	Protocol Error in Data Phase
				Reset Source: hsrst_n
				`0h No protocol error in data phase`
				`1h Protocol error in data phase detected (MCAN_PSR[10-8] DLEC != 0.7)`

27	PEA	R/W1TC	0h	Protocol Error in Arbitration Phase
				Reset Source: hsrst_n
				`0h No protocol error in arbitration phase`
				`1h Protocol error in arbitration phase detected (MCAN_PSR[2-0] LEC != 0.7)`

Table 14-30955. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	WDI	R/W1TC	0h	Watchdog Interrupt Reset Source: hsrst_n 0h `No Message RAM Watchdog event occurred` 1h `Message RAM Watchdog event due to missing READY`
25	BO	R/W1TC	0h	Bus_Off Status Reset Source: hsrst_n 0h `Bus_Off status unchanged` 1h `Bus_Off status changed`
24	EW	R/W1TC	0h	Warning Status Reset Source: hsrst_n 0h `Error_Warning status unchanged` 1h `Error_Warning status changed`
23	EP	R/W1TC	0h	Error Passive Reset Source: hsrst_n 0h `Error_Passive status unchanged` 1h `Error_Passive status changed`
22	ELO	R/W1TC	0h	Error Logging Overflow Reset Source: hsrst_n 0h `CAN Error Logging Counter did not overflow` 1h `Overflow of CAN Error Logging Counter occurred`
21	BEU	R/W1TC	0h	Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by input signal generated by parity/ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets the MCAN_CCCR[0] INIT bit to 1. This is done to avoid transmission of corrupted data. Reset Source: hsrst_n 0h `No bit error detected when reading from Message RAM` 1h `Bit error detected, uncorrected (example: parity logic)`
20	RESERVED	NONE	0h	Reserved
19	DRX	R/W1TC	0h	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. Reset Source: hsrst_n 0h `No Rx Buffer updated` 1h `At least one received message stored into an Rx Buffer`
18	TOO	R/W1TC	0h	Timeout Occurred Reset Source: hsrst_n 0h `No timeout` 1h `Timeout reached`

Table 14-30955. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	MRAF	R/W1TC	0h	Message RAM Access Failure The flag is set, when the Rx Handler: a) has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. b) was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated respectively the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN module is switched into Restricted Operation Mode (see Restricted Operation Mode). To leave Restricted Operation Mode, the Host CPU has to reset the MCAN_CCCR[2] ASM bit. Reset Source: hsrst_n 0h No Message RAM access failure occurred 1h Message RAM access failure occurred
16	TSW	R/W1TC	0h	Timestamp Wraparound Reset Source: hsrst_n 0h No timestamp counter wrap-around 1h Timestamp counter wrapped around
15	TEFL	R/W1TC	0h	Tx Event FIFO Element Lost Reset Source: hsrst_n 0h No Tx Event FIFO element lost 1h Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W1TC	0h	Tx Event FIFO Full Reset Source: hsrst_n 0h Tx Event FIFO not full 1h Tx Event FIFO full
13	TEFW	R/W1TC	0h	Tx Event FIFO Watermark Reached Reset Source: hsrst_n 0h Tx Event FIFO fill level below watermark 1h Tx Event FIFO fill level reached watermark
12	TEFN	R/W1TC	0h	Tx Event FIFO New Entry Reset Source: hsrst_n 0h Tx Event FIFO unchanged 1h Tx Handler wrote Tx Event FIFO element
11	TFE	R/W1TC	0h	Tx FIFO Empty Reset Source: hsrst_n 0h Tx FIFO non-empty 1h Tx FIFO empty
10	TCF	R/W1TC	0h	Transmission Cancellation Finished Reset Source: hsrst_n 0h No transmission cancellation finished 1h Transmission cancellation finished

Table 14-30955. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TC	R/W1TC	0h	Transmission Completed Reset Source: hsrst_n 0h No transmission completed 1h Transmission completed
8	HPM	R/W1TC	0h	High Priority Message Reset Source: hsrst_n 0h No high priority message received 1h High priority message received
7	RF1L	R/W1TC	0h	Rx FIFO 1 Message Lost Reset Source: hsrst_n 0h No Rx FIFO 1 message lost 1h Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W1TC	0h	Rx FIFO 1 Full Reset Source: hsrst_n 0h Rx FIFO 1 not full 1h Rx FIFO 1 full
5	RF1W	R/W1TC	0h	Rx FIFO 1 Watermark Reached Reset Source: hsrst_n 0h Rx FIFO 1 fill level below watermark 1h Rx FIFO 1 fill level reached watermark
4	RF1N	R/W1TC	0h	Rx FIFO 1 New Message Reset Source: hsrst_n 0h No new message written to Rx FIFO 1 1h New message written to Rx FIFO 1
3	RF0L	R/W1TC	0h	Rx FIFO 0 Message Lost Reset Source: hsrst_n 0h No Rx FIFO 0 message lost 1h Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W1TC	0h	Rx FIFO 0 Full Reset Source: hsrst_n 0h Rx FIFO 0 not full 1h Rx FIFO 0 full
1	RF0W	R/W1TC	0h	Rx FIFO 0 Watermark Reached Reset Source: hsrst_n 0h Rx FIFO 0 fill level below watermark 1h Rx FIFO 0 fill level reached watermark
0	RF0N	R/W1TC	0h	Rx FIFO 0 New Message Reset Source: hsrst_n 0h No new message written to Rx FIFO 0 1h New message written to Rx FIFO 0

14.9.5.1.2.33 MCAN_CORE_IE Register

1 MCAN_CORE_IE Register (Offset = 54h) [reset = 0h]

Interrupt enable/disable

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Table 14-30956. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1054h**
MCU_MCAN0	**04E0 8054h**
MCU_MCAN1	**04E1 8054h**

Figure 14-10256. MCAN_CORE_IE Name Register

31	30	29	28	27	26	25	24
RESERVED		ARAE	PEDE	PEAE	WDIE	BOE	EWE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30958. MCAN_CORE_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARAE	R/W	0h	Access to Reserved Address Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

28	PEDE	R/W	0h	Protocol Error in Data Phase Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

26	WDIE	R/W	0h	Watchdog Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

Table 14-30958. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

25	BOE	R/W	0h	Bus_Off Status Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

24	EWE	R/W	0h	Warning Status Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

23	EPE	R/W	0h	Error Passive Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

22	ELOE	R/W	0h	Error Logging Overflow Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

21	BEUE	R/W	0h	Bit Error Uncorrected Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

20	BECE	R/W	0h	Bit Error Corrected Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Enable Reset Source: hsrst_n

18	TOOE	R/W	0h	Timeout Occurred Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

17	MRAFE	R/W	0h	Message RAM Access Failure Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

16	TSWE	R/W	0h	Timestamp Wraparound Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

15	TEFLE	R/W	0h	Tx Event FIFO Event Lost Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

14	TEFFE	R/W	0h	Tx Event FIFO Full Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

Table 14-30958. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

12	TEFNE	R/W	0h	Tx Event FIFO New Entry Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

11	TFEE	R/W	0h	Tx FIFO Empty Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

10	TCFE	R/W	0h	Transmission Cancellation Finished Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

9	TCE	R/W	0h	Transmission Completed Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

8	HPME	R/W	0h	High Priority Message Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

6	RF1FE	R/W	0h	Rx FIFO 1 Full Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

4	RF1NE	R/W	0h	Rx FIFO 1 New Message Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

Table 14-30958. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	RF0FE	R/W	0h	Rx FIFO 0 Full Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

0	RF0NE	R/W	0h	Rx FIFO 0 New Message Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

14.9.5.1.2.34 MCAN_CORE_ILS Register

1 MCAN_CORE_ILS Register (Offset = 58h) [reset = 0h]

Interrupt line select (m_can_int0 or m_can_int1)

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Table 14-30959. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1058h**
MCU_MCAN0	**04E0 8058h**
MCU_MCAN1	**04E1 8058h**

Figure 14-10257. MCAN_CORE_ILS Name Register

31	30	29	28	27	26	25	24
RESERVED		ARAL	PEDL	PEAL	WDIL	BOL	EWL
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-30961. MCAN_CORE_ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARAL	R/W	0h	Access to Reserved Address Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

28	PEDL	R/W	0h	Protocol Error in Data Phase Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

26	WDIL	R/W	0h	Watchdog Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

Table 14-30961. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	BOL	R/W	0h	Bus_Off Status Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
24	EWL	R/W	0h	Warning Status Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
23	EPL	R/W	0h	Error Passive Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
22	ELOL	R/W	0h	Error Logging Overflow Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
21	BEUL	R/W	0h	Bit Error Uncorrected Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
20	BECL	R/W	0h	Bit Error Corrected Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
19	DRXL	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
18	TOOL	R/W	0h	Timeout Occurred Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
17	MRAFL	R/W	0h	Message RAM Access Failure Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
16	TSWL	R/W	0h	Timestamp Wraparound Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
15	TEFLL	R/W	0h	Tx Event FIFO Event Lost Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1

Table 14-30961. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	TEFFL	R/W	0h	Tx Event FIFO Full Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
11	TFEL	R/W	0h	Tx FIFO Empty Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
10	TCFL	R/W	0h	Transmission Cancellation Finished Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
9	TCL	R/W	0h	Transmission Completed Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
8	HPML	R/W	0h	High Priority Message Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
6	RF1FL	R/W	0h	Rx FIFO 1 Full Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1

Table 14-30961. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
2	RF0FL	R/W	0h	Rx FIFO 0 Full Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1

14.9.5.1.2.35 MCAN_CORE_ILE Register

1 MCAN_CORE_ILE Register (Offset = 5Ch) [reset = 0h]

Enable/disable interrupt lines m_can_int0 / m_can_int1

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Table 14-30962. Instance Table

Instance Name	Physical Address
MCAN0	**2070 105Ch**
MCU_MCAN0	**04E0 805Ch**
MCU_MCAN1	**04E1 805Ch**

Figure 14-10258. MCAN_CORE_ILE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EINT1	EINT0
NONE						R/W	R/W
0h						0h	0h

Table 14-30964. MCAN_CORE_ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved

1	EINT1	R/W	0h	Enable Interrupt Line 1
				Reset Source: hsrst_n
				`0h      Interrupt line INT1 disabled`
				`1h      Interrupt line INT1 enabled`

0	EINT0	R/W	0h	Enable Interrupt Line 0
				Reset Source: hsrst_n
				`0h      Interrupt line INT0 disabled`
				`1h      Interrupt line INT0 enabled`

14.9.5.1.2.36 MCAN_CORE_RESERVED55 Register

1 MCAN_CORE_RESERVED55 Register (Offset = 60h) [reset = 0h]

Reserved field

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Table 14-30965. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1060h**
MCU_MCAN0	**04E0 8060h**
MCU_MCAN1	**04E1 8060h**

Figure 14-10259. MCAN_CORE_RESERVED55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30967. MCAN_CORE_RESERVED55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.37 MCAN_CORE_RESERVED66 Register

1 MCAN_CORE_RESERVED66 Register (Offset = 64h) [reset = 0h]

Reserved field

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Table 14-30968. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1064h**
MCU_MCAN0	**04E0 8064h**
MCU_MCAN1	**04E1 8064h**

Figure 14-10260. MCAN_CORE_RESERVED66 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30970. MCAN_CORE_RESERVED66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.38 MCAN_CORE_RESERVED77 Register

1 MCAN_CORE_RESERVED77 Register (Offset = 68h) [reset = 0h]

Reserved field

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Table 14-30971. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1068h**
MCU_MCAN0	**04E0 8068h**
MCU_MCAN1	**04E1 8068h**

Figure 14-10261. MCAN_CORE_RESERVED77 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30973. MCAN_CORE_RESERVED77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.39 MCAN_CORE_RESERVED88 Register

1 MCAN_CORE_RESERVED88 Register (Offset = 6Ch) [reset = 0h]

Reserved field

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Table 14-30974. Instance Table

Instance Name	Physical Address
MCAN0	**2070 106Ch**
MCU_MCAN0	**04E0 806Ch**
MCU_MCAN1	**04E1 806Ch**

Figure 14-10262. MCAN_CORE_RESERVED88 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30976. MCAN_CORE_RESERVED88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.40 MCAN_CORE_RESERVED99 Register

1 MCAN_CORE_RESERVED99 Register (Offset = 70h) [reset = 0h]

Reserved field

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Table 14-30977. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1070h**
MCU_MCAN0	**04E0 8070h**
MCU_MCAN1	**04E1 8070h**

Figure 14-10263. MCAN_CORE_RESERVED99 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30979. MCAN_CORE_RESERVED99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.41 MCAN_CORE_RESERVED1010 Register

1 MCAN_CORE_RESERVED1010 Register (Offset = 74h) [reset = 0h]

Reserved field

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Table 14-30980. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1074h**
MCU_MCAN0	**04E0 8074h**
MCU_MCAN1	**04E1 8074h**

Figure 14-10264. MCAN_CORE_RESERVED1010 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30982. MCAN_CORE_RESERVED1010 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.42 MCAN_CORE_RESERVED1111 Register

1 MCAN_CORE_RESERVED1111 Register (Offset = 78h) [reset = 0h]

Reserved field

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Table 14-30983. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1078h**
MCU_MCAN0	**04E0 8078h**
MCU_MCAN1	**04E1 8078h**

Figure 14-10265. MCAN_CORE_RESERVED1111 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30985. MCAN_CORE_RESERVED1111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.43 MCAN_CORE_RESERVED1212 Register

1 MCAN_CORE_RESERVED1212 Register (Offset = 7Ch) [reset = 0h]

Reserved field

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Table 14-30986. Instance Table

Instance Name	Physical Address
MCAN0	**2070 107Ch**
MCU_MCAN0	**04E0 807Ch**
MCU_MCAN1	**04E1 807Ch**

Figure 14-10266. MCAN_CORE_RESERVED1212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-30988. MCAN_CORE_RESERVED1212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.44 MCAN_CORE_GFC Register

1 MCAN_CORE_GFC Register (Offset = 80h) [reset = 0h]

Handling of non-matching frames and remote frames

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Table 14-30989. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1080h**
MCU_MCAN0	**04E0 8080h**
MCU_MCAN1	**04E1 8080h**

Figure 14-10267. MCAN_CORE_GFC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ANFS		ANFE		RRFS	RRFE
NONE		R/W		R/W		R/W	R/W
0h		0h		0h		0h	0h

Table 14-30991. MCAN_CORE_GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:4	ANFS	R/W	0h	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. Reset Source: hsrst_n 0h Accept in Rx FIFO 0 1h Accept in Rx FIFO 1 2h Reject 3h Reject
3:2	ANFE	R/W	0h	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. Reset Source: hsrst_n 0h Accept in Rx FIFO 0 1h Accept in Rx FIFO 1 2h Reject 3h Reject

Table 14-30991. MCAN_CORE_GFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RRFS	R/W	0h	Reject Remote Frames Standard Reset Source: hsrst_n 0h `Filter remote frames with 11-bit standard IDs` 1h `Reject all remote frames with 11-bit standard IDs`
0	RRFE	R/W	0h	Reject Remote Frames Extended Reset Source: hsrst_n 0h `Filter remote frames with 29-bit extended IDs` 1h `Reject all remote frames with 29-bit extended IDs`

14.9.5.1.2.45 MCAN_CORE_SIDFC Register

1 MCAN_CORE_SIDFC Register (Offset = 84h) [reset = 0h]

Number of filter elements, pointer to start of filter list

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Table 14-30992. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1084h**
MCU_MCAN0	**04E0 8084h**
MCU_MCAN1	**04E1 8084h**

Figure 14-10268. MCAN_CORE_SIDFC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
LSS							
R/W							
0h							
15	14	13	12	11	10	9	8
FLSSA							
R/W							
0h							
7	6	5	4	3	2	1	0
FLSSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-30994. MCAN_CORE_SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23:16	LSS	R/W	0h	List Size Standard
				Reset Source: hsrst_n
				`0h` `No standard Message ID filter`
				`1h-80h` `Number of standard Message ID filter elements`
				`>80h` `Values greater than 128 are interpreted as 128`

15:2	FLSSA	R/W	0h	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.46 MCAN_CORE_XIDFC Register

1 MCAN_CORE_XIDFC Register (Offset = 88h) [reset = 0h]

Number of filter elements, pointer to start of filter list

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Table 14-30995. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1088h**
MCU_MCAN0	**04E0 8088h**
MCU_MCAN1	**04E1 8088h**

Figure 14-10269. MCAN_CORE_XIDFC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	LSE						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
FLESA							
R/W							
0h							
7	6	5	4	3	2	1	0
FLESA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-30997. MCAN_CORE_XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	LSE	R/W	0h	List Size Extended Reset Source: hsrst_n 0h No extended Message ID filter 1h-40h Number of extended Message ID filter elements >40h Values greater than 64 are interpreted as 64
15:2	FLESA	R/W	0h	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.47 MCAN_CORE_RESERVED1313 Register

1 MCAN_CORE_RESERVED1313 Register (Offset = 8Ch) [reset = 0h]

Reserved field

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Table 14-30998. Instance Table

Instance Name	Physical Address
MCAN0	**2070 108Ch**
MCU_MCAN0	**04E0 808Ch**
MCU_MCAN1	**04E1 808Ch**

Figure 14-10270. MCAN_CORE_RESERVED1313 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31000. MCAN_CORE_RESERVED1313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.48 MCAN_CORE_XIDAM Register

1 MCAN_CORE_XIDAM Register (Offset = 90h) [reset = 1FFFFFFFh]

29-bit logical AND mask for J1939

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Table 14-31001. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1090h**
MCU_MCAN0	**04E0 8090h**
MCU_MCAN1	**04E1 8090h**

Figure 14-10271. MCAN_CORE_XIDAM Name Register

31	30	29	28	27	26	25	24
RESERVED			EIDM				
NONE			R/W				
0h			1FFFFFFFh				
23	22	21	20	19	18	17	16
EIDM							
R/W							
1FFFFFFFh							
15	14	13	12	11	10	9	8
EIDM							
R/W							
1FFFFFFFh							
7	6	5	4	3	2	1	0
EIDM							
R/W							
1FFFFFFFh							

Table 14-31003. MCAN_CORE_XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	EIDM	R/W	1FFFFFFFh	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Reset Source: hsrst_n

14.9.5.1.2.49 MCAN_CORE_HPMS Register

1 MCAN_CORE_HPMS Register (Offset = 94h) [reset = 0h]

Status monitoring of incoming high priority messages

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Table 14-31004. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1094h**
MCU_MCAN0	**04E0 8094h**
MCU_MCAN1	**04E1 8094h**

Figure 14-10272. MCAN_CORE_HPMS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
FLST	FIDX						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
MSI		BIDX					
R		R					
0h		0h					

Table 14-31006. MCAN_CORE_HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	FLST	R	0h	Filter List Indicates the filter list of the matching filter element. Reset Source: hsrst_n 0h Standard Filter List 1h Extended Filter List
14:8	FIDX	R	0h	Filter Index Index of matching filter element. Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1. Reset Source: hsrst_n
7:6	MSI	R	0h	Message Storage Indicator Reset Source: hsrst_n 0h No FIFO selected 1h FIFO message lost 2h Message stored in FIFO 0 3h Message stored in FIFO 1

Table 14-31006. MCAN_CORE_HPMS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BIDX	R	0h	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when the MCAN_HPMS[7-6] MSI = 1h. Reset Source: hsrst_n

14.9.5.1.2.50 MCAN_CORE_NDAT1 Register

1 MCAN_CORE_NDAT1 Register (Offset = 98h) [reset = 0h]

NewDat flags of dedicated Rx buffers 0-31

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Table 14-31007. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1098h**
MCU_MCAN0	**04E0 8098h**
MCU_MCAN1	**04E1 8098h**

Figure 14-10273. MCAN_CORE_NDAT1 Name Register

31	30	29	28	27	26	25	24
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31009. MCAN_CORE_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	ND31	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

30	ND30	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

29	ND29	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

28	ND28	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

Table 14-31009. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ND27	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
26	ND26	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
25	ND25	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
24	ND24	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
23	ND23	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
22	ND22	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
21	ND21	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
20	ND20	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
19	ND19	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
18	ND18	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
17	ND17	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-31009. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ND16	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
15	ND15	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
14	ND14	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
13	ND13	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
12	ND12	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
11	ND11	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
10	ND10	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
9	ND9	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
8	ND8	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
7	ND7	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
6	ND6	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-31009. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

5	ND5	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

4	ND4	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

3	ND3	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

2	ND2	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

1	ND1	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

0	ND0	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

14.9.5.1.2.51 MCAN_CORE_NDAT2 Register

1 MCAN_CORE_NDAT2 Register (Offset = 9Ch) [reset = 0h]

NewDat flags of dedicated Rx buffers 32-63

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Table 14-31010. Instance Table

Instance Name	Physical Address
MCAN0	**2070 109Ch**
MCU_MCAN0	**04E0 809Ch**
MCU_MCAN1	**04E1 809Ch**

Figure 14-10274. MCAN_CORE_NDAT2 Name Register

31	30	29	28	27	26	25	24
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31012. MCAN_CORE_NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	ND63	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

30	ND62	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

29	ND61	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

28	ND60	R/W1TC	0h	New Data
				Reset Source: hsrst_n
				`0h Rx Buffer not updated`
				`1h Rx Buffer updated from new message`

Table 14-31012. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ND59	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
26	ND58	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
25	ND57	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
24	ND56	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
23	ND55	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
22	ND54	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
21	ND53	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
20	ND52	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
19	ND51	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
18	ND50	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
17	ND49	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-31012. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ND48	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
15	ND47	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
14	ND46	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
13	ND45	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
12	ND44	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
11	ND43	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
10	ND42	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
9	ND41	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
8	ND40	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
7	ND39	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
6	ND38	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-31012. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ND37	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
4	ND36	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
3	ND35	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
2	ND34	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
1	ND33	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
0	ND32	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

14.9.5.1.2.52 MCAN_CORE_RXF0C Register

1 MCAN_CORE_RXF0C Register (Offset = A0h) [reset = 0h]

FIFO 0 operation mode, watermark, size and start address

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Table 14-31013. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A0h**
MCU_MCAN0	**04E0 80A0h**
MCU_MCAN1	**04E1 80A0h**

Figure 14-10275. MCAN_CORE_RXF0C Name Register

31	30	29	28	27	26	25	24
F0OM	F0WM						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	F0S						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
F0SA							
R/W							
0h							
7	6	5	4	3	2	1	0
F0SA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-31015. MCAN_CORE_RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description

31	F0OM	R/W	0h	FIFO 0 Operation Mode
				FIFO 0 can be operated in blocking or in overwrite mode (see Rx FIFOs).
				Reset Source: hsrst_n
				`0h FIFO 0 blocking mode`
				`1h FIFO 0 overwrite mode`

30:24	F0WM	R/W	0h	Rx FIFO 0 Watermark
				Reset Source: hsrst_n
				`0h watermark interrupt disabled`
				`1h-40h Level for Rx FIFO 0 watermark interrupt (MCAN_IR[1] RF0W)`
				`>40h watermark interrupt disabled`

23	RESERVED	NONE	0h	Reserved

Table 14-31015. MCAN_CORE_RXF0C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

22:16	F0S	R/W	0h	Rx FIFO 0 Size
				Reset Source: hsrst_n
				`0h` `No Rx FIFO 0`
				`1h-40h` `Number of Rx FIFO 0 elements`
				`>40h` `Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to MCAN_RXF0C[22-16] F0S - 1.`

15:2	F0SA	R/W	0h	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.53 MCAN_CORE_RXF0S Register

1 MCAN_CORE_RXF0S Register (Offset = A4h) [reset = 0h]

FIFO 0 message lost/full indication, put index, get index and fill level

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Table 14-31016. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A4h**
MCU_MCAN0	**04E0 80A4h**
MCU_MCAN1	**04E1 80A4h**

Figure 14-10276. MCAN_CORE_RXF0S Name Register

31	30	29	28	27	26	25	24
RESERVED						RF0L	F0F
NONE						R	R
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		F0PI					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		F0GI					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	F0FL						
NONE	R						
0h	0h						

Table 14-31018. MCAN_CORE_RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	RF0L	R	0h	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag MCAN_IR[3] RF0L. When the MCAN_IR[3] RF0L flag is reset, this bit is also reset. Note: OverWriting the oldest message when the MCAN_RXF0C[31] F0OM = 1h Reset Source: hsrst_n 0h `No Rx FIFO 0 message lost` 1h `Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero`
24	F0F	R	0h	Rx FIFO 0 Full Reset Source: hsrst_n 0h `Rx FIFO 0 not full` 1h `Rx FIFO 0 full`
23:22	RESERVED	NONE	0h	Reserved
21:16	F0PI	R	0h	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Reset Source: hsrst_n

Table 14-31018. MCAN_CORE_RXF0S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	RESERVED	NONE	0h	Reserved
13:8	F0GI	R	0h	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	F0FL	R	0h	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. Reset Source: hsrst_n

14.9.5.1.2.54 MCAN_CORE_RXF0A Register

1 MCAN_CORE_RXF0A Register (Offset = A8h) [reset = 0h]

FIFO 0 acknowledge last index of read buffers, updates get index and fill level

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Table 14-31019. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A8h**
MCU_MCAN0	**04E0 80A8h**
MCU_MCAN1	**04E1 80A8h**

Figure 14-10277. MCAN_CORE_RXF0A Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		F0AI					
NONE		R/W					
0h		0h					

Table 14-31021. MCAN_CORE_RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to the MCAN_RXF0A[5-0] F0AI field. This will set the Rx FIFO 0 Get Index MCAN_RXF0S[13-8] F0GI field to the MCAN_RXF0A[5-0] F0AI field + 1 and update the FIFO 0 Fill Level MCAN_RXF0S[6-0] F0FL field. Reset Source: hsrst_n

14.9.5.1.2.55 MCAN_CORE_RXBC Register

1 MCAN_CORE_RXBC Register (Offset = ACh) [reset = 0h]

Start address of Rx buffer section

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Table 14-31022. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10ACh**
MCU_MCAN0	**04E0 80ACh**
MCU_MCAN1	**04E1 80ACh**

Figure 14-10278. MCAN_CORE_RXBC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RBSA							
R/W							
0h							
7	6	5	4	3	2	1	0
RBSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-31024. MCAN_CORE_RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:2	RBSA	R/W	0h	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address, see Message RAM Configuration). Also used to reference debug messages A, B, C. Note: Debug feature is not supported. Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.56 MCAN_CORE_RXF1C Register

1 MCAN_CORE_RXF1C Register (Offset = B0h) [reset = 0h]

FIFO 1 operation mode, watermark, size and start address

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Table 14-31025. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B0h**
MCU_MCAN0	**04E0 80B0h**
MCU_MCAN1	**04E1 80B0h**

Figure 14-10279. MCAN_CORE_RXF1C Name Register

31	30	29	28	27	26	25	24
F1OM	F1WM						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	F1S						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
F1SA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F1SA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-31027. MCAN_CORE_RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description

31	F1OM	R/W	0h	FIFO 1 Operation Mode
				FIFO 1 can be operated in blocking or in overwrite mode (see Rx FIFOs).
				Reset Source: hsrst_n
				`0h FIFO 1 blocking mode`
				`1h FIFO 1 overwrite mode`

30:24	F1WM	R/W	0h	Rx FIFO 1 Watermark
				Reset Source: hsrst_n
				`0h watermark interrupt disabled`
				`1h-40h Level for Rx FIFO 1 watermark interrupt (MCAN_IR[5] RF1W)`
				`>40h watermark interrupt disabled`

23	RESERVED	NONE	0h	Reserved

Table 14-31027. MCAN_CORE_RXF1C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:16	F1S	R/W	0h	Rx FIFO 1 Size Reset Source: hsrst_n 0h No Rx FIFO 1 1h-40h Number of Rx FIFO 1 elements >40h Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to MCAN_RXF1C[22-16] F1S - 1.
15:2	F1SA	R/W	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.57 MCAN_CORE_RXF1S Register

1 MCAN_CORE_RXF1S Register (Offset = B4h) [reset = 0h]

FIFO 1 message lost/full indication, put index, get index and fill level

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Table 14-31028. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B4h**
MCU_MCAN0	**04E0 80B4h**
MCU_MCAN1	**04E1 80B4h**

Figure 14-10280. MCAN_CORE_RXF1S Name Register

31	30	29	28	27	26	25	24
DMS		RESERVED				RF1L	F1F
R		NONE				R	R
0h		0h				0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		F1PI					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		F1GI					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	F1FL						
NONE	R						
0h	0h						

Table 14-31030. MCAN_CORE_RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description

31:30	DMS	R	0h	Debug Message Status
				Note: Debug feature is not supported.
				Reset Source: hsrst_n
				`0h` `Idle state, wait for reception of debug messages, DMA request is cleared`
				`1h` `Debug message A received`
				`2h` `Debug messages A, B received`
				`3h` `Debug messages A, B, C received, DMA request is set`

29:26	RESERVED	NONE	0h	Reserved

25	RF1L	R	0h	Rx FIFO 1 Message Lost
				This bit is a copy of interrupt flag MCAN_IR[7] RF1L. When the MCAN_IR[7] RF1L flag is reset, this bit is also reset.
				Note: OverWriting the oldest message when the MCAN_RXF1C[31] F1OM = 1h
				Reset Source: hsrst_n
				`0h` `No Rx FIFO 1 message lost`
				`1h` `Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero`

Table 14-31030. MCAN_CORE_RXF1S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

24	F1F	R	0h	Rx FIFO 1 Full
				Reset Source: hsrst_n
				`0h Rx FIFO 1 not full`
				`1h Rx FIFO 1 full`

23:22	RESERVED	NONE	0h	Reserved
21:16	F1PI	R	0h	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Reset Source: hsrst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	F1GI	R	0h	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	F1FL	R	0h	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. Reset Source: hsrst_n

14.9.5.1.2.58 MCAN_CORE_RXF1A Register

1 MCAN_CORE_RXF1A Register (Offset = B8h) [reset = 0h]

FIFO 1 acknowledge last index of read buffers, updates get index and fill level

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Table 14-31031. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B8h**
MCU_MCAN0	**04E0 80B8h**
MCU_MCAN1	**04E1 80B8h**

Figure 14-10281. MCAN_CORE_RXF1A Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		F1AI					
NONE		R/W					
0h		0h					

Table 14-31033. MCAN_CORE_RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to the MCAN_RXF1A[5-0] F1AI field. This will set the Rx FIFO 1 Get Index MCAN_RXF1S[13-8] F1GI field to the MCAN_RXF1A[5-0] F1AI field + 1 and update the FIFO 1 Fill Level MCAN_RXF1S[6-0] F1FL field. Reset Source: hsrst_n

14.9.5.1.2.59 MCAN_CORE_RXESC Register

1 MCAN_CORE_RXESC Register (Offset = BCh) [reset = 0h]

Configure data field size for storage of accepted frames

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Table 14-31034. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10BCh**
MCU_MCAN0	**04E0 80BCh**
MCU_MCAN1	**04E1 80BCh**

Figure 14-10282. MCAN_CORE_RXESC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">RBDS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">F1DS</td><td>RESERVED</td><td colspan="3">F0DS</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-31036. MCAN_CORE_RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	RBDS	R/W	0h	Rx Buffer Data Field Size Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field
7	RESERVED	NONE	0h	Reserved

Table 14-31036. MCAN_CORE_RXESC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	F1DS	R/W	0h	Rx FIFO 1 Data Field Size Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field
3	RESERVED	NONE	0h	Reserved
2:0	F0DS	R/W	0h	Rx FIFO 0 Data Field Size Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by the MCAN_RXESC register are stored to the Rx Buffer respectively Rx FIFO element. The rest of the frame's data field is ignored. Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field

14.9.5.1.2.60 MCAN_CORE_TXBC Register

1 MCAN_CORE_TXBC Register (Offset = C0h) [reset = 0h]

Configure Tx FIFO/Queue mode, Tx FIFO/Queue size, number of dedicated Tx buffers, Tx buffer start address

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Table 14-31037. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C0h**
MCU_MCAN0	**04E0 80C0h**
MCU_MCAN1	**04E1 80C0h**

Figure 14-10283. MCAN_CORE_TXBC Name Register

31	30	29	28	27	26	25	24
RESERVED	TFQM	TFQS					
NONE	R/W	R/W					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED		NDTB					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
TBSA							
R/W							
0h							
7	6	5	4	3	2	1	0
TBSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-31039. MCAN_CORE_TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved

30	TFQM	R/W	0h	Tx FIFO/Queue Mode
				Reset Source: hsrst_n
				`0h` `Tx FIFO operation`
				`1h` `Tx Queue operation`

29:24	TFQS	R/W	0h	Transmit FIFO/Queue Size
				Reset Source: hsrst_n
				`0h` `No Tx FIFO/Queue`
				`1h-20h` `Number of Tx Buffers used for Tx FIFO/Queue`
				`>20h` `Values greater than 32 are interpreted as 32`

23:22	RESERVED	NONE	0h	Reserved

Table 14-31039. MCAN_CORE_TXBC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	NDTB	R/W	0h	Number of Dedicated Transmit Buffers Reset Source: hsrst_n 0h No Dedicated Tx Buffers 1h-20h Number of Dedicated Tx Buffers >20h Values greater than 32 are interpreted as 32
15:2	TBSA	R/W	0h	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Message RAM Configuration). Note: Be aware that the sum of the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.61 MCAN_CORE_TXFQS Register

1 MCAN_CORE_TXFQS Register (Offset = C4h) [reset = 0h]

Tx FIFO/Queue full indication and put index, Tx FIFO get index and fill level

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Table 14-31040. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C4h**
MCU_MCAN0	**04E0 80C4h**
MCU_MCAN1	**04E1 80C4h**

Figure 14-10284. MCAN_CORE_TXFQS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TFQF	TFQPI				
NONE		R	R				
0h		0h	0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TFGI				
NONE			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TFFL					
NONE		R					
0h		0h					

Table 14-31042. MCAN_CORE_TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved

21	TFQF	R	0h	Tx FIFO/Queue Full
				Reset Source: hsrst_n
				`0h Tx FIFO/Queue not full`
				`1h Tx FIFO/Queue full`

20:16	TFQPI	R	0h	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TFGI	R	0h	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). Reset Source: hsrst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-31042. MCAN_CORE_TXFQS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	TFFL	R	0h	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from the MCAN_TXFQS[12-8] TFGI field, range 0 to 32. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Reset Source: hsrst_n

14.9.5.1.2.62 MCAN_CORE_TXESC Register

1 MCAN_CORE_TXESC Register (Offset = C8h) [reset = 0h]

Configure data field size for frame transmission

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Table 14-31043. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C8h**
MCU_MCAN0	**04E0 80C8h**
MCU_MCAN1	**04E1 80C8h**

Figure 14-10285. MCAN_CORE_TXESC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TBDS		
NONE					R/W		
0h					0h		

Table 14-31045. MCAN_CORE_TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TBDS	R/W	0h	Tx Buffer Data Field Size Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC[2-0] TBDS, the bytes not defined by the Tx Buffer are transmitted as CCh (padding bytes). Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field

14.9.5.1.2.63 MCAN_CORE_TXBRP Register

1 MCAN_CORE_TXBRP Register (Offset = CCh) [reset = 0h]

Tx buffers with pending transmission request

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Table 14-31046. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10CCh**
MCU_MCAN0	**04E0 80CCh**
MCU_MCAN1	**04E1 80CCh**

Figure 14-10286. MCAN_CORE_TXBRP Name Register

31	30	29	28	27	26	25	24
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31048. MCAN_CORE_TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRP31	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
30	TRP30	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
29	TRP29	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
28	TRP28	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

Table 14-31048. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	TRP27	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
26	TRP26	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
25	TRP25	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
24	TRP24	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
23	TRP23	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
22	TRP22	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
21	TRP21	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
20	TRP20	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
19	TRP19	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
18	TRP18	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
17	TRP17	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

Table 14-31048. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TRP16	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
15	TRP15	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
14	TRP14	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
13	TRP13	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
12	TRP12	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
11	TRP11	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
10	TRP10	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
9	TRP9	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
8	TRP8	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
7	TRP7	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
6	TRP6	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

Table 14-31048. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TRP5	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
4	TRP4	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
3	TRP3	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
2	TRP2	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
1	TRP1	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
0	TRP0	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

14.9.5.1.2.64 MCAN_CORE_TXBAR Register

1 MCAN_CORE_TXBAR Register (Offset = D0h) [reset = 0h]

Add transmission requests

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Table 14-31049. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D0h**
MCU_MCAN0	**04E0 80D0h**
MCU_MCAN1	**04E1 80D0h**

Figure 14-10287. MCAN_CORE_TXBAR Name Register

31	30	29	28	27	26	25	24
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31051. MCAN_CORE_TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description

31	AR31	R/W1TC	0h	Add Request
				Reset Source: hsrst_n
				`0h No transmission request added`
				`1h Transmission requested added`

30	AR30	R/W1TC	0h	Add Request
				Reset Source: hsrst_n
				`0h No transmission request added`
				`1h Transmission requested added`

29	AR29	R/W1TC	0h	Add Request
				Reset Source: hsrst_n
				`0h No transmission request added`
				`1h Transmission requested added`

28	AR28	R/W1TC	0h	Add Request
				Reset Source: hsrst_n
				`0h No transmission request added`
				`1h Transmission requested added`

Table 14-31051. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	AR27	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
26	AR26	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
25	AR25	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
24	AR24	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
23	AR23	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
22	AR22	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
21	AR21	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
20	AR20	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
19	AR19	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
18	AR18	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
17	AR17	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

Table 14-31051. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AR16	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
15	AR15	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
14	AR14	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
13	AR13	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
12	AR12	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
11	AR11	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
10	AR10	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
9	AR9	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
8	AR8	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
7	AR7	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
6	AR6	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

Table 14-31051. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	AR5	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
4	AR4	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
3	AR3	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
2	AR2	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
1	AR1	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
0	AR0	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

14.9.5.1.2.65 MCAN_CORE_TXBCR Register

1 MCAN_CORE_TXBCR Register (Offset = D4h) [reset = 0h]

Request cancellation of pending transmissions

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Table 14-31052. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D4h**
MCU_MCAN0	**04E0 80D4h**
MCU_MCAN1	**04E1 80D4h**

Figure 14-10288. MCAN_CORE_TXBCR Name Register

31	30	29	28	27	26	25	24
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31054. MCAN_CORE_TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description

31	CR31	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

30	CR30	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

29	CR29	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

28	CR28	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

Table 14-31054. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CR27	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
26	CR26	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
25	CR25	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
24	CR24	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
23	CR23	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
22	CR22	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
21	CR21	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
20	CR20	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
19	CR19	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
18	CR18	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
17	CR17	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending

Table 14-31054. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CR16	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
15	CR15	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
14	CR14	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
13	CR13	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
12	CR12	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
11	CR11	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
10	CR10	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
9	CR9	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
8	CR8	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
7	CR7	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
6	CR6	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending

Table 14-31054. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CR5	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
4	CR4	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
3	CR3	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
2	CR2	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
1	CR1	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
0	CR0	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending

14.9.5.1.2.66 MCAN_CORE_TXBTO Register

1 MCAN_CORE_TXBTO Register (Offset = D8h) [reset = 0h]

Signals successful transmissions, set when corresponding TXBRP flag is cleared

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Table 14-31055. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D8h**
MCU_MCAN0	**04E0 80D8h**
MCU_MCAN1	**04E1 80D8h**

Figure 14-10289. MCAN_CORE_TXBTO Name Register

31	30	29	28	27	26	25	24
TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31057. MCAN_CORE_TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description

31	TO31	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

30	TO30	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

29	TO29	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

28	TO28	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

Table 14-31057. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	TO27	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
26	TO26	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
25	TO25	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
24	TO24	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
23	TO23	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
22	TO22	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
21	TO21	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
20	TO20	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
19	TO19	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
18	TO18	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
17	TO17	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred

Table 14-31057. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

16	TO16	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

15	TO15	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

14	TO14	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

13	TO13	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

12	TO12	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

11	TO11	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

10	TO10	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

9	TO9	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

8	TO8	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

7	TO7	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

6	TO6	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

Table 14-31057. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TO5	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
4	TO4	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
3	TO3	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
2	TO2	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
1	TO1	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
0	TO0	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred

14.9.5.1.2.67 MCAN_CORE_TXBCF Register

1 MCAN_CORE_TXBCF Register (Offset = DCh) [reset = 0h]

Signals successful transmit cancellation, set when corresponding TXBRP flag is cleared after cancellation request

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Table 14-31058. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10DCh**
MCU_MCAN0	**04E0 80DCh**
MCU_MCAN1	**04E1 80DCh**

Figure 14-10290. MCAN_CORE_TXBCF Name Register

31	30	29	28	27	26	25	24
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31060. MCAN_CORE_TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description

31	CF31	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

30	CF30	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

29	CF29	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

28	CF28	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

Table 14-31060. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CF27	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
26	CF26	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
25	CF25	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
24	CF24	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
23	CF23	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
22	CF22	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
21	CF21	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
20	CF20	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
19	CF19	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
18	CF18	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
17	CF17	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished

Table 14-31060. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CF16	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
15	CF15	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
14	CF14	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
13	CF13	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
12	CF12	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
11	CF11	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
10	CF10	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
9	CF9	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
8	CF8	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
7	CF7	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
6	CF6	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished

Table 14-31060. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

5	CF5	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

4	CF4	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

3	CF3	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

2	CF2	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

1	CF1	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

0	CF0	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

14.9.5.1.2.68 MCAN_CORE_TXBTIE Register

1 MCAN_CORE_TXBTIE Register (Offset = E0h) [reset = 0h]

Enable transmit interrupts for selected Tx buffers

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Table 14-31061. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E0h**
MCU_MCAN0	**04E0 80E0h**
MCU_MCAN1	**04E1 80E0h**

Figure 14-10291. MCAN_CORE_TXBTIE Name Register

31	30	29	28	27	26	25	24
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31063. MCAN_CORE_TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description

31	TIE31	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

30	TIE30	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

29	TIE29	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

28	TIE28	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

Table 14-31063. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

27	TIE27	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

26	TIE26	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

25	TIE25	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

24	TIE24	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

23	TIE23	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

22	TIE22	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

21	TIE21	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

20	TIE20	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

19	TIE19	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

18	TIE18	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

17	TIE17	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

Table 14-31063. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

16	TIE16	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

15	TIE15	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

14	TIE14	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

13	TIE13	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

12	TIE12	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

11	TIE11	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

10	TIE10	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

9	TIE9	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

8	TIE8	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

7	TIE7	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

6	TIE6	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

Table 14-31063. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

5	TIE5	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

4	TIE4	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

3	TIE3	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

2	TIE2	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

1	TIE1	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

0	TIE0	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

14.9.5.1.2.69 MCAN_CORE_TXBCIE Register

1 MCAN_CORE_TXBCIE Register (Offset = E4h) [reset = 0h]

Enable cancellation finished interrupts for selected Tx buffers

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Table 14-31064. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E4h**
MCU_MCAN0	**04E0 80E4h**
MCU_MCAN1	**04E1 80E4h**

Figure 14-10292. MCAN_CORE_TXBCIE Name Register

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31066. MCAN_CORE_TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
30	CFIE30	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
29	CFIE29	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
28	CFIE28	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-31066. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CFIE27	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
26	CFIE26	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
25	CFIE25	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
24	CFIE24	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
23	CFIE23	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
22	CFIE22	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
21	CFIE21	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
20	CFIE20	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
19	CFIE19	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
18	CFIE18	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
17	CFIE17	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-31066. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CFIE16	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
15	CFIE15	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
14	CFIE14	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
13	CFIE13	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
12	CFIE12	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
11	CFIE11	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
10	CFIE10	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
9	CFIE9	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
8	CFIE8	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
7	CFIE7	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
6	CFIE6	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-31066. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CFIE5	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
4	CFIE4	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
3	CFIE3	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
2	CFIE2	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
1	CFIE1	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
0	CFIE0	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

14.9.5.1.2.70 MCAN_CORE_RESERVED1414 Register

1 MCAN_CORE_RESERVED1414 Register (Offset = E8h) [reset = 0h]

Reserved Field

Return to Summary Table

Table 14-31067. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E8h**
MCU_MCAN0	**04E0 80E8h**
MCU_MCAN1	**04E1 80E8h**

Figure 14-10293. MCAN_CORE_RESERVED1414 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31069. MCAN_CORE_RESERVED1414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.71 MCAN_CORE_RESERVED1515 Register

1 MCAN_CORE_RESERVED1515 Register (Offset = ECh) [reset = 0h]

Reserved Field

Return to Summary Table

Table 14-31070. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10ECh**
MCU_MCAN0	**04E0 80ECh**
MCU_MCAN1	**04E1 80ECh**

Figure 14-10294. MCAN_CORE_RESERVED1515 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31072. MCAN_CORE_RESERVED1515 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.72 MCAN_CORE_TXEFC Register

1 MCAN_CORE_TXEFC Register (Offset = F0h) [reset = 0h]

Tx event FIFO watermark, size and start address

Return to Summary Table

Table 14-31073. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F0h**
MCU_MCAN0	**04E0 80F0h**
MCU_MCAN1	**04E1 80F0h**

Figure 14-10295. MCAN_CORE_TXEFC Name Register

31	30	29	28	27	26	25	24
RESERVED		EFWM					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		EFS					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
EFSA							
R/W							
0h							
7	6	5	4	3	2	1	0
EFSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-31075. MCAN_CORE_TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	EFWM	R/W	0h	Event FIFO Watermark Reset Source: hsrst_n 0h Watermark interrupt disabled 1h-20h Level for Tx Event FIFO watermark interrupt (MCAN_IR[13] TEFW) >20h Watermark interrupt disabled
23:22	RESERVED	NONE	0h	Reserved
21:16	EFS	R/W	0h	Event FIFO Size Reset Source: hsrst_n 0h Tx Event FIFO disabled 1h-20h Number of Tx Event FIFO elements >20h Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to MCAN_TXEFC[21-16] EFS field - 1.

Table 14-31075. MCAN_CORE_TXEFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:2	EFSA	R/W	0h	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.73 MCAN_CORE_TXEFS Register

1 MCAN_CORE_TXEFS Register (Offset = F4h) [reset = 0h]

Tx event FIFO element lost/full indication, put index, get index, and fill level

Return to Summary Table

Table 14-31076. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F4h**
MCU_MCAN0	**04E0 80F4h**
MCU_MCAN1	**04E1 80F4h**

Figure 14-10296. MCAN_CORE_TXEFS Name Register

31	30	29	28	27	26	25	24
RESERVED						TEFL	EFF
NONE						R	R
0h						0h	0h
23	22	21	20	19	18	17	16
RESERVED			EFPI				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			EFGI				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		EFFL					
NONE		R					
0h		0h					

Table 14-31078. MCAN_CORE_TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

25	TEFL	R	0h	This bit is a copy of interrupt flag MCAN_IR[15] TEFL. When the MCAN_IR[15] TEFL flag is reset, this bit is also reset.
				Reset Source: hsrst_n
				`0h No Tx Event FIFO element lost`
				`1h Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.`

24	EFF	R	0h	Event FIFO Full
				Reset Source: hsrst_n
				`0h Tx Event FIFO not full`
				`1h Tx Event FIFO full`

23:21	RESERVED	NONE	0h	Reserved
20:16	EFPI	R	0h	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved

Table 14-31078. MCAN_CORE_TXEFS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	EFGI	R	0h	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. Reset Source: hsrst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	EFFL	R	0h	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. Reset Source: hsrst_n

14.9.5.1.2.74 MCAN_CORE_TXEFA Register

1 MCAN_CORE_TXEFA Register (Offset = F8h) [reset = 0h]

Tx event FIFO acknowledge last index of read elements, updates get index and fill level

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Table 14-31079. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F8h**
MCU_MCAN0	**04E0 80F8h**
MCU_MCAN1	**04E1 80F8h**

Figure 14-10297. MCAN_CORE_TXEFA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EFAI</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-31081. MCAN_CORE_TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EFAI	R/W	0h	After the Host CPU has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to the MCAN_TXEFA[4-0] EFAI field. This will set the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field to the MCAN_TXEFA[4-0] EFAI field + 1 and update the Event FIFO Fill Level MCAN_TXEFS[5-0] EFFL field. Reset Source: hsrst_n

14.9.5.1.2.75 MCAN_CORE_RESERVED1616 Register

1 MCAN_CORE_RESERVED1616 Register (Offset = FCh) [reset = 0h]

Reserved Field

Return to Summary Table

Table 14-31082. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10FCh**
MCU_MCAN0	**04E0 80FCh**
MCU_MCAN1	**04E1 80FCh**

Figure 14-10298. MCAN_CORE_RESERVED1616 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31084. MCAN_CORE_RESERVED1616 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.76 MCAN_CORE_RESERVUPPER256_j Register

1 MCAN_CORE_RESERVUPPER256_j Register (Offset = 100h + formula) [reset = 0h]

Reserved Field

Return to Summary Table

Offset = 100h + (j * 4h); where j = 0 to 63d

Table 14-31085. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1100h + formula**
MCU_MCAN0	**04E0 8100h + formula**
MCU_MCAN1	**04E1 8100h + formula**

Figure 14-10299. MCAN_CORE_RESERVUPPER256_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31087. MCAN_CORE_RESERVUPPER256_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.77 MCAN_MSGMEM_RAM_RAM_REG_j Register

1 MCAN_MSGMEM_RAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to Summary Table

Offset = 0h + (j * 4h); where j = 0 to 4351d

Table 14-31088. Instance Table

Instance Name	Physical Address
MCAN0	**2070 8000h + formula**
MCU_MCAN0	**04E0 0000h + formula**
MCU_MCAN1	**04E1 0000h + formula**

Figure 14-10300. MCAN_MSGMEM_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-31090. MCAN_MSGMEM_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.9.5.1.2.78 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

Return to Summary Table

Table 14-31091. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8000h**
MCU_MCAN0	**0470 1000h**
MCU_MCAN1	**0470 2000h**

Figure 14-10301. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-31093. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL Version
10:8	REVMAJ	R	2h	Major Version
7:6	CUSTOM	R	0h	Custom Version
5:0	REVMIN	R	1h	Minor Version

14.9.5.1.2.79 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-31094. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8008h**
MCU_MCAN0	**0470 1008h**
MCU_MCAN1	**0470 2008h**

Figure 14-10302. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31096. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1TS	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

14.9.5.1.2.80 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2h]

Misc Status

Return to Summary Table

Table 14-31097. Instance Table

Instance Name	Physical Address
MCAN0	**2401 800Ch**
MCU_MCAN0	**0470 100Ch**
MCU_MCAN1	**0470 200Ch**

Figure 14-10303. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					2h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
2h							

Table 14-31099. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2h	Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator.

14.9.5.1.2.81 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-31100. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8010h + formula**
MCU_MCAN0	**0470 1010h + formula**
MCU_MCAN1	**0470 2010h + formula**

Figure 14-10304. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-31102. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.5.1.2.82 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-31103. Instance Table

Instance Name	Physical Address
MCAN0	**2401 803Ch**
MCU_MCAN0	**0470 103Ch**
MCU_MCAN1	**0470 203Ch**

Figure 14-10305. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-31105. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Single Error Correction End Of Interrupt (SEC EOI)

14.9.5.1.2.83 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-31106. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8040h**
MCU_MCAN0	**0470 1040h**
MCU_MCAN1	**0470 2040h**

Figure 14-10306. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_PEND	MSGMEM_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31108. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.9.5.1.2.84 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-31109. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8080h**
MCU_MCAN0	**0470 1080h**
MCU_MCAN1	**0470 2080h**

Figure 14-10307. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_SET	MSGMEM_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31111. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.9.5.1.2.85 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-31112. Instance Table

Instance Name	Physical Address
MCAN0	**2401 80C0h**
MCU_MCAN0	**0470 10C0h**
MCU_MCAN1	**0470 20C0h**

Figure 14-10308. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-31114. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.9.5.1.2.86 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-31115. Instance Table

Instance Name	Physical Address
MCAN0	**2401 813Ch**
MCU_MCAN0	**0470 113Ch**
MCU_MCAN1	**0470 213Ch**

Figure 14-10309. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-31117. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Double Error Correction End Of Interrupt (DED EOI)

14.9.5.1.2.87 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-31118. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8140h**
MCU_MCAN0	**0470 1140h**
MCU_MCAN1	**0470 2140h**

Figure 14-10310. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_PEND	MSGMEM_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31120. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.9.5.1.2.88 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-31121. Instance Table

Instance Name	**Physical Address**
MCAN0	**2401 8180h**
MCU_MCAN0	**0470 1180h**
MCU_MCAN1	**0470 2180h**

Figure 14-10311. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_SET	MSGMEM_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31123. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.9.5.1.2.89 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-31124. Instance Table

Instance Name	Physical Address
MCAN0	**2401 81C0h**
MCU_MCAN0	**0470 11C0h**
MCU_MCAN1	**0470 21C0h**

Figure 14-10312. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-31126. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.9.5.1.2.90 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-31127. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8200h**
MCU_MCAN0	**0470 1200h**
MCU_MCAN1	**0470 2200h**

Figure 14-10313. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31129. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt Enable Set for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TS	0h	Interrupt Enable Set for Parity Errors

14.9.5.1.2.91 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-31130. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8204h**
MCU_MCAN0	**0470 1204h**
MCU_MCAN1	**0470 2204h**

Figure 14-10314. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-31132. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt Enable Clear for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TC	0h	Interrupt Enable Clear for Parity Errors

14.9.5.1.2.92 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-31133. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8208h**
MCU_MCAN0	**0470 1208h**
MCU_MCAN1	**0470 2208h**

Figure 14-10315. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-31135. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt Status Set for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WI	0h	Interrupt Status Set for Parity Errors

14.9.5.1.2.93 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-31136. Instance Table

Instance Name	Physical Address
MCAN0	**2401 820Ch**
MCU_MCAN0	**0470 120Ch**
MCU_MCAN1	**0470 220Ch**

Figure 14-10316. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-31138. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt Status Clear for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WD	0h	Interrupt Status Clear for Parity Errors

14.9.5.2 ECAP

ECAP

14.9.5.2.1 ECAP Summaries

ECAP Summaries

Table 14-31139. ECAP Registers, Base Address=2310 0000h, Length=256

Offset	Length	Register Name	ECAP0 Physical Address	ECAP1 Physical Address	ECAP2 Physical Address
0h	32	ECAP_TSCNT	2310 0000h	2311 0000h	2312 0000h
4h	32	ECAP_CNTPHS	2310 0004h	2311 0004h	2312 0004h
8h	32	ECAP_CAP1	2310 0008h	2311 0008h	2312 0008h
Ch	32	ECAP_CAP2	2310 000Ch	2311 000Ch	2312 000Ch
10h	32	ECAP_CAP3	2310 0010h	2311 0010h	2312 0010h
14h	32	ECAP_CAP4	2310 0014h	2311 0014h	2312 0014h
28h	32	ECAP_ECCTL	2310 0028h	2311 0028h	2312 0028h
2Ch	32	ECAP_ECINT_EN_FLG	2310 002Ch	2311 002Ch	2312 002Ch
30h	32	ECAP_ECINT_CLR_FRC	2310 0030h	2311 0030h	2312 0030h
5Ch	32	ECAP_PID	2310 005Ch	2311 005Ch	2312 005Ch

14.9.5.2.2 ECAP Registers

ECAP Registers

14.9.5.2.2.1 ECAP_TSCNT Register

1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

Time Stamp Counter Register

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Table 14-31140. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0000h**
ECAP1	**2311 0000h**
ECAP2	**2312 0000h**

Figure 14-10317. ECAP_TSCNT Name Register

31	30	29	28	27	26	25	24
TSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
TSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
TSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
TSCNT							
R/W							
0h							

Table 14-31142. ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCNT	R/W	0h	Active 32 bit Counter register which is used as the Capture time-base Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.2 ECAP_CNTPHS Register

1 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

Counter Phase Control Register

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Table 14-31143. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0004h**
ECAP1	**2311 0004h**
ECAP2	**2312 0004h**

Figure 14-10318. ECAP_CNTPHS Name Register

31	30	29	28	27	26	25	24
CNTPHS							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTPHS							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTPHS							
R/W							
0h							

Table 14-31145. ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase Lag/Lead. This register shadows the ECAP_TSCNT register and is loaded into the ECAP_TSCNT register upon either a SYNCI event or software force via a control bit. Used to achieve phase control sync with respect to other ECAP and EPWM time-bases. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.3 ECAP_CAP1 Register

1 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

Capture-1 Register

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Table 14-31146. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0008h**
ECAP1	**2311 0008h**
ECAP2	**2312 0008h**

Figure 14-10319. ECAP_CAP1 Name Register

31	30	29	28	27	26	25	24
CAP1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP1							
R/W							
0h							

Table 14-31148. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes/initialisation. 3. APRD shadow register (ECAP_CAP3) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.4 ECAP_CAP2 Register

1 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

Capture-2 Register

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Table 14-31149. Instance Table

Instance Name	Physical Address
ECAP0	**2310 000Ch**
ECAP1	**2311 000Ch**
ECAP2	**2312 000Ch**

Figure 14-10320. ECAP_CAP2 Name Register

31	30	29	28	27	26	25	24
CAP2							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP2							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP2							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP2							
R/W							
0h							

Table 14-31151. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes. 3. ACMP shadow register (ECAP_CAP4) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.5 ECAP_CAP3 Register

1 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

Capture-3 Register

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Table 14-31152. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0010h**
ECAP1	**2311 0010h**
ECAP2	**2312 0010h**

Figure 14-10321. ECAP_CAP3 Name Register

31	30	29	28	27	26	25	24
CAP3							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP3							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP3							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP3							
R/W							
0h							

Table 14-31154. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.6 ECAP_CAP4 Register

1 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

Capture-4 Register

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Table 14-31155. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0014h**
ECAP1	**2311 0014h**
ECAP2	**2312 0014h**

Figure 14-10322. ECAP_CAP4 Name Register

31	30	29	28	27	26	25	24
CAP4							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP4							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP4							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP4							
R/W							
0h							

Table 14-31157. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the compare shadow (ACMP) register. User updates the PWM Compare value via this register. In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.2.2.7 ECAP_ECCTL Register

1 ECAP_ECCTL Register (Offset = 28h) [reset = 60000h]

ECAP Control Register

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Table 14-31158. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0028h**
ECAP1	**2311 0028h**
ECAP2	**2312 0028h**

Figure 14-10323. ECAP_ECCTL Name Register

31	30	29	28	27	26	25	24
FILTER					APWMPOL	CAP_APWM	SWSYNC
R					R/W	R/W	WTC
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARM_RESET	STOPVALUE		CONT_ONESHT
R/W		R/W	R/W	WTC	R/W		R/W
0h		0h	0h	0h	3h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FREE_SOFT		EVTFLTPS					CAPLDEN
R/W		R/W					R/W
0h		0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31160. ECAP_ECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	FILTER	R	0h	Reset Source: vbus_rst_mod_g_rst_n

26	APWMPOL	R/W	0h	APWM Output Polarity Select:
				Note: This is applicable only in APWM operating mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h Output is Active High (Compare value defines High time)`
				`1h Output is Active Low (Compare value defines Low time)`

Table 14-31160. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CAP_APWM	R/W	0h	CAP/APWM Operating Mode Select: Reset Source: vbus_rst_mod_g_rst_n 0h ECAP module operates in Capture mode. This mode forces the following configuration: 1. Inhibits the ECAP_TSCNT register resets via PRD event. 2. Inhibits the Shadow loads on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Permits user to enable the ECAP_CAP1 to ECAP_CAP4 register load. 4. CAPx/APWMx pin operates as a Capture input. 1h ECAP module operates in APWM mode. This mode forces the following configuration: 1. Resets the ECAP_TSCNT register on PRD event (period boundary) 2. Permits Shadow loading on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Disables loading of Time-stamps into the ECAP_CAP1 - ECAP_CAP4 registers 4. CAPx/APWMx pin operates as a APWM output.
24	SWSYNC	WTC	0h	Software Forced Counter (ECAP_TSCNT) Synchronizing: Reset Source: vbus_rst_mod_g_rst_n 0h Writing a zero has no effect. Reading will always return a zero. 1h Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0h
23:22	SYNCO_SEL	R/W	0h	SyncOut Select: Note: Selection PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if user believes it to be useful. Reset Source: vbus_rst_mod_g_rst_n 0h Select SyncIn event to be the SyncOut signal (pass through) 1h Select PRD event to be the SyncOut signal 2h Disable SyncOut Signal 3h Disable SyncOut Signal
21	SYNCI_EN	R/W	0h	Counter (ECAP_TSCNT) SyncIn select mode: Reset Source: vbus_rst_mod_g_rst_n 0h Disable SyncIn option 1h Enable Counter (ECAP_TSCNT) to be loaded from the ECAP_CNTPHS register upon either a SYNCI signal or a software force event.
20	TSCNTSTP	R/W	0h	Counter Stop (freeze) Control: Reset Source: vbus_rst_mod_g_rst_n 0h Counter Stopped 1h Counter Free Running
19	REARM_RESET	WTC	0h	One-Shot Re-arming Control Wait for stop trigger: Reset Source: vbus_rst_mod_g_rst_n 0h Has no effect. Reading always returns a 0h 1h Arms the One-Shot sequence: 1. Resets the Mod4 counter to zero. 2. Un-freezes the Mod4 counter. 3. Enables Capture Register Loads.

Table 14-31160. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:17	STOPVALUE	R/W	3h	Stop Value for One-Shot Mode: This is the number (between 1 and 4) of captures allowed to occur before the ECAP_CAP1 through ECAP_CAP4 registers are frozen (capture sequence is stopped). Notes: [1] STOPVALUE is compared to Mod4 counter, when equal, two actions occur: 1. Mod4 Counter is stopped (frozen) 2. Capture register loads are inhibited [2] In one shot mode, further interrupt events are blocked until we re-arm, once the number of events captured has been reached. Reset Source: vbus_rst_mod_g_rst_n 0h Stop after Capture Event 1 1h Stop after Capture Event 2 2h Stop after Capture Event 3 3h Stop after Capture Event 4
16	CONT_ONESHT	R/W	0h	Continuous or One-shot Mode Control (applicable only in Capture mode): Reset Source: vbus_rst_mod_g_rst_n 0h Operate in Continuous mode 1h Operate in One-Shot mode
15:14	FREE_SOFT	R/W	0h	Emulation Control Reset Source: vbus_rst_mod_g_rst_n 0h ECAP_TSCNT Counter stops immediately on emulation suspend 1h ECAP_TSCNT Counter runs until = 0h 3h ECAP_TSCNT Counter is unaffected by emulation suspend (Run Free)
13:9	EVTFLTPS	R/W	0h	Event Filter Prescale Select: Reset Source: vbus_rst_mod_g_rst_n 0h Divide by 1 (no prescale, by-pass the prescaler) 1Eh Divide by 60 1Fh Divide by 62 1h Divide by 2 2h Divide by 4 3h Divide by 6 4h Divide by 8 5h Divide by 10
8	CAPLDEN	R/W	0h	Enable Loading of the ECAP_CAP1 to ECAP_CAP4 registers on a capture event: Reset Source: vbus_rst_mod_g_rst_n 0h Disable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time. 1h Enable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4: Reset Source: vbus_rst_mod_g_rst_n 0h Do Not reset Counter on Capture Event 4 (absolute time stamp) 1h Reset counter after Event 4 time-stamp has been captured (used in Difference mode operation)

Table 14-31160. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CAP4POL	R/W	0h	Capture Event 4 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 4 triggered on a Rising Edge (RE) 1h Capture event 4 triggered on a Falling Edge (FE)
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 3 (absolute time stamp) 1h Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 3 triggered on a Rising Edge (RE) 1h Capture event 3 triggered on a Falling Edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 2 (absolute time stamp) 1h Reset Counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 2 triggered on a Rising Edge (RE) 1h Capture event 2 triggered on a Falling Edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 1 (absolute time stamp) 1h Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 1 triggered on a Rising Edge (RE) 1h Capture event 1 triggered on a Falling Edge (FE)

14.9.5.2.2.8 ECAP_ECINT_EN_FLG Register

1 ECAP_ECINT_EN_FLG Register (Offset = 2Ch) [reset = 0h]

ECAP Interrupt Enable and Flag Register

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Table 14-31161. Instance Table

Instance Name	Physical Address
ECAP0	**2310 002Ch**
ECAP1	**2311 002Ch**
ECAP2	**2312 002Ch**

Figure 14-10324. ECAP_ECINT_EN_FLG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FLG	PRDEQ_FLG	CNTOVF_FLG	CEVT4_FLG	CEVT3_FLG	CEVT2_FLG	CEVT1_FLG	INT_FLG
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_EN	PRDEQ_EN	CNTOVF_EN	CEVT4_EN	CEVT3_EN	CEVT2_EN	CEVT1_EN	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31163. ECAP_ECINT_EN_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	CMPEQ_FLG	R	0h	Compare Equal Status Flag: Note: This flag is only active in APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred 1h Indicates the counter (ECAP_TSCNT) reached the Compare register value (ACMP)
22	PRDEQ_FLG	R	0h	Period Equal Status Flag: Note: This flag is only active in APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred 1h Indicates the Counter (ECAP_TSCNT) reached the Period register value (APER) and was reset.

Table 14-31163. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CNTOVF_FLG	R	0h	Counter Overflow Status Flag: Note: This flag is active in CAP and APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the Counter (ECAP_TSCNT) has made the transition from FFFF FFFFh to 0000 0000h
20	CEVT4_FLG	R	0h	Capture Event 4 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the fourth event occurred at ECAPx pin.
19	CEVT3_FLG	R	0h	Capture Event 3 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the third event occurred at ECAPx pin.
18	CEVT2_FLG	R	0h	Capture Event 2 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the second event occurred at ECAPx pin.
17	CEVT1_FLG	R	0h	Capture Event 1 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the first event occurred at ECAPx pin.
16	INT_FLG	R	0h	Global Interrupt Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no interrupt generated. 1h Indicates that an interrupt was generated from one of the following events.
15:8	RESERVED	NONE	0h	Reserved
7	CMPEQ_EN	R/W	0h	Compare Equal Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Compare Equal as an Interrupt source 1h Enable Compare Equal as an Interrupt source
6	PRDEQ_EN	R/W	0h	Period Equal Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Period Equal as an Interrupt source 1h Enable Period Equal as an Interrupt source
5	CNTOVF_EN	R/W	0h	Counter Overflow Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Counter Overflow as an Interrupt source 1h Enable Counter Overflow as an Interrupt source

Table 14-31163. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CEVT4_EN	R/W	0h	Capture Event 4 Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Capture Event 4 as an Interrupt source: 1h Enable Capture Event 4 as an Interrupt source
3	CEVT3_EN	R/W	0h	Capture Event 3 Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Capture Event 3 as an Interrupt source: 1h Enable Capture Event 3 as an Interrupt source
2	CEVT2_EN	R/W	0h	Capture Event 2 Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Capture Event 2 as an Interrupt source: 1h Enable Capture Event 2 as an Interrupt source
1	CEVT1_EN	R/W	0h	Capture Event 1 Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Capture Event 1 as an Interrupt source: 1h Enable Capture Event 1 as an Interrupt source
0	RESERVED	NONE	0h	Reserved

14.9.5.2.2.9 ECAP_ECINT_CLR_FRC Register

1 ECAP_ECINT_CLR_FRC Register (Offset = 30h) [reset = 0h]

ECAP Interrupt Clear and Forcing Register

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Table 14-31164. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0030h**
ECAP1	**2311 0030h**
ECAP2	**2312 0030h**

Figure 14-10325. ECAP_ECINT_CLR_FRC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FRC	PRDEQ_FRC	CNTOVF_FRC	CEVT4_FRC	CEVT3_FRC	CEVT2_FRC	CEVT1_FRC	RESERVED
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	NONE
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_CLR	PRDEQ_CLR	CNTOVF_CLR	CEVT4_CLR	CEVT3_CLR	CEVT2_CLR	CEVT1_CLR	INT_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31166. ECAP_ECINT_CLR_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23	CMPEQ_FRC	W1TS	0h	Force Compare Equal:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0h`
				`1h Writing a 1h to this bit will set the CMPEQ_FLG flag bit.`

22	PRDEQ_FRC	W1TS	0h	Force Period Equal:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0.`
				`1h Writing a 1h to this bit will set the PRDEQ_FLG flag bit.`

21	CNTOVF_FRC	W1TS	0h	Force Counter Overflow:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0.`
				`1h Writing a 1h to this bit will set the CNTOVF_FLG flag bit.`

Table 14-31166. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CEVT4_FRC	W1TS	0h	Force Capture Event 4: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT4_FLG flag bit.
19	CEVT3_FRC	W1TS	0h	Force Capture Event 3: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT3_FLG flag bit.
18	CEVT2_FRC	W1TS	0h	Force Capture Event 2: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT2_FLG flag bit.
17	CEVT1_FRC	W1TS	0h	Force Capture Event 1: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT1_FLG flag bit.
16:8	RESERVED	NONE	0h	Reserved
7	CMPEQ_CLR	W1TC	0h	Compare Equal Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CMPEQ_FLG flag condition.
6	PRDEQ_CLR	W1TC	0h	Period Equal Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the PRDEQ_FLG flag condition.
5	CNTOVF_CLR	W1TC	0h	Counter Overflow Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CNTOVF_FLG flag condition.
4	CEVT4_CLR	W1TC	0h	Capture Event 4 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT4_FLG flag condition.
3	CEVT3_CLR	W1TC	0h	Capture Event 3 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT3_FLG flag condition.
2	CEVT2_CLR	W1TC	0h	Capture Event 2 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT2_FLG flag condition.

Table 14-31166. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1_CLR	W1TC	0h	Capture Event 1 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT1_FLG flag condition.
0	INT_CLR	W1TC	0h	Global Interrupt Clear Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the INT_FLG flag and enable further interrupts to be generated if any of the event flags are set to 1h.

14.9.5.2.2.10 ECAP_PID Register

1 ECAP_PID Register (Offset = 5Ch) [reset = 44D24100h]

Peripheral ID Register

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Table 14-31167. Instance Table

Instance Name	Physical Address
ECAP0	**2310 005Ch**
ECAP1	**2311 005Ch**
ECAP2	**2312 005Ch**

Figure 14-10326. ECAP_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNCTION			
R		R		R			
1h		0h		4D2h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
4D2h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
8h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-31169. ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Reset Source: vbus_rst_mod_g_rst_n
29:28	RESERVED	R	0h	
27:16	FUNCTION	R	4D2h	Reset Source: vbus_rst_mod_g_rst_n
15:11	RTL	R	8h	Reset Source: vbus_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Reset Source: vbus_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Reset Source: vbus_rst_mod_g_rst_n
5:0	MINOR	R	0h	Reset Source: vbus_rst_mod_g_rst_n

14.9.5.3 EPWM

EPWM

14.9.5.3.1 EPWM Summaries

EPWM Summaries

Table 14-31170. EPWM Registers, Base Address=2300 0000h, Length=256

Offset	Length	Register Name	EPWM0 Physical Address	EPWM1 Physical Address	EPWM2 Physical Address
0h	16	EPWM_TBCTL	2300 0000h	2301 0000h	2302 0000h
2h	16	EPWM_TBSTS	2300 0002h	2301 0002h	2302 0002h
4h	16	EPWM_TBPHSHR	2300 0004h	2301 0004h	2302 0004h
6h	16	EPWM_TBPHS	2300 0006h	2301 0006h	2302 0006h
8h	16	EPWM_TBCNT	2300 0008h	2301 0008h	2302 0008h
Ah	16	EPWM_TBPRD	2300 000Ah	2301 000Ah	2302 000Ah
Eh	16	EPWM_CMPCTL	2300 000Eh	2301 000Eh	2302 000Eh
10h	16	EPWM_CMPAHR	2300 0010h	2301 0010h	2302 0010h
12h	16	EPWM_CMPA	2300 0012h	2301 0012h	2302 0012h
14h	16	EPWM_CMPB	2300 0014h	2301 0014h	2302 0014h
16h	16	EPWM_AQCTLA	2300 0016h	2301 0016h	2302 0016h
18h	16	EPWM_AQCTLB	2300 0018h	2301 0018h	2302 0018h
1Ah	16	EPWM_AQSFRC	2300 001Ah	2301 001Ah	2302 001Ah
1Ch	16	EPWM_AQCSFRC	2300 001Ch	2301 001Ch	2302 001Ch
1Eh	16	EPWM_DBCTL	2300 001Eh	2301 001Eh	2302 001Eh
20h	16	EPWM_DBRED	2300 0020h	2301 0020h	2302 0020h
22h	16	EPWM_DBFED	2300 0022h	2301 0022h	2302 0022h
24h	16	EPWM_TZSEL	2300 0024h	2301 0024h	2302 0024h
28h	16	EPWM_TZCTL	2300 0028h	2301 0028h	2302 0028h
2Ah	16	EPWM_TZEINT	2300 002Ah	2301 002Ah	2302 002Ah
2Ch	16	EPWM_TZFLG	2300 002Ch	2301 002Ch	2302 002Ch
2Eh	16	EPWM_TZCLR	2300 002Eh	2301 002Eh	2302 002Eh
30h	16	EPWM_TZFRC	2300 0030h	2301 0030h	2302 0030h
32h	16	EPWM_ETSEL	2300 0032h	2301 0032h	2302 0032h
34h	16	EPWM_ETPS	2300 0034h	2301 0034h	2302 0034h
36h	16	EPWM_ETFLG	2300 0036h	2301 0036h	2302 0036h
38h	16	EPWM_ETCLR	2300 0038h	2301 0038h	2302 0038h
3Ah	16	EPWM_ETFRC	2300 003Ah	2301 003Ah	2302 003Ah
3Ch	16	EPWM_PCCTL	2300 003Ch	2301 003Ch	2302 003Ch
5Ch	32	EPWM_PID	2300 005Ch	2301 005Ch	2302 005Ch

14.9.5.3.2 EPWM Registers

EPWM Registers

14.9.5.3.2.1 EPWM_TBCTL Register

1 EPWM_TBCTL Register (Offset = 0h) [reset = 83h]

Time-Base Control Register

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Table 14-31171. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0000h**
EPWM1	**2301 0000h**
EPWM2	**2302 0000h**

Figure 14-10327. EPWM_TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W		R/W	R/W			R/W	
0h		0h	0h			1h	
7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W	R/W	R/W		R/W	R/W	R/W	
1h	0h	0h		0h	0h	3h	

Table 14-31173. EPWM_TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Mode Bits These bits select the behavior of the ePWM time-base counter during emulation events: 0h Stop after the next time-base counter increment or decrement 1h Stop when counter completes a whole cycle (a) Up-count mode: stop when the time-base counter = period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD). (b) Down-count mode: stop when the time-base counter = 0000 (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h Free run 3h Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode The PHSDIR bit indicates the direction the time-base counter [TBCNT] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register This is irrespective of the direction of the counter before the synchronization event In the up-count and down-count modes this bit is ignored 0h Count down after the synchronization event 1h Count up after the synchronization event
12:10	CLKDIV	R/W	0h	Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] 0h /1 (default on reset) 1h /2 2h /4 3h /8 4h /16 5h /32 6h /64 7h /128

Table 14-31173. EPWM_TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:7	HSPCLKDIV	R/W	1h	High-Speed Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral 0h /1 1h /2 (default on reset) 2h /4 3h /6 4h /8 5h /10 6h /12 7h /14
6	SWFSYNC	R/W	0h	Software Forced Synchronization Pulse 0h Writing a 0h 1h Writing a 1h
5:4	SYNCOSEL	R/W	0h	Synchronization Output Select These bits select the source of the EPWMxSYNCO signal 0h EPWMxSYNC 1h TBCNT = 0: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h TBCNT = CMPB: Time-base counter equal to counter-compare B (EPWM_TBCNT[15-0] TBCNT = EPWM_CMPB[15-0] CMPB) 3h Disable EPWMxSYNCO signal
3	PRDLD	R/W	0h	Active Period Register Load From Shadow Register Select 0h The period register (EPWM_TBPRD) is loaded from its shadow register when the time-base counter, EPWM_TBCNT[15-0] TBCNT, is equal to zero. A write or read to the EPWM_TBPRD register accesses the shadow register. 1h Load the EPWM_TBPRD register immediately without using a shadow register. A write or read to the EPWM_TBPRD register directly accesses the active register.
2	PHSEN	R/W	0h	Counter Register Load From Phase Register Enable 0h Do not load the time-base counter (EPWM_TBCNT) from the time-base phase register (EPWM_TBPHS) 1h Load the time-base counter with the phase register when an EPWMxSYNCI input signal occurs or when a software synchronization is forced by the SWFSYNC bit.
1:0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change These bits set the time-base counter mode of operation as follows: 0h Up-count mode 1h Down-count mode 2h Up-down-count mode 3h Stop-freeze counter operation (default on reset)

14.9.5.3.2.2 EPWM_TBSTS Register

1 EPWM_TBSTS Register (Offset = 2h) [reset = 0h]

Time-Base Status Register

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Table 14-31174. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0002h**
EPWM1	**2301 0002h**
EPWM2	**2302 0002h**

Figure 14-10328. EPWM_TBSTS Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1					CTRMAX	SYNCI	CTRDIR
R					R/W1TC	R/W1TC	R
0h					0h	0h	0h

Table 14-31176. EPWM_TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	CTRMAX	R/W1TC	0h	Time-Base Counter Max Latched Status Bit 0h Reading a 0h 1h Reading a 1h
1	SYNCI	R/W1TC	0h	Input Synchronization Latched Status Bit 0h Writing a 0h 1h Reading a 1h
0	CTRDIR	R	0h	Time-Base Counter Direction Status Bit At reset, the counter is frozen, therefore, this bit has no meaning To make this bit meaningful, you must first set the appropriate mode via TBCTL[CTRMODE] 0h Time-Base Counter is currently counting down 1h Time-Base Counter is currently counting up

14.9.5.3.2.3 EPWM_TBPHSHR Register

1 EPWM_TBPHSHR Register (Offset = 4h) [reset = 0h]

Time Base Phase High Resolution Register

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Table 14-31177. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0004h**
EPWM1	**2301 0004h**
EPWM2	**2302 0004h**

Figure 14-10329. EPWM_TBPHSHR Name Register

15	14	13	12	11	10	9	8
TBPHSH							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							
R							
0h							

Table 14-31179. EPWM_TBPHSHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TBPHSH	R/W	0h	Time-base phase high-resolution bits
7:0	RESERVED1	R	0h	Reserved

14.9.5.3.2.4 EPWM_TBPHS Register

1 EPWM_TBPHS Register (Offset = 6h) [reset = 0h]

Time Base Phase Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension, otherwise, this location is reserved.

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Table 14-31180. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0006h**
EPWM1	**2301 0006h**
EPWM2	**2302 0006h**

Figure 14-10330. EPWM_TBPHS Name Register

15	14	13	12	11	10	9	8
TBPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
TBPHS							
R/W							
0h							

Table 14-31182. EPWM_TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPHS	R/W	0h	These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal [a] If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase [b] If TBCTL[PHSEN] = 1, then the time-base counter [TBCNT] will be loaded with the phase [TBPHS] when a synchronization event occurs The synchronization event can be initiated by the input synchronization signal [EPWMxSYNCI] or by a software forced synchronization

14.9.5.3.2.5 EPWM_TBCNT Register

1 EPWM_TBCNT Register (Offset = 8h) [reset = 0h]

Time Base Counter Register

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Table 14-31183. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0008h**
EPWM1	**2301 0008h**
EPWM2	**2302 0008h**

Figure 14-10331. EPWM_TBCNT Name Register

15	14	13	12	11	10	9	8
TBCNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBCNT							
R/W							
0h							

Table 14-31185. EPWM_TBCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBCNT	R/W	0h	Reading these bits gives the current time-base counter value Writing to these bits sets the current time-base counter value The update happens as soon as the write occurs The write is NOT synchronized to the time-base clock [TBCLK] and the register is not shadowed

14.9.5.3.2.6 EPWM_TBPRD Register

1 EPWM_TBPRD Register (Offset = Ah) [reset = 0h]

Time Base Period Register

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Table 14-31186. Instance Table

Instance Name	Physical Address
EPWM0	**2300 000Ah**
EPWM1	**2301 000Ah**
EPWM2	**2302 000Ah**

Figure 14-10332. EPWM_TBPRD Name Register

15	14	13	12	11	10	9	8
TBPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPRD							
R/W							
0h							

Table 14-31188. EPWM_TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPRD	R/W	0h	These bits determine the period of the time-base counter This sets the PWM frequency Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit By default this register is shadowed [a] If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the active register will be loaded from the shadow register when the time-base counter equals zero [b] If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [c] The active and shadow registers share the same memory map address

14.9.5.3.2.7 EPWM_CMPCTL Register

1 EPWM_CMPCTL Register (Offset = Eh) [reset = 0h]

Counter Compare Control Register

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Table 14-31189. Instance Table

Instance Name	Physical Address
EPWM0	**2300 000Eh**
EPWM1	**2301 000Eh**
EPWM2	**2302 000Eh**

Figure 14-10333. EPWM_CMPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1						SHDWBFULL	SHDWAFULL
R						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED2	SHDWBMODE	RESERVED3	SHDWAMODE	LOADBMODE		LOADAMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Table 14-31191. EPWM_CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9	SHDWBFULL	R	0h	Counter-compare B [CMPB] Shadow Register Full Status Flag This bit self clears once a load-strobe occurs 0h CMPB shadow FIFO not full yet 1h Indicates the CMPB shadow FIFO is full. A CPU write will overwrite current shadow value.
8	SHDWAFULL	R	0h	Counter-compare A [CMPA] Shadow Register Full Status Flag The flag bit is set when a 32 bit write to CMPA:CMPAHR register or a 16 bit write to CMPA register is made A 16 bit write to CMPAHR register will not affect the flag This bit self clears once a load-strobe occurs 0h CMPA shadow FIFO not full yet 1h Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value
7	RESERVED2	R	0h	Reserved
6	SHDWBMODE	R/W	0h	Counter-compare B [CMPB] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action.
5	RESERVED3	R	0h	Reserved

Table 14-31191. EPWM_CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SHDWAMODE	R/W	0h	Counter-compare A [CMPA] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action.
3:2	LOADBMODE	R/W	0h	Active Counter-Compare B [CMPB] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1] 0h Load on EPWM_TBCNT[15-0] TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT= 0000h) 1h Load on EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0 or EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD 3h Freeze (no loads possible)
1:0	LOADAMODE	R/W	0h	Active Counter-Compare A [CMPA] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1] 0h Load on TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 1h Load on TBCNT = TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT= EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0h 3h Freeze (no loads possible)

14.9.5.3.2.8 EPWM_CMPAHR Register

1 EPWM_CMPAHR Register (Offset = 10h) [reset = 0h]

Counter Compare A High Resolution Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, this location is reserved.

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Table 14-31192. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0010h**
EPWM1	**2301 0010h**
EPWM2	**2302 0010h**

Figure 14-10334. EPWM_CMPAHR Name Register

15	14	13	12	11	10	9	8
CMPAHR							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED1							
R							
0h							

Table 14-31194. EPWM_CMPAHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CMPAHR	R/W	0h	Compare A High-Resolution register bits for MEP step control A minimum value of 1h is needed to enable HRPWM capabilities Valid MEP range of operation 1-255h
7:0	RESERVED1	R	0h	Reserved

14.9.5.3.2.9 EPWM_CMPA Register

1 EPWM_CMPA Register (Offset = 12h) [reset = 0h]

Counter Compare A Register

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Table 14-31195. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0012h**
EPWM1	**2301 0012h**
EPWM2	**2302 0012h**

Figure 14-10335. EPWM_CMPA Name Register

15	14	13	12	11	10	9	8
CMPA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPA							
R/W							
0h							

Table 14-31197. EPWM_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPA	R/W	0h	The value in the active CMPA register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register [b] Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.9.5.3.2.10 EPWM_CMPB Register

1 EPWM_CMPB Register (Offset = 14h) [reset = 0h]

Counter Compare B Register

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Table 14-31198. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0014h**
EPWM1	**2301 0014h**
EPWM2	**2302 0014h**

Figure 14-10336. EPWM_CMPB Name Register

15	14	13	12	11	10	9	8
CMPB							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPB							
R/W							
0h							

Table 14-31200. EPWM_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPB	R/W	0h	The value in the active CMPB register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing, the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register: [b] Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.9.5.3.2.11 EPWM_AQCTLA Register

1 EPWM_AQCTLA Register (Offset = 16h) [reset = 0h]

Action Qualifier Control Register For Output A

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Table 14-31201. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0016h**
EPWM1	**2301 0016h**
EPWM2	**2302 0016h**

Figure 14-10337. EPWM_AQCTLA Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-31203. EPWM_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved
11:10	CBD	R/W	0h	Action when the time-base counter equals the active CMPB register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low

Table 14-31203. EPWM_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low

14.9.5.3.2.12 EPWM_AQCTLB Register

1 EPWM_AQCTLB Register (Offset = 18h) [reset = 0h]

Action Qualifier Control Register For Output B

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Table 14-31204. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0018h**
EPWM1	**2301 0018h**
EPWM2	**2302 0018h**

Figure 14-10338. EPWM_AQCTLB Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-31206. EPWM_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved

11:10	CBD	R/W	0h	Action when the counter equals the active CMPB register and the counter is decrementing
				`0h Do nothing (action disabled)`
				`1h Clear: force EPWMxB output low`
				`2h Set: force EPWMxB output high`
				`3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low`

9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing
				`0h Do nothing (action disabled)`
				`1h Clear: force EPWMxB output low`
				`2h Set: force EPWMxB output high`
				`3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low`

7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing
				`0h Do nothing (action disabled)`
				`1h Clear: force EPWMxB output low`
				`2h Set: force EPWMxB output high`
				`3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low`

Table 14-31206. EPWM_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low

14.9.5.3.2.13 EPWM_AQSFRC Register

1 EPWM_AQSFRC Register (Offset = 1Ah) [reset = 0h]

Action Qualifier Software Force Register

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Table 14-31207. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Ah**
EPWM1	**2301 001Ah**
EPWM2	**2302 001Ah**

Figure 14-10339. EPWM_AQSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W		R/W1TC	R/W		R/W1TC	R/W	
0h		0h	0h		0h	0h	

Table 14-31209. EPWM_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED1	R	0h	Reserved
7:6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options
5	OTSFB	R/W1TC	0h	One-Time Software Forced Event on Output B 0h Writing a 0h (1h Initiates a single s/w forced event
4:3	ACTSFB	R/W	0h	Action when One-Time Software Force B Is invoked 0h Does nothing (action disabled) 1h Clear (low) 2h Set (high) 3h Toggle (Low -> High, High -> Low).
2	OTSFA	R/W1TC	0h	One-Time Software Forced Event on Output A 0h Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (that is, a forced event is initiated). 1h Initiates a single software forced event.
1:0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 0h Does nothing (action disabled). 1h Clear (low). 2h Set (high). 3h Toggle (Low -> High, High -> Low).

14.9.5.3.2.14 EPWM_AQCSFRC Register

1 EPWM_AQCSFRC Register (Offset = 1Ch) [reset = 0h]

Action Qualifier Continuous S/W Force Register

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Table 14-31210. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Ch**
EPWM1	**2301 001Ch**
EPWM2	**2302 001Ch**

Figure 14-10340. EPWM_AQCSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1				CSFB		CSFA	
R				R/W		R/W	
0h				0h		0h	

Table 14-31212. EPWM_AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved

3:2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register To configure shadow mode, use AQSFRC[RLDCSF]
				`0h Forcing disabled, that is, has no effect`
				`1h Forces a continuous low on output B`
				`2h Forces a continuous high on output B`
				`3h Software forcing is disabled and has no effect`

1:0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register
				`0h Forcing disabled, that is, has no effect`
				`1h Forces a continuous low on output A`
				`2h Forces a continuous high on output A`
				`3h Software forcing is disabled and has no effect`

14.9.5.3.2.15 EPWM_DBCTL Register

1 EPWM_DBCTL Register (Offset = 1Eh) [reset = 0h]

Dead-Band Generator Control Register

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Table 14-31213. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Eh**
EPWM1	**2301 001Eh**
EPWM2	**2302 001Eh**

Figure 14-10341. EPWM_DBCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1		IN_MODE		POLSEL		OUT_MODE	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-31215. EPWM_DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED1	R	0h	Reserved
5:4	IN_MODE	R/W	0h	Dead Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch This allows you to select the input source to the falling-edge and rising-edge delay To produce classical dead-band waveforms, the default is EPWMxA In is the source for both falling and rising-edge delays 0h `EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.` 1h `EPWMxB In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.` 2h `EPWMxA In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.` 3h `EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.`

Table 14-31215. EPWM_DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0,0 Other enhanced modes are also possible, but not regarded as typical usage modes 0h Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default). 1h Active low complementary (ALC) mode. EPWMxA is inverted. 2h Active high complementary (AHC). EPWMxB is inverted. 3h Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.
1:0	OUT_MODE	R/W	0h	Dead-band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay 0h Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect. 1h Disable rising-edge delay. The EPWMxA signal from the action- qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field. 2h Disable falling-edge delay. The EPWMxB signal from the action- qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule. The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field. 3h Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.

14.9.5.3.2.16 EPWM_DBRED Register

1 EPWM_DBRED Register (Offset = 20h) [reset = 0h]

Dead-Band Generator Rising Edge Delay Count Register

Return to Summary Table

Table 14-31216. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0020h**
EPWM1	**2301 0020h**
EPWM2	**2302 0020h**

Figure 14-10342. EPWM_DBRED Name Register

15	14	13	12	11	10	9	8
RESERVED1						DEL	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
DEL							
R/W							
0h							

Table 14-31218. EPWM_DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Rising Edge Delay Count 10 bit counter

14.9.5.3.2.17 EPWM_DBFED Register

1 EPWM_DBFED Register (Offset = 22h) [reset = 0h]

Dead-Band Generator Falling Edge Delay Count Register

Return to Summary Table

Table 14-31219. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0022h**
EPWM1	**2301 0022h**
EPWM2	**2302 0022h**

Figure 14-10343. EPWM_DBFED Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">DEL</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31221. EPWM_DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Falling Edge Delay Count 10 bit counter

14.9.5.3.2.18 EPWM_TZSEL Register

1 EPWM_TZSEL Register (Offset = 24h) [reset = 0h]

Trip Zone Select Register

Return to Summary Table

Table 14-31222. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0024h**
EPWM1	**2301 0024h**
EPWM2	**2302 0024h**

Figure 14-10344. EPWM_TZSEL Name Register

15	14	13	12	11	10	9	8
OSHTN							
R/W							
0h							
7	6	5	4	3	2	1	0
CBCN							
R/W							
0h							

Table 14-31224. EPWM_TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description

15:8	OSHTN	R/W	0h	Trip-zone n [TZn] select One-Shot [OSHT] trip-zone enable/disable When any of the enabled pins go low, a one-shot trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs The one-shot trip condition remains latched until you clear the condition via the TZCLR register
				`0h` `Disable TZn as a one-shot trip source for this EPWM module`
				`1h` `Enable TZn as a one-shot trip source for this EPWM module`

7:0	CBCN	R/W	0h	Trip-zone n [TZn] select Cycle-by-Cycle [CBC] trip-zone enable/disable When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero
				`0h` `Disable TZn as a CBC trip source for this EPWM module`
				`1h` `Enable TZn as a CBC trip source for this EPWM module`

14.9.5.3.2.19 EPWM_TZCTL Register

1 EPWM_TZCTL Register (Offset = 28h) [reset = 0h]

Trip Zone Control Register

Return to Summary Table

Table 14-31225. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0028h**
EPWM1	**2301 0028h**
EPWM2	**2302 0028h**

Figure 14-10345. EPWM_TZCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				TZB		TZA	
R				R/W		R/W	
0h				0h		0h	

Table 14-31227. EPWM_TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved

3:2	TZB	R/W	0h	When a trip event occurs the following action is taken on output EPWMxB Which trip-zone pins can cause an event is defined in the TZSEL register
				`0h High impedance (EPWMxB = High-impedance state)`
				`1h Force EPWMxB to a high state`
				`2h Force EPWMxB to a low state`
				`3h Do nothing, no action is taken on EPWMxB.`

1:0	TZA	R/W	0h	When a trip event occurs the following action is taken on output EPWMxA Which trip-zone pins can cause an event is defined in the TZSEL register
				`0h High impedance (EPWMxA = High-impedance state)`
				`1h Force EPWMxA to a high state`
				`2h Force EPWMxA to a low state`
				`3h Do nothing, no action is taken on EPWMxA.`

14.9.5.3.2.20 EPWM_TZEINT Register

1 EPWM_TZEINT Register (Offset = 2Ah) [reset = 0h]

Trip Zone Enable Interrupt Register

Return to Summary Table

Table 14-31228. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Ah**
EPWM1	**2301 002Ah**
EPWM2	**2302 002Ah**

Figure 14-10346. EPWM_TZEINT Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1					OST	CBC	RESERVED2
R					R/W	R/W	R
0h					0h	0h	0h

Table 14-31230. EPWM_TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0h Disable one-shot interrupt generation 1h Enable Interrupt generation a one-shot trip event will cause a EPWMxTZINT interrupt.
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0h Disable cycle-by-cycle interrupt generation 1h Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMxTZINT interrupt.
0	RESERVED2	R	0h	Reserved

14.9.5.3.2.21 EPWM_TZFLG Register

1 EPWM_TZFLG Register (Offset = 2Ch) [reset = 0h]

Trip Zone Flag Register

Return to Summary Table

Table 14-31231. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Ch**
EPWM1	**2301 002Ch**
EPWM2	**2302 002Ch**

Figure 14-10347. EPWM_TZFLG Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1					OST	CBC	INT
R					R	R	R
0h					0h	0h	0h

Table 14-31233. EPWM_TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0h No one-shot trip event has occurred 1h Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0h No cycle-by-cycle trip event has occurred 1h Indicates a trip event has occurred on a pin selected as a cycle-by-cycle trip source. The EPWM_TZFLG[1] CBC bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h)
0	INT	R	0h	Latched Trip Interrupt Status Flag 0h Indicates no interrupt has been generated 1h Indicates an EPWMxTZINT interrupt was generated because of a trip condition. No further EPWMxTZINT interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.

14.9.5.3.2.22 EPWM_TZCLR Register

1 EPWM_TZCLR Register (Offset = 2Eh) [reset = 0h]

Trip Zone Clear Register

Return to Summary Table

Table 14-31234. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Eh**
EPWM1	**2301 002Eh**
EPWM2	**2302 002Eh**

Figure 14-10348. EPWM_TZCLR Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1					OST	CBC	INT
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-31236. EPWM_TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Clear Flag for One-Shot Trip [OST] Latch 0h Has no effect. Always reads back a 0h 1h Clears this Trip (set) condition
1	CBC	R/W	0h	Clear Flag for Cycle-By-Cycle [CBC] Trip Latch 0h Has no effect. Always reads back a 0h 1h Clears this Trip (set) condition
0	INT	R/W	0h	Global Interrupt Clear Flag 0h Has no effect. Always reads back a 0h 1h Clears the trip-interrupt flag for this EPWM module (EPWM_TZFLG[0] INT)

14.9.5.3.2.23 EPWM_TZFRC Register

1 EPWM_TZFRC Register (Offset = 30h) [reset = 0h]

Trip Zone Force Register

Return to Summary Table

Table 14-31237. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0030h**
EPWM1	**2301 0030h**
EPWM2	**2302 0030h**

Figure 14-10349. EPWM_TZFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1					OST	CBC	RESERVED2
R					R/W	R/W	R
0h					0h	0h	0h

Table 14-31239. EPWM_TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved

2	OST	R/W	0h	Force a One-Shot Trip Event via Software
				`0h` `writing of 0h`
				`1h` `Forces a one-shot trip event and sets the EPWM_TZFLG[2] OST bit.`

1	CBC	R/W	0h	Force a Cycle-by-Cycle Trip Event via Software
				`0h` `writing of 0h`
				`1h` `Forces a cycle-by-cycle trip event and sets the EPWM_TZFLG[1] CBC bit.`

0	RESERVED2	R	0h	Reserved

14.9.5.3.2.24 EPWM_ETSEL Register

1 EPWM_ETSEL Register (Offset = 32h) [reset = 0h]

Event Trigger Selection Register

Return to Summary Table

Table 14-31240. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0032h**
EPWM1	**2301 0032h**
EPWM2	**2302 0032h**

Figure 14-10350. EPWM_ETSEL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td>INTEN</td><td colspan="3">INTSEL</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-31242. EPWM_ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3	INTEN	R/W	0h	Enable ePWM Interrupt [EPWMx_INT] Generation 0h Disable EPWMx_INT generation 1h Enable EPWMx_INT generation
2:0	INTSEL	R/W	0h	ePWM Interrupt [EPWMx_INT] Selection Options 0h Reserved 1h Enable event time-base counter equal to zero. (EPWM_TBCNT = 0000h) 2h Enable event time-base counter equal to period (EPWM_TBCNT = EPWM_TBPRD) 3h Reserved 4h Enable event time-base counter equal to CMPA when the timer is incrementing 5h Enable event time-base counter equal to CMPA when the timer is decrementing 6h Enable event time-base counter equal to CMPB when the timer is incrementing 7h Enable event time-base counter equal to CMPB when the timer is decrementing

14.9.5.3.2.25 EPWM_ETPS Register

1 EPWM_ETPS Register (Offset = 34h) [reset = 0h]

Event Trigger Pre-Scale Register

Return to Summary Table

Table 14-31243. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0034h**
EPWM1	**2301 0034h**
EPWM2	**2302 0034h**

Figure 14-10351. EPWM_ETPS Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				INTCNT		INTPRD	
R				R		R/W	
0h				0h		0h	

Table 14-31245. EPWM_ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3:2	INTCNT	R	0h	ePWM Interrupt Event [EPWMx_INT] Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred These bits are automatically cleared when an interrupt pulse is generated If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD] 0h No events have occurred 1h 1 event has occurred 2h 2 events have occurred 3h 3 events have occurred

Table 14-31245. EPWM_ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	INTPRD	R/W	0h	ePWM Interrupt [EPWMx_INT] Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated To be generated, the interrupt must be enabled [ETSEL[INT] = 1] If the interrupt status flag is set from a previous interrupt [ETFLG[INT] = 1] then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit This allows for one interrupt to be pending while another is still being serviced Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear Writing a INTPRD value that is less than the current counter value will result in an undefined state If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented 0h Disable the interrupt event counter. No interrupt will be generated and the EPWM_ETFRC[0] INT bit is ignored. 1h Generate an interrupt on the first event INTCNT = 0b01 (first event) 2h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b10 (second event) 3h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b11 (third event)

14.9.5.3.2.26 EPWM_ETFLG Register

1 EPWM_ETFLG Register (Offset = 36h) [reset = 0h]

Event Trigger Flag Register

Return to Summary Table

Table 14-31246. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0036h**
EPWM1	**2301 0036h**
EPWM2	**2302 0036h**

Figure 14-10352. EPWM_ETFLG Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED1</td><td>INT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-31248. EPWM_ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved

0	INT	R	0h	Latched ePWM Interrupt [EPWMx_INT] Status Flag
				`0h` `Indicates no event occurred.`
				`1h` `Indicates that an EPWMx interrupt (EWPMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the EPWM_ETFLG[0] INT bit is still set. If an interrupt is pending, it will not be generated until after the EPWM_ETFLG[0] INT bit is cleared.`

14.9.5.3.2.27 EPWM_ETCLR Register

1 EPWM_ETCLR Register (Offset = 38h) [reset = 0h]

Event Trigger Clear Register

Return to Summary Table

Table 14-31249. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0038h**
EPWM1	**2301 0038h**
EPWM2	**2302 0038h**

Figure 14-10353. EPWM_ETCLR Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED1</td><td>INT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-31251. EPWM_ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	ePWM Interrupt [EPWMx_INT] Flag Clear Bit

14.9.5.3.2.28 EPWM_ETFRC Register

1 EPWM_ETFRC Register (Offset = 3Ah) [reset = 0h]

Event Trigger Force Register

Return to Summary Table

Table 14-31252. Instance Table

Instance Name	Physical Address
EPWM0	**2300 003Ah**
EPWM1	**2301 003Ah**
EPWM2	**2302 003Ah**

Figure 14-10354. EPWM_ETFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1							INT
R							R
0h							0h

Table 14-31254. EPWM_ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved

0	INT	R	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register The INT flag bit will be set regardless
				`0h` `Writing a 0 has no effect. Always reads back a 0h`
				`1h` `Writing 1 clears the EPWM_ETFLG[0] INT flag bit and enable further interrupts pulses to be generated.`

14.9.5.3.2.29 EPWM_PCCTL Register

1 EPWM_PCCTL Register (Offset = 3Ch) [reset = 0h]

PWM Chopper Control Register

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Table 14-31255. Instance Table

Instance Name	Physical Address
EPWM0	**2300 003Ch**
EPWM1	**2301 003Ch**
EPWM2	**2302 003Ch**

Figure 14-10355. EPWM_PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1					CHPDUTY		
R					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0h			0h				0h

Table 14-31257. EPWM_PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED1	R	0h	Reserved
10:8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 0h Duty = 1/8 (12.5%) 1h Duty = 2/8 (25.0%) 2h Duty = 3/8 (37.5%) 3h Duty = 4/8 (50.0%) 4h Duty = 5/8 (62.5%) 5h Duty = 6/8 (75.0%) 6h Duty = 7/8 (87.5%) 7h Reserved
7:5	CHPFREQ	R/W	0h	Chopping Clock Frequency 0h Divide by 1 (no prescale) 1h Divide by 2 2h Divide by 3 3h Divide by 4 4h Divide by 5 5h Divide by 6 6h Divide by 7 7h Divide by 8
4:1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0h 1 - SYSCLKOUT/8 wide 1h 2 - SYSCLKOUT/8 wide 2h 3 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide
0	CHPEN	R/W	0h	PWM-chopping Enable 0h Disable (bypass) PWM chopping function 1h Enable chopping function

14.9.5.3.2.30 EPWM_PID Register

1 EPWM_PID Register (Offset = 5Ch) [reset = 44D10903h]

EHRPWM Peripheral ID Register. The IP revision register is used by software to track features, bugs, and compatibility.

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Table 14-31258. Instance Table

Instance Name	Physical Address
EPWM0	**2300 005Ch**
EPWM1	**2301 005Ch**
EPWM2	**2302 005Ch**

Figure 14-10356. EPWM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED1		FUNC			
R		R		R			
1h		0h		4D1h			
23	22	21	20	19	18	17	16
FUNC							
R							
4D1h							
15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
1h					1h		
7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		3h					

Table 14-31260. EPWM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between the old scheme and current
29:28	RESERVED1	R	0h	Reserved
27:16	FUNC	R	4D1h	FUNC
15:11	R_RTL	R	1h	RTL version [R], maintained by IP design owner
10:8	X_MAJOR	R	1h	Major revision [X]
7:6	CUSTOM	R	0h	CUSTOM
5:0	Y_MINOR	R	3h	Minor revision [Y]

14.9.5.4 EQEP

EQEP

14.9.5.4.1 EQEP Summaries

EQEP Summaries

Table 14-31261. EQEP Registers, Base Address=2320 0000h, Length=256

Offset	Length	Register Name	EQEP0 Physical Address	EQEP1 Physical Address	EQEP2 Physical Address
0h	32	EQEP_QPOSCNT	2320 0000h	2321 0000h	2322 0000h
4h	32	EQEP_QPOSINIT	2320 0004h	2321 0004h	2322 0004h
8h	32	EQEP_QPOSMAX	2320 0008h	2321 0008h	2322 0008h
Ch	32	EQEP_QPOSCMP	2320 000Ch	2321 000Ch	2322 000Ch
10h	32	EQEP_QPOSILAT	2320 0010h	2321 0010h	2322 0010h
14h	32	EQEP_QPOSSLAT	2320 0014h	2321 0014h	2322 0014h
18h	32	EQEP_QPOSLAT	2320 0018h	2321 0018h	2322 0018h
1Ch	32	EQEP_QUTMR	2320 001Ch	2321 001Ch	2322 001Ch
20h	32	EQEP_QUPRD	2320 0020h	2321 0020h	2322 0020h
24h	16	EQEP_QWDTMR	2320 0024h	2321 0024h	2322 0024h
26h	16	EQEP_QWDPRD	2320 0026h	2321 0026h	2322 0026h
28h	16	EQEP_QDECCTL_TYPE2	2320 0028h	2321 0028h	2322 0028h
2Ah	16	EQEP_QEPCTL	2320 002Ah	2321 002Ah	2322 002Ah
2Ch	16	EQEP_QCAPCTL	2320 002Ch	2321 002Ch	2322 002Ch
2Eh	16	EQEP_QPOSCTL	2320 002Eh	2321 002Eh	2322 002Eh
30h	16	EQEP_QEINT_TYPE1	2320 0030h	2321 0030h	2322 0030h
32h	16	EQEP_QFLG_TYPE1	2320 0032h	2321 0032h	2322 0032h
34h	16	EQEP_QCLR_TYPE1	2320 0034h	2321 0034h	2322 0034h
36h	16	EQEP_QFRC_TYPE1	2320 0036h	2321 0036h	2322 0036h
38h	16	EQEP_QEPSTS_TYPE1	2320 0038h	2321 0038h	2322 0038h
3Ah	16	EQEP_QCTMR	2320 003Ah	2321 003Ah	2322 003Ah
3Ch	16	EQEP_QCPRD	2320 003Ch	2321 003Ch	2322 003Ch
3Eh	16	EQEP_QCTMRLAT	2320 003Eh	2321 003Eh	2322 003Eh
40h	16	EQEP_QCPRDLAT	2320 0040h	2321 0040h	2322 0040h
42h	16	EQEP_RESERVED_1_J	2320 0042h + formula	2321 0042h + formula	2322 0042h + formula
5Ch	32	EQEP_PID	2320 005Ch	2321 005Ch	2322 005Ch
60h	32	EQEP_REV_TYPE2	2320 0060h	2321 0060h	2322 0060h
64h	32	EQEP_QEPSTROBESEL	2320 0064h	2321 0064h	2322 0064h
68h	32	EQEP_QMACTRL	2320 0068h	2321 0068h	2322 0068h
6Ch	32	EQEP_QEPSRCSEL	2320 006Ch	2321 006Ch	2322 006Ch
70h	16	EQEP_RESERVED_2_J	2320 0070h + formula	2321 0070h + formula	2322 0070h + formula

14.9.5.4.2 EQEP Registers

EQEP Registers

14.9.5.4.2.1 EQEP_QPOSCNT Register

1 EQEP_QPOSCNT Register (Offset = 0h) [reset = 0h]

Position Counter

Return to Summary Table

Table 14-31262. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0000h**
EQEP1	**2321 0000h**
EQEP2	**2322 0000h**

Figure 14-10357. EQEP_QPOSCNT Name Register

31	30	29	28	27	26	25	24
QPOSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCNT							
R/W							
0h							

Table 14-31264. EQEP_QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCNT	R/W	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.2 EQEP_QPOSINIT Register

1 EQEP_QPOSINIT Register (Offset = 4h) [reset = 0h]

Position Counter Init

Return to Summary Table

Table 14-31265. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0004h**
EQEP1	**2321 0004h**
EQEP2	**2322 0004h**

Figure 14-10358. EQEP_QPOSINIT Name Register

31	30	29	28	27	26	25	24
QPOSINIT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSINIT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSINIT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSINIT							
R/W							
0h							

Table 14-31267. EQEP_QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSINIT	R/W	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.3 EQEP_QPOSMAX Register

1 EQEP_QPOSMAX Register (Offset = 8h) [reset = 0h]

Maximum Position Count

Return to Summary Table

Table 14-31268. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0008h**
EQEP1	**2321 0008h**
EQEP2	**2322 0008h**

Figure 14-10359. EQEP_QPOSMAX Name Register

31	30	29	28	27	26	25	24
QPOSMAX							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSMAX							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSMAX							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSMAX							
R/W							
0h							

Table 14-31270. EQEP_QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.4 EQEP_QPOSCMP Register

1 EQEP_QPOSCMP Register (Offset = Ch) [reset = 0h]

Position Compare

Return to Summary Table

Table 14-31271. Instance Table

Instance Name	Physical Address
EQEP0	**2320 000Ch**
EQEP1	**2321 000Ch**
EQEP2	**2322 000Ch**

Figure 14-10360. EQEP_QPOSCMP Name Register

31	30	29	28	27	26	25	24
QPOSCMP							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCMP							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCMP							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCMP							
R/W							
0h							

Table 14-31273. EQEP_QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCMP	R/W	0h	Position Compare The position-compare value in this register is compared with the position counter [QPOSCNT] to generate sync output and/or interrupt on compare match. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.5 EQEP_QPOSILAT Register

1 EQEP_QPOSILAT Register (Offset = 10h) [reset = 0h]

Index Position Latch

Return to Summary Table

Table 14-31274. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0010h**
EQEP1	**2321 0010h**
EQEP2	**2322 0010h**

Figure 14-10361. EQEP_QPOSILAT Name Register

31	30	29	28	27	26	25	24
QPOSILAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSILAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSILAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSILAT							
R							
0h							

Table 14-31276. EQEP_QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.6 EQEP_QPOSSLAT Register

1 EQEP_QPOSSLAT Register (Offset = 14h) [reset = 0h]

Strobe Position Latch

Return to Summary Table

Table 14-31277. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0014h**
EQEP1	**2321 0014h**
EQEP2	**2322 0014h**

Figure 14-10362. EQEP_QPOSSLAT Name Register

31	30	29	28	27	26	25	24
QPOSSLAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSSLAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSSLAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSSLAT							
R							
0h							

Table 14-31279. EQEP_QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSSLAT	R	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.7 EQEP_QPOSLAT Register

1 EQEP_QPOSLAT Register (Offset = 18h) [reset = 0h]

Position Latch

Return to Summary Table

Table 14-31280. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0018h**
EQEP1	**2321 0018h**
EQEP2	**2322 0018h**

Figure 14-10363. EQEP_QPOSLAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">QPOSLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">QPOSLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QPOSLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QPOSLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31282. EQEP_QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on a unit time out event. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.8 EQEP_QUTMR Register

1 EQEP_QUTMR Register (Offset = 1Ch) [reset = 0h]

QEP Unit Timer

Return to Summary Table

Table 14-31283. Instance Table

Instance Name	Physical Address
EQEP0	**2320 001Ch**
EQEP1	**2321 001Ch**
EQEP2	**2322 001Ch**

Figure 14-10364. EQEP_QUTMR Name Register

31	30	29	28	27	26	25	24
QUTMR							
R/W							
0h							
23	22	21	20	19	18	17	16
QUTMR							
R/W							
0h							
15	14	13	12	11	10	9	8
QUTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QUTMR							
R/W							
0h							

Table 14-31285. EQEP_QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUTMR	R/W	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.9 EQEP_QUPRD Register

1 EQEP_QUPRD Register (Offset = 20h) [reset = 0h]

QEP Unit Period

Return to Summary Table

Table 14-31286. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0020h**
EQEP1	**2321 0020h**
EQEP2	**2322 0020h**

Figure 14-10365. EQEP_QUPRD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">QUPRD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">QUPRD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QUPRD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QUPRD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31288. EQEP_QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUPRD	R/W	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.10 EQEP_QWDTMR Register

1 EQEP_QWDTMR Register (Offset = 24h) [reset = 0h]

QEP Watchdog Timer

Return to Summary Table

Table 14-31289. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0024h**
EQEP1	**2321 0024h**
EQEP2	**2322 0024h**

Figure 14-10366. EQEP_QWDTMR Name Register

15	14	13	12	11	10	9	8
QWDTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QWDTMR							
R/W							
0h							

Table 14-31291. EQEP_QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDTMR	R/W	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.11 EQEP_QWDPRD Register

1 EQEP_QWDPRD Register (Offset = 26h) [reset = 0h]

QEP Watchdog Period

Return to Summary Table

Table 14-31292. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0026h**
EQEP1	**2321 0026h**
EQEP2	**2322 0026h**

Figure 14-10367. EQEP_QWDPRD Name Register

15	14	13	12	11	10	9	8
QWDPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QWDPRD							
R/W							
0h							

Table 14-31294. EQEP_QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDPRD	R/W	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.12 EQEP_QDECCTL_TYPE2 Register

1 EQEP_QDECCTL_TYPE2 Register (Offset = 28h) [reset = 0h]

Quadrature Decoder Control

Return to Summary Table

Table 14-31295. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0028h**
EQEP1	**2321 0028h**
EQEP2	**2322 0028h**

Figure 14-10368. EQEP_QDECCTL_TYPE2 Name Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QBP	QIP	QSP	RESERVED_1				QIDIRE
R/W	R/W	R/W	R				R/W
0h	0h	0h	0h				0h

Table 14-31297. EQEP_QDECCTL_TYPE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	QSRC	R/W	0h	Position-counter source selection Reset Source: vbus_rst_mod_g_rst_n
13	SOEN	R/W	0h	Sync output-enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable position-compare sync output 1 Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection Reset Source: vbus_rst_mod_g_rst_n 0 Index pin is used for sync output 1 Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate Reset Source: vbus_rst_mod_g_rst_n 0 2x resolution: Count the rising/falling edge 1 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter Reset Source: vbus_rst_mod_g_rst_n 0 Quadrature-clock inputs are not swapped 1 Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option Reset Source: vbus_rst_mod_g_rst_n 0 Disable gating of Index pulse 1 Gate the index pin with strobe

Table 14-31297. EQEP_QDECCTL_TYPE2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	QAP	R/W	0h	QEPA input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPA input`
7	QBP	R/W	0h	QEPB input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPB input`
6	QIP	R/W	0h	QEPI input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPI input`
5	QSP	R/W	0h	QEPS input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPS input`
4:1	RESERVED_1	R	0h	Reserved
0	QIDIRE	R/W	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.13 EQEP_QEPCTL Register

1 EQEP_QEPCTL Register (Offset = 2Ah) [reset = 0h]

QEP Control

Return to Summary Table

Table 14-31298. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Ah**
EQEP1	**2321 002Ah**
EQEP2	**2322 002Ah**

Figure 14-10369. EQEP_QEPCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-31300. EQEP_QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation mode Reset Source: vbus_rst_mod_g_rst_n 0 QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 1 QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 2 QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 3 Same as FREE_SOFT_2
13:12	PCRM	R/W	0h	Postion counter reset Reset Source: vbus_rst_mod_g_rst_n 0 Position counter reset on an index event 1 Position counter reset on the maximum position 2 Position counter reset on the first index event 3 Position counter reset on a unit time event

Table 14-31300. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	SEI	R/W	0h	Strobe event initialization of position counter Reset Source: vbus_rst_mod_g_rst_n 0 Does nothing (action disabled) 1 Does nothing (action disabled) 2 Initializes the position counter on rising edge of the QEPS signal 3 Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9:8	IEI	R/W	0h	Index event init of position count Reset Source: vbus_rst_mod_g_rst_n 0 Do nothing (action disabled) 1 Do nothing (action disabled) 2 Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 3 Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)
7	SWI	R/W	0h	Software init position counter Reset Source: vbus_rst_mod_g_rst_n 0 Do nothing (action disabled) 1 Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	R/W	0h	Strobe event latch of position counter Reset Source: vbus_rst_mod_g_rst_n 0 The position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1 Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5:4	IEL	R/W	0h	Index event latch of position counter [software index marker] Reset Source: vbus_rst_mod_g_rst_n 0 Reserved 1 Latches position counter on rising edge of the index signal 2 Latches position counter on falling edge of the index signal 3 Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.

Table 14-31300. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QPEN	R/W	0h	Quadrature position counter enable/software reset Reset Source: vbus_rst_mod_g_rst_n 0 Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLAG register do not show value as 0 and show the actual state of that flag. 1 eQEP position counter is enabled
2	QCLM	R/W	0h	QEP capture latch mode Reset Source: vbus_rst_mod_g_rst_n 0 Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1 Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	R/W	0h	QEP unit timer enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable eQEP unit timer 1 Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable the eQEP watchdog timer 1 Enable the eQEP watchdog timer

14.9.5.4.2.14 EQEP_QCAPCTL Register

1 EQEP_QCAPCTL Register (Offset = 2Ch) [reset = 0h]

Qaudrature Capture Control

Return to Summary Table

Table 14-31301. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Ch**
EQEP1	**2321 002Ch**
EQEP2	**2322 002Ch**

Figure 14-10370. EQEP_QCAPCTL Name Register

15	14	13	12	11	10	9	8
CEN	RESERVED_1						
R/W	R						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED_1	CCPS			UPPS			
R	R/W			R/W			
0h	0h			0h			

Table 14-31303. EQEP_QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture Reset Source: vbus_rst_mod_g_rst_n 0 `eQEP capture unit is disabled` 1 `eQEP capture unit is enabled`
14:7	RESERVED_1	R	0h	Reserved
6:4	CCPS	R/W	0h	eQEP capture timer clock prescaler Reset Source: vbus_rst_mod_g_rst_n 0 `CAPCLK = SYSCLKOUT/1` 1 `CAPCLK = SYSCLKOUT/2` 2 `CAPCLK = SYSCLKOUT/4` 3 `CAPCLK = SYSCLKOUT/8` 4 `CAPCLK = SYSCLKOUT/16` 5 `CAPCLK = SYSCLKOUT/32` 6 `CAPCLK = SYSCLKOUT/64` 7 `CAPCLK = SYSCLKOUT/128`

Table 14-31303. EQEP_QCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	UPPS	R/W	0h	Unit position event prescaler Reset Source: vbus_rst_mod_g_rst_n 0 `UPEVNT = QCLK/1` 1 `UPEVNT = QCLK/2` 2 `UPEVNT = QCLK/4` 3 `UPEVNT = QCLK/8` 4 `UPEVNT = QCLK/16` 5 `UPEVNT = QCLK/32` 6 `UPEVNT = QCLK/64` 7 `UPEVNT = QCLK/128` 8 `UPEVNT = QCLK/256` 9 `UPEVNT = QCLK/512` 10 `UPEVNT = QCLK/1024` 11 `UPEVNT = QCLK/2048` 12 `Reserved` 13 `Reserved` 14 `Reserved` 15 `Reserved`

14.9.5.4.2.15 EQEP_QPOSCTL Register

1 EQEP_QPOSCTL Register (Offset = 2Eh) [reset = 0h]

Position Compare Control

Return to Summary Table

Table 14-31304. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Eh**
EQEP1	**2321 002Eh**
EQEP2	**2322 002Eh**

Figure 14-10371. EQEP_QPOSCTL Name Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCSPW							
R/W							
0h							

Table 14-31306. EQEP_QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description

15	PCSHDW	R/W	0h	Position compare of shadow enable
				Reset Source: vbus_rst_mod_g_rst_n
				`0 Shadow disabled, load Immediate`
				`1 Shadow enabled`

14	PCLOAD	R/W	0h	Position compare of shadow load
				Reset Source: vbus_rst_mod_g_rst_n
				`0 Load on QPOSCNT = 0`
				`1 Load when QPOSCNT = QPOSCMP`

13	PCPOL	R/W	0h	Polarity of sync output
				Reset Source: vbus_rst_mod_g_rst_n
				`0 Active HIGH pulse output`
				`1 Active LOW pulse output`

12	PCE	R/W	0h	Position compare enable/disable
				Reset Source: vbus_rst_mod_g_rst_n
				`0 Disable position compare unit`
				`1 Enable position compare unit`

11:0	PCSPW	R/W	0h	Select-position-compare sync output pulse width
				Reset Source: vbus_rst_mod_g_rst_n
				`0 1 * 4 * SYSCLKOUT cycles`
				`1 2 * 4 * SYSCLKOUT cycles`
				`4095 4096 * 4 * SYSCLKOUT cycles`

14.9.5.4.2.16 EQEP_QEINT_TYPE1 Register

1 EQEP_QEINT_TYPE1 Register (Offset = 30h) [reset = 0h]

QEP Interrupt Control

Return to Summary Table

Table 14-31307. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0030h**
EQEP1	**2321 0030h**
EQEP2	**2322 0030h**

Figure 14-10372. EQEP_QEINT_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31309. EQEP_QEINT_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	QMAE	R/W	0h	QMA Error Interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
11	UTO	R/W	0h	Unit time out interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled

Table 14-31309. EQEP_QEINT_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Position counter overflow interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
5	PCU	R/W	0h	Position counter underflow interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
4	WTO	R/W	0h	Watchdog time out interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
3	QDC	R/W	0h	Quadrature direction change interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
2	QPE	R/W	0h	Quadrature phase error interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
1	PCE	R/W	0h	Position counter error interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
0	RESERVED_1	R	0h	Reserved

14.9.5.4.2.17 EQEP_QFLG_TYPE1 Register

1 EQEP_QFLG_TYPE1 Register (Offset = 32h) [reset = 0h]

QEP Interrupt Flag

Return to Summary Table

Table 14-31310. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0032h**
EQEP1	**2321 0032h**
EQEP2	**2322 0032h**

Figure 14-10373. EQEP_QFLG_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31312. EQEP_QFLG_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved

12	QMAE	R	0h	QMA Error interrupt flag
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No interrupt generated`
				`1 Interrupt was generated`

11	UTO	R	0h	Unit time out interrupt flag
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No interrupt generated`
				`1 Set by eQEP unit timer period match`

10	IEL	R	0h	Index event latch interrupt flag
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No interrupt generated`
				`1 This bit is set after latching the QPOSCNT to QPOSILAT`

9	SEL	R	0h	Strobe event latch interrupt flag
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No interrupt generated`
				`1 This bit is set after latching the QPOSCNT to QPOSSLAT`

8	PCM	R	0h	eQEP compare match event interrupt flag
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No interrupt generated`
				`1 This bit is set on position-compare match`

Table 14-31312. EQEP_QFLG_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PCR	R	0h	Position-compare ready interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `This bit is set after transferring the shadow register value to the active position compare register`
6	PCO	R	0h	Position counter overflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `This bit is set on position counter overflow.`
5	PCU	R	0h	Position counter underflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `This bit is set on position counter underflow.`
4	WTO	R	0h	Watchdog timeout interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `Set by watchdog timeout`
3	QDC	R	0h	Quadrature direction change interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `Interrupt was generated`
2	PHE	R	0h	Quadrature phase error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `Set on simultaneous transition of QEPA and QEPB`
1	PCE	R	0h	Position counter error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `Position counter error`
0	INT	R	0h	Global interrupt status flag Reset Source: vbus_rst_mod_g_rst_n 0 `No interrupt generated` 1 `Interrupt was generated`

14.9.5.4.2.18 EQEP_QCLR_TYPE1 Register

1 EQEP_QCLR_TYPE1 Register (Offset = 34h) [reset = 0h]

QEP Interrupt Clear

Return to Summary Table

Table 14-31313. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0034h**
EQEP1	**2321 0034h**
EQEP2	**2322 0034h**

Figure 14-10374. EQEP_QCLR_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31315. EQEP_QCLR_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	QMAE	R/W	0h	Clear QMA Error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
11	UTO	R/W	0h	Clear unit time out interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
10	IEL	R/W	0h	Clear index event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
9	SEL	R/W	0h	Clear strobe event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
8	PCM	R/W	0h	Clear eQEP compare match event interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
7	PCR	R/W	0h	Clear position-compare ready interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`

Table 14-31315. EQEP_QCLR_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Clear position counter overflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
5	PCU	R/W	0h	Clear position counter underflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
4	WTO	R/W	0h	Clear watchdog timeout interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
3	QDC	R/W	0h	Clear quadrature direction change interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
2	PHE	R/W	0h	Clear quadrature phase error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
1	PCE	R/W	0h	Clear position counter error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
0	INT	R/W	0h	Global interrupt clear flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`

14.9.5.4.2.19 EQEP_QFRC_TYPE1 Register

1 EQEP_QFRC_TYPE1 Register (Offset = 36h) [reset = 0h]

QEP Interrupt Force

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Table 14-31316. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0036h**
EQEP1	**2321 0036h**
EQEP2	**2322 0036h**

Figure 14-10375. EQEP_QFRC_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31318. EQEP_QFRC_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved

12	QMAE	R/W	0h	Force QMA error interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

11	UTO	R/W	0h	Force unit time out interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

10	IEL	R/W	0h	Force index event latch interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

9	SEL	R/W	0h	Force strobe event latch interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

8	PCM	R/W	0h	Force position-compare match interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

7	PCR	R/W	0h	Force position-compare ready interrupt
				Reset Source: vbus_rst_mod_g_rst_n
				`0 No effect`
				`1 Force the interrupt`

Table 14-31318. EQEP_QFRC_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Force position counter overflow interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
5	PCU	R/W	0h	Force position counter underflow interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
4	WTO	R/W	0h	Force watchdog time out interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
3	QDC	R/W	0h	Force quadrature direction change interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
2	PHE	R/W	0h	Force quadrature phase error interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
1	PCE	R/W	0h	Force position counter error interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
0	RESERVED_1	R	0h	Reserved

14.9.5.4.2.20 EQEP_QEPSTS_TYPE1 Register

1 EQEP_QEPSTS_TYPE1 Register (Offset = 38h) [reset = 80h]

QEP Status

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Table 14-31319. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0038h**
EQEP1	**2321 0038h**
EQEP2	**2322 0038h**

Figure 14-10376. EQEP_QEPSTS_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W	R	R	R	R/W	R/W	R/W	R
1h	0h	0h	0h	0h	0h	0h	0h

Table 14-31321. EQEP_QEPSTS_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	UPEVNT	R/W	1h	Unit position event flag Reset Source: vbus_rst_mod_g_rst_n 0 `No unit position event detected` 1 `Unit position event detected. Write 1 to clear`
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement) on the first index event` 1 `Clockwise rotation (or forward movement) on the first index event`
5	QDF	R	0h	Quadrature direction flag Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement)` 1 `Clockwise rotation (or forward movement)`
4	QDLF	R	0h	eQEP direction latch flag Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement) on index event marker` 1 `Clockwise rotation (or forward movement) on index event marker`

Table 14-31321. EQEP_QEPSTS_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COEF	R/W	0h	Capture overflow error flag Reset Source: vbus_rst_mod_g_rst_n 0 Overflow has not occurred. 1 Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	R/W	0h	Capture direction error flag Reset Source: vbus_rst_mod_g_rst_n 0 Capture direction error has not occurred. 1 Direction change occurred between the capture position event. This bit is cleared by writing a '1'.
1	FIMF	R/W	0h	First index marker flag Reset Source: vbus_rst_mod_g_rst_n 0 First index pulse has not occurred. 1 Set by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Reset Source: vbus_rst_mod_g_rst_n 0 No error occurred during the last index transition 1 Position counter error

14.9.5.4.2.21 EQEP_QCTMR Register

1 EQEP_QCTMR Register (Offset = 3Ah) [reset = 0h]

QEP Capture Timer

Return to Summary Table

Table 14-31322. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Ah**
EQEP1	**2321 003Ah**
EQEP2	**2322 003Ah**

Figure 14-10377. EQEP_QCTMR Name Register

15	14	13	12	11	10	9	8
QCTMR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QCTMR							
R/W							
0h							

Table 14-31324. EQEP_QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMR	R/W	0h	This register provides time base for edge capture unit. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.22 EQEP_QCPRD Register

1 EQEP_QCPRD Register (Offset = 3Ch) [reset = 0h]

QEP Capture Period

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Table 14-31325. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Ch**
EQEP1	**2321 003Ch**
EQEP2	**2322 003Ch**

Figure 14-10378. EQEP_QCPRD Name Register

15	14	13	12	11	10	9	8
QCPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QCPRD							
R/W							
0h							

Table 14-31327. EQEP_QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.23 EQEP_QCTMRLAT Register

1 EQEP_QCTMRLAT Register (Offset = 3Eh) [reset = 0h]

QEP Capture Latch

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Table 14-31328. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Eh**
EQEP1	**2321 003Eh**
EQEP2	**2322 003Eh**

Figure 14-10379. EQEP_QCTMRLAT Name Register

15	14	13	12	11	10	9	8
QCTMRLAT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QCTMRLAT							
R							
0h							

Table 14-31330. EQEP_QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.24 EQEP_QCPRDLAT Register

1 EQEP_QCPRDLAT Register (Offset = 40h) [reset = 0h]

QEP Capture Period Latch

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Table 14-31331. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0040h**
EQEP1	**2321 0040h**
EQEP2	**2322 0040h**

Figure 14-10380. EQEP_QCPRDLAT Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QCPRDLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QCPRDLAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31333. EQEP_QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRDLAT	R	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.25 EQEP_RESERVED_1_j Register

1 EQEP_RESERVED_1_j Register (Offset = 42h + formula) [reset = 0h]

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Offset = 42h + (j * 2h); where j = 0 to 12d

Table 14-31334. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0042h + formula**
EQEP1	**2321 0042h + formula**
EQEP2	**2322 0042h + formula**

Figure 14-10381. EQEP_RESERVED_1_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-31336. EQEP_RESERVED_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.5.4.2.26 EQEP_PID Register

1 EQEP_PID Register (Offset = 5Ch) [reset = 44D30200h]

Peripheral ID Register

Return to Summary Table

Table 14-31337. Instance Table

Instance Name	Physical Address
EQEP0	**2320 005Ch**
EQEP1	**2321 005Ch**
EQEP2	**2322 005Ch**

Figure 14-10382. EQEP_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">RESERVED</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">4D3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4D3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-31339. EQEP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Reset Source: vbus_rst_mod_g_rst_n
29:28	RESERVED	R	0h	
27:16	FUNCTION	R	4D3h	Reset Source: vbus_rst_mod_g_rst_n
15:11	RTL	R	0h	Reset Source: vbus_rst_mod_g_rst_n
10:8	MAJOR	R	2h	Reset Source: vbus_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Reset Source: vbus_rst_mod_g_rst_n
5:0	MINOR	R	0h	Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.27 EQEP_REV_TYPE2 Register

1 EQEP_REV_TYPE2 Register (Offset = 60h) [reset = 9h]

QEP Revision Number

Return to Summary Table

Table 14-31340. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0060h**
EQEP1	**2321 0060h**
EQEP2	**2322 0060h**

Figure 14-10383. EQEP_REV_TYPE2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		MINOR			MAJOR		
R		R			R		
0h		1h			1h		

Table 14-31342. EQEP_REV_TYPE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_1	R	0h	Reserved
5:3	MINOR	R	1h	This field specifies the Minor Revision number for the eQEP IP. Reset Source: vbus_rst_mod_g_rst_n
2:0	MAJOR	R	1h	This field specifies the Major Revision number for the eQEP IP. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.28 EQEP_QEPSTROBESEL Register

1 EQEP_QEPSTROBESEL Register (Offset = 64h) [reset = 0h]

QEP Strobe select register

Return to Summary Table

Table 14-31343. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0064h**
EQEP1	**2321 0064h**
EQEP2	**2322 0064h**

Figure 14-10384. EQEP_QEPSTROBESEL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						STROBESEL	
R						R/W	
0h						0h	

Table 14-31345. EQEP_QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1:0	STROBESEL	R/W	0h	Strobe source select: Reset Source: vbus_rst_mod_g_rst_n 0 QEP Strobe after polarity mux 1 QEP Strobe after polarity mux. Same as QS_AFTER_POL_MUX 2 QEP Strobe after polarity mux ORed with ADCSOCA 3 QEP Strobe after polarity mux ORed with ADCSOCB

14.9.5.4.2.29 EQEP_QMACTRL Register

1 EQEP_QMACTRL Register (Offset = 68h) [reset = 0h]

QMA Control register

Return to Summary Table

Table 14-31346. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0068h**
EQEP1	**2321 0068h**
EQEP2	**2322 0068h**

Figure 14-10385. EQEP_QMACTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1					MODE		
R					R/W		
0h					0h		

Table 14-31348. EQEP_QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved
2:0	MODE	R/W	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed [reserved] 1xx : QMA Module is bypassed [reserved] Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.30 EQEP_QEPSRCSEL Register

1 EQEP_QEPSRCSEL Register (Offset = 6Ch) [reset = 0h]

QEP Source Select Register

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Table 14-31349. Instance Table

Instance Name	Physical Address
EQEP0	**2320 006Ch**
EQEP1	**2321 006Ch**
EQEP2	**2322 006Ch**

Figure 14-10386. EQEP_QEPSRCSEL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
QEPSSEL				QEPISEL			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
QEPBSEL				QEPASEL			
R/W				R/W			
0h				0h			

Table 14-31351. EQEP_QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved
15:12	QEPSSEL	R/W	0h	QEP Strobe source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
11:8	QEPISEL	R/W	0h	QEP Index source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
7:4	QEPBSEL	R/W	0h	QEPB source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
3:0	QEPASEL	R/W	0h	QEPA source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n

14.9.5.4.2.31 EQEP_RESERVED_2_j Register

1 EQEP_RESERVED_2_j Register (Offset = 70h + formula) [reset = 0h]

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Offset = 70h + (j * 2h); where j = 0 to 7d

Table 14-31352. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0070h + formula**
EQEP1	**2321 0070h + formula**
EQEP2	**2322 0070h + formula**

Figure 14-10387. EQEP_RESERVED_2_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-31354. EQEP_RESERVED_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.6 Camera Subsystem Registers

14.9.6.1 dphy_rx

dphy_rx

14.9.6.1.1 dphy_rx Summaries

dphy_rx Summaries

Table 14-31355. K3_DPHY_RX Registers, Base Address=3011 0000h, Length=4096

Offset	Length	Register Name	DPHY_RX0 Physical Address
20h	32	K3_DPHY_RX_CMN0_CMN_DIG_TBIT2	3011 0020h
40h	32	K3_DPHY_RX_CMN0_CMN_DIG_TBIT10	3011 0040h
4Ch	32	K3_DPHY_RX_CMN0_CMN_DIG_TBIT13	3011 004Ch
50h	32	K3_DPHY_RX_CMN0_CMN_DIG_TBIT14	3011 0050h
B00h	32	K3_DPHY_RX_PCS_TX_DIG_TBIT0	3011 0B00h
B04h	32	K3_DPHY_RX_PCS_TX_DIG_TBIT1	3011 0B04h
B08h	32	K3_DPHY_RX_PCS_TX_DIG_TBIT2	3011 0B08h
B0Ch	32	K3_DPHY_RX_PCS_TX_DIG_TBIT3	3011 0B0Ch

Table 14-31356. K3_DPHY_WRAP_REGS Registers, Base Address=3011 1000h, Length=256

Offset	Length	Register Name	DPHY_RX0 Physical Address
0h	32	K3_DPHY_WRAP_REGS_LANE	3011 1000h

14.9.6.1.2 dphy_rx Registers

dphy_rx Registers

14.9.6.1.2.1 K3_DPHY_RX_CMN0_CMN_DIG_TBIT2 Register

1 K3_DPHY_RX_CMN0_CMN_DIG_TBIT2 Register (Offset = 20h) [reset = 28h]

CMN_DIG_TBIT2

Return to Summary Table

Table 14-31357. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0020h**

Figure 14-10388. K3_DPHY_RX_CMN0_CMN_DIG_TBIT2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">UNUSED</td><td>O_CMN_RX_MODE_EN</td><td>O_CMN_TX_MODE_EN</td><td>O_SSM_WAIT_BGCAL_EN</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>14h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">O_SSM_WAIT_BGCAL_EN</td><td>O_CMN_SSM_EN</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">14h</td><td>0h</td></tr>
</table>

Table 14-31359. K3_DPHY_RX_CMN0_CMN_DIG_TBIT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	UNUSED	R	0h	RESERVED
10	O_CMN_RX_MODE_EN	R/W	0h	Enable CMN RX related StateMachines
9	O_CMN_TX_MODE_EN	R/W	0h	Enable CMN TX related StateMachines
8:1	O_SSM_WAIT_BGCAL_EN	R/W	14h	Wait time for Calibrations enable after bandgap is enabled [in us]
0	O_CMN_SSM_EN	R/W	0h	Enable CMN startup state machine

14.9.6.1.2.2 K3_DPHY_RX_CMN0_CMN_DIG_TBIT10 Register

1 K3_DPHY_RX_CMN0_CMN_DIG_TBIT10 Register (Offset = 40h) [reset = 800000h]

CMN_DIG_TBIT10

Return to Summary Table

Table 14-31360. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0040h**

Figure 14-10389. K3_DPHY_RX_CMN0_CMN_DIG_TBIT10 Name Register

31	30	29	28	27	26	25	24
UNUSED				O_ANA_PLL_BYTECLK_DIV			
R				R/W			
0h				8h			
23	22	21	20	19	18	17	16
O_ANA_PLL_BYTECLK_DIV				O_ANA_PLL_GM_PWM_DIV_LOW			
R/W				R/W			
8h				0h			
15	14	13	12	11	10	9	8
O_ANA_PLL_GM_PWM_DIV_LOW						O_ANA_PLL_GM_PWM_DIV_HIGH	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
O_ANA_PLL_GM_PWM_DIV_HIGH							
R/W							
0h							

Table 14-31362. K3_DPHY_RX_CMN0_CMN_DIG_TBIT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	UNUSED	R	0h	RESERVED
27:20	O_ANA_PLL_BYTECLK_DIV	R/W	8h	Byteclk divider value
19:10	O_ANA_PLL_GM_PWM_DIV_LOW	R/W	0h	Low division value setting for the gm PWM control divider
9:0	O_ANA_PLL_GM_PWM_DIV_HIGH	R/W	0h	High division value setting for the gm PWM control divider

14.9.6.1.2.3 K3_DPHY_RX_CMN0_CMN_DIG_TBIT13 Register

1 K3_DPHY_RX_CMN0_CMN_DIG_TBIT13 Register (Offset = 4Ch) [reset = 0h]

CMN_DIG_TBIT13

Return to Summary Table

Table 14-31363. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 004Ch**

Figure 14-10390. K3_DPHY_RX_CMN0_CMN_DIG_TBIT13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">O_ANA_PLL_FB_DIV_LOW_TM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">O_ANA_PLL_FB_DIV_LOW_TM</td><td>O_ANA_PLL_FB_DIV_LOW_TM_SEL</td><td colspan="5">O_ANA_PLL_FB_DIV_HIGH_TM</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">O_ANA_PLL_FB_DIV_HIGH_TM</td><td>O_ANA_PLL_FB_DIV_HIGH_TM_SEL</td><td colspan="2">UNUSED</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td colspan="2">R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31365. K3_DPHY_RX_CMN0_CMN_DIG_TBIT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	O_ANA_PLL_FB_DIV_LOW_TM	R/W	0h	forced value for pll_fb_div_clk_low
21	O_ANA_PLL_FB_DIV_LOW_TM_SEL	R/W	0h	pll_fb_div_clk_low forced from test registers
20:11	O_ANA_PLL_FB_DIV_HIGH_TM	R/W	0h	forced value for pll_fb_div_clk_high
10	O_ANA_PLL_FB_DIV_HIGH_TM_SEL	R/W	0h	pll_fb_div_clk_high forced from test registers
9:0	UNUSED	R	0h	RESERVED

14.9.6.1.2.4 K3_DPHY_RX_CMN0_CMN_DIG_TBIT14 Register

1 K3_DPHY_RX_CMN0_CMN_DIG_TBIT14 Register (Offset = 50h) [reset = 0h]

CMN_DIG_TBIT14

Return to Summary Table

Table 14-31366. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0050h**

Figure 14-10391. K3_DPHY_RX_CMN0_CMN_DIG_TBIT14 Name Register

31	30	29	28	27	26	25	24
UNUSED							
R							
0h							
23	22	21	20	19	18	17	16
UNUSED							
R							
0h							
15	14	13	12	11	10	9	8
UNUSED			O_ANA_PLL_OP_DIV_TM				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
O_ANA_PLL_OP_DIV_TM	O_ANA_PLL_OP_DIV_TM_SEL	O_ANA_PLL_IP_DIV_TM					O_ANA_PLL_IP_DIV_TM_SEL
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-31368. K3_DPHY_RX_CMN0_CMN_DIG_TBIT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	UNUSED	R	0h	RESERVED
12:7	O_ANA_PLL_OP_DIV_TM	R/W	0h	forced value for op_div
6	O_ANA_PLL_OP_DIV_TM_SEL	R/W	0h	op_div forced from test registers
5:1	O_ANA_PLL_IP_DIV_TM	R/W	0h	forced value for ip_div
0	O_ANA_PLL_IP_DIV_TM_SEL	R/W	0h	ip_div forced from test registers

14.9.6.1.2.5 K3_DPHY_RX_PCS_TX_DIG_TBIT0 Register

1 K3_DPHY_RX_PCS_TX_DIG_TBIT0 Register (Offset = B00h) [reset = 0h]

PHY_BAND_CONTROL

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Table 14-31369. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0B00h**

Figure 14-10392. K3_DPHY_RX_PCS_TX_DIG_TBIT0 Name Register

31	30	29	28	27	26	25	24
UNUSED							
R							
0h							
23	22	21	20	19	18	17	16
UNUSED							
R							
0h							
15	14	13	12	11	10	9	8
UNUSED						BAND_CTL_REG_R	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
BAND_CTL_REG_R			BAND_CTL_REG_L				
R/W			R/W				
0h			0h				

Table 14-31371. K3_DPHY_RX_PCS_TX_DIG_TBIT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	UNUSED	R	0h	RESERVED
9:5	BAND_CTL_REG_R	R/W	0h	Data Rate [80_100] MHz
4:0	BAND_CTL_REG_L	R/W	0h	Data Rate [80_100] MHz

14.9.6.1.2.6 K3_DPHY_RX_PCS_TX_DIG_TBIT1 Register

1 K3_DPHY_RX_PCS_TX_DIG_TBIT1 Register (Offset = B04h) [reset = 0h]

PHY_PSM_CONFIG

Return to Summary Table

Table 14-31372. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0B04h**

Figure 14-10393. K3_DPHY_RX_PCS_TX_DIG_TBIT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">UNUSED</td><td>PSM_CLOCK_FREQ</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">PSM_CLOCK_FREQ</td><td>PSM_CLOCK_FREQ_EN</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-31374. K3_DPHY_RX_PCS_TX_DIG_TBIT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	UNUSED	R	0h	RESERVED
8:1	PSM_CLOCK_FREQ	R/W	0h	psm_clock freq value
0	PSM_CLOCK_FREQ_EN	R/W	0h	take psm_clock_freq from tbit

14.9.6.1.2.7 K3_DPHY_RX_PCS_TX_DIG_TBIT2 Register

1 K3_DPHY_RX_PCS_TX_DIG_TBIT2 Register (Offset = B08h) [reset = 22222222h]

PHY_PI_PH2_DL_CONFIG

Return to Summary Table

Table 14-31375. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0B08h**

Figure 14-10394. K3_DPHY_RX_PCS_TX_DIG_TBIT2 Name Register

31	30	29	28	27	26	25	24
POWER_SW_2_TIME_DL_R_3				POWER_SW_2_TIME_DL_R_2			
R/W				R/W			
2h				2h			
23	22	21	20	19	18	17	16
POWER_SW_2_TIME_DL_R_1				POWER_SW_2_TIME_DL_R_0			
R/W				R/W			
2h				2h			
15	14	13	12	11	10	9	8
POWER_SW_2_TIME_DL_L_3				POWER_SW_2_TIME_DL_L_2			
R/W				R/W			
2h				2h			
7	6	5	4	3	2	1	0
POWER_SW_2_TIME_DL_L_1				POWER_SW_2_TIME_DL_L_0			
R/W				R/W			
2h				2h			

Table 14-31377. K3_DPHY_RX_PCS_TX_DIG_TBIT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	POWER_SW_2_TIME_DL_R_3	R/W	2h	power_sw_2_time_dl_r_3
27:24	POWER_SW_2_TIME_DL_R_2	R/W	2h	power_sw_2_time_dl_r_2
23:20	POWER_SW_2_TIME_DL_R_1	R/W	2h	power_sw_2_time_dl_r_1
19:16	POWER_SW_2_TIME_DL_R_0	R/W	2h	power_sw_2_time_dl_r_0
15:12	POWER_SW_2_TIME_DL_L_3	R/W	2h	power_sw_2_time_dl_l_3
11:8	POWER_SW_2_TIME_DL_L_2	R/W	2h	power_sw_2_time_dl_l_2
7:4	POWER_SW_2_TIME_DL_L_1	R/W	2h	power_sw_2_time_dl_l_1
3:0	POWER_SW_2_TIME_DL_L_0	R/W	2h	power_sw_2_time_dl_l_0

14.9.6.1.2.8 K3_DPHY_RX_PCS_TX_DIG_TBIT3 Register

1 K3_DPHY_RX_PCS_TX_DIG_TBIT3 Register (Offset = B0Ch) [reset = 222h]

PHY_PI_PH2_CL_CMN_CONFIG

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Table 14-31378. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 0B0Ch**

Figure 14-10395. K3_DPHY_RX_PCS_TX_DIG_TBIT3 Name Register

31	30	29	28	27	26	25	24
UNUSED							
R							
0h							
23	22	21	20	19	18	17	16
UNUSED							
R							
0h							
15	14	13	12	11	10	9	8
UNUSED				POWER_SW_2_TIME_CMN			
R				R/W			
0h				2h			
7	6	5	4	3	2	1	0
POWER_SW_2_TIME_CL_R				POWER_SW_2_TIME_CL_L			
R/W				R/W			
2h				2h			

Table 14-31380. K3_DPHY_RX_PCS_TX_DIG_TBIT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	UNUSED	R	0h	RESERVED
11:8	POWER_SW_2_TIME_CMN	R/W	2h	power_sw_2_time_cmn
7:4	POWER_SW_2_TIME_CL_R	R/W	2h	power_sw_2_time_cl_r
3:0	POWER_SW_2_TIME_CL_L	R/W	2h	power_sw_2_time_cl_l

14.9.6.1.2.9 K3_DPHY_WRAP_REGS_LANE Register

1 K3_DPHY_WRAP_REGS_LANE Register (Offset = 0h) [reset = 0h]

lane control and status

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Table 14-31381. Instance Table

Instance Name	Physical Address
DPHY_RX0	**3011 1000h**

Figure 14-10396. K3_DPHY_WRAP_REGS_LANE Name Register

31	30	29	28	27	26	25	24
RXCLKACTIVE HSCLK	CMN_READY	RESERVED			PSO_DISABLE	RESERVED	PSO_CMN
R	R	NONE			R/W	NONE	R/W
0h	0h	0h			0h	0h	0h
23	22	21	20	19	18	17	16
LANE_RSTB_CMN	PSM_CLOCK_FREQ						
R/W	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED				IPCONFIG_CMN			CLK_SWAPDPDN_DL_L_3
NONE				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
CLK_SWAPDPDN_DL_L_2	DATA_SWAPDPDN_DL_L_3	DATA_SWAPDPDN_DL_L_2	CLK_SWAPDPDN_DL_L_1	CLK_SWAPDPDN_DL_L_0	DATA_SWAPDPDN_DL_L_1	DATA_SWAPDPDN_DL_L_0	CLK_SWAPDPDN_CL_L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-31383. K3_DPHY_WRAP_REGS_LANE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RXCLKACTIVEHSCLK	R	0h	Receiver high speed clock active: Driven active when the receiver high speed clock is active. 1'b0: Receiver high speed clock not active, 1'b1: Receiver high speed clock active Reset Source: rst_n
30	CMN_READY	R	0h	Common ready indication: Indicates the completion of the startup process of the common module. Once this signal is driven active, the PMA lanes may be released from reset. 1'b0 : Indicates that the startup process for the common components is not complete. This will be the case for both the power on reset sequence, and when the common is transitioning into and out of the low power modes. 1'b1: Indicates that the startup process for the common components is complete and the common is ready. Note that this is a function of the PLL being enabled and locked. Reset Source: rst_n
29:27	RESERVED	NONE	0h	Reserved

Table 14-31383. K3_DPHY_WRAP_REGS_LANE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	PSO_DISABLE	R/W	0h	Disable power shut off: Disables the ability to switch off the analog switched power islands in the lane when in the ultra low power state. 1'b0: Power islands are switched off and on under the normal control of the escape mode process. 1'b1: Power island shutoff functions disabled, and switched power islands forced to the enabled state. Reset Source: rst_n
25	RESERVED	NONE	0h	Reserved
24	PSO_CMN	R/W	0h	Disable power shut off: Power Shutoff signal for CMN 1 : CMN is power OFF 0 : CMN is power ON Reset Source: rst_n
23	LANE_RSTB_CMN	R/W	0h	SW reset for CMN. 0:asserted 1:released Reset Source: rst_n
22:16	PSM_CLOCK_FREQ	R/W	0h	PMA state machine clock frequency divider control: This signal specifies a divider value used to create an internal divided clock that is a function of the psm_clock clock. This signal must be driven with a value such that the frequency of the divided clock is 1 MHz. In the case where it is not possible for the divided clock to be exactly 1 MHz, a value should be selected that results in the clock frequency being the closest to 1 MHz. The following specifies the divider settings that the values of this signal correspond to. # 8'h00 : Reserved # 8'h01 : Div 1 # 8'h02 : Div 2 # 8'h03 : Div 3 # 8'h04 : Div 4 ... # 8'hFF : Div 255 Note: PSM clock has a maximum frequency of 100 MHz. values beyond 100 should not be programmed Reset Source: rst_n
15:12	RESERVED	NONE	0h	Reserved
11:9	IPCONFIG_CMN	R/W	0h	This signal decides which clock lane acts as initiator clock lane to all data lanes. Needed only for RX IP. Bit[2]: Reserved CASE {Bit[1],Bit[0]}: 00: Left RX clk lane provides clock to all left and right data lanes. 01: Left RX clk lane provides clock to all right data lanes, Right RX clk lane provides clock to all left data lanes. 10: Right RX clk lane provides clock to all right data lanes, Left RX clk lane provides clock to all left data lanes. 11: Right RX clk lane provides clock to all left and right data lanes. Reset Source: rst_n
8	CLK_SWAPDPDN_DL_L_3	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
7	CLK_SWAPDPDN_DL_L_2	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
6	DATA_SWAPDPDN_DL_L_3	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
5	DATA_SWAPDPDN_DL_L_2	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
4	CLK_SWAPDPDN_DL_L_1	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
3	CLK_SWAPDPDN_DL_L_0	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n

Table 14-31383. K3_DPHY_WRAP_REGS_LANE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DATA_SWAPDPDN_DL_L_1	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
1	DATA_SWAPDPDN_DL_L_0	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n
0	CLK_SWAPDPDN_CL_L	R/W	0h	Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b0: Not swapped 1'b1: Swapped Reset Source: rst_n

14.9.7 Timer Modules Registers

14.9.7.1 GTC

GTC

14.9.7.1.1 GTC Summaries

GTC Summaries

Table 14-31384. GTC_CFG0 Registers, Base Address=00A8 0000h, Length=1024

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG0_PID	00A8 0000h
4h	32	GTC_CFG0_GTC_PID	00A8 0004h
8h	32	GTC_CFG0_PUSHEVT	00A8 0008h

Table 14-31385. GTC_CFG1 Registers, Base Address=00A9 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG1_CNTCR	00A9 0000h
4h	32	GTC_CFG1_CNTSR	00A9 0004h
8h	32	GTC_CFG1_CNTCV_LO	00A9 0008h
Ch	32	GTC_CFG1_CNTCV_HI	00A9 000Ch
20h	32	GTC_CFG1_CNTFID0	00A9 0020h
24h	32	GTC_CFG1_CNTFID1	00A9 0024h

Table 14-31386. GTC_CFG2 Registers, Base Address=00AA 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG2_CNTCVS_LO	00AA 0000h
4h	32	GTC_CFG2_CNTCVS_HI	00AA 0004h

Table 14-31387. GTC_CFG3 Registers, Base Address=00AB 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
8h	32	GTC_CFG3_CNTTIDR	00AB 0008h

14.9.7.1.2 GTC Registers

GTC Registers

14.9.7.1.2.1 GTC_CFG0_PID Register

1 GTC_CFG0_PID Register (Offset = 0h) [reset = 61800209h]

PID register

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Table 14-31388. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A8 0000h**

Figure 14-10397. GTC_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM		PID_MINOR					
R		R					
0h		9h					

Table 14-31390. GTC_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	9h	Reset Source: mod_g_rst_n

14.9.7.1.2.2 GTC_CFG0_GTC_PID Register

1 GTC_CFG0_GTC_PID Register (Offset = 4h) [reset = 661A0000h]

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Table 14-31391. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A8 0004h**

Figure 14-10398. GTC_CFG0_GTC_PID Name Register

31	30	29	28	27	26	25	24
GTC_PID_SCHEME		GTC_PID_BU		GTC_PID_FUNC			
R		R		R			
1h		2h		61Ah			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GTC_PID_FUNC							
R							
61Ah							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GTC_PID_R_RTL					GTC_PID_X_MAJOR		
R					R		
X					X		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GTC_PID_CUSTOM		GTC_PID_Y_MINOR					
R		R					
X		X					

Table 14-31393. GTC_CFG0_GTC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	GTC_PID_SCHEME	R	1h	PID follows new scheme Reset Source: mod_por_rst_n
29:28	GTC_PID_BU	R	2h	Business unit - Processors Reset Source: mod_por_rst_n
27:16	GTC_PID_FUNC	R	61Ah	Module functional identifier - GTC module Reset Source: mod_por_rst_n
15:11	GTC_PID_R_RTL	R	X	RTL revision number - actual value determined by RTL Reset Source: mod_por_rst_n
10:8	GTC_PID_X_MAJOR	R	X	Major revision number - actual value determined by RTL Reset Source: mod_por_rst_n
7:6	GTC_PID_CUSTOM	R	X	Custom revision number - actual value determined by RTL Reset Source: mod_por_rst_n
5:0	GTC_PID_Y_MINOR	R	X	Minor revision number - actual value determined by RTL Reset Source: mod_por_rst_n

14.9.7.1.2.3 GTC_CFG0_PUSHEVT Register

1 GTC_CFG0_PUSHEVT Register (Offset = 8h) [reset = 0h]

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Table 14-31394. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A8 0008h**

Figure 14-10399. GTC_CFG0_PUSHEVT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PUSHEVT_EXPBIT_SEL</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-31396. GTC_CFG0_PUSHEVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PUSHEVT_EXPBIT_SEL	R/W	0h	Selects which bit [63:0] of the System Counter value is exported on the push_evt output. This field controls the 64:1 mux that drives the push_evt output. Reset Source: mod_por_rst_n

14.9.7.1.2.4 GTC_CFG1_CNTCR Register

1 GTC_CFG1_CNTCR Register (Offset = 0h) [reset = 0h]

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Table 14-31397. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A9 0000h**

Figure 14-10400. GTC_CFG1_CNTCR Name Register

31	30	29	28	27	26	25	24
CNTCR_FCREQ							
R							
0h							
23	22	21	20	19	18	17	16
CNTCR_FCREQ							
R							
0h							
15	14	13	12	11	10	9	8
CNTCR_FCREQ							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNTCR_HDBG	CNTCR_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-31399. GTC_CFG1_CNTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTCR_FCREQ	R	0h	Frequency Change Request Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTCR_HDBG	R/W	0h	Halt on Debug Reset Source: mod_por_rst_n
0	CNTCR_EN	R/W	0h	Enable System Counter Reset Source: mod_por_rst_n

14.9.7.1.2.5 GTC_CFG1_CNTSR Register

1 GTC_CFG1_CNTSR Register (Offset = 4h) [reset = 0h]

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Table 14-31400. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0004h

Figure 14-10401. GTC_CFG1_CNTSR Name Register

31	30	29	28	27	26	25	24
CNTSR_FCACK							
R							
0h							
23	22	21	20	19	18	17	16
CNTSR_FCACK							
R							
0h							
15	14	13	12	11	10	9	8
CNTSR_FCACK							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNTSR_DBGH	RESERVED
NONE						R	NONE
0h						X	0h

Table 14-31402. GTC_CFG1_CNTSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTSR_FCACK	R	0h	Frequency Change Ackowledge Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTSR_DBGH	R	X	Debug Halt Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.9.7.1.2.6 GTC_CFG1_CNTCV_LO Register

1 GTC_CFG1_CNTCV_LO Register (Offset = 8h) [reset = 0h]

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Table 14-31403. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A9 0008h**

Figure 14-10402. GTC_CFG1_CNTCV_LO Name Register

31	30	29	28	27	26	25	24
CNTCV_LO_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCV_LO_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCV_LO_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCV_LO_COUNTVALUE							
R							
X							

Table 14-31405. GTC_CFG1_CNTCV_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.9.7.1.2.7 GTC_CFG1_CNTCV_HI Register

1 GTC_CFG1_CNTCV_HI Register (Offset = Ch) [reset = 0h]

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Table 14-31406. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A9 000Ch**

Figure 14-10403. GTC_CFG1_CNTCV_HI Name Register

31	30	29	28	27	26	25	24
CNTCV_HI_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCV_HI_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCV_HI_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCV_HI_COUNTVALUE							
R							
X							

Table 14-31408. GTC_CFG1_CNTCV_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.9.7.1.2.8 GTC_CFG1_CNTFID0 Register

1 GTC_CFG1_CNTFID0 Register (Offset = 20h) [reset = 0h]

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Table 14-31409. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A9 0020h**

Figure 14-10404. GTC_CFG1_CNTFID0 Name Register

31	30	29	28	27	26	25	24
CNTFID0_FREQVALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTFID0_FREQVALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTFID0_FREQVALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTFID0_FREQVALUE							
R/W							
0h							

Table 14-31411. GTC_CFG1_CNTFID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID0_FREQVALUE	R/W	0h	Indicates the base update frequency of the System Counter in Hz. Reset Source: mod_por_rst_n

14.9.7.1.2.9 GTC_CFG1_CNTFID1 Register

1 GTC_CFG1_CNTFID1 Register (Offset = 24h) [reset = 0h]

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Table 14-31412. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00A9 0024h**

Figure 14-10405. GTC_CFG1_CNTFID1 Name Register

31	30	29	28	27	26	25	24
CNTFID1_FREQVALUE							
R							
0h							
23	22	21	20	19	18	17	16
CNTFID1_FREQVALUE							
R							
0h							
15	14	13	12	11	10	9	8
CNTFID1_FREQVALUE							
R							
0h							
7	6	5	4	3	2	1	0
CNTFID1_FREQVALUE							
R							
0h							

Table 14-31414. GTC_CFG1_CNTFID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID1_FREQVALUE	R	0h	Frequency table end indicator Reset Source: mod_por_rst_n

14.9.7.1.2.10 GTC_CFG2_CNTCVS_LO Register

1 GTC_CFG2_CNTCVS_LO Register (Offset = 0h) [reset = 0h]

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Table 14-31415. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00AA 0000h**

Figure 14-10406. GTC_CFG2_CNTCVS_LO Name Register

31	30	29	28	27	26	25	24
CNTCVS_LO_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCVS_LO_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCVS_LO_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCVS_LO_COUNTVALUE							
R							
X							

Table 14-31417. GTC_CFG2_CNTCVS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCVS_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.9.7.1.2.11 GTC_CFG2_CNTCVS_HI Register

1 GTC_CFG2_CNTCVS_HI Register (Offset = 4h) [reset = 0h]

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Table 14-31418. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00AA 0004h**

Figure 14-10407. GTC_CFG2_CNTCVS_HI Name Register

31	30	29	28	27	26	25	24
CNTCVS_HI_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCVS_HI_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCVS_HI_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCVS_HI_COUNTVALUE							
R							
X							

Table 14-31420. GTC_CFG2_CNTCVS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCVS_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.9.7.1.2.12 GTC_CFG3_CNTTIDR Register

1 GTC_CFG3_CNTTIDR Register (Offset = 8h) [reset = 0h]

Return to Summary Table

Table 14-31421. Instance Table

Instance Name	Physical Address
WKUP_GTC0	**00AB 0008h**

Figure 14-10408. GTC_CFG3_CNTTIDR Name Register

31	30	29	28	27	26	25	24
CNTTIDR_FRAME7				CNTTIDR_FRAME6			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
CNTTIDR_FRAME5				CNTTIDR_FRAME4			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
CNTTIDR_FRAME3				CNTTIDR_FRAME2			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
CNTTIDR_FRAME1				CNTTIDR_FRAME0			
R				R			
0h				0h			

Table 14-31423. GTC_CFG3_CNTTIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CNTTIDR_FRAME7	R	0h	Indicates the features of timer frame7. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
27:24	CNTTIDR_FRAME6	R	0h	Indicates the features of timer frame6. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
23:20	CNTTIDR_FRAME5	R	0h	Indicates the features of timer frame5. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
19:16	CNTTIDR_FRAME4	R	0h	Indicates the features of timer frame4. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
15:12	CNTTIDR_FRAME3	R	0h	Indicates the features of timer frame3. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
11:8	CNTTIDR_FRAME2	R	0h	Indicates the features of timer frame2. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
7:4	CNTTIDR_FRAME1	R	0h	Indicates the features of timer frame1. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

Table 14-31423. GTC_CFG3_CNTTIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CNTTIDR_FRAME0	R	0h	Indicates the features of timer frame0. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

14.9.7.2 RTI_CFG1

RTI_CFG1

14.9.7.2.1 RTI_CFG1 Summaries

RTI_CFG1 Summaries

Table 14-31424. RTI Registers, Base Address=0E04 0000h, Length=256

Offset	Length	Register Name	RTI4 Physical Address	RTI0 Physical Address	RTI1 Physical Address
0h	32	RTI_RTIGCTRL	0488 0000h	0E00 0000h	0E01 0000h
4h	32	RTI_RTITBCTRL	0488 0004h	0E00 0004h	0E01 0004h
8h	32	RTI_RTICAPCTRL	0488 0008h	0E00 0008h	0E01 0008h
Ch	32	RTI_RTICOMPCTRL	0488 000Ch	0E00 000Ch	0E01 000Ch
10h	32	RTI_RTIFRC0	0488 0010h	0E00 0010h	0E01 0010h
14h	32	RTI_RTIUC0	0488 0014h	0E00 0014h	0E01 0014h
18h	32	RTI_RTICPUC0	0488 0018h	0E00 0018h	0E01 0018h
20h	32	RTI_RTICAFRC0	0488 0020h	0E00 0020h	0E01 0020h
24h	32	RTI_RTICAUC0	0488 0024h	0E00 0024h	0E01 0024h
30h	32	RTI_RTIFRC1	0488 0030h	0E00 0030h	0E01 0030h
34h	32	RTI_RTIUC1	0488 0034h	0E00 0034h	0E01 0034h
38h	32	RTI_RTICPUC1	0488 0038h	0E00 0038h	0E01 0038h
40h	32	RTI_RTICAFRC1	0488 0040h	0E00 0040h	0E01 0040h
44h	32	RTI_RTICAUC1	0488 0044h	0E00 0044h	0E01 0044h
50h	32	RTI_RTICOMP0	0488 0050h	0E00 0050h	0E01 0050h
54h	32	RTI_RTIUDCP0	0488 0054h	0E00 0054h	0E01 0054h
58h	32	RTI_RTICOMP1	0488 0058h	0E00 0058h	0E01 0058h
5Ch	32	RTI_RTIUDCP1	0488 005Ch	0E00 005Ch	0E01 005Ch
60h	32	RTI_RTICOMP2	0488 0060h	0E00 0060h	0E01 0060h
64h	32	RTI_RTIUDCP2	0488 0064h	0E00 0064h	0E01 0064h
68h	32	RTI_RTICOMP3	0488 0068h	0E00 0068h	0E01 0068h
6Ch	32	RTI_RTIUDCP3	0488 006Ch	0E00 006Ch	0E01 006Ch
70h	32	RTI_RTITBLCOMP	0488 0070h	0E00 0070h	0E01 0070h
74h	32	RTI_RTITBHCOMP	0488 0074h	0E00 0074h	0E01 0074h
80h	32	RTI_RTISETINT	0488 0080h	0E00 0080h	0E01 0080h
84h	32	RTI_RTICLEARINT	0488 0084h	0E00 0084h	0E01 0084h
88h	32	RTI_RTIINTFLAG	0488 0088h	0E00 0088h	0E01 0088h
90h	32	RTI_RTIDWDCTRL	0488 0090h	0E00 0090h	0E01 0090h
94h	32	RTI_RTIDWDPRLD	0488 0094h	0E00 0094h	0E01 0094h
98h	32	RTI_RTIWDSTATUS	0488 0098h	0E00 0098h	0E01 0098h
9Ch	32	RTI_RTIWDKEY	0488 009Ch	0E00 009Ch	0E01 009Ch
A0h	32	RTI_RTIDWDCNTR	0488 00A0h	0E00 00A0h	0E01 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	0488 00A4h	0E00 00A4h	0E01 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	0488 00A8h	0E00 00A8h	0E01 00A8h
ACh	32	RTI_RTIINTCLRENABLE	0488 00ACh	0E00 00ACh	0E01 00ACh
B0h	32	RTI_RTICOMP0CLR	0488 00B0h	0E00 00B0h	0E01 00B0h
B4h	32	RTI_RTICOMP1CLR	0488 00B4h	0E00 00B4h	0E01 00B4h
B8h	32	RTI_RTICOMP2CLR	0488 00B8h	0E00 00B8h	0E01 00B8h

Table 14-31424. RTI Registers, Base Address=0E04 0000h, Length=256 (continued)

Offset	Length	Register Name	RTI4 Physical Address	RTI0 Physical Address	RTI1 Physical Address
BCh	32	RTI_RTICOMP3CLR	0488 00BCh	0E00 00BCh	0E01 00BCh

Table 14-31425. RTI Registers, Base Address=0E04 0000h, Length=256

Offset	Length	Register Name	RTI2 Physical Address	RTI3 Physical Address	MCU_RTI0 Physical Address
0h	32	RTI_RTIGCTRL	0E02 0000h	0E03 0000h	0E04 0000h
4h	32	RTI_RTITBCTRL	0E02 0004h	0E03 0004h	0E04 0004h
8h	32	RTI_RTICAPCTRL	0E02 0008h	0E03 0008h	0E04 0008h
Ch	32	RTI_RTICOMPCTRL	0E02 000Ch	0E03 000Ch	0E04 000Ch
10h	32	RTI_RTIFRC0	0E02 0010h	0E03 0010h	0E04 0010h
14h	32	RTI_RTIUC0	0E02 0014h	0E03 0014h	0E04 0014h
18h	32	RTI_RTICPUC0	0E02 0018h	0E03 0018h	0E04 0018h
20h	32	RTI_RTICAFRC0	0E02 0020h	0E03 0020h	0E04 0020h
24h	32	RTI_RTICAUC0	0E02 0024h	0E03 0024h	0E04 0024h
30h	32	RTI_RTIFRC1	0E02 0030h	0E03 0030h	0E04 0030h
34h	32	RTI_RTIUC1	0E02 0034h	0E03 0034h	0E04 0034h
38h	32	RTI_RTICPUC1	0E02 0038h	0E03 0038h	0E04 0038h
40h	32	RTI_RTICAFRC1	0E02 0040h	0E03 0040h	0E04 0040h
44h	32	RTI_RTICAUC1	0E02 0044h	0E03 0044h	0E04 0044h
50h	32	RTI_RTICOMP0	0E02 0050h	0E03 0050h	0E04 0050h
54h	32	RTI_RTIUDCP0	0E02 0054h	0E03 0054h	0E04 0054h
58h	32	RTI_RTICOMP1	0E02 0058h	0E03 0058h	0E04 0058h
5Ch	32	RTI_RTIUDCP1	0E02 005Ch	0E03 005Ch	0E04 005Ch
60h	32	RTI_RTICOMP2	0E02 0060h	0E03 0060h	0E04 0060h
64h	32	RTI_RTIUDCP2	0E02 0064h	0E03 0064h	0E04 0064h
68h	32	RTI_RTICOMP3	0E02 0068h	0E03 0068h	0E04 0068h
6Ch	32	RTI_RTIUDCP3	0E02 006Ch	0E03 006Ch	0E04 006Ch
70h	32	RTI_RTITBLCOMP	0E02 0070h	0E03 0070h	0E04 0070h
74h	32	RTI_RTITBHCOMP	0E02 0074h	0E03 0074h	0E04 0074h
80h	32	RTI_RTISETINT	0E02 0080h	0E03 0080h	0E04 0080h
84h	32	RTI_RTICLEARINT	0E02 0084h	0E03 0084h	0E04 0084h
88h	32	RTI_RTIINTFLAG	0E02 0088h	0E03 0088h	0E04 0088h
90h	32	RTI_RTIDWDCTRL	0E02 0090h	0E03 0090h	0E04 0090h
94h	32	RTI_RTIDWDPRLD	0E02 0094h	0E03 0094h	0E04 0094h
98h	32	RTI_RTIWDSTATUS	0E02 0098h	0E03 0098h	0E04 0098h
9Ch	32	RTI_RTIWDKEY	0E02 009Ch	0E03 009Ch	0E04 009Ch
A0h	32	RTI_RTIDWDCNTR	0E02 00A0h	0E03 00A0h	0E04 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	0E02 00A4h	0E03 00A4h	0E04 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	0E02 00A8h	0E03 00A8h	0E04 00A8h
ACh	32	RTI_RTIINTCLRENABLE	0E02 00ACh	0E03 00ACh	0E04 00ACh
B0h	32	RTI_RTICOMP0CLR	0E02 00B0h	0E03 00B0h	0E04 00B0h
B4h	32	RTI_RTICOMP1CLR	0E02 00B4h	0E03 00B4h	0E04 00B4h
B8h	32	RTI_RTICOMP2CLR	0E02 00B8h	0E03 00B8h	0E04 00B8h
BCh	32	RTI_RTICOMP3CLR	0E02 00BCh	0E03 00BCh	0E04 00BCh

Table 14-31426. RTI Registers, Base Address=0E04 0000h, Length=256

Offset	Length	Register Name	WKUP_RTI0 Physical Address
0h	32	RTI_RTIGCTRL	2B00 0000h
4h	32	RTI_RTITBCTRL	2B00 0004h
8h	32	RTI_RTICAPCTRL	2B00 0008h
Ch	32	RTI_RTICOMPCTRL	2B00 000Ch
10h	32	RTI_RTIFRC0	2B00 0010h
14h	32	RTI_RTIUC0	2B00 0014h
18h	32	RTI_RTICPUC0	2B00 0018h
20h	32	RTI_RTICAFRC0	2B00 0020h
24h	32	RTI_RTICAUC0	2B00 0024h
30h	32	RTI_RTIFRC1	2B00 0030h
34h	32	RTI_RTIUC1	2B00 0034h
38h	32	RTI_RTICPUC1	2B00 0038h
40h	32	RTI_RTICAFRC1	2B00 0040h
44h	32	RTI_RTICAUC1	2B00 0044h
50h	32	RTI_RTICOMP0	2B00 0050h
54h	32	RTI_RTIUDCP0	2B00 0054h
58h	32	RTI_RTICOMP1	2B00 0058h
5Ch	32	RTI_RTIUDCP1	2B00 005Ch
60h	32	RTI_RTICOMP2	2B00 0060h
64h	32	RTI_RTIUDCP2	2B00 0064h
68h	32	RTI_RTICOMP3	2B00 0068h
6Ch	32	RTI_RTIUDCP3	2B00 006Ch
70h	32	RTI_RTITBLCOMP	2B00 0070h
74h	32	RTI_RTITBHCOMP	2B00 0074h
80h	32	RTI_RTISETINT	2B00 0080h
84h	32	RTI_RTICLEARINT	2B00 0084h
88h	32	RTI_RTIINTFLAG	2B00 0088h
90h	32	RTI_RTIDWDCTRL	2B00 0090h
94h	32	RTI_RTIDWDPRLD	2B00 0094h
98h	32	RTI_RTIWDSTATUS	2B00 0098h
9Ch	32	RTI_RTIWDKEY	2B00 009Ch
A0h	32	RTI_RTIDWDCNTR	2B00 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	2B00 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	2B00 00A8h
ACh	32	RTI_RTIINTCLRENABLE	2B00 00ACh
B0h	32	RTI_RTICOMP0CLR	2B00 00B0h
B4h	32	RTI_RTICOMP1CLR	2B00 00B4h
B8h	32	RTI_RTICOMP2CLR	2B00 00B8h
BCh	32	RTI_RTICOMP3CLR	2B00 00BCh

14.9.7.2.2 RTI_CFG1 Registers

RTI_CFG1 Registers

14.9.7.2.2.1 RTI_RTIGCTRL Register

1 RTI_RTIGCTRL Register (Offset = 0h) [reset = 0h]

RTI Global Control Register

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Table 14-31427. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0000h**
RTI0	**0E00 0000h**
RTI1	**0E01 0000h**
RTI2	**0E02 0000h**
RTI3	**0E03 0000h**
RTI4	**0E04 0000h**
WKUP_RTI0	**2B00 0000h**

Figure 14-10409. RTI_RTIGCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NTUSEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>COS</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CNT1EN</td><td>CNT0EN</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31429. RTI_RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

Table 14-31429. RTI_RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	NTUSEL	R/W	0h	These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode (read): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Privilege mode (write): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Reset Source: mod_g_rst_n
15	COS	R/W	0h	This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode (read): 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode (write): 0 = stop counters in debug mode 1 = continue counting in debug mode Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1	CNT1EN	R/W	0h	The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n
0	CNT0EN	R/W	0h	The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n

14.9.7.2.2.2 RTI_RTITBCTRL Register

1 RTI_RTITBCTRL Register (Offset = 4h) [reset = 0h]

RTI Timebase Control Register

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Table 14-31430. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0004h**
RTI0	**0E00 0004h**
RTI1	**0E01 0004h**
RTI2	**0E02 0004h**
RTI3	**0E03 0004h**
RTI4	**0E04 0004h**
WKUP_RTI0	**2B00 0004h**

Figure 14-10410. RTI_RTITBCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>INC</td><td>TBEXT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31432. RTI_RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	INC	R/W	0h	This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode (read): 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode (write): 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock Reset Source: mod_g_rst_n

Table 14-31432. RTI_RTITBCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TBEXT	R/W	0h	The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode (read): 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode (write): 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme Reset Source: mod_g_rst_n

14.9.7.2.2.3 RTI_RTICAPCTRL Register

1 RTI_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

RTI Capture Control Register

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Table 14-31433. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0008h**
RTI0	**0E00 0008h**
RTI1	**0E01 0008h**
RTI2	**0E02 0008h**
RTI3	**0E03 0008h**
RTI4	**0E04 0008h**
WKUP_RTI0	**2B00 0008h**

Figure 14-10411. RTI_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CAPCNTR1	CAPCNTR0
NONE						R/W	R/W
0h						0h	0h

Table 14-31435. RTI_RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CAPCNTR1	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n

Table 14-31435. RTI_RTICAPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAPCNTR0	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n

14.9.7.2.2.4 RTI_RTICOMPCTRL Register

1 RTI_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

RTI Compare Control Register

Return to Summary Table

Table 14-31436. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 000Ch**
RTI0	**0E00 000Ch**
RTI1	**0E01 000Ch**
RTI2	**0E02 000Ch**
RTI3	**0E03 000Ch**
RTI4	**0E04 000Ch**
WKUP_RTI0	**2B00 000Ch**

Figure 14-10412. RTI_RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			COMPSEL3	RESERVED			COMPSEL2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			COMPSEL1	RESERVED			COMPSEL0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-31438. RTI_RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COMPSEL3	R/W	0h	This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE	0h	Reserved

Table 14-31438. RTI_RTICOMPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	COMPSEL2	R/W	0h	This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	COMPSEL1	R/W	0h	This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	COMPSEL0	R/W	0h	This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n

14.9.7.2.2.5 RTI_RTIFRC0 Register

1 RTI_RTIFRC0 Register (Offset = 10h) [reset = 0h]

RTI Free Running Counter 0 Register

Return to Summary Table

Table 14-31439. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0010h**
RTI0	**0E00 0010h**
RTI1	**0E01 0010h**
RTI2	**0E02 0010h**
RTI3	**0E03 0010h**
RTI4	**0E04 0010h**
WKUP_RTI0	**2B00 0010h**

Figure 14-10413. RTI_RTIFRC0 Name Register

31	30	29	28	27	26	25	24
FRC0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FRC0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FRC0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRC0							
R/W							
0h							

Table 14-31441. RTI_RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Reset Source: mod_g_rst_n

14.9.7.2.2.6 RTI_RTIUC0 Register

1 RTI_RTIUC0 Register (Offset = 14h) [reset = 0h]

RTI Up Counter 0 Register

Return to Summary Table

Table 14-31442. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0014h**
RTI0	**0E00 0014h**
RTI1	**0E01 0014h**
RTI2	**0E02 0014h**
RTI3	**0E03 0014h**
RTI4	**0E04 0014h**
WKUP_RTI0	**2B00 0014h**

Figure 14-10414. RTI_RTIUC0 Name Register

31	30	29	28	27	26	25	24
UC0							
R/W							
0h							
23	22	21	20	19	18	17	16
UC0							
R/W							
0h							
15	14	13	12	11	10	9	8
UC0							
R/W							
0h							
7	6	5	4	3	2	1	0
UC0							
R/W							
0h							

Table 14-31444. RTI_RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode (read): value of the counter when the Free Running Counter 0 was read Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows. Reset Source: mod_g_rst_n

14.9.7.2.2.7 RTI_RTICPUC0 Register

1 RTI_RTICPUC0 Register (Offset = 18h) [reset = 0h]

RTI Compare Up Counter 0 Register

Return to Summary Table

Table 14-31445. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0018h**
RTI0	**0E00 0018h**
RTI1	**0E01 0018h**
RTI2	**0E02 0018h**
RTI3	**0E03 0018h**
RTI4	**0E04 0018h**
WKUP_RTI0	**2B00 0018h**

Figure 14-10415. RTI_RTICPUC0 Name Register

31	30	29	28	27	26	25	24
CPUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC0							
R/W							
0h							

Table 14-31447. RTI_RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0: fFRC0 = R-----T---I---C----L----K-- 232 If CPUC0 0: fFRC0 = ----R----T----I--C-----L---K------- CPUC0 + 1 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Reset Source: mod_g_rst_n

14.9.7.2.2.8 RTI_RTICAFRC0 Register

1 RTI_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

RTI Capture Free Running Counter 0 Register

Return to Summary Table

Table 14-31448. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0020h**
RTI0	**0E00 0020h**
RTI1	**0E01 0020h**
RTI2	**0E02 0020h**
RTI3	**0E03 0020h**
RTI4	**0E04 0020h**
WKUP_RTI0	**2B00 0020h**

Figure 14-10416. RTI_RTICAFRC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CAFRC0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CAFRC0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CAFRC0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAFRC0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31450. RTI_RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R	0h	This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 0 on a capture event Reset Source: mod_g_rst_n

14.9.7.2.2.9 RTI_RTICAUC0 Register

1 RTI_RTICAUC0 Register (Offset = 24h) [reset = 0h]

RTI Capture Up Counter 0 Register

Return to Summary Table

Table 14-31451. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0024h**
RTI0	**0E00 0024h**
RTI1	**0E01 0024h**
RTI2	**0E02 0024h**
RTI3	**0E03 0024h**
RTI4	**0E04 0024h**
WKUP_RTI0	**2B00 0024h**

Figure 14-10417. RTI_RTICAUC0 Name Register

31	30	29	28	27	26	25	24
CAUC0							
R							
0h							
23	22	21	20	19	18	17	16
CAUC0							
R							
0h							
15	14	13	12	11	10	9	8
CAUC0							
R							
0h							
7	6	5	4	3	2	1	0
CAUC0							
R							
0h							

Table 14-31453. RTI_RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R	0h	This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 0 on a capture event Reset Source: mod_g_rst_n

14.9.7.2.2.10 RTI_RTIFRC1 Register

1 RTI_RTIFRC1 Register (Offset = 30h) [reset = 0h]

RTI Free Running Counter 1 Register

Return to Summary Table

Table 14-31454. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0030h**
RTI0	**0E00 0030h**
RTI1	**0E01 0030h**
RTI2	**0E02 0030h**
RTI3	**0E03 0030h**
RTI4	**0E04 0030h**
WKUP_RTI0	**2B00 0030h**

Figure 14-10418. RTI_RTIFRC1 Name Register

31	30	29	28	27	26	25	24
FRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC1							
R/W							
0h							

Table 14-31456. RTI_RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Reset Source: mod_g_rst_n

14.9.7.2.2.11 RTI_RTIUC1 Register

1 RTI_RTIUC1 Register (Offset = 34h) [reset = 0h]

RTI Up Counter 1 Register

Return to Summary Table

Table 14-31457. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0034h**
RTI0	**0E00 0034h**
RTI1	**0E01 0034h**
RTI2	**0E02 0034h**
RTI3	**0E03 0034h**
RTI4	**0E04 0034h**
WKUP_RTI0	**2B00 0034h**

Figure 14-10419. RTI_RTIUC1 Name Register

31	30	29	28	27	26	25	24
UC1							
R/W							
0h							
23	22	21	20	19	18	17	16
UC1							
R/W							
0h							
15	14	13	12	11	10	9	8
UC1							
R/W							
0h							
7	6	5	4	3	2	1	0
UC1							
R/W							
0h							

Table 14-31459. RTI_RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode (read): value of the counter when the Free Running Counter 1 was read Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be disabled in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since UC1 has to count up until it overflows. Reset Source: mod_g_rst_n

14.9.7.2.2.12 RTI_RTICPUC1 Register

1 RTI_RTICPUC1 Register (Offset = 38h) [reset = 0h]

RTI Compare Up Counter 1 Register

Return to Summary Table

Table 14-31460. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0038h**
RTI0	**0E00 0038h**
RTI1	**0E01 0038h**
RTI2	**0E02 0038h**
RTI3	**0E03 0038h**
RTI4	**0E04 0038h**
WKUP_RTI0	**2B00 0038h**

Figure 14-10420. RTI_RTICPUC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CPUC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CPUC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CPUC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CPUC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31462. RTI_RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0: fFRC1 = R-----T---I---C----L----K-- 232 If CPUC1 0: fFRC1 = ----R----T----I--C-----L---K------- CPUC1 + 1 User and privilege mode (read): current compare value Privilege mode (write): the compare value is updated Reset Source: mod_g_rst_n

14.9.7.2.2.13 RTI_RTICAFRC1 Register

1 RTI_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

RTI Capture Free Running Counter 1 Register

Return to Summary Table

Table 14-31463. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0040h**
RTI0	**0E00 0040h**
RTI1	**0E01 0040h**
RTI2	**0E02 0040h**
RTI3	**0E03 0040h**
RTI4	**0E04 0040h**
WKUP_RTI0	**2B00 0040h**

Figure 14-10421. RTI_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24
CAFRC1							
R							
0h							
23	22	21	20	19	18	17	16
CAFRC1							
R							
0h							
15	14	13	12	11	10	9	8
CAFRC1							
R							
0h							
7	6	5	4	3	2	1	0
CAFRC1							
R							
0h							

Table 14-31465. RTI_RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R	0h	This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 1 on a capture event Reset Source: mod_g_rst_n

14.9.7.2.2.14 RTI_RTICAUC1 Register

1 RTI_RTICAUC1 Register (Offset = 44h) [reset = 0h]

RTI Capture Up Counter 1 Register

Return to Summary Table

Table 14-31466. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0044h**
RTI0	**0E00 0044h**
RTI1	**0E01 0044h**
RTI2	**0E02 0044h**
RTI3	**0E03 0044h**
RTI4	**0E04 0044h**
WKUP_RTI0	**2B00 0044h**

Figure 14-10422. RTI_RTICAUC1 Name Register

31	30	29	28	27	26	25	24
CAUC1							
R							
0h							
23	22	21	20	19	18	17	16
CAUC1							
R							
0h							
15	14	13	12	11	10	9	8
CAUC1							
R							
0h							
7	6	5	4	3	2	1	0
CAUC1							
R							
0h							

Table 14-31468. RTI_RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R	0h	This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 1 on a capture event Reset Source: mod_g_rst_n

14.9.7.2.2.15 RTI_RTICOMP0 Register

1 RTI_RTICOMP0 Register (Offset = 50h) [reset = 0h]

RTI Compare 0 Register

Return to Summary Table

Table 14-31469. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0050h**
RTI0	**0E00 0050h**
RTI1	**0E01 0050h**
RTI2	**0E02 0050h**
RTI3	**0E03 0050h**
RTI4	**0E04 0050h**
WKUP_RTI0	**2B00 0050h**

Figure 14-10423. RTI_RTICOMP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31471. RTI_RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.16 RTI_RTIUDCP0 Register

1 RTI_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

RTI Update Compare 0 Register

Return to Summary Table

Table 14-31472. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0054h**
RTI0	**0E00 0054h**
RTI1	**0E01 0054h**
RTI2	**0E02 0054h**
RTI3	**0E03 0054h**
RTI4	**0E04 0054h**
WKUP_RTI0	**2B00 0054h**

Figure 14-10424. RTI_RTIUDCP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UDCP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">UDCP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UDCP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UDCP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31474. RTI_RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 0 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.7.2.2.17 RTI_RTICOMP1 Register

1 RTI_RTICOMP1 Register (Offset = 58h) [reset = 0h]

RTI Compare 1 Register

Return to Summary Table

Table 14-31475. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0058h**
RTI0	**0E00 0058h**
RTI1	**0E01 0058h**
RTI2	**0E02 0058h**
RTI3	**0E03 0058h**
RTI4	**0E04 0058h**
WKUP_RTI0	**2B00 0058h**

Figure 14-10425. RTI_RTICOMP1 Name Register

31	30	29	28	27	26	25	24
COMP1							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1							
R/W							
0h							

Table 14-31477. RTI_RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.18 RTI_RTIUDCP1 Register

1 RTI_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

RTI Update Compare 1 Register

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Table 14-31478. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 005Ch**
RTI0	**0E00 005Ch**
RTI1	**0E01 005Ch**
RTI2	**0E02 005Ch**
RTI3	**0E03 005Ch**
RTI4	**0E04 005Ch**
WKUP_RTI0	**2B00 005Ch**

Figure 14-10426. RTI_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24
UDCP1							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP1							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP1							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP1							
R/W							
0h							

Table 14-31480. RTI_RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	This registers holds a value, which is added to the value in the compare 1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 1 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.7.2.2.19 RTI_RTICOMP2 Register

1 RTI_RTICOMP2 Register (Offset = 60h) [reset = 0h]

RTI Compare 2 Register

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Table 14-31481. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0060h**
RTI0	**0E00 0060h**
RTI1	**0E01 0060h**
RTI2	**0E02 0060h**
RTI3	**0E03 0060h**
RTI4	**0E04 0060h**
WKUP_RTI0	**2B00 0060h**

Figure 14-10427. RTI_RTICOMP2 Name Register

31	30	29	28	27	26	25	24
COMP2							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2							
R/W							
0h							

Table 14-31483. RTI_RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.20 RTI_RTIUDCP2 Register

1 RTI_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

RTI Update Compare 2 Register

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Table 14-31484. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0064h**
RTI0	**0E00 0064h**
RTI1	**0E01 0064h**
RTI2	**0E02 0064h**
RTI3	**0E03 0064h**
RTI4	**0E04 0064h**
WKUP_RTI0	**2B00 0064h**

Figure 14-10428. RTI_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24
UDCP2							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP2							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP2							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP2							
R/W							
0h							

Table 14-31486. RTI_RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 2 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.7.2.2.21 RTI_RTICOMP3 Register

1 RTI_RTICOMP3 Register (Offset = 68h) [reset = 0h]

RTI Compare 3 Register

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Table 14-31487. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0068h**
RTI0	**0E00 0068h**
RTI1	**0E01 0068h**
RTI2	**0E02 0068h**
RTI3	**0E03 0068h**
RTI4	**0E04 0068h**
WKUP_RTI0	**2B00 0068h**

Figure 14-10429. RTI_RTICOMP3 Name Register

31	30	29	28	27	26	25	24
COMP3							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3							
R/W							
0h							

Table 14-31489. RTI_RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.22 RTI_RTIUDCP3 Register

1 RTI_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

RTI Update Compare 3 Register

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Table 14-31490. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 006Ch**
RTI0	**0E00 006Ch**
RTI1	**0E01 006Ch**
RTI2	**0E02 006Ch**
RTI3	**0E03 006Ch**
RTI4	**0E04 006Ch**
WKUP_RTI0	**2B00 006Ch**

Figure 14-10430. RTI_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24
UDCP3							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP3							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP3							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP3							
R/W							
0h							

Table 14-31492. RTI_RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 3 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.7.2.2.23 RTI_RTITBLCOMP Register

1 RTI_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

RTI External Clock Timebase Low Compare Register

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Table 14-31493. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0070h**
RTI0	**0E00 0070h**
RTI1	**0E01 0070h**
RTI2	**0E02 0070h**
RTI3	**0E03 0070h**
RTI4	**0E04 0070h**
WKUP_RTI0	**2B00 0070h**

Figure 14-10431. RTI_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24
TBLCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBLCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBLCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBLCOMP							
R/W							
0h							

Table 14-31495. RTI_RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.9.7.2.2.24 RTI_RTITBHCOMP Register

1 RTI_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

RTI External Clock Timebase High Compare Register

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Table 14-31496. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0074h**
RTI0	**0E00 0074h**
RTI1	**0E01 0074h**
RTI2	**0E02 0074h**
RTI3	**0E03 0074h**
RTI4	**0E04 0074h**
WKUP_RTI0	**2B00 0074h**

Figure 14-10432. RTI_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24
TBHCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBHCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBHCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBHCOMP							
R/W							
0h							

Table 14-31498. RTI_RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.9.7.2.2.25 RTI_RTISETINT Register

1 RTI_RTISETINT Register (Offset = 80h) [reset = 0h]

RTI Set/Status Interrupt Register

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Table 14-31499. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0080h**
RTI0	**0E00 0080h**
RTI1	**0E01 0080h**
RTI2	**0E02 0080h**
RTI3	**0E03 0080h**
RTI4	**0E04 0080h**
WKUP_RTI0	**2B00 0080h**

Figure 14-10433. RTI_RTISETINT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					SETOVL1INT	SETOVL0INT	SETTBINT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				SETDMA3	SETDMA2	SETDMA1	SETDMA0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED				SETINT3	SETINT2	SETINT1	SETINT0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-31501. RTI_RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	SETOVL1INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
17	SETOVL0INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

Table 14-31501. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SETTBINT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	SETDMA3	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
10	SETDMA2	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
9	SETDMA1	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
8	SETDMA0	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	SETINT3	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
2	SETINT2	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

Table 14-31501. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETINT1	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
0	SETINT0	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

14.9.7.2.2.26 RTI_RTICLEARINT Register

1 RTI_RTICLEARINT Register (Offset = 84h) [reset = 0h]

RTI Clear/Status Interrupt Register

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Table 14-31502. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0084h**
RTI0	**0E00 0084h**
RTI1	**0E01 0084h**
RTI2	**0E02 0084h**
RTI3	**0E03 0084h**
RTI4	**0E04 0084h**
WKUP_RTI0	**2B00 0084h**

Figure 14-10434. RTI_RTICLEARINT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-31504. RTI_RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	CLEAROVL1INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

Table 14-31504. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CLEAROVL0INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
16	CLEARTBINT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	CLEARDMA3	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
10	CLEARDMA2	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
9	CLEARDMA1	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
8	CLEARDMA0	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	CLEARINT3	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

Table 14-31504. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CLEARINT2	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
1	CLEARINT1	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
0	CLEARINT0	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

14.9.7.2.2.27 RTI_RTIINTFLAG Register

1 RTI_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

RTI Interrupt Flag Register

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Table 14-31505. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0088h**
RTI0	**0E00 0088h**
RTI1	**0E01 0088h**
RTI2	**0E02 0088h**
RTI3	**0E03 0088h**
RTI4	**0E04 0088h**
WKUP_RTI0	**2B00 0088h**

Figure 14-10435. RTI_RTIINTFLAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					OVL1INT	OVL0INT	TBINT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INT3	INT2	INT1	INT0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-31507. RTI_RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	OVL1INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n

Table 14-31507. RTI_RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OVL0INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
16	TBINT	R/W1TC	0h	User and privilege mode (read): this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3	INT3	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
2	INT2	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
1	INT1	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
0	INT0	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n

14.9.7.2.2.28 RTI_RTIDWDCTRL Register

1 RTI_RTIDWDCTRL Register (Offset = 90h) [reset = 5312ACEDh]

Digital Watchdog Control Register

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Table 14-31508. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0090h**
RTI0	**0E00 0090h**
RTI1	**0E01 0090h**
RTI2	**0E02 0090h**
RTI3	**0E03 0090h**
RTI4	**0E04 0090h**
WKUP_RTI0	**2B00 0090h**

Figure 14-10436. RTI_RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24
DWDCTRL							
R/W							
5312ACEDh							
23	22	21	20	19	18	17	16
DWDCTRL							
R/W							
5312ACEDh							
15	14	13	12	11	10	9	8
DWDCTRL							
R/W							
5312ACEDh							
7	6	5	4	3	2	1	0
DWDCTRL							
R/W							
5312ACEDh							

Table 14-31510. RTI_RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	5312ACEDh	User and priviledge mode (read): 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged (enabled or disabled) Priviledge mode (write): 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged (stays enabled or disabled) Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again. Reset Source: mod_g_rst_n

14.9.7.2.2.29 RTI_RTIDWDPRLD Register

1 RTI_RTIDWDPRLD Register (Offset = 94h) [reset = FFFh]

Digital Watchdog Preload Register

Return to Summary Table

Table 14-31511. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0094h**
RTI0	**0E00 0094h**
RTI1	**0E01 0094h**
RTI2	**0E02 0094h**
RTI3	**0E03 0094h**
RTI4	**0E04 0094h**
WKUP_RTI0	**2B00 0094h**

Figure 14-10437. RTI_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				DWDPRLD			
NONE				R/W			
0h				FFFh			
7	6	5	4	3	2	1	0
DWDPRLD							
R/W							
FFFh							

Table 14-31513. RTI_RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved

Table 14-31513. RTI_RTIDWDPRLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	DWDPRLD	R/W	FFFh	User and priviledge mode (read): A read from this register in any CPU mode returns the current preload value. Priviledge mode (write): If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires. When the application services the DWD, the preload register contents are copied left- justified into the DWD down counter and it starts counting down from that value. If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = (RTIDWDPRLD+1) x 213 / RTICLK1 where: RTIDWDPRLD = 0...4095 Reset Source: mod_g_rst_n

14.9.7.2.2.30 RTI_RTIWDSTATUS Register

1 RTI_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status Register

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Table 14-31514. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0098h**
RTI0	**0E00 0098h**
RTI1	**0E01 0098h**
RTI2	**0E02 0098h**
RTI3	**0E03 0098h**
RTI4	**0E04 0098h**
WKUP_RTI0	**2B00 0098h**

Figure 14-10438. RTI_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DWWD	END	START	KEYST	DWDST	AWDST
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-31516. RTI_RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-31516. RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DWWD	R/W1TC	0h	This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode (read): 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS reg- ister except for the AWD ST flag. Clearing of the status flags will deassert the non- maskable interrupt generated due to violation of the DWWD. Reset Source: mod_g_rst_n
4	END	R/W1TC	0h	This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode (read): 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
3	START	R/W1TC	0h	This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode (read): 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
2	KEYST	R/W1TC	0h	This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode (read): 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n
1	DWDST	R/W1TC	0h	status flag and is maintained for compatibility reasons. User and priviledge mode (read): 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n

Table 14-31516. RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AWDST	R/W1TC	0h	User and priviledge mode (read): 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n

14.9.7.2.2.31 RTI_RTIWDKEY Register

1 RTI_RTIWDKEY Register (Offset = 9Ch) [reset = A35Ch]

Watchdog Key Register

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Table 14-31517. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 009Ch**
RTI0	**0E00 009Ch**
RTI1	**0E01 009Ch**
RTI2	**0E02 009Ch**
RTI3	**0E03 009Ch**
RTI4	**0E04 009Ch**
WKUP_RTI0	**2B00 009Ch**

Figure 14-10439. RTI_RTIWDKEY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDKEY							
R/W							
A35Ch							
7	6	5	4	3	2	1	0
WDKEY							
R/W							
A35Ch							

Table 14-31519. RTI_RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved

Table 14-31519. RTI_RTIWDKEY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	WDKEY	R/W	A35Ch	User and privilege mode reads are indeterminate. Privilege mode (write): A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1's. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation. Table 2. Example of a WDKEY sequence Value written to Step WDKEY Result 1 0x0A35C No Action 2 0x0A35C No Action 3 0x0E51A WDKEY is enabled for reset by next 0x0A35C 4 0x0E51A WDKEY is enabled for reset by next 0x0A35C 5 0x0E51A WDKEY is enabled for reset by next 0x0A35C 6 0x0A35C Watchdog is reset 7 0x0A35C No Action 8 0x0E51A WDKEY is enabled for reset by next 0x0A35C 9 0x0A35C Watchdog is reset 10 0x0E51A WDKEY is enabled for reset by next 0x0A35C 11 0x02345 System reset; incorrect value written to WDKEY Reset Source: mod_g_rst_n

14.9.7.2.2.32 RTI_RTIDWDCNTR Register

1 RTI_RTIDWDCNTR Register (Offset = A0h) [reset = 1FFFFFFh]

Digital Watchdog Down Counter

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Table 14-31520. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A0h**
RTI0	**0E00 00A0h**
RTI1	**0E01 00A0h**
RTI2	**0E02 00A0h**
RTI3	**0E03 00A0h**
RTI4	**0E04 00A0h**
WKUP_RTI0	**2B00 00A0h**

Figure 14-10440. RTI_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							DWDCNTR
NONE							R
0h							1FFFFFFh
23	22	21	20	19	18	17	16
DWDCNTR							
R							
1FFFFFFh							
15	14	13	12	11	10	9	8
DWDCNTR							
R							
1FFFFFFh							
7	6	5	4	3	2	1	0
DWDCNTR							
R							
1FFFFFFh							

Table 14-31522. RTI_RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:0	DWDCNTR	R	1FFFFFFh	The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode (read): Reads return the current counter value. Privilege mode (write): Writes don't have an effect. Reset Source: mod_g_rst_n

14.9.7.2.2.33 RTI_RTIDWWDRXNCTRL Register

1 RTI_RTIDWWDRXNCTRL Register (Offset = A4h) [reset = 5h]

Digital Windowed Watchdog Reaction Control

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Table 14-31523. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A4h**
RTI0	**0E00 00A4h**
RTI1	**0E01 00A4h**
RTI2	**0E02 00A4h**
RTI3	**0E03 00A4h**
RTI4	**0E04 00A4h**
WKUP_RTI0	**2B00 00A4h**

Figure 14-10441. RTI_RTIDWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				WWDRXN			
NONE				R/W			
0h				5h			

Table 14-31525. RTI_RTIDWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

Table 14-31525. RTI_RTIDWWDRXNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WWDRXN	R/W	5h	User and privilege mode (read), privileged mode (write): 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.9.7.2.2.34 RTI_RTIDWWDSIZECTRL Register

1 RTI_RTIDWWDSIZECTRL Register (Offset = A8h) [reset = 5h]

Digital Windowed Watchdog Window Size Control

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Table 14-31526. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A8h**
RTI0	**0E00 00A8h**
RTI1	**0E01 00A8h**
RTI2	**0E02 00A8h**
RTI3	**0E03 00A8h**
RTI4	**0E04 00A8h**
WKUP_RTI0	**2B00 00A8h**

Figure 14-10442. RTI_RTIDWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24
WWDSIZE							
R/W							
5h							
23	22	21	20	19	18	17	16
WWDSIZE							
R/W							
5h							
15	14	13	12	11	10	9	8
WWDSIZE							
R/W							
5h							
7	6	5	4	3	2	1	0
WWDSIZE							
R/W							
5h							

Table 14-31528. RTI_RTIDWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	5h	User and privilege mode (read), privileged mode (write): Table 3. Windowed Watchdog Window Size Configuration Value written to WWDSIZE Window Size 0x00000005 100% (The functionality is the same as the standard time-out digital watchdog.) 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other 3.125% value Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.9.7.2.2.35 RTI_RTIINTCLRENABLE Register

1 RTI_RTIINTCLRENABLE Register (Offset = ACh) [reset = 5050505h]

RTI Compare Interrupt Clear Enable Register

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Table 14-31529. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00ACh**
RTI0	**0E00 00ACh**
RTI1	**0E01 00ACh**
RTI2	**0E02 00ACh**
RTI3	**0E03 00ACh**
RTI4	**0E04 00ACh**
WKUP_RTI0	**2B00 00ACh**

Figure 14-10443. RTI_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED				INTCLRENABLE3			
NONE				R/W			
0h				5h			
23	22	21	20	19	18	17	16
RESERVED				INTCLRENABLE2			
NONE				R/W			
0h				5h			
15	14	13	12	11	10	9	8
RESERVED				INTCLRENABLE1			
NONE				R/W			
0h				5h			
7	6	5	4	3	2	1	0
RESERVED				INTCLRENABLE0			
NONE				R/W			
0h				5h			

Table 14-31531. RTI_RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	INTCLRENABLE3	R/W	5h	Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt. Reset Source: mod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved

Table 14-31531. RTI_RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	INTCLRENABLE2	R/W	5h	Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt. Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	INTCLRENABLE1	R/W	5h	Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt. Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	INTCLRENABLE0	R/W	5h	Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt. Note: Hook-up of Compare Interrupt to a device pin The RTI module generates up to 4 compare interrupts. The connection between one or more of these compare interrupt(s) to a device pin is completely device-dependent. Refer to the device datasheet to identify the actual pin(s) that connects to the compare interrupt(s). Reset Source: mod_g_rst_n

14.9.7.2.2.36 RTI_RTICOMP0CLR Register

1 RTI_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

RTI Compare 0 Clear Register

Return to Summary Table

Table 14-31532. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00B0h**
RTI0	**0E00 00B0h**
RTI1	**0E01 00B0h**
RTI2	**0E02 00B0h**
RTI3	**0E03 00B0h**
RTI4	**0E04 00B0h**
WKUP_RTI0	**2B00 00B0h**

Figure 14-10444. RTI_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24
COMP0CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP0CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP0CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP0CLR							
R/W							
0h							

Table 14-31534. RTI_RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.37 RTI_RTICOMP1CLR Register

1 RTI_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

RTI Compare 1 Clear Register

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Table 14-31535. Instance Table

Instance Name	Physical Address
MCU_RTI0	0488 00B4h
RTI0	0E00 00B4h
RTI1	0E01 00B4h
RTI2	0E02 00B4h
RTI3	0E03 00B4h
RTI4	0E04 00B4h
WKUP_RTI0	2B00 00B4h

Figure 14-10445. RTI_RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24
COMP1CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1CLR							
R/W							
0h							

Table 14-31537. RTI_RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 1 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.38 RTI_RTICOMP2CLR Register

1 RTI_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

RTI Compare 2 Clear Register

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Table 14-31538. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00B8h**
RTI0	**0E00 00B8h**
RTI1	**0E01 00B8h**
RTI2	**0E02 00B8h**
RTI3	**0E03 00B8h**
RTI4	**0E04 00B8h**
WKUP_RTI0	**2B00 00B8h**

Figure 14-10446. RTI_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24
COMP2CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2CLR							
R/W							
0h							

Table 14-31540. RTI_RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 2 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.2.2.39 RTI_RTICOMP3CLR Register

1 RTI_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

RTI Compare 3 Clear Register

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Table 14-31541. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00BCh**
RTI0	**0E00 00BCh**
RTI1	**0E01 00BCh**
RTI2	**0E02 00BCh**
RTI3	**0E03 00BCh**
RTI4	**0E04 00BCh**
WKUP_RTI0	**2B00 00BCh**

Figure 14-10447. RTI_RTICOMP3CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMP3CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMP3CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMP3CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP3CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31543. RTI_RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 3 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.7.3 rtcss

rtcss

14.9.7.3.1 rtcss Summaries

rtcss Summaries

Table 14-31544. RTC Registers, Base Address=2B1F 0000h, Length=128

Offset	Length	Register Name	WKUP_rtcss0 Physical Address
0h	32	RTC_MOD_VER	2B1F 0000h
4h	32	RTC_SUB_S_CNT	2B1F 0004h
8h	32	RTC_S_CNT_LSW	2B1F 0008h
Ch	32	RTC_S_CNT_MSW	2B1F 000Ch
10h	32	RTC_COMP	2B1F 0010h
18h	32	RTC_OFF_ON_S_CNT_LSW	2B1F 0018h
1Ch	32	RTC_OFF_ON_S_CNT_MSW	2B1F 001Ch
20h	32	RTC_ON_OFF_S_CNT_LSW	2B1F 0020h
24h	32	RTC_ON_OFF_S_CNT_MSW	2B1F 0024h
28h	32	RTC_DEBOUNCE	2B1F 0028h
2Ch	32	RTC_ANALOG	2B1F 002Ch
30h	32	RTC_SCRATCH0_J	2B1F 0030h + formula
50h	32	RTC_GENRAL_CTL	2B1F 0050h
54h	32	RTC_IRQSTATUS_RAW_SYS	2B1F 0054h
58h	32	RTC_IRQSTATUS_SYS	2B1F 0058h
5Ch	32	RTC_IRQENABLE_SET_SYS	2B1F 005Ch
60h	32	RTC_IRQENABLE_CLR_SYS	2B1F 0060h
68h	32	RTC_SYNCPEND	2B1F 0068h
70h	32	RTC_KICK0	2B1F 0070h
74h	32	RTC_KICK1	2B1F 0074h

14.9.7.3.2 rtcss Registers

rtcss Registers

14.9.7.3.2.1 RTC_MOD_VER Register

1 RTC_MOD_VER Register (Offset = 0h) [reset = 68C00101h]

The Module and Version Register identifies the module identifier and revision of the RTC module.

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Table 14-31545. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0000h**

Figure 14-10448. RTC_MOD_VER Name Register

31	30	29	28	27	26	25	24
MODULE_ID							
R							
68C0h							
23	22	21	20	19	18	17	16
MODULE_ID							
R							
68C0h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REVISION		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		1h					

Table 14-31547. RTC_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	68C0h	RTC module ID.
15:11	RTL_VERSION	R	0h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	1h	Minor Revision.

14.9.7.3.2.2 RTC_SUB_S_CNT Register

1 RTC_SUB_S_CNT Register (Offset = 4h) [reset = 0h]

This register counts the 32768 Hz clock events

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Table 14-31548. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0004h**

Figure 14-10449. RTC_SUB_S_CNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED	SUB_S_CNT						
NONE	R/W						
0h	0h						

7	6	5	4	3	2	1	0
SUB_S_CNT							
R/W							
0h							

Table 14-31550. RTC_SUB_S_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:0	SUB_S_CNT	R/W	0h	This counts the 32768 Hz clock events to achive 1 sec event for the sec counter, rollvers after 0x7fff or 1 Sec running on 32768Hz

14.9.7.3.2.3 RTC_S_CNT_LSW Register

1 RTC_S_CNT_LSW Register (Offset = 8h) [reset = 0h]

The lower word of the seconds counter

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Table 14-31551. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0008h**

Figure 14-10450. RTC_S_CNT_LSW Name Register

31	30	29	28	27	26	25	24
S_CNT_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
S_CNT_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
S_CNT_LSW							
R/W							
0h							
7	6	5	4	3	2	1	0
S_CNT_LSW							
R/W							
0h							

Table 14-31553. RTC_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	S_CNT_LSW	R/W	0h	This counts the 1 sec events, it is the lower 32 bits of the 48 bit counter, 1 = 1 Seconds, 2 = 2 Seconds, N = N Seconds

14.9.7.3.2.4 RTC_S_CNT_MSW Register

1 RTC_S_CNT_MSW Register (Offset = Ch) [reset = 0h]

The upper word of the seconds counter

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Table 14-31554. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 000Ch**

Figure 14-10451. RTC_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
S_CNT_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
S_CNT_MSW							
R/W							
0h							

Table 14-31556. RTC_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	S_CNT_MSW	R/W	0h	This counts the 1 sec events, it is the upper 16 bits of the 48 bit counter

14.9.7.3.2.5 RTC_COMP Register

1 RTC_COMP Register (Offset = 10h) [reset = 0h]

This register used to program the value of the 32768 periods to be added to the 32768 counter every 4096 Secs. This is used to compensate the oscillator drift.

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Table 14-31557. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0010h**

Figure 14-10452. RTC_COMP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MSB_COMP							
R/W							
0h							
7	6	5	4	3	2	1	0
LSB_COMP							
R/W							
0h							

Table 14-31559. RTC_COMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MSB_COMP	R/W	0h	Indicates number of 32-kHz periods to be added into the 32-kHz counter every 4096 Secs, twos complement That means that to add one 32-kHz oscillator period every hour, the SW must write FFFF into COMP_MSB and COMP_LSB. To remove one 32-kHz oscillator period every hour, the SW must write 0001 into RTC_COMP_MSB and RTC_COMP_LSB. The 7FFF value is forbidden.
7:0	LSB_COMP	R/W	0h	Indicates number of 32-kHz periods to be added into the 32-kHz counter every 4096 Secs, twos complement That means that to add one 32-kHz oscillator period every hour, the SW must write FFFF into COMP_MSB and COMP_LSB. To remove one 32-kHz oscillator period every hour, the SW must write 0001 into RTC_COMP_MSB and RTC_COMP_LSB. The 7FFF value is forbidden.

14.9.7.3.2.6 RTC_OFF_ON_S_CNT_LSW Register

1 RTC_OFF_ON_S_CNT_LSW Register (Offset = 18h) [reset = 1h]

This register defines the OFF to ON time event

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Table 14-31560. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0018h**

Figure 14-10453. RTC_OFF_ON_S_CNT_LSW Name Register

31	30	29	28	27	26	25	24
OFF_ON_S_CNT_LSW							
R/W							
1h							
23	22	21	20	19	18	17	16
OFF_ON_S_CNT_LSW							
R/W							
1h							
15	14	13	12	11	10	9	8
OFF_ON_S_CNT_LSW							
R/W							
1h							
7	6	5	4	3	2	1	0
OFF_ON_S_CNT_LSW							
R/W							
1h							

Table 14-31562. RTC_OFF_ON_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OFF_ON_S_CNT_LSW	R/W	1h	The lower word of the OFF to ON time

14.9.7.3.2.7 RTC_OFF_ON_S_CNT_MSW Register

1 RTC_OFF_ON_S_CNT_MSW Register (Offset = 1Ch) [reset = 8000h]

This register defines the OFF to ON time event

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Table 14-31563. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 001Ch**

Figure 14-10454. RTC_OFF_ON_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFF_ON_S_CNT_MSW							
R/W							
8000h							
7	6	5	4	3	2	1	0
OFF_ON_S_CNT_MSW							
R/W							
8000h							

Table 14-31565. RTC_OFF_ON_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFF_ON_S_CNT_MSW	R/W	8000h	The

14.9.7.3.2.8 RTC_ON_OFF_S_CNT_LSW Register

1 RTC_ON_OFF_S_CNT_LSW Register (Offset = 20h) [reset = 1h]

This register defines the ON to OFF time event

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Table 14-31566. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0020h**

Figure 14-10455. RTC_ON_OFF_S_CNT_LSW Name Register

31	30	29	28	27	26	25	24
ON_OFF_S_CNT_LSW							
R/W							
1h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ON_OFF_S_CNT_LSW							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ON_OFF_S_CNT_LSW							
R/W							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ON_OFF_S_CNT_LSW							
R/W							
1h							

Table 14-31568. RTC_ON_OFF_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ON_OFF_S_CNT_LSW	R/W	1h	The

14.9.7.3.2.9 RTC_ON_OFF_S_CNT_MSW Register

1 RTC_ON_OFF_S_CNT_MSW Register (Offset = 24h) [reset = 8000h]

This register defines the ON to OFF time event

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Table 14-31569. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0024h**

Figure 14-10456. RTC_ON_OFF_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ON_OFF_S_CNT_MSW							
R/W							
8000h							
7	6	5	4	3	2	1	0
ON_OFF_S_CNT_MSW							
R/W							
8000h							

Table 14-31571. RTC_ON_OFF_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ON_OFF_S_CNT_MSW	R/W	8000h	The

14.9.7.3.2.10 RTC_DEBOUNCE Register

1 RTC_DEBOUNCE Register (Offset = 28h) [reset = 0h]

The Debounce register defines the debounce timer useing the 32768 Hz clock. It allows choosing the timing or the accuracy of

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Table 14-31572. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0028h**

Figure 14-10457. RTC_DEBOUNCE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEBOUNCE							
R/W							
0h							

Table 14-31574. RTC_DEBOUNCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEBOUNCE	R/W	0h	Debounce time 0 debounce time is 30.52 uS N debounce time is 30.52us*(N+1)

14.9.7.3.2.11 RTC_ANALOG Register

1 RTC_ANALOG Register (Offset = 2Ch) [reset = 0h]

This register goes to the Analog Block

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Table 14-31575. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 002Ch

Figure 14-10458. RTC_ANALOG Name Register

31	30	29	28	27	26	25	24
ANALOG							
R/W							
0h							
23	22	21	20	19	18	17	16
ANALOG							
R/W							
0h							
15	14	13	12	11	10	9	8
ANALOG							
R/W							
0h							
7	6	5	4	3	2	1	0
ANALOG							
R/W							
0h							

Table 14-31577. RTC_ANALOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ANALOG	R/W	0h	Analog Configuration MMR

14.9.7.3.2.12 RTC_SCRATCH0_j Register

1 RTC_SCRATCH0_j Register (Offset = 30h + formula) [reset = 0h]

The Scratch Storage Registers can be used to hold information in the battery backuped domain while the device is powered down.

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Offset = 30h + (j * 4h); where j = 0 to 7d

Table 14-31578. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0030h + formula**

Figure 14-10459. RTC_SCRATCH0_j Name Register

31	30	29	28	27	26	25	24
SCRATCH0							
R/W							
X							
23	22	21	20	19	18	17	16
SCRATCH0							
R/W							
X							
15	14	13	12	11	10	9	8
SCRATCH0							
R/W							
X							
7	6	5	4	3	2	1	0
SCRATCH0							
R/W							
X							

Table 14-31580. RTC_SCRATCH0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SCRATCH0	R/W	X	The scratch0 holds data in the battery backed domain for use by the device when powered on. This would typically be used to store signatures other information of similar ilk.

14.9.7.3.2.13 RTC_GENRAL_CTL Register

1 RTC_GENRAL_CTL Register (Offset = 50h) [reset = 0h]

This is the main RTC control register

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Table 14-31581. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0050h**

Figure 14-10460. RTC_GENRAL_CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CNT_FMODE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>UNLOCK</td><td>RESERVED</td><td>O32K_OSC_DEP_EN</td><td colspan="3">RESERVED</td><td>SW_OFF</td><td>PWR_OFF_EN</td></tr>
<tr><td>R</td><td>NONE</td><td>R/W</td><td colspan="3">NONE</td><td>W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>X</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">WKUP_DB_EN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">WKUP_POL</td><td colspan="4">WKUP_EN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-31583. RTC_GENRAL_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CNT_FMODE	R/W	0h	This defines which read freeze mode is enabled, 10 = S_CNT_LSW When SW reads S_CNT_LSW it will snap S_CNT_MSW 01 = SUB_S_CNT When SW reads SUB_S_CNT it will snap S_CNT_MSW and S_CNT_LSW 00 = Disable
23	UNLOCK	R	0h	The status of the UNLOCKED state, 1 = UnLocked 0 = Locked
22	RESERVED	NONE	0h	Reserved
21	O32K_OSC_DEP_EN	R/W	0h	This controls if a high to low transition dependence is required before the CORE domain can read or write the ON domain, 1 = Enable 0 = Disable
20:18	RESERVED	NONE	0h	Reserved
17	SW_OFF	W	X	The SW can issue a ON_OFF event, Wrt 1 for OFF event Wrt 0 has no effect, The OFF event will occur within 31uS and relock the core
16	PWR_OFF_EN	R/W	0h	This allows the PMIC_ENABLE to go from a ON to OFF state by SW or ON_OFF event
15:12	RESERVED	NONE	0h	Reserved
11:8	WKUP_DB_EN	R/W	0h	External Wakeup Debounce Enable 1 = Enable 0 = Disable

Table 14-31583. RTC_GENRAL_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	WKUP_POL	R/W	0h	External Wakeup Polarity 1 = Active High = Active Low
3:0	WKUP_EN	R/W	0h	External Wakeup Enable 1 = Enable 0 = Disable

14.9.7.3.2.14 RTC_IRQSTATUS_RAW_SYS Register

1 RTC_IRQSTATUS_RAW_SYS Register (Offset = 54h) [reset = 0h]

Interrupt Raw Status Register

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Table 14-31584. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0054h**

Figure 14-10461. RTC_IRQSTATUS_RAW_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EVENT_OFF_ON	EVENT_ON_OFF
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31586. RTC_IRQSTATUS_RAW_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EVENT_OFF_ON	R/W1TS	0h	Raw status of OFF_ON interrupt for event_off_on. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
0	EVENT_ON_OFF	R/W1TS	0h	Raw status of ON_OFF interrupt for event_on_off. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

14.9.7.3.2.15 RTC_IRQSTATUS_SYS Register

1 RTC_IRQSTATUS_SYS Register (Offset = 58h) [reset = 0h]

The EXT_WAKEUP events are level-sensitive and not edge-sensitive. When debounce is enabled, clearing an EXT_WAKEUP event may have no effect because the interrupt triggers again immediately. See the Interrupt Service Routine section of the Programming Usage Guide.

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Table 14-31587. Instance Table

Instance Name	**Physical Address**
WKUP_RTCSS0	**2B1F 0058h**

Figure 14-10462. RTC_IRQSTATUS_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EVENT_OFF_ON	EVENT_ON_OFF
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-31589. RTC_IRQSTATUS_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EVENT_OFF_ON	R/W1TC	0h	Enabled status of OFF_ON interrupt for event_off_on. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
0	EVENT_ON_OFF	R/W1TC	0h	Enabled status of ON_OFF interrupt for event_on_off. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

14.9.7.3.2.16 RTC_IRQENABLE_SET_SYS Register

1 RTC_IRQENABLE_SET_SYS Register (Offset = 5Ch) [reset = 0h]

Interrupt Enable Set Register

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Table 14-31590. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 005Ch

Figure 14-10463. RTC_IRQENABLE_SET_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EN_EVENT_OFF_ON	EN_EVENT_ON_OFF
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-31592. RTC_IRQENABLE_SET_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EN_EVENT_OFF_ON	R/W1TS	0h	Enable set for OFF_ON interrupt for event_off_on. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	EN_EVENT_ON_OFF	R/W1TS	0h	Enable set for ON_OFF interrupt for event_on_off. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

14.9.7.3.2.17 RTC_IRQENABLE_CLR_SYS Register

1 RTC_IRQENABLE_CLR_SYS Register (Offset = 60h) [reset = 0h]

Interrupt Enable Clear Register

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Table 14-31593. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0060h**

Figure 14-10464. RTC_IRQENABLE_CLR_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EN_EVENT_OFF_ON	EN_EVENT_ON_OFF
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-31595. RTC_IRQENABLE_CLR_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EN_EVENT_OFF_ON	R/W1TC	0h	Enable clear for OFF_ON interrupt for event_off_on. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	EN_EVENT_ON_OFF	R/W1TC	0h	Enable clear for ON_OFF interrupt for event_on_off. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

14.9.7.3.2.18 RTC_SYNCPEND Register

1 RTC_SYNCPEND Register (Offset = 68h) [reset = 0h]

The SW can determine status of wrt and rd access along with other status from the ON domain
This register is located in the CORE domain and provides the control and status of the MMR Sync state machine. The RELOAD_FROM_BBD bit directly controls the the MMR Sync state machine in the DIG_CORE domain and ignores the Functional Protection state machine. The RELOAD_FROM_BBD bit can be written with 1 regardless of if RTC is locked or unlocked. RTC will ignore a write of 1 to the RELOAD_FROM_BBD bit if RTC_SYNCPEND.RD_PEND is 1, or if RTC_SYNCPEND.WR_PEND is 1, or if any interrupt status bit in the RTC_IRQSTATUS_RAW_SYS register is 1.

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Table 14-31596. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0068h**

Figure 14-10465. RTC_SYNCPEND Name Register

31	30	29	28	27	26	25	24
RELOAD_FROM_BBD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PWR_ENABLE_ST
NONE							R
0h							X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WKUP_DB_ST				WRT_ERR	O32K_CLK_OBS	RD_PEND	WR_PEND
R				R/W1TC	R	R/W	R/W
X				0h	X	X	0h

Table 14-31598. RTC_SYNCPEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RELOAD_FROM_BBD	R/W	0h	The reload_from_bbd allows the registers to be reloaded from the battery backed domain. This is only allowed when the battery backed domain interface state machine is idle. Writing 1 triggers the MMR Sync to read the registers from the battery backed domain. This requires RD_PEND, WR_PEND, and all interrupts' raw status to be 0 when this is written. This operation affects the RD_PEND bit.
30:9	RESERVED	NONE	0h	Reserved
8	PWR_ENABLE_ST	R	X	The SW can read the state of PIMIC_ENABLE pin, this is raw state
7:4	WKUP_DB_ST	R	X	The SW can read the state of EXT_WAKEUP pins, this is raw state

Table 14-31598. RTC_SYNCPEND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	WRT_ERR	R/W1TC	0h	Write Error Condition Wrt 1 to Clr Set when SW tries to Wrt when RTL is LOCKED or Wrt when RD_PEND is set 0 `Not Occurred` 1 `Occurred`
2	O32K_CLK_OBS	R	X	The SW can read the state of the main 32k clock
1	RD_PEND	R/W	X	Status of synchronization from ON Domain after CORE reset or RELOAD_FROM_BBD 0 `Completed` 1 `Pending or active`
0	WR_PEND	R/W	0h	Status of synchronization to ON Domain after writing to CORE Domain over VBUS 0 `Completed` 1 `Pending or active`

14.9.7.3.2.19 RTC_KICK0 Register

1 RTC_KICK0 Register (Offset = 70h) [reset = 0h]

The written data must be 0x83e70b13 to unlock this register. It must be written before the Kick1 register. The normal procedure to re-lock the functional protection mechanism is to write 0 to this register.

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Table 14-31599. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0070h**

Figure 14-10466. RTC_KICK0 Name Register

31	30	29	28	27	26	25	24
KICK0							
W							
X							
23	22	21	20	19	18	17	16
KICK0							
W							
X							
15	14	13	12	11	10	9	8
KICK0							
W							
X							
7	6	5	4	3	2	1	0
KICK0							
W							
X							

Table 14-31601. RTC_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KICK0	W	X	Kick0 MMR, must write 0x83e70b13 to unlock this register

14.9.7.3.2.20 RTC_KICK1 Register

1 RTC_KICK1 Register (Offset = 74h) [reset = 0h]

The Kick1 register allows writing to unlock the kick1 data and the kicker mechanism to write to other MMRs. The written data must be 0x95a4f1e0 to unlock this register. If this is unlocked after the kick0 register is unlocked then the kicker mechanism is unlocked
The HOST must ensure that there is at least 60 microseconds of delay between a "new" lock state to a "new" unlock state. This should be implemented by ensuring that RTC_SYNCPEND.WR_PEND is 0 before performing the unlock writes. This is a consequence of the limitation that the functional unlock sequence must not be written while the mechanism is unlocked; if the unlock sequence is written at the wrong time, then the core domain and battery domain will not agree about their unlocked status. This will not be diagnosable in software and there is no recommended error recovery sequence for this condition.
For No Analog support, leave it unlocked.

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Table 14-31602. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	**2B1F 0074h**

Figure 14-10467. RTC_KICK1 Name Register

31	30	29	28	27	26	25	24
KICK1							
W							
X							
23	22	21	20	19	18	17	16
KICK1							
W							
X							
15	14	13	12	11	10	9	8
KICK1							
W							
X							
7	6	5	4	3	2	1	0
KICK1							
W							
X							

Table 14-31604. RTC_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KICK1	W	X	Kick1 MMR, must write 0x95a4f1e0 to unlock this register and the other MMRs

14.9.7.4 TIMER

TIMER

14.9.7.4.1 TIMER Summaries

TIMER Summaries

Table 14-31605. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER0 Physical Address	TIMER1 Physical Address	TIMER2 Physical Address
0h	32	DMTIMER1MS_TIDR	0480 0000h	0481 0000h	0482 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0480 0010h	0481 0010h	0482 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0480 0020h	0481 0020h	0482 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0480 0024h	0481 0024h	0482 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0480 0028h	0481 0028h	0482 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0480 002Ch	0481 002Ch	0482 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0480 0030h	0481 0030h	0482 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0480 0034h	0481 0034h	0482 0034h
38h	32	DMTIMER1MS_TCLR	0480 0038h	0481 0038h	0482 0038h
3Ch	32	DMTIMER1MS_TCRR	0480 003Ch	0481 003Ch	0482 003Ch
40h	32	DMTIMER1MS_TLDR	0480 0040h	0481 0040h	0482 0040h
44h	32	DMTIMER1MS_TTGR	0480 0044h	0481 0044h	0482 0044h
48h	32	DMTIMER1MS_TWPS	0480 0048h	0481 0048h	0482 0048h
4Ch	32	DMTIMER1MS_TMAR	0480 004Ch	0481 004Ch	0482 004Ch
50h	32	DMTIMER1MS_TCAR1	0480 0050h	0481 0050h	0482 0050h
54h	32	DMTIMER1MS_TSICR	0480 0054h	0481 0054h	0482 0054h
58h	32	DMTIMER1MS_TCAR2	0480 0058h	0481 0058h	0482 0058h
5Ch	32	DMTIMER1MS_TPIR	0480 005Ch	0481 005Ch	0482 005Ch
60h	32	DMTIMER1MS_TNIR	0480 0060h	0481 0060h	0482 0060h
64h	32	DMTIMER1MS_TCVR	0480 0064h	0481 0064h	0482 0064h
68h	32	DMTIMER1MS_TOCR	0480 0068h	0481 0068h	0482 0068h
6Ch	32	DMTIMER1MS_TOWR	0480 006Ch	0481 006Ch	0482 006Ch

Table 14-31606. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER3 Physical Address	TIMER4 Physical Address	TIMER5 Physical Address
0h	32	DMTIMER1MS_TIDR	0483 0000h	0240 0000h	0241 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0483 0010h	0240 0010h	0241 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0483 0020h	0240 0020h	0241 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0483 0024h	0240 0024h	0241 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0483 0028h	0240 0028h	0241 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0483 002Ch	0240 002Ch	0241 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0483 0030h	0240 0030h	0241 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0483 0034h	0240 0034h	0241 0034h
38h	32	DMTIMER1MS_TCLR	0483 0038h	0240 0038h	0241 0038h
3Ch	32	DMTIMER1MS_TCRR	0483 003Ch	0240 003Ch	0241 003Ch
40h	32	DMTIMER1MS_TLDR	0483 0040h	0240 0040h	0241 0040h

Table 14-31606. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER3 Physical Address	TIMER4 Physical Address	TIMER5 Physical Address
44h	32	DMTIMER1MS_TTGR	0483 0044h	0240 0044h	0241 0044h
48h	32	DMTIMER1MS_TWPS	0483 0048h	0240 0048h	0241 0048h
4Ch	32	DMTIMER1MS_TMAR	0483 004Ch	0240 004Ch	0241 004Ch
50h	32	DMTIMER1MS_TCAR1	0483 0050h	0240 0050h	0241 0050h
54h	32	DMTIMER1MS_TSICR	0483 0054h	0240 0054h	0241 0054h
58h	32	DMTIMER1MS_TCAR2	0483 0058h	0240 0058h	0241 0058h
5Ch	32	DMTIMER1MS_TPIR	0483 005Ch	0240 005Ch	0241 005Ch
60h	32	DMTIMER1MS_TNIR	0483 0060h	0240 0060h	0241 0060h
64h	32	DMTIMER1MS_TCVR	0483 0064h	0240 0064h	0241 0064h
68h	32	DMTIMER1MS_TOCR	0483 0068h	0240 0068h	0241 0068h
6Ch	32	DMTIMER1MS_TOWR	0483 006Ch	0240 006Ch	0241 006Ch

Table 14-31607. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER6 Physical Address	TIMER7 Physical Address	MCU_TIMER0 Physical Address
0h	32	DMTIMER1MS_TIDR	0242 0000h	0243 0000h	0244 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0242 0010h	0243 0010h	0244 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0242 0020h	0243 0020h	0244 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0242 0024h	0243 0024h	0244 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0242 0028h	0243 0028h	0244 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0242 002Ch	0243 002Ch	0244 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0242 0030h	0243 0030h	0244 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0242 0034h	0243 0034h	0244 0034h
38h	32	DMTIMER1MS_TCLR	0242 0038h	0243 0038h	0244 0038h
3Ch	32	DMTIMER1MS_TCRR	0242 003Ch	0243 003Ch	0244 003Ch
40h	32	DMTIMER1MS_TLDR	0242 0040h	0243 0040h	0244 0040h
44h	32	DMTIMER1MS_TTGR	0242 0044h	0243 0044h	0244 0044h
48h	32	DMTIMER1MS_TWPS	0242 0048h	0243 0048h	0244 0048h
4Ch	32	DMTIMER1MS_TMAR	0242 004Ch	0243 004Ch	0244 004Ch
50h	32	DMTIMER1MS_TCAR1	0242 0050h	0243 0050h	0244 0050h
54h	32	DMTIMER1MS_TSICR	0242 0054h	0243 0054h	0244 0054h
58h	32	DMTIMER1MS_TCAR2	0242 0058h	0243 0058h	0244 0058h
5Ch	32	DMTIMER1MS_TPIR	0242 005Ch	0243 005Ch	0244 005Ch
60h	32	DMTIMER1MS_TNIR	0242 0060h	0243 0060h	0244 0060h
64h	32	DMTIMER1MS_TCVR	0242 0064h	0243 0064h	0244 0064h
68h	32	DMTIMER1MS_TOCR	0242 0068h	0243 0068h	0244 0068h
6Ch	32	DMTIMER1MS_TOWR	0242 006Ch	0243 006Ch	0244 006Ch

Table 14-31608. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	MCU_TIMER1 Physical Address	MCU_TIMER2 Physical Address	MCU_TIMER3 Physical Address
0h	32	DMTIMER1MS_TIDR	0245 0000h	0246 0000h	0247 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0245 0010h	0246 0010h	0247 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0245 0020h	0246 0020h	0247 0020h

Table 14-31608. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_TIMER1 Physical Address	MCU_TIMER2 Physical Address	MCU_TIMER3 Physical Address
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0245 0024h	0246 0024h	0247 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0245 0028h	0246 0028h	0247 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0245 002Ch	0246 002Ch	0247 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0245 0030h	0246 0030h	0247 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0245 0034h	0246 0034h	0247 0034h
38h	32	DMTIMER1MS_TCLR	0245 0038h	0246 0038h	0247 0038h
3Ch	32	DMTIMER1MS_TCRR	0245 003Ch	0246 003Ch	0247 003Ch
40h	32	DMTIMER1MS_TLDR	0245 0040h	0246 0040h	0247 0040h
44h	32	DMTIMER1MS_TTGR	0245 0044h	0246 0044h	0247 0044h
48h	32	DMTIMER1MS_TWPS	0245 0048h	0246 0048h	0247 0048h
4Ch	32	DMTIMER1MS_TMAR	0245 004Ch	0246 004Ch	0247 004Ch
50h	32	DMTIMER1MS_TCAR1	0245 0050h	0246 0050h	0247 0050h
54h	32	DMTIMER1MS_TSICR	0245 0054h	0246 0054h	0247 0054h
58h	32	DMTIMER1MS_TCAR2	0245 0058h	0246 0058h	0247 0058h
5Ch	32	DMTIMER1MS_TPIR	0245 005Ch	0246 005Ch	0247 005Ch
60h	32	DMTIMER1MS_TNIR	0245 0060h	0246 0060h	0247 0060h
64h	32	DMTIMER1MS_TCVR	0245 0064h	0246 0064h	0247 0064h
68h	32	DMTIMER1MS_TOCR	0245 0068h	0246 0068h	0247 0068h
6Ch	32	DMTIMER1MS_TOWR	0245 006Ch	0246 006Ch	0247 006Ch

Table 14-31609. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	WKUP_TIMER0 Physical Address	WKUP_TIMER1 Physical Address
0h	32	DMTIMER1MS_TIDR	2B10 0000h	2B11 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	2B10 0010h	2B11 0010h
20h	32	DMTIMER1MS_IRQ_EOI	2B10 0020h	2B11 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	2B10 0024h	2B11 0024h
28h	32	DMTIMER1MS_IRQSTATUS	2B10 0028h	2B11 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	2B10 002Ch	2B11 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	2B10 0030h	2B11 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	2B10 0034h	2B11 0034h
38h	32	DMTIMER1MS_TCLR	2B10 0038h	2B11 0038h
3Ch	32	DMTIMER1MS_TCRR	2B10 003Ch	2B11 003Ch
40h	32	DMTIMER1MS_TLDR	2B10 0040h	2B11 0040h
44h	32	DMTIMER1MS_TTGR	2B10 0044h	2B11 0044h
48h	32	DMTIMER1MS_TWPS	2B10 0048h	2B11 0048h
4Ch	32	DMTIMER1MS_TMAR	2B10 004Ch	2B11 004Ch
50h	32	DMTIMER1MS_TCAR1	2B10 0050h	2B11 0050h
54h	32	DMTIMER1MS_TSICR	2B10 0054h	2B11 0054h
58h	32	DMTIMER1MS_TCAR2	2B10 0058h	2B11 0058h
5Ch	32	DMTIMER1MS_TPIR	2B10 005Ch	2B11 005Ch
60h	32	DMTIMER1MS_TNIR	2B10 0060h	2B11 0060h
64h	32	DMTIMER1MS_TCVR	2B10 0064h	2B11 0064h
68h	32	DMTIMER1MS_TOCR	2B10 0068h	2B11 0068h

Table 14-31609. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	WKUP_TIMER0 Physical Address	WKUP_TIMER1 Physical Address
6Ch	32	DMTIMER1MS_TOWR	2B10 006Ch	2B11 006Ch

14.9.7.4.2 TIMER Registers

TIMER Registers

14.9.7.4.2.1 DMTIMER1MS_TIDR Register

1 DMTIMER1MS_TIDR Register (Offset = 0h) [reset = 50003900h]

Peripheral ID

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Table 14-31610. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0000h
MCU_TIMER1	0481 0000h
MCU_TIMER2	0482 0000h
MCU_TIMER3	0483 0000h
TIMER0	0240 0000h
TIMER1	0241 0000h
TIMER2	0242 0000h
TIMER3	0243 0000h
TIMER4	0244 0000h
TIMER5	0245 0000h
TIMER6	0246 0000h
TIMER7	0247 0000h
WKUP_TIMER0	2B10 0000h
WKUP_TIMER1	2B11 0000h

Figure 14-10468. DMTIMER1MS_TIDR Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		1h		0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
7h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-31612. DMTIMER1MS_TIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: mod_g_rst_n

Table 14-31612. DMTIMER1MS_TIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

29:28	BU	R	1h	Business Unit
				Reset Source: mod_g_rst_n
				`1 Wireless BU`
				`2 Processors BU`

27:16	MODULE_ID	R	0h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	7h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.9.7.4.2.2 DMTIMER1MS_TIOCP_CFG Register

1 DMTIMER1MS_TIOCP_CFG Register (Offset = 10h) [reset = 8h]

This register controls the various parameters of the OCP interface

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Table 14-31613. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0010h**
MCU_TIMER1	**0481 0010h**
MCU_TIMER2	**0482 0010h**
MCU_TIMER3	**0483 0010h**
TIMER0	**0240 0010h**
TIMER1	**0241 0010h**
TIMER2	**0242 0010h**
TIMER3	**0243 0010h**
TIMER4	**0244 0010h**
TIMER5	**0245 0010h**
TIMER6	**0246 0010h**
TIMER7	**0247 0010h**
WKUP_TIMER0	**2B10 0010h**
WKUP_TIMER1	**2B11 0010h**

Figure 14-10469. DMTIMER1MS_TIOCP_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				IDLEMODE		EMUFREE	SOFTRESET
NONE				R/W		R/W	R/W
0h				2h		0h	0h

Table 14-31615. DMTIMER1MS_TIOCP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

Table 14-31615. DMTIMER1MS_TIOCP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Idle Mode Reset Source: mod_g_rst_n 0 local target's idle state follows (acknowledges) the system's idle reuquests unconditionaly, i.e. regardless of the IP module's internal requirments. Back mode, for debug only. 1 local target never enteres idle state. Back mode, for debug only. 2 local target's idle state eventually follows (acknowledges) the systems' idle requests, depending on the IP module's internal requirments. IP module shall not generate (IRQ- or DMA-request-releated) wakeup events. 3 local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirents. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) impolemented.
1	EMUFREE	R/W	0h	Emulation Mode Reset Source: mod_g_rst_n 0 The timer is frozen in emulation mode (PI_SUSPEND signal active) 1 The timer runs free, regardless of PI_SUSPEND value
0	SOFTRESET	R/W	0h	Software reset Reset Source: mod_g_rst_n 0 Read: Reset Done, no pending action Write: no action 1 Read: Reset ongoing Write: initiate software reset

14.9.7.4.2.3 DMTIMER1MS_IRQ_EOI Register

1 DMTIMER1MS_IRQ_EOI Register (Offset = 20h) [reset = 0h]

Allows the generation of further pulses on the interrupt line, if an new interrupt event is pending, when using the pulsed output. Unused when using the level interrupt line

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Table 14-31616. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0020h
MCU_TIMER1	0481 0020h
MCU_TIMER2	0482 0020h
MCU_TIMER3	0483 0020h
TIMER0	0240 0020h
TIMER1	0241 0020h
TIMER2	0242 0020h
TIMER3	0243 0020h
TIMER4	0244 0020h
TIMER5	0245 0020h
TIMER6	0246 0020h
TIMER7	0247 0020h
WKUP_TIMER0	2B10 0020h
WKUP_TIMER1	2B11 0020h

Figure 14-10470. DMTIMER1MS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINE_NUMBER
NONE							R/W
0h							0h

Table 14-31618. DMTIMER1MS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

Table 14-31618. DMTIMER1MS_IRQ_EOI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LINE_NUMBER	R/W	0h	Idle Mode Reset Source: mod_g_rst_n 0 `End of interrupt`

14.9.7.4.2.4 DMTIMER1MS_IRQSTATUS_RAW Register

1 DMTIMER1MS_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug

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Table 14-31619. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0024h**
MCU_TIMER1	**0481 0024h**
MCU_TIMER2	**0482 0024h**
MCU_TIMER3	**0483 0024h**
TIMER0	**0240 0024h**
TIMER1	**0241 0024h**
TIMER2	**0242 0024h**
TIMER3	**0243 0024h**
TIMER4	**0244 0024h**
TIMER5	**0245 0024h**
TIMER6	**0246 0024h**
TIMER7	**0247 0024h**
WKUP_TIMER0	**2B10 0024h**
WKUP_TIMER1	**2B11 0024h**

Figure 14-10471. DMTIMER1MS_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-31621. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n

Table 14-31621. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.7.4.2.5 DMTIMER1MS_IRQSTATUS Register

1 DMTIMER1MS_IRQSTATUS Register (Offset = 28h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register.Enabled status isn't set unless event is enabled.Write 1 to clear the status after interrupt has been serviced;raw status gets cleared, i.e. even if not enabled

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Table 14-31622. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0028h**
MCU_TIMER1	**0481 0028h**
MCU_TIMER2	**0482 0028h**
MCU_TIMER3	**0483 0028h**
TIMER0	**0240 0028h**
TIMER1	**0241 0028h**
TIMER2	**0242 0028h**
TIMER3	**0243 0028h**
TIMER4	**0244 0028h**
TIMER5	**0245 0028h**
TIMER6	**0246 0028h**
TIMER7	**0247 0028h**
WKUP_TIMER0	**2B10 0028h**
WKUP_TIMER1	**2B11 0028h**

Figure 14-10472. DMTIMER1MS_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-31624. DMTIMER1MS_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n

Table 14-31624. DMTIMER1MS_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.7.4.2.6 DMTIMER1MS_IRQSTATUS_SET Register

1 DMTIMER1MS_IRQSTATUS_SET Register (Offset = 2Ch) [reset = 0h]

Component interrupt request enable Write 1 to set;enable interrupt. Readout equal to corresponding _CLR register.

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Table 14-31625. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 002Ch
MCU_TIMER1	0481 002Ch
MCU_TIMER2	0482 002Ch
MCU_TIMER3	0483 002Ch
TIMER0	0240 002Ch
TIMER1	0241 002Ch
TIMER2	0242 002Ch
TIMER3	0243 002Ch
TIMER4	0244 002Ch
TIMER5	0245 002Ch
TIMER6	0246 002Ch
TIMER7	0247 002Ch
WKUP_TIMER0	2B10 002Ch
WKUP_TIMER1	2B11 002Ch

Figure 14-10473. DMTIMER1MS_IRQSTATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>TCAR_IT_FLAG</td><td>OVF_IT_FLAG</td><td>MAT_IT_FLAG</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31627. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n

Table 14-31627. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.7.4.2.7 DMTIMER1MS_IRQSTATUS_CLR Register

1 DMTIMER1MS_IRQSTATUS_CLR Register (Offset = 30h) [reset = 0h]

Component interrupt request enable. Write 1 to clear; disable interrupt. Readout equal to corresponding _SET register

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Table 14-31628. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0030h
MCU_TIMER1	0481 0030h
MCU_TIMER2	0482 0030h
MCU_TIMER3	0483 0030h
TIMER0	0240 0030h
TIMER1	0241 0030h
TIMER2	0242 0030h
TIMER3	0243 0030h
TIMER4	0244 0030h
TIMER5	0245 0030h
TIMER6	0246 0030h
TIMER7	0247 0030h
WKUP_TIMER0	2B10 0030h
WKUP_TIMER1	2B11 0030h

Figure 14-10474. DMTIMER1MS_IRQSTATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-31630. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n

Table 14-31630. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.7.4.2.8 DMTIMER1MS_IRQWAKEEN Register

1 DMTIMER1MS_IRQWAKEEN Register (Offset = 34h) [reset = 0h]

Wakeup-enabled events taking place when module is idle shall generate an asynchronous wakeup

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Table 14-31631. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0034h
MCU_TIMER1	0481 0034h
MCU_TIMER2	0482 0034h
MCU_TIMER3	0483 0034h
TIMER0	0240 0034h
TIMER1	0241 0034h
TIMER2	0242 0034h
TIMER3	0243 0034h
TIMER4	0244 0034h
TIMER5	0245 0034h
TIMER6	0246 0034h
TIMER7	0247 0034h
WKUP_TIMER0	2B10 0034h
WKUP_TIMER1	2B11 0034h

Figure 14-10475. DMTIMER1MS_IRQWAKEEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MAT_WUP_ENA	OVF_WUP_ENA	TCAR_WUP_ENA
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-31633. DMTIMER1MS_IRQWAKEEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MAT_WUP_ENA	R/W	0h	Match Wakeup Enable Reset Source: mod_g_rst_n

Table 14-31633. DMTIMER1MS_IRQWAKEEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OVF_WUP_ENA	R/W	0h	Overflow Wakeup Enable Reset Source: mod_g_rst_n
0	TCAR_WUP_ENA	R/W	0h	Capture Wakeup Enable Reset Source: mod_g_rst_n

14.9.7.4.2.9 DMTIMER1MS_TCLR Register

1 DMTIMER1MS_TCLR Register (Offset = 38h) [reset = 0h]

This register controls optional features specific to the timer functionality

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Table 14-31634. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0038h
MCU_TIMER1	0481 0038h
MCU_TIMER2	0482 0038h
MCU_TIMER3	0483 0038h
TIMER0	0240 0038h
TIMER1	0241 0038h
TIMER2	0242 0038h
TIMER3	0243 0038h
TIMER4	0244 0038h
TIMER5	0245 0038h
TIMER6	0246 0038h
TIMER7	0247 0038h
WKUP_TIMER0	2B10 0038h
WKUP_TIMER1	2B11 0038h

Figure 14-10476. DMTIMER1MS_TCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>GPO_CFG</td><td>CAPT_MODE</td><td>PT</td><td colspan="2">TRG</td><td colspan="2">TCM</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SCPWM</td><td>CE</td><td>PRE</td><td colspan="3">PTV</td><td>AR</td><td>ST</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31636. DMTIMER1MS_TCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	GPO_CFG	R/W	0h	This field drives directly the timer_gpocfg port Reset Source: mod_g_rst_n

Table 14-31636. DMTIMER1MS_TCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CAPT_MODE	R/W	0h	Capture mode select bit; First/second Reset Source: mod_g_rst_n 0 Capture first enabled capture event in TCAR1 1 Capture first enabled capture event in TCAR2
12	PT	R/W	0h	Pulse or Toggle select bit Reset Source: mod_g_rst_n 0 Pulse modulation 0 Toggle modulation
11:10	TRG	R/W	0h	Trigger Output Mode Reset Source: mod_g_rst_n 0 No Trigger 1 Overflow Trigger 2 Overflow and match Trigger
9:8	TCM	R/W	0h	Transition Capture Mode Reset Source: mod_g_rst_n 0 No capture 1 Capture on rising edges of PI_EVNETCAPT 2 Capture on falling edges of PI_EVENTCAPT 3 Capture on both edges of PI_EVNENTCAPT
7	SCPWM	R/W	0h	Pulse Width Modulation output pin default value Reset Source: mod_g_rst_n
6	CE	R/W	0h	Compare Enable Reset Source: mod_g_rst_n 0 compare disabled 1 compare enabled
5	PRE	R/W	0h	Prescaler Enable Reset Source: mod_g_rst_n 0 Prescaler disabeld 1 Prescaler Enabled
4:2	PTV	R/W	0h	Trigger Output Mode. The timer counter is prescaled with the value: 2^PTV Reset Source: mod_g_rst_n
1	AR	R/W	0h	Auto-reload mode Reset Source: mod_g_rst_n 0 One shot mode overflow 1 Auto-reload mode overflow
0	ST	R/W	0h	Start/Stop timer control Reset Source: mod_g_rst_n 0 Stop the timer 1 Start the timer

14.9.7.4.2.10 DMTIMER1MS_TCRR Register

1 DMTIMER1MS_TCRR Register (Offset = 3Ch) [reset = 0h]

This register holds the value of the internal counter

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Table 14-31637. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 003Ch
MCU_TIMER1	0481 003Ch
MCU_TIMER2	0482 003Ch
MCU_TIMER3	0483 003Ch
TIMER0	0240 003Ch
TIMER1	0241 003Ch
TIMER2	0242 003Ch
TIMER3	0243 003Ch
TIMER4	0244 003Ch
TIMER5	0245 003Ch
TIMER6	0246 003Ch
TIMER7	0247 003Ch
WKUP_TIMER0	2B10 003Ch
WKUP_TIMER1	2B11 003Ch

Figure 14-10477. DMTIMER1MS_TCRR Name Register

31	30	29	28	27	26	25	24
TIMER_COUNTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TIMER_COUNTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TIMER_COUNTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TIMER_COUNTER							
R/W							
0h							

Table 14-31639. DMTIMER1MS_TCRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIMER_COUNTER	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.9.7.4.2.11 DMTIMER1MS_TLDR Register

1 DMTIMER1MS_TLDR Register (Offset = 40h) [reset = 0h]

This register holds the timer's load value

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Table 14-31640. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0040h
MCU_TIMER1	0481 0040h
MCU_TIMER2	0482 0040h
MCU_TIMER3	0483 0040h
TIMER0	0240 0040h
TIMER1	0241 0040h
TIMER2	0242 0040h
TIMER3	0243 0040h
TIMER4	0244 0040h
TIMER5	0245 0040h
TIMER6	0246 0040h
TIMER7	0247 0040h
WKUP_TIMER0	2B10 0040h
WKUP_TIMER1	2B11 0040h

Figure 14-10478. DMTIMER1MS_TLDR Name Register

31	30	29	28	27	26	25	24
LOAD_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
LOAD_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
LOAD_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
LOAD_VALUE							
R/W							
0h							

Table 14-31642. DMTIMER1MS_TLDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOAD_VALUE	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.9.7.4.2.12 DMTIMER1MS_TTGR Register

1 DMTIMER1MS_TTGR Register (Offset = 44h) [reset = 0h]

This register triggers a counter reload of timer by writing any value in it

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Table 14-31643. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0044h
MCU_TIMER1	0481 0044h
MCU_TIMER2	0482 0044h
MCU_TIMER3	0483 0044h
TIMER0	0240 0044h
TIMER1	0241 0044h
TIMER2	0242 0044h
TIMER3	0243 0044h
TIMER4	0244 0044h
TIMER5	0245 0044h
TIMER6	0246 0044h
TIMER7	0247 0044h
WKUP_TIMER0	2B10 0044h
WKUP_TIMER1	2B11 0044h

Figure 14-10479. DMTIMER1MS_TTGR Name Register

31	30	29	28	27	26	25	24
TTRG_VLAUE							
R/W							
0h							
23	22	21	20	19	18	17	16
TTRG_VLAUE							
R/W							
0h							
15	14	13	12	11	10	9	8
TTRG_VLAUE							
R/W							
0h							
7	6	5	4	3	2	1	0
TTRG_VLAUE							
R/W							
0h							

Table 14-31645. DMTIMER1MS_TTGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TTRG_VLAUE	R/W	0h	The value of the trigger register. During reads, it always return 0xFFFF_FFFF Reset Source: mod_g_rst_n

14.9.7.4.2.13 DMTIMER1MS_TWPS Register

1 DMTIMER1MS_TWPS Register (Offset = 48h) [reset = 0h]

This register contains the write posting bits for all writ-able functional registers

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Table 14-31646. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0048h**
MCU_TIMER1	**0481 0048h**
MCU_TIMER2	**0482 0048h**
MCU_TIMER3	**0483 0048h**
TIMER0	**0240 0048h**
TIMER1	**0241 0048h**
TIMER2	**0242 0048h**
TIMER3	**0243 0048h**
TIMER4	**0244 0048h**
TIMER5	**0245 0048h**
TIMER6	**0246 0048h**
TIMER7	**0247 0048h**
WKUP_TIMER0	**2B10 0048h**
WKUP_TIMER1	**2B11 0048h**

Figure 14-10480. DMTIMER1MS_TWPS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>W_PEND_TOWR</td><td>W_PEND_TOCR</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>W_PEND_TCVR</td><td>W_PEND_TNIR</td><td>W_PEND_TPIR</td><td>W_PEND_TMAR</td><td>W_PEND_TTGR</td><td>W_PEND_TLDR</td><td>W_PEND_TCRR</td><td>W_PEND_TCLR</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31648. DMTIMER1MS_TWPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	W_PEND_TOWR	R	0h	Write pending for register TOWR Reset Source: mod_g_rst_n

Table 14-31648. DMTIMER1MS_TWPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	W_PEND_TOCR	R	0h	Write pending for register TOCR Reset Source: mod_g_rst_n
7	W_PEND_TCVR	R	0h	Write pending for register TCVR Reset Source: mod_g_rst_n
6	W_PEND_TNIR	R	0h	Write pending for register TNIR Reset Source: mod_g_rst_n
5	W_PEND_TPIR	R	0h	Write pending for register TPIR Reset Source: mod_g_rst_n
4	W_PEND_TMAR	R	0h	Write pending for register TMAR Reset Source: mod_g_rst_n
3	W_PEND_TTGR	R	0h	Write pending for register TTGR Reset Source: mod_g_rst_n
2	W_PEND_TLDR	R	0h	Write pending for register TLDR Reset Source: mod_g_rst_n
1	W_PEND_TCRR	R	0h	Write pending for register TCRR Reset Source: mod_g_rst_n
0	W_PEND_TCLR	R	0h	Write pending for register TCLR Reset Source: mod_g_rst_n

14.9.7.4.2.14 DMTIMER1MS_TMAR Register

1 DMTIMER1MS_TMAR Register (Offset = 4Ch) [reset = 0h]

This register holds the match value to be compared with the counter's value

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Table 14-31649. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 004Ch
MCU_TIMER1	0481 004Ch
MCU_TIMER2	0482 004Ch
MCU_TIMER3	0483 004Ch
TIMER0	0240 004Ch
TIMER1	0241 004Ch
TIMER2	0242 004Ch
TIMER3	0243 004Ch
TIMER4	0244 004Ch
TIMER5	0245 004Ch
TIMER6	0246 004Ch
TIMER7	0247 004Ch
WKUP_TIMER0	2B10 004Ch
WKUP_TIMER1	2B11 004Ch

Figure 14-10481. DMTIMER1MS_TMAR Name Register

31	30	29	28	27	26	25	24
COMPARE_VLAUE							
R/W							
0h							
23	22	21	20	19	18	17	16
COMPARE_VLAUE							
R/W							
0h							
15	14	13	12	11	10	9	8
COMPARE_VLAUE							
R/W							
0h							
7	6	5	4	3	2	1	0
COMPARE_VLAUE							
R/W							
0h							

Table 14-31651. DMTIMER1MS_TMAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMPARE_VLAUE	R/W	0h	The value of the match register Reset Source: mod_g_rst_n

14.9.7.4.2.15 DMTIMER1MS_TCAR1 Register

1 DMTIMER1MS_TCAR1 Register (Offset = 50h) [reset = 0h]

This register holds the value of the first counter register capture

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Table 14-31652. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0050h
MCU_TIMER1	0481 0050h
MCU_TIMER2	0482 0050h
MCU_TIMER3	0483 0050h
TIMER0	0240 0050h
TIMER1	0241 0050h
TIMER2	0242 0050h
TIMER3	0243 0050h
TIMER4	0244 0050h
TIMER5	0245 0050h
TIMER6	0246 0050h
TIMER7	0247 0050h
WKUP_TIMER0	2B10 0050h
WKUP_TIMER1	2B11 0050h

Figure 14-10482. DMTIMER1MS_TCAR1 Name Register

31	30	29	28	27	26	25	24
CAPTURE_VALUE1							
R							
0h							
23	22	21	20	19	18	17	16
CAPTURE_VALUE1							
R							
0h							
15	14	13	12	11	10	9	8
CAPTURE_VALUE1							
R							
0h							
7	6	5	4	3	2	1	0
CAPTURE_VALUE1							
R							
0h							

Table 14-31654. DMTIMER1MS_TCAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE1	R	0h	The value of first captured counter register Reset Source: mod_g_rst_n

14.9.7.4.2.16 DMTIMER1MS_TSICR Register

1 DMTIMER1MS_TSICR Register (Offset = 54h) [reset = 0h]

Timer Synchronous Interface Control Register

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Table 14-31655. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0054h
MCU_TIMER1	0481 0054h
MCU_TIMER2	0482 0054h
MCU_TIMER3	0483 0054h
TIMER0	0240 0054h
TIMER1	0241 0054h
TIMER2	0242 0054h
TIMER3	0243 0054h
TIMER4	0244 0054h
TIMER5	0245 0054h
TIMER6	0246 0054h
TIMER7	0247 0054h
WKUP_TIMER0	2B10 0054h
WKUP_TIMER1	2B11 0054h

Figure 14-10483. DMTIMER1MS_TSICR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			READ_AFTER_IDLE	READ_MODE	POSTED	SFT	RESERVED
NONE			W	W	R/W	R/W	NONE
0h			0h	0h	X	0h	0h

Table 14-31657. DMTIMER1MS_TSICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-31657. DMTIMER1MS_TSICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	READ_AFTER_IDLE	W	0h	Select if the synchronization mechanism used for first TCRR read operation after IDLE state is active Reset Source: mod_g_rst_n 0 `The synchronization mechanism is enabled` 1 `The synchronization mechanism is disabled`
3	READ_MODE	W	0h	Select posted/non-posted mode for read operation. This bit is not used when configured in posted mode Reset Source: mod_g_rst_n 0 `when the module is configurated in non-posted mode the read operation is executed as posted read` 1 `when the module is configured in non-posted mode the read operation is executed as read non-posted`
2	POSTED	R/W	X	Reset value of POSTED depends on hardware integration module at design time. Software must read POSTED field to get the hardwar module configuration Reset Source: mod_g_rst_n 0 `Posted mode inactive: will delay the command accept output signal` 1 `Posted mode active`
1	SFT	R/W	0h	This bit reset all the functional part of teh module Reset Source: mod_g_rst_n 0 `Software reset is disabled` 1 `Software reset is enabled`
0	RESERVED	NONE	0h	Reserved

14.9.7.4.2.17 DMTIMER1MS_TCAR2 Register

1 DMTIMER1MS_TCAR2 Register (Offset = 58h) [reset = 0h]

This register holds the value of the second counter register capture

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Table 14-31658. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0058h**
MCU_TIMER1	**0481 0058h**
MCU_TIMER2	**0482 0058h**
MCU_TIMER3	**0483 0058h**
TIMER0	**0240 0058h**
TIMER1	**0241 0058h**
TIMER2	**0242 0058h**
TIMER3	**0243 0058h**
TIMER4	**0244 0058h**
TIMER5	**0245 0058h**
TIMER6	**0246 0058h**
TIMER7	**0247 0058h**
WKUP_TIMER0	**2B10 0058h**
WKUP_TIMER1	**2B11 0058h**

Figure 14-10484. DMTIMER1MS_TCAR2 Name Register

31	30	29	28	27	26	25	24
CAPTURE_VALUE2							
R							
0h							
23	22	21	20	19	18	17	16
CAPTURE_VALUE2							
R							
0h							
15	14	13	12	11	10	9	8
CAPTURE_VALUE2							
R							
0h							
7	6	5	4	3	2	1	0
CAPTURE_VALUE2							
R							
0h							

Table 14-31660. DMTIMER1MS_TCAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE2	R	0h	The value of second captured counter register Reset Source: mod_g_rst_n

14.9.7.4.2.18 DMTIMER1MS_TPIR Register

1 DMTIMER1MS_TPIR Register (Offset = 5Ch) [reset = 0h]

This register is used for 1ms tick generation. The TPIR register holds the value of the positive increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-31661. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 005Ch
MCU_TIMER1	0481 005Ch
MCU_TIMER2	0482 005Ch
MCU_TIMER3	0483 005Ch
TIMER0	0240 005Ch
TIMER1	0241 005Ch
TIMER2	0242 005Ch
TIMER3	0243 005Ch
TIMER4	0244 005Ch
TIMER5	0245 005Ch
TIMER6	0246 005Ch
TIMER7	0247 005Ch
WKUP_TIMER0	2B10 005Ch
WKUP_TIMER1	2B11 005Ch

Figure 14-10485. DMTIMER1MS_TPIR Name Register

31	30	29	28	27	26	25	24
POSITIVE_INC_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
POSITIVE_INC_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
POSITIVE_INC_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
POSITIVE_INC_VALUE							
R/W							
0h							

Table 14-31663. DMTIMER1MS_TPIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POSITIVE_INC_VALUE	R/W	0h	The value of the positive increment Reset Source: mod_g_rst_n

14.9.7.4.2.19 DMTIMER1MS_TNIR Register

1 DMTIMER1MS_TNIR Register (Offset = 60h) [reset = 0h]

This register is used for 1ms tick generation. The TNIR register holds the value of the negative increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-31664. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0060h**
MCU_TIMER1	**0481 0060h**
MCU_TIMER2	**0482 0060h**
MCU_TIMER3	**0483 0060h**
TIMER0	**0240 0060h**
TIMER1	**0241 0060h**
TIMER2	**0242 0060h**
TIMER3	**0243 0060h**
TIMER4	**0244 0060h**
TIMER5	**0245 0060h**
TIMER6	**0246 0060h**
TIMER7	**0247 0060h**
WKUP_TIMER0	**2B10 0060h**
WKUP_TIMER1	**2B11 0060h**

Figure 14-10486. DMTIMER1MS_TNIR Name Register

31	30	29	28	27	26	25	24
NEGATIVE_INC_VALUE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NEGATIVE_INC_VALUE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NEGATIVE_INC_VALUE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEGATIVE_INC_VALUE							
R/W							
0h							

Table 14-31666. DMTIMER1MS_TNIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NEGATIVE_INC_VALUE	R/W	0h	The value of the negative increment Reset Source: mod_g_rst_n

14.9.7.4.2.20 DMTIMER1MS_TCVR Register

1 DMTIMER1MS_TCVR Register (Offset = 64h) [reset = 0h]

This register is used for 1ms tick generation. The TCVR register defines whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-31667. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0064h**
MCU_TIMER1	**0481 0064h**
MCU_TIMER2	**0482 0064h**
MCU_TIMER3	**0483 0064h**
TIMER0	**0240 0064h**
TIMER1	**0241 0064h**
TIMER2	**0242 0064h**
TIMER3	**0243 0064h**
TIMER4	**0244 0064h**
TIMER5	**0245 0064h**
TIMER6	**0246 0064h**
TIMER7	**0247 0064h**
WKUP_TIMER0	**2B10 0064h**
WKUP_TIMER1	**2B11 0064h**

Figure 14-10487. DMTIMER1MS_TCVR Name Register

31	30	29	28	27	26	25	24
COUNTER_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTER_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTER_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTER_VALUE							
R/W							
0h							

Table 14-31669. DMTIMER1MS_TCVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTER_VALUE	R/W	0h	The value of CVR counter Reset Source: mod_g_rst_n

14.9.7.4.2.21 DMTIMER1MS_TOCR Register

1 DMTIMER1MS_TOCR Register (Offset = 68h) [reset = 0h]

This register is used to mask the tick interrupt for a selected number of ticks

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Table 14-31670. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0068h**
MCU_TIMER1	**0481 0068h**
MCU_TIMER2	**0482 0068h**
MCU_TIMER3	**0483 0068h**
TIMER0	**0240 0068h**
TIMER1	**0241 0068h**
TIMER2	**0242 0068h**
TIMER3	**0243 0068h**
TIMER4	**0244 0068h**
TIMER5	**0245 0068h**
TIMER6	**0246 0068h**
TIMER7	**0247 0068h**
WKUP_TIMER0	**2B10 0068h**
WKUP_TIMER1	**2B11 0068h**

Figure 14-10488. DMTIMER1MS_TOCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_COUNTER_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_COUNTER_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_COUNTER_VALUE							
R/W							
0h							

Table 14-31672. DMTIMER1MS_TOCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OVF_COUNTER_VALUE	R/W	0h	The number of overflow events Reset Source: mod_g_rst_n

14.9.7.4.2.22 DMTIMER1MS_TOWR Register

1 DMTIMER1MS_TOWR Register (Offset = 6Ch) [reset = 0h]

This register holds the number of masked overflow interrupts

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Table 14-31673. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 006Ch**
MCU_TIMER1	**0481 006Ch**
MCU_TIMER2	**0482 006Ch**
MCU_TIMER3	**0483 006Ch**
TIMER0	**0240 006Ch**
TIMER1	**0241 006Ch**
TIMER2	**0242 006Ch**
TIMER3	**0243 006Ch**
TIMER4	**0244 006Ch**
TIMER5	**0245 006Ch**
TIMER6	**0246 006Ch**
TIMER7	**0247 006Ch**
WKUP_TIMER0	**2B10 006Ch**
WKUP_TIMER1	**2B11 006Ch**

Figure 14-10489. DMTIMER1MS_TOWR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_WRAPPING_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_WRAPPING_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_WRAPPING_VALUE							
R/W							
0h							

Table 14-31675. DMTIMER1MS_TOWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OVF_WRAPPING_VALUE	R/W	0h	The number of masked interrupts Reset Source: mod_g_rst_n

14.9.8 Internal Diagnostics Modules Registers

14.9.8.1 DCC

DCC

14.9.8.1.1 DCC Summaries

DCC Summaries

Table 14-31676. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC2_DCCGCTRL	0080 0000h	0080 4000h	0080 8000h
4h	32	DCC2_DCCREV	0080 0004h	0080 4004h	0080 8004h
8h	32	DCC2_DCCCNTSEED0	0080 0008h	0080 4008h	0080 8008h
Ch	32	DCC2_DCCVALIDSEED0	0080 000Ch	0080 400Ch	0080 800Ch
10h	32	DCC2_DCCCNTSEED1	0080 0010h	0080 4010h	0080 8010h
14h	32	DCC2_DCCSTATUS	0080 0014h	0080 4014h	0080 8014h
18h	32	DCC2_DCCCNT0	0080 0018h	0080 4018h	0080 8018h
1Ch	32	DCC2_DCCVALID0	0080 001Ch	0080 401Ch	0080 801Ch
20h	32	DCC2_DCCCNT1	0080 0020h	0080 4020h	0080 8020h
24h	32	DCC2_DCCCLKSRC1	0080 0024h	0080 4024h	0080 8024h
28h	32	DCC2_DCCCLKSRC0	0080 0028h	0080 4028h	0080 8028h
2Ch	32	DCC2_DCCGCTRL2	0080 002Ch	0080 402Ch	0080 802Ch
30h	32	DCC2_DCCSTATUS2	0080 0030h	0080 4030h	0080 8030h
34h	32	DCC2_DCCERRCNT	0080 0034h	0080 4034h	0080 8034h

Table 14-31677. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC3 Physical Address	DCC4 Physical Address	DCC5 Physical Address
0h	32	DCC2_DCCGCTRL	0080 C000h	0081 0000h	0081 4000h
4h	32	DCC2_DCCREV	0080 C004h	0081 0004h	0081 4004h
8h	32	DCC2_DCCCNTSEED0	0080 C008h	0081 0008h	0081 4008h
Ch	32	DCC2_DCCVALIDSEED0	0080 C00Ch	0081 000Ch	0081 400Ch
10h	32	DCC2_DCCCNTSEED1	0080 C010h	0081 0010h	0081 4010h
14h	32	DCC2_DCCSTATUS	0080 C014h	0081 0014h	0081 4014h
18h	32	DCC2_DCCCNT0	0080 C018h	0081 0018h	0081 4018h
1Ch	32	DCC2_DCCVALID0	0080 C01Ch	0081 001Ch	0081 401Ch
20h	32	DCC2_DCCCNT1	0080 C020h	0081 0020h	0081 4020h
24h	32	DCC2_DCCCLKSRC1	0080 C024h	0081 0024h	0081 4024h
28h	32	DCC2_DCCCLKSRC0	0080 C028h	0081 0028h	0081 4028h
2Ch	32	DCC2_DCCGCTRL2	0080 C02Ch	0081 002Ch	0081 402Ch
30h	32	DCC2_DCCSTATUS2	0080 C030h	0081 0030h	0081 4030h
34h	32	DCC2_DCCERRCNT	0080 C034h	0081 0034h	0081 4034h

Table 14-31678. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC6 Physical Address	MCU_DCC0 Physical Address	MCU_DCC1 Physical Address
0h	32	DCC2_DCCGCTRL	0081 8000h	04C0 0000h	04C1 0000h
4h	32	DCC2_DCCREV	0081 8004h	04C0 0004h	04C1 0004h
8h	32	DCC2_DCCCNTSEED0	0081 8008h	04C0 0008h	04C1 0008h

Table 14-31678. DCC2 Registers, Base Address=0080 0000h, Length=64 (continued)

Offset	Length	Register Name	DCC6 Physical Address	MCU_DCC0 Physical Address	MCU_DCC1 Physical Address
Ch	32	DCC2_DCCVALIDSEED0	0081 800Ch	04C0 000Ch	04C1 000Ch
10h	32	DCC2_DCCCNTSEED1	0081 8010h	04C0 0010h	04C1 0010h
14h	32	DCC2_DCCSTATUS	0081 8014h	04C0 0014h	04C1 0014h
18h	32	DCC2_DCCCNT0	0081 8018h	04C0 0018h	04C1 0018h
1Ch	32	DCC2_DCCVALID0	0081 801Ch	04C0 001Ch	04C1 001Ch
20h	32	DCC2_DCCCNT1	0081 8020h	04C0 0020h	04C1 0020h
24h	32	DCC2_DCCCLKSRC1	0081 8024h	04C0 0024h	04C1 0024h
28h	32	DCC2_DCCCLKSRC0	0081 8028h	04C0 0028h	04C1 0028h
2Ch	32	DCC2_DCCGCTRL2	0081 802Ch	04C0 002Ch	04C1 002Ch
30h	32	DCC2_DCCSTATUS2	0081 8030h	04C0 0030h	04C1 0030h
34h	32	DCC2_DCCERRCNT	0081 8034h	04C0 0034h	04C1 0034h

14.9.8.1.2 DCC Registers

DCC Registers

14.9.8.1.2.1 DCC2_DCCGCTRL Register

1 DCC2_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Starts / stops the counters. Clears the error signal.

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Table 14-31679. Instance Table

Instance Name	Physical Address
DCC0	**0080 0000h**
DCC1	**0080 4000h**
DCC2	**0080 8000h**
DCC3	**0080 C000h**
DCC4	**0081 0000h**
DCC5	**0081 4000h**
DCC6	**0081 8000h**
MCU_DCC0	**04C0 0000h**
MCU_DCC1	**04C1 0000h**

Figure 14-10490. DCC2_DCCGCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DONEENA				SINGLESHOT			
R/W				R/W			
5h				5h			
7	6	5	4	3	2	1	0
ERRENA				DCCENA			
R/W				R/W			
5h				5h			

Table 14-31681. DCC2_DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	DONEENA	R/W	5h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation

Table 14-31681. DCC2_DCCGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SINGLESHOT	R/W	5h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error)
7:4	ERRENA	R/W	5h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101 = the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101 = disable error signal generation others = enable error signal generation
3:0	DCCENA	R/W	5h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101 = counters are stopped others = counters are running Privilege and debug mode (write): 0101 = stop counters and error-checking others = load the counters with their seed values and begin counting

14.9.8.1.2.2 DCC2_DCCREV Register

1 DCC2_DCCREV Register (Offset = 4h) [reset = 40010B00h]

Specifies the module version.

Return to Summary Table

Table 14-31682. Instance Table

Instance Name	Physical Address
DCC0	**0080 0004h**
DCC1	**0080 4004h**
DCC2	**0080 8004h**
DCC3	**0080 C004h**
DCC4	**0081 0004h**
DCC5	**0081 4004h**
DCC6	**0081 8004h**
MCU_DCC0	**04C0 0004h**
MCU_DCC1	**04C1 0004h**

Figure 14-10491. DCC2_DCCREV Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		NONE		R			
1h		0h		1h			
23	22	21	20	19	18	17	16
FUNC							
R							
1h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
1h					3h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-31684. DCC2_DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
29:28	RESERVED	NONE	0h	Reserved
27:16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
15:11	RTL	R	1h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x1 Privilege and debug mode (write): Writes have no effect.

Table 14-31684. DCC2_DCCREV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	MAJOR	R	3h	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7:6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
5:0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

14.9.8.1.2.3 DCC2_DCCCNTSEED0 Register

1 DCC2_DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Seed value for the counter attached to clock source 0

Return to Summary Table

Table 14-31685. Instance Table

Instance Name	Physical Address
DCC0	**0080 0008h**
DCC1	**0080 4008h**
DCC2	**0080 8008h**
DCC3	**0080 C008h**
DCC4	**0081 0008h**
DCC5	**0081 4008h**
DCC6	**0081 8008h**
MCU_DCC0	**04C0 0008h**
MCU_DCC1	**04C1 0008h**

Figure 14-10492. DCC2_DCCCNTSEED0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">COUNTSEED0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNTSEED0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNTSEED0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31687. DCC2_DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0. NOTE: Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation.

14.9.8.1.2.4 DCC2_DCCVALIDSEED0 Register

1 DCC2_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Seed value for the timeout counter attached to clock source 0.

Return to Summary Table

Table 14-31688. Instance Table

Instance Name	Physical Address
DCC0	**0080 000Ch**
DCC1	**0080 400Ch**
DCC2	**0080 800Ch**
DCC3	**0080 C00Ch**
DCC4	**0081 000Ch**
DCC5	**0081 400Ch**
DCC6	**0081 800Ch**
MCU_DCC0	**04C0 000Ch**
MCU_DCC1	**04C1 000Ch**

Figure 14-10493. DCC2_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALIDSEED0							
R/W							
0h							
7	6	5	4	3	2	1	0
VALIDSEED0							
R/W							
0h							

Table 14-31690. DCC2_DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0. NOTE: Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register.

14.9.8.1.2.5 DCC2_DCCCNTSEED1 Register

1 DCC2_DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Seed value for the counter attached to clock source 1.

Return to Summary Table

Table 14-31691. Instance Table

Instance Name	Physical Address
DCC0	**0080 0010h**
DCC1	**0080 4010h**
DCC2	**0080 8010h**
DCC3	**0080 C010h**
DCC4	**0081 0010h**
DCC5	**0081 4010h**
DCC6	**0081 8010h**
MCU_DCC0	**04C0 0010h**
MCU_DCC1	**04C1 0010h**

Figure 14-10494. DCC2_DCCCNTSEED1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">COUNTSEED1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNTSEED1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNTSEED1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31693. DCC2_DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1. NOTE: Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation.

14.9.8.1.2.6 DCC2_DCCSTATUS Register

1 DCC2_DCCSTATUS Register (Offset = 14h) [reset = 0h]

Specifies the status of the DCC Module.

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Table 14-31694. Instance Table

Instance Name	Physical Address
DCC0	**0080 0014h**
DCC1	**0080 4014h**
DCC2	**0080 8014h**
DCC3	**0080 C014h**
DCC4	**0081 0014h**
DCC5	**0081 4014h**
DCC6	**0081 8014h**
MCU_DCC0	**04C0 0014h**
MCU_DCC1	**04C1 0014h**

Figure 14-10495. DCC2_DCCSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>DONEFLG</td><td>ERRFLG</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-31696. DCC2_DCCSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag

Table 14-31696. DCC2_DCCSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

14.9.8.1.2.7 DCC2_DCCCNT0 Register

1 DCC2_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Value of the counter attached to clock source 0.

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Table 14-31697. Instance Table

Instance Name	Physical Address
DCC0	**0080 0018h**
DCC1	**0080 4018h**
DCC2	**0080 8018h**
DCC3	**0080 C018h**
DCC4	**0081 0018h**
DCC5	**0081 4018h**
DCC6	**0081 8018h**
MCU_DCC0	**04C0 0018h**
MCU_DCC1	**04C1 0018h**

Figure 14-10496. DCC2_DCCCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COUNT0			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT0							
R							
0h							

Table 14-31699. DCC2_DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns the current value for counter 0. Privilege and debug mode (write): Writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.8.1.2.8 DCC2_DCCVALID0 Register

1 DCC2_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Value of the valid counter attached to clock source 0.

Return to Summary Table

Table 14-31700. Instance Table

Instance Name	Physical Address
DCC0	**0080 001Ch**
DCC1	**0080 401Ch**
DCC2	**0080 801Ch**
DCC3	**0080 C01Ch**
DCC4	**0081 001Ch**
DCC5	**0081 401Ch**
DCC6	**0081 801Ch**
MCU_DCC0	**04C0 001Ch**
MCU_DCC1	**04C1 001Ch**

Figure 14-10497. DCC2_DCCVALID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALID0							
R							
0h							
7	6	5	4	3	2	1	0
VALID0							
R							
0h							

Table 14-31702. DCC2_DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns the current value for valid counter 0. Privilege and debug mode (write): writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.8.1.2.9 DCC2_DCCCNT1 Register

1 DCC2_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Value of the counter attached to clock source 1.

Return to Summary Table

Table 14-31703. Instance Table

Instance Name	Physical Address
DCC0	**0080 0020h**
DCC1	**0080 4020h**
DCC2	**0080 8020h**
DCC3	**0080 C020h**
DCC4	**0081 0020h**
DCC5	**0081 4020h**
DCC6	**0081 8020h**
MCU_DCC0	**04C0 0020h**
MCU_DCC1	**04C1 0020h**

Figure 14-10498. DCC2_DCCCNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNT1			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
COUNT1							
R							
0h							
7	6	5	4	3	2	1	0
COUNT1							
R							
0h							

Table 14-31705. DCC2_DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.8.1.2.10 DCC2_DCCCLKSRC1 Register

1 DCC2_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Selects the clock source for counter 1.

Return to Summary Table

Table 14-31706. Instance Table

Instance Name	Physical Address
DCC0	**0080 0024h**
DCC1	**0080 4024h**
DCC2	**0080 8024h**
DCC3	**0080 C024h**
DCC4	**0081 0024h**
DCC5	**0081 4024h**
DCC6	**0081 8024h**
MCU_DCC0	**04C0 0024h**
MCU_DCC1	**04C1 0024h**

Figure 14-10499. DCC2_DCCCLKSRC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">KEY</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CLKSRC1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-31708. DCC2_DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1.
11:5	RESERVED	NONE	0h	Reserved

Table 14-31708. DCC2_DCCCLKSRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC. Privilege and debug mode (write): Sets the value of CLKSRC. 0000 Clk source 0 is selected for COUNT1 0001 Clk source 1 is selected for COUNT1 0010 Clk source 2 is selected for COUNT1 0011 Clk source 3 is selected for COUNT1 0100 Clk source 4 is selected for COUNT1 0101 Clk source 5 is selected for COUNT1 0110 Clk source 6 is selected for COUNT1 0111 Clk source 7 is selected for COUNT1 1000-1111 VCLK is selected for COUNT1

14.9.8.1.2.11 DCC2_DCCCLKSRC0 Register

1 DCC2_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Selects the clock source for counter 0.

Return to Summary Table

Table 14-31709. Instance Table

Instance Name	Physical Address
DCC0	**0080 0028h**
DCC1	**0080 4028h**
DCC2	**0080 8028h**
DCC3	**0080 C028h**
DCC4	**0081 0028h**
DCC5	**0081 4028h**
DCC6	**0081 8028h**
MCU_DCC0	**04C0 0028h**
MCU_DCC1	**04C1 0028h**

Figure 14-10500. DCC2_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CLKSRC0			
NONE				R/W			
0h				0h			

Table 14-31711. DCC2_DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0.
11:4	RESERVED	NONE	0h	Reserved

Table 14-31711. DCC2_DCCCLKSRC0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0. NOTE: DCC does not generate an error when the clock source is VCLK and VCLK is not present. Note: newer versions of DCC only provide one encoding for VCLK selection (MS encodings are tied off) 0000 Clock0[0] is selected as source for COUNT0 0001 Clock0[1] is selected as source for COUNT0 0010 Clock0[2] is selected as source for COUNT0 Other Values VCLK is selected as source for COUNT0

14.9.8.1.2.12 DCC2_DCCGCTRL2 Register

1 DCC2_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Allows configuring different modes of operation for DCC.

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Table 14-31712. Instance Table

Instance Name	Physical Address
DCC0	**0080 002Ch**
DCC1	**0080 402Ch**
DCC2	**0080 802Ch**
DCC3	**0080 C02Ch**
DCC4	**0081 002Ch**
DCC5	**0081 402Ch**
DCC6	**0081 802Ch**
MCU_DCC0	**04C0 002Ch**
MCU_DCC1	**04C1 002Ch**

Figure 14-10501. DCC2_DCCGCTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FIFO_NONERR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">FIFO_READ</td><td colspan="4">CONT_ON_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">5h</td><td colspan="4">5h</td></tr>
</table>

Table 14-31714. DCC2_DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	FIFO_NONERR	R/W	5h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not.

Table 14-31714. DCC2_DCCGCTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	FIFO_READ	R/W	5h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read.
3:0	CONT_ON_ERR	R/W	5h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition.

14.9.8.1.2.13 DCC2_DCCSTATUS2 Register

1 DCC2_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Specifies the status of the DCC FIFOs.

Return to Summary Table

Table 14-31715. Instance Table

Instance Name	Physical Address
DCC0	**0080 0030h**
DCC1	**0080 4030h**
DCC2	**0080 8030h**
DCC3	**0080 C030h**
DCC4	**0081 0030h**
DCC5	**0081 4030h**
DCC6	**0081 8030h**
MCU_DCC0	**04C0 0030h**
MCU_DCC1	**04C1 0030h**

Figure 14-10502. DCC2_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE		R	R	R	R	R	R
0h		0h	0h	0h	1h	1h	1h

Table 14-31717. DCC2_DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.

Table 14-31717. DCC2_DCCSTATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

14.9.8.1.2.14 DCC2_DCCERRCNT Register

1 DCC2_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Counts number of errors since last clear.

Return to Summary Table

Table 14-31718. Instance Table

Instance Name	Physical Address
DCC0	**0080 0034h**
DCC1	**0080 4034h**
DCC2	**0080 8034h**
DCC3	**0080 C034h**
DCC4	**0081 0034h**
DCC5	**0081 4034h**
DCC6	**0081 8034h**
MCU_DCC0	**04C0 0034h**
MCU_DCC1	**04C1 0034h**

Figure 14-10503. DCC2_DCCERRCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ERRCNT	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
ERRCNT							
R/W							
0h							

Table 14-31720. DCC2_DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

14.9.8.2 ESM

ESM

14.9.8.2.1 ESM Summaries

ESM Summaries

Table 14-31721. ESM Registers, Base Address=0042 0000h, Length=4096

Offset	Length	Register Name	ESM0 Physical Address
0h	32	ESM_PID	0042 0000h
4h	32	ESM_INFO	0042 0004h
8h	32	ESM_EN	0042 0008h
Ch	32	ESM_SFT_RST	0042 000Ch
10h	32	ESM_ERR_RAW	0042 0010h
14h	32	ESM_ERR_STS	0042 0014h
18h	32	ESM_ERR_EN_SET	0042 0018h
1Ch	32	ESM_ERR_EN_CLR	0042 001Ch
20h	32	ESM_LOW_PRI	0042 0020h
24h	32	ESM_HI_PRI	0042 0024h
28h	32	ESM_LOW	0042 0028h
2Ch	32	ESM_HI	0042 002Ch
30h	32	ESM_EOI	0042 0030h
40h	32	ESM_PIN_CTRL	0042 0040h
44h	32	ESM_PIN_STS	0042 0044h
48h	32	ESM_PIN_CNTR	0042 0048h
4Ch	32	ESM_PIN_CNTR_PRE	0042 004Ch
50h	32	ESM_PWMH_PIN_CNTR	0042 0050h
54h	32	ESM_PWMH_PIN_CNTR_PRE	0042 0054h
58h	32	ESM_PWML_PIN_CNTR	0042 0058h
5Ch	32	ESM_PWML_PIN_CNTR_PRE	0042 005Ch
0h	32	ESM_ERR_GRP_RAW_J	0042 0000h + formula
4h	32	ESM_ERR_GRP_STS_J	0042 0004h + formula
8h	32	ESM_ERR_GRP_INTR_EN_SET_J	0042 0008h + formula
Ch	32	ESM_ERR_GRP_INTR_EN_CLR_J	0042 000Ch + formula
10h	32	ESM_ERR_GRP_INT_PRIO_J	0042 0010h + formula
14h	32	ESM_ERR_GRP_PIN_EN_SET_J	0042 0014h + formula
18h	32	ESM_ERR_GRP_PIN_EN_CLR_J	0042 0018h + formula

14.9.8.2.2 ESM Registers

ESM Registers

14.9.8.2.2.1 ESM_PID Register

1 ESM_PID Register (Offset = 0h) [reset = 6FE04900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-31722. Instance Table

Instance Name	Physical Address
ESM0	**0042 0000h**

Figure 14-10504. ESM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		FE0h			
23	22	21	20	19	18	17	16
FUNC							
R							
FE0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-31724. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: por_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: por_rst_n
27:16	FUNC	R	FE0h	Module ID Reset Source: por_rst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: por_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: por_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: por_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: por_rst_n

14.9.8.2.2.2 ESM_INFO Register

1 ESM_INFO Register (Offset = 4h) [reset = 107h]

The Info Register gives the configuration Inforrmation of this ESM.

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Table 14-31725. Instance Table

Instance Name	Physical Address
ESM0	**0042 0004h**

Figure 14-10505. ESM_INFO Name Register

31	30	29	28	27	26	25	24
LAST_RESET	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PULSE_GROUPS							
R							
1h							
7	6	5	4	3	2	1	0
GROUPS							
R							
7h							

Table 14-31727. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	Indicates the Source of the last Reset Reset Source: por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	PULSE_GROUPS	R	1h	Number of Pulse Error Groups Reset Source: por_rst_n
7:0	GROUPS	R	7h	Total number of Error Groups Reset Source: por_rst_n

14.9.8.2.2.3 ESM_EN Register

1 ESM_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the initiator interrupt mask

Return to Summary Table

Table 14-31728. Instance Table

Instance Name	Physical Address
ESM0	**0042 0008h**

Figure 14-10506. ESM_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				R/W			
0h				0h			

Table 14-31730. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	R/W	0h	Global Enable Reset Source: por_rst_n

14.9.8.2.2.4 ESM_SFT_RST Register

1 ESM_SFT_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables

Return to Summary Table

Table 14-31731. Instance Table

Instance Name	Physical Address
ESM0	**0042 000Ch**

Figure 14-10507. ESM_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 14-31733. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Global Soft Reset Reset Source: por_rst_n

14.9.8.2.2.5 ESM_ERR_RAW Register

1 ESM_ERR_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors

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Table 14-31734. Instance Table

Instance Name	Physical Address
ESM0	**0042 0010h**

Figure 14-10508. ESM_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	STS						
NONE	R/W1TS						
0h	0h						

Table 14-31736. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	STS	R/W1TS	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.2.2.6 ESM_ERR_STS Register

1 ESM_ERR_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register

Return to Summary Table

Table 14-31737. Instance Table

Instance Name	Physical Address
ESM0	**0042 0014h**

Figure 14-10509. ESM_ERR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MSK						
NONE	R/W1TC						
0h	0h						

Table 14-31739. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	MSK	R/W1TC	0h	This is the masked status/clear for config errors Reset Source: por_rst_n

14.9.8.2.2.7 ESM_ERR_EN_SET Register

1 ESM_ERR_EN_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register

Return to Summary Table

Table 14-31740. Instance Table

Instance Name	Physical Address
ESM0	**0042 0018h**

Figure 14-10510. ESM_ERR_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MSK						
NONE	R/W1TS						
0h	0h						

Table 14-31742. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	MSK	R/W1TS	0h	This is the mask enable set for config errors Reset Source: por_rst_n

14.9.8.2.2.8 ESM_ERR_EN_CLR Register

1 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register

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Table 14-31743. Instance Table

Instance Name	Physical Address
ESM0	**0042 001Ch**

Figure 14-10511. ESM_ERR_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MSK						
NONE	R/W1TC						
0h	0h						

Table 14-31745. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	MSK	R/W1TC	0h	This is the mask enable clear for config errors Reset Source: por_rst_n

14.9.8.2.2.9 ESM_LOW_PRI Register

1 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt

Return to Summary Table

Table 14-31746. Instance Table

Instance Name	Physical Address
ESM0	**0042 0020h**

Figure 14-10512. ESM_LOW_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 14-31748. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding low priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding low priority level interrupt Reset Source: por_rst_n

14.9.8.2.2.10 ESM_HI_PRI Register

1 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt

Return to Summary Table

Table 14-31749. Instance Table

Instance Name	Physical Address
ESM0	**0042 0024h**

Figure 14-10513. ESM_HI_PRI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-31751. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding high priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding high priority level interrupt Reset Source: por_rst_n

14.9.8.2.2.11 ESM_LOW Register

1 ESM_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have oustanding low priority interrupts

Return to Summary Table

Table 14-31752. Instance Table

Instance Name	Physical Address
ESM0	**0042 0028h**

Figure 14-10514. ESM_LOW Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-31754. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.2.2.12 ESM_HI Register

1 ESM_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have oustanding high priority interrupts

Return to Summary Table

Table 14-31755. Instance Table

Instance Name	Physical Address
ESM0	**0042 002Ch**

Figure 14-10515. ESM_HI Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-31757. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.2.2.13 ESM_EOI Register

1 ESM_EOI Register (Offset = 30h) [reset = 0h]

End of Interrupt Register

Return to Summary Table

Table 14-31758. Instance Table

Instance Name	Physical Address
ESM0	**0042 0030h**

Figure 14-10516. ESM_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">KEY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31760. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	KEY	W	0h	This is the interrupt being serviced Reset Source: por_rst_n

14.9.8.2.2.14 ESM_PIN_CTRL Register

1 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error_pin_n output

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Table 14-31761. Instance Table

Instance Name	Physical Address
ESM0	**0042 0040h**

Figure 14-10517. ESM_PIN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PWM_EN				KEY			
R/W				R/W			
0h				0h			

Table 14-31763. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PWM_EN	R/W	0h	PWM enable Reset Source: por_rst_n
3:0	KEY	R/W	0h	Pin Control Key Reset Source: por_rst_n

14.9.8.2.2.15 ESM_PIN_STS Register

1 ESM_PIN_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error_pin_n output

Return to Summary Table

Table 14-31764. Instance Table

Instance Name	Physical Address
ESM0	**0042 0044h**

Figure 14-10518. ESM_PIN_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							VAL
NONE							R
0h							0h

Table 14-31766. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	VAL	R	0h	Value of the error_pin_n Reset Source: por_rst_n

14.9.8.2.2.16 ESM_PIN_CNTR Register

1 ESM_PIN_CNTR Register (Offset = 48h) [reset = 0h]

This register shows the current value of the error pin counter

Return to Summary Table

Table 14-31767. Instance Table

Instance Name	Physical Address
ESM0	**0042 0048h**

Figure 14-10519. ESM_PIN_CNTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31769. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.2.2.17 ESM_PIN_CNTR_PRE Register

1 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

This register contains the value that is loaded in to the Error Counter

Return to Summary Table

Table 14-31770. Instance Table

Instance Name	Physical Address
ESM0	**0042 004Ch**

Figure 14-10520. ESM_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31772. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.2.2.18 ESM_PWMH_PIN_CNTR Register

1 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

This register shows the current value of the error pin PWM high counter

Return to Summary Table

Table 14-31773. Instance Table

Instance Name	Physical Address
ESM0	**0042 0050h**

Figure 14-10521. ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-31775. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.2.2.19 ESM_PWMH_PIN_CNTR_PRE Register

1 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

This register contains the value that is loaded in to the Error PWM High Counter

Return to Summary Table

Table 14-31776. Instance Table

Instance Name	Physical Address
ESM0	**0042 0054h**

Figure 14-10522. ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31778. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.2.2.20 ESM_PWML_PIN_CNTR Register

1 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

This register shows the current value of the error pin PWM low counter

Return to Summary Table

Table 14-31779. Instance Table

Instance Name	Physical Address
ESM0	**0042 0058h**

Figure 14-10523. ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-31781. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.2.2.21 ESM_PWML_PIN_CNTR_PRE Register

1 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

This register contains the value that is loaded in to the Error PWM Low Counter

Return to Summary Table

Table 14-31782. Instance Table

Instance Name	Physical Address
ESM0	**0042 005Ch**

Figure 14-10524. ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31784. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.2.2.22 ESM_ERR_GRP_RAW_j Register

1 ESM_ERR_GRP_RAW_j Register (Offset = 0h + formula) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to Summary Table

Offset = 400h + (j * 20h); where j = 0 to 6d

Table 14-31785. Instance Table

Instance Name	Physical Address
ESM0	0042 0000h + formula

Figure 14-10525. ESM_ERR_GRP_RAW_j Name Register

31	30	29	28	27	26	25	24
STS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
STS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
STS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 14-31787. ESM_ERR_GRP_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W1TS	0h	This is the raw status/set for errors Group A Reset Source: por_rst_n

14.9.8.2.2.23 ESM_ERR_GRP_STS_j Register

1 ESM_ERR_GRP_STS_j Register (Offset = 4h + formula) [reset = 0h]

Error Enable and Clear Register

Return to Summary Table

Offset = 404h + (j * 20h); where j = 0 to 6d

Table 14-31788. Instance Table

Instance Name	Physical Address
ESM0	**0042 0004h + formula**

Figure 14-10526. ESM_ERR_GRP_STS_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31790. ESM_ERR_GRP_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the masked status/clear for errors in Group A Reset Source: por_rst_n

14.9.8.2.2.24 ESM_ERR_GRP_INTR_EN_SET_j Register

1 ESM_ERR_GRP_INTR_EN_SET_j Register (Offset = 8h + formula) [reset = 0h]

Level Error Enable Set Register

Return to Summary Table

Offset = 408h + (j * 20h); where j = 0 to 6d

Table 14-31791. Instance Table

Instance Name	Physical Address
ESM0	**0042 0008h + formula**

Figure 14-10527. ESM_ERR_GRP_INTR_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-31793. ESM_ERR_GRP_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the mask enable set for errors in Group A Reset Source: por_rst_n

14.9.8.2.2.25 ESM_ERR_GRP_INTR_EN_CLR_j Register

1 ESM_ERR_GRP_INTR_EN_CLR_j Register (Offset = Ch + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 40Ch + (j * 20h); where j = 0 to 6d

Table 14-31794. Instance Table

Instance Name	Physical Address
ESM0	**0042 000Ch + formula**

Figure 14-10528. ESM_ERR_GRP_INTR_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31796. ESM_ERR_GRP_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the mask enable clear for errors in Group A Reset Source: por_rst_n

14.9.8.2.2.26 ESM_ERR_GRP_INT_PRIO_j Register

1 ESM_ERR_GRP_INT_PRIO_j Register (Offset = 10h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 410h + (j * 20h); where j = 0 to 6d

Table 14-31797. Instance Table

Instance Name	Physical Address
ESM0	**0042 0010h + formula**

Figure 14-10529. ESM_ERR_GRP_INT_PRIO_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W							
0h							

Table 14-31799. ESM_ERR_GRP_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W	0h	This is interrupt priority for errors in Group A Reset Source: por_rst_n

14.9.8.2.2.27 ESM_ERR_GRP_PIN_EN_SET_j Register

1 ESM_ERR_GRP_PIN_EN_SET_j Register (Offset = 14h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 414h + (j * 20h); where j = 0 to 6d

Table 14-31800. Instance Table

Instance Name	Physical Address
ESM0	**0042 0014h + formula**

Figure 14-10530. ESM_ERR_GRP_PIN_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-31802. ESM_ERR_GRP_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the error pin influence enable set for errors in Group A Reset Source: por_rst_n

14.9.8.2.2.28 ESM_ERR_GRP_PIN_EN_CLR_j Register

1 ESM_ERR_GRP_PIN_EN_CLR_j Register (Offset = 18h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 418h + (j * 20h); where j = 0 to 6d

Table 14-31803. Instance Table

Instance Name	Physical Address
ESM0	**0042 0018h + formula**

Figure 14-10531. ESM_ERR_GRP_PIN_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31805. ESM_ERR_GRP_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the error pin influence enable clear for errors in Group A Reset Source: por_rst_n

14.9.8.3 ESM

ESM

14.9.8.3.1 ESM Summaries

ESM Summaries

Table 14-31806. ESM Registers, Base Address=0410 0000h, Length=4096

Offset	Length	Register Name	WKUP_ESM0 Physical Address
0h	32	ESM_PID	0410 0000h
4h	32	ESM_INFO	0410 0004h
8h	32	ESM_EN	0410 0008h
Ch	32	ESM_SFT_RST	0410 000Ch
10h	32	ESM_ERR_RAW	0410 0010h
14h	32	ESM_ERR_STS	0410 0014h
18h	32	ESM_ERR_EN_SET	0410 0018h
1Ch	32	ESM_ERR_EN_CLR	0410 001Ch
20h	32	ESM_LOW_PRI	0410 0020h
24h	32	ESM_HI_PRI	0410 0024h
28h	32	ESM_LOW	0410 0028h
2Ch	32	ESM_HI	0410 002Ch
30h	32	ESM_EOI	0410 0030h
40h	32	ESM_PIN_CTRL	0410 0040h
44h	32	ESM_PIN_STS	0410 0044h
48h	32	ESM_PIN_CNTR	0410 0048h
4Ch	32	ESM_PIN_CNTR_PRE	0410 004Ch
50h	32	ESM_PWMH_PIN_CNTR	0410 0050h
54h	32	ESM_PWMH_PIN_CNTR_PRE	0410 0054h
58h	32	ESM_PWML_PIN_CNTR	0410 0058h
5Ch	32	ESM_PWML_PIN_CNTR_PRE	0410 005Ch
0h	32	ESM_ERR_GRP_RAW_J	0410 0000h + formula
4h	32	ESM_ERR_GRP_STS_J	0410 0004h + formula
8h	32	ESM_ERR_GRP_INTR_EN_SET_J	0410 0008h + formula
Ch	32	ESM_ERR_GRP_INTR_EN_CLR_J	0410 000Ch + formula
10h	32	ESM_ERR_GRP_INT_PRIO_J	0410 0010h + formula
14h	32	ESM_ERR_GRP_PIN_EN_SET_J	0410 0014h + formula
18h	32	ESM_ERR_GRP_PIN_EN_CLR_J	0410 0018h + formula

14.9.8.3.2 ESM Registers

ESM Registers

14.9.8.3.2.1 ESM_PID Register

1 ESM_PID Register (Offset = 0h) [reset = 6FE04900h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-31807. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0000h**

Figure 14-10532. ESM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		FE0h			

23	22	21	20	19	18	17	16
FUNC							
R							
FE0h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					1h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-31809. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: por_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: por_rst_n
27:16	FUNC	R	FE0h	Module ID Reset Source: por_rst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: por_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: por_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: por_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: por_rst_n

14.9.8.3.2.2 ESM_INFO Register

1 ESM_INFO Register (Offset = 4h) [reset = 103h]

The Info Register gives the configuration Inforrmation of this ESM.

Return to Summary Table

Table 14-31810. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0004h**

Figure 14-10533. ESM_INFO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>LAST_RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PULSE_GROUPS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GROUPS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-31812. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	Indicates the Source of the last Reset Reset Source: por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	PULSE_GROUPS	R	1h	Number of Pulse Error Groups Reset Source: por_rst_n
7:0	GROUPS	R	3h	Total number of Error Groups Reset Source: por_rst_n

14.9.8.3.2.3 ESM_EN Register

1 ESM_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the initiator interrupt mask

Return to Summary Table

Table 14-31813. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0008h**

Figure 14-10534. ESM_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				R/W			
0h				0h			

Table 14-31815. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	R/W	0h	Global Enable Reset Source: por_rst_n

14.9.8.3.2.4 ESM_SFT_RST Register

1 ESM_SFT_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables

Return to Summary Table

Table 14-31816. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 000Ch**

Figure 14-10535. ESM_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 14-31818. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Global Soft Reset Reset Source: por_rst_n

14.9.8.3.2.5 ESM_ERR_RAW Register

1 ESM_ERR_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors

Return to Summary Table

Table 14-31819. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0010h**

Figure 14-10536. ESM_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					STS		
NONE					R/W1TS		
0h					0h		

Table 14-31821. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	STS	R/W1TS	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.3.2.6 ESM_ERR_STS Register

1 ESM_ERR_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register

Return to Summary Table

Table 14-31822. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0014h**

Figure 14-10537. ESM_ERR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TC		
0h					0h		

Table 14-31824. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TC	0h	This is the masked status/clear for config errors Reset Source: por_rst_n

14.9.8.3.2.7 ESM_ERR_EN_SET Register

1 ESM_ERR_EN_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register

Return to Summary Table

Table 14-31825. Instance Table

Instance Name	**Physical Address**
WKUP_ESM0	**0410 0018h**

Figure 14-10538. ESM_ERR_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TS		
0h					0h		

Table 14-31827. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TS	0h	This is the mask enable set for config errors Reset Source: por_rst_n

14.9.8.3.2.8 ESM_ERR_EN_CLR Register

1 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-31828. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 001Ch**

Figure 14-10539. ESM_ERR_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TC		
0h					0h		

Table 14-31830. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TC	0h	This is the mask enable clear for config errors Reset Source: por_rst_n

14.9.8.3.2.9 ESM_LOW_PRI Register

1 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt

Return to Summary Table

Table 14-31831. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0020h**

Figure 14-10540. ESM_LOW_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 14-31833. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding low priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding low priority level interrupt Reset Source: por_rst_n

14.9.8.3.2.10 ESM_HI_PRI Register

1 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt

Return to Summary Table

Table 14-31834. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0024h**

Figure 14-10541. ESM_HI_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 14-31836. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding high priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding high priority level interrupt Reset Source: por_rst_n

14.9.8.3.2.11 ESM_LOW Register

1 ESM_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have oustanding low priority interrupts

Return to Summary Table

Table 14-31837. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0028h**

Figure 14-10542. ESM_LOW Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-31839. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.3.2.12 ESM_HI Register

1 ESM_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have oustanding high priority interrupts

Return to Summary Table

Table 14-31840. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 002Ch**

Figure 14-10543. ESM_HI Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-31842. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.9.8.3.2.13 ESM_EOI Register

1 ESM_EOI Register (Offset = 30h) [reset = 0h]

End of Interrupt Register

Return to Summary Table

Table 14-31843. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0030h**

Figure 14-10544. ESM_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">KEY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31845. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	KEY	W	0h	This is the interrupt being serviced Reset Source: por_rst_n

14.9.8.3.2.14 ESM_PIN_CTRL Register

1 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error_pin_n output

Return to Summary Table

Table 14-31846. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0040h**

Figure 14-10545. ESM_PIN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PWM_EN				KEY			
R/W				R/W			
0h				0h			

Table 14-31848. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PWM_EN	R/W	0h	PWM enable Reset Source: por_rst_n
3:0	KEY	R/W	0h	Pin Control Key Reset Source: por_rst_n

14.9.8.3.2.15 ESM_PIN_STS Register

1 ESM_PIN_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error_pin_n output

Return to Summary Table

Table 14-31849. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0044h**

Figure 14-10546. ESM_PIN_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							VAL
NONE							R
0h							0h

Table 14-31851. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	VAL	R	0h	Value of the error_pin_n Reset Source: por_rst_n

14.9.8.3.2.16 ESM_PIN_CNTR Register

1 ESM_PIN_CNTR Register (Offset = 48h) [reset = 0h]

This register shows the current value of the error pin counter

Return to Summary Table

Table 14-31852. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0048h**

Figure 14-10547. ESM_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-31854. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.3.2.17 ESM_PIN_CNTR_PRE Register

1 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

This register contains the value that is loaded in to the Error Counter

Return to Summary Table

Table 14-31855. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 004Ch**

Figure 14-10548. ESM_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31857. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.3.2.18 ESM_PWMH_PIN_CNTR Register

1 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

This register shows the current value of the error pin PWM high counter

Return to Summary Table

Table 14-31858. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0050h**

Figure 14-10549. ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-31860. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.3.2.19 ESM_PWMH_PIN_CNTR_PRE Register

1 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

This register contains the value that is loaded in to the Error PWM High Counter

Return to Summary Table

Table 14-31861. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0054h**

Figure 14-10550. ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31863. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.3.2.20 ESM_PWML_PIN_CNTR Register

1 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

This register shows the current value of the error pin PWM low counter

Return to Summary Table

Table 14-31864. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0058h**

Figure 14-10551. ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-31866. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.9.8.3.2.21 ESM_PWML_PIN_CNTR_PRE Register

1 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

This register contains the value that is loaded in to the Error PWM Low Counter

Return to Summary Table

Table 14-31867. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 005Ch**

Figure 14-10552. ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-31869. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.9.8.3.2.22 ESM_ERR_GRP_RAW_j Register

1 ESM_ERR_GRP_RAW_j Register (Offset = 0h + formula) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to Summary Table

Offset = 400h + (j * 20h); where j = 0 to 2d

Table 14-31870. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0000h + formula**

Figure 14-10553. ESM_ERR_GRP_RAW_j Name Register

31	30	29	28	27	26	25	24
STS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
STS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
STS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 14-31872. ESM_ERR_GRP_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W1TS	0h	This is the raw status/set for errors Group A Reset Source: por_rst_n

14.9.8.3.2.23 ESM_ERR_GRP_STS_j Register

1 ESM_ERR_GRP_STS_j Register (Offset = 4h + formula) [reset = 0h]

Error Enable and Clear Register

Return to Summary Table

Offset = 404h + (j * 20h); where j = 0 to 2d

Table 14-31873. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0004h + formula**

Figure 14-10554. ESM_ERR_GRP_STS_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31875. ESM_ERR_GRP_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the masked status/clear for errors in Group A Reset Source: por_rst_n

14.9.8.3.2.24 ESM_ERR_GRP_INTR_EN_SET_j Register

1 ESM_ERR_GRP_INTR_EN_SET_j Register (Offset = 8h + formula) [reset = 0h]

Level Error Enable Set Register

Return to Summary Table

Offset = 408h + (j * 20h); where j = 0 to 2d

Table 14-31876. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0008h + formula**

Figure 14-10555. ESM_ERR_GRP_INTR_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-31878. ESM_ERR_GRP_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the mask enable set for errors in Group A Reset Source: por_rst_n

14.9.8.3.2.25 ESM_ERR_GRP_INTR_EN_CLR_j Register

1 ESM_ERR_GRP_INTR_EN_CLR_j Register (Offset = Ch + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 40Ch + (j * 20h); where j = 0 to 2d

Table 14-31879. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 000Ch + formula**

Figure 14-10556. ESM_ERR_GRP_INTR_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31881. ESM_ERR_GRP_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the mask enable clear for errors in Group A Reset Source: por_rst_n

14.9.8.3.2.26 ESM_ERR_GRP_INT_PRIO_j Register

1 ESM_ERR_GRP_INT_PRIO_j Register (Offset = 10h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 410h + (j * 20h); where j = 0 to 2d

Table 14-31882. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0010h + formula**

Figure 14-10557. ESM_ERR_GRP_INT_PRIO_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W							
0h							

Table 14-31884. ESM_ERR_GRP_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W	0h	This is interrupt priority for errors in Group A Reset Source: por_rst_n

14.9.8.3.2.27 ESM_ERR_GRP_PIN_EN_SET_j Register

1 ESM_ERR_GRP_PIN_EN_SET_j Register (Offset = 14h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 414h + (j * 20h); where j = 0 to 2d

Table 14-31885. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0014h + formula**

Figure 14-10558. ESM_ERR_GRP_PIN_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-31887. ESM_ERR_GRP_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the error pin influence enable set for errors in Group A Reset Source: por_rst_n

14.9.8.3.2.28 ESM_ERR_GRP_PIN_EN_CLR_j Register

1 ESM_ERR_GRP_PIN_EN_CLR_j Register (Offset = 18h + formula) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Offset = 418h + (j * 20h); where j = 0 to 2d

Table 14-31888. Instance Table

Instance Name	Physical Address
WKUP_ESM0	**0410 0018h + formula**

Figure 14-10559. ESM_ERR_GRP_PIN_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-31890. ESM_ERR_GRP_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the error pin influence enable clear for errors in Group A Reset Source: por_rst_n

14.9.8.4 MCRC64

MCRC64

14.9.8.4.1 MCRC64 Summaries

MCRC64 Summaries

Table 14-31891. CRC Registers, Base Address=3030 0000h, Length=4096

Offset	Length	Register Name	MCRC64_0 Physical Address	MCU_MCRC64_0 Physical Address
0h	32	CRC_CTRL0	3030 0000h	04D0 0000h
8h	32	CRC_CTRL1	3030 0008h	04D0 0008h
10h	32	CRC_CTRL2	3030 0010h	04D0 0010h
18h	32	CRC_INTS	3030 0018h	04D0 0018h
20h	32	CRC_INTR	3030 0020h	04D0 0020h
28h	32	CRC_STATUS	3030 0028h	04D0 0028h
30h	32	CRC_INT_OFFSET_REG	3030 0030h	04D0 0030h
38h	32	CRC_BUSY	3030 0038h	04D0 0038h
40h	32	CRC_PCOUNT_REG1	3030 0040h	04D0 0040h
44h	32	CRC_SCOUNT_REG1	3030 0044h	04D0 0044h
48h	32	CRC_CURSEC_REG1	3030 0048h	04D0 0048h
4Ch	32	CRC_WDTOPLD1	3030 004Ch	04D0 004Ch
50h	32	CRC_BCTOPLD1	3030 0050h	04D0 0050h
60h	32	CRC_PSA_SIGREGL1	3030 0060h	04D0 0060h
64h	32	CRC_PSA_SIGREGH1	3030 0064h	04D0 0064h
68h	32	CRC_REGL1	3030 0068h	04D0 0068h
6Ch	32	CRC_REGH1	3030 006Ch	04D0 006Ch
70h	32	CRC_PSA_SECSIGREGL1	3030 0070h	04D0 0070h
74h	32	CRC_PSA_SECSIGREGH1	3030 0074h	04D0 0074h
78h	32	CRC_RAW_DATAREGL1	3030 0078h	04D0 0078h
7Ch	32	CRC_RAW_DATAREGH1	3030 007Ch	04D0 007Ch
80h	32	CRC_PCOUNT_REG2	3030 0080h	04D0 0080h
84h	32	CRC_SCOUNT_REG2	3030 0084h	04D0 0084h
88h	32	CRC_CURSEC_REG2	3030 0088h	04D0 0088h
8Ch	32	CRC_WDTOPLD2	3030 008Ch	04D0 008Ch
90h	32	CRC_BCTOPLD2	3030 0090h	04D0 0090h
A0h	32	CRC_PSA_SIGREGL2	3030 00A0h	04D0 00A0h
A4h	32	CRC_PSA_SIGREGH2	3030 00A4h	04D0 00A4h
A8h	32	CRC_REGL2	3030 00A8h	04D0 00A8h
ACh	32	CRC_REGH2	3030 00ACh	04D0 00ACh
B0h	32	CRC_PSA_SECSIGREGL2	3030 00B0h	04D0 00B0h
B4h	32	CRC_PSA_SECSIGREGH2	3030 00B4h	04D0 00B4h
B8h	32	CRC_RAW_DATAREGL2	3030 00B8h	04D0 00B8h
BCh	32	CRC_RAW_DATAREGH2	3030 00BCh	04D0 00BCh
C0h	32	CRC_PCOUNT_REG3	3030 00C0h	04D0 00C0h
C4h	32	CRC_SCOUNT_REG3	3030 00C4h	04D0 00C4h
C8h	32	CRC_CURSEC_REG3	3030 00C8h	04D0 00C8h

Table 14-31891. CRC Registers, Base Address=3030 0000h, Length=4096 (continued)

Offset	Length	Register Name	MCRC64_0 Physical Address	MCU_MCRC64_0 Physical Address
CCh	32	CRC_WDTOPLD3	3030 00CCh	04D0 00CCh
D0h	32	CRC_BCTOPLD3	3030 00D0h	04D0 00D0h
E0h	32	CRC_PSA_SIGREGL3	3030 00E0h	04D0 00E0h
E4h	32	CRC_PSA_SIGREGH3	3030 00E4h	04D0 00E4h
E8h	32	CRC_REGL3	3030 00E8h	04D0 00E8h
ECh	32	CRC_REGH3	3030 00ECh	04D0 00ECh
F0h	32	CRC_PSA_SECSIGREGL3	3030 00F0h	04D0 00F0h
F4h	32	CRC_PSA_SECSIGREGH3	3030 00F4h	04D0 00F4h
F8h	32	CRC_RAW_DATAREGL3	3030 00F8h	04D0 00F8h
FCh	32	CRC_RAW_DATAREGH3	3030 00FCh	04D0 00FCh
100h	32	CRC_PCOUNT_REG4	3030 0100h	04D0 0100h
104h	32	CRC_SCOUNT_REG4	3030 0104h	04D0 0104h
108h	32	CRC_CURSEC_REG4	3030 0108h	04D0 0108h
10Ch	32	CRC_WDTOPLD4	3030 010Ch	04D0 010Ch
110h	32	CRC_BCTOPLD4	3030 0110h	04D0 0110h
120h	32	CRC_PSA_SIGREGL4	3030 0120h	04D0 0120h
124h	32	CRC_PSA_SIGREGH4	3030 0124h	04D0 0124h
128h	32	CRC_REGL4	3030 0128h	04D0 0128h
12Ch	32	CRC_REGH4	3030 012Ch	04D0 012Ch
130h	32	CRC_PSA_SECSIGREGL4	3030 0130h	04D0 0130h
134h	32	CRC_PSA_SECSIGREGH4	3030 0134h	04D0 0134h
138h	32	CRC_RAW_DATAREGL4	3030 0138h	04D0 0138h
13Ch	32	CRC_RAW_DATAREGH4	3030 013Ch	04D0 013Ch
140h	32	CRC_MBUS_SEL	3030 0140h	04D0 0140h
200h	32	CRC_I0_PSA_SIGREG1_CPY_J	3030 0200h + formula	04D0 0200h + formula
280h	32	CRC_I0_PSA_SIGREG2_CPY_J	3030 0280h + formula	04D0 0280h + formula
300h	32	CRC_I0_PSA_SIGREG3_CPY_J	3030 0300h + formula	04D0 0300h + formula
380h	32	CRC_I0_PSA_SIGREG4_CPY_J	3030 0380h + formula	04D0 0380h + formula

14.9.8.4.2 MCRC64 Registers

MCRC64 Registers

14.9.8.4.2.1 CRC_CTRL0 Register

1 CRC_CTRL0 Register (Offset = 0h) [reset = 0h]

CRC Global Control Register 0

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Table 14-31892. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0000h**
MCU_MCRC64_0	**04D0 0000h**

Figure 14-10560. CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_PSA_SWRE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_PSA_SWRE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_PSA_SWRE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_PSA_SWRE
NONE							R/W
0h							0h

Table 14-31894. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_PSA_SWRE	R/W	0h	Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
23:17	RESERVED	NONE	0h	Reserved
16	CH3_PSA_SWRE	R/W	0h	Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
15:9	RESERVED	NONE	0h	Reserved
8	CH2_PSA_SWRE	R/W	0h	Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset

Table 14-31894. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE	0h	Reserved
0	CH1_PSA_SWRE	R/W	0h	Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset

14.9.8.4.2.2 CRC_CTRL1 Register

1 CRC_CTRL1 Register (Offset = 8h) [reset = 0h]

CRC Global Control Register 1

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Table 14-31895. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0008h**
MCU_MCRC64_0	**04D0 0008h**

Figure 14-10561. CRC_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PWDN
NONE							R/W
0h							0h

Table 14-31897. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PWDN	R/W	0h	Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode. 1 = MCRC is in power down mode.

14.9.8.4.2.3 CRC_CTRL2 Register

1 CRC_CTRL2 Register (Offset = 10h) [reset = 0h]

Data capture mode is especially useful when it is used in conjunction when data trace (CH1_TRACEEN) for channel 1. The seed value can be planted in PSA Signature Register during data capture mode by writing a seed value into PSA Signature Register. Data trace enable bit is then set to snoop and compress any read transaction on Data buses. When trace enable bit is set, CH1_MODE is automatically reset to data capture mode. To change mode from one to another in the middle of an on-going mode user should take the following steps:

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Table 14-31898. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0010h**
MCU_MCRC64_0	**04D0 0010h**

Figure 14-10562. CRC_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED						CH4_MODE	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						CH3_MODE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						CH2_MODE	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED			CH1_TRACEEN	RESERVED		CH1_MODE	
NONE			R/W	NONE		R/W	
0h			0h	0h		0h	

Table 14-31900. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CH4_MODE	R/W	0h	Channel 4 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode For all four channels the seed value can be first planted into PSA register before the Channel Mode is switched to Full-CPU mode since host CPU controls the amount of data for compression. During AUTO mode, the PSA register is automatically reset to zero at the end of each sector compression.
23:18	RESERVED	NONE	0h	Reserved

Table 14-31900. CRC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	CH3_MODE	R/W	0h	Channel 3 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
15:10	RESERVED	NONE	0h	Reserved
9:8	CH2_MODE	R/W	0h	Channel 2 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TRACEEN	R/W	0h	Channel 1 Data Trace Enable When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable
3:2	RESERVED	NONE	0h	Reserved
1:0	CH1_MODE	R/W	0h	Channel 1 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode

14.9.8.4.2.4 CRC_INTS Register

1 CRC_INTS Register (Offset = 18h) [reset = 0h]

CRC Interrupt Enable Set Register

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Table 14-31901. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0018h**
MCU_MCRC64_0	**04D0 0018h**

Figure 14-10563. CRC_INTS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENS_	CH4_UNDERENS	CH4_OVERENS	CH4_CRC_FAILENS	CH4_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT_ENS	CH3_UNDERENS	CH3_OVERENS	CH3_CRC_FAILENS	CH3_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT_ENS_	CH2_UNDERENS	CH2_OVERENS	CH2_CRC_FAILENS	CH2_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT_ENS_	CH1_UNDERENS	CH1_OVERENS	CH1_CRC_FAILENS	CH1_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-31903. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENS_	R/W1TS	0h	Channel 4 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENS	R/W1TS	0h	Channel 4 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENS	R/W1TS	0h	Channel 4 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-31903. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENS	R/W1TS	0h	Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENS	R/W1TS	0h	Channel 4 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENS	R/W1TS	0h	Channel 3 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENS	R/W1TS	0h	Channel 3 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENS	R/W1TS	0h	Channel 3 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENS	R/W1TS	0h	Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENS	R/W1TS	0h	Channel 3 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENS_	R/W1TS	0h	Channel 2 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-31903. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENS	R/W1TS	0h	Channel 2 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENS	R/W1TS	0h	Channel 2 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENS	R/W1TS	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENS	R/W1TS	0h	Channel 2 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENS_	R/W1TS	0h	Channel 1 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENS	R/W1TS	0h	Channel 1 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENS	R/W1TS	0h	Channel 1 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENS	R/W1TS	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-31903. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENS	R/W1TS	0h	Channel 1 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable

14.9.8.4.2.5 CRC_INTR Register

1 CRC_INTR Register (Offset = 20h) [reset = 0h]

CRC Interrupt Enable Reset Register

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Table 14-31904. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0020h**
MCU_MCRC64_0	**04D0 0020h**

Figure 14-10564. CRC_INTR Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENR	CH4_UNDERENR	CH4_OVERENR	CH4_CRC_FAILENR	CH4_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT_ENR_	CH3_UNDERENR	CH3_OVERENR	CH3_CRC_FAILENR	CH3_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT_ENR_	CH2_UNDERENR	CH2_OVERENR	CH2_CRC_FAILENR	CH2_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT_ENR_	CH1_UNDERENR	CH1_OVERENR	CH1_CRC_FAILENR	CH1_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-31906. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENR	R/W1TC	0h	Channel 4 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENR	R/W1TC	0h	Channel 4 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENR	R/W1TC	0h	Channel 4 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-31906. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENR	R/W1TC	0h	Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENR	R/W1TC	0h	Channel 4 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENR_	R/W1TC	0h	Channel 3 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENR	R/W1TC	0h	Channel 3 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENR	R/W1TC	0h	Channel 3 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENR	R/W1TC	0h	Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENR	R/W1TC	0h	Channel 3 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENR_	R/W1TC	0h	Channel 2 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-31906. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENR	R/W1TC	0h	Channel 2 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENR	R/W1TC	0h	Channel 2 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENR	R/W1TC	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENR	R/W1TC	0h	Channel 2 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENR_	R/W1TC	0h	Channel 1 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENR	R/W1TC	0h	Channel 1 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENR	R/W1TC	0h	Channel 1 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENR	R/W1TC	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-31906. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENR	R/W1TC	0h	Channel 1 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable

14.9.8.4.2.6 CRC_STATUS Register

1 CRC_STATUS Register (Offset = 28h) [reset = 0h]

CRC Interrupt Status Register

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Table 14-31907. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0028h**
MCU_MCRC64_0	**04D0 0028h**

Figure 14-10565. CRC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT	CH4_UNDER	CH4_OVER	CH4_CRC_FAIL	CH4_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT	CH3_UNDER	CH3_OVER	CH3_CRC_FAIL	CH3_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT	CH2_UNDER	CH2_OVER	CH2_CRC_FAIL	CH2_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT	CH1_UNDER	CH1_OVER	CH1_CRC_FAIL	CH1_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-31909. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT	R/W1TC	0h	Channel 4 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
27	CH4_UNDER	R/W1TC	0h	Channel 4 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
26	CH4_OVER	R/W1TC	0h	Channel 4 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
25	CH4_CRC_FAIL	R/W1TC	0h	Channel 4 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active

Table 14-31909. CRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CH4_CCIT	R/W1TC	0h	Channel 4 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT	R/W1TC	0h	Channel 3 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
19	CH3_UNDER	R/W1TC	0h	Channel 3 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
18	CH3_OVER	R/W1TC	0h	Channel 3 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
17	CH3_CRC_FAIL	R/W1TC	0h	Channel 3 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
16	CH3_CCIT	R/W1TC	0h	Channel 3 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT	R/W1TC	0h	Channel 2 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
11	CH2_UNDER	R/W1TC	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
10	CH2_OVER	R/W1TC	0h	Channel 2 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
9	CH2_CRC_FAIL	R/W1TC	0h	Channel 2 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
8	CH2_CCIT	R/W1TC	0h	Channel 2 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT	R/W1TC	0h	Channel 1 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
3	CH1_UNDER	R/W1TC	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
2	CH1_OVER	R/W1TC	0h	Channel 1 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active

Table 14-31909. CRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CH1_CRC_FAIL	R/W1TC	0h	Channel 1 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
0	CH1_CCIT	R/W1TC	0h	Channel 1 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active

14.9.8.4.2.7 CRC_INT_OFFSET_REG Register

1 CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = 0h]

CRC Interrupt Offset

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Table 14-31910. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0030h**
MCU_MCRC64_0	**04D0 0030h**

Figure 14-10566. CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CRC							
R							
0h							

Table 14-31912. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CRC	R	0h	Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clears the respective interrupt flag.

14.9.8.4.2.8 CRC_BUSY Register

1 CRC_BUSY Register (Offset = 38h) [reset = 0h]

CRC Busy Register

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Table 14-31913. Instance Table

Instance Name	**Physical Address**
MCRC64_0	**3030 0038h**
MCU_MCRC64_0	**04D0 0038h**

Figure 14-10567. CRC_BUSY Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_BUSY
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_BUSY
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_BUSY
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_BUSY
NONE							R
0h							0h

Table 14-31915. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
23:17	RESERVED	NONE	0h	Reserved
16	CH3_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
15:9	RESERVED	NONE	0h	Reserved
8	CH2_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
7:1	RESERVED	NONE	0h	Reserved
0	CH1_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.

14.9.8.4.2.9 CRC_PCOUNT_REG1 Register

1 CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = 0h]

CRC Pattern Counter Preload Register1

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Table 14-31916. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0040h**
MCU_MCRC64_0	**04D0 0040h**

Figure 14-10568. CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT1							
R/W							
0h							

Table 14-31918. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT1	R/W	0h	Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.8.4.2.10 CRC_SCOUNT_REG1 Register

1 CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = 0h]

CRC Sector Counter Preload Register1

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Table 14-31919. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0044h**
MCU_MCRC64_0	**04D0 0044h**

Figure 14-10569. CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT1							
R/W							
0h							

Table 14-31921. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT1	R/W	0h	Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.8.4.2.11 CRC_CURSEC_REG1 Register

1 CRC_CURSEC_REG1 Register (Offset = 48h) [reset = 0h]

CRC Current Sector Register 1

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Table 14-31922. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0048h**
MCU_MCRC64_0	**04D0 0048h**

Figure 14-10570. CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC1							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC1							
R							
0h							

Table 14-31924. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC1	R	0h	Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.8.4.2.12 CRC_WDTOPLD1 Register

1 CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = 0h]

CRC channel 1 Watchdog Timeout Preload Register A

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Table 14-31925. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 004Ch**
MCU_MCRC64_0	**04D0 004Ch**

Figure 14-10571. CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD1							
R/W							
0h							

Table 14-31927. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD1	R/W	0h	Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.8.4.2.13 CRC_BCTOPLD1 Register

1 CRC_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

CRC channel 1 Block Complete Timeout Preload Register B

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Table 14-31928. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0050h**
MCU_MCRC64_0	**04D0 0050h**

Figure 14-10572. CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD1							
R/W							
0h							

Table 14-31930. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD1	R/W	0h	Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

14.9.8.4.2.14 CRC_PSA_SIGREGL1 Register

1 CRC_PSA_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Channel 1 PSA signature low register

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Table 14-31931. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0060h**
MCU_MCRC64_0	**04D0 0060h**

Figure 14-10573. CRC_PSA_SIGREGL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASIG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASIG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASIG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASIG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31933. CRC_PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1	R/W	0h	Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register.

14.9.8.4.2.15 CRC_PSA_SIGREGH1 Register

1 CRC_PSA_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Channel 1 PSA signature high register

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Table 14-31934. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0064h**
MCU_MCRC64_0	**04D0 0064h**

Figure 14-10574. CRC_PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASIG1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1_63_32							
R/W							
0h							

Table 14-31936. CRC_PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1_63_32	R/W	0h	Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register.

14.9.8.4.2.16 CRC_REGL1 Register

1 CRC_REGL1 Register (Offset = 68h) [reset = 0h]

Channel 1 CRC value low register

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Table 14-31937. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0068h**
MCU_MCRC64_0	**04D0 0068h**

Figure 14-10575. CRC_REGL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31939. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1	R/W	0h	Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register.

14.9.8.4.2.17 CRC_REGH1 Register

1 CRC_REGH1 Register (Offset = 6Ch) [reset = 0h]

Channel 1 CRC value high register

Return to Summary Table

Table 14-31940. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 006Ch**
MCU_MCRC64_0	**04D0 006Ch**

Figure 14-10576. CRC_REGH1 Name Register

31	30	29	28	27	26	25	24
CRC1_47_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1_47_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1_47_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1_47_32							
R/W							
0h							

Table 14-31942. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_47_32	R/W	0h	Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register.

14.9.8.4.2.18 CRC_PSA_SECSIGREGL1 Register

1 CRC_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Channel 1 PSA sector signature low register

Return to Summary Table

Table 14-31943. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0070h**
MCU_MCRC64_0	**04D0 0070h**

Figure 14-10577. CRC_PSA_SECSIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG1							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG1							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG1							
R							
0h							

Table 14-31945. CRC_PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1	R	0h	Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register.

14.9.8.4.2.19 CRC_PSA_SECSIGREGH1 Register

1 CRC_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Channel 1 PSA sector signature high register

Return to Summary Table

Table 14-31946. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0074h**
MCU_MCRC64_0	**04D0 0074h**

Figure 14-10578. CRC_PSA_SECSIGREGH1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASECSIG1_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASECSIG1_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASECSIG1_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASECSIG1_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31948. CRC_PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_63_32	R	0h	Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register.

14.9.8.4.2.20 CRC_RAW_DATAREGL1 Register

1 CRC_RAW_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Channel 1 Raw Data Low Register

Return to Summary Table

Table 14-31949. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0078h**
MCU_MCRC64_0	**04D0 0078h**

Figure 14-10579. CRC_RAW_DATAREGL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RAW_DATA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RAW_DATA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RAW_DATA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAW_DATA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31951. CRC_RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1	R	0h	Channel 1 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.8.4.2.21 CRC_RAW_DATAREGH1 Register

1 CRC_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Channel 1 Raw Data High Register

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Table 14-31952. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 007Ch**
MCU_MCRC64_0	**04D0 007Ch**

Figure 14-10580. CRC_RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1_47_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1_47_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1_47_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1_47_32							
R							
0h							

Table 14-31954. CRC_RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_47_32	R	0h	Channel 1 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.8.4.2.22 CRC_PCOUNT_REG2 Register

1 CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = 0h]

CRC Pattern Counter Preload Register2

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Table 14-31955. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0080h**
MCU_MCRC64_0	**04D0 0080h**

Figure 14-10581. CRC_PCOUNT_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CRC_PAT_COUNT2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31957. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT2	R/W	0h	CRC Pattern Counter Preload Register 2 This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.8.4.2.23 CRC_SCOUNT_REG2 Register

1 CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = 0h]

CRC Sector Counter Preload Register2

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Table 14-31958. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0084h**
MCU_MCRC64_0	**04D0 0084h**

Figure 14-10582. CRC_SCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT2							
R/W							
0h							

Table 14-31960. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT2	R/W	0h	Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.8.4.2.24 CRC_CURSEC_REG2 Register

1 CRC_CURSEC_REG2 Register (Offset = 88h) [reset = 0h]

CRC Current Sector Register 2

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Table 14-31961. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0088h**
MCU_MCRC64_0	**04D0 0088h**

Figure 14-10583. CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_CURSEC2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_CURSEC2							
R							
0h							

Table 14-31963. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC2	R	0h	Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.8.4.2.25 CRC_WDTOPLD2 Register

1 CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = 0h]

CRC channel 2 Watchdog Timeout Preload Register

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Table 14-31964. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 008Ch**
MCU_MCRC64_0	**04D0 008Ch**

Figure 14-10584. CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD2							
R/W							
0h							

Table 14-31966. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD2	R/W	0h	Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.8.4.2.26 CRC_BCTOPLD2 Register

1 CRC_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

CRC channel 2 Block Complete Timeout Preload Register

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Table 14-31967. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0090h**
MCU_MCRC64_0	**04D0 0090h**

Figure 14-10585. CRC_BCTOPLD2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31969. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD2	R/W	0h	Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.8.4.2.27 CRC_PSA_SIGREGL2 Register

1 CRC_PSA_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Channel 2 PSA signature low register

Return to Summary Table

Table 14-31970. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00A0h**
MCU_MCRC64_0	**04D0 00A0h**

Figure 14-10586. CRC_PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASIG2							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2							
R/W							
0h							

Table 14-31972. CRC_PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2	R/W	0h	Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

14.9.8.4.2.28 CRC_PSA_SIGREGH2 Register

1 CRC_PSA_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Channel 2 PSA signature high register

Return to Summary Table

Table 14-31973. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00A4h**
MCU_MCRC64_0	**04D0 00A4h**

Figure 14-10587. CRC_PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASIG2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2_63_32							
R/W							
0h							

Table 14-31975. CRC_PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2_63_32	R/W	0h	Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

14.9.8.4.2.29 CRC_REGL2 Register

1 CRC_REGL2 Register (Offset = A8h) [reset = 0h]

Channel 2 CRC value low register

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Table 14-31976. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00A8h**
MCU_MCRC64_0	**04D0 00A8h**

Figure 14-10588. CRC_REGL2 Name Register

31	30	29	28	27	26	25	24
CRC2							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2							
R/W							
0h							

Table 14-31978. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2	R/W	0h	Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

14.9.8.4.2.30 CRC_REGH2 Register

1 CRC_REGH2 Register (Offset = ACh) [reset = 0h]

Channel 2 CRC value high register

Return to Summary Table

Table 14-31979. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00ACh**
MCU_MCRC64_0	**04D0 00ACh**

Figure 14-10589. CRC_REGH2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CRC2_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC2_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC2_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC2_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31981. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_63_32	R/W	0h	Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

14.9.8.4.2.31 CRC_PSA_SECSIGREGL2 Register

1 CRC_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Channel 2 PSA sector signature low register

Return to Summary Table

Table 14-31982. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00B0h**
MCU_MCRC64_0	**04D0 00B0h**

Figure 14-10590. CRC_PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2							
R							
0h							

Table 14-31984. CRC_PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2	R	0h	Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

14.9.8.4.2.32 CRC_PSA_SECSIGREGH2 Register

1 CRC_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Channel 2 PSA sector signature high register

Return to Summary Table

Table 14-31985. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00B4h**
MCU_MCRC64_0	**04D0 00B4h**

Figure 14-10591. CRC_PSA_SECSIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2_63_32							
R							
0h							

Table 14-31987. CRC_PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_63_32	R	0h	Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

14.9.8.4.2.33 CRC_RAW_DATAREGL2 Register

1 CRC_RAW_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Channel 2 Raw Data Low Register

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Table 14-31988. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00B8h**
MCU_MCRC64_0	**04D0 00B8h**

Figure 14-10592. CRC_RAW_DATAREGL2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2							
R							
0h							

Table 14-31990. CRC_RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2	R	0h	Channel 2 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.8.4.2.34 CRC_RAW_DATAREGH2 Register

1 CRC_RAW_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Channel 2 Raw Data High Register

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Table 14-31991. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00BCh**
MCU_MCRC64_0	**04D0 00BCh**

Figure 14-10593. CRC_RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2_63_32							
R							
0h							

Table 14-31993. CRC_RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_63_32	R	0h	Channel 2 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.8.4.2.35 CRC_PCOUNT_REG3 Register

1 CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = 0h]

CRC Pattern Counter Preload Register3

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Table 14-31994. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00C0h**
MCU_MCRC64_0	**04D0 00C0h**

Figure 14-10594. CRC_PCOUNT_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-31996. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT3	R/W	0h	Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.8.4.2.36 CRC_SCOUNT_REG3 Register

1 CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = 0h]

CRC Sector Counter Preload Register3

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Table 14-31997. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00C4h**
MCU_MCRC64_0	**04D0 00C4h**

Figure 14-10595. CRC_SCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT3							
R/W							
0h							

Table 14-31999. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT3	R/W	0h	Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.8.4.2.37 CRC_CURSEC_REG3 Register

1 CRC_CURSEC_REG3 Register (Offset = C8h) [reset = 0h]

CRC Current Sector Register 3

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Table 14-32000. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00C8h**
MCU_MCRC64_0	**04D0 00C8h**

Figure 14-10596. CRC_CURSEC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC3							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC3							
R							
0h							

Table 14-32002. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC3	R	0h	Channel 3 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.8.4.2.38 CRC_WDTOPLD3 Register

1 CRC_WDTOPLD3 Register (Offset = CCh) [reset = 0h]

CRC channel 3 Watchdog Timeout Preload Register

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Table 14-32003. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00CCh**
MCU_MCRC64_0	**04D0 00CCh**

Figure 14-10597. CRC_WDTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD3							
R/W							
0h							

Table 14-32005. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD3	R/W	0h	Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.8.4.2.39 CRC_BCTOPLD3 Register

1 CRC_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

CRC channel 3 Block Complete Timeout Preload Register

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Table 14-32006. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00D0h**
MCU_MCRC64_0	**04D0 00D0h**

Figure 14-10598. CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD3							
R/W							
0h							

Table 14-32008. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD3	R/W	0h	Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.8.4.2.40 CRC_PSA_SIGREGL3 Register

1 CRC_PSA_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Channel 3 PSA signature low register

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Table 14-32009. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00E0h**
MCU_MCRC64_0	**04D0 00E0h**

Figure 14-10599. CRC_PSA_SIGREGL3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASIG3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASIG3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASIG3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASIG3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32011. CRC_PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3	R/W	0h	Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG3[31:0] register.

14.9.8.4.2.41 CRC_PSA_SIGREGH3 Register

1 CRC_PSA_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Channel 3 PSA signature high register

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Table 14-32012. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00E4h**
MCU_MCRC64_0	**04D0 00E4h**

Figure 14-10600. CRC_PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASIG3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3_63_32							
R/W							
0h							

Table 14-32014. CRC_PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3_63_32	R/W	0h	Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG3[63:32] register.

14.9.8.4.2.42 CRC_REGL3 Register

1 CRC_REGL3 Register (Offset = E8h) [reset = 0h]

Channel 3 CRC value low register

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Table 14-32015. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00E8h**
MCU_MCRC64_0	**04D0 00E8h**

Figure 14-10601. CRC_REGL3 Name Register

31	30	29	28	27	26	25	24
CRC3							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3							
R/W							
0h							

Table 14-32017. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3	R/W	0h	Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC3[31:0] register.

14.9.8.4.2.43 CRC_REGH3 Register

1 CRC_REGH3 Register (Offset = ECh) [reset = 0h]

Channel 3 CRC value high register

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Table 14-32018. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00ECh**
MCU_MCRC64_0	**04D0 00ECh**

Figure 14-10602. CRC_REGH3 Name Register

31	30	29	28	27	26	25	24
CRC3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3_63_32							
R/W							
0h							

Table 14-32020. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3_63_32	R/W	0h	Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC3[63:32] register.

14.9.8.4.2.44 CRC_PSA_SECSIGREGL3 Register

1 CRC_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Channel 3 PSA sector signature low register

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Table 14-32021. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00F0h**
MCU_MCRC64_0	**04D0 00F0h**

Figure 14-10603. CRC_PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3							
R							
0h							

Table 14-32023. CRC_PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3	R	0h	Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG3[31:0] register.

14.9.8.4.2.45 CRC_PSA_SECSIGREGH3 Register

1 CRC_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Channel 3 PSA sector signature high register

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Table 14-32024. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00F4h**
MCU_MCRC64_0	**04D0 00F4h**

Figure 14-10604. CRC_PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3_63_32							
R							
0h							

Table 14-32026. CRC_PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3_63_32	R	0h	Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG3[63:32] register.

14.9.8.4.2.46 CRC_RAW_DATAREGL3 Register

1 CRC_RAW_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Channel 3 Raw Data Low Register

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Table 14-32027. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00F8h**
MCU_MCRC64_0	**04D0 00F8h**

Figure 14-10605. CRC_RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3							
R							
0h							

Table 14-32029. CRC_RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3	R	0h	Channel 3 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.8.4.2.47 CRC_RAW_DATAREGH3 Register

1 CRC_RAW_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Channel 3 Raw Data High Register

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Table 14-32030. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 00FCh**
MCU_MCRC64_0	**04D0 00FCh**

Figure 14-10606. CRC_RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3_63_32							
R							
0h							

Table 14-32032. CRC_RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3_63_32	R	0h	Channel 3 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.8.4.2.48 CRC_PCOUNT_REG4 Register

1 CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = 0h]

CRC Pattern Counter Preload Register4

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Table 14-32033. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0100h**
MCU_MCRC64_0	**04D0 0100h**

Figure 14-10607. CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CRC_PAT_COUNT4			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_PAT_COUNT4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_PAT_COUNT4							
R/W							
0h							

Table 14-32035. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT4	R/W	0h	Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.8.4.2.49 CRC_SCOUNT_REG4 Register

1 CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = 0h]

CRC Sector Counter Preload Register4

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Table 14-32036. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0104h**
MCU_MCRC64_0	**04D0 0104h**

Figure 14-10608. CRC_SCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_SEC_COUNT4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_SEC_COUNT4							
R/W							
0h							

Table 14-32038. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT4	R/W	0h	Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.8.4.2.50 CRC_CURSEC_REG4 Register

1 CRC_CURSEC_REG4 Register (Offset = 108h) [reset = 0h]

CRC Current Sector Register 4

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Table 14-32039. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0108h**
MCU_MCRC64_0	**04D0 0108h**

Figure 14-10609. CRC_CURSEC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC4							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC4							
R							
0h							

Table 14-32041. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC4	R	0h	In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.

14.9.8.4.2.51 CRC_WDTOPLD4 Register

1 CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = 0h]

CRC channel 4 Watchdog Timeout Preload Register

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Table 14-32042. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 010Ch**
MCU_MCRC64_0	**04D0 010Ch**

Figure 14-10610. CRC_WDTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD4							
R/W							
0h							

Table 14-32044. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD4	R/W	0h	This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.8.4.2.52 CRC_BCTOPLD4 Register

1 CRC_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

CRC channel 4 Block Complete Timeout Preload Register

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Table 14-32045. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0110h**
MCU_MCRC64_0	**04D0 0110h**

Figure 14-10611. CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD4							
R/W							
0h							

Table 14-32047. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD4	R/W	0h	This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.8.4.2.53 CRC_PSA_SIGREGL4 Register

1 CRC_PSA_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Channel 4 PSA signature low register

Return to Summary Table

Table 14-32048. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0120h**
MCU_MCRC64_0	**04D0 0120h**

Figure 14-10612. CRC_PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASIG4							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4							
R/W							
0h							

Table 14-32050. CRC_PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4	R/W	0h	This register contains the value stored at PSASIG4[31:0] register.

14.9.8.4.2.54 CRC_PSA_SIGREGH4 Register

1 CRC_PSA_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Channel 4 PSA signature high register

Return to Summary Table

Table 14-32051. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0124h**
MCU_MCRC64_0	**04D0 0124h**

Figure 14-10613. CRC_PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASIG4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4_63_32							
R/W							
0h							

Table 14-32053. CRC_PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4_63_32	R/W	0h	This register contains the value stored at PSASIG4[63:32] register.

14.9.8.4.2.55 CRC_REGL4 Register

1 CRC_REGL4 Register (Offset = 128h) [reset = 0h]

Channel 4 CRC value low register

Return to Summary Table

Table 14-32054. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0128h**
MCU_MCRC64_0	**04D0 0128h**

Figure 14-10614. CRC_REGL4 Name Register

31	30	29	28	27	26	25	24
CRC4							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4							
R/W							
0h							

Table 14-32056. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4	R/W	0h	Channel 4 CRC Value Low Register.

14.9.8.4.2.56 CRC_REGH4 Register

1 CRC_REGH4 Register (Offset = 12Ch) [reset = 0h]

Channel 4 CRC value high register

Return to Summary Table

Table 14-32057. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 012Ch**
MCU_MCRC64_0	**04D0 012Ch**

Figure 14-10615. CRC_REGH4 Name Register

31	30	29	28	27	26	25	24
CRC4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4_63_32							
R/W							
0h							

Table 14-32059. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4_63_32	R/W	0h	Channel 4 CRC Value High Register.

14.9.8.4.2.57 CRC_PSA_SECSIGREGL4 Register

1 CRC_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Channel 4 PSA sector signature low register

Return to Summary Table

Table 14-32060. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0130h**
MCU_MCRC64_0	**04D0 0130h**

Figure 14-10616. CRC_PSA_SECSIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG4							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG4							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG4							
R							
0h							

Table 14-32062. CRC_PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4	R	0h	Channel 4 PSA Sector Signature Low Register.

14.9.8.4.2.58 CRC_PSA_SECSIGREGH4 Register

1 CRC_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Channel 4 PSA sector signature high register

Return to Summary Table

Table 14-32063. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0134h**
MCU_MCRC64_0	**04D0 0134h**

Figure 14-10617. CRC_PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG4_63_32							
R							
0h							

Table 14-32065. CRC_PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4_63_32	R	0h	Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG4[63:32] register.

14.9.8.4.2.59 CRC_RAW_DATAREGL4 Register

1 CRC_RAW_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Channel 4 Raw Data Low Register

Return to Summary Table

Table 14-32066. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0138h**
MCU_MCRC64_0	**04D0 0138h**

Figure 14-10618. CRC_RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4							
R							
0h							

Table 14-32068. CRC_RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4	R	0h	Channel 4 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.8.4.2.60 CRC_RAW_DATAREGH4 Register

1 CRC_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Channel 4 Raw Data High Register

Return to Summary Table

Table 14-32069. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 013Ch**
MCU_MCRC64_0	**04D0 013Ch**

Figure 14-10619. CRC_RAW_DATAREGH4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4_63_32							
R							
0h							

Table 14-32071. CRC_RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4_63_32	R	0h	Channel 4 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.8.4.2.61 CRC_MBUS_SEL Register

1 CRC_MBUS_SEL Register (Offset = 140h) [reset = 7h]

Data bus tracing selection

Return to Summary Table

Table 14-32072. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0140h**
MCU_MCRC64_0	**04D0 0140h**

Figure 14-10620. CRC_MBUS_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MEN	DTC_MEN	ITC_MEN
NONE					R/W	R/W	R/W
0h					1h	1h	1h

Table 14-32074. CRC_MBUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MEN	R/W	1h	Enable/disables the tracing of VBUSM 0: Tracing of VBUSM controller bus has been disabled 1: Tracing of VBUSM controller bus has been enabled
1	DTC_MEN	R/W	1h	Enable/disables the tracing of data TCM 0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITC_MEN	R/W	1h	Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled Please refer the description of CPU Data trace at page 1-21 for the priority between different data buses.

14.9.8.4.2.62 CRC_I0_PSA_SIGREG1_CPY_j Register

1 CRC_I0_PSA_SIGREG1_CPY_j Register (Offset = 200h + formula) [reset = 0h]

Region for Channel 1 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = 200h + (j * 4h); where j = 0 to 31d

Table 14-32075. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0200h + formula**
MCU_MCRC64_0	**04D0 0200h + formula**

Figure 14-10621. CRC_I0_PSA_SIGREG1_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG1_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG1_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG1_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG1_CPY0							
W							
0h							

Table 14-32077. CRC_I0_PSA_SIGREG1_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG1_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG1 register for DMA destination, it is write only, the result can be found in the PSASIG1 register.

14.9.8.4.2.63 CRC_I0_PSA_SIGREG2_CPY_j Register

1 CRC_I0_PSA_SIGREG2_CPY_j Register (Offset = 280h + formula) [reset = 0h]

Region for Channel 2 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = 280h + (j * 4h); where j = 0 to 31d

Table 14-32078. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0280h + formula**
MCU_MCRC64_0	**04D0 0280h + formula**

Figure 14-10622. CRC_I0_PSA_SIGREG2_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG2_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG2_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG2_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG2_CPY0							
W							
0h							

Table 14-32080. CRC_I0_PSA_SIGREG2_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG2_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG2 register for DMA destination, it is write only, the result can be found in the PSASIG2 register.

14.9.8.4.2.64 CRC_I0_PSA_SIGREG3_CPY_j Register

1 CRC_I0_PSA_SIGREG3_CPY_j Register (Offset = 300h + formula) [reset = 0h]

Region for Channel 3 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = 300h + (j * 4h); where j = 0 to 31d

Table 14-32081. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0300h + formula**
MCU_MCRC64_0	**04D0 0300h + formula**

Figure 14-10623. CRC_I0_PSA_SIGREG3_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG3_CPY0							
W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
I0_PSASIG3_CPY0							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I0_PSASIG3_CPY0							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I0_PSASIG3_CPY0							
W							
0h							

Table 14-32083. CRC_I0_PSA_SIGREG3_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG3_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG3 register for DMA destination, it is write only, the result can be found in the PSASIG3 register.

14.9.8.4.2.65 CRC_I0_PSA_SIGREG4_CPY_j Register

1 CRC_I0_PSA_SIGREG4_CPY_j Register (Offset = 380h + formula) [reset = 0h]

Region for Channel 4 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = 380h + (j * 4h); where j = 0 to 31d

Table 14-32084. Instance Table

Instance Name	Physical Address
MCRC64_0	**3030 0380h + formula**
MCU_MCRC64_0	**04D0 0380h + formula**

Figure 14-10624. CRC_I0_PSA_SIGREG4_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG4_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG4_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG4_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG4_CPY0							
W							
0h							

Table 14-32086. CRC_I0_PSA_SIGREG4_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG4_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG4 register for DMA destination, it is write only, the result can be found in the PSASIG4 register.

14.9.8.5 ECC Aggregator Registers

14.9.8.5.1 ECC_AGGR

ECC_AGGR

14.9.8.5.1.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32087. ECC_AGGR Registers, Base Address=3F00 F000h, Length=1024

Offset	Length	Register Name	ECC_AGGR0 Physical Address
0h	32	ECC_AGGR_REV	3F00 F000h
8h	32	ECC_AGGR_VECTOR	3F00 F008h
Ch	32	ECC_AGGR_STAT	3F00 F00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 F010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 F03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 F040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 F080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 F0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 F13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 F140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 F180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 F1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 F200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 F204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 F208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 F20Ch

14.9.8.5.1.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.1.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

Return to Summary Table

Table 14-32088. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F000h**

Figure 14-10625. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32090. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.1.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-32091. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F008h**

Figure 14-10626. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32093. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.1.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = Dh]

Misc Status

Return to Summary Table

Table 14-32094. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F00Ch**

Figure 14-10627. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
Dh							

Table 14-32096. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	Dh	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.1.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32097. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F010h + formula**

Figure 14-10628. ECC_AGGR_RESERVED_SVBUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32099. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.1.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32100. Instance Table

Instance Name	Physical Address
ECC_AGGR0	3F00 F03Ch

Figure 14-10629. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32102. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32103. Instance Table

Instance Name	Physical Address
ECC_AGGR0	3F00 F040h

Figure 14-10630. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_PEND	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_PEND	IMAILBOX4_MAIN_0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32105. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend

Table 14-32105. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32106. Instance Table

Instance Name	Physical Address
ECC_AGGR0	3F00 F080h

Figure 14-10631. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_SET	IMAILBOX4_MAIN_0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32108. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved

Table 14-32108. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend

Table 14-32108. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32109. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F0C0h**

Figure 14-10632. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_CLR	IMAILBOX4_MAIN_0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32111. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved

Table 14-32111. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend

Table 14-32111. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32112. Instance Table

Instance Name	**Physical Address**
ECC_AGGR0	**3F00 F13Ch**

Figure 14-10633. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32114. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32115. Instance Table

Instance Name	Physical Address
ECC_AGGR0	3F00 F140h

Figure 14-10634. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_PEND	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_PEND	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_PEND	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_PEND	IMAILBOX4_MAIN_0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32117. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend

Table 14-32117. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32118. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F180h**

Figure 14-10635. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_SET	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_SET	IMAILBOX4_MAIN_0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32120. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved

Table 14-32120. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend

Table 14-32120. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32121. Instance Table

Instance Name	Physical Address
ECC_AGGR0	3F00 F1C0h

Figure 14-10636. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_CLR	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_CLR	IMAILBOX4_MAIN_0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32123. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved

Table 14-32123. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_src_busecc_pend
11	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_PKTDMA_CRED_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_pktdma_cred_dst_busecc_pend
10	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_src_busecc_pend
9	ISAM62A_SEC_BR_MAIN_0_IP2P_SA3_DMSS_CFG_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_sec_br_main_0_Ip2p_sa3_dmss_cfg_dst_busecc_pend
8	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_src_busecc_pend
7	AM62A_MAIN_FW_CBASS_ISMS_MAIN_0_FWMGR_CFG_P2P_BRIDGE_ISMS_MAIN_0_FWMGR_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Isms_main_0_fwmgr_cfg_p2p_bridge_Isms_main_0_fwmgr_cfg_bridge_dst_busecc_pend
6	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
5	AM62A_MAIN_FW_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
4	AM62A_MAIN_IPCSS_CBASS_HSM_CLK_2_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_IPCSS_cbass_HSM_CLK_2_clk_edc_ctrl_cbass_int_HSM_CLK_2_busecc_pend
3	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_TIFS_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_TIFS_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_Isms_main_0_tifs_vbusp_s_p2p_bridge_Isms_main_0_tifs_vbusp_s_bridge_busecc_pend
2	AM62A_MAIN_CENTRAL_CBASS_ISMS_MAIN_0_HSM_VBUSP_S_P2P_BRIDGE_ISMS_MAIN_0_HSM_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_Isms_main_0_hsm_vbusp_s_p2p_bridge_Isms_main_0_hsm_vbusp_s_bridge_busecc_pend

Table 14-32123. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AM62A_MAIN_CENTRAL_CBASS_HSM_CLK_1_CLK_EDC_CTRL_CBASS_INT_HSM_CLK_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_central_cbass_HSM_CLK_1_clk_edc_ctrl_cbass_int_HSM_CLK_1_busecc_pend
0	IMAILBOX4_MAIN_0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Imailbox4_main_0_ramecc_pend

14.9.8.5.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32124. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F200h**

Figure 14-10637. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-32126. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-32127. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F204h**

Figure 14-10638. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32129. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32130. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F208h**

Figure 14-10639. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32132. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32133. Instance Table

Instance Name	Physical Address
ECC_AGGR0	**3F00 F20Ch**

Figure 14-10640. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32135. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.2 ECC_AGGR

ECC_AGGR

14.9.8.5.2.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32136. ECC_AGGR Registers, Base Address=3F00 E000h, Length=1024

Offset	Length	Register Name	ECC_AGGR1 Physical Address
0h	32	ECC_AGGR_REV	3F00 E000h
8h	32	ECC_AGGR_VECTOR	3F00 E008h
Ch	32	ECC_AGGR_STAT	3F00 E00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 E010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 E03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 E040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 E080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 E0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 E13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 E140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 E180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 E1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 E200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 E204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 E208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 E20Ch

14.9.8.5.2.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.2.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32137. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E000h**

Figure 14-10641. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32139. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.2.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32140. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E008h**

Figure 14-10642. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32142. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.2.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-32143. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E00Ch**

Figure 14-10643. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-32145. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.2.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32146. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E010h + formula**

Figure 14-10644. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							

23	22	21	20	19	18	17	16
DATA							
R/W							
0h							

15	14	13	12	11	10	9	8
DATA							
R/W							
0h							

7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32148. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.2.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32149. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E03Ch**

Figure 14-10645. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32151. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.2.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32152. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E040h**

Figure 14-10646. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND
NONE							R/W1TS
0h							0h

Table 14-32154. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32155. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E080h**

Figure 14-10647. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-32157. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32158. Instance Table

Instance Name	Physical Address
ECC_AGGR1	3F00 E0C0h

Figure 14-10648. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-32160. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32161. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E13Ch**

Figure 14-10649. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32163. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.2.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32164. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E140h**

Figure 14-10650. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND
NONE							R/W1TS
0h							0h

Table 14-32166. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32167. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E180h**

Figure 14-10651. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-32169. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32170. Instance Table

Instance Name	Physical Address
ECC_AGGR1	3F00 E1C0h

Figure 14-10652. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-32172. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	AM62A_MAIN_FW_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_main_fw_cbass_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend

14.9.8.5.2.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32173. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E200h**

Figure 14-10653. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32175. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.2.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32176. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E204h**

Figure 14-10654. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32178. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.2.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32179. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E208h**

Figure 14-10655. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32181. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.2.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32182. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**3F00 E20Ch**

Figure 14-10656. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32184. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.3 ECC_AGGR

ECC_AGGR

14.9.8.5.3.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32185. ECC_AGGR Registers, Base Address=0470 3000h, Length=1024

Offset	Length	Register Name	MCU_ECC_AGGR0 Physical Address
0h	32	ECC_AGGR_REV	0470 3000h
8h	32	ECC_AGGR_VECTOR	0470 3008h
Ch	32	ECC_AGGR_STAT	0470 300Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0470 3010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0470 303Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0470 3040h
44h	32	ECC_AGGR_SEC_STATUS_REG1	0470 3044h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0470 3080h
84h	32	ECC_AGGR_SEC_ENABLE_SET_REG1	0470 3084h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0470 30C0h
C4h	32	ECC_AGGR_SEC_ENABLE_CLR_REG1	0470 30C4h
13Ch	32	ECC_AGGR_DED_EOI_REG	0470 313Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0470 3140h
144h	32	ECC_AGGR_DED_STATUS_REG1	0470 3144h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0470 3180h
184h	32	ECC_AGGR_DED_ENABLE_SET_REG1	0470 3184h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0470 31C0h
1C4h	32	ECC_AGGR_DED_ENABLE_CLR_REG1	0470 31C4h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0470 3200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0470 3204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0470 3208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0470 320Ch

14.9.8.5.3.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.3.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32186. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3000h**

Figure 14-10657. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32188. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.3.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32189. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3008h**

Figure 14-10658. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-32191. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.3.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2Bh]

Misc Status

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Table 14-32192. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 300Ch**

Figure 14-10659. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					2Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
2Bh							

Table 14-32194. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.3.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32195. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3010h + formula**

Figure 14-10660. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32197. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.3.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32198. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 303Ch**

Figure 14-10661. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32200. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32201. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3040h**

Figure 14-10662. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_PEND	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_PEND	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0

Figure 14-10662. ECC_AGGR_SEC_STATUS_REG0 Name Register (continued)

ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_PEND	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32203. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend

Table 14-32203. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend

Table 14-32203. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend

Table 14-32203. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.7 ECC_AGGR_SEC_STATUS_REG1 Register

1 ECC_AGGR_SEC_STATUS_REG1 Register (Offset = 44h) [reset = 0h]

Interrupt Status Register 1

Return to Summary Table

Table 14-32204. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3044h**

Figure 14-10663. ECC_AGGR_SEC_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_PEND	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32206. ECC_AGGR_SEC_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32206. ECC_AGGR_SEC_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.8 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-32207. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3080h**

Figure 14-10664. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_SET	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Figure 14-10664. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register (continued)

7	6	5	4	3	2	1	0
ISAM62A_MCU2DM_VBUSMGASKET_MCU_1_EDC_CTRL_ENABLE_SET	ISAM62A_DM2MCU_VBUSMGASKET_MCU_0_EDC_CTRL_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32209. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend

Table 14-32209. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend

Table 14-32209. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend

Table 14-32209. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.9 ECC_AGGR_SEC_ENABLE_SET_REG1 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG1 Register (Offset = 84h) [reset = 0h]

Interrupt Enable Set Register 1

Return to Summary Table

Table 14-32210. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3084h**

Figure 14-10665. ECC_AGGR_SEC_ENABLE_SET_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_SET	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32212. ECC_AGGR_SEC_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32212. ECC_AGGR_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.10 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-32213. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 30C0h**

Figure 14-10666. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_CLR	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Figure 14-10666. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register (continued)

7	6	5	4	3	2	1	0
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_CLR	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32215. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend

Table 14-32215. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend

Table 14-32215. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend

Table 14-32215. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.11 ECC_AGGR_SEC_ENABLE_CLR_REG1 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG1 Register (Offset = C4h) [reset = 0h]

Interrupt Enable Clear Register 1

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Table 14-32216. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 30C4h**

Figure 14-10667. ECC_AGGR_SEC_ENABLE_CLR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_CLR	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32218. ECC_AGGR_SEC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32218. ECC_AGGR_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.12 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-32219. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 313Ch**

Figure 14-10668. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32221. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.3.2.13 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-32222. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3140h**

Figure 14-10669. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_PEND	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_PEND	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_PEND	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0

Figure 14-10669. ECC_AGGR_DED_STATUS_REG0 Name Register (continued)

ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_PEND	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32224. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend

Table 14-32224. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend

Table 14-32224. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend

Table 14-32224. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.14 ECC_AGGR_DED_STATUS_REG1 Register

1 ECC_AGGR_DED_STATUS_REG1 Register (Offset = 144h) [reset = 0h]

Interrupt Status Register 1

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Table 14-32225. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3144h**

Figure 14-10670. ECC_AGGR_DED_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_PEND	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_PEND	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32227. ECC_AGGR_DED_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32227. ECC_AGGR_DED_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.15 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32228. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3180h**

Figure 14-10671. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_SET	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Figure 14-10671. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register (continued)

7	6	5	4	3	2	1	0
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_SET	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32230. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend

Table 14-32230. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend

Table 14-32230. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend

Table 14-32230. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.16 ECC_AGGR_DED_ENABLE_SET_REG1 Register

1 ECC_AGGR_DED_ENABLE_SET_REG1 Register (Offset = 184h) [reset = 0h]

Interrupt Enable Set Register 1

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Table 14-32231. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3184h**

Figure 14-10672. ECC_AGGR_DED_ENABLE_SET_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_SET	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32233. ECC_AGGR_DED_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32233. ECC_AGGR_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.17 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32234. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 31C0h**

Figure 14-10673. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_CLR	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Figure 14-10673. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register (continued)

7	6	5	4	3	2	1	0
ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_CLR	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32236. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_src_busecc_pend
30	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_P2M_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRM_64B_CLK1_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_p2m_bridge_br_SCRP_32b_clk2_to_SCRM_64b_clk1_l0_bridge_dst_busecc_pend
29	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_src_busecc_pend
28	AM62A_MCU_CBASS_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_M2P_BRIDGE_BR_SCRM_64B_CLK1_TO_SCRP_32B_CLK2_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_m2p_bridge_br_SCRM_64b_clk1_to_SCRP_32b_clk2_l0_bridge_dst_busecc_pend
27	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_1_pend
26	AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk4_scr_am62a_mcu_cbass_SCRP_32b_clk4_scr_edc_ctrl_busecc_0_pend

Table 14-32236. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_1_pend
24	AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_AM62A_MCU_CBASS_SCRP_32B_CLK2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRP_32b_clk2_scr_am62a_mcu_cbass_SCRP_32b_clk2_scr_edc_ctrl_busecc_0_pend
23	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_1_pend
22	AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_AM62A_MCU_CBASS_SCRM_64B_CLK1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_SCRM_64b_clk1_scr_am62a_mcu_cbass_SCRM_64b_clk1_scr_edc_ctrl_busecc_0_pend
21	AM62A_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
20	AM62A_MCU_CBASS_MCU_SYSCLK0_2_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_2_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_2_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_2_busecc_pend
19	AM62A_MCU_CBASS_MCU_SYSCLK0_1_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_MCU_SYSCLK0_1_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_1_busecc_pend
18	AM62A_MCU_CBASS_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_PULSAR_UL_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_pulsar_ul_ecc_aggr_mcu_0_cfg_bridge_busecc_pend
17	AM62A_MCU_CBASS_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM62A_MCU_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_p2p_bridge_Isam62a_mcu_mcu_ecc_aggr_mcu_0_cfg_bridge_busecc_pend

Table 14-32236. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_src_busecc_pend
15	AM62A_MCU_CBASS_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_P2P_BRIDGE_ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_p2p_bridge_Isam62a_mcu2dm_vbusm_gasket_mcu_1_cfg_bridge_dst_busecc_pend
14	AM62A_MCU_CBASS_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_P2P_BRIDGE_IPULSAR_ULS_MCU_0_CPU0_CFG_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Ipulsar_uls_mcu_0_cpu0_cfg_slv_p2p_bridge_Ipulsar_uls_mcu_0_cpu0_cfg_slv_bridge_busecc_pend
13	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_1_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_1_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Imsram32kx64e_mcu_1_cfg_p2p_bridge_Imsram32kx64e_mcu_1_cfg_bridge_busecc_pend
12	AM62A_MCU_CBASS_IMSRAM32KX64E_MCU_0_CFG_P2P_BRIDGE_IMSRAM32KX64E_MCU_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Imsram32kx64e_mcu_0_cfg_p2p_bridge_Imsram32kx64e_mcu_0_cfg_bridge_busecc_pend
11	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_src_busecc_pend
10	AM62A_MCU_CBASS_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_p2p_bridge_Iam62a_mcu_cbass_mcu_0_cbass_err_slv_bridge_dst_busecc_pend
9	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_WR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_wr_ramecc_pend
8	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_RD_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_rd_ramecc_pend

Table 14-32236. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ISAM62A_MCU2DM_VBUSM_GASKET_MCU_1_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu2dm_vbusm_gasket_mcu_1_edc_ctrl_pend
6	ISAM62A_DM2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_dm2mcu_vbusm_gasket_mcu_0_edc_ctrl_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_src_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_dst_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_src_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_dst_busecc_pend
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_src_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_dst_busecc_pend

14.9.8.5.3.2.18 ECC_AGGR_DED_ENABLE_CLR_REG1 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG1 Register (Offset = 1C4h) [reset = 0h]

Interrupt Enable Clear Register 1

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Table 14-32237. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	0470 31C4h

Figure 14-10674. ECC_AGGR_DED_ENABLE_CLR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_CLR	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32239. ECC_AGGR_DED_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
9	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_src_busecc_pend
8	AM62A_MCU_CBASS_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_MCU_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_mcu_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_dst_busecc_pend
7	AM62A_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
6	AM62A_MCU_CBASS_ERR_SCR_AM62A_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_err_scr_am62a_mcu_cbass_err_scr_edc_ctrl_busecc_pend
5	AM62A_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_busecc_pend
4	AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_AM62A_MCU_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_int_dmsc_scr_am62a_mcu_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend
3	AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_AM62A_MCU_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_default_mmrs_am62a_mcu_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
2	AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_AM62A_MCU_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_cbass_default_err_am62a_mcu_cbass_cbass_default_err_edc_ctrl_busecc_pend
1	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_src_busecc_pend

Table 14-32239. ECC_AGGR_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AM62A_MCU_CBASS_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_P2P_BRIDGE_BR_SCRP_32B_CLK2_TO_SCRP_32B_CLK4_L0_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_cbass_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_p2p_bridge_br_SCRP_32b_clk2_to_SCRP_32b_clk4_l0_bridge_dst_busecc_pend

14.9.8.5.3.2.19 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32240. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3200h**

Figure 14-10675. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32242. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.3.2.20 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32243. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3204h**

Figure 14-10676. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32245. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.3.2.21 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32246. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 3208h**

Figure 14-10677. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32248. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.3.2.22 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32249. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR0	**0470 320Ch**

Figure 14-10678. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32251. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.4 ECC_AGGR

ECC_AGGR

14.9.8.5.4.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32252. ECC_AGGR Registers, Base Address=0470 4000h, Length=1024

Offset	Length	Register Name	MCU_ECC_AGGR1 Physical Address
0h	32	ECC_AGGR_REV	0470 4000h
8h	32	ECC_AGGR_VECTOR	0470 4008h
Ch	32	ECC_AGGR_STAT	0470 400Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0470 4010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0470 403Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0470 4040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0470 4080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0470 40C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0470 413Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0470 4140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0470 4180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0470 41C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0470 4200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0470 4204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0470 4208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0470 420Ch

14.9.8.5.4.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.4.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32253. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4000h**

Figure 14-10679. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32255. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.4.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32256. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4008h**

Figure 14-10680. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32258. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.4.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 7h]

Misc Status

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Table 14-32259. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 400Ch**

Figure 14-10681. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					7h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
7h							

Table 14-32261. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	7h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.4.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32262. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4010h + formula**

Figure 14-10682. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32264. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.4.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32265. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 403Ch**

Figure 14-10683. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32267. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.4.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32268. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4040h**

Figure 14-10684. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ECCAGG_PEND	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32270. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32270. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32271. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4080h**

Figure 14-10685. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ECCAGG_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32273. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32273. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32274. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 40C0h**

Figure 14-10686. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ECCAGG_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32276. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32276. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32277. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 413Ch**

Figure 14-10687. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32279. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.4.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32280. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4140h**

Figure 14-10688. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	ECCAGG_PEND	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_PEND	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32282. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32282. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32283. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4180h**

Figure 14-10689. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ECCAGG_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_SET	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32285. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32285. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32286. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 41C0h**

Figure 14-10690. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ECCAGG_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_CLR	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32288. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
5	ISAM62A_MCU_PULSAR_UL_BR__IECC_AGGR_CFG_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Iecc_aggr_cfg_dst_busecc_pend
4	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_PMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_pmst_src_busecc_pend
3	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_P2P_CPU0_CFG_SLV_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_p2p_cpu0_cfg_slv_dst_busecc_pend
2	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_WMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_wmst_src_busecc_pend

Table 14-32288. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_SLV_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_slv_dst_busecc_pend
0	ISAM62A_MCU_PULSAR_UL_BR__ICPU0_M2M_CPU0_RMST_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_mcu_pulsar_ul_br__Icpu0_m2m_cpu0_rmst_src_busecc_pend

14.9.8.5.4.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32289. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4200h**

Figure 14-10691. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32291. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.4.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32292. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4204h**

Figure 14-10692. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32294. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.4.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32295. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 4208h**

Figure 14-10693. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-32297. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.4.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32298. Instance Table

Instance Name	Physical Address
MCU_ECC_AGGR1	**0470 420Ch**

Figure 14-10694. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32300. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.5 ECC_AGGR

ECC_AGGR

14.9.8.5.5.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32301. ECC_AGGR Registers, Base Address=2B60 0000h, Length=1024

Offset	Length	Register Name	WKUP_ECC_AGGR0 Physical Address
0h	32	ECC_AGGR_REV	2B60 0000h
8h	32	ECC_AGGR_VECTOR	2B60 0008h
Ch	32	ECC_AGGR_STAT	2B60 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	2B60 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	2B60 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2B60 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2B60 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2B60 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2B60 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2B60 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2B60 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2B60 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2B60 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2B60 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2B60 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2B60 020Ch

14.9.8.5.5.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.5.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32302. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0000h**

Figure 14-10695. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32304. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.5.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32305. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0008h**

Figure 14-10696. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-32307. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.5.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = Bh]

Misc Status

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Table 14-32308. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 000Ch**

Figure 14-10697. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
Bh							

Table 14-32310. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.5.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32311. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0010h + formula**

Figure 14-10698. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32313. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.5.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32314. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 003Ch**

Figure 14-10699. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32316. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.5.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32317. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0040h**

Figure 14-10700. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_PEND	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_PEND	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_PEND

Figure 14-10700. ECC_AGGR_SEC_STATUS_REG0 Name Register (continued)

R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32319. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend

Table 14-32319. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32320. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0080h**

Figure 14-10701. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0

Figure 14-10701. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register (continued)

AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUS_ECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUS_ECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32322. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend

Table 14-32322. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32323. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 00C0h**

Figure 14-10702. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
7	6	5	4	3	2	1	0

Figure 14-10702. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register (continued)

AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32325. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend

Table 14-32325. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32326. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 013Ch**

Figure 14-10703. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32328. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.5.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32329. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0140h**

Figure 14-10704. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED					ECCAGG_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

7	6	5	4	3	2	1	0
AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_PEND	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_PEND	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_PEND

Figure 14-10704. ECC_AGGR_DED_STATUS_REG0 Name Register (continued)

R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32331. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend

Table 14-32331. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32332. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0180h**

Figure 14-10705. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
7	6	5	4	3	2	1	0

Figure 14-10705. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register (continued)

AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32334. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend

Table 14-32334. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32335. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 01C0h**

Figure 14-10706. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					ECCAGG_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
7	6	5	4	3	2	1	0

Figure 14-10706. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register (continued)

AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32337. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
9	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
8	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_src_edc_ctrl_busecc_pend
7	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_src_busecc_pend

Table 14-32337. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_src_busecc_pend
5	AM62A_WKUP_DM_CBASS_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_DM_DM_ECC_AGGR_WKUP_0_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_dm_dm_ecc_aggr_wkup_0_cfg_bridge_dst_busecc_pend
4	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_src_edc_ctrl_busecc_pend
3	AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_ISA3SS_AM62A_MAIN_0_PKTDMA_MEM_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_am62a_wkup_dm_cbass_Isa3ss_am62a_main_0_pktdma_mem_m2m_bridge_dst_edc_ctrl_busecc_pend
2	AM62A_WKUP_DM_CBASS_IK3VTM_N16FFC_WKUP_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_WKUP_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Ik3vtm_n16ffc_wkup_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_wkup_0_vbusp_bridge_busecc_pend
1	AM62A_WKUP_DM_CBASS_DM_CLK_4_CLK_EDC_CTRL_CBASS_INT_DM_CLK_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_DM_CLK_4_clk_edc_ctrl_cbass_int_DM_CLK_4_busecc_pend
0	AM62A_WKUP_DM_CBASS_DM_CLK_1_CLK_EDC_CTRL_CBASS_INT_DM_CLK_1_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_DM_CLK_1_clk_edc_ctrl_cbass_int_DM_CLK_1_busecc_pend

14.9.8.5.5.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32338. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0200h**

Figure 14-10707. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32340. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.5.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-32341. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0204h**

Figure 14-10708. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-32343. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.5.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32344. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 0208h**

Figure 14-10709. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-32346. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.5.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32347. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR0	**2B60 020Ch**

Figure 14-10710. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32349. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.6 ECC_AGGR

ECC_AGGR

14.9.8.5.6.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32350. ECC_AGGR Registers, Base Address=2B60 1000h, Length=1024

Offset	Length	Register Name	WKUP_ECC_AGGR1 Physical Address
0h	32	ECC_AGGR_REV	2B60 1000h
8h	32	ECC_AGGR_VECTOR	2B60 1008h
Ch	32	ECC_AGGR_STAT	2B60 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	2B60 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	2B60 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2B60 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2B60 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2B60 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2B60 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2B60 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2B60 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2B60 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2B60 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2B60 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2B60 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2B60 120Ch

14.9.8.5.6.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.6.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32351. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1000h**

Figure 14-10711. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-32353. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.6.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32354. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1008h**

Figure 14-10712. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-32356. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.6.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-32357. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 100Ch**

Figure 14-10713. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-32359. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.6.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32360. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1010h + formula**

Figure 14-10714. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32362. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.6.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32363. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 103Ch**

Figure 14-10715. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32365. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.6.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32366. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1040h**

Figure 14-10716. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECCAGG_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-32368. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

Table 14-32368. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32369. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1080h**

Figure 14-10717. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				ECCAGG_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-32371. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

Table 14-32371. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32372. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 10C0h**

Figure 14-10718. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECCAGG_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-32374. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

Table 14-32374. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32375. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 113Ch**

Figure 14-10719. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32377. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.6.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32378. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1140h**

Figure 14-10720. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECCAGG_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-32380. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

Table 14-32380. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32381. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1180h**

Figure 14-10721. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECCAGG_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_ECC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_ECC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-32383. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

Table 14-32383. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32384. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 11C0h**

Figure 14-10722. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECCAGG_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-32386. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

Table 14-32386. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
1	AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_AM62A_WKUP_DM_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_MCU_CBASS_DATA_L0_M2M_BRIDGE_DST_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_am62a_wkup_dm_cbass_export_am62a_wkup_dm_cbass_to_am62a_mcu_cbass_data_l0_m2m_bridge_dst_edc_ctrl_busecc_pend
0	AM62A_WKUP_DM_CBASS_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_P2P_BRIDGE_ISAM62A_DM_MCU_ECC_AGGR_WKUP_1_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_dm_cbass_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_p2p_bridge_Isam62a_dm_mcu_ecc_aggr_wkup_1_cfg_bridge_dst_busecc_pend

14.9.8.5.6.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32387. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1200h**

Figure 14-10723. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32389. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.6.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32390. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1204h**

Figure 14-10724. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32392. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.6.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32393. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 1208h**

Figure 14-10725. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32395. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.6.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32396. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR1	**2B60 120Ch**

Figure 14-10726. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32398. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.7 ECC_AGGR

ECC_AGGR

14.9.8.5.7.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-32399. ECC_AGGR Registers, Base Address=0403 0000h, Length=1024

Offset	Length	Register Name	WKUP_ECC_AGGR2 Physical Address
0h	32	ECC_AGGR_REV	0403 0000h
8h	32	ECC_AGGR_VECTOR	0403 0008h
Ch	32	ECC_AGGR_STAT	0403 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0403 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0403 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0403 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0403 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0403 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0403 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0403 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0403 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0403 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0403 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0403 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0403 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0403 020Ch

14.9.8.5.7.2 ECC_AGGR Registers

ECC_AGGR Registers

14.9.8.5.7.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32400. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0000h**

Figure 14-10727. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-32402. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.7.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32403. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0008h**

Figure 14-10728. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32405. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.7.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 11h]

Misc Status

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Table 14-32406. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 000Ch**

Figure 14-10729. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">11h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">11h</td></tr>
</table>

Table 14-32408. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	11h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.7.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32409. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0010h + formula**

Figure 14-10730. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32411. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.7.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32412. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 003Ch**

Figure 14-10731. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32414. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.7.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32415. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0040h**

Figure 14-10732. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECCAGG_PEND
NONE							R/W1TS
0h							0h
15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_PEND	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS

Figure 14-10732. ECC_AGGR_SEC_STATUS_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32417. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32417. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32418. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0080h**

Figure 14-10733. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECCAGG_ENABLE_SET
NONE							R/W1TS
0h							0h
15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS

Figure 14-10733. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32420. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32420. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32421. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 00C0h**

Figure 14-10734. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							ECCAGG_ENABLE_CLR
NONE							R/W1TC
0h							0h

15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC

Figure 14-10734. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32423. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32423. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32424. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 013Ch**

Figure 14-10735. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32426. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.7.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32427. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0140h**

Figure 14-10736. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECCAGG_PEND
NONE							R/W1TS
0h							0h
15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_PEND	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS

Figure 14-10736. ECC_AGGR_DED_STATUS_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32429. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32429. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_PEND	R/W1TS	0h	Interrupt Pending Status for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32430. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0180h**

Figure 14-10737. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECCAGG_ENABLE_SET
NONE							R/W1TS
0h							0h
15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS

Figure 14-10737. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32432. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32432. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32433. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 01C0h**

Figure 14-10738. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECCAGG_ENABLE_CLR
NONE							R/W1TC
0h							0h
15	14	13	12	11	10	9	8
AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC

Figure 14-10738. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register (continued)

0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32435. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
15	AM62A_WKUP_SAFE_CBASS_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM62A_WKUP_DM_CBASS_TO_AM62A_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_m2p_bridge_export_am62a_wkup_dm_cbass_to_am62a_wkup_safe_cbass_data_l0_bridge_busecc_pend
14	AM62A_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
13	AM62A_WKUP_SAFE_CBASS_ERR_SCR_AM62A_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_err_scr_am62a_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
12	AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM62A_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_cbass_default_err_am62a_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
11	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_1_pend
10	AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_AM62A_WKUP_SAFE_CBASS_SCRP_SAFE_CLK4_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_am62a_wkup_safe_cbass_SCRP_safe_clk4_scr_edc_ctrl_busecc_0_pend
9	AM62A_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
8	AM62A_WKUP_SAFE_CBASS_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_BRIDGE_ISAM62A_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_bridge_Isam62a_wkup_safe_ecc_aggr_wkup_0_cfg_bridge_busecc_pend

Table 14-32435. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AM62A_WKUP_SAFE_CBASS_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM62A_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_wkup_safe_cbass_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_bridge_Iam62a_wkup_safe_cbass_wkup_0_cbass_err_slv_bridge_busecc_pend
6	ISAM62A_DM2WS_VBUSM_GASKET_MCU_0_EDC_CTRL_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Isam62a_dm2ws_vbusm_gasket_mcu_0_edc_ctrl_pend
5	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM62AXX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62axx_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM62A_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM62A_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am62a_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.9.8.5.7.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32436. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0200h**

Figure 14-10739. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32438. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.7.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32439. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0204h**

Figure 14-10740. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32441. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.7.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32442. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 0208h**

Figure 14-10741. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32444. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.7.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32445. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	**0403 020Ch**

Figure 14-10742. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32447. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.5.8 DMASS_ECC_AGGR_0

DMASS_ECC_AGGR_0

14.9.8.5.8.1 DMASS_ECC_AGGR_0 Summaries

DMASS_ECC_AGGR_0 Summaries

Table 14-32448. ECC_AGGR Registers, Base Address=3F00 5000h, Length=1024

Offset	Length	Register Name	DMASS0_ECC_AGGR_0 Physical Address
0h	32	ECC_AGGR_REV	3F00 5000h
8h	32	ECC_AGGR_VECTOR	3F00 5008h
Ch	32	ECC_AGGR_STAT	3F00 500Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 5010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 503Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 5040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 5080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 50C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 513Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 5140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 5180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 51C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 5200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 5204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 5208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 520Ch

14.9.8.5.8.2 DMASS_ECC_AGGR_0 Registers

DMASS_ECC_AGGR_0 Registers

14.9.8.5.8.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-32449. Instance Table

Instance Name	**Physical Address**
DMASS0_ECC_AGGR_0	**3F00 5000h**

Figure 14-10743. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-32451. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.8.5.8.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-32452. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5008h**

Figure 14-10744. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32454. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.8.5.8.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Ch]

Misc Status

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Table 14-32455. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 500Ch**

Figure 14-10745. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Ch		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Ch							

Table 14-32457. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Ch	Indicates the number of RAMS serviced by the ECC aggregator

14.9.8.5.8.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 10h + (j * 4h); where j = 0 to 7d

Table 14-32458. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5010h + formula**

Figure 14-10746. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-32460. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.8.5.8.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-32461. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 503Ch**

Figure 14-10747. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32463. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.8.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32464. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5040h**

Figure 14-10748. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32466. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend

Table 14-32466. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32467. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5080h**

Figure 14-10749. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32469. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-32469. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32470. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 50C0h**

Figure 14-10750. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32472. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-32472. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-32473. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 513Ch**

Figure 14-10751. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-32475. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.8.5.8.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-32476. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5140h**

Figure 14-10752. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32478. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend

Table 14-32478. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-32479. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5180h**

Figure 14-10753. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32481. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-32481. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-32482. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 51C0h**

Figure 14-10754. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32484. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-32484. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.9.8.5.8.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-32485. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5200h**

Figure 14-10755. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-32487. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.8.5.8.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-32488. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5204h**

Figure 14-10756. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-32490. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.8.5.8.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-32491. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 5208h**

Figure 14-10757. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-32493. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.8.5.8.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-32494. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	**3F00 520Ch**

Figure 14-10758. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-32496. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.8.6 PBIST

PBIST

14.9.8.6.1 PBIST Summaries

PBIST Summaries

Table 14-32497. PBIST Registers, Base Address=3F11 0000h, Length=1024

Offset	Length	Register Name	PBIST0 Physical Address	WKUP_PBIST0 Physical Address	WKUP_PBIST1 Physical Address
0h	32	PBIST_RF0L	04F0 0000h	3F11 0000h	2B50 0000h
4h	32	PBIST_RF1L	04F0 0004h	3F11 0004h	2B50 0004h
8h	32	PBIST_RF2L	04F0 0008h	3F11 0008h	2B50 0008h
Ch	32	PBIST_RF3L	04F0 000Ch	3F11 000Ch	2B50 000Ch
10h	32	PBIST_RF4L	04F0 0010h	3F11 0010h	2B50 0010h
14h	32	PBIST_RF5L	04F0 0014h	3F11 0014h	2B50 0014h
18h	32	PBIST_RF6L	04F0 0018h	3F11 0018h	2B50 0018h
1Ch	32	PBIST_RF7L	04F0 001Ch	3F11 001Ch	2B50 001Ch
20h	32	PBIST_RF8L	04F0 0020h	3F11 0020h	2B50 0020h
24h	32	PBIST_RF9L	04F0 0024h	3F11 0024h	2B50 0024h
28h	32	PBIST_RF10L	04F0 0028h	3F11 0028h	2B50 0028h
2Ch	32	PBIST_RF11L	04F0 002Ch	3F11 002Ch	2B50 002Ch
30h	32	PBIST_RF12L	04F0 0030h	3F11 0030h	2B50 0030h
34h	32	PBIST_RF13L	04F0 0034h	3F11 0034h	2B50 0034h
38h	32	PBIST_RF14L	04F0 0038h	3F11 0038h	2B50 0038h
3Ch	32	PBIST_RF15L	04F0 003Ch	3F11 003Ch	2B50 003Ch
40h	32	PBIST_RF0U	04F0 0040h	3F11 0040h	2B50 0040h
44h	32	PBIST_RF1U	04F0 0044h	3F11 0044h	2B50 0044h
48h	32	PBIST_RF2U	04F0 0048h	3F11 0048h	2B50 0048h
4Ch	32	PBIST_RF3U	04F0 004Ch	3F11 004Ch	2B50 004Ch
50h	32	PBIST_RF4U	04F0 0050h	3F11 0050h	2B50 0050h
54h	32	PBIST_RF5U	04F0 0054h	3F11 0054h	2B50 0054h
58h	32	PBIST_RF6U	04F0 0058h	3F11 0058h	2B50 0058h
5Ch	32	PBIST_RF7U	04F0 005Ch	3F11 005Ch	2B50 005Ch
60h	32	PBIST_RF8U	04F0 0060h	3F11 0060h	2B50 0060h
64h	32	PBIST_RF9U	04F0 0064h	3F11 0064h	2B50 0064h
68h	32	PBIST_RF10U	04F0 0068h	3F11 0068h	2B50 0068h
6Ch	32	PBIST_RF11U	04F0 006Ch	3F11 006Ch	2B50 006Ch
70h	32	PBIST_RF12U	04F0 0070h	3F11 0070h	2B50 0070h
74h	32	PBIST_RF13U	04F0 0074h	3F11 0074h	2B50 0074h
78h	32	PBIST_RF14U	04F0 0078h	3F11 0078h	2B50 0078h
7Ch	32	PBIST_RF15U	04F0 007Ch	3F11 007Ch	2B50 007Ch
100h	32	PBIST_A0	04F0 0100h	3F11 0100h	2B50 0100h
104h	32	PBIST_A1	04F0 0104h	3F11 0104h	2B50 0104h
108h	32	PBIST_A2	04F0 0108h	3F11 0108h	2B50 0108h
10Ch	32	PBIST_A3	04F0 010Ch	3F11 010Ch	2B50 010Ch
110h	32	PBIST_L0	04F0 0110h	3F11 0110h	2B50 0110h

Table 14-32497. PBIST Registers, Base Address=3F11 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST0 Physical Address	WKUP_PBIST0 Physical Address	WKUP_PBIST1 Physical Address
114h	32	PBIST_L1	04F0 0114h	3F11 0114h	2B50 0114h
118h	32	PBIST_L2	04F0 0118h	3F11 0118h	2B50 0118h
11Ch	32	PBIST_L3	04F0 011Ch	3F11 011Ch	2B50 011Ch
120h	32	PBIST_D	04F0 0120h	3F11 0120h	2B50 0120h
124h	32	PBIST_E	04F0 0124h	3F11 0124h	2B50 0124h
130h	32	PBIST_CA0	04F0 0130h	3F11 0130h	2B50 0130h
134h	32	PBIST_CA1	04F0 0134h	3F11 0134h	2B50 0134h
138h	32	PBIST_CA2	04F0 0138h	3F11 0138h	2B50 0138h
13Ch	32	PBIST_CA3	04F0 013Ch	3F11 013Ch	2B50 013Ch
140h	32	PBIST_CL0	04F0 0140h	3F11 0140h	2B50 0140h
144h	32	PBIST_CL1	04F0 0144h	3F11 0144h	2B50 0144h
148h	32	PBIST_CL2	04F0 0148h	3F11 0148h	2B50 0148h
14Ch	32	PBIST_CL3	04F0 014Ch	3F11 014Ch	2B50 014Ch
150h	32	PBIST_I0	04F0 0150h	3F11 0150h	2B50 0150h
154h	32	PBIST_I1	04F0 0154h	3F11 0154h	2B50 0154h
158h	32	PBIST_I2	04F0 0158h	3F11 0158h	2B50 0158h
15Ch	32	PBIST_I3	04F0 015Ch	3F11 015Ch	2B50 015Ch
160h	32	PBIST_RAMT	04F0 0160h	3F11 0160h	2B50 0160h
164h	32	PBIST_DLR	04F0 0164h	3F11 0164h	2B50 0164h
168h	32	PBIST_CMS	04F0 0168h	3F11 0168h	2B50 0168h
16Ch	32	PBIST_STR	04F0 016Ch	3F11 016Ch	2B50 016Ch
170h	64	PBIST_SCR	04F0 0170h	3F11 0170h	2B50 0170h
178h	32	PBIST_CSR	04F0 0178h	3F11 0178h	2B50 0178h
17Ch	32	PBIST_FDLY	04F0 017Ch	3F11 017Ch	2B50 017Ch
180h	32	PBIST_PACT	04F0 0180h	3F11 0180h	2B50 0180h
184h	32	PBIST_PID	04F0 0184h	3F11 0184h	2B50 0184h
188h	32	PBIST_OVER	04F0 0188h	3F11 0188h	2B50 0188h
190h	64	PBIST_FSRF	04F0 0190h	3F11 0190h	2B50 0190h
198h	64	PBIST_FSRC	04F0 0198h	3F11 0198h	2B50 0198h
1A0h	64	PBIST_FSRA	04F0 01A0h	3F11 01A0h	2B50 01A0h
1A8h	32	PBIST_FSRDL0	04F0 01A8h	3F11 01A8h	2B50 01A8h
1B0h	32	PBIST_FSRDL1	04F0 01B0h	3F11 01B0h	2B50 01B0h
1B4h	32	PBIST_MARGIN_MODE	04F0 01B4h	3F11 01B4h	2B50 01B4h
1B8h	32	PBIST_WRENZ	04F0 01B8h	3F11 01B8h	2B50 01B8h
1BCh	32	PBIST_PAGE_PGS	04F0 01BCh	3F11 01BCh	2B50 01BCh
1C0h	32	PBIST_ROM	04F0 01C0h	3F11 01C0h	2B50 01C0h
1C4h	32	PBIST_ALGO	04F0 01C4h	3F11 01C4h	2B50 01C4h
1C8h	64	PBIST_RINFO	04F0 01C8h	3F11 01C8h	2B50 01C8h

Table 14-32498. PBIST Registers, Base Address=3F11 0000h, Length=1024

Offset	Length	Register Name	MCU_PBIST0 Physical Address
0h	32	PBIST_RF0L	2B51 0000h
4h	32	PBIST_RF1L	2B51 0004h
8h	32	PBIST_RF2L	2B51 0008h

Table 14-32498. PBIST Registers, Base Address=3F11 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_PBIST0 Physical Address
Ch	32	PBIST_RF3L	2B51 000Ch
10h	32	PBIST_RF4L	2B51 0010h
14h	32	PBIST_RF5L	2B51 0014h
18h	32	PBIST_RF6L	2B51 0018h
1Ch	32	PBIST_RF7L	2B51 001Ch
20h	32	PBIST_RF8L	2B51 0020h
24h	32	PBIST_RF9L	2B51 0024h
28h	32	PBIST_RF10L	2B51 0028h
2Ch	32	PBIST_RF11L	2B51 002Ch
30h	32	PBIST_RF12L	2B51 0030h
34h	32	PBIST_RF13L	2B51 0034h
38h	32	PBIST_RF14L	2B51 0038h
3Ch	32	PBIST_RF15L	2B51 003Ch
40h	32	PBIST_RF0U	2B51 0040h
44h	32	PBIST_RF1U	2B51 0044h
48h	32	PBIST_RF2U	2B51 0048h
4Ch	32	PBIST_RF3U	2B51 004Ch
50h	32	PBIST_RF4U	2B51 0050h
54h	32	PBIST_RF5U	2B51 0054h
58h	32	PBIST_RF6U	2B51 0058h
5Ch	32	PBIST_RF7U	2B51 005Ch
60h	32	PBIST_RF8U	2B51 0060h
64h	32	PBIST_RF9U	2B51 0064h
68h	32	PBIST_RF10U	2B51 0068h
6Ch	32	PBIST_RF11U	2B51 006Ch
70h	32	PBIST_RF12U	2B51 0070h
74h	32	PBIST_RF13U	2B51 0074h
78h	32	PBIST_RF14U	2B51 0078h
7Ch	32	PBIST_RF15U	2B51 007Ch
100h	32	PBIST_A0	2B51 0100h
104h	32	PBIST_A1	2B51 0104h
108h	32	PBIST_A2	2B51 0108h
10Ch	32	PBIST_A3	2B51 010Ch
110h	32	PBIST_L0	2B51 0110h
114h	32	PBIST_L1	2B51 0114h
118h	32	PBIST_L2	2B51 0118h
11Ch	32	PBIST_L3	2B51 011Ch
120h	32	PBIST_D	2B51 0120h
124h	32	PBIST_E	2B51 0124h
130h	32	PBIST_CA0	2B51 0130h
134h	32	PBIST_CA1	2B51 0134h
138h	32	PBIST_CA2	2B51 0138h
13Ch	32	PBIST_CA3	2B51 013Ch
140h	32	PBIST_CL0	2B51 0140h
144h	32	PBIST_CL1	2B51 0144h

Table 14-32498. PBIST Registers, Base Address=3F11 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_PBIST0 Physical Address
148h	32	PBIST_CL2	2B51 0148h
14Ch	32	PBIST_CL3	2B51 014Ch
150h	32	PBIST_I0	2B51 0150h
154h	32	PBIST_I1	2B51 0154h
158h	32	PBIST_I2	2B51 0158h
15Ch	32	PBIST_I3	2B51 015Ch
160h	32	PBIST_RAMT	2B51 0160h
164h	32	PBIST_DLR	2B51 0164h
168h	32	PBIST_CMS	2B51 0168h
16Ch	32	PBIST_STR	2B51 016Ch
170h	64	PBIST_SCR	2B51 0170h
178h	32	PBIST_CSR	2B51 0178h
17Ch	32	PBIST_FDLY	2B51 017Ch
180h	32	PBIST_PACT	2B51 0180h
184h	32	PBIST_PID	2B51 0184h
188h	32	PBIST_OVER	2B51 0188h
190h	64	PBIST_FSRF	2B51 0190h
198h	64	PBIST_FSRC	2B51 0198h
1A0h	64	PBIST_FSRA	2B51 01A0h
1A8h	32	PBIST_FSRDL0	2B51 01A8h
1B0h	32	PBIST_FSRDL1	2B51 01B0h
1B4h	32	PBIST_MARGIN_MODE	2B51 01B4h
1B8h	32	PBIST_WRENZ	2B51 01B8h
1BCh	32	PBIST_PAGE_PGS	2B51 01BCh
1C0h	32	PBIST_ROM	2B51 01C0h
1C4h	32	PBIST_ALGO	2B51 01C4h
1C8h	64	PBIST_RINFO	2B51 01C8h

14.9.8.6.2 PBIST Registers

PBIST Registers

14.9.8.6.2.1 PBIST_RF0L Register

1 PBIST_RF0L Register (Offset = 0h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32499. Instance Table

Instance Name	Physical Address
MCU_PBIST0	04F0 0000h
PBIST0	3F11 0000h
WKUP_PBIST0	2B50 0000h
WKUP_PBIST1	2B51 0000h

Figure 14-10759. PBIST_RF0L Name Register

31	30	29	28	27	26	25	24
RF0L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF0L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF0L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF0L							
R/W							
0h							

Table 14-32501. PBIST_RF0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0L	R/W	0h	Register Files / Instruction Registers RF0 lower (RF0L) Reset Source: mod_g_rst_n

14.9.8.6.2.2 PBIST_RF1L Register

1 PBIST_RF1L Register (Offset = 4h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32502. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0004h**
PBIST0	**3F11 0004h**
WKUP_PBIST0	**2B50 0004h**
WKUP_PBIST1	**2B51 0004h**

Figure 14-10760. PBIST_RF1L Name Register

31	30	29	28	27	26	25	24
RF1L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF1L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF1L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF1L							
R/W							
0h							

Table 14-32504. PBIST_RF1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF1L	R/W	0h	Register Files / Instruction Registers RF1 lower (RF1L) Reset Source: mod_g_rst_n

14.9.8.6.2.3 PBIST_RF2L Register

1 PBIST_RF2L Register (Offset = 8h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32505. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0008h**
PBIST0	**3F11 0008h**
WKUP_PBIST0	**2B50 0008h**
WKUP_PBIST1	**2B51 0008h**

Figure 14-10761. PBIST_RF2L Name Register

31	30	29	28	27	26	25	24
RF2L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF2L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF2L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF2L							
R/W							
0h							

Table 14-32507. PBIST_RF2L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2L	R/W	0h	Register Files / Instruction Registers RF2 lower (RF2L) Reset Source: mod_g_rst_n

14.9.8.6.2.4 PBIST_RF3L Register

1 PBIST_RF3L Register (Offset = Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32508. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 000Ch**
PBIST0	**3F11 000Ch**
WKUP_PBIST0	**2B50 000Ch**
WKUP_PBIST1	**2B51 000Ch**

Figure 14-10762. PBIST_RF3L Name Register

31	30	29	28	27	26	25	24
RF3L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF3L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF3L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF3L							
R/W							
0h							

Table 14-32510. PBIST_RF3L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3L	R/W	0h	Register Files / Instruction Registers RF3 lower (RF3L) Reset Source: mod_g_rst_n

14.9.8.6.2.5 PBIST_RF4L Register

1 PBIST_RF4L Register (Offset = 10h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32511. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0010h**
PBIST0	**3F11 0010h**
WKUP_PBIST0	**2B50 0010h**
WKUP_PBIST1	**2B51 0010h**

Figure 14-10763. PBIST_RF4L Name Register

31	30	29	28	27	26	25	24
RF4L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4L							
R/W							
0h							

Table 14-32513. PBIST_RF4L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4L	R/W	0h	Register Files / Instruction Registers RF4 lower (RF4L) Reset Source: mod_g_rst_n

14.9.8.6.2.6 PBIST_RF5L Register

1 PBIST_RF5L Register (Offset = 14h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32514. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0014h**
PBIST0	**3F11 0014h**
WKUP_PBIST0	**2B50 0014h**
WKUP_PBIST1	**2B51 0014h**

Figure 14-10764. PBIST_RF5L Name Register

31	30	29	28	27	26	25	24
RF5L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF5L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF5L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF5L							
R/W							
0h							

Table 14-32516. PBIST_RF5L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5L	R/W	0h	Register Files / Instruction Registers RF5 lower (RF5L) Reset Source: mod_g_rst_n

14.9.8.6.2.7 PBIST_RF6L Register

1 PBIST_RF6L Register (Offset = 18h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32517. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0018h**
PBIST0	**3F11 0018h**
WKUP_PBIST0	**2B50 0018h**
WKUP_PBIST1	**2B51 0018h**

Figure 14-10765. PBIST_RF6L Name Register

31	30	29	28	27	26	25	24
RF6L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF6L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF6L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF6L							
R/W							
0h							

Table 14-32519. PBIST_RF6L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6L	R/W	0h	Register Files / Instruction Registers RF6 lower (RF6L) Reset Source: mod_g_rst_n

14.9.8.6.2.8 PBIST_RF7L Register

1 PBIST_RF7L Register (Offset = 1Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32520. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 001Ch**
PBIST0	**3F11 001Ch**
WKUP_PBIST0	**2B50 001Ch**
WKUP_PBIST1	**2B51 001Ch**

Figure 14-10766. PBIST_RF7L Name Register

31	30	29	28	27	26	25	24
RF7L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7L							
R/W							
0h							

Table 14-32522. PBIST_RF7L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7L	R/W	0h	Register Files / Instruction Registers RF7 lower (RF7L) Reset Source: mod_g_rst_n

14.9.8.6.2.9 PBIST_RF8L Register

1 PBIST_RF8L Register (Offset = 20h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32523. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0020h**
PBIST0	**3F11 0020h**
WKUP_PBIST0	**2B50 0020h**
WKUP_PBIST1	**2B51 0020h**

Figure 14-10767. PBIST_RF8L Name Register

31	30	29	28	27	26	25	24
RF8L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF8L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF8L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF8L							
R/W							
0h							

Table 14-32525. PBIST_RF8L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8L	R/W	0h	Register Files / Instruction Registers RF8 lower (RF8L) Reset Source: mod_g_rst_n

14.9.8.6.2.10 PBIST_RF9L Register

1 PBIST_RF9L Register (Offset = 24h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32526. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0024h**
PBIST0	**3F11 0024h**
WKUP_PBIST0	**2B50 0024h**
WKUP_PBIST1	**2B51 0024h**

Figure 14-10768. PBIST_RF9L Name Register

31	30	29	28	27	26	25	24
RF9L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF9L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF9L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF9L							
R/W							
0h							

Table 14-32528. PBIST_RF9L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9L	R/W	0h	Register Files / Instruction Registers RF9 lower (RF9L) Reset Source: mod_g_rst_n

14.9.8.6.2.11 PBIST_RF10L Register

1 PBIST_RF10L Register (Offset = 28h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32529. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0028h**
PBIST0	**3F11 0028h**
WKUP_PBIST0	**2B50 0028h**
WKUP_PBIST1	**2B51 0028h**

Figure 14-10769. PBIST_RF10L Name Register

31	30	29	28	27	26	25	24
RF10L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF10L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF10L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF10L							
R/W							
0h							

Table 14-32531. PBIST_RF10L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10L	R/W	0h	Register Files / Instruction Registers RF10 lower (RF10L) Reset Source: mod_g_rst_n

14.9.8.6.2.12 PBIST_RF11L Register

1 PBIST_RF11L Register (Offset = 2Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32532. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 002Ch**
PBIST0	**3F11 002Ch**
WKUP_PBIST0	**2B50 002Ch**
WKUP_PBIST1	**2B51 002Ch**

Figure 14-10770. PBIST_RF11L Name Register

31	30	29	28	27	26	25	24
RF11L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF11L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF11L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF11L							
R/W							
0h							

Table 14-32534. PBIST_RF11L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11L	R/W	0h	Register Files / Instruction Registers RF11 lower (RF11L) Reset Source: mod_g_rst_n

14.9.8.6.2.13 PBIST_RF12L Register

1 PBIST_RF12L Register (Offset = 30h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32535. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0030h**
PBIST0	**3F11 0030h**
WKUP_PBIST0	**2B50 0030h**
WKUP_PBIST1	**2B51 0030h**

Figure 14-10771. PBIST_RF12L Name Register

31	30	29	28	27	26	25	24
RF12L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12L							
R/W							
0h							

Table 14-32537. PBIST_RF12L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12L	R/W	0h	Register Files / Instruction Registers RF12 lower (RF12L) Reset Source: mod_g_rst_n

14.9.8.6.2.14 PBIST_RF13L Register

1 PBIST_RF13L Register (Offset = 34h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32538. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0034h**
PBIST0	**3F11 0034h**
WKUP_PBIST0	**2B50 0034h**
WKUP_PBIST1	**2B51 0034h**

Figure 14-10772. PBIST_RF13L Name Register

31	30	29	28	27	26	25	24
RF13L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF13L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF13L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF13L							
R/W							
0h							

Table 14-32540. PBIST_RF13L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13L	R/W	0h	Register Files / Instruction Registers RF13 lower (RF13L) Reset Source: mod_g_rst_n

14.9.8.6.2.15 PBIST_RF14L Register

1 PBIST_RF14L Register (Offset = 38h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32541. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0038h**
PBIST0	**3F11 0038h**
WKUP_PBIST0	**2B50 0038h**
WKUP_PBIST1	**2B51 0038h**

Figure 14-10773. PBIST_RF14L Name Register

31	30	29	28	27	26	25	24
RF14L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF14L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF14L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF14L							
R/W							
0h							

Table 14-32543. PBIST_RF14L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14L	R/W	0h	Register Files / Instruction Registers RF14 lower (RF14L) Reset Source: mod_g_rst_n

14.9.8.6.2.16 PBIST_RF15L Register

1 PBIST_RF15L Register (Offset = 3Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32544. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 003Ch**
PBIST0	**3F11 003Ch**
WKUP_PBIST0	**2B50 003Ch**
WKUP_PBIST1	**2B51 003Ch**

Figure 14-10774. PBIST_RF15L Name Register

31	30	29	28	27	26	25	24
RF15L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF15L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF15L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF15L							
R/W							
0h							

Table 14-32546. PBIST_RF15L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15L	R/W	0h	Register Files / Instruction Registers RF15 lower (RF15L) Reset Source: mod_g_rst_n

14.9.8.6.2.17 PBIST_RF0U Register

1 PBIST_RF0U Register (Offset = 40h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32547. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0040h**
PBIST0	**3F11 0040h**
WKUP_PBIST0	**2B50 0040h**
WKUP_PBIST1	**2B51 0040h**

Figure 14-10775. PBIST_RF0U Name Register

31	30	29	28	27	26	25	24
RF0U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF0U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF0U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF0U							
R/W							
0h							

Table 14-32549. PBIST_RF0U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0U	R/W	0h	Register Files / Instruction Registers RF0 upper (RF0U) Reset Source: mod_g_rst_n

14.9.8.6.2.18 PBIST_RF1U Register

1 PBIST_RF1U Register (Offset = 44h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32550. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0044h**
PBIST0	**3F11 0044h**
WKUP_PBIST0	**2B50 0044h**
WKUP_PBIST1	**2B51 0044h**

Figure 14-10776. PBIST_RF1U Name Register

31	30	29	28	27	26	25	24
RF1U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF1U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF1U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF1U							
R/W							
0h							

Table 14-32552. PBIST_RF1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF1U	R/W	0h	Register Files / Instruction Registers RF1 upper (RF1U) Reset Source: mod_g_rst_n

14.9.8.6.2.19 PBIST_RF2U Register

1 PBIST_RF2U Register (Offset = 48h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32553. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0048h**
PBIST0	**3F11 0048h**
WKUP_PBIST0	**2B50 0048h**
WKUP_PBIST1	**2B51 0048h**

Figure 14-10777. PBIST_RF2U Name Register

31	30	29	28	27	26	25	24
RF2U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF2U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF2U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF2U							
R/W							
0h							

Table 14-32555. PBIST_RF2U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2U	R/W	0h	Register Files / Instruction Registers RF2 upper (RF2U) Reset Source: mod_g_rst_n

14.9.8.6.2.20 PBIST_RF3U Register

1 PBIST_RF3U Register (Offset = 4Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32556. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 004Ch**
PBIST0	**3F11 004Ch**
WKUP_PBIST0	**2B50 004Ch**
WKUP_PBIST1	**2B51 004Ch**

Figure 14-10778. PBIST_RF3U Name Register

31	30	29	28	27	26	25	24
RF3U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF3U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF3U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF3U							
R/W							
0h							

Table 14-32558. PBIST_RF3U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3U	R/W	0h	Register Files / Instruction Registers RF3 upper (RF3U) Reset Source: mod_g_rst_n

14.9.8.6.2.21 PBIST_RF4U Register

1 PBIST_RF4U Register (Offset = 50h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32559. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0050h**
PBIST0	**3F11 0050h**
WKUP_PBIST0	**2B50 0050h**
WKUP_PBIST1	**2B51 0050h**

Figure 14-10779. PBIST_RF4U Name Register

31	30	29	28	27	26	25	24
RF4U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4U							
R/W							
0h							

Table 14-32561. PBIST_RF4U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4U	R/W	0h	Register Files / Instruction Registers RF4 upper (RF4U) Reset Source: mod_g_rst_n

14.9.8.6.2.22 PBIST_RF5U Register

1 PBIST_RF5U Register (Offset = 54h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32562. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0054h**
PBIST0	**3F11 0054h**
WKUP_PBIST0	**2B50 0054h**
WKUP_PBIST1	**2B51 0054h**

Figure 14-10780. PBIST_RF5U Name Register

31	30	29	28	27	26	25	24
RF5U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF5U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF5U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF5U							
R/W							
0h							

Table 14-32564. PBIST_RF5U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5U	R/W	0h	Register Files / Instruction Registers RF5 upper (RF5U) Reset Source: mod_g_rst_n

14.9.8.6.2.23 PBIST_RF6U Register

1 PBIST_RF6U Register (Offset = 58h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32565. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0058h**
PBIST0	**3F11 0058h**
WKUP_PBIST0	**2B50 0058h**
WKUP_PBIST1	**2B51 0058h**

Figure 14-10781. PBIST_RF6U Name Register

31	30	29	28	27	26	25	24
RF6U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF6U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF6U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF6U							
R/W							
0h							

Table 14-32567. PBIST_RF6U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6U	R/W	0h	Register Files / Instruction Registers RF6 upper (RF6U) Reset Source: mod_g_rst_n

14.9.8.6.2.24 PBIST_RF7U Register

1 PBIST_RF7U Register (Offset = 5Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32568. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 005Ch**
PBIST0	**3F11 005Ch**
WKUP_PBIST0	**2B50 005Ch**
WKUP_PBIST1	**2B51 005Ch**

Figure 14-10782. PBIST_RF7U Name Register

31	30	29	28	27	26	25	24
RF7U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7U							
R/W							
0h							

Table 14-32570. PBIST_RF7U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7U	R/W	0h	Register Files / Instruction Registers RF7 upper (RF7U) Reset Source: mod_g_rst_n

14.9.8.6.2.25 PBIST_RF8U Register

1 PBIST_RF8U Register (Offset = 60h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32571. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0060h**
PBIST0	**3F11 0060h**
WKUP_PBIST0	**2B50 0060h**
WKUP_PBIST1	**2B51 0060h**

Figure 14-10783. PBIST_RF8U Name Register

31	30	29	28	27	26	25	24
RF8U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF8U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF8U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF8U							
R/W							
0h							

Table 14-32573. PBIST_RF8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8U	R/W	0h	Register Files / Instruction Registers RF8 upper (RF8U) Reset Source: mod_g_rst_n

14.9.8.6.2.26 PBIST_RF9U Register

1 PBIST_RF9U Register (Offset = 64h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32574. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0064h**
PBIST0	**3F11 0064h**
WKUP_PBIST0	**2B50 0064h**
WKUP_PBIST1	**2B51 0064h**

Figure 14-10784. PBIST_RF9U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32576. PBIST_RF9U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9U	R/W	0h	Register Files / Instruction Registers RF9 upper (RF9U) Reset Source: mod_g_rst_n

14.9.8.6.2.27 PBIST_RF10U Register

1 PBIST_RF10U Register (Offset = 68h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32577. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0068h**
PBIST0	**3F11 0068h**
WKUP_PBIST0	**2B50 0068h**
WKUP_PBIST1	**2B51 0068h**

Figure 14-10785. PBIST_RF10U Name Register

31	30	29	28	27	26	25	24
RF10U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF10U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF10U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF10U							
R/W							
0h							

Table 14-32579. PBIST_RF10U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10U	R/W	0h	Register Files / Instruction Registers RF10 upper (RF10U) Reset Source: mod_g_rst_n

14.9.8.6.2.28 PBIST_RF11U Register

1 PBIST_RF11U Register (Offset = 6Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32580. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 006Ch**
PBIST0	**3F11 006Ch**
WKUP_PBIST0	**2B50 006Ch**
WKUP_PBIST1	**2B51 006Ch**

Figure 14-10786. PBIST_RF11U Name Register

31	30	29	28	27	26	25	24
RF11U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF11U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF11U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF11U							
R/W							
0h							

Table 14-32582. PBIST_RF11U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11U	R/W	0h	Register Files / Instruction Registers RF11 upper (RF11U) Reset Source: mod_g_rst_n

14.9.8.6.2.29 PBIST_RF12U Register

1 PBIST_RF12U Register (Offset = 70h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32583. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0070h**
PBIST0	**3F11 0070h**
WKUP_PBIST0	**2B50 0070h**
WKUP_PBIST1	**2B51 0070h**

Figure 14-10787. PBIST_RF12U Name Register

31	30	29	28	27	26	25	24
RF12U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12U							
R/W							
0h							

Table 14-32585. PBIST_RF12U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12U	R/W	0h	Register Files / Instruction Registers RF12 upper (RF12U) Reset Source: mod_g_rst_n

14.9.8.6.2.30 PBIST_RF13U Register

1 PBIST_RF13U Register (Offset = 74h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-32586. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0074h**
PBIST0	**3F11 0074h**
WKUP_PBIST0	**2B50 0074h**
WKUP_PBIST1	**2B51 0074h**

Figure 14-10788. PBIST_RF13U Name Register

31	30	29	28	27	26	25	24
RF13U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF13U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF13U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF13U							
R/W							
0h							

Table 14-32588. PBIST_RF13U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13U	R/W	0h	Register Files / Instruction Registers RF13 upper (RF13U) Reset Source: mod_g_rst_n

14.9.8.6.2.31 PBIST_RF14U Register

1 PBIST_RF14U Register (Offset = 78h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32589. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0078h**
PBIST0	**3F11 0078h**
WKUP_PBIST0	**2B50 0078h**
WKUP_PBIST1	**2B51 0078h**

Figure 14-10789. PBIST_RF14U Name Register

31	30	29	28	27	26	25	24
RF14U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF14U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF14U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF14U							
R/W							
0h							

Table 14-32591. PBIST_RF14U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14U	R/W	0h	Register Files / Instruction Registers RF14 upper (RF14U) Reset Source: mod_g_rst_n

14.9.8.6.2.32 PBIST_RF15U Register

1 PBIST_RF15U Register (Offset = 7Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-32592. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 007Ch**
PBIST0	**3F11 007Ch**
WKUP_PBIST0	**2B50 007Ch**
WKUP_PBIST1	**2B51 007Ch**

Figure 14-10790. PBIST_RF15U Name Register

31	30	29	28	27	26	25	24
RF15U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF15U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF15U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF15U							
R/W							
0h							

Table 14-32594. PBIST_RF15U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15U	R/W	0h	Register Files / Instruction Registers RF15 upper (RF15U) Reset Source: mod_g_rst_n

14.9.8.6.2.33 PBIST_A0 Register

1 PBIST_A0 Register (Offset = 100h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-32595. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0100h**
PBIST0	**3F11 0100h**
WKUP_PBIST0	**2B50 0100h**
WKUP_PBIST1	**2B51 0100h**

Figure 14-10791. PBIST_A0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A0							
R/W							
0h							
7	6	5	4	3	2	1	0
A0							
R/W							
0h							

Table 14-32597. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A0	R/W	0h	Variable Address Register 0 (A0) Reset Source: mod_g_rst_n

14.9.8.6.2.34 PBIST_A1 Register

1 PBIST_A1 Register (Offset = 104h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-32598. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0104h**
PBIST0	**3F11 0104h**
WKUP_PBIST0	**2B50 0104h**
WKUP_PBIST1	**2B51 0104h**

Figure 14-10792. PBIST_A1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A1							
R/W							
0h							
7	6	5	4	3	2	1	0
A1							
R/W							
0h							

Table 14-32600. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A1	R/W	0h	Variable Address Register 1 (A1) Reset Source: mod_g_rst_n

14.9.8.6.2.35 PBIST_A2 Register

1 PBIST_A2 Register (Offset = 108h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-32601. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0108h**
PBIST0	**3F11 0108h**
WKUP_PBIST0	**2B50 0108h**
WKUP_PBIST1	**2B51 0108h**

Figure 14-10793. PBIST_A2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">A2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">A2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32603. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A2	R/W	0h	Variable Address Register 2 (A2) Reset Source: mod_g_rst_n

14.9.8.6.2.36 PBIST_A3 Register

1 PBIST_A3 Register (Offset = 10Ch) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-32604. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 010Ch**
PBIST0	**3F11 010Ch**
WKUP_PBIST0	**2B50 010Ch**
WKUP_PBIST1	**2B51 010Ch**

Figure 14-10794. PBIST_A3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A3							
R/W							
0h							
7	6	5	4	3	2	1	0
A3							
R/W							
0h							

Table 14-32606. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A3	R/W	0h	Variable Address Register 3 (A3) Reset Source: mod_g_rst_n

14.9.8.6.2.37 PBIST_L0 Register

1 PBIST_L0 Register (Offset = 110h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-32607. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0110h**
PBIST0	**3F11 0110h**
WKUP_PBIST0	**2B50 0110h**
WKUP_PBIST1	**2B51 0110h**

Figure 14-10795. PBIST_L0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L0							
R/W							
0h							
7	6	5	4	3	2	1	0
L0							
R/W							
0h							

Table 14-32609. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L0	R/W	0h	Variable Loop Count Register 0 (L0) Reset Source: mod_g_rst_n

14.9.8.6.2.38 PBIST_L1 Register

1 PBIST_L1 Register (Offset = 114h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-32610. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0114h**
PBIST0	**3F11 0114h**
WKUP_PBIST0	**2B50 0114h**
WKUP_PBIST1	**2B51 0114h**

Figure 14-10796. PBIST_L1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L1							
R/W							
0h							
7	6	5	4	3	2	1	0
L1							
R/W							
0h							

Table 14-32612. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L1	R/W	0h	Variable Loop Count Register 1 (L1) Reset Source: mod_g_rst_n

14.9.8.6.2.39 PBIST_L2 Register

1 PBIST_L2 Register (Offset = 118h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-32613. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0118h**
PBIST0	**3F11 0118h**
WKUP_PBIST0	**2B50 0118h**
WKUP_PBIST1	**2B51 0118h**

Figure 14-10797. PBIST_L2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L2							
R/W							
0h							
7	6	5	4	3	2	1	0
L2							
R/W							
0h							

Table 14-32615. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L2	R/W	0h	Variable Loop Count Register 2 (L2) Reset Source: mod_g_rst_n

14.9.8.6.2.40 PBIST_L3 Register

1 PBIST_L3 Register (Offset = 11Ch) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-32616. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 011Ch**
PBIST0	**3F11 011Ch**
WKUP_PBIST0	**2B50 011Ch**
WKUP_PBIST1	**2B51 011Ch**

Figure 14-10798. PBIST_L3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L3							
R/W							
0h							
7	6	5	4	3	2	1	0
L3							
R/W							
0h							

Table 14-32618. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L3	R/W	0h	Variable Loop Count Register 3 (L3) Reset Source: mod_g_rst_n

14.9.8.6.2.41 PBIST_D Register

1 PBIST_D Register (Offset = 120h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-32619. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0120h**
PBIST0	**3F11 0120h**
WKUP_PBIST0	**2B50 0120h**
WKUP_PBIST1	**2B51 0120h**

Figure 14-10799. PBIST_D Name Register

31	30	29	28	27	26	25	24
D1							
R/W							
0h							
23	22	21	20	19	18	17	16
D1							
R/W							
0h							
15	14	13	12	11	10	9	8
D0							
R/W							
0h							
7	6	5	4	3	2	1	0
D0							
R/W							
0h							

Table 14-32621. PBIST_D Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	D1	R/W	0h	DD1 Data Register Upper 16 (D1) Reset Source: mod_g_rst_n
15:0	D0	R/W	0h	DD0 Data Register Lower 16 (D0) Reset Source: mod_g_rst_n

14.9.8.6.2.42 PBIST_E Register

1 PBIST_E Register (Offset = 124h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-32622. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0124h**
PBIST0	**3F11 0124h**
WKUP_PBIST0	**2B50 0124h**
WKUP_PBIST1	**2B51 0124h**

Figure 14-10800. PBIST_E Name Register

31	30	29	28	27	26	25	24
E1							
R/W							
0h							
23	22	21	20	19	18	17	16
E1							
R/W							
0h							
15	14	13	12	11	10	9	8
E0							
R/W							
0h							
7	6	5	4	3	2	1	0
E0							
R/W							
0h							

Table 14-32624. PBIST_E Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	E1	R/W	0h	EE1 Data Register Upper 16 (E1) Reset Source: mod_g_rst_n
15:0	E0	R/W	0h	EE0 Data Register Lower 16 (E0) Reset Source: mod_g_rst_n

14.9.8.6.2.43 PBIST_CA0 Register

1 PBIST_CA0 Register (Offset = 130h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-32625. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0130h**
PBIST0	**3F11 0130h**
WKUP_PBIST0	**2B50 0130h**
WKUP_PBIST1	**2B51 0130h**

Figure 14-10801. PBIST_CA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CA0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CA0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32627. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA0	R/W	0h	Constant Address Register 0 (CA0) Reset Source: mod_g_rst_n

14.9.8.6.2.44 PBIST_CA1 Register

1 PBIST_CA1 Register (Offset = 134h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-32628. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0134h**
PBIST0	**3F11 0134h**
WKUP_PBIST0	**2B50 0134h**
WKUP_PBIST1	**2B51 0134h**

Figure 14-10802. PBIST_CA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA1							
R/W							
0h							
7	6	5	4	3	2	1	0
CA1							
R/W							
0h							

Table 14-32630. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA1	R/W	0h	Constant Address Register 1 (CA1) Reset Source: mod_g_rst_n

14.9.8.6.2.45 PBIST_CA2 Register

1 PBIST_CA2 Register (Offset = 138h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-32631. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0138h**
PBIST0	**3F11 0138h**
WKUP_PBIST0	**2B50 0138h**
WKUP_PBIST1	**2B51 0138h**

Figure 14-10803. PBIST_CA2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA2							
R/W							
0h							
7	6	5	4	3	2	1	0
CA2							
R/W							
0h							

Table 14-32633. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA2	R/W	0h	Constant Address Register 2 (CA2) Reset Source: mod_g_rst_n

14.9.8.6.2.46 PBIST_CA3 Register

1 PBIST_CA3 Register (Offset = 13Ch) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-32634. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 013Ch**
PBIST0	**3F11 013Ch**
WKUP_PBIST0	**2B50 013Ch**
WKUP_PBIST1	**2B51 013Ch**

Figure 14-10804. PBIST_CA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA3							
R/W							
0h							
7	6	5	4	3	2	1	0
CA3							
R/W							
0h							

Table 14-32636. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA3	R/W	0h	Constant Address Register 3 (CA3) Reset Source: mod_g_rst_n

14.9.8.6.2.47 PBIST_CL0 Register

1 PBIST_CL0 Register (Offset = 140h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-32637. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0140h**
PBIST0	**3F11 0140h**
WKUP_PBIST0	**2B50 0140h**
WKUP_PBIST1	**2B51 0140h**

Figure 14-10805. PBIST_CL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL0							
R/W							
0h							
7	6	5	4	3	2	1	0
CL0							
R/W							
0h							

Table 14-32639. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL0	R/W	0h	Constant Loop Count Register 0 (CL0) Reset Source: mod_g_rst_n

14.9.8.6.2.48 PBIST_CL1 Register

1 PBIST_CL1 Register (Offset = 144h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-32640. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0144h**
PBIST0	**3F11 0144h**
WKUP_PBIST0	**2B50 0144h**
WKUP_PBIST1	**2B51 0144h**

Figure 14-10806. PBIST_CL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL1							
R/W							
0h							
7	6	5	4	3	2	1	0
CL1							
R/W							
0h							

Table 14-32642. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL1	R/W	0h	Constant Loop Count Register 1 (CL1) Reset Source: mod_g_rst_n

14.9.8.6.2.49 PBIST_CL2 Register

1 PBIST_CL2 Register (Offset = 148h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-32643. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0148h**
PBIST0	**3F11 0148h**
WKUP_PBIST0	**2B50 0148h**
WKUP_PBIST1	**2B51 0148h**

Figure 14-10807. PBIST_CL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CL2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CL2							
R/W							
0h							

Table 14-32645. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL2	R/W	0h	Constant Loop Count Register 2 (CL2) Reset Source: mod_g_rst_n

14.9.8.6.2.50 PBIST_CL3 Register

1 PBIST_CL3 Register (Offset = 14Ch) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-32646. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 014Ch**
PBIST0	**3F11 014Ch**
WKUP_PBIST0	**2B50 014Ch**
WKUP_PBIST1	**2B51 014Ch**

Figure 14-10808. PBIST_CL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL3							
R/W							
0h							
7	6	5	4	3	2	1	0
CL3							
R/W							
0h							

Table 14-32648. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL3	R/W	0h	Constant Loop Count Register 3 (CL3) Reset Source: mod_g_rst_n

14.9.8.6.2.51 PBIST_I0 Register

1 PBIST_I0 Register (Offset = 150h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-32649. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0150h**
PBIST0	**3F11 0150h**
WKUP_PBIST0	**2B50 0150h**
WKUP_PBIST1	**2B51 0150h**

Figure 14-10809. PBIST_I0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-32651. PBIST_I0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 0 (I0) Reset Source: mod_g_rst_n

14.9.8.6.2.52 PBIST_I1 Register

1 PBIST_I1 Register (Offset = 154h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-32652. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0154h**
PBIST0	**3F11 0154h**
WKUP_PBIST0	**2B50 0154h**
WKUP_PBIST1	**2B51 0154h**

Figure 14-10810. PBIST_I1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-32654. PBIST_I1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 1 (I1) Reset Source: mod_g_rst_n

14.9.8.6.2.53 PBIST_I2 Register

1 PBIST_I2 Register (Offset = 158h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-32655. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0158h**
PBIST0	**3F11 0158h**
WKUP_PBIST0	**2B50 0158h**
WKUP_PBIST1	**2B51 0158h**

Figure 14-10811. PBIST_I2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32657. PBIST_I2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 2 (I2) Reset Source: mod_g_rst_n

14.9.8.6.2.54 PBIST_I3 Register

1 PBIST_I3 Register (Offset = 15Ch) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-32658. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 015Ch**
PBIST0	**3F11 015Ch**
WKUP_PBIST0	**2B50 015Ch**
WKUP_PBIST1	**2B51 015Ch**

Figure 14-10812. PBIST_I3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-32660. PBIST_I3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 3 (I3) Reset Source: mod_g_rst_n

14.9.8.6.2.55 PBIST_RAMT Register

1 PBIST_RAMT Register (Offset = 160h) [reset = 0h]

RAM Configuration Register

Return to Summary Table

Table 14-32661. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0160h**
PBIST0	**3F11 0160h**
WKUP_PBIST0	**2B50 0160h**
WKUP_PBIST1	**2B51 0160h**

Figure 14-10813. PBIST_RAMT Name Register

31	30	29	28	27	26	25	24
RGS							
R/W							
0h							
23	22	21	20	19	18	17	16
RDS							
R/W							
0h							
15	14	13	12	11	10	9	8
DWR							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		PLS				RLS	
NONE		R/W				R/W	
0h		0h				0h	

Table 14-32663. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RGS	R/W	0h	RAM Group Select RGS Reset Source: mod_g_rst_n
23:16	RDS	R/W	0h	Return Data select RDS Reset Source: mod_g_rst_n
15:8	DWR	R/W	0h	Data Width Register DWR Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:2	PLS	R/W	0h	Pipeline Latency Select Reset Source: mod_g_rst_n
1:0	RLS	R/W	0h	RAM Latency Select Reset Source: mod_g_rst_n

14.9.8.6.2.56 PBIST_DLR Register

1 PBIST_DLR Register (Offset = 164h) [reset = 208h]

Datalogger Register

Return to Summary Table

Table 14-32664. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0164h**
PBIST0	**3F11 0164h**
WKUP_PBIST0	**2B50 0164h**
WKUP_PBIST1	**2B51 0164h**

Figure 14-10814. PBIST_DLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
BRP							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DLR1_RTM	DLR1_GNG	DLR1_MISR
NONE					R/W	R/W	R/W
0h					0h	1h	0h
7	6	5	4	3	2	1	0
DLR0_TSM	DLR0_CFMM	DLR0_ECAM	DLR0_CAM	DLR0_TCK	DLR0_ROM	DLR0_IDDQ	DLR0_DCM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	0h	0h	0h

Table 14-32666. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	BRP	R/W	0h	Datalogger 2 (BRP) Reset Source: mod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10	DLR1_RTM	R/W	0h	Retention testing mode Reset Source: mod_g_rst_n
9	DLR1_GNG	R/W	1h	GO / NO-GO testing mode Reset Source: mod_g_rst_n
8	DLR1_MISR	R/W	0h	MISR testing mode (mainly for ROM testing) Reset Source: mod_g_rst_n
7	DLR0_TSM	R/W	0h	Time stamp mode Reset Source: mod_g_rst_n
6	DLR0_CFMM	R/W	0h	Column Fail Masking mode Reset Source: mod_g_rst_n

Table 14-32666. PBIST_DLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DLR0_ECAM	R/W	0h	Emulation cache access mode Reset Source: mod_g_rst_n
4	DLR0_CAM	R/W	0h	Config access mode Reset Source: mod_g_rst_n
3	DLR0_TCK	R/W	1h	TCK Gated mode Reset Source: mod_g_rst_n
2	DLR0_ROM	R/W	0h	ROM-based testing mode Reset Source: mod_g_rst_n
1	DLR0_IDDQ	R/W	0h	IDDQ testing mode Reset Source: mod_g_rst_n
0	DLR0_DCM	R/W	0h	Distributed Compare mode Reset Source: mod_g_rst_n

14.9.8.6.2.57 PBIST_CMS Register

1 PBIST_CMS Register (Offset = 168h) [reset = 0h]

Clock-Mux Select Register

Return to Summary Table

Table 14-32667. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0168h**
PBIST0	**3F11 0168h**
WKUP_PBIST0	**2B50 0168h**
WKUP_PBIST1	**2B51 0168h**

Figure 14-10815. PBIST_CMS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMS			
NONE				R/W			
0h				0h			

Table 14-32669. PBIST_CMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CMS	R/W	0h	Clock Mux Select (CMS) Reset Source: mod_g_rst_n

14.9.8.6.2.58 PBIST_STR Register

1 PBIST_STR Register (Offset = 16Ch) [reset = 0h]

Program Control Register

Return to Summary Table

Table 14-32670. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 016Ch**
PBIST0	**3F11 016Ch**
WKUP_PBIST0	**2B50 016Ch**
WKUP_PBIST1	**2B51 016Ch**

Figure 14-10816. PBIST_STR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CHK	STEP	STOP	RES	START
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-32672. PBIST_STR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CHK	R/W	0h	Check MISR mode Reset Source: mod_g_rst_n
3	STEP	R/W	0h	Step / Step for emulation mode Reset Source: mod_g_rst_n
2	STOP	R/W	0h	Stop Reset Source: mod_g_rst_n
1	RES	R/W	0h	Resume / Emulation read Reset Source: mod_g_rst_n
0	START	R/W	0h	Start / Time Stamp mode restart Reset Source: mod_g_rst_n

14.9.8.6.2.59 PBIST_SCR Register

1 PBIST_SCR Register (Offset = 170h) [reset = FEDCBA9876542F40h]

Address Scrambling Register

Return to Summary Table

Table 14-32673. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0170h**
PBIST0	**3F11 0170h**
WKUP_PBIST0	**2B50 0170h**
WKUP_PBIST1	**2B51 0170h**

Figure 14-10817. PBIST_SCR Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">SCR7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FEh</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">SCR6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">DCh</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">SCR5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">BAh</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">SCR4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">98h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SCR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">32h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SCR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-32675. PBIST_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	SCR7	R/W	FEh	Address Scrambling Register 7 Reset Source: mod_g_rst_n
55:48	SCR6	R/W	DCh	Address Scrambling Register 6 Reset Source: mod_g_rst_n
47:40	SCR5	R/W	BAh	Address Scrambling Register 5 Reset Source: mod_g_rst_n

Table 14-32675. PBIST_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	SCR4	R/W	98h	Address Scrambling Register 4 Reset Source: mod_g_rst_n
31:24	SCR3	R/W	76h	Address Scrambling Register 3 Reset Source: mod_g_rst_n
23:16	SCR2	R/W	54h	Address Scrambling Register 2 Reset Source: mod_g_rst_n
15:8	SCR1	R/W	32h	Address Scrambling Register 1 Reset Source: mod_g_rst_n
7:0	SCR0	R/W	10h	Address Scrambling Register 0 Reset Source: mod_g_rst_n

14.9.8.6.2.60 PBIST_CSR Register

1 PBIST_CSR Register (Offset = 178h) [reset = 0h]

Chip Select Register

Return to Summary Table

Table 14-32676. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0178h**
PBIST0	**3F11 0178h**
WKUP_PBIST0	**2B50 0178h**
WKUP_PBIST1	**2B51 0178h**

Figure 14-10818. PBIST_CSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CSR3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CSR2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CSR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CSR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32678. PBIST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CSR3	R/W	0h	Chip Select 3 (CSR3) Reset Source: mod_g_rst_n
23:16	CSR2	R/W	0h	Chip Select 2 (CSR2) Reset Source: mod_g_rst_n
15:8	CSR1	R/W	0h	Chip Select 1(CSR1) Reset Source: mod_g_rst_n
7:0	CSR0	R/W	0h	Chip Select 0 (CSR0) Reset Source: mod_g_rst_n

14.9.8.6.2.61 PBIST_FDLY Register

1 PBIST_FDLY Register (Offset = 17Ch) [reset = 68h]

Fail Delay Register

Return to Summary Table

Table 14-32679. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 017Ch**
PBIST0	**3F11 017Ch**
WKUP_PBIST0	**2B50 017Ch**
WKUP_PBIST1	**2B51 017Ch**

Figure 14-10819. PBIST_FDLY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDLY							
R/W							
68h							

Table 14-32681. PBIST_FDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDLY	R/W	68h	Fail Delay (FDLY) Reset Source: mod_g_rst_n

14.9.8.6.2.62 PBIST_PACT Register

1 PBIST_PACT Register (Offset = 180h) [reset = 0h]

PACT Register

Return to Summary Table

Table 14-32682. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0180h**
PBIST0	**3F11 0180h**
WKUP_PBIST0	**2B50 0180h**
WKUP_PBIST1	**2B51 0180h**

Figure 14-10820. PBIST_PACT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PACT
NONE							R/W
0h							0h

Table 14-32684. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PACT	R/W	0h	PBIST Activate (PACT) Reset Source: mod_g_rst_n

14.9.8.6.2.63 PBIST_PID Register

1 PBIST_PID Register (Offset = 184h) [reset = 0h]

PBIST_ID Register

Return to Summary Table

Table 14-32685. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0184h**
PBIST0	**3F11 0184h**
WKUP_PBIST0	**2B50 0184h**
WKUP_PBIST1	**2B51 0184h**

Figure 14-10821. PBIST_PID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PID				
NONE			R/W				
0h			0h				

Table 14-32687. PBIST_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PID	R/W	0h	PBIST ID Reset Source: mod_g_rst_n

14.9.8.6.2.64 PBIST_OVER Register

1 PBIST_OVER Register (Offset = 188h) [reset = 9h]

Override Register

Return to Summary Table

Table 14-32688. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0188h**
PBIST0	**3F11 0188h**
WKUP_PBIST0	**2B50 0188h**
WKUP_PBIST1	**2B51 0188h**

Figure 14-10822. PBIST_OVER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ALGO	MM	READ	RINFO
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	1h

Table 14-32690. PBIST_OVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ALGO	R/W	1h	PBIST Override Algorithm Override Reset Source: mod_g_rst_n
2	MM	R/W	0h	PBIST Override Multiple Memory Reset Source: mod_g_rst_n
1	READ	R/W	0h	PBIST Override READ Override Reset Source: mod_g_rst_n
0	RINFO	R/W	1h	PBIST Override RINFO Override Reset Source: mod_g_rst_n

14.9.8.6.2.65 PBIST_FSRF Register

1 PBIST_FSRF Register (Offset = 190h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-32691. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0190h**
PBIST0	**3F11 0190h**
WKUP_PBIST0	**2B50 0190h**
WKUP_PBIST1	**2B51 0190h**

Figure 14-10823. PBIST_FSRF Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							FRSF1
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FRSF0
NONE							R
0h							0h

Table 14-32693. PBIST_FSRF Register Field Descriptions

Bit	Field	Type	Reset	Description
63:33	RESERVED	NONE	0h	Reserved
32	FRSF1	R	0h	Fail Status Fail - Port 1 (FSRF1) Reset Source: mod_g_rst_n
31:1	RESERVED	NONE	0h	Reserved
0	FRSF0	R	0h	Fail Status Fail - Port 0 (FSRF0) Reset Source: mod_g_rst_n

14.9.8.6.2.66 PBIST_FSRC Register

1 PBIST_FSRC Register (Offset = 198h) [reset = 0h]

Fail Status Count Register

Return to Summary Table

Table 14-32694. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 0198h**
PBIST0	**3F11 0198h**
WKUP_PBIST0	**2B50 0198h**
WKUP_PBIST1	**2B51 0198h**

Figure 14-10824. PBIST_FSRC Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-32696. PBIST_FSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
63:36	RESERVED	NONE	0h	Reserved
35:32	FSRC1	R	0h	Fail Status Count - Port 1 (FSRC1) Reset Source: mod_g_rst_n
31:4	RESERVED	NONE	0h	Reserved
3:0	FSRC0	R	0h	Fail Status Count - Port 0 (FSRC0) Reset Source: mod_g_rst_n

14.9.8.6.2.67 PBIST_FSRA Register

1 PBIST_FSRA Register (Offset = 1A0h) [reset = 0h]

Fail Status Address Register

Return to Summary Table

Table 14-32697. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01A0h**
PBIST0	**3F11 01A0h**
WKUP_PBIST0	**2B50 01A0h**
WKUP_PBIST1	**2B51 01A0h**

Figure 14-10825. PBIST_FSRA Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
FSRA1							
R							
0h							
39	38	37	36	35	34	33	32
FSRA1							
R							
0h							
15	14	13	12	11	10	9	8
FSRA0							
R							
0h							
7	6	5	4	3	2	1	0
FSRA0							
R							
0h							

Table 14-32699. PBIST_FSRA Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RESERVED	NONE	0h	Reserved
47:32	FSRA1	R	0h	Fail Status Address - Port 1 (FSRA1) Reset Source: mod_g_rst_n
31:16	RESERVED	NONE	0h	Reserved
15:0	FSRA0	R	0h	Fail Status Address - Port 0 (FSRA0) Reset Source: mod_g_rst_n

14.9.8.6.2.68 PBIST_FSRDL0 Register

1 PBIST_FSRDL0 Register (Offset = 1A8h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-32700. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01A8h**
PBIST0	**3F11 01A8h**
WKUP_PBIST0	**2B50 01A8h**
WKUP_PBIST1	**2B51 01A8h**

Figure 14-10826. PBIST_FSRDL0 Name Register

31	30	29	28	27	26	25	24
FSRDL0							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL0							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL0							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL0							
R							
0h							

Table 14-32702. PBIST_FSRDL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL0	R	0h	Fail Status Data - Port 0 (FSRDL0) Reset Source: mod_g_rst_n

14.9.8.6.2.69 PBIST_FSRDL1 Register

1 PBIST_FSRDL1 Register (Offset = 1B0h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-32703. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01B0h**
PBIST0	**3F11 01B0h**
WKUP_PBIST0	**2B50 01B0h**
WKUP_PBIST1	**2B51 01B0h**

Figure 14-10827. PBIST_FSRDL1 Name Register

31	30	29	28	27	26	25	24
FSRDL1							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL1							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL1							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL1							
R							
0h							

Table 14-32705. PBIST_FSRDL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL1	R	0h	Fail Status Data - Port 1 (FSRDL1) Reset Source: mod_g_rst_n

14.9.8.6.2.70 PBIST_MARGIN_MODE Register

1 PBIST_MARGIN_MODE Register (Offset = 1B4h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-32706. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01B4h**
PBIST0	**3F11 01B4h**
WKUP_PBIST0	**2B50 01B4h**
WKUP_PBIST1	**2B51 01B4h**

Figure 14-10828. PBIST_MARGIN_MODE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PBIST_DFT_READ		PBIST_DFT_WRITE	
NONE				R		R	
0h				0h		0h	

Table 14-32708. PBIST_MARGIN_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	PBIST_DFT_READ	R	0h	pbist_dft_read[1:0] Reset Source: mod_g_rst_n
1:0	PBIST_DFT_WRITE	R	0h	pbist_dft_write[1:0] Reset Source: mod_g_rst_n

14.9.8.6.2.71 PBIST_WRENZ Register

1 PBIST_WRENZ Register (Offset = 1B8h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-32709. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01B8h**
PBIST0	**3F11 01B8h**
WKUP_PBIST0	**2B50 01B8h**
WKUP_PBIST1	**2B51 01B8h**

Figure 14-10829. PBIST_WRENZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WRENZ	
NONE						R	
0h						0h	

Table 14-32711. PBIST_WRENZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	WRENZ	R	0h	pbist_ram_wrenz[1:0] Reset Source: mod_g_rst_n

14.9.8.6.2.72 PBIST_PAGE_PGS Register

1 PBIST_PAGE_PGS Register (Offset = 1BCh) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-32712. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01BCh**
PBIST0	**3F11 01BCh**
WKUP_PBIST0	**2B50 01BCh**
WKUP_PBIST1	**2B51 01BCh**

Figure 14-10830. PBIST_PAGE_PGS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PGS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-32714. PBIST_PAGE_PGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PGS	R	0h	pbist_ram_pgs[1:0] Reset Source: mod_g_rst_n

14.9.8.6.2.73 PBIST_ROM Register

1 PBIST_ROM Register (Offset = 1C0h) [reset = 3h]

ROM Mask Register

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Table 14-32715. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01C0h**
PBIST0	**3F11 01C0h**
WKUP_PBIST0	**2B50 01C0h**
WKUP_PBIST1	**2B51 01C0h**

Figure 14-10831. PBIST_ROM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROM	
NONE						R/W	
0h						3h	

Table 14-32717. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ROM	R/W	3h	ROM Mask (ROM) Reset Source: mod_g_rst_n

14.9.8.6.2.74 PBIST_ALGO Register

1 PBIST_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

Algorithm Mask Register

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Table 14-32718. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01C4h**
PBIST0	**3F11 01C4h**
WKUP_PBIST0	**2B50 01C4h**
WKUP_PBIST1	**2B51 01C4h**

Figure 14-10832. PBIST_ALGO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ALGO_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ALGO_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALGO_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALGO_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-32720. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO_3	R/W	FFh	ROM Algorithm Mask 3 (ALGO 3) Reset Source: mod_g_rst_n
23:16	ALGO_2	R/W	FFh	ROM Algorithm Mask 2 (ALGO 2) Reset Source: mod_g_rst_n
15:8	ALGO_1	R/W	FFh	ROM Algorithm Mask 1 (ALGO 1) Reset Source: mod_g_rst_n
7:0	ALGO_0	R/W	FFh	ROM Algorithm Mask 0 (ALGO 0) Reset Source: mod_g_rst_n

14.9.8.6.2.75 PBIST_RINFO Register

1 PBIST_RINFO Register (Offset = 1C8h) [reset = 1000000000000180h]

RAM Info Mask Register

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Table 14-32721. Instance Table

Instance Name	Physical Address
MCU_PBIST0	**04F0 01C8h**
PBIST0	**3F11 01C8h**
WKUP_PBIST0	**2B50 01C8h**
WKUP_PBIST1	**2B51 01C8h**

Figure 14-10833. PBIST_RINFO Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">U3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">U2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">U1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">U0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">L0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-32723. PBIST_RINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	U3	R/W	FFh	RAM Info Mask Upper 3 (RINFOU3) Reset Source: mod_g_rst_n
55:48	U2	R/W	FFh	RAM Info Mask Upper 2 (RINFOU2) Reset Source: mod_g_rst_n
47:40	U1	R/W	FFh	RAM Info Mask Upper 1 (RINFOU1) Reset Source: mod_g_rst_n

Table 14-32723. PBIST_RINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	U0	R/W	FFh	RAM Info Mask Upper 0 (RINFOU0) Reset Source: mod_g_rst_n
31:24	L3	R/W	FFh	RAM Info Mask Lower 3 (RINFOL3) Reset Source: mod_g_rst_n
23:16	L2	R/W	FFh	RAM Info Mask Lower 2 (RINFOL2) Reset Source: mod_g_rst_n
15:8	L1	R/W	FFh	RAM Info Mask Lower 1 (RINFOL1) Reset Source: mod_g_rst_n
7:0	L0	R/W	FFh	RAM Info Mask Lower 0 (RINFOL0) Reset Source: mod_g_rst_n

14.10 On-Chip Debug Registers

14.10.1 debugss

debugss

14.10.1.1 debugss Summaries

debugss Summaries

Table 14-32724. DEBUGSS_SYS Registers, Base Address=4100 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	DEBUGSS_SYS_TRACE	4100 0000h

Table 14-32725. DEBUGSS_DEBUG_CELL_ROM_SLV Registers, Base Address=0007 3C02 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1	0007 3C02 0004h
8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2	0007 3C02 0008h
Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3	0007 3C02 000Ch
10h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4	0007 3C02 0010h
14h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5	0007 3C02 0014h
18h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6	0007 3C02 0018h
1Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7	0007 3C02 001Ch
20h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8	0007 3C02 0020h
24h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9	0007 3C02 0024h
28h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10	0007 3C02 0028h
2Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11	0007 3C02 002Ch
30h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12	0007 3C02 0030h
34h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13	0007 3C02 0034h
50h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14	0007 3C02 0050h
FD0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4	0007 3C02 0FD0h
FD4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5	0007 3C02 0FD4h
FD8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6	0007 3C02 0FD8h
FDCh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7	0007 3C02 0FDCh
FE0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0	0007 3C02 0FE0h
FE4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1	0007 3C02 0FE4h
FE8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2	0007 3C02 0FE8h
FECh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3	0007 3C02 0FECh
FF0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0	0007 3C02 0FF0h
FF4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1	0007 3C02 0FF4h
FF8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2	0007 3C02 0FF8h
FFCh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3	0007 3C02 0FFCh

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CTSET2_CFG_CTSETID	0007 3C02 2000h
10h	32	CTSET2_CFG_CTSETSYSCFG	0007 3C02 2010h
14h	32	CTSET2_CFG_SETSTR	0007 3C02 2014h

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
18h	32	CTSET2_CFG_DBGTIMELOW	0007 3C02 2018h
1Ch	32	CTSET2_CFG_DBGTIMEHI	0007 3C02 201Ch
24h	32	CTSET2_CFG_CTSETCFG	0007 3C02 2024h
28h	32	CTSET2_CFG_SETSPLREG	0007 3C02 2028h
30h	32	CTSET2_CFG_SETEVTENBL1	0007 3C02 2030h
34h	32	CTSET2_CFG_SETEVTENBL2	0007 3C02 2034h
38h	32	CTSET2_CFG_SETEVTENBL3	0007 3C02 2038h
3Ch	32	CTSET2_CFG_SETEVTENBL4	0007 3C02 203Ch
40h	32	CTSET2_CFG_SETEVTENBL5	0007 3C02 2040h
44h	32	CTSET2_CFG_SETEVTENBL6	0007 3C02 2044h
48h	32	CTSET2_CFG_SETEVTENBL7	0007 3C02 2048h
4Ch	32	CTSET2_CFG_SETEVTENBL8	0007 3C02 204Ch
50h	32	CTSET2_CFG_SETMSTID	0007 3C02 2050h
800h	32	CTSET2_CFG_CTCNTL	0007 3C02 2800h
804h	32	CTSET2_CFG_CTNUMDBG	0007 3C02 2804h
808h	32	CTSET2_CFG_CTUSERACCCTL	0007 3C02 2808h
820h	32	CTSET2_CFG_CTSTMCNTL	0007 3C02 2820h
824h	32	CTSET2_CFG_CTSTMMSTID	0007 3C02 2824h
828h	32	CTSET2_CFG_CTSTMINTVL	0007 3C02 2828h
82Ch	32	CTSET2_CFG_CTSTMSEL0	0007 3C02 282Ch
830h	32	CTSET2_CFG_CTSTMSEL1	0007 3C02 2830h
840h	32	CTSET2_CFG_CTINTVLR0	0007 3C02 2840h
844h	32	CTSET2_CFG_CTINTVLR1	0007 3C02 2844h
848h	32	CTSET2_CFG_CTINTVLR2	0007 3C02 2848h
84Ch	32	CTSET2_CFG_CTINTVLR3	0007 3C02 284Ch
850h	32	CTSET2_CFG_CTINTVLR4	0007 3C02 2850h
854h	32	CTSET2_CFG_CTINTVLR5	0007 3C02 2854h
858h	32	CTSET2_CFG_CTINTVLR6	0007 3C02 2858h
85Ch	32	CTSET2_CFG_CTINTVLR7	0007 3C02 285Ch
860h	32	CTSET2_CFG_CTINTVLR8	0007 3C02 2860h
864h	32	CTSET2_CFG_CTINTVLR9	0007 3C02 2864h
868h	32	CTSET2_CFG_CTINTVLR10	0007 3C02 2868h
86Ch	32	CTSET2_CFG_CTINTVLR11	0007 3C02 286Ch
870h	32	CTSET2_CFG_CTINTVLR12	0007 3C02 2870h
874h	32	CTSET2_CFG_CTINTVLR13	0007 3C02 2874h
878h	32	CTSET2_CFG_CTINTVLR14	0007 3C02 2878h
87Ch	32	CTSET2_CFG_CTINTVLR15	0007 3C02 287Ch
8A0h	32	CTSET2_CFG_CTDBGSGL0	0007 3C02 28A0h
8A4h	32	CTSET2_CFG_CTDBGSGL1	0007 3C02 28A4h
8A8h	32	CTSET2_CFG_CTDBGSGL2	0007 3C02 28A8h
8ACh	32	CTSET2_CFG_CTDBGSGL3	0007 3C02 28ACh
8B0h	32	CTSET2_CFG_CTDBGSGL4	0007 3C02 28B0h
8B4h	32	CTSET2_CFG_CTDBGSGL5	0007 3C02 28B4h
8B8h	32	CTSET2_CFG_CTDBGSGL6	0007 3C02 28B8h
8BCh	32	CTSET2_CFG_CTDBGSGL7	0007 3C02 28BCh

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
9F0h	32	CTSET2_CFG_CTGNBL0	0007 3C02 29F0h
9F4h	32	CTSET2_CFG_CTGNBL1	0007 3C02 29F4h
9F8h	32	CTSET2_CFG_CTGRST0	0007 3C02 29F8h
9FCh	32	CTSET2_CFG_CTGRST1	0007 3C02 29FCh
A00h	32	CTSET2_CFG_CTCR0	0007 3C02 2A00h
A04h	32	CTSET2_CFG_CTCR1	0007 3C02 2A04h
A08h	32	CTSET2_CFG_CTCR2	0007 3C02 2A08h
A0Ch	32	CTSET2_CFG_CTCR3	0007 3C02 2A0Ch
A10h	32	CTSET2_CFG_CTCR4	0007 3C02 2A10h
A14h	32	CTSET2_CFG_CTCR5	0007 3C02 2A14h
A18h	32	CTSET2_CFG_CTCR6	0007 3C02 2A18h
A1Ch	32	CTSET2_CFG_CTCR7	0007 3C02 2A1Ch
A20h	32	CTSET2_CFG_CTCR8	0007 3C02 2A20h
A24h	32	CTSET2_CFG_CTCR9	0007 3C02 2A24h
A28h	32	CTSET2_CFG_CTCR10	0007 3C02 2A28h
A2Ch	32	CTSET2_CFG_CTCR11	0007 3C02 2A2Ch
A30h	32	CTSET2_CFG_CTCR12	0007 3C02 2A30h
A34h	32	CTSET2_CFG_CTCR13	0007 3C02 2A34h
A38h	32	CTSET2_CFG_CTCR14	0007 3C02 2A38h
A3Ch	32	CTSET2_CFG_CTCR15	0007 3C02 2A3Ch
A40h	32	CTSET2_CFG_CTCR16	0007 3C02 2A40h
A44h	32	CTSET2_CFG_CTCR17	0007 3C02 2A44h
A48h	32	CTSET2_CFG_CTCR18	0007 3C02 2A48h
A4Ch	32	CTSET2_CFG_CTCR19	0007 3C02 2A4Ch
A50h	32	CTSET2_CFG_CTCR20	0007 3C02 2A50h
A54h	32	CTSET2_CFG_CTCR21	0007 3C02 2A54h
A58h	32	CTSET2_CFG_CTCR22	0007 3C02 2A58h
A5Ch	32	CTSET2_CFG_CTCR23	0007 3C02 2A5Ch
A60h	32	CTSET2_CFG_CTCR24	0007 3C02 2A60h
A64h	32	CTSET2_CFG_CTCR25	0007 3C02 2A64h
A68h	32	CTSET2_CFG_CTCR26	0007 3C02 2A68h
A6Ch	32	CTSET2_CFG_CTCR27	0007 3C02 2A6Ch
A70h	32	CTSET2_CFG_CTCR28	0007 3C02 2A70h
A74h	32	CTSET2_CFG_CTCR29	0007 3C02 2A74h
A78h	32	CTSET2_CFG_CTCR30	0007 3C02 2A78h
A7Ch	32	CTSET2_CFG_CTCR31	0007 3C02 2A7Ch
A80h	32	CTSET2_CFG_CTOWN0	0007 3C02 2A80h
A84h	32	CTSET2_CFG_CTOWN1	0007 3C02 2A84h
A88h	32	CTSET2_CFG_CTOWN2	0007 3C02 2A88h
A8Ch	32	CTSET2_CFG_CTOWN3	0007 3C02 2A8Ch
A90h	32	CTSET2_CFG_CTOWN4	0007 3C02 2A90h
A94h	32	CTSET2_CFG_CTOWN5	0007 3C02 2A94h
A98h	32	CTSET2_CFG_CTOWN6	0007 3C02 2A98h
A9Ch	32	CTSET2_CFG_CTOWN7	0007 3C02 2A9Ch
AA0h	32	CTSET2_CFG_CTOWN8	0007 3C02 2AA0h

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
AA4h	32	CTSET2_CFG_CTOWN9	0007 3C02 2AA4h
AA8h	32	CTSET2_CFG_CTOWN10	0007 3C02 2AA8h
AACh	32	CTSET2_CFG_CTOWN11	0007 3C02 2AACh
AB0h	32	CTSET2_CFG_CTOWN12	0007 3C02 2AB0h
AB4h	32	CTSET2_CFG_CTOWN13	0007 3C02 2AB4h
AB8h	32	CTSET2_CFG_CTOWN14	0007 3C02 2AB8h
ABCh	32	CTSET2_CFG_CTOWN15	0007 3C02 2ABCh
AC0h	32	CTSET2_CFG_CTOWN16	0007 3C02 2AC0h
AC4h	32	CTSET2_CFG_CTOWN17	0007 3C02 2AC4h
AC8h	32	CTSET2_CFG_CTOWN18	0007 3C02 2AC8h
ACCh	32	CTSET2_CFG_CTOWN19	0007 3C02 2ACCh
AD0h	32	CTSET2_CFG_CTOWN20	0007 3C02 2AD0h
AD4h	32	CTSET2_CFG_CTOWN21	0007 3C02 2AD4h
AD8h	32	CTSET2_CFG_CTOWN22	0007 3C02 2AD8h
ADCh	32	CTSET2_CFG_CTOWN23	0007 3C02 2ADCh
AE0h	32	CTSET2_CFG_CTOWN24	0007 3C02 2AE0h
AE4h	32	CTSET2_CFG_CTOWN25	0007 3C02 2AE4h
AE8h	32	CTSET2_CFG_CTOWN26	0007 3C02 2AE8h
AECh	32	CTSET2_CFG_CTOWN27	0007 3C02 2AECh
AF0h	32	CTSET2_CFG_CTOWN28	0007 3C02 2AF0h
AF4h	32	CTSET2_CFG_CTOWN29	0007 3C02 2AF4h
AF8h	32	CTSET2_CFG_CTOWN30	0007 3C02 2AF8h
AFCh	32	CTSET2_CFG_CTOWN31	0007 3C02 2AFCh
B00h	32	CTSET2_CFG_CTFILT0	0007 3C02 2B00h
B04h	32	CTSET2_CFG_CTFILT1	0007 3C02 2B04h
B08h	32	CTSET2_CFG_CTFILT2	0007 3C02 2B08h
B0Ch	32	CTSET2_CFG_CTFILT3	0007 3C02 2B0Ch
B10h	32	CTSET2_CFG_CTFILT4	0007 3C02 2B10h
B14h	32	CTSET2_CFG_CTFILT5	0007 3C02 2B14h
B18h	32	CTSET2_CFG_CTFILT6	0007 3C02 2B18h
B1Ch	32	CTSET2_CFG_CTFILT7	0007 3C02 2B1Ch
B20h	32	CTSET2_CFG_CTFILT8	0007 3C02 2B20h
B24h	32	CTSET2_CFG_CTFILT9	0007 3C02 2B24h
B28h	32	CTSET2_CFG_CTFILT10	0007 3C02 2B28h
B2Ch	32	CTSET2_CFG_CTFILT11	0007 3C02 2B2Ch
B30h	32	CTSET2_CFG_CTFILT12	0007 3C02 2B30h
B34h	32	CTSET2_CFG_CTFILT13	0007 3C02 2B34h
B38h	32	CTSET2_CFG_CTFILT14	0007 3C02 2B38h
B3Ch	32	CTSET2_CFG_CTFILT15	0007 3C02 2B3Ch
B40h	32	CTSET2_CFG_CTFILT16	0007 3C02 2B40h
B44h	32	CTSET2_CFG_CTFILT17	0007 3C02 2B44h
B48h	32	CTSET2_CFG_CTFILT18	0007 3C02 2B48h
B4Ch	32	CTSET2_CFG_CTFILT19	0007 3C02 2B4Ch
B50h	32	CTSET2_CFG_CTFILT20	0007 3C02 2B50h
B54h	32	CTSET2_CFG_CTFILT21	0007 3C02 2B54h

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
B58h	32	CTSET2_CFG_CTFILT22	0007 3C02 2B58h
B5Ch	32	CTSET2_CFG_CTFILT23	0007 3C02 2B5Ch
B60h	32	CTSET2_CFG_CTFILT24	0007 3C02 2B60h
B64h	32	CTSET2_CFG_CTFILT25	0007 3C02 2B64h
B68h	32	CTSET2_CFG_CTFILT26	0007 3C02 2B68h
B6Ch	32	CTSET2_CFG_CTFILT27	0007 3C02 2B6Ch
B70h	32	CTSET2_CFG_CTFILT28	0007 3C02 2B70h
B74h	32	CTSET2_CFG_CTFILT29	0007 3C02 2B74h
B78h	32	CTSET2_CFG_CTFILT30	0007 3C02 2B78h
B7Ch	32	CTSET2_CFG_CTFILT31	0007 3C02 2B7Ch
B80h	32	CTSET2_CFG_CTCNTR0	0007 3C02 2B80h
B84h	32	CTSET2_CFG_CTCNTR1	0007 3C02 2B84h
B88h	32	CTSET2_CFG_CTCNTR2	0007 3C02 2B88h
B8Ch	32	CTSET2_CFG_CTCNTR3	0007 3C02 2B8Ch
B90h	32	CTSET2_CFG_CTCNTR4	0007 3C02 2B90h
B94h	32	CTSET2_CFG_CTCNTR5	0007 3C02 2B94h
B98h	32	CTSET2_CFG_CTCNTR6	0007 3C02 2B98h
B9Ch	32	CTSET2_CFG_CTCNTR7	0007 3C02 2B9Ch
BA0h	32	CTSET2_CFG_CTCNTR8	0007 3C02 2BA0h
BA4h	32	CTSET2_CFG_CTCNTR9	0007 3C02 2BA4h
BA8h	32	CTSET2_CFG_CTCNTR10	0007 3C02 2BA8h
BACh	32	CTSET2_CFG_CTCNTR11	0007 3C02 2BACh
BB0h	32	CTSET2_CFG_CTCNTR12	0007 3C02 2BB0h
BB4h	32	CTSET2_CFG_CTCNTR13	0007 3C02 2BB4h
BB8h	32	CTSET2_CFG_CTCNTR14	0007 3C02 2BB8h
BBCh	32	CTSET2_CFG_CTCNTR15	0007 3C02 2BBCh
BC0h	32	CTSET2_CFG_CTCNTR16	0007 3C02 2BC0h
BC4h	32	CTSET2_CFG_CTCNTR17	0007 3C02 2BC4h
BC8h	32	CTSET2_CFG_CTCNTR18	0007 3C02 2BC8h
BCCh	32	CTSET2_CFG_CTCNTR19	0007 3C02 2BCCh
BD0h	32	CTSET2_CFG_CTCNTR20	0007 3C02 2BD0h
BD4h	32	CTSET2_CFG_CTCNTR21	0007 3C02 2BD4h
BD8h	32	CTSET2_CFG_CTCNTR22	0007 3C02 2BD8h
BDCh	32	CTSET2_CFG_CTCNTR23	0007 3C02 2BDCh
BE0h	32	CTSET2_CFG_CTCNTR24	0007 3C02 2BE0h
BE4h	32	CTSET2_CFG_CTCNTR25	0007 3C02 2BE4h
BE8h	32	CTSET2_CFG_CTCNTR26	0007 3C02 2BE8h
BECh	32	CTSET2_CFG_CTCNTR27	0007 3C02 2BECh
BF0h	32	CTSET2_CFG_CTCNTR28	0007 3C02 2BF0h
BF4h	32	CTSET2_CFG_CTCNTR29	0007 3C02 2BF4h
BF8h	32	CTSET2_CFG_CTCNTR30	0007 3C02 2BF8h
BFCh	32	CTSET2_CFG_CTCNTR31	0007 3C02 2BFCh
C00h	32	CTSET2_CFG_CT_EOI	0007 3C02 2C00h
C04h	32	CTSET2_CFG_CTIRQSTAT_RAW	0007 3C02 2C04h
C08h	32	CTSET2_CFG_CTIRQSTAT	0007 3C02 2C08h

Table 14-32726. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
C0Ch	32	CTSET2_CFG_CTIRQENABLE_SET	0007 3C02 2C0Ch
C10h	32	CTSET2_CFG_CTIRQENABLE_CLR	0007 3C02 2C10h
1800h	32	CTSET2_CFG_STPTCR	0007 3C02 3800h
1804h	32	CTSET2_CFG_STPTID	0007 3C02 3804h
1810h	32	CTSET2_CFG_STPASYNC	0007 3C02 3810h
1814h	32	CTSET2_CFG_STPFFCR	0007 3C02 3814h
1818h	32	CTSET2_CFG_STPFEAT1	0007 3C02 3818h

Table 14-32727. CXATBREPLICATOR_CFG Registers, Base Address=0007 3C02 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CXATBREPLICATOR_CFG_IDFILTER0	0007 3C02 4000h
4h	32	CXATBREPLICATOR_CFG_IDFILTER1	0007 3C02 4004h
EF8h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR1	0007 3C02 4EF8h
EFCh	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR0	0007 3C02 4EFCh
F00h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITCTRL	0007 3C02 4F00h
FA0h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMSET	0007 3C02 4FA0h
FA4h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMCLR	0007 3C02 4FA4h
FB0h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LAR	0007 3C02 4FB0h
FB4h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LSR	0007 3C02 4FB4h
FB8h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_AUTHSTATUS	0007 3C02 4FB8h
FC8h	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVID	0007 3C02 4FC8h
FCCh	32	CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVTYPE	0007 3C02 4FCCh
FD0h	32	CXATBREPLICATOR_CFG_PIDR4	0007 3C02 4FD0h
FE0h	32	CXATBREPLICATOR_CFG_PIDR0	0007 3C02 4FE0h
FE4h	32	CXATBREPLICATOR_CFG_PIDR1	0007 3C02 4FE4h
FE8h	32	CXATBREPLICATOR_CFG_PIDR2	0007 3C02 4FE8h
FECh	32	CXATBREPLICATOR_CFG_PIDR3	0007 3C02 4FECh
FF0h	32	CXATBREPLICATOR_CFG_CIDR0	0007 3C02 4FF0h
FF4h	32	CXATBREPLICATOR_CFG_CIDR1	0007 3C02 4FF4h
FF8h	32	CXATBREPLICATOR_CFG_CIDR2	0007 3C02 4FF8h
FFCh	32	CXATBREPLICATOR_CFG_CIDR3	0007 3C02 4FFCh

Table 14-32728. CT_TBR Registers, Base Address=0007 3C02 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
4h	32	CT_TBR_CT_TBR_RAMSZ	0007 3C02 5004h
8h	32	CT_TBR_CT_TBR_FIFOSZ	0007 3C02 5008h
Ch	32	CT_TBR_CT_TBR_STAT	0007 3C02 500Ch

Table 14-32728. CT_TBR Registers, Base Address=0007 3C02 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
10h	32	CT_TBR_CT_TBR_RAMRDAT	0007 3C02 5010h
14h	32	CT_TBR_CT_TBR_RAMRPTR	0007 3C02 5014h
18h	32	CT_TBR_CT_TBR_RAMWPTR	0007 3C02 5018h
1Ch	32	CT_TBR_CT_TBR_TRGCNT	0007 3C02 501Ch
20h	32	CT_TBR_CT_TBR_CTRL	0007 3C02 5020h
24h	32	CT_TBR_CT_TBR_RAMWDAT	0007 3C02 5024h
100h	32	CT_TBR_CT_TBR_OUTLVL	0007 3C02 5100h
104h	32	CT_TBR_CT_TBR_SICTRL	0007 3C02 5104h
108h	32	CT_TBR_CT_TBR_IDPERIOD	0007 3C02 5108h
10Ch	32	CT_TBR_CT_TBR_SEQCNTL	0007 3C02 510Ch
120h	32	CT_TBR_CT_TBR_EOI	0007 3C02 5120h
124h	32	CT_TBR_CT_TBR_IRQSTATUS_RAW	0007 3C02 5124h
128h	32	CT_TBR_CT_TBR_IRQSTATUS	0007 3C02 5128h
12Ch	32	CT_TBR_CT_TBR_IRQENABLE_SET	0007 3C02 512Ch
130h	32	CT_TBR_CT_TBR_IRQENABLE_CLR	0007 3C02 5130h
300h	32	CT_TBR_CT_TBR_OPSTAT	0007 3C02 5300h
304h	32	CT_TBR_CT_TBR_OPCTRL	0007 3C02 5304h
FA0h	32	CT_TBR_CLAIMSET	0007 3C02 5FA0h
FA4h	32	CT_TBR_CLAIMCLR	0007 3C02 5FA4h
FB0h	32	CT_TBR_LOCKACC	0007 3C02 5FB0h
FB4h	32	CT_TBR_LOCKSTAT	0007 3C02 5FB4h
FB8h	32	CT_TBR_AUTHSTAT	0007 3C02 5FB8h
FC8h	32	CT_TBR_DEVID	0007 3C02 5FC8h
FCCh	32	CT_TBR_DEVTYPE	0007 3C02 5FCCh
FD0h	32	CT_TBR_PERIPHID4	0007 3C02 5FD0h
FD4h	32	CT_TBR_PERIPHID5	0007 3C02 5FD4h
FD8h	32	CT_TBR_PERIPHID6	0007 3C02 5FD8h
FDCh	32	CT_TBR_PERIPHID7	0007 3C02 5FDCh
FE0h	32	CT_TBR_PERIPHID0	0007 3C02 5FE0h
FE4h	32	CT_TBR_PERIPHID1	0007 3C02 5FE4h
FE8h	32	CT_TBR_PERIPHID2	0007 3C02 5FE8h
FECh	32	CT_TBR_PERIPHID3	0007 3C02 5FECh
FF0h	32	CT_TBR_COMPID0	0007 3C02 5FF0h
FF4h	32	CT_TBR_COMPID1	0007 3C02 5FF4h
FF8h	32	CT_TBR_COMPID2	0007 3C02 5FF8h
FFCh	32	CT_TBR_COMPID3	0007 3C02 5FFCh

Table 14-32729. CSCTI_CFG Registers, Base Address=0007 3C02 6000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 6000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 6010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 6014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 6018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 601Ch

Table 14-32729. CSCTI_CFG Registers, Base Address=0007 3C02 6000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 6020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 6024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 6028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 602Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 6030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 6034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 6038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 603Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 60A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 60A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 60A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 60ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 60B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 60B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 60B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 60BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 6130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 6134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 6138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 613Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 6140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 6144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 6EDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 6EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 6EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 6EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 6EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 6EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 6EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 6EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 6F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 6FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 6FA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 6FB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 6FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 6FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 6FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 6FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 6FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 6FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 6FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 6FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 6FECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 6FF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 6FF4h

Table 14-32729. CSCTI_CFG Registers, Base Address=0007 3C02 6000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 6FF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 6FFCh

Table 14-32730. CSCTI_CFG Registers, Base Address=0007 3C02 8000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 8000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 8010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 8014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 8018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 801Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 8020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 8024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 8028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 802Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 8030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 8034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 8038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 803Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 80A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 80A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 80A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 80ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 80B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 80B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 80B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 80BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 8130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 8134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 8138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 813Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 8140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 8144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 8EDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 8EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 8EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 8EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 8EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 8EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 8EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 8EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 8F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 8FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 8FA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 8FB0h

Table 14-32730. CSCTI_CFG Registers, Base Address=0007 3C02 8000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 8FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 8FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 8FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 8FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 8FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 8FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 8FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 8FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 8FECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 8FF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 8FF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 8FF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 8FFCh

Table 14-32731. CSCTI_CFG Registers, Base Address=0007 3C02 9000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 9000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 9010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 9014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 9018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 901Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 9020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 9024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 9028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 902Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 9030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 9034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 9038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 903Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 90A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 90A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 90A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 90ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 90B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 90B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 90B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 90BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 9130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 9134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 9138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 913Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 9140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 9144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 9EDCh

Table 14-32731. CSCTI_CFG Registers, Base Address=0007 3C02 9000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 9EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 9EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 9EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 9EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 9EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 9EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 9EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 9F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 9FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 9FA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 9FB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 9FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 9FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 9FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 9FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 9FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 9FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 9FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 9FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 9FECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 9FF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 9FF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 9FF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 9FFCh

Table 14-32732. CSCTI_CFG Registers, Base Address=0007 3C02 A000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 A000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 A010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 A014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 A018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 A01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 A020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 A024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 A028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 A02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 A030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 A034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 A038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 A03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 A0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 A0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 A0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 A0ACh

Table 14-32732. CSCTI_CFG Registers, Base Address=0007 3C02 A000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 A0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 A0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 A0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 A0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 A130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 A134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 A138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 A13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 A140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 A144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 AEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 AEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 AEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 AEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 AEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 AEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 AEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 AEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 AF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 AFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 AFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 AFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 AFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 AFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 AFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 AFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 AFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 AFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 AFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 AFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 AFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 AFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 AFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 AFF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 AFFCh

Table 14-32733. CSCTI_CFG Registers, Base Address=0007 3C02 B000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 B000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 B010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 B014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 B018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 B01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 B020h

Table 14-32733. CSCTI_CFG Registers, Base Address=0007 3C02 B000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 B024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 B028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 B02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 B030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 B034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 B038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 B03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 B0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 B0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 B0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 B0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 B0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 B0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 B0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 B0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 B130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 B134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 B138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 B13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 B140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 B144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 BEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 BEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 BEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 BEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 BEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 BEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 BEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 BEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 BF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 BFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 BFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 BFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 BFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 BFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 BFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 BFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 BFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 BFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 BFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 BFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 BFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 BFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 BFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 BFF8h

Table 14-32733. CSCTI_CFG Registers, Base Address=0007 3C02 B000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 BFFCh

Table 14-32734. CSCTI_CFG Registers, Base Address=0007 3C02 C000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 C000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 C010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 C014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 C018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 C01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 C020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 C024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 C028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 C02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 C030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 C034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 C038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 C03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 C0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 C0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 C0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 C0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 C0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 C0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 C0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 C0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 C130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 C134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 C138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 C13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 C140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 C144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 CEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 CEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 CEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 CEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 CEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 CEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 CEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 CEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 CF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 CFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 CFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 CFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 CFB4h

Table 14-32734. CSCTI_CFG Registers, Base Address=0007 3C02 C000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 CFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 CFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 CFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 CFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 CFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 CFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 CFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 CFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 CFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 CFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 CFF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 CFFCh

Table 14-32735. CSCTI_CFG Registers, Base Address=0007 3C02 D000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 D000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 D010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 D014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 D018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 D01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 D020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 D024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 D028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 D02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 D030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 D034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 D038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 D03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 D0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 D0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 D0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 D0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 D0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 D0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 D0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 D0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 D130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 D134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 D138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 D13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 D140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 D144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 DEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 DEE0h

Table 14-32735. CSCTI_CFG Registers, Base Address=0007 3C02 D000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 DEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 DEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 DEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 DEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 DEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 DEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 DF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 DFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 DFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 DFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 DFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 DFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 DFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 DFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 DFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 DFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 DFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 DFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 DFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 DFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 DFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 DFF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 DFFCh

Table 14-32736. CSCTI_CFG Registers, Base Address=0007 3C02 E000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 E000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 E010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 E014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 E018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 E01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 E020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 E024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 E028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 E02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 E030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 E034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 E038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 E03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 E0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 E0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 E0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 E0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 E0B0h

Table 14-32736. CSCTI_CFG Registers, Base Address=0007 3C02 E000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 E0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 E0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 E0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 E130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 E134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 E138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 E13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 E140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 E144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 EEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 EEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 EEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 EEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 EEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 EEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 EEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 EEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 EF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 EFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 EFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 EFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 EFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 EFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 EFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 EFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 EFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 EFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 EFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 EFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 EFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 EFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 EFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 EFF8h
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 EFFCh

Table 14-32737. CSCTI_CFG Registers, Base Address=0007 3C02 F000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 F000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 F010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 F014h
18h	32	CSCTI_CFG_CTIAPPCLR	0007 3C02 F018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 F01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 F020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 F024h

Table 14-32737. CSCTI_CFG Registers, Base Address=0007 3C02 F000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 F028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 F02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 F030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 F034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 F038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 F03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 F0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 F0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 F0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 F0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 F0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 F0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 F0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 F0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 F130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 F134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 F138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 F13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 F140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 F144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 FEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 FEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 FEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 FEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 FEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 FEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 FEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 FEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 FF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 FFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 FFA4h
FB0h	32	CSCTI_CFG_LOCKACCESS	0007 3C02 FFB0h
FB4h	32	CSCTI_CFG_LOCKSTATUS	0007 3C02 FFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 FFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 FFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 FFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 FFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 FFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 FFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 FFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 FFECh
FF0h	32	CSCTI_CFG_COMPONID0	0007 3C02 FFF0h
FF4h	32	CSCTI_CFG_COMPONID1	0007 3C02 FFF4h
FF8h	32	CSCTI_CFG_COMPONID2	0007 3C02 FFF8h

Table 14-32737. CSCTI_CFG Registers, Base Address=0007 3C02 F000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FFCh	32	CSCTI_CFG_COMPONID3	0007 3C02 FFFCh

14.10.1.2 debugss Registers

debugss Registers

14.10.1.2.1 DEBUGSS_SYS_TRACE Register

1 DEBUGSS_SYS_TRACE Register (Offset = 0h) [reset = 0h]

This register contains TBR trace read data

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Table 14-32738. Instance Table

Instance Name	Physical Address
DEBUGSS0	**4100 0000h**

Figure 14-10834. DEBUGSS_SYS_TRACE Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-32740. DEBUGSS_SYS_TRACE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	TBR TRACE data

14.10.1.2.2 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register (Offset = 4h) [reset = 2002h]

rom table entry 1

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Table 14-32741. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0004h**

Figure 14-10835. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Name Register

31	30	29	28	27	26	25	24
ID							
R							
1001h							
23	22	21	20	19	18	17	16
ID							
R							
1001h							
15	14	13	12	11	10	9	8
ID							
R							
1001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
1001h							0h

Table 14-32743. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	1001h	4kB - MSMCv3 CSCTI Instance 1 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.3 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register (Offset = 8h) [reset = 4002h]

rom table entry 2

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Table 14-32744. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0008h**

Figure 14-10836. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Name Register

31	30	29	28	27	26	25	24
ID							
R							
2001h							
23	22	21	20	19	18	17	16
ID							
R							
2001h							
15	14	13	12	11	10	9	8
ID							
R							
2001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
2001h							0h

Table 14-32746. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	2001h	4kB - MSMCv3 CSCTI Instance 2 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.4 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register (Offset = Ch) [reset = 5002h]

rom table entry 3

Return to Summary Table

Table 14-32747. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 000Ch**

Figure 14-10837. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
2801h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
2801h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
2801h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
2801h							0h

Table 14-32749. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	2801h	4kB - MSMCv3 CSCTI Instance 3 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.5 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register (Offset = 10h) [reset = 6002h]

rom table entry 4

Return to Summary Table

Table 14-32750. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0010h**

Figure 14-10838. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Name Register

31	30	29	28	27	26	25	24
ID							
R							
3001h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
3001h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
3001h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
3001h							0h

Table 14-32752. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	3001h	4kB - MSMCv3 CSCTI Instance 4 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.6 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register (Offset = 14h) [reset = 7002h]

rom table entry 5

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Table 14-32753. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0014h**

Figure 14-10839. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Name Register

31	30	29	28	27	26	25	24
ID							
R							
3801h							
23	22	21	20	19	18	17	16
ID							
R							
3801h							
15	14	13	12	11	10	9	8
ID							
R							
3801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
3801h							0h

Table 14-32755. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	3801h	4kB - MSMCv3 CSCTI Instance 5 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.7 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register (Offset = 18h) [reset = 8002h]

rom table entry 6

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Table 14-32756. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0018h**

Figure 14-10840. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Name Register

31	30	29	28	27	26	25	24
ID							
R							
4001h							
23	22	21	20	19	18	17	16
ID							
R							
4001h							
15	14	13	12	11	10	9	8
ID							
R							
4001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
4001h							0h

Table 14-32758. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	4001h	4kB - MSMCv3 CSCTI Instance 6 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.8 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register (Offset = 1Ch) [reset = 9002h]

rom table entry 7

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Table 14-32759. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 001Ch**

Figure 14-10841. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Name Register

31	30	29	28	27	26	25	24
ID							
R							
4801h							
23	22	21	20	19	18	17	16
ID							
R							
4801h							
15	14	13	12	11	10	9	8
ID							
R							
4801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
4801h							0h

Table 14-32761. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	4801h	4kB - MSMCv3 CSCTI Instance 7 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.9 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register (Offset = 20h) [reset = A002h]

rom table entry 8

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Table 14-32762. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0020h**

Figure 14-10842. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Name Register

31	30	29	28	27	26	25	24
ID							
R							
5001h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
5001h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
5001h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
5001h							0h

Table 14-32764. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	5001h	256kB - Processor Cluster Instance 0 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.10 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register (Offset = 24h) [reset = B002h]

rom table entry 9

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Table 14-32765. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0024h**

Figure 14-10843. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Name Register

31	30	29	28	27	26	25	24
ID							
R							
5801h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
5801h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
5801h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
5801h							0h

Table 14-32767. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	5801h	256kB - Processor Cluster Instance 1 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.11 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register (Offset = 28h) [reset = C002h]

rom table entry 10

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Table 14-32768. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0028h**

Figure 14-10844. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Name Register

31	30	29	28	27	26	25	24
ID							
R							
6001h							
23	22	21	20	19	18	17	16
ID							
R							
6001h							
15	14	13	12	11	10	9	8
ID							
R							
6001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
6001h							0h

Table 14-32770. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	6001h	256kB - Processor Cluster Instance 2 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.12 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register (Offset = 2Ch) [reset = D002h]

rom table entry 11

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Table 14-32771. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 002Ch**

Figure 14-10845. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Name Register

31	30	29	28	27	26	25	24
ID							
R							
6801h							
23	22	21	20	19	18	17	16
ID							
R							
6801h							
15	14	13	12	11	10	9	8
ID							
R							
6801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
6801h							0h

Table 14-32773. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	6801h	256kB - Processor Cluster Instance 3 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.13 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register (Offset = 30h) [reset = E002h]

rom table entry 12

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Table 14-32774. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0030h**

Figure 14-10846. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7001h							
23	22	21	20	19	18	17	16
ID							
R							
7001h							
15	14	13	12	11	10	9	8
ID							
R							
7001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
7001h							0h

Table 14-32776. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	7001h	256kB - Processor Cluster Instance 4 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.14 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register (Offset = 34h) [reset = F002h]

rom table entry 13

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Table 14-32777. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0034h**

Figure 14-10847. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7801h							
23	22	21	20	19	18	17	16
ID							
R							
7801h							
15	14	13	12	11	10	9	8
ID							
R							
7801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
7801h							0h

Table 14-32779. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	7801h	256kB - Processor Cluster Instance 5 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.15 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register (Offset = 50h) [reset = 0h]

rom table entry 20

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Table 14-32780. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0050h**

Figure 14-10848. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-32782. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	End of table Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.16 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral Identification Register Number 4

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Table 14-32783. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD0h**

Figure 14-10849. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32785. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.17 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register Number 5

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Table 14-32786. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD4h**

Figure 14-10850. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-32788. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.18 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register Number 6

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Table 14-32789. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD8h**

Figure 14-10851. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							
R							
0h							

Table 14-32791. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.19 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register Number 7

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Table 14-32792. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FDCh**

Figure 14-10852. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-32794. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.20 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register (Offset = FE0h) [reset = D1h]

Peripheral Identification Register Number 0

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Table 14-32795. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE0h**

Figure 14-10853. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
ID							
R							
D1h							
23	22	21	20	19	18	17	16
ID							
R							
D1h							
15	14	13	12	11	10	9	8
ID							
R							
D1h							
7	6	5	4	3	2	1	0
ID							
R							
D1h							

Table 14-32797. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	D1h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.21 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register (Offset = FE4h) [reset = 7Eh]

Peripheral Identification Register Number 1

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Table 14-32798. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE4h**

Figure 14-10854. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7Eh							
23	22	21	20	19	18	17	16
ID							
R							
7Eh							
15	14	13	12	11	10	9	8
ID							
R							
7Eh							
7	6	5	4	3	2	1	0
ID							
R							
7Eh							

Table 14-32800. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	7Eh	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.22 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register (Offset = FE8h) [reset = 9h]

Peripheral Identification Register Number 2

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Table 14-32801. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE8h**

Figure 14-10855. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
ID							
R							
9h							
23	22	21	20	19	18	17	16
ID							
R							
9h							
15	14	13	12	11	10	9	8
ID							
R							
9h							
7	6	5	4	3	2	1	0
ID							
R							
9h							

Table 14-32803. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	9h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.23 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register Number 3

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Table 14-32804. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FECh**

Figure 14-10856. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-32806. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.24 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register Number 0

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Table 14-32807. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FF0h**

Figure 14-10857. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Name Register

31	30	29	28	27	26	25	24
ID							
R							
Dh							
23	22	21	20	19	18	17	16
ID							
R							
Dh							
15	14	13	12	11	10	9	8
ID							
R							
Dh							
7	6	5	4	3	2	1	0
ID							
R							
Dh							

Table 14-32809. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	Dh	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.25 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register (Offset = FF4h) [reset = 10h]

Component Identification Register Number 1

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Table 14-32810. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FF4h**

Figure 14-10858. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Name Register

31	30	29	28	27	26	25	24
ID							
R							
10h							
23	22	21	20	19	18	17	16
ID							
R							
10h							
15	14	13	12	11	10	9	8
ID							
R							
10h							
7	6	5	4	3	2	1	0
ID							
R							
10h							

Table 14-32812. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	10h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.26 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register Number 2

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Table 14-32813. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FF8h**

Figure 14-10859. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Name Register

31	30	29	28	27	26	25	24
ID							
R							
5h							
23	22	21	20	19	18	17	16
ID							
R							
5h							
15	14	13	12	11	10	9	8
ID							
R							
5h							
7	6	5	4	3	2	1	0
ID							
R							
5h							

Table 14-32815. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	5h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.27 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register Number 3

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Table 14-32816. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FFCh**

Figure 14-10860. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
B1h							
23	22	21	20	19	18	17	16
ID							
R							
B1h							
15	14	13	12	11	10	9	8
ID							
R							
B1h							
7	6	5	4	3	2	1	0
ID							
R							
B1h							

Table 14-32818. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	B1h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.10.1.2.28 CTSET2_CFG_CTSETID Register

1 CTSET2_CFG_CTSETID Register (Offset = 0h) [reset = 62800200h]

CTSET identification register

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Table 14-32819. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2000h**

Figure 14-10861. CTSET2_CFG_CTSETID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		280h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
280h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REV		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-32821. CTSET2_CFG_CTSETID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old Scheme and current
29:28	BU	R	2h	The value 10b designates this as Processor Business Unit IP
27:16	FUNCTION	R	280h	Function : Indicates a Debug IP (0x2nn) and 0x80 is the identifier for CT-SET
15:11	RTL_VERSION	R	0h	This field changes on bug fix, and resets to '0' when either Minor Revision or Major Revision field changes
10:8	MAJOR_REV	R	2h	Major Revision. This field changes when there is a major feature change.
7:6	CUSTOM	R	0h	Indicates a special version for a particular device. 0 if non-custom
5:0	MINOR_REV	R	0h	Minor Revision. This field changes when features are scaled up or down

14.10.1.2.29 CTSET2_CFG_CTSETSYSCFG Register

1 CTSET2_CFG_CTSETSYSCFG Register (Offset = 10h) [reset = 8h]

CTSET system configuration register

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Table 14-32822. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2010h**

Figure 14-10862. CTSET2_CFG_CTSETSYSCFG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				IDLEMODE		RESERVED	SOFTRESET
R				R/W		R	R/W
0h				2h		0h	0h

Table 14-32824. CTSET2_CFG_CTSETSYSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED1	R	0h	Reserved, returns 0
3:2	IDLEMODE	R/W	2h	Sets the Idle Mode for CTSET (0=Force Idle, 1=No Idle, 2=Smart Idle, 3= Smart Idle wakeup)
1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	This will reset entire CTSET, except the registers and the CFG interface. This bit is automatically cleared by hardware. Reads always return 0

14.10.1.2.30 CTSET2_CFG_SETSTR Register

1 CTSET2_CFG_SETSTR Register (Offset = 14h) [reset = 101h]

CTSET status register

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Table 14-32825. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2014h**

Figure 14-10863. CTSET2_CFG_SETSTR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							HWFIFOEMPTY
R							R
0h							1h
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							1h

Table 14-32827. CTSET2_CFG_SETSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8	HWFIFOEMPTY	R	1h	System Event Trace FIFO status, 1 is empty, 0 means captured data not yet exported
7:1	RESERVED	R	0h	Reserved, returns 0
0	RESETDONE	R	1h	Reset status, 0 means reset ongoing, 1 indicates completed

14.10.1.2.31 CTSET2_CFG_DBGTIMELOW Register

1 CTSET2_CFG_DBGTIMELOW Register (Offset = 18h) [reset = 0h]

The 32 low order bits of the debug time value supplied on the time input interface

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Table 14-32828. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2018h**

Figure 14-10864. CTSET2_CFG_DBGTIMELOW Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-32830. CTSET2_CFG_DBGTIMELOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.10.1.2.32 CTSET2_CFG_DBGTIMEHI Register

1 CTSET2_CFG_DBGTIMEHI Register (Offset = 1Ch) [reset = 0h]

The 32 high order bits of the debug time value supplied on the time input interface

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Table 14-32831. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 201Ch**

Figure 14-10865. CTSET2_CFG_DBGTIMEHI Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-32833. CTSET2_CFG_DBGTIMEHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.10.1.2.33 CTSET2_CFG_CTSETCFG Register

1 CTSET2_CFG_CTSETCFG Register (Offset = 24h) [reset = 20000010h]

The 32 low order bits of the debug time value supplied on the time input interface The 32 high order bits of the debug time value supplied on the time input interface. Reading DBGTIMEHI latches the lower 32 bits of debug time value CTSET configuration register

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Table 14-32834. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2024h**

Figure 14-10866. CTSET2_CFG_CTSETCFG Name Register

31	30	29	28	27	26	25	24
CLAIM				RESERVED2			
R/W				R			
2h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYSEVENTCAPTEN	RESERVED1		EVENTLEVEL	MSGMODE	STOPCAPT	STARTCAPT	RESERVED
R/W	R		R/W	R/W	R/W	R/W	R
0h	0h		1h	0h	0h	0h	0h

Table 14-32836. CTSET2_CFG_CTSETCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CLAIM	R/W	2h	Claim control and status. To program any bits other than 31 : 28, CTSET ownership must be claimed using bits 31 : 28.
27:8	RESERVED2	R	0h	Reserved, returns 0
7	SYSEVENTCAPTEN	R/W	0h	When 1 the System event capture is enabled
6:5	RESERVED1	R	0h	Reserved, returns 0
4	EVENTLEVEL	R/W	1h	0 enables low level event detection, 1 enables high level event detection
3	MSGMODE	R/W	0h	Message generated based on event detection, 0 is sampling window, 1 is event detection
2	STOPCAPT	R/W	0h	Stop capturing system events from external trigger detection
1	STARTCAPT	R/W	0h	Start capturing system events from external trigger detection
0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.34 CTSET2_CFG_SETSPLREG Register

1 CTSET2_CFG_SETSPLREG Register (Offset = 28h) [reset = 0h]

System Event Sampling Window register

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Table 14-32837. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2028h**

Figure 14-10867. CTSET2_CFG_SETSPLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
WINDOWSIZE							
R/W							
0h							

Table 14-32839. CTSET2_CFG_SETSPLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	WINDOWSIZE	R/W	0h	System events sampling window size expressed as CTSET cycles

14.10.1.2.35 CTSET2_CFG_SETEVTENBL1 Register

1 CTSET2_CFG_SETEVTENBL1 Register (Offset = 30h) [reset = 0h]

System event detection enable register 1

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Table 14-32840. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2030h**

Figure 14-10868. CTSET2_CFG_SETEVTENBL1 Name Register

31	30	29	28	27	26	25	24
EVENT32DETEN	EVENT31DETEN	EVENT30DETEN	EVENT29DETEN	EVENT28DETEN	EVENT27DETEN	EVENT26DETEN	EVENT25DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT24DETEN	EVENT23DETEN	EVENT22DETEN	EVENT21DETEN	EVENT20DETEN	EVENT19DETEN	EVENT18DETEN	EVENT17DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT16DETEN	EVENT15DETEN	EVENT14DETEN	EVENT13DETEN	EVENT12DETEN	EVENT11DETEN	EVENT10DETEN	EVENT9DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT8DETEN	EVENT7DETEN	EVENT6DETEN	EVENT5DETEN	EVENT4DETEN	EVENT3DETEN	EVENT2DETEN	EVENT1DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32842. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT32DETEN	R/W	0h	Event(32) Detection Enable
30	EVENT31DETEN	R/W	0h	Event(31) Detection Enable
29	EVENT30DETEN	R/W	0h	Event(30) Detection Enable
28	EVENT29DETEN	R/W	0h	Event(29) Detection Enable
27	EVENT28DETEN	R/W	0h	Event(28) Detection Enable
26	EVENT27DETEN	R/W	0h	Event(27) Detection Enable
25	EVENT26DETEN	R/W	0h	Event(26) Detection Enable
24	EVENT25DETEN	R/W	0h	Event(25) Detection Enable
23	EVENT24DETEN	R/W	0h	Event(24) Detection Enable
22	EVENT23DETEN	R/W	0h	Event(23) Detection Enable
21	EVENT22DETEN	R/W	0h	Event(22) Detection Enable
20	EVENT21DETEN	R/W	0h	Event(21) Detection Enable
19	EVENT20DETEN	R/W	0h	Event(20) Detection Enable
18	EVENT19DETEN	R/W	0h	Event(19) Detection Enable
17	EVENT18DETEN	R/W	0h	Event(18) Detection Enable

Table 14-32842. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT17DETEN	R/W	0h	Event(17) Detection Enable
15	EVENT16DETEN	R/W	0h	Event(16) Detection Enable
14	EVENT15DETEN	R/W	0h	Event(15) Detection Enable
13	EVENT14DETEN	R/W	0h	Event(14) Detection Enable
12	EVENT13DETEN	R/W	0h	Event(13) Detection Enable
11	EVENT12DETEN	R/W	0h	Event(12) Detection Enable
10	EVENT11DETEN	R/W	0h	Event(11) Detection Enable
9	EVENT10DETEN	R/W	0h	Event(10) Detection Enable
8	EVENT9DETEN	R/W	0h	Event(9) Detection Enable
7	EVENT8DETEN	R/W	0h	Event(8) Detection Enable
6	EVENT7DETEN	R/W	0h	Event(7) Detection Enable
5	EVENT6DETEN	R/W	0h	Event(6) Detection Enable
4	EVENT5DETEN	R/W	0h	Event(5) Detection Enable
3	EVENT4DETEN	R/W	0h	Event(4) Detection Enable
2	EVENT3DETEN	R/W	0h	Event(3) Detection Enable
1	EVENT2DETEN	R/W	0h	Event(2) Detection Enable
0	EVENT1DETEN	R/W	0h	Event(1) Detection Enable

14.10.1.2.36 CTSET2_CFG_SETEVTENBL2 Register

1 CTSET2_CFG_SETEVTENBL2 Register (Offset = 34h) [reset = 0h]

System event detection enable register 2 (if number of events > 32)

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Table 14-32843. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2034h**

Figure 14-10869. CTSET2_CFG_SETEVTENBL2 Name Register

31	30	29	28	27	26	25	24
EVENT64DETEN	EVENT63DETEN	EVENT62DETEN	EVENT61DETEN	EVENT60DETEN	EVENT59DETEN	EVENT58DETEN	EVENT57DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT56DETEN	EVENT55DETEN	EVENT54DETEN	EVENT53DETEN	EVENT52DETEN	EVENT51DETEN	EVENT50DETEN	EVENT49DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT48DETEN	EVENT47DETEN	EVENT46DETEN	EVENT45DETEN	EVENT44DETEN	EVENT43DETEN	EVENT42DETEN	EVENT41DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT40DETEN	EVENT39DETEN	EVENT38DETEN	EVENT37DETEN	EVENT36DETEN	EVENT35DETEN	EVENT34DETEN	EVENT33DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32845. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT64DETEN	R/W	0h	Event(64) Detection Enable
30	EVENT63DETEN	R/W	0h	Event(63) Detection Enable
29	EVENT62DETEN	R/W	0h	Event(62) Detection Enable
28	EVENT61DETEN	R/W	0h	Event(61) Detection Enable
27	EVENT60DETEN	R/W	0h	Event(60) Detection Enable
26	EVENT59DETEN	R/W	0h	Event(59) Detection Enable
25	EVENT58DETEN	R/W	0h	Event(58) Detection Enable
24	EVENT57DETEN	R/W	0h	Event(57) Detection Enable
23	EVENT56DETEN	R/W	0h	Event(56) Detection Enable
22	EVENT55DETEN	R/W	0h	Event(55) Detection Enable
21	EVENT54DETEN	R/W	0h	Event(54) Detection Enable
20	EVENT53DETEN	R/W	0h	Event(53) Detection Enable
19	EVENT52DETEN	R/W	0h	Event(52) Detection Enable
18	EVENT51DETEN	R/W	0h	Event(51) Detection Enable
17	EVENT50DETEN	R/W	0h	Event(50) Detection Enable

Table 14-32845. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT49DETEN	R/W	0h	Event(49) Detection Enable
15	EVENT48DETEN	R/W	0h	Event(48) Detection Enable
14	EVENT47DETEN	R/W	0h	Event(47) Detection Enable
13	EVENT46DETEN	R/W	0h	Event(46) Detection Enable
12	EVENT45DETEN	R/W	0h	Event(45) Detection Enable
11	EVENT44DETEN	R/W	0h	Event(44) Detection Enable
10	EVENT43DETEN	R/W	0h	Event(43) Detection Enable
9	EVENT42DETEN	R/W	0h	Event(42) Detection Enable
8	EVENT41DETEN	R/W	0h	Event(41) Detection Enable
7	EVENT40DETEN	R/W	0h	Event(40) Detection Enable
6	EVENT39DETEN	R/W	0h	Event(39) Detection Enable
5	EVENT38DETEN	R/W	0h	Event(38) Detection Enable
4	EVENT37DETEN	R/W	0h	Event(37) Detection Enable
3	EVENT36DETEN	R/W	0h	Event(36) Detection Enable
2	EVENT35DETEN	R/W	0h	Event(35) Detection Enable
1	EVENT34DETEN	R/W	0h	Event(34) Detection Enable
0	EVENT33DETEN	R/W	0h	Event(33) Detection Enable

14.10.1.2.37 CTSET2_CFG_SETEVTENBL3 Register

1 CTSET2_CFG_SETEVTENBL3 Register (Offset = 38h) [reset = 0h]

System event detection enable register 3 (if number of events > 64)

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Table 14-32846. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2038h**

Figure 14-10870. CTSET2_CFG_SETEVTENBL3 Name Register

31	30	29	28	27	26	25	24
EVENT96DETEN	EVENT95DETEN	EVENT94DETEN	EVENT93DETEN	EVENT92DETEN	EVENT91DETEN	EVENT90DETEN	EVENT89DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT88DETEN	EVENT87DETEN	EVENT86DETEN	EVENT85DETEN	EVENT84DETEN	EVENT83DETEN	EVENT82DETEN	EVENT81DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT80DETEN	EVENT79DETEN	EVENT78DETEN	EVENT77DETEN	EVENT76DETEN	EVENT75DETEN	EVENT74DETEN	EVENT73DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT72DETEN	EVENT71DETEN	EVENT70DETEN	EVENT69DETEN	EVENT68DETEN	EVENT67DETEN	EVENT66DETEN	EVENT65DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32848. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT96DETEN	R/W	0h	Event(96) Detection Enable
30	EVENT95DETEN	R/W	0h	Event(95) Detection Enable
29	EVENT94DETEN	R/W	0h	Event(94) Detection Enable
28	EVENT93DETEN	R/W	0h	Event(93) Detection Enable
27	EVENT92DETEN	R/W	0h	Event(92) Detection Enable
26	EVENT91DETEN	R/W	0h	Event(91) Detection Enable
25	EVENT90DETEN	R/W	0h	Event(90) Detection Enable
24	EVENT89DETEN	R/W	0h	Event(89) Detection Enable
23	EVENT88DETEN	R/W	0h	Event(88) Detection Enable
22	EVENT87DETEN	R/W	0h	Event(87) Detection Enable
21	EVENT86DETEN	R/W	0h	Event(86) Detection Enable
20	EVENT85DETEN	R/W	0h	Event(85) Detection Enable
19	EVENT84DETEN	R/W	0h	Event(84) Detection Enable
18	EVENT83DETEN	R/W	0h	Event(83) Detection Enable
17	EVENT82DETEN	R/W	0h	Event(82) Detection Enable

Table 14-32848. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT81DETEN	R/W	0h	Event(81) Detection Enable
15	EVENT80DETEN	R/W	0h	Event(80) Detection Enable
14	EVENT79DETEN	R/W	0h	Event(79) Detection Enable
13	EVENT78DETEN	R/W	0h	Event(78) Detection Enable
12	EVENT77DETEN	R/W	0h	Event(77) Detection Enable
11	EVENT76DETEN	R/W	0h	Event(76) Detection Enable
10	EVENT75DETEN	R/W	0h	Event(75) Detection Enable
9	EVENT74DETEN	R/W	0h	Event(74) Detection Enable
8	EVENT73DETEN	R/W	0h	Event(73) Detection Enable
7	EVENT72DETEN	R/W	0h	Event(72) Detection Enable
6	EVENT71DETEN	R/W	0h	Event(71) Detection Enable
5	EVENT70DETEN	R/W	0h	Event(70) Detection Enable
4	EVENT69DETEN	R/W	0h	Event(69) Detection Enable
3	EVENT68DETEN	R/W	0h	Event(68) Detection Enable
2	EVENT67DETEN	R/W	0h	Event(67) Detection Enable
1	EVENT66DETEN	R/W	0h	Event(66) Detection Enable
0	EVENT65DETEN	R/W	0h	Event(65) Detection Enable

14.10.1.2.38 CTSET2_CFG_SETEVTENBL4 Register

1 CTSET2_CFG_SETEVTENBL4 Register (Offset = 3Ch) [reset = 0h]

System event detection enable register 4 (if number of events > 96)

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Table 14-32849. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 203Ch**

Figure 14-10871. CTSET2_CFG_SETEVTENBL4 Name Register

31	30	29	28	27	26	25	24
EVENT128DETEN	EVENT127DETEN	EVENT126DETEN	EVENT125DETEN	EVENT124DETEN	EVENT123DETEN	EVENT122DETEN	EVENT121DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT120DETEN	EVENT119DETEN	EVENT118DETEN	EVENT117DETEN	EVENT116DETEN	EVENT115DETEN	EVENT114DETEN	EVENT113DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT112DETEN	EVENT111DETEN	EVENT110DETEN	EVENT109DETEN	EVENT108DETEN	EVENT107DETEN	EVENT106DETEN	EVENT105DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT104DETEN	EVENT103DETEN	EVENT102DETEN	EVENT101DETEN	EVENT100DETEN	EVENT99DETEN	EVENT98DETEN	EVENT97DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32851. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT128DETEN	R/W	0h	Event(128) Detection Enable
30	EVENT127DETEN	R/W	0h	Event(127) Detection Enable
29	EVENT126DETEN	R/W	0h	Event(126) Detection Enable
28	EVENT125DETEN	R/W	0h	Event(125) Detection Enable
27	EVENT124DETEN	R/W	0h	Event(124) Detection Enable
26	EVENT123DETEN	R/W	0h	Event(123) Detection Enable
25	EVENT122DETEN	R/W	0h	Event(122) Detection Enable
24	EVENT121DETEN	R/W	0h	Event(121) Detection Enable
23	EVENT120DETEN	R/W	0h	Event(120) Detection Enable
22	EVENT119DETEN	R/W	0h	Event(119) Detection Enable
21	EVENT118DETEN	R/W	0h	Event(118) Detection Enable
20	EVENT117DETEN	R/W	0h	Event(117) Detection Enable
19	EVENT116DETEN	R/W	0h	Event(116) Detection Enable
18	EVENT115DETEN	R/W	0h	Event(115) Detection Enable
17	EVENT114DETEN	R/W	0h	Event(114) Detection Enable

Table 14-32851. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT113DETEN	R/W	0h	Event(113) Detection Enable
15	EVENT112DETEN	R/W	0h	Event(112) Detection Enable
14	EVENT111DETEN	R/W	0h	Event(111) Detection Enable
13	EVENT110DETEN	R/W	0h	Event(110) Detection Enable
12	EVENT109DETEN	R/W	0h	Event(109) Detection Enable
11	EVENT108DETEN	R/W	0h	Event(108) Detection Enable
10	EVENT107DETEN	R/W	0h	Event(107) Detection Enable
9	EVENT106DETEN	R/W	0h	Event(106) Detection Enable
8	EVENT105DETEN	R/W	0h	Event(105) Detection Enable
7	EVENT104DETEN	R/W	0h	Event(104) Detection Enable
6	EVENT103DETEN	R/W	0h	Event(103) Detection Enable
5	EVENT102DETEN	R/W	0h	Event(102) Detection Enable
4	EVENT101DETEN	R/W	0h	Event(101) Detection Enable
3	EVENT100DETEN	R/W	0h	Event(100) Detection Enable
2	EVENT99DETEN	R/W	0h	Event(99) Detection Enable
1	EVENT98DETEN	R/W	0h	Event(98) Detection Enable
0	EVENT97DETEN	R/W	0h	Event(97) Detection Enable

14.10.1.2.39 CTSET2_CFG_SETEVTENBL5 Register

1 CTSET2_CFG_SETEVTENBL5 Register (Offset = 40h) [reset = 0h]

System event detection enable register 5 (if number of events > 128)

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Table 14-32852. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2040h

Figure 14-10872. CTSET2_CFG_SETEVTENBL5 Name Register

31	30	29	28	27	26	25	24
EVENT160DETEN	EVENT159DETEN	EVENT158DETEN	EVENT157DETEN	EVENT156DETEN	EVENT155DETEN	EVENT154DETEN	EVENT153DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT152DETEN	EVENT151DETEN	EVENT150DETEN	EVENT149DETEN	EVENT148DETEN	EVENT147DETEN	EVENT1468DETEN	EVENT145DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT144DETEN	EVENT143DETEN	EVENT142DETEN	EVENT141DETEN	EVENT140DETEN	EVENT139DETEN	EVENT138DETEN	EVENT137DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT136DETEN	EVENT135DETEN	EVENT134DETEN	EVENT133DETEN	EVENT132DETEN	EVENT131DETEN	EVENT130DETEN	EVENT129DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32854. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT160DETEN	R/W	0h	Event(160) Detection Enable
30	EVENT159DETEN	R/W	0h	Event(159) Detection Enable
29	EVENT158DETEN	R/W	0h	Event(158) Detection Enable
28	EVENT157DETEN	R/W	0h	Event(157) Detection Enable
27	EVENT156DETEN	R/W	0h	Event(156) Detection Enable
26	EVENT155DETEN	R/W	0h	Event(155) Detection Enable
25	EVENT154DETEN	R/W	0h	Event(154) Detection Enable
24	EVENT153DETEN	R/W	0h	Event(153) Detection Enable
23	EVENT152DETEN	R/W	0h	Event(152) Detection Enable
22	EVENT151DETEN	R/W	0h	Event(151) Detection Enable
21	EVENT150DETEN	R/W	0h	Event(150) Detection Enable
20	EVENT149DETEN	R/W	0h	Event(149) Detection Enable
19	EVENT148DETEN	R/W	0h	Event(148) Detection Enable
18	EVENT147DETEN	R/W	0h	Event(147) Detection Enable
17	EVENT1468DETEN	R/W	0h	Event(146) Detection Enable

Table 14-32854. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT145DETEN	R/W	0h	Event(145) Detection Enable
15	EVENT144DETEN	R/W	0h	Event(144) Detection Enable
14	EVENT143DETEN	R/W	0h	Event(143) Detection Enable
13	EVENT142DETEN	R/W	0h	Event(142) Detection Enable
12	EVENT141DETEN	R/W	0h	Event(141) Detection Enable
11	EVENT140DETEN	R/W	0h	Event(140) Detection Enable
10	EVENT139DETEN	R/W	0h	Event(139) Detection Enable
9	EVENT138DETEN	R/W	0h	Event(138) Detection Enable
8	EVENT137DETEN	R/W	0h	Event(137) Detection Enable
7	EVENT136DETEN	R/W	0h	Event(136) Detection Enable
6	EVENT135DETEN	R/W	0h	Event(135) Detection Enable
5	EVENT134DETEN	R/W	0h	Event(134) Detection Enable
4	EVENT133DETEN	R/W	0h	Event(133) Detection Enable
3	EVENT132DETEN	R/W	0h	Event(132) Detection Enable
2	EVENT131DETEN	R/W	0h	Event(131) Detection Enable
1	EVENT130DETEN	R/W	0h	Event(130) Detection Enable
0	EVENT129DETEN	R/W	0h	Event(129) Detection Enable

14.10.1.2.40 CTSET2_CFG_SETEVTENBL6 Register

1 CTSET2_CFG_SETEVTENBL6 Register (Offset = 44h) [reset = 0h]

System event detection enable register 6 (if number of events > 160)

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Table 14-32855. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2044h

Figure 14-10873. CTSET2_CFG_SETEVTENBL6 Name Register

31	30	29	28	27	26	25	24
EVENT192DETEN	EVENT191DETEN	EVENT190DETEN	EVENT189DETEN	EVENT188DETEN	EVENT187DETEN	EVENT186DETEN	EVENT185DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT184DETEN	EVENT183DETEN	EVENT182DETEN	EVENT181DETEN	EVENT180DETEN	EVENT179DETEN	EVENT178DETEN	EVENT177DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT176DETEN	EVENT175DETEN	EVENT174DETEN	EVENT173DETEN	EVENT172DETEN	EVENT171DETEN	EVENT170DETEN	EVENT169DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT168DETEN	EVENT167DETEN	EVENT166DETEN	EVENT165DETEN	EVENT164DETEN	EVENT163DETEN	EVENT162DETEN	EVENT161DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32857. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT192DETEN	R/W	0h	Event(192) Detection Enable
30	EVENT191DETEN	R/W	0h	Event(191) Detection Enable
29	EVENT190DETEN	R/W	0h	Event(190) Detection Enable
28	EVENT189DETEN	R/W	0h	Event(189) Detection Enable
27	EVENT188DETEN	R/W	0h	Event(188) Detection Enable
26	EVENT187DETEN	R/W	0h	Event(187) Detection Enable
25	EVENT186DETEN	R/W	0h	Event(186) Detection Enable
24	EVENT185DETEN	R/W	0h	Event(185) Detection Enable
23	EVENT184DETEN	R/W	0h	Event(184) Detection Enable
22	EVENT183DETEN	R/W	0h	Event(183) Detection Enable
21	EVENT182DETEN	R/W	0h	Event(182) Detection Enable
20	EVENT181DETEN	R/W	0h	Event(181) Detection Enable
19	EVENT180DETEN	R/W	0h	Event(180) Detection Enable
18	EVENT179DETEN	R/W	0h	Event(179) Detection Enable
17	EVENT178DETEN	R/W	0h	Event(178) Detection Enable

Table 14-32857. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT177DETEN	R/W	0h	Event(177) Detection Enable
15	EVENT176DETEN	R/W	0h	Event(176) Detection Enable
14	EVENT175DETEN	R/W	0h	Event(175) Detection Enable
13	EVENT174DETEN	R/W	0h	Event(174) Detection Enable
12	EVENT173DETEN	R/W	0h	Event(173) Detection Enable
11	EVENT172DETEN	R/W	0h	Event(172) Detection Enable
10	EVENT171DETEN	R/W	0h	Event(171) Detection Enable
9	EVENT170DETEN	R/W	0h	Event(170) Detection Enable
8	EVENT169DETEN	R/W	0h	Event(169) Detection Enable
7	EVENT168DETEN	R/W	0h	Event(168) Detection Enable
6	EVENT167DETEN	R/W	0h	Event(167) Detection Enable
5	EVENT166DETEN	R/W	0h	Event(166) Detection Enable
4	EVENT165DETEN	R/W	0h	Event(165) Detection Enable
3	EVENT164DETEN	R/W	0h	Event(164) Detection Enable
2	EVENT163DETEN	R/W	0h	Event(163) Detection Enable
1	EVENT162DETEN	R/W	0h	Event(162) Detection Enable
0	EVENT161DETEN	R/W	0h	Event(161) Detection Enable

14.10.1.2.41 CTSET2_CFG_SETEVTENBL7 Register

1 CTSET2_CFG_SETEVTENBL7 Register (Offset = 48h) [reset = 0h]

System event detection enable register 7 (if number of events > 192)

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Table 14-32858. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2048h

Figure 14-10874. CTSET2_CFG_SETEVTENBL7 Name Register

31	30	29	28	27	26	25	24
EVENT224DETEN	EVENT223DETEN	EVENT222DETEN	EVENT221DETEN	EVENT220DETEN	EVENT219DETEN	EVENT218DETEN	EVENT217DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT216DETEN	EVENT215DETEN	EVENT214DETEN	EVENT213DETEN	EVENT212DETEN	EVENT211DETEN	EVENT210DETEN	EVENT209DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT208DETEN	EVENT207DETEN	EVENT206DETEN	EVENT205DETEN	EVENT204DETEN	EVENT203DETEN	EVENT202DETEN	EVENT201DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT200DETEN	EVENT199DETEN	EVENT198DETEN	EVENT197DETEN	EVENT196DETEN	EVENT195DETEN	EVENT194DETEN	EVENT193DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32860. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT224DETEN	R/W	0h	Event(224) Detection Enable
30	EVENT223DETEN	R/W	0h	Event(223) Detection Enable
29	EVENT222DETEN	R/W	0h	Event(222) Detection Enable
28	EVENT221DETEN	R/W	0h	Event(221) Detection Enable
27	EVENT220DETEN	R/W	0h	Event(220) Detection Enable
26	EVENT219DETEN	R/W	0h	Event(219) Detection Enable
25	EVENT218DETEN	R/W	0h	Event(218) Detection Enable
24	EVENT217DETEN	R/W	0h	Event(217) Detection Enable
23	EVENT216DETEN	R/W	0h	Event(216) Detection Enable
22	EVENT215DETEN	R/W	0h	Event(215) Detection Enable
21	EVENT214DETEN	R/W	0h	Event(214) Detection Enable
20	EVENT213DETEN	R/W	0h	Event(213) Detection Enable
19	EVENT212DETEN	R/W	0h	Event(212) Detection Enable
18	EVENT211DETEN	R/W	0h	Event(211) Detection Enable
17	EVENT210DETEN	R/W	0h	Event(210) Detection Enable

Table 14-32860. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT209DETEN	R/W	0h	Event(209) Detection Enable
15	EVENT208DETEN	R/W	0h	Event(208) Detection Enable
14	EVENT207DETEN	R/W	0h	Event(207) Detection Enable
13	EVENT206DETEN	R/W	0h	Event(206) Detection Enable
12	EVENT205DETEN	R/W	0h	Event(205) Detection Enable
11	EVENT204DETEN	R/W	0h	Event(204) Detection Enable
10	EVENT203DETEN	R/W	0h	Event(203) Detection Enable
9	EVENT202DETEN	R/W	0h	Event(202) Detection Enable
8	EVENT201DETEN	R/W	0h	Event(201) Detection Enable
7	EVENT200DETEN	R/W	0h	Event(200) Detection Enable
6	EVENT199DETEN	R/W	0h	Event(199) Detection Enable
5	EVENT198DETEN	R/W	0h	Event(198) Detection Enable
4	EVENT197DETEN	R/W	0h	Event(197) Detection Enable
3	EVENT196DETEN	R/W	0h	Event(196) Detection Enable
2	EVENT195DETEN	R/W	0h	Event(195) Detection Enable
1	EVENT194DETEN	R/W	0h	Event(194) Detection Enable
0	EVENT193DETEN	R/W	0h	Event(193) Detection Enable

14.10.1.2.42 CTSET2_CFG_SETEVTENBL8 Register

1 CTSET2_CFG_SETEVTENBL8 Register (Offset = 4Ch) [reset = 0h]

System event detection enable register 8 (if number of events > 224)

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Table 14-32861. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 204Ch**

Figure 14-10875. CTSET2_CFG_SETEVTENBL8 Name Register

31	30	29	28	27	26	25	24
EVENT256DETEN	EVENT255DETEN	EVENT254DETEN	EVENT253DETEN	EVENT252DETEN	EVENT251DETEN	EVENT250DETEN	EVENT249DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT248DETEN	EVENT247DETEN	EVENT246DETEN	EVENT245DETEN	EVENT244DETEN	EVENT243DETEN	EVENT242DETEN	EVENT241DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT240DETEN	EVENT239DETEN	EVENT238DETEN	EVENT237DETEN	EVENT236DETEN	EVENT235DETEN	EVENT234DETEN	EVENT233DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT232DETEN	EVENT231DETEN	EVENT230DETEN	EVENT229DETEN	EVENT228DETEN	EVENT227DETEN	EVENT226DETEN	EVENT225DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-32863. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT256DETEN	R/W	0h	Event(256) Detection Enable
30	EVENT255DETEN	R/W	0h	Event(255) Detection Enable
29	EVENT254DETEN	R/W	0h	Event(254) Detection Enable
28	EVENT253DETEN	R/W	0h	Event(253) Detection Enable
27	EVENT252DETEN	R/W	0h	Event(252) Detection Enable
26	EVENT251DETEN	R/W	0h	Event(251) Detection Enable
25	EVENT250DETEN	R/W	0h	Event(250) Detection Enable
24	EVENT249DETEN	R/W	0h	Event(249) Detection Enable
23	EVENT248DETEN	R/W	0h	Event(248) Detection Enable
22	EVENT247DETEN	R/W	0h	Event(247) Detection Enable
21	EVENT246DETEN	R/W	0h	Event(246) Detection Enable
20	EVENT245DETEN	R/W	0h	Event(245) Detection Enable
19	EVENT244DETEN	R/W	0h	Event(244) Detection Enable
18	EVENT243DETEN	R/W	0h	Event(243) Detection Enable
17	EVENT242DETEN	R/W	0h	Event(242) Detection Enable

Table 14-32863. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT241DETEN	R/W	0h	Event(241) Detection Enable
15	EVENT240DETEN	R/W	0h	Event(240) Detection Enable
14	EVENT239DETEN	R/W	0h	Event(239) Detection Enable
13	EVENT238DETEN	R/W	0h	Event(238) Detection Enable
12	EVENT237DETEN	R/W	0h	Event(237) Detection Enable
11	EVENT236DETEN	R/W	0h	Event(236) Detection Enable
10	EVENT235DETEN	R/W	0h	Event(235) Detection Enable
9	EVENT234DETEN	R/W	0h	Event(234) Detection Enable
8	EVENT233DETEN	R/W	0h	Event(233) Detection Enable
7	EVENT232DETEN	R/W	0h	Event(232) Detection Enable
6	EVENT231DETEN	R/W	0h	Event(231) Detection Enable
5	EVENT230DETEN	R/W	0h	Event(230) Detection Enable
4	EVENT229DETEN	R/W	0h	Event(229) Detection Enable
3	EVENT228DETEN	R/W	0h	Event(228) Detection Enable
2	EVENT227DETEN	R/W	0h	Event(227) Detection Enable
1	EVENT226DETEN	R/W	0h	Event(226) Detection Enable
0	EVENT225DETEN	R/W	0h	Event(225) Detection Enable

14.10.1.2.43 CTSET2_CFG_SETMSTID Register

1 CTSET2_CFG_SETMSTID Register (Offset = 50h) [reset = 0h]

System Event Initiator ID

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Table 14-32864. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2050h**

Figure 14-10876. CTSET2_CFG_SETMSTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
MASTID							
R/W							
0h							

Table 14-32866. CTSET2_CFG_SETMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.10.1.2.44 CTSET2_CFG_CTCNTL Register

1 CTSET2_CFG_CTCNTL Register (Offset = 800h) [reset = 0h]

Counter Timer Control

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Table 14-32867. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2800h**

Figure 14-10877. CTSET2_CFG_CTCNTL Name Register

31	30	29	28	27	26	25	24
NUMSTM						NUMINPT	
R						R	
0h						0h	
23	22	21	20	19	18	17	16
NUMINPT						NUMTIMR	
R						R	
0h						0h	
15	14	13	12	11	10	9	8
NUMTIMR			NUMCNTR				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
NUMCNTR	REVID				RESERVED	RESERVED	NUMCOREMD
R	R				NONE	R	R
0h	0h				0h	0h	0h

Table 14-32869. CTSET2_CFG_CTCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NUMSTM	R	0h	Number of counters that can export via STM
25:18	NUMINPT	R	0h	Number of event input signals
17:13	NUMTIMR	R	0h	Number of timers in the module
12:7	NUMCNTR	R	0h	Number of counters in the module
6:3	REVID	R	0h	Revision ID of CTSET
2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	0h	Reserved, returns 0
0	NUMCOREMD	R	0h	Indicated the number of mode bus interfaces, 0 is 2 CPU buses, 1 is 4 buses

14.10.1.2.45 CTSET2_CFG_CTNUMDBG Register

1 CTSET2_CFG_CTNUMDBG Register (Offset = 804h) [reset = 0h]

Counter Timer Number Debug Event Register

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Table 14-32870. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2804h**

Figure 14-10878. CTSET2_CFG_CTNUMDBG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	NUMEVT		
R				NONE	R		
0h				0h	0h		

Table 14-32872. CTSET2_CFG_CTNUMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	NUMEVT	R	0h	Number of input selectors for debug events

14.10.1.2.46 CTSET2_CFG_CTUSERACCCTL Register

1 CTSET2_CFG_CTUSERACCCTL Register (Offset = 808h) [reset = 0h]

Counter Timer User Access Control, can only be written in priviledged mode

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Table 14-32873. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2808h**

Figure 14-10879. CTSET2_CFG_CTUSERACCCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					SECUSER	RUSER	NRUSER
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-32875. CTSET2_CFG_CTUSERACCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
1	RUSER	R/W	0h	Counter functions while system is in Root-User mode
0	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode

14.10.1.2.47 CTSET2_CFG_CTSTMCNTL Register

1 CTSET2_CFG_CTSTMCNTL Register (Offset = 820h) [reset = 0h]

Counter Timer STM Control register

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Table 14-32876. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2820h**

Figure 14-10880. CTSET2_CFG_CTSTMCNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				NUMXPORT			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
NUMXPORT		XPORTACT	CCMPORT	CCMAVAIL	CSMXPORT	SENDOVR	ENBL
R		R	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-32878. CTSET2_CFG_CTSTMCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:6	NUMXPORT	R	0h	The total number of counters designated for export
5	XPORTACT	R	0h	Indicates if a frame is currently being written to the STM.
4	CCMPORT	R/W	0h	SW control of CCM message export
3	CCMAVAIL	R/W	0h	CTSET supports CCM export
2	CSMXPORT	R/W	0h	SW control of CSM message export
1	SENDOVR	R/W	0h	Send overflow data in CSM frame
0	ENBL	R/W	0h	CTSET STM global enable for counter/timer messages

14.10.1.2.48 CTSET2_CFG_CTSTMMSTID Register

1 CTSET2_CFG_CTSTMMSTID Register (Offset = 824h) [reset = 0h]

Counter Timer STM Initiator ID register

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Table 14-32879. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2824h**

Figure 14-10881. CTSET2_CFG_CTSTMMSTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
MASTID							
R/W							
0h							

Table 14-32881. CTSET2_CFG_CTSTMMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module

14.10.1.2.49 CTSET2_CFG_CTSTMINTVL Register

1 CTSET2_CFG_CTSTMINTVL Register (Offset = 828h) [reset = 0h]

Counter Timer STM Interval Register

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Table 14-32882. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2828h**

Figure 14-10882. CTSET2_CFG_CTSTMINTVL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">INTERVAL</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32884. CTSET2_CFG_CTSTMINTVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	INTERVAL	R/W	0h	Counter Timer Periodic export interval

14.10.1.2.50 CTSET2_CFG_CTSTMSEL0 Register

1 CTSET2_CFG_CTSTMSEL0 Register (Offset = 82Ch) [reset = 0h]

Counter Timer STM Counter Select Register 0. This Selects Counter 0 to 31

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Table 14-32885. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 282Ch**

Figure 14-10883. CTSET2_CFG_CTSTMSEL0 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-32887. CTSET2_CFG_CTSTMSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.10.1.2.51 CTSET2_CFG_CTSTMSEL1 Register

1 CTSET2_CFG_CTSTMSEL1 Register (Offset = 830h) [reset = 0h]

Counter Timer STM Counter Select Register 1. This Selects Counter 32 to 63

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Table 14-32888. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2830h**

Figure 14-10884. CTSET2_CFG_CTSTMSEL1 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-32890. CTSET2_CFG_CTSTMSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.10.1.2.52 CTSET2_CFG_CTINTVLR0 Register

1 CTSET2_CFG_CTINTVLR0 Register (Offset = 840h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32891. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2840h

Figure 14-10885. CTSET2_CFG_CTINTVLR0 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32893. CTSET2_CFG_CTINTVLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.53 CTSET2_CFG_CTINTVLR1 Register

1 CTSET2_CFG_CTINTVLR1 Register (Offset = 844h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32894. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2844h**

Figure 14-10886. CTSET2_CFG_CTINTVLR1 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32896. CTSET2_CFG_CTINTVLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.54 CTSET2_CFG_CTINTVLR2 Register

1 CTSET2_CFG_CTINTVLR2 Register (Offset = 848h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32897. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2848h**

Figure 14-10887. CTSET2_CFG_CTINTVLR2 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32899. CTSET2_CFG_CTINTVLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.55 CTSET2_CFG_CTINTVLR3 Register

1 CTSET2_CFG_CTINTVLR3 Register (Offset = 84Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32900. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 284Ch**

Figure 14-10888. CTSET2_CFG_CTINTVLR3 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32902. CTSET2_CFG_CTINTVLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.56 CTSET2_CFG_CTINTVLR4 Register

1 CTSET2_CFG_CTINTVLR4 Register (Offset = 850h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32903. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2850h**

Figure 14-10889. CTSET2_CFG_CTINTVLR4 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32905. CTSET2_CFG_CTINTVLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.57 CTSET2_CFG_CTINTVLR5 Register

1 CTSET2_CFG_CTINTVLR5 Register (Offset = 854h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32906. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2854h**

Figure 14-10890. CTSET2_CFG_CTINTVLR5 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32908. CTSET2_CFG_CTINTVLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.58 CTSET2_CFG_CTINTVLR6 Register

1 CTSET2_CFG_CTINTVLR6 Register (Offset = 858h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32909. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2858h**

Figure 14-10891. CTSET2_CFG_CTINTVLR6 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32911. CTSET2_CFG_CTINTVLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.59 CTSET2_CFG_CTINTVLR7 Register

1 CTSET2_CFG_CTINTVLR7 Register (Offset = 85Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32912. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 285Ch**

Figure 14-10892. CTSET2_CFG_CTINTVLR7 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32914. CTSET2_CFG_CTINTVLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.60 CTSET2_CFG_CTINTVLR8 Register

1 CTSET2_CFG_CTINTVLR8 Register (Offset = 860h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32915. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2860h**

Figure 14-10893. CTSET2_CFG_CTINTVLR8 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32917. CTSET2_CFG_CTINTVLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.61 CTSET2_CFG_CTINTVLR9 Register

1 CTSET2_CFG_CTINTVLR9 Register (Offset = 864h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32918. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2864h**

Figure 14-10894. CTSET2_CFG_CTINTVLR9 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32920. CTSET2_CFG_CTINTVLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.62 CTSET2_CFG_CTINTVLR10 Register

1 CTSET2_CFG_CTINTVLR10 Register (Offset = 868h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32921. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2868h**

Figure 14-10895. CTSET2_CFG_CTINTVLR10 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32923. CTSET2_CFG_CTINTVLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.63 CTSET2_CFG_CTINTVLR11 Register

1 CTSET2_CFG_CTINTVLR11 Register (Offset = 86Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32924. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 286Ch

Figure 14-10896. CTSET2_CFG_CTINTVLR11 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32926. CTSET2_CFG_CTINTVLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.64 CTSET2_CFG_CTINTVLR12 Register

1 CTSET2_CFG_CTINTVLR12 Register (Offset = 870h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32927. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2870h**

Figure 14-10897. CTSET2_CFG_CTINTVLR12 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32929. CTSET2_CFG_CTINTVLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.65 CTSET2_CFG_CTINTVLR13 Register

1 CTSET2_CFG_CTINTVLR13 Register (Offset = 874h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32930. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2874h**

Figure 14-10898. CTSET2_CFG_CTINTVLR13 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32932. CTSET2_CFG_CTINTVLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.66 CTSET2_CFG_CTINTVLR14 Register

1 CTSET2_CFG_CTINTVLR14 Register (Offset = 878h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32933. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2878h**

Figure 14-10899. CTSET2_CFG_CTINTVLR14 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-32935. CTSET2_CFG_CTINTVLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.67 CTSET2_CFG_CTINTVLR15 Register

1 CTSET2_CFG_CTINTVLR15 Register (Offset = 87Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-32936. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 287Ch**

Figure 14-10900. CTSET2_CFG_CTINTVLR15 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTERVAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTERVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTERVAL							
R/W							
0h							

Table 14-32938. CTSET2_CFG_CTINTVLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.10.1.2.68 CTSET2_CFG_CTDBGSGL0 Register

1 CTSET2_CFG_CTDBGSGL0 Register (Offset = 8A0h) [reset = 0h]

Timer Interval Register 0. Interval match value for timer 0 in CTSET Timer Interval Register 1. Interval match value for timer 1 in CTSET Timer Interval Register 2. Interval match value for timer 2 in CTSET Timer Interval Register 3. Interval match value for timer 3 in CTSET Timer Interval Register 4. Interval match value for timer 4 in CTSET Timer Interval Register 5. Interval match value for timer 5 in CTSET Timer Interval Register 6. Interval match value for timer 6 in CTSET Timer Interval Register 7. Interval match value for timer 7 in CTSET Timer Interval Register 8. Interval match value for timer 8 in CTSET Timer Interval Register 9. Interval match value for timer 9 in CTSET Timer Interval Register 10. Interval match value for timer 10 in CTSET Timer Interval Register 11. Interval match value for timer 11 in CTSET Timer Interval Register 12. Interval match value for timer 12 in CTSET Timer Interval Register 13. Interval match value for timer 13 in CTSET Timer Interval Register 14. Interval match value for timer 14 in CTSET Timer Interval Register 15. Interval match value for timer 15 in CTSET Counter Timer Debug Event Register 0

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Table 14-32939. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A0h**

Figure 14-10901. CTSET2_CFG_CTDBGSGL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32941. CTSET2_CFG_CTDBGSGL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.69 CTSET2_CFG_CTDBGSGL1 Register

1 CTSET2_CFG_CTDBGSGL1 Register (Offset = 8A4h) [reset = 0h]

Counter Timer Debug Event Register 1

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Table 14-32942. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A4h**

Figure 14-10902. CTSET2_CFG_CTDBGSGL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32944. CTSET2_CFG_CTDBGSGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.70 CTSET2_CFG_CTDBGSGL2 Register

1 CTSET2_CFG_CTDBGSGL2 Register (Offset = 8A8h) [reset = 0h]

Counter Timer Debug Event Register 2

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Table 14-32945. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A8h**

Figure 14-10903. CTSET2_CFG_CTDBGSGL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32947. CTSET2_CFG_CTDBGSGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.71 CTSET2_CFG_CTDBGSGL3 Register

1 CTSET2_CFG_CTDBGSGL3 Register (Offset = 8ACh) [reset = 0h]

Counter Timer Debug Event Register 3

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Table 14-32948. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28ACh**

Figure 14-10904. CTSET2_CFG_CTDBGSGL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32950. CTSET2_CFG_CTDBGSGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.72 CTSET2_CFG_CTDBGSGL4 Register

1 CTSET2_CFG_CTDBGSGL4 Register (Offset = 8B0h) [reset = 0h]

Counter Timer Debug Event Register 4

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Table 14-32951. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B0h**

Figure 14-10905. CTSET2_CFG_CTDBGSGL4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32953. CTSET2_CFG_CTDBGSGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.73 CTSET2_CFG_CTDBGSGL5 Register

1 CTSET2_CFG_CTDBGSGL5 Register (Offset = 8B4h) [reset = 0h]

Counter Timer Debug Event Register5

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Table 14-32954. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B4h**

Figure 14-10906. CTSET2_CFG_CTDBGSGL5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32956. CTSET2_CFG_CTDBGSGL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.74 CTSET2_CFG_CTDBGSGL6 Register

1 CTSET2_CFG_CTDBGSGL6 Register (Offset = 8B8h) [reset = 0h]

Counter Timer Debug Event Register 6

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Table 14-32957. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B8h**

Figure 14-10907. CTSET2_CFG_CTDBGSGL6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-32959. CTSET2_CFG_CTDBGSGL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.75 CTSET2_CFG_CTDBGSGL7 Register

1 CTSET2_CFG_CTDBGSGL7 Register (Offset = 8BCh) [reset = 0h]

Counter Timer Debug Event Register 7

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Table 14-32960. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28BCh**

Figure 14-10908. CTSET2_CFG_CTDBGSGL7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-32962. CTSET2_CFG_CTDBGSGL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.10.1.2.76 CTSET2_CFG_CTGNBL0 Register

1 CTSET2_CFG_CTGNBL0 Register (Offset = 9F0h) [reset = 0h]

Counter Timer Global Enable Register 0. This enables Counter 0 to 31

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Table 14-32963. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 29F0h

Figure 14-10909. CTSET2_CFG_CTGNBL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-32965. CTSET2_CFG_CTGNBL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter. Bits 30 and 31 will be high if global time stamp output interface is enabled

14.10.1.2.77 CTSET2_CFG_CTGNBL1 Register

1 CTSET2_CFG_CTGNBL1 Register (Offset = 9F4h) [reset = 0h]

Counter Timer Global Enable Register 1. This enables Counter 32 to 63

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Table 14-32966. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 29F4h**

Figure 14-10910. CTSET2_CFG_CTGNBL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-32968. CTSET2_CFG_CTGNBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter

14.10.1.2.78 CTSET2_CFG_CTGRST0 Register

1 CTSET2_CFG_CTGRST0 Register (Offset = 9F8h) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 0 to 31

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Table 14-32969. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29F8h**

Figure 14-10911. CTSET2_CFG_CTGRST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-32971. CTSET2_CFG_CTGRST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared. When Global Time Stamp output interface is enabled, counter 31 and counter 30 should not be written to any value

14.10.1.2.79 CTSET2_CFG_CTGRST1 Register

1 CTSET2_CFG_CTGRST1 Register (Offset = 9FCh) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 32 to 63

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Table 14-32972. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29FCh**

Figure 14-10912. CTSET2_CFG_CTGRST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-32974. CTSET2_CFG_CTGRST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared.

14.10.1.2.80 CTSET2_CFG_CTCR0 Register

1 CTSET2_CFG_CTCR0 Register (Offset = A00h) [reset = 0h]

Counter Timer Control Register 0

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Table 14-32975. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2A00h

Figure 14-10913. CTSET2_CFG_CTCR0 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32977. CTSET2_CFG_CTCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32977. CTSET2_CFG_CTCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.81 CTSET2_CFG_CTCR1 Register

1 CTSET2_CFG_CTCR1 Register (Offset = A04h) [reset = 0h]

Counter Timer Control Register 1

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Table 14-32978. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A04h**

Figure 14-10914. CTSET2_CFG_CTCR1 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32980. CTSET2_CFG_CTCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32980. CTSET2_CFG_CTCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.82 CTSET2_CFG_CTCR2 Register

1 CTSET2_CFG_CTCR2 Register (Offset = A08h) [reset = 0h]

Counter Timer Control Register 2

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Table 14-32981. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A08h**

Figure 14-10915. CTSET2_CFG_CTCR2 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32983. CTSET2_CFG_CTCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32983. CTSET2_CFG_CTCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.83 CTSET2_CFG_CTCR3 Register

1 CTSET2_CFG_CTCR3 Register (Offset = A0Ch) [reset = 0h]

Counter Timer Control Register 3

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Table 14-32984. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A0Ch**

Figure 14-10916. CTSET2_CFG_CTCR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-32986. CTSET2_CFG_CTCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32986. CTSET2_CFG_CTCR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.84 CTSET2_CFG_CTCR4 Register

1 CTSET2_CFG_CTCR4 Register (Offset = A10h) [reset = 0h]

Counter Timer Control Register 4

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Table 14-32987. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A10h**

Figure 14-10917. CTSET2_CFG_CTCR4 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32989. CTSET2_CFG_CTCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32989. CTSET2_CFG_CTCR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.85 CTSET2_CFG_CTCR5 Register

1 CTSET2_CFG_CTCR5 Register (Offset = A14h) [reset = 0h]

Counter Timer Control Register 5

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Table 14-32990. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A14h**

Figure 14-10918. CTSET2_CFG_CTCR5 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32992. CTSET2_CFG_CTCR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32992. CTSET2_CFG_CTCR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.86 CTSET2_CFG_CTCR6 Register

1 CTSET2_CFG_CTCR6 Register (Offset = A18h) [reset = 0h]

Counter Timer Control Register 6

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Table 14-32993. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A18h**

Figure 14-10919. CTSET2_CFG_CTCR6 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32995. CTSET2_CFG_CTCR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32995. CTSET2_CFG_CTCR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.87 CTSET2_CFG_CTCR7 Register

1 CTSET2_CFG_CTCR7 Register (Offset = A1Ch) [reset = 0h]

Counter Timer Control Register 7

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Table 14-32996. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2A1Ch

Figure 14-10920. CTSET2_CFG_CTCR7 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-32998. CTSET2_CFG_CTCR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-32998. CTSET2_CFG_CTCR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.88 CTSET2_CFG_CTCR8 Register

1 CTSET2_CFG_CTCR8 Register (Offset = A20h) [reset = 0h]

Counter Timer Control Register 8

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Table 14-32999. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A20h**

Figure 14-10921. CTSET2_CFG_CTCR8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33001. CTSET2_CFG_CTCR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33001. CTSET2_CFG_CTCR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.89 CTSET2_CFG_CTCR9 Register

1 CTSET2_CFG_CTCR9 Register (Offset = A24h) [reset = 0h]

Counter Timer Control Register 9

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Table 14-33002. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A24h**

Figure 14-10922. CTSET2_CFG_CTCR9 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33004. CTSET2_CFG_CTCR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33004. CTSET2_CFG_CTCR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.90 CTSET2_CFG_CTCR10 Register

1 CTSET2_CFG_CTCR10 Register (Offset = A28h) [reset = 0h]

Counter Timer Control Register 10

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Table 14-33005. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A28h**

Figure 14-10923. CTSET2_CFG_CTCR10 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33007. CTSET2_CFG_CTCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33007. CTSET2_CFG_CTCR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.91 CTSET2_CFG_CTCR11 Register

1 CTSET2_CFG_CTCR11 Register (Offset = A2Ch) [reset = 0h]

Counter Timer Control Register 11

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Table 14-33008. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A2Ch**

Figure 14-10924. CTSET2_CFG_CTCR11 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33010. CTSET2_CFG_CTCR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33010. CTSET2_CFG_CTCR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.92 CTSET2_CFG_CTCR12 Register

1 CTSET2_CFG_CTCR12 Register (Offset = A30h) [reset = 0h]

Counter Timer Control Register 12

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Table 14-33011. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A30h**

Figure 14-10925. CTSET2_CFG_CTCR12 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33013. CTSET2_CFG_CTCR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33013. CTSET2_CFG_CTCR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.93 CTSET2_CFG_CTCR13 Register

1 CTSET2_CFG_CTCR13 Register (Offset = A34h) [reset = 0h]

Counter Timer Control Register 13

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Table 14-33014. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A34h**

Figure 14-10926. CTSET2_CFG_CTCR13 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33016. CTSET2_CFG_CTCR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33016. CTSET2_CFG_CTCR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.94 CTSET2_CFG_CTCR14 Register

1 CTSET2_CFG_CTCR14 Register (Offset = A38h) [reset = 0h]

Counter Timer Control Register 14

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Table 14-33017. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A38h**

Figure 14-10927. CTSET2_CFG_CTCR14 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33019. CTSET2_CFG_CTCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33019. CTSET2_CFG_CTCR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.95 CTSET2_CFG_CTCR15 Register

1 CTSET2_CFG_CTCR15 Register (Offset = A3Ch) [reset = 0h]

Counter Timer Control Register 15

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Table 14-33020. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A3Ch**

Figure 14-10928. CTSET2_CFG_CTCR15 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33022. CTSET2_CFG_CTCR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33022. CTSET2_CFG_CTCR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.96 CTSET2_CFG_CTCR16 Register

1 CTSET2_CFG_CTCR16 Register (Offset = A40h) [reset = 0h]

Counter Timer Control Register 16

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Table 14-33023. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A40h**

Figure 14-10929. CTSET2_CFG_CTCR16 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33025. CTSET2_CFG_CTCR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33025. CTSET2_CFG_CTCR16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.97 CTSET2_CFG_CTCR17 Register

1 CTSET2_CFG_CTCR17 Register (Offset = A44h) [reset = 0h]

Counter Timer Control Register 17

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Table 14-33026. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A44h**

Figure 14-10930. CTSET2_CFG_CTCR17 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33028. CTSET2_CFG_CTCR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33028. CTSET2_CFG_CTCR17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.98 CTSET2_CFG_CTCR18 Register

1 CTSET2_CFG_CTCR18 Register (Offset = A48h) [reset = 0h]

Counter Timer Control Register 18

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Table 14-33029. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A48h**

Figure 14-10931. CTSET2_CFG_CTCR18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33031. CTSET2_CFG_CTCR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33031. CTSET2_CFG_CTCR18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.99 CTSET2_CFG_CTCR19 Register

1 CTSET2_CFG_CTCR19 Register (Offset = A4Ch) [reset = 0h]

Counter Timer Control Register 19

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Table 14-33032. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A4Ch**

Figure 14-10932. CTSET2_CFG_CTCR19 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33034. CTSET2_CFG_CTCR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33034. CTSET2_CFG_CTCR19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.100 CTSET2_CFG_CTCR20 Register

1 CTSET2_CFG_CTCR20 Register (Offset = A50h) [reset = 0h]

Counter Timer Control Register 20

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Table 14-33035. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A50h**

Figure 14-10933. CTSET2_CFG_CTCR20 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33037. CTSET2_CFG_CTCR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33037. CTSET2_CFG_CTCR20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.101 CTSET2_CFG_CTCR21 Register

1 CTSET2_CFG_CTCR21 Register (Offset = A54h) [reset = 0h]

Counter Timer Control Register 21

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Table 14-33038. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A54h**

Figure 14-10934. CTSET2_CFG_CTCR21 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33040. CTSET2_CFG_CTCR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33040. CTSET2_CFG_CTCR21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.102 CTSET2_CFG_CTCR22 Register

1 CTSET2_CFG_CTCR22 Register (Offset = A58h) [reset = 0h]

Counter Timer Control Register 22

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Table 14-33041. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A58h**

Figure 14-10935. CTSET2_CFG_CTCR22 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33043. CTSET2_CFG_CTCR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33043. CTSET2_CFG_CTCR22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.103 CTSET2_CFG_CTCR23 Register

1 CTSET2_CFG_CTCR23 Register (Offset = A5Ch) [reset = 0h]

Counter Timer Control Register 23

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Table 14-33044. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A5Ch**

Figure 14-10936. CTSET2_CFG_CTCR23 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33046. CTSET2_CFG_CTCR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33046. CTSET2_CFG_CTCR23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.104 CTSET2_CFG_CTCR24 Register

1 CTSET2_CFG_CTCR24 Register (Offset = A60h) [reset = 0h]

Counter Timer Control Register 24

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Table 14-33047. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A60h**

Figure 14-10937. CTSET2_CFG_CTCR24 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33049. CTSET2_CFG_CTCR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33049. CTSET2_CFG_CTCR24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.105 CTSET2_CFG_CTCR25 Register

1 CTSET2_CFG_CTCR25 Register (Offset = A64h) [reset = 0h]

Counter Timer Control Register 25

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Table 14-33050. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A64h**

Figure 14-10938. CTSET2_CFG_CTCR25 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33052. CTSET2_CFG_CTCR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33052. CTSET2_CFG_CTCR25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.106 CTSET2_CFG_CTCR26 Register

1 CTSET2_CFG_CTCR26 Register (Offset = A68h) [reset = 0h]

Counter Timer Control Register 26

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Table 14-33053. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A68h**

Figure 14-10939. CTSET2_CFG_CTCR26 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33055. CTSET2_CFG_CTCR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33055. CTSET2_CFG_CTCR26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.107 CTSET2_CFG_CTCR27 Register

1 CTSET2_CFG_CTCR27 Register (Offset = A6Ch) [reset = 0h]

Counter Timer Control Register 27

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Table 14-33056. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A6Ch**

Figure 14-10940. CTSET2_CFG_CTCR27 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33058. CTSET2_CFG_CTCR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33058. CTSET2_CFG_CTCR27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.108 CTSET2_CFG_CTCR28 Register

1 CTSET2_CFG_CTCR28 Register (Offset = A70h) [reset = 0h]

Counter Timer Control Register 28

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Table 14-33059. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A70h**

Figure 14-10941. CTSET2_CFG_CTCR28 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33061. CTSET2_CFG_CTCR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33061. CTSET2_CFG_CTCR28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.109 CTSET2_CFG_CTCR29 Register

1 CTSET2_CFG_CTCR29 Register (Offset = A74h) [reset = 0h]

Counter Timer Control Register 29

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Table 14-33062. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2A74h

Figure 14-10942. CTSET2_CFG_CTCR29 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33064. CTSET2_CFG_CTCR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33064. CTSET2_CFG_CTCR29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.110 CTSET2_CFG_CTCR30 Register

1 CTSET2_CFG_CTCR30 Register (Offset = A78h) [reset = 0h]

Counter Timer Control Register 30

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Table 14-33065. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A78h**

Figure 14-10943. CTSET2_CFG_CTCR30 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-33067. CTSET2_CFG_CTCR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33067. CTSET2_CFG_CTCR30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.111 CTSET2_CFG_CTCR31 Register

1 CTSET2_CFG_CTCR31 Register (Offset = A7Ch) [reset = 0h]

Counter Timer Control Register 31

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Table 14-33068. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A7Ch**

Figure 14-10944. CTSET2_CFG_CTCR31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33070. CTSET2_CFG_CTCR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-33070. CTSET2_CFG_CTCR31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.10.1.2.112 CTSET2_CFG_CTOWN0 Register

1 CTSET2_CFG_CTOWN0 Register (Offset = A80h) [reset = 20000000h]

Counter/Timer Ownership register 0

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Table 14-33071. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A80h**

Figure 14-10945. CTSET2_CFG_CTOWN0 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33073. CTSET2_CFG_CTOWN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.113 CTSET2_CFG_CTOWN1 Register

1 CTSET2_CFG_CTOWN1 Register (Offset = A84h) [reset = 20000000h]

Counter/Timer Ownership register 1

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Table 14-33074. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A84h**

Figure 14-10946. CTSET2_CFG_CTOWN1 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33076. CTSET2_CFG_CTOWN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.114 CTSET2_CFG_CTOWN2 Register

1 CTSET2_CFG_CTOWN2 Register (Offset = A88h) [reset = 20000000h]

Counter/Timer Ownership register 2

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Table 14-33077. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A88h**

Figure 14-10947. CTSET2_CFG_CTOWN2 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33079. CTSET2_CFG_CTOWN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.115 CTSET2_CFG_CTOWN3 Register

1 CTSET2_CFG_CTOWN3 Register (Offset = A8Ch) [reset = 20000000h]

Counter/Timer Ownership register 3

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Table 14-33080. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A8Ch**

Figure 14-10948. CTSET2_CFG_CTOWN3 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33082. CTSET2_CFG_CTOWN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.116 CTSET2_CFG_CTOWN4 Register

1 CTSET2_CFG_CTOWN4 Register (Offset = A90h) [reset = 20000000h]

Counter/Timer Ownership register 4

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Table 14-33083. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A90h**

Figure 14-10949. CTSET2_CFG_CTOWN4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33085. CTSET2_CFG_CTOWN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.117 CTSET2_CFG_CTOWN5 Register

1 CTSET2_CFG_CTOWN5 Register (Offset = A94h) [reset = 20000000h]

Counter/Timer Ownership register 5

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Table 14-33086. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A94h**

Figure 14-10950. CTSET2_CFG_CTOWN5 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33088. CTSET2_CFG_CTOWN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.118 CTSET2_CFG_CTOWN6 Register

1 CTSET2_CFG_CTOWN6 Register (Offset = A98h) [reset = 20000000h]

Counter/Timer Ownership register 6

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Table 14-33089. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A98h**

Figure 14-10951. CTSET2_CFG_CTOWN6 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33091. CTSET2_CFG_CTOWN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.119 CTSET2_CFG_CTOWN7 Register

1 CTSET2_CFG_CTOWN7 Register (Offset = A9Ch) [reset = 20000000h]

Counter/Timer Ownership register 7

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Table 14-33092. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A9Ch**

Figure 14-10952. CTSET2_CFG_CTOWN7 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33094. CTSET2_CFG_CTOWN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.120 CTSET2_CFG_CTOWN8 Register

1 CTSET2_CFG_CTOWN8 Register (Offset = AA0h) [reset = 20000000h]

Counter/Timer Ownership register 8

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Table 14-33095. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA0h**

Figure 14-10953. CTSET2_CFG_CTOWN8 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33097. CTSET2_CFG_CTOWN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.121 CTSET2_CFG_CTOWN9 Register

1 CTSET2_CFG_CTOWN9 Register (Offset = AA4h) [reset = 20000000h]

Counter/Timer Ownership register 9

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Table 14-33098. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA4h**

Figure 14-10954. CTSET2_CFG_CTOWN9 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33100. CTSET2_CFG_CTOWN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.122 CTSET2_CFG_CTOWN10 Register

1 CTSET2_CFG_CTOWN10 Register (Offset = AA8h) [reset = 20000000h]

Counter/Timer Ownership register 10

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Table 14-33101. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA8h**

Figure 14-10955. CTSET2_CFG_CTOWN10 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33103. CTSET2_CFG_CTOWN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.123 CTSET2_CFG_CTOWN11 Register

1 CTSET2_CFG_CTOWN11 Register (Offset = AACh) [reset = 20000000h]

Counter/Timer Ownership register 11

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Table 14-33104. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AACh**

Figure 14-10956. CTSET2_CFG_CTOWN11 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33106. CTSET2_CFG_CTOWN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.124 CTSET2_CFG_CTOWN12 Register

1 CTSET2_CFG_CTOWN12 Register (Offset = AB0h) [reset = 20000000h]

Counter/Timer Ownership register 12

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Table 14-33107. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2AB0h**

Figure 14-10957. CTSET2_CFG_CTOWN12 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33109. CTSET2_CFG_CTOWN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.125 CTSET2_CFG_CTOWN13 Register

1 CTSET2_CFG_CTOWN13 Register (Offset = AB4h) [reset = 20000000h]

Counter/Timer Ownership register 13

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Table 14-33110. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AB4h**

Figure 14-10958. CTSET2_CFG_CTOWN13 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33112. CTSET2_CFG_CTOWN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.126 CTSET2_CFG_CTOWN14 Register

1 CTSET2_CFG_CTOWN14 Register (Offset = AB8h) [reset = 20000000h]

Counter/Timer Ownership register 14

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Table 14-33113. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AB8h**

Figure 14-10959. CTSET2_CFG_CTOWN14 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33115. CTSET2_CFG_CTOWN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.127 CTSET2_CFG_CTOWN15 Register

1 CTSET2_CFG_CTOWN15 Register (Offset = ABCh) [reset = 20000000h]

Counter/Timer Ownership register 15

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Table 14-33116. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2ABCh**

Figure 14-10960. CTSET2_CFG_CTOWN15 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33118. CTSET2_CFG_CTOWN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.128 CTSET2_CFG_CTOWN16 Register

1 CTSET2_CFG_CTOWN16 Register (Offset = AC0h) [reset = 20000000h]

Counter/Timer Ownership register 16

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Table 14-33119. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AC0h**

Figure 14-10961. CTSET2_CFG_CTOWN16 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33121. CTSET2_CFG_CTOWN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.129 CTSET2_CFG_CTOWN17 Register

1 CTSET2_CFG_CTOWN17 Register (Offset = AC4h) [reset = 20000000h]

Counter/Timer Ownership register 17

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Table 14-33122. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AC4h**

Figure 14-10962. CTSET2_CFG_CTOWN17 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33124. CTSET2_CFG_CTOWN17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.130 CTSET2_CFG_CTOWN18 Register

1 CTSET2_CFG_CTOWN18 Register (Offset = AC8h) [reset = 20000000h]

Counter/Timer Ownership register 18

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Table 14-33125. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AC8h**

Figure 14-10963. CTSET2_CFG_CTOWN18 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33127. CTSET2_CFG_CTOWN18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.131 CTSET2_CFG_CTOWN19 Register

1 CTSET2_CFG_CTOWN19 Register (Offset = ACCh) [reset = 20000000h]

Counter/Timer Ownership register 19

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Table 14-33128. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2ACCh**

Figure 14-10964. CTSET2_CFG_CTOWN19 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33130. CTSET2_CFG_CTOWN19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.132 CTSET2_CFG_CTOWN20 Register

1 CTSET2_CFG_CTOWN20 Register (Offset = AD0h) [reset = 20000000h]

Counter/Timer Ownership register 20

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Table 14-33131. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD0h**

Figure 14-10965. CTSET2_CFG_CTOWN20 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33133. CTSET2_CFG_CTOWN20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.133 CTSET2_CFG_CTOWN21 Register

1 CTSET2_CFG_CTOWN21 Register (Offset = AD4h) [reset = 20000000h]

Counter/Timer Ownership register 21

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Table 14-33134. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD4h**

Figure 14-10966. CTSET2_CFG_CTOWN21 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33136. CTSET2_CFG_CTOWN21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.134 CTSET2_CFG_CTOWN22 Register

1 CTSET2_CFG_CTOWN22 Register (Offset = AD8h) [reset = 20000000h]

Counter/Timer Ownership register 22

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Table 14-33137. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD8h**

Figure 14-10967. CTSET2_CFG_CTOWN22 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33139. CTSET2_CFG_CTOWN22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.135 CTSET2_CFG_CTOWN23 Register

1 CTSET2_CFG_CTOWN23 Register (Offset = ADCh) [reset = 20000000h]

Counter/Timer Ownership register2 3

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Table 14-33140. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2ADCh**

Figure 14-10968. CTSET2_CFG_CTOWN23 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33142. CTSET2_CFG_CTOWN23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.136 CTSET2_CFG_CTOWN24 Register

1 CTSET2_CFG_CTOWN24 Register (Offset = AE0h) [reset = 20000000h]

Counter/Timer Ownership register 24

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Table 14-33143. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2AE0h**

Figure 14-10969. CTSET2_CFG_CTOWN24 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33145. CTSET2_CFG_CTOWN24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.137 CTSET2_CFG_CTOWN25 Register

1 CTSET2_CFG_CTOWN25 Register (Offset = AE4h) [reset = 20000000h]

Counter/Timer Ownership register 25

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Table 14-33146. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AE4h**

Figure 14-10970. CTSET2_CFG_CTOWN25 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33148. CTSET2_CFG_CTOWN25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.138 CTSET2_CFG_CTOWN26 Register

1 CTSET2_CFG_CTOWN26 Register (Offset = AE8h) [reset = 20000000h]

Counter/Timer Ownership register 26

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Table 14-33149. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AE8h**

Figure 14-10971. CTSET2_CFG_CTOWN26 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33151. CTSET2_CFG_CTOWN26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.139 CTSET2_CFG_CTOWN27 Register

1 CTSET2_CFG_CTOWN27 Register (Offset = AECh) [reset = 20000000h]

Counter/Timer Ownership register 27

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Table 14-33152. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AECh**

Figure 14-10972. CTSET2_CFG_CTOWN27 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33154. CTSET2_CFG_CTOWN27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.140 CTSET2_CFG_CTOWN28 Register

1 CTSET2_CFG_CTOWN28 Register (Offset = AF0h) [reset = 20000000h]

Counter/Timer Ownership register 28

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Table 14-33155. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AF0h**

Figure 14-10973. CTSET2_CFG_CTOWN28 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-33157. CTSET2_CFG_CTOWN28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.141 CTSET2_CFG_CTOWN29 Register

1 CTSET2_CFG_CTOWN29 Register (Offset = AF4h) [reset = 20000000h]

Counter/Timer Ownership register 29

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Table 14-33158. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AF4h**

Figure 14-10974. CTSET2_CFG_CTOWN29 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33160. CTSET2_CFG_CTOWN29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.142 CTSET2_CFG_CTOWN30 Register

1 CTSET2_CFG_CTOWN30 Register (Offset = AF8h) [reset = 20000000h]

Counter/Timer Ownership register 30

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Table 14-33161. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AF8h**

Figure 14-10975. CTSET2_CFG_CTOWN30 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-33163. CTSET2_CFG_CTOWN30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.143 CTSET2_CFG_CTOWN31 Register

1 CTSET2_CFG_CTOWN31 Register (Offset = AFCh) [reset = 20000000h]

Counter/Timer Ownership register 31

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Table 14-33164. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AFCh**

Figure 14-10976. CTSET2_CFG_CTOWN31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33166. CTSET2_CFG_CTOWN31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.144 CTSET2_CFG_CTFILT0 Register

1 CTSET2_CFG_CTFILT0 Register (Offset = B00h) [reset = 0h]

Counter Timer 0 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33167. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B00h**

Figure 14-10977. CTSET2_CFG_CTFILT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33169. CTSET2_CFG_CTFILT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.145 CTSET2_CFG_CTFILT1 Register

1 CTSET2_CFG_CTFILT1 Register (Offset = B04h) [reset = 0h]

Counter Timer 1 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33170. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B04h**

Figure 14-10978. CTSET2_CFG_CTFILT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33172. CTSET2_CFG_CTFILT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.146 CTSET2_CFG_CTFILT2 Register

1 CTSET2_CFG_CTFILT2 Register (Offset = B08h) [reset = 0h]

Counter Timer 2 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33173. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B08h**

Figure 14-10979. CTSET2_CFG_CTFILT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33175. CTSET2_CFG_CTFILT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.147 CTSET2_CFG_CTFILT3 Register

1 CTSET2_CFG_CTFILT3 Register (Offset = B0Ch) [reset = 0h]

Counter Timer 3 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33176. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B0Ch**

Figure 14-10980. CTSET2_CFG_CTFILT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33178. CTSET2_CFG_CTFILT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.148 CTSET2_CFG_CTFILT4 Register

1 CTSET2_CFG_CTFILT4 Register (Offset = B10h) [reset = 0h]

Counter Timer 4 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33179. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B10h**

Figure 14-10981. CTSET2_CFG_CTFILT4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33181. CTSET2_CFG_CTFILT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.149 CTSET2_CFG_CTFILT5 Register

1 CTSET2_CFG_CTFILT5 Register (Offset = B14h) [reset = 0h]

Counter Timer 5 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33182. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B14h**

Figure 14-10982. CTSET2_CFG_CTFILT5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33184. CTSET2_CFG_CTFILT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.150 CTSET2_CFG_CTFILT6 Register

1 CTSET2_CFG_CTFILT6 Register (Offset = B18h) [reset = 0h]

Counter Timer 6 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33185. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B18h**

Figure 14-10983. CTSET2_CFG_CTFILT6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33187. CTSET2_CFG_CTFILT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.151 CTSET2_CFG_CTFILT7 Register

1 CTSET2_CFG_CTFILT7 Register (Offset = B1Ch) [reset = 0h]

Counter Timer 7 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33188. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B1Ch

Figure 14-10984. CTSET2_CFG_CTFILT7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33190. CTSET2_CFG_CTFILT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.152 CTSET2_CFG_CTFILT8 Register

1 CTSET2_CFG_CTFILT8 Register (Offset = B20h) [reset = 0h]

Counter Timer 8 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33191. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B20h**

Figure 14-10985. CTSET2_CFG_CTFILT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33193. CTSET2_CFG_CTFILT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.153 CTSET2_CFG_CTFILT9 Register

1 CTSET2_CFG_CTFILT9 Register (Offset = B24h) [reset = 0h]

Counter Timer 9 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33194. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B24h**

Figure 14-10986. CTSET2_CFG_CTFILT9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33196. CTSET2_CFG_CTFILT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.154 CTSET2_CFG_CTFILT10 Register

1 CTSET2_CFG_CTFILT10 Register (Offset = B28h) [reset = 0h]

Counter Timer 10 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33197. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B28h**

Figure 14-10987. CTSET2_CFG_CTFILT10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33199. CTSET2_CFG_CTFILT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.155 CTSET2_CFG_CTFILT11 Register

1 CTSET2_CFG_CTFILT11 Register (Offset = B2Ch) [reset = 0h]

Counter Timer 11 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33200. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B2Ch**

Figure 14-10988. CTSET2_CFG_CTFILT11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33202. CTSET2_CFG_CTFILT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.156 CTSET2_CFG_CTFILT12 Register

1 CTSET2_CFG_CTFILT12 Register (Offset = B30h) [reset = 0h]

Counter Timer 12 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33203. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B30h

Figure 14-10989. CTSET2_CFG_CTFILT12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33205. CTSET2_CFG_CTFILT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.157 CTSET2_CFG_CTFILT13 Register

1 CTSET2_CFG_CTFILT13 Register (Offset = B34h) [reset = 0h]

Counter Timer 13 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33206. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B34h**

Figure 14-10990. CTSET2_CFG_CTFILT13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33208. CTSET2_CFG_CTFILT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.158 CTSET2_CFG_CTFILT14 Register

1 CTSET2_CFG_CTFILT14 Register (Offset = B38h) [reset = 0h]

Counter Timer 14 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33209. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B38h**

Figure 14-10991. CTSET2_CFG_CTFILT14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33211. CTSET2_CFG_CTFILT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.159 CTSET2_CFG_CTFILT15 Register

1 CTSET2_CFG_CTFILT15 Register (Offset = B3Ch) [reset = 0h]

Counter Timer 15 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33212. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B3Ch**

Figure 14-10992. CTSET2_CFG_CTFILT15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33214. CTSET2_CFG_CTFILT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.160 CTSET2_CFG_CTFILT16 Register

1 CTSET2_CFG_CTFILT16 Register (Offset = B40h) [reset = 0h]

Counter Timer 16 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33215. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B40h**

Figure 14-10993. CTSET2_CFG_CTFILT16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33217. CTSET2_CFG_CTFILT16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.161 CTSET2_CFG_CTFILT17 Register

1 CTSET2_CFG_CTFILT17 Register (Offset = B44h) [reset = 0h]

Counter Timer 17 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33218. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B44h**

Figure 14-10994. CTSET2_CFG_CTFILT17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33220. CTSET2_CFG_CTFILT17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.162 CTSET2_CFG_CTFILT18 Register

1 CTSET2_CFG_CTFILT18 Register (Offset = B48h) [reset = 0h]

Counter Timer 18 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33221. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B48h**

Figure 14-10995. CTSET2_CFG_CTFILT18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33223. CTSET2_CFG_CTFILT18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.163 CTSET2_CFG_CTFILT19 Register

1 CTSET2_CFG_CTFILT19 Register (Offset = B4Ch) [reset = 0h]

Counter Timer 19 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33224. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B4Ch**

Figure 14-10996. CTSET2_CFG_CTFILT19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33226. CTSET2_CFG_CTFILT19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.164 CTSET2_CFG_CTFILT20 Register

1 CTSET2_CFG_CTFILT20 Register (Offset = B50h) [reset = 0h]

Counter Timer 20 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33227. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B50h**

Figure 14-10997. CTSET2_CFG_CTFILT20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33229. CTSET2_CFG_CTFILT20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.165 CTSET2_CFG_CTFILT21 Register

1 CTSET2_CFG_CTFILT21 Register (Offset = B54h) [reset = 0h]

Counter Timer 21 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33230. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B54h**

Figure 14-10998. CTSET2_CFG_CTFILT21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33232. CTSET2_CFG_CTFILT21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.166 CTSET2_CFG_CTFILT22 Register

1 CTSET2_CFG_CTFILT22 Register (Offset = B58h) [reset = 0h]

Counter Timer 22 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33233. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B58h**

Figure 14-10999. CTSET2_CFG_CTFILT22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33235. CTSET2_CFG_CTFILT22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.167 CTSET2_CFG_CTFILT23 Register

1 CTSET2_CFG_CTFILT23 Register (Offset = B5Ch) [reset = 0h]

Counter Timer 23 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33236. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B5Ch**

Figure 14-11000. CTSET2_CFG_CTFILT23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33238. CTSET2_CFG_CTFILT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.168 CTSET2_CFG_CTFILT24 Register

1 CTSET2_CFG_CTFILT24 Register (Offset = B60h) [reset = 0h]

Counter Timer 24 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33239. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B60h**

Figure 14-11001. CTSET2_CFG_CTFILT24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33241. CTSET2_CFG_CTFILT24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.169 CTSET2_CFG_CTFILT25 Register

1 CTSET2_CFG_CTFILT25 Register (Offset = B64h) [reset = 0h]

Counter Timer 25 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33242. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B64h**

Figure 14-11002. CTSET2_CFG_CTFILT25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33244. CTSET2_CFG_CTFILT25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.170 CTSET2_CFG_CTFILT26 Register

1 CTSET2_CFG_CTFILT26 Register (Offset = B68h) [reset = 0h]

Counter Timer 26 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33245. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B68h**

Figure 14-11003. CTSET2_CFG_CTFILT26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33247. CTSET2_CFG_CTFILT26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.171 CTSET2_CFG_CTFILT27 Register

1 CTSET2_CFG_CTFILT27 Register (Offset = B6Ch) [reset = 0h]

Counter Timer 27 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33248. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B6Ch**

Figure 14-11004. CTSET2_CFG_CTFILT27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33250. CTSET2_CFG_CTFILT27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.172 CTSET2_CFG_CTFILT28 Register

1 CTSET2_CFG_CTFILT28 Register (Offset = B70h) [reset = 0h]

Counter Timer 28 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33251. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B70h**

Figure 14-11005. CTSET2_CFG_CTFILT28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33253. CTSET2_CFG_CTFILT28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.173 CTSET2_CFG_CTFILT29 Register

1 CTSET2_CFG_CTFILT29 Register (Offset = B74h) [reset = 0h]

Counter Timer 29 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33254. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B74h**

Figure 14-11006. CTSET2_CFG_CTFILT29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33256. CTSET2_CFG_CTFILT29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.174 CTSET2_CFG_CTFILT30 Register

1 CTSET2_CFG_CTFILT30 Register (Offset = B78h) [reset = 0h]

Counter Timer 30 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33257. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B78h**

Figure 14-11007. CTSET2_CFG_CTFILT30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33259. CTSET2_CFG_CTFILT30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.175 CTSET2_CFG_CTFILT31 Register

1 CTSET2_CFG_CTFILT31 Register (Offset = B7Ch) [reset = 0h]

Counter Timer 31 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-33260. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B7Ch**

Figure 14-11008. CTSET2_CFG_CTFILT31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33262. CTSET2_CFG_CTFILT31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.10.1.2.176 CTSET2_CFG_CTCNTR0 Register

1 CTSET2_CFG_CTCNTR0 Register (Offset = B80h) [reset = 0h]

Counter Timer Counter Register 0

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Table 14-33263. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B80h**

Figure 14-11009. CTSET2_CFG_CTCNTR0 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33265. CTSET2_CFG_CTCNTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.177 CTSET2_CFG_CTCNTR1 Register

1 CTSET2_CFG_CTCNTR1 Register (Offset = B84h) [reset = 0h]

Counter Timer Counter Register 1

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Table 14-33266. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B84h**

Figure 14-11010. CTSET2_CFG_CTCNTR1 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33268. CTSET2_CFG_CTCNTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.178 CTSET2_CFG_CTCNTR2 Register

1 CTSET2_CFG_CTCNTR2 Register (Offset = B88h) [reset = 0h]

Counter Timer Counter Register 2

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Table 14-33269. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B88h**

Figure 14-11011. CTSET2_CFG_CTCNTR2 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33271. CTSET2_CFG_CTCNTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.179 CTSET2_CFG_CTCNTR3 Register

1 CTSET2_CFG_CTCNTR3 Register (Offset = B8Ch) [reset = 0h]

Counter Timer Counter Register 3

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Table 14-33272. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B8Ch**

Figure 14-11012. CTSET2_CFG_CTCNTR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33274. CTSET2_CFG_CTCNTR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.180 CTSET2_CFG_CTCNTR4 Register

1 CTSET2_CFG_CTCNTR4 Register (Offset = B90h) [reset = 0h]

Counter Timer Counter Register 4

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Table 14-33275. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B90h**

Figure 14-11013. CTSET2_CFG_CTCNTR4 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33277. CTSET2_CFG_CTCNTR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.181 CTSET2_CFG_CTCNTR5 Register

1 CTSET2_CFG_CTCNTR5 Register (Offset = B94h) [reset = 0h]

Counter Timer Counter Register 5

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Table 14-33278. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B94h**

Figure 14-11014. CTSET2_CFG_CTCNTR5 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33280. CTSET2_CFG_CTCNTR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.182 CTSET2_CFG_CTCNTR6 Register

1 CTSET2_CFG_CTCNTR6 Register (Offset = B98h) [reset = 0h]

Counter Timer Counter Register 6

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Table 14-33281. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B98h**

Figure 14-11015. CTSET2_CFG_CTCNTR6 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33283. CTSET2_CFG_CTCNTR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.183 CTSET2_CFG_CTCNTR7 Register

1 CTSET2_CFG_CTCNTR7 Register (Offset = B9Ch) [reset = 0h]

Counter Timer Counter Register 7

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Table 14-33284. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B9Ch**

Figure 14-11016. CTSET2_CFG_CTCNTR7 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33286. CTSET2_CFG_CTCNTR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.184 CTSET2_CFG_CTCNTR8 Register

1 CTSET2_CFG_CTCNTR8 Register (Offset = BA0h) [reset = 0h]

Counter Timer Counter Register 8

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Table 14-33287. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA0h**

Figure 14-11017. CTSET2_CFG_CTCNTR8 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33289. CTSET2_CFG_CTCNTR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.185 CTSET2_CFG_CTCNTR9 Register

1 CTSET2_CFG_CTCNTR9 Register (Offset = BA4h) [reset = 0h]

Counter Timer Counter Register 9

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Table 14-33290. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA4h**

Figure 14-11018. CTSET2_CFG_CTCNTR9 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33292. CTSET2_CFG_CTCNTR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.186 CTSET2_CFG_CTCNTR10 Register

1 CTSET2_CFG_CTCNTR10 Register (Offset = BA8h) [reset = 0h]

Counter Timer Counter Register 10

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Table 14-33293. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA8h**

Figure 14-11019. CTSET2_CFG_CTCNTR10 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33295. CTSET2_CFG_CTCNTR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.187 CTSET2_CFG_CTCNTR11 Register

1 CTSET2_CFG_CTCNTR11 Register (Offset = BACh) [reset = 0h]

Counter Timer Counter Register 11

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Table 14-33296. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BACh**

Figure 14-11020. CTSET2_CFG_CTCNTR11 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33298. CTSET2_CFG_CTCNTR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.188 CTSET2_CFG_CTCNTR12 Register

1 CTSET2_CFG_CTCNTR12 Register (Offset = BB0h) [reset = 0h]

Counter Timer Counter Register 12

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Table 14-33299. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB0h**

Figure 14-11021. CTSET2_CFG_CTCNTR12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33301. CTSET2_CFG_CTCNTR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.189 CTSET2_CFG_CTCNTR13 Register

1 CTSET2_CFG_CTCNTR13 Register (Offset = BB4h) [reset = 0h]

Counter Timer Counter Register 13

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Table 14-33302. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB4h**

Figure 14-11022. CTSET2_CFG_CTCNTR13 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33304. CTSET2_CFG_CTCNTR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.190 CTSET2_CFG_CTCNTR14 Register

1 CTSET2_CFG_CTCNTR14 Register (Offset = BB8h) [reset = 0h]

Counter Timer Counter Register 14

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Table 14-33305. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB8h**

Figure 14-11023. CTSET2_CFG_CTCNTR14 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33307. CTSET2_CFG_CTCNTR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.191 CTSET2_CFG_CTCNTR15 Register

1 CTSET2_CFG_CTCNTR15 Register (Offset = BBCh) [reset = 0h]

Counter Timer Counter Register 15

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Table 14-33308. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BBCh**

Figure 14-11024. CTSET2_CFG_CTCNTR15 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33310. CTSET2_CFG_CTCNTR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.192 CTSET2_CFG_CTCNTR16 Register

1 CTSET2_CFG_CTCNTR16 Register (Offset = BC0h) [reset = 0h]

Counter Timer Counter Register 16

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Table 14-33311. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC0h**

Figure 14-11025. CTSET2_CFG_CTCNTR16 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33313. CTSET2_CFG_CTCNTR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.193 CTSET2_CFG_CTCNTR17 Register

1 CTSET2_CFG_CTCNTR17 Register (Offset = BC4h) [reset = 0h]

Counter Timer Counter Register 17

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Table 14-33314. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC4h**

Figure 14-11026. CTSET2_CFG_CTCNTR17 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33316. CTSET2_CFG_CTCNTR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.194 CTSET2_CFG_CTCNTR18 Register

1 CTSET2_CFG_CTCNTR18 Register (Offset = BC8h) [reset = 0h]

Counter Timer Counter Register 18

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Table 14-33317. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC8h**

Figure 14-11027. CTSET2_CFG_CTCNTR18 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33319. CTSET2_CFG_CTCNTR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.195 CTSET2_CFG_CTCNTR19 Register

1 CTSET2_CFG_CTCNTR19 Register (Offset = BCCh) [reset = 0h]

Counter Timer Counter Register 19

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Table 14-33320. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BCCh**

Figure 14-11028. CTSET2_CFG_CTCNTR19 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33322. CTSET2_CFG_CTCNTR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.196 CTSET2_CFG_CTCNTR20 Register

1 CTSET2_CFG_CTCNTR20 Register (Offset = BD0h) [reset = 0h]

Counter Timer Counter Register 20

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Table 14-33323. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD0h**

Figure 14-11029. CTSET2_CFG_CTCNTR20 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33325. CTSET2_CFG_CTCNTR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.197 CTSET2_CFG_CTCNTR21 Register

1 CTSET2_CFG_CTCNTR21 Register (Offset = BD4h) [reset = 0h]

Counter Timer Counter Register 21

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Table 14-33326. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD4h**

Figure 14-11030. CTSET2_CFG_CTCNTR21 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33328. CTSET2_CFG_CTCNTR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.198 CTSET2_CFG_CTCNTR22 Register

1 CTSET2_CFG_CTCNTR22 Register (Offset = BD8h) [reset = 0h]

Counter Timer Counter Register 22

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Table 14-33329. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD8h**

Figure 14-11031. CTSET2_CFG_CTCNTR22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33331. CTSET2_CFG_CTCNTR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.199 CTSET2_CFG_CTCNTR23 Register

1 CTSET2_CFG_CTCNTR23 Register (Offset = BDCh) [reset = 0h]

Counter Timer Counter Register 23

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Table 14-33332. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BDCh**

Figure 14-11032. CTSET2_CFG_CTCNTR23 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33334. CTSET2_CFG_CTCNTR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.200 CTSET2_CFG_CTCNTR24 Register

1 CTSET2_CFG_CTCNTR24 Register (Offset = BE0h) [reset = 0h]

Counter Timer Counter Register 24

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Table 14-33335. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE0h**

Figure 14-11033. CTSET2_CFG_CTCNTR24 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33337. CTSET2_CFG_CTCNTR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.201 CTSET2_CFG_CTCNTR25 Register

1 CTSET2_CFG_CTCNTR25 Register (Offset = BE4h) [reset = 0h]

Counter Timer Counter Register 25

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Table 14-33338. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE4h**

Figure 14-11034. CTSET2_CFG_CTCNTR25 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33340. CTSET2_CFG_CTCNTR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.202 CTSET2_CFG_CTCNTR26 Register

1 CTSET2_CFG_CTCNTR26 Register (Offset = BE8h) [reset = 0h]

Counter Timer Counter Register 26

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Table 14-33341. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE8h**

Figure 14-11035. CTSET2_CFG_CTCNTR26 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33343. CTSET2_CFG_CTCNTR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.203 CTSET2_CFG_CTCNTR27 Register

1 CTSET2_CFG_CTCNTR27 Register (Offset = BECh) [reset = 0h]

Counter Timer Counter Register 27

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Table 14-33344. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BECh**

Figure 14-11036. CTSET2_CFG_CTCNTR27 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33346. CTSET2_CFG_CTCNTR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.204 CTSET2_CFG_CTCNTR28 Register

1 CTSET2_CFG_CTCNTR28 Register (Offset = BF0h) [reset = 0h]

Counter Timer Counter Register 28

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Table 14-33347. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF0h**

Figure 14-11037. CTSET2_CFG_CTCNTR28 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33349. CTSET2_CFG_CTCNTR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.205 CTSET2_CFG_CTCNTR29 Register

1 CTSET2_CFG_CTCNTR29 Register (Offset = BF4h) [reset = 0h]

Counter Timer Counter Register 29

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Table 14-33350. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF4h**

Figure 14-11038. CTSET2_CFG_CTCNTR29 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33352. CTSET2_CFG_CTCNTR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.206 CTSET2_CFG_CTCNTR30 Register

1 CTSET2_CFG_CTCNTR30 Register (Offset = BF8h) [reset = 0h]

Counter Timer Counter Register 30

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Table 14-33353. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF8h**

Figure 14-11039. CTSET2_CFG_CTCNTR30 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33355. CTSET2_CFG_CTCNTR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.207 CTSET2_CFG_CTCNTR31 Register

1 CTSET2_CFG_CTCNTR31 Register (Offset = BFCh) [reset = 0h]

Counter Timer Counter Register 31

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Table 14-33356. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BFCh**

Figure 14-11040. CTSET2_CFG_CTCNTR31 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-33358. CTSET2_CFG_CTCNTR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.10.1.2.208 CTSET2_CFG_CT_EOI Register

1 CTSET2_CFG_CT_EOI Register (Offset = C00h) [reset = 0h]

Counter Timer EOI Register. This register is the End of Interrupt used by SW to signal HW that an interrupt event service is complete and an interrupt can be rearmed. This register exists only if NUMTIMR > 0

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Table 14-33359. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C00h**

Figure 14-11041. CTSET2_CFG_CT_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI
R							R/W
0h							0h

Table 14-33361. CTSET2_CFG_CT_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	EOI	R/W	0h	EOI value

14.10.1.2.209 CTSET2_CFG_CTIRQSTAT_RAW Register

1 CTSET2_CFG_CTIRQSTAT_RAW Register (Offset = C04h) [reset = 0h]

Counter Timer IRQSTATUS RAW Register. This register indicates the raw status of the interrupt. It can be written by SW for testing. This register exists only if NUMTIMR > 0

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Table 14-33362. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C04h**

Figure 14-11042. CTSET2_CFG_CTIRQSTAT_RAW Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IRQ							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IRQ							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IRQ							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IRQ							
R/W							
0h							

Table 14-33364. CTSET2_CFG_CTIRQSTAT_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IRQ	R/W	0h	IRQSTATUS_RAW value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.10.1.2.210 CTSET2_CFG_CTIRQSTAT Register

1 CTSET2_CFG_CTIRQSTAT Register (Offset = C08h) [reset = 0h]

Counter Timer IRQSTATUS Register. This bit clears the interrupt event. SW can also read this bit to indicate that the interrupt is active and enabled. This register exists only if NUMTIMR > 0

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Table 14-33365. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C08h**

Figure 14-11043. CTSET2_CFG_CTIRQSTAT Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IE							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IE							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IE							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IE							
R/W							
0h							

Table 14-33367. CTSET2_CFG_CTIRQSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IE	R/W	0h	IRQSTATUS value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.10.1.2.211 CTSET2_CFG_CTIRQENABLE_SET Register

1 CTSET2_CFG_CTIRQENABLE_SET Register (Offset = C0Ch) [reset = 0h]

Counter Timer IRQENABLE_SET Register. This register is to enable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-33368. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C0Ch**

Figure 14-11044. CTSET2_CFG_CTIRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IES							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IES							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IES							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IES							
R/W							
0h							

Table 14-33370. CTSET2_CFG_CTIRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IES	R/W	0h	IRQSET value. This bit sets the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.10.1.2.212 CTSET2_CFG_CTIRQENABLE_CLR Register

1 CTSET2_CFG_CTIRQENABLE_CLR Register (Offset = C10h) [reset = 0h]

Counter Timer IRQENABLE_CLR Register. This register is to disable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-33371. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C10h**

Figure 14-11045. CTSET2_CFG_CTIRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IEC							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IEC							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IEC							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IEC							
R/W							
0h							

Table 14-33373. CTSET2_CFG_CTIRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IEC	R/W	0h	IRQCLR value. This bit clears the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.10.1.2.213 CTSET2_CFG_STPTCR Register

1 CTSET2_CFG_STPTCR Register (Offset = 1800h) [reset = 4h]

STP Trace Control Register

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Table 14-33374. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3800h**

Figure 14-11046. CTSET2_CFG_STPTCR Name Register

31	30	29	28	27	26	25	24
RESERVED3							MOD_FIFOFULL
R							R
0h							0h
23	22	21	20	19	18	17	16
DATA_FIFOFULL	RESERVED2						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED2		COMPEN	RESERVED1		SYNCEN	TSEN	RESERVED
R		R/W	R		R	R/W	R
0h		0h	0h		1h	0h	0h

Table 14-33376. CTSET2_CFG_STPTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED3	R	0h	Reserved, returns 0
24	MOD_FIFOFULL	R	0h	STPMI2ATB internal MID packet fifo is full
23	DATA_FIFOFULL	R	0h	STPMI2ATB internal Data packet fifo is full
22:6	RESERVED2	R	0h	Reserved, returns 0
5	COMPEN	R/W	0h	Compression of Data enable
4:3	RESERVED1	R	0h	Reserved, returns 0
2	SYNCEN	R	1h	The value 1 indicates STPASYNC is supported
1	TSEN	R/W	0h	Timestamp Enable. This bit is static and should not be changed dynamically. This should be changed before client is enabled.
0	RESERVED	R	0h	Reserved, returns 0

14.10.1.2.214 CTSET2_CFG_STPTID Register

1 CTSET2_CFG_STPTID Register (Offset = 1804h) [reset = 0h]

STP Trace ID Register

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Table 14-33377. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3804h**

Figure 14-11047. CTSET2_CFG_STPTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	TRACEID						
R	R/W						
0h	0h						

Table 14-33379. CTSET2_CFG_STPTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6:0	TRACEID	R/W	0h	Trace ID value. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.10.1.2.215 CTSET2_CFG_STPASYNC Register

1 CTSET2_CFG_STPASYNC Register (Offset = 1810h) [reset = 130Ch]

STP Synchronization Control Register

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Table 14-33380. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3810h**

Figure 14-11048. CTSET2_CFG_STPASYNC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>EXPMODE</td><td colspan="4">COUNT</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>1h</td><td colspan="4">30Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">30Ch</td></tr>
</table>

Table 14-33382. CTSET2_CFG_STPASYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R	0h	Reserved, returns 0
12	EXPMODE	R/W	1h	Exponent mode, A value of 1 sets count to 2 to the Nth, where Nth is ((bits 11 : 8)+12). A value of 0 sets Count to N (bits 11 : 0)
11:0	COUNT	R/W	30Ch	The number of bytes between Synchronization packets

14.10.1.2.216 CTSET2_CFG_STPFFCR Register

1 CTSET2_CFG_STPFFCR Register (Offset = 1814h) [reset = 0h]

STP Flush Control Register

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Table 14-33383. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3814h**

Figure 14-11049. CTSET2_CFG_STPFFCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1		FORCEFLUSH	RESERVED			ASYNCPE	AUTOFLUSH
R		R/W	R			R/W	R/W
0h		0h	0h			0h	0h

Table 14-33385. CTSET2_CFG_STPFFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R	0h	Reserved, returns 0
5	FORCEFLUSH	R/W	0h	Write a 1 to force a flush, automatically clears after the operation is complete
4:2	RESERVED	R	0h	Reserved, returns 0
1	ASYNCPE	R/W	0h	Async Priority Enable. 0 indicates ASYNC packet priority is lower than trace. 1 indicates priority escalates on second synchronization request
0	AUTOFLUSH	R/W	0h	Auto flush enable. When set, on every complete data (ATDATA : WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This should be written before client IP enabled

14.10.1.2.217 CTSET2_CFG_STPFEAT1 Register

1 CTSET2_CFG_STPFEAT1 Register (Offset = 1818h) [reset = 21h]

STP Features 1 Register

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Table 14-33386. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3818h**

Figure 14-11050. CTSET2_CFG_STPFEAT1 Name Register

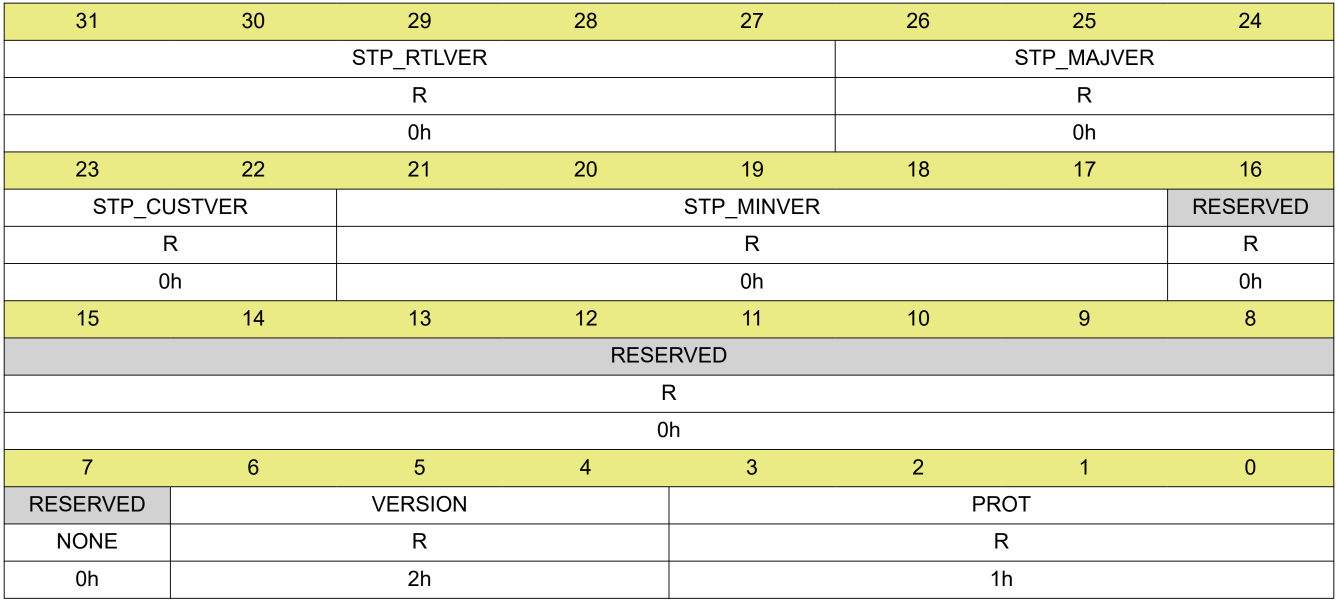

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">STP_RTLVER</td><td colspan="3">STP_MAJVER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">STP_CUSTVER</td><td colspan="5">STP_MINVER</td><td>RESERVED</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">VERSION</td><td colspan="4">PROT</td></tr>
<tr><td>NONE</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">2h</td><td colspan="4">1h</td></tr>
</table>

Table 14-33388. CTSET2_CFG_STPFEAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	STP_RTLVER	R	0h	RTL Version. Reset each time major or minor version is updated
26:24	STP_MAJVER	R	0h	Functional Major Version. This is the first version of STPMI2ATB
23:22	STP_CUSTVER	R	0h	Custom Version (not used)
21:17	STP_MINVER	R	0h	Functional Minor Version
16:8	RESERVED	R	0h	Reserved, returns 0
7	RESERVED	NONE	0h	Reserved
6:4	VERSION	R	2h	STP2.0 Time Stamp, Value of 011 indicates Natural binary timestamp, a value of 100 indicates gray binary timestamps
3:0	PROT	R	1h	Protocol Revision. Value of 0001 indicates STP 2.0

14.10.1.2.218 CXATBREPLICATOR_CFG_IDFILTER0 Register

1 CXATBREPLICATOR_CFG_IDFILTER0 Register (Offset = 0h) [reset = 0h]

Allows the setting of ID filter for Initiator 0.

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Table 14-33389. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4000h**

Figure 14-11051. CXATBREPLICATOR_CFG_IDFILTER0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ID0_70_7F	ID0_60_6F	ID0_50_5F	ID0_40_4F	ID0_30_3F	ID0_20_2F	ID0_10_1F	ID0_0_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-33391. CXATBREPLICATOR_CFG_IDFILTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ID0_70_7F	R/W	0h	Enable or disable ID filtering for id's 0x70 to 0x7F
6	ID0_60_6F	R/W	0h	Enable or disable ID filtering for id's 0x60 to 0x6F
5	ID0_50_5F	R/W	0h	Enable or disable ID filtering for id's 0x50 to 0x5F
4	ID0_40_4F	R/W	0h	Enable or disable ID filtering for id's 0x40 to 0x4F
3	ID0_30_3F	R/W	0h	Enable or disable ID filtering for id's 0x30 to 0x3F
2	ID0_20_2F	R/W	0h	Enable or disable ID filtering for id's 0x20 to 0x2F
1	ID0_10_1F	R/W	0h	Enable or disable ID filtering for id's 0x10 to 0x1F
0	ID0_0_F	R/W	0h	Enable or disable ID filtering for id's 0x0 to 0xF

14.10.1.2.219 CXATBREPLICATOR_CFG_IDFILTER1 Register

1 CXATBREPLICATOR_CFG_IDFILTER1 Register (Offset = 4h) [reset = 0h]

Allows the setting of ID filter for Initiator 1.

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Table 14-33392. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4004h**

Figure 14-11052. CXATBREPLICATOR_CFG_IDFILTER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ID1_70_7F</td><td>ID1_60_6F</td><td>ID1_50_5F</td><td>ID1_40_4F</td><td>ID1_30_3F</td><td>ID1_20_2F</td><td>ID1_10_1F</td><td>ID1_0_F</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33394. CXATBREPLICATOR_CFG_IDFILTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ID1_70_7F	R/W	0h	Enable or disable ID filtering for id's 0x70 to 0x7F
6	ID1_60_6F	R/W	0h	Enable or disable ID filtering for id's 0x60 to 0x6F
5	ID1_50_5F	R/W	0h	Enable or disable ID filtering for id's 0x50 to 0x5F
4	ID1_40_4F	R/W	0h	Enable or disable ID filtering for id's 0x40 to 0x4F
3	ID1_30_3F	R/W	0h	Enable or disable ID filtering for id's 0x30 to 0x3F
2	ID1_20_2F	R/W	0h	Enable or disable ID filtering for id's 0x20 to 0x2F
1	ID1_10_1F	R/W	0h	Enable or disable ID filtering for id's 0x10 to 0x1F
0	ID1_0_F	R/W	0h	Enable or disable ID filtering for id's 0x0 to 0xF

14.10.1.2.220 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR1 Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR1 Register (Offset = EF8h) [reset = 0h]

Returns the value of the ATREADYM0, ATREADYM1 and ATVALIDS inputs in integration mode.

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Table 14-33395. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4EF8h**

Figure 14-11053. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATVALIDS_R	RESERVED	ATREADYM1_R	ATREADYM0_R
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-33397. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ATVALIDS_R	R	0h	Reads the value of the ATVALIDS input :
2	RESERVED	NONE	0h	Reserved
1	ATREADYM1_R	R	0h	Reads the value of the ATREADYM1 input :
0	ATREADYM0_R	R	0h	Reads the value of the ATREADYM0 input :

14.10.1.2.221 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR0 Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR0 Register (Offset = EFCh) [reset = 0h]

Controls the value of the ATVALIDM0, ATVALIDM1 and ATREADYS outputs in integration mode.

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Table 14-33398. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4EFCh**

Figure 14-11054. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>ATREADYS_W</td><td>RESERVED</td><td>ATVALIDM1_W</td><td>RESERVED</td><td>ATVALIDM0_W</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td>R/W</td><td>NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-33400. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	ATREADYS_W	R/W	0h	Sets the value of the ATREADYS output :
3	RESERVED	NONE	0h	Reserved
2	ATVALIDM1_W	R/W	0h	Sets the value of the ATVALIDM1 output :
1	RESERVED	NONE	0h	Reserved
0	ATVALIDM0_W	R/W	0h	Sets the value of the ATVALIDM0 output :

14.10.1.2.222 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITCTRL Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITCTRL Register (Offset = F00h) [reset = 0h]

Used to enable topology detection. See the CoreSight Architecture Specification for more information. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving. p/ > Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-33401. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4F00h**

Figure 14-11055. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-33403. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Enables the component to switch from functional mode to integration mode and back. If no integration functionality is implemented, this register must read as zero.

14.10.1.2.223 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMSET Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMSET Register (Offset = FA0h) [reset = Fh]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-33404. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FA0h**

Figure 14-11056. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				Fh			

Table 14-33406. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	Fh	This claim tag bit is implemented

14.10.1.2.224 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMCLR Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-33407. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FA4h**

Figure 14-11057. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-33409. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.225 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LAR Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers.

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Table 14-33410. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FB0h**

Figure 14-11058. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-33412. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. An invalid write has the affect of removing write access.

14.10.1.2.226 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LSR Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register, 0xFB0.

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Table 14-33413. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 4FB4h**

Figure 14-11059. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-33415. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register, 0xFB0, is implemented as 8-bit or 32-bit.
1	LOCKGRANT	R	1h	Returns the current status of the Lock.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device.

14.10.1.2.227 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_AUTHSTATUS Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register

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Table 14-33416. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FB8h**

Figure 14-11060. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		0h		0h	

Table 14-33418. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	0h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	0h	Indicates the security level for non-secure invasive debug

14.10.1.2.228 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVID Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVID Register (Offset = FC8h) [reset = 2h]

Indicates the capabilities of the CoreSight Replicator.

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Table 14-33419. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FC8h**

Figure 14-11061. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PORTNUM			
NONE				R			
0h				2h			

Table 14-33421. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PORTNUM	R	2h	This value indicates the number of initiator ports implemented.

14.10.1.2.229 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVTYPE Register

1 CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVTYPE Register (Offset = FCCh) [reset = 22h]

Provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-33422. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FCCh**

Figure 14-11062. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
2h				2h			

Table 14-33424. CXATBREPLICATOR_CFG_CXATBREPLICATOR_REGISTERS_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	2h	Sub-classification within the major category :
3:0	MAJOR_TYPE	R	2h	Major classification grouping for this debug or trace component :

14.10.1.2.230 CXATBREPLICATOR_CFG_PIDR4 Register

1 CXATBREPLICATOR_CFG_PIDR4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-33425. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FD0h**

Figure 14-11063. CXATBREPLICATOR_CFG_PIDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FOURKB_COUNT				JEP106_CONT			
R				R			
0h				4h			

Table 14-33427. CXATBREPLICATOR_CFG_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	FOURKB_COUNT	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB, this must read as 0x0, 4KB only. For 8KB set to 0x1, for 16KB set to 0x2, for 32KB set to 0x3, and so on.
3:0	JEP106_CONT	R	4h	JEDEC continuation code indicating the designer of the component, together with the identity code.

14.10.1.2.231 CXATBREPLICATOR_CFG_PIDR0 Register

1 CXATBREPLICATOR_CFG_PIDR0 Register (Offset = FE0h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-33428. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FE0h**

Figure 14-11064. CXATBREPLICATOR_CFG_PIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_NUMBER_BITS7TO0							
R							
9h							

Table 14-33430. CXATBREPLICATOR_CFG_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_NUMBER_BITS7TO0	R	9h	Bits [7 : 0] of the component part number. This is selected by the designer of the component.

14.10.1.2.232 CXATBREPLICATOR_CFG_PIDR1 Register

1 CXATBREPLICATOR_CFG_PIDR1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-33431. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FE4h**

Figure 14-11065. CXATBREPLICATOR_CFG_PIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
JEP106_BITS3TO0				PART_NUMBER_BITS11TO8			
R				R			
0h				9h			

Table 14-33433. CXATBREPLICATOR_CFG_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	JEP106_BITS3TO0	R	0h	Bits [3 : 0] of the JEDEC identity code indicating the designer of the component, together with the continuation code.
3:0	PART_NUMBER_BITS11TO8	R	9h	Bits [11 : 8] of the component part number. This is selected by the designer of the component.

14.10.1.2.233 CXATBREPLICATOR_CFG_PIDR2 Register

1 CXATBREPLICATOR_CFG_PIDR2 Register (Offset = FE8h) [reset = 18h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-33434. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FE8h**

Figure 14-11066. CXATBREPLICATOR_CFG_PIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	JEP106_BITS6TO4		
R				R	R		
1h				1h	0h		

Table 14-33436. CXATBREPLICATOR_CFG_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	1h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is used as a look-up to establish the exact major and minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used.
2:0	JEP106_BITS6TO4	R	0h	Bits [6 : 4] of the JEDEC identity code indicating the designer of the component, together with the continuation code.

14.10.1.2.234 CXATBREPLICATOR_CFG_PIDR3 Register

1 CXATBREPLICATOR_CFG_PIDR3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-33437. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FECh**

Figure 14-11067. CXATBREPLICATOR_CFG_PIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CUSTOMER_MODIFIED			
R				R			
0h				0h			

Table 14-33439. CXATBREPLICATOR_CFG_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CUSTOMER_MODIFIED	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.235 CXATBREPLICATOR_CFG_CIDR0 Register

1 CXATBREPLICATOR_CFG_CIDR0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-33440. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF0h**

Figure 14-11068. CXATBREPLICATOR_CFG_CIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
Dh							

Table 14-33442. CXATBREPLICATOR_CFG_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	Dh	Contains bits [24 : 31] of the component identification.

14.10.1.2.236 CXATBREPLICATOR_CFG_CIDR1 Register

1 CXATBREPLICATOR_CFG_CIDR1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-33443. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF4h**

Figure 14-11069. CXATBREPLICATOR_CFG_CIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PREAMBLE			
R				R			
9h				0h			

Table 14-33445. CXATBREPLICATOR_CFG_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component, for example, ROM table or CoreSight component.
3:0	PREAMBLE	R	0h	Contains bits [19 : 16] of the component identification.

14.10.1.2.237 CXATBREPLICATOR_CFG_CIDR2 Register

1 CXATBREPLICATOR_CFG_CIDR2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33446. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF8h**

Figure 14-11070. CXATBREPLICATOR_CFG_CIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
5h							

Table 14-33448. CXATBREPLICATOR_CFG_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	5h	Contains bits [15 : 8] of the component identification.

14.10.1.2.238 CXATBREPLICATOR_CFG_CIDR3 Register

1 CXATBREPLICATOR_CFG_CIDR3 Register (Offset = FFCh) [reset = B1h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33449. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FFCh**

Figure 14-11071. CXATBREPLICATOR_CFG_CIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
B1h							

Table 14-33451. CXATBREPLICATOR_CFG_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	B1h	Contains bits [7 : 0] of the component identification.

14.10.1.2.239 CT_TBR_CT_TBR_RAMSZ Register

1 CT_TBR_CT_TBR_RAMSZ Register (Offset = 4h) [reset = 0h]

CT-TBR RAM Size Register This register indicates the size of the local memory buffer interfaced with the CT-TBR This register can be used to determine if the CT_TBR is synthesized for System Bridge Mode only. It will read 0x00000000 in this configuration.

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Table 14-33452. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5004h**

Figure 14-11072. CT_TBR_CT_TBR_RAMSZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					RAM_SIZE		
R					R		
0h					0h		

Table 14-33454. CT_TBR_CT_TBR_RAMSZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2:0	RAM_SIZE	R	0h	Indicates the size of the local memory1 Read 0x0 : No local buffer. TBR Bridge only configuration Read 0x1 : 4K bytes Read 0x2 : 8K bytes Read 0x3 : 16K bytes Read 0x4 : 32K bytes Read 0x5 : 64K bytes Read 0x6 : 128K bytes Read 0x7 : Reserved

14.10.1.2.240 CT_TBR_CT_TBR_FIFOSZ Register

1 CT_TBR_CT_TBR_FIFOSZ Register (Offset = 8h) [reset = 0h]

CT-TBR Output FIFO Size Register This register indicates the size of output FIFO used to transfer data to the system target interface

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Table 14-33455. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5008h**

Figure 14-11073. CT_TBR_CT_TBR_FIFOSZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					FIFO_SIZE		
R					R		
0h					0h		

Table 14-33457. CT_TBR_CT_TBR_FIFOSZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2:0	FIFO_SIZE	R	0h	Indicates the size of the output FIFO Read 0x0 : 128 bytes Read 0x1 : 256 bytes Read 0x2 : 512 bytes Read 0x3 : 1024 bytes Read 0x4 : 2048 bytes Read 0x5-0x7 : Reserved

14.10.1.2.241 CT_TBR_CT_TBR_STAT Register

1 CT_TBR_CT_TBR_STAT Register (Offset = Ch) [reset = 28h]

TBR Status Register This register indicates status of various functions performed by CT-TBR

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Table 14-33458. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 500Ch**

Figure 14-11074. CT_TBR_CT_TBR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESET_OUT	PARTIAL_OUT	DRAIN_DONE	FMT_DONE	CPT_DONE	TRIG	WRAP
R	R	R	R	R	R	R	R
0h	0h	1h	0h	1h	0h	0h	0h

Table 14-33460. CT_TBR_CT_TBR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	
6	RESET_OUT	R	0h	Reset Active bit indicates that at least one of the domains in the CT-TBR is currently being held in reset. Read 0b : All domains and/or interfaces of the CT-TBR are out of reset Read 1b : At least one of the domains and/or interfaces of the CT-TBR are being held in reset
5	PARTIAL_OUT	R	1h	Indicates that a partial output block (0 < Level < Trigger Threshold) is in the TBR memory (output buffer and possibly local RAM) and that an OUTFLUSH sequence may be required since there is no valid data to available to increase the amount of data past the OUTLVL threshold (i.e. local RAM buffer is empty). This bit is not set if the partial output block is the result of currently active block read request (i.e. it is already actively draining). This bit is only valid in System Bridge Mode. Read 0b : A partial frame does not exist or there is pending data in the local data RAMs that might complete any partial output blocks. Read 1b : A partial output block is in the buffer and there is not valid data available to push this through the system without an OUTFLUSH. Enabling acquisition (CTRL : ENBL 0- > 1) resets the output FIFO pointers and RAM pointers, so this bit will be set to 0 each time acquisition is enabled.

Table 14-33460. CT_TBR_CT_TBR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DRAIN_DONE	R	0h	Indicates the whether there is data in the output FIFO. This bit is only valid in System Bridge Mode. Read 0b : There is still valid data in the CT-TBR output FIFO Read 1b : All valid data in the CT-TBR output FIFO has been transferred via the system interface. Enabling acquisition (CTRL : ENBL 0- > 1) resets the output FIFO pointers, so this bit will be set to 0 each time acquisition is enabled.
3	FMT_DONE	R	1h	Indicates that all pending local memory transactions from the formatter are complete and no more data will be posted from the formatter. Read 0b : Data may still be pending Read 1b : Final data from the formatter has been posted. This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
2	CPT_DONE	R	0h	Indicates that ATB interface is disabled and trace data capture is complete. Read 0b : Trace capture still active Read 1b : Trace capture complete This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
1	TRIG	R	0h	Indicates that the local memory buffer has been locked as the result of a trigger. This bit is only valid in Buffer Mode and will always read 0 in System Bridge mode Read 0b : No trigger seen. Read 1b : Trigger input detected and buffer locked This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
0	WRAP	R	0h	This bit is active in buffer mode only and is not present in CT-TBR configurations that only support System bridge mode Indicates that the local memory write pointer has incremented past the upper boundary of the memory reset to the lowest address (at least once). Read 0b : No wrap Read 1b : Write pointer has wrapped This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b

14.10.1.2.242 CT_TBR_CT_TBR_RAMRDAT Register

1 CT_TBR_CT_TBR_RAMRDAT Register (Offset = 10h) [reset = 0h]

RAM Read Data Register This register is used to transfer data from the local memory to client This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-33461. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5010h**

Figure 14-11075. CT_TBR_CT_TBR_RAMRDAT Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-33463. CT_TBR_CT_TBR_RAMRDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The 32-bit data value pointed to by the RAMRPTR register Reading returns the value at the index specified by RAMRPTR. RAMRPTR is then incremented automatically.

14.10.1.2.243 CT_TBR_CT_TBR_RAMRPTR Register

1 CT_TBR_CT_TBR_RAMRPTR Register (Offset = 14h) [reset = 0h]

RAM Read Pointer Register Indexes into the local memory for reading 32-bit values via RAMRDAT This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-33464. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5014h**

Figure 14-11076. CT_TBR_CT_TBR_RAMRPTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PTR					
R/W		R/W					
0h		0h					
15	14	13	12	11	10	9	8
PTR							
R/W							
0h							
7	6	5	4	3	2	1	0
PTR							
R/W							
0h							

Table 14-33466. CT_TBR_CT_TBR_RAMRPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	R/W	0h	
21:0	PTR	R/W	0h	This field designates the index of the 32-bit RAM location to be read via RAMRDAT. Read returns the current value of the pointer Write sets the value and initiates a read from the designated address. This field increments automatically when a value is read from RAMRDAT. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

14.10.1.2.244 CT_TBR_CT_TBR_RAMWPTR Register

1 CT_TBR_CT_TBR_RAMWPTR Register (Offset = 18h) [reset = 0h]

This field designates the index of the 32-bit RAM location to be written via RAMWDAT. Read : Returns the current value of the pointer Write : Sets the value Writes will always force the bits 1 : 0 of write_value to 0. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

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Table 14-33467. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5018h**

Figure 14-11077. CT_TBR_CT_TBR_RAMWPTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PTR					
R/W		R/W					
0h		0h					
15	14	13	12	11	10	9	8
PTR							
R/W							
0h							
7	6	5	4	3	2	1	0
PTR							
R/W							
0h							

Table 14-33469. CT_TBR_CT_TBR_RAMWPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	R/W	0h	
21:0	PTR	R/W	0h	This field designates the index of the 32-bit RAM location to be read via RAMRDAT. Read returns the current value of the pointer Write sets the value and initiates a read from the designated address. This field increments automatically when a value is read from RAMRDAT. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

14.10.1.2.245 CT_TBR_CT_TBR_TRGCNT Register

1 CT_TBR_CT_TBR_TRGCNT Register (Offset = 1Ch) [reset = 0h]

Trigger Count Register This register controls the amount of data written to the local memory after a trigger input is detected

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Table 14-33470. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 501Ch**

Figure 14-11078. CT_TBR_CT_TBR_TRGCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED			COUNT				
R/W			R/W				
0h			0h				
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-33472. CT_TBR_CT_TBR_TRGCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R/W	0h	
12:0	COUNT	R/W	0h	Controls the number of 128-bit words written to local memory after a trigger input is detected on the CTI interface. When the input trigger is active and a trigger is detected, an internal register starts counting the number of 128-bit words written to local memory. When that counter equals COUNT + 1, the memory is locked and the CAPT_DONE and the TRIG bits in the STAT register are set. - Setting COUNT to a low index will lock trace that occurred before the trigger - Setting COUNT to a high index will lock trace that occurred after the trigger - Setting COUNT to an intermediate index will lock trace that occurred around the trigger Read : Returns the current configured value of the trigger counter Write : Sets a new value. This register can be read at any time but can only be written when acquisition is disabled in CNTL. The internal count register is not visible to the application, but it is reset cleared by hardware when the CTRL'ENBL bit transitions from 0 to 1. The width of the COUNT field is actually log2(RAM size in Bytes / 16) When configured for System Bridge only, the COUNT field is fixed a 10-bits (9 : 0). This allows the CT-TBR to capture and forward up to 1024 frames of data after the trigger event.

14.10.1.2.246 CT_TBR_CT_TBR_CTRL Register

1 CT_TBR_CT_TBR_CTRL Register (Offset = 20h) [reset = 0h]

CT-TBR Control Register This register controls the global enable/disable functions of the CT-TBR

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Table 14-33473. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5020h**

Figure 14-11079. CT_TBR_CT_TBR_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			IDLE_EMPTY	SYNCREQ_WRAP	SRST	MODE	ENBL
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-33475. CT_TBR_CT_TBR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R/W	0h	
4	IDLE_EMPTY	R/W	0h	Controls whether the CT_TBR can enter idle with data present Read 0x0 : All internal buffers must be empty before idle requests are acknowledged Read 0x1 : CT_TBR can idle with valid data Write 0x0 : Clear idle with valid data Write 0x1 : Set idle with valid data
3	SYNCREQ_WRAP	R/W	0h	Controls whether the CT-TBR will issue a pulse on SYNREQ each time the local buffer write pointer wraps back to address 0. Read 0x0 : SYNCREQ generation is suppressed Read 0x1 : SYNCREQ on buffer wrap is enabled Write 0x0 : Disable SYNCREQ generation Write 0x1 : Enable SYNCREQ generation
2	SRST	R/W	0h	Software initiated reset control Read 0x0 : Always Write 0x0 : No action Write 0x1 : Initiates a software reset
1	MODE	R/W	0h	This field is the top-level control for determining the operating mode of the module Read 0x0 : Module is in Buffer Mode Read 0x1 : Module is in System Bridge Mode Write 0x0 : Set Buffer Mode Write 0x1 : Set System Bridge Mode This bit can only be written when the ENBL bit is '0' Setting it when acquisition in enabled may result in undefined behavior. This bit is read only and set to '1' when CT-TBR is synthesized for System Bridge only operation.

Table 14-33475. CT_TBR_CT_TBR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ENBL	R/W	0h	This field is the top-level control for enabling trace acquisition and processing in the module. Read 0x0 : Module is disabled Read 0x1 : Module is enabled (trace data is being captured and stored to local memory) Write 0x0 : Disable module Write 0x1 : Enable module

14.10.1.2.247 CT_TBR_CT_TBR_RAMWDAT Register

1 CT_TBR_CT_TBR_RAMWDAT Register (Offset = 24h) [reset = 0h]

RAM Write Data Register This register is used to transfer data from the client to local memory This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-33476. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5024h**

Figure 14-11080. CT_TBR_CT_TBR_RAMWDAT Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-33478. CT_TBR_CT_TBR_RAMWDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	The 32-bit data value to be written to local memory Writing initiates the transfer of data to the location pointed at by RAMWPTR. RAMWPTR is then incremented automatically. This register should not be used when the data acquisition is enabled (results are undefined).

14.10.1.2.248 CT_TBR_CT_TBR_OUTLVL Register

1 CT_TBR_CT_TBR_OUTLVL Register (Offset = 100h) [reset = 63h]

Output FIFO Trigger Level Register This register controls the size of the data blocks transferred through the output FIFO and across the system interface

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Table 14-33479. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5100h**

Figure 14-11081. CT_TBR_CT_TBR_OUTLVL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMBLOCK							
R/W							
0h							
7	6	5	4	3	2	1	0
BLOCKSZ							
R/W							
63h							

Table 14-33481. CT_TBR_CT_TBR_OUTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:8	NUMBLOCK	R/W	0h	Determines blocks (value + 1) that must be sent over the system interface to complete a higher level data frame for transport. This field is used to calculate the total output trigger threshold when used in conjunction with BLOCKSZ field. Output Trigger Threshold (in frames) = (BLOCKSZ + 1) * (NUMBLOCK + 1) The threshold calculations include data in the output FIFO and local RAM buffers (if local RAM exists). Read : Returns the current configured value of the number of blocks in the high level data frame Write : Sets a new value. This register is only valid when the CT-TBR is operating in System Bridge mode This register can be read at any time but can only be written when acquisition is disabled in CNTL. In addition, SW should only update NUMBLOCK when the following conditions are all true : " An output flush sequence is not active (OPCTL : OUTFLUSH == 0) " The system interface output buffer is empty (STAT : DRAIN_DONE == 1)

Table 14-33481. CT_TBR_CT_TBR_OUTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	BLOCKSZ	R/W	63h	Determines the block size (the number of 128-bit frames + 1) used by the DMA engine Reading data over the system interface. This field is used to calculate the total output trigger threshold when used in conjunction with NUMBLOCK field. The block size is used by the DMA event logic to determine when to deassert the DMA request. Output Trigger Threshold (in frames) = (BLOCKSZ + 1) * (NUMBLOCK + 1) The threshold calculations include data in the output FIFO and local RAM buffers (if local RAM exists). Read : Returns the current configured value of the block size Write : Sets a new value. The minimum value for BLOCKSZ is 0xF. If configured for less than 0xF, the behavior of the system interface is undefined. This register is only valid when the CT-TBR is operating in System Bridge mode This register can be read at any time but can only be written when acquisition is disabled in CNTL. In addition, SW should only update BLOCKSZ when the following conditions are all true : " An output flush sequence is not active (OPCTL : OUTFLUSH == 0) " The system interface output buffer is empty (STAT : DRAIN_DONE == 1)

14.10.1.2.249 CT_TBR_CT_TBR_SICTRL Register

1 CT_TBR_CT_TBR_SICTRL Register (Offset = 104h) [reset = 32h]

CT-TBR System Interface Control This register provides control and status for the system interface of the CT-TBR

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Table 14-33482. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5104h

Figure 14-11082. CT_TBR_CT_TBR_SICTRL Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED1		IDLE_MODE		RESERVED	ERR	REQ_PEND	DATA_WIDTH
R/W		R/W		R	R/W	R	R/W
0h		3h		0h	0h	1h	0h

Table 14-33484. CT_TBR_CT_TBR_SICTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R/W	0h	
5:4	IDLE_MODE	R/W	3h	This bit-field controls the idle behavior of the CT-TRB Read : Indicates the Idle modes outlined below Write 00b : Set Force-Idle. For CT-TBR, Force-Idle is identical to Smart-Idle Write 01b : Set No-Idle : The CT_TBR will acknowledge the idle request, but never transition to the idle state Write 10b : Set Smart-Idle : The CT-TBR uses the smart idle protocol. This is the default mode. Write 11b : Set Smart-Idle-Wkup : Since the CT-TBR does not support internal wakeup, this mode is identical to Smart-Idle
3	RESERVED	R	0h	
2	ERR	R/W	0h	This bit indicates that an access on the System Target I/F resulted in a error Read 0x0 : No errors since last clear Read 0x1 : At least one error condition on the I/F since last clear Write 0x0 : No effect Write 0x1 : Clears bit to 0 This bit clears to 0 when data acquisition is enabled (CTRL : ENBL 0- > 1)
1	REQ_PEND	R	1h	This bit indicates if a read request is pending or active on the system interface Read 0x0 : No read requests pending or active Read 0x1 : A system initiator has posted a read request on the system interface and this request is pending or being serviced

Table 14-33484. CT_TBR_CT_TBR_SICTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DATA_WIDTH	R/W	0h	This bit controls the supported access size for the system interface Read 0x0 : System interface will only support 32-bit reads Read 0x1 : System interface will only support 64-bit reads Write 0x0 : Set 32-bit mode Write 0x1 : Set 64-bit mode This bit is RO and set to 0 when synthesized for 32-bit data width

14.10.1.2.250 CT_TBR_CT_TBR_IDPERIOD Register

1 CT_TBR_CT_TBR_IDPERIOD Register (Offset = 108h) [reset = 0h]

ID Repeat Period Register This register controls the number of frames (without and ID change marker) that will be sent before the formatter forces and ID marker

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Table 14-33485. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5108h**

Figure 14-11083. CT_TBR_CT_TBR_IDPERIOD Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PERIOD	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIOD							
R/W							
0h							

Table 14-33487. CT_TBR_CT_TBR_IDPERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	R/W	0h	
9:0	PERIOD	R/W	0h	Controls the number of 128-bit frames (with no ID change markers) that the formatter will forward before forcing an artificial ID change. Read : Returns the current configured value of the period Write : Sets the value Setting to 0 disables the forcing of IDs, but this is not recommended. PERIOD should only be updated when trace acquisition is disabled

14.10.1.2.251 CT_TBR_CT_TBR_SEQCNTL Register

1 CT_TBR_CT_TBR_SEQCNTL Register (Offset = 10Ch) [reset = 7274496h]

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Table 14-33488. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 510Ch**

Figure 14-11084. CT_TBR_CT_TBR_SEQCNTL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R/W							
Eh							
23	22	21	20	19	18	17	16
RESERVED2	SEQID						
R/W	R/W						
Eh	27h						
15	14	13	12	11	10	9	8
RESERVED						PERIOD	
R/W						R/W	
11h						96h	
7	6	5	4	3	2	1	0
PERIOD							
R/W							
96h							

Table 14-33490. CT_TBR_CT_TBR_SEQCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED2	R/W	Eh	
22:16	SEQID	R/W	27h	PERIOD1This defined the ATID used when inserting the incrementing sequence byte. The reset value is the highest free ID supported in the TWP specification, but this can be overwritten by SW if there are system collisions
15:10	RESERVED	R/W	11h	
9:0	PERIOD	R/W	96h	Controls the number of 128-bit frames that the formatter will forward before inserting an 8-bit incrementing sequence number into a frame using ATID defined in SEQID Read : Returns the current configured value of the period Write : Sets the value Setting to 0 disables the insertion of the incrementing sequence bytes, PERIOD should only be updated when trace acquisition is disabled

14.10.1.2.252 CT_TBR_CT_TBR_EOI Register

1 CT_TBR_CT_TBR_EOI Register (Offset = 120h) [reset = 0h]

CT-TBR EOI register This register is the End of Interrupt used by SW to signal HW that an interrupt service is complete and an interrupt can be rearmed.

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Table 14-33491. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5120h**

Figure 14-11085. CT_TBR_CT_TBR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_VECT</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-33493. CT_TBR_CT_TBR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R/W	0h	
0	EOI_VECT	R/W	0h	This bit is used by SW to signal that a particular interrupt generated by the IP can be rearmed. Read 0x0 : Always Write 0x0 : DAV_IRQ is rearmed (it is IRQ index 0 for this IP) Write 0x1 : AQCMP_IRQ is rearmed (it is IRQ index 1)

14.10.1.2.253 CT_TBR_CT_TBR_IRQSTATUS_RAW Register

1 CT_TBR_CT_TBR_IRQSTATUS_RAW Register (Offset = 124h) [reset = 0h]

CT-TBR IRQ Status (Raw) register This register provides control and status for the interrupt/event interface The IRQSTATUS_RAW register may be modified while acquisition is enabled

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Table 14-33494. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 5124h**

Figure 14-11086. CT_TBR_CT_TBR_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						AQCMP_IRQ	DAV_IRQ
R/W						R/W	R/W
0h						0h	0h

Table 14-33496. CT_TBR_CT_TBR_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IRQ	R/W	0h	This bit controls the acquisition complete interrupt/event generation for testing Read 0x0 : Acquisition complete interrupt is not active Read 0x1 : Acquisition complete interrupt is active and awaiting completion. The enabled state is not considered. Write 0x0 : No effect Write 0x1 : Sets the interrupt request for testing
0	DAV_IRQ	R/W	0h	This bit controls the data available interrupt/event generation for testing Read 0x0 : Data available interrupt is not active Read 0x1 : Data available interrupt is active and awaiting completion. The enabled state is not considered. Write 0x0 : No effect Write 0x1 : Sets the interrupt request for testing

14.10.1.2.254 CT_TBR_CT_TBR_IRQSTATUS Register

1 CT_TBR_CT_TBR_IRQSTATUS Register (Offset = 128h) [reset = 0h]

CT-TBR IRQ Status register This register provides control and status for the interrupt/event interface The IRQSTATUS register may be modified while acquisition is enabled

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Table 14-33497. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5128h**

Figure 14-11087. CT_TBR_CT_TBR_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						AQCMP_IE	DAV_IE
R/W						R/W	R/W
0h						0h	0h

Table 14-33499. CT_TBR_CT_TBR_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IE	R/W	0h	Acquisition complete interrupt enable Read 0x0 : Acquisition complete interrupt/event generation is either not pending or it is not enabled Read 0x1 : The acquisition complete interrupt is pending and enabled. Write 0x0 : No effect Write 0x1 : Clears a pending Acquisition complete interrupt
0	DAV_IE	R/W	0h	Data Available interrupt enable Read 0x0 : Data available interrupt/event generation is either not pending or it is disabled Read 0x1 : Data available interrupt is pending and enabled. Write 0x0 : No effect Write 0x1 : Clears a pending data available interrupt

14.10.1.2.255 CT_TBR_CT_TBR_IRQENABLE_SET Register

1 CT_TBR_CT_TBR_IRQENABLE_SET Register (Offset = 12Ch) [reset = 0h]

CT-TBR IRQ Enable set register This register provides control for the interrupt/event interface The IRQENABLE_SET register may be modified while acquisition is enabled

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Table 14-33500. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 512Ch**

Figure 14-11088. CT_TBR_CT_TBR_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						AQCMP_IES	DAV_IES
R/W						R/W	R/W
0h						0h	0h

Table 14-33502. CT_TBR_CT_TBR_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IES	R/W	0h	Provides enable state and sets the enable of the acquisition complete interrupt/event Read 0x0 : The acquisition complete interrupt is disabled Read 0x1 : The acquisition complete interrupt is enabled Write 0x0 : No effect Write 0x1 : Enables the acquisition complete interrupt/event
0	DAV_IES	R/W	0h	Provides enable state and sets the enable of the data available interrupt/event Read 0x0 : The data available interrupt is disabled Read 0x1 : The data available interrupt is enabled Write 0x0 : No effect Write 0x1 : Enables the data available interrupt/event

14.10.1.2.256 CT_TBR_CT_TBR_IRQENABLE_CLR Register

1 CT_TBR_CT_TBR_IRQENABLE_CLR Register (Offset = 130h) [reset = 0h]

CT-TBR IRQ Enable clear register This register provides control for the interrupt/event interface The IRQENABLE_CLR register may be modified while acquisition is enabled

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Table 14-33503. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5130h**

Figure 14-11089. CT_TBR_CT_TBR_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						AQCMP_IEC	DAV_IEC
R/W						R/W	R/W
0h						0h	0h

Table 14-33505. CT_TBR_CT_TBR_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IEC	R/W	0h	Provides enable state and clears the enable of the data available interrupt/event Read 0x0 : The acquisition complete interrupt is disabled Read 0x1 : The acquisition complete interrupt is enabled Write 0x0 : No effect Write 0x1 : Disables the acquisition complete interrupt/event
0	DAV_IEC	R/W	0h	Provides enable state and clears the enable of the data available interrupt/event Read 0x0 : The data available interrupt is disabled Read 0x1 : The data available interrupt is enabled Write 0x0 : No effect Write 0x1 : Disables the data available interrupt/event

14.10.1.2.257 CT_TBR_CT_TBR_OPSTAT Register

1 CT_TBR_CT_TBR_OPSTAT Register (Offset = 300h) [reset = 2h]

Operation Status Register This register provides information on the status of various operations of the CT-TBR

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Table 14-33506. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5300h**

Figure 14-11090. CT_TBR_CT_TBR_OPSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						FMT_HALTED	FLSH_ACT
R						R	R
0h						1h	0h

Table 14-33508. CT_TBR_CT_TBR_OPSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	
1	FMT_HALTED	R	1h	This bit indicates that the formatter is halted and the last available data has been written to the local memory. It is functionally equivalent to the FMT_DONE bit in the STAT register. Read 0x0 : Formatter block is active Read 0x1 : Formatter block is disabled This bit is cleared by hardware when the CTRL'ENBL bit transitions from 0 to 1.
0	FLSH_ACT	R	0h	This bit indicates that a flush request is being processed by the CT-TBR Read 0x0 : No flush requests are active Read 0x1 : Flush request is pending completion

14.10.1.2.258 CT_TBR_CT_TBR_OPCTRL Register

1 CT_TBR_CT_TBR_OPCTRL Register (Offset = 304h) [reset = 512h]

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Table 14-33509. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5304h**

Figure 14-11091. CT_TBR_CT_TBR_OPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED4							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED4						SYNCREQ	OUTFLUSH
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
STP_FULL	RESERVED3	STP_TRG	STP_FLSH	RESERVED2	TRG_FLSH	TRG_EVT	TRG_TRGIN
R/W	R	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	1h
7	6	5	4	3	2	1	0
RESERVED1	FLUSH	FLSH_TRG	FLSH_FLSHIN	RESERVED		INSRT_TRG	FMT_ENBL
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	1h	0h		1h	0h

Table 14-33511. CT_TBR_CT_TBR_OPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED4	R	0h	
17	SYNCREQ	R/W	0h	This bit is allows the SW to stimulate a synchronization request to all the upstream trace components. Read 0x0 : This bit always reads as 0 Write 0x0 : Has no effect Write 0x1 : Results in the assertion of the SYNCREQ signal on the ATB target for one ATCLK cycle. SYNCREQ is available in any operating mode. SYNCREQ should only be written while trace acquisition is enabled.
16	OUTFLUSH	R/W	0h	This bit is the flush control. For the output FIFO (System Bridge Mode) it triggers a flush of this buffer and the flush completes when the last OUTLEVEL + 1 sized burst is read on the system Interface. Read 0x0 : No output flush operation is active Read 0x1 : Output flush operation is active Write 0x0 : No meaning Write 0x1 : Initiate an output buffer flush. Automatically clears to 0 when the operation completes OUTFLUSH may be written while trace acquisition is enabled
15	STP_FULL	R/W	0h	This bit controls whether the formatter stops operation when the local memory buffer is full. This 'one-shot' mode prevents the write pointer from wrapping, Read 0x0 : Formatter continues when write pointer wraps back to the lowest address Read 0x1 : Formatter stops operation when the local memory is full Write 0x0 : Disable formatter halt on full Write 0x1 : Enable formatter halt on full This bit is only functional when the CT-TBR is configured for Buffer Mode (CTRL : MODE == 0).
14	RESERVED3	R	0h	

Table 14-33511. CT_TBR_CT_TBR_OPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	STP_TRG	R/W	0h	This bit controls whether the formatter stops operation when a trigger is detected Read 0x0 : Formatter continues when trigger is detected Read 0x1 : Formatter stops operation when trigger is detected Write 0x0 : Disable formatter halt on trigger Write 0x1 : Enable formatter halt on trigger
12	STP_FLSH	R/W	0h	This bit controls whether the formatter stops operation when a flush completes Read 0x0 : Formatter continues after flush completion Read 0x1 : Formatter stops operation when flush completes Write 0x0 : Disable formatter halt on flush completion Write 0x1 : Enable formatter halt on flush completion
11	RESERVED2	R	0h	
10	TRG_FLSH	R/W	1h	This bit controls whether a trigger event is generated when a flush completes Read 0x0 : No trigger event generated when flush is completed. Read 0x1 : Trigger event generated Write 0x0 : Disable trigger event generation Write 0x1 : Enable trigger event generation
9	TRG_EVT	R/W	0h	This bit controls whether the action associated with a trigger is delayed until the trigger counter matches the value in TRGCNT : COUNT + 1. Read 0x0 : No trigger counter delay Read 0x1 : Trigger action delayed until trigger count match Write 0x0 : Disable trigger delay Write 0x1 : Enable trigger delay
8	TRG_TRGIN	R/W	1h	This bit controls whether a trigger event is generated when a rising edge is detected on the TRIGIN input on the CTI interface. Setting this bit also enables trigger event generation when a trigger ID (ATID = 0x7d) is seen on the ATB interface. Read 0x0 : No trigger event generated on TRIGIN assertion. Read 0x1 : Trigger event generated Write 0x0 : Disable trigger event generation Write 0x1 : Enable trigger event generation
7	RESERVED1	R	0h	
6	FLUSH	R/W	0h	This bit is the manual flush control. It triggers a flush from the trace data sources into the CT-TBR Read 0x0 : No manual flush operation is active Read 0x1 : Manual flush operation is active Write 0x0 : No meaning Write 0x1 : Initiate a manual flush. Automatically clears to 0 when the operation completes FLUSH may be written while trace acquisition is enabled
5	FLSH_TRG	R/W	0h	This bit controls whether a flush operation is initiated when a trigger condition is detected by the CT-TBR Read 0x0 : Flush on trigger event is disabled Read 0x1 : Flush on trigger event is enabled Write 0x0 : Disable flush on trigger event Write 0x1 : Enable flush on trigger event
4	FLSH_FLSHIN	R/W	1h	This bit controls whether a flush operation is initiated when a rising edge is detected on the FLUSHIN input signal Read 0x0 : Flush on FLUSHIN is disabled Read 0x1 : Flush on FLUSHIN is enabled Write 0x0 : Disable flush on FLUSHIN Write 0x1 : Enable flush on FLUSHIN
3:2	RESERVED	R	0h	
1	INSRT_TRG	R/W	1h	This bit controls whether the TWP trigger sequence is inserted into the TWP frame a trigger condition is encountered Read 0x0 : Trigger insertion is disabled Read 0x1 : Trigger insertion is enabled Write 0x0 : Disable trigger insertion Write 0x1 : Enable trigger insertion
0	FMT_ENBL	R/W	0h	This bit controls whether the ATB input data is formatted into 128-bit TWP frames Read 0x0 : Formatting is disabled Read 0x1 : Formatting is enabled Write 0x0 : Disable formatting Write 0x1 : Enable formatting

14.10.1.2.259 CT_TBR_CLAIMSET Register

1 CT_TBR_CLAIMSET Register (Offset = FA0h) [reset = 1h]

The Claim Tag Set Register The register is used to manage handshakes between application and tools SW using the CT-TBR

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Table 14-33512. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5FA0h

Figure 14-11092. CT_TBR_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTSET			
R				R/W			
0h				1h			

Table 14-33514. CT_TBR_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	
3:0	CTSET	R/W	1h	This bit sets the Claim Tag Read 0xF : Always. Indicates that claim tag has 4 valid bits Write 0x0 : No effect Write 0x1-F : Bit value of '1' sets the corresponding Claim Tag bit

14.10.1.2.260 CT_TBR_CLAIMCLR Register

1 CT_TBR_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

The Claim Tag Clear Register The register is used to manage handshakes between application and tools SW using the CT-TBR

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Table 14-33515. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FA4h**

Figure 14-11093. CT_TBR_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCLR			
R				R			
0h				0h			

Table 14-33517. CT_TBR_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	
3:0	CTCLR	R	0h	This bit clears the Claim Tag Read : The current claim tag value Write 0x0 : No effect Write 0x1-F : Bit value of '1' clears the corresponding bit in the Claim Tag

14.10.1.2.261 CT_TBR_LOCKACC Register

1 CT_TBR_LOCKACC Register (Offset = FB0h) [reset = 0h]

The Lock Access Register The register is used to enabled application use of the CT-TBR

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Table 14-33518. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FB0h**

Figure 14-11094. CT_TBR_LOCKACC Name Register

31	30	29	28	27	26	25	24
CODE							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
CODE							
R							
0h							
7	6	5	4	3	2	1	0
CODE							
R							
0h							

Table 14-33520. CT_TBR_LOCKACC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CODE	R	0h	This bit-field is used to unlock the CT-TBR for use by the application Write 0xC5ACCE55 : Unlocks the CT-TBR Write any other value : Lock the CT-TBR

14.10.1.2.262 CT_TBR_LOCKSTAT Register

1 CT_TBR_LOCKSTAT Register (Offset = FB4h) [reset = 2h]

The Lock Status Register The register is used to manage application use of the CT-TBR

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Table 14-33521. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FB4h**

Figure 14-11095. CT_TBR_LOCKSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKSZ	STAT	LOCKIMP
R					R	R	R
0h					0h	1h	0h

Table 14-33523. CT_TBR_LOCKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2	LOCKSZ	R	0h	This bit-field indicates the size of the lock access bit-field Read 0x0 : indicates the lock access field is 32-bits wide
1	STAT	R	1h	This bit-field indicates the current state of the lock Read 0x0 : indicates the module is not locked from application accesses Read 0x1 : Indicates the module is locked
0	LOCKIMP	R	0h	This bit-field indicates if the module implements a lock access mechanism Read 0x1 : Indicates a lock is present

14.10.1.2.263 CT_TBR_AUTHSTAT Register

1 CT_TBR_AUTHSTAT Register (Offset = FB8h) [reset = 0h]

Authorization Status Register Indicates which security features (if any) are implemented in the module.

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Table 14-33524. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FB8h**

Figure 14-11096. CT_TBR_AUTHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
S_NI_STAT		S_I_STAT		NS_NI_STAT		NS_I_STAT	
R		R		R		R	
0h		0h		0h		0h	

Table 14-33526. CT_TBR_AUTHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:6	S_NI_STAT	R	0h	Secure, non-invasive debug status Read 0x0 : Indicates CT-TBR does not implement this feature
5:4	S_I_STAT	R	0h	
3:2	NS_NI_STAT	R	0h	
1:0	NS_I_STAT	R	0h	Non-secure, invasive debug status Read 0x0 : Indicates CT-TBR does not implement this feature

14.10.1.2.264 CT_TBR_DEVID Register

1 CT_TBR_DEVID Register (Offset = FC8h) [reset = 18h]

Device Identification Register Defines the major and minor versions of this implementation of the CT-TBR

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Table 14-33527. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FC8h**

Figure 14-11097. CT_TBR_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
REV_MAJOR				REV_MIN			
R				R			
1h				8h			

Table 14-33529. CT_TBR_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REV_MAJOR	R	1h	
3:0	REV_MIN	R	8h	Minor revision number Read 0x0 : The only minor revision currently supported

14.10.1.2.265 CT_TBR_DEVTYPE Register

1 CT_TBR_DEVTYPE Register (Offset = FCCh) [reset = 33h]

Device Type Register Indicates the top-level function of the module

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Table 14-33530. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FCCh**

Figure 14-11098. CT_TBR_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAIN_CLASS			
R				R			
3h				3h			

Table 14-33532. CT_TBR_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	SUB_TYPE	R	3h	Identifies the sub-type based upon class Read 0x2 : Indicates the CT-TBR is an embedded trace buffer
3:0	MAIN_CLASS	R	3h	Identifies the top level class to the module Read 0x1 : Indicates the CT-TBR is a trace sink

14.10.1.2.266 CT_TBR_PERIPHID4 Register

1 CT_TBR_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral Identification Register Number 4 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33533. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5FD0h

Figure 14-11099. CT_TBR_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KB_COUNT				JEP_CONT			
R				R			
0h				0h			

Table 14-33535. CT_TBR_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	KB_COUNT	R	0h	Indicates the number of 4KB block of configuration memory (+ 1) used by this module. Read 0x0 : CT-TBR uses one block
3:0	JEP_CONT	R	0h	JEDEC manufacture code continuation code Read 0x0 : TI JEP number does not use continuation

14.10.1.2.267 CT_TBR_PERIPHID5 Register

1 CT_TBR_PERIPHID5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register Number 5 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33536. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FD4h**

Figure 14-11100. CT_TBR_PERIPHID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PID5							
R							
0h							

Table 14-33538. CT_TBR_PERIPHID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	PID5	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.10.1.2.268 CT_TBR_PERIPHID6 Register

1 CT_TBR_PERIPHID6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register Number 6 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33539. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FD8h**

Figure 14-11101. CT_TBR_PERIPHID6 Name Register

31	30	29	28	27	26	25	24
PID7							
R							
0h							
23	22	21	20	19	18	17	16
PID7							
R							
0h							
15	14	13	12	11	10	9	8
PID7							
R							
0h							
7	6	5	4	3	2	1	0
PID6							
R							
0h							

Table 14-33541. CT_TBR_PERIPHID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	PID7	R	0h	
7:0	PID6	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.10.1.2.269 CT_TBR_PERIPHID7 Register

1 CT_TBR_PERIPHID7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register Number 7 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33542. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FDCh**

Figure 14-11102. CT_TBR_PERIPHID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PID7							
R							
0h							

Table 14-33544. CT_TBR_PERIPHID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	PID7	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.10.1.2.270 CT_TBR_PERIPHID0 Register

1 CT_TBR_PERIPHID0 Register (Offset = FE0h) [reset = 223h]

Peripheral Identification Register Number 0 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33545. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5FE0h

Figure 14-11103. CT_TBR_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
2h							
23	22	21	20	19	18	17	16
RESERVED							
R							
2h							
15	14	13	12	11	10	9	8
RESERVED							
R							
2h							
7	6	5	4	3	2	1	0
PART_ML							
R							
23h							

Table 14-33547. CT_TBR_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	2h	
7:0	PART_ML	R	23h	The middle and lower BCD value of the part number. Read 0xDF : CT-TBR BCD part number is EDF

14.10.1.2.271 CT_TBR_PERIPHID1 Register

1 CT_TBR_PERIPHID1 Register (Offset = FE4h) [reset = 126h]

Peripheral Identification Register Number 1 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33548. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FE4h**

Figure 14-11104. CT_TBR_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
1h							
23	22	21	20	19	18	17	16
RESERVED							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED							
R							
1h							
7	6	5	4	3	2	1	0
JEPID_L				PART_U			
R				R			
2h				6h			

Table 14-33550. CT_TBR_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	1h	
7:4	JEPID_L	R	2h	JEP106 ID[3 : 0]. Read 0x7 : TI JEP106 ID is 0x17
3:0	PART_U	R	6h	The upper BCD value of the part number. Read 0xE : CT-TBR BCD part number is EDF

14.10.1.2.272 CT_TBR_PERIPHID2 Register

1 CT_TBR_PERIPHID2 Register (Offset = FE8h) [reset = 24h]

Peripheral Identification Register Number 2 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33551. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FE8h**

Figure 14-11105. CT_TBR_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
REVNUM				JEDEC	JEPID_H		
R				R	R		
2h				0h	4h		

Table 14-33553. CT_TBR_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REVNUM	R	2h	Revision number of the peripheral module Read 0x0 : Only revision of CT-TBR
3	JEDEC	R	0h	Indicates JEDEC ID was used Read 0x1 : JEDEC ID is used
2:0	JEPID_H	R	4h	JEP106 ID[6 : 4]. Read 0x1 : TI JEP106 ID is 0x17

14.10.1.2.273 CT_TBR_PERIPHID3 Register

1 CT_TBR_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register Number 3 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-33554. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FECh**

Figure 14-11106. CT_TBR_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CUSTMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33556. CT_TBR_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REVAND	R	0h	Indicates the errata fix version of the IP Read 0x0 : CT-TBR uses one block
3:0	CUSTMOD	R	0h	Indicates that the module was reusable IP that was modified by the customer Read 0x0 : CT-TBR is native IP

14.10.1.2.274 CT_TBR_COMPID0 Register

1 CT_TBR_COMPID0 Register (Offset = FF0h) [reset = 13h]

Component Identification Register Number 0 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-33557. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF0h**

Figure 14-11107. CT_TBR_COMPID0 Name Register

31	30	29	28	27	26	25	24
CID1							
R							
0h							
23	22	21	20	19	18	17	16
CID1							
R							
0h							
15	14	13	12	11	10	9	8
CID1							
R							
0h							
7	6	5	4	3	2	1	0
CID0							
R							
13h							

Table 14-33559. CT_TBR_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CID1	R	0h	
7:0	CID0	R	13h	The fixed preamble for the component ID Read 0x0D : CID0 Preamble is fixed at 0x0D

14.10.1.2.275 CT_TBR_COMPID1 Register

1 CT_TBR_COMPID1 Register (Offset = FF4h) [reset = 144h]

Component Identification Register Number 1 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-33560. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF4h**

Figure 14-11108. CT_TBR_COMPID1 Name Register

31	30	29	28	27	26	25	24
CLASS1							
R							
1h							
23	22	21	20	19	18	17	16
CLASS1							
R							
1h							
15	14	13	12	11	10	9	8
CLASS1							
R							
1h							
7	6	5	4	3	2	1	0
CLASS				CID1			
R				R			
4h				4h			

Table 14-33562. CT_TBR_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CLASS1	R	1h	
7:4	CLASS	R	4h	Indicates the class of the component Read 0x9 : CT-TBR is a CoreSight component
3:0	CID1	R	4h	The fixed preamble for the component ID Read 0x0 : CID1 Preamble is fixed at 0x0

14.10.1.2.276 CT_TBR_COMPID2 Register

1 CT_TBR_COMPID2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register Number 2 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-33563. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF8h**

Figure 14-11109. CT_TBR_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CID2							
R							
5h							

Table 14-33565. CT_TBR_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	CID2	R	5h	The fixed preamble for the component ID Read 0x05 : CID2 Preamble is fixed at 0x05

14.10.1.2.277 CT_TBR_COMPID3 Register

1 CT_TBR_COMPID3 Register (Offset = FFCh) [reset = 177h]

2Component Identification Register Number 3 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-33566. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FFCh**

Figure 14-11110. CT_TBR_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
1h							
23	22	21	20	19	18	17	16
RESERVED							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED							
R							
1h							
7	6	5	4	3	2	1	0
CID3							
R							
77h							

Table 14-33568. CT_TBR_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	1h	
7:0	CID3	R	77h	The fixed preamble for the component ID Read 0x05 : CID2 Preamble is fixed at 0x05

14.10.1.2.278 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-33569. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11111. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-33571. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.279 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-33572. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11112. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-33574. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.280 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-33575. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11113. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-33577. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.281 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-33578. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F018h

Figure 14-11114. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-33580. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.282 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-33581. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11115. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-33583. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.283 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33584. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11116. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33586. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.284 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33587. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11117. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33589. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.285 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33590. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F028h

Figure 14-11118. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33592. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.286 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33593. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11119. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33595. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.287 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33596. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11120. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33598. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.288 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33599. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F034h

Figure 14-11121. CSCTI_CFG_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33601. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.289 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33602. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F038h

Figure 14-11122. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33604. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.290 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33605. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11123. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33607. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.291 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33608. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11124. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33610. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.292 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33611. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11125. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33613. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.293 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33614. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11126. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33616. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.294 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33617. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11127. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33619. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.295 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33620. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11128. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33622. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.296 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33623. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11129. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33625. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.297 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33626. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11130. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33628. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.298 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33629. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11131. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33631. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.299 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-33632. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11132. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-33634. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.300 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-33635. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11133. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-33637. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.301 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-33638. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11134. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-33640. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.302 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-33641. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11135. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-33643. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.303 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-33644. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11136. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-33646. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.304 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-33647. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11137. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-33649. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.305 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-33650. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11138. CSCTI_CFG_ITCHINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHINACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33652. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.306 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-33653. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11139. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-33655. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.307 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-33656. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11140. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-33658. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.308 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-33659. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11141. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-33661. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.309 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-33662. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11142. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-33664. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.310 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-33665. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11143. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-33667. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.311 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-33668. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11144. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-33670. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.312 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-33671. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11145. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTTRIGIN							
R							
0h							

Table 14-33673. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.313 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-33674. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11146. CSCTI_CFG_ITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTEGRATION_MODE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-33676. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.314 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-33677. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11147. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-33679. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.315 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-33680. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11148. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-33682. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.316 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-33683. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11149. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-33685. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.317 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-33686. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11150. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-33688. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.318 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-33689. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11151. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-33691. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.319 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-33692. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11152. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-33694. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.320 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-33695. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11153. CSCTI_CFG_DEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB_TYPE</td><td colspan="4">MAJOR_TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">4h</td></tr>
</table>

Table 14-33697. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.321 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-33698. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11154. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-33700. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.322 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-33701. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11155. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-33703. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.323 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-33704. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11156. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-33706. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.324 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-33707. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11157. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-33709. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.325 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-33710. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11158. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-33712. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.326 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-33713. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11159. CSCTI_CFG_COMPONID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-33715. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.327 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-33716. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11160. CSCTI_CFG_COMPONID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33718. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.328 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33719. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11161. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-33721. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.329 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33722. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11162. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-33724. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.330 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-33725. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11163. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-33727. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.331 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-33728. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11164. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-33730. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.332 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-33731. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11165. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-33733. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.333 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-33734. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11166. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-33736. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.334 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-33737. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11167. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-33739. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.335 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33740. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11168. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33742. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.336 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33743. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11169. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33745. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.337 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33746. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11170. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33748. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.338 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33749. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11171. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33751. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.339 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33752. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11172. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33754. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.340 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33755. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11173. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33757. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.341 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33758. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11174. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33760. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.342 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33761. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11175. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33763. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.343 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33764. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11176. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33766. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.344 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33767. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11177. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33769. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.345 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33770. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11178. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33772. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.346 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33773. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11179. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33775. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.347 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33776. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11180. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33778. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.348 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33779. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11181. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33781. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.349 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33782. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11182. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33784. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.350 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33785. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11183. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33787. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.351 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

Return to Summary Table

Table 14-33788. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11184. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-33790. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.352 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

Return to Summary Table

Table 14-33791. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11185. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRIGOUTSTATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33793. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.353 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-33794. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11186. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-33796. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.354 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

Return to Summary Table

Table 14-33797. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11187. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-33799. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.355 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-33800. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11188. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-33802. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.356 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-33803. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11189. CSCTI_CFG_ASICCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ASICCTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33805. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.357 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-33806. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11190. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-33808. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.358 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-33809. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11191. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-33811. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.359 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-33812. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11192. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-33814. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.360 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-33815. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11193. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-33817. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.361 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-33818. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11194. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-33820. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.362 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-33821. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11195. CSCTI_CFG_ITTRIGOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUTACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33823. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.363 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-33824. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11196. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-33826. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.364 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-33827. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11197. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-33829. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.365 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-33830. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11198. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-33832. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.366 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-33833. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11199. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33835. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.367 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-33836. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11200. CSCTI_CFG_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMCLR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33838. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.368 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-33839. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11201. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-33841. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.369 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-33842. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11202. CSCTI_CFG_LOCKSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>LOCKTYPE</td><td>LOCKGRANT</td><td>LOCKEXIST</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-33844. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.370 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-33845. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11203. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-33847. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.371 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-33848. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11204. CSCTI_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-33850. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.372 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-33851. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11205. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-33853. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.373 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-33854. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11206. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R				R			
0h				4h			

Table 14-33856. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.374 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-33857. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11207. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R							
6h							

Table 14-33859. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.375 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-33860. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11208. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-33862. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.376 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-33863. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11209. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-33865. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.377 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-33866. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11210. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-33868. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.378 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-33869. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11211. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-33871. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.379 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-33872. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11212. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-33874. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.380 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33875. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11213. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-33877. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.381 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-33878. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11214. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-33880. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.382 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-33881. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11215. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-33883. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.383 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-33884. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11216. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-33886. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.384 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-33887. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11217. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-33889. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.385 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-33890. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11218. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-33892. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.386 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-33893. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11219. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-33895. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.387 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33896. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11220. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33898. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.388 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33899. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11221. CSCTI_CFG_CTIINEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33901. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.389 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33902. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11222. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33904. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.390 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33905. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11223. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33907. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.391 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33908. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11224. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33910. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.392 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33911. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11225. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33913. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.393 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33914. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11226. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33916. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.394 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-33917. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11227. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-33919. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.395 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33920. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11228. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33922. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.396 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33923. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11229. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33925. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.397 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33926. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11230. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33928. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.398 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33929. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11231. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33931. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.399 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33932. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11232. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33934. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.400 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33935. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11233. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33937. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.401 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33938. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11234. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-33940. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.402 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-33941. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11235. CSCTI_CFG_CTIOUTEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33943. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.403 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-33944. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11236. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-33946. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.404 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-33947. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11237. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-33949. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.405 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-33950. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11238. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-33952. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.406 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-33953. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11239. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-33955. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.407 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-33956. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11240. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-33958. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.408 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-33959. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11241. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-33961. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.409 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-33962. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11242. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-33964. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.410 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-33965. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11243. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTTRIGINACK							
R/W							
0h							

Table 14-33967. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.411 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-33968. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11244. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-33970. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.412 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-33971. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11245. CSCTI_CFG_ITTRIGOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33973. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.413 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-33974. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11246. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-33976. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.414 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-33977. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11247. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-33979. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.415 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-33980. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11248. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-33982. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.416 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-33983. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11249. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-33985. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.417 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-33986. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11250. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-33988. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.418 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-33989. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11251. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-33991. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.419 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-33992. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11252. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-33994. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.420 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-33995. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11253. CSCTI_CFG_LOCKACCESS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-33997. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.421 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-33998. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11254. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34000. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.422 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34001. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11255. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34003. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.423 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34004. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11256. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-34006. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.424 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34007. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11257. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34009. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.425 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34010. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11258. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34012. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.426 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34013. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11259. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34015. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.427 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34016. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11260. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34018. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.428 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34019. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11261. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34021. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.429 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34022. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11262. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R				R			
0h				0h			

Table 14-34024. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.430 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34025. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11263. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34027. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.431 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34028. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11264. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34030. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.432 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34031. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11265. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34033. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.433 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34034. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11266. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34036. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.434 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34037. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11267. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34039. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.435 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34040. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11268. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34042. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.436 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34043. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11269. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34045. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.437 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34046. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11270. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34048. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.438 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34049. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11271. CSCTI_CFG_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPULSE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34051. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.439 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34052. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11272. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34054. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.440 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34055. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11273. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34057. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.441 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34058. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11274. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34060. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.442 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34061. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11275. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34063. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.443 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34064. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11276. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34066. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.444 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34067. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11277. CSCTI_CFG_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34069. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.445 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34070. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11278. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34072. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.446 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34073. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11279. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34075. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.447 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34076. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11280. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34078. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.448 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34079. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11281. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34081. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.449 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34082. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11282. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34084. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.450 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34085. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11283. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34087. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.451 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34088. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11284. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34090. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.452 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-34091. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11285. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34093. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.453 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34094. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11286. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34096. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.454 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34097. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11287. CSCTI_CFG_CTIOUTEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34099. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.455 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34100. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11288. CSCTI_CFG_CTITRIGINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRIGINSTATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-34102. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.456 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

Return to Summary Table

Table 14-34103. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11289. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-34105. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.457 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34106. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11290. CSCTI_CFG_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTICHINSTATUS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34108. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.458 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34109. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11291. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-34111. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.459 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34112. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11292. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34114. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.460 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34115. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11293. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASICCTL							
R/W							
0h							

Table 14-34117. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.461 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34118. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11294. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-34120. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.462 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34121. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11295. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-34123. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.463 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34124. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11296. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34126. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.464 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34127. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11297. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-34129. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.465 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

Return to Summary Table

Table 14-34130. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11298. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34132. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.466 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34133. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11299. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34135. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.467 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34136. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11300. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-34138. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.468 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34139. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11301. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34141. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.469 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34142. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11302. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34144. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.470 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34145. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11303. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-34147. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.471 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34148. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11304. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-34150. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.472 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34151. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11305. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-34153. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.473 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34154. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11306. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34156. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.474 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34157. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11307. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34159. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.475 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34160. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11308. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMTRIG							
R							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-34162. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.476 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34163. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11309. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34165. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.477 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34166. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11310. CSCTI_CFG_PERIPHID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-34168. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.478 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34169. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11311. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34171. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.479 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34172. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11312. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34174. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.480 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34175. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11313. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34177. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.481 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34178. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11314. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-34180. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.482 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34181. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11315. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34183. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.483 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34184. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11316. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34186. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.484 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34187. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11317. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34189. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.485 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34190. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11318. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34192. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.486 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34193. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11319. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34195. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.487 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34196. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11320. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34198. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.488 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34199. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11321. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34201. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.489 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34202. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F018h

Figure 14-11322. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34204. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.490 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cti響clk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34205. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11323. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-34207. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.491 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34208. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11324. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34210. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.492 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34211. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-11325. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34213. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.493 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34214. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F028h

Figure 14-11326. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34216. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.494 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34217. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11327. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34219. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.495 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34220. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11328. CSCTI_CFG_CTIINEN4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34222. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.496 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34223. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11329. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34225. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.497 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34226. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11330. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34228. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.498 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34229. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11331. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34231. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.499 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34232. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11332. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34234. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.500 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34235. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11333. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34237. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.501 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34238. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11334. CSCTI_CFG_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34240. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.502 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34241. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11335. CSCTI_CFG_CTIOUTEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34243. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.503 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34244. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11336. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34246. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.504 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34247. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11337. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34249. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.505 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34250. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11338. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34252. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.506 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34253. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11339. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34255. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.507 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34256. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11340. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-34258. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.508 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-34259. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11341. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-34261. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.509 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34262. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11342. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-34264. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.510 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34265. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11343. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-34267. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.511 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34268. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11344. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34270. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.512 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34271. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11345. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-34273. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.513 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34274. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11346. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-34276. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.514 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34277. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11347. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-34279. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.515 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34280. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11348. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34282. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.516 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34283. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEE8h

Figure 14-11349. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-34285. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.517 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-34286. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11350. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34288. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.518 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34289. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11351. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34291. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.519 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34292. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11352. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-34294. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.520 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34295. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11353. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34297. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.521 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34298. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11354. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34300. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.522 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34301. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11355. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-34303. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.523 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34304. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11356. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-34306. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.524 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34307. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11357. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-34309. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.525 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34310. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11358. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34312. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.526 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34313. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11359. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34315. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.527 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34316. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11360. CSCTI_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-34318. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.528 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34319. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11361. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34321. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.529 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34322. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11362. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34324. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.530 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34325. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11363. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34327. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.531 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34328. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11364. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34330. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.532 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34331. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11365. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34333. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.533 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34334. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11366. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R				R			
0h				0h			

Table 14-34336. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.534 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34337. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11367. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34339. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.535 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34340. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11368. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34342. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.536 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34343. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11369. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34345. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.537 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34346. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11370. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34348. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.538 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34349. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11371. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34351. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.539 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34352. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11372. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34354. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.540 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34355. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11373. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34357. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.541 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34358. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F018h

Figure 14-11374. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34360. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.542 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34361. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11375. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-34363. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.543 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34364. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11376. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34366. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.544 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34367. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11377. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34369. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.545 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34370. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11378. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34372. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.546 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34373. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11379. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34375. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.547 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34376. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11380. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34378. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.548 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34379. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F034h

Figure 14-11381. CSCTI_CFG_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34381. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.549 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34382. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11382. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34384. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.550 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34385. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11383. CSCTI_CFG_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34387. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.551 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34388. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11384. CSCTI_CFG_CTIOUTEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34390. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.552 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34391. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11385. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34393. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.553 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34394. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11386. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34396. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.554 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34397. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11387. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34399. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.555 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34400. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11388. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34402. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.556 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34403. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11389. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34405. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.557 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34406. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11390. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34408. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.558 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34409. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11391. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34411. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.559 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34412. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11392. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-34414. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.560 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-34415. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11393. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGOUTSTATUS							
R							
0h							

Table 14-34417. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.561 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34418. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11394. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-34420. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.562 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34421. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11395. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-34423. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.563 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34424. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11396. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34426. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.564 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34427. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11397. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-34429. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.565 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34430. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11398. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-34432. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.566 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34433. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11399. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-34435. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.567 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34436. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11400. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34438. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.568 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34439. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11401. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-34441. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.569 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-34442. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11402. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34444. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.570 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34445. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11403. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34447. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.571 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34448. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11404. CSCTI_CFG_ITCHIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHIN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34450. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.572 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34451. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11405. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34453. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.573 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34454. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11406. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34456. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.574 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34457. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11407. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-34459. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.575 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34460. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11408. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-34462. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.576 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34463. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFB0h

Figure 14-11409. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-34465. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.577 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34466. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11410. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34468. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.578 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34469. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11411. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34471. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.579 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34472. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11412. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			

15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							

7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-34474. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.580 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34475. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11413. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34477. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.581 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34478. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11414. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34480. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.582 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34481. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11415. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34483. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.583 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34484. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11416. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34486. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.584 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34487. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11417. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34489. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.585 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34490. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11418. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34492. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.586 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34493. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11419. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34495. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.587 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34496. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11420. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34498. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.588 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34499. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11421. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34501. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.589 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34502. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11422. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34504. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.590 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34505. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11423. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34507. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.591 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34508. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11424. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34510. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.592 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34511. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11425. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34513. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.593 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34514. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11426. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34516. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.594 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34517. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11427. CSCTI_CFG_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPULSE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34519. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.595 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34520. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11428. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34522. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.596 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34523. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-11429. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34525. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.597 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34526. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F028h

Figure 14-11430. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34528. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.598 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34529. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11431. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34531. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.599 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34532. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11432. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34534. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.600 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34535. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11433. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34537. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.601 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34538. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11434. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34540. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.602 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34541. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F03Ch

Figure 14-11435. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34543. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.603 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34544. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11436. CSCTI_CFG_CTIOUTEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34546. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.604 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34547. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11437. CSCTI_CFG_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34549. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.605 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34550. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11438. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34552. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.606 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-34553. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11439. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34555. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.607 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34556. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11440. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34558. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.608 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34559. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11441. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34561. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.609 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34562. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11442. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34564. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.610 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34565. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11443. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34567. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.611 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34568. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11444. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-34570. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.612 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-34571. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11445. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-34573. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.613 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34574. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11446. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-34576. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.614 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34577. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11447. CSCTI_CFG_CTICHOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTICHOUTSTATUS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34579. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.615 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34580. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11448. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34582. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.616 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34583. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11449. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-34585. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.617 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34586. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11450. CSCTI_CFG_ITCHINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHINACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34588. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.618 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34589. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11451. CSCTI_CFG_ITTRIGINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGINACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-34591. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.619 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34592. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11452. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34594. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.620 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34595. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11453. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-34597. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.621 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-34598. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11454. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34600. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.622 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34601. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11455. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34603. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.623 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34604. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11456. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-34606. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.624 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34607. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11457. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34609. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.625 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34610. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11458. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34612. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.626 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34613. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11459. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34615. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.627 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34616. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11460. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-34618. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.628 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34619. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11461. CSCTI_CFG_LOCKACCESS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-34621. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.629 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34622. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11462. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34624. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.630 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34625. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11463. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34627. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.631 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34628. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11464. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMTRIG							
R							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-34630. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.632 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34631. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11465. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34633. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.633 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34634. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11466. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34636. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.634 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34637. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11467. CSCTI_CFG_PERIPHID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6h</td></tr>
</table>

Table 14-34639. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.635 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34640. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11468. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34642. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.636 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34643. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11469. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34645. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.637 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34646. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11470. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R				R			
0h				0h			

Table 14-34648. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.638 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34649. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11471. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34651. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.639 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34652. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11472. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34654. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.640 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34655. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11473. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34657. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.641 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34658. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11474. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34660. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.642 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34661. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11475. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34663. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.643 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34664. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11476. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34666. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.644 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34667. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11477. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34669. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.645 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34670. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11478. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34672. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.646 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34673. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11479. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-34675. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.647 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34676. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11480. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34678. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.648 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34679. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-11481. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34681. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.649 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34682. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11482. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34684. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.650 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34685. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11483. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34687. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.651 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34688. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11484. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34690. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.652 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34691. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11485. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34693. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.653 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34694. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11486. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34696. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.654 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34697. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11487. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34699. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.655 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34700. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11488. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34702. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.656 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34703. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11489. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34705. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.657 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34706. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11490. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34708. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.658 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34709. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11491. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34711. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.659 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34712. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11492. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34714. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.660 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34715. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11493. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34717. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.661 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34718. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11494. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34720. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.662 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34721. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11495. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34723. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.663 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34724. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11496. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-34726. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.664 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-34727. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11497. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-34729. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.665 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34730. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11498. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-34732. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.666 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34733. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11499. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-34735. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.667 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34736. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11500. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34738. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.668 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34739. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11501. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASICCTL							
R/W							
0h							

Table 14-34741. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.669 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34742. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11502. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-34744. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.670 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34745. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-11503. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-34747. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.671 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34748. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-11504. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34750. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.672 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34751. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11505. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-34753. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.673 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-34754. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11506. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34756. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.674 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34757. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-11507. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34759. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.675 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34760. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11508. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-34762. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.676 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34763. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11509. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34765. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.677 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34766. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11510. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34768. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.678 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34769. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11511. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34771. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.679 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34772. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11512. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-34774. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.680 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34775. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11513. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-34777. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.681 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34778. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11514. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34780. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.682 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34781. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11515. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34783. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.683 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34784. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11516. CSCTI_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-34786. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.684 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34787. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11517. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-34789. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.685 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34790. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11518. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34792. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.686 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-34793. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11519. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34795. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.687 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-34796. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11520. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34798. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.688 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-34799. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11521. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34801. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.689 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-34802. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11522. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-34804. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.690 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34805. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11523. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34807. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.691 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-34808. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11524. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34810. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.692 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34811. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11525. CSCTI_CFG_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-34813. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.693 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34814. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11526. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34816. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.1.2.694 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-34817. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-11527. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-34819. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.10.1.2.695 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-34820. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-11528. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-34822. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.696 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-34823. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-11529. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-34825. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.10.1.2.697 CSCTI_CFG_CTIAPPCLR Register

1 CSCTI_CFG_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-34826. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-11530. CSCTI_CFG_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-34828. CSCTI_CFG_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.698 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-34829. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-11531. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-34831. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.10.1.2.699 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34832. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-11532. CSCTI_CFG_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34834. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.700 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34835. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-11533. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34837. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.701 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34838. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-11534. CSCTI_CFG_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34840. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.702 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34841. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-11535. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34843. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.703 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34844. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-11536. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34846. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.704 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34847. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-11537. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34849. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.705 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34850. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-11538. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-34852. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.706 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-34853. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-11539. CSCTI_CFG_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34855. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.10.1.2.707 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34856. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-11540. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34858. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.708 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34859. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-11541. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34861. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.709 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34862. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-11542. CSCTI_CFG_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34864. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.710 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34865. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-11543. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34867. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.711 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34868. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-11544. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34870. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.712 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34871. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-11545. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34873. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.713 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34874. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-11546. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34876. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.714 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-34877. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-11547. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-34879. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.10.1.2.715 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-34880. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-11548. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-34882. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.10.1.2.716 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-34883. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-11549. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-34885. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.10.1.2.717 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-34886. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-11550. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-34888. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.10.1.2.718 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-34889. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-11551. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-34891. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.10.1.2.719 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-34892. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-11552. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-34894. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.10.1.2.720 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-34895. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-11553. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-34897. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.10.1.2.721 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-34898. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-11554. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-34900. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.10.1.2.722 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-34901. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEE0h

Figure 14-11555. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-34903. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.10.1.2.723 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-34904. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEE4h

Figure 14-11556. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-34906. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.10.1.2.724 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-34907. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-11557. CSCTI_CFG_ITTRIGOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-34909. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.10.1.2.725 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-34910. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-11558. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-34912. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.10.1.2.726 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-34913. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEF0h

Figure 14-11559. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-34915. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.10.1.2.727 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-34916. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-11560. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-34918. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.10.1.2.728 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-34919. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-11561. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-34921. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.10.1.2.729 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-34922. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-11562. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-34924. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.10.1.2.730 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-34925. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-11563. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-34927. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.10.1.2.731 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-34928. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-11564. CSCTI_CFG_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMCLR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34930. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.10.1.2.732 CSCTI_CFG_LOCKACCESS Register

1 CSCTI_CFG_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-34931. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-11565. CSCTI_CFG_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-34933. CSCTI_CFG_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.10.1.2.733 CSCTI_CFG_LOCKSTATUS Register

1 CSCTI_CFG_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-34934. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-11566. CSCTI_CFG_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-34936. CSCTI_CFG_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.10.1.2.734 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-34937. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-11567. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-34939. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.10.1.2.735 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-34940. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-11568. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-34942. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.10.1.2.736 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-34943. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-11569. CSCTI_CFG_DEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB_TYPE</td><td colspan="4">MAJOR_TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">4h</td></tr>
</table>

Table 14-34945. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.10.1.2.737 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-34946. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-11570. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-34948. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.10.1.2.738 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

Return to Summary Table

Table 14-34949. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-11571. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-34951. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.10.1.2.739 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

Return to Summary Table

Table 14-34952. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-11572. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R				R			
0h				9h			

Table 14-34954. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.10.1.2.740 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

Return to Summary Table

Table 14-34955. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-11573. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-34957. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.10.1.2.741 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

Return to Summary Table

Table 14-34958. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-11574. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-34960. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.10.1.2.742 CSCTI_CFG_COMPONID0 Register

1 CSCTI_CFG_COMPONID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-34961. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-11575. CSCTI_CFG_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-34963. CSCTI_CFG_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.10.1.2.743 CSCTI_CFG_COMPONID1 Register

1 CSCTI_CFG_COMPONID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

Return to Summary Table

Table 14-34964. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-11576. CSCTI_CFG_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-34966. CSCTI_CFG_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.10.1.2.744 CSCTI_CFG_COMPONID2 Register

1 CSCTI_CFG_COMPONID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34967. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-11577. CSCTI_CFG_COMPONID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-34969. CSCTI_CFG_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.10.1.2.745 CSCTI_CFG_COMPONID3 Register

1 CSCTI_CFG_COMPONID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-34970. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-11578. CSCTI_CFG_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-34972. CSCTI_CFG_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.10.2 DEBUGSS_WRAP

DEBUGSS_WRAP

14.10.2.1 DEBUGSS_WRAP Summaries

DEBUGSS_WRAP Summaries

Table 14-34973. ROM_TABLE_0_0 Registers, Base Address=0007 0000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_0_0_ROM_ENTRY0	0007 0000 0000h
4h	32	ROM_TABLE_0_0_ROM_ENTRY1	0007 0000 0004h
8h	32	ROM_TABLE_0_0_ROM_ENTRY2	0007 0000 0008h
8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY0	0007 0000 0008h
Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY1	0007 0000 000Ch
10h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY2	0007 0000 0010h
14h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY3	0007 0000 0014h
18h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY4	0007 0000 0018h
1Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY5	0007 0000 001Ch
20h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY6	0007 0000 0020h
24h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY7	0007 0000 0024h
28h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY8	0007 0000 0028h
2Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY9	0007 0000 002Ch
30h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY10	0007 0000 0030h
34h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY11	0007 0000 0034h
38h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY12	0007 0000 0038h
3Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY13	0007 0000 003Ch
40h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY14	0007 0000 0040h
44h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY15	0007 0000 0044h
48h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY16	0007 0000 0048h
4Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY17	0007 0000 004Ch
50h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY18	0007 0000 0050h
54h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY19	0007 0000 0054h
58h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY20	0007 0000 0058h
5Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY21	0007 0000 005Ch
60h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY22	0007 0000 0060h
64h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY23	0007 0000 0064h
68h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY24	0007 0000 0068h
6Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY25	0007 0000 006Ch
70h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY26	0007 0000 0070h
74h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY27	0007 0000 0074h
78h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY28	0007 0000 0078h
7Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY29	0007 0000 007Ch
80h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY30	0007 0000 0080h
84h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY31	0007 0000 0084h
88h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY32	0007 0000 0088h
8Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY33	0007 0000 008Ch
90h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY34	0007 0000 0090h

Table 14-34973. ROM_TABLE_0_0 Registers, Base Address=0007 0000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
94h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY35	0007 0000 0094h
98h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY36	0007 0000 0098h
9Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY37	0007 0000 009Ch
A0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY38	0007 0000 00A0h
A4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY39	0007 0000 00A4h
A8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY40	0007 0000 00A8h
ACh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY41	0007 0000 00ACh
B0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY42	0007 0000 00B0h
B4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY43	0007 0000 00B4h
B8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY44	0007 0000 00B8h
BCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY45	0007 0000 00BCh
C0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY46	0007 0000 00C0h
C4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY47	0007 0000 00C4h
C8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY48	0007 0000 00C8h
CCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY49	0007 0000 00CCh
D0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY50	0007 0000 00D0h
D4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY51	0007 0000 00D4h
D8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY52	0007 0000 00D8h
DCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY53	0007 0000 00DCh
E0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY54	0007 0000 00E0h
E4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY55	0007 0000 00E4h
E8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY56	0007 0000 00E8h
ECh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY57	0007 0000 00ECh
F0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY58	0007 0000 00F0h
F4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY59	0007 0000 00F4h
F8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY60	0007 0000 00F8h
FCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY61	0007 0000 00FCh
100h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY62	0007 0000 0100h
104h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY63	0007 0000 0104h
108h	32	ROM_TABLE_0_0_PERIPHID0	0007 0000 0108h
10Ch	32	ROM_TABLE_0_0_PERIPHID1	0007 0000 010Ch
110h	32	ROM_TABLE_0_0_PERIPHID2	0007 0000 0110h
114h	32	ROM_TABLE_0_0_PERIPHID3	0007 0000 0114h
118h	32	ROM_TABLE_0_0_PERIPHID4	0007 0000 0118h
3FCh	32	ROM_TABLE_0_0_COMPID0	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID1	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID2	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID3	0007 0000 03FCh

Table 14-34974. CFGAP_CFG_0 Registers, Base Address=0007 0000 2000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CFGAP_CFG_0_JTAGID_REG	0007 0000 2000h
4h	32	CFGAP_CFG_0_USERID_REG	0007 0000 2004h
8h	32	CFGAP_CFG_0_VERSION_REG	0007 0000 2008h

Table 14-34974. CFGAP_CFG_0 Registers, Base Address=0007 0000 2000h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
Ch	32	CFGAP_CFG_0_SYSTEMSTATUS	0007 0000 200Ch
FCh	32	CFGAP_CFG_0_APID_REGISTER	0007 0000 20FCh

Table 14-34975. APBAP_CFG_0 Registers, Base Address=0007 0000 2100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	APBAP_CFG_0_CSWREG	0007 0000 2100h
4h	32	APBAP_CFG_0_TAREG	0007 0000 2104h
Ch	32	APBAP_CFG_0_DRWREG	0007 0000 210Ch
10h	32	APBAP_CFG_0_BD0REG	0007 0000 2110h
14h	32	APBAP_CFG_0_BD1REG	0007 0000 2114h
18h	32	APBAP_CFG_0_BD2REG	0007 0000 2118h
1Ch	32	APBAP_CFG_0_BD3REG	0007 0000 211Ch
F8h	32	APBAP_CFG_0_ROM_REGISTER	0007 0000 21F8h
FCh	32	APBAP_CFG_0_ID_REGISTER	0007 0000 21FCh

Table 14-34976. AXIAP_CFG_0 Registers, Base Address=0007 0000 2200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	AXIAP_CFG_0_CSWREG	0007 0000 2200h
4h	32	AXIAP_CFG_0_TAREGL	0007 0000 2204h
8h	32	AXIAP_CFG_0_TAREGH	0007 0000 2208h
Ch	32	AXIAP_CFG_0_DRWREG	0007 0000 220Ch
10h	32	AXIAP_CFG_0_BD0REG	0007 0000 2210h
14h	32	AXIAP_CFG_0_BD1REG	0007 0000 2214h
18h	32	AXIAP_CFG_0_BD2REG	0007 0000 2218h
1Ch	32	AXIAP_CFG_0_BD3REG	0007 0000 221Ch
20h	32	AXIAP_CFG_0_MBT_REGISTER	0007 0000 2220h
F0h	32	AXIAP_CFG_0_ROM_HI_REGISTER	0007 0000 22F0h
F4h	32	AXIAP_CFG_0_CFG_REGISTER	0007 0000 22F4h
F8h	32	AXIAP_CFG_0_ROM_LO_REGISTER	0007 0000 22F8h
FCh	32	AXIAP_CFG_0_ID_REGISTER	0007 0000 22FCh

Table 14-34977. PWRAP_CFG_0 Registers, Base Address=0007 0000 2300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PWRAP_CFG_0_CORE_PRECREG0	0007 0000 2300h
4h	32	PWRAP_CFG_0_CORE_PRECREG1	0007 0000 2304h
8h	32	PWRAP_CFG_0_CORE_PRECREG2	0007 0000 2308h
Ch	32	PWRAP_CFG_0_CORE_PRECREG3	0007 0000 230Ch
10h	32	PWRAP_CFG_0_CORE_PRECREG4	0007 0000 2310h
14h	32	PWRAP_CFG_0_CORE_PRECREG5	0007 0000 2314h
18h	32	PWRAP_CFG_0_CORE_PRECREG6	0007 0000 2318h
1Ch	32	PWRAP_CFG_0_CORE_PRECREG7	0007 0000 231Ch
20h	32	PWRAP_CFG_0_CORE_PRECREG8	0007 0000 2320h
24h	32	PWRAP_CFG_0_CORE_PRECREG9	0007 0000 2324h

Table 14-34977. PWRAP_CFG_0 Registers, Base Address=0007 0000 2300h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
28h	32	PWRAP_CFG_0_CORE_PRECREG10	0007 0000 2328h
2Ch	32	PWRAP_CFG_0_CORE_PRECREG11	0007 0000 232Ch
30h	32	PWRAP_CFG_0_CORE_PRECREG12	0007 0000 2330h
34h	32	PWRAP_CFG_0_CORE_PRECREG13	0007 0000 2334h
38h	32	PWRAP_CFG_0_CORE_PRECREG14	0007 0000 2338h
3Ch	32	PWRAP_CFG_0_CORE_PRECREG15	0007 0000 233Ch
40h	32	PWRAP_CFG_0_CORE_PRECREG16	0007 0000 2340h
44h	32	PWRAP_CFG_0_CORE_PRECREG17	0007 0000 2344h
48h	32	PWRAP_CFG_0_CORE_PRECREG18	0007 0000 2348h
4Ch	32	PWRAP_CFG_0_CORE_PRECREG19	0007 0000 234Ch
50h	32	PWRAP_CFG_0_CORE_PRECREG20	0007 0000 2350h
54h	32	PWRAP_CFG_0_CORE_PRECREG21	0007 0000 2354h
58h	32	PWRAP_CFG_0_CORE_PRECREG22	0007 0000 2358h
5Ch	32	PWRAP_CFG_0_CORE_PRECREG23	0007 0000 235Ch
60h	32	PWRAP_CFG_0_CORE_PRECREG24	0007 0000 2360h
64h	32	PWRAP_CFG_0_CORE_PRECREG25	0007 0000 2364h
68h	32	PWRAP_CFG_0_CORE_PRECREG26	0007 0000 2368h
6Ch	32	PWRAP_CFG_0_CORE_PRECREG27	0007 0000 236Ch
70h	32	PWRAP_CFG_0_CORE_PRECREG28	0007 0000 2370h
74h	32	PWRAP_CFG_0_CORE_PRECREG29	0007 0000 2374h
78h	32	PWRAP_CFG_0_CORE_PRECREG30	0007 0000 2378h
7Ch	32	PWRAP_CFG_0_CORE_PRECREG31	0007 0000 237Ch
F0h	32	PWRAP_CFG_0_SYS_PRECREG	0007 0000 23F0h
FCh	32	PWRAP_CFG_0_ID_REGISTER	0007 0000 23FCh

Table 14-34978. PVIEW_CFG_0 Registers, Base Address=0007 0000 2400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PVIEW_CFG_0_PVIEW_STATE0	0007 0000 2400h
F0h	32	PVIEW_CFG_0_PVIEW_CAPABILITY	0007 0000 24F0h
FCh	32	PVIEW_CFG_0_ID_REGISTER	0007 0000 24FCh

Table 14-34979. JTAGAP_CFG_0 Registers, Base Address=0007 0000 2500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	JTAGAP_CFG_0_CSW	0007 0000 2500h
4h	32	JTAGAP_CFG_0_PSEL_REG	0007 0000 2504h
8h	32	JTAGAP_CFG_0_PSTA_REG	0007 0000 2508h
10h	32	JTAGAP_CFG_0_BYTEFIFO1	0007 0000 2510h
14h	32	JTAGAP_CFG_0_BYTEFIFO2	0007 0000 2514h
18h	32	JTAGAP_CFG_0_BYTEFIFO3	0007 0000 2518h
1Ch	32	JTAGAP_CFG_0_BYTEFIFO4	0007 0000 251Ch
FCh	32	JTAGAP_CFG_0_ID_REGISTER	0007 0000 25FCh

Table 14-34980. SECAP_CFG_0 Registers, Base Address=0007 0000 2600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	SECAP_CFG_0_TXDATA	0007 0000 2600h
4h	32	SECAP_CFG_0_TXCTRL	0007 0000 2604h
8h	32	SECAP_CFG_0_RXDATA	0007 0000 2608h
Ch	32	SECAP_CFG_0_RXCTRL	0007 0000 260Ch

Table 14-34981. CORTEX0_CFG_0 Registers, Base Address=0007 0000 2700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX0_CFG_0_CSWREG	0007 0000 2700h
4h	32	CORTEX0_CFG_0_TAREG	0007 0000 2704h
Ch	32	CORTEX0_CFG_0_DRWREG	0007 0000 270Ch
10h	32	CORTEX0_CFG_0_BD0REG	0007 0000 2710h
14h	32	CORTEX0_CFG_0_BD1REG	0007 0000 2714h
18h	32	CORTEX0_CFG_0_BD2REG	0007 0000 2718h
1Ch	32	CORTEX0_CFG_0_BD3REG	0007 0000 271Ch
F8h	32	CORTEX0_CFG_0_ROM_REGISTER	0007 0000 27F8h
FCh	32	CORTEX0_CFG_0_ID_REGISTER	0007 0000 27FCh

Table 14-34982. CORTEX1_CFG_0 Registers, Base Address=0007 0000 2800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX1_CFG_0_CSWREG	0007 0000 2800h
4h	32	CORTEX1_CFG_0_TAREG	0007 0000 2804h
Ch	32	CORTEX1_CFG_0_DRWREG	0007 0000 280Ch
10h	32	CORTEX1_CFG_0_BD0REG	0007 0000 2810h
14h	32	CORTEX1_CFG_0_BD1REG	0007 0000 2814h
18h	32	CORTEX1_CFG_0_BD2REG	0007 0000 2818h
1Ch	32	CORTEX1_CFG_0_BD3REG	0007 0000 281Ch
F8h	32	CORTEX1_CFG_0_ROM_REGISTER	0007 0000 28F8h
FCh	32	CORTEX1_CFG_0_ID_REGISTER	0007 0000 28FCh

Table 14-34983. CORTEX2_CFG_0 Registers, Base Address=0007 0000 2900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX2_CFG_0_CSWREG	0007 0000 2900h
4h	32	CORTEX2_CFG_0_TAREG	0007 0000 2904h
Ch	32	CORTEX2_CFG_0_DRWREG	0007 0000 290Ch
10h	32	CORTEX2_CFG_0_BD0REG	0007 0000 2910h
14h	32	CORTEX2_CFG_0_BD1REG	0007 0000 2914h
18h	32	CORTEX2_CFG_0_BD2REG	0007 0000 2918h
1Ch	32	CORTEX2_CFG_0_BD3REG	0007 0000 291Ch
F8h	32	CORTEX2_CFG_0_ROM_REGISTER	0007 0000 29F8h
FCh	32	CORTEX2_CFG_0_ID_REGISTER	0007 0000 29FCh

Table 14-34984. CORTEX3_CFG_0 Registers, Base Address=0007 0000 2A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX3_CFG_0_CSWREG	0007 0000 2A00h
4h	32	CORTEX3_CFG_0_TAREG	0007 0000 2A04h
Ch	32	CORTEX3_CFG_0_DRWREG	0007 0000 2A0Ch
10h	32	CORTEX3_CFG_0_BD0REG	0007 0000 2A10h
14h	32	CORTEX3_CFG_0_BD1REG	0007 0000 2A14h
18h	32	CORTEX3_CFG_0_BD2REG	0007 0000 2A18h
1Ch	32	CORTEX3_CFG_0_BD3REG	0007 0000 2A1Ch
F8h	32	CORTEX3_CFG_0_ROM_REGISTER	0007 0000 2AF8h
FCh	32	CORTEX3_CFG_0_ID_REGISTER	0007 0000 2AFCh

Table 14-34985. CORTEX4_CFG_0 Registers, Base Address=0007 0000 2B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX4_CFG_0_CSWREG	0007 0000 2B00h
4h	32	CORTEX4_CFG_0_TAREG	0007 0000 2B04h
Ch	32	CORTEX4_CFG_0_DRWREG	0007 0000 2B0Ch
10h	32	CORTEX4_CFG_0_BD0REG	0007 0000 2B10h
14h	32	CORTEX4_CFG_0_BD1REG	0007 0000 2B14h
18h	32	CORTEX4_CFG_0_BD2REG	0007 0000 2B18h
1Ch	32	CORTEX4_CFG_0_BD3REG	0007 0000 2B1Ch
F8h	32	CORTEX4_CFG_0_ROM_REGISTER	0007 0000 2BF8h
FCh	32	CORTEX4_CFG_0_ID_REGISTER	0007 0000 2BFCh

Table 14-34986. CORTEX5_CFG_0 Registers, Base Address=0007 0000 2C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX5_CFG_0_CSWREG	0007 0000 2C00h
4h	32	CORTEX5_CFG_0_TAREG	0007 0000 2C04h
Ch	32	CORTEX5_CFG_0_DRWREG	0007 0000 2C0Ch
10h	32	CORTEX5_CFG_0_BD0REG	0007 0000 2C10h
14h	32	CORTEX5_CFG_0_BD1REG	0007 0000 2C14h
18h	32	CORTEX5_CFG_0_BD2REG	0007 0000 2C18h
1Ch	32	CORTEX5_CFG_0_BD3REG	0007 0000 2C1Ch
F8h	32	CORTEX5_CFG_0_ROM_REGISTER	0007 0000 2CF8h
FCh	32	CORTEX5_CFG_0_ID_REGISTER	0007 0000 2CFCh

Table 14-34987. CORTEX6_CFG_0 Registers, Base Address=0007 0000 2D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX6_CFG_0_CSWREG	0007 0000 2D00h
4h	32	CORTEX6_CFG_0_TAREG	0007 0000 2D04h
Ch	32	CORTEX6_CFG_0_DRWREG	0007 0000 2D0Ch
10h	32	CORTEX6_CFG_0_BD0REG	0007 0000 2D10h
14h	32	CORTEX6_CFG_0_BD1REG	0007 0000 2D14h
18h	32	CORTEX6_CFG_0_BD2REG	0007 0000 2D18h
1Ch	32	CORTEX6_CFG_0_BD3REG	0007 0000 2D1Ch

Table 14-34987. CORTEX6_CFG_0 Registers, Base Address=0007 0000 2D00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
F8h	32	CORTEX6_CFG_0_ROM_REGISTER	0007 0000 2DF8h
FCh	32	CORTEX6_CFG_0_ID_REGISTER	0007 0000 2DFCh

Table 14-34988. CORTEX7_CFG_0 Registers, Base Address=0007 0000 2E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX7_CFG_0_CSWREG	0007 0000 2E00h
4h	32	CORTEX7_CFG_0_TAREG	0007 0000 2E04h
Ch	32	CORTEX7_CFG_0_DRWREG	0007 0000 2E0Ch
10h	32	CORTEX7_CFG_0_BD0REG	0007 0000 2E10h
14h	32	CORTEX7_CFG_0_BD1REG	0007 0000 2E14h
18h	32	CORTEX7_CFG_0_BD2REG	0007 0000 2E18h
1Ch	32	CORTEX7_CFG_0_BD3REG	0007 0000 2E1Ch
F8h	32	CORTEX7_CFG_0_ROM_REGISTER	0007 0000 2EF8h
FCh	32	CORTEX7_CFG_0_ID_REGISTER	0007 0000 2EFCh

Table 14-34989. CORTEX8_CFG_0 Registers, Base Address=0007 0000 2F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX8_CFG_0_CSWREG	0007 0000 2F00h
4h	32	CORTEX8_CFG_0_TAREG	0007 0000 2F04h
Ch	32	CORTEX8_CFG_0_DRWREG	0007 0000 2F0Ch
10h	32	CORTEX8_CFG_0_BD0REG	0007 0000 2F10h
14h	32	CORTEX8_CFG_0_BD1REG	0007 0000 2F14h
18h	32	CORTEX8_CFG_0_BD2REG	0007 0000 2F18h
1Ch	32	CORTEX8_CFG_0_BD3REG	0007 0000 2F1Ch
F8h	32	CORTEX8_CFG_0_ROM_REGISTER	0007 0000 2FF8h
FCh	32	CORTEX8_CFG_0_ID_REGISTER	0007 0000 2FFCh

Table 14-34990. ROM_TABLE_1_0 Registers, Base Address=0007 2000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_1_0_ROM_ENTRY0	0007 2000 0000h
4h	32	ROM_TABLE_1_0_ROM_ENTRY1	0007 2000 0004h
8h	32	ROM_TABLE_1_0_ROM_ENTRY2	0007 2000 0008h
Ch	32	ROM_TABLE_1_0_ROM_ENTRY3	0007 2000 000Ch
10h	32	ROM_TABLE_1_0_ROM_ENTRY4	0007 2000 0010h
14h	32	ROM_TABLE_1_0_ROM_ENTRY5	0007 2000 0014h
18h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER0	0007 2000 0018h
1Ch	32	ROM_TABLE_1_0_COMPUTE_CLUSTER1	0007 2000 001Ch
20h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER2	0007 2000 0020h
24h	32	ROM_TABLE_1_0_DEBUG_CELL0	0007 2000 0024h
28h	32	ROM_TABLE_1_0_DEBUG_CELL1	0007 2000 0028h
2Ch	32	ROM_TABLE_1_0_DEBUG_CELL2	0007 2000 002Ch
30h	32	ROM_TABLE_1_0_DEBUG_CELL3	0007 2000 0030h
34h	32	ROM_TABLE_1_0_DEBUG_CELL4	0007 2000 0034h

Table 14-34990. ROM_TABLE_1_0 Registers, Base Address=0007 2000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
38h	32	ROM_TABLE_1_0_DEBUG_CELL5	0007 2000 0038h
3Ch	32	ROM_TABLE_1_0_DEBUG_CELL6	0007 2000 003Ch
40h	32	ROM_TABLE_1_0_DEBUG_CELL7	0007 2000 0040h
44h	32	ROM_TABLE_1_0_DEBUG_CELL8	0007 2000 0044h
48h	32	ROM_TABLE_1_0_DEBUG_CELL9	0007 2000 0048h
4Ch	32	ROM_TABLE_1_0_DEBUG_CELL10	0007 2000 004Ch
50h	32	ROM_TABLE_1_0_DEBUG_CELL11	0007 2000 0050h
50h	32	ROM_TABLE_1_0_EXTCSCOMP0	0007 2000 0050h
54h	32	ROM_TABLE_1_0_EXTCSCOMP1	0007 2000 0054h
58h	32	ROM_TABLE_1_0_EXTCSCOMP2	0007 2000 0058h
5Ch	32	ROM_TABLE_1_0_EXTCSCOMP3	0007 2000 005Ch
60h	32	ROM_TABLE_1_0_EXTCSCOMP4	0007 2000 0060h
64h	32	ROM_TABLE_1_0_EXTCSCOMP5	0007 2000 0064h
68h	32	ROM_TABLE_1_0_EXTCSCOMP6	0007 2000 0068h
6Ch	32	ROM_TABLE_1_0_EXTCSCOMP7	0007 2000 006Ch
70h	32	ROM_TABLE_1_0_EXTCSCOMP8	0007 2000 0070h
74h	32	ROM_TABLE_1_0_EXTCSCOMP9	0007 2000 0074h
78h	32	ROM_TABLE_1_0_EXTCSCOMP10	0007 2000 0078h
7Ch	32	ROM_TABLE_1_0_EXTCSCOMP11	0007 2000 007Ch

Table 14-34991. CSCTI Registers, Base Address=0007 2000 1000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSCTI_CTICONTROL	0007 2000 1000h
10h	32	CSCTI_CTIINTACK	0007 2000 1010h
14h	32	CSCTI_CTIAPPSET	0007 2000 1014h
18h	32	CSCTI_CTIAPPCLR	0007 2000 1018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 2000 101Ch
20h	32	CSCTI_CTIINEN0	0007 2000 1020h
24h	32	CSCTI_CTIINEN1	0007 2000 1024h
28h	32	CSCTI_CTIINEN2	0007 2000 1028h
2Ch	32	CSCTI_CTIINEN3	0007 2000 102Ch
30h	32	CSCTI_CTIINEN4	0007 2000 1030h
34h	32	CSCTI_CTIINEN5	0007 2000 1034h
38h	32	CSCTI_CTIINEN6	0007 2000 1038h
3Ch	32	CSCTI_CTIINEN7	0007 2000 103Ch
A0h	32	CSCTI_CTIOUTEN0	0007 2000 10A0h
A4h	32	CSCTI_CTIOUTEN1	0007 2000 10A4h
A8h	32	CSCTI_CTIOUTEN2	0007 2000 10A8h
ACh	32	CSCTI_CTIOUTEN3	0007 2000 10ACh
B0h	32	CSCTI_CTIOUTEN4	0007 2000 10B0h
B4h	32	CSCTI_CTIOUTEN5	0007 2000 10B4h
B8h	32	CSCTI_CTIOUTEN6	0007 2000 10B8h
BCh	32	CSCTI_CTIOUTEN7	0007 2000 10BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 2000 1130h

Table 14-34991. CSCTI Registers, Base Address=0007 2000 1000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 2000 1134h
138h	32	CSCTI_CTICHINSTATUS	0007 2000 1138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 2000 113Ch
140h	32	CSCTI_CTIGATE	0007 2000 1140h
144h	32	CSCTI_ASICCTL	0007 2000 1144h
EDCh	32	CSCTI_ITCHINACK	0007 2000 1EDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 2000 1EE0h
EE4h	32	CSCTI_ITCHOUT	0007 2000 1EE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 2000 1EE8h
EECh	32	CSCTI_ITCHOUTACK	0007 2000 1EECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 2000 1EF0h
EF4h	32	CSCTI_ITCHIN	0007 2000 1EF4h
EF8h	32	CSCTI_ITTRIGIN	0007 2000 1EF8h
F00h	32	CSCTI_ITCTRL	0007 2000 1F00h
FA0h	32	CSCTI_CLAIMSET	0007 2000 1FA0h
FA4h	32	CSCTI_CLAIMCLR	0007 2000 1FA4h
FB0h	32	CSCTI_LOCKACCESS	0007 2000 1FB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 2000 1FB4h
FB8h	32	CSCTI_AUTHSTATUS	0007 2000 1FB8h
FC8h	32	CSCTI_DEVID	0007 2000 1FC8h
FCCh	32	CSCTI_DEVTYPE	0007 2000 1FCCh
FD0h	32	CSCTI_PERIPHID4	0007 2000 1FD0h
FE0h	32	CSCTI_PERIPHID0	0007 2000 1FE0h
FE4h	32	CSCTI_PERIPHID1	0007 2000 1FE4h
FE8h	32	CSCTI_PERIPHID2	0007 2000 1FE8h
FECh	32	CSCTI_PERIPHID3	0007 2000 1FECh
FF0h	32	CSCTI_COMPONID0	0007 2000 1FF0h
FF4h	32	CSCTI_COMPONID1	0007 2000 1FF4h
FF8h	32	CSCTI_COMPONID2	0007 2000 1FF8h
FFCh	32	CSCTI_COMPONID3	0007 2000 1FFCh

Table 14-34992. DRM_CFG_0 Registers, Base Address=0007 2000 2000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	DRM_CFG_0_PERIPH_ID	0007 2000 2000h
4h	32	DRM_CFG_0_VERSION	0007 2000 2004h
8h	32	DRM_CFG_0_CAPABILITY	0007 2000 2008h
Ch	32	DRM_CFG_0_TRACE_CTRL	0007 2000 200Ch
10h	32	DRM_CFG_0_VBUSM_CTRL	0007 2000 2010h
14h	32	DRM_CFG_0_DAP_TIMEOUT	0007 2000 2014h
18h	32	DRM_CFG_0_CONFIG	0007 2000 2018h
1Ch	32	DRM_CFG_0_EMUTRIGEN	0007 2000 201Ch
20h	32	DRM_CFG_0_BINVALLO	0007 2000 2020h
24h	32	DRM_CFG_0_BINVALHI	0007 2000 2024h
200h	32	DRM_CFG_0_SUSPEND_REG0	0007 2000 2200h

Table 14-34992. DRM_CFG_0 Registers, Base Address=0007 2000 2000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
204h	32	DRM_CFG_0_SUSPEND_REG1	0007 2000 2204h
208h	32	DRM_CFG_0_SUSPEND_REG2	0007 2000 2208h
20Ch	32	DRM_CFG_0_SUSPEND_REG3	0007 2000 220Ch
210h	32	DRM_CFG_0_SUSPEND_REG4	0007 2000 2210h
214h	32	DRM_CFG_0_SUSPEND_REG5	0007 2000 2214h
218h	32	DRM_CFG_0_SUSPEND_REG6	0007 2000 2218h
21Ch	32	DRM_CFG_0_SUSPEND_REG7	0007 2000 221Ch
220h	32	DRM_CFG_0_SUSPEND_REG8	0007 2000 2220h
224h	32	DRM_CFG_0_SUSPEND_REG9	0007 2000 2224h
228h	32	DRM_CFG_0_SUSPEND_REG10	0007 2000 2228h
22Ch	32	DRM_CFG_0_SUSPEND_REG11	0007 2000 222Ch
230h	32	DRM_CFG_0_SUSPEND_REG12	0007 2000 2230h
234h	32	DRM_CFG_0_SUSPEND_REG13	0007 2000 2234h
238h	32	DRM_CFG_0_SUSPEND_REG14	0007 2000 2238h
23Ch	32	DRM_CFG_0_SUSPEND_REG15	0007 2000 223Ch
240h	32	DRM_CFG_0_SUSPEND_REG16	0007 2000 2240h
244h	32	DRM_CFG_0_SUSPEND_REG17	0007 2000 2244h
248h	32	DRM_CFG_0_SUSPEND_REG18	0007 2000 2248h
24Ch	32	DRM_CFG_0_SUSPEND_REG19	0007 2000 224Ch
250h	32	DRM_CFG_0_SUSPEND_REG20	0007 2000 2250h
254h	32	DRM_CFG_0_SUSPEND_REG21	0007 2000 2254h
258h	32	DRM_CFG_0_SUSPEND_REG22	0007 2000 2258h
25Ch	32	DRM_CFG_0_SUSPEND_REG23	0007 2000 225Ch
260h	32	DRM_CFG_0_SUSPEND_REG24	0007 2000 2260h
264h	32	DRM_CFG_0_SUSPEND_REG25	0007 2000 2264h
268h	32	DRM_CFG_0_SUSPEND_REG26	0007 2000 2268h
26Ch	32	DRM_CFG_0_SUSPEND_REG27	0007 2000 226Ch
270h	32	DRM_CFG_0_SUSPEND_REG28	0007 2000 2270h
274h	32	DRM_CFG_0_SUSPEND_REG29	0007 2000 2274h
278h	32	DRM_CFG_0_SUSPEND_REG30	0007 2000 2278h
27Ch	32	DRM_CFG_0_SUSPEND_REG31	0007 2000 227Ch

Table 14-34993. CSTPIU_CFG_0 Registers, Base Address=0007 2000 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSTPIU_CFG_0_SUPPORTSIZE	0007 2000 4000h
4h	32	CSTPIU_CFG_0_CURPORTSIZE	0007 2000 4004h
100h	32	CSTPIU_CFG_0_TRIGMODEREG	0007 2000 4100h
104h	32	CSTPIU_CFG_0_TRIGCTRREG	0007 2000 4104h
108h	32	CSTPIU_CFG_0_TRIGMPYREG	0007 2000 4108h
200h	32	CSTPIU_CFG_0_SUPTESTPAT	0007 2000 4200h
204h	32	CSTPIU_CFG_0_CURTESTPAT	0007 2000 4204h
208h	32	CSTPIU_CFG_0_TESTPATCNT	0007 2000 4208h
300h	32	CSTPIU_CFG_0_FORMFLUSHSTAT	0007 2000 4300h
304h	32	CSTPIU_CFG_0_FORMFLUSHCTL	0007 2000 4304h

Table 14-34993. CSTPIU_CFG_0 Registers, Base Address=0007 2000 4000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
308h	32	CSTPIU_CFG_0_FORMSYNCCTR	0007 2000 4308h
400h	32	CSTPIU_CFG_0_EXTCTLIN	0007 2000 4400h
404h	32	CSTPIU_CFG_0_EXTCTLOUT	0007 2000 4404h
EE4h	32	CSTPIU_CFG_0_ITTRFLINACK	0007 2000 4EE4h
EE8h	32	CSTPIU_CFG_0_ITTRFLIN	0007 2000 4EE8h
EECh	32	CSTPIU_CFG_0_ITATBDATA0	0007 2000 4EECh
EF0h	32	CSTPIU_CFG_0_ITATBCTR2	0007 2000 4EF0h
EF4h	32	CSTPIU_CFG_0_ITATBCTR1	0007 2000 4EF4h
EF8h	32	CSTPIU_CFG_0_ITATBCTR0	0007 2000 4EF8h
F00h	32	CSTPIU_CFG_0_INTCTRL	0007 2000 4F00h
FA0h	32	CSTPIU_CFG_0_CTSET	0007 2000 4FA0h
FA4h	32	CSTPIU_CFG_0_CTCLR	0007 2000 4FA4h
FB0h	32	CSTPIU_CFG_0_LAREG	0007 2000 4FB0h
FB4h	32	CSTPIU_CFG_0_LSREG	0007 2000 4FB4h
FB8h	32	CSTPIU_CFG_0_AUTHST	0007 2000 4FB8h
FC8h	32	CSTPIU_CFG_0_DEVID	0007 2000 4FC8h
FCCh	32	CSTPIU_CFG_0_DEVTYPEID	0007 2000 4FCCh
FD0h	32	CSTPIU_CFG_0_PERID4	0007 2000 4FD0h
FE0h	32	CSTPIU_CFG_0_PERID0	0007 2000 4FE0h
FE4h	32	CSTPIU_CFG_0_PERID1	0007 2000 4FE4h
FE8h	32	CSTPIU_CFG_0_PERID2	0007 2000 4FE8h
FECh	32	CSTPIU_CFG_0_PERID3	0007 2000 4FECh
FF0h	32	CSTPIU_CFG_0_COMPID0	0007 2000 4FF0h
FF4h	32	CSTPIU_CFG_0_COMPID1	0007 2000 4FF4h
FF8h	32	CSTPIU_CFG_0_COMPID2	0007 2000 4FF8h
FFCh	32	CSTPIU_CFG_0_COMPID3	0007 2000 4FFCh

Table 14-34994. CTF_CFG_0 Registers, Base Address=0007 2000 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CTF_CFG_0_CSTFCTLREG	0007 2000 5000h
4h	32	CTF_CFG_0_PRIORCTLREG	0007 2000 5004h
EECh	32	CTF_CFG_0_ITATBDATA0	0007 2000 5EECh
EF0h	32	CTF_CFG_0_ITATBCTR2	0007 2000 5EF0h
EF4h	32	CTF_CFG_0_ITATBCTR1	0007 2000 5EF4h
EF8h	32	CTF_CFG_0_ITATBCTR0	0007 2000 5EF8h
F00h	32	CTF_CFG_0_INTCTRL	0007 2000 5F00h
FA0h	32	CTF_CFG_0_CTSET	0007 2000 5FA0h
FA4h	32	CTF_CFG_0_CTCLR	0007 2000 5FA4h
FB0h	32	CTF_CFG_0_LAREG	0007 2000 5FB0h
FB4h	32	CTF_CFG_0_LSREG	0007 2000 5FB4h
FB8h	32	CTF_CFG_0_AUTHST	0007 2000 5FB8h
FC8h	32	CTF_CFG_0_DEVID	0007 2000 5FC8h
FCCh	32	CTF_CFG_0_DEVTYPEID	0007 2000 5FCCh
FD0h	32	CTF_CFG_0_PERID4	0007 2000 5FD0h

Table 14-34994. CTF_CFG_0 Registers, Base Address=0007 2000 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FD4h	32	CTF_CFG_0_PERID5	0007 2000 5FD4h
FD8h	32	CTF_CFG_0_PERID6	0007 2000 5FD8h
FDCh	32	CTF_CFG_0_PERID7	0007 2000 5FDCh
FE0h	32	CTF_CFG_0_PERID0	0007 2000 5FE0h
FE4h	32	CTF_CFG_0_PERID1	0007 2000 5FE4h
FE8h	32	CTF_CFG_0_PERID2	0007 2000 5FE8h
FECh	32	CTF_CFG_0_PERID3	0007 2000 5FECh
FF0h	32	CTF_CFG_0_COMPID0	0007 2000 5FF0h
FF4h	32	CTF_CFG_0_COMPID1	0007 2000 5FF4h
FF8h	32	CTF_CFG_0_COMPID2	0007 2000 5FF8h
FFCh	32	CTF_CFG_0_COMPID3	0007 2000 5FFCh

Table 14-34995. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_0_1_ROM_ENTRY0	0007 4000 0000h
4h	32	ROM_TABLE_0_1_ROM_ENTRY1	0007 4000 0004h
8h	32	ROM_TABLE_0_1_ROM_ENTRY2	0007 4000 0008h
8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY0	0007 4000 0008h
Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY1	0007 4000 000Ch
10h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY2	0007 4000 0010h
14h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY3	0007 4000 0014h
18h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY4	0007 4000 0018h
1Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY5	0007 4000 001Ch
20h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY6	0007 4000 0020h
24h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY7	0007 4000 0024h
28h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY8	0007 4000 0028h
2Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY9	0007 4000 002Ch
30h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY10	0007 4000 0030h
34h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY11	0007 4000 0034h
38h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY12	0007 4000 0038h
3Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY13	0007 4000 003Ch
40h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY14	0007 4000 0040h
44h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY15	0007 4000 0044h
48h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY16	0007 4000 0048h
4Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY17	0007 4000 004Ch
50h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY18	0007 4000 0050h
54h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY19	0007 4000 0054h
58h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY20	0007 4000 0058h
5Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY21	0007 4000 005Ch
60h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY22	0007 4000 0060h
64h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY23	0007 4000 0064h
68h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY24	0007 4000 0068h
6Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY25	0007 4000 006Ch
70h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY26	0007 4000 0070h

Table 14-34995. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
74h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY27	0007 4000 0074h
78h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY28	0007 4000 0078h
7Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY29	0007 4000 007Ch
80h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY30	0007 4000 0080h
84h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY31	0007 4000 0084h
88h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY32	0007 4000 0088h
8Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY33	0007 4000 008Ch
90h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY34	0007 4000 0090h
94h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY35	0007 4000 0094h
98h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY36	0007 4000 0098h
9Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY37	0007 4000 009Ch
A0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY38	0007 4000 00A0h
A4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY39	0007 4000 00A4h
A8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY40	0007 4000 00A8h
ACh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY41	0007 4000 00ACh
B0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY42	0007 4000 00B0h
B4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY43	0007 4000 00B4h
B8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY44	0007 4000 00B8h
BCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY45	0007 4000 00BCh
C0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY46	0007 4000 00C0h
C4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY47	0007 4000 00C4h
C8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY48	0007 4000 00C8h
CCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY49	0007 4000 00CCh
D0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY50	0007 4000 00D0h
D4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY51	0007 4000 00D4h
D8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY52	0007 4000 00D8h
DCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY53	0007 4000 00DCh
E0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY54	0007 4000 00E0h
E4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY55	0007 4000 00E4h
E8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY56	0007 4000 00E8h
ECh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY57	0007 4000 00ECh
F0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY58	0007 4000 00F0h
F4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY59	0007 4000 00F4h
F8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY60	0007 4000 00F8h
FCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY61	0007 4000 00FCh
100h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY62	0007 4000 0100h
104h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY63	0007 4000 0104h
108h	32	ROM_TABLE_0_1_PERIPHID0	0007 4000 0108h
10Ch	32	ROM_TABLE_0_1_PERIPHID1	0007 4000 010Ch
110h	32	ROM_TABLE_0_1_PERIPHID2	0007 4000 0110h
114h	32	ROM_TABLE_0_1_PERIPHID3	0007 4000 0114h
118h	32	ROM_TABLE_0_1_PERIPHID4	0007 4000 0118h
3FCh	32	ROM_TABLE_0_1_COMPID0	0007 4000 03FCh
3FCh	32	ROM_TABLE_0_1_COMPID1	0007 4000 03FCh
3FCh	32	ROM_TABLE_0_1_COMPID2	0007 4000 03FCh

Table 14-34995. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
3FCh	32	ROM_TABLE_0_1_COMPID3	0007 4000 03FCh

Table 14-34996. CFGAP_CFG_1 Registers, Base Address=0007 4000 2000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CFGAP_CFG_1_JTAGID_REG	0007 4000 2000h
4h	32	CFGAP_CFG_1_USERID_REG	0007 4000 2004h
8h	32	CFGAP_CFG_1_VERSION_REG	0007 4000 2008h
Ch	32	CFGAP_CFG_1_SYSTEMSTATUS	0007 4000 200Ch
FCh	32	CFGAP_CFG_1_APID_REGISTER	0007 4000 20FCh

Table 14-34997. APBAP_CFG_1 Registers, Base Address=0007 4000 2100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	APBAP_CFG_1_CSWREG	0007 4000 2100h
4h	32	APBAP_CFG_1_TAREG	0007 4000 2104h
Ch	32	APBAP_CFG_1_DRWREG	0007 4000 210Ch
10h	32	APBAP_CFG_1_BD0REG	0007 4000 2110h
14h	32	APBAP_CFG_1_BD1REG	0007 4000 2114h
18h	32	APBAP_CFG_1_BD2REG	0007 4000 2118h
1Ch	32	APBAP_CFG_1_BD3REG	0007 4000 211Ch
F8h	32	APBAP_CFG_1_ROM_REGISTER	0007 4000 21F8h
FCh	32	APBAP_CFG_1_ID_REGISTER	0007 4000 21FCh

Table 14-34998. AXIAP_CFG_1 Registers, Base Address=0007 4000 2200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	AXIAP_CFG_1_CSWREG	0007 4000 2200h
4h	32	AXIAP_CFG_1_TAREGL	0007 4000 2204h
8h	32	AXIAP_CFG_1_TAREGH	0007 4000 2208h
Ch	32	AXIAP_CFG_1_DRWREG	0007 4000 220Ch
10h	32	AXIAP_CFG_1_BD0REG	0007 4000 2210h
14h	32	AXIAP_CFG_1_BD1REG	0007 4000 2214h
18h	32	AXIAP_CFG_1_BD2REG	0007 4000 2218h
1Ch	32	AXIAP_CFG_1_BD3REG	0007 4000 221Ch
20h	32	AXIAP_CFG_1_MBT_REGISTER	0007 4000 2220h
F0h	32	AXIAP_CFG_1_ROM_HI_REGISTER	0007 4000 22F0h
F4h	32	AXIAP_CFG_1_CFG_REGISTER	0007 4000 22F4h
F8h	32	AXIAP_CFG_1_ROM_LO_REGISTER	0007 4000 22F8h
FCh	32	AXIAP_CFG_1_ID_REGISTER	0007 4000 22FCh

Table 14-34999. PWRAP_CFG_1 Registers, Base Address=0007 4000 2300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PWRAP_CFG_1_CORE_PRECREG0	0007 4000 2300h
4h	32	PWRAP_CFG_1_CORE_PRECREG1	0007 4000 2304h
8h	32	PWRAP_CFG_1_CORE_PRECREG2	0007 4000 2308h

Table 14-34999. PWRAP_CFG_1 Registers, Base Address=0007 4000 2300h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
Ch	32	PWRAP_CFG_1_CORE_PRECREG3	0007 4000 230Ch
10h	32	PWRAP_CFG_1_CORE_PRECREG4	0007 4000 2310h
14h	32	PWRAP_CFG_1_CORE_PRECREG5	0007 4000 2314h
18h	32	PWRAP_CFG_1_CORE_PRECREG6	0007 4000 2318h
1Ch	32	PWRAP_CFG_1_CORE_PRECREG7	0007 4000 231Ch
20h	32	PWRAP_CFG_1_CORE_PRECREG8	0007 4000 2320h
24h	32	PWRAP_CFG_1_CORE_PRECREG9	0007 4000 2324h
28h	32	PWRAP_CFG_1_CORE_PRECREG10	0007 4000 2328h
2Ch	32	PWRAP_CFG_1_CORE_PRECREG11	0007 4000 232Ch
30h	32	PWRAP_CFG_1_CORE_PRECREG12	0007 4000 2330h
34h	32	PWRAP_CFG_1_CORE_PRECREG13	0007 4000 2334h
38h	32	PWRAP_CFG_1_CORE_PRECREG14	0007 4000 2338h
3Ch	32	PWRAP_CFG_1_CORE_PRECREG15	0007 4000 233Ch
40h	32	PWRAP_CFG_1_CORE_PRECREG16	0007 4000 2340h
44h	32	PWRAP_CFG_1_CORE_PRECREG17	0007 4000 2344h
48h	32	PWRAP_CFG_1_CORE_PRECREG18	0007 4000 2348h
4Ch	32	PWRAP_CFG_1_CORE_PRECREG19	0007 4000 234Ch
50h	32	PWRAP_CFG_1_CORE_PRECREG20	0007 4000 2350h
54h	32	PWRAP_CFG_1_CORE_PRECREG21	0007 4000 2354h
58h	32	PWRAP_CFG_1_CORE_PRECREG22	0007 4000 2358h
5Ch	32	PWRAP_CFG_1_CORE_PRECREG23	0007 4000 235Ch
60h	32	PWRAP_CFG_1_CORE_PRECREG24	0007 4000 2360h
64h	32	PWRAP_CFG_1_CORE_PRECREG25	0007 4000 2364h
68h	32	PWRAP_CFG_1_CORE_PRECREG26	0007 4000 2368h
6Ch	32	PWRAP_CFG_1_CORE_PRECREG27	0007 4000 236Ch
70h	32	PWRAP_CFG_1_CORE_PRECREG28	0007 4000 2370h
74h	32	PWRAP_CFG_1_CORE_PRECREG29	0007 4000 2374h
78h	32	PWRAP_CFG_1_CORE_PRECREG30	0007 4000 2378h
7Ch	32	PWRAP_CFG_1_CORE_PRECREG31	0007 4000 237Ch
F0h	32	PWRAP_CFG_1_SYS_PRECREG	0007 4000 23F0h
FCh	32	PWRAP_CFG_1_ID_REGISTER	0007 4000 23FCh

Table 14-35000. PVIEW_CFG_1 Registers, Base Address=0007 4000 2400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PVIEW_CFG_1_PVIEW_STATE0	0007 4000 2400h
F0h	32	PVIEW_CFG_1_PVIEW_CAPABILITY	0007 4000 24F0h
FCh	32	PVIEW_CFG_1_ID_REGISTER	0007 4000 24FCh

Table 14-35001. JTAGAP_CFG_1 Registers, Base Address=0007 4000 2500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	JTAGAP_CFG_1_CSW	0007 4000 2500h
4h	32	JTAGAP_CFG_1_PSEL_REG	0007 4000 2504h
8h	32	JTAGAP_CFG_1_PSTA_REG	0007 4000 2508h
10h	32	JTAGAP_CFG_1_BYTEFIFO1	0007 4000 2510h

Table 14-35001. JTAGAP_CFG_1 Registers, Base Address=0007 4000 2500h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
14h	32	JTAGAP_CFG_1_BYTEFIFO2	0007 4000 2514h
18h	32	JTAGAP_CFG_1_BYTEFIFO3	0007 4000 2518h
1Ch	32	JTAGAP_CFG_1_BYTEFIFO4	0007 4000 251Ch
FCh	32	JTAGAP_CFG_1_ID_REGISTER	0007 4000 25FCh

Table 14-35002. SECAP_CFG_1 Registers, Base Address=0007 4000 2600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	SECAP_CFG_1_TXDATA	0007 4000 2600h
4h	32	SECAP_CFG_1_TXCTRL	0007 4000 2604h
8h	32	SECAP_CFG_1_RXDATA	0007 4000 2608h
Ch	32	SECAP_CFG_1_RXCTRL	0007 4000 260Ch

Table 14-35003. CORTEX0_CFG_1 Registers, Base Address=0007 4000 2700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX0_CFG_1_CSWREG	0007 4000 2700h
4h	32	CORTEX0_CFG_1_TAREG	0007 4000 2704h
Ch	32	CORTEX0_CFG_1_DRWREG	0007 4000 270Ch
10h	32	CORTEX0_CFG_1_BD0REG	0007 4000 2710h
14h	32	CORTEX0_CFG_1_BD1REG	0007 4000 2714h
18h	32	CORTEX0_CFG_1_BD2REG	0007 4000 2718h
1Ch	32	CORTEX0_CFG_1_BD3REG	0007 4000 271Ch
F8h	32	CORTEX0_CFG_1_ROM_REGISTER	0007 4000 27F8h
FCh	32	CORTEX0_CFG_1_ID_REGISTER	0007 4000 27FCh

Table 14-35004. CORTEX1_CFG_1 Registers, Base Address=0007 4000 2800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX1_CFG_1_CSWREG	0007 4000 2800h
4h	32	CORTEX1_CFG_1_TAREG	0007 4000 2804h
Ch	32	CORTEX1_CFG_1_DRWREG	0007 4000 280Ch
10h	32	CORTEX1_CFG_1_BD0REG	0007 4000 2810h
14h	32	CORTEX1_CFG_1_BD1REG	0007 4000 2814h
18h	32	CORTEX1_CFG_1_BD2REG	0007 4000 2818h
1Ch	32	CORTEX1_CFG_1_BD3REG	0007 4000 281Ch
F8h	32	CORTEX1_CFG_1_ROM_REGISTER	0007 4000 28F8h
FCh	32	CORTEX1_CFG_1_ID_REGISTER	0007 4000 28FCh

Table 14-35005. CORTEX2_CFG_1 Registers, Base Address=0007 4000 2900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX2_CFG_1_CSWREG	0007 4000 2900h
4h	32	CORTEX2_CFG_1_TAREG	0007 4000 2904h
Ch	32	CORTEX2_CFG_1_DRWREG	0007 4000 290Ch
10h	32	CORTEX2_CFG_1_BD0REG	0007 4000 2910h
14h	32	CORTEX2_CFG_1_BD1REG	0007 4000 2914h

Table 14-35005. CORTEX2_CFG_1 Registers, Base Address=0007 4000 2900h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
18h	32	CORTEX2_CFG_1_BD2REG	0007 4000 2918h
1Ch	32	CORTEX2_CFG_1_BD3REG	0007 4000 291Ch
F8h	32	CORTEX2_CFG_1_ROM_REGISTER	0007 4000 29F8h
FCh	32	CORTEX2_CFG_1_ID_REGISTER	0007 4000 29FCh

Table 14-35006. CORTEX3_CFG_1 Registers, Base Address=0007 4000 2A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX3_CFG_1_CSWREG	0007 4000 2A00h
4h	32	CORTEX3_CFG_1_TAREG	0007 4000 2A04h
Ch	32	CORTEX3_CFG_1_DRWREG	0007 4000 2A0Ch
10h	32	CORTEX3_CFG_1_BD0REG	0007 4000 2A10h
14h	32	CORTEX3_CFG_1_BD1REG	0007 4000 2A14h
18h	32	CORTEX3_CFG_1_BD2REG	0007 4000 2A18h
1Ch	32	CORTEX3_CFG_1_BD3REG	0007 4000 2A1Ch
F8h	32	CORTEX3_CFG_1_ROM_REGISTER	0007 4000 2AF8h
FCh	32	CORTEX3_CFG_1_ID_REGISTER	0007 4000 2AFCh

Table 14-35007. CORTEX4_CFG_1 Registers, Base Address=0007 4000 2B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX4_CFG_1_CSWREG	0007 4000 2B00h
4h	32	CORTEX4_CFG_1_TAREG	0007 4000 2B04h
Ch	32	CORTEX4_CFG_1_DRWREG	0007 4000 2B0Ch
10h	32	CORTEX4_CFG_1_BD0REG	0007 4000 2B10h
14h	32	CORTEX4_CFG_1_BD1REG	0007 4000 2B14h
18h	32	CORTEX4_CFG_1_BD2REG	0007 4000 2B18h
1Ch	32	CORTEX4_CFG_1_BD3REG	0007 4000 2B1Ch
F8h	32	CORTEX4_CFG_1_ROM_REGISTER	0007 4000 2BF8h
FCh	32	CORTEX4_CFG_1_ID_REGISTER	0007 4000 2BFCh

Table 14-35008. CORTEX5_CFG_1 Registers, Base Address=0007 4000 2C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX5_CFG_1_CSWREG	0007 4000 2C00h
4h	32	CORTEX5_CFG_1_TAREG	0007 4000 2C04h
Ch	32	CORTEX5_CFG_1_DRWREG	0007 4000 2C0Ch
10h	32	CORTEX5_CFG_1_BD0REG	0007 4000 2C10h
14h	32	CORTEX5_CFG_1_BD1REG	0007 4000 2C14h
18h	32	CORTEX5_CFG_1_BD2REG	0007 4000 2C18h
1Ch	32	CORTEX5_CFG_1_BD3REG	0007 4000 2C1Ch
F8h	32	CORTEX5_CFG_1_ROM_REGISTER	0007 4000 2CF8h
FCh	32	CORTEX5_CFG_1_ID_REGISTER	0007 4000 2CFCh

Table 14-35009. CORTEX6_CFG_1 Registers, Base Address=0007 4000 2D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX6_CFG_1_CSWREG	0007 4000 2D00h
4h	32	CORTEX6_CFG_1_TAREG	0007 4000 2D04h
Ch	32	CORTEX6_CFG_1_DRWREG	0007 4000 2D0Ch
10h	32	CORTEX6_CFG_1_BD0REG	0007 4000 2D10h
14h	32	CORTEX6_CFG_1_BD1REG	0007 4000 2D14h
18h	32	CORTEX6_CFG_1_BD2REG	0007 4000 2D18h
1Ch	32	CORTEX6_CFG_1_BD3REG	0007 4000 2D1Ch
F8h	32	CORTEX6_CFG_1_ROM_REGISTER	0007 4000 2DF8h
FCh	32	CORTEX6_CFG_1_ID_REGISTER	0007 4000 2DFCh

Table 14-35010. CORTEX7_CFG_1 Registers, Base Address=0007 4000 2E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX7_CFG_1_CSWREG	0007 4000 2E00h
4h	32	CORTEX7_CFG_1_TAREG	0007 4000 2E04h
Ch	32	CORTEX7_CFG_1_DRWREG	0007 4000 2E0Ch
10h	32	CORTEX7_CFG_1_BD0REG	0007 4000 2E10h
14h	32	CORTEX7_CFG_1_BD1REG	0007 4000 2E14h
18h	32	CORTEX7_CFG_1_BD2REG	0007 4000 2E18h
1Ch	32	CORTEX7_CFG_1_BD3REG	0007 4000 2E1Ch
F8h	32	CORTEX7_CFG_1_ROM_REGISTER	0007 4000 2EF8h
FCh	32	CORTEX7_CFG_1_ID_REGISTER	0007 4000 2EFCh

Table 14-35011. CORTEX8_CFG_1 Registers, Base Address=0007 4000 2F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX8_CFG_1_CSWREG	0007 4000 2F00h
4h	32	CORTEX8_CFG_1_TAREG	0007 4000 2F04h
Ch	32	CORTEX8_CFG_1_DRWREG	0007 4000 2F0Ch
10h	32	CORTEX8_CFG_1_BD0REG	0007 4000 2F10h
14h	32	CORTEX8_CFG_1_BD1REG	0007 4000 2F14h
18h	32	CORTEX8_CFG_1_BD2REG	0007 4000 2F18h
1Ch	32	CORTEX8_CFG_1_BD3REG	0007 4000 2F1Ch
F8h	32	CORTEX8_CFG_1_ROM_REGISTER	0007 4000 2FF8h
FCh	32	CORTEX8_CFG_1_ID_REGISTER	0007 4000 2FFCh

Table 14-35012. ROM_TABLE_1_1 Registers, Base Address=0007 6000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_1_1_ROM_ENTRY0	0007 6000 0000h
4h	32	ROM_TABLE_1_1_ROM_ENTRY1	0007 6000 0004h
8h	32	ROM_TABLE_1_1_ROM_ENTRY2	0007 6000 0008h
Ch	32	ROM_TABLE_1_1_ROM_ENTRY3	0007 6000 000Ch
10h	32	ROM_TABLE_1_1_ROM_ENTRY4	0007 6000 0010h
14h	32	ROM_TABLE_1_1_ROM_ENTRY5	0007 6000 0014h
18h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER0	0007 6000 0018h

Table 14-35012. ROM_TABLE_1_1 Registers, Base Address=0007 6000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
1Ch	32	ROM_TABLE_1_1_COMPUTE_CLUSTER1	0007 6000 001Ch
20h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER2	0007 6000 0020h
24h	32	ROM_TABLE_1_1_DEBUG_CELL0	0007 6000 0024h
28h	32	ROM_TABLE_1_1_DEBUG_CELL1	0007 6000 0028h
2Ch	32	ROM_TABLE_1_1_DEBUG_CELL2	0007 6000 002Ch
30h	32	ROM_TABLE_1_1_DEBUG_CELL3	0007 6000 0030h
34h	32	ROM_TABLE_1_1_DEBUG_CELL4	0007 6000 0034h
38h	32	ROM_TABLE_1_1_DEBUG_CELL5	0007 6000 0038h
3Ch	32	ROM_TABLE_1_1_DEBUG_CELL6	0007 6000 003Ch
40h	32	ROM_TABLE_1_1_DEBUG_CELL7	0007 6000 0040h
44h	32	ROM_TABLE_1_1_DEBUG_CELL8	0007 6000 0044h
48h	32	ROM_TABLE_1_1_DEBUG_CELL9	0007 6000 0048h
4Ch	32	ROM_TABLE_1_1_DEBUG_CELL10	0007 6000 004Ch
50h	32	ROM_TABLE_1_1_DEBUG_CELL11	0007 6000 0050h
50h	32	ROM_TABLE_1_1_EXTCSCOMP0	0007 6000 0050h
54h	32	ROM_TABLE_1_1_EXTCSCOMP1	0007 6000 0054h
58h	32	ROM_TABLE_1_1_EXTCSCOMP2	0007 6000 0058h
5Ch	32	ROM_TABLE_1_1_EXTCSCOMP3	0007 6000 005Ch
60h	32	ROM_TABLE_1_1_EXTCSCOMP4	0007 6000 0060h
64h	32	ROM_TABLE_1_1_EXTCSCOMP5	0007 6000 0064h
68h	32	ROM_TABLE_1_1_EXTCSCOMP6	0007 6000 0068h
6Ch	32	ROM_TABLE_1_1_EXTCSCOMP7	0007 6000 006Ch
70h	32	ROM_TABLE_1_1_EXTCSCOMP8	0007 6000 0070h
74h	32	ROM_TABLE_1_1_EXTCSCOMP9	0007 6000 0074h
78h	32	ROM_TABLE_1_1_EXTCSCOMP10	0007 6000 0078h
7Ch	32	ROM_TABLE_1_1_EXTCSCOMP11	0007 6000 007Ch

Table 14-35013. CSCTI Registers, Base Address=0007 6000 1000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSCTI_CTICONTROL	0007 6000 1000h
10h	32	CSCTI_CTIINTACK	0007 6000 1010h
14h	32	CSCTI_CTIAPPSET	0007 6000 1014h
18h	32	CSCTI_CTIAPPCLR	0007 6000 1018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 6000 101Ch
20h	32	CSCTI_CTIINEN0	0007 6000 1020h
24h	32	CSCTI_CTIINEN1	0007 6000 1024h
28h	32	CSCTI_CTIINEN2	0007 6000 1028h
2Ch	32	CSCTI_CTIINEN3	0007 6000 102Ch
30h	32	CSCTI_CTIINEN4	0007 6000 1030h
34h	32	CSCTI_CTIINEN5	0007 6000 1034h
38h	32	CSCTI_CTIINEN6	0007 6000 1038h
3Ch	32	CSCTI_CTIINEN7	0007 6000 103Ch
A0h	32	CSCTI_CTIOUTEN0	0007 6000 10A0h
A4h	32	CSCTI_CTIOUTEN1	0007 6000 10A4h

Table 14-35013. CSCTI Registers, Base Address=0007 6000 1000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
A8h	32	CSCTI_CTIOUTEN2	0007 6000 10A8h
ACh	32	CSCTI_CTIOUTEN3	0007 6000 10ACh
B0h	32	CSCTI_CTIOUTEN4	0007 6000 10B0h
B4h	32	CSCTI_CTIOUTEN5	0007 6000 10B4h
B8h	32	CSCTI_CTIOUTEN6	0007 6000 10B8h
BCh	32	CSCTI_CTIOUTEN7	0007 6000 10BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 6000 1130h
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 6000 1134h
138h	32	CSCTI_CTICHINSTATUS	0007 6000 1138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 6000 113Ch
140h	32	CSCTI_CTIGATE	0007 6000 1140h
144h	32	CSCTI_ASICCTL	0007 6000 1144h
EDCh	32	CSCTI_ITCHINACK	0007 6000 1EDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 6000 1EE0h
EE4h	32	CSCTI_ITCHOUT	0007 6000 1EE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 6000 1EE8h
EECh	32	CSCTI_ITCHOUTACK	0007 6000 1EECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 6000 1EF0h
EF4h	32	CSCTI_ITCHIN	0007 6000 1EF4h
EF8h	32	CSCTI_ITTRIGIN	0007 6000 1EF8h
F00h	32	CSCTI_ITCTRL	0007 6000 1F00h
FA0h	32	CSCTI_CLAIMSET	0007 6000 1FA0h
FA4h	32	CSCTI_CLAIMCLR	0007 6000 1FA4h
FB0h	32	CSCTI_LOCKACCESS	0007 6000 1FB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 6000 1FB4h
FB8h	32	CSCTI_AUTHSTATUS	0007 6000 1FB8h
FC8h	32	CSCTI_DEVID	0007 6000 1FC8h
FCCh	32	CSCTI_DEVTYPE	0007 6000 1FCCh
FD0h	32	CSCTI_PERIPHID4	0007 6000 1FD0h
FE0h	32	CSCTI_PERIPHID0	0007 6000 1FE0h
FE4h	32	CSCTI_PERIPHID1	0007 6000 1FE4h
FE8h	32	CSCTI_PERIPHID2	0007 6000 1FE8h
FECh	32	CSCTI_PERIPHID3	0007 6000 1FECh
FF0h	32	CSCTI_COMPONID0	0007 6000 1FF0h
FF4h	32	CSCTI_COMPONID1	0007 6000 1FF4h
FF8h	32	CSCTI_COMPONID2	0007 6000 1FF8h
FFCh	32	CSCTI_COMPONID3	0007 6000 1FFCh

Table 14-35014. DRM_CFG_1 Registers, Base Address=0007 6000 2000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	DRM_CFG_1_PERIPH_ID	0007 6000 2000h
4h	32	DRM_CFG_1_VERSION	0007 6000 2004h
8h	32	DRM_CFG_1_CAPABILITY	0007 6000 2008h
Ch	32	DRM_CFG_1_TRACE_CTRL	0007 6000 200Ch

Table 14-35014. DRM_CFG_1 Registers, Base Address=0007 6000 2000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
10h	32	DRM_CFG_1_VBUSM_CTRL	0007 6000 2010h
14h	32	DRM_CFG_1_DAP_TIMEOUT	0007 6000 2014h
18h	32	DRM_CFG_1_CONFIG	0007 6000 2018h
1Ch	32	DRM_CFG_1_EMUTRIGEN	0007 6000 201Ch
20h	32	DRM_CFG_1_BINVALLO	0007 6000 2020h
24h	32	DRM_CFG_1_BINVALHI	0007 6000 2024h
200h	32	DRM_CFG_1_SUSPEND_REG0	0007 6000 2200h
204h	32	DRM_CFG_1_SUSPEND_REG1	0007 6000 2204h
208h	32	DRM_CFG_1_SUSPEND_REG2	0007 6000 2208h
20Ch	32	DRM_CFG_1_SUSPEND_REG3	0007 6000 220Ch
210h	32	DRM_CFG_1_SUSPEND_REG4	0007 6000 2210h
214h	32	DRM_CFG_1_SUSPEND_REG5	0007 6000 2214h
218h	32	DRM_CFG_1_SUSPEND_REG6	0007 6000 2218h
21Ch	32	DRM_CFG_1_SUSPEND_REG7	0007 6000 221Ch
220h	32	DRM_CFG_1_SUSPEND_REG8	0007 6000 2220h
224h	32	DRM_CFG_1_SUSPEND_REG9	0007 6000 2224h
228h	32	DRM_CFG_1_SUSPEND_REG10	0007 6000 2228h
22Ch	32	DRM_CFG_1_SUSPEND_REG11	0007 6000 222Ch
230h	32	DRM_CFG_1_SUSPEND_REG12	0007 6000 2230h
234h	32	DRM_CFG_1_SUSPEND_REG13	0007 6000 2234h
238h	32	DRM_CFG_1_SUSPEND_REG14	0007 6000 2238h
23Ch	32	DRM_CFG_1_SUSPEND_REG15	0007 6000 223Ch
240h	32	DRM_CFG_1_SUSPEND_REG16	0007 6000 2240h
244h	32	DRM_CFG_1_SUSPEND_REG17	0007 6000 2244h
248h	32	DRM_CFG_1_SUSPEND_REG18	0007 6000 2248h
24Ch	32	DRM_CFG_1_SUSPEND_REG19	0007 6000 224Ch
250h	32	DRM_CFG_1_SUSPEND_REG20	0007 6000 2250h
254h	32	DRM_CFG_1_SUSPEND_REG21	0007 6000 2254h
258h	32	DRM_CFG_1_SUSPEND_REG22	0007 6000 2258h
25Ch	32	DRM_CFG_1_SUSPEND_REG23	0007 6000 225Ch
260h	32	DRM_CFG_1_SUSPEND_REG24	0007 6000 2260h
264h	32	DRM_CFG_1_SUSPEND_REG25	0007 6000 2264h
268h	32	DRM_CFG_1_SUSPEND_REG26	0007 6000 2268h
26Ch	32	DRM_CFG_1_SUSPEND_REG27	0007 6000 226Ch
270h	32	DRM_CFG_1_SUSPEND_REG28	0007 6000 2270h
274h	32	DRM_CFG_1_SUSPEND_REG29	0007 6000 2274h
278h	32	DRM_CFG_1_SUSPEND_REG30	0007 6000 2278h
27Ch	32	DRM_CFG_1_SUSPEND_REG31	0007 6000 227Ch

Table 14-35015. CSTPIU_CFG_1 Registers, Base Address=0007 6000 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSTPIU_CFG_1_SUPPORTSIZE	0007 6000 4000h
4h	32	CSTPIU_CFG_1_CURPORTSIZE	0007 6000 4004h
100h	32	CSTPIU_CFG_1_TRIGMODEREG	0007 6000 4100h

Table 14-35015. CSTPIU_CFG_1 Registers, Base Address=0007 6000 4000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
104h	32	CSTPIU_CFG_1_TRIGCTRREG	0007 6000 4104h
108h	32	CSTPIU_CFG_1_TRIGMPYREG	0007 6000 4108h
200h	32	CSTPIU_CFG_1_SUPTESTPAT	0007 6000 4200h
204h	32	CSTPIU_CFG_1_CURTESTPAT	0007 6000 4204h
208h	32	CSTPIU_CFG_1_TESTPATCNT	0007 6000 4208h
300h	32	CSTPIU_CFG_1_FORMFLUSHSTAT	0007 6000 4300h
304h	32	CSTPIU_CFG_1_FORMFLUSHCTL	0007 6000 4304h
308h	32	CSTPIU_CFG_1_FORMSYNCCTR	0007 6000 4308h
400h	32	CSTPIU_CFG_1_EXTCTLIN	0007 6000 4400h
404h	32	CSTPIU_CFG_1_EXTCTLOUT	0007 6000 4404h
EE4h	32	CSTPIU_CFG_1_ITTRFLINACK	0007 6000 4EE4h
EE8h	32	CSTPIU_CFG_1_ITTRFLIN	0007 6000 4EE8h
EECh	32	CSTPIU_CFG_1_ITATBDATA0	0007 6000 4EECh
EF0h	32	CSTPIU_CFG_1_ITATBCTR2	0007 6000 4EF0h
EF4h	32	CSTPIU_CFG_1_ITATBCTR1	0007 6000 4EF4h
EF8h	32	CSTPIU_CFG_1_ITATBCTR0	0007 6000 4EF8h
F00h	32	CSTPIU_CFG_1_INTCTRL	0007 6000 4F00h
FA0h	32	CSTPIU_CFG_1_CTSET	0007 6000 4FA0h
FA4h	32	CSTPIU_CFG_1_CTCLR	0007 6000 4FA4h
FB0h	32	CSTPIU_CFG_1_LAREG	0007 6000 4FB0h
FB4h	32	CSTPIU_CFG_1_LSREG	0007 6000 4FB4h
FB8h	32	CSTPIU_CFG_1_AUTHST	0007 6000 4FB8h
FC8h	32	CSTPIU_CFG_1_DEVID	0007 6000 4FC8h
FCCh	32	CSTPIU_CFG_1_DEVTYPEID	0007 6000 4FCCh
FD0h	32	CSTPIU_CFG_1_PERID4	0007 6000 4FD0h
FE0h	32	CSTPIU_CFG_1_PERID0	0007 6000 4FE0h
FE4h	32	CSTPIU_CFG_1_PERID1	0007 6000 4FE4h
FE8h	32	CSTPIU_CFG_1_PERID2	0007 6000 4FE8h
FECh	32	CSTPIU_CFG_1_PERID3	0007 6000 4FECh
FF0h	32	CSTPIU_CFG_1_COMPID0	0007 6000 4FF0h
FF4h	32	CSTPIU_CFG_1_COMPID1	0007 6000 4FF4h
FF8h	32	CSTPIU_CFG_1_COMPID2	0007 6000 4FF8h
FFCh	32	CSTPIU_CFG_1_COMPID3	0007 6000 4FFCh

Table 14-35016. CTF_CFG_1 Registers, Base Address=0007 6000 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CTF_CFG_1_CSTFCTLREG	0007 6000 5000h
4h	32	CTF_CFG_1_PRIORCTLREG	0007 6000 5004h
EECh	32	CTF_CFG_1_ITATBDATA0	0007 6000 5EECh
EF0h	32	CTF_CFG_1_ITATBCTR2	0007 6000 5EF0h
EF4h	32	CTF_CFG_1_ITATBCTR1	0007 6000 5EF4h
EF8h	32	CTF_CFG_1_ITATBCTR0	0007 6000 5EF8h
F00h	32	CTF_CFG_1_INTCTRL	0007 6000 5F00h
FA0h	32	CTF_CFG_1_CTSET	0007 6000 5FA0h

Table 14-35016. CTF_CFG_1 Registers, Base Address=0007 6000 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FA4h	32	CTF_CFG_1_CTCLR	0007 6000 5FA4h
FB0h	32	CTF_CFG_1_LAREG	0007 6000 5FB0h
FB4h	32	CTF_CFG_1_LSREG	0007 6000 5FB4h
FB8h	32	CTF_CFG_1_AUTHST	0007 6000 5FB8h
FC8h	32	CTF_CFG_1_DEVID	0007 6000 5FC8h
FCCh	32	CTF_CFG_1_DEVTYPEID	0007 6000 5FCCh
FD0h	32	CTF_CFG_1_PERID4	0007 6000 5FD0h
FD4h	32	CTF_CFG_1_PERID5	0007 6000 5FD4h
FD8h	32	CTF_CFG_1_PERID6	0007 6000 5FD8h
FDCh	32	CTF_CFG_1_PERID7	0007 6000 5FDCh
FE0h	32	CTF_CFG_1_PERID0	0007 6000 5FE0h
FE4h	32	CTF_CFG_1_PERID1	0007 6000 5FE4h
FE8h	32	CTF_CFG_1_PERID2	0007 6000 5FE8h
FECh	32	CTF_CFG_1_PERID3	0007 6000 5FECh
FF0h	32	CTF_CFG_1_COMPID0	0007 6000 5FF0h
FF4h	32	CTF_CFG_1_COMPID1	0007 6000 5FF4h
FF8h	32	CTF_CFG_1_COMPID2	0007 6000 5FF8h
FFCh	32	CTF_CFG_1_COMPID3	0007 6000 5FFCh

14.10.2.2 DEBUGSS_WRAP Registers

DEBUGSS_WRAP Registers

14.10.2.2.1 ROM_TABLE_0_0_ROM_ENTRY0 Register

1 ROM_TABLE_0_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

rom table entry 0

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Table 14-35017. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0000h**

Figure 14-11579. ROM_TABLE_0_0_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
2h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35019. ROM_TABLE_0_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.2 ROM_TABLE_0_0_ROM_ENTRY1 Register

1 ROM_TABLE_0_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

rom table entry 1

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Table 14-35020. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0004h**

Figure 14-11580. ROM_TABLE_0_0_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2000h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-35022. ROM_TABLE_0_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.3 ROM_TABLE_0_0_ROM_ENTRY2 Register

1 ROM_TABLE_0_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

rom table entry 2

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Table 14-35023. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0008h**

Figure 14-11581. ROM_TABLE_0_0_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-35025. ROM_TABLE_0_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.4 ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

rom table manual entry 0

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Table 14-35026. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0008h**

Figure 14-11582. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35028. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.5 ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

rom table manual entry 1

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Table 14-35029. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 000Ch**

Figure 14-11583. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35031. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.6 ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

rom table manual entry 2

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Table 14-35032. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0010h**

Figure 14-11584. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35034. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.7 ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

rom table manual entry 3

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Table 14-35035. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0014h**

Figure 14-11585. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35037. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.8 ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

rom table manual entry 4

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Table 14-35038. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0018h**

Figure 14-11586. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35040. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.9 ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

rom table manual entry 5

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Table 14-35041. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 001Ch**

Figure 14-11587. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35043. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.10 ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

rom table manual entry 6

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Table 14-35044. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0020h**

Figure 14-11588. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35046. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.11 ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

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Table 14-35047. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0024h**

Figure 14-11589. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35049. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.12 ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

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Table 14-35050. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0028h**

Figure 14-11590. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35052. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.13 ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

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Table 14-35053. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 002Ch**

Figure 14-11591. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35055. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.14 ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

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Table 14-35056. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0030h**

Figure 14-11592. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35058. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.15 ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

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Table 14-35059. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0034h**

Figure 14-11593. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35061. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.16 ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

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Table 14-35062. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0038h**

Figure 14-11594. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35064. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.17 ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

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Table 14-35065. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 003Ch**

Figure 14-11595. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35067. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.18 ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

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Table 14-35068. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0040h**

Figure 14-11596. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35070. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.19 ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

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Table 14-35071. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0044h**

Figure 14-11597. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35073. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.20 ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

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Table 14-35074. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0048h**

Figure 14-11598. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35076. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.21 ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

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Table 14-35077. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 004Ch**

Figure 14-11599. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35079. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.22 ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

rom table manual entry 18

Return to Summary Table

Table 14-35080. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0050h**

Figure 14-11600. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35082. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.23 ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

rom table manual entry 19

Return to Summary Table

Table 14-35083. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0054h**

Figure 14-11601. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35085. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.24 ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

rom table manual entry 20

Return to Summary Table

Table 14-35086. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0058h**

Figure 14-11602. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35088. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.25 ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

rom table manual entry 21

Return to Summary Table

Table 14-35089. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 005Ch**

Figure 14-11603. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35091. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.26 ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

rom table manual entry 22

Return to Summary Table

Table 14-35092. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0060h**

Figure 14-11604. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35094. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.27 ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

rom table manual entry 23

Return to Summary Table

Table 14-35095. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	**0007 0000 0064h**

Figure 14-11605. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35097. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.28 ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

rom table manual entry 24

Return to Summary Table

Table 14-35098. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0068h**

Figure 14-11606. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35100. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.29 ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

rom table manual entry 25

Return to Summary Table

Table 14-35101. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 006Ch**

Figure 14-11607. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35103. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.30 ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

rom table manual entry 26

Return to Summary Table

Table 14-35104. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0070h**

Figure 14-11608. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35106. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.31 ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

rom table manual entry 27

Return to Summary Table

Table 14-35107. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0074h**

Figure 14-11609. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35109. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.32 ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

rom table manual entry 28

Return to Summary Table

Table 14-35110. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0078h**

Figure 14-11610. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35112. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.33 ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

rom table manual entry 29

Return to Summary Table

Table 14-35113. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 007Ch**

Figure 14-11611. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35115. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.34 ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

rom table manual entry 30

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Table 14-35116. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0080h**

Figure 14-11612. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35118. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.35 ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

rom table manual entry 31

Return to Summary Table

Table 14-35119. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0084h**

Figure 14-11613. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35121. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.36 ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

rom table manual entry 32

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Table 14-35122. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0088h**

Figure 14-11614. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35124. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.37 ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

rom table manual entry 33

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Table 14-35125. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 008Ch**

Figure 14-11615. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35127. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.38 ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

rom table manual entry 34

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Table 14-35128. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0090h**

Figure 14-11616. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35130. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.39 ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

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Table 14-35131. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0094h**

Figure 14-11617. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35133. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.40 ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

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Table 14-35134. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0098h**

Figure 14-11618. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35136. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.41 ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

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Table 14-35137. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 009Ch**

Figure 14-11619. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35139. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.42 ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

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Table 14-35140. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00A0h**

Figure 14-11620. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35142. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.43 ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

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Table 14-35143. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00A4h**

Figure 14-11621. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35145. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.44 ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

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Table 14-35146. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00A8h**

Figure 14-11622. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35148. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.45 ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

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Table 14-35149. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00ACh**

Figure 14-11623. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35151. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.46 ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

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Table 14-35152. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00B0h**

Figure 14-11624. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35154. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.47 ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-35155. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00B4h**

Figure 14-11625. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35157. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.48 ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

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Table 14-35158. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00B8h**

Figure 14-11626. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35160. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.49 ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

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Table 14-35161. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00BCh**

Figure 14-11627. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35163. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.50 ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-35164. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00C0h**

Figure 14-11628. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35166. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.51 ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

rom table manual entry 47

Return to Summary Table

Table 14-35167. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00C4h**

Figure 14-11629. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35169. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.52 ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

rom table manual entry 48

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Table 14-35170. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00C8h**

Figure 14-11630. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35172. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.53 ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

rom table manual entry 49

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Table 14-35173. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00CCh**

Figure 14-11631. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35175. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.54 ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

rom table manual entry 50

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Table 14-35176. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00D0h**

Figure 14-11632. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35178. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.55 ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

rom table manual entry 51

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Table 14-35179. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00D4h**

Figure 14-11633. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35181. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.56 ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

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Table 14-35182. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00D8h**

Figure 14-11634. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35184. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.57 ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

rom table manual entry 53

Return to Summary Table

Table 14-35185. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00DCh**

Figure 14-11635. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35187. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.58 ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

rom table manual entry 54

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Table 14-35188. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00E0h**

Figure 14-11636. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35190. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.59 ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

rom table manual entry 55

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Table 14-35191. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00E4h**

Figure 14-11637. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35193. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.60 ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

rom table manual entry 56

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Table 14-35194. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00E8h**

Figure 14-11638. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35196. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.61 ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

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Table 14-35197. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00ECh**

Figure 14-11639. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35199. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.62 ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

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Table 14-35200. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00F0h**

Figure 14-11640. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35202. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.63 ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

rom table manual entry 59

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Table 14-35203. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00F4h**

Figure 14-11641. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35205. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.64 ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

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Table 14-35206. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 00F8h**

Figure 14-11642. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-35208. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.65 ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

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Table 14-35209. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00FCh

Figure 14-11643. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35211. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.66 ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

rom table manual entry 62

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Table 14-35212. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0100h**

Figure 14-11644. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35214. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.67 ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register

1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

rom table manual entry 63

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Table 14-35215. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0104h**

Figure 14-11645. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-35217. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.68 ROM_TABLE_0_0_PERIPHID0 Register

1 ROM_TABLE_0_0_PERIPHID0 Register (Offset = 108h) [reset = 2h]

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Table 14-35218. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0108h

Figure 14-11646. ROM_TABLE_0_0_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35220. ROM_TABLE_0_0_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.69 ROM_TABLE_0_0_PERIPHID1 Register

1 ROM_TABLE_0_0_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

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Table 14-35221. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 010Ch**

Figure 14-11647. ROM_TABLE_0_0_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35223. ROM_TABLE_0_0_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.70 ROM_TABLE_0_0_PERIPHID2 Register

1 ROM_TABLE_0_0_PERIPHID2 Register (Offset = 110h) [reset = 2h]

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Table 14-35224. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0110h**

Figure 14-11648. ROM_TABLE_0_0_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35226. ROM_TABLE_0_0_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.71 ROM_TABLE_0_0_PERIPHID3 Register

1 ROM_TABLE_0_0_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-35227. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0114h**

Figure 14-11649. ROM_TABLE_0_0_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35229. ROM_TABLE_0_0_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.72 ROM_TABLE_0_0_PERIPHID4 Register

1 ROM_TABLE_0_0_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-35230. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 0118h**

Figure 14-11650. ROM_TABLE_0_0_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35232. ROM_TABLE_0_0_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.73 ROM_TABLE_0_0_COMPID0 Register

1 ROM_TABLE_0_0_COMPID0 Register (Offset = 3FCh) [reset = Dh]

component id

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Table 14-35233. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 03FCh**

Figure 14-11651. ROM_TABLE_0_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
Dh							
23	22	21	20	19	18	17	16
VAR							
R							
Dh							
15	14	13	12	11	10	9	8
VAR							
R							
Dh							
7	6	5	4	3	2	1	0
VAR							
R							
Dh							

Table 14-35235. ROM_TABLE_0_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.10.2.2.74 ROM_TABLE_0_0_COMPID1 Register

1 ROM_TABLE_0_0_COMPID1 Register (Offset = 3FCh) [reset = 10h]

component id

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Table 14-35236. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 03FCh**

Figure 14-11652. ROM_TABLE_0_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAR							
R							
10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAR							
R							
10h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAR							
R							
10h							

Table 14-35238. ROM_TABLE_0_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.10.2.2.75 ROM_TABLE_0_0_COMPID2 Register

1 ROM_TABLE_0_0_COMPID2 Register (Offset = 3FCh) [reset = 5h]

component id

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Table 14-35239. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 03FCh**

Figure 14-11653. ROM_TABLE_0_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-35241. ROM_TABLE_0_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.10.2.2.76 ROM_TABLE_0_0_COMPID3 Register

1 ROM_TABLE_0_0_COMPID3 Register (Offset = 3FCh) [reset = B1h]

component id

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Table 14-35242. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 03FCh**

Figure 14-11654. ROM_TABLE_0_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
B1h							
23	22	21	20	19	18	17	16
VAR							
R							
B1h							
15	14	13	12	11	10	9	8
VAR							
R							
B1h							
7	6	5	4	3	2	1	0
VAR							
R							
B1h							

Table 14-35244. ROM_TABLE_0_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.10.2.2.77 CFGAP_CFG_0_JTAGID_REG Register

1 CFGAP_CFG_0_JTAGID_REG Register (Offset = 0h) [reset = 0h]

This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-35245. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2000h**

Figure 14-11655. CFGAP_CFG_0_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-35247. CFGAP_CFG_0_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.10.2.2.78 CFGAP_CFG_0_USERID_REG Register

1 CFGAP_CFG_0_USERID_REG Register (Offset = 4h) [reset = 0h]

This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-35248. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2004h**

Figure 14-11656. CFGAP_CFG_0_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-35250. CFGAP_CFG_0_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.10.2.2.79 CFGAP_CFG_0_VERSION_REG Register

1 CFGAP_CFG_0_VERSION_REG Register (Offset = 8h) [reset = 0h]

This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-35251. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2008h**

Figure 14-11657. CFGAP_CFG_0_VERSION_REG Name Register

31	30	29	28	27	26	25	24
MAJOR_REV				MINOR_REV			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							JTAG_AP
R							R
0h							0h
7	6	5	4	3	2	1	0
POWERAP	AXIAP	APBAP	SECURITYAP	SPARE	ICEPICKM	TRIGGERSUPPORT	TRACESUPPORT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-35253. CFGAP_CFG_0_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.10.2.2.80 CFGAP_CFG_0_SYSTEMSTATUS Register

1 CFGAP_CFG_0_SYSTEMSTATUS Register (Offset = Ch) [reset = 0h]

Reading this register returns system status information.

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Table 14-35254. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 200Ch**

Figure 14-11658. CFGAP_CFG_0_SYSTEMSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-35256. CFGAP_CFG_0_SYSTEMSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved, returns 0

14.10.2.2.81 CFGAP_CFG_0_APID_REGISTER Register

1 CFGAP_CFG_0_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Reading this register returns the ID information for this AP.

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Table 14-35257. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 20FCh**

Figure 14-11659. CFGAP_CFG_0_APID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				107h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
107h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				1h			

Table 14-35259. CFGAP_CFG_0_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.82 APBAP_CFG_0_CSWREG Register

1 APBAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Control/Status Register

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Table 14-35260. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2100h**

Figure 14-11660. APBAP_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35262. APBAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.83 APBAP_CFG_0_TAREG Register

1 APBAP_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35263. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2104h**

Figure 14-11661. APBAP_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							

Table 14-35265. APBAP_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANSFER_ADDRESS_REGISTER	R/W	0h	This register contains the address to write to or read from

14.10.2.2.84 APBAP_CFG_0_DRWREG Register

1 APBAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35266. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 210Ch**

Figure 14-11662. APBAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35268. APBAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.85 APBAP_CFG_0_BD0REG Register

1 APBAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35269. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2110h**

Figure 14-11663. APBAP_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35271. APBAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.86 APBAP_CFG_0_BD1REG Register

1 APBAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35272. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2114h**

Figure 14-11664. APBAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35274. APBAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.87 APBAP_CFG_0_BD2REG Register

1 APBAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35275. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2118h**

Figure 14-11665. APBAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35277. APBAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.88 APBAP_CFG_0_BD3REG Register

1 APBAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35278. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 211Ch**

Figure 14-11666. APBAP_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35280. APBAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.89 APBAP_CFG_0_ROM_REGISTER Register

1 APBAP_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the APB ROM Address.

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Table 14-35281. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 21F8h**

Figure 14-11667. APBAP_CFG_0_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35283. APBAP_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.10.2.2.90 APBAP_CFG_0_ID_REGISTER Register

1 APBAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35284. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 21FCh**

Figure 14-11668. APBAP_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35286. APBAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.10.2.2.91 AXIAP_CFG_0_CSWREG Register

1 AXIAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This is the control/status register

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Table 14-35287. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2200h**

Figure 14-11669. AXIAP_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
DBGSWEN	TYPEEXT						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPIDEN	RESERVED2						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TYPE				MODE			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRINPROG	RESERVED1	ADDR_INC		RESERVED0	SIZE		
R	R	R/W		R	R		
0h	0h	0h		0h	0h		

Table 14-35289. AXIAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.10.2.2.92 AXIAP_CFG_0_TAREGL Register

1 AXIAP_CFG_0_TAREGL Register (Offset = 4h) [reset = 0h]

This register contains the lower 32-bits of address to write to or read from.

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Table 14-35290. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2204h**

Figure 14-11670. AXIAP_CFG_0_TAREGL Name Register

31	30	29	28	27	26	25	24
TAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TAL							
R/W							
0h							

Table 14-35292. AXIAP_CFG_0_TAREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAL	R/W	0h	This register contains the lower 32-bits of address

14.10.2.2.93 AXIAP_CFG_0_TAREGH Register

1 AXIAP_CFG_0_TAREGH Register (Offset = 8h) [reset = 0h]

This register contains the upper 32-bits of address to write to or read from.

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Table 14-35293. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2208h**

Figure 14-11671. AXIAP_CFG_0_TAREGH Name Register

31	30	29	28	27	26	25	24
TAH							
R/W							
0h							
23	22	21	20	19	18	17	16
TAH							
R/W							
0h							
15	14	13	12	11	10	9	8
TAH							
R/W							
0h							
7	6	5	4	3	2	1	0
TAH							
R/W							
0h							

Table 14-35295. AXIAP_CFG_0_TAREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAH	R/W	0h	This register contains the upper 32-bits of address

14.10.2.2.94 AXIAP_CFG_0_DRWREG Register

1 AXIAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35296. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 220Ch**

Figure 14-11672. AXIAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35298. AXIAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.95 AXIAP_CFG_0_BD0REG Register

1 AXIAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35299. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2210h**

Figure 14-11673. AXIAP_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35301. AXIAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.96 AXIAP_CFG_0_BD1REG Register

1 AXIAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35302. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2214h**

Figure 14-11674. AXIAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35304. AXIAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.97 AXIAP_CFG_0_BD2REG Register

1 AXIAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35305. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2218h**

Figure 14-11675. AXIAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35307. AXIAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.98 AXIAP_CFG_0_BD3REG Register

1 AXIAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35308. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 221Ch**

Figure 14-11676. AXIAP_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35310. AXIAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.99 AXIAP_CFG_0_MBT_REGISTER Register

1 AXIAP_CFG_0_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

This register sets memory barrier attributes

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Table 14-35311. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2220h**

Figure 14-11677. AXIAP_CFG_0_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-35313. AXIAP_CFG_0_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.10.2.2.100 AXIAP_CFG_0_ROM_HI_REGISTER Register

1 AXIAP_CFG_0_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Reading this register returns the AXI ROM Address (63-32).

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Table 14-35314. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 22F0h**

Figure 14-11678. AXIAP_CFG_0_ROM_HI_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_HI_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_HI_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_HI_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_HI_REGISTER_ADDRESS							
R							
0h							

Table 14-35316. AXIAP_CFG_0_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.10.2.2.101 AXIAP_CFG_0_CFG_REGISTER Register

1 AXIAP_CFG_0_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-35317. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 22F4h**

Figure 14-11679. AXIAP_CFG_0_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-35319. AXIAP_CFG_0_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.10.2.2.102 AXIAP_CFG_0_ROM_LO_REGISTER Register

1 AXIAP_CFG_0_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AXI ROM Address (31:12) .

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Table 14-35320. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 22F8h**

Figure 14-11680. AXIAP_CFG_0_ROM_LO_REGISTER Name Register

31	30	29	28	27	26	25	24
LOWBASE							
R							
0h							
23	22	21	20	19	18	17	16
LOWBASE							
R							
0h							
15	14	13	12	11	10	9	8
LOWBASE				RESERVED			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						FORMAT	PRESENT
R						R	R
0h						0h	0h

Table 14-35322. AXIAP_CFG_0_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.10.2.2.103 AXIAP_CFG_0_ID_REGISTER Register

1 AXIAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35323. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 22FCh**

Figure 14-11681. AXIAP_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35325. AXIAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.10.2.2.104 PWRAP_CFG_0_CORE_PRECREG0 Register

1 PWRAP_CFG_0_CORE_PRECREG0 Register (Offset = 0h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. There can be upto 32 of these registers

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Table 14-35326. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2300h**

Figure 14-11682. PWRAP_CFG_0_CORE_PRECREG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RETENTION	RST_OCCURED	PWR_LOSS_DET	INHIBIT_SLEEP	DEBUG_POWER	UNNAT_RESET	IN_RESET_RLS_WIR	RESET_MODE
R	R/W	R/W	R/W	R/W	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESET_MODE		DEBUG_ENABLE	RSV11_12		EXEC_ACTION_DEBUG_ATTEN	RSV8_9	
R/W		R/W	R		R/W	R	
0h		0h	0h		0h	0h	
7	6	5	4	3	2	1	0
PWRDOWNSRD	RSV6	POWERED	CLKDOWNSRD	FORCE_ACTIVE	CLOCKED	SECURITY	PRESENT
R	R	R	R	R/W	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-35328. PWRAP_CFG_0_CORE_PRECREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23	RETENTION	R	0h	Core is in retention mode
22	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
21	PWR_LOSS_DET	R/W	0h	Power Loss Detected Sticky bit, write a 1 to clear this bit
20	INHIBIT_SLEEP	R/W	0h	Inhinit Sleep Block core from entering sleep mode
19	DEBUG_POWER	R/W	0h	Core debug logic is powered
18	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
17	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the WIR When read this returns the reset status, 1 indicates core is in reset
16:14	RESET_MODE	R/W	0h	Reset Mode 0=normal, 1=WIR, 2=Blk Rst, 3=Blk Assert, 4=Halt on Rst, 5=Cancel, 6=Halt and Block, 7=Halt-Blk-assert
13	DEBUG_ENABLE	R/W	0h	Debug Enabled signal to the core
12:11	RSV11_12	R	0h	Reserved, return 0
10	EXEC_ACTION_DEBUG_ATTEN	R/W	0h	Writing this bit causes Execution Read will return the Debug Attention input value

Table 14-35328. PWRAP_CFG_0_CORE_PRECREG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RSV8_9	R	0h	Reserved, returns 0 when read
7	PWRDOWNDSRD	R	0h	The core wants to turn off it's power when high
6	RSV6	R	0h	Reserved, returns 0 when read
5	POWERED	R	0h	Core is powered up when high
4	CLKDOWNDSRD	R	0h	The core wants to turn off it's clock when high
3	FORCE_ACTIVE	R/W	0h	Force core active Turn on power and clocks
2	CLOCKED	R	0h	When high the core clock is active
1	SECURITY	R	0h	Security bit When high security is allowing access
0	PRESENT	R	0h	The core controlled by this register exists when 1

14.10.2.2.105 PWRAP_CFG_0_CORE_PRECREG1 Register

1 PWRAP_CFG_0_CORE_PRECREG1 Register (Offset = 4h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35329. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2304h**

Figure 14-11683. PWRAP_CFG_0_CORE_PRECREG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35331. PWRAP_CFG_0_CORE_PRECREG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.106 PWRAP_CFG_0_CORE_PRECREG2 Register

1 PWRAP_CFG_0_CORE_PRECREG2 Register (Offset = 8h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35332. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2308h**

Figure 14-11684. PWRAP_CFG_0_CORE_PRECREG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35334. PWRAP_CFG_0_CORE_PRECREG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.107 PWRAP_CFG_0_CORE_PRECREG3 Register

1 PWRAP_CFG_0_CORE_PRECREG3 Register (Offset = Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35335. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 230Ch**

Figure 14-11685. PWRAP_CFG_0_CORE_PRECREG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35337. PWRAP_CFG_0_CORE_PRECREG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.108 PWRAP_CFG_0_CORE_PRECREG4 Register

1 PWRAP_CFG_0_CORE_PRECREG4 Register (Offset = 10h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35338. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2310h**

Figure 14-11686. PWRAP_CFG_0_CORE_PRECREG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35340. PWRAP_CFG_0_CORE_PRECREG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.109 PWRAP_CFG_0_CORE_PRECREG5 Register

1 PWRAP_CFG_0_CORE_PRECREG5 Register (Offset = 14h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35341. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2314h**

Figure 14-11687. PWRAP_CFG_0_CORE_PRECREG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35343. PWRAP_CFG_0_CORE_PRECREG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.110 PWRAP_CFG_0_CORE_PRECREG6 Register

1 PWRAP_CFG_0_CORE_PRECREG6 Register (Offset = 18h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35344. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2318h**

Figure 14-11688. PWRAP_CFG_0_CORE_PRECREG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35346. PWRAP_CFG_0_CORE_PRECREG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.111 PWRAP_CFG_0_CORE_PRECREG7 Register

1 PWRAP_CFG_0_CORE_PRECREG7 Register (Offset = 1Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35347. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 231Ch**

Figure 14-11689. PWRAP_CFG_0_CORE_PRECREG7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35349. PWRAP_CFG_0_CORE_PRECREG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.112 PWRAP_CFG_0_CORE_PRECREG8 Register

1 PWRAP_CFG_0_CORE_PRECREG8 Register (Offset = 20h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35350. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2320h**

Figure 14-11690. PWRAP_CFG_0_CORE_PRECREG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35352. PWRAP_CFG_0_CORE_PRECREG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.113 PWRAP_CFG_0_CORE_PRECREG9 Register

1 PWRAP_CFG_0_CORE_PRECREG9 Register (Offset = 24h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35353. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2324h**

Figure 14-11691. PWRAP_CFG_0_CORE_PRECREG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35355. PWRAP_CFG_0_CORE_PRECREG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.114 PWRAP_CFG_0_CORE_PRECREG10 Register

1 PWRAP_CFG_0_CORE_PRECREG10 Register (Offset = 28h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35356. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2328h**

Figure 14-11692. PWRAP_CFG_0_CORE_PRECREG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35358. PWRAP_CFG_0_CORE_PRECREG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.115 PWRAP_CFG_0_CORE_PRECREG11 Register

1 PWRAP_CFG_0_CORE_PRECREG11 Register (Offset = 2Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35359. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 232Ch**

Figure 14-11693. PWRAP_CFG_0_CORE_PRECREG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35361. PWRAP_CFG_0_CORE_PRECREG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.116 PWRAP_CFG_0_CORE_PRECREG12 Register

1 PWRAP_CFG_0_CORE_PRECREG12 Register (Offset = 30h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35362. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2330h**

Figure 14-11694. PWRAP_CFG_0_CORE_PRECREG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35364. PWRAP_CFG_0_CORE_PRECREG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.117 PWRAP_CFG_0_CORE_PRECREG13 Register

1 PWRAP_CFG_0_CORE_PRECREG13 Register (Offset = 34h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35365. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2334h**

Figure 14-11695. PWRAP_CFG_0_CORE_PRECREG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35367. PWRAP_CFG_0_CORE_PRECREG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.118 PWRAP_CFG_0_CORE_PRECREG14 Register

1 PWRAP_CFG_0_CORE_PRECREG14 Register (Offset = 38h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35368. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2338h**

Figure 14-11696. PWRAP_CFG_0_CORE_PRECREG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35370. PWRAP_CFG_0_CORE_PRECREG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.119 PWRAP_CFG_0_CORE_PRECREG15 Register

1 PWRAP_CFG_0_CORE_PRECREG15 Register (Offset = 3Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35371. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 233Ch**

Figure 14-11697. PWRAP_CFG_0_CORE_PRECREG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35373. PWRAP_CFG_0_CORE_PRECREG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.120 PWRAP_CFG_0_CORE_PRECREG16 Register

1 PWRAP_CFG_0_CORE_PRECREG16 Register (Offset = 40h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35374. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2340h**

Figure 14-11698. PWRAP_CFG_0_CORE_PRECREG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35376. PWRAP_CFG_0_CORE_PRECREG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.121 PWRAP_CFG_0_CORE_PRECREG17 Register

1 PWRAP_CFG_0_CORE_PRECREG17 Register (Offset = 44h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35377. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2344h**

Figure 14-11699. PWRAP_CFG_0_CORE_PRECREG17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35379. PWRAP_CFG_0_CORE_PRECREG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.122 PWRAP_CFG_0_CORE_PRECREG18 Register

1 PWRAP_CFG_0_CORE_PRECREG18 Register (Offset = 48h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35380. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2348h**

Figure 14-11700. PWRAP_CFG_0_CORE_PRECREG18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35382. PWRAP_CFG_0_CORE_PRECREG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.123 PWRAP_CFG_0_CORE_PRECREG19 Register

1 PWRAP_CFG_0_CORE_PRECREG19 Register (Offset = 4Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35383. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 234Ch**

Figure 14-11701. PWRAP_CFG_0_CORE_PRECREG19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35385. PWRAP_CFG_0_CORE_PRECREG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.124 PWRAP_CFG_0_CORE_PRECREG20 Register

1 PWRAP_CFG_0_CORE_PRECREG20 Register (Offset = 50h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35386. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2350h**

Figure 14-11702. PWRAP_CFG_0_CORE_PRECREG20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35388. PWRAP_CFG_0_CORE_PRECREG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.125 PWRAP_CFG_0_CORE_PRECREG21 Register

1 PWRAP_CFG_0_CORE_PRECREG21 Register (Offset = 54h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35389. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2354h**

Figure 14-11703. PWRAP_CFG_0_CORE_PRECREG21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35391. PWRAP_CFG_0_CORE_PRECREG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.126 PWRAP_CFG_0_CORE_PRECREG22 Register

1 PWRAP_CFG_0_CORE_PRECREG22 Register (Offset = 58h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35392. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2358h**

Figure 14-11704. PWRAP_CFG_0_CORE_PRECREG22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35394. PWRAP_CFG_0_CORE_PRECREG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.127 PWRAP_CFG_0_CORE_PRECREG23 Register

1 PWRAP_CFG_0_CORE_PRECREG23 Register (Offset = 5Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35395. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 235Ch**

Figure 14-11705. PWRAP_CFG_0_CORE_PRECREG23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35397. PWRAP_CFG_0_CORE_PRECREG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.128 PWRAP_CFG_0_CORE_PRECREG24 Register

1 PWRAP_CFG_0_CORE_PRECREG24 Register (Offset = 60h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35398. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2360h**

Figure 14-11706. PWRAP_CFG_0_CORE_PRECREG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35400. PWRAP_CFG_0_CORE_PRECREG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.129 PWRAP_CFG_0_CORE_PRECREG25 Register

1 PWRAP_CFG_0_CORE_PRECREG25 Register (Offset = 64h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35401. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2364h**

Figure 14-11707. PWRAP_CFG_0_CORE_PRECREG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35403. PWRAP_CFG_0_CORE_PRECREG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.130 PWRAP_CFG_0_CORE_PRECREG26 Register

1 PWRAP_CFG_0_CORE_PRECREG26 Register (Offset = 68h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35404. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2368h**

Figure 14-11708. PWRAP_CFG_0_CORE_PRECREG26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35406. PWRAP_CFG_0_CORE_PRECREG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.131 PWRAP_CFG_0_CORE_PRECREG27 Register

1 PWRAP_CFG_0_CORE_PRECREG27 Register (Offset = 6Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35407. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 236Ch**

Figure 14-11709. PWRAP_CFG_0_CORE_PRECREG27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35409. PWRAP_CFG_0_CORE_PRECREG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.132 PWRAP_CFG_0_CORE_PRECREG28 Register

1 PWRAP_CFG_0_CORE_PRECREG28 Register (Offset = 70h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35410. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2370h**

Figure 14-11710. PWRAP_CFG_0_CORE_PRECREG28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35412. PWRAP_CFG_0_CORE_PRECREG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.133 PWRAP_CFG_0_CORE_PRECREG29 Register

1 PWRAP_CFG_0_CORE_PRECREG29 Register (Offset = 74h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35413. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2374h**

Figure 14-11711. PWRAP_CFG_0_CORE_PRECREG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35415. PWRAP_CFG_0_CORE_PRECREG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.134 PWRAP_CFG_0_CORE_PRECREG30 Register

1 PWRAP_CFG_0_CORE_PRECREG30 Register (Offset = 78h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35416. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2378h**

Figure 14-11712. PWRAP_CFG_0_CORE_PRECREG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35418. PWRAP_CFG_0_CORE_PRECREG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.135 PWRAP_CFG_0_CORE_PRECREG31 Register

1 PWRAP_CFG_0_CORE_PRECREG31 Register (Offset = 7Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-35419. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 237Ch

Figure 14-11713. PWRAP_CFG_0_CORE_PRECREG31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35421. PWRAP_CFG_0_CORE_PRECREG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.136 PWRAP_CFG_0_SYS_PRECREG Register

1 PWRAP_CFG_0_SYS_PRECREG Register (Offset = F0h) [reset = 0h]

This register is used to control system level functionality

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Table 14-35422. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 23F0h**

Figure 14-11714. PWRAP_CFG_0_SYS_PRECREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED			DBGCON_WE	DBGCON			
R			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
UNNAT_RESET	RST_OCCURED	SYSTEM_STAT	RSV12_BIT	GLOB_EXEC_TRIG	CLR_EX_FLAGS	GLOB_EXEC_MSK	IN_RESET_RLS_WIR
R	R/W	R	R	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
WIR_REQ	BLK_SYS_RST	RESERVED0		DEV_TYPE			SYS_RST_REQ
R/W	R/W	R		R			R/W
0h	0h	0h		0h			0h

Table 14-35424. PWRAP_CFG_0_SYS_PRECREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved, returns 0
20	DBGCON_WE	R/W	0h	This bit must be high to write to the debug connect field
19:16	DBGCON	R/W	0h	The system debugger must write a value of 0x9 to be connected and access the debug logic
15	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
14	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
13	SYSTEM_STAT	R	0h	System Status input, application specificall
12	RSV12_BIT	R	0h	Reserved, read returns 0
11	GLOB_EXEC_TRIG	R	0h	
10	CLR_EX_FLAGS	R/W	0h	Clear all run flags
9	GLOB_EXEC_MSK	R/W	0h	Global Execute Mask
8	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the global WIR When read this returns the in reset status
7	WIR_REQ	R/W	0h	Wait In Reset Request
6	BLK_SYS_RST	R/W	0h	Block System Reset
5:4	RESERVED0	R	0h	Reserved0, returns 0
3:1	DEV_TYPE	R	0h	Device Type tieoff value Test, emulator, secure, etc

Table 14-35424. PWRAP_CFG_0_SYS_PRECREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYS_RST_REQ	R/W	0h	System Reset Request This bit will be reset once reset occurs

14.10.2.2.137 PWRAP_CFG_0_ID_REGISTER Register

1 PWRAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 2E0002h]

Reading this register returns the ID information for this AP.

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Table 14-35425. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 23FCh**

Figure 14-11715. PWRAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				17h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
17h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				2h			

Table 14-35427. PWRAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	17h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	2h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.10.2.2.138 PVIEW_CFG_0_PVIEW_STATE0 Register

1 PVIEW_CFG_0_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-35428. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2400h**

Figure 14-11716. PVIEW_CFG_0_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	22	21	20	19	18	17	16
POWER_VIEW_STATE_REG0							
R							
0h							
15	14	13	12	11	10	9	8
POWER_VIEW_STATE_REG0							
R							
0h							
7	6	5	4	3	2	1	0
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-35430. PVIEW_CFG_0_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.10.2.2.139 PVIEW_CFG_0_PVIEW_CAPABILITY Register

1 PVIEW_CFG_0_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-35431. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 24F0h**

Figure 14-11717. PVIEW_CFG_0_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-35433. PVIEW_CFG_0_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.10.2.2.140 PVIEW_CFG_0_ID_REGISTER Register

1 PVIEW_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35434. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 24FCh**

Figure 14-11718. PVIEW_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35436. PVIEW_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.10.2.2.141 JTAGAP_CFG_0_CSW Register

1 JTAGAP_CFG_0_CSW Register (Offset = 0h) [reset = 0h]

This register provides control and status information

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Table 14-35437. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2500h

Figure 14-11719. JTAGAP_CFG_0_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-35439. JTAGAP_CFG_0_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.10.2.2.142 JTAGAP_CFG_0_PSEL_REG Register

1 JTAGAP_CFG_0_PSEL_REG Register (Offset = 4h) [reset = 0h]

This 8-bit register is used to select the JTAG port.

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Table 14-35440. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2504h**

Figure 14-11720. JTAGAP_CFG_0_PSEL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PORT_SELECT_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35442. JTAGAP_CFG_0_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.10.2.2.143 JTAGAP_CFG_0_PSTA_REG Register

1 JTAGAP_CFG_0_PSTA_REG Register (Offset = 8h) [reset = 0h]

A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

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Table 14-35443. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2508h**

Figure 14-11721. JTAGAP_CFG_0_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-35445. JTAGAP_CFG_0_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.10.2.2.144 JTAGAP_CFG_0_BYTEFIFO1 Register

1 JTAGAP_CFG_0_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-35446. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2510h**

Figure 14-11722. JTAGAP_CFG_0_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-35448. JTAGAP_CFG_0_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.10.2.2.145 JTAGAP_CFG_0_BYTEFIFO2 Register

1 JTAGAP_CFG_0_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

Return to Summary Table

Table 14-35449. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2514h**

Figure 14-11723. JTAGAP_CFG_0_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-35451. JTAGAP_CFG_0_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.10.2.2.146 JTAGAP_CFG_0_BYTEFIFO3 Register

1 JTAGAP_CFG_0_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

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Table 14-35452. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2518h**

Figure 14-11724. JTAGAP_CFG_0_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_3							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_3							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_3							
R/W							
0h							

Table 14-35454. JTAGAP_CFG_0_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.10.2.2.147 JTAGAP_CFG_0_BYTEFIFO4 Register

1 JTAGAP_CFG_0_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

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Table 14-35455. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 251Ch**

Figure 14-11725. JTAGAP_CFG_0_BYTEFIFO4 Name Register

31	30	29	28	27	26	25	24
BYTE_FIFO_4							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_4							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_4							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_4							
R/W							
0h							

Table 14-35457. JTAGAP_CFG_0_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.10.2.2.148 JTAGAP_CFG_0_ID_REGISTER Register

1 JTAGAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35458. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 25FCh**

Figure 14-11726. JTAGAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35460. JTAGAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.10.2.2.149 SECAP_CFG_0_TXDATA Register

1 SECAP_CFG_0_TXDATA Register (Offset = 0h) [reset = 0h]

Data value to send to security controller. Apllication specific

Return to Summary Table

Table 14-35461. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2600h**

Figure 14-11727. SECAP_CFG_0_TXDATA Name Register

31	30	29	28	27	26	25	24
TX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_DATA_REGISTER							
R/W							
0h							

Table 14-35463. SECAP_CFG_0_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	

14.10.2.2.150 SECAP_CFG_0_TXCTRL Register

1 SECAP_CFG_0_TXCTRL Register (Offset = 4h) [reset = 0h]

Register to send control information to the Security Controller, Application specific

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Table 14-35464. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2604h**

Figure 14-11728. SECAP_CFG_0_TXCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">TX_CONTROL</td><td>TXDAV</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-35466. SECAP_CFG_0_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.10.2.2.151 SECAP_CFG_0_RXDATA Register

1 SECAP_CFG_0_RXDATA Register (Offset = 8h) [reset = 0h]

Data value from the security controller. Apllication specific

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Table 14-35467. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2608h**

Figure 14-11729. SECAP_CFG_0_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-35469. SECAP_CFG_0_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	

14.10.2.2.152 SECAP_CFG_0_RXCTRL Register

1 SECAP_CFG_0_RXCTRL Register (Offset = Ch) [reset = 0h]

Register to receive control information from the Security Controller

Return to Summary Table

Table 14-35470. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 260Ch**

Figure 14-11730. SECAP_CFG_0_RXCTRL Name Register

31	30	29	28	27	26	25	24
RX_CONTROL							
R							
0h							
23	22	21	20	19	18	17	16
RX_CONTROL							
R							
0h							
15	14	13	12	11	10	9	8
RX_CONTROL							
R							
0h							
7	6	5	4	3	2	1	0
RX_CONTROL							RXDAV
R							R
0h							0h

Table 14-35472. SECAP_CFG_0_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.10.2.2.153 CORTEX0_CFG_0_CSWREG Register

1 CORTEX0_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-35473. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2700h**

Figure 14-11731. CORTEX0_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35475. CORTEX0_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.154 CORTEX0_CFG_0_TAREG Register

1 CORTEX0_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35476. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2704h**

Figure 14-11732. CORTEX0_CFG_0_TAREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35478. CORTEX0_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.155 CORTEX0_CFG_0_DRWREG Register

1 CORTEX0_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35479. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 270Ch**

Figure 14-11733. CORTEX0_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35481. CORTEX0_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.156 CORTEX0_CFG_0_BD0REG Register

1 CORTEX0_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35482. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2710h**

Figure 14-11734. CORTEX0_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35484. CORTEX0_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.157 CORTEX0_CFG_0_BD1REG Register

1 CORTEX0_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35485. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2714h**

Figure 14-11735. CORTEX0_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35487. CORTEX0_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.158 CORTEX0_CFG_0_BD2REG Register

1 CORTEX0_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35488. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2718h**

Figure 14-11736. CORTEX0_CFG_0_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35490. CORTEX0_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.159 CORTEX0_CFG_0_BD3REG Register

1 CORTEX0_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35491. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 271Ch**

Figure 14-11737. CORTEX0_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35493. CORTEX0_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.160 CORTEX0_CFG_0_ROM_REGISTER Register

1 CORTEX0_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35494. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 27F8h**

Figure 14-11738. CORTEX0_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35496. CORTEX0_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.161 CORTEX0_CFG_0_ID_REGISTER Register

1 CORTEX0_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-35497. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 27FCh**

Figure 14-11739. CORTEX0_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35499. CORTEX0_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.162 CORTEX1_CFG_0_CSWREG Register

1 CORTEX1_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-35500. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2800h**

Figure 14-11740. CORTEX1_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35502. CORTEX1_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.163 CORTEX1_CFG_0_TAREG Register

1 CORTEX1_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-35503. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2804h**

Figure 14-11741. CORTEX1_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35505. CORTEX1_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.164 CORTEX1_CFG_0_DRWREG Register

1 CORTEX1_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-35506. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 280Ch**

Figure 14-11742. CORTEX1_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35508. CORTEX1_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.165 CORTEX1_CFG_0_BD0REG Register

1 CORTEX1_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35509. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2810h**

Figure 14-11743. CORTEX1_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35511. CORTEX1_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.166 CORTEX1_CFG_0_BD1REG Register

1 CORTEX1_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35512. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2814h**

Figure 14-11744. CORTEX1_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35514. CORTEX1_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.167 CORTEX1_CFG_0_BD2REG Register

1 CORTEX1_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35515. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2818h**

Figure 14-11745. CORTEX1_CFG_0_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35517. CORTEX1_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.168 CORTEX1_CFG_0_BD3REG Register

1 CORTEX1_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35518. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 281Ch**

Figure 14-11746. CORTEX1_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35520. CORTEX1_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.169 CORTEX1_CFG_0_ROM_REGISTER Register

1 CORTEX1_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35521. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 28F8h**

Figure 14-11747. CORTEX1_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35523. CORTEX1_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.170 CORTEX1_CFG_0_ID_REGISTER Register

1 CORTEX1_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35524. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 28FCh**

Figure 14-11748. CORTEX1_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35526. CORTEX1_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.171 CORTEX2_CFG_0_CSWREG Register

1 CORTEX2_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-35527. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2900h**

Figure 14-11749. CORTEX2_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35529. CORTEX2_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.172 CORTEX2_CFG_0_TAREG Register

1 CORTEX2_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35530. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2904h**

Figure 14-11750. CORTEX2_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35532. CORTEX2_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.173 CORTEX2_CFG_0_DRWREG Register

1 CORTEX2_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-35533. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 290Ch**

Figure 14-11751. CORTEX2_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35535. CORTEX2_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.174 CORTEX2_CFG_0_BD0REG Register

1 CORTEX2_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35536. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2910h**

Figure 14-11752. CORTEX2_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35538. CORTEX2_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.175 CORTEX2_CFG_0_BD1REG Register

1 CORTEX2_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35539. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2914h**

Figure 14-11753. CORTEX2_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35541. CORTEX2_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.176 CORTEX2_CFG_0_BD2REG Register

1 CORTEX2_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35542. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2918h**

Figure 14-11754. CORTEX2_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35544. CORTEX2_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.177 CORTEX2_CFG_0_BD3REG Register

1 CORTEX2_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35545. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 291Ch**

Figure 14-11755. CORTEX2_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35547. CORTEX2_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.178 CORTEX2_CFG_0_ROM_REGISTER Register

1 CORTEX2_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-35548. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 29F8h**

Figure 14-11756. CORTEX2_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35550. CORTEX2_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.179 CORTEX2_CFG_0_ID_REGISTER Register

1 CORTEX2_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35551. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 29FCh**

Figure 14-11757. CORTEX2_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35553. CORTEX2_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.180 CORTEX3_CFG_0_CSWREG Register

1 CORTEX3_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-35554. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A00h**

Figure 14-11758. CORTEX3_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35556. CORTEX3_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.181 CORTEX3_CFG_0_TAREG Register

1 CORTEX3_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35557. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A04h**

Figure 14-11759. CORTEX3_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35559. CORTEX3_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.182 CORTEX3_CFG_0_DRWREG Register

1 CORTEX3_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35560. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A0Ch**

Figure 14-11760. CORTEX3_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35562. CORTEX3_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.183 CORTEX3_CFG_0_BD0REG Register

1 CORTEX3_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35563. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A10h**

Figure 14-11761. CORTEX3_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35565. CORTEX3_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.184 CORTEX3_CFG_0_BD1REG Register

1 CORTEX3_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35566. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A14h**

Figure 14-11762. CORTEX3_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35568. CORTEX3_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.185 CORTEX3_CFG_0_BD2REG Register

1 CORTEX3_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35569. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A18h**

Figure 14-11763. CORTEX3_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35571. CORTEX3_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.186 CORTEX3_CFG_0_BD3REG Register

1 CORTEX3_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35572. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2A1Ch**

Figure 14-11764. CORTEX3_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35574. CORTEX3_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.187 CORTEX3_CFG_0_ROM_REGISTER Register

1 CORTEX3_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-35575. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2AF8h**

Figure 14-11765. CORTEX3_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35577. CORTEX3_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.188 CORTEX3_CFG_0_ID_REGISTER Register

1 CORTEX3_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35578. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2AFCh**

Figure 14-11766. CORTEX3_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			

23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h

15	14	13	12	11	10	9	8
SPARE							
R							
0h							

7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35580. CORTEX3_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.189 CORTEX4_CFG_0_CSWREG Register

1 CORTEX4_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-35581. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B00h**

Figure 14-11767. CORTEX4_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35583. CORTEX4_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.190 CORTEX4_CFG_0_TAREG Register

1 CORTEX4_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35584. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B04h**

Figure 14-11768. CORTEX4_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35586. CORTEX4_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.191 CORTEX4_CFG_0_DRWREG Register

1 CORTEX4_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35587. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B0Ch**

Figure 14-11769. CORTEX4_CFG_0_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35589. CORTEX4_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.192 CORTEX4_CFG_0_BD0REG Register

1 CORTEX4_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35590. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B10h**

Figure 14-11770. CORTEX4_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35592. CORTEX4_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.193 CORTEX4_CFG_0_BD1REG Register

1 CORTEX4_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35593. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B14h**

Figure 14-11771. CORTEX4_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35595. CORTEX4_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.194 CORTEX4_CFG_0_BD2REG Register

1 CORTEX4_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35596. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B18h**

Figure 14-11772. CORTEX4_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35598. CORTEX4_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.195 CORTEX4_CFG_0_BD3REG Register

1 CORTEX4_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-35599. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2B1Ch**

Figure 14-11773. CORTEX4_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35601. CORTEX4_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.196 CORTEX4_CFG_0_ROM_REGISTER Register

1 CORTEX4_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-35602. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2BF8h**

Figure 14-11774. CORTEX4_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35604. CORTEX4_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.197 CORTEX4_CFG_0_ID_REGISTER Register

1 CORTEX4_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-35605. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2BFCh**

Figure 14-11775. CORTEX4_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35607. CORTEX4_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.198 CORTEX5_CFG_0_CSWREG Register

1 CORTEX5_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-35608. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C00h**

Figure 14-11776. CORTEX5_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35610. CORTEX5_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.199 CORTEX5_CFG_0_TAREG Register

1 CORTEX5_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-35611. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C04h**

Figure 14-11777. CORTEX5_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35613. CORTEX5_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.200 CORTEX5_CFG_0_DRWREG Register

1 CORTEX5_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-35614. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C0Ch**

Figure 14-11778. CORTEX5_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35616. CORTEX5_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.201 CORTEX5_CFG_0_BD0REG Register

1 CORTEX5_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35617. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C10h**

Figure 14-11779. CORTEX5_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35619. CORTEX5_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.202 CORTEX5_CFG_0_BD1REG Register

1 CORTEX5_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35620. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C14h**

Figure 14-11780. CORTEX5_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35622. CORTEX5_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.203 CORTEX5_CFG_0_BD2REG Register

1 CORTEX5_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35623. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C18h**

Figure 14-11781. CORTEX5_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35625. CORTEX5_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.204 CORTEX5_CFG_0_BD3REG Register

1 CORTEX5_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35626. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2C1Ch**

Figure 14-11782. CORTEX5_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35628. CORTEX5_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.205 CORTEX5_CFG_0_ROM_REGISTER Register

1 CORTEX5_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35629. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2CF8h

Figure 14-11783. CORTEX5_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35631. CORTEX5_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.206 CORTEX5_CFG_0_ID_REGISTER Register

1 CORTEX5_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-35632. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2CFCh**

Figure 14-11784. CORTEX5_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35634. CORTEX5_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.207 CORTEX6_CFG_0_CSWREG Register

1 CORTEX6_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-35635. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D00h**

Figure 14-11785. CORTEX6_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35637. CORTEX6_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.208 CORTEX6_CFG_0_TAREG Register

1 CORTEX6_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35638. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D04h**

Figure 14-11786. CORTEX6_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35640. CORTEX6_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.209 CORTEX6_CFG_0_DRWREG Register

1 CORTEX6_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-35641. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D0Ch**

Figure 14-11787. CORTEX6_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35643. CORTEX6_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.210 CORTEX6_CFG_0_BD0REG Register

1 CORTEX6_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35644. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D10h**

Figure 14-11788. CORTEX6_CFG_0_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35646. CORTEX6_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.211 CORTEX6_CFG_0_BD1REG Register

1 CORTEX6_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35647. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D14h**

Figure 14-11789. CORTEX6_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35649. CORTEX6_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.212 CORTEX6_CFG_0_BD2REG Register

1 CORTEX6_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35650. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D18h**

Figure 14-11790. CORTEX6_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35652. CORTEX6_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.213 CORTEX6_CFG_0_BD3REG Register

1 CORTEX6_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35653. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2D1Ch**

Figure 14-11791. CORTEX6_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35655. CORTEX6_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.214 CORTEX6_CFG_0_ROM_REGISTER Register

1 CORTEX6_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35656. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2DF8h**

Figure 14-11792. CORTEX6_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35658. CORTEX6_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.215 CORTEX6_CFG_0_ID_REGISTER Register

1 CORTEX6_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-35659. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2DFCh**

Figure 14-11793. CORTEX6_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35661. CORTEX6_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.216 CORTEX7_CFG_0_CSWREG Register

1 CORTEX7_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-35662. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E00h**

Figure 14-11794. CORTEX7_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35664. CORTEX7_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.217 CORTEX7_CFG_0_TAREG Register

1 CORTEX7_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-35665. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E04h**

Figure 14-11795. CORTEX7_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35667. CORTEX7_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.218 CORTEX7_CFG_0_DRWREG Register

1 CORTEX7_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-35668. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E0Ch**

Figure 14-11796. CORTEX7_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-35670. CORTEX7_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.219 CORTEX7_CFG_0_BD0REG Register

1 CORTEX7_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35671. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E10h**

Figure 14-11797. CORTEX7_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35673. CORTEX7_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.220 CORTEX7_CFG_0_BD1REG Register

1 CORTEX7_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35674. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E14h**

Figure 14-11798. CORTEX7_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35676. CORTEX7_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.221 CORTEX7_CFG_0_BD2REG Register

1 CORTEX7_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35677. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E18h**

Figure 14-11799. CORTEX7_CFG_0_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35679. CORTEX7_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.222 CORTEX7_CFG_0_BD3REG Register

1 CORTEX7_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35680. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2E1Ch**

Figure 14-11800. CORTEX7_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35682. CORTEX7_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.223 CORTEX7_CFG_0_ROM_REGISTER Register

1 CORTEX7_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35683. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2EF8h**

Figure 14-11801. CORTEX7_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35685. CORTEX7_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.224 CORTEX7_CFG_0_ID_REGISTER Register

1 CORTEX7_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-35686. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2EFCh**

Figure 14-11802. CORTEX7_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35688. CORTEX7_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.225 CORTEX8_CFG_0_CSWREG Register

1 CORTEX8_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-35689. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F00h**

Figure 14-11803. CORTEX8_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-35691. CORTEX8_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.226 CORTEX8_CFG_0_TAREG Register

1 CORTEX8_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-35692. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F04h**

Figure 14-11804. CORTEX8_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-35694. CORTEX8_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.227 CORTEX8_CFG_0_DRWREG Register

1 CORTEX8_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-35695. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F0Ch**

Figure 14-11805. CORTEX8_CFG_0_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35697. CORTEX8_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.228 CORTEX8_CFG_0_BD0REG Register

1 CORTEX8_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35698. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F10h**

Figure 14-11806. CORTEX8_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-35700. CORTEX8_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.229 CORTEX8_CFG_0_BD1REG Register

1 CORTEX8_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35701. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F14h**

Figure 14-11807. CORTEX8_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-35703. CORTEX8_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.230 CORTEX8_CFG_0_BD2REG Register

1 CORTEX8_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35704. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F18h**

Figure 14-11808. CORTEX8_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-35706. CORTEX8_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.231 CORTEX8_CFG_0_BD3REG Register

1 CORTEX8_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-35707. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2F1Ch**

Figure 14-11809. CORTEX8_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-35709. CORTEX8_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.232 CORTEX8_CFG_0_ROM_REGISTER Register

1 CORTEX8_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-35710. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2FF8h**

Figure 14-11810. CORTEX8_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-35712. CORTEX8_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.233 CORTEX8_CFG_0_ID_REGISTER Register

1 CORTEX8_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-35713. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 0000 2FFCh**

Figure 14-11811. CORTEX8_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-35715. CORTEX8_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.234 ROM_TABLE_1_0_ROM_ENTRY0 Register

1 ROM_TABLE_1_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

rom table entry 0

Return to Summary Table

Table 14-35716. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0000h**

Figure 14-11812. ROM_TABLE_1_0_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35718. ROM_TABLE_1_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.235 ROM_TABLE_1_0_ROM_ENTRY1 Register

1 ROM_TABLE_1_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

rom table entry 1

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Table 14-35719. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0004h**

Figure 14-11813. ROM_TABLE_1_0_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-35721. ROM_TABLE_1_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.236 ROM_TABLE_1_0_ROM_ENTRY2 Register

1 ROM_TABLE_1_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

rom table entry 2

Return to Summary Table

Table 14-35722. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0008h**

Figure 14-11814. ROM_TABLE_1_0_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	3h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
3h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
3h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35724. ROM_TABLE_1_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.237 ROM_TABLE_1_0_ROM_ENTRY3 Register

1 ROM_TABLE_1_0_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

rom table entry 3

Return to Summary Table

Table 14-35725. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 000Ch**

Figure 14-11815. ROM_TABLE_1_0_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35727. ROM_TABLE_1_0_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.238 ROM_TABLE_1_0_ROM_ENTRY4 Register

1 ROM_TABLE_1_0_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

rom table entry 4

Return to Summary Table

Table 14-35728. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0010h**

Figure 14-11816. ROM_TABLE_1_0_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
5h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35730. ROM_TABLE_1_0_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.239 ROM_TABLE_1_0_ROM_ENTRY5 Register

1 ROM_TABLE_1_0_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

rom table entry 5

Return to Summary Table

Table 14-35731. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0014h**

Figure 14-11817. ROM_TABLE_1_0_ROM_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1000h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-35733. ROM_TABLE_1_0_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.240 ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register

1 ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

compute cluster rom table entry 0

Return to Summary Table

Table 14-35734. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0018h**

Figure 14-11818. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35736. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.241 ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register

1 ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

compute cluster rom table entry 1

Return to Summary Table

Table 14-35737. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 001Ch**

Figure 14-11819. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1400h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35739. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.242 ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register

1 ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

compute cluster rom table entry 2

Return to Summary Table

Table 14-35740. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0020h**

Figure 14-11820. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1800h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1800h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1800h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35742. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.243 ROM_TABLE_1_0_DEBUG_CELL0 Register

1 ROM_TABLE_1_0_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

debug cell rom table entry 0

Return to Summary Table

Table 14-35743. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0024h**

Figure 14-11821. ROM_TABLE_1_0_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35745. ROM_TABLE_1_0_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.244 ROM_TABLE_1_0_DEBUG_CELL1 Register

1 ROM_TABLE_1_0_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

debug cell rom table entry 1

Return to Summary Table

Table 14-35746. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0028h**

Figure 14-11822. ROM_TABLE_1_0_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C10h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35748. ROM_TABLE_1_0_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.245 ROM_TABLE_1_0_DEBUG_CELL2 Register

1 ROM_TABLE_1_0_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

debug cell rom table entry 2

Return to Summary Table

Table 14-35749. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 002Ch**

Figure 14-11823. ROM_TABLE_1_0_DEBUG_CELL2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35751. ROM_TABLE_1_0_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.246 ROM_TABLE_1_0_DEBUG_CELL3 Register

1 ROM_TABLE_1_0_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

debug cell rom table entry 3

Return to Summary Table

Table 14-35752. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0030h

Figure 14-11824. ROM_TABLE_1_0_DEBUG_CELL3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C30h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C30h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35754. ROM_TABLE_1_0_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.247 ROM_TABLE_1_0_DEBUG_CELL4 Register

1 ROM_TABLE_1_0_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

debug cell rom table entry 4

Return to Summary Table

Table 14-35755. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0034h**

Figure 14-11825. ROM_TABLE_1_0_DEBUG_CELL4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C40h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C40h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C40h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35757. ROM_TABLE_1_0_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.248 ROM_TABLE_1_0_DEBUG_CELL5 Register

1 ROM_TABLE_1_0_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

debug cell rom table entry 5

Return to Summary Table

Table 14-35758. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0038h**

Figure 14-11826. ROM_TABLE_1_0_DEBUG_CELL5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C50h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C50h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C50h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35760. ROM_TABLE_1_0_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.249 ROM_TABLE_1_0_DEBUG_CELL6 Register

1 ROM_TABLE_1_0_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

debug cell rom table entry 6

Return to Summary Table

Table 14-35761. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 003Ch**

Figure 14-11827. ROM_TABLE_1_0_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35763. ROM_TABLE_1_0_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.250 ROM_TABLE_1_0_DEBUG_CELL7 Register

1 ROM_TABLE_1_0_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

debug cell rom table entry 7

Return to Summary Table

Table 14-35764. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0040h**

Figure 14-11828. ROM_TABLE_1_0_DEBUG_CELL7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C70h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C70h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C70h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35766. ROM_TABLE_1_0_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.251 ROM_TABLE_1_0_DEBUG_CELL8 Register

1 ROM_TABLE_1_0_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

debug cell rom table entry 8

Return to Summary Table

Table 14-35767. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0044h**

Figure 14-11829. ROM_TABLE_1_0_DEBUG_CELL8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C80h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C80h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C80h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35769. ROM_TABLE_1_0_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.252 ROM_TABLE_1_0_DEBUG_CELL9 Register

1 ROM_TABLE_1_0_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

debug cell rom table entry 9

Return to Summary Table

Table 14-35770. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0048h**

Figure 14-11830. ROM_TABLE_1_0_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35772. ROM_TABLE_1_0_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.253 ROM_TABLE_1_0_DEBUG_CELL10 Register

1 ROM_TABLE_1_0_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

debug cell rom table entry 10

Return to Summary Table

Table 14-35773. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 004Ch**

Figure 14-11831. ROM_TABLE_1_0_DEBUG_CELL10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35775. ROM_TABLE_1_0_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.254 ROM_TABLE_1_0_DEBUG_CELL11 Register

1 ROM_TABLE_1_0_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

debug cell rom table entry 11

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Table 14-35776. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0050h**

Figure 14-11832. ROM_TABLE_1_0_DEBUG_CELL11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1CB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1CB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35778. ROM_TABLE_1_0_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.255 ROM_TABLE_1_0_EXTCSCOMP0 Register

1 ROM_TABLE_1_0_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

external coresight componenet rom table entry 0

Return to Summary Table

Table 14-35779. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0050h

Figure 14-11833. ROM_TABLE_1_0_EXTCSCOMP0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D00h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D00h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35781. ROM_TABLE_1_0_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.256 ROM_TABLE_1_0_EXTCSCOMP1 Register

1 ROM_TABLE_1_0_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

external coresight componenet rom table entry 1

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Table 14-35782. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0054h**

Figure 14-11834. ROM_TABLE_1_0_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D10h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35784. ROM_TABLE_1_0_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.257 ROM_TABLE_1_0_EXTCSCOMP2 Register

1 ROM_TABLE_1_0_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

external coresight componenet rom table entry 2

Return to Summary Table

Table 14-35785. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0058h**

Figure 14-11835. ROM_TABLE_1_0_EXTCSCOMP2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D20h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D20h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35787. ROM_TABLE_1_0_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.258 ROM_TABLE_1_0_EXTCSCOMP3 Register

1 ROM_TABLE_1_0_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

external coresight componenet rom table entry 3

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Table 14-35788. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 005Ch**

Figure 14-11836. ROM_TABLE_1_0_EXTCSCOMP3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D30h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D30h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D30h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35790. ROM_TABLE_1_0_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.259 ROM_TABLE_1_0_EXTCSCOMP4 Register

1 ROM_TABLE_1_0_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

external coresight componenet rom table entry 4

Return to Summary Table

Table 14-35791. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0060h**

Figure 14-11837. ROM_TABLE_1_0_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35793. ROM_TABLE_1_0_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.260 ROM_TABLE_1_0_EXTCSCOMP5 Register

1 ROM_TABLE_1_0_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

external coresight componenet rom table entry 5

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Table 14-35794. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0064h**

Figure 14-11838. ROM_TABLE_1_0_EXTCSCOMP5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D50h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D50h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D50h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35796. ROM_TABLE_1_0_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.261 ROM_TABLE_1_0_EXTCSCOMP6 Register

1 ROM_TABLE_1_0_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

external coresight componenet rom table entry 6

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Table 14-35797. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0068h**

Figure 14-11839. ROM_TABLE_1_0_EXTCSCOMP6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D60h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D60h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D60h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35799. ROM_TABLE_1_0_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.262 ROM_TABLE_1_0_EXTCSCOMP7 Register

1 ROM_TABLE_1_0_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

external coresight componenet rom table entry 7

Return to Summary Table

Table 14-35800. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 006Ch**

Figure 14-11840. ROM_TABLE_1_0_EXTCSCOMP7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D70h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D70h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D70h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35802. ROM_TABLE_1_0_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.263 ROM_TABLE_1_0_EXTCSCOMP8 Register

1 ROM_TABLE_1_0_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

external coresight componenet rom table entry 8

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Table 14-35803. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0070h**

Figure 14-11841. ROM_TABLE_1_0_EXTCSCOMP8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D80h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D80h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D80h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35805. ROM_TABLE_1_0_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.264 ROM_TABLE_1_0_EXTCSCOMP9 Register

1 ROM_TABLE_1_0_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

external coresight componenet rom table entry 9

Return to Summary Table

Table 14-35806. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0074h**

Figure 14-11842. ROM_TABLE_1_0_EXTCSCOMP9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D90h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D90h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D90h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-35808. ROM_TABLE_1_0_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.265 ROM_TABLE_1_0_EXTCSCOMP10 Register

1 ROM_TABLE_1_0_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

external coresight componenet rom table entry 10

Return to Summary Table

Table 14-35809. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 0078h**

Figure 14-11843. ROM_TABLE_1_0_EXTCSCOMP10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1DA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1DA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1DA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35811. ROM_TABLE_1_0_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.266 ROM_TABLE_1_0_EXTCSCOMP11 Register

1 ROM_TABLE_1_0_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

external coresight componenet rom table entry 11

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Table 14-35812. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 007Ch**

Figure 14-11844. ROM_TABLE_1_0_EXTCSCOMP11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1DB0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1DB0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1DB0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-35814. ROM_TABLE_1_0_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.267 CSCTI_CTICONTROL Register

1 CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register.

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Table 14-35815. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1000h**

Figure 14-11845. CSCTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
R							R/W
0h							0h

Table 14-35817. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	GLBEN	R/W	0h	Enables or disables the Embedded Cross Trigger, 1=enabled

14.10.2.2.268 CSCTI_CTIINTACK Register

1 CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Interrupt Acknowledge Register.

Return to Summary Table

Table 14-35818. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1010h**

Figure 14-11846. CSCTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-35820. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INTACK	R/W	0h	Acknowledges the corresponding CTITRIGOUT output Write 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW There is one bit of the register for each CTITRIGOUT output

14.10.2.2.269 CSCTI_CTIAPPSET Register

1 CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register.

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Table 14-35821. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1014h**

Figure 14-11847. CSCTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
R				R/W			
0h				0h			

Table 14-35823. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPSET	R/W	0h	The CTI Application Trigger Set Register is read/write A write to this register causes a channel event to be raised, corresponding to the bit written to

14.10.2.2.270 CSCTI_CTIAPPCLR Register

1 CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register.

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Table 14-35824. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1018h**

Figure 14-11848. CSCTI_CTIAPPCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPCLR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35826. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPCLR	R/W	0h	The CTI Application Trigger Clear Register is write-only A write to this register causes a channel event to be cleared, corresponding to the bit written to

14.10.2.2.271 CSCTI_CTIAPPPULSE Register

1 CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Trigger Pulse Register.

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Table 14-35827. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 101Ch

Figure 14-11849. CSCTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPPULSE			
R				R/W			
0h				0h			

Table 14-35829. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPPULSE	R/W	0h	The CTI Application Pulse Register is write-only A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to This register clears itself immediately

14.10.2.2.272 CSCTI_CTIINEN0 Register

1 CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 0

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Table 14-35830. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1020h**

Figure 14-11850. CSCTI_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35832. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.273 CSCTI_CTIINEN1 Register

1 CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 1

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Table 14-35833. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1024h**

Figure 14-11851. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	TRIGINEN		
R				NONE	R/W		
0h				0h	0h		

Table 14-35835. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.274 CSCTI_CTIINEN2 Register

1 CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 2

Return to Summary Table

Table 14-35836. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1028h**

Figure 14-11852. CSCTI_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35838. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.275 CSCTI_CTIINEN3 Register

1 CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 3

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Table 14-35839. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 102Ch**

Figure 14-11853. CSCTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-35841. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.276 CSCTI_CTIINEN4 Register

1 CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 4

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Table 14-35842. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1030h**

Figure 14-11854. CSCTI_CTIINEN4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35844. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.277 CSCTI_CTIINEN5 Register

1 CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 5

Return to Summary Table

Table 14-35845. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1034h**

Figure 14-11855. CSCTI_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35847. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.278 CSCTI_CTIINEN6 Register

1 CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 6

Return to Summary Table

Table 14-35848. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1038h**

Figure 14-11856. CSCTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-35850. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.279 CSCTI_CTIINEN7 Register

1 CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 7

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Table 14-35851. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 103Ch**

Figure 14-11857. CSCTI_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35853. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.280 CSCTI_CTIOUTEN0 Register

1 CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Channel to Trigger Enable Register 0

Return to Summary Table

Table 14-35854. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A0h**

Figure 14-11858. CSCTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35856. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.281 CSCTI_CTIOUTEN1 Register

1 CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Channel to Trigger Enable Register 1

Return to Summary Table

Table 14-35857. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A4h**

Figure 14-11859. CSCTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35859. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.282 CSCTI_CTIOUTEN2 Register

1 CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Channel to Trigger Enable Register 2

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Table 14-35860. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A8h**

Figure 14-11860. CSCTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35862. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.283 CSCTI_CTIOUTEN3 Register

1 CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Channel to Trigger Enable Register 3

Return to Summary Table

Table 14-35863. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10ACh

Figure 14-11861. CSCTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35865. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.284 CSCTI_CTIOUTEN4 Register

1 CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Channel to Trigger Enable Register 4

Return to Summary Table

Table 14-35866. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10B0h**

Figure 14-11862. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35868. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.285 CSCTI_CTIOUTEN5 Register

1 CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Channel to Trigger Enable Register 5

Return to Summary Table

Table 14-35869. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10B4h**

Figure 14-11863. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35871. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.286 CSCTI_CTIOUTEN6 Register

1 CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Channel to Trigger Enable Register 6

Return to Summary Table

Table 14-35872. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10B8h**

Figure 14-11864. CSCTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-35874. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.287 CSCTI_CTIOUTEN7 Register

1 CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Channel to Trigger Enable Register 7

Return to Summary Table

Table 14-35875. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10BCh**

Figure 14-11865. CSCTI_CTIOUTEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35877. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.288 CSCTI_CTITRIGINSTATUS Register

1 CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

Return to Summary Table

Table 14-35878. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1130h**

Figure 14-11866. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-35880. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGINSTATUS	R	0h	Shows the status of the CTITRIGIN inputs: 1=CTITRIGIN is active, 0=CTITRIGIN is inactive

14.10.2.2.289 CSCTI_CTITRIGOUTSTATUS Register

1 CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

Return to Summary Table

Table 14-35881. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1134h**

Figure 14-11867. CSCTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-35883. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the CTITRIGOUT outputs: 1=CTITRIGOUT is active, 0=CTITRIGOUT is inactive

14.10.2.2.290 CSCTI_CTICHINSTATUS Register

1 CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

Return to Summary Table

Table 14-35884. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1138h**

Figure 14-11868. CSCTI_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CHINSTATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35886. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHINSTATUS	R	0h	Shows the status of the CTICHIN inputs: 1=CTICHIN is active, 0=CTICHIN is inactive

14.10.2.2.291 CSCTI_CTICHOUTSTATUS Register

1 CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-35887. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 113Ch**

Figure 14-11869. CSCTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CHOUTSTATUS			
R				R			
0h				0h			

Table 14-35889. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHOUTSTATUS	R	0h	Shows the status of the CTICHOUT outputs: 1=CTICHOUT is active, 0=CTICHOUT is inactive

14.10.2.2.292 CSCTI_CTIGATE Register

1 CSCTI_CTIGATE Register (Offset = 140h) [reset = 0h]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs.

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Table 14-35890. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1140h**

Figure 14-11870. CSCTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN			
R				R			
0h				0h			

Table 14-35892. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTIGATEEN	R	0h	Gate enable for the four channels [1 per bit]

14.10.2.2.293 CSCTI_ASICCTL Register

1 CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Allows external multiplexing of the trigger signals

Return to Summary Table

Table 14-35893. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1144h**

Figure 14-11871. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASICCTL							
R/W							
0h							

Table 14-35895. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]

14.10.2.2.294 CSCTI_ITCHINACK Register

1 CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

Integration and Test register

Return to Summary Table

Table 14-35896. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EDCh

Figure 14-11872. CSCTI_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
R				R/W			
0h				0h			

Table 14-35898. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHINACK	R/W	0h	Sets the value of the CTCHINACK outputs

14.10.2.2.295 CSCTI_ITTRIGINACK Register

1 CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

ITTRIGINACK Register

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Table 14-35899. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE0h**

Figure 14-11873. CSCTI_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-35901. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGINACK	R/W	0h	Sets the value of the CTTRIGINACK outputs

14.10.2.2.296 CSCTI_ITCHOUT Register

1 CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

ITCHOUT Register

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Table 14-35902. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE4h**

Figure 14-11874. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
R				R/W			
0h				0h			

Table 14-35904. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHOUT	R/W	0h	Sets the value of the CTCHOUT outputs

14.10.2.2.297 CSCTI_ITTRIGOUT Register

1 CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

ITTRIGOUT Register

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Table 14-35905. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE8h**

Figure 14-11875. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTTRIGOUT							
R/W							
0h							

Table 14-35907. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUT	R/W	0h	Sets the value of the CTTRIGOUT outputs

14.10.2.2.298 CSCTI_ITCHOUTACK Register

1 CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

ITCHOUTACK Register

Return to Summary Table

Table 14-35908. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EECh**

Figure 14-11876. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTCHOUTACK							
R/W							
0h							

Table 14-35910. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTCHOUTACK	R/W	0h	Sets the value of the CTCHOUTACK outputs

14.10.2.2.299 CSCTI_ITTRIGOUTACK Register

1 CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

ITTRIGOUTACK Register

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Table 14-35911. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF0h**

Figure 14-11877. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-35913. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUTACK	R	0h	Reads the value of the CTTRIGOUTACK inputs

14.10.2.2.300 CSCTI_ITCHIN Register

1 CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

ITCHIN Register

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Table 14-35914. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF4h**

Figure 14-11878. CSCTI_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
R				R			
0h				0h			

Table 14-35916. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHIN	R	0h	Reads the value of the CTCHIN inputs

14.10.2.2.301 CSCTI_ITTRIGIN Register

1 CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

ITTRIGIN Register

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Table 14-35917. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF8h**

Figure 14-11879. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-35919. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGIN	R	0h	Reads the value of the CTTRIGIN inputs

14.10.2.2.302 CSCTI_ITCTRL Register

1 CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

ITCTRL Register

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Table 14-35920. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1F00h**

Figure 14-11880. CSCTI_ITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ITEN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-35922. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	ITEN	R/W	0h	Integration Test control enable

14.10.2.2.303 CSCTI_CLAIMSET Register

1 CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-35923. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FA0h**

Figure 14-11881. CSCTI_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-35925. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.304 CSCTI_CLAIMCLR Register

1 CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-35926. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FA4h**

Figure 14-11882. CSCTI_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-35928. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.305 CSCTI_LOCKACCESS Register

1 CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-35929. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FB0h**

Figure 14-11883. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
LOCKACCESSREG							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCKACCESSREG							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCKACCESSREG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCKACCESSREG							
R/W							
0h							

Table 14-35931. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKACCESSREG	R/W	0h	Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers If paddrdbg31 is high, this is ignored

14.10.2.2.306 CSCTI_LOCKSTATUS Register

1 CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-35932. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB4h

Figure 14-11884. CSCTI_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-35934. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.307 CSCTI_AUTHSTATUS Register

1 CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-35935. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FB8h**

Figure 14-11885. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-35937. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.308 CSCTI_DEVID Register

1 CSCTI_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-35938. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FC8h**

Figure 14-11886. CSCTI_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUM_ECT_CHANNELS			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
NUM_ECT_TRIGGERS							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED7_5			IMPLEMENTATION_DEFINED				
R			R				
0h			0h				

Table 14-35940. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved, returns 0
19:16	NUM_ECT_CHANNELS	R	0h	Number of ECT Channels available
15:8	NUM_ECT_TRIGGERS	R	0h	Number of ECT trigger available
7:5	RESERVED7_5	R	0h	Reserved, returns 0
4:0	IMPLEMENTATION_DEFINED	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Outputs using ASICCTL Defailt value of 0 indicates no multiplexing present

14.10.2.2.309 CSCTI_DEVTYPE Register

1 CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-35941. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FCCh**

Figure 14-11887. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-35943. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.10.2.2.310 CSCTI_PERIPHID4 Register

1 CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-35944. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FD0h**

Figure 14-11888. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-35946. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.311 CSCTI_PERIPHID0 Register

1 CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-35947. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FE0h**

Figure 14-11889. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-35949. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.312 CSCTI_PERIPHID1 Register

1 CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-35950. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FE4h**

Figure 14-11890. CSCTI_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-35952. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.313 CSCTI_PERIPHID2 Register

1 CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-35953. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE8h

Figure 14-11891. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-35955. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.314 CSCTI_PERIPHID3 Register

1 CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-35956. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FECh**

Figure 14-11892. CSCTI_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-35958. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.315 CSCTI_COMPONID0 Register

1 CSCTI_COMPONID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-35959. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF0h

Figure 14-11893. CSCTI_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-35961. CSCTI_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.316 CSCTI_COMPONID1 Register

1 CSCTI_COMPONID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-35962. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FF4h**

Figure 14-11894. CSCTI_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-35964. CSCTI_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.317 CSCTI_COMPONID2 Register

1 CSCTI_COMPONID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-35965. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FF8h**

Figure 14-11895. CSCTI_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-35967. CSCTI_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.318 CSCTI_COMPONID3 Register

1 CSCTI_COMPONID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

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Table 14-35968. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FFCh**

Figure 14-11896. CSCTI_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-35970. CSCTI_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.319 DRM_CFG_0_PERIPH_ID Register

1 DRM_CFG_0_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

This register is used to determine what the functionality of this peripheral is.

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Table 14-35971. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2000h**

Figure 14-11897. DRM_CFG_0_PERIPH_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		283h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
283h							
15	14	13	12	11	10	9	8
RTLREV					MAJOR		
R					R		
Ch					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-35973. DRM_CFG_0_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.10.2.2.320 DRM_CFG_0_VERSION Register

1 DRM_CFG_0_VERSION Register (Offset = 4h) [reset = 0h]

This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-35974. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2004h**

Figure 14-11898. DRM_CFG_0_VERSION Name Register

31	30	29	28	27	26	25	24
MAJOR_VERSION							
R							
0h							
23	22	21	20	19	18	17	16
MAJOR_VERSION							
R							
0h							
15	14	13	12	11	10	9	8
MINOR_VERSION							
R							
0h							
7	6	5	4	3	2	1	0
MINOR_VERSION							
R							
0h							

Table 14-35976. DRM_CFG_0_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.10.2.2.321 DRM_CFG_0_CAPABILITY Register

1 DRM_CFG_0_CAPABILITY Register (Offset = 8h) [reset = 0h]

This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-35977. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2008h**

Figure 14-11899. DRM_CFG_0_CAPABILITY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">NUM_SUSPENDS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_PERIPHERALS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-35979. DRM_CFG_0_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.10.2.2.322 DRM_CFG_0_TRACE_CTRL Register

1 DRM_CFG_0_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-35980. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 200Ch**

Figure 14-11900. DRM_CFG_0_TRACE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CENTER_SAMPLING</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-35982. DRM_CFG_0_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.10.2.2.323 DRM_CFG_0_VBUSM_CTRL Register

1 DRM_CFG_0_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-35983. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2010h**

Figure 14-11901. DRM_CFG_0_VBUSM_CTRL Name Register

31	30	29	28	27	26	25	24
DOM_INPUT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DOM_INPUT			RESERVED				
R			R				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBUSM_PRIV		VBUSM_SECURE	VBUSM_DEBUG	CTL_PRIV		CTL_SECURE	EMUDBG
R		R	R	R/W		R/W	R/W
0h		0h	0h	0h		0h	0h

Table 14-35985. DRM_CFG_0_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.10.2.2.324 DRM_CFG_0_DAP_TIMEOUT Register

1 DRM_CFG_0_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-35986. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2014h**

Figure 14-11902. DRM_CFG_0_DAP_TIMEOUT Name Register

31	30	29	28	27	26	25	24
DAP_TIMEOUT_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DAP_TIMEOUT_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DAP_TIMEOUT_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAP_TIMEOUT_REGISTER							
R/W							
0h							

Table 14-35988. DRM_CFG_0_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.10.2.2.325 DRM_CFG_0_CONFIG Register

1 DRM_CFG_0_CONFIG Register (Offset = 18h) [reset = 0h]

This register adds softreset capability to the suspend module.

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Table 14-35989. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2018h**

Figure 14-11903. DRM_CFG_0_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFTRESET
R							R/W
0h							0h

Table 14-35991. DRM_CFG_0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.10.2.2.326 DRM_CFG_0_EMUTRIGEN Register

1 DRM_CFG_0_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

This register is used to enable EMU triggers.

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Table 14-35992. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 201Ch**

Figure 14-11904. DRM_CFG_0_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-35994. DRM_CFG_0_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.10.2.2.327 DRM_CFG_0_BINVALLO Register

1 DRM_CFG_0_BINVALLO Register (Offset = 20h) [reset = 0h]

Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-35995. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2020h**

Figure 14-11905. DRM_CFG_0_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-35997. DRM_CFG_0_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.10.2.2.328 DRM_CFG_0_BINVALHI Register

1 DRM_CFG_0_BINVALHI Register (Offset = 24h) [reset = 0h]

Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-35998. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2024h**

Figure 14-11906. DRM_CFG_0_BINVALHI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	BINTIMEHI						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
BINTIMEHI							
R							
0h							

Table 14-36000. DRM_CFG_0_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.10.2.2.329 DRM_CFG_0_SUSPEND_REG0 Register

1 DRM_CFG_0_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-36001. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2200h**

Figure 14-11907. DRM_CFG_0_SUSPEND_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>SELECT</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SELECT</td><td colspan="3">RESERVED0</td><td>SUSPEND_CTL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-36003. DRM_CFG_0_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.10.2.2.330 DRM_CFG_0_SUSPEND_REG1 Register

1 DRM_CFG_0_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36004. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2204h**

Figure 14-11908. DRM_CFG_0_SUSPEND_REG1 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_1							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_1							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_1							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_1							
R/W							
0h							

Table 14-36006. DRM_CFG_0_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.331 DRM_CFG_0_SUSPEND_REG2 Register

1 DRM_CFG_0_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36007. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2208h

Figure 14-11909. DRM_CFG_0_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_2							
R/W							
0h							

Table 14-36009. DRM_CFG_0_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.332 DRM_CFG_0_SUSPEND_REG3 Register

1 DRM_CFG_0_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36010. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 220Ch**

Figure 14-11910. DRM_CFG_0_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-36012. DRM_CFG_0_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.333 DRM_CFG_0_SUSPEND_REG4 Register

1 DRM_CFG_0_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36013. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2210h**

Figure 14-11911. DRM_CFG_0_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-36015. DRM_CFG_0_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.334 DRM_CFG_0_SUSPEND_REG5 Register

1 DRM_CFG_0_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36016. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2214h**

Figure 14-11912. DRM_CFG_0_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-36018. DRM_CFG_0_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.335 DRM_CFG_0_SUSPEND_REG6 Register

1 DRM_CFG_0_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36019. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2218h**

Figure 14-11913. DRM_CFG_0_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-36021. DRM_CFG_0_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.336 DRM_CFG_0_SUSPEND_REG7 Register

1 DRM_CFG_0_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36022. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 221Ch**

Figure 14-11914. DRM_CFG_0_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-36024. DRM_CFG_0_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.337 DRM_CFG_0_SUSPEND_REG8 Register

1 DRM_CFG_0_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36025. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2220h**

Figure 14-11915. DRM_CFG_0_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-36027. DRM_CFG_0_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.338 DRM_CFG_0_SUSPEND_REG9 Register

1 DRM_CFG_0_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36028. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2224h**

Figure 14-11916. DRM_CFG_0_SUSPEND_REG9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36030. DRM_CFG_0_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.339 DRM_CFG_0_SUSPEND_REG10 Register

1 DRM_CFG_0_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36031. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2228h**

Figure 14-11917. DRM_CFG_0_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-36033. DRM_CFG_0_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.340 DRM_CFG_0_SUSPEND_REG11 Register

1 DRM_CFG_0_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36034. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 222Ch**

Figure 14-11918. DRM_CFG_0_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-36036. DRM_CFG_0_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.341 DRM_CFG_0_SUSPEND_REG12 Register

1 DRM_CFG_0_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36037. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2230h**

Figure 14-11919. DRM_CFG_0_SUSPEND_REG12 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_12							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_12							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_12							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_12							
R/W							
0h							

Table 14-36039. DRM_CFG_0_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.342 DRM_CFG_0_SUSPEND_REG13 Register

1 DRM_CFG_0_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36040. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2234h**

Figure 14-11920. DRM_CFG_0_SUSPEND_REG13 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_13							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_13							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_13							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_13							
R/W							
0h							

Table 14-36042. DRM_CFG_0_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.343 DRM_CFG_0_SUSPEND_REG14 Register

1 DRM_CFG_0_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36043. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2238h**

Figure 14-11921. DRM_CFG_0_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-36045. DRM_CFG_0_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.344 DRM_CFG_0_SUSPEND_REG15 Register

1 DRM_CFG_0_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36046. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 223Ch**

Figure 14-11922. DRM_CFG_0_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-36048. DRM_CFG_0_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.345 DRM_CFG_0_SUSPEND_REG16 Register

1 DRM_CFG_0_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36049. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2240h**

Figure 14-11923. DRM_CFG_0_SUSPEND_REG16 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_16							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_16							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_16							
R/W							
0h							

Table 14-36051. DRM_CFG_0_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.346 DRM_CFG_0_SUSPEND_REG17 Register

1 DRM_CFG_0_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36052. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2244h**

Figure 14-11924. DRM_CFG_0_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-36054. DRM_CFG_0_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.347 DRM_CFG_0_SUSPEND_REG18 Register

1 DRM_CFG_0_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36055. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2248h**

Figure 14-11925. DRM_CFG_0_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-36057. DRM_CFG_0_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.348 DRM_CFG_0_SUSPEND_REG19 Register

1 DRM_CFG_0_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36058. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 224Ch**

Figure 14-11926. DRM_CFG_0_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-36060. DRM_CFG_0_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.349 DRM_CFG_0_SUSPEND_REG20 Register

1 DRM_CFG_0_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36061. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2250h**

Figure 14-11927. DRM_CFG_0_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_20							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_20							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_20							
R/W							
0h							

Table 14-36063. DRM_CFG_0_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.350 DRM_CFG_0_SUSPEND_REG21 Register

1 DRM_CFG_0_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36064. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2254h**

Figure 14-11928. DRM_CFG_0_SUSPEND_REG21 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_21							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_21							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_21							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_21							
R/W							
0h							

Table 14-36066. DRM_CFG_0_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.351 DRM_CFG_0_SUSPEND_REG22 Register

1 DRM_CFG_0_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36067. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2258h**

Figure 14-11929. DRM_CFG_0_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-36069. DRM_CFG_0_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.352 DRM_CFG_0_SUSPEND_REG23 Register

1 DRM_CFG_0_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36070. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 225Ch**

Figure 14-11930. DRM_CFG_0_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-36072. DRM_CFG_0_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.353 DRM_CFG_0_SUSPEND_REG24 Register

1 DRM_CFG_0_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36073. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2260h**

Figure 14-11931. DRM_CFG_0_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-36075. DRM_CFG_0_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.354 DRM_CFG_0_SUSPEND_REG25 Register

1 DRM_CFG_0_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36076. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2264h**

Figure 14-11932. DRM_CFG_0_SUSPEND_REG25 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_25							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_25							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_25							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_25							
R/W							
0h							

Table 14-36078. DRM_CFG_0_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.355 DRM_CFG_0_SUSPEND_REG26 Register

1 DRM_CFG_0_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36079. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2268h**

Figure 14-11933. DRM_CFG_0_SUSPEND_REG26 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_26							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_26							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_26							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_26							
R/W							
0h							

Table 14-36081. DRM_CFG_0_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.356 DRM_CFG_0_SUSPEND_REG27 Register

1 DRM_CFG_0_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36082. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 226Ch**

Figure 14-11934. DRM_CFG_0_SUSPEND_REG27 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_27							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_27							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_27							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_27							
R/W							
0h							

Table 14-36084. DRM_CFG_0_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.357 DRM_CFG_0_SUSPEND_REG28 Register

1 DRM_CFG_0_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36085. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2270h**

Figure 14-11935. DRM_CFG_0_SUSPEND_REG28 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_28							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_28							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_28							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_28							
R/W							
0h							

Table 14-36087. DRM_CFG_0_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.358 DRM_CFG_0_SUSPEND_REG29 Register

1 DRM_CFG_0_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36088. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2274h**

Figure 14-11936. DRM_CFG_0_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-36090. DRM_CFG_0_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.359 DRM_CFG_0_SUSPEND_REG30 Register

1 DRM_CFG_0_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36091. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 2278h**

Figure 14-11937. DRM_CFG_0_SUSPEND_REG30 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_30							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_30							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_30							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_30							
R/W							
0h							

Table 14-36093. DRM_CFG_0_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.360 DRM_CFG_0_SUSPEND_REG31 Register

1 DRM_CFG_0_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-36094. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 227Ch**

Figure 14-11938. DRM_CFG_0_SUSPEND_REG31 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_31							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_31							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_31							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_31							
R/W							
0h							

Table 14-36096. DRM_CFG_0_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.361 CSTPIU_CFG_0_SUPPORTSIZE Register

1 CSTPIU_CFG_0_SUPPORTSIZE Register (Offset = 0h) [reset = 0h]

This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-36097. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4000h**

Figure 14-11939. CSTPIU_CFG_0_SUPPORTSIZE Name Register

31	30	29	28	27	26	25	24
SUPPORTSIZEREG							
R							
0h							
23	22	21	20	19	18	17	16
SUPPORTSIZEREG							
R							
0h							
15	14	13	12	11	10	9	8
SUPPORTSIZEREG							
R							
0h							
7	6	5	4	3	2	1	0
SUPPORTSIZEREG							
R							
0h							

Table 14-36099. CSTPIU_CFG_0_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	0h	This register indicates how many trace pins are available for export One pin per bit, right justified

14.10.2.2.362 CSTPIU_CFG_0_CURPORTSIZE Register

1 CSTPIU_CFG_0_CURPORTSIZE Register (Offset = 4h) [reset = 0h]

The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-36100. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4004h**

Figure 14-11940. CSTPIU_CFG_0_CURPORTSIZE Name Register

31	30	29	28	27	26	25	24
CURRENTPORTSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
CURRENTPORTSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
CURRENTPORTSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
CURRENTPORTSIZE							
R/W							
0h							

Table 14-36102. CSTPIU_CFG_0_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	0h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.10.2.2.363 CSTPIU_CFG_0_TRIGMODEREG Register

1 CSTPIU_CFG_0_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-36103. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4100h**

Figure 14-11941. CSTPIU_CFG_0_TRIGMODEREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						TRGRUN	TRIGGERED
R						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED2							TCOUNT8
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED1			MUILTPLIERS				
R			R				
0h			0h				

Table 14-36105. CSTPIU_CFG_0_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running A trigger has occurred but the counter is not at zero
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported Each bit is a mpy value

14.10.2.2.364 CSTPIU_CFG_0_TRIGCTRREG Register

1 CSTPIU_CFG_0_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-36106. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4104h**

Figure 14-11942. CSTPIU_CFG_0_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGCOUNT							
R/W							
0h							

Table 14-36108. CSTPIU_CFG_0_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted

14.10.2.2.365 CSTPIU_CFG_0_TRIGMPYREG Register

1 CSTPIU_CFG_0_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-36109. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4108h**

Figure 14-11943. CSTPIU_CFG_0_TRIGMPYREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MULTIPLIER</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-36111. CSTPIU_CFG_0_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K

14.10.2.2.366 CSTPIU_CFG_0_SUPTESTPAT Register

1 CSTPIU_CFG_0_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-36112. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4200h**

Figure 14-11944. CSTPIU_CFG_0_SUPTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">PATTERN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36114. CSTPIU_CFG_0_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.10.2.2.367 CSTPIU_CFG_0_CURTESTPAT Register

1 CSTPIU_CFG_0_CURTESTPAT Register (Offset = 204h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-36115. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4204h**

Figure 14-11945. CSTPIU_CFG_0_CURTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						MODE	
R						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				RESERVED	PATTERN		
R				NONE	R/W		
0h				0h	0h		

Table 14-36117. CSTPIU_CFG_0_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.10.2.2.368 CSTPIU_CFG_0_TESTPATCNT Register

1 CSTPIU_CFG_0_TESTPATCNT Register (Offset = 208h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-36118. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4208h**

Figure 14-11946. CSTPIU_CFG_0_TESTPATCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PATTERNCOUNT							
R/W							
0h							

Table 14-36120. CSTPIU_CFG_0_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.10.2.2.369 CSTPIU_CFG_0_FORMFLUSHSTAT Register

1 CSTPIU_CFG_0_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-36121. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4300h**

Figure 14-11947. CSTPIU_CFG_0_FORMFLUSHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TCPRESENT	FTSTOPPED	FLINPROG
R					R	R	R
0h					0h	0h	0h

Table 14-36123. CSTPIU_CFG_0_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped The formatter has received a stop request signal and all trace data and post-amble has been output
0	FLINPROG	R	0h	Flush In Progress This is an indication of the current state of AFVALIDS

14.10.2.2.370 CSTPIU_CFG_0_FORMFLUSHCTL Register

1 CSTPIU_CFG_0_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

This register controls the generation of stop, trigger, and flush events.

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Table 14-36124. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4304h**

Figure 14-11948. CSTPIU_CFG_0_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-36126. CSTPIU_CFG_0_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS]
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system It is cleared when this flush has been serviced
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting Do not embed Triggers into the formatted stream

14.10.2.2.371 CSTPIU_CFG_0_FORMSYNCCTR Register

1 CSTPIU_CFG_0_FORMSYNCCTR Register (Offset = 308h) [reset = 0h]

This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-36127. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4308h**

Figure 14-11949. CSTPIU_CFG_0_FORMSYNCCTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CYCCOUNT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CYCCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36129. CSTPIU_CFG_0_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	0h	12-bit counter value to indicate the number of complete frames between full sync packets

14.10.2.2.372 CSTPIU_CFG_0_EXTCTLIN Register

1 CSTPIU_CFG_0_EXTCTLIN Register (Offset = 400h) [reset = 0h]

This register inputs data from an external port (if used)

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Table 14-36130. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4400h**

Figure 14-11950. CSTPIU_CFG_0_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-36132. CSTPIU_CFG_0_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.10.2.2.373 CSTPIU_CFG_0_EXTCTLOUT Register

1 CSTPIU_CFG_0_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

This register is output to an external port (if used)

Return to Summary Table

Table 14-36133. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4404h**

Figure 14-11951. CSTPIU_CFG_0_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-36135. CSTPIU_CFG_0_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.10.2.2.374 CSTPIU_CFG_0_ITTRFLINACK Register

1 CSTPIU_CFG_0_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Integration Test Trigger In and Flush In Acknowledge.

Return to Summary Table

Table 14-36136. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4EE4h**

Figure 14-11952. CSTPIU_CFG_0_ITTRFLINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ATID	
R						R/W	
0h						0h	

Table 14-36138. CSTPIU_CFG_0_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.10.2.2.375 CSTPIU_CFG_0_ITTRFLIN Register

1 CSTPIU_CFG_0_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Integration Test Trigger In and Flush In Register.

Return to Summary Table

Table 14-36139. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EE8h

Figure 14-11953. CSTPIU_CFG_0_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
INTEGRATIONTRFLIN							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATIONTRFLIN							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATIONTRFLIN							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATIONTRFLIN							
R/W							
0h							

Table 14-36141. CSTPIU_CFG_0_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATIONTRFLIN	R/W	0h	

14.10.2.2.376 CSTPIU_CFG_0_ITATBDATA0 Register

1 CSTPIU_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test ATB Data Register 0

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Table 14-36142. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4EECh**

Figure 14-11954. CSTPIU_CFG_0_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_REG							
R/W							
0h							

Table 14-36144. CSTPIU_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_REG	R/W	0h	

14.10.2.2.377 CSTPIU_CFG_0_ITATBCTR2 Register

1 CSTPIU_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test ATB Control Register 2.

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Table 14-36145. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4EF0h**

Figure 14-11955. CSTPIU_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							

Table 14-36147. CSTPIU_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG2	R/W	0h	

14.10.2.2.378 CSTPIU_CFG_0_ITATBCTR1 Register

1 CSTPIU_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test ATB Control Register 1.

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Table 14-36148. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4EF4h**

Figure 14-11956. CSTPIU_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							

Table 14-36150. CSTPIU_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG1	R/W	0h	

14.10.2.2.379 CSTPIU_CFG_0_ITATBCTR0 Register

1 CSTPIU_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test ATB Control Register 0

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Table 14-36151. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4EF8h**

Figure 14-11957. CSTPIU_CFG_0_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							

Table 14-36153. CSTPIU_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG0	R/W	0h	

14.10.2.2.380 CSTPIU_CFG_0_INTCTRL Register

1 CSTPIU_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-36154. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4F00h**

Figure 14-11958. CSTPIU_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-36156. CSTPIU_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.10.2.2.381 CSTPIU_CFG_0_CTSET Register

1 CSTPIU_CFG_0_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-36157. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FA0h**

Figure 14-11959. CSTPIU_CFG_0_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-36159. CSTPIU_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.382 CSTPIU_CFG_0_CTCLR Register

1 CSTPIU_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-36160. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FA4h**

Figure 14-11960. CSTPIU_CFG_0_CTCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36162. CSTPIU_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.383 CSTPIU_CFG_0_LAREG Register

1 CSTPIU_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-36163. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FB0h**

Figure 14-11961. CSTPIU_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-36165. CSTPIU_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.10.2.2.384 CSTPIU_CFG_0_LSREG Register

1 CSTPIU_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-36166. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FB4h**

Figure 14-11962. CSTPIU_CFG_0_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-36168. CSTPIU_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.385 CSTPIU_CFG_0_AUTHST Register

1 CSTPIU_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-36169. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FB8h**

Figure 14-11963. CSTPIU_CFG_0_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-36171. CSTPIU_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.386 CSTPIU_CFG_0_DEVID Register

1 CSTPIU_CFG_0_DEVID Register (Offset = FC8h) [reset = 0h]

This shows the characteristics of the TPIU

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Table 14-36172. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FC8h**

Figure 14-11964. CSTPIU_CFG_0_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED				SWO_UART	SWO_MANCHESTER	TRACE_CLOCK_SUP	FIFO_SIZE
R				R	R	R	R
0h				0h	0h	0h	0h

7	6	5	4	3	2	1	0
FIFO_SIZE		CLOCK_RELATIONSHIP	HIDDEN_MUXING				
R		R	R				
0h		0h	0h				

Table 14-36174. CSTPIU_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWO_UART	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported Defaul = 0
10	SWO_MANCHESTER	R	0h	Indicates Serial Wire Output [Manchester] is not supported Default = 0
9	TRACE_CLOCK_SUP	R	0h	Indicates trace clock + data is supported
8:6	FIFO_SIZE	R	0h	FIFO size in powers of 2 A value of 2 gives a FIFO size of 4 entries, 16 bytes Default is3'b010
5	CLOCK_RELATIONSHIP	R	0h	Indicates the relationship between ATCLK and TRACECLKIN 0x1 indicates asynchronous
4:0	HIDDEN_MUXING	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB Currently only 0x00 is supported, that is, no multiplexing present

14.10.2.2.387 CSTPIU_CFG_0_DEVTYPEID Register

1 CSTPIU_CFG_0_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-36175. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FCCh**

Figure 14-11965. CSTPIU_CFG_0_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-36177. CSTPIU_CFG_0_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.10.2.2.388 CSTPIU_CFG_0_PERID4 Register

1 CSTPIU_CFG_0_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-36178. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FD0h**

Figure 14-11966. CSTPIU_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-36180. CSTPIU_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.389 CSTPIU_CFG_0_PERID0 Register

1 CSTPIU_CFG_0_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-36181. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FE0h**

Figure 14-11967. CSTPIU_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-36183. CSTPIU_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.390 CSTPIU_CFG_0_PERID1 Register

1 CSTPIU_CFG_0_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-36184. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FE4h**

Figure 14-11968. CSTPIU_CFG_0_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-36186. CSTPIU_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.391 CSTPIU_CFG_0_PERID2 Register

1 CSTPIU_CFG_0_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-36187. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FE8h**

Figure 14-11969. CSTPIU_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPH_ID2							
R							
0h							

Table 14-36189. CSTPIU_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.392 CSTPIU_CFG_0_PERID3 Register

1 CSTPIU_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-36190. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	**0007 2000 4FECh**

Figure 14-11970. CSTPIU_CFG_0_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-36192. CSTPIU_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.393 CSTPIU_CFG_0_COMPID0 Register

1 CSTPIU_CFG_0_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-36193. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FF0h

Figure 14-11971. CSTPIU_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-36195. CSTPIU_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.394 CSTPIU_CFG_0_COMPID1 Register

1 CSTPIU_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-36196. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FF4h**

Figure 14-11972. CSTPIU_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-36198. CSTPIU_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.395 CSTPIU_CFG_0_COMPID2 Register

1 CSTPIU_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-36199. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FF8h**

Figure 14-11973. CSTPIU_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-36201. CSTPIU_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.396 CSTPIU_CFG_0_COMPID3 Register

1 CSTPIU_CFG_0_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

Return to Summary Table

Table 14-36202. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 4FFCh**

Figure 14-11974. CSTPIU_CFG_0_COMPID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36204. CSTPIU_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.397 CTF_CFG_0_CSTFCTLREG Register

1 CTF_CFG_0_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

It enables the target ports and defines the hold time of the target ports.

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Table 14-36205. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5000h**

Figure 14-11975. CTF_CFG_0_CSTFCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				MINHOLDTIME			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SLVPORTEN							
R/W							
0h							

Table 14-36207. CTF_CFG_0_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel initiator port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.10.2.2.398 CTF_CFG_0_PRIORCTLREG Register

1 CTF_CFG_0_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-36208. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5004h**

Figure 14-11976. CTF_CFG_0_PRIORCTLREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">PRIPORT7</td><td colspan="3">PRIPORT6</td><td colspan="2">PRIPORT5</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="3">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PRIPORT5</td><td colspan="3">PRIPORT4</td><td colspan="3">PRIPORT3</td><td>PRIPORT2</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PRIPORT2</td><td colspan="3">PRIPORT1</td><td colspan="3">PRIPORT0</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-36210. CTF_CFG_0_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.10.2.2.399 CTF_CFG_0_ITATBDATA0 Register

1 CTF_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test Register.

Return to Summary Table

Table 14-36211. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5EECh

Figure 14-11977. CTF_CFG_0_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			ATDATA31	ATDATA23	ATDATA15	ATDATA7	ATDATA0
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-36213. CTF_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.10.2.2.400 CTF_CFG_0_ITATBCTR2 Register

1 CTF_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test Control Register 2.

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Table 14-36214. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5EF0h**

Figure 14-11978. CTF_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-36216. CTF_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.10.2.2.401 CTF_CFG_0_ITATBCTR1 Register

1 CTF_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test Control Register 1.

Return to Summary Table

Table 14-36217. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5EF4h**

Figure 14-11979. CTF_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-36219. CTF_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.10.2.2.402 CTF_CFG_0_ITATBCTR0 Register

1 CTF_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test Control Register 0.

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Table 14-36220. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5EF8h**

Figure 14-11980. CTF_CFG_0_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1						ATBYTES	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						AFREADY	ATVALID
R						R/W	R/W
0h						0h	0h

Table 14-36222. CTF_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.10.2.2.403 CTF_CFG_0_INTCTRL Register

1 CTF_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-36223. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5F00h**

Figure 14-11981. CTF_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-36225. CTF_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.10.2.2.404 CTF_CFG_0_CTSET Register

1 CTF_CFG_0_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-36226. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FA0h**

Figure 14-11982. CTF_CFG_0_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-36228. CTF_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.405 CTF_CFG_0_CTCLR Register

1 CTF_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-36229. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FA4h**

Figure 14-11983. CTF_CFG_0_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-36231. CTF_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.406 CTF_CFG_0_LAREG Register

1 CTF_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-36232. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FB0h**

Figure 14-11984. CTF_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-36234. CTF_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.10.2.2.407 CTF_CFG_0_LSREG Register

1 CTF_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-36235. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	**0007 2000 5FB4h**

Figure 14-11985. CTF_CFG_0_LSREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">LOCK_STATUS</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-36237. CTF_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.408 CTF_CFG_0_AUTHST Register

1 CTF_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-36238. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FB8h**

Figure 14-11986. CTF_CFG_0_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-36240. CTF_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.409 CTF_CFG_0_DEVID Register

1 CTF_CFG_0_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

Return to Summary Table

Table 14-36241. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FC8h**

Figure 14-11987. CTF_CFG_0_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-36243. CTF_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.10.2.2.410 CTF_CFG_0_DEVTYPEID Register

1 CTF_CFG_0_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

Return to Summary Table

Table 14-36244. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FCCh**

Figure 14-11988. CTF_CFG_0_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-36246. CTF_CFG_0_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.10.2.2.411 CTF_CFG_0_PERID4 Register

1 CTF_CFG_0_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

Return to Summary Table

Table 14-36247. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FD0h**

Figure 14-11989. CTF_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-36249. CTF_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.412 CTF_CFG_0_PERID5 Register

1 CTF_CFG_0_PERID5 Register (Offset = FD4h) [reset = 0h]

Peripheral ID5 Register

Return to Summary Table

Table 14-36250. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FD4h**

Figure 14-11990. CTF_CFG_0_PERID5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIPH_ID5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36252. CTF_CFG_0_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.10.2.2.413 CTF_CFG_0_PERID6 Register

1 CTF_CFG_0_PERID6 Register (Offset = FD8h) [reset = 0h]

Peripheral ID6 Register

Return to Summary Table

Table 14-36253. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FD8h**

Figure 14-11991. CTF_CFG_0_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-36255. CTF_CFG_0_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.10.2.2.414 CTF_CFG_0_PERID7 Register

1 CTF_CFG_0_PERID7 Register (Offset = FDCh) [reset = 0h]

Peripheral ID7 Register

Return to Summary Table

Table 14-36256. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FDCh**

Figure 14-11992. CTF_CFG_0_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID7							
R							
0h							

Table 14-36258. CTF_CFG_0_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.10.2.2.415 CTF_CFG_0_PERID0 Register

1 CTF_CFG_0_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

Return to Summary Table

Table 14-36259. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FE0h**

Figure 14-11993. CTF_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-36261. CTF_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.416 CTF_CFG_0_PERID1 Register

1 CTF_CFG_0_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

Return to Summary Table

Table 14-36262. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FE4h**

Figure 14-11994. CTF_CFG_0_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-36264. CTF_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.417 CTF_CFG_0_PERID2 Register

1 CTF_CFG_0_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

Return to Summary Table

Table 14-36265. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FE8h

Figure 14-11995. CTF_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-36267. CTF_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.418 CTF_CFG_0_PERID3 Register

1 CTF_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-36268. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FECh**

Figure 14-11996. CTF_CFG_0_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-36270. CTF_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.419 CTF_CFG_0_COMPID0 Register

1 CTF_CFG_0_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

Return to Summary Table

Table 14-36271. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FF0h**

Figure 14-11997. CTF_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-36273. CTF_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.420 CTF_CFG_0_COMPID1 Register

1 CTF_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

Return to Summary Table

Table 14-36274. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FF4h**

Figure 14-11998. CTF_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-36276. CTF_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.421 CTF_CFG_0_COMPID2 Register

1 CTF_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

Return to Summary Table

Table 14-36277. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FF8h**

Figure 14-11999. CTF_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-36279. CTF_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.422 CTF_CFG_0_COMPID3 Register

1 CTF_CFG_0_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

Return to Summary Table

Table 14-36280. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 2000 5FFCh**

Figure 14-12000. CTF_CFG_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-36282. CTF_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.423 ROM_TABLE_0_1_ROM_ENTRY0 Register

1 ROM_TABLE_0_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

rom table entry 0

Return to Summary Table

Table 14-36283. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0000h**

Figure 14-12001. ROM_TABLE_0_1_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
2h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36285. ROM_TABLE_0_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.424 ROM_TABLE_0_1_ROM_ENTRY1 Register

1 ROM_TABLE_0_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

rom table entry 1

Return to Summary Table

Table 14-36286. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0004h**

Figure 14-12002. ROM_TABLE_0_1_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2000h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-36288. ROM_TABLE_0_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.425 ROM_TABLE_0_1_ROM_ENTRY2 Register

1 ROM_TABLE_0_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

rom table entry 2

Return to Summary Table

Table 14-36289. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0008h**

Figure 14-12003. ROM_TABLE_0_1_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RA30			PWRID
NONE				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36291. ROM_TABLE_0_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.426 ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

rom table manual entry 0

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Table 14-36292. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0008h**

Figure 14-12004. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36294. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.427 ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

rom table manual entry 1

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Table 14-36295. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 000Ch**

Figure 14-12005. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36297. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.428 ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

rom table manual entry 2

Return to Summary Table

Table 14-36298. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0010h**

Figure 14-12006. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36300. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.429 ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

rom table manual entry 3

Return to Summary Table

Table 14-36301. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0014h**

Figure 14-12007. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36303. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.430 ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

rom table manual entry 4

Return to Summary Table

Table 14-36304. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0018h**

Figure 14-12008. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36306. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.431 ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

rom table manual entry 5

Return to Summary Table

Table 14-36307. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 001Ch**

Figure 14-12009. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36309. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.432 ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

rom table manual entry 6

Return to Summary Table

Table 14-36310. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0020h**

Figure 14-12010. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36312. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.433 ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

rom table manual entry 7

Return to Summary Table

Table 14-36313. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0024h**

Figure 14-12011. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36315. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.434 ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

rom table manual entry 8

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Table 14-36316. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0028h**

Figure 14-12012. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36318. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.435 ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

rom table manual entry 9

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Table 14-36319. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 002Ch**

Figure 14-12013. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36321. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.436 ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

rom table manual entry 10

Return to Summary Table

Table 14-36322. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0030h**

Figure 14-12014. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36324. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.437 ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

rom table manual entry 11

Return to Summary Table

Table 14-36325. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0034h**

Figure 14-12015. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36327. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.438 ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

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Table 14-36328. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0038h**

Figure 14-12016. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36330. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.439 ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

rom table manual entry 13

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Table 14-36331. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 003Ch**

Figure 14-12017. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36333. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.440 ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

rom table manual entry 14

Return to Summary Table

Table 14-36334. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0040h**

Figure 14-12018. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36336. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.441 ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

rom table manual entry 15

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Table 14-36337. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0044h**

Figure 14-12019. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36339. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.442 ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

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Table 14-36340. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0048h**

Figure 14-12020. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36342. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.443 ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

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Table 14-36343. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 004Ch**

Figure 14-12021. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36345. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.444 ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

rom table manual entry 18

Return to Summary Table

Table 14-36346. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0050h**

Figure 14-12022. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36348. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.445 ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

rom table manual entry 19

Return to Summary Table

Table 14-36349. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0054h**

Figure 14-12023. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36351. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.446 ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

rom table manual entry 20

Return to Summary Table

Table 14-36352. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0058h**

Figure 14-12024. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36354. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.447 ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

rom table manual entry 21

Return to Summary Table

Table 14-36355. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 005Ch**

Figure 14-12025. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36357. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.448 ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

rom table manual entry 22

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Table 14-36358. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0060h**

Figure 14-12026. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36360. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.449 ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

rom table manual entry 23

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Table 14-36361. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0064h**

Figure 14-12027. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36363. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.450 ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

rom table manual entry 24

Return to Summary Table

Table 14-36364. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0068h**

Figure 14-12028. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36366. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.451 ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

rom table manual entry 25

Return to Summary Table

Table 14-36367. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 006Ch**

Figure 14-12029. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36369. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.452 ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

rom table manual entry 26

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Table 14-36370. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0070h**

Figure 14-12030. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36372. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.453 ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

rom table manual entry 27

Return to Summary Table

Table 14-36373. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0074h**

Figure 14-12031. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36375. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.454 ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

rom table manual entry 28

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Table 14-36376. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0078h**

Figure 14-12032. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36378. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.455 ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

rom table manual entry 29

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Table 14-36379. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 007Ch**

Figure 14-12033. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36381. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.456 ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

rom table manual entry 30

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Table 14-36382. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0080h**

Figure 14-12034. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36384. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.457 ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

rom table manual entry 31

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Table 14-36385. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0084h**

Figure 14-12035. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36387. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.458 ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

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Table 14-36388. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0088h**

Figure 14-12036. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36390. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.459 ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

rom table manual entry 33

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Table 14-36391. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 008Ch**

Figure 14-12037. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36393. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.460 ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

rom table manual entry 34

Return to Summary Table

Table 14-36394. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0090h**

Figure 14-12038. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36396. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.461 ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

rom table manual entry 35

Return to Summary Table

Table 14-36397. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0094h**

Figure 14-12039. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36399. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.462 ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

rom table manual entry 36

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Table 14-36400. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0098h**

Figure 14-12040. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36402. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.463 ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

rom table manual entry 37

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Table 14-36403. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 009Ch**

Figure 14-12041. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36405. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.464 ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

rom table manual entry 38

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Table 14-36406. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00A0h**

Figure 14-12042. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36408. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.465 ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

rom table manual entry 39

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Table 14-36409. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00A4h**

Figure 14-12043. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36411. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.466 ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

rom table manual entry 40

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Table 14-36412. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00A8h**

Figure 14-12044. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36414. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.467 ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

rom table manual entry 41

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Table 14-36415. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00ACh**

Figure 14-12045. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36417. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.468 ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

rom table manual entry 42

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Table 14-36418. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00B0h**

Figure 14-12046. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36420. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.469 ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-36421. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00B4h**

Figure 14-12047. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36423. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.470 ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

rom table manual entry 44

Return to Summary Table

Table 14-36424. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00B8h**

Figure 14-12048. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36426. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.471 ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

rom table manual entry 45

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Table 14-36427. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00BCh**

Figure 14-12049. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36429. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.472 ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-36430. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00C0h

Figure 14-12050. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36432. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.473 ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

rom table manual entry 47

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Table 14-36433. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00C4h**

Figure 14-12051. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36435. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.474 ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

rom table manual entry 48

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Table 14-36436. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00C8h**

Figure 14-12052. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36438. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.475 ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

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Table 14-36439. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00CCh**

Figure 14-12053. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36441. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.476 ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

rom table manual entry 50

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Table 14-36442. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00D0h**

Figure 14-12054. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36444. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.477 ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

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Table 14-36445. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00D4h**

Figure 14-12055. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36447. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.478 ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

rom table manual entry 52

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Table 14-36448. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00D8h**

Figure 14-12056. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36450. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.479 ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

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Table 14-36451. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00DCh**

Figure 14-12057. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36453. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.480 ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

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Table 14-36454. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00E0h**

Figure 14-12058. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36456. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.481 ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

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Table 14-36457. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00E4h**

Figure 14-12059. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36459. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.482 ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

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Table 14-36460. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00E8h**

Figure 14-12060. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36462. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.483 ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

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Table 14-36463. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00ECh**

Figure 14-12061. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36465. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.484 ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

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Table 14-36466. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00F0h**

Figure 14-12062. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36468. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.485 ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

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Table 14-36469. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00F4h**

Figure 14-12063. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36471. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.486 ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

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Table 14-36472. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00F8h**

Figure 14-12064. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36474. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.487 ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

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Table 14-36475. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 00FCh**

Figure 14-12065. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36477. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.488 ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

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Table 14-36478. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0100h**

Figure 14-12066. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-36480. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.489 ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register

1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

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Table 14-36481. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0104h**

Figure 14-12067. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36483. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.10.2.2.490 ROM_TABLE_0_1_PERIPHID0 Register

1 ROM_TABLE_0_1_PERIPHID0 Register (Offset = 108h) [reset = 2h]

debug cell rom table periphids 0

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Table 14-36484. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0108h**

Figure 14-12068. ROM_TABLE_0_1_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-36486. ROM_TABLE_0_1_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.491 ROM_TABLE_0_1_PERIPHID1 Register

1 ROM_TABLE_0_1_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

debug cell rom table periphids 1

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Table 14-36487. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 010Ch**

Figure 14-12069. ROM_TABLE_0_1_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-36489. ROM_TABLE_0_1_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.492 ROM_TABLE_0_1_PERIPHID2 Register

1 ROM_TABLE_0_1_PERIPHID2 Register (Offset = 110h) [reset = 2h]

debug cell rom table periphids 2

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Table 14-36490. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0110h**

Figure 14-12070. ROM_TABLE_0_1_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-36492. ROM_TABLE_0_1_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.493 ROM_TABLE_0_1_PERIPHID3 Register

1 ROM_TABLE_0_1_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-36493. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0114h**

Figure 14-12071. ROM_TABLE_0_1_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-36495. ROM_TABLE_0_1_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.494 ROM_TABLE_0_1_PERIPHID4 Register

1 ROM_TABLE_0_1_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-36496. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 0118h**

Figure 14-12072. ROM_TABLE_0_1_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-36498. ROM_TABLE_0_1_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.495 ROM_TABLE_0_1_COMPID0 Register

1 ROM_TABLE_0_1_COMPID0 Register (Offset = 3FCh) [reset = Dh]

component id

Return to Summary Table

Table 14-36499. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 03FCh**

Figure 14-12073. ROM_TABLE_0_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
Dh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAR							
R							
Dh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAR							
R							
Dh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAR							
R							
Dh							

Table 14-36501. ROM_TABLE_0_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.10.2.2.496 ROM_TABLE_0_1_COMPID1 Register

1 ROM_TABLE_0_1_COMPID1 Register (Offset = 3FCh) [reset = 10h]

component id

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Table 14-36502. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 03FCh**

Figure 14-12074. ROM_TABLE_0_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	22	21	20	19	18	17	16
VAR							
R							
10h							
15	14	13	12	11	10	9	8
VAR							
R							
10h							
7	6	5	4	3	2	1	0
VAR							
R							
10h							

Table 14-36504. ROM_TABLE_0_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.10.2.2.497 ROM_TABLE_0_1_COMPID2 Register

1 ROM_TABLE_0_1_COMPID2 Register (Offset = 3FCh) [reset = 5h]

component id

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Table 14-36505. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 03FCh**

Figure 14-12075. ROM_TABLE_0_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-36507. ROM_TABLE_0_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.10.2.2.498 ROM_TABLE_0_1_COMPID3 Register

1 ROM_TABLE_0_1_COMPID3 Register (Offset = 3FCh) [reset = B1h]

component id

Return to Summary Table

Table 14-36508. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 03FCh**

Figure 14-12076. ROM_TABLE_0_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
B1h							
23	22	21	20	19	18	17	16
VAR							
R							
B1h							
15	14	13	12	11	10	9	8
VAR							
R							
B1h							
7	6	5	4	3	2	1	0
VAR							
R							
B1h							

Table 14-36510. ROM_TABLE_0_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.10.2.2.499 CFGAP_CFG_1_JTAGID_REG Register

1 CFGAP_CFG_1_JTAGID_REG Register (Offset = 0h) [reset = 0h]

This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-36511. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2000h

Figure 14-12077. CFGAP_CFG_1_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-36513. CFGAP_CFG_1_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.10.2.2.500 CFGAP_CFG_1_USERID_REG Register

1 CFGAP_CFG_1_USERID_REG Register (Offset = 4h) [reset = 0h]

This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-36514. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2004h**

Figure 14-12078. CFGAP_CFG_1_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-36516. CFGAP_CFG_1_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.10.2.2.501 CFGAP_CFG_1_VERSION_REG Register

1 CFGAP_CFG_1_VERSION_REG Register (Offset = 8h) [reset = 0h]

This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-36517. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2008h**

Figure 14-12079. CFGAP_CFG_1_VERSION_REG Name Register

31	30	29	28	27	26	25	24
MAJOR_REV				MINOR_REV			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							JTAG_AP
R							R
0h							0h
7	6	5	4	3	2	1	0
POWERAP	AXIAP	APBAP	SECURITYAP	SPARE	ICEPICKM	TRIGGERSUPPORT	TRACESUPPORT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-36519. CFGAP_CFG_1_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.10.2.2.502 CFGAP_CFG_1_SYSTEMSTATUS Register

1 CFGAP_CFG_1_SYSTEMSTATUS Register (Offset = Ch) [reset = 0h]

Reading this register returns system status information.

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Table 14-36520. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 200Ch**

Figure 14-12080. CFGAP_CFG_1_SYSTEMSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-36522. CFGAP_CFG_1_SYSTEMSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved, returns 0

14.10.2.2.503 CFGAP_CFG_1_APID_REGISTER Register

1 CFGAP_CFG_1_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Reading this register returns the ID information for this AP.

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Table 14-36523. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 20FCh**

Figure 14-12081. CFGAP_CFG_1_APID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				107h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
107h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				1h			

Table 14-36525. CFGAP_CFG_1_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.504 APBAP_CFG_1_CSWREG Register

1 APBAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Control/Status Register

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Table 14-36526. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2100h**

Figure 14-12082. APBAP_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36528. APBAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.505 APBAP_CFG_1_TAREG Register

1 APBAP_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-36529. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2104h**

Figure 14-12083. APBAP_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							

Table 14-36531. APBAP_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANSFER_ADDRESS_REGISTER	R/W	0h	This register contains the address to write to or read from

14.10.2.2.506 APBAP_CFG_1_DRWREG Register

1 APBAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-36532. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 210Ch**

Figure 14-12084. APBAP_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36534. APBAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.507 APBAP_CFG_1_BD0REG Register

1 APBAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36535. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2110h**

Figure 14-12085. APBAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36537. APBAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.508 APBAP_CFG_1_BD1REG Register

1 APBAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36538. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2114h**

Figure 14-12086. APBAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36540. APBAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.509 APBAP_CFG_1_BD2REG Register

1 APBAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36541. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2118h**

Figure 14-12087. APBAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36543. APBAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.510 APBAP_CFG_1_BD3REG Register

1 APBAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36544. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 211Ch**

Figure 14-12088. APBAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36546. APBAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.511 APBAP_CFG_1_ROM_REGISTER Register

1 APBAP_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the APB ROM Address.

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Table 14-36547. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 21F8h**

Figure 14-12089. APBAP_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36549. APBAP_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.10.2.2.512 APBAP_CFG_1_ID_REGISTER Register

1 APBAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-36550. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 21FCh**

Figure 14-12090. APBAP_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36552. APBAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.10.2.2.513 AXIAP_CFG_1_CSWREG Register

1 AXIAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This is the control/status register

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Table 14-36553. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2200h**

Figure 14-12091. AXIAP_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DBGSWEN</td><td colspan="7">TYPEEXT</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>SPIDEN</td><td colspan="7">RESERVED2</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">TYPE</td><td colspan="4">MODE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TRINPROG</td><td>RESERVED1</td><td colspan="2">ADDR_INC</td><td>RESERVED0</td><td colspan="3">SIZE</td></tr>
<tr><td>R</td><td>R</td><td colspan="2">R/W</td><td>R</td><td colspan="3">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-36555. AXIAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.10.2.2.514 AXIAP_CFG_1_TAREGL Register

1 AXIAP_CFG_1_TAREGL Register (Offset = 4h) [reset = 0h]

This register contains the lower 32-bits of address to write to or read from.

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Table 14-36556. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2204h**

Figure 14-12092. AXIAP_CFG_1_TAREGL Name Register

31	30	29	28	27	26	25	24
TAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TAL							
R/W							
0h							

Table 14-36558. AXIAP_CFG_1_TAREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAL	R/W	0h	This register contains the lower 32-bits of address

14.10.2.2.515 AXIAP_CFG_1_TAREGH Register

1 AXIAP_CFG_1_TAREGH Register (Offset = 8h) [reset = 0h]

This register contains the upper 32-bits of address to write to or read from.

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Table 14-36559. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2208h**

Figure 14-12093. AXIAP_CFG_1_TAREGH Name Register

31	30	29	28	27	26	25	24
TAH							
R/W							
0h							
23	22	21	20	19	18	17	16
TAH							
R/W							
0h							
15	14	13	12	11	10	9	8
TAH							
R/W							
0h							
7	6	5	4	3	2	1	0
TAH							
R/W							
0h							

Table 14-36561. AXIAP_CFG_1_TAREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAH	R/W	0h	This register contains the upper 32-bits of address

14.10.2.2.516 AXIAP_CFG_1_DRWREG Register

1 AXIAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-36562. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 220Ch**

Figure 14-12094. AXIAP_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36564. AXIAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.517 AXIAP_CFG_1_BD0REG Register

1 AXIAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36565. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2210h**

Figure 14-12095. AXIAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36567. AXIAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.518 AXIAP_CFG_1_BD1REG Register

1 AXIAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36568. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2214h**

Figure 14-12096. AXIAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36570. AXIAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.519 AXIAP_CFG_1_BD2REG Register

1 AXIAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36571. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2218h**

Figure 14-12097. AXIAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36573. AXIAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.520 AXIAP_CFG_1_BD3REG Register

1 AXIAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36574. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 221Ch**

Figure 14-12098. AXIAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36576. AXIAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.521 AXIAP_CFG_1_MBT_REGISTER Register

1 AXIAP_CFG_1_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

This register sets memory barrier attributes

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Table 14-36577. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2220h**

Figure 14-12099. AXIAP_CFG_1_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-36579. AXIAP_CFG_1_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.10.2.2.522 AXIAP_CFG_1_ROM_HI_REGISTER Register

1 AXIAP_CFG_1_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Reading this register returns the AXI ROM Address (63-32).

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Table 14-36580. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 22F0h**

Figure 14-12100. AXIAP_CFG_1_ROM_HI_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_HI_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_HI_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_HI_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_HI_REGISTER_ADDRESS							
R							
0h							

Table 14-36582. AXIAP_CFG_1_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.10.2.2.523 AXIAP_CFG_1_CFG_REGISTER Register

1 AXIAP_CFG_1_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-36583. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 22F4h**

Figure 14-12101. AXIAP_CFG_1_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-36585. AXIAP_CFG_1_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.10.2.2.524 AXIAP_CFG_1_ROM_LO_REGISTER Register

1 AXIAP_CFG_1_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AXI ROM Address (31:12) .

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Table 14-36586. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 22F8h

Figure 14-12102. AXIAP_CFG_1_ROM_LO_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOWBASE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOWBASE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">LOWBASE</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>FORMAT</td><td>PRESENT</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-36588. AXIAP_CFG_1_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.10.2.2.525 AXIAP_CFG_1_ID_REGISTER Register

1 AXIAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-36589. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 22FCh**

Figure 14-12103. AXIAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36591. AXIAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.10.2.2.526 PWRAP_CFG_1_CORE_PRECREG0 Register

1 PWRAP_CFG_1_CORE_PRECREG0 Register (Offset = 0h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. There can be upto 32 of these registers

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Table 14-36592. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2300h**

Figure 14-12104. PWRAP_CFG_1_CORE_PRECREG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RETENTION	RST_OCCURED	PWR_LOSS_DET	INHIBIT_SLEEP	DEBUG_POWER	UNNAT_RESET	IN_RESET_RLS_WIR	RESET_MODE
R	R/W	R/W	R/W	R/W	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESET_MODE		DEBUG_ENABLE	RSV11_12		EXEC_ACTION_DEBUG_ATTEN	RSV8_9	
R/W		R/W	R		R/W	R	
0h		0h	0h		0h	0h	
7	6	5	4	3	2	1	0
PWRDOWNSRD	RSV6	POWERED	CLKDOWNDSRD	FORCE_ACTIVE	CLOCKED	SECURITY	PRESENT
R	R	R	R	R/W	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-36594. PWRAP_CFG_1_CORE_PRECREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23	RETENTION	R	0h	Core is in retention mode
22	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
21	PWR_LOSS_DET	R/W	0h	Power Loss Detected Sticky bit, write a 1 to clear this bit
20	INHIBIT_SLEEP	R/W	0h	Inhinit Sleep Block core from entering sleep mode
19	DEBUG_POWER	R/W	0h	Core debug logic is powered
18	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
17	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the WIR When read this returns the reset status, 1 indicates core is in reset
16:14	RESET_MODE	R/W	0h	Reset Mode 0=normal, 1=WIR, 2=Blk Rst, 3=Blk Assert, 4=Halt on Rst, 5=Cancel, 6=Halt and Block, 7=Halt-Blk-assert
13	DEBUG_ENABLE	R/W	0h	Debug Enabled signal to the core
12:11	RSV11_12	R	0h	Reserved, return 0
10	EXEC_ACTION_DEBUG_ATTEN	R/W	0h	Writing this bit causes Execution Read will return the Debug Attention input value

Table 14-36594. PWRAP_CFG_1_CORE_PRECREG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RSV8_9	R	0h	Reserved, returns 0 when read
7	PWRDOWNDSRD	R	0h	The core wants to turn off it's power when high
6	RSV6	R	0h	Reserved, returns 0 when read
5	POWERED	R	0h	Core is powered up when high
4	CLKDOWNDSRD	R	0h	The core wants to turn off it's clock when high
3	FORCE_ACTIVE	R/W	0h	Force core active Turn on power and clocks
2	CLOCKED	R	0h	When high the core clock is active
1	SECURITY	R	0h	Security bit When high security is allowing access
0	PRESENT	R	0h	The core controlled by this register exists when 1

14.10.2.2.527 PWRAP_CFG_1_CORE_PRECREG1 Register

1 PWRAP_CFG_1_CORE_PRECREG1 Register (Offset = 4h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36595. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2304h**

Figure 14-12105. PWRAP_CFG_1_CORE_PRECREG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36597. PWRAP_CFG_1_CORE_PRECREG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.528 PWRAP_CFG_1_CORE_PRECREG2 Register

1 PWRAP_CFG_1_CORE_PRECREG2 Register (Offset = 8h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

Return to Summary Table

Table 14-36598. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2308h**

Figure 14-12106. PWRAP_CFG_1_CORE_PRECREG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36600. PWRAP_CFG_1_CORE_PRECREG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.529 PWRAP_CFG_1_CORE_PRECREG3 Register

1 PWRAP_CFG_1_CORE_PRECREG3 Register (Offset = Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36601. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 230Ch**

Figure 14-12107. PWRAP_CFG_1_CORE_PRECREG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36603. PWRAP_CFG_1_CORE_PRECREG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.530 PWRAP_CFG_1_CORE_PRECREG4 Register

1 PWRAP_CFG_1_CORE_PRECREG4 Register (Offset = 10h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36604. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2310h**

Figure 14-12108. PWRAP_CFG_1_CORE_PRECREG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36606. PWRAP_CFG_1_CORE_PRECREG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.531 PWRAP_CFG_1_CORE_PRECREG5 Register

1 PWRAP_CFG_1_CORE_PRECREG5 Register (Offset = 14h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36607. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2314h**

Figure 14-12109. PWRAP_CFG_1_CORE_PRECREG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36609. PWRAP_CFG_1_CORE_PRECREG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.532 PWRAP_CFG_1_CORE_PRECREG6 Register

1 PWRAP_CFG_1_CORE_PRECREG6 Register (Offset = 18h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36610. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2318h**

Figure 14-12110. PWRAP_CFG_1_CORE_PRECREG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36612. PWRAP_CFG_1_CORE_PRECREG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.533 PWRAP_CFG_1_CORE_PRECREG7 Register

1 PWRAP_CFG_1_CORE_PRECREG7 Register (Offset = 1Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36613. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 231Ch**

Figure 14-12111. PWRAP_CFG_1_CORE_PRECREG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36615. PWRAP_CFG_1_CORE_PRECREG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.534 PWRAP_CFG_1_CORE_PRECREG8 Register

1 PWRAP_CFG_1_CORE_PRECREG8 Register (Offset = 20h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36616. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2320h**

Figure 14-12112. PWRAP_CFG_1_CORE_PRECREG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36618. PWRAP_CFG_1_CORE_PRECREG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.535 PWRAP_CFG_1_CORE_PRECREG9 Register

1 PWRAP_CFG_1_CORE_PRECREG9 Register (Offset = 24h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

Return to Summary Table

Table 14-36619. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2324h**

Figure 14-12113. PWRAP_CFG_1_CORE_PRECREG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36621. PWRAP_CFG_1_CORE_PRECREG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.536 PWRAP_CFG_1_CORE_PRECREG10 Register

1 PWRAP_CFG_1_CORE_PRECREG10 Register (Offset = 28h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36622. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2328h**

Figure 14-12114. PWRAP_CFG_1_CORE_PRECREG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36624. PWRAP_CFG_1_CORE_PRECREG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.537 PWRAP_CFG_1_CORE_PRECREG11 Register

1 PWRAP_CFG_1_CORE_PRECREG11 Register (Offset = 2Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36625. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 232Ch**

Figure 14-12115. PWRAP_CFG_1_CORE_PRECREG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36627. PWRAP_CFG_1_CORE_PRECREG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.538 PWRAP_CFG_1_CORE_PRECREG12 Register

1 PWRAP_CFG_1_CORE_PRECREG12 Register (Offset = 30h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36628. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2330h**

Figure 14-12116. PWRAP_CFG_1_CORE_PRECREG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36630. PWRAP_CFG_1_CORE_PRECREG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.539 PWRAP_CFG_1_CORE_PRECREG13 Register

1 PWRAP_CFG_1_CORE_PRECREG13 Register (Offset = 34h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36631. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2334h**

Figure 14-12117. PWRAP_CFG_1_CORE_PRECREG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36633. PWRAP_CFG_1_CORE_PRECREG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.540 PWRAP_CFG_1_CORE_PRECREG14 Register

1 PWRAP_CFG_1_CORE_PRECREG14 Register (Offset = 38h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36634. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2338h**

Figure 14-12118. PWRAP_CFG_1_CORE_PRECREG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36636. PWRAP_CFG_1_CORE_PRECREG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.541 PWRAP_CFG_1_CORE_PRECREG15 Register

1 PWRAP_CFG_1_CORE_PRECREG15 Register (Offset = 3Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36637. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 233Ch**

Figure 14-12119. PWRAP_CFG_1_CORE_PRECREG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36639. PWRAP_CFG_1_CORE_PRECREG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.542 PWRAP_CFG_1_CORE_PRECREG16 Register

1 PWRAP_CFG_1_CORE_PRECREG16 Register (Offset = 40h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36640. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2340h**

Figure 14-12120. PWRAP_CFG_1_CORE_PRECREG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36642. PWRAP_CFG_1_CORE_PRECREG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.543 PWRAP_CFG_1_CORE_PRECREG17 Register

1 PWRAP_CFG_1_CORE_PRECREG17 Register (Offset = 44h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36643. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2344h**

Figure 14-12121. PWRAP_CFG_1_CORE_PRECREG17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36645. PWRAP_CFG_1_CORE_PRECREG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.544 PWRAP_CFG_1_CORE_PRECREG18 Register

1 PWRAP_CFG_1_CORE_PRECREG18 Register (Offset = 48h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

Return to Summary Table

Table 14-36646. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2348h**

Figure 14-12122. PWRAP_CFG_1_CORE_PRECREG18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36648. PWRAP_CFG_1_CORE_PRECREG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.545 PWRAP_CFG_1_CORE_PRECREG19 Register

1 PWRAP_CFG_1_CORE_PRECREG19 Register (Offset = 4Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

Return to Summary Table

Table 14-36649. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 234Ch**

Figure 14-12123. PWRAP_CFG_1_CORE_PRECREG19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36651. PWRAP_CFG_1_CORE_PRECREG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.546 PWRAP_CFG_1_CORE_PRECREG20 Register

1 PWRAP_CFG_1_CORE_PRECREG20 Register (Offset = 50h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

Return to Summary Table

Table 14-36652. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2350h**

Figure 14-12124. PWRAP_CFG_1_CORE_PRECREG20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36654. PWRAP_CFG_1_CORE_PRECREG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.547 PWRAP_CFG_1_CORE_PRECREG21 Register

1 PWRAP_CFG_1_CORE_PRECREG21 Register (Offset = 54h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36655. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2354h**

Figure 14-12125. PWRAP_CFG_1_CORE_PRECREG21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36657. PWRAP_CFG_1_CORE_PRECREG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.548 PWRAP_CFG_1_CORE_PRECREG22 Register

1 PWRAP_CFG_1_CORE_PRECREG22 Register (Offset = 58h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36658. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2358h**

Figure 14-12126. PWRAP_CFG_1_CORE_PRECREG22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36660. PWRAP_CFG_1_CORE_PRECREG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.549 PWRAP_CFG_1_CORE_PRECREG23 Register

1 PWRAP_CFG_1_CORE_PRECREG23 Register (Offset = 5Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36661. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 235Ch**

Figure 14-12127. PWRAP_CFG_1_CORE_PRECREG23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36663. PWRAP_CFG_1_CORE_PRECREG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.550 PWRAP_CFG_1_CORE_PRECREG24 Register

1 PWRAP_CFG_1_CORE_PRECREG24 Register (Offset = 60h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36664. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2360h**

Figure 14-12128. PWRAP_CFG_1_CORE_PRECREG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36666. PWRAP_CFG_1_CORE_PRECREG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.551 PWRAP_CFG_1_CORE_PRECREG25 Register

1 PWRAP_CFG_1_CORE_PRECREG25 Register (Offset = 64h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36667. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2364h**

Figure 14-12129. PWRAP_CFG_1_CORE_PRECREG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36669. PWRAP_CFG_1_CORE_PRECREG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.552 PWRAP_CFG_1_CORE_PRECREG26 Register

1 PWRAP_CFG_1_CORE_PRECREG26 Register (Offset = 68h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36670. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2368h**

Figure 14-12130. PWRAP_CFG_1_CORE_PRECREG26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36672. PWRAP_CFG_1_CORE_PRECREG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.553 PWRAP_CFG_1_CORE_PRECREG27 Register

1 PWRAP_CFG_1_CORE_PRECREG27 Register (Offset = 6Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36673. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 236Ch**

Figure 14-12131. PWRAP_CFG_1_CORE_PRECREG27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36675. PWRAP_CFG_1_CORE_PRECREG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.554 PWRAP_CFG_1_CORE_PRECREG28 Register

1 PWRAP_CFG_1_CORE_PRECREG28 Register (Offset = 70h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36676. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2370h**

Figure 14-12132. PWRAP_CFG_1_CORE_PRECREG28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36678. PWRAP_CFG_1_CORE_PRECREG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.555 PWRAP_CFG_1_CORE_PRECREG29 Register

1 PWRAP_CFG_1_CORE_PRECREG29 Register (Offset = 74h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36679. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2374h**

Figure 14-12133. PWRAP_CFG_1_CORE_PRECREG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36681. PWRAP_CFG_1_CORE_PRECREG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.556 PWRAP_CFG_1_CORE_PRECREG30 Register

1 PWRAP_CFG_1_CORE_PRECREG30 Register (Offset = 78h) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36682. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2378h**

Figure 14-12134. PWRAP_CFG_1_CORE_PRECREG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36684. PWRAP_CFG_1_CORE_PRECREG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.557 PWRAP_CFG_1_CORE_PRECREG31 Register

1 PWRAP_CFG_1_CORE_PRECREG31 Register (Offset = 7Ch) [reset = 0h]

These registers are used to control functionality of CPUs without JTAG ports. See CORE_PRECREG0 for details

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Table 14-36685. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 237Ch**

Figure 14-12135. PWRAP_CFG_1_CORE_PRECREG31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36687. PWRAP_CFG_1_CORE_PRECREG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.558 PWRAP_CFG_1_SYS_PRECREG Register

1 PWRAP_CFG_1_SYS_PRECREG Register (Offset = F0h) [reset = 0h]

This register is used to control system level functionality

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Table 14-36688. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 23F0h

Figure 14-12136. PWRAP_CFG_1_SYS_PRECREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED			DBGCON_WE	DBGCON			
R			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
UNNAT_RESET	RST_OCCURED	SYSTEM_STAT	RSV12_BIT	GLOB_EXEC_TRIG	CLR_EX_FLAGS	GLOB_EXEC_MSK	IN_RESET_RLS_WIR
R	R/W	R	R	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
WIR_REQ	BLK_SYS_RST	RESERVED0		DEV_TYPE			SYS_RST_REQ
R/W	R/W	R		R			R/W
0h	0h	0h		0h			0h

Table 14-36690. PWRAP_CFG_1_SYS_PRECREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved, returns 0
20	DBGCON_WE	R/W	0h	This bit must be high to write to the debug connect field
19:16	DBGCON	R/W	0h	The system debugger must write a value of 0x9 to be connected and access the debug logic
15	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
14	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
13	SYSTEM_STAT	R	0h	System Status input, application specificall
12	RSV12_BIT	R	0h	Reserved, read returns 0
11	GLOB_EXEC_TRIG	R	0h	
10	CLR_EX_FLAGS	R/W	0h	Clear all run flags
9	GLOB_EXEC_MSK	R/W	0h	Global Execute Mask
8	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the global WIR When read this returns the in reset status
7	WIR_REQ	R/W	0h	Wait In Reset Request
6	BLK_SYS_RST	R/W	0h	Block System Reset
5:4	RESERVED0	R	0h	Reserved0, returns 0
3:1	DEV_TYPE	R	0h	Device Type tieoff value Test, emulator, secure, etc

Table 14-36690. PWRAP_CFG_1_SYS_PRECREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYS_RST_REQ	R/W	0h	System Reset Request This bit will be reset once reset occurs

14.10.2.2.559 PWRAP_CFG_1_ID_REGISTER Register

1 PWRAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 2E0002h]

Reading this register returns the ID information for this AP.

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Table 14-36691. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 23FCh**

Figure 14-12137. PWRAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">17h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">17h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-36693. PWRAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	17h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	2h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.10.2.2.560 PVIEW_CFG_1_PVIEW_STATE0 Register

1 PVIEW_CFG_1_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-36694. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2400h**

Figure 14-12138. PVIEW_CFG_1_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	22	21	20	19	18	17	16
POWER_VIEW_STATE_REG0							
R							
0h							
15	14	13	12	11	10	9	8
POWER_VIEW_STATE_REG0							
R							
0h							
7	6	5	4	3	2	1	0
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-36696. PVIEW_CFG_1_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.10.2.2.561 PVIEW_CFG_1_PVIEW_CAPABILITY Register

1 PVIEW_CFG_1_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-36697. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 24F0h**

Figure 14-12139. PVIEW_CFG_1_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-36699. PVIEW_CFG_1_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.10.2.2.562 PVIEW_CFG_1_ID_REGISTER Register

1 PVIEW_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-36700. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 24FCh**

Figure 14-12140. PVIEW_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36702. PVIEW_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.10.2.2.563 JTAGAP_CFG_1_CSW Register

1 JTAGAP_CFG_1_CSW Register (Offset = 0h) [reset = 0h]

This register provides control and status information

Return to Summary Table

Table 14-36703. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2500h**

Figure 14-12141. JTAGAP_CFG_1_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-36705. JTAGAP_CFG_1_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.10.2.2.564 JTAGAP_CFG_1_PSEL_REG Register

1 JTAGAP_CFG_1_PSEL_REG Register (Offset = 4h) [reset = 0h]

This 8-bit register is used to select the JTAG port.

Return to Summary Table

Table 14-36706. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2504h**

Figure 14-12142. JTAGAP_CFG_1_PSEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_SELECT_REGISTER							
R/W							
0h							

Table 14-36708. JTAGAP_CFG_1_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.10.2.2.565 JTAGAP_CFG_1_PSTA_REG Register

1 JTAGAP_CFG_1_PSTA_REG Register (Offset = 8h) [reset = 0h]

A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

Return to Summary Table

Table 14-36709. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2508h**

Figure 14-12143. JTAGAP_CFG_1_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-36711. JTAGAP_CFG_1_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.10.2.2.566 JTAGAP_CFG_1_BYTEFIFO1 Register

1 JTAGAP_CFG_1_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-36712. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2510h**

Figure 14-12144. JTAGAP_CFG_1_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-36714. JTAGAP_CFG_1_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.10.2.2.567 JTAGAP_CFG_1_BYTEFIFO2 Register

1 JTAGAP_CFG_1_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

Return to Summary Table

Table 14-36715. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2514h**

Figure 14-12145. JTAGAP_CFG_1_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-36717. JTAGAP_CFG_1_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.10.2.2.568 JTAGAP_CFG_1_BYTEFIFO3 Register

1 JTAGAP_CFG_1_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

Return to Summary Table

Table 14-36718. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2518h**

Figure 14-12146. JTAGAP_CFG_1_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYTE_FIFO_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BYTE_FIFO_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTE_FIFO_3							
R/W							
0h							

Table 14-36720. JTAGAP_CFG_1_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.10.2.2.569 JTAGAP_CFG_1_BYTEFIFO4 Register

1 JTAGAP_CFG_1_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

Return to Summary Table

Table 14-36721. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 251Ch**

Figure 14-12147. JTAGAP_CFG_1_BYTEFIFO4 Name Register

31	30	29	28	27	26	25	24
BYTE_FIFO_4							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_4							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_4							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_4							
R/W							
0h							

Table 14-36723. JTAGAP_CFG_1_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.10.2.2.570 JTAGAP_CFG_1_ID_REGISTER Register

1 JTAGAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-36724. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 25FCh**

Figure 14-12148. JTAGAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36726. JTAGAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.10.2.2.571 SECAP_CFG_1_TXDATA Register

1 SECAP_CFG_1_TXDATA Register (Offset = 0h) [reset = 0h]

Data value to send to security controller. Apllication specific

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Table 14-36727. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2600h**

Figure 14-12149. SECAP_CFG_1_TXDATA Name Register

31	30	29	28	27	26	25	24
TX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_DATA_REGISTER							
R/W							
0h							

Table 14-36729. SECAP_CFG_1_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	

14.10.2.2.572 SECAP_CFG_1_TXCTRL Register

1 SECAP_CFG_1_TXCTRL Register (Offset = 4h) [reset = 0h]

Register to send control information to the Security Controller, Application specific

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Table 14-36730. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2604h**

Figure 14-12150. SECAP_CFG_1_TXCTRL Name Register

31	30	29	28	27	26	25	24
TX_CONTROL							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_CONTROL							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_CONTROL							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_CONTROL							TXDAV
R/W							R
0h							0h

Table 14-36732. SECAP_CFG_1_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.10.2.2.573 SECAP_CFG_1_RXDATA Register

1 SECAP_CFG_1_RXDATA Register (Offset = 8h) [reset = 0h]

Data value from the security controller. Apllication specific

Return to Summary Table

Table 14-36733. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2608h**

Figure 14-12151. SECAP_CFG_1_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-36735. SECAP_CFG_1_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	

14.10.2.2.574 SECAP_CFG_1_RXCTRL Register

1 SECAP_CFG_1_RXCTRL Register (Offset = Ch) [reset = 0h]

Register to receive control information from the Security Controller

Return to Summary Table

Table 14-36736. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 260Ch**

Figure 14-12152. SECAP_CFG_1_RXCTRL Name Register

31	30	29	28	27	26	25	24
RX_CONTROL							
R							
0h							
23	22	21	20	19	18	17	16
RX_CONTROL							
R							
0h							
15	14	13	12	11	10	9	8
RX_CONTROL							
R							
0h							
7	6	5	4	3	2	1	0
RX_CONTROL							RXDAV
R							R
0h							0h

Table 14-36738. SECAP_CFG_1_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.10.2.2.575 CORTEX0_CFG_1_CSWREG Register

1 CORTEX0_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-36739. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2700h**

Figure 14-12153. CORTEX0_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36741. CORTEX0_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.576 CORTEX0_CFG_1_TAREG Register

1 CORTEX0_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-36742. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2704h**

Figure 14-12154. CORTEX0_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36744. CORTEX0_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.577 CORTEX0_CFG_1_DRWREG Register

1 CORTEX0_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-36745. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 270Ch**

Figure 14-12155. CORTEX0_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36747. CORTEX0_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.578 CORTEX0_CFG_1_BD0REG Register

1 CORTEX0_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36748. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2710h**

Figure 14-12156. CORTEX0_CFG_1_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36750. CORTEX0_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.579 CORTEX0_CFG_1_BD1REG Register

1 CORTEX0_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36751. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2714h**

Figure 14-12157. CORTEX0_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36753. CORTEX0_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.580 CORTEX0_CFG_1_BD2REG Register

1 CORTEX0_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36754. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2718h**

Figure 14-12158. CORTEX0_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36756. CORTEX0_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.581 CORTEX0_CFG_1_BD3REG Register

1 CORTEX0_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36757. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 271Ch**

Figure 14-12159. CORTEX0_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36759. CORTEX0_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.582 CORTEX0_CFG_1_ROM_REGISTER Register

1 CORTEX0_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36760. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 27F8h**

Figure 14-12160. CORTEX0_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36762. CORTEX0_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.583 CORTEX0_CFG_1_ID_REGISTER Register

1 CORTEX0_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36763. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 27FCh**

Figure 14-12161. CORTEX0_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36765. CORTEX0_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.584 CORTEX1_CFG_1_CSWREG Register

1 CORTEX1_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36766. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2800h**

Figure 14-12162. CORTEX1_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36768. CORTEX1_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.585 CORTEX1_CFG_1_TAREG Register

1 CORTEX1_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-36769. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2804h**

Figure 14-12163. CORTEX1_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36771. CORTEX1_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.586 CORTEX1_CFG_1_DRWREG Register

1 CORTEX1_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36772. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 280Ch**

Figure 14-12164. CORTEX1_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36774. CORTEX1_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.587 CORTEX1_CFG_1_BD0REG Register

1 CORTEX1_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36775. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2810h

Figure 14-12165. CORTEX1_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36777. CORTEX1_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.588 CORTEX1_CFG_1_BD1REG Register

1 CORTEX1_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36778. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2814h**

Figure 14-12166. CORTEX1_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36780. CORTEX1_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.589 CORTEX1_CFG_1_BD2REG Register

1 CORTEX1_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36781. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2818h**

Figure 14-12167. CORTEX1_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36783. CORTEX1_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.590 CORTEX1_CFG_1_BD3REG Register

1 CORTEX1_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36784. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 281Ch**

Figure 14-12168. CORTEX1_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36786. CORTEX1_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.591 CORTEX1_CFG_1_ROM_REGISTER Register

1 CORTEX1_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-36787. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 28F8h**

Figure 14-12169. CORTEX1_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36789. CORTEX1_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.592 CORTEX1_CFG_1_ID_REGISTER Register

1 CORTEX1_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36790. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 28FCh**

Figure 14-12170. CORTEX1_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36792. CORTEX1_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.593 CORTEX2_CFG_1_CSWREG Register

1 CORTEX2_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-36793. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2900h**

Figure 14-12171. CORTEX2_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36795. CORTEX2_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.594 CORTEX2_CFG_1_TAREG Register

1 CORTEX2_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-36796. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2904h**

Figure 14-12172. CORTEX2_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36798. CORTEX2_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.595 CORTEX2_CFG_1_DRWREG Register

1 CORTEX2_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36799. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 290Ch**

Figure 14-12173. CORTEX2_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36801. CORTEX2_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.596 CORTEX2_CFG_1_BD0REG Register

1 CORTEX2_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36802. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2910h**

Figure 14-12174. CORTEX2_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36804. CORTEX2_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.597 CORTEX2_CFG_1_BD1REG Register

1 CORTEX2_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36805. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2914h**

Figure 14-12175. CORTEX2_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36807. CORTEX2_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.598 CORTEX2_CFG_1_BD2REG Register

1 CORTEX2_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36808. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2918h**

Figure 14-12176. CORTEX2_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36810. CORTEX2_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.599 CORTEX2_CFG_1_BD3REG Register

1 CORTEX2_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36811. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 291Ch**

Figure 14-12177. CORTEX2_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36813. CORTEX2_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.600 CORTEX2_CFG_1_ROM_REGISTER Register

1 CORTEX2_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36814. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 29F8h**

Figure 14-12178. CORTEX2_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36816. CORTEX2_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.601 CORTEX2_CFG_1_ID_REGISTER Register

1 CORTEX2_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36817. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 29FCh**

Figure 14-12179. CORTEX2_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36819. CORTEX2_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.602 CORTEX3_CFG_1_CSWREG Register

1 CORTEX3_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36820. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A00h**

Figure 14-12180. CORTEX3_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36822. CORTEX3_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.603 CORTEX3_CFG_1_TAREG Register

1 CORTEX3_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-36823. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A04h**

Figure 14-12181. CORTEX3_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36825. CORTEX3_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.604 CORTEX3_CFG_1_DRWREG Register

1 CORTEX3_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36826. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A0Ch**

Figure 14-12182. CORTEX3_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36828. CORTEX3_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.605 CORTEX3_CFG_1_BD0REG Register

1 CORTEX3_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36829. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A10h**

Figure 14-12183. CORTEX3_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36831. CORTEX3_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.606 CORTEX3_CFG_1_BD1REG Register

1 CORTEX3_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36832. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A14h**

Figure 14-12184. CORTEX3_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36834. CORTEX3_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.607 CORTEX3_CFG_1_BD2REG Register

1 CORTEX3_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36835. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A18h**

Figure 14-12185. CORTEX3_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36837. CORTEX3_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.608 CORTEX3_CFG_1_BD3REG Register

1 CORTEX3_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36838. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2A1Ch**

Figure 14-12186. CORTEX3_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36840. CORTEX3_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.609 CORTEX3_CFG_1_ROM_REGISTER Register

1 CORTEX3_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36841. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2AF8h

Figure 14-12187. CORTEX3_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36843. CORTEX3_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.610 CORTEX3_CFG_1_ID_REGISTER Register

1 CORTEX3_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36844. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2AFCh**

Figure 14-12188. CORTEX3_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36846. CORTEX3_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.611 CORTEX4_CFG_1_CSWREG Register

1 CORTEX4_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36847. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B00h**

Figure 14-12189. CORTEX4_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36849. CORTEX4_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.612 CORTEX4_CFG_1_TAREG Register

1 CORTEX4_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-36850. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B04h**

Figure 14-12190. CORTEX4_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36852. CORTEX4_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.613 CORTEX4_CFG_1_DRWREG Register

1 CORTEX4_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36853. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B0Ch**

Figure 14-12191. CORTEX4_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36855. CORTEX4_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.614 CORTEX4_CFG_1_BD0REG Register

1 CORTEX4_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36856. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B10h**

Figure 14-12192. CORTEX4_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36858. CORTEX4_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.615 CORTEX4_CFG_1_BD1REG Register

1 CORTEX4_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36859. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B14h**

Figure 14-12193. CORTEX4_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36861. CORTEX4_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.616 CORTEX4_CFG_1_BD2REG Register

1 CORTEX4_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36862. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B18h**

Figure 14-12194. CORTEX4_CFG_1_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36864. CORTEX4_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.617 CORTEX4_CFG_1_BD3REG Register

1 CORTEX4_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36865. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2B1Ch**

Figure 14-12195. CORTEX4_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36867. CORTEX4_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.618 CORTEX4_CFG_1_ROM_REGISTER Register

1 CORTEX4_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36868. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2BF8h**

Figure 14-12196. CORTEX4_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36870. CORTEX4_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.619 CORTEX4_CFG_1_ID_REGISTER Register

1 CORTEX4_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36871. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2BFCh**

Figure 14-12197. CORTEX4_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-36873. CORTEX4_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.620 CORTEX5_CFG_1_CSWREG Register

1 CORTEX5_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36874. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C00h**

Figure 14-12198. CORTEX5_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36876. CORTEX5_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.621 CORTEX5_CFG_1_TAREG Register

1 CORTEX5_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-36877. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C04h**

Figure 14-12199. CORTEX5_CFG_1_TAREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36879. CORTEX5_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.622 CORTEX5_CFG_1_DRWREG Register

1 CORTEX5_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36880. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C0Ch**

Figure 14-12200. CORTEX5_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36882. CORTEX5_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.623 CORTEX5_CFG_1_BD0REG Register

1 CORTEX5_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36883. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C10h**

Figure 14-12201. CORTEX5_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36885. CORTEX5_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.624 CORTEX5_CFG_1_BD1REG Register

1 CORTEX5_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36886. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C14h**

Figure 14-12202. CORTEX5_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36888. CORTEX5_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.625 CORTEX5_CFG_1_BD2REG Register

1 CORTEX5_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36889. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C18h**

Figure 14-12203. CORTEX5_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36891. CORTEX5_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.626 CORTEX5_CFG_1_BD3REG Register

1 CORTEX5_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36892. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2C1Ch**

Figure 14-12204. CORTEX5_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36894. CORTEX5_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.627 CORTEX5_CFG_1_ROM_REGISTER Register

1 CORTEX5_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36895. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2CF8h**

Figure 14-12205. CORTEX5_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36897. CORTEX5_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.628 CORTEX5_CFG_1_ID_REGISTER Register

1 CORTEX5_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36898. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2CFCh**

Figure 14-12206. CORTEX5_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36900. CORTEX5_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.629 CORTEX6_CFG_1_CSWREG Register

1 CORTEX6_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36901. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D00h**

Figure 14-12207. CORTEX6_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36903. CORTEX6_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.630 CORTEX6_CFG_1_TAREG Register

1 CORTEX6_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

Return to Summary Table

Table 14-36904. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D04h**

Figure 14-12208. CORTEX6_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36906. CORTEX6_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.631 CORTEX6_CFG_1_DRWREG Register

1 CORTEX6_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36907. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D0Ch**

Figure 14-12209. CORTEX6_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36909. CORTEX6_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.632 CORTEX6_CFG_1_BD0REG Register

1 CORTEX6_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36910. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D10h**

Figure 14-12210. CORTEX6_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36912. CORTEX6_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.633 CORTEX6_CFG_1_BD1REG Register

1 CORTEX6_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36913. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D14h**

Figure 14-12211. CORTEX6_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36915. CORTEX6_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.634 CORTEX6_CFG_1_BD2REG Register

1 CORTEX6_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36916. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2D18h**

Figure 14-12212. CORTEX6_CFG_1_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-36918. CORTEX6_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.635 CORTEX6_CFG_1_BD3REG Register

1 CORTEX6_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36919. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D1Ch

Figure 14-12213. CORTEX6_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36921. CORTEX6_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.636 CORTEX6_CFG_1_ROM_REGISTER Register

1 CORTEX6_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-36922. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2DF8h

Figure 14-12214. CORTEX6_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36924. CORTEX6_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.637 CORTEX6_CFG_1_ID_REGISTER Register

1 CORTEX6_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36925. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2DFCh**

Figure 14-12215. CORTEX6_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36927. CORTEX6_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.638 CORTEX7_CFG_1_CSWREG Register

1 CORTEX7_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-36928. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E00h**

Figure 14-12216. CORTEX7_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36930. CORTEX7_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.639 CORTEX7_CFG_1_TAREG Register

1 CORTEX7_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-36931. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E04h**

Figure 14-12217. CORTEX7_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36933. CORTEX7_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.640 CORTEX7_CFG_1_DRWREG Register

1 CORTEX7_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-36934. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E0Ch**

Figure 14-12218. CORTEX7_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36936. CORTEX7_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.641 CORTEX7_CFG_1_BD0REG Register

1 CORTEX7_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36937. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E10h**

Figure 14-12219. CORTEX7_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36939. CORTEX7_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.642 CORTEX7_CFG_1_BD1REG Register

1 CORTEX7_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36940. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E14h**

Figure 14-12220. CORTEX7_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36942. CORTEX7_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.643 CORTEX7_CFG_1_BD2REG Register

1 CORTEX7_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36943. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E18h

Figure 14-12221. CORTEX7_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36945. CORTEX7_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.644 CORTEX7_CFG_1_BD3REG Register

1 CORTEX7_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36946. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2E1Ch**

Figure 14-12222. CORTEX7_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36948. CORTEX7_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.645 CORTEX7_CFG_1_ROM_REGISTER Register

1 CORTEX7_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-36949. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2EF8h**

Figure 14-12223. CORTEX7_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36951. CORTEX7_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.646 CORTEX7_CFG_1_ID_REGISTER Register

1 CORTEX7_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-36952. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2EFCh**

Figure 14-12224. CORTEX7_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36954. CORTEX7_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.647 CORTEX8_CFG_1_CSWREG Register

1 CORTEX8_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-36955. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F00h**

Figure 14-12225. CORTEX8_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-36957. CORTEX8_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.10.2.2.648 CORTEX8_CFG_1_TAREG Register

1 CORTEX8_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

This register contains the address to write to or read from.

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Table 14-36958. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F04h**

Figure 14-12226. CORTEX8_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-36960. CORTEX8_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.10.2.2.649 CORTEX8_CFG_1_DRWREG Register

1 CORTEX8_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-36961. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F0Ch**

Figure 14-12227. CORTEX8_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-36963. CORTEX8_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.10.2.2.650 CORTEX8_CFG_1_BD0REG Register

1 CORTEX8_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36964. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F10h**

Figure 14-12228. CORTEX8_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-36966. CORTEX8_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.651 CORTEX8_CFG_1_BD1REG Register

1 CORTEX8_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-36967. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F14h**

Figure 14-12229. CORTEX8_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-36969. CORTEX8_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.652 CORTEX8_CFG_1_BD2REG Register

1 CORTEX8_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36970. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F18h**

Figure 14-12230. CORTEX8_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-36972. CORTEX8_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.653 CORTEX8_CFG_1_BD3REG Register

1 CORTEX8_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-36973. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2F1Ch**

Figure 14-12231. CORTEX8_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-36975. CORTEX8_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.10.2.2.654 CORTEX8_CFG_1_ROM_REGISTER Register

1 CORTEX8_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-36976. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2FF8h**

Figure 14-12232. CORTEX8_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-36978. CORTEX8_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.10.2.2.655 CORTEX8_CFG_1_ID_REGISTER Register

1 CORTEX8_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-36979. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 4000 2FFCh**

Figure 14-12233. CORTEX8_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-36981. CORTEX8_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.10.2.2.656 ROM_TABLE_1_1_ROM_ENTRY0 Register

1 ROM_TABLE_1_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

rom table entry 0

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Table 14-36982. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0000h**

Figure 14-12234. ROM_TABLE_1_1_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36984. ROM_TABLE_1_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.657 ROM_TABLE_1_1_ROM_ENTRY1 Register

1 ROM_TABLE_1_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

rom table entry 1

Return to Summary Table

Table 14-36985. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0004h**

Figure 14-12235. ROM_TABLE_1_1_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36987. ROM_TABLE_1_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.658 ROM_TABLE_1_1_ROM_ENTRY2 Register

1 ROM_TABLE_1_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

rom table entry 2

Return to Summary Table

Table 14-36988. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0008h**

Figure 14-12236. ROM_TABLE_1_1_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">3h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-36990. ROM_TABLE_1_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.659 ROM_TABLE_1_1_ROM_ENTRY3 Register

1 ROM_TABLE_1_1_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

rom table entry 3

Return to Summary Table

Table 14-36991. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 000Ch**

Figure 14-12237. ROM_TABLE_1_1_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36993. ROM_TABLE_1_1_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.660 ROM_TABLE_1_1_ROM_ENTRY4 Register

1 ROM_TABLE_1_1_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

rom table entry 4

Return to Summary Table

Table 14-36994. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0010h**

Figure 14-12238. ROM_TABLE_1_1_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
5h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36996. ROM_TABLE_1_1_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.661 ROM_TABLE_1_1_ROM_ENTRY5 Register

1 ROM_TABLE_1_1_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

rom table entry 5

Return to Summary Table

Table 14-36997. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0014h**

Figure 14-12239. ROM_TABLE_1_1_ROM_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-36999. ROM_TABLE_1_1_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.10.2.2.662 ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register

1 ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

compute cluster rom table entry 0

Return to Summary Table

Table 14-37000. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0018h**

Figure 14-12240. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1000h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37002. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.663 ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register

1 ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

compute cluster rom table entry 1

Return to Summary Table

Table 14-37003. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 001Ch**

Figure 14-12241. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1400h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37005. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.664 ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register

1 ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

compute cluster rom table entry 2

Return to Summary Table

Table 14-37006. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0020h**

Figure 14-12242. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1800h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1800h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1800h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37008. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.665 ROM_TABLE_1_1_DEBUG_CELL0 Register

1 ROM_TABLE_1_1_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

debug cell rom table entry 0

Return to Summary Table

Table 14-37009. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0024h

Figure 14-12243. ROM_TABLE_1_1_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37011. ROM_TABLE_1_1_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.666 ROM_TABLE_1_1_DEBUG_CELL1 Register

1 ROM_TABLE_1_1_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

debug cell rom table entry 1

Return to Summary Table

Table 14-37012. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0028h**

Figure 14-12244. ROM_TABLE_1_1_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37014. ROM_TABLE_1_1_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.667 ROM_TABLE_1_1_DEBUG_CELL2 Register

1 ROM_TABLE_1_1_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

debug cell rom table entry 2

Return to Summary Table

Table 14-37015. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 002Ch**

Figure 14-12245. ROM_TABLE_1_1_DEBUG_CELL2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37017. ROM_TABLE_1_1_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.668 ROM_TABLE_1_1_DEBUG_CELL3 Register

1 ROM_TABLE_1_1_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

debug cell rom table entry 3

Return to Summary Table

Table 14-37018. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0030h**

Figure 14-12246. ROM_TABLE_1_1_DEBUG_CELL3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C30h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C30h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37020. ROM_TABLE_1_1_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.669 ROM_TABLE_1_1_DEBUG_CELL4 Register

1 ROM_TABLE_1_1_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

debug cell rom table entry 4

Return to Summary Table

Table 14-37021. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0034h**

Figure 14-12247. ROM_TABLE_1_1_DEBUG_CELL4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C40h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C40h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C40h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37023. ROM_TABLE_1_1_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.670 ROM_TABLE_1_1_DEBUG_CELL5 Register

1 ROM_TABLE_1_1_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

debug cell rom table entry 5

Return to Summary Table

Table 14-37024. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0038h**

Figure 14-12248. ROM_TABLE_1_1_DEBUG_CELL5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C50h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C50h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C50h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37026. ROM_TABLE_1_1_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.671 ROM_TABLE_1_1_DEBUG_CELL6 Register

1 ROM_TABLE_1_1_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

debug cell rom table entry 6

Return to Summary Table

Table 14-37027. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 003Ch**

Figure 14-12249. ROM_TABLE_1_1_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37029. ROM_TABLE_1_1_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.672 ROM_TABLE_1_1_DEBUG_CELL7 Register

1 ROM_TABLE_1_1_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

debug cell rom table entry 7

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Table 14-37030. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0040h**

Figure 14-12250. ROM_TABLE_1_1_DEBUG_CELL7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37032. ROM_TABLE_1_1_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.673 ROM_TABLE_1_1_DEBUG_CELL8 Register

1 ROM_TABLE_1_1_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

debug cell rom table entry 8

Return to Summary Table

Table 14-37033. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0044h**

Figure 14-12251. ROM_TABLE_1_1_DEBUG_CELL8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C80h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C80h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C80h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37035. ROM_TABLE_1_1_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.674 ROM_TABLE_1_1_DEBUG_CELL9 Register

1 ROM_TABLE_1_1_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

debug cell rom table entry 9

Return to Summary Table

Table 14-37036. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0048h**

Figure 14-12252. ROM_TABLE_1_1_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37038. ROM_TABLE_1_1_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.675 ROM_TABLE_1_1_DEBUG_CELL10 Register

1 ROM_TABLE_1_1_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

debug cell rom table entry 10

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Table 14-37039. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 004Ch**

Figure 14-12253. ROM_TABLE_1_1_DEBUG_CELL10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-37041. ROM_TABLE_1_1_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.676 ROM_TABLE_1_1_DEBUG_CELL11 Register

1 ROM_TABLE_1_1_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

debug cell rom table entry 11

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Table 14-37042. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0050h**

Figure 14-12254. ROM_TABLE_1_1_DEBUG_CELL11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CB0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CB0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CB0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-37044. ROM_TABLE_1_1_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.677 ROM_TABLE_1_1_EXTCSCOMP0 Register

1 ROM_TABLE_1_1_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

external coresight componenet rom table entry 0

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Table 14-37045. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0050h**

Figure 14-12255. ROM_TABLE_1_1_EXTCSCOMP0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37047. ROM_TABLE_1_1_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.678 ROM_TABLE_1_1_EXTCSCOMP1 Register

1 ROM_TABLE_1_1_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

external coresight componenet rom table entry 1

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Table 14-37048. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0054h**

Figure 14-12256. ROM_TABLE_1_1_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D10h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37050. ROM_TABLE_1_1_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.679 ROM_TABLE_1_1_EXTCSCOMP2 Register

1 ROM_TABLE_1_1_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

external coresight componenet rom table entry 2

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Table 14-37051. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0058h**

Figure 14-12257. ROM_TABLE_1_1_EXTCSCOMP2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D20h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D20h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37053. ROM_TABLE_1_1_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.680 ROM_TABLE_1_1_EXTCSCOMP3 Register

1 ROM_TABLE_1_1_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

external coresight componenet rom table entry 3

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Table 14-37054. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 005Ch**

Figure 14-12258. ROM_TABLE_1_1_EXTCSCOMP3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D30h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D30h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37056. ROM_TABLE_1_1_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.681 ROM_TABLE_1_1_EXTCSCOMP4 Register

1 ROM_TABLE_1_1_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

external coresight componenet rom table entry 4

Return to Summary Table

Table 14-37057. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0060h**

Figure 14-12259. ROM_TABLE_1_1_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D40h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37059. ROM_TABLE_1_1_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.682 ROM_TABLE_1_1_EXTCSCOMP5 Register

1 ROM_TABLE_1_1_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

external coresight componenet rom table entry 5

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Table 14-37060. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0064h**

Figure 14-12260. ROM_TABLE_1_1_EXTCSCOMP5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D50h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D50h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D50h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37062. ROM_TABLE_1_1_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.683 ROM_TABLE_1_1_EXTCSCOMP6 Register

1 ROM_TABLE_1_1_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

external coresight componenet rom table entry 6

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Table 14-37063. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0068h**

Figure 14-12261. ROM_TABLE_1_1_EXTCSCOMP6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D60h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D60h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D60h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37065. ROM_TABLE_1_1_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.684 ROM_TABLE_1_1_EXTCSCOMP7 Register

1 ROM_TABLE_1_1_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

external coresight componenet rom table entry 7

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Table 14-37066. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 006Ch**

Figure 14-12262. ROM_TABLE_1_1_EXTCSCOMP7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37068. ROM_TABLE_1_1_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.685 ROM_TABLE_1_1_EXTCSCOMP8 Register

1 ROM_TABLE_1_1_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

external coresight componenet rom table entry 8

Return to Summary Table

Table 14-37069. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0070h**

Figure 14-12263. ROM_TABLE_1_1_EXTCSCOMP8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D80h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D80h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D80h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37071. ROM_TABLE_1_1_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.686 ROM_TABLE_1_1_EXTCSCOMP9 Register

1 ROM_TABLE_1_1_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

external coresight componenet rom table entry 9

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Table 14-37072. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0074h**

Figure 14-12264. ROM_TABLE_1_1_EXTCSCOMP9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D90h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D90h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37074. ROM_TABLE_1_1_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.687 ROM_TABLE_1_1_EXTCSCOMP10 Register

1 ROM_TABLE_1_1_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

external coresight componenet rom table entry 10

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Table 14-37075. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 0078h**

Figure 14-12265. ROM_TABLE_1_1_EXTCSCOMP10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DA0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1DA0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1DA0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37077. ROM_TABLE_1_1_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.688 ROM_TABLE_1_1_EXTCSCOMP11 Register

1 ROM_TABLE_1_1_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

external coresight componenet rom table entry 11

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Table 14-37078. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 007Ch**

Figure 14-12266. ROM_TABLE_1_1_EXTCSCOMP11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DB0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1DB0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1DB0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-37080. ROM_TABLE_1_1_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.10.2.2.689 CSCTI_CTICONTROL Register

1 CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register.

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Table 14-37081. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1000h**

Figure 14-12267. CSCTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
R							R/W
0h							0h

Table 14-37083. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	GLBEN	R/W	0h	Enables or disables the Embedded Cross Trigger, 1=enabled

14.10.2.2.690 CSCTI_CTIINTACK Register

1 CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Interrupt Acknowledge Register.

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Table 14-37084. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1010h**

Figure 14-12268. CSCTI_CTIINTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37086. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INTACK	R/W	0h	Acknowledges the corresponding CTITRIGOUT output Write 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW There is one bit of the register for each CTITRIGOUT output

14.10.2.2.691 CSCTI_CTIAPPSET Register

1 CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register.

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Table 14-37087. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1014h**

Figure 14-12269. CSCTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
R				R/W			
0h				0h			

Table 14-37089. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPSET	R/W	0h	The CTI Application Trigger Set Register is read/write A write to this register causes a channel event to be raised, corresponding to the bit written to

14.10.2.2.692 CSCTI_CTIAPPCLR Register

1 CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register.

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Table 14-37090. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1018h**

Figure 14-12270. CSCTI_CTIAPPCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPCLR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37092. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPCLR	R/W	0h	The CTI Application Trigger Clear Register is write-only A write to this register causes a channel event to be cleared, corresponding to the bit written to

14.10.2.2.693 CSCTI_CTIAPPPULSE Register

1 CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Trigger Pulse Register.

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Table 14-37093. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 101Ch**

Figure 14-12271. CSCTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPPULSE			
R				R/W			
0h				0h			

Table 14-37095. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPPULSE	R/W	0h	The CTI Application Pulse Register is write-only A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to This register clears itself immediately

14.10.2.2.694 CSCTI_CTIINEN0 Register

1 CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 0

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Table 14-37096. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1020h**

Figure 14-12272. CSCTI_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-37098. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.695 CSCTI_CTIINEN1 Register

1 CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 1

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Table 14-37099. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1024h

Figure 14-12273. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	TRIGINEN		
R				NONE	R/W		
0h				0h	0h		

Table 14-37101. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.696 CSCTI_CTIINEN2 Register

1 CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 2

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Table 14-37102. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1028h**

Figure 14-12274. CSCTI_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37104. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.697 CSCTI_CTIINEN3 Register

1 CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 3

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Table 14-37105. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 102Ch**

Figure 14-12275. CSCTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-37107. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.698 CSCTI_CTIINEN4 Register

1 CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 4

Return to Summary Table

Table 14-37108. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1030h**

Figure 14-12276. CSCTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-37110. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.699 CSCTI_CTIINEN5 Register

1 CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 5

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Table 14-37111. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1034h**

Figure 14-12277. CSCTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-37113. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.700 CSCTI_CTIINEN6 Register

1 CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 6

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Table 14-37114. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1038h**

Figure 14-12278. CSCTI_CTIINEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37116. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.701 CSCTI_CTIINEN7 Register

1 CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 7

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Table 14-37117. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 103Ch**

Figure 14-12279. CSCTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-37119. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.10.2.2.702 CSCTI_CTIOUTEN0 Register

1 CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Channel to Trigger Enable Register 0

Return to Summary Table

Table 14-37120. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A0h**

Figure 14-12280. CSCTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37122. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.703 CSCTI_CTIOUTEN1 Register

1 CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Channel to Trigger Enable Register 1

Return to Summary Table

Table 14-37123. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A4h**

Figure 14-12281. CSCTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37125. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.704 CSCTI_CTIOUTEN2 Register

1 CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Channel to Trigger Enable Register 2

Return to Summary Table

Table 14-37126. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10A8h**

Figure 14-12282. CSCTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37128. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.705 CSCTI_CTIOUTEN3 Register

1 CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Channel to Trigger Enable Register 3

Return to Summary Table

Table 14-37129. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10ACh**

Figure 14-12283. CSCTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37131. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.706 CSCTI_CTIOUTEN4 Register

1 CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Channel to Trigger Enable Register 4

Return to Summary Table

Table 14-37132. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B0h

Figure 14-12284. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37134. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.707 CSCTI_CTIOUTEN5 Register

1 CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Channel to Trigger Enable Register 5

Return to Summary Table

Table 14-37135. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10B4h**

Figure 14-12285. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37137. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.708 CSCTI_CTIOUTEN6 Register

1 CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Channel to Trigger Enable Register 6

Return to Summary Table

Table 14-37138. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B8h

Figure 14-12286. CSCTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37140. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.709 CSCTI_CTIOUTEN7 Register

1 CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Channel to Trigger Enable Register 7

Return to Summary Table

Table 14-37141. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 10BCh**

Figure 14-12287. CSCTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-37143. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.10.2.2.710 CSCTI_CTITRIGINSTATUS Register

1 CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

Return to Summary Table

Table 14-37144. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1130h**

Figure 14-12288. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-37146. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGINSTATUS	R	0h	Shows the status of the CTITRIGIN inputs: 1=CTITRIGIN is active, 0=CTITRIGIN is inactive

14.10.2.2.711 CSCTI_CTITRIGOUTSTATUS Register

1 CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

Return to Summary Table

Table 14-37147. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1134h**

Figure 14-12289. CSCTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGOUTSTATUS							
R							
0h							

Table 14-37149. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the CTITRIGOUT outputs: 1=CTITRIGOUT is active, 0=CTITRIGOUT is inactive

14.10.2.2.712 CSCTI_CTICHINSTATUS Register

1 CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

Return to Summary Table

Table 14-37150. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1138h

Figure 14-12290. CSCTI_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CHINSTATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37152. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHINSTATUS	R	0h	Shows the status of the CTICHIN inputs: 1=CTICHIN is active, 0=CTICHIN is inactive

14.10.2.2.713 CSCTI_CTICHOUTSTATUS Register

1 CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-37153. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 113Ch**

Figure 14-12291. CSCTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CHOUTSTATUS			
R				R			
0h				0h			

Table 14-37155. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHOUTSTATUS	R	0h	Shows the status of the CTICHOUT outputs: 1=CTICHOUT is active, 0=CTICHOUT is inactive

14.10.2.2.714 CSCTI_CTIGATE Register

1 CSCTI_CTIGATE Register (Offset = 140h) [reset = 0h]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs.

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Table 14-37156. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1140h**

Figure 14-12292. CSCTI_CTIGATE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTIGATEEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37158. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTIGATEEN	R	0h	Gate enable for the four channels [1 per bit]

14.10.2.2.715 CSCTI_ASICCTL Register

1 CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Allows external multiplexing of the trigger signals

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Table 14-37159. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1144h**

Figure 14-12293. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-37161. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]

14.10.2.2.716 CSCTI_ITCHINACK Register

1 CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

Integration and Test register

Return to Summary Table

Table 14-37162. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EDCh**

Figure 14-12294. CSCTI_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
R				R/W			
0h				0h			

Table 14-37164. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHINACK	R/W	0h	Sets the value of the CTCHINACK outputs

14.10.2.2.717 CSCTI_ITTRIGINACK Register

1 CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

ITTRIGINACK Register

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Table 14-37165. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE0h**

Figure 14-12295. CSCTI_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-37167. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGINACK	R/W	0h	Sets the value of the CTTRIGINACK outputs

14.10.2.2.718 CSCTI_ITCHOUT Register

1 CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

ITCHOUT Register

Return to Summary Table

Table 14-37168. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE4h**

Figure 14-12296. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
R				R/W			
0h				0h			

Table 14-37170. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHOUT	R/W	0h	Sets the value of the CTCHOUT outputs

14.10.2.2.719 CSCTI_ITTRIGOUT Register

1 CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

ITTRIGOUT Register

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Table 14-37171. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EE8h**

Figure 14-12297. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-37173. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUT	R/W	0h	Sets the value of the CTTRIGOUT outputs

14.10.2.2.720 CSCTI_ITCHOUTACK Register

1 CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

ITCHOUTACK Register

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Table 14-37174. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EECh**

Figure 14-12298. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTCHOUTACK							
R/W							
0h							

Table 14-37176. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTCHOUTACK	R/W	0h	Sets the value of the CTCHOUTACK outputs

14.10.2.2.721 CSCTI_ITTRIGOUTACK Register

1 CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

ITTRIGOUTACK Register

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Table 14-37177. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF0h**

Figure 14-12299. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-37179. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUTACK	R	0h	Reads the value of the CTTRIGOUTACK inputs

14.10.2.2.722 CSCTI_ITCHIN Register

1 CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

ITCHIN Register

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Table 14-37180. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF4h**

Figure 14-12300. CSCTI_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
R				R			
0h				0h			

Table 14-37182. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHIN	R	0h	Reads the value of the CTCHIN inputs

14.10.2.2.723 CSCTI_ITTRIGIN Register

1 CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

ITTRIGIN Register

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Table 14-37183. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1EF8h**

Figure 14-12301. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-37185. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGIN	R	0h	Reads the value of the CTTRIGIN inputs

14.10.2.2.724 CSCTI_ITCTRL Register

1 CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

ITCTRL Register

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Table 14-37186. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1F00h**

Figure 14-12302. CSCTI_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							ITEN
R							R/W
0h							0h

Table 14-37188. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	ITEN	R/W	0h	Integration Test control enable

14.10.2.2.725 CSCTI_CLAIMSET Register

1 CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-37189. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FA0h**

Figure 14-12303. CSCTI_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-37191. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.726 CSCTI_CLAIMCLR Register

1 CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-37192. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FA4h**

Figure 14-12304. CSCTI_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37194. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.727 CSCTI_LOCKACCESS Register

1 CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-37195. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FB0h**

Figure 14-12305. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
LOCKACCESSREG							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKACCESSREG							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKACCESSREG							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKACCESSREG							
R/W							
0h							

Table 14-37197. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKACCESSREG	R/W	0h	Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers If paddrdbg31 is high, this is ignored

14.10.2.2.728 CSCTI_LOCKSTATUS Register

1 CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-37198. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FB4h**

Figure 14-12306. CSCTI_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-37200. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.729 CSCTI_AUTHSTATUS Register

1 CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-37201. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FB8h**

Figure 14-12307. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-37203. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.730 CSCTI_DEVID Register

1 CSCTI_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-37204. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FC8h**

Figure 14-12308. CSCTI_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUM_ECT_CHANNELS			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
NUM_ECT_TRIGGERS							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED7_5			IMPLEMENTATION_DEFINED				
R			R				
0h			0h				

Table 14-37206. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved, returns 0
19:16	NUM_ECT_CHANNELS	R	0h	Number of ECT Channels available
15:8	NUM_ECT_TRIGGERS	R	0h	Number of ECT trigger available
7:5	RESERVED7_5	R	0h	Reserved, returns 0
4:0	IMPLEMENTATION_DEFINED	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Outputs using ASICCTL Defailt value of 0 indicates no multiplexing present

14.10.2.2.731 CSCTI_DEVTYPE Register

1 CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-37207. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FCCh**

Figure 14-12309. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-37209. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.10.2.2.732 CSCTI_PERIPHID4 Register

1 CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-37210. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FD0h**

Figure 14-12310. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-37212. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.733 CSCTI_PERIPHID0 Register

1 CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-37213. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FE0h**

Figure 14-12311. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-37215. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.734 CSCTI_PERIPHID1 Register

1 CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-37216. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FE4h**

Figure 14-12312. CSCTI_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-37218. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.735 CSCTI_PERIPHID2 Register

1 CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-37219. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE8h

Figure 14-12313. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-37221. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.736 CSCTI_PERIPHID3 Register

1 CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-37222. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FECh**

Figure 14-12314. CSCTI_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-37224. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.737 CSCTI_COMPONID0 Register

1 CSCTI_COMPONID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-37225. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FF0h**

Figure 14-12315. CSCTI_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-37227. CSCTI_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.738 CSCTI_COMPONID1 Register

1 CSCTI_COMPONID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-37228. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FF4h**

Figure 14-12316. CSCTI_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-37230. CSCTI_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.739 CSCTI_COMPONID2 Register

1 CSCTI_COMPONID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-37231. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FF8h**

Figure 14-12317. CSCTI_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-37233. CSCTI_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.740 CSCTI_COMPONID3 Register

1 CSCTI_COMPONID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

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Table 14-37234. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 1FFCh**

Figure 14-12318. CSCTI_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-37236. CSCTI_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.741 DRM_CFG_1_PERIPH_ID Register

1 DRM_CFG_1_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

This register is used to determine what the functionality of this peripheral is.

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Table 14-37237. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2000h**

Figure 14-12319. DRM_CFG_1_PERIPH_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		283h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
283h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLREV					MAJOR		
R					R		
Ch					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-37239. DRM_CFG_1_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.10.2.2.742 DRM_CFG_1_VERSION Register

1 DRM_CFG_1_VERSION Register (Offset = 4h) [reset = 0h]

This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-37240. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2004h**

Figure 14-12320. DRM_CFG_1_VERSION Name Register

31	30	29	28	27	26	25	24
MAJOR_VERSION							
R							
0h							
23	22	21	20	19	18	17	16
MAJOR_VERSION							
R							
0h							
15	14	13	12	11	10	9	8
MINOR_VERSION							
R							
0h							
7	6	5	4	3	2	1	0
MINOR_VERSION							
R							
0h							

Table 14-37242. DRM_CFG_1_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.10.2.2.743 DRM_CFG_1_CAPABILITY Register

1 DRM_CFG_1_CAPABILITY Register (Offset = 8h) [reset = 0h]

This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-37243. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2008h**

Figure 14-12321. DRM_CFG_1_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		NUM_SUSPENDS					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
NUM_PERIPHERALS							
R							
0h							

Table 14-37245. DRM_CFG_1_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.10.2.2.744 DRM_CFG_1_TRACE_CTRL Register

1 DRM_CFG_1_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-37246. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 200Ch**

Figure 14-12322. DRM_CFG_1_TRACE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CENTER_SAMPLING</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-37248. DRM_CFG_1_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.10.2.2.745 DRM_CFG_1_VBUSM_CTRL Register

1 DRM_CFG_1_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-37249. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2010h**

Figure 14-12323. DRM_CFG_1_VBUSM_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DOM_INPUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">DOM_INPUT</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VBUSM_PRIV</td><td>VBUSM_SECURE</td><td>VBUSM_DEBUG</td><td colspan="2">CTL_PRIV</td><td>CTL_SECURE</td><td>EMUDBG</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-37251. DRM_CFG_1_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.10.2.2.746 DRM_CFG_1_DAP_TIMEOUT Register

1 DRM_CFG_1_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-37252. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2014h**

Figure 14-12324. DRM_CFG_1_DAP_TIMEOUT Name Register

31	30	29	28	27	26	25	24
DAP_TIMEOUT_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DAP_TIMEOUT_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DAP_TIMEOUT_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DAP_TIMEOUT_REGISTER							
R/W							
0h							

Table 14-37254. DRM_CFG_1_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.10.2.2.747 DRM_CFG_1_CONFIG Register

1 DRM_CFG_1_CONFIG Register (Offset = 18h) [reset = 0h]

This register adds softreset capability to the suspend module.

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Table 14-37255. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2018h

Figure 14-12325. DRM_CFG_1_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFTRESET
R							R/W
0h							0h

Table 14-37257. DRM_CFG_1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.10.2.2.748 DRM_CFG_1_EMUTRIGEN Register

1 DRM_CFG_1_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

This register is used to enable EMU triggers.

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Table 14-37258. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 201Ch**

Figure 14-12326. DRM_CFG_1_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-37260. DRM_CFG_1_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.10.2.2.749 DRM_CFG_1_BINVALLO Register

1 DRM_CFG_1_BINVALLO Register (Offset = 20h) [reset = 0h]

Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-37261. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2020h**

Figure 14-12327. DRM_CFG_1_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-37263. DRM_CFG_1_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.10.2.2.750 DRM_CFG_1_BINVALHI Register

1 DRM_CFG_1_BINVALHI Register (Offset = 24h) [reset = 0h]

Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-37264. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2024h**

Figure 14-12328. DRM_CFG_1_BINVALHI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">BINTIMEHI</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BINTIMEHI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37266. DRM_CFG_1_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.10.2.2.751 DRM_CFG_1_SUSPEND_REG0 Register

1 DRM_CFG_1_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-37267. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2200h**

Figure 14-12329. DRM_CFG_1_SUSPEND_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>SELECT</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SELECT</td><td colspan="3">RESERVED0</td><td>SUSPEND_CTL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-37269. DRM_CFG_1_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.10.2.2.752 DRM_CFG_1_SUSPEND_REG1 Register

1 DRM_CFG_1_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37270. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2204h**

Figure 14-12330. DRM_CFG_1_SUSPEND_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37272. DRM_CFG_1_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.753 DRM_CFG_1_SUSPEND_REG2 Register

1 DRM_CFG_1_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37273. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2208h**

Figure 14-12331. DRM_CFG_1_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_2							
R/W							
0h							

Table 14-37275. DRM_CFG_1_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.754 DRM_CFG_1_SUSPEND_REG3 Register

1 DRM_CFG_1_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37276. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 220Ch**

Figure 14-12332. DRM_CFG_1_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-37278. DRM_CFG_1_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.755 DRM_CFG_1_SUSPEND_REG4 Register

1 DRM_CFG_1_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37279. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2210h**

Figure 14-12333. DRM_CFG_1_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-37281. DRM_CFG_1_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.756 DRM_CFG_1_SUSPEND_REG5 Register

1 DRM_CFG_1_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37282. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2214h**

Figure 14-12334. DRM_CFG_1_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-37284. DRM_CFG_1_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.757 DRM_CFG_1_SUSPEND_REG6 Register

1 DRM_CFG_1_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37285. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2218h**

Figure 14-12335. DRM_CFG_1_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-37287. DRM_CFG_1_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.758 DRM_CFG_1_SUSPEND_REG7 Register

1 DRM_CFG_1_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37288. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 221Ch**

Figure 14-12336. DRM_CFG_1_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-37290. DRM_CFG_1_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.759 DRM_CFG_1_SUSPEND_REG8 Register

1 DRM_CFG_1_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37291. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2220h**

Figure 14-12337. DRM_CFG_1_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-37293. DRM_CFG_1_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.760 DRM_CFG_1_SUSPEND_REG9 Register

1 DRM_CFG_1_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37294. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2224h**

Figure 14-12338. DRM_CFG_1_SUSPEND_REG9 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_9							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUSPEND_REG_9							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SUSPEND_REG_9							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUSPEND_REG_9							
R/W							
0h							

Table 14-37296. DRM_CFG_1_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.761 DRM_CFG_1_SUSPEND_REG10 Register

1 DRM_CFG_1_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37297. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2228h**

Figure 14-12339. DRM_CFG_1_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-37299. DRM_CFG_1_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.762 DRM_CFG_1_SUSPEND_REG11 Register

1 DRM_CFG_1_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37300. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 222Ch**

Figure 14-12340. DRM_CFG_1_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-37302. DRM_CFG_1_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.763 DRM_CFG_1_SUSPEND_REG12 Register

1 DRM_CFG_1_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37303. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2230h**

Figure 14-12341. DRM_CFG_1_SUSPEND_REG12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37305. DRM_CFG_1_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.764 DRM_CFG_1_SUSPEND_REG13 Register

1 DRM_CFG_1_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37306. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2234h**

Figure 14-12342. DRM_CFG_1_SUSPEND_REG13 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_13							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_13							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_13							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_13							
R/W							
0h							

Table 14-37308. DRM_CFG_1_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.765 DRM_CFG_1_SUSPEND_REG14 Register

1 DRM_CFG_1_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37309. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2238h**

Figure 14-12343. DRM_CFG_1_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-37311. DRM_CFG_1_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.766 DRM_CFG_1_SUSPEND_REG15 Register

1 DRM_CFG_1_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37312. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 223Ch**

Figure 14-12344. DRM_CFG_1_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-37314. DRM_CFG_1_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.767 DRM_CFG_1_SUSPEND_REG16 Register

1 DRM_CFG_1_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37315. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2240h**

Figure 14-12345. DRM_CFG_1_SUSPEND_REG16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37317. DRM_CFG_1_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.768 DRM_CFG_1_SUSPEND_REG17 Register

1 DRM_CFG_1_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37318. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2244h**

Figure 14-12346. DRM_CFG_1_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-37320. DRM_CFG_1_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.769 DRM_CFG_1_SUSPEND_REG18 Register

1 DRM_CFG_1_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37321. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2248h**

Figure 14-12347. DRM_CFG_1_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-37323. DRM_CFG_1_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.770 DRM_CFG_1_SUSPEND_REG19 Register

1 DRM_CFG_1_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37324. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 224Ch**

Figure 14-12348. DRM_CFG_1_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-37326. DRM_CFG_1_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.771 DRM_CFG_1_SUSPEND_REG20 Register

1 DRM_CFG_1_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37327. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2250h**

Figure 14-12349. DRM_CFG_1_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_20							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_20							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_20							
R/W							
0h							

Table 14-37329. DRM_CFG_1_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.772 DRM_CFG_1_SUSPEND_REG21 Register

1 DRM_CFG_1_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37330. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2254h**

Figure 14-12350. DRM_CFG_1_SUSPEND_REG21 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_21							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_21							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_21							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_21							
R/W							
0h							

Table 14-37332. DRM_CFG_1_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.773 DRM_CFG_1_SUSPEND_REG22 Register

1 DRM_CFG_1_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37333. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2258h**

Figure 14-12351. DRM_CFG_1_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-37335. DRM_CFG_1_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.774 DRM_CFG_1_SUSPEND_REG23 Register

1 DRM_CFG_1_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37336. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 225Ch**

Figure 14-12352. DRM_CFG_1_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-37338. DRM_CFG_1_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.775 DRM_CFG_1_SUSPEND_REG24 Register

1 DRM_CFG_1_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37339. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2260h**

Figure 14-12353. DRM_CFG_1_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-37341. DRM_CFG_1_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.776 DRM_CFG_1_SUSPEND_REG25 Register

1 DRM_CFG_1_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37342. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2264h**

Figure 14-12354. DRM_CFG_1_SUSPEND_REG25 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_25							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_25							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_25							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_25							
R/W							
0h							

Table 14-37344. DRM_CFG_1_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.777 DRM_CFG_1_SUSPEND_REG26 Register

1 DRM_CFG_1_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37345. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2268h**

Figure 14-12355. DRM_CFG_1_SUSPEND_REG26 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_26</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_26</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_26</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_26</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37347. DRM_CFG_1_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.778 DRM_CFG_1_SUSPEND_REG27 Register

1 DRM_CFG_1_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37348. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 226Ch**

Figure 14-12356. DRM_CFG_1_SUSPEND_REG27 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_27							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_27							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_27							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_27							
R/W							
0h							

Table 14-37350. DRM_CFG_1_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.779 DRM_CFG_1_SUSPEND_REG28 Register

1 DRM_CFG_1_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

Return to Summary Table

Table 14-37351. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2270h**

Figure 14-12357. DRM_CFG_1_SUSPEND_REG28 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_28							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_28							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_28							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_28							
R/W							
0h							

Table 14-37353. DRM_CFG_1_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.780 DRM_CFG_1_SUSPEND_REG29 Register

1 DRM_CFG_1_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

Return to Summary Table

Table 14-37354. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2274h**

Figure 14-12358. DRM_CFG_1_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-37356. DRM_CFG_1_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.781 DRM_CFG_1_SUSPEND_REG30 Register

1 DRM_CFG_1_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37357. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 2278h**

Figure 14-12359. DRM_CFG_1_SUSPEND_REG30 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_30							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_30							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_30							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_30							
R/W							
0h							

Table 14-37359. DRM_CFG_1_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.782 DRM_CFG_1_SUSPEND_REG31 Register

1 DRM_CFG_1_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-37360. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 227Ch**

Figure 14-12360. DRM_CFG_1_SUSPEND_REG31 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_31							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_31							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_31							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_31							
R/W							
0h							

Table 14-37362. DRM_CFG_1_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.10.2.2.783 CSTPIU_CFG_1_SUPPORTSIZE Register

1 CSTPIU_CFG_1_SUPPORTSIZE Register (Offset = 0h) [reset = 0h]

This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-37363. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4000h**

Figure 14-12361. CSTPIU_CFG_1_SUPPORTSIZE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUPPORTSIZEREG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUPPORTSIZEREG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUPPORTSIZEREG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUPPORTSIZEREG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37365. CSTPIU_CFG_1_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	0h	This register indicates how many trace pins are available for export One pin per bit, right justified

14.10.2.2.784 CSTPIU_CFG_1_CURPORTSIZE Register

1 CSTPIU_CFG_1_CURPORTSIZE Register (Offset = 4h) [reset = 0h]

The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-37366. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4004h**

Figure 14-12362. CSTPIU_CFG_1_CURPORTSIZE Name Register

31	30	29	28	27	26	25	24
CURRENTPORTSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
CURRENTPORTSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
CURRENTPORTSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
CURRENTPORTSIZE							
R/W							
0h							

Table 14-37368. CSTPIU_CFG_1_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	0h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.10.2.2.785 CSTPIU_CFG_1_TRIGMODEREG Register

1 CSTPIU_CFG_1_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-37369. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4100h**

Figure 14-12363. CSTPIU_CFG_1_TRIGMODEREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>TRGRUN</td><td>TRIGGERED</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED2</td><td>TCOUNT8</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td colspan="5">MUILTPLIERS</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-37371. CSTPIU_CFG_1_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running A trigger has occurred but the counter is not at zero
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported Each bit is a mpy value

14.10.2.2.786 CSTPIU_CFG_1_TRIGCTRREG Register

1 CSTPIU_CFG_1_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-37372. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4104h**

Figure 14-12364. CSTPIU_CFG_1_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGCOUNT							
R/W							
0h							

Table 14-37374. CSTPIU_CFG_1_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted

14.10.2.2.787 CSTPIU_CFG_1_TRIGMPYREG Register

1 CSTPIU_CFG_1_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-37375. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4108h**

Figure 14-12365. CSTPIU_CFG_1_TRIGMPYREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			MULTIPLIER				
R			R/W				
0h			0h				

Table 14-37377. CSTPIU_CFG_1_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K

14.10.2.2.788 CSTPIU_CFG_1_SUPTESTPAT Register

1 CSTPIU_CFG_1_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-37378. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4200h**

Figure 14-12366. CSTPIU_CFG_1_SUPTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						MODE	
R						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				PATTERN			
R				R			
0h				0h			

Table 14-37380. CSTPIU_CFG_1_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.10.2.2.789 CSTPIU_CFG_1_CURTESTPAT Register

1 CSTPIU_CFG_1_CURTESTPAT Register (Offset = 204h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-37381. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4204h**

Figure 14-12367. CSTPIU_CFG_1_CURTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						MODE	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				RESERVED	PATTERN		
R				NONE	R/W		
0h				0h	0h		

Table 14-37383. CSTPIU_CFG_1_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.10.2.2.790 CSTPIU_CFG_1_TESTPATCNT Register

1 CSTPIU_CFG_1_TESTPATCNT Register (Offset = 208h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-37384. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4208h**

Figure 14-12368. CSTPIU_CFG_1_TESTPATCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PATTERNCOUNT							
R/W							
0h							

Table 14-37386. CSTPIU_CFG_1_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.10.2.2.791 CSTPIU_CFG_1_FORMFLUSHSTAT Register

1 CSTPIU_CFG_1_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-37387. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4300h**

Figure 14-12369. CSTPIU_CFG_1_FORMFLUSHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCPRESENT	FTSTOPPED	FLINPROG
R					R	R	R
0h					0h	0h	0h

Table 14-37389. CSTPIU_CFG_1_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped The formatter has received a stop request signal and all trace data and post-amble has been output
0	FLINPROG	R	0h	Flush In Progress This is an indication of the current state of AFVALIDS

14.10.2.2.792 CSTPIU_CFG_1_FORMFLUSHCTL Register

1 CSTPIU_CFG_1_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

This register controls the generation of stop, trigger, and flush events.

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Table 14-37390. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4304h**

Figure 14-12370. CSTPIU_CFG_1_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-37392. CSTPIU_CFG_1_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS]
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system It is cleared when this flush has been serviced
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting Do not embed Triggers into the formatted stream

14.10.2.2.793 CSTPIU_CFG_1_FORMSYNCCTR Register

1 CSTPIU_CFG_1_FORMSYNCCTR Register (Offset = 308h) [reset = 0h]

This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-37393. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4308h**

Figure 14-12371. CSTPIU_CFG_1_FORMSYNCCTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				CYCCOUNT			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CYCCOUNT							
R/W							
0h							

Table 14-37395. CSTPIU_CFG_1_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	0h	12-bit counter value to indicate the number of complete frames between full sync packets

14.10.2.2.794 CSTPIU_CFG_1_EXTCTLIN Register

1 CSTPIU_CFG_1_EXTCTLIN Register (Offset = 400h) [reset = 0h]

This register inputs data from an external port (if used)

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Table 14-37396. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4400h**

Figure 14-12372. CSTPIU_CFG_1_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-37398. CSTPIU_CFG_1_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.10.2.2.795 CSTPIU_CFG_1_EXTCTLOUT Register

1 CSTPIU_CFG_1_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

This register is output to an external port (if used)

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Table 14-37399. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4404h**

Figure 14-12373. CSTPIU_CFG_1_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-37401. CSTPIU_CFG_1_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.10.2.2.796 CSTPIU_CFG_1_ITTRFLINACK Register

1 CSTPIU_CFG_1_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Integration Test Trigger In and Flush In Acknowledge.

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Table 14-37402. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EE4h**

Figure 14-12374. CSTPIU_CFG_1_ITTRFLINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ATID</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-37404. CSTPIU_CFG_1_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.10.2.2.797 CSTPIU_CFG_1_ITTRFLIN Register

1 CSTPIU_CFG_1_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Integration Test Trigger In and Flush In Register.

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Table 14-37405. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EE8h**

Figure 14-12375. CSTPIU_CFG_1_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
INTEGRATIONTRFLIN							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATIONTRFLIN							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATIONTRFLIN							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATIONTRFLIN							
R/W							
0h							

Table 14-37407. CSTPIU_CFG_1_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATIONTRFLIN	R/W	0h	

14.10.2.2.798 CSTPIU_CFG_1_ITATBDATA0 Register

1 CSTPIU_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test ATB Data Register 0

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Table 14-37408. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EECh**

Figure 14-12376. CSTPIU_CFG_1_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTEGRATION_TEST_ATB_REG							
R/W							
0h							

Table 14-37410. CSTPIU_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_REG	R/W	0h	

14.10.2.2.799 CSTPIU_CFG_1_ITATBCTR2 Register

1 CSTPIU_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test ATB Control Register 2.

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Table 14-37411. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EF0h**

Figure 14-12377. CSTPIU_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							

Table 14-37413. CSTPIU_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG2	R/W	0h	

14.10.2.2.800 CSTPIU_CFG_1_ITATBCTR1 Register

1 CSTPIU_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test ATB Control Register 1.

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Table 14-37414. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EF4h**

Figure 14-12378. CSTPIU_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							

Table 14-37416. CSTPIU_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG1	R/W	0h	

14.10.2.2.801 CSTPIU_CFG_1_ITATBCTR0 Register

1 CSTPIU_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test ATB Control Register 0

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Table 14-37417. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4EF8h**

Figure 14-12379. CSTPIU_CFG_1_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							

Table 14-37419. CSTPIU_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG0	R/W	0h	

14.10.2.2.802 CSTPIU_CFG_1_INTCTRL Register

1 CSTPIU_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-37420. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4F00h**

Figure 14-12380. CSTPIU_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-37422. CSTPIU_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.10.2.2.803 CSTPIU_CFG_1_CTSET Register

1 CSTPIU_CFG_1_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-37423. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FA0h**

Figure 14-12381. CSTPIU_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-37425. CSTPIU_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.804 CSTPIU_CFG_1_CTCLR Register

1 CSTPIU_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-37426. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FA4h**

Figure 14-12382. CSTPIU_CFG_1_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-37428. CSTPIU_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.805 CSTPIU_CFG_1_LAREG Register

1 CSTPIU_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-37429. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FB0h**

Figure 14-12383. CSTPIU_CFG_1_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-37431. CSTPIU_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.10.2.2.806 CSTPIU_CFG_1_LSREG Register

1 CSTPIU_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-37432. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FB4h**

Figure 14-12384. CSTPIU_CFG_1_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-37434. CSTPIU_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.807 CSTPIU_CFG_1_AUTHST Register

1 CSTPIU_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-37435. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FB8h**

Figure 14-12385. CSTPIU_CFG_1_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-37437. CSTPIU_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.808 CSTPIU_CFG_1_DEVID Register

1 CSTPIU_CFG_1_DEVID Register (Offset = FC8h) [reset = 0h]

This shows the characteristics of the TPIU

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Table 14-37438. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FC8h**

Figure 14-12386. CSTPIU_CFG_1_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				SWO_UART	SWO_MANCHESTER	TRACE_CLOCK_SUP	FIFO_SIZE
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
FIFO_SIZE		CLOCK_RELATIONSHIP	HIDDEN_MUXING				
R		R	R				
0h		0h	0h				

Table 14-37440. CSTPIU_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWO_UART	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported Defaul = 0
10	SWO_MANCHESTER	R	0h	Indicates Serial Wire Output [Manchester] is not supported Default = 0
9	TRACE_CLOCK_SUP	R	0h	Indicates trace clock + data is supported
8:6	FIFO_SIZE	R	0h	FIFO size in powers of 2 A value of 2 gives a FIFO size of 4 entries, 16 bytes Default is3'b010
5	CLOCK_RELATIONSHIP	R	0h	Indicates the relationship between ATCLK and TRACECLKIN 0x1 indicates asynchronous
4:0	HIDDEN_MUXING	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB Currently only 0x00 is supported, that is, no multiplexing present

14.10.2.2.809 CSTPIU_CFG_1_DEVTYPEID Register

1 CSTPIU_CFG_1_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-37441. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FCCh**

Figure 14-12387. CSTPIU_CFG_1_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-37443. CSTPIU_CFG_1_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.10.2.2.810 CSTPIU_CFG_1_PERID4 Register

1 CSTPIU_CFG_1_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-37444. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FD0h**

Figure 14-12388. CSTPIU_CFG_1_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-37446. CSTPIU_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.811 CSTPIU_CFG_1_PERID0 Register

1 CSTPIU_CFG_1_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-37447. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FE0h**

Figure 14-12389. CSTPIU_CFG_1_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-37449. CSTPIU_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.812 CSTPIU_CFG_1_PERID1 Register

1 CSTPIU_CFG_1_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-37450. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FE4h**

Figure 14-12390. CSTPIU_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-37452. CSTPIU_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.813 CSTPIU_CFG_1_PERID2 Register

1 CSTPIU_CFG_1_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-37453. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FE8h**

Figure 14-12391. CSTPIU_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-37455. CSTPIU_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.814 CSTPIU_CFG_1_PERID3 Register

1 CSTPIU_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-37456. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	**0007 6000 4FECh**

Figure 14-12392. CSTPIU_CFG_1_PERID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERPIH_ID3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37458. CSTPIU_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.815 CSTPIU_CFG_1_COMPID0 Register

1 CSTPIU_CFG_1_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-37459. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FF0h**

Figure 14-12393. CSTPIU_CFG_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-37461. CSTPIU_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.816 CSTPIU_CFG_1_COMPID1 Register

1 CSTPIU_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

Return to Summary Table

Table 14-37462. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FF4h**

Figure 14-12394. CSTPIU_CFG_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-37464. CSTPIU_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.817 CSTPIU_CFG_1_COMPID2 Register

1 CSTPIU_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

Return to Summary Table

Table 14-37465. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FF8h**

Figure 14-12395. CSTPIU_CFG_1_COMPID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37467. CSTPIU_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.818 CSTPIU_CFG_1_COMPID3 Register

1 CSTPIU_CFG_1_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

Return to Summary Table

Table 14-37468. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 4FFCh**

Figure 14-12396. CSTPIU_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-37470. CSTPIU_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.819 CTF_CFG_1_CSTFCTLREG Register

1 CTF_CFG_1_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

It enables the target ports and defines the hold time of the target ports.

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Table 14-37471. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5000h**

Figure 14-12397. CTF_CFG_1_CSTFCTLREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MINHOLDTIME</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SLVPORTEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37473. CTF_CFG_1_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel initiator port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.10.2.2.820 CTF_CFG_1_PRIORCTLREG Register

1 CTF_CFG_1_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-37474. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5004h**

Figure 14-12398. CTF_CFG_1_PRIORCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
PRIPORT7			PRIPORT6			PRIPORT5	
R/W			R/W			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
PRIPORT5	PRIPORT4			PRIPORT3			PRIPORT2
R/W	R/W			R/W			R/W
0h	0h			0h			0h
7	6	5	4	3	2	1	0
PRIPORT2		PRIPORT1			PRIPORT0		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-37476. CTF_CFG_1_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.10.2.2.821 CTF_CFG_1_ITATBDATA0 Register

1 CTF_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test Register.

Return to Summary Table

Table 14-37477. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EECh

Figure 14-12399. CTF_CFG_1_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			ATDATA31	ATDATA23	ATDATA15	ATDATA7	ATDATA0
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-37479. CTF_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.10.2.2.822 CTF_CFG_1_ITATBCTR2 Register

1 CTF_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test Control Register 2.

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Table 14-37480. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5EF0h**

Figure 14-12400. CTF_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-37482. CTF_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.10.2.2.823 CTF_CFG_1_ITATBCTR1 Register

1 CTF_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test Control Register 1.

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Table 14-37483. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EF4h

Figure 14-12401. CTF_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-37485. CTF_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.10.2.2.824 CTF_CFG_1_ITATBCTR0 Register

1 CTF_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test Control Register 0.

Return to Summary Table

Table 14-37486. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5EF8h**

Figure 14-12402. CTF_CFG_1_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1						ATBYTES	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						AFREADY	ATVALID
R						R/W	R/W
0h						0h	0h

Table 14-37488. CTF_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.10.2.2.825 CTF_CFG_1_INTCTRL Register

1 CTF_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-37489. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5F00h**

Figure 14-12403. CTF_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-37491. CTF_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.10.2.2.826 CTF_CFG_1_CTSET Register

1 CTF_CFG_1_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-37492. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FA0h**

Figure 14-12404. CTF_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-37494. CTF_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.10.2.2.827 CTF_CFG_1_CTCLR Register

1 CTF_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

Return to Summary Table

Table 14-37495. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FA4h**

Figure 14-12405. CTF_CFG_1_CTCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-37497. CTF_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.10.2.2.828 CTF_CFG_1_LAREG Register

1 CTF_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-37498. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FB0h**

Figure 14-12406. CTF_CFG_1_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-37500. CTF_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.10.2.2.829 CTF_CFG_1_LSREG Register

1 CTF_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-37501. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FB4h**

Figure 14-12407. CTF_CFG_1_LSREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">LOCK_STATUS</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-37503. CTF_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.10.2.2.830 CTF_CFG_1_AUTHST Register

1 CTF_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-37504. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FB8h**

Figure 14-12408. CTF_CFG_1_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-37506. CTF_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.10.2.2.831 CTF_CFG_1_DEVID Register

1 CTF_CFG_1_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-37507. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FC8h

Figure 14-12409. CTF_CFG_1_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-37509. CTF_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.10.2.2.832 CTF_CFG_1_DEVTYPEID Register

1 CTF_CFG_1_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-37510. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FCCh**

Figure 14-12410. CTF_CFG_1_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-37512. CTF_CFG_1_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.10.2.2.833 CTF_CFG_1_PERID4 Register

1 CTF_CFG_1_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

Return to Summary Table

Table 14-37513. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FD0h**

Figure 14-12411. CTF_CFG_1_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-37515. CTF_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.10.2.2.834 CTF_CFG_1_PERID5 Register

1 CTF_CFG_1_PERID5 Register (Offset = FD4h) [reset = 0h]

Peripheral ID5 Register

Return to Summary Table

Table 14-37516. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FD4h**

Figure 14-12412. CTF_CFG_1_PERID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID5							
R							
0h							

Table 14-37518. CTF_CFG_1_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.10.2.2.835 CTF_CFG_1_PERID6 Register

1 CTF_CFG_1_PERID6 Register (Offset = FD8h) [reset = 0h]

Peripheral ID6 Register

Return to Summary Table

Table 14-37519. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FD8h**

Figure 14-12413. CTF_CFG_1_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-37521. CTF_CFG_1_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.10.2.2.836 CTF_CFG_1_PERID7 Register

1 CTF_CFG_1_PERID7 Register (Offset = FDCh) [reset = 0h]

Peripheral ID7 Register

Return to Summary Table

Table 14-37522. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FDCh**

Figure 14-12414. CTF_CFG_1_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPH_ID7							
R							
0h							

Table 14-37524. CTF_CFG_1_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.10.2.2.837 CTF_CFG_1_PERID0 Register

1 CTF_CFG_1_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

Return to Summary Table

Table 14-37525. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FE0h**

Figure 14-12415. CTF_CFG_1_PERID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIPH_ID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37527. CTF_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.10.2.2.838 CTF_CFG_1_PERID1 Register

1 CTF_CFG_1_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

Return to Summary Table

Table 14-37528. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FE4h**

Figure 14-12416. CTF_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-37530. CTF_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.10.2.2.839 CTF_CFG_1_PERID2 Register

1 CTF_CFG_1_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

Return to Summary Table

Table 14-37531. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	**0007 6000 5FE8h**

Figure 14-12417. CTF_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-37533. CTF_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.10.2.2.840 CTF_CFG_1_PERID3 Register

1 CTF_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-37534. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FECh**

Figure 14-12418. CTF_CFG_1_PERID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERPIH_ID3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37536. CTF_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.10.2.2.841 CTF_CFG_1_COMPID0 Register

1 CTF_CFG_1_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

Return to Summary Table

Table 14-37537. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FF0h**

Figure 14-12419. CTF_CFG_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-37539. CTF_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.842 CTF_CFG_1_COMPID1 Register

1 CTF_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

Return to Summary Table

Table 14-37540. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FF4h**

Figure 14-12420. CTF_CFG_1_COMPID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-37542. CTF_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.843 CTF_CFG_1_COMPID2 Register

1 CTF_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

Return to Summary Table

Table 14-37543. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FF8h**

Figure 14-12421. CTF_CFG_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMP_ID2							
R							
0h							

Table 14-37545. CTF_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.10.2.2.844 CTF_CFG_1_COMPID3 Register

1 CTF_CFG_1_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

Return to Summary Table

Table 14-37546. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	**0007 6000 5FFCh**

Figure 14-12422. CTF_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-37548. CTF_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 4, 2024 to November 15, 2025 (from Revision (December 2024) to Revision A (November 2025)) **Page**

- Remove note about device family..12
- Update RAT..13
- Update MCU R5F ATCM/BTCM address..29
- Update RTC Unsupported Features..184
- Added "Two digital voltage domains" in section RTC Unsupported Features 184
- Added Content of Initialization Chapter..462
- Remove "_" from PADCONFIGx Register name..475
- Remove "_" from PADCONFIGx Register name..477
- Add information about errata affecting operation frequency..477
- Remove "_" from PADCONFIGx Register name..481
- Remove "_" from PADCONFIGx Register name..482
- Remove "_" from PADCONFIGx Register name..483
- Remove "_" from PADCONFIGx Register name..485
- Remove "_" from PADCONFIGx Register name..486
- Remove "_" from PADCONFIGx Register name..488
- Remove "_" from PADCONFIGx Register name..490
- Remove "_" from PADCONFIGx Register name..494
- Remove "_" from PADCONFIGx Register name..496
- Remove "_" from PADCONFIGx Register name..498
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- Update register names..537
- AVS Class-0 not supported. Removed from list of features..551
- Update register names..570
- Update register names..572
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- Update register names..579
- Update register names..582
- Update register names..583
- Update register names..585
- Update register names..587
- Update register names..588
- Update MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register name..612
- Update register name..612
- Update register names..615
- Add Interrupt Controller section. Remove Time Sync Support..732
- I2C: Genericize I2C Module image..1092
- I2C: Updated note under I2C Block Diagram to clarify the i variables..1100
- I2C: Updated note in I2C Clocking to clarify the i variables..1101
- I2C: Updated subsection reference to parent of the subsection 1109

- MCSPI: MCSPI Interface Signals in Controller Mode updated to a more generic image............................ 1122
- MCSPI: Update MCSPI Channels to show as CH(i) instead of CHi.. 1122
- SPI: Basic MCSPI Pins for Peripheral Mode table and diagrams updated to be nire generic 1123
- Add addition information to Polarity and Phase regarding data transfer..1125
- SPI: Update Global Initialization of Surrounding Modues to mention not all modules are applicable 1153
- Added RX, TX, CTS and RTS signals to main domain. 1171
- UART: changed description in *System Using RS-485 Communication* to better align with UART instance used in section's image.. 1172
- UART: Changed *IrDA Mode Interface Signals* image and paragraph to be more generic...........................1173
- UART: Made *CIR Mode Interface Signals* diagram and paragraph more generic....................................... 1181
- Update DLL and DLH Hex values associated with 160MHz and 192MHz Source Clock............................1208
- CPSW: Update interface mode registers to more generic name. 1239
- CPSW: Updated RMII clocking register to more generic name..1240
- CPSW: Updated CPSW CPTS CLKSEL to generic bit name... 1306
- CPSW: Change to generic CPTS_CLKSEL name.. 1308
- CPSW: updated to generic names for ENET1_CTRL and ENET2_CTRL.. 1336
- Fixed typo of SDIO version from 4.0 to 3.0.. 1498
- EPW: Updated instance counts and register names for Time-Base Clocks...1655
- GTC: Updated CLKSEL register name 1738
- RTC Chapter updated...1746
- Timers: Updated paragraph to clarify instance counts. Updated register reference to register name instead of register region...1763
- DCC: Update note and image to be generic...1787
- Update Pad Configuration Register Functional Description Table...6868
- Mark ISO_OVR as Reserved.. 6868
- Add Drive Strength Control options..6868

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